

Compal Confidential

Schematic Document

Cantiga + ICH9

2008 / 12 / 10 Rev:1.0

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	
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				Document Number	Rev
				LA-4841P	1.0
Date: Monday, December 15, 2008				Sheet	1 of 45

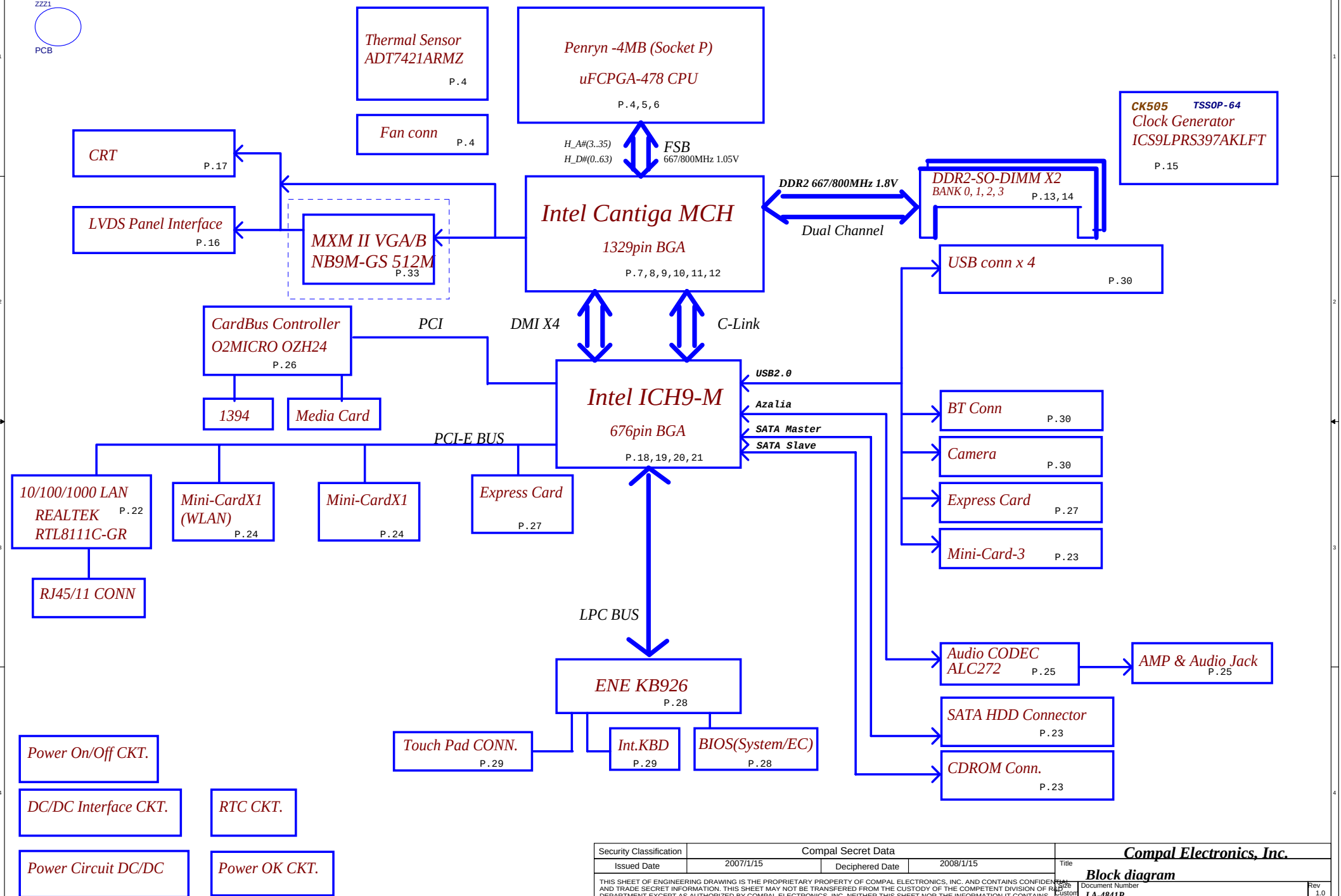
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File Name : LA-4841P

ZZZ1

PCB

MLK 14



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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Block diagram
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Voltage Rails O MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

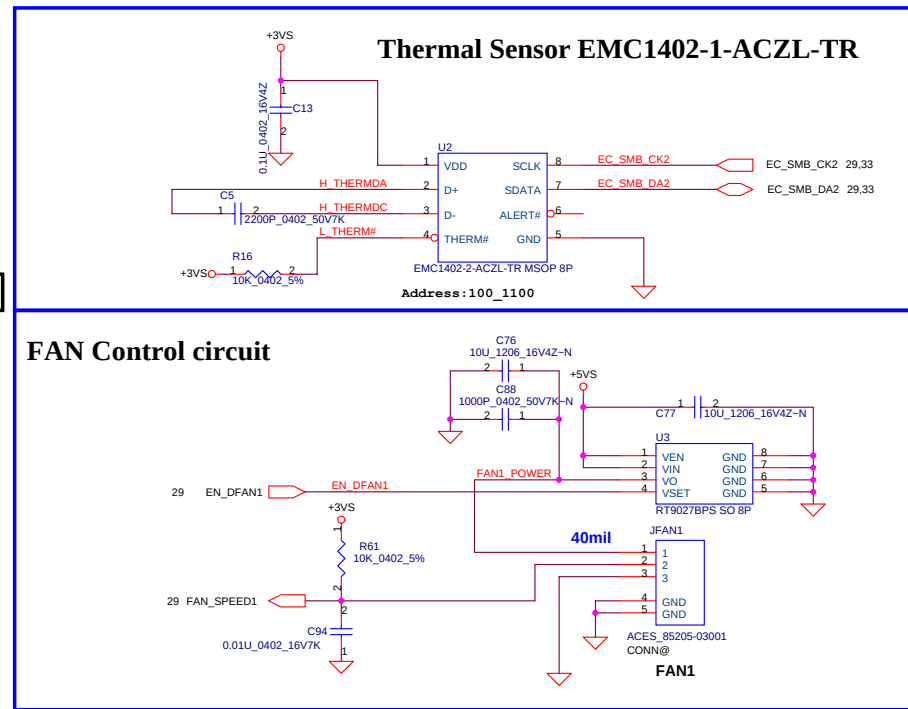
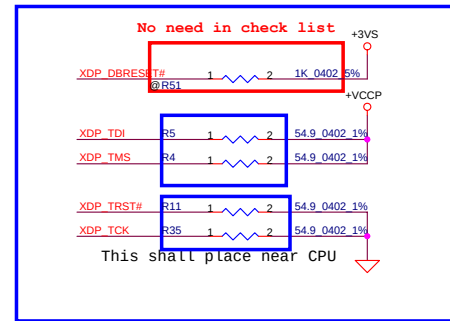
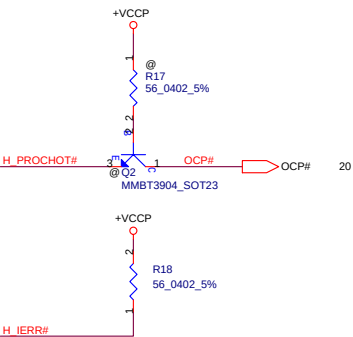
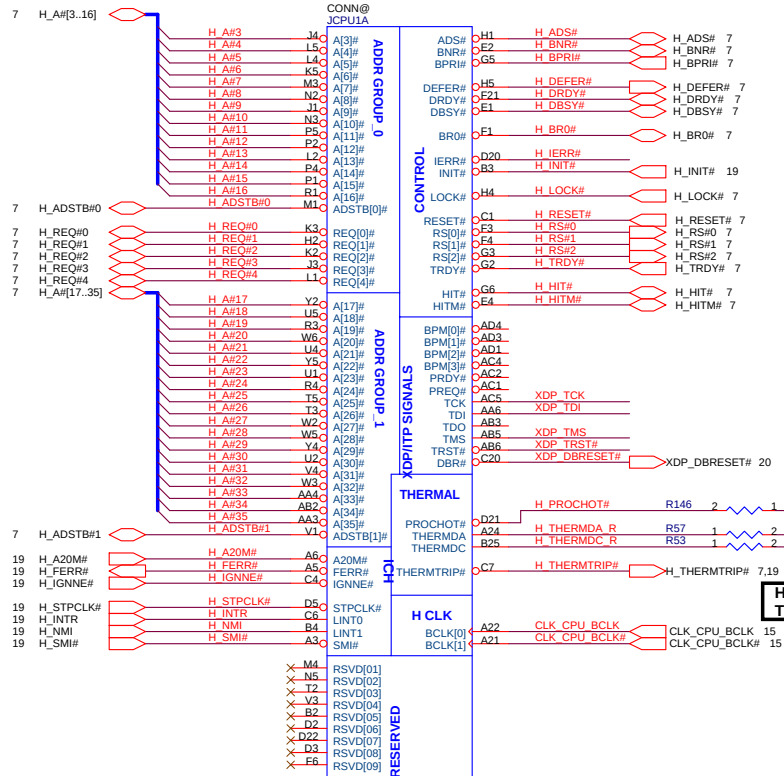
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

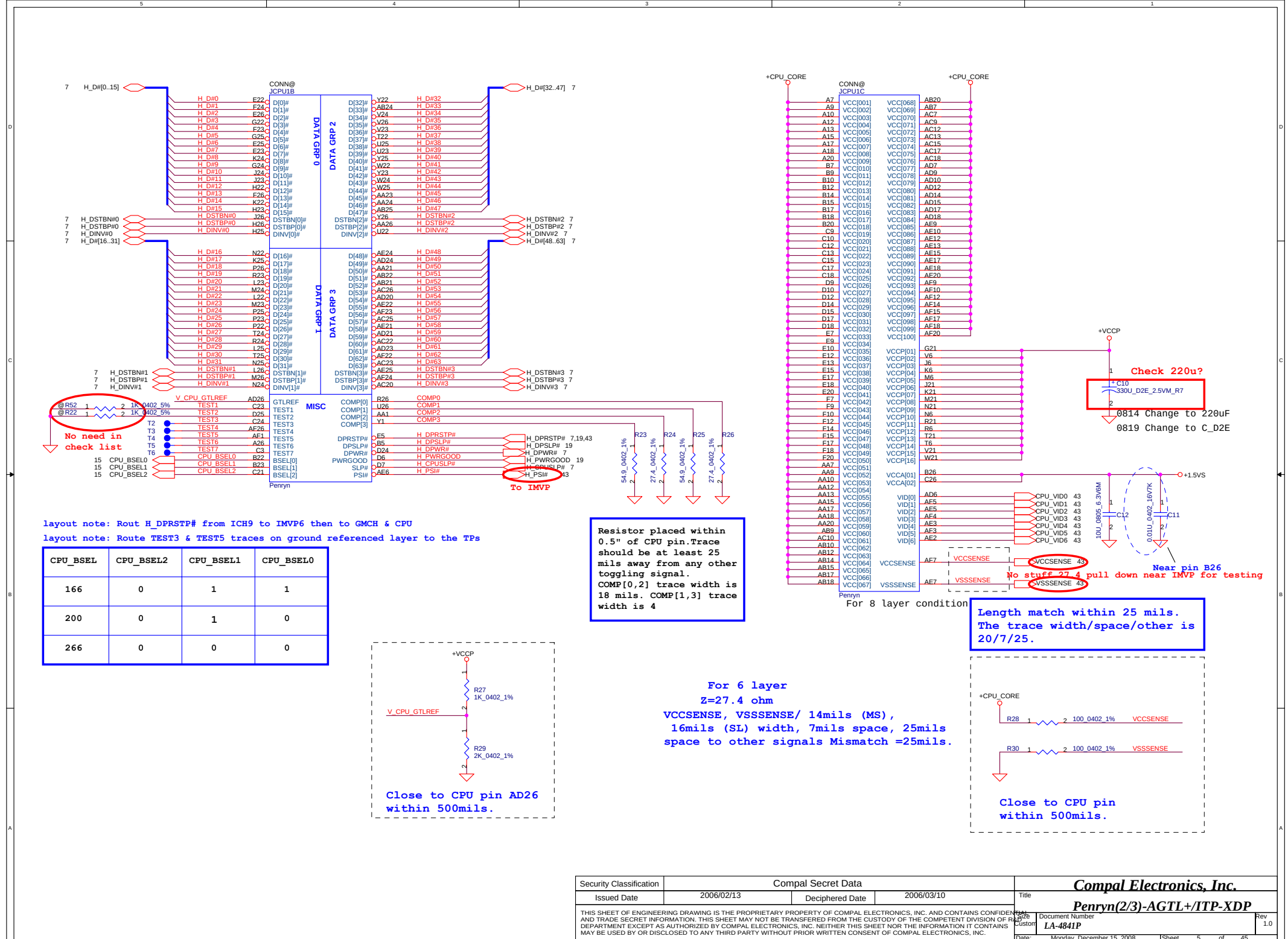
I2C / SMBUS ADDRESSING

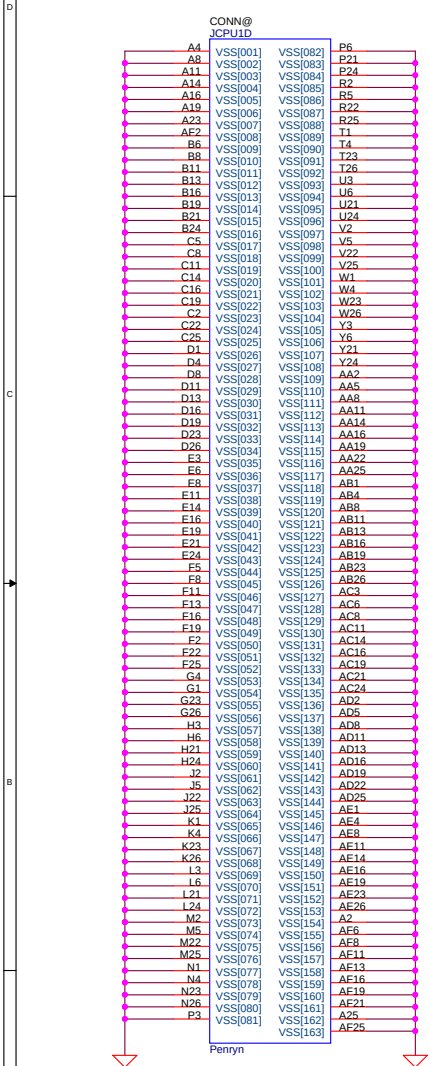
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

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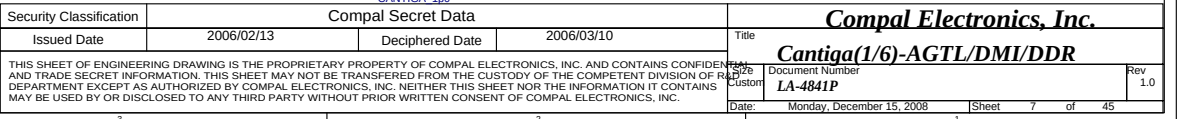


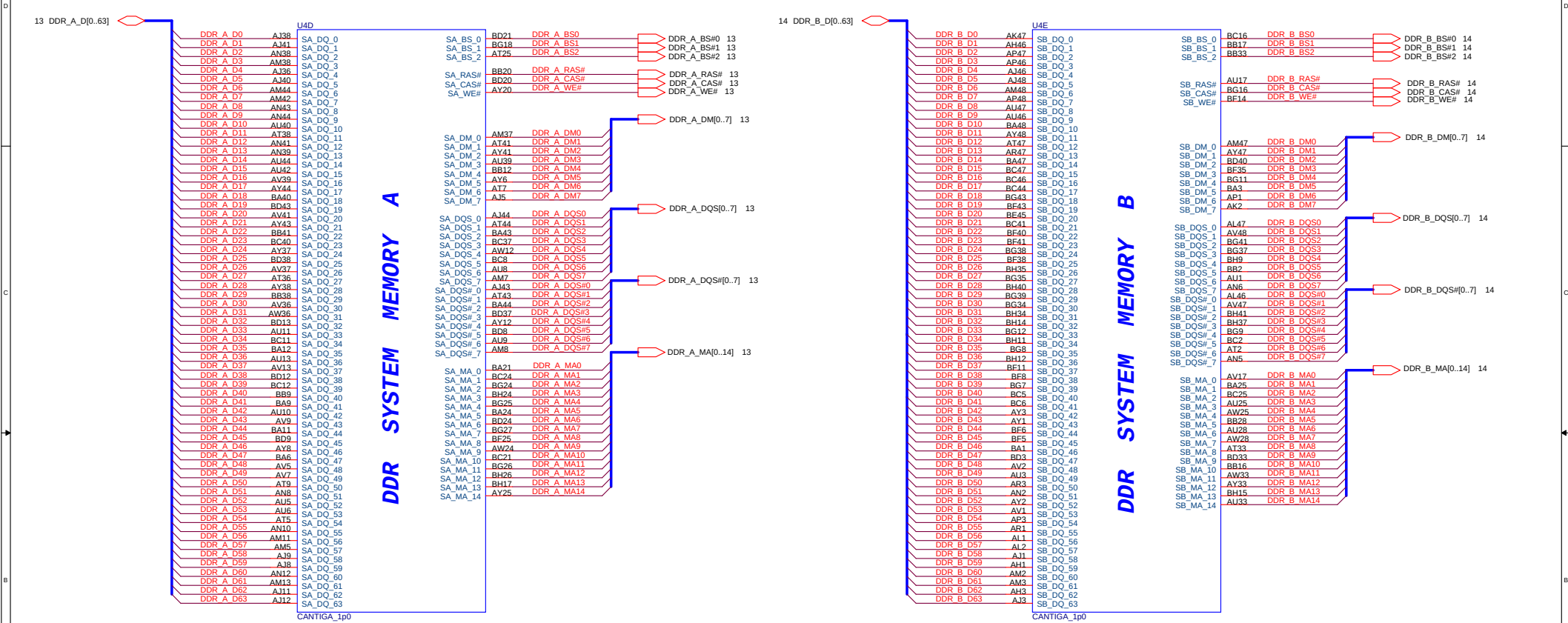
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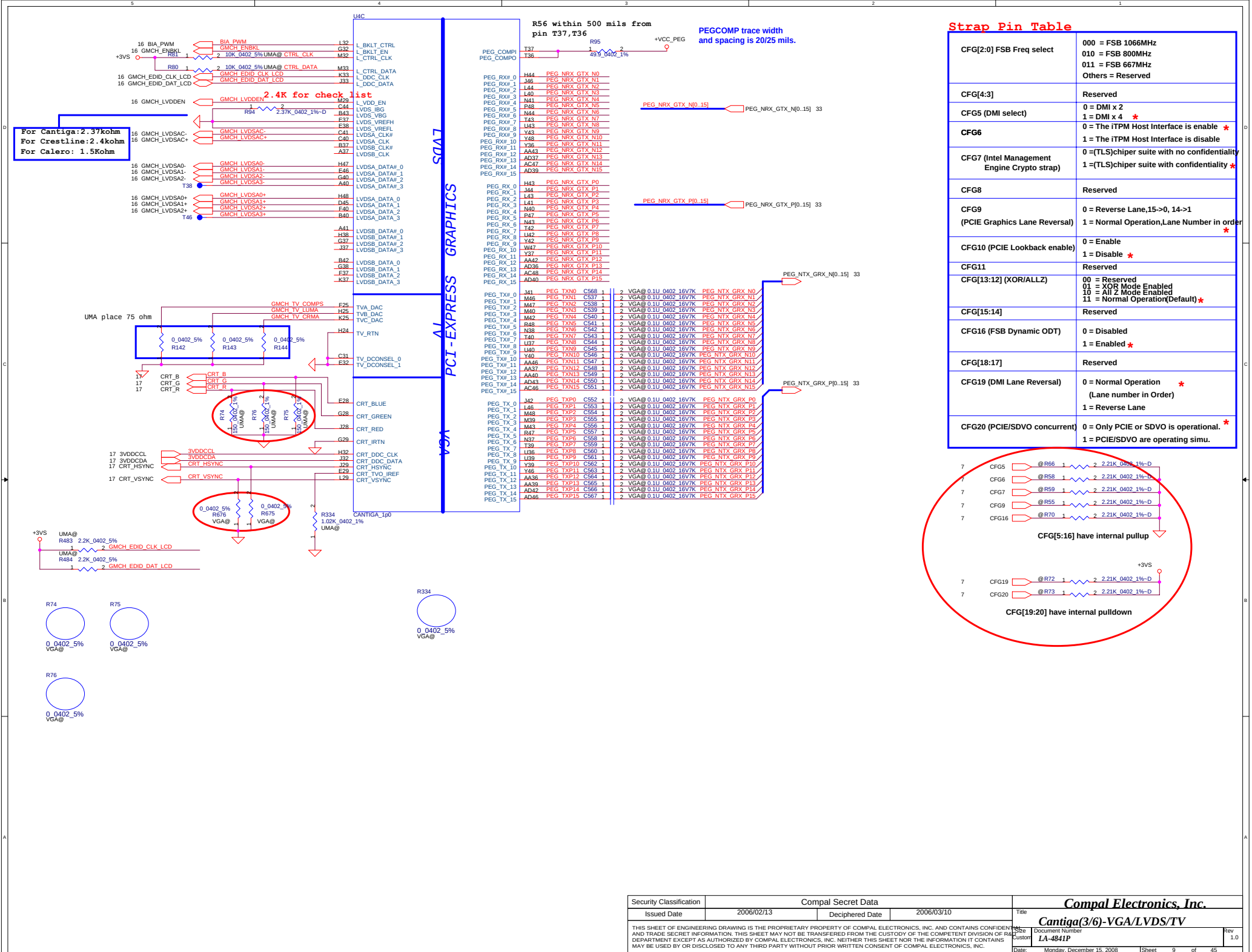




5	4	3	2	1
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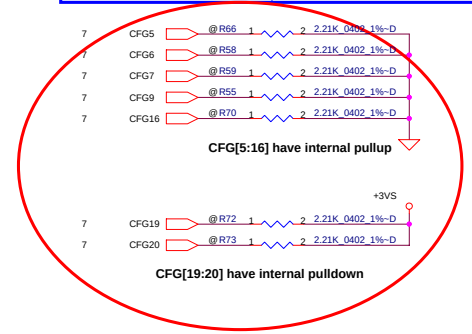


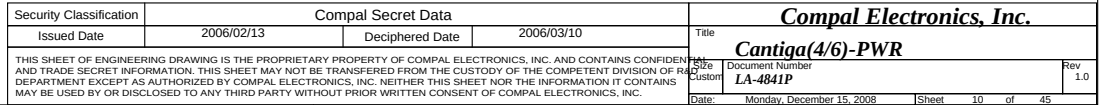


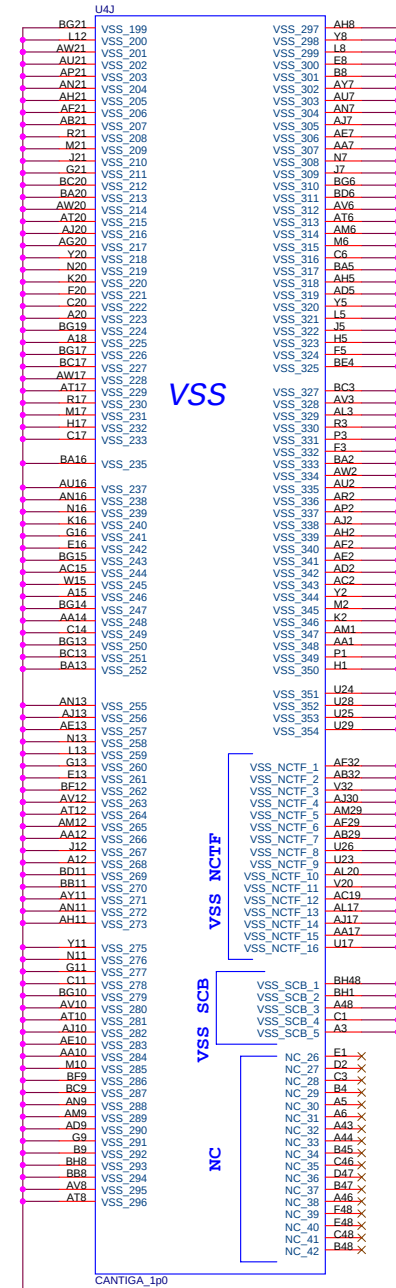
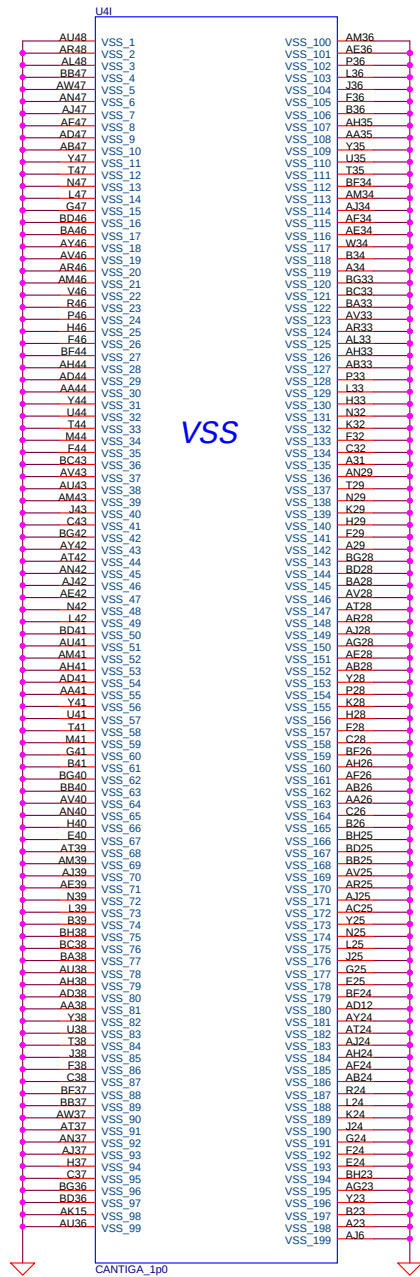


Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable * 1 = The ITPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation 1 = Reverse Lane *
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

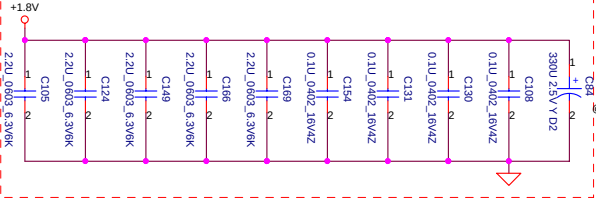




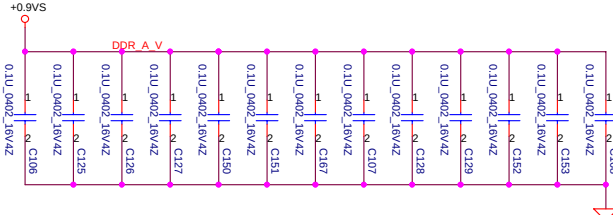


8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]

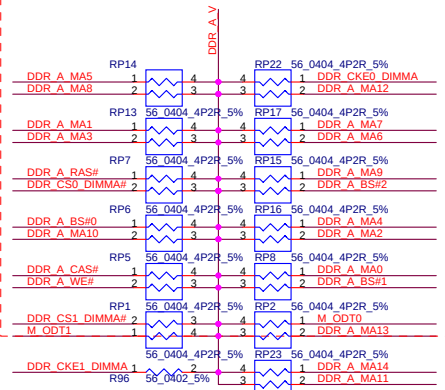
Layout Note:
Place near JDIM1



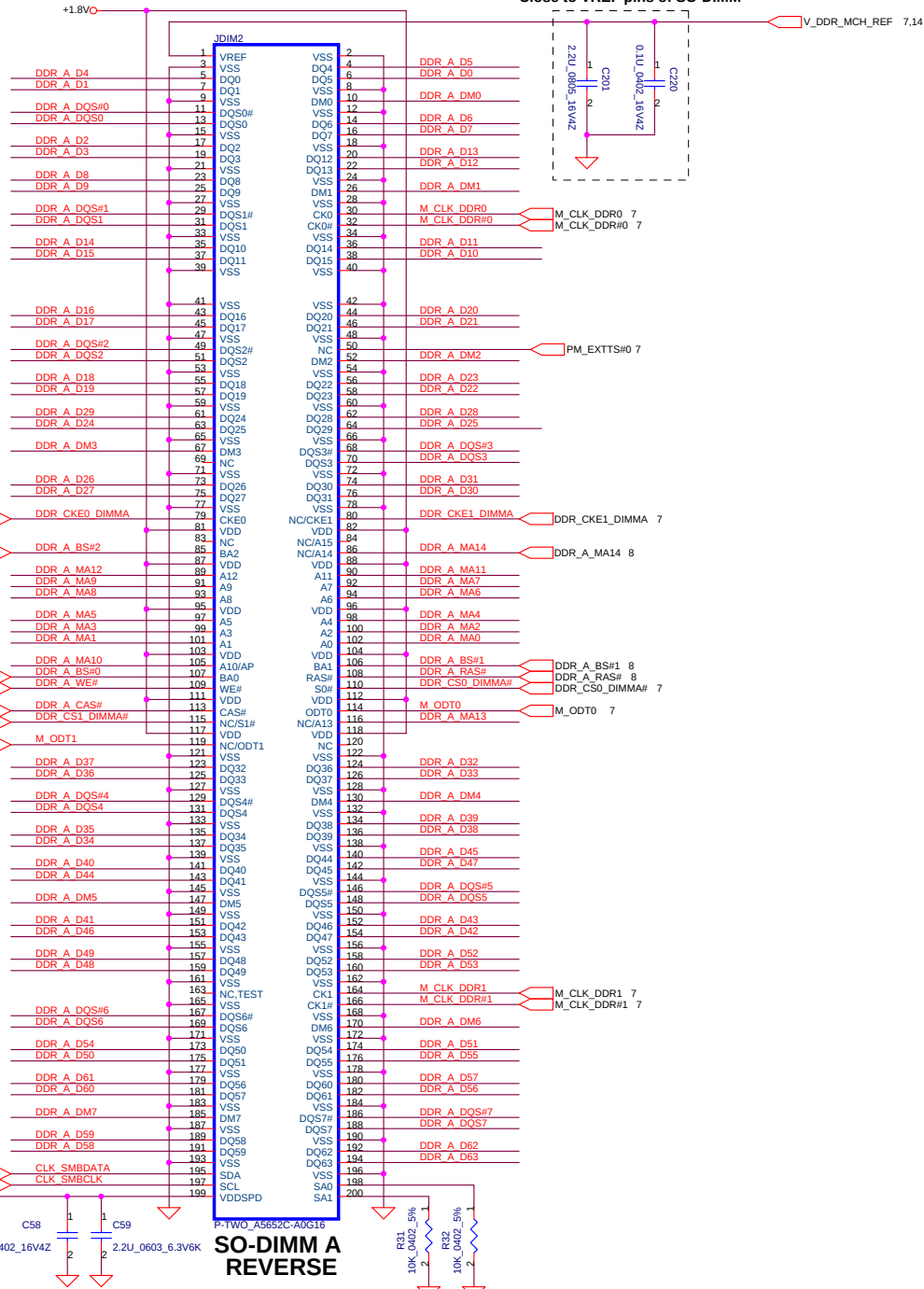
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V



Layout Note:
Place these resistor
closely JP41, all
trace length Max=1.5\"/>

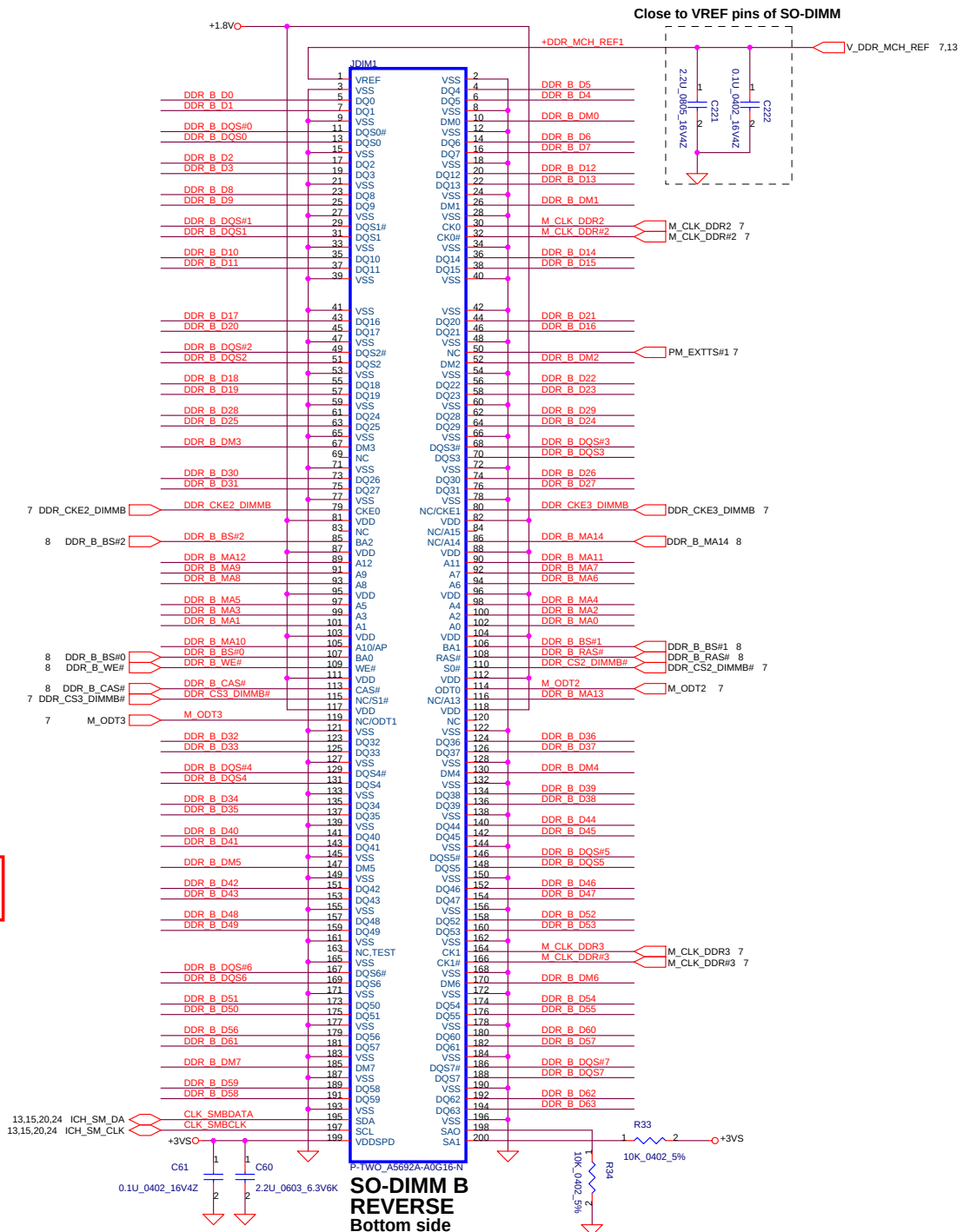
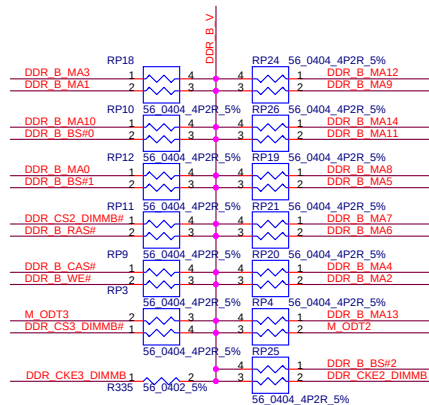


Layout Note:
Place these resistor
closely JP41, all
trace length Max=1.5\"/>



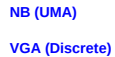
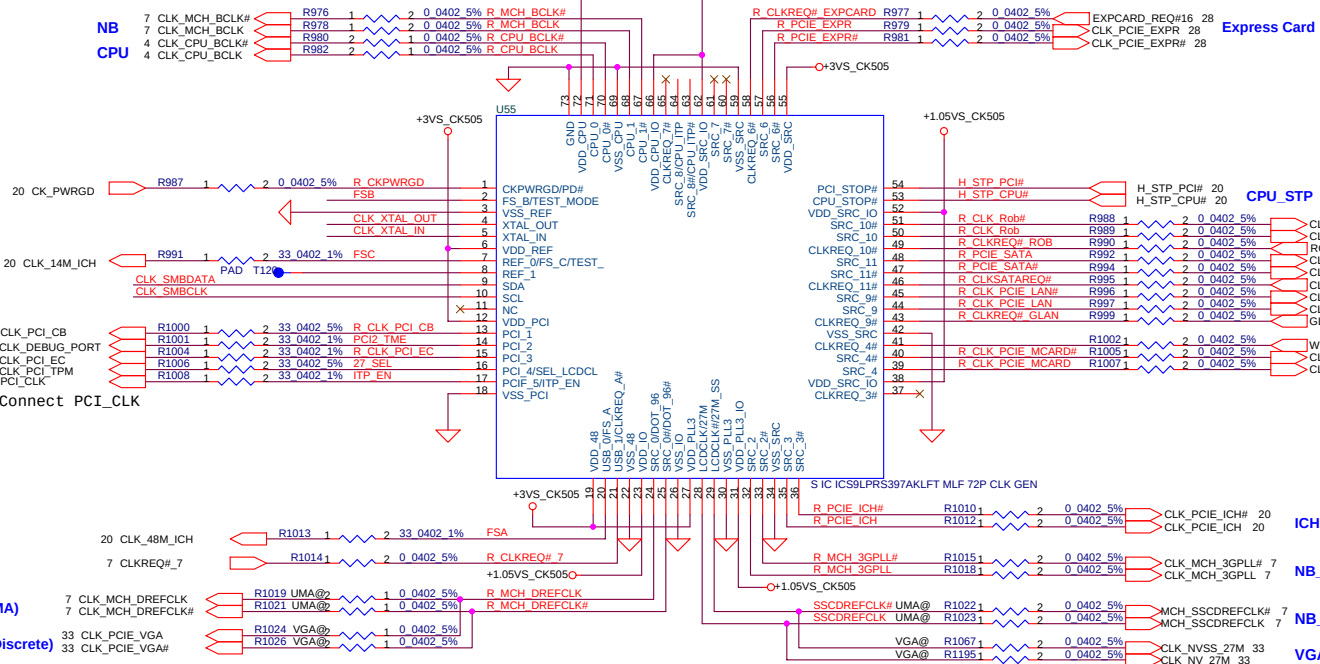
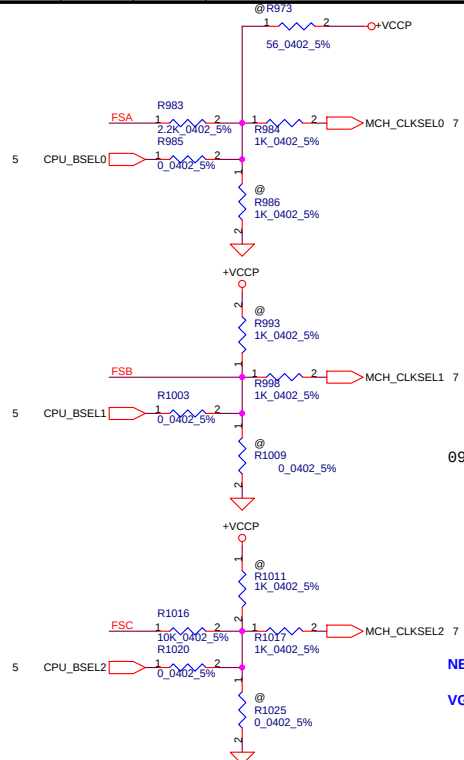
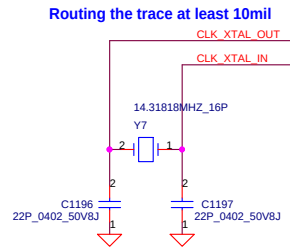
SO-DIMM A
REVERSE
Bottom side

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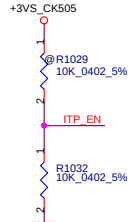
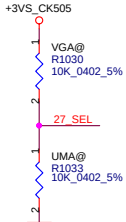
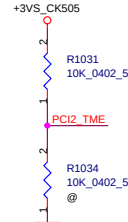


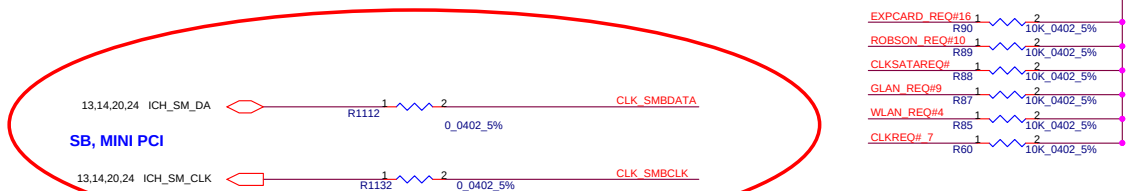
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



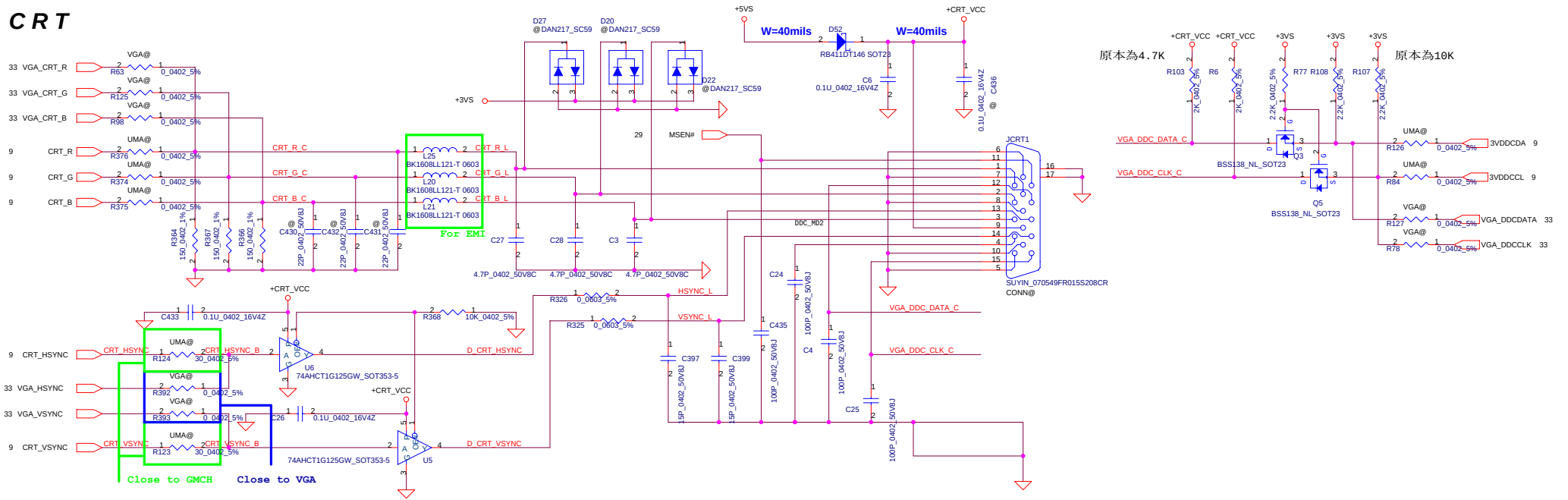
ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed

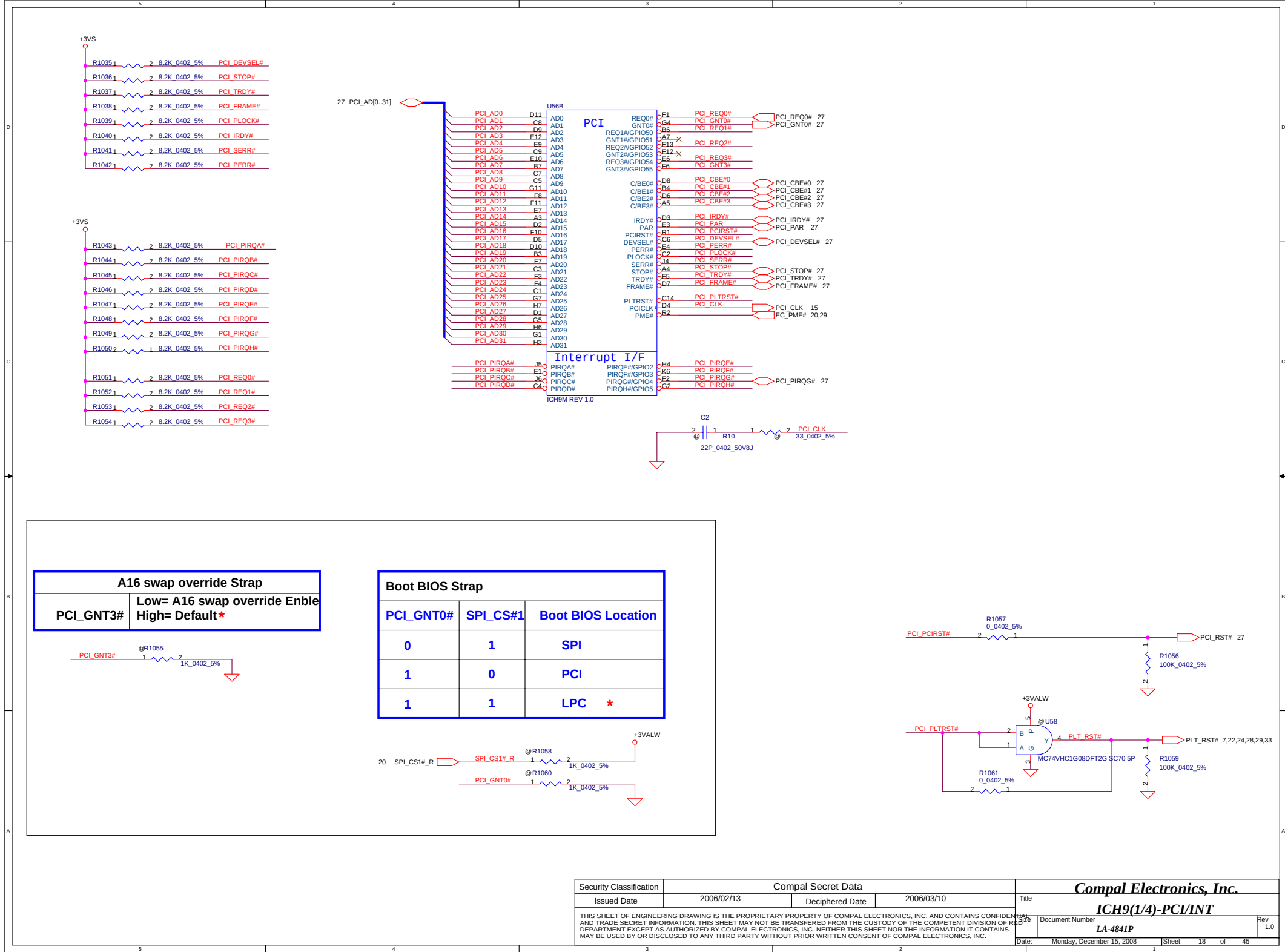


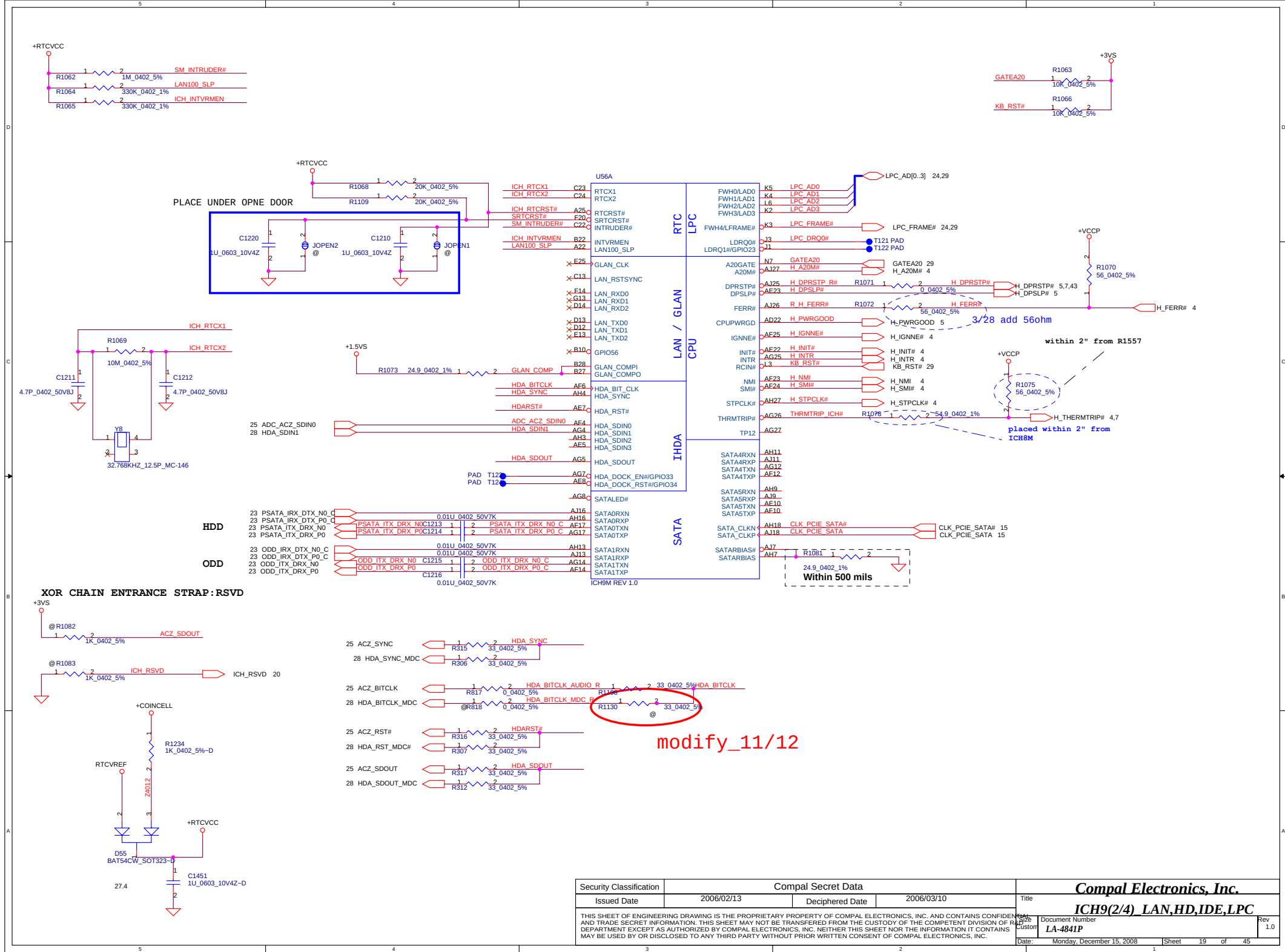
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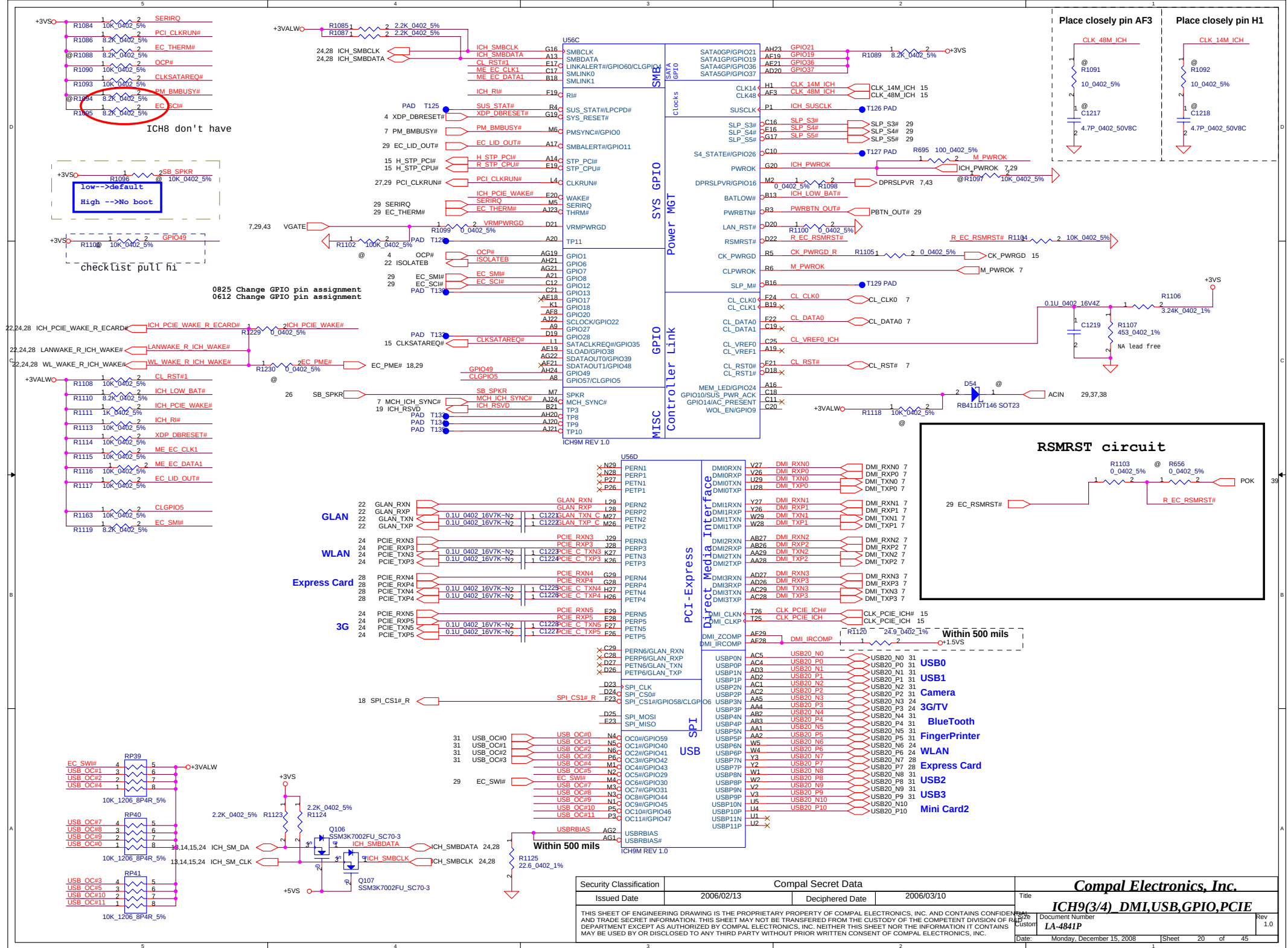
CRT

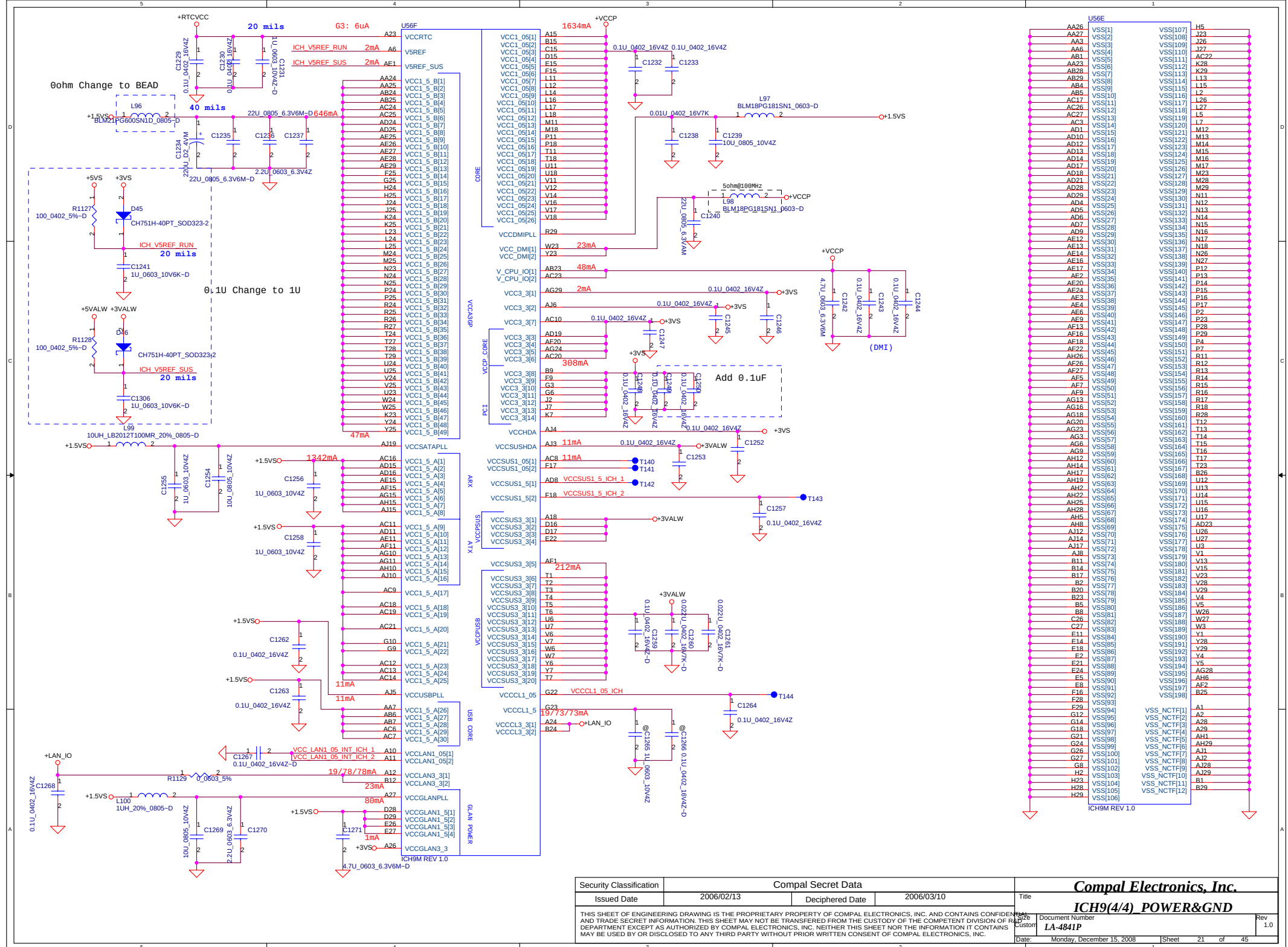


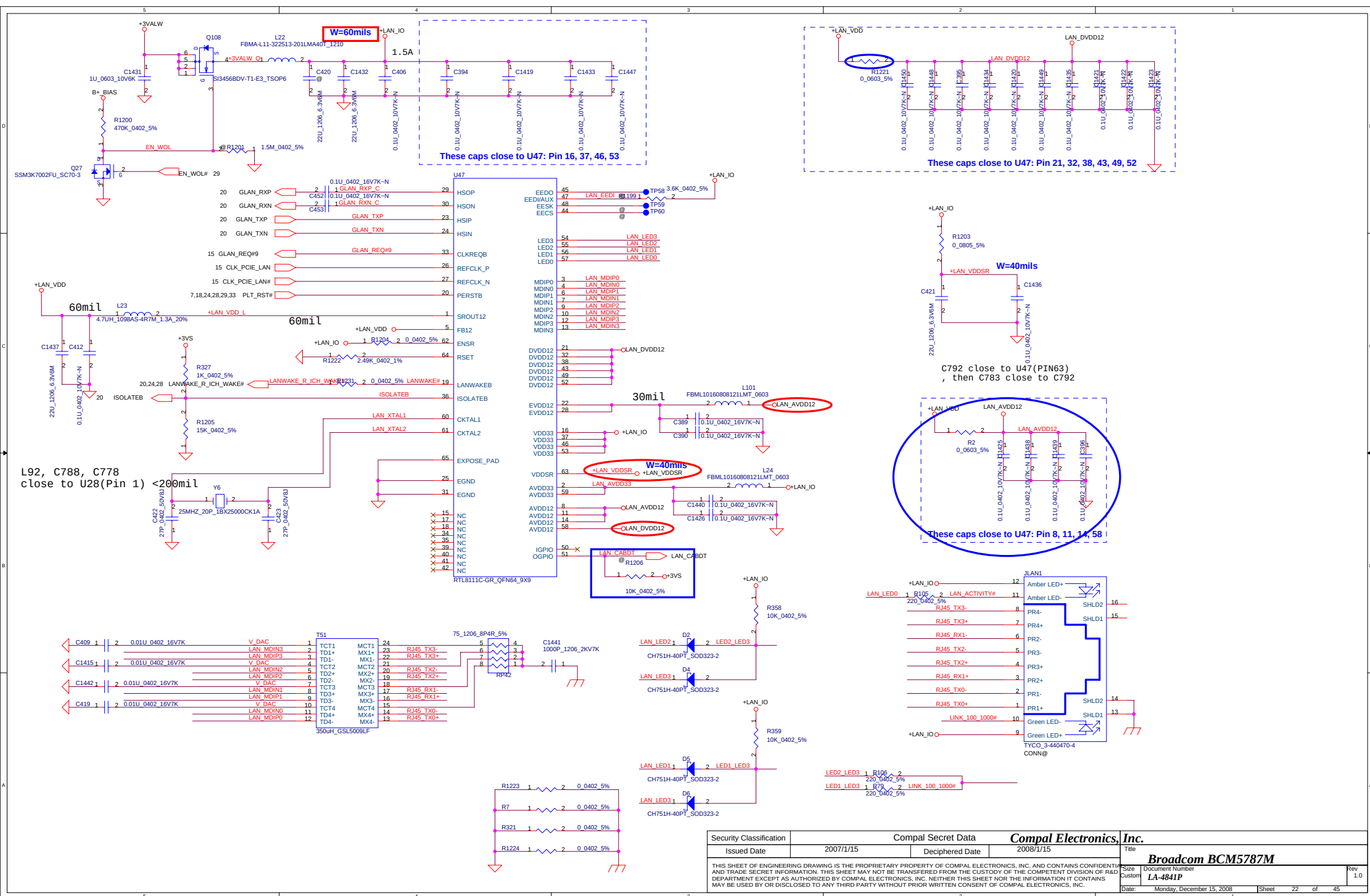
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Size Custom	Document Number LA-4841P		Rev 1.0
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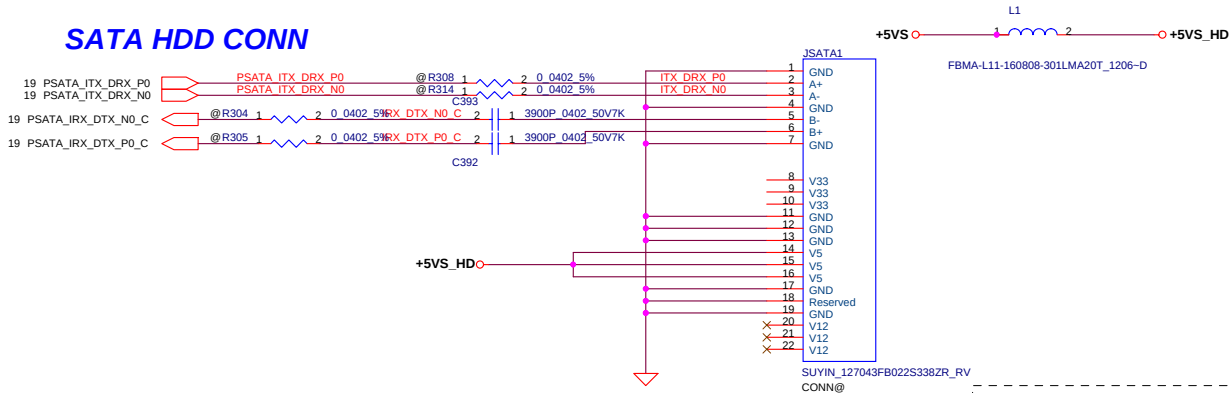




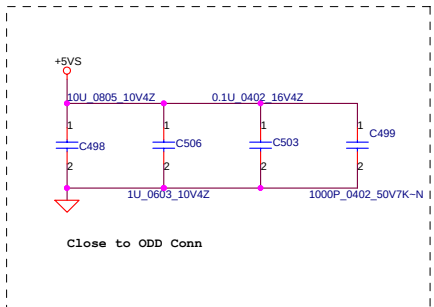
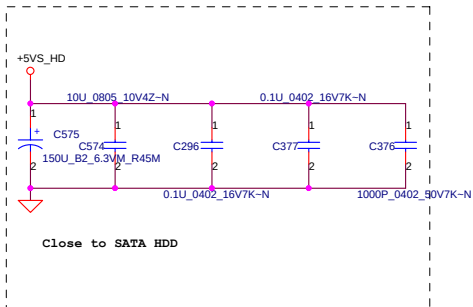
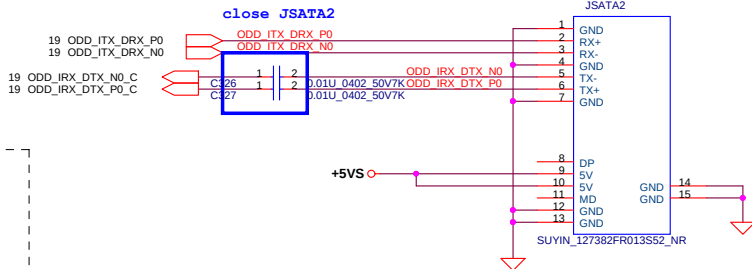




SATA HDD CONN

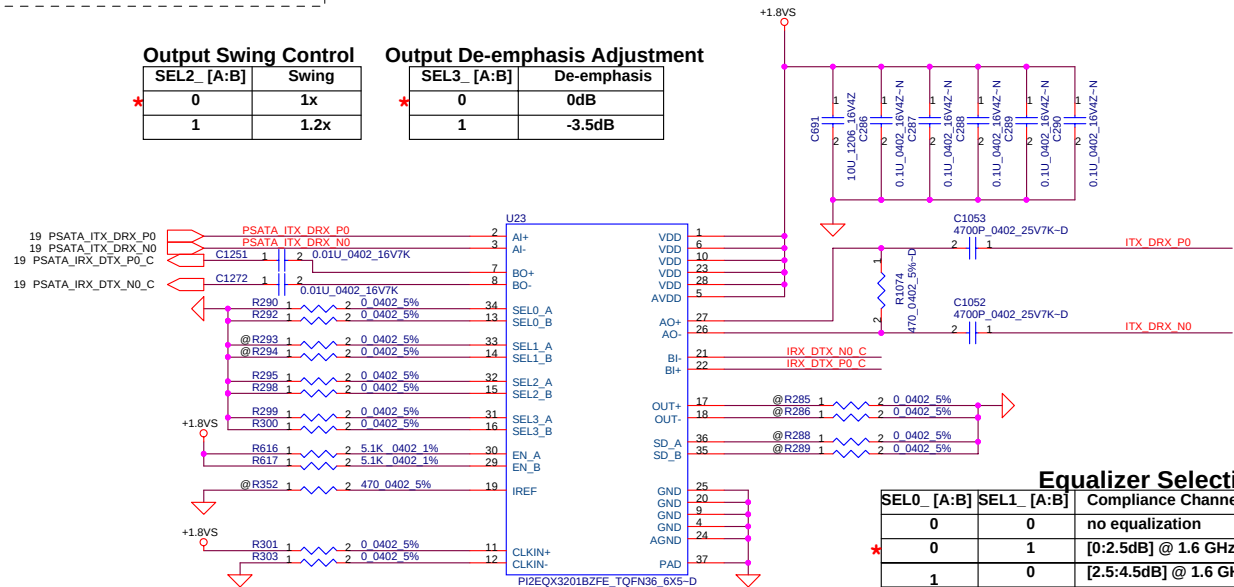


SATA ODD CONN



Output Swing Control	
SEL2_ [A:B]	Swing
0	1x
1	1.2x

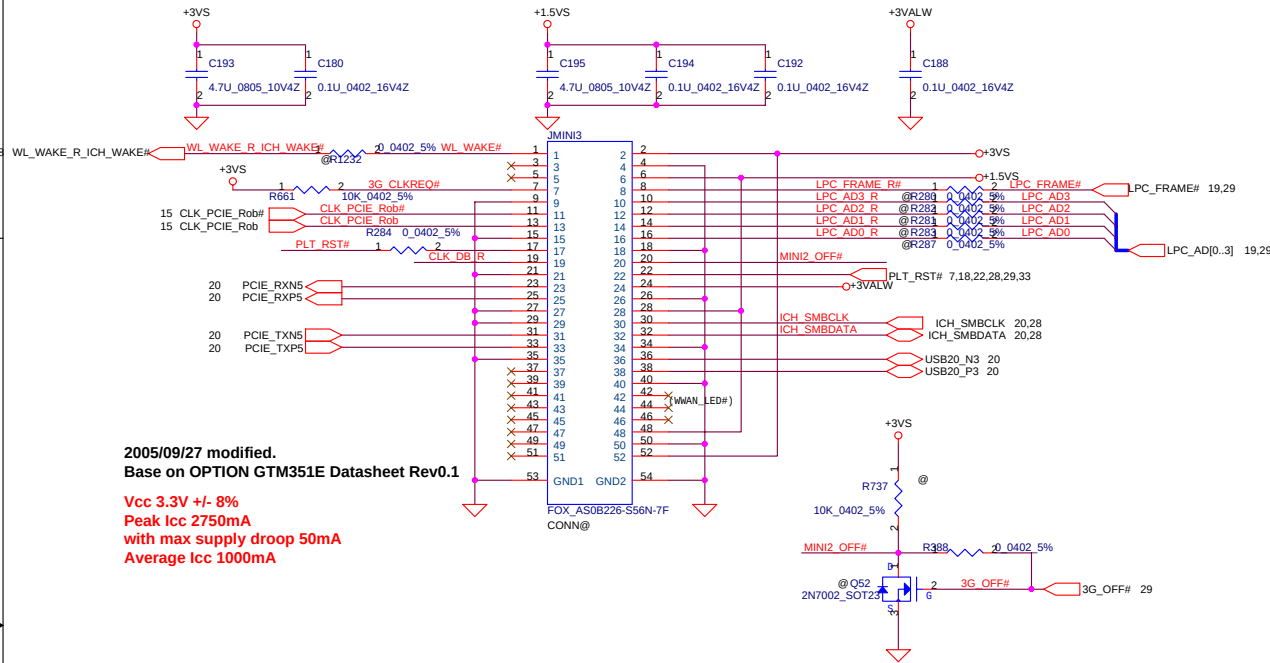
Output De-emphasis Adjustment	
SEL3_ [A:B]	De-emphasis
0	0dB
1	-3.5dB



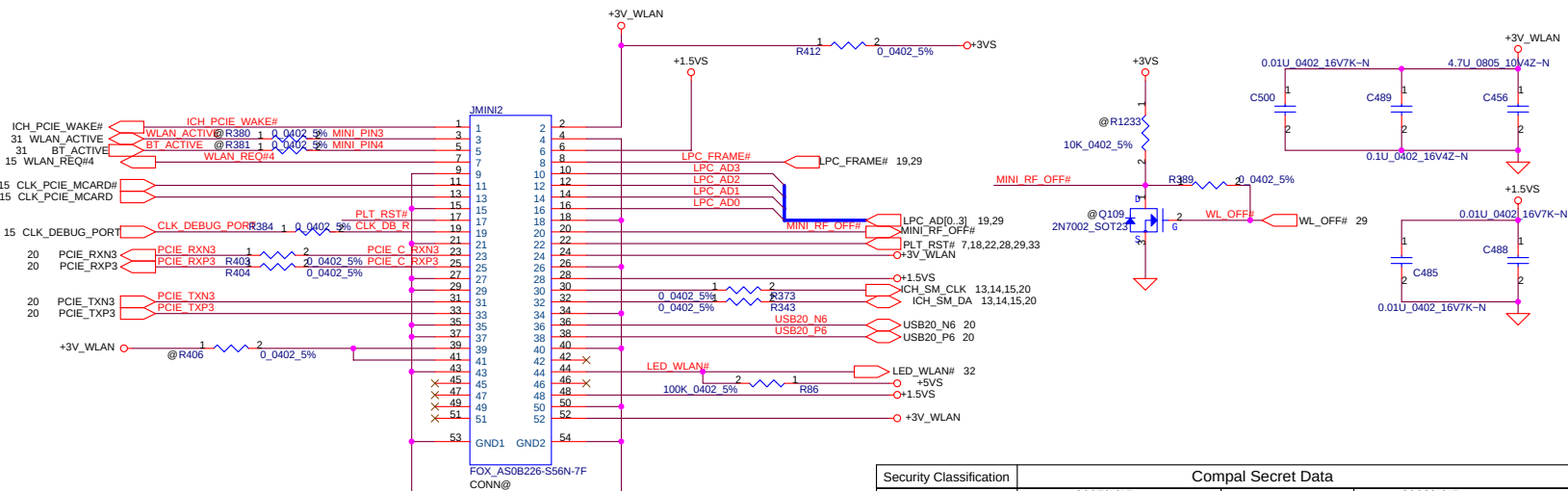
Equalizer Selection

SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

Mini-Express Card for 3G Or TV Tuner

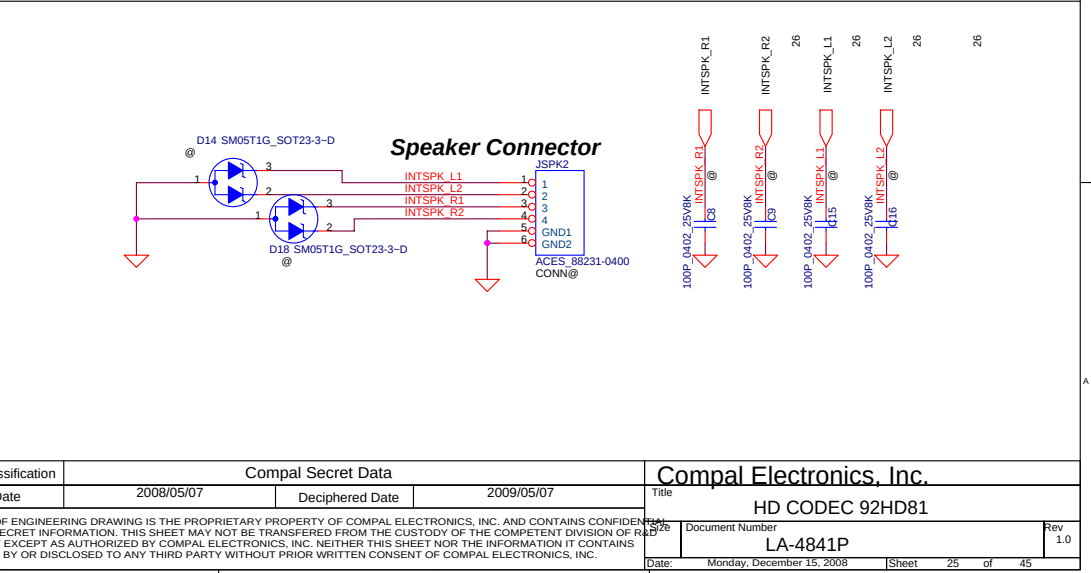
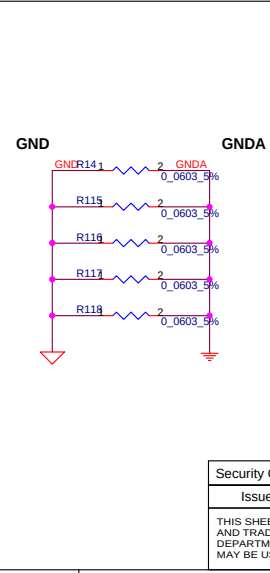
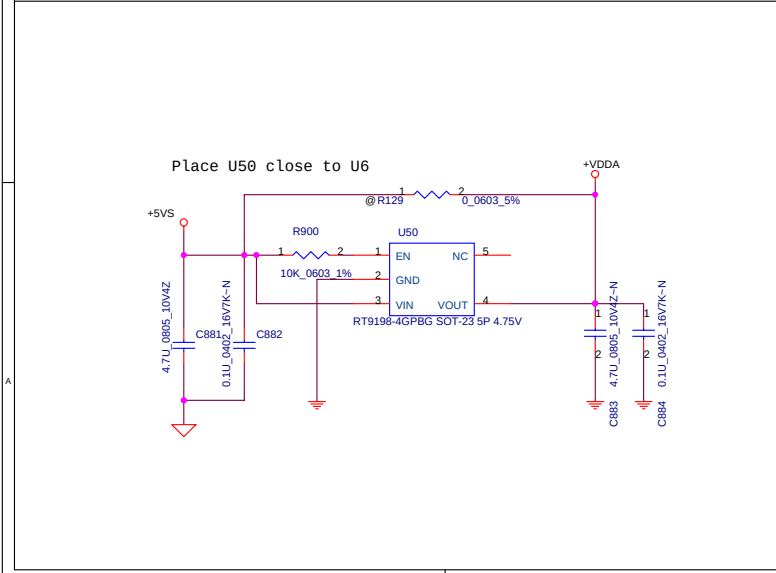
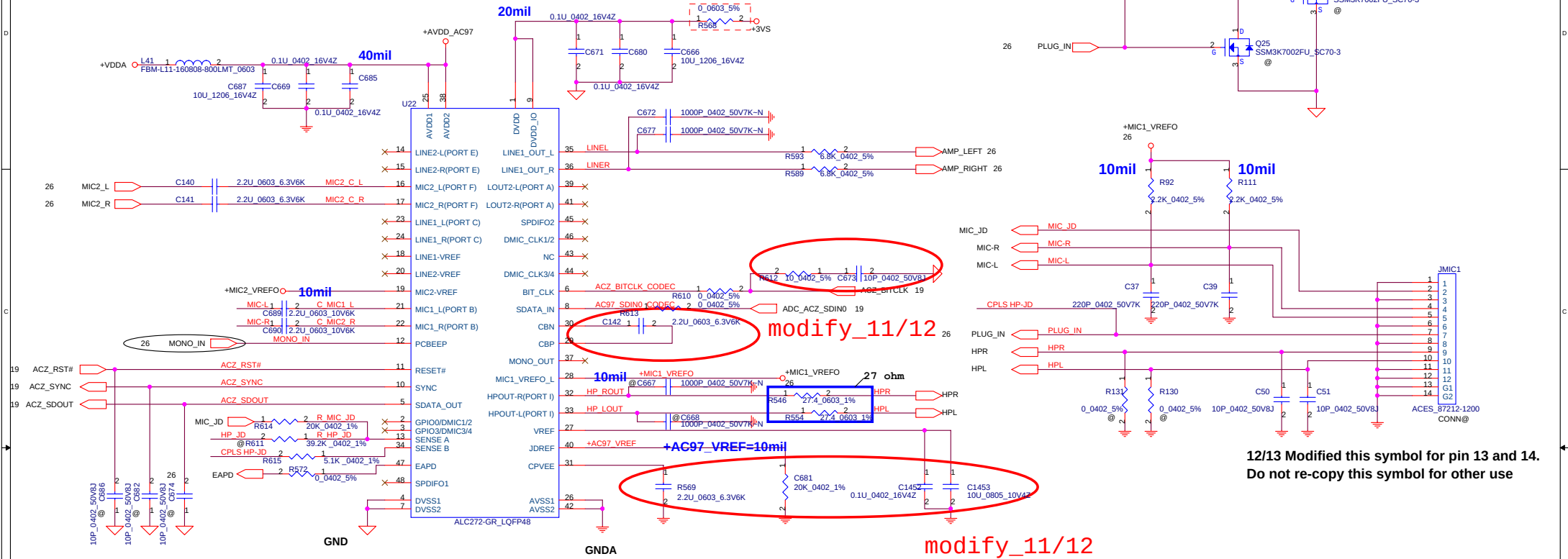


Mini-Express Card---WLAN

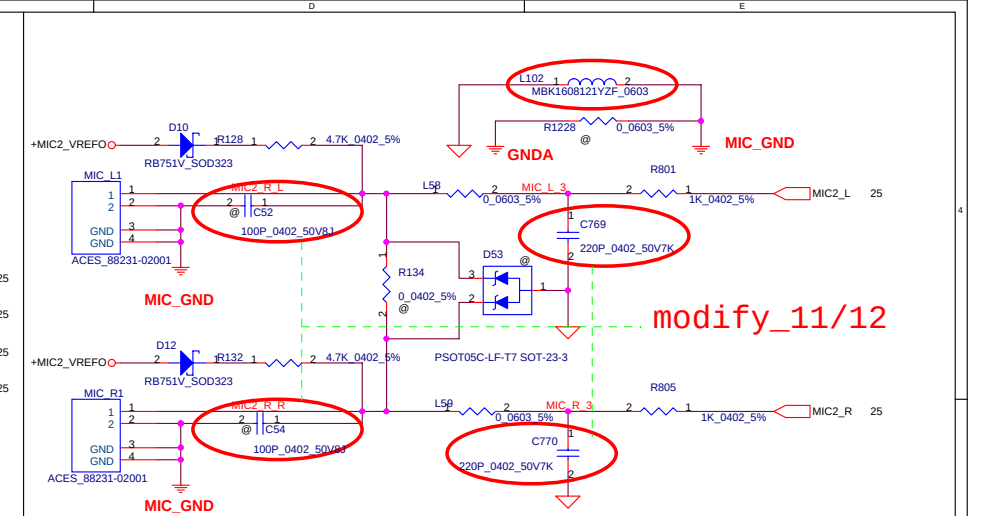
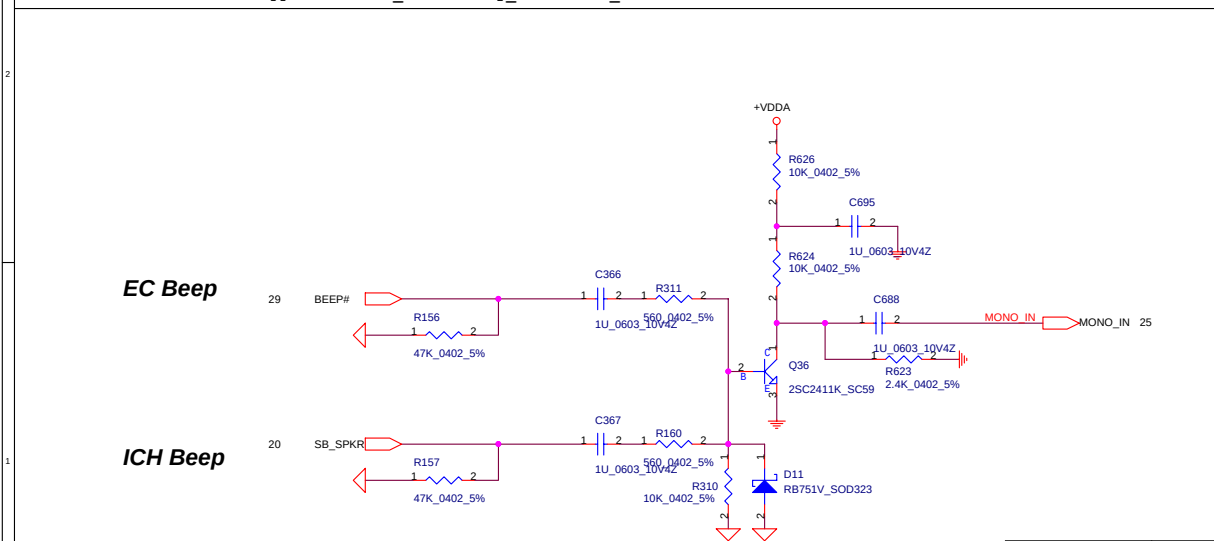
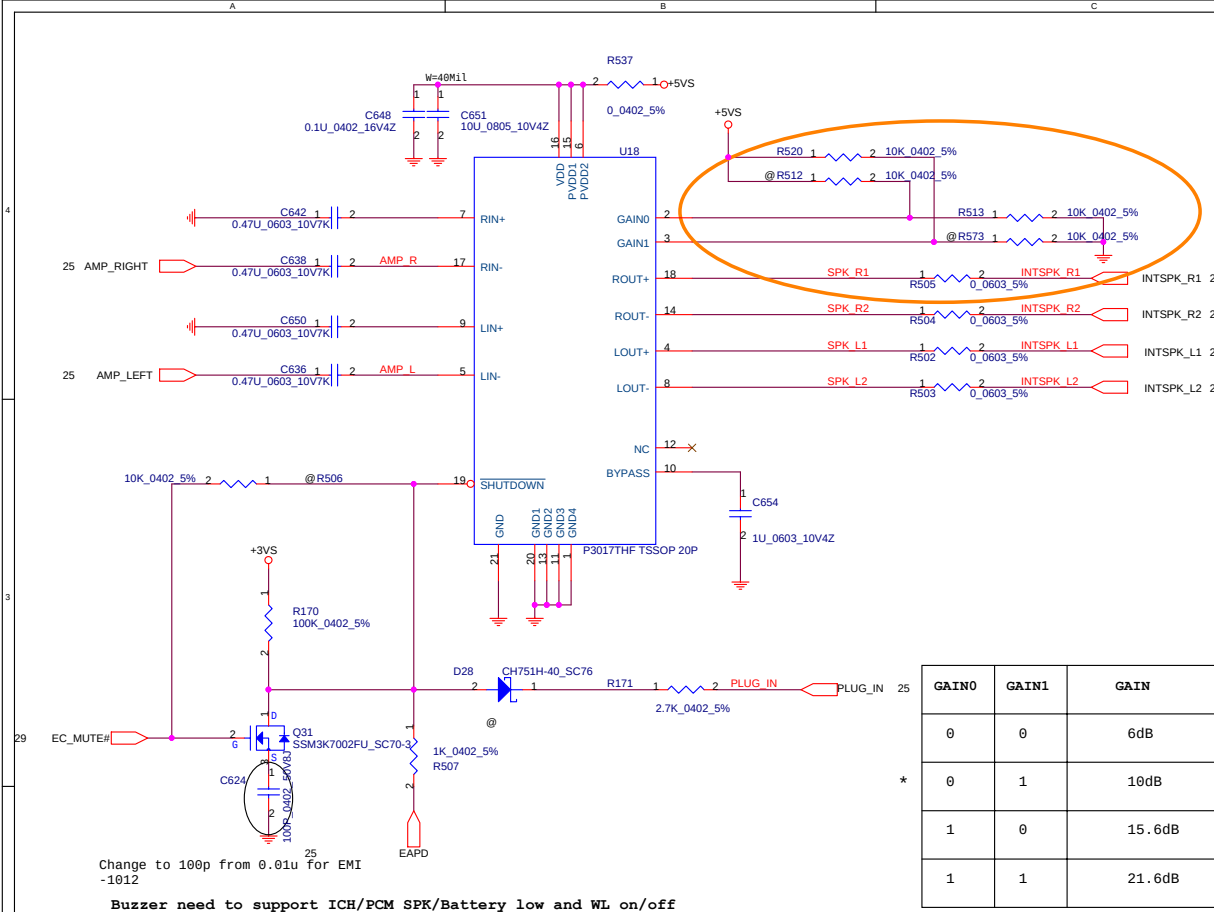


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				Mini-Card/LED			
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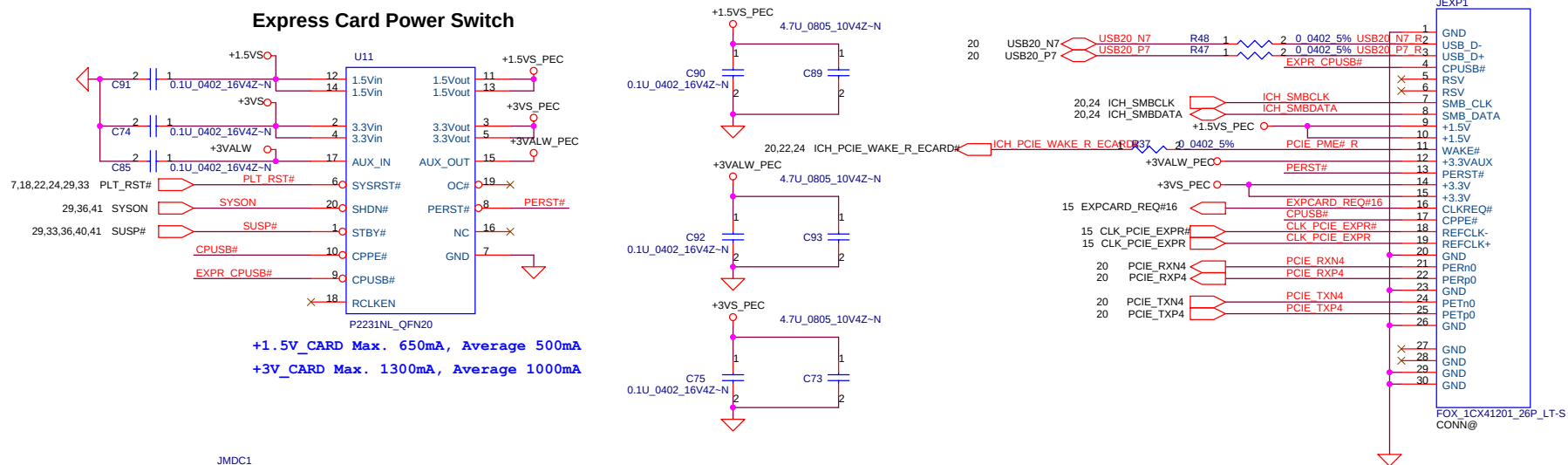
HD Audio Codec



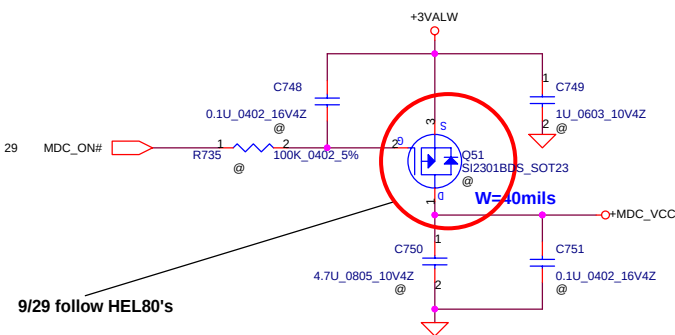
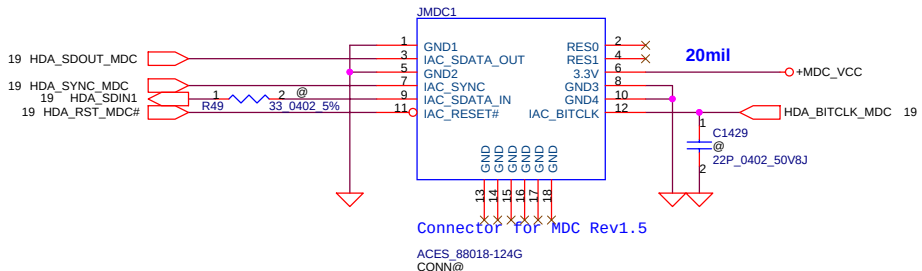
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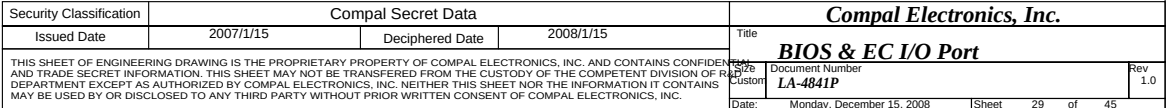
Express card

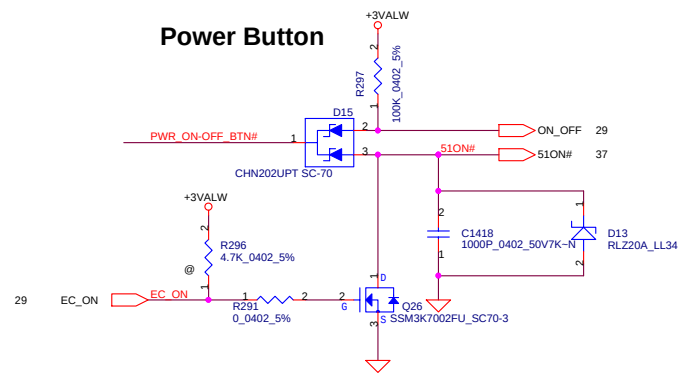


MDC Conn.

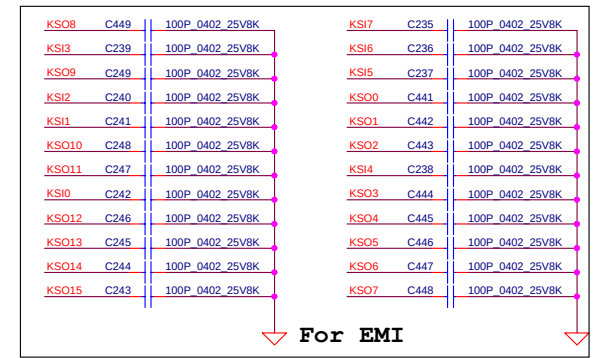
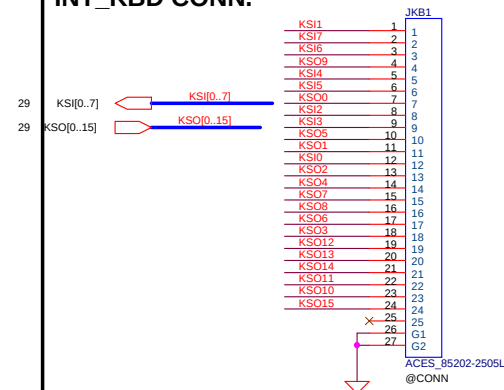


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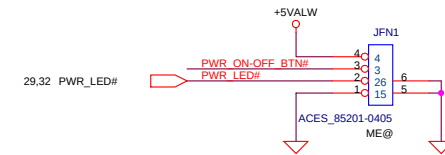




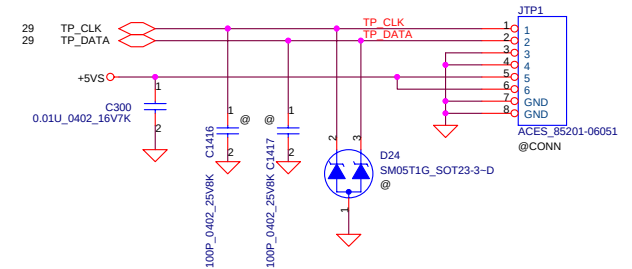
INT_KBD CONN.



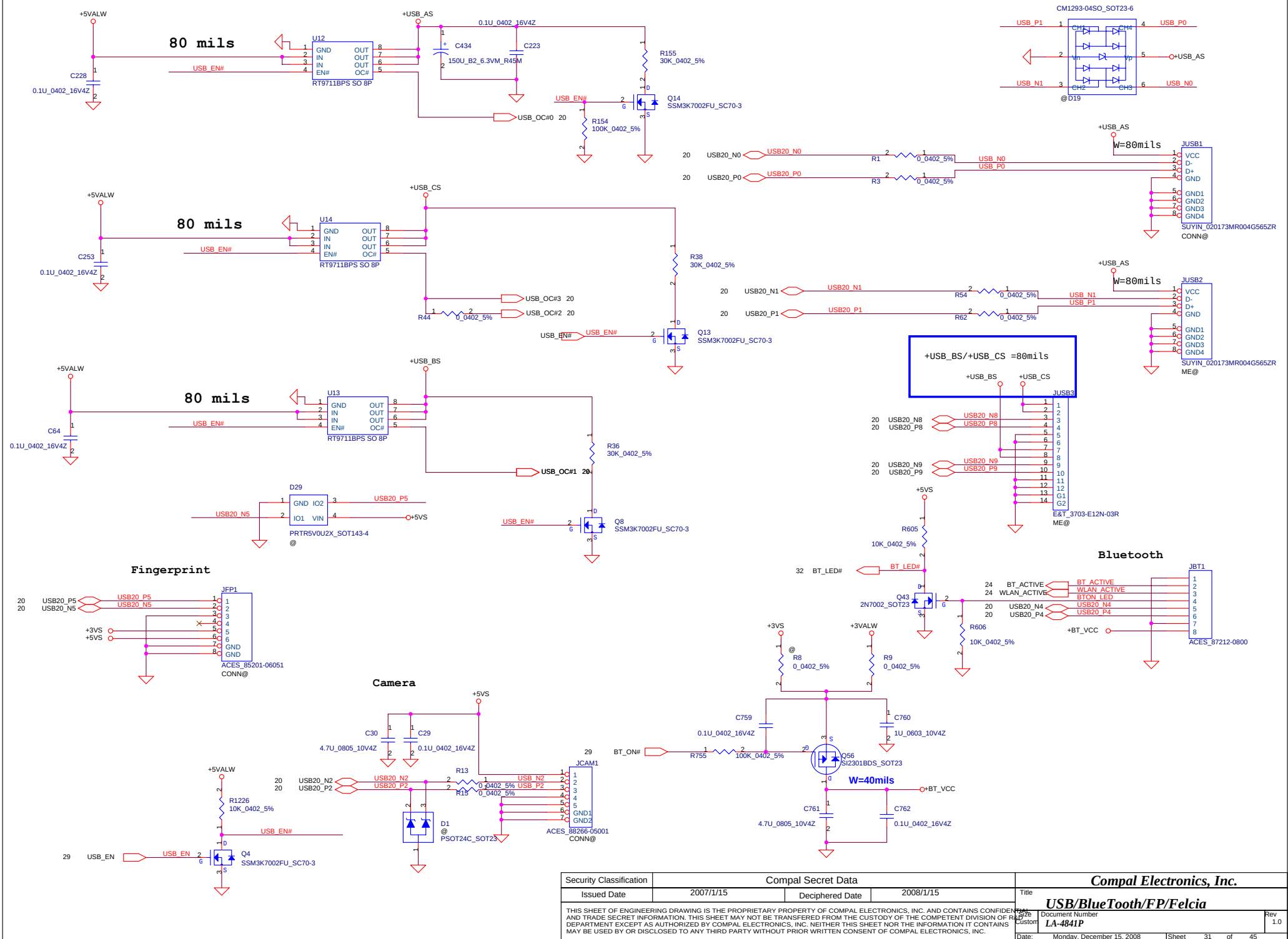
SW/B CONN.

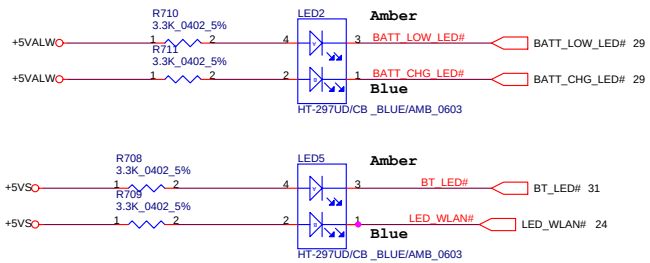
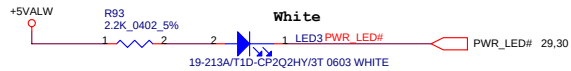


Touch PAD/B CONN.

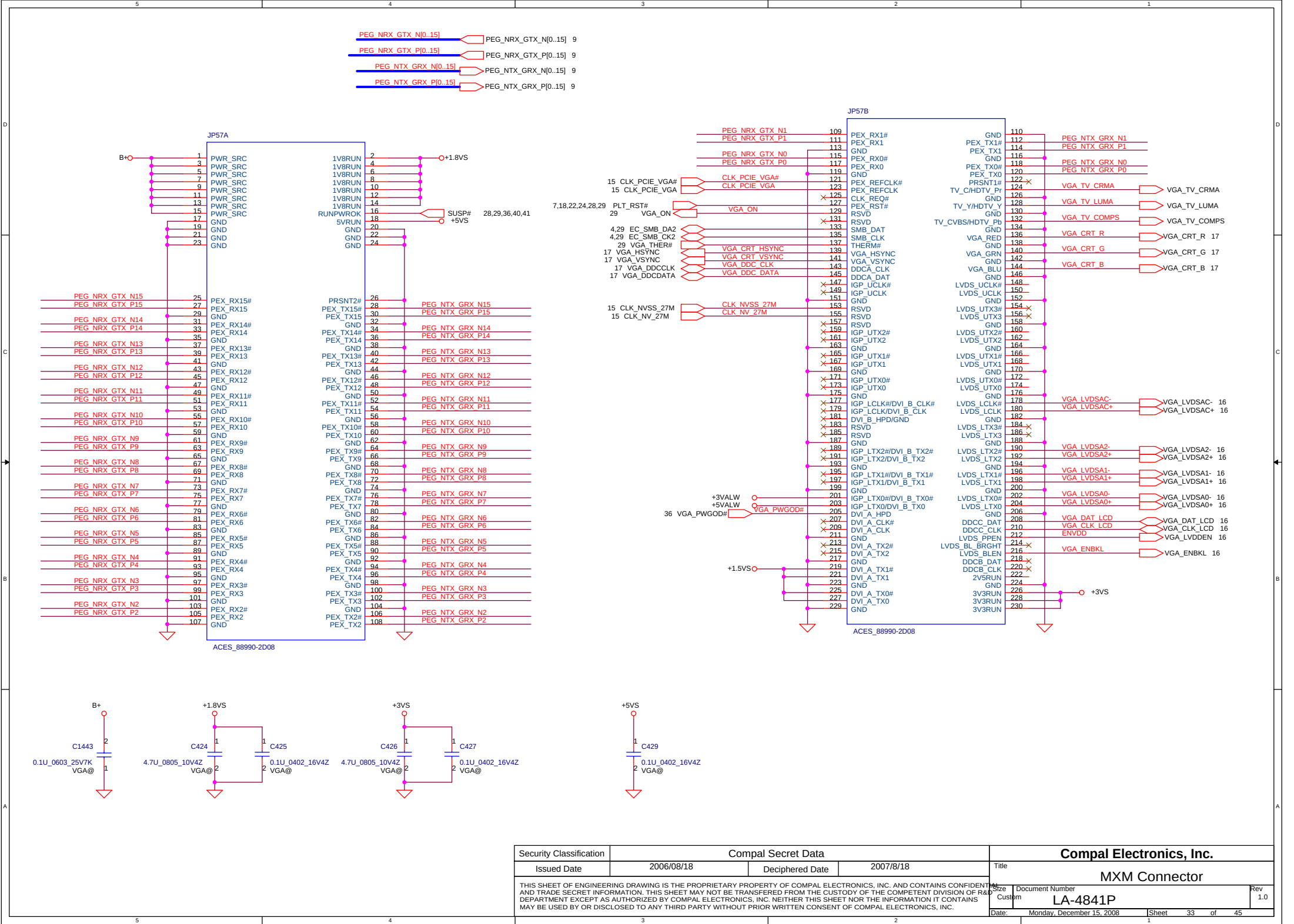


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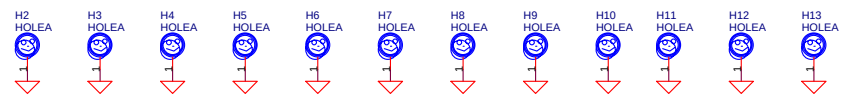


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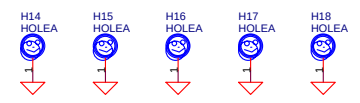


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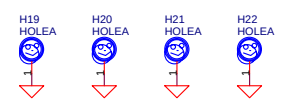
H_3P0



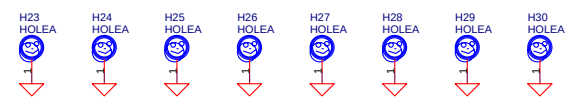
H_3P7



H_4P2



H_3P2

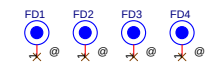


H_5P6

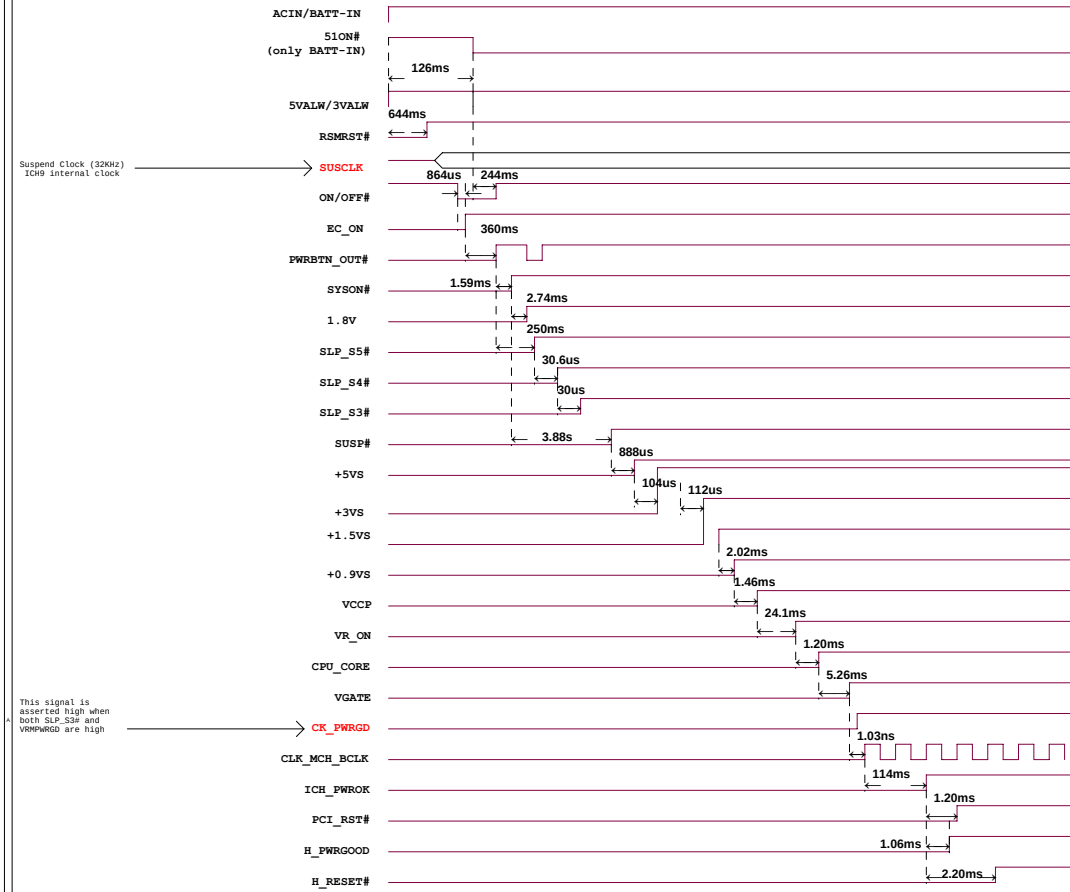


H_4P4

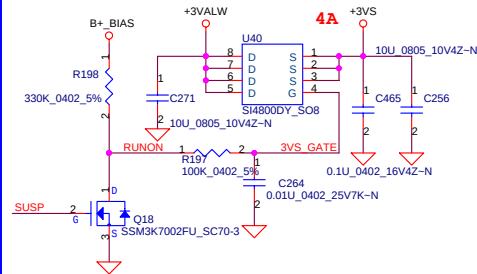
H_3P1N



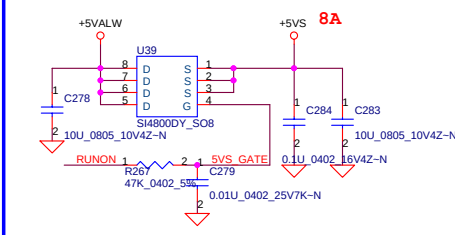
KAL80 POWER UP SEQUENCE



+3VALW to +3VS Transfer

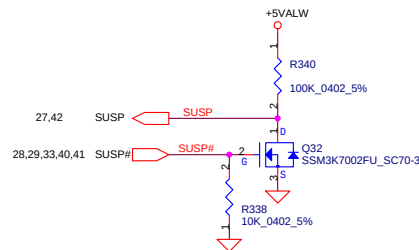
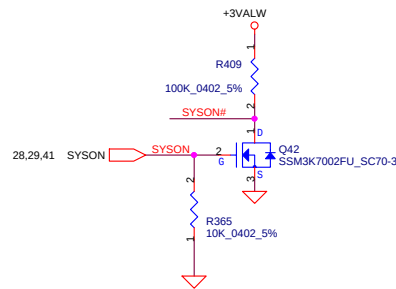
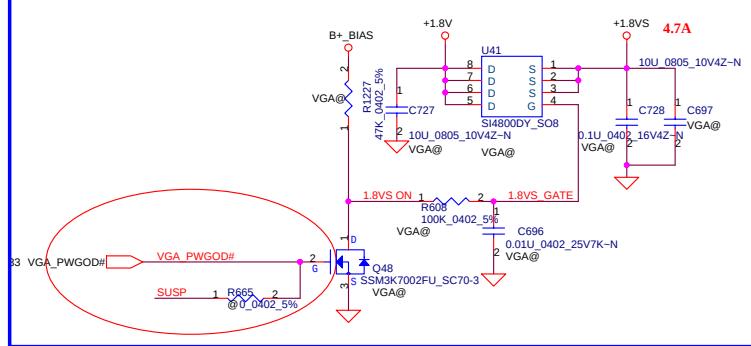


+5VALW to +5VS Transfer

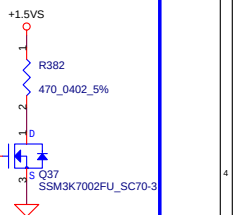
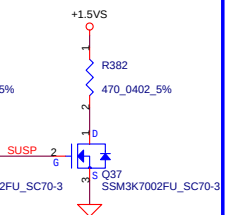
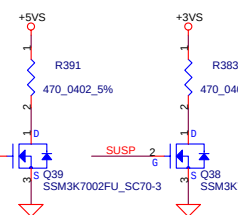
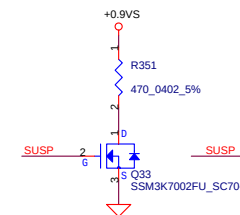
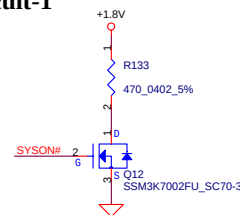


+CPU_CORE 1 2 0.1U_0402_16V4Z-N +VCCP

+1.8V to +1.8VS Transfer



Discharge circuit-1



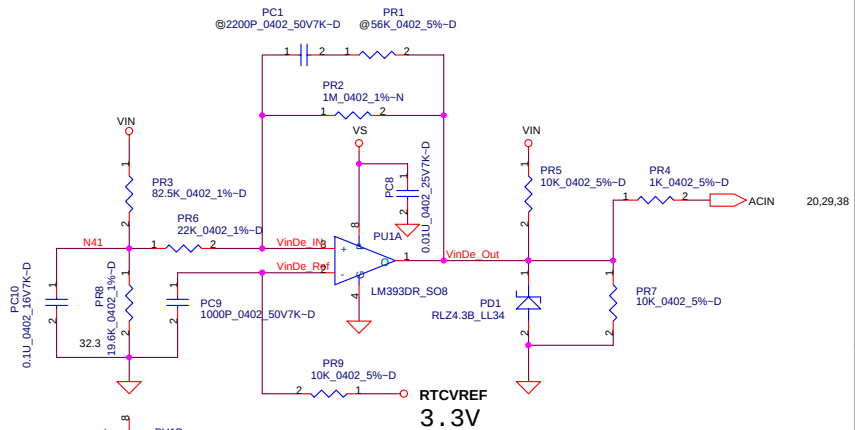
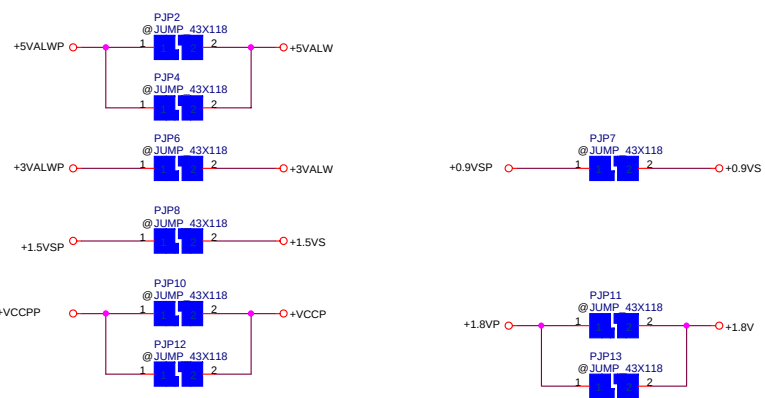
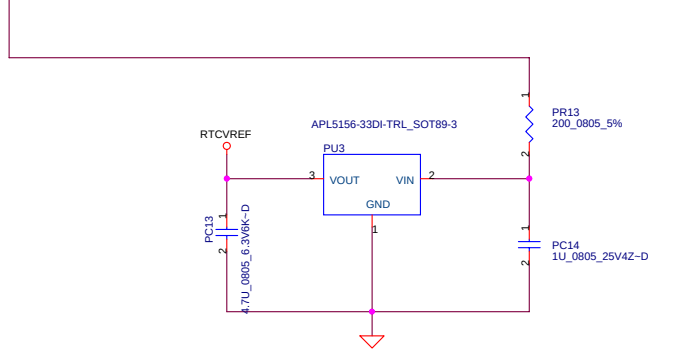
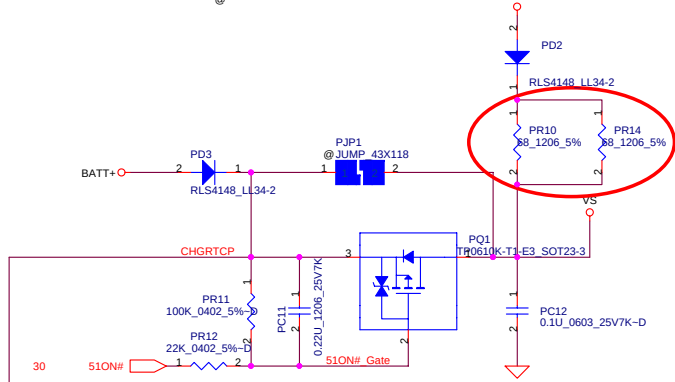
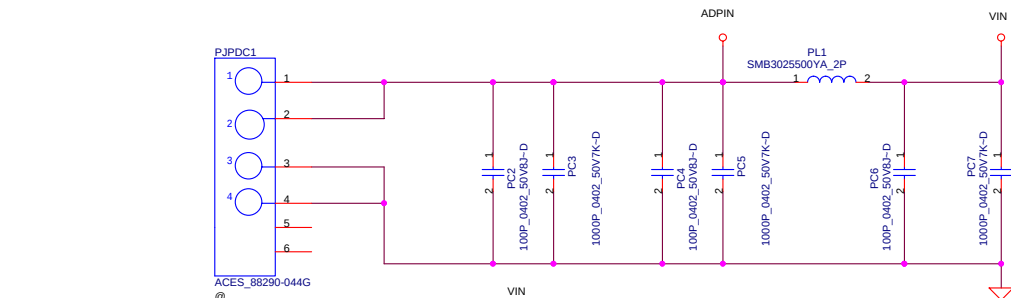
SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

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Compal Electronics, Inc.

DC/DC Circuits

LA-4841P



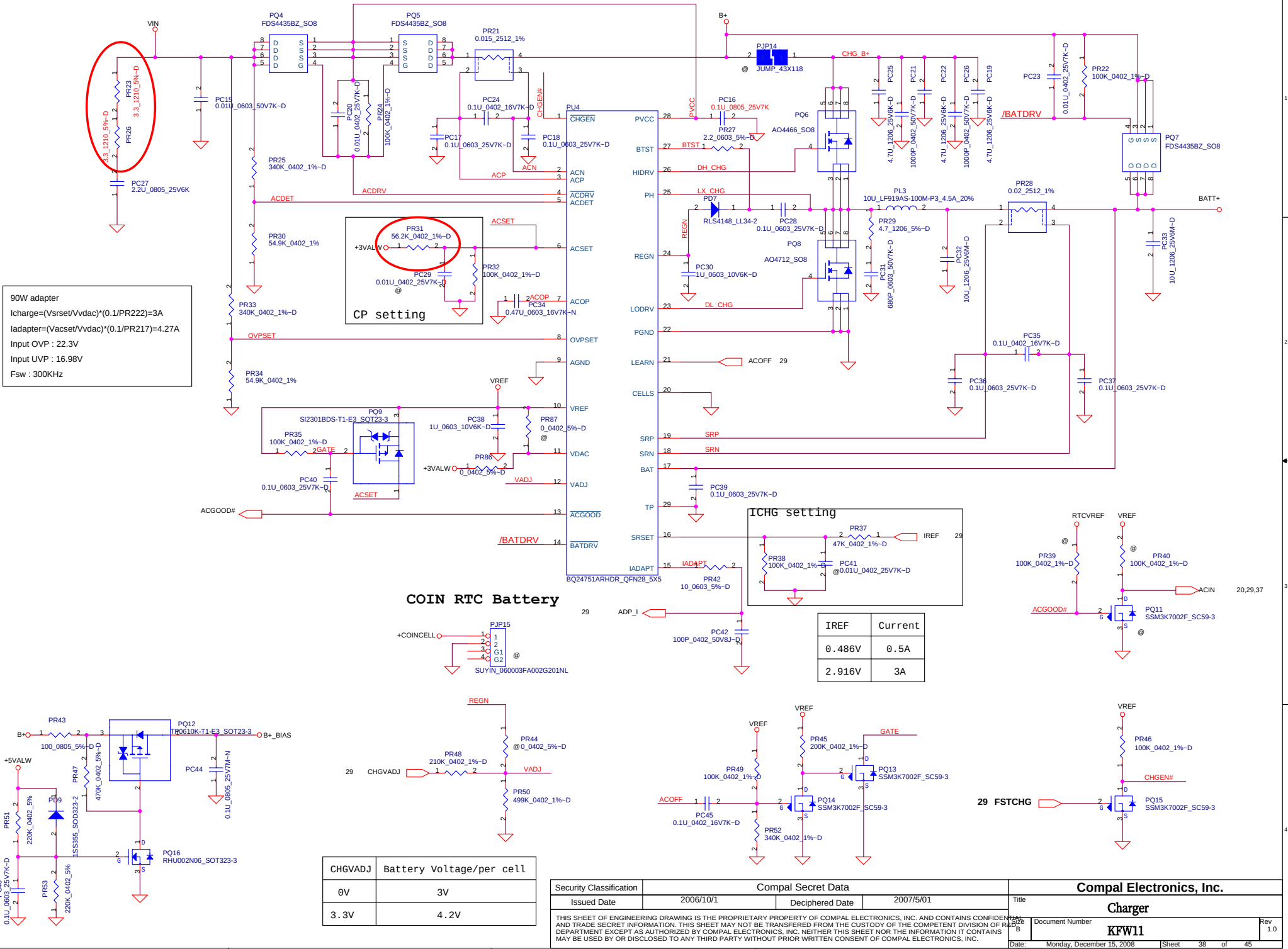
	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

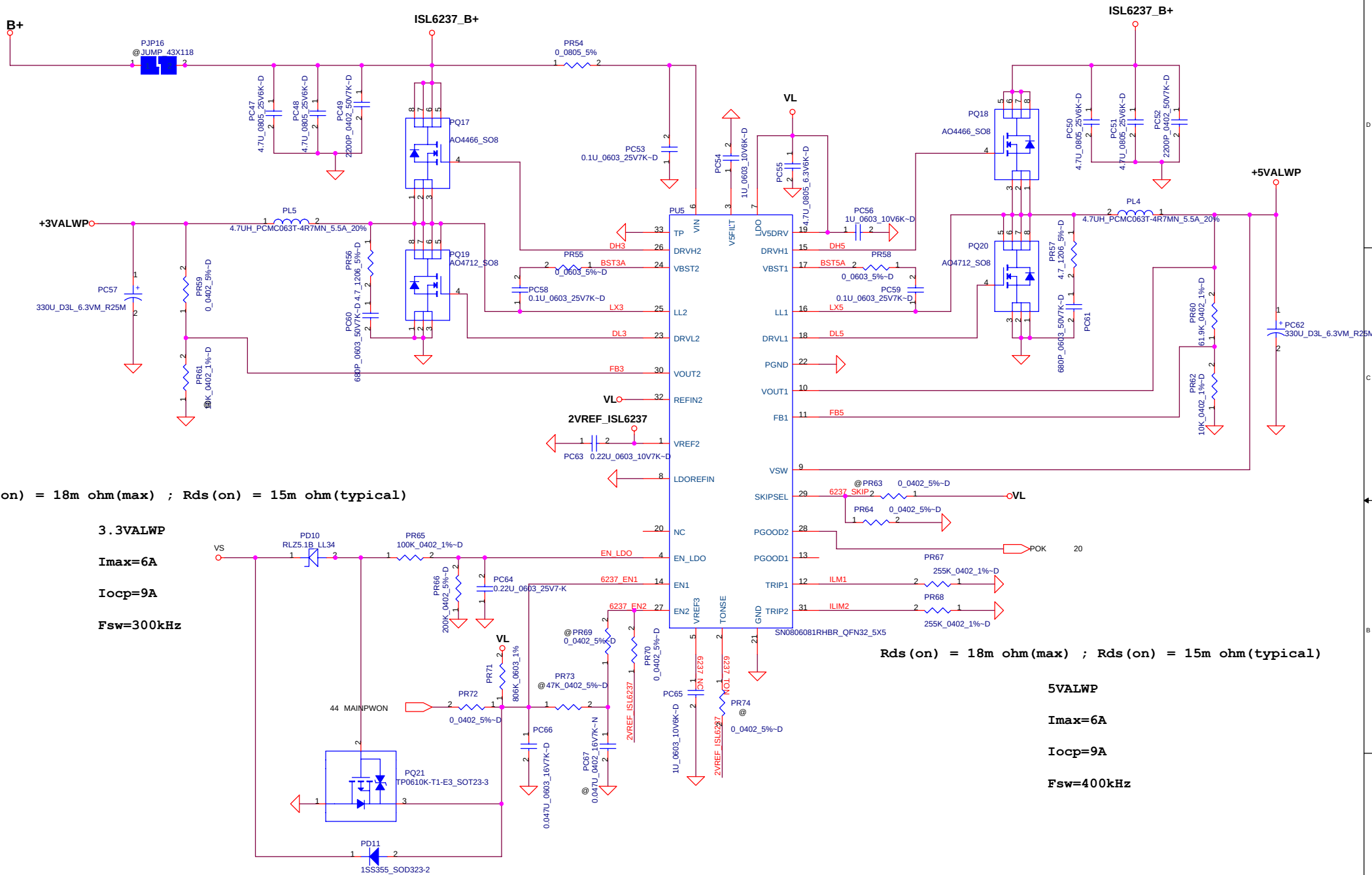
90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR222) = 3A$
 $I_{adapter} = (V_{vacset}/V_{vdac}) * (0.1/PR217) = 4.27A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz

COIN RTC Battery

CHGVADJ	Battery Voltage/per cell
0V	3V
3.3V	4.2V

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$R_{ds(on)} = 18\text{m ohm(max)} ; R_{ds(on)} = 15\text{m ohm(typical)}$

3.3VALWP

$$I_{max}=6A$$
$$I_{ocp} = 9A$$

$F_{sw}=300\text{kHz}$

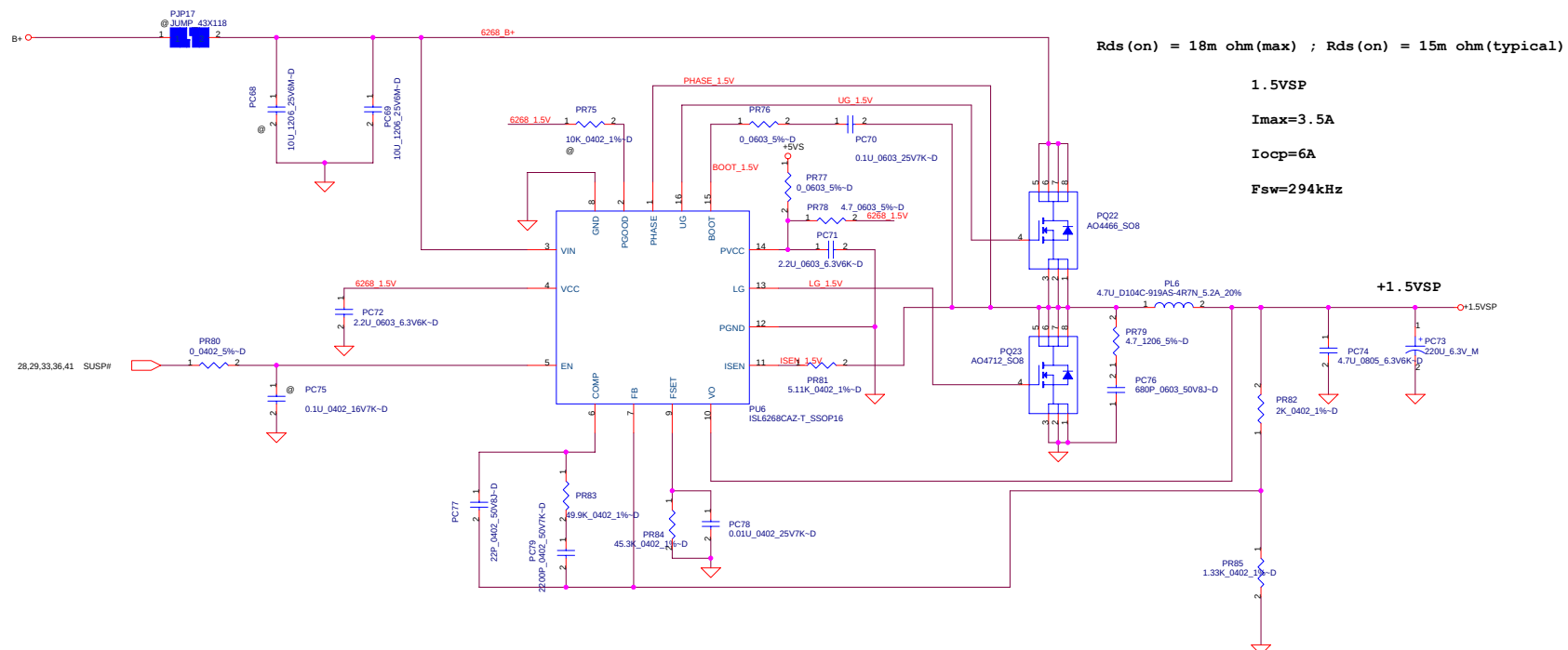
$R_{ds(on)} = 18\text{m ohm(max)} ; R_{ds(on)} = 15\text{m ohm(typical)}$

5VALWP

$$I_{\max} = 6A$$
$$I_{ocp} = 9A$$

$F_{sw}=400kHz$

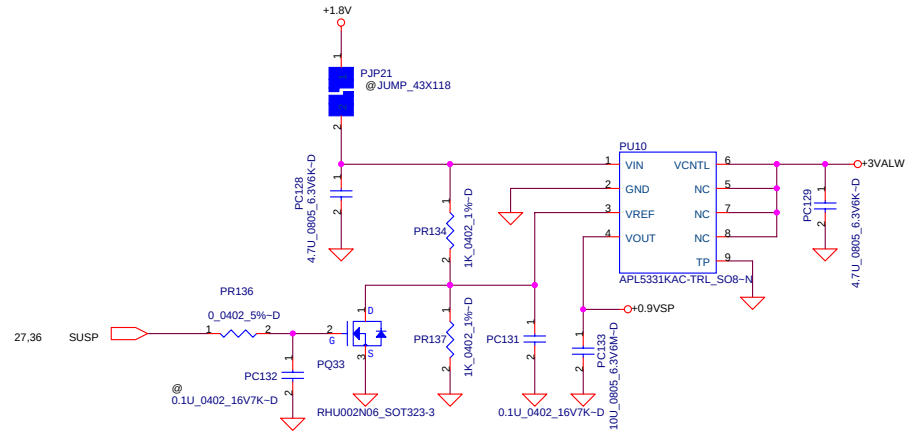
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Issued Date	2006/10/1	Deciphered Date	2007/05/30	Title	+3VALWP, +5VALWP	
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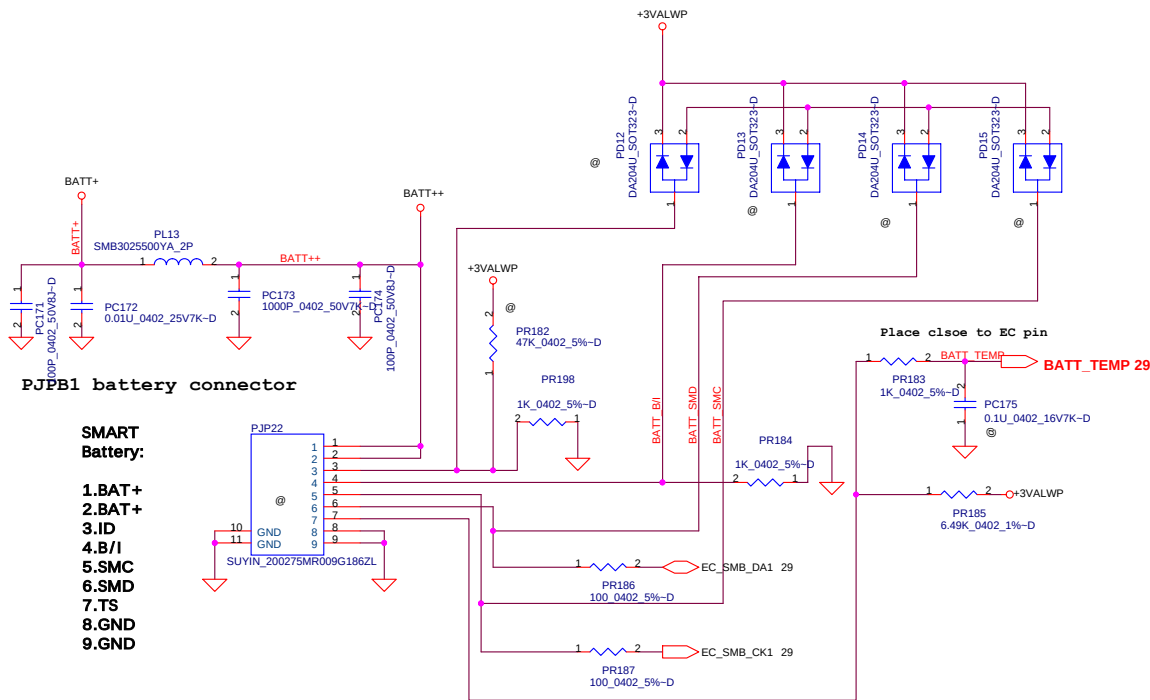
Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

1.5VSP
Imax=3.5A
Iocp=6A
Fsw=294kHz

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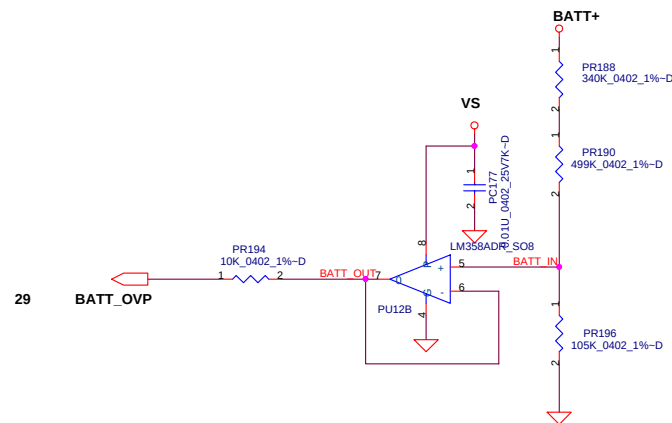


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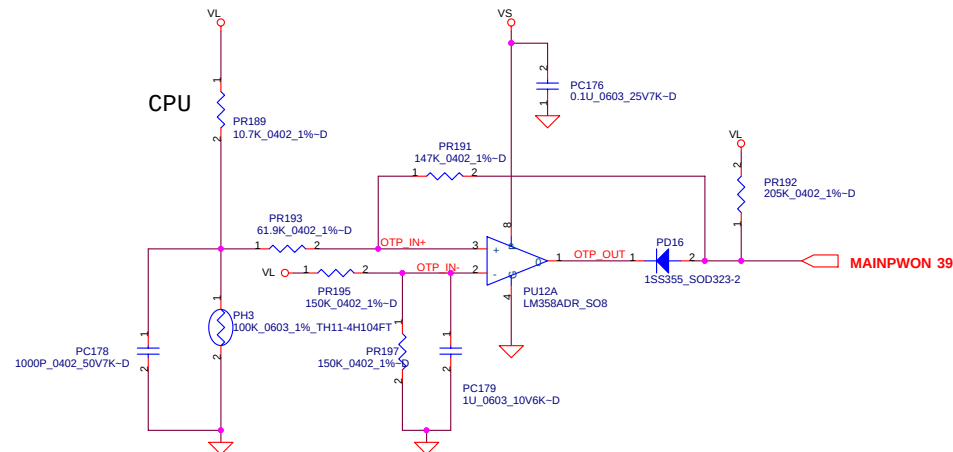


CPU

PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C



OVP voltage :
 LI-3S :13.50V--BATT-OVP=1.5V
 BATT-OVP=0.111*BATT+



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