

COMPAL CONFIDENTIAL

MODEL NAME : **VAW30**
PCB NO : **LA-9832P (DA8000XL000)**
BOM P/N : **4319M931L01**
GPIO MAP: X.X

Alpine 14"

Haswell ULT

2013-08-23(Gerber)

REV : 1.0

@ : Nopop Component

1@ : M/B SPI ROM

TAA@ : TAA/B SPI ROM

CONN@ : Connector Component

DIS@ : Discrete Pop Component

UMA@ : UMA Pop Component

EMI@ : EMI Component

ESD@ : ESD Component

RF@ : RF Component

XDP@ : XDP Component

eTP@ : TS eTP Component

NeTP@ : TS non - eTP Component

76_U3@ : USB 3.0 Redriver

1 @ 2 : Short_Pad

Interleaved Memory

MB.PCB	
Part Number	Description
0AXXXXXXXX	PCB 8LD LA-9832P REV1 M/B DIS

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Title		Cover Sheet	
Size	Document Number	Rev	
	LA-9832P	0.5	
Date:	Thursday, August 15, 2013	Sheet	1 of 64

POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and
PM Table

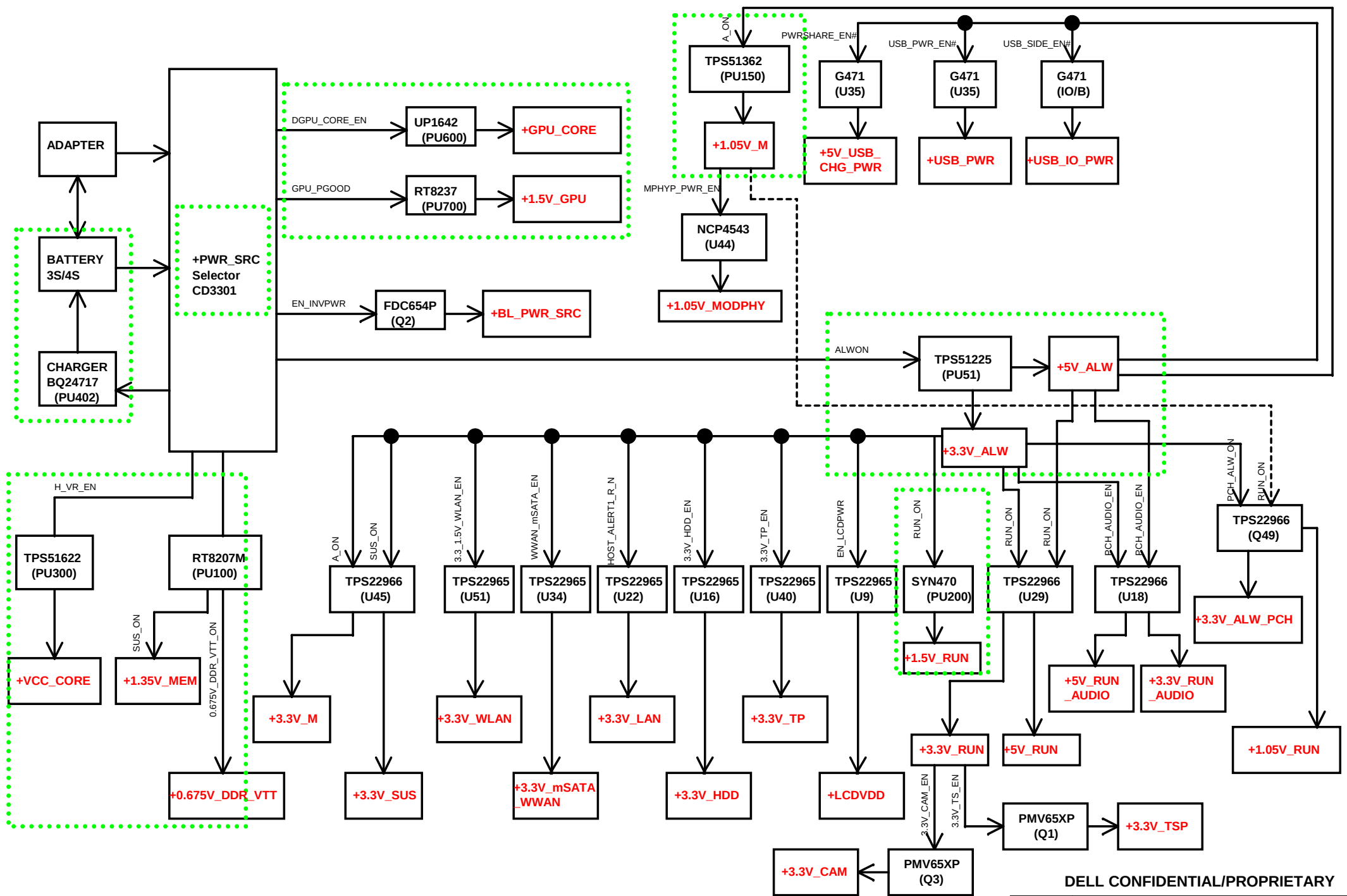
PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->MB-->LEFT
	USB3.0 2		USB3.0-->IOB-->Rear Right
PCIE 1	USB3.0 3		PCIE1-->MMI PCIE
PCIE 2	USB3.0 4		USB3.0-->Docking
PCIE 3			LOM
PCIE 4			WLAN (WiGi)
PCIE 5			GPU(DIS)/Express card(UMA)
PCIE 6		SATA 3	WWAN(mSATA)/Express card(PCIE)
		SATA 2	ODD
		SATA 1	HDD
		SATA 0	DOCK

HSW ULT	USB PORT#	DESTINATION
	0	IO (Right)
	1	JUSB1(Left)
	2	USB DB(Rear Left)
	3	DOCK
	4	Dock
	5	WebCAM
	6	Touch Screen
	7	USB HUB

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Index and Config.			
Size	Document Number	Rev	
	LA-9832P	0.5	
Date:	Thursday, June 13, 2013	Sheet	3 of 64

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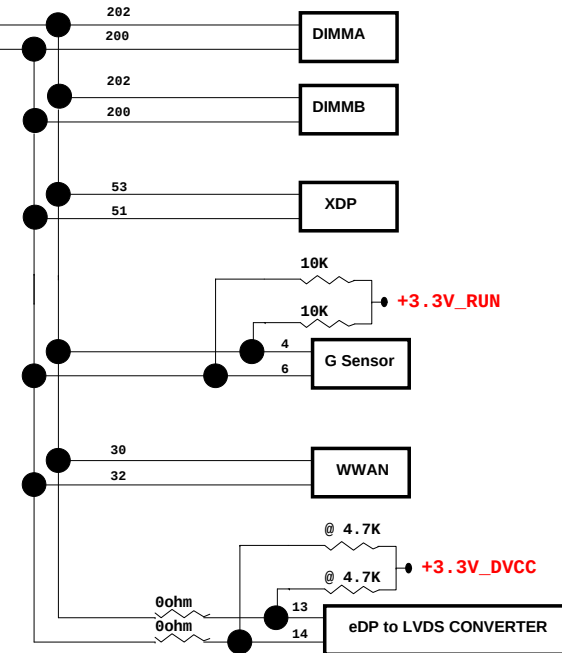
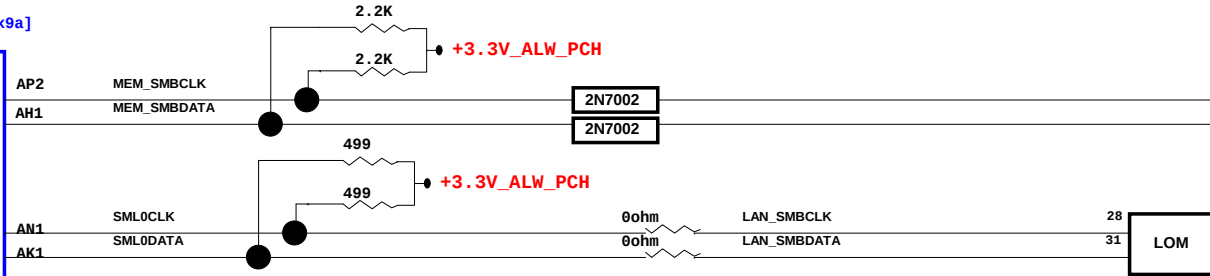
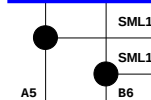
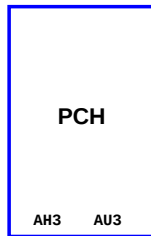
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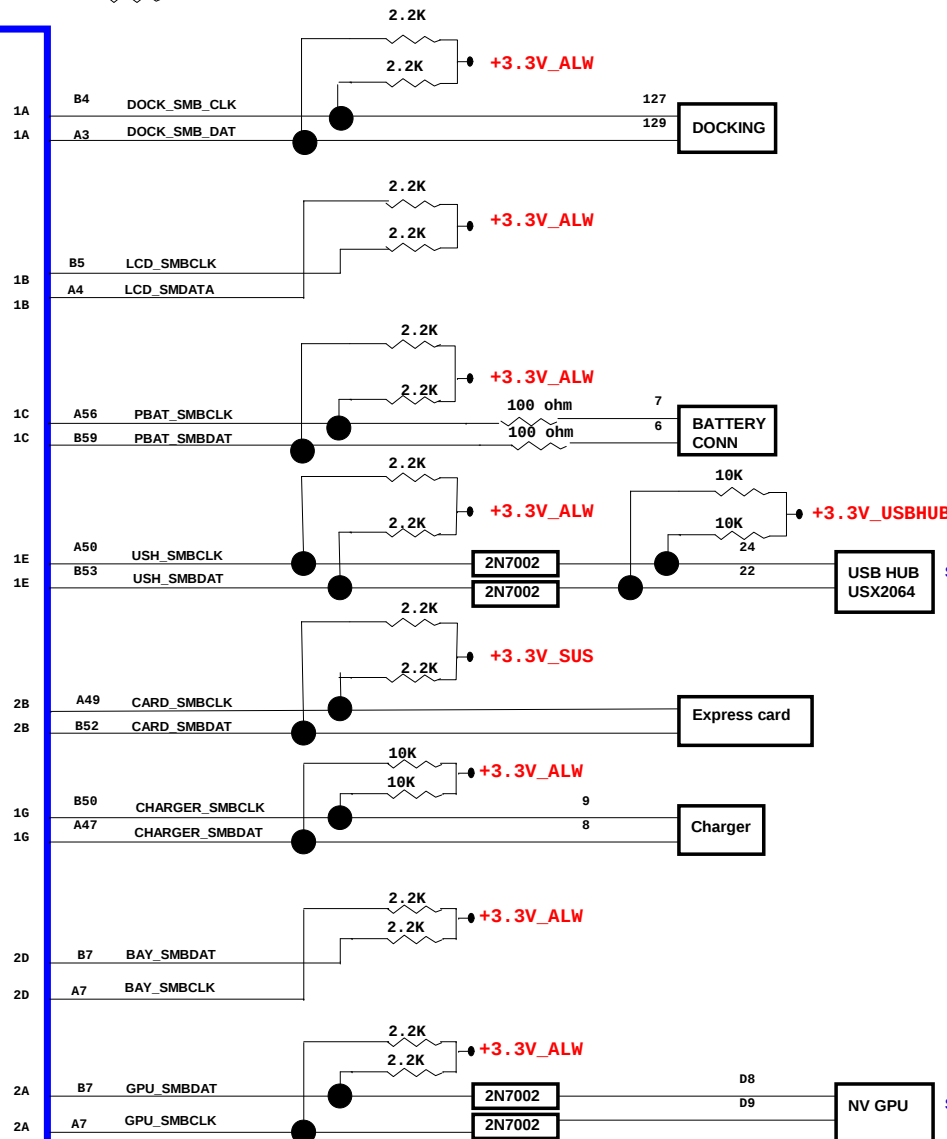
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Title	Power Rail		
Size	Document Number	Rev	
	LA-9832P	0.5	
Date:	Thursday, June 13, 2013	Sheet	4 of 64

SMBUS Address [0x9a]



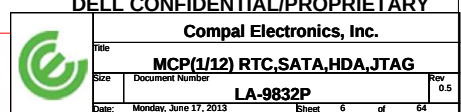
KBC

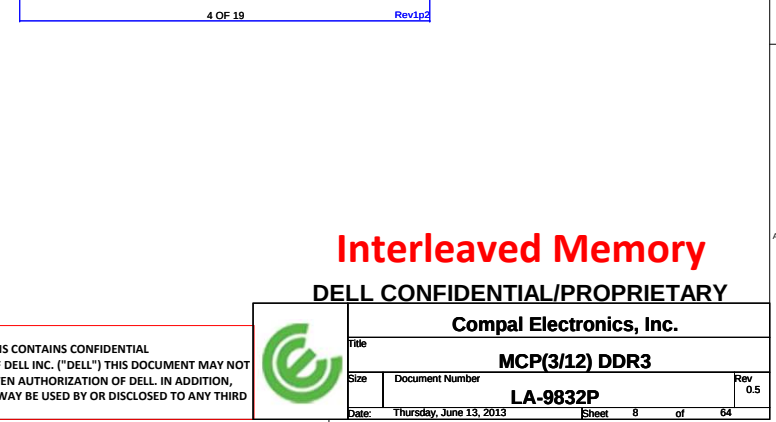
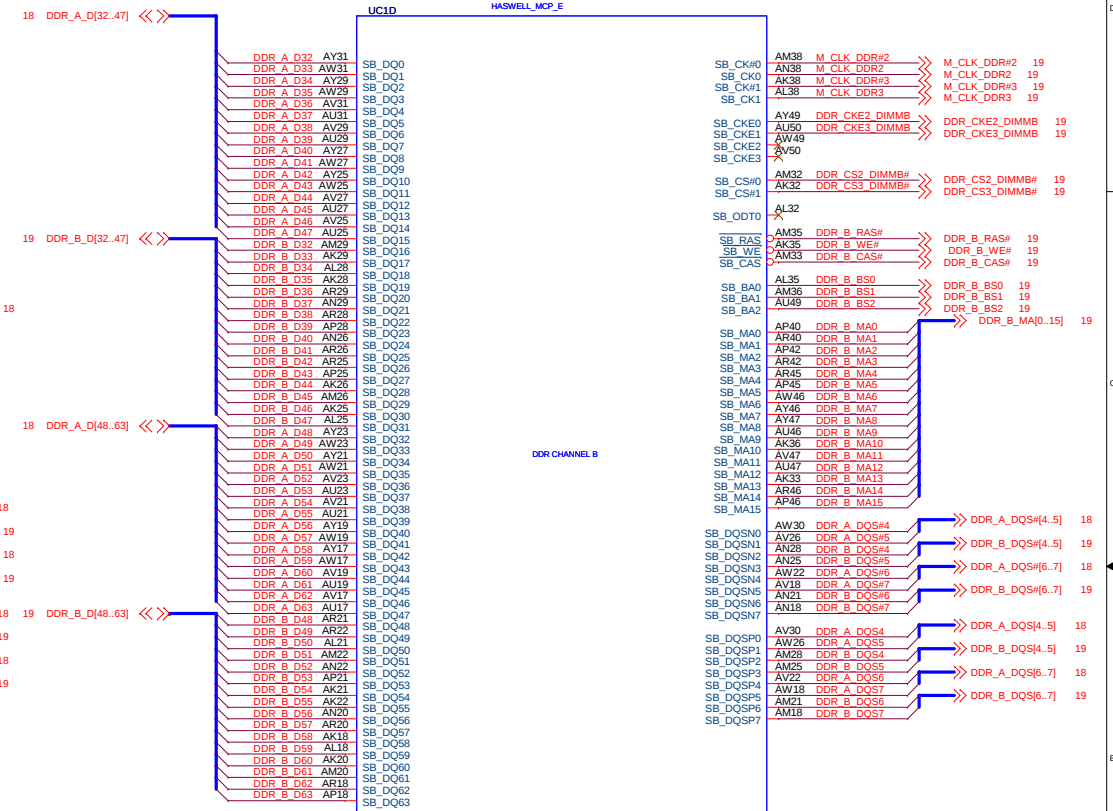
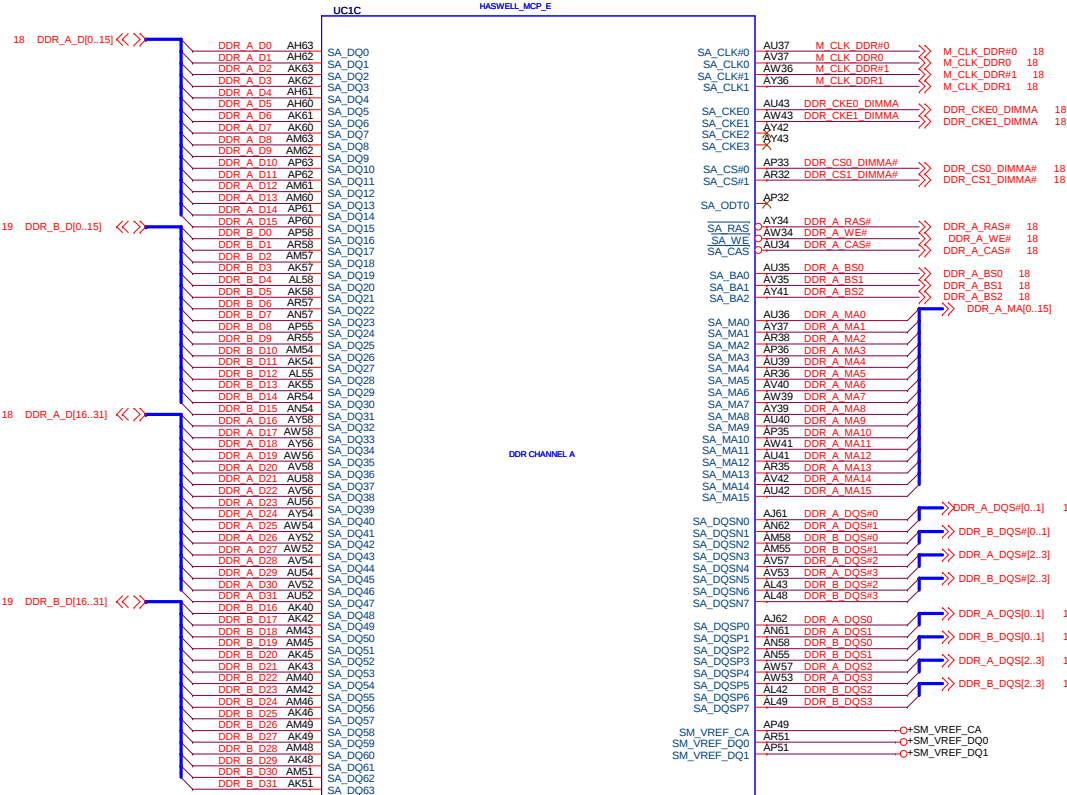


MEC 5075

SMBUS Address [0x2c]

SMBUS Address [0x9e]





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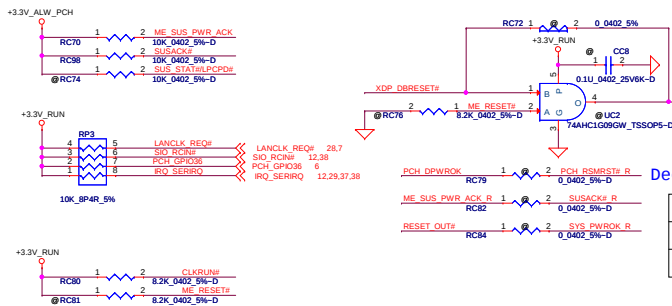
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MCP(3/12) DDR3

LA-9832P

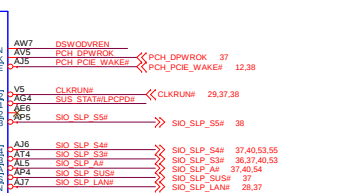
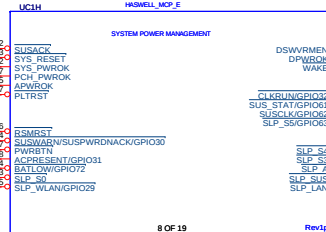
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Date: Thursday, June 13, 2013 Sheet 8 of 64

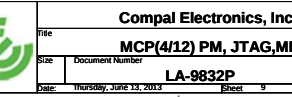
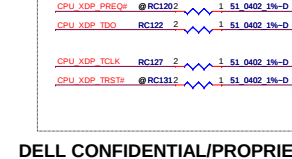
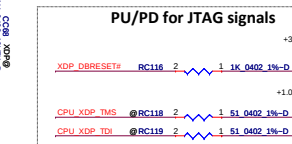
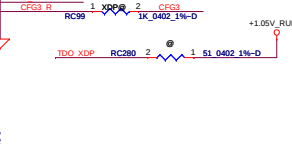
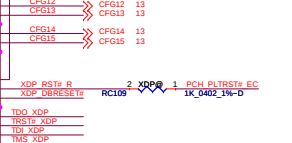
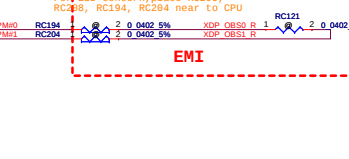
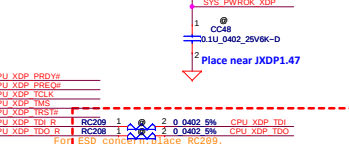
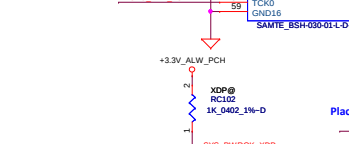
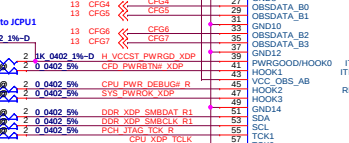
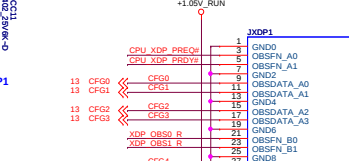
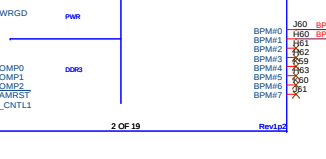
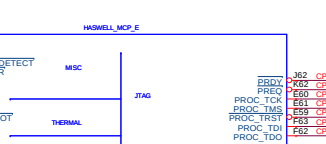
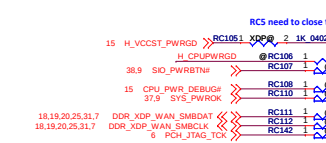
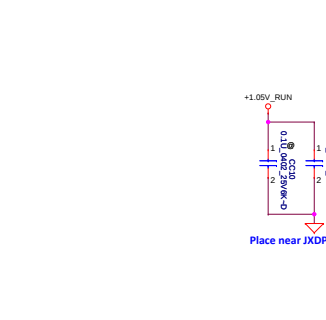
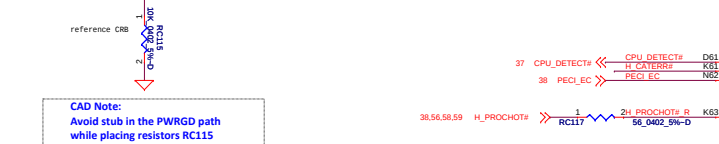
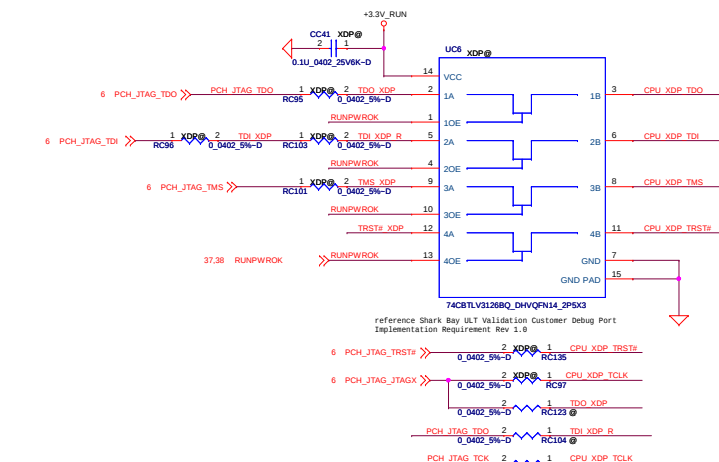
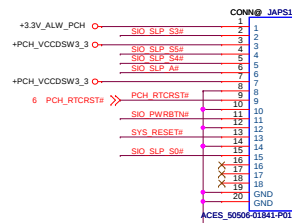


DeepSleep and Non-DeepSleep config:

Config	DSx	Non-DSx
Pop	RC86, R319, RC267	RC79, RC82, RC265
Depop	RC79, RC82, RC265	RC86, R319, RC267



DSWDDVREN - ON THE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED



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MCP(4/12) PM, JTAG,MISC

LA-9832P

Rev 0.5

Date: Thursday, June 13, 2013

Sheet 9 of 64

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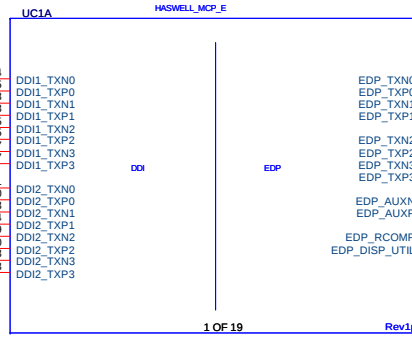


Intel check list has updated correctly

DP HUB <-----

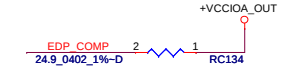
HDMI <-----

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21	DDI1_LANE_P0	<<<	DDI1_LANE_P0	C55	DDI1_TXP0
21	DDI1_LANE_N1	<<<	DDI1_LANE_N1	B58	DDI1_TXN1
21	DDI1_LANE_P1	<<<	DDI1_LANE_P1	C58	DDI1_TXP1
21	DDI1_LANE_N2	<<<	DDI1_LANE_N2	B55	DDI1_TXN2
21	DDI1_LANE_P2	<<<	DDI1_LANE_P2	A55	DDI1_TXP2
21	DDI1_LANE_N3	<<<	DDI1_LANE_N3	A57	DDI1_TXN3
21	DDI1_LANE_P3	<<<	DDI1_LANE_P3	B57	DDI1_TXP3
23	TMDS_N2	<<<	TMDS_N2	C51	DDI2_TXN0
23	TMDS_P2	<<<	TMDS_P2	C50	DDI2_TXP0
23	TMDS_N1	<<<	TMDS_N1	C53	DDI2_TXN1
23	TMDS_P1	<<<	TMDS_P1	B54	DDI2_TXP1
23	TMDS_N0	<<<	TMDS_N0	C49	DDI2_TXN2
23	TMDS_P0	<<<	TMDS_P0	B50	DDI2_TXP2
23	TMDS_CLK#	<<<	TMDS_CLK#	A53	DDI2_TXN3
23	TMDS_CLK	<<<	TMDS_CLK	B53	DDI2_TXP3

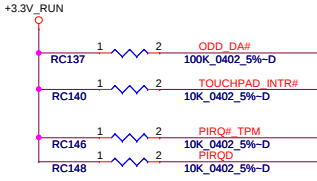


COMPENSATION PU FOR eDP

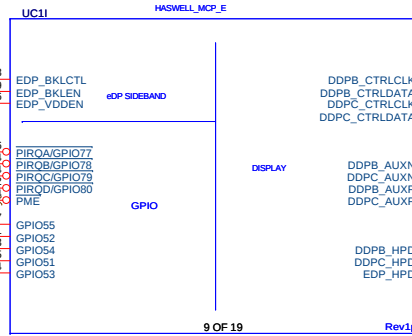
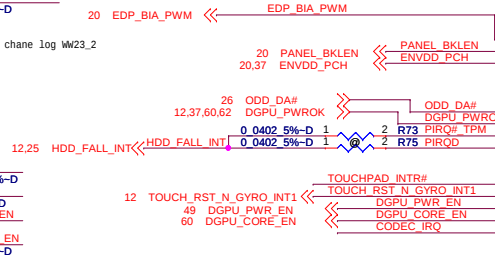
follow intel feedback



CAD Note: Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

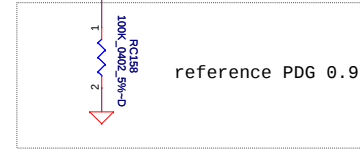
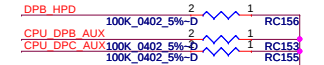
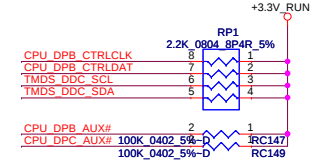


reference 0.55 design chane log W23_2



Intel WW18 Strapping option

Intel WW18 Strapping option

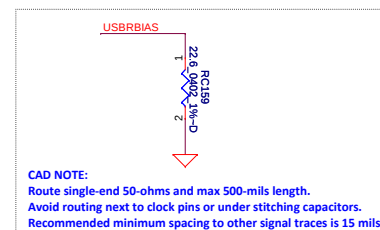
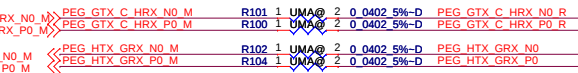


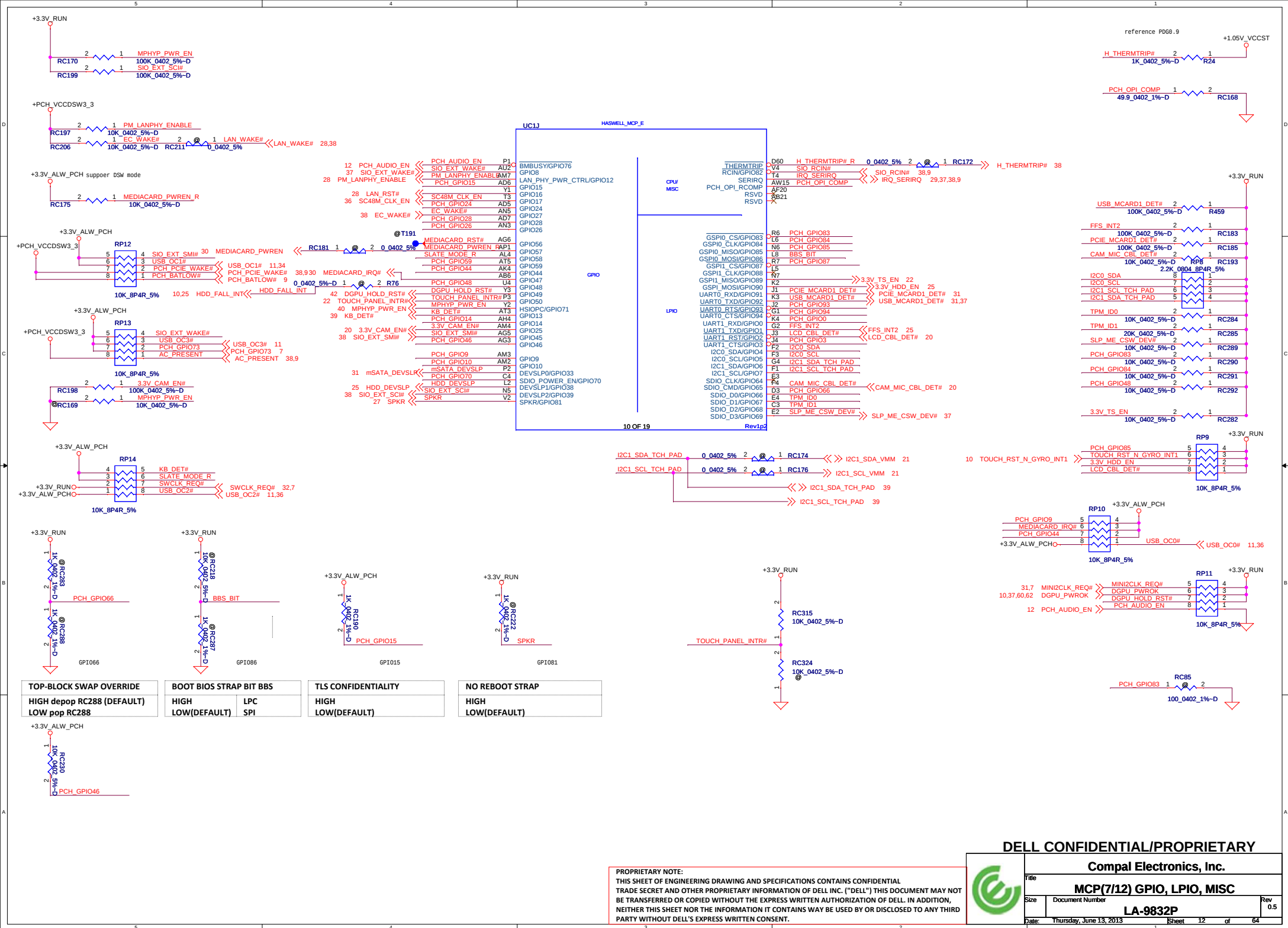
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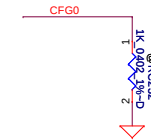
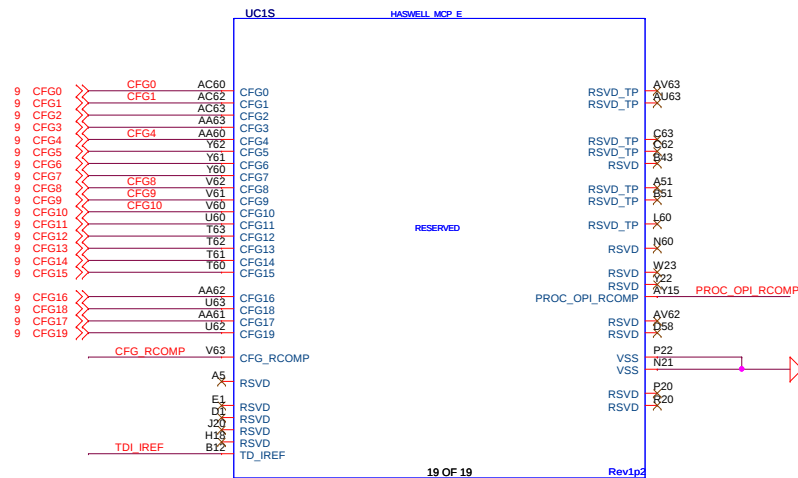
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Size	Document Number	LA-9832P	Rev 0.5
Date	Thursday, June 13, 2013	Sheet 10	of 64

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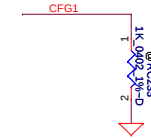




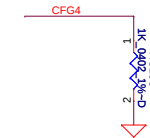
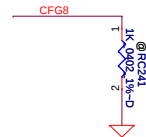
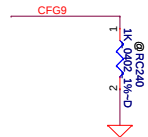
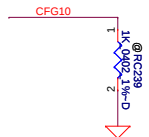
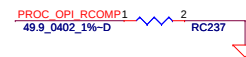
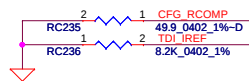
CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed



PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed



SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available peggardless of the locking of the unit

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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MCP(8/12) CFG, RSVD

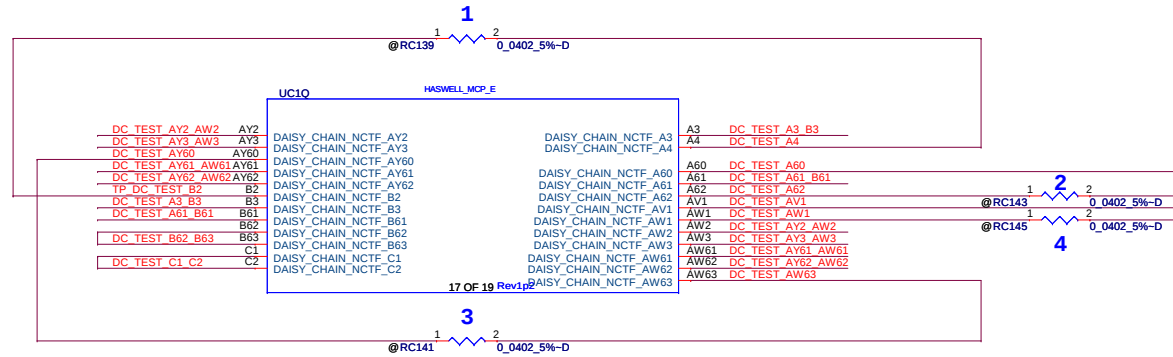
LA-9832P

Rev	
0.5	

LA-9832P

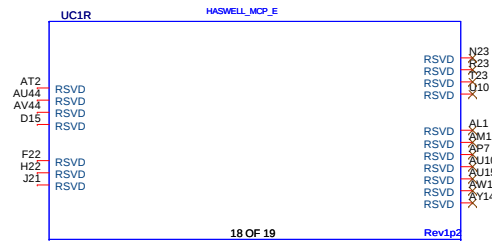
Date: Thursday, June 12, 2013 Page: 13 of 64

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Package Daisy Chain:

1. B2 - PKG - C1 - PCB - C2 - PKG - B3 - PCB - A3 - PKG - A4
2. A62 - PKG - A61 - PCB - B61 - PKG - B62 - PCB - B63 - PKG - A60
3. AY60 - PKG - AW61 - PCB - AY61 - PKG - AW62 - PCB - AY62 - PKG - AW63
4. AW1 - PKG - AW3 - PCB - AY3 - PKG - AW2 - PCB - AY2 - PKG - AV1



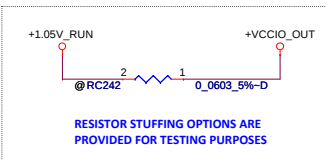
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Title		MCP(9/12) TP,RSVD	
Size	Document Number	LA-9832P	Rev 0.5
Date:	Thursday, June 13, 2013	Sheet 14	of 64



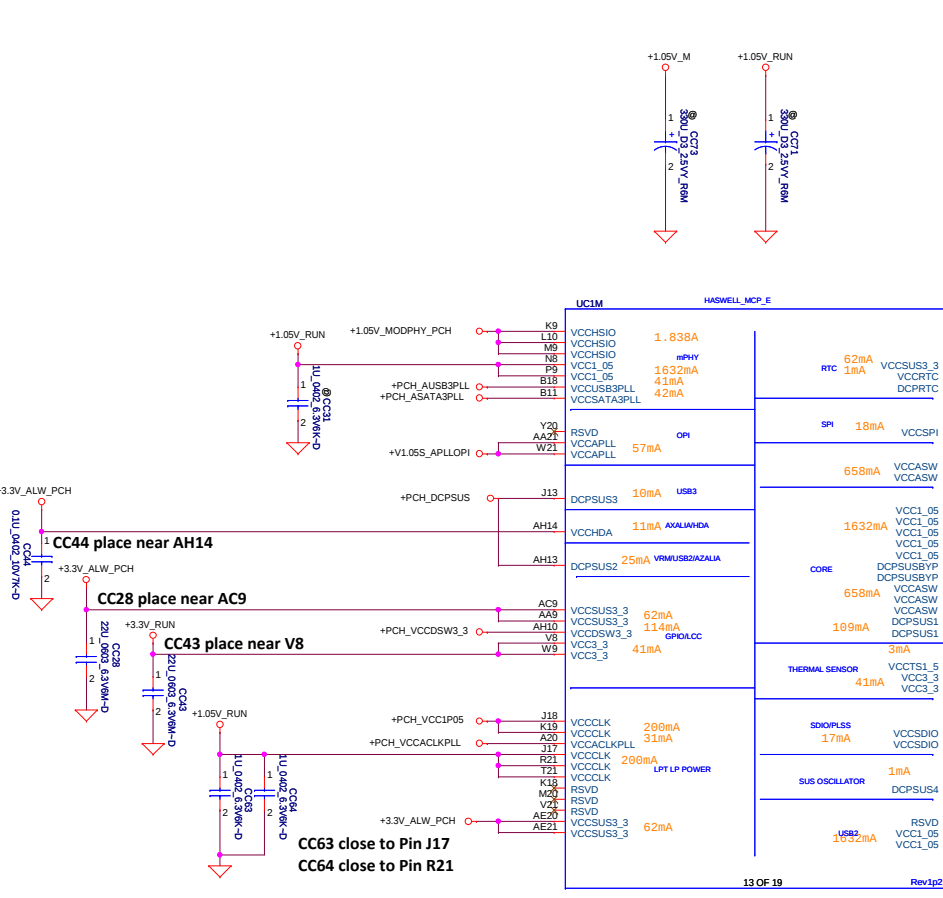
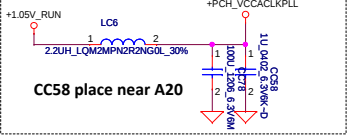
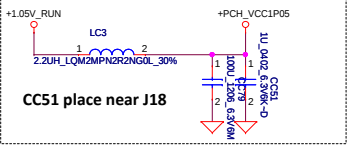
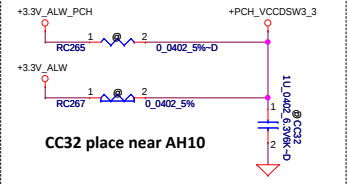
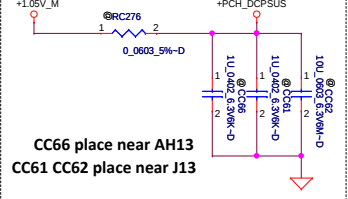
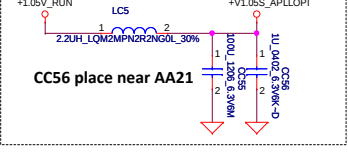
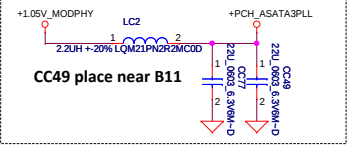
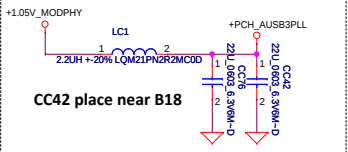
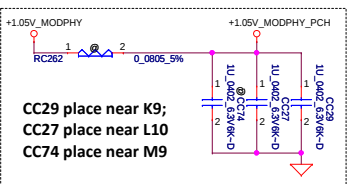
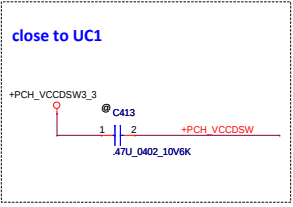
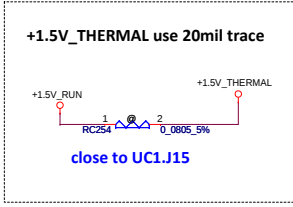


Table 6-3. Pre-Si I_{CC} max Estimates

Voltage Rail	Voltage (V)	S0 I _{CC} max Current (A) ¹	Sx I _{CC} max Current (A) ²	Deep Sx I _{CC} max (A) ³	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCDHA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1 ⁴	1.05	0.109	0.014	0	0
DcpSus2 ⁴	1.05	0.025	0.001	0	0
DcpSus3 ⁴	1.05	0.010	0.003	0	0
DcpSus4 ⁴	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 μA See notes 1, 2



DeepSleep and Non-DeepSleep config:

Config	DSx	Non-DSx
Pop	RC86, R319, RC267	RC79, RC82, RC265
Depop	RC79, RC82, RC265	RC86, R319, RC267

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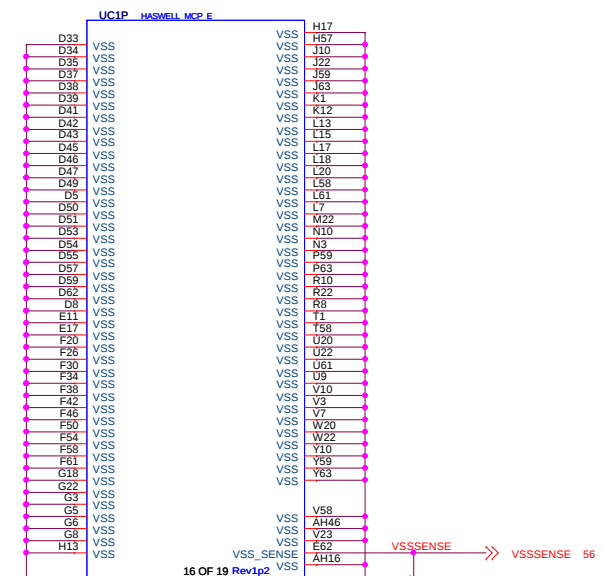
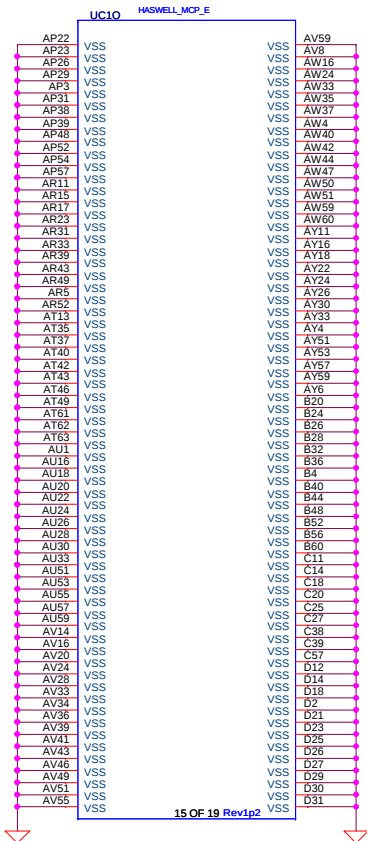
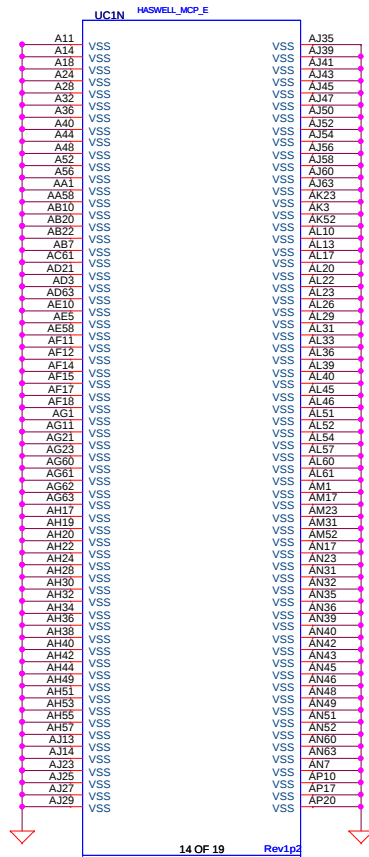
MCP(11/12) Power

LA-9832P

Rev 0.5

Friday, August 30, 2013

Sheet 16 of 64



CAD Note: RC260 SHOULD BE PLACED CLOSE TO CPU

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MCP(12/12) VSS			
Size	Document Number	Rev	0.5
LA-9832P			
Date:	Thursday, June 13, 2013	Sheet	17 of 64

2-3A to 1 DIMMs/channel

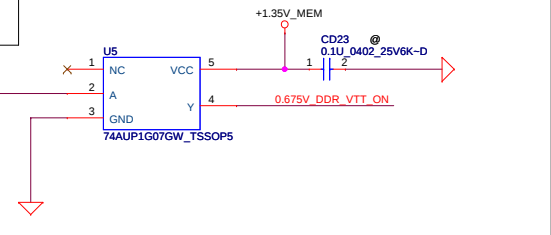
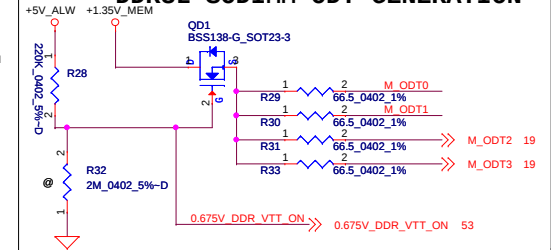
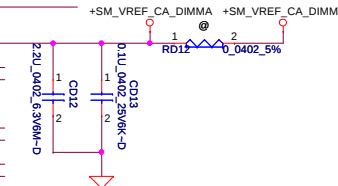
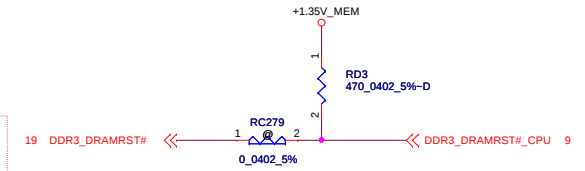
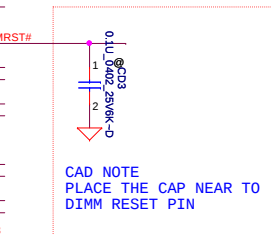
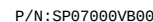
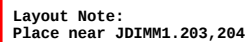


```

8 DDR_A_DQS#[0..7] <<>>
8 DDR_A_D[0..63] <<>>
8 DDR_A_DQS[0..7] <<>>
8 DDR_A_MA[0..15] >>

```

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



0.5

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Title			
DDRIII DIMM1			
Size	Document Number		Rev
	LA-9832P		0.5
Date:	Thursday, June 13, 2013	Sheet 18 of	64

JDIMM2 H=4mm 2-3A to 1 DIMMs/channel

Reverse Type

CAD NOTE
PLACE THE CAP NEAR TO
DIMM RESET PIN

Interleaved Memory

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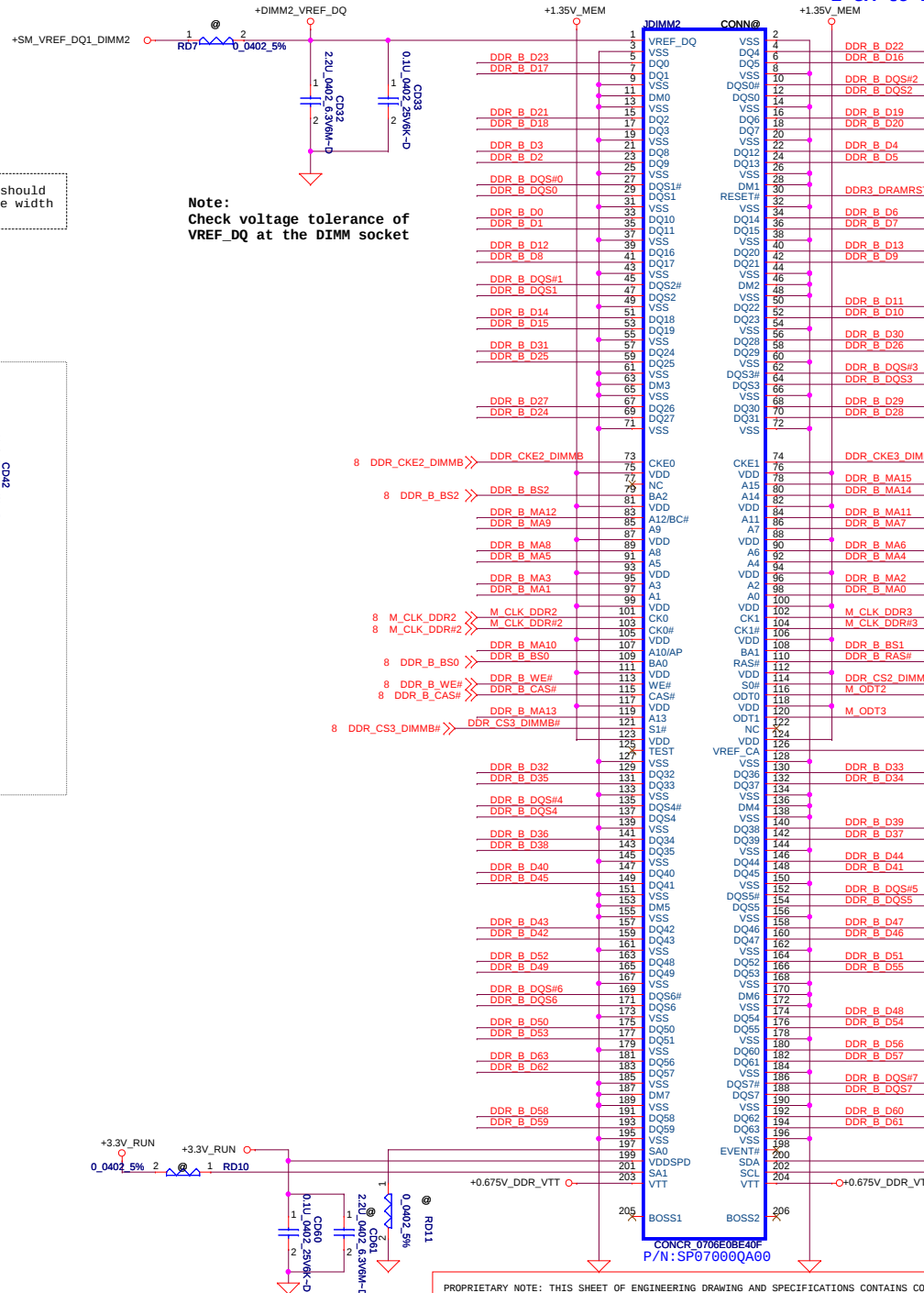
DDRIII DIMM2

LA-9832P

Rev 0.5

Date: Thursday, June 13, 2013 Sheet 19 of 64

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Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

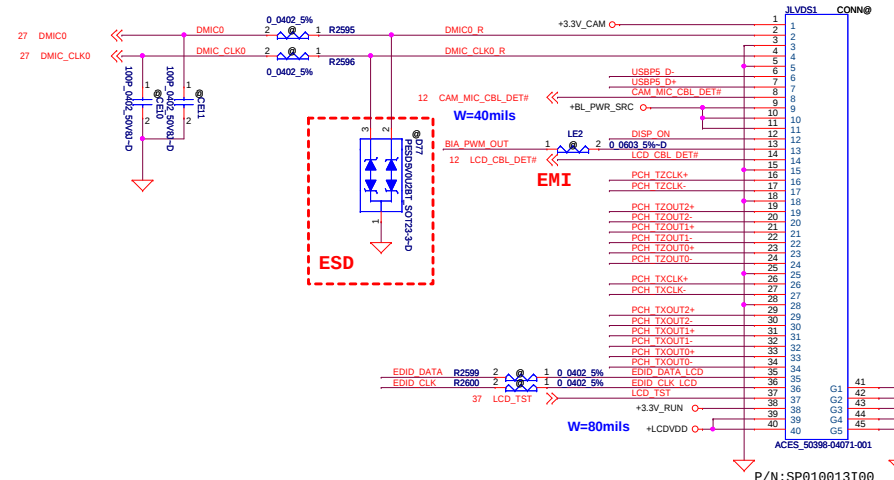
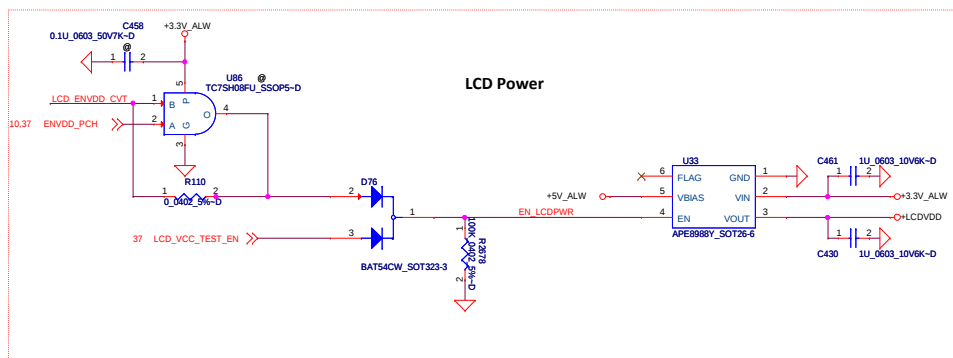
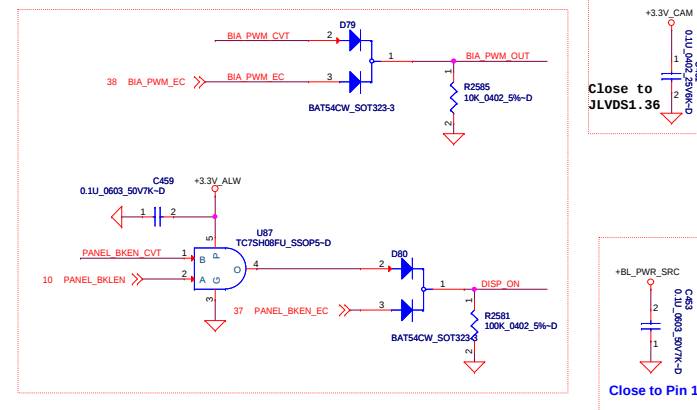
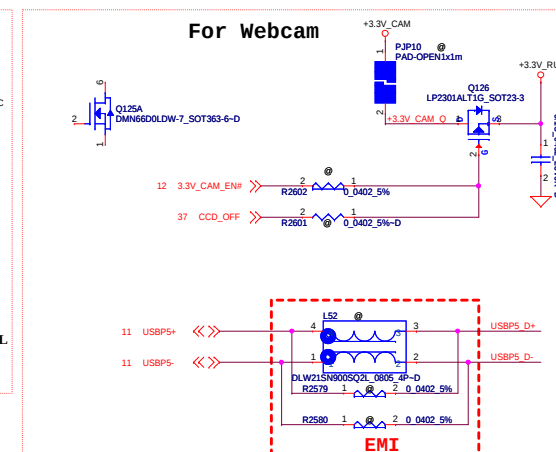
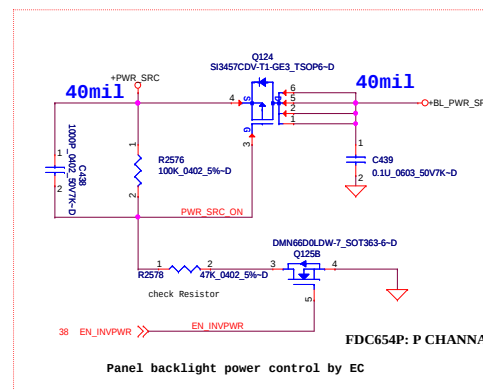
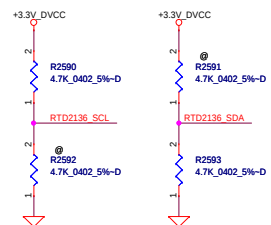
Layout Note:
Place near JDIMM2

Layout Note:
Place near JDIMM2.203,204



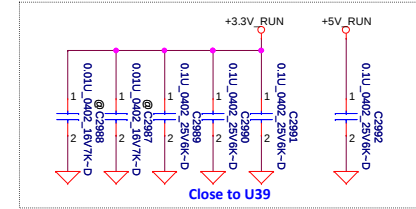
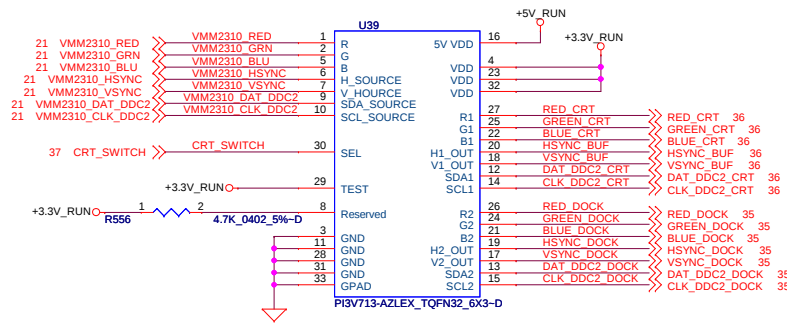


Pin 47 Pin 48	0	1
0	X	EP Mode
1	Internal ROM only	EEPROM

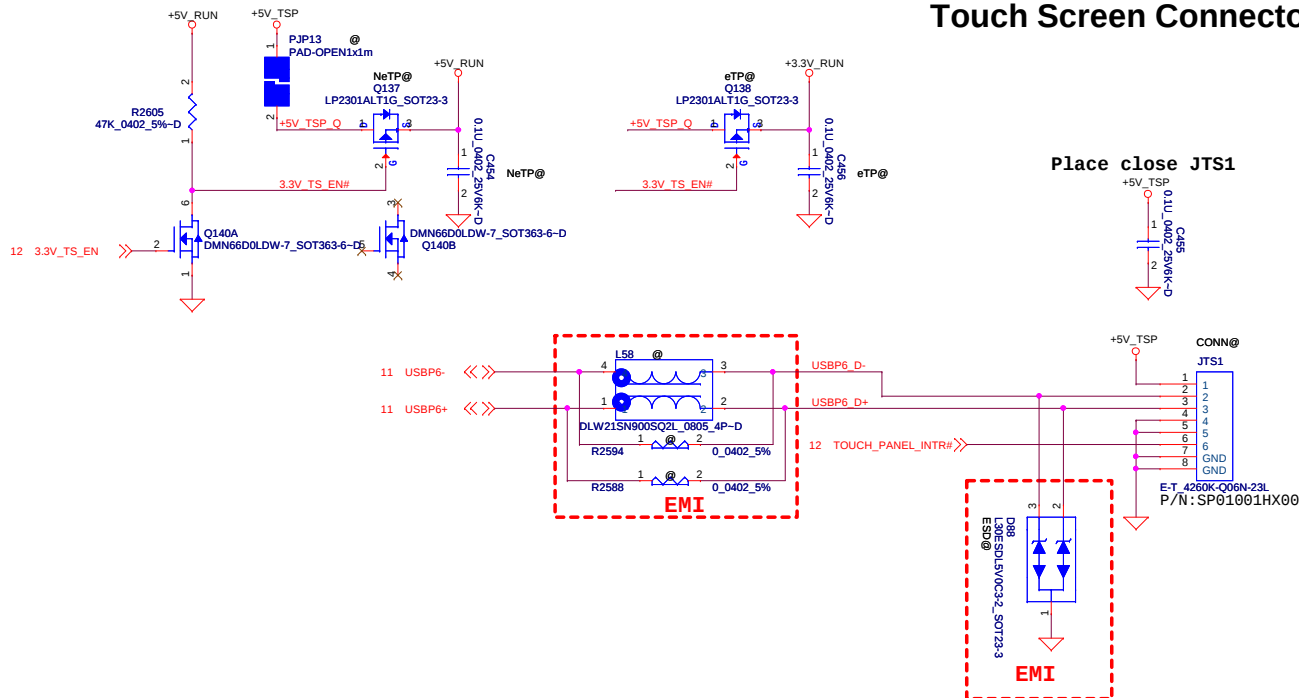


CRT SW for MB/DOCK

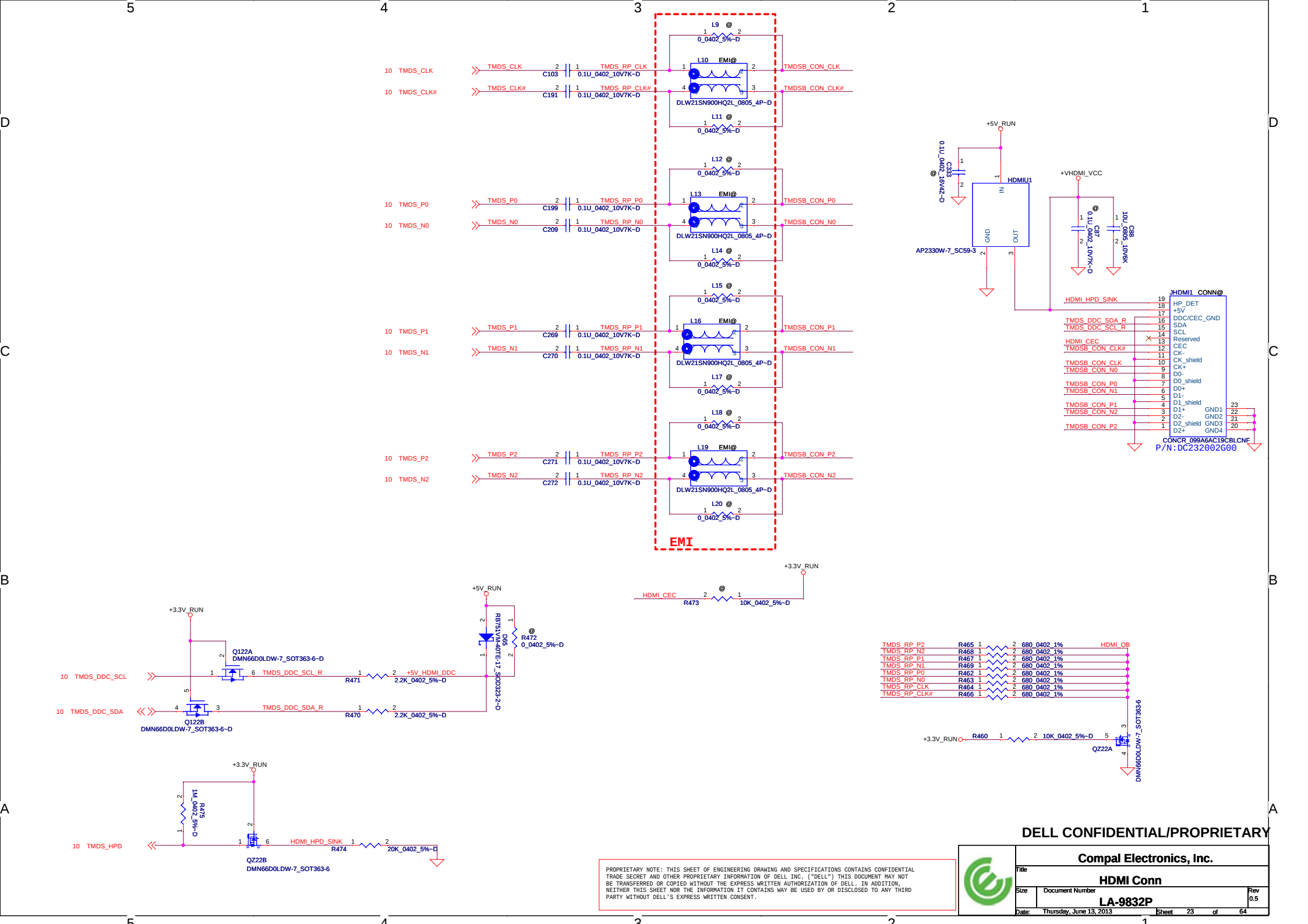
SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



Touch Screen Connector



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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Date:	Thursday, June 13, 2013	Sheet	22	of	64



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HDMI Conn

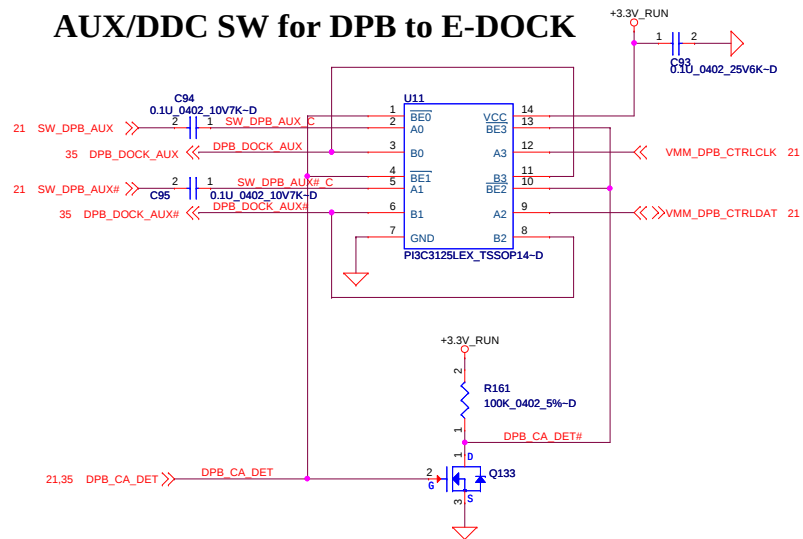
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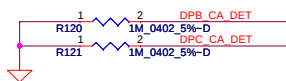
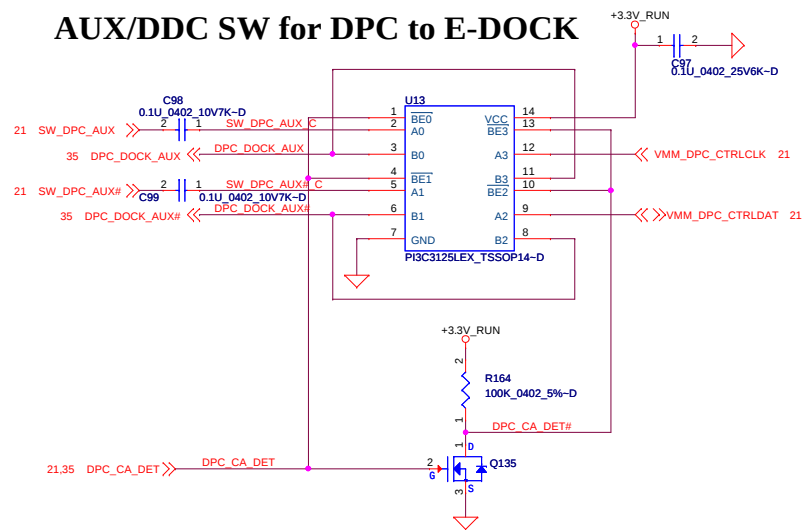
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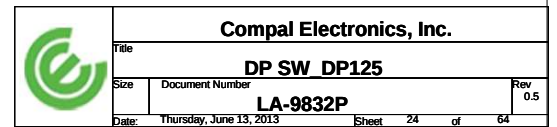
AUX/DDC SW for DPB to E-DOCK



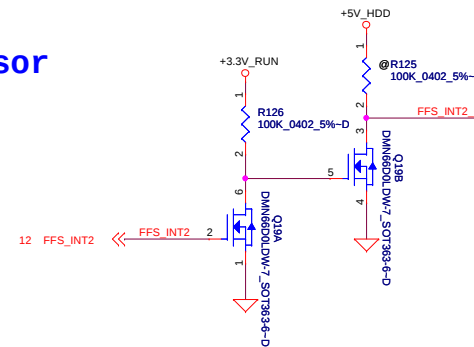
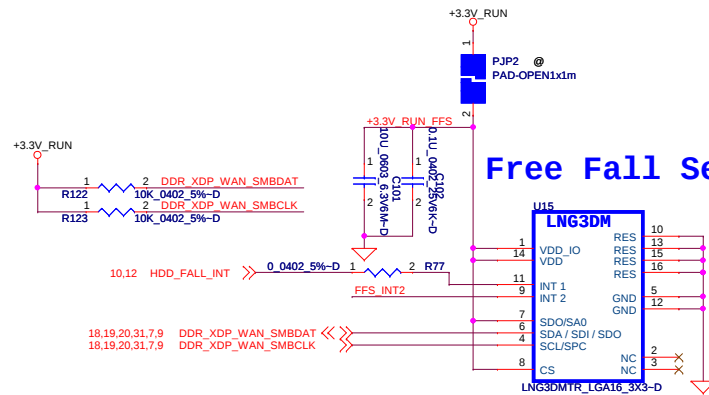
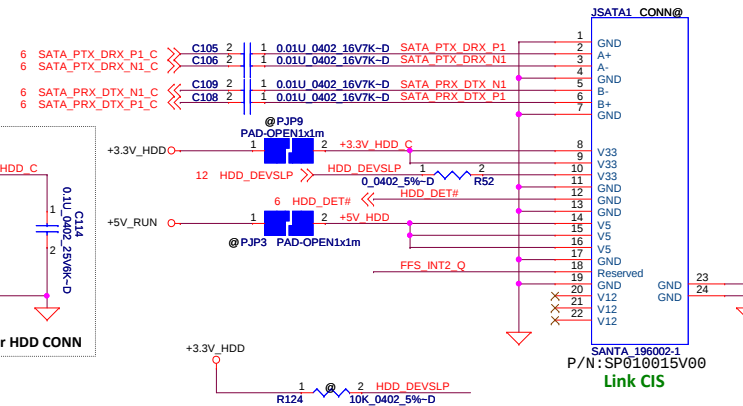
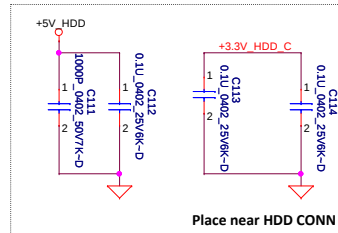
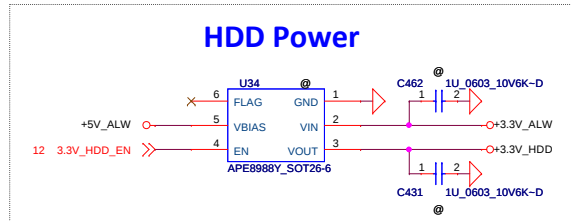
AUX/DDC SW for DPC to E-DOCK



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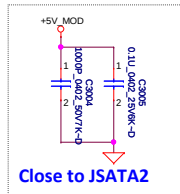
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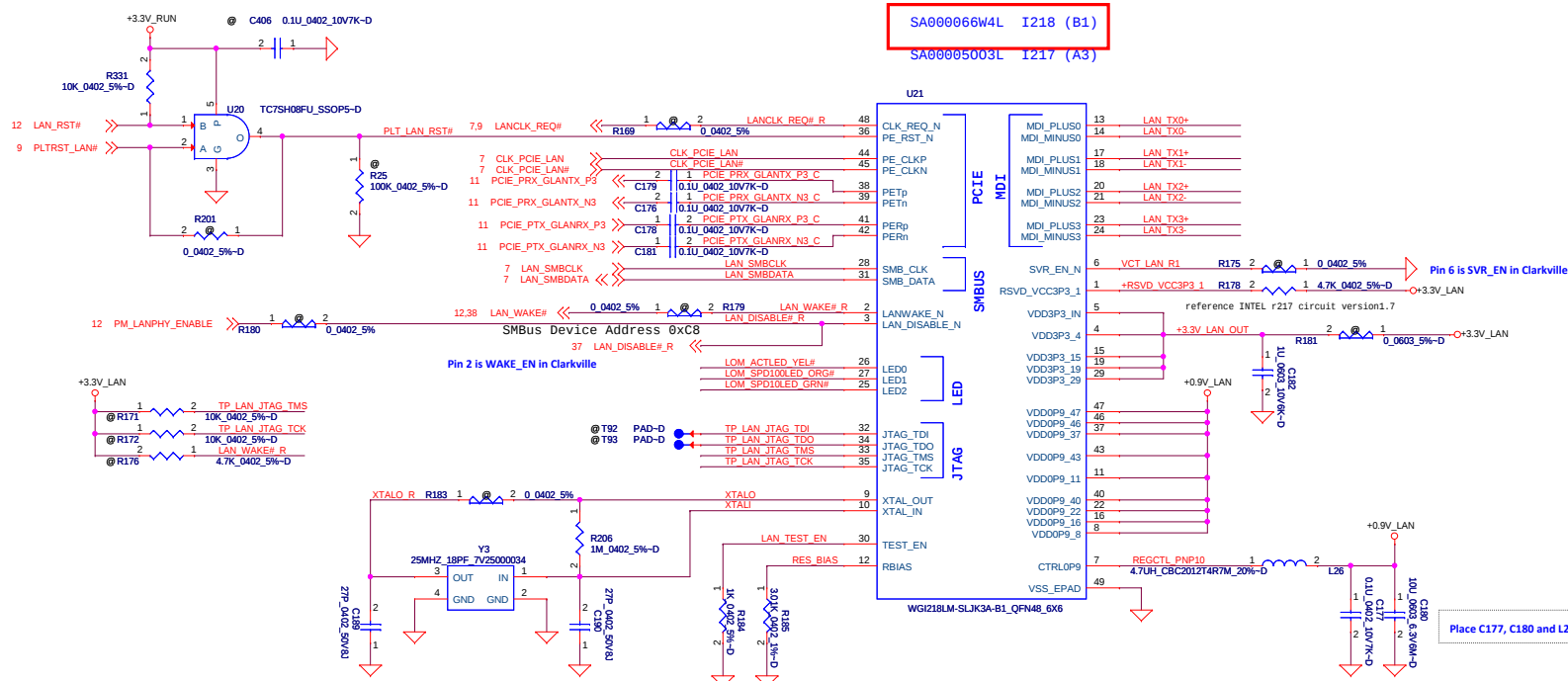
HDD CONN			Rev
Title	HDD CONN		0.5
Size	Document Number	LA-9832P	
Date	Thursday, June 13, 2013	Sheet	25 of 64

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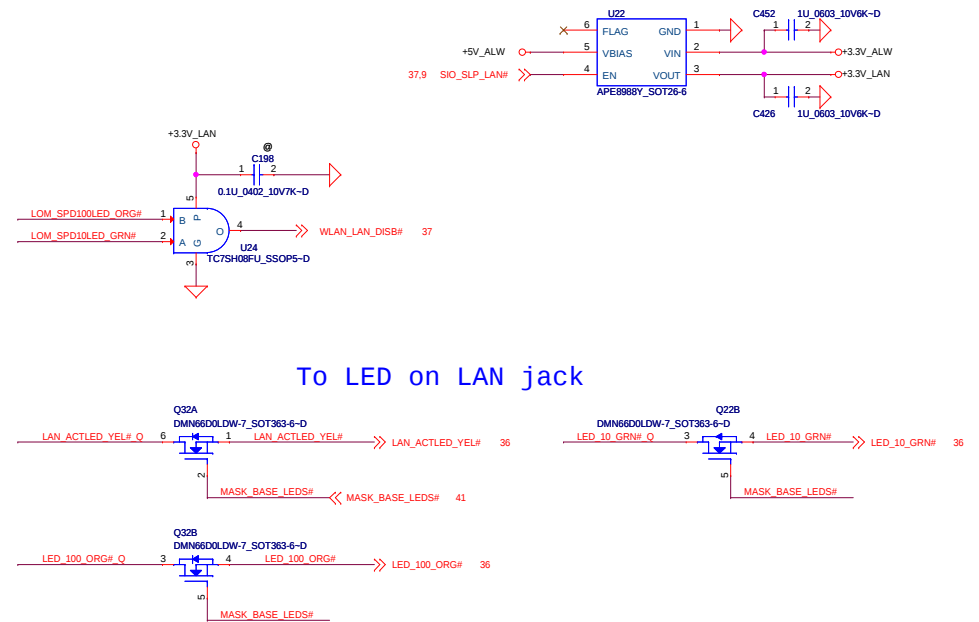
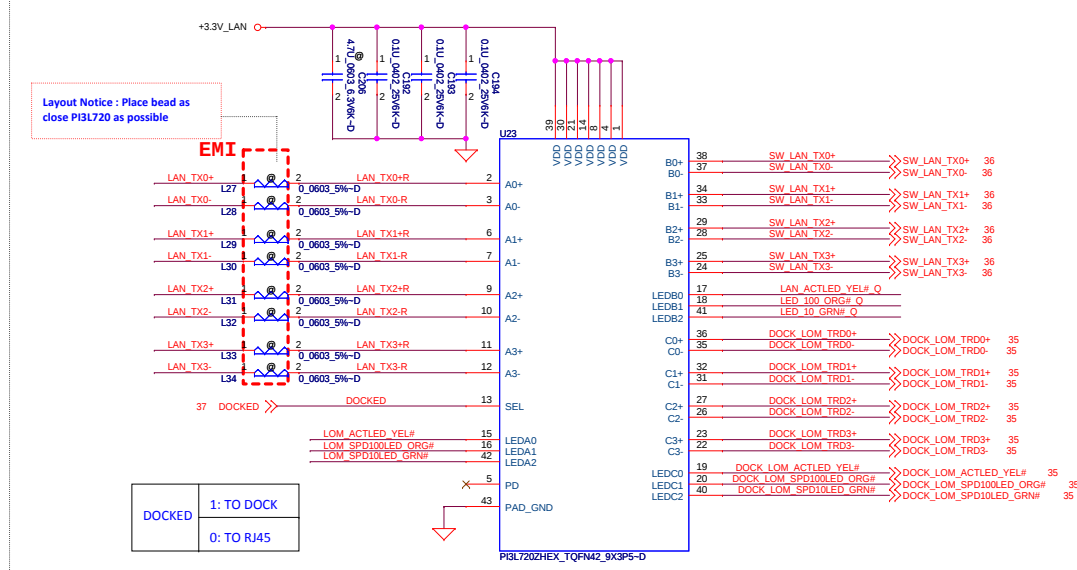
The schematic diagram illustrates the power and signal connections for the AP9888Y_S0T26 module. The module is connected to a +5V_ALW supply and a +5V_RUN supply. It includes components like U29 (AP9888Y_S0T26), C460 (1U_0603 10V6K-D), C432 (1U_0603 10V6K-D), and P49202 (PAD-OPEN1x1m).



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Date:	Thursday, June 13, 2013	Sheet	26 of 64



LAN ANALOG SWITCH



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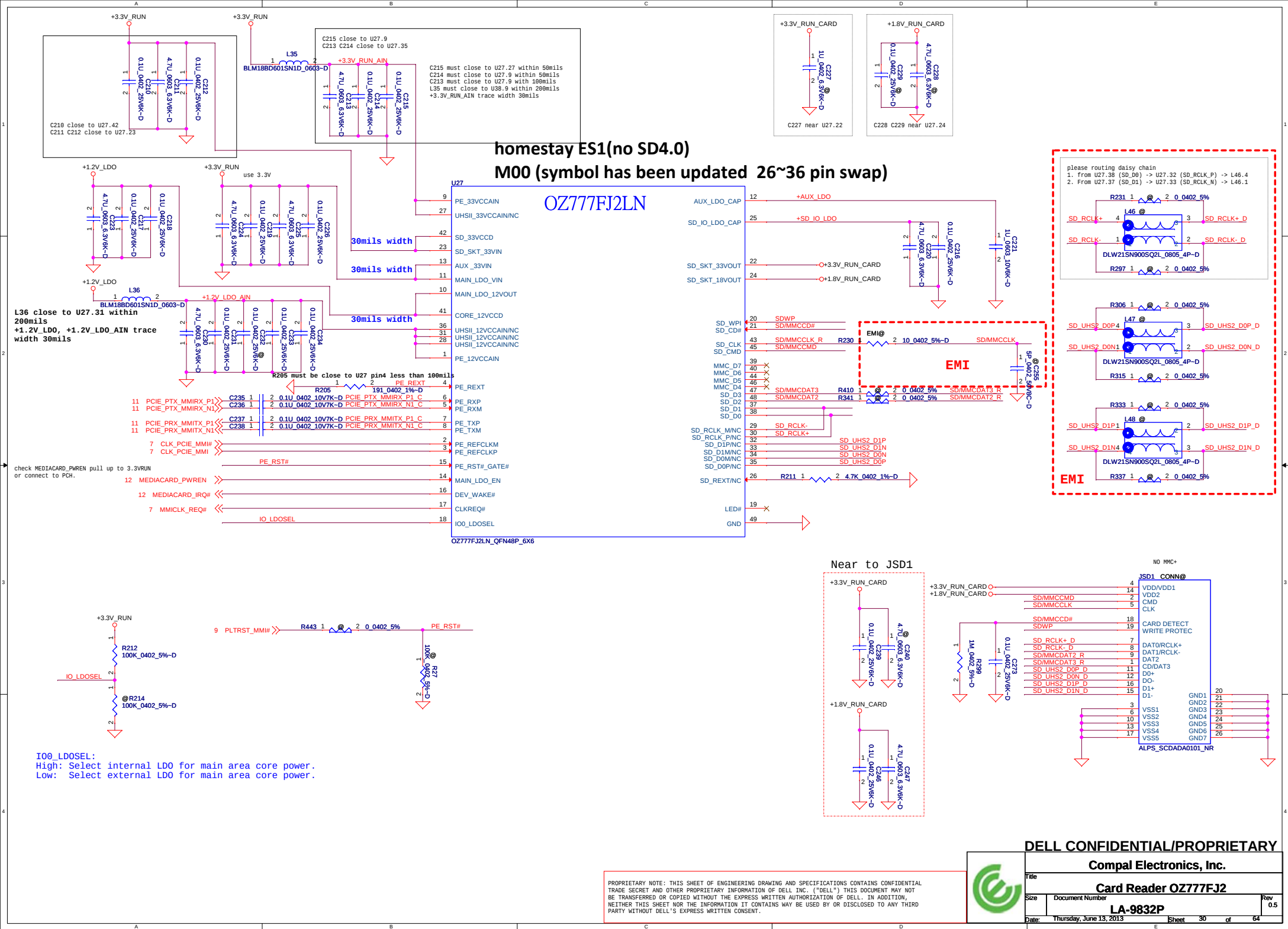


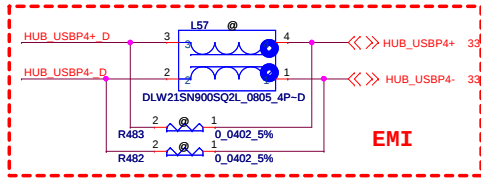
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LAN Lewisville / LAN SW			
Size Document Number			
LA-9832P			
Date: Tuesday, August 13, 2013			
Sheet 28 of 64			

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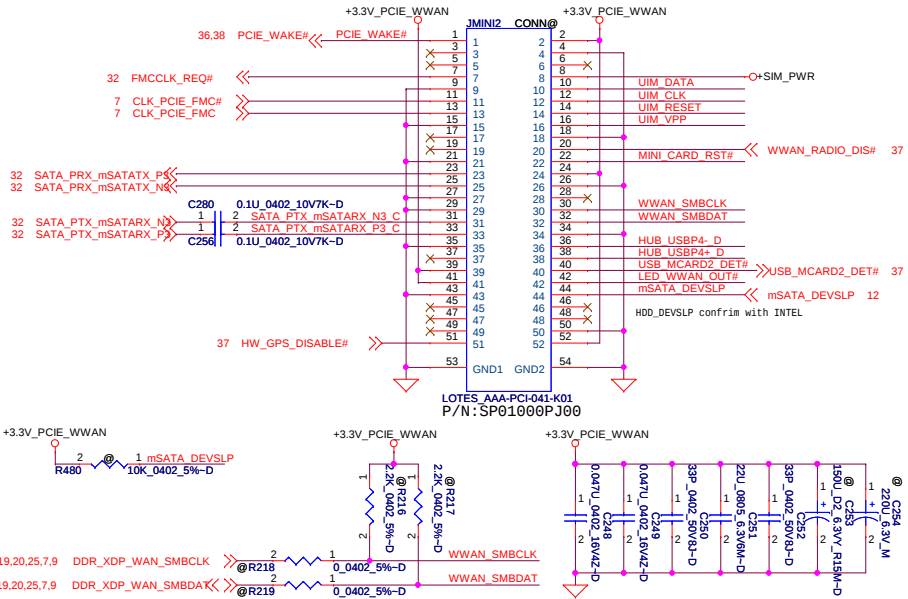


Title			
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Size	Document Number		Rev
	LA-9832P		0.5
Date:	Thursday, June 13, 2013	Sheet	29 of 64

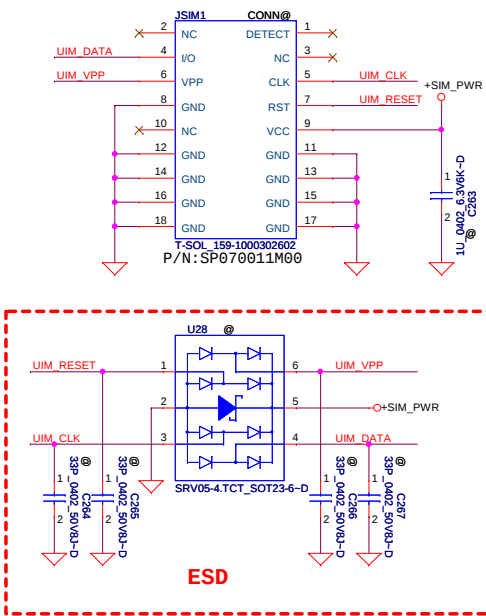




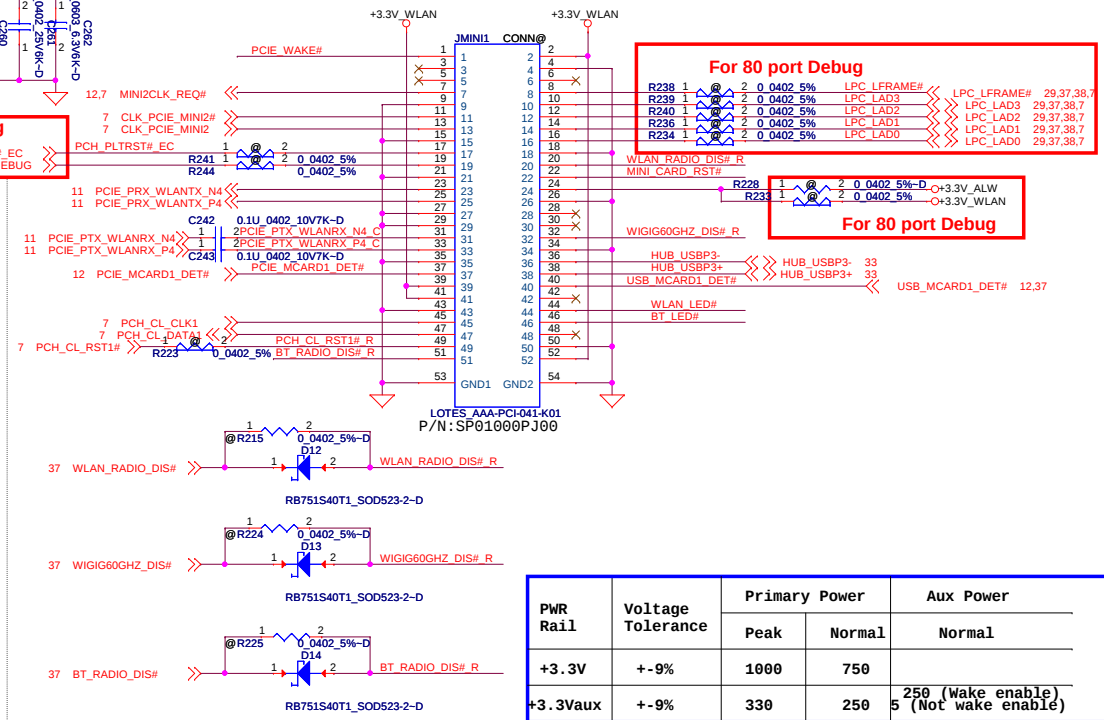
FMC: Mini WWAN/LTE H=8



uSIM Card Push-Push

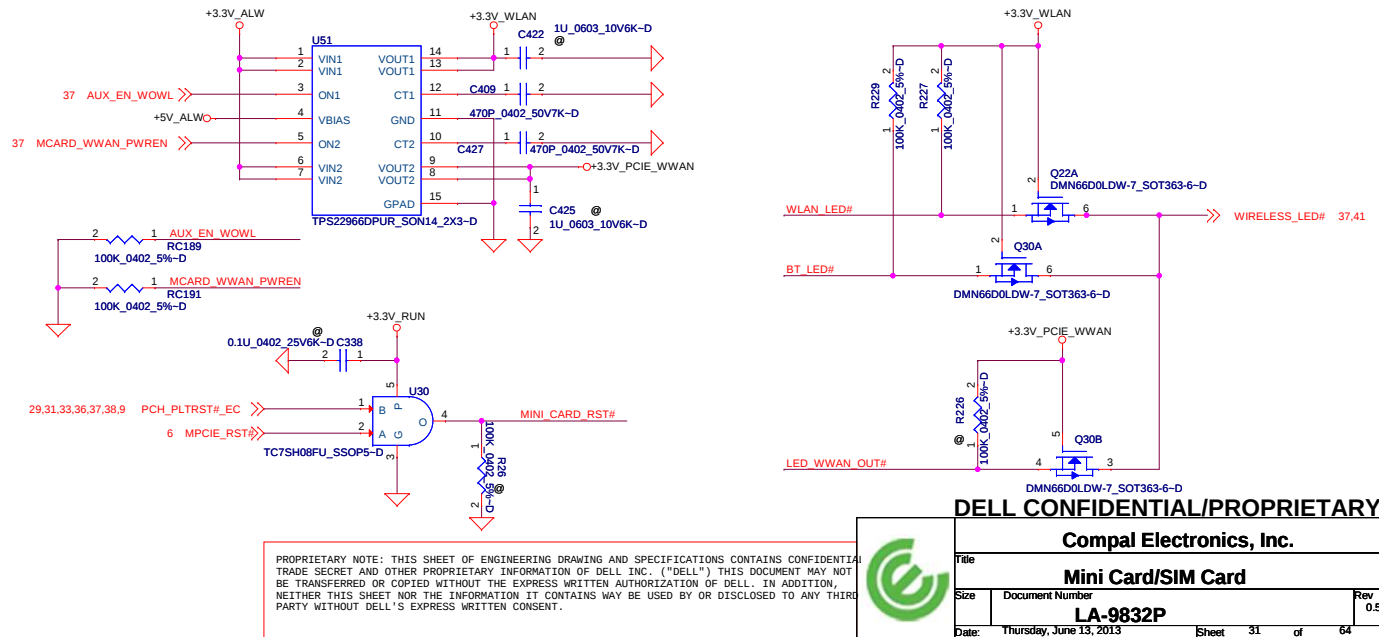


HMC: Mini WLAN/WiFi/BT H=4



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (wake enable) 5 (Not wake enable)

LED control circuit



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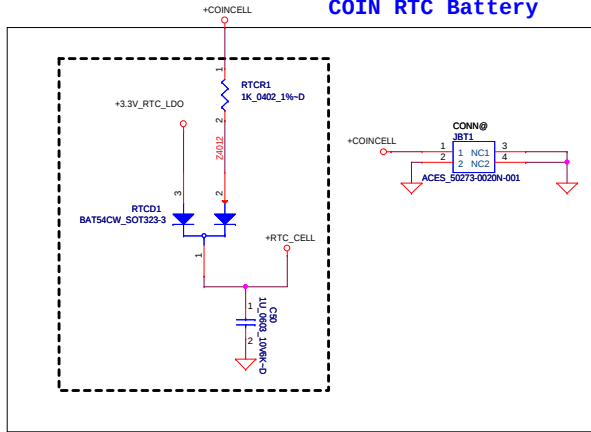
Mini Card/SIM Card

LA-9832P

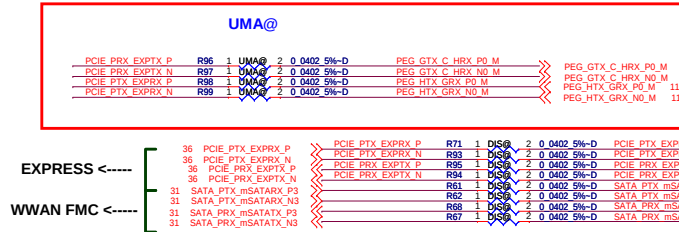
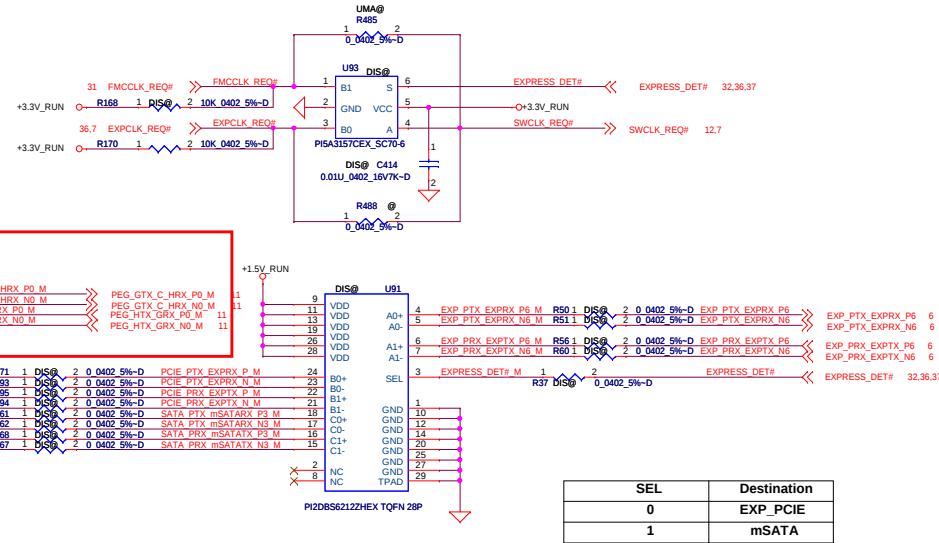
Date: Thursday, June 13, 2013 Sheet 31 of 64

EXP/FMC PCIe clock/REQ Switch

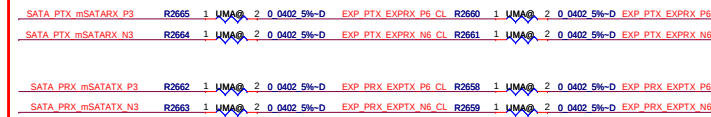
COIN RTC Battery



B \ S	EXPRESS_DET#
EXPCLK_REQ#	0
FMCLK_REQ#	1



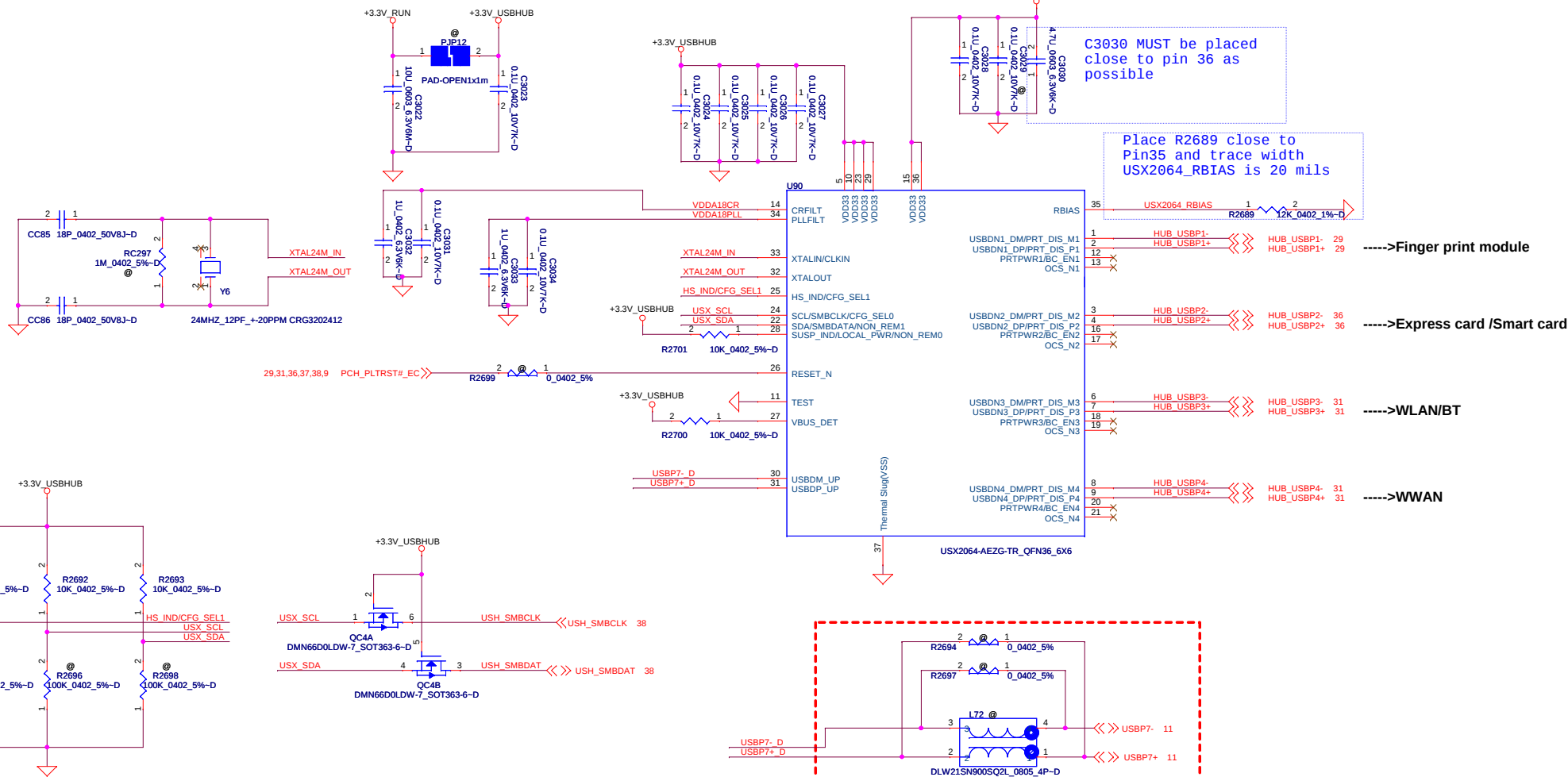
UMA@ Co-Layout with PI2DBS6212 PCIe/SATA SW



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Compal Electronics, Inc.	
RTC Batt/PCIE SATA SW	
Size	Document Number
LA-9832P	Rev 0.5
Date: Thursday, June 13, 2013	Sheet 32 of 64



USX2064 CFG Selection Table

CFG_SEL[0]	0	1
CFG_SEL[1]	Default	SMBus slave device
0	Default	I2C EEPROM
1	Bus-powered operation	I2C EEPROM

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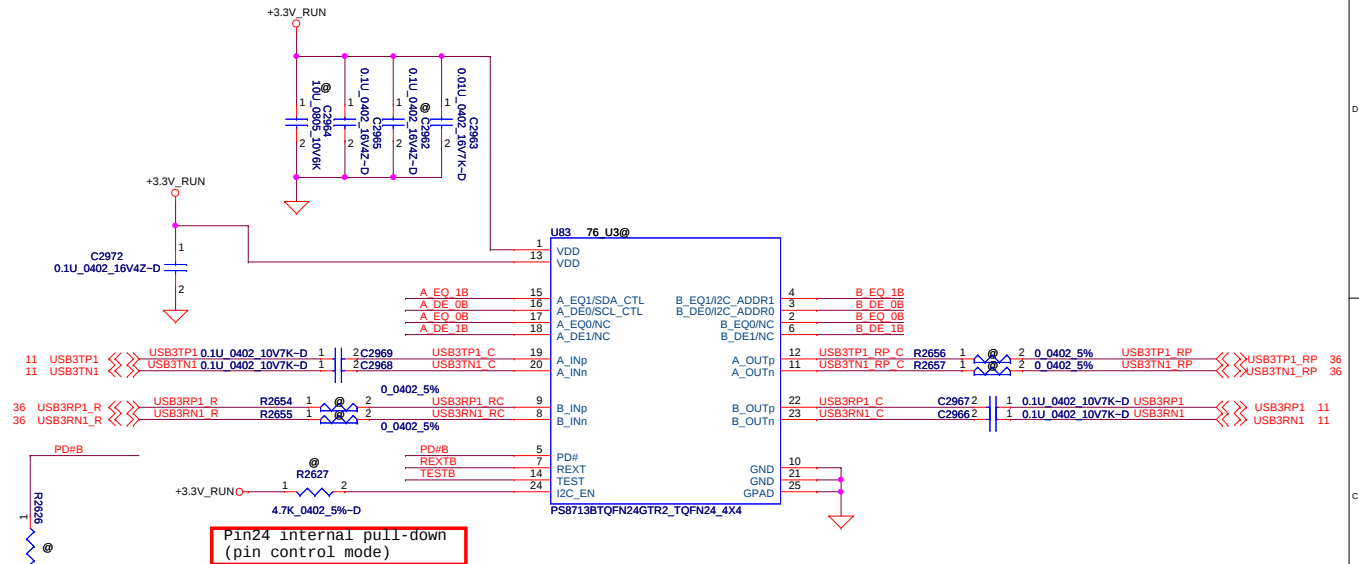
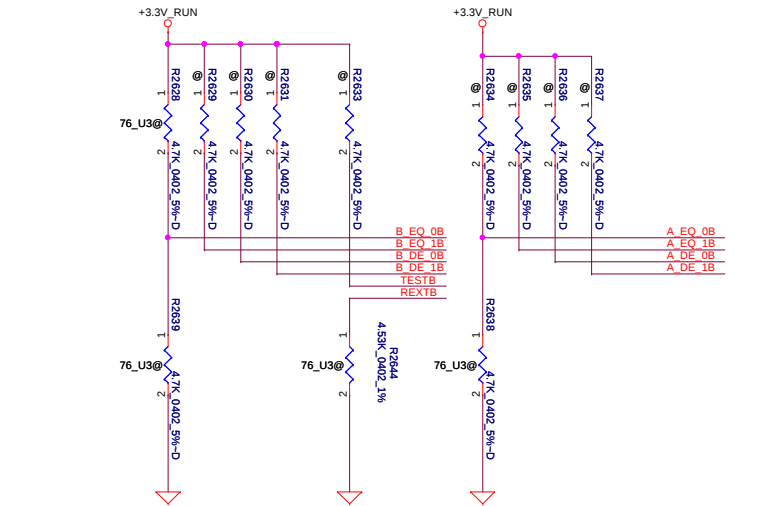
Compal Electronics, Inc.

USB2.0 HUB-USX2064

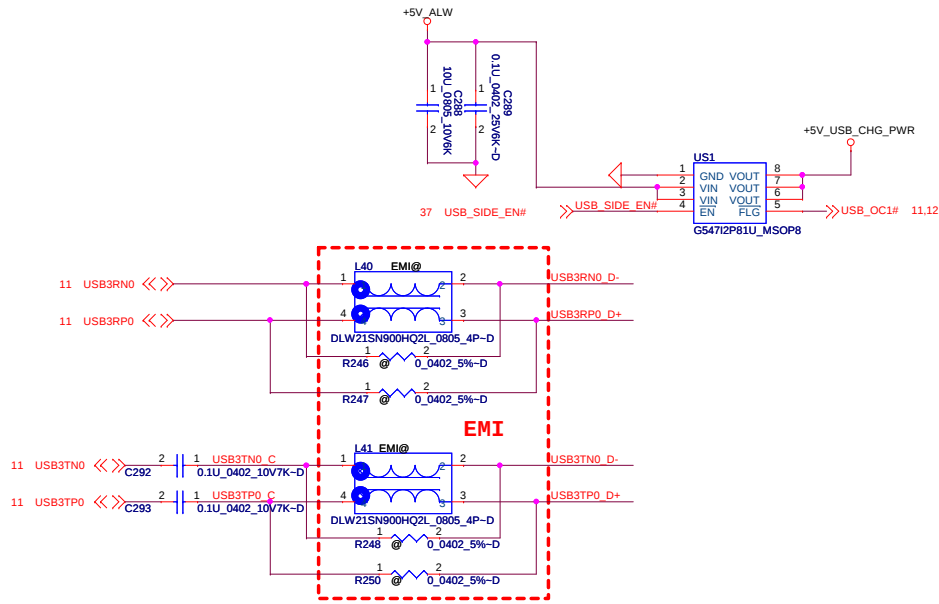
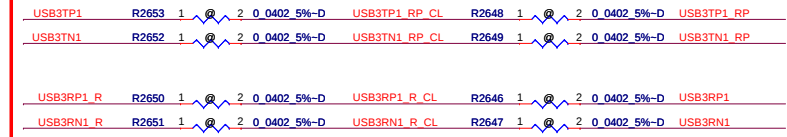
LA-9832P

Date: Monday, June 17, 2013 Sheet 33 of 64

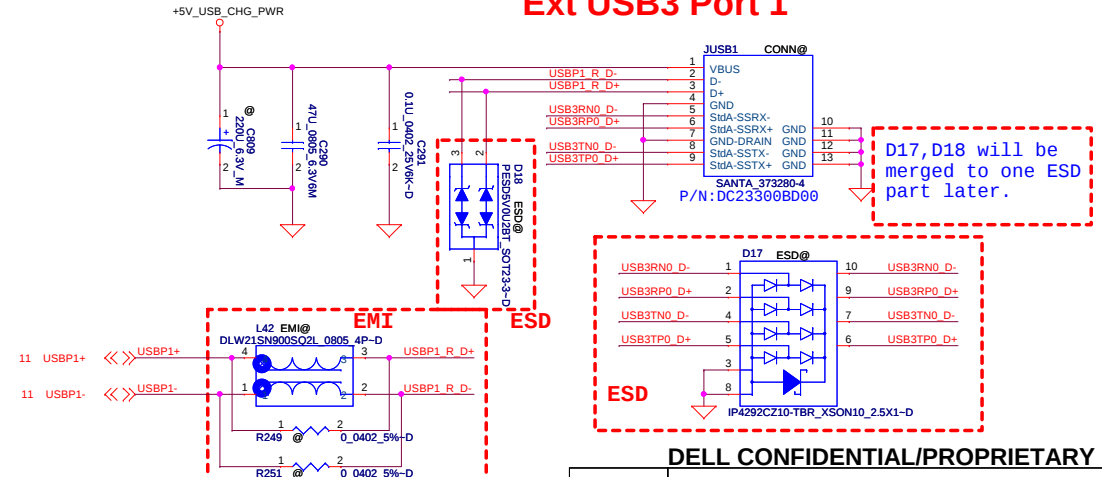
USB 3.0 Re-driver for IOB



Co-Layout with PS8713B USB3.0 re-driver



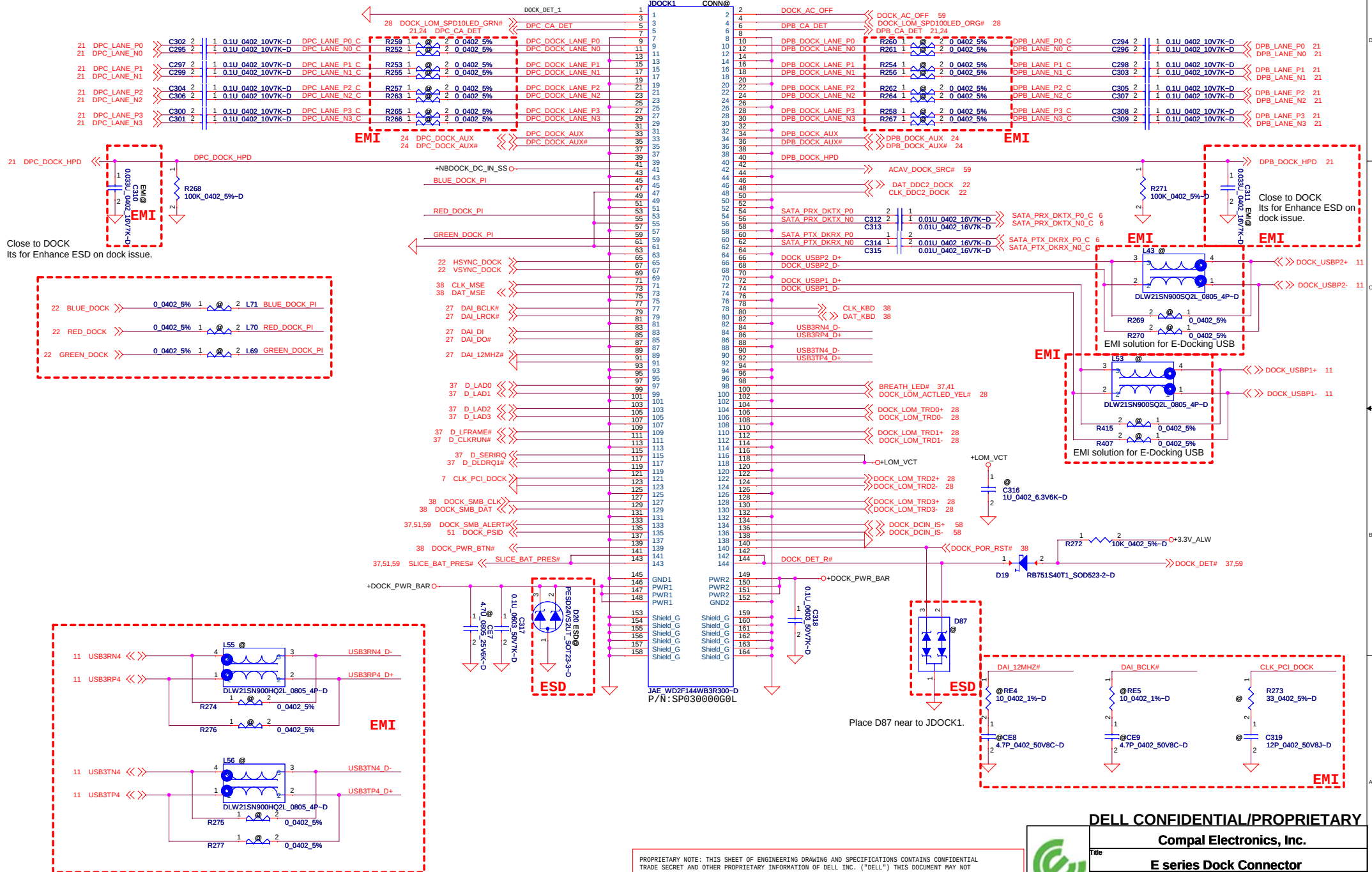
Ext USB3 Port 1



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USB on MB/Redriver			
LA-9832P	Rev 0.5		
Friday, August 30, 2013	Sheet 34	of 64	

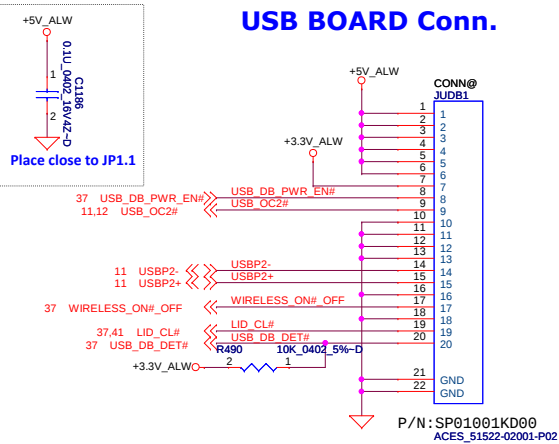
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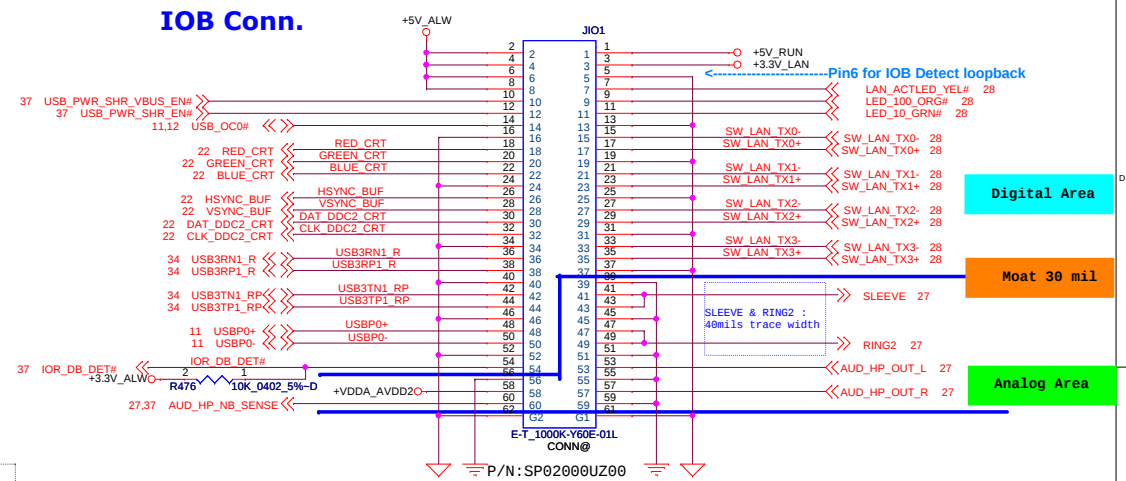
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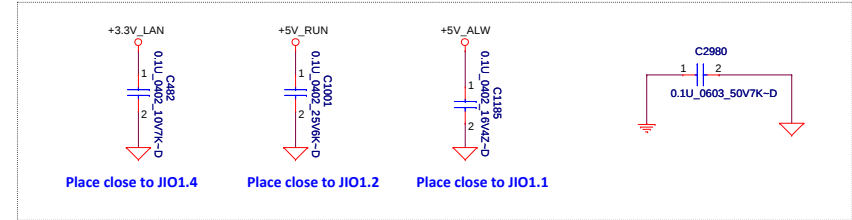
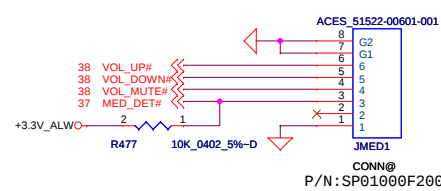
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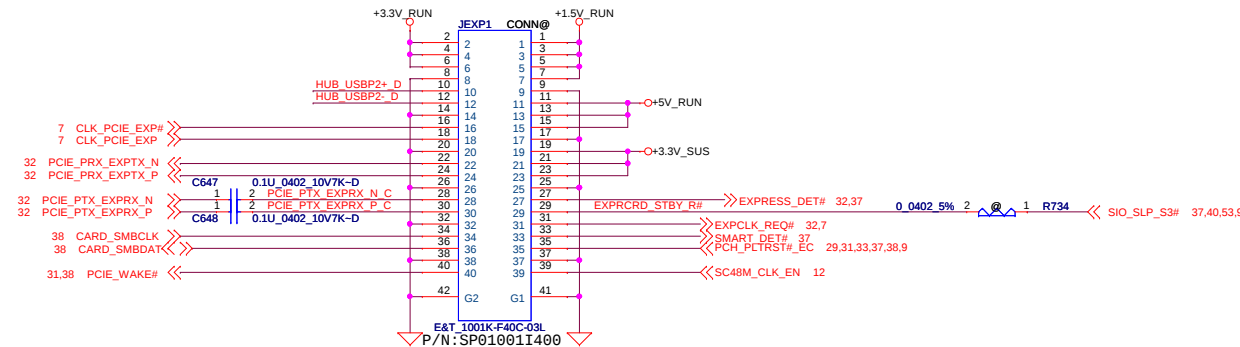
IOB Conn.



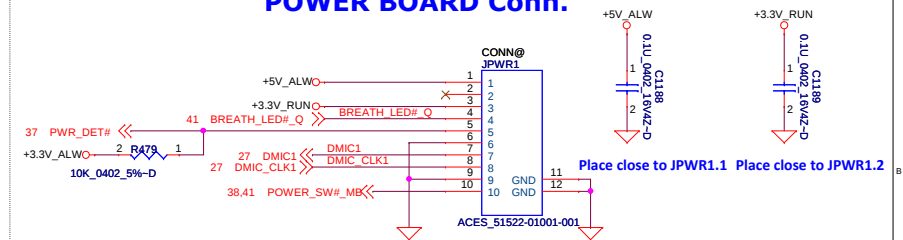
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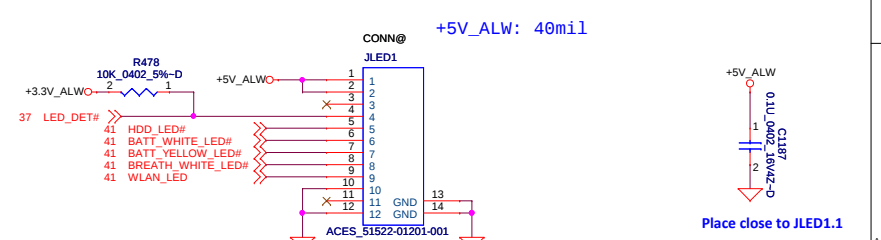
Express/Smart Card Conn.



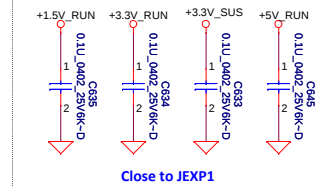
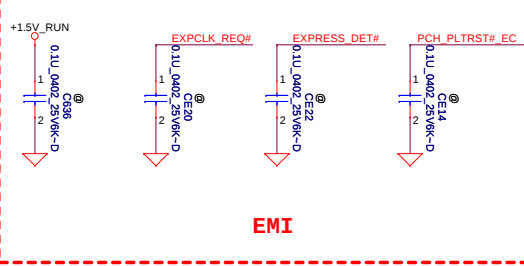
POWER BOARD Conn.



LED EXTERNAL BOARD Conn.



Link CIS



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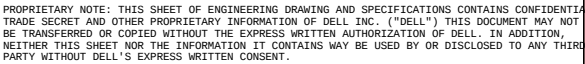
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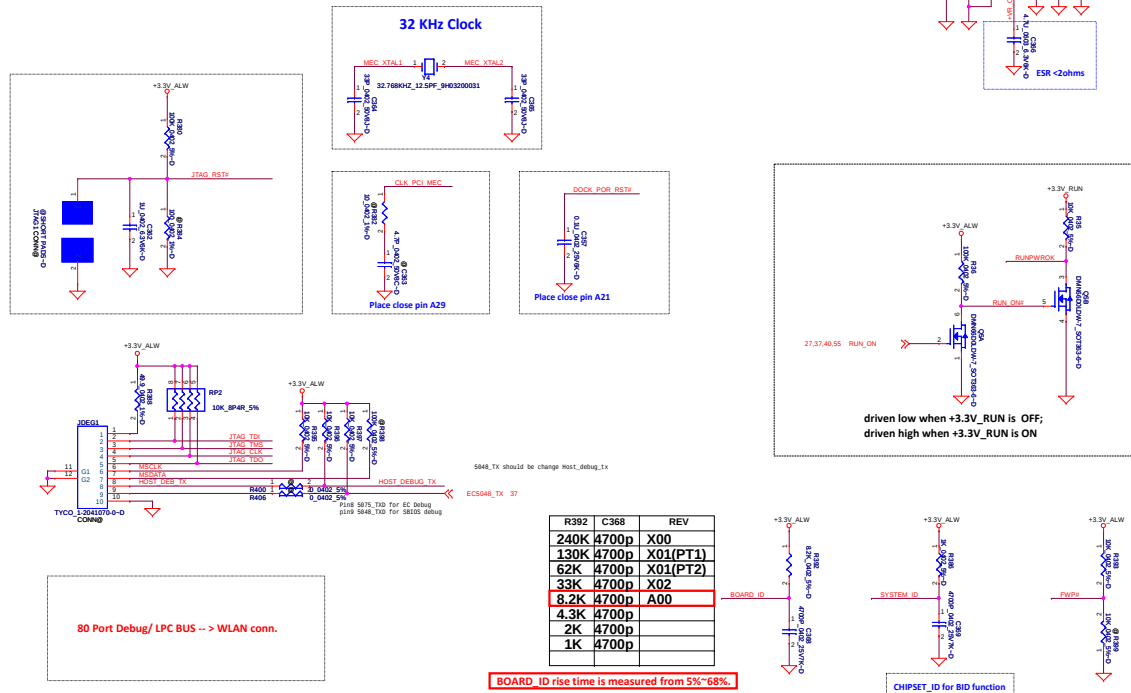
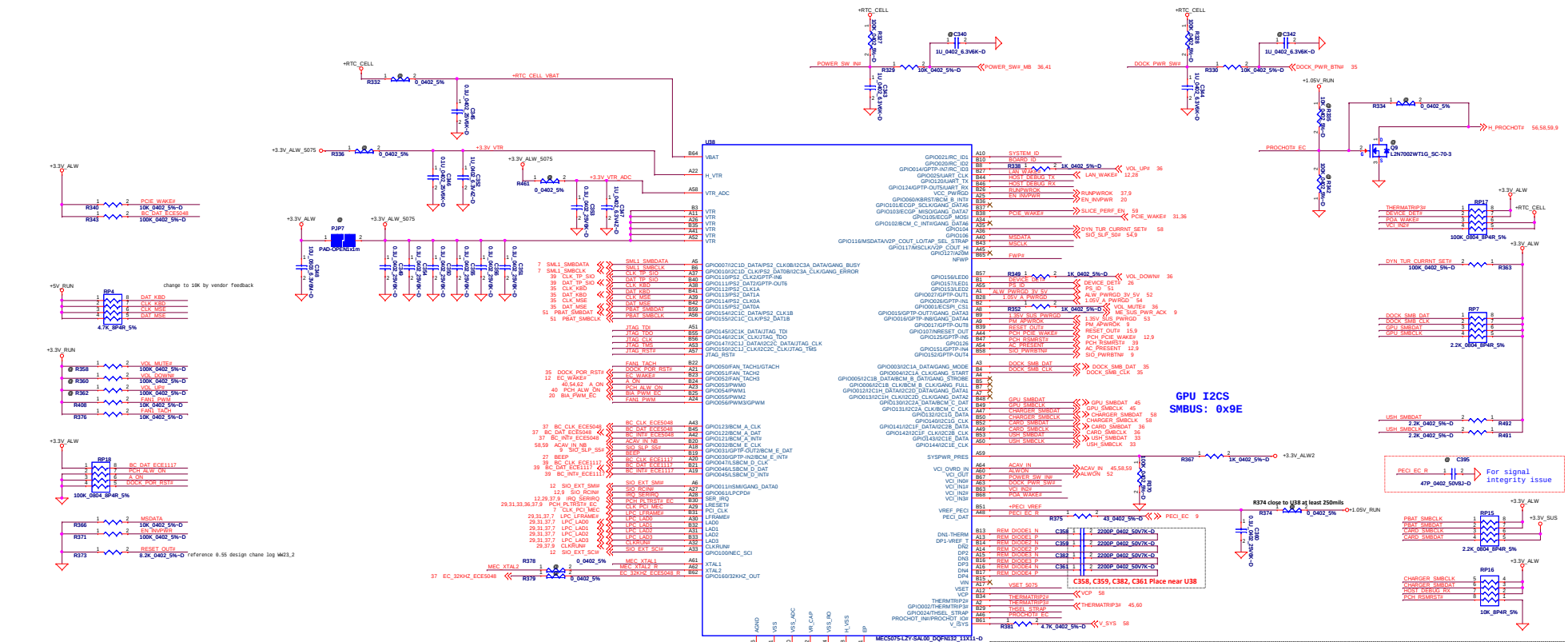
Compal Electronics, Inc.

I/O Conn

LA-9832P

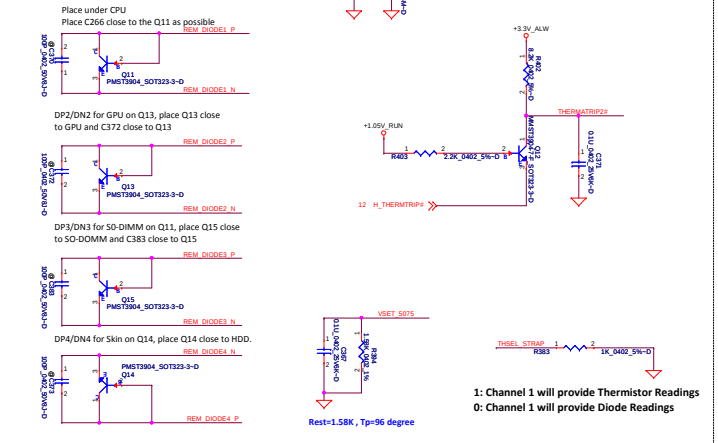
Date: Thursday, August 22, 2013 Sheet 36 of 64



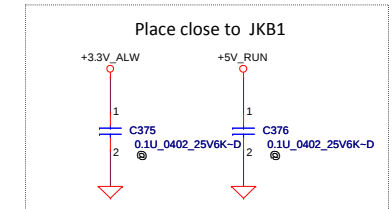
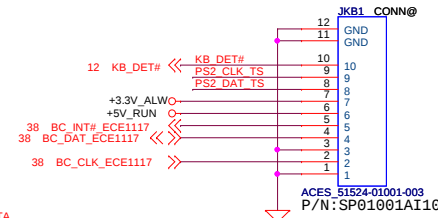
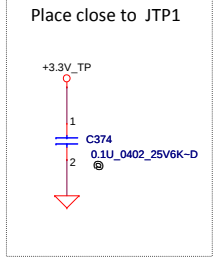
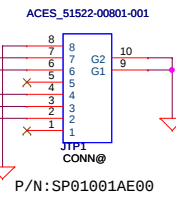
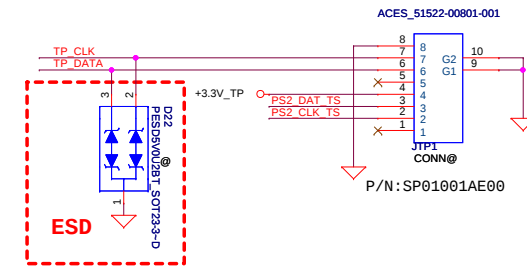
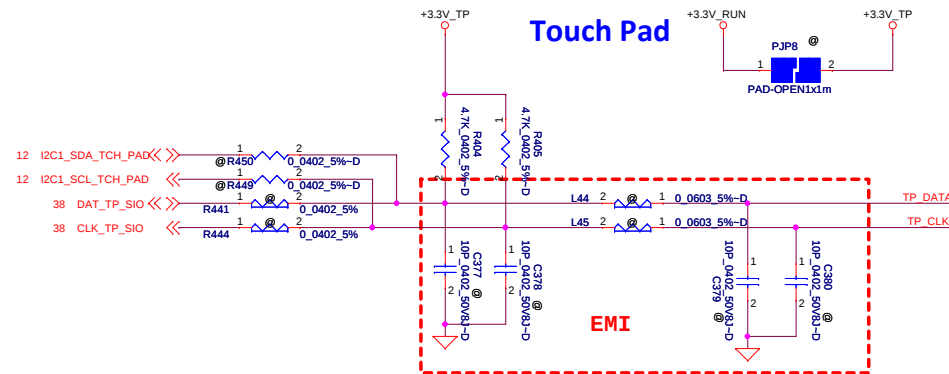


5075 Setting for Thermal Design

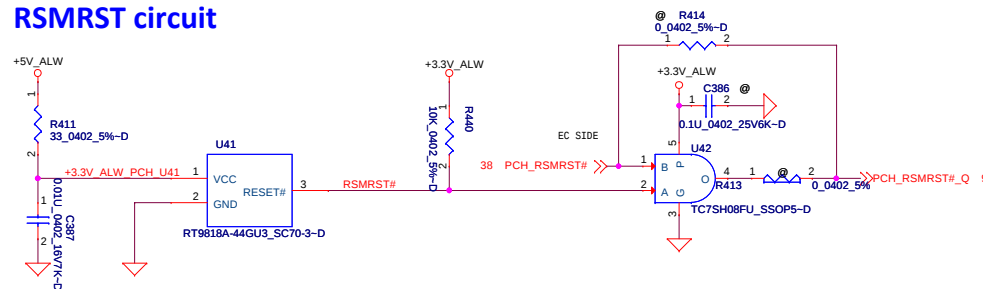
5075 Channel	Location
DP1/DN1	CPU(OTP)
DP2/DN2	Skin
DP3/DN3	SO-DIMM
DP4/DN4	HDD



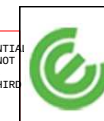
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RSMRST circuit



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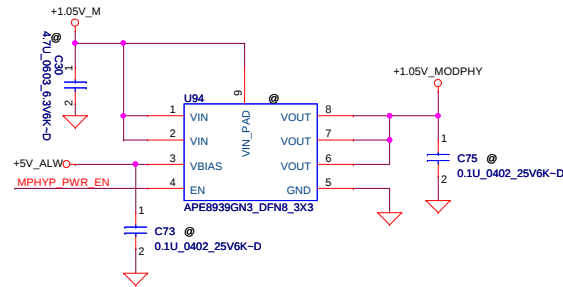
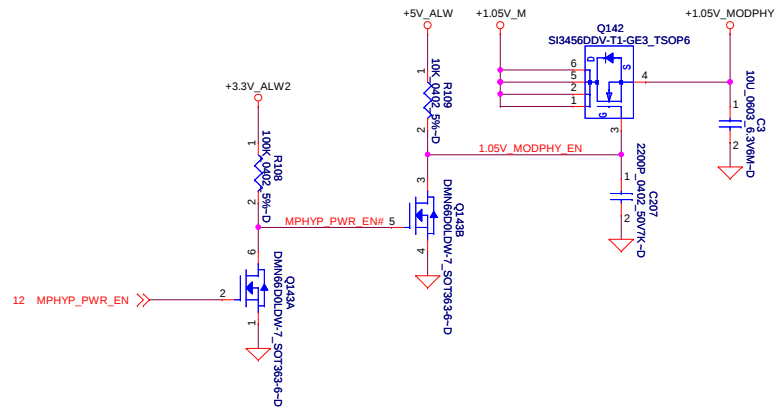


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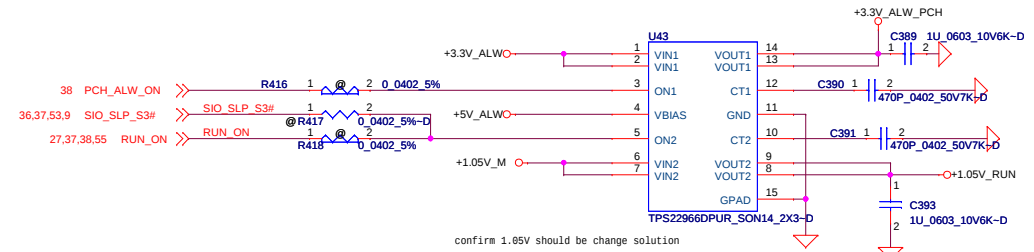
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Size	Document Number	Rev	
	LA-9832P	0.5	
Date	Thursday, June 13, 2013	Sheet	39 of 64

+1.05V_MODPHY source

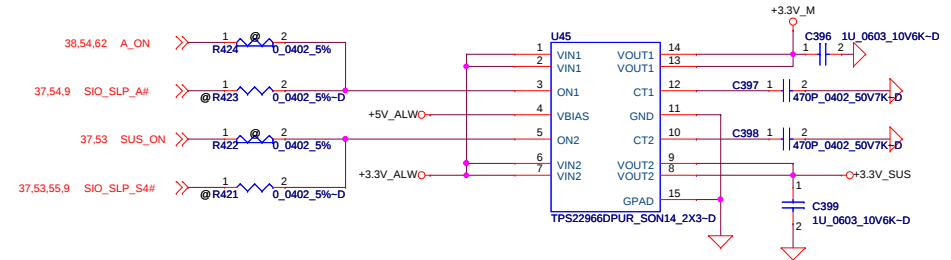


DC/DC Interface

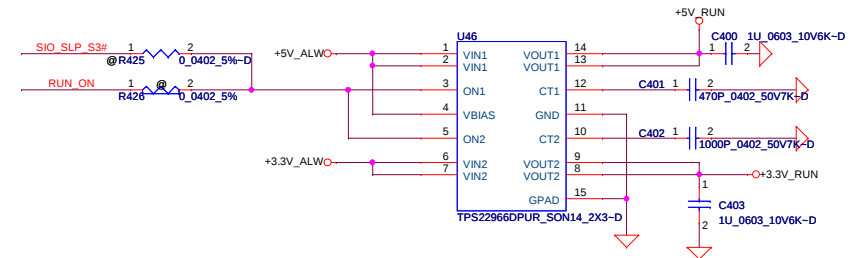
+3.3V_ALW_PCH/+1.05V_RUN source



+3.3V_SUS/+3.3V_M source



+3.3V_RUN/+5V_RUN source



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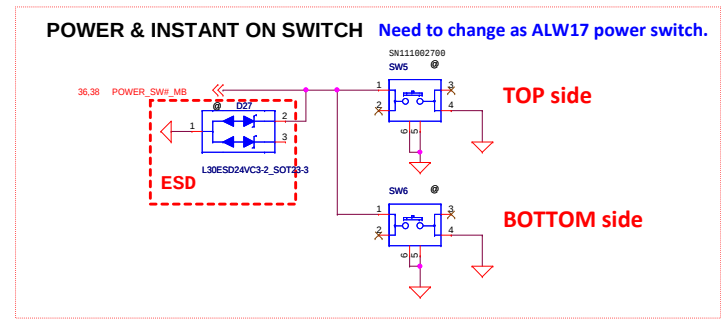
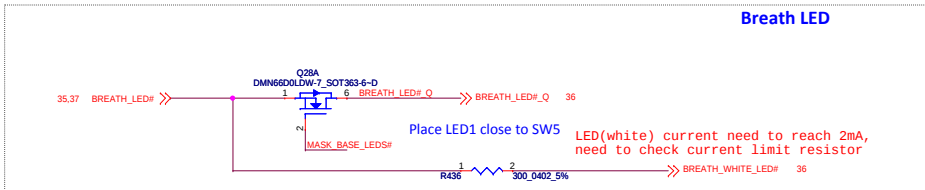
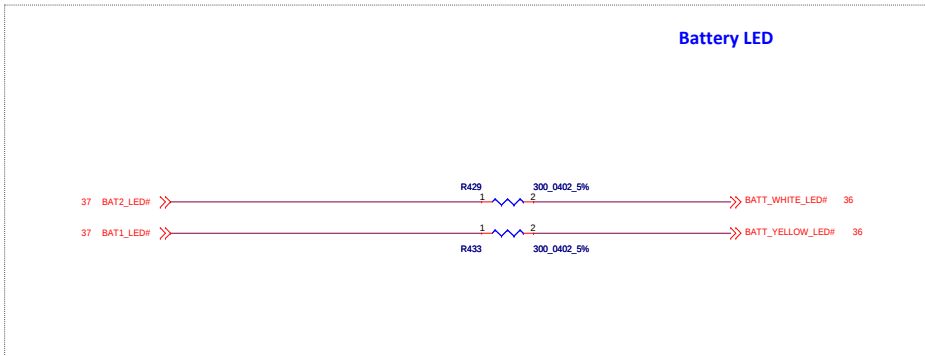
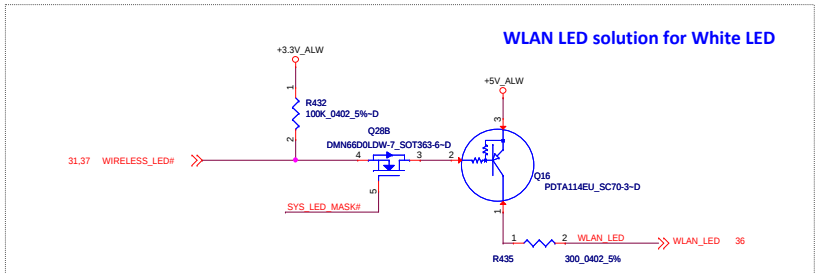
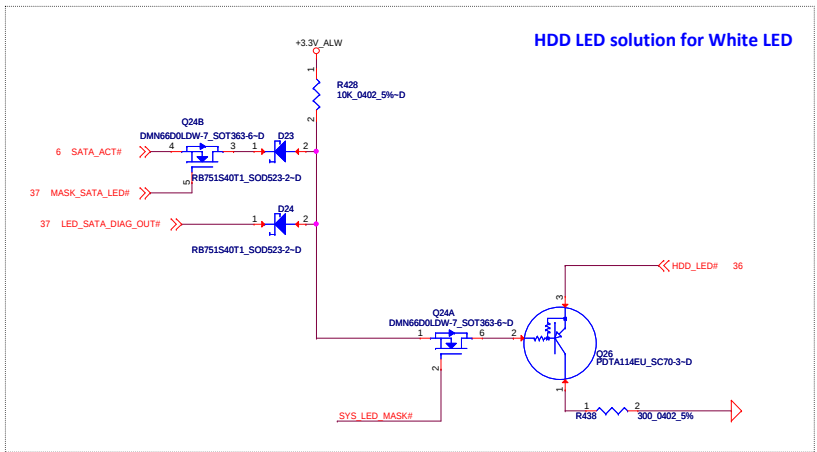
Compal Electronics, Inc.

POWER CONTROL

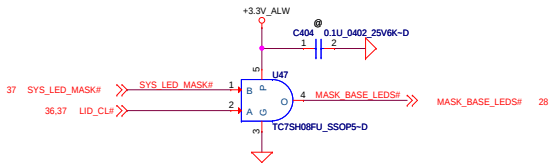
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Date: Thursday, June 13, 2013 Sheet 40 of 64

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Lid has been moved to DB.



Fiducial Mark

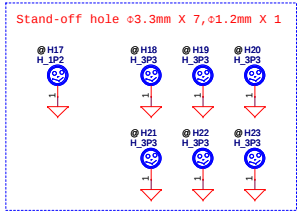
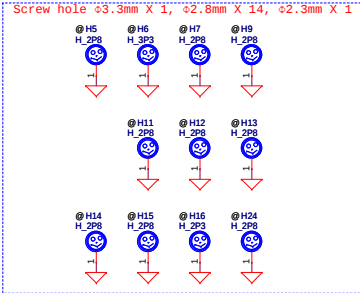
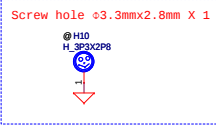
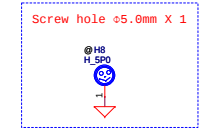
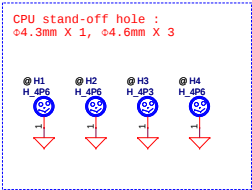
FD1
FIDUCIAL MARK-D

FD2
FIDUCIAL MARK-D

FD3
FIDUCIAL MARK-D

FD4
FIDUCIAL MARK-D

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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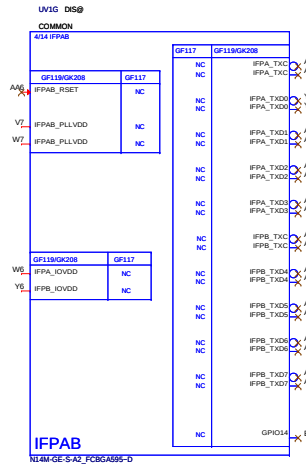
PAD & ME & LED

Document Number: **LA-9832P**

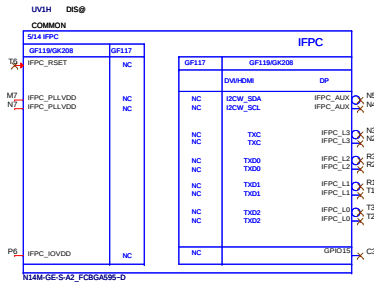
Date: Wednesday, August 14, 2013 Sheet 41 of 64

Rev 0.5

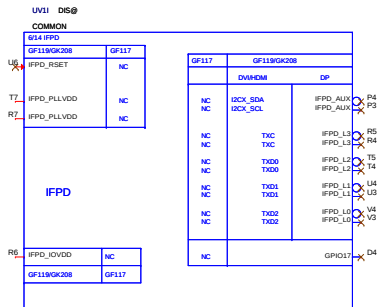
IFPA/B



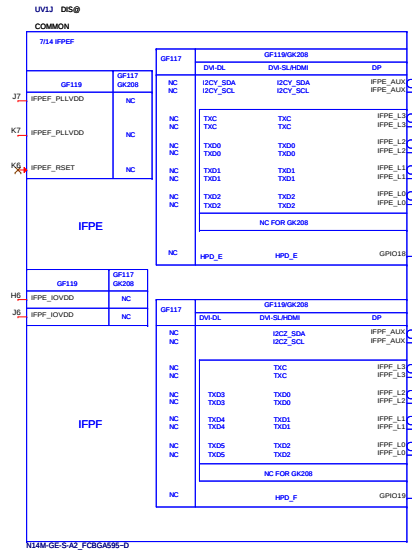
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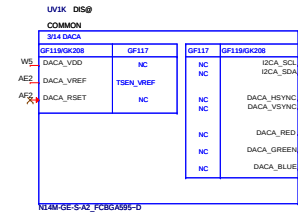
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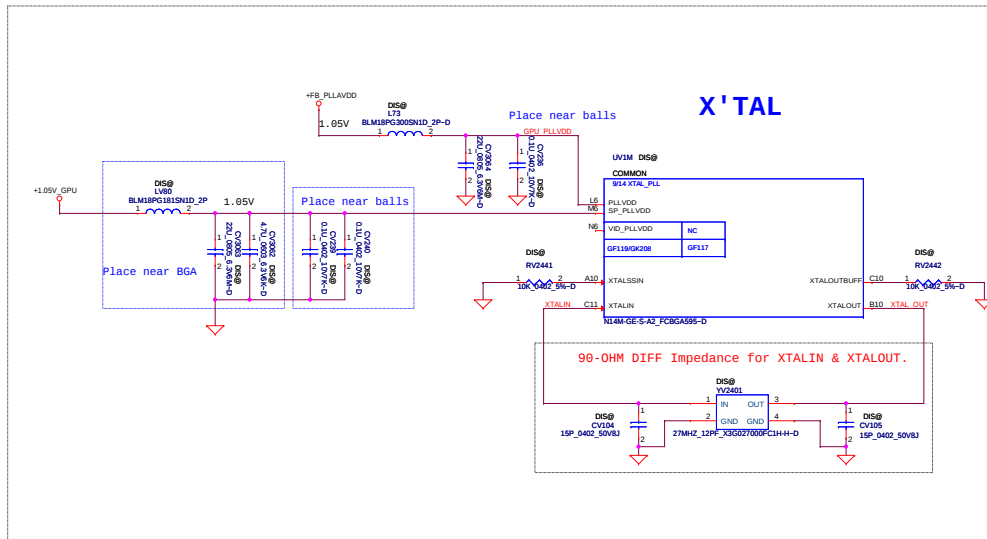
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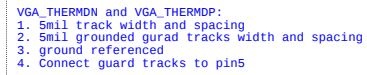
DAC_A



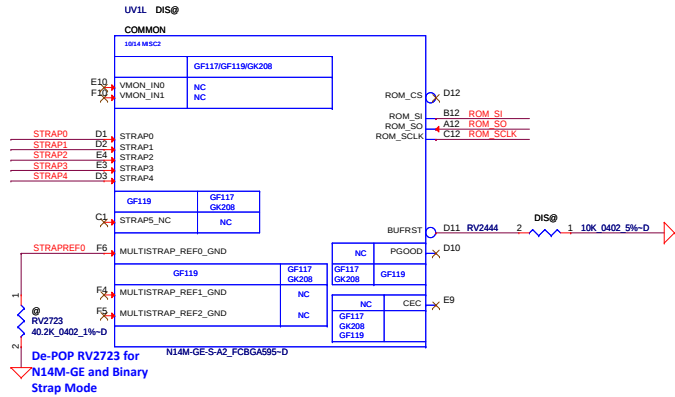
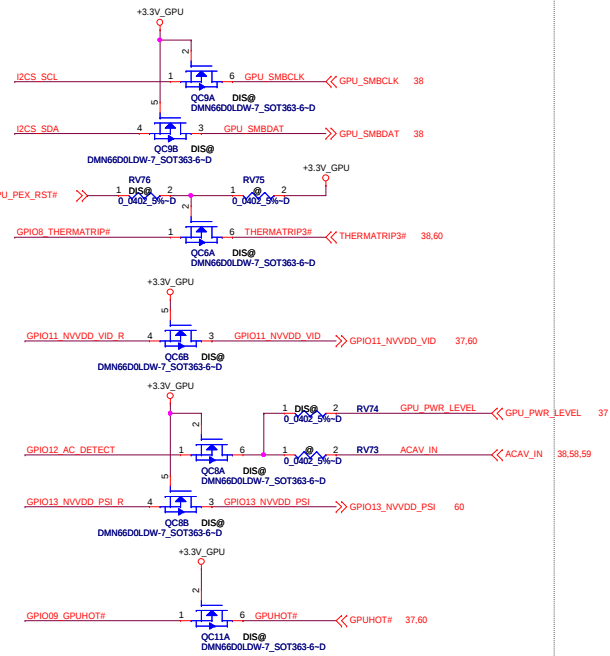
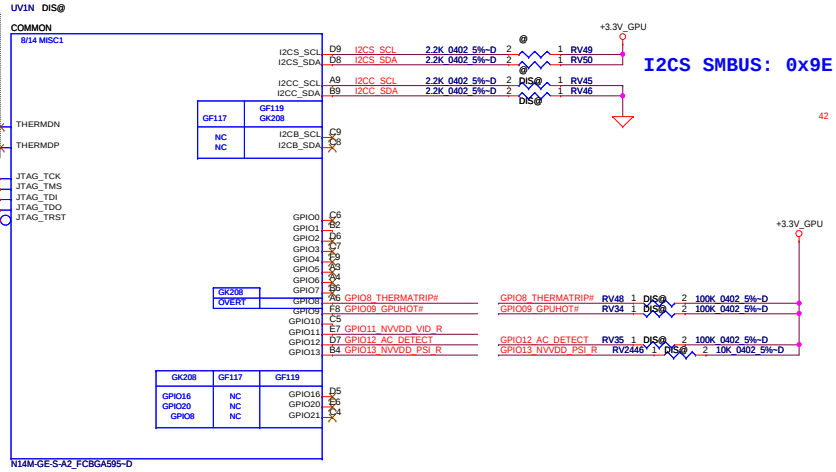
X' TAL



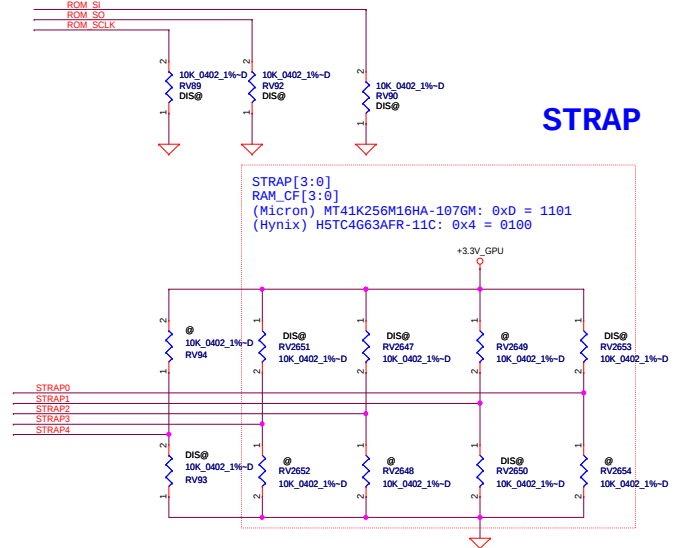
GPIO



For Boundary
Scan using.



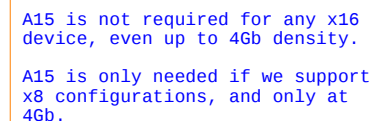
STRAP



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Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	
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				Document Number	0.5
				LA-9832P	
Date:	Wednesday, August 14, 2013	Sheet	45	of	64


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VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E
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VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E
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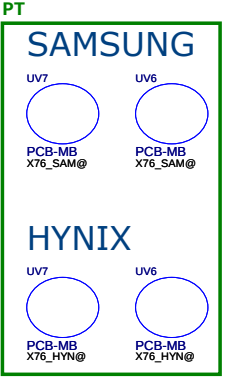
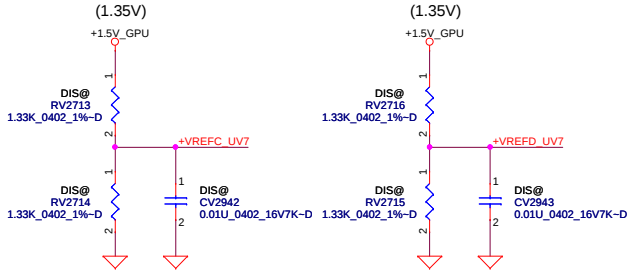
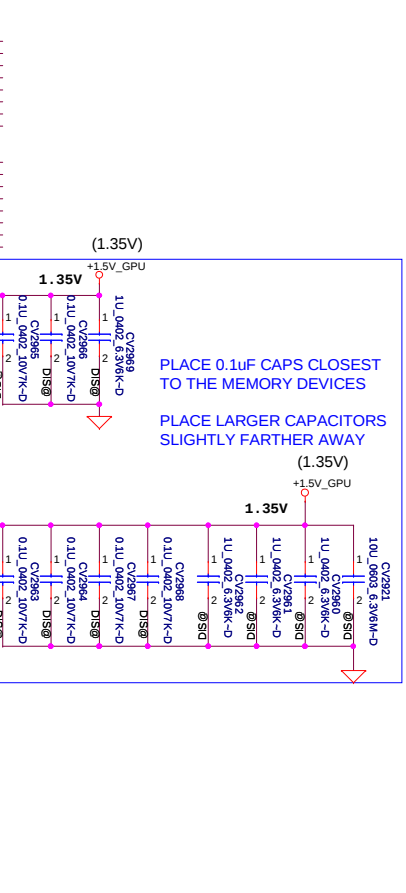
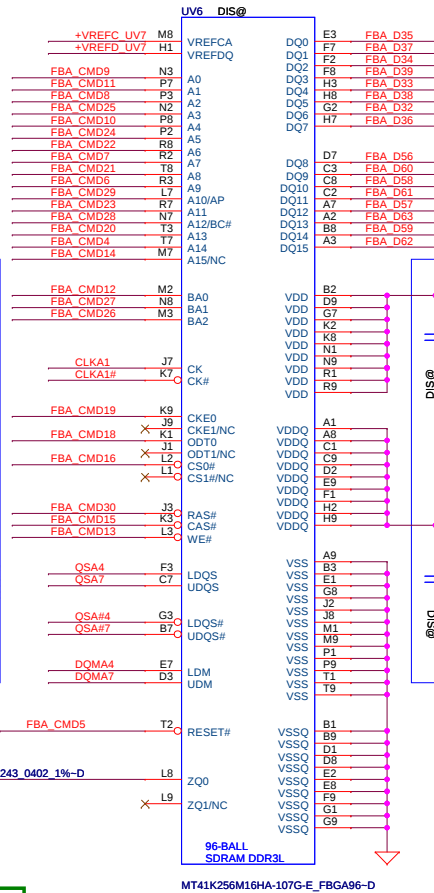
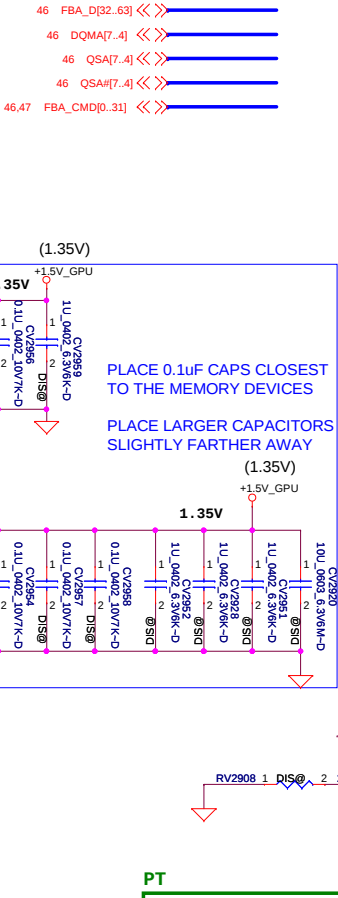
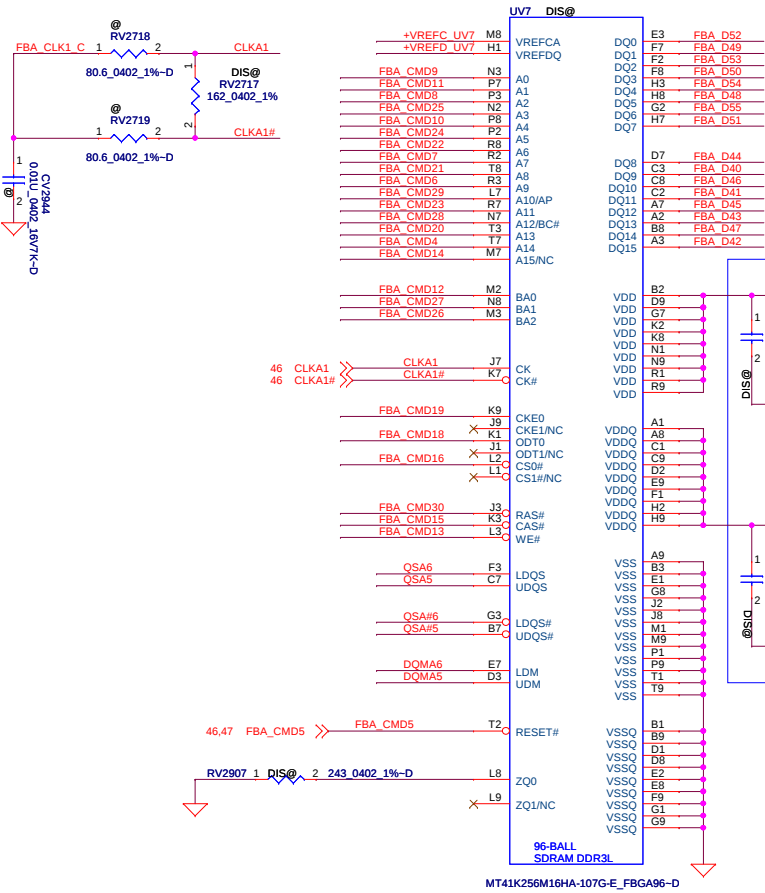


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				Date:	Thursday, June 13, 2013	Sheet 47 of 64

Memory Partition A - Upper 32 bits [64..32]

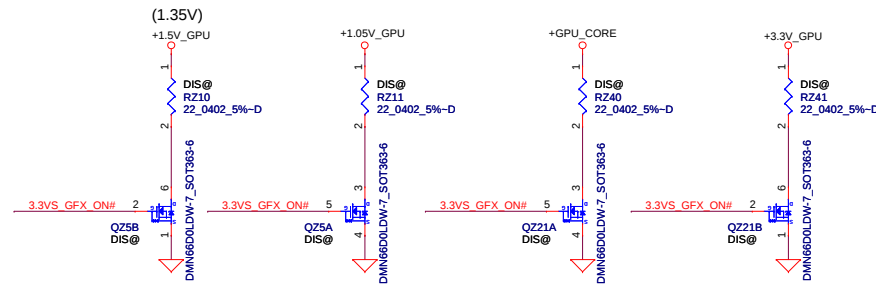
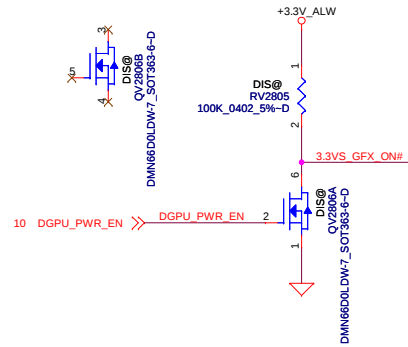
VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E

VRAM P/N changes to Micron 900Mhz
MT41K256M16HA-107G:E

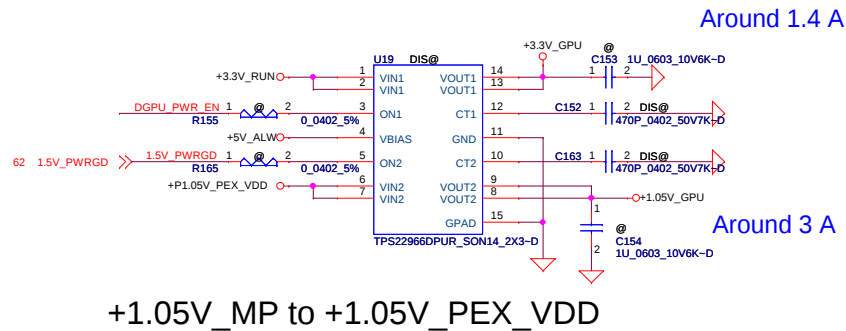


A15 is not required for any x16 device, even up to 4Gb density.
A15 is only needed if we support x8 configurations, and only at 4Gb.

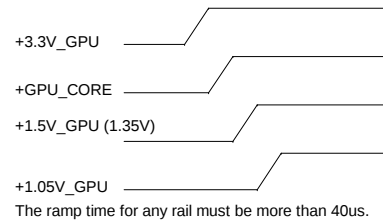
GPU Power Discharge Path



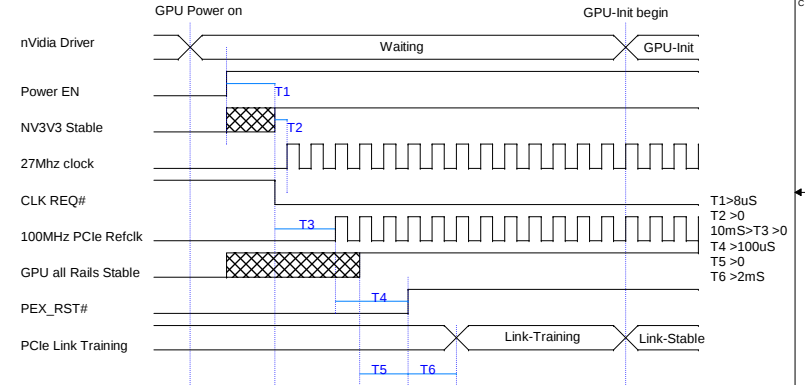
+3.3VRUN to +3.3V_RUN_GFX



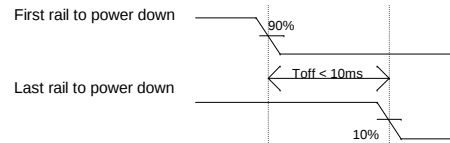
GPU Power Up Power Rail Sequence



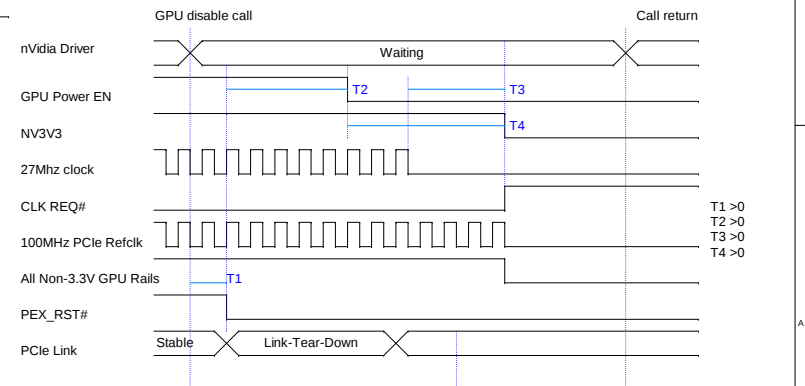
GPU Power Up Sub-system Sequence



GPU Power Down Sequence



GPU Power Down Sub-system Sequence



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Issued Date		2011/07/15	Deciphered Date	2012/07/15	Title	
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					Document Number	Rev 0.5
Date:					Thursday, August 15, 2013	
Sheet					49 of 64	

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			Compal Electronics, Inc.		
Title			BLANK PAGE		
Size	Document Number		Rev		
	LA-9832P		0.5		
Date:	Thursday, June 13, 2013		Sheet	50	of 64

EMI (47.1)

Primary Battery Connector

37.1

EMI (47.1)
Dell feature: ESD&EMI

Others (37.1)
PWR support

Dell feature: ESD&EMI

PSID circuit (39.1)
Dell feature: PSID

Dell feature: Support dock

DC_IN+ Source

Dell feature
peak power

EMI (47.1)

37.1

Charger (40.2)

EMI (47.1)

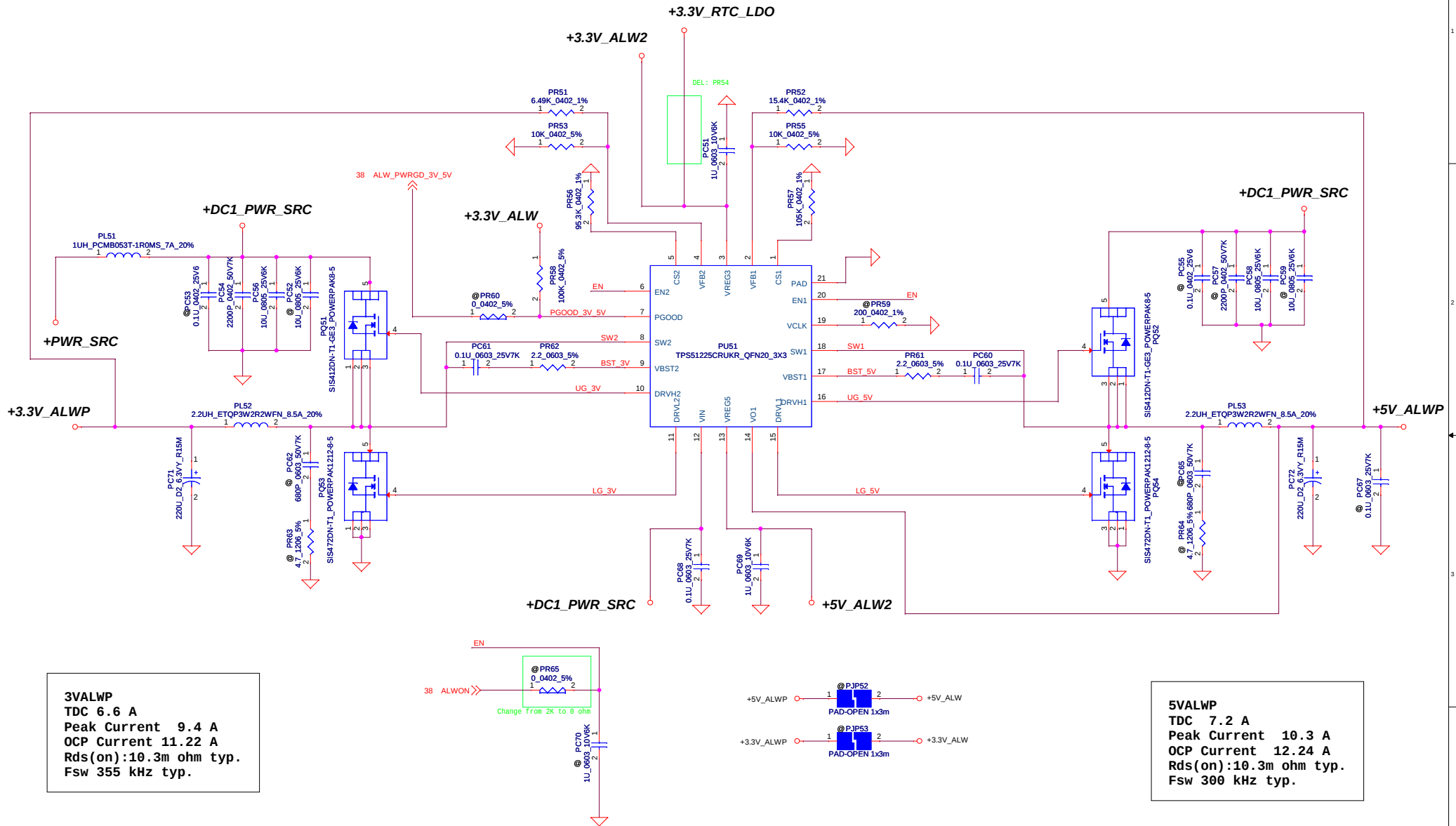
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Compal Electronics, Inc.

+DCIN

Size Document Number LA-XXXX Rev 0.1
Date: Wednesday, August 14, 2013 Sheet 51 of 64

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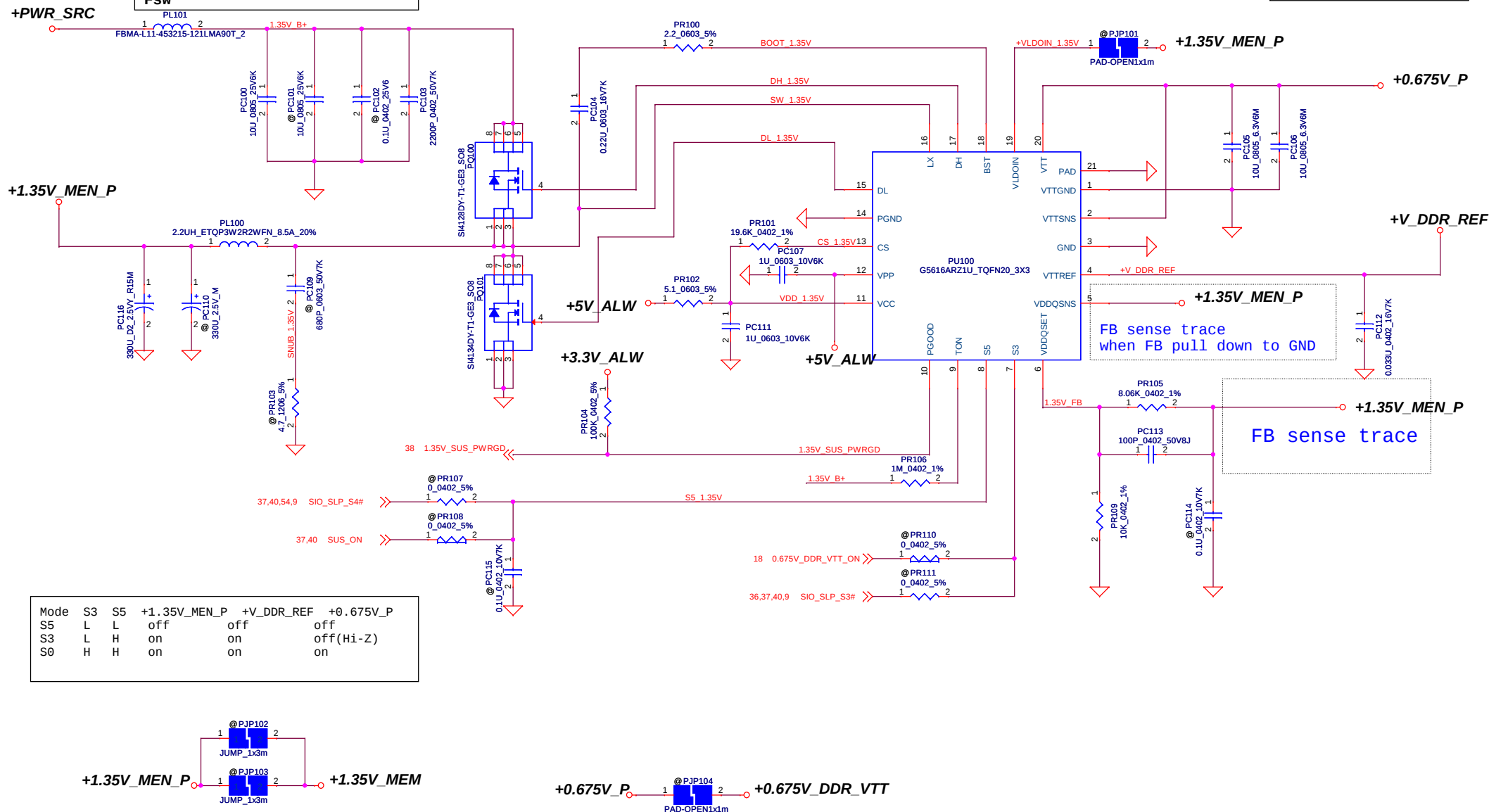


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Title		PWR +5V_ALW/3.3V_ALW	
Size	Document Number	LA-XXXX	
Date	Wednesday, August 14, 2013	Sheet	52 of 64
Rev	0.1		

1.35V_{olt} +/- 5%
TDC: 7.2 A
Peak Current: 10.3 A
OCP current: 12.24 A
Rds(on):14.5m ohm typ
Fsw

0.675Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.8925A



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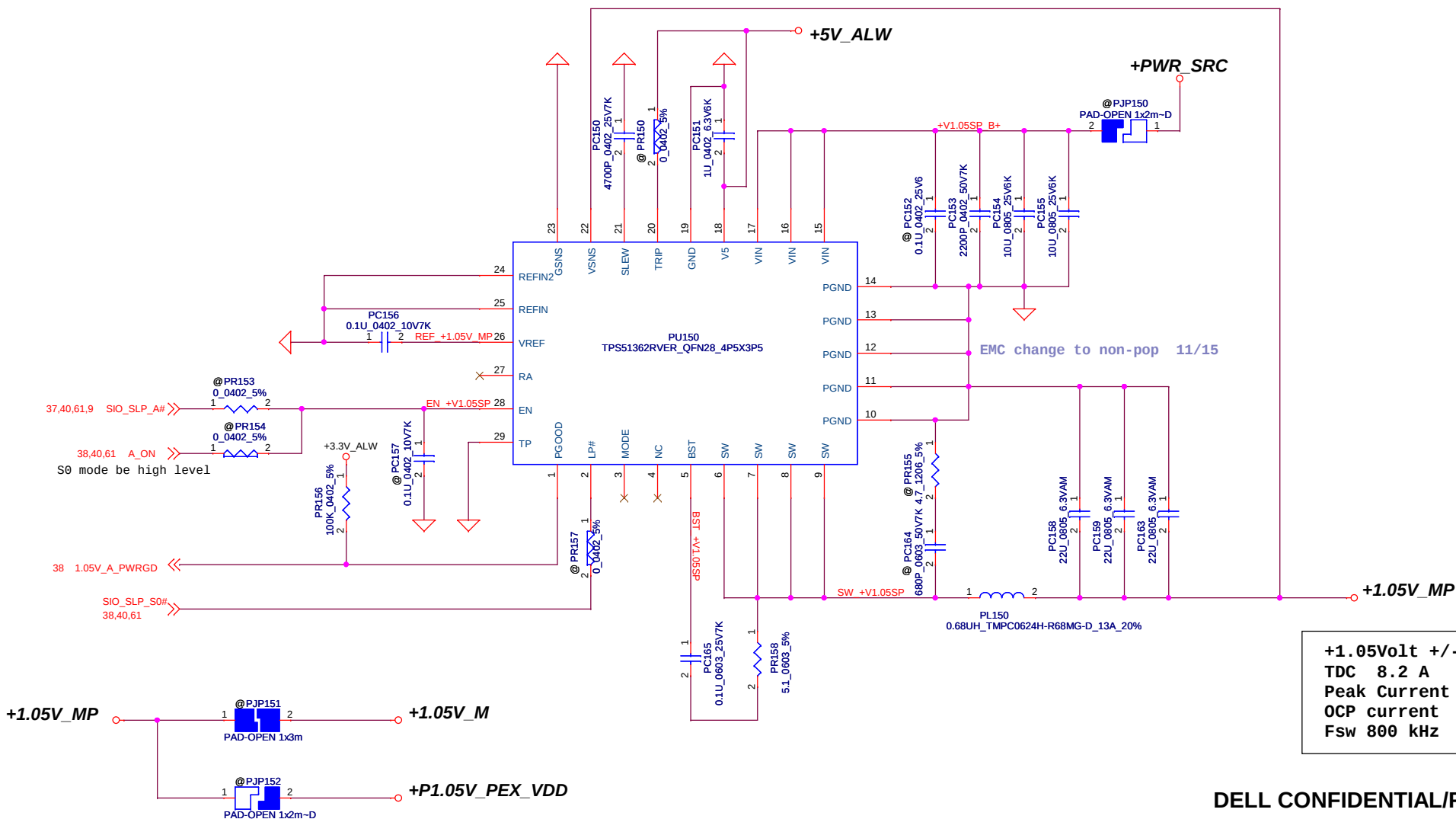
Compal Electronics, Inc.

Title	PWR +1.35V MEN/+0.675V DDR
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Size	Document Number	Rev
	LA XXXX	0.1

Date: Wednesday, August 14, 2013 Sheet 53 of 64

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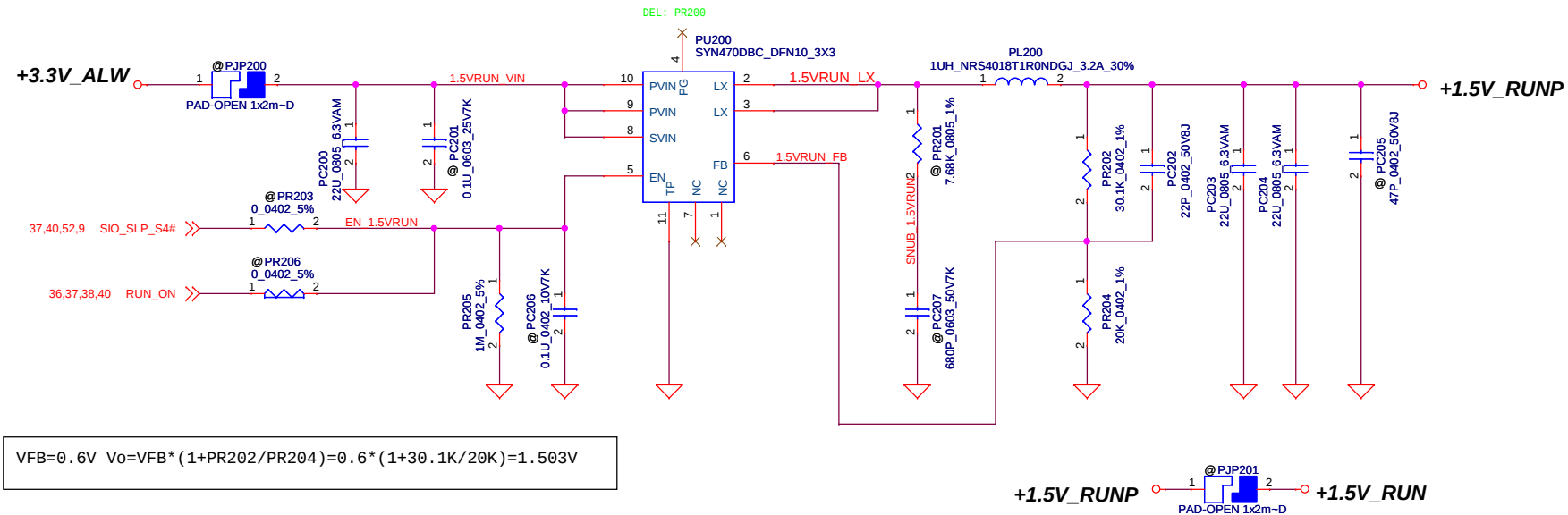


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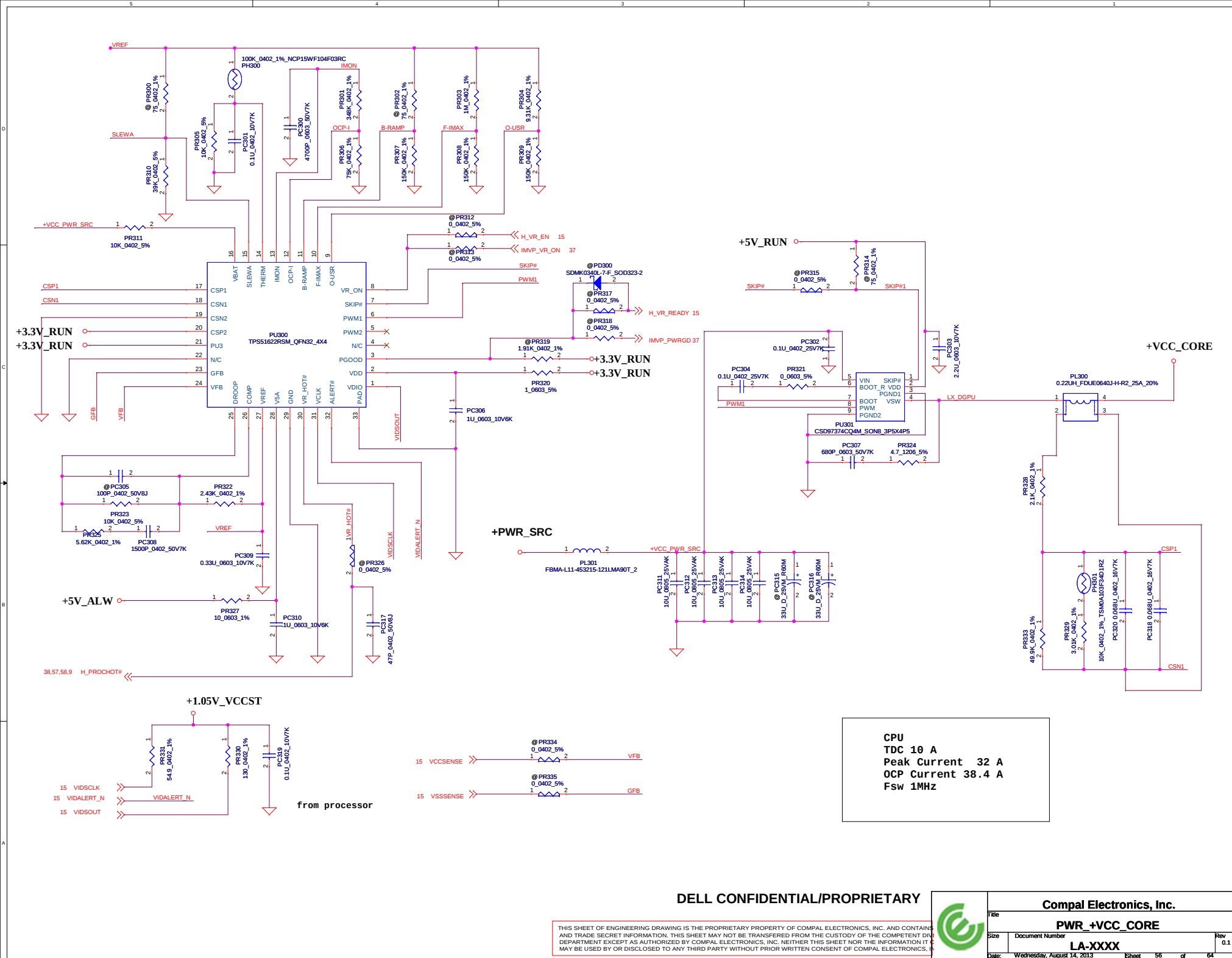
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Compal Electronics, Inc.			
Title			
PWR +1.05VTTTP			
Size	Document Number		Rev
	LA-XXXX		0.1
Date:	Wednesday, August 14, 2013		Sheet 54 of 64

1.5Volt
Frequency 1MHz
TDC 0.65A
Peak Current 0.93A
OCP current 3.5A (Fix)



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Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>	Title	PWR_1.5V_RUN
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				Date: Wednesday, August 14, 2013	Sheet 55 of 64

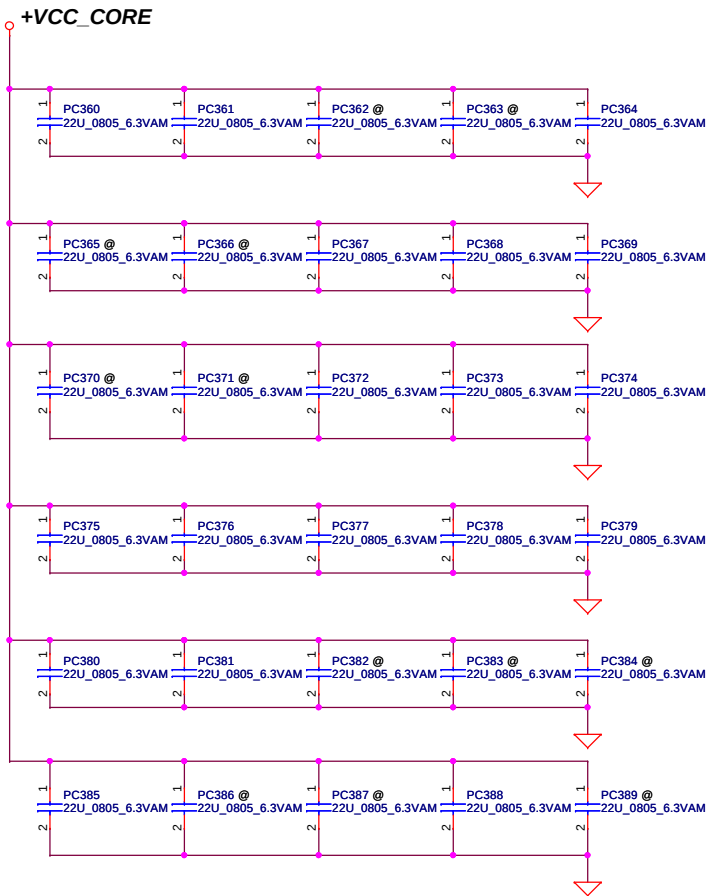


CPU
TDC 10 A
Peak Current 32 A
OCP Current 38.4 A
Fsw 1MHz

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Compal Electronics, Inc.			
File	PWR_+VCC_CORE		
Size	Document Number	Rev	
	LA-XXXX	0.1	
Date	Wednesday, August 14, 2013	Sheet	56 of 64



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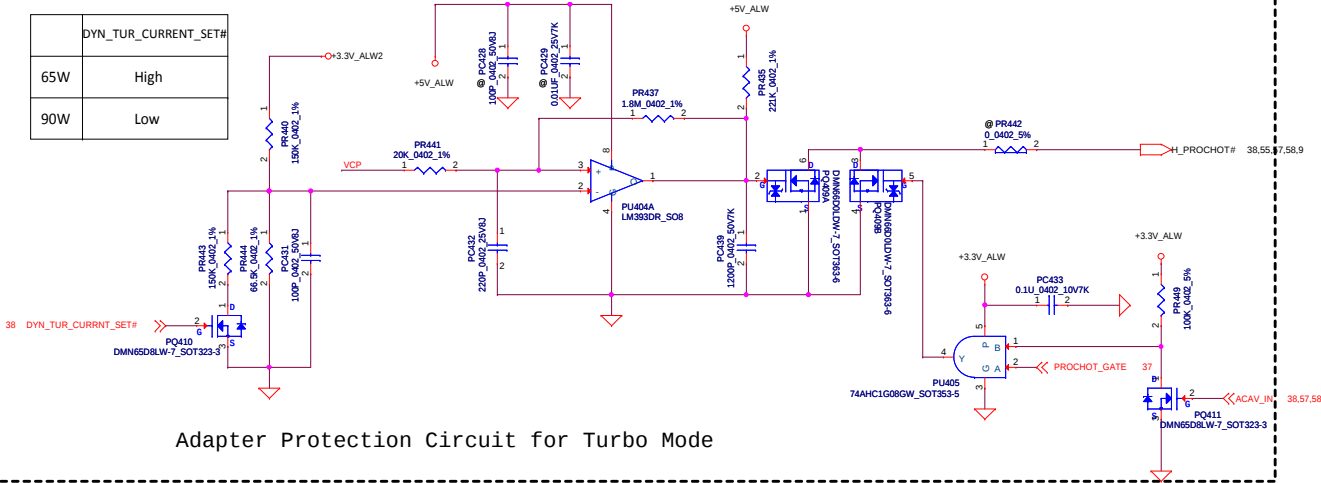
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PWR_PROCESSOR DECOUPLING		
Size	Document Number	Rev
	LA-XXXX	0.1
Date:	Wednesday, August 14, 2013	Sheet 57 of 64

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Charger controller (40.1)
Support Component (40.2)

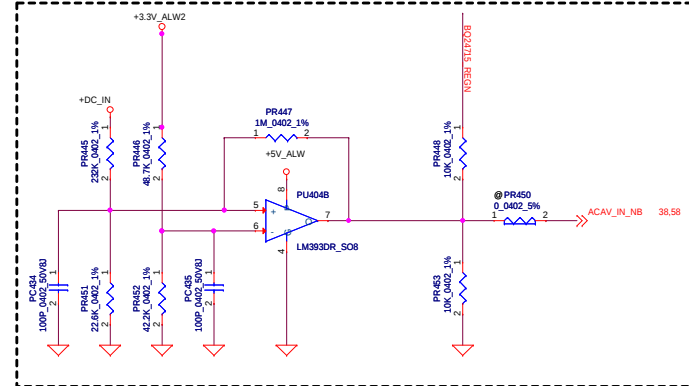
Adapter protection (39.7)
Dell feature: AC protect

DYN_TUR_CURRENT_SET#	
65W	High
90W	Low



E-dock power(41.2)
Dell feature

E-dock power(41.2)
Dell feature: AC protect



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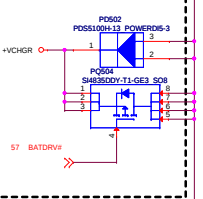
PWR_Charger

LA-XXXX

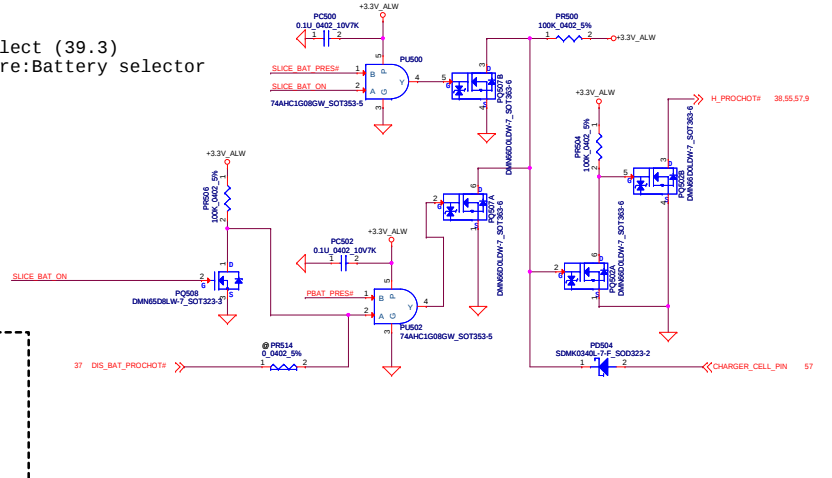
Size	Document Number	Rev
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Date:	Wednesday, August 14, 2013	Sheet 58 of 64

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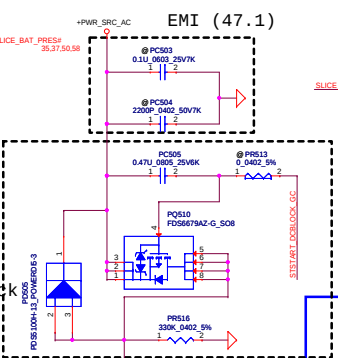
Charger (40.2)



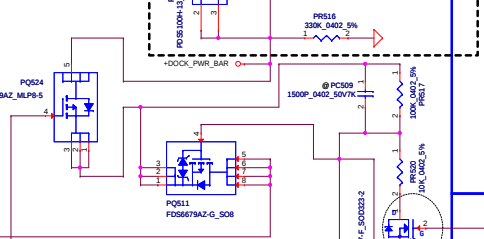
Battery select (39.3)
Dell feature: Battery selector



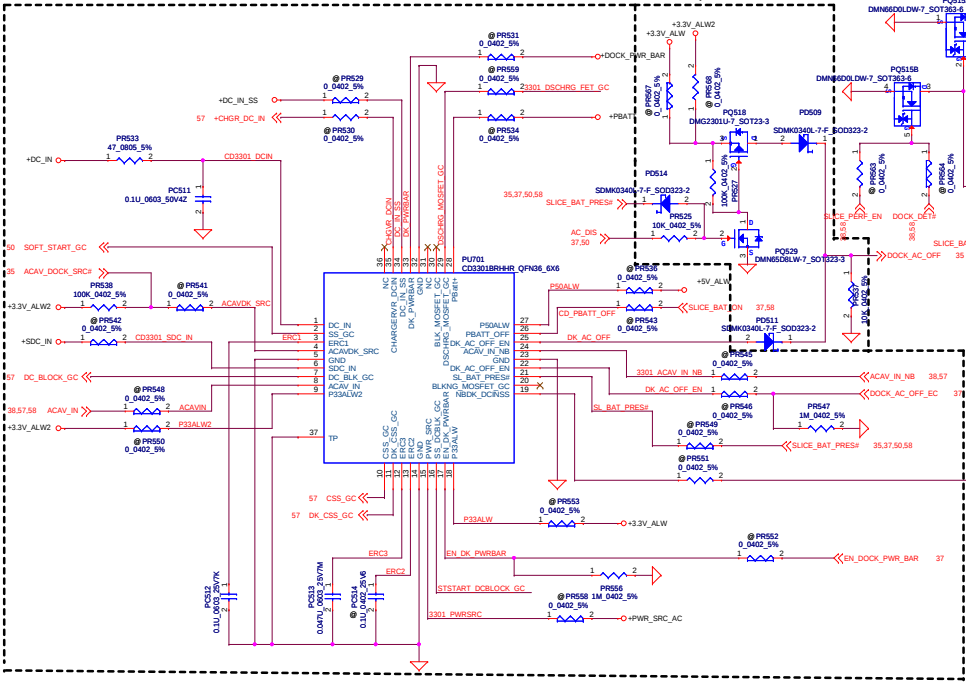
EMI (47.1)



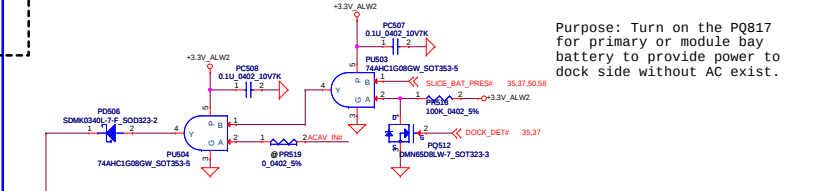
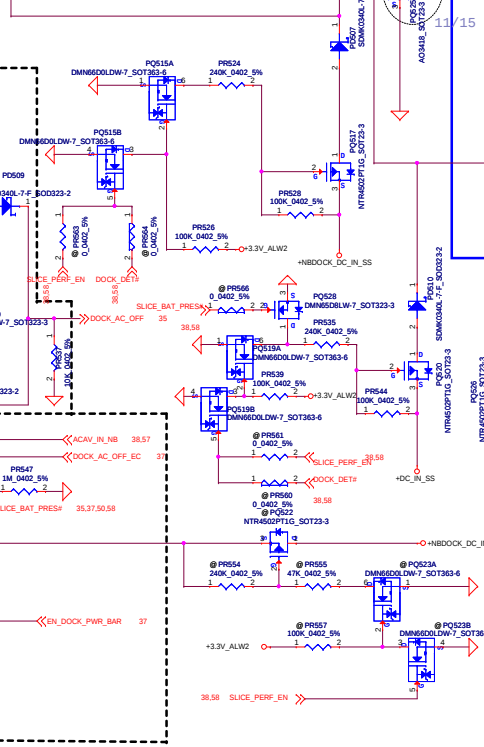
E-dock power(41.2)
Dell feature: Support dock



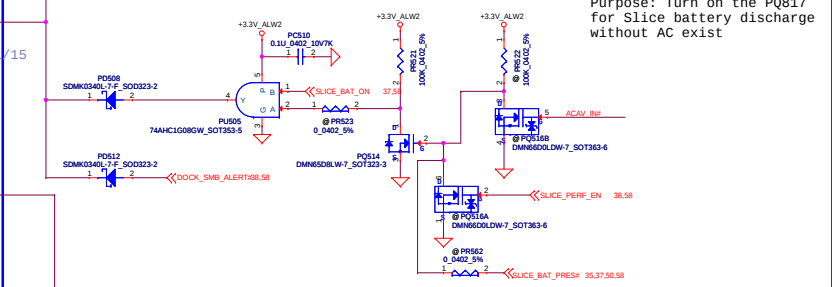
Edock controller(41.1), support component(41.2)
Dell feature: Support dock



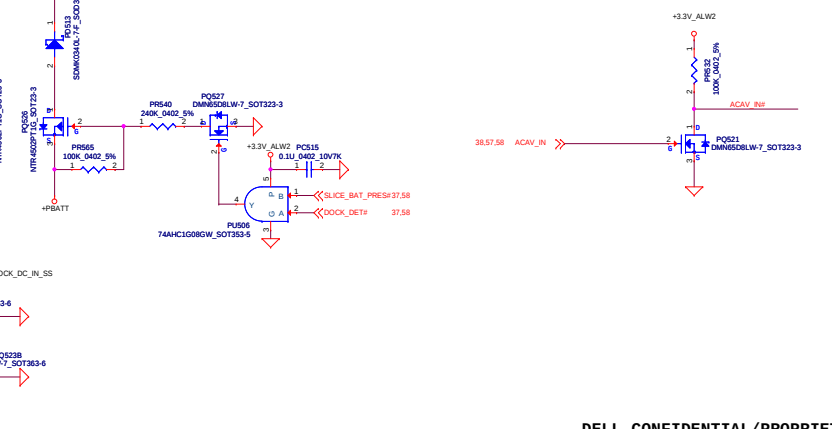
Charger (37.1)
Dell feature: Peak power



Purpose: Turn on the P5017 for primary or module bay battery to provide power to dock side without AC exist.



Purpose: Turn on the P5017 for Slice battery discharge without AC exist



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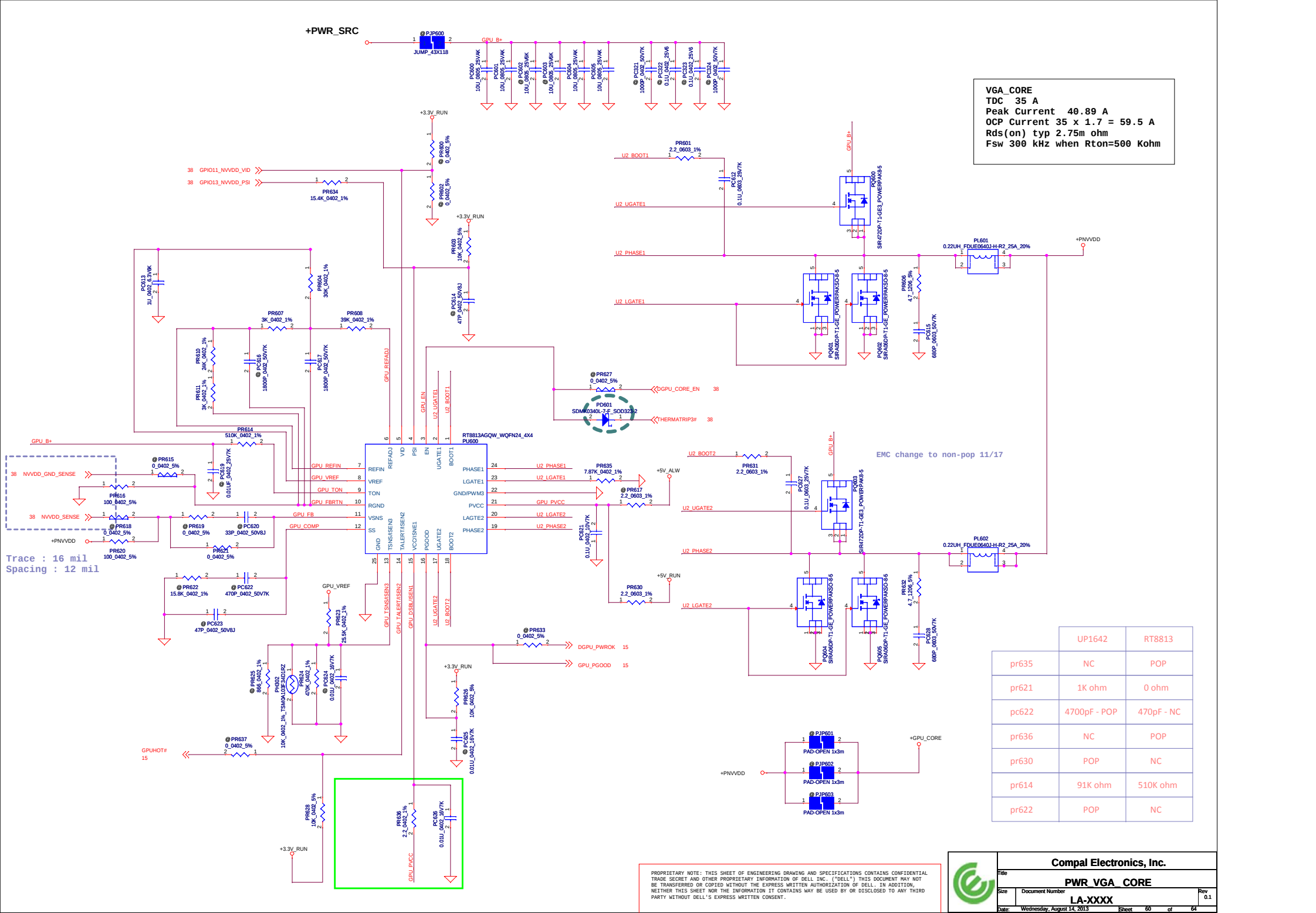
PWR Selector

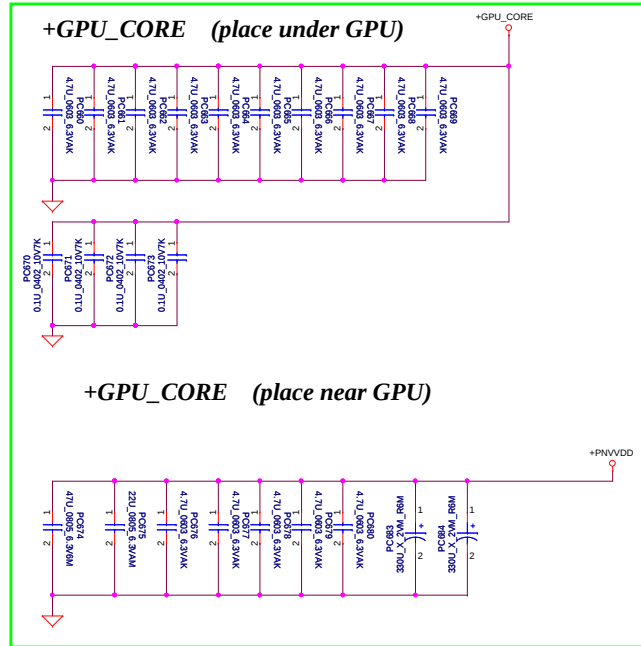
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Rev	0.1
Size	Document Number
Date	Tuesday, August 20, 2013
Sheet	59 of 64





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Title

PWR_GPU_DECOUPLING

Size

Document Number

LA-8821P

Date

Wednesday, August 14, 2013

Sheet

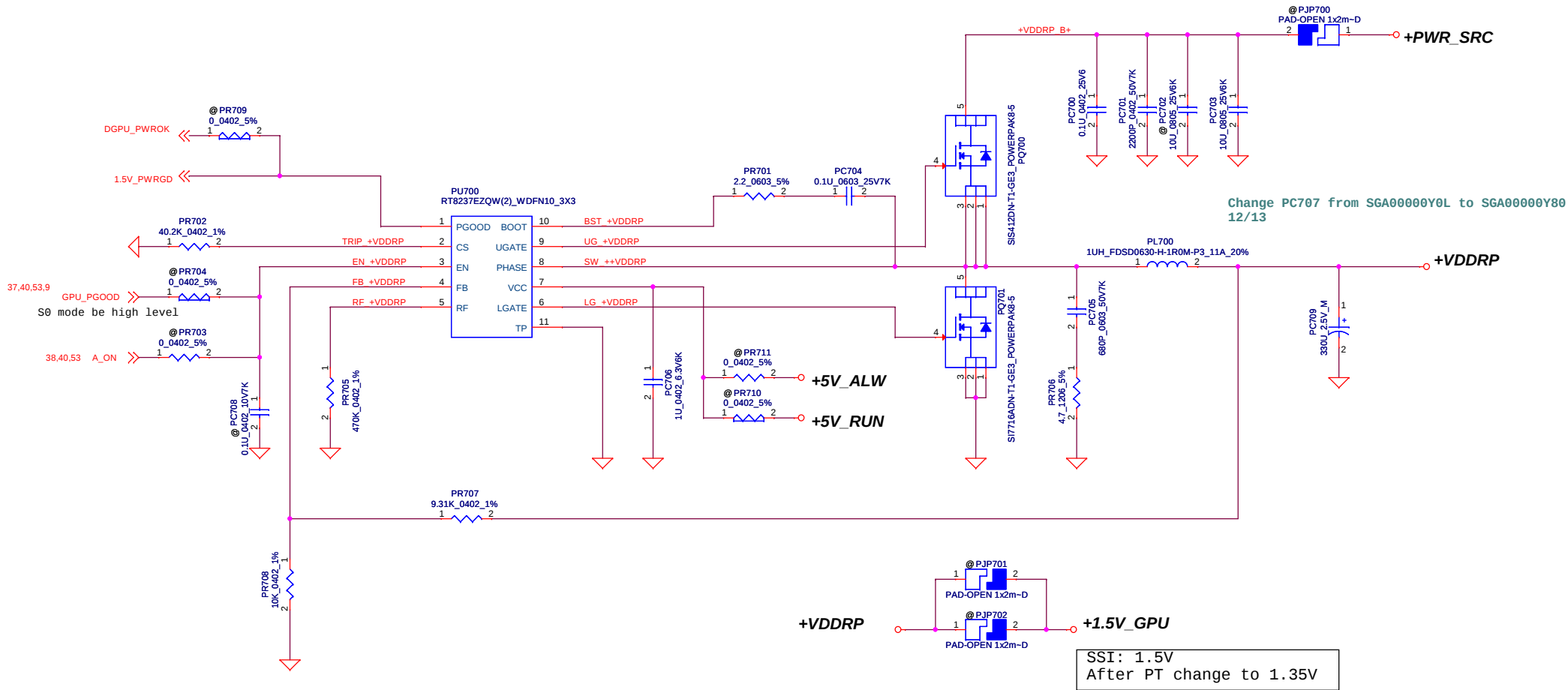
61

of

64

Rev

0.1



+VDDRP(1.35V)
TDC 2.94A
Peak Current 4.2A
OCP current 5A
Rds(on):13.5m ohm typ
Fsw 290 kHz when Rrf=470 Kohm

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Title			PWR +1.5VDDR	
Size	Document Number			Rev
	LA-9391P			0.1
Date:	Wednesday, August 14, 2013			Sheet 62 of 64

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	58	Adapter Protection Circuit	2013/1/30	Power	PC432 220pF is not popular part	Change to 0402 size	X00
2	59	P59-PWR_Selector	2013/2/4	Power	Battery voltage leakage to docking if only battery	Add: PD513, PQ526, PR565, PR540, PQ527, PU506, PC515	X00
3	56	Vcore fine tune	2013/2/7	Power	Vcore fine tune	Modify: PR306, PR301, PR333, PR328, PR325, PR322, PL300	X00
4	57	Vcorecapacitor reduce	2013/2/7	Power	Vcore output capacitor reduce	NC: PC371 ,PC386, PC370 ,PC382,PC383	X00
5	58	Charger	2013/2/18	Power	Reserve H_PROCHOT# delay time fine tune by soft ware	Add "MODULE_BATT_PRES#" and PR454(Cancel 3/19)	X00
6	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 240K to 100K: PR503, PR528, PR544, PR565	X00
7	59	P59-PWR_Selector	2013/2/26	Power	Adjust divider resistor for MOSFET	Change from 47K to 240K: PR501, PR524, PR535, PR540	X00
8	59	P59-PWR_Selector	2013/2/26	Power	SUT will unexpected shut down if un-docking during S0/S3	Add: PQ528, PR566	X00
9	51	"PBAT_PRES#" ESD fail	2013/3/4	Power	ESD PD1 fail, even connect 3.3V to VBUS pin	Change PD1 to PD1, PD2(TVNST52302AB0)	X00
10	59	P59-PWR_Selector	2013/3/6	Power	SB903380020 FDN338P derating fail	PQ500, PQ517,PQ520,PQ522,PQ526 change to SB000007900, PQ1change to SB000009300	X00
11	51	PC5 down size	2013/3/12	Power	PC5 down size	Change PC5 from 0805 to 0603 size	X00
12	51,59	AC_DIS# net change	2013/3/12	Power	AC_DIS# should high enable, not low enable	AC_DIS# change to AC_DIS	X00
13		EMC open issue	2013/3/18	Power	Add parts for EMI	PR606,PC615, PR632, PC628, PR706, PC705, PR324, PC307	X00
14	60, 62	PU600, PU601 VCC	2013/3/19	Power	DIS S3 power consumption voer 200mW	Add PR630 PR711, PR710 for reserve +5V_RUN	X00
15	61	Change DGPU output cap	2013/3/19	Power	For thermal issue change DGPU power output cap.-14"	Change PC683,PC684	X00
16	62	GPU DDR change to 1.35V	2013/3/19	Power	Change VDDR output voltage from 1.5V to 1.35V	Change PR707 from 11.5K to 9.1K	X00
17	54	+1.05V dynamic load test	2013/3/19	Power	+1.05V dynamic load over spec	Change PL150 from 1uH to 0.68uH	X00
18	58	Change output chock	2013/3/20	Power	Same as 14" for height limit	Charger output choke change to 2.2uH	X00
19	60	0 ohm resistor	2013/3/21	Power	0 ohm 1% vender is not correct in ISPD	Change PR621 0ohm from 1% to 5%	X00
20	54	1.05V dynamic over spec	2013/3/21	Power	1.05V dynamic over spec	Change PL150 from 1uH to 0.68uH	X00
21	59	Modify for Peak power	2013/3/21	Power	Modify schematic	PQ529, PQ518, PR527 and PR567	X00
22	NA	Reserve	Reserve	Power	Reserve	Reserve	X01
23	60	DGPU core output ripple	2013/5/10	Power	Output ripple with a low frequence ripple	+PWR_SRC do not include feedback via	X01
24	60	DGPU core output ripple	2013/5/10	Power	Output ripple with a low frequence ripple	+PWR_SRC do not include feedback via	X01
25	59	14" 組裝問題	2013/5/10	Power	PD512 太靠邊板	Move location	X01

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Title			EE PIR(1)
Size	Document Number		LA-XXXX
Date	Wednesday, August 14, 2013	Sheet	64 of 64
		Rev	1.0

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Size	Document Number		Rev
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Date:	Wednesday, August 14, 2013	Sheet	64 of 64

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Size	Document Number	Rev	
	LA-9832P	0.5	
Date:	Friday, August 30, 2013	Sheet	65 of 64