VFKTA

Rosetta 10FTG

LA-9861P REV 1.0 Schematic

Intel Processor (Ivy Bridge/Sandy Bridge)+
PCH(Panther Point)

2013-02-19 Rev 1.0

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	Cover Page
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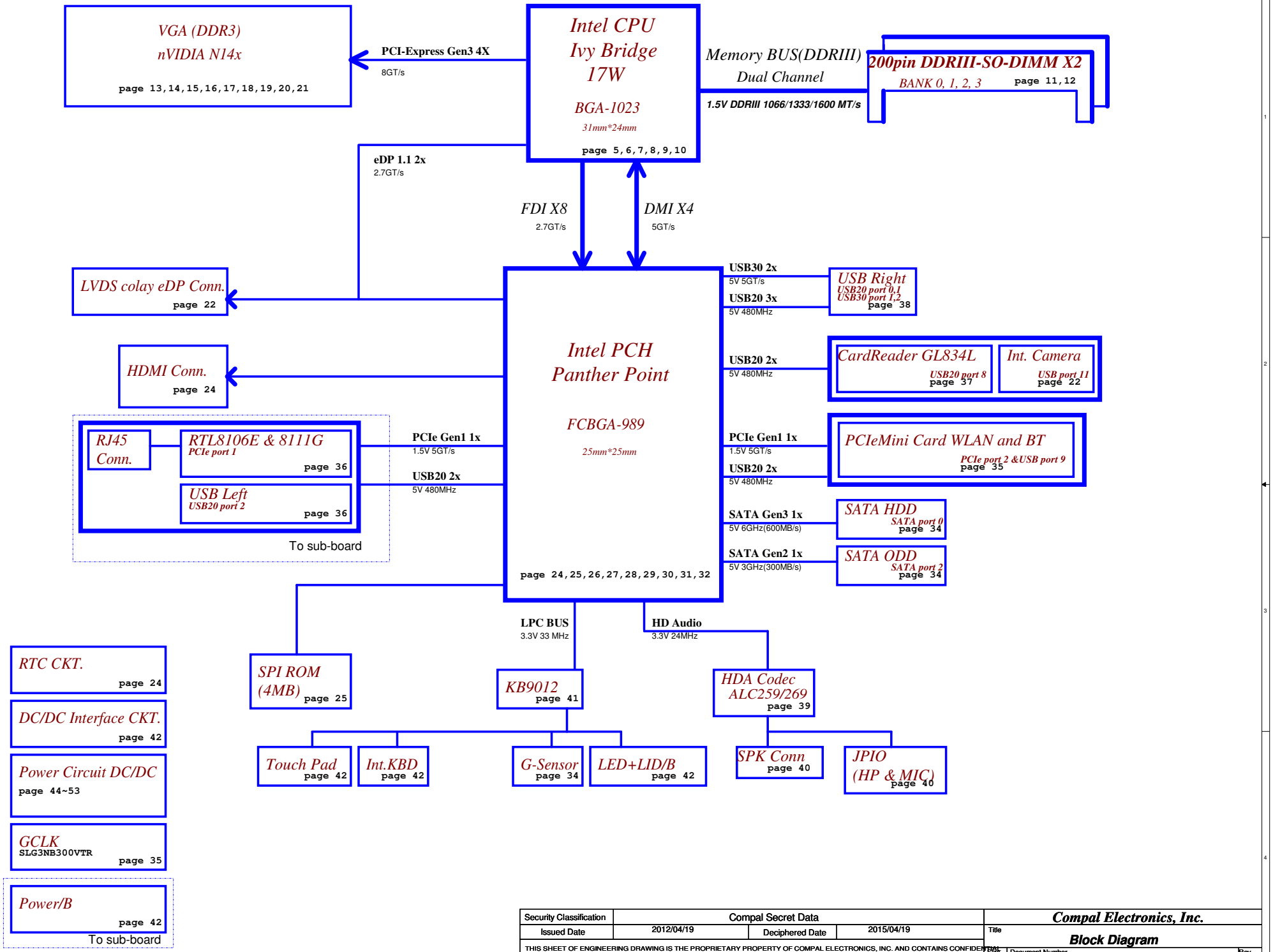

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Compal Electronics, Inc.			
Title: Block Diagram			
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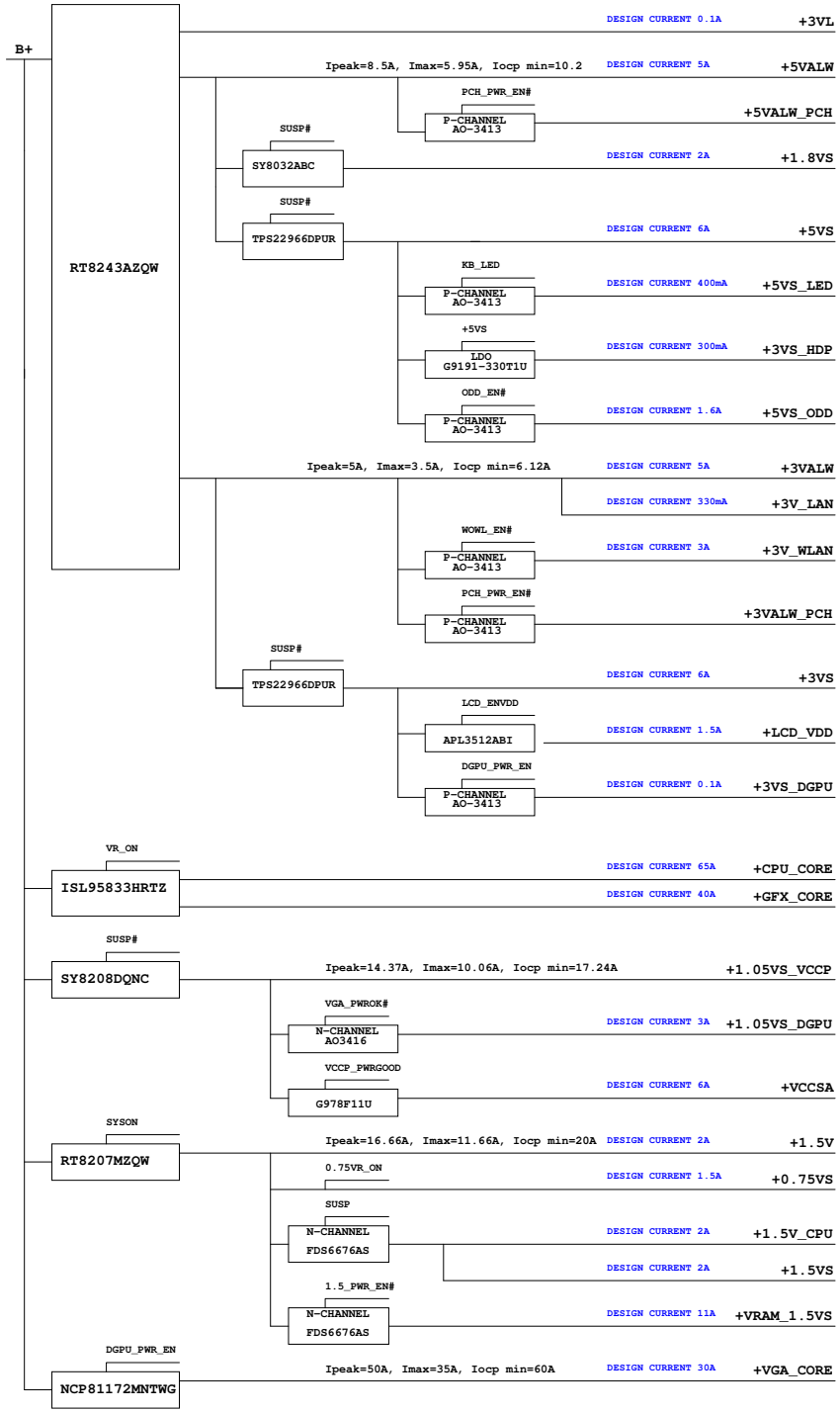

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Title: **Power Tree**

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b
+3VL	USB S&C 14640	35 H	0011 0101 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b

BTO Option Table

Function	CPU					
description	IVB i7 3537U	IVB i5 3337U	IVB i3 3227U	IVB i3 2375M	IVB P 2117U	IVB C 847
explain	IVB i7 3537U	IVB i5 3337U	IVB i3 3227U	IVB i3 2375M	IVB P 2117U	IVB C 847
BTO	CPUI73537UR1@	CPUI53337UR1@	CPUI33227UR1@	CPUI32375MR1@	CPUP2117UR1@	CPUC847R1@
	CPUI73537UR3@	CPUI53337UR3@	CPUI33227UR3@	CPUI32375MR3@	CPUP2117UR3@	CPUC847R3@

Function	SKU	PCH		GPU		VRAM	EC	
description	Optimus	Panther Point		N14M-GL	N14P-GV2	Dual Rank	EC	
explain	Optimus	HM76	HM70	N14M-GL	N14P-GV2	Dual Rank	KB9012	NPCE885N
BTO	OPT@	HM76R1@	HM70R1@	N14MGL@	N14PGV2@	DRANK@	9012@	885@
		HM76R3@	HM70R3@	N14MGLR1@ N14MGLR3@	N14PGV2R1@ N14PGV2R3@			

Function	LVDS-eDP		Camera & Mic	USB S&C		CRT			Touch Screen
description	LVDS-eDP		Camera & Mic	14640	14641	CRT			Touch Screen
explain	LVDS	eDP	Camera & Mic	14640	14641	w/ CRT		w/o CRT	Touch Screen
BTO	LVDS@	IEDP@	CAM_EMI@	14640@	14641@	CRT@	CRT_EMI@	NOCRT@	TOUCH_EMI@

Function	WOWL		G-SENSOR	ZPODD		GCLK		VRAM SKU for GV2
description	WOWL		G-SENSOR	ZPODD		GCLK	non-GCLK	Single Rank
explain	w/	w/o	G-SENSOR	w/	w/o	GCLK	non-GCLK	Single Rank
BTO	WOWL@	NOWOWL@	GSENSOR@	ZPODD@	NONZP@	GCLK@	NOGCLK@	GVSR@

Function	Sleep & Music		KB Light	EMI/ESD part		
description	Sleep & Music		KB Light	EMI/ESD part		
explain	w/ S&M	w/o S&M	KB Light	EMI/ESD part		
BTO	269@	259@	KBL@	EMI@	ESD@	

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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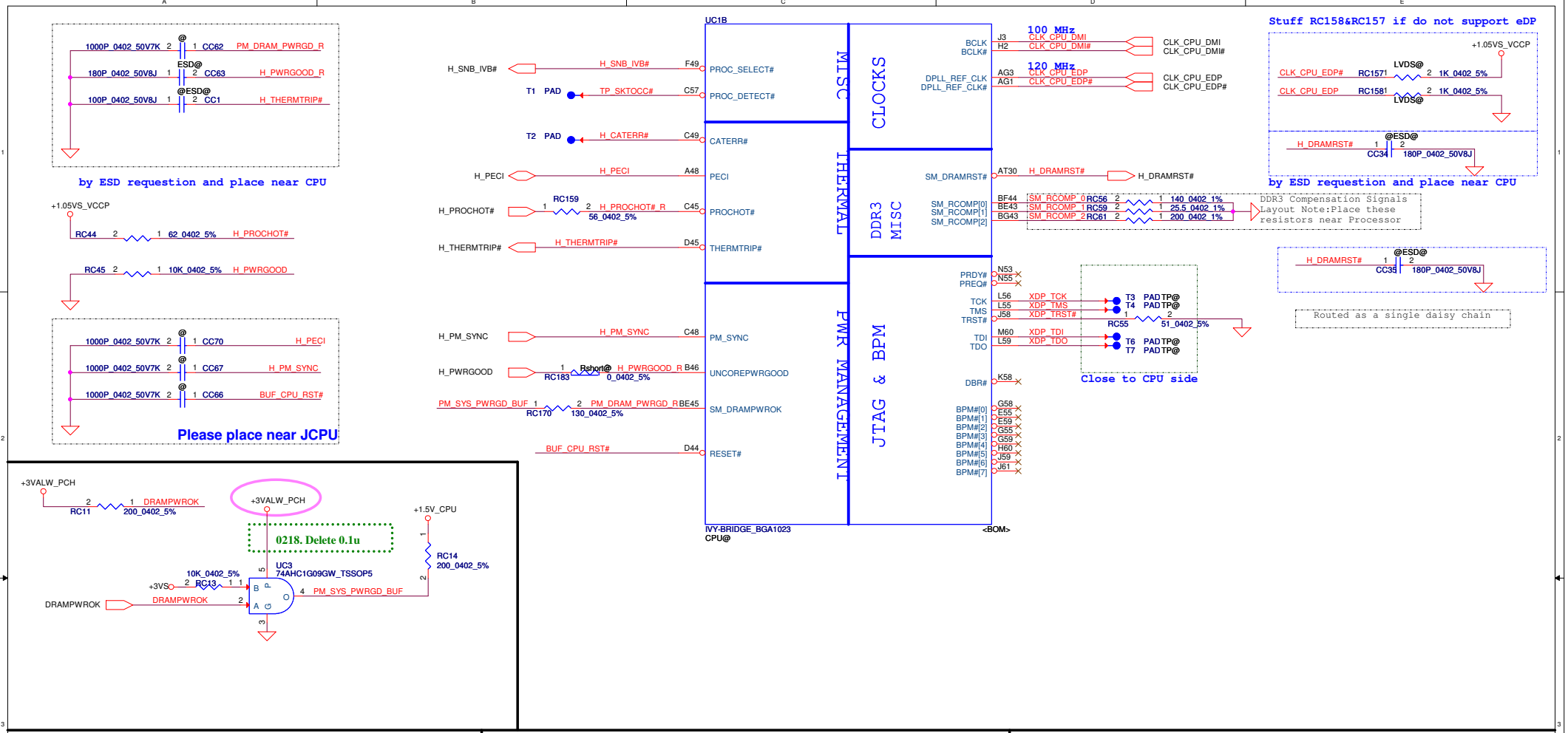
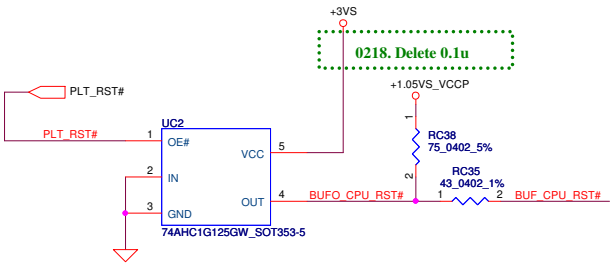
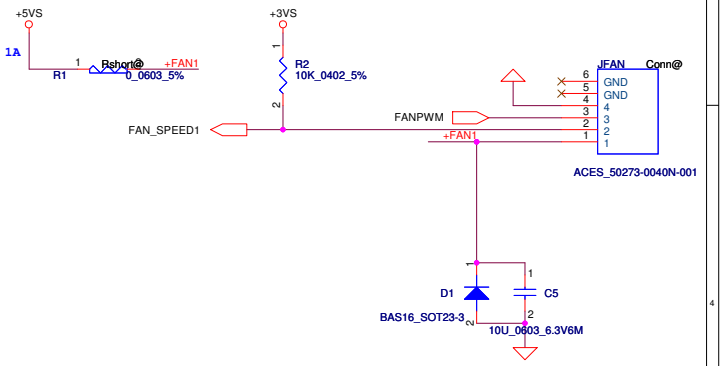


Buffered Rest to CPU



XDP Connector

FAN Control Circuit



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Title	Ivy Bridge_JTAG/XDP/FAN		
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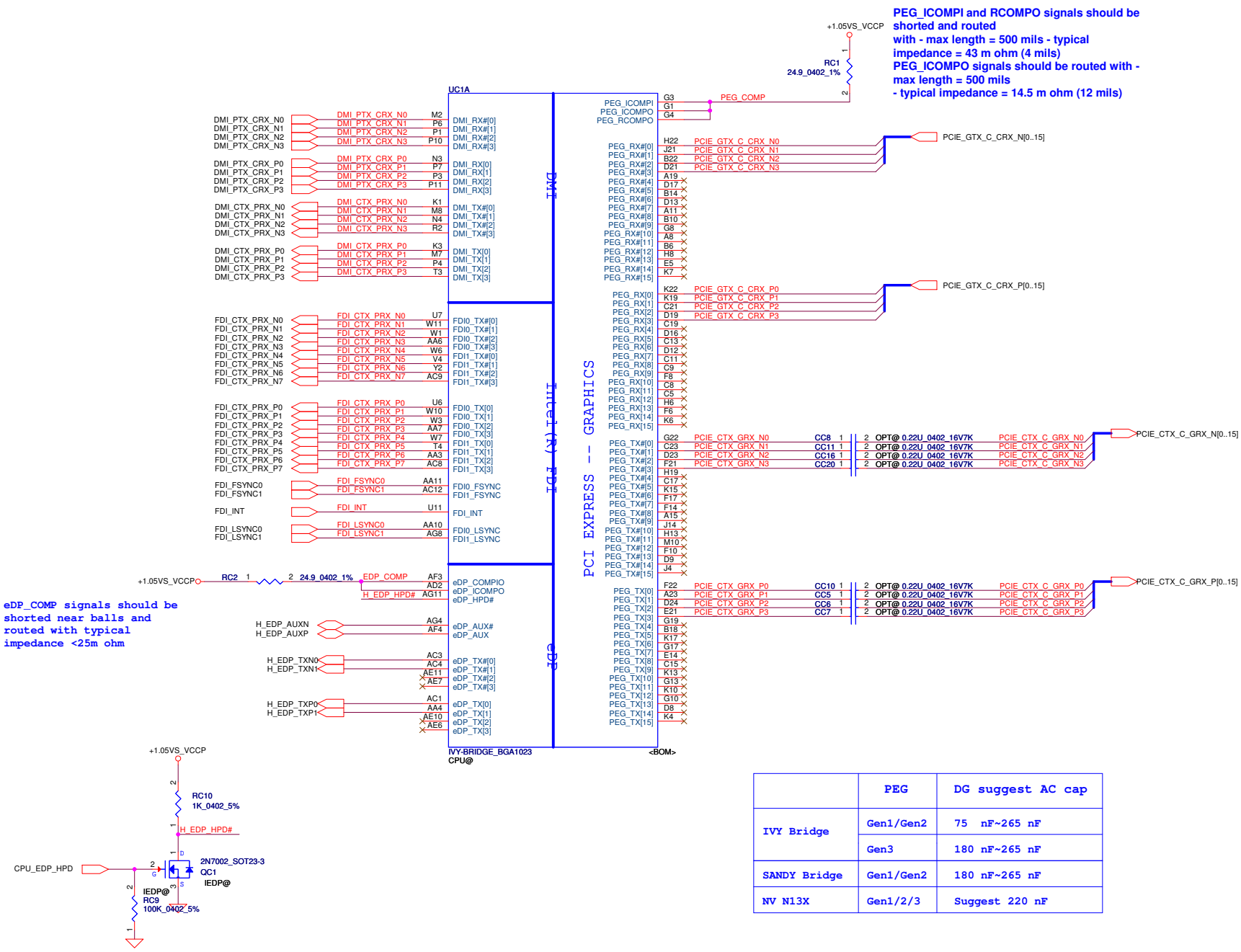

	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF~265 nF
	Gen3	180 nF~265 nF
SANDY Bridge	Gen1/Gen2	180 nF~265 nF
NV N13X	Gen1/2/3	Suggest 220 nF

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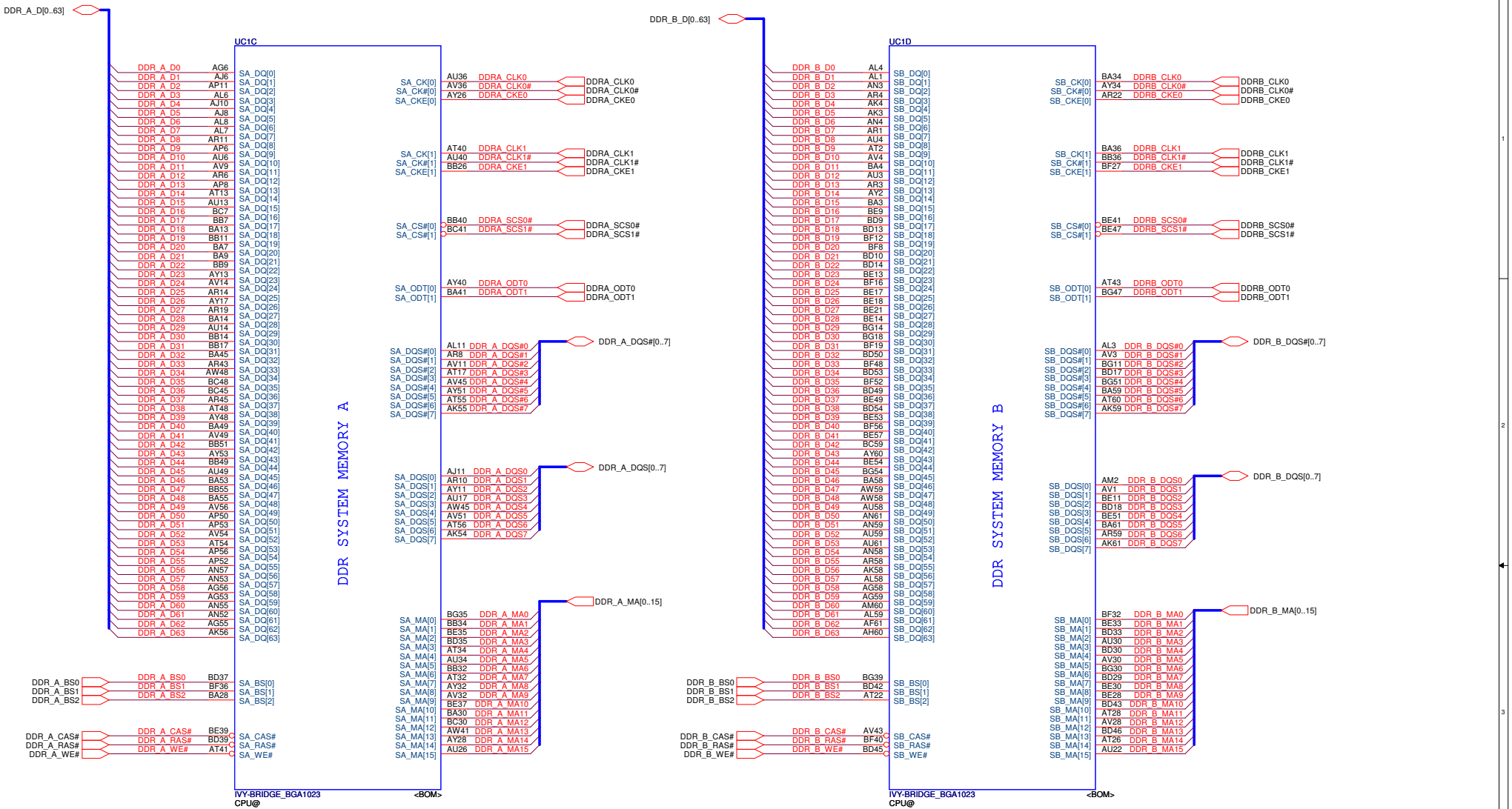

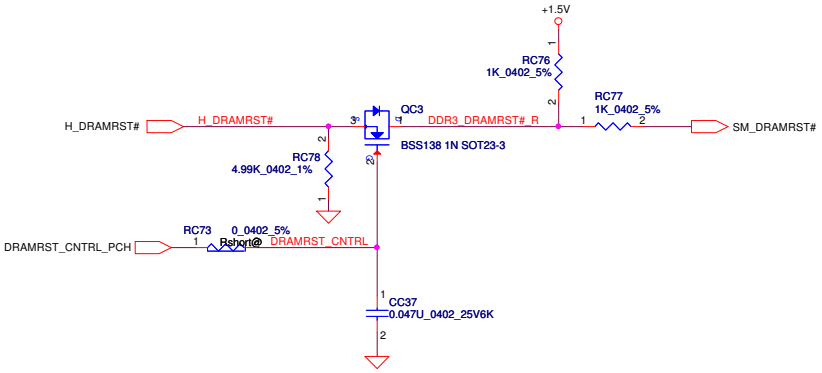

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Title	*Ivy Bridge_DDR3*
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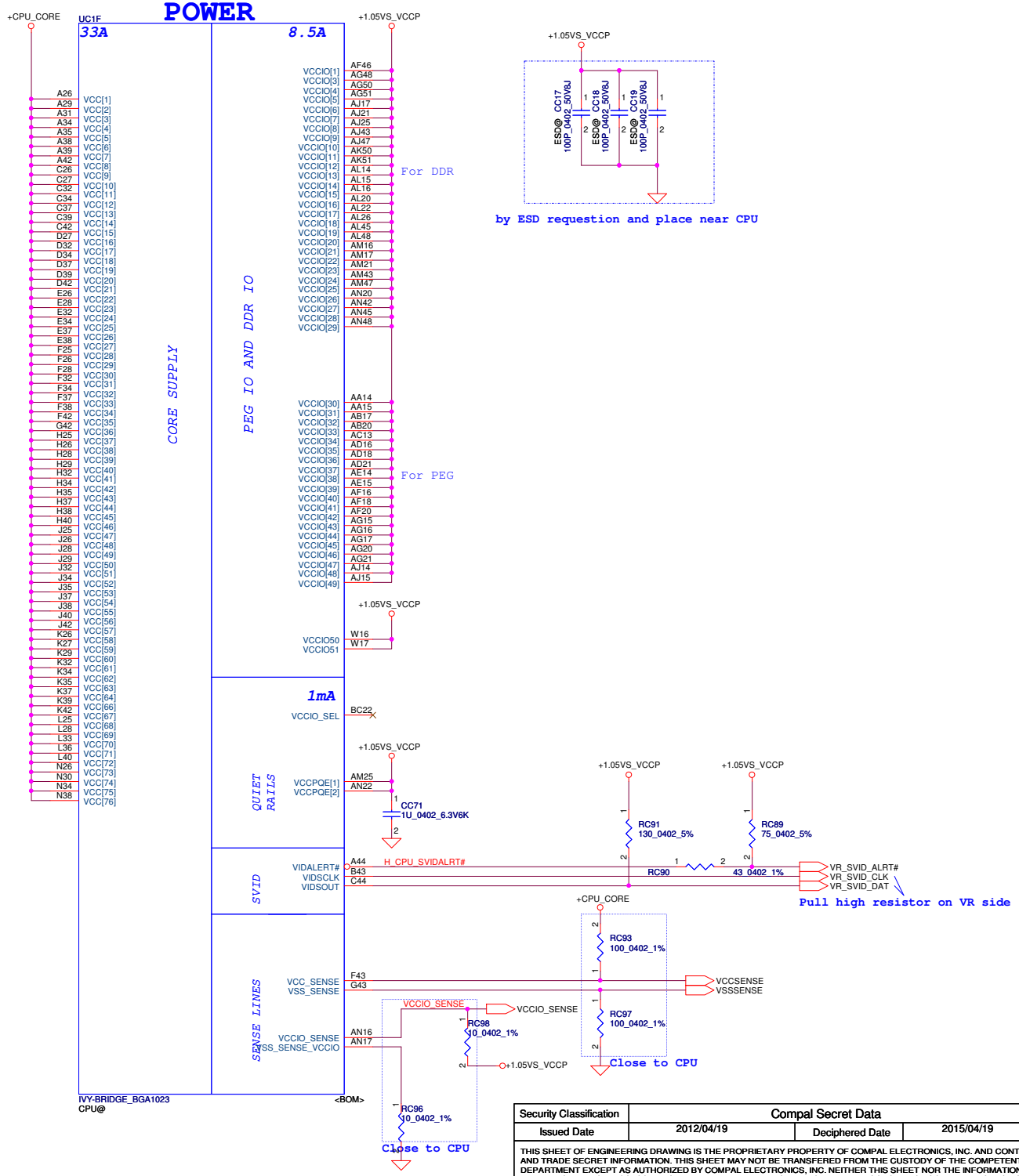
POWER



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Title: *Ivy Bridge_POWER-1*

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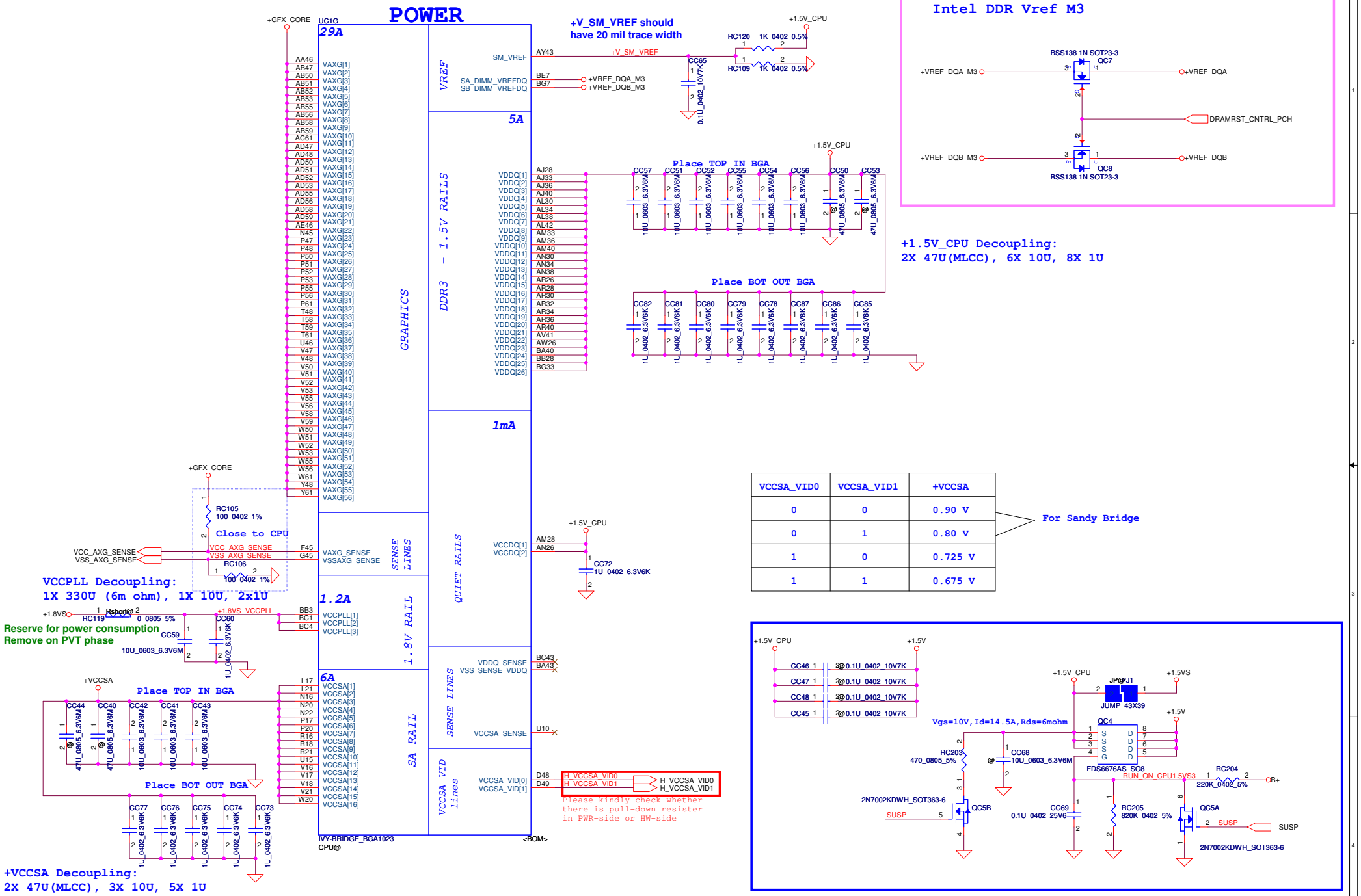
POWER



Intel DDR Vref M3

+1.5V_CPU Decoupling:
2X 47U(MLCC), 6X 10U, 8X 1U

VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge

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Title	Ivy Bridge_POWER-2
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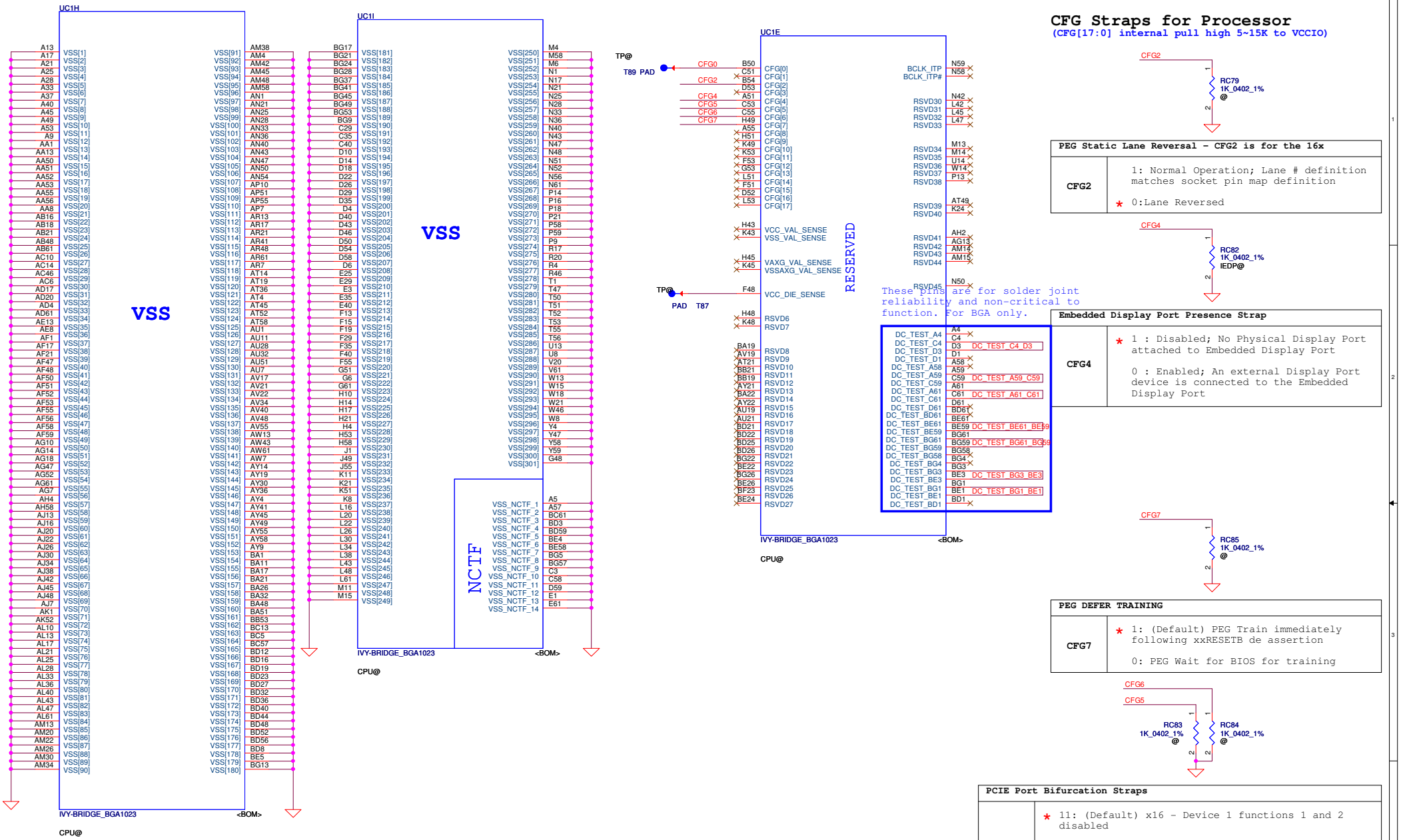

CFG Straps for Processor

(CFG[17:0] internal pull high 5~15K to VCCIO)

CFG2 — RC79 1K_0402_1% @

PEG Static Lane Reversal – CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG4 — RC82 1K_0402_1% IEDP@

Embedded Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7 — RC85 1K_0402_1% @

PEG DEFER TRAINING

CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG6 — RC83 1K_0402_1% @

CFG5 — RC84 1K_0402_1% @

PCIE Port Bifurcation Straps

CFG[6:5]	* 11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled; function 2 disabled 01: Reserved – (Device 1 function 1 disabled; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

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Title	Ivy Bridge_GND/RSVD/CFG
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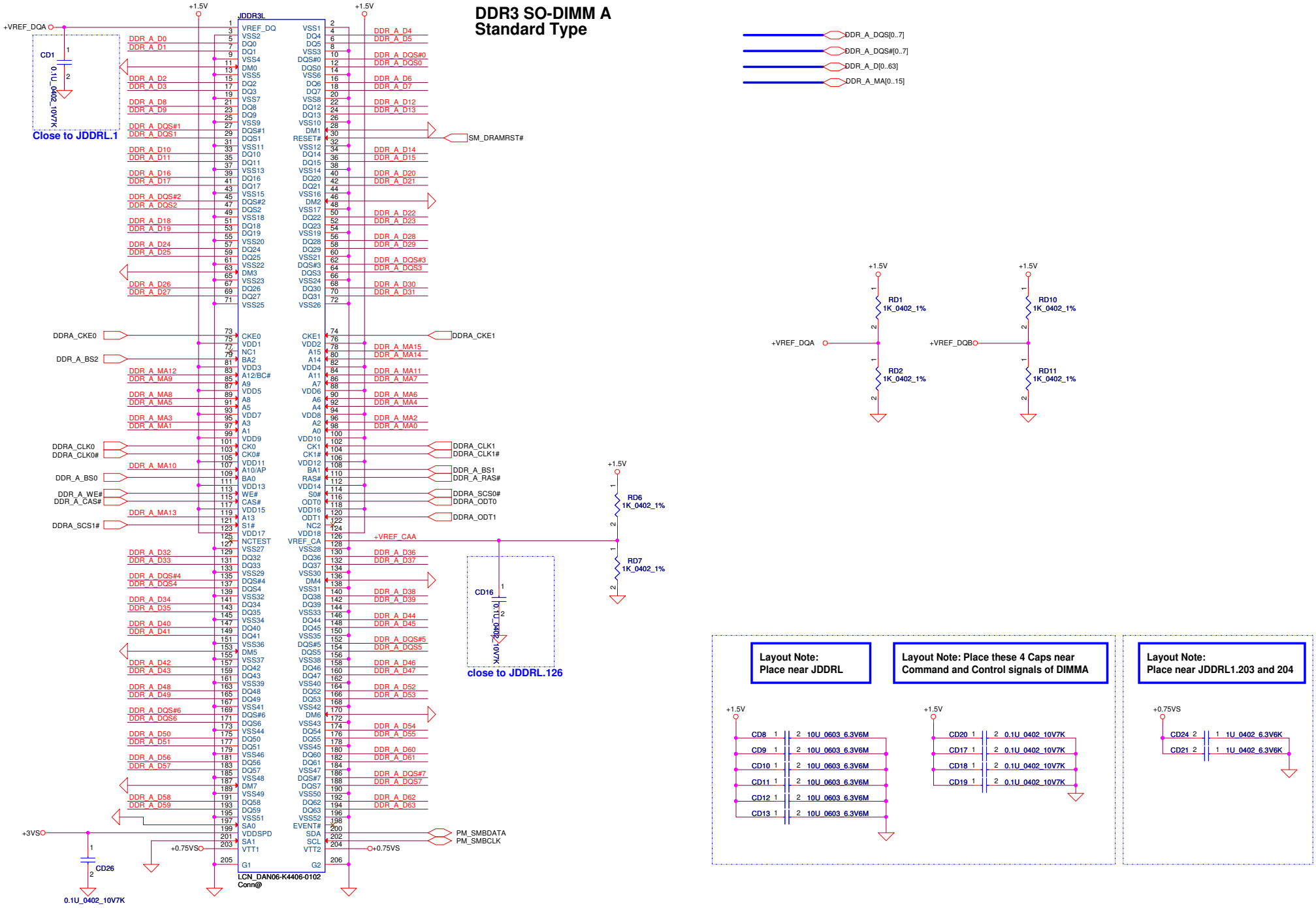
DDR3 SO-DIMM A
Standard Type



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Compal Electronics, Inc.	
Title	DDRIII-SODIMM0
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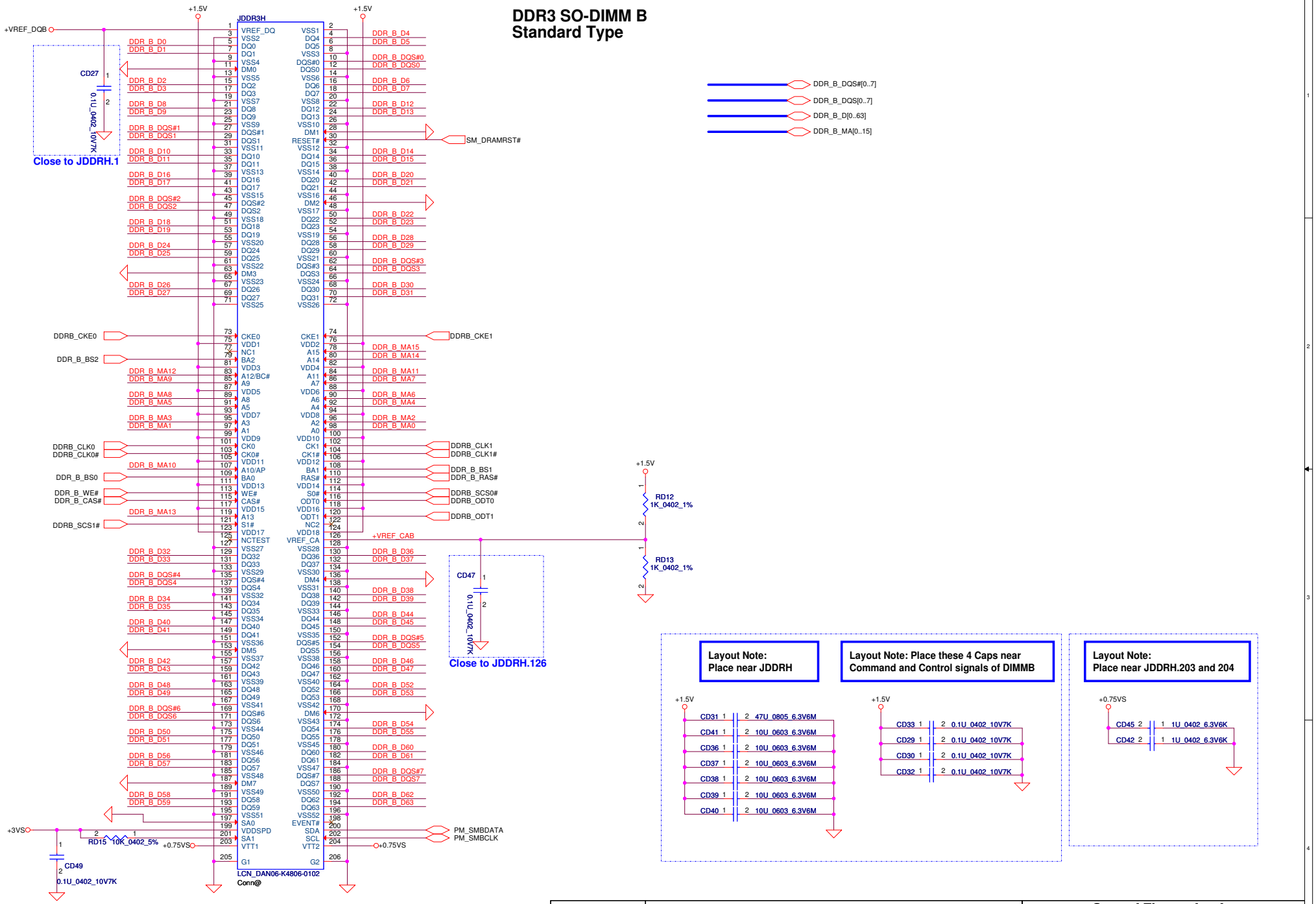
DDR3 SO-DIMM B
Standard Type



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Title: ***DDRIII-SODIMM1***

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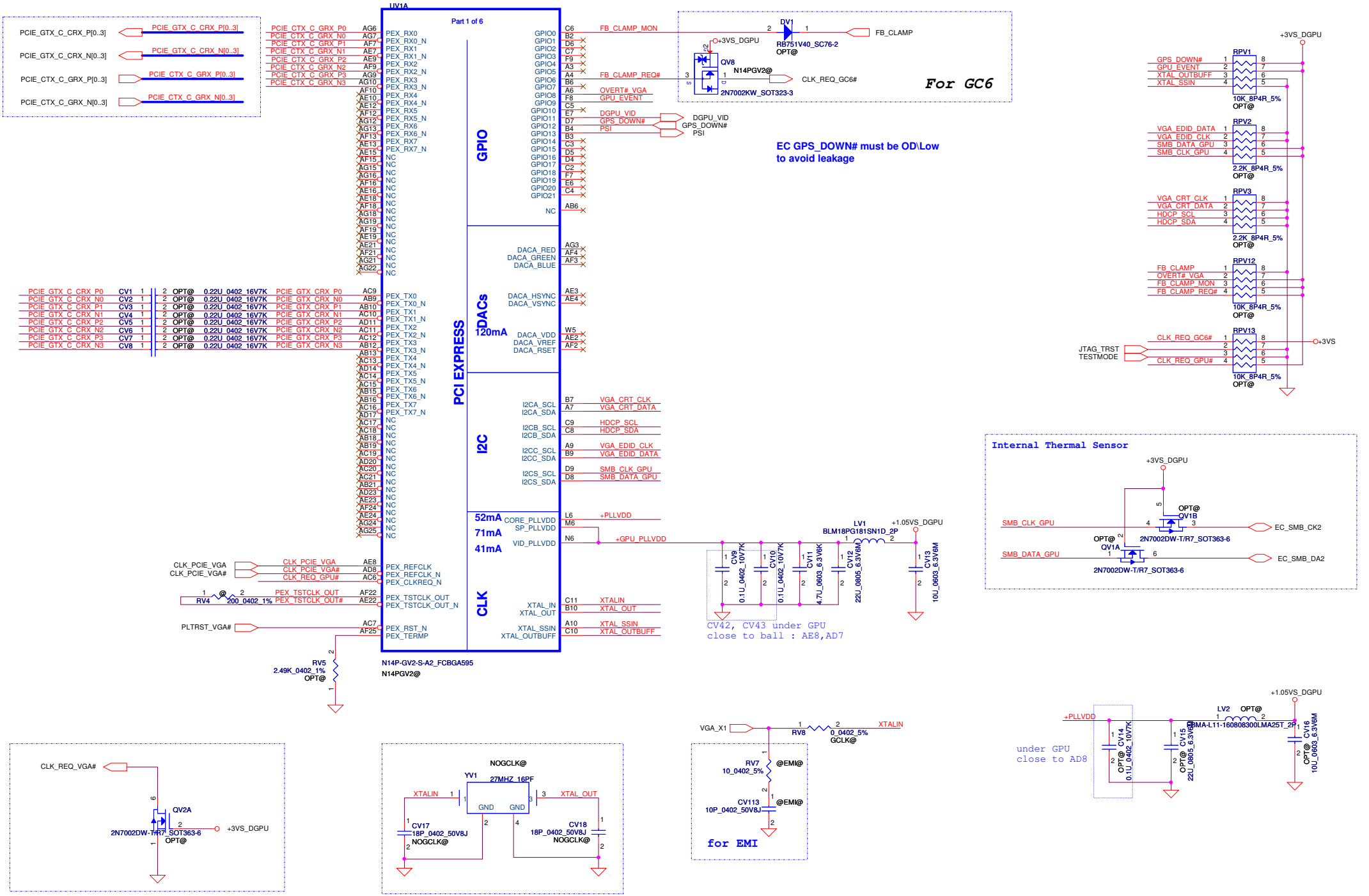

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Title	VGA_N14x PEG & DAC		
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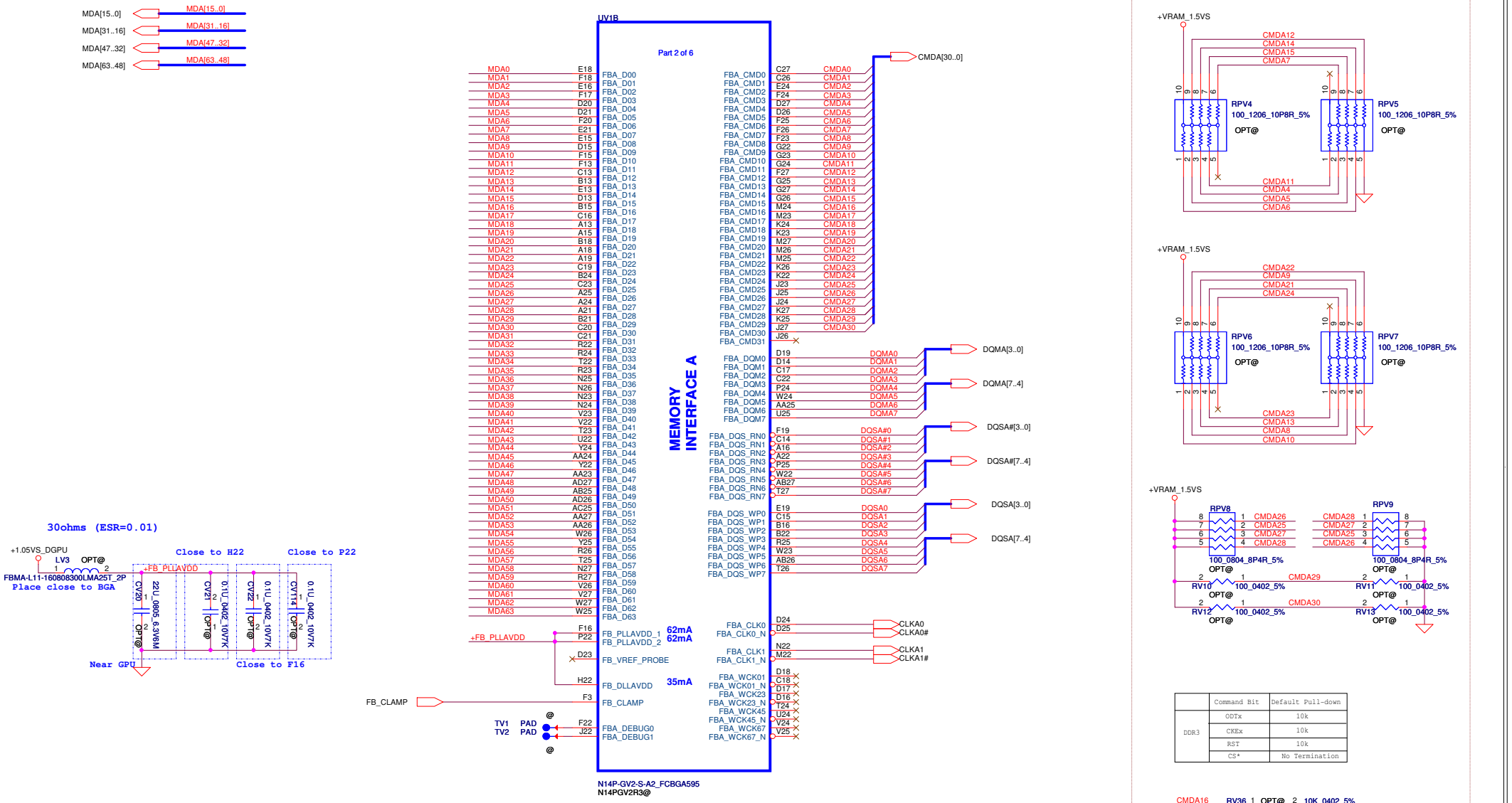
VRAM Interface



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

CMDA16	RV36	1 OPT@ 2	10K_0402_5%		
CMDA19	RV37	1 OPT@ 2	10K_0402_5%		
CMDA3	RV38	1 OPT@ 2	10K_0402_5%		
CMDA0	RV40	1 OPT@ 2	10K_0402_5%		
CMDA20	RV15	1 OPT@ 2	10K_0402_5%		

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Title: N14x VRAM Interface			
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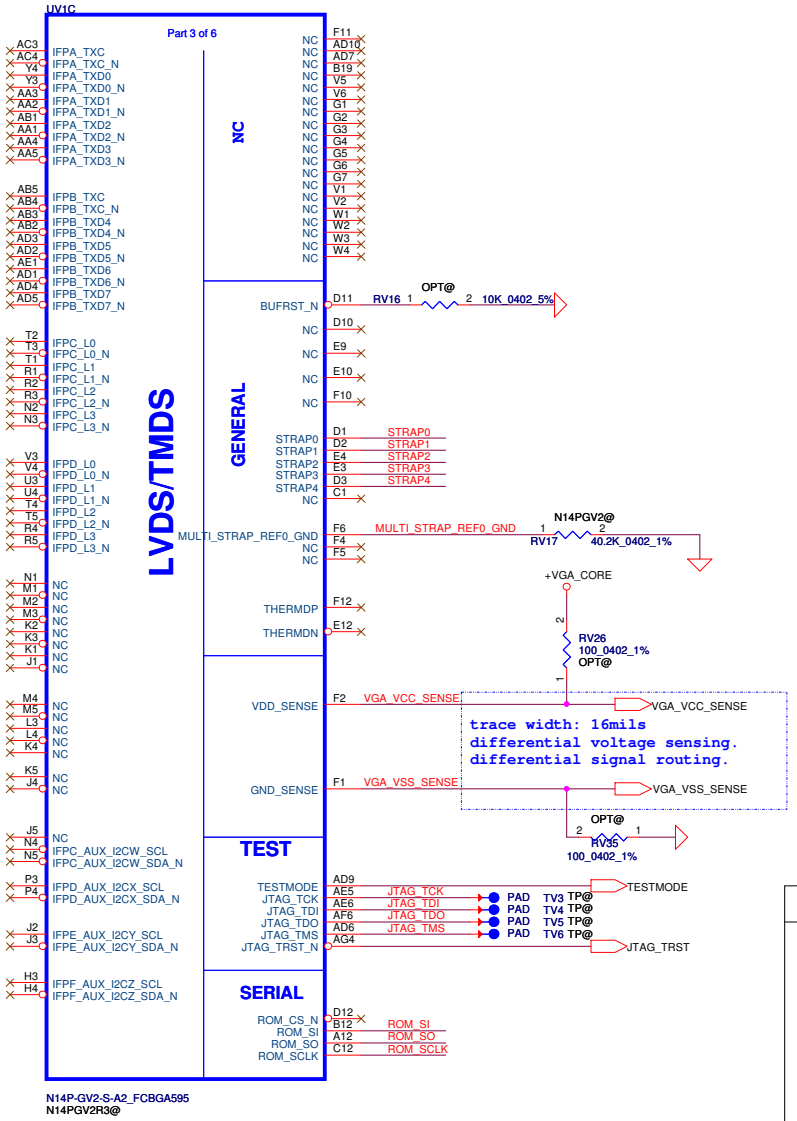
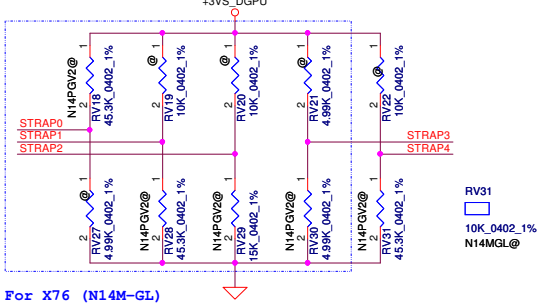


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	**PCI_DEVID[4]**	SUB_VENDOR	**PCI_DEVID[5]**	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	**RAMCFG[3]**	**RAMCFG[2]**	**RAMCFG[1]**	**RAMCFG[0]**
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	**PCI_DEVID[3]**	**PCI_DEVID[2]**	**PCI_DEVID[1]**	**PCI_DEVID[0]**
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

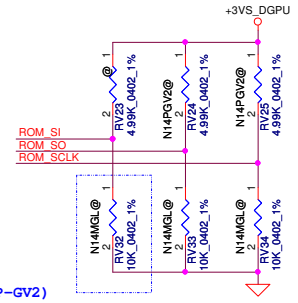
SKU	Device ID	biit5 to bit0
N14P-GV2	TBD	010010
N14M-GL	0x1140	000000

Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

MULTI LEVEL STRAPS



For X76 (N14M-GL)



For X76 (N14P-GV2)

GPU		FB Memory gDDR3			ROM_SI
N14P-GV2	128Mx16	Samsung	900MHz	K4W2G1646E-BC11	PD 45K
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	PD 34.8K
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	PD 30K
	256Mx16	Samsung	900MHz	K4W4G1646B-HC11	PD 20K
		Micron	900MHz	MT41K256M16HA-107G	PD 10K

GPU		FB Memory gDDR3			STRAP[3:0]
N14M-GL	128Mx16	Samsung	900MHz	K4W2G1646E-BC11	0101
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	0110
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	0001
	256Mx16	Samsung	900MHz	K4W4G1646B-HC11	1011
		Hynix	900MHz	H5TC4G63AFR-11C	0100
		Micron	900MHz	MT41K256M16HA-107G	1101

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Title: VGA_N14x LVDS&TMDS

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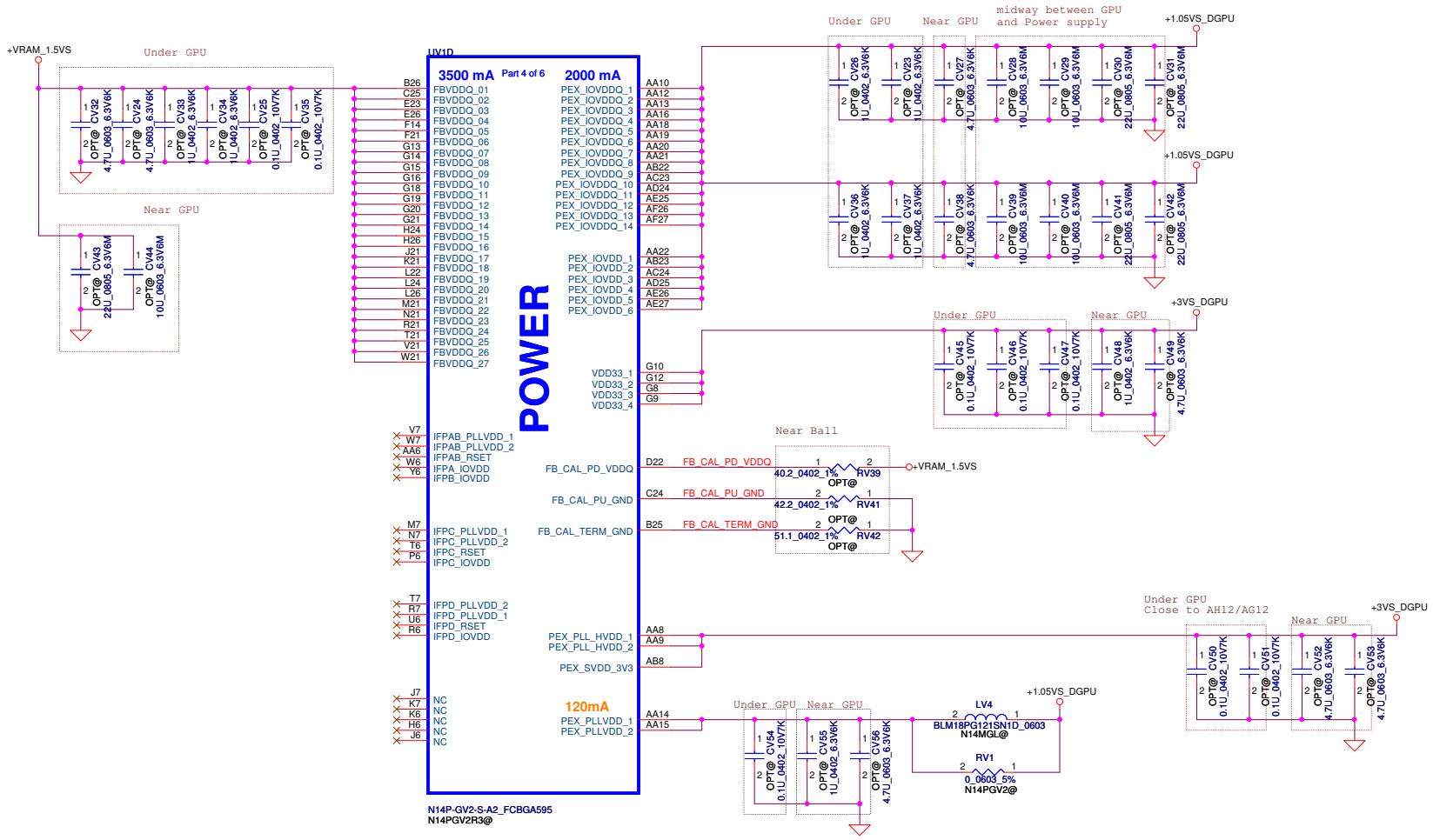

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Title: **VGA_N14x POWER**

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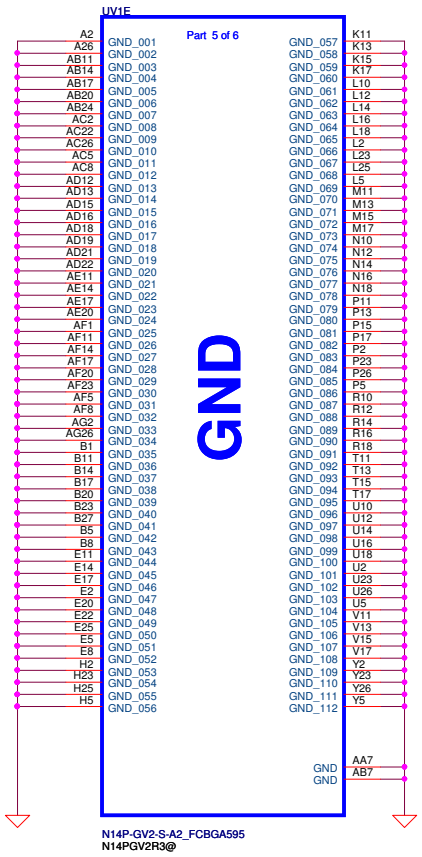
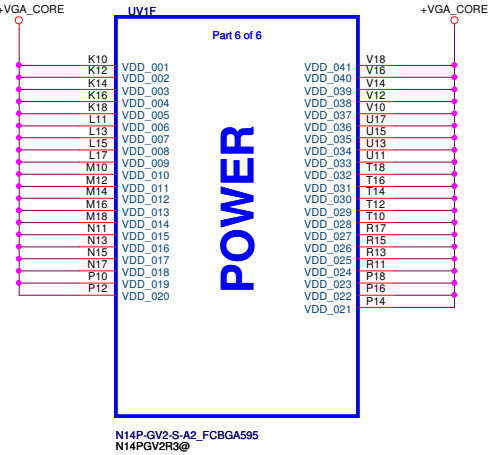
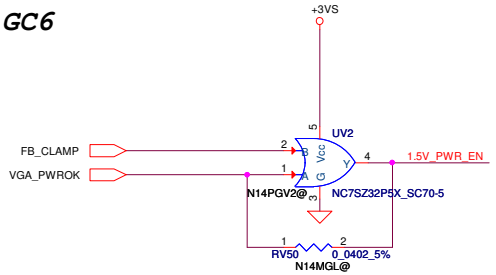
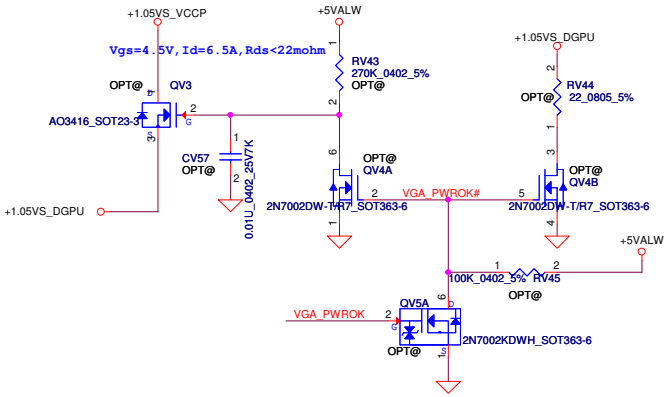




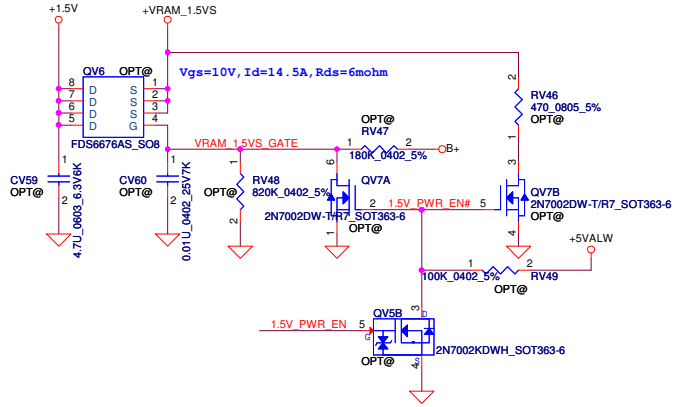
For GC6



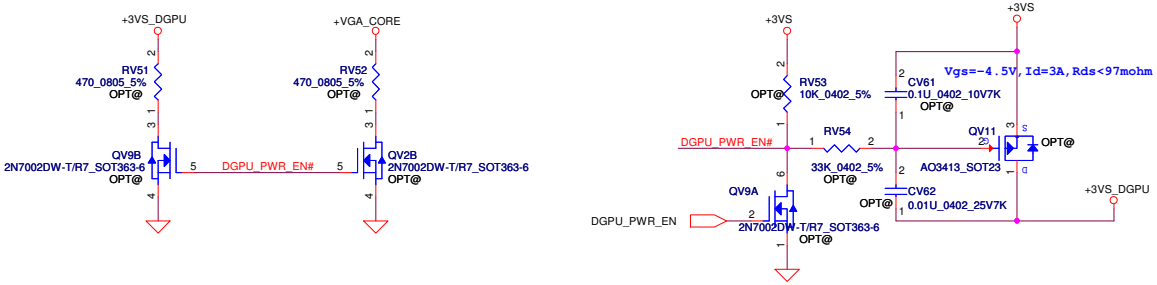
+1.05VS_VCCP to +1.05VS_DGPU



+1.5V to +VRAM_1.5VS



+3VS to +3VS_DGPU



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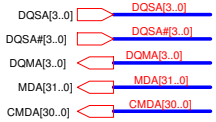
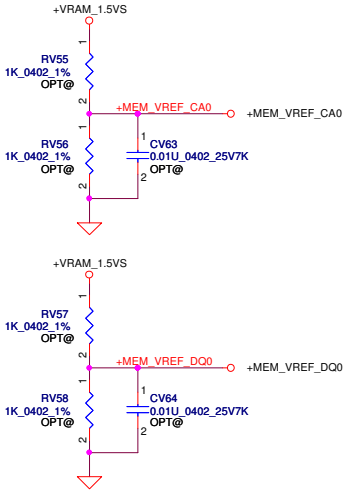
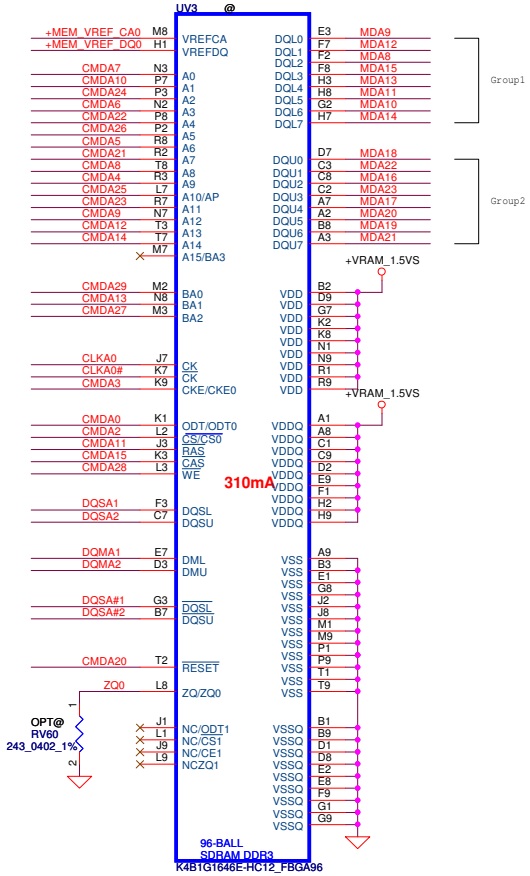
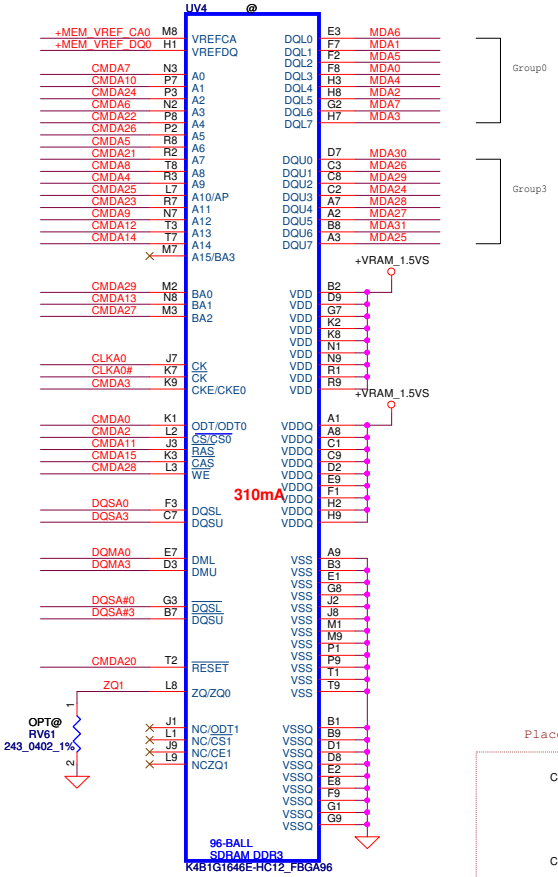
RANK 0 [31...0]

VRAM DDR3 Chips



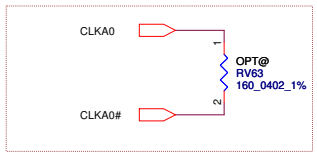




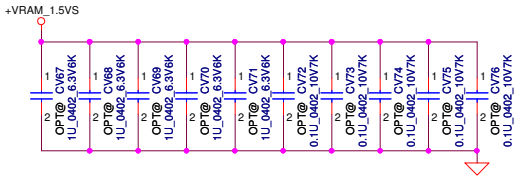


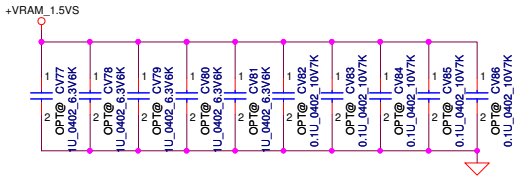
Mode E Address	Rank 0 0..31	Rank 0 32..63	Rank 1 0..31	Rank 1 32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

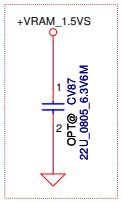
Place close to the first T point



Place close to RANK0 VRAM





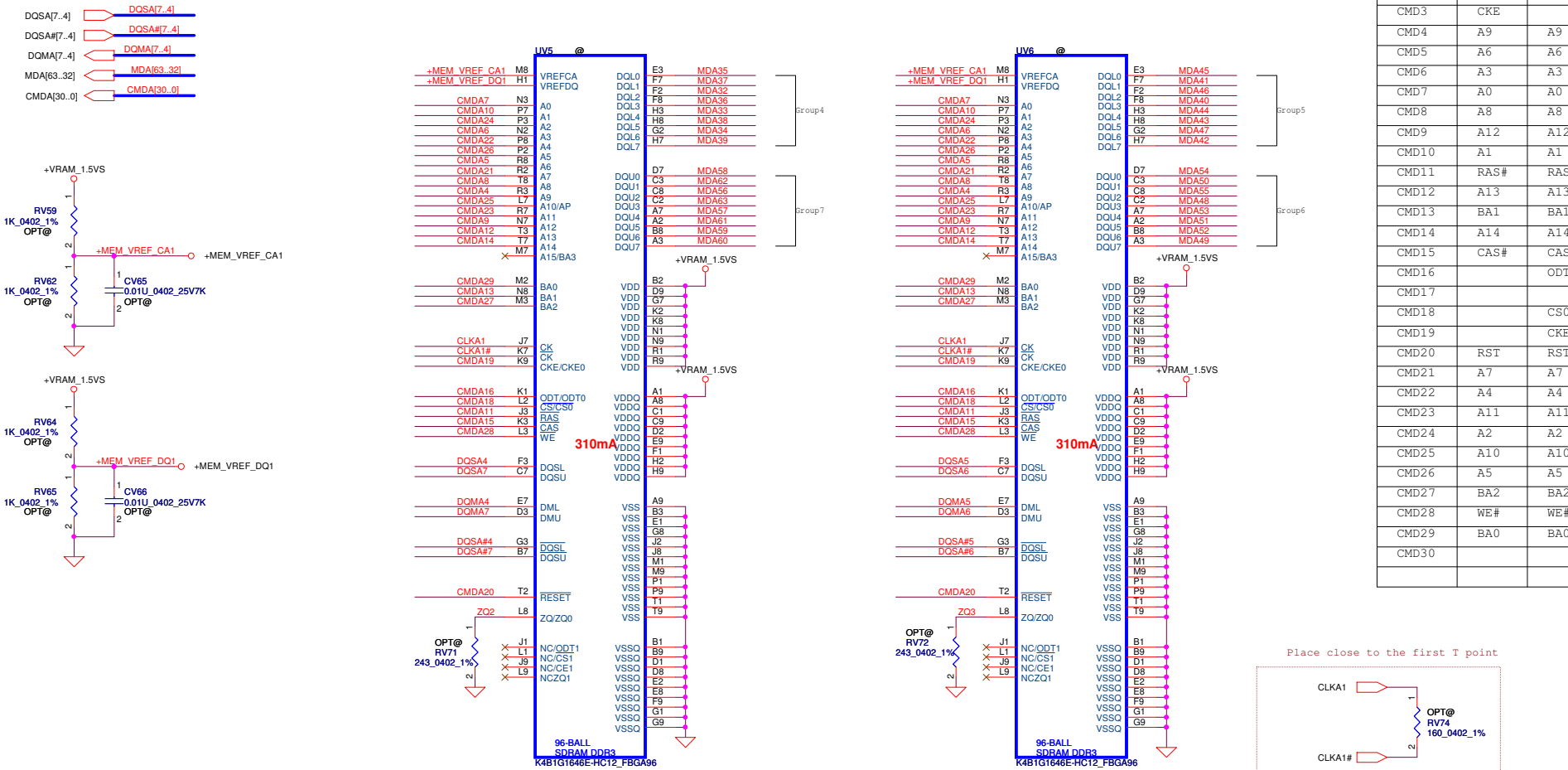


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/28	Deciphered Date 2013/09/28	Title: VGA_N14x VRAM RANK 0L
Size: Custom	Document Number		Rev: 1.0
Date: Monday, March 11, 2013	Sheet 18 of 56		

RANK 0 [63...32]

VRAM DDR3 Chips

Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

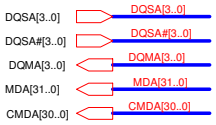
Title: **VGA_N14x VRAM RANK 0H**

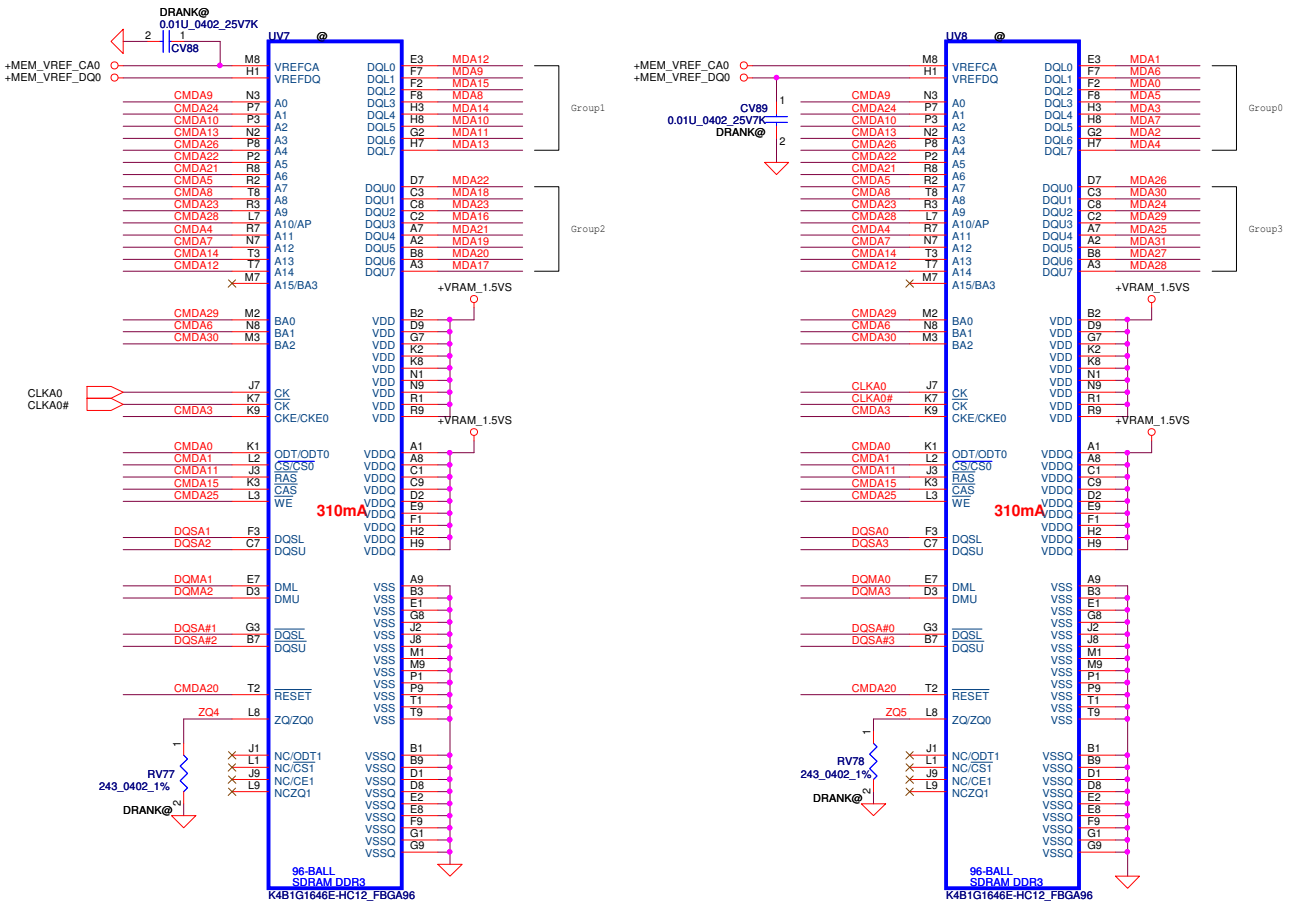
Size	Document Number	Rev
Custom		1.0

Date: Monday, March 11, 2013 Sheet 19 of 56

RANK 1 [31...0]

VRAM DDR3 Chips





Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Compal Electronics, Inc.

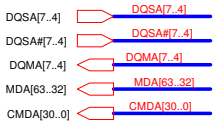
Title: VGA_N14x VRAM RANK 1L

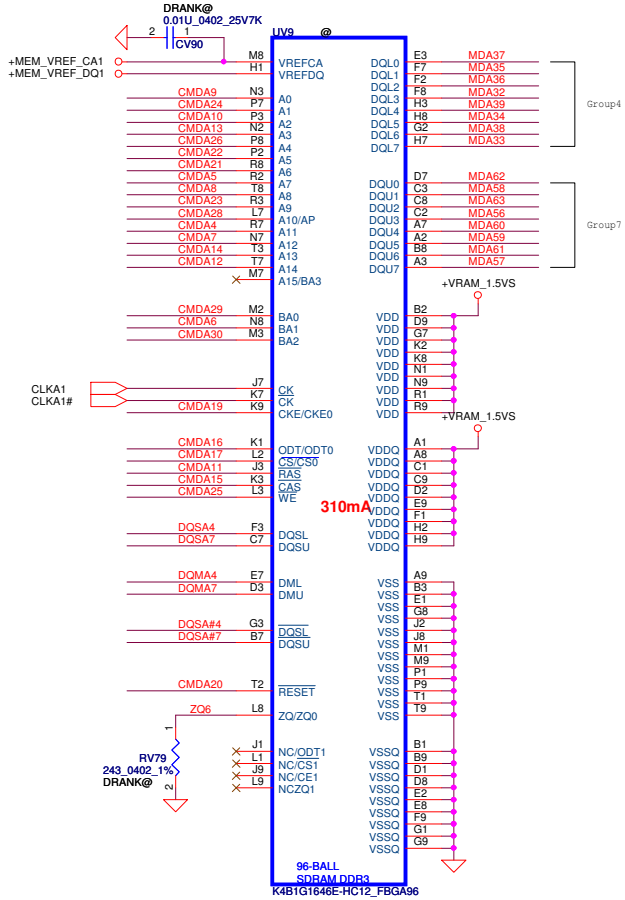
Size: Custom | Document Number | Rev: 1.0

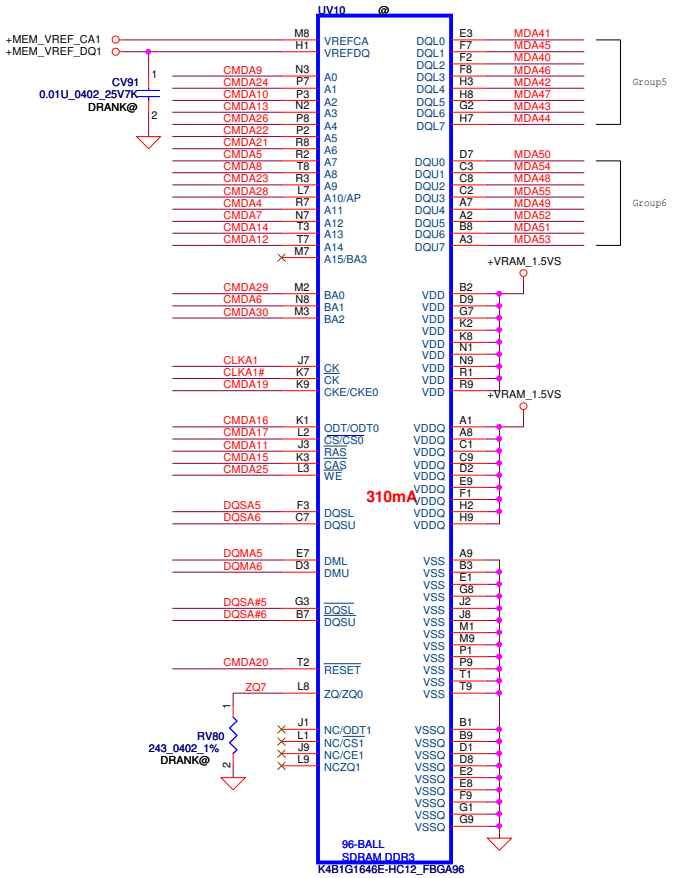
Date: Monday, March 11, 2013 | Sheet 20 of 56

RANK 1 [63...32]

VRAM DDR3 Chips







Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

Title: VGA_N14x VRAM RANK 1H

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Custom		1.0

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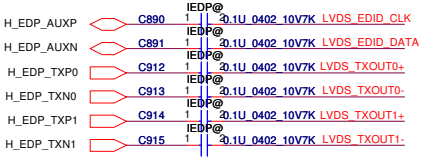
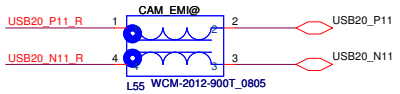
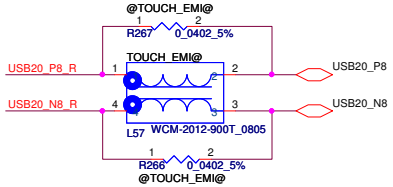
For eDP Panel



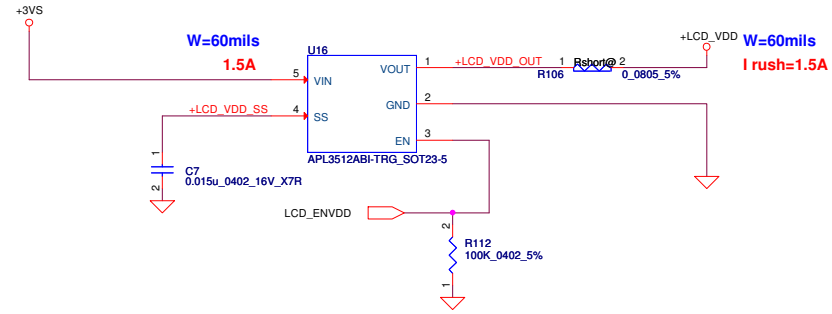


Reserve for EMI request



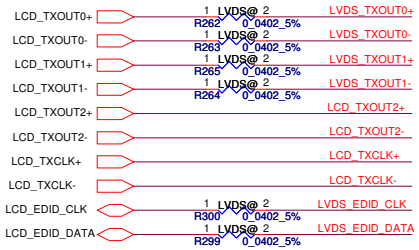
LCD POWER CIRCUIT

Need check eDP&LVDS both 3V power rail.



Reserve for EMI request

For LVDS 1ch Panel



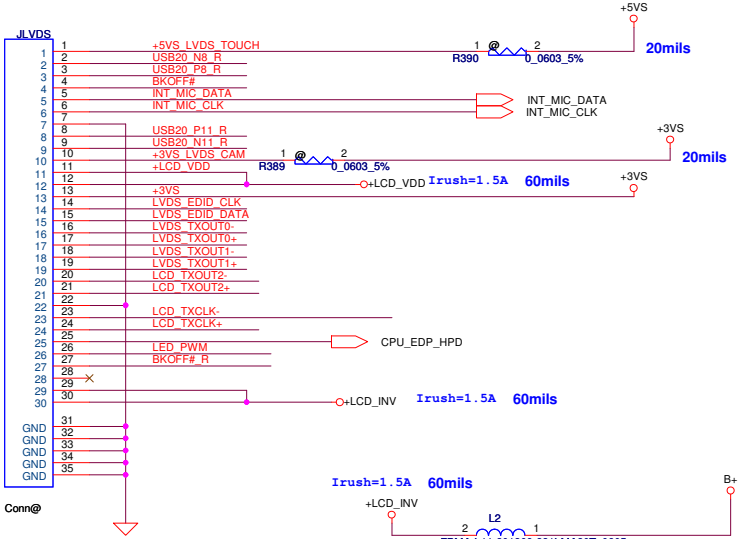
LVDS colay eDP cable

Pin define will be change after ME ready

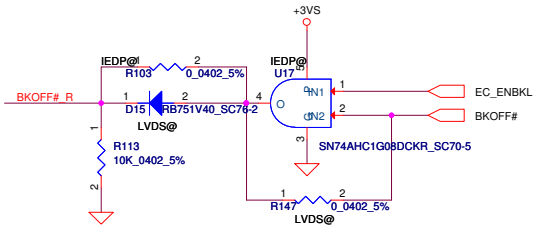
pin1-4 Touch function for panel

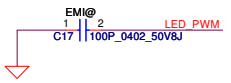
pin5-10 For Webcam with single or dual MIC

pin11-30 For LVDS or EDP panel

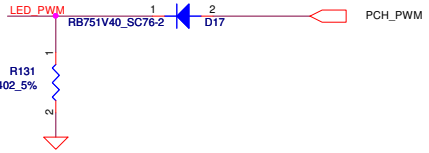


Reserve for eDP panel potential issue





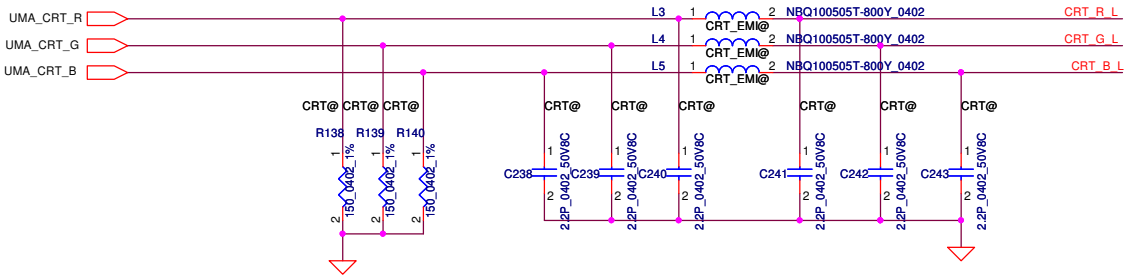
For EMI request , cut in on PVT phase.
Place close CONN.

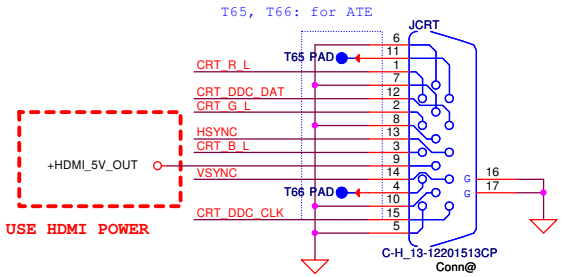


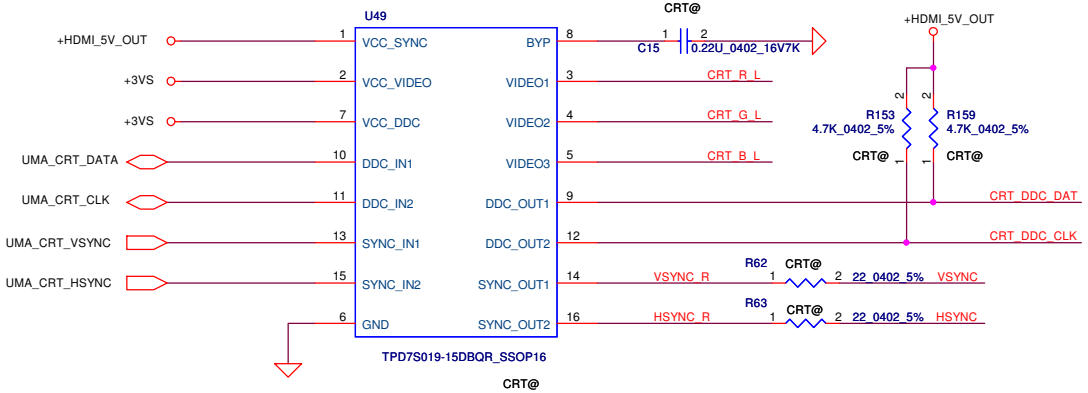
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/24	Deciphered Date 2013/09/24	Title: LVDS

Size: Custom	Document Number: VFKTA		Rev: 1.0
Date: Monday, March 11, 2013	Sheet 22 of 56		

CRT CONNECTOR







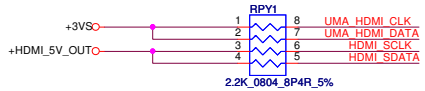
Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: *CRT*

Size | Document Number: **VFKTA** | Rev: 1.0

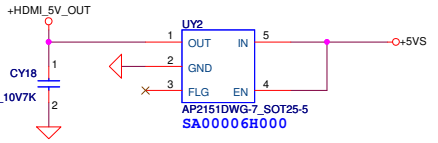
Date: Monday, March 11, 2013 | Sheet 23 of 56

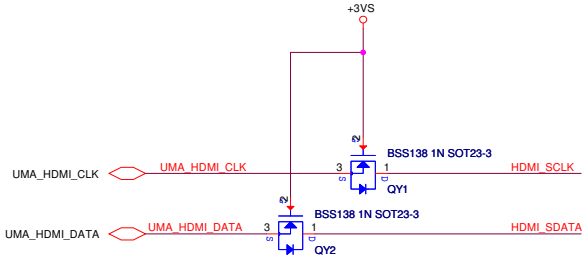


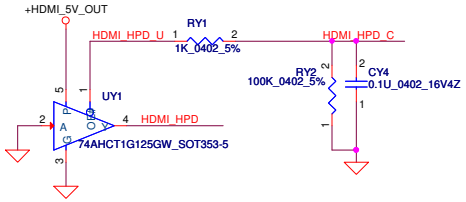
OE#	A	Y
L	L	L
L	H	H
H	X	Z

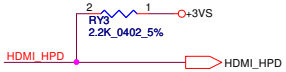
HDMI POWER CIRCUIT

VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A

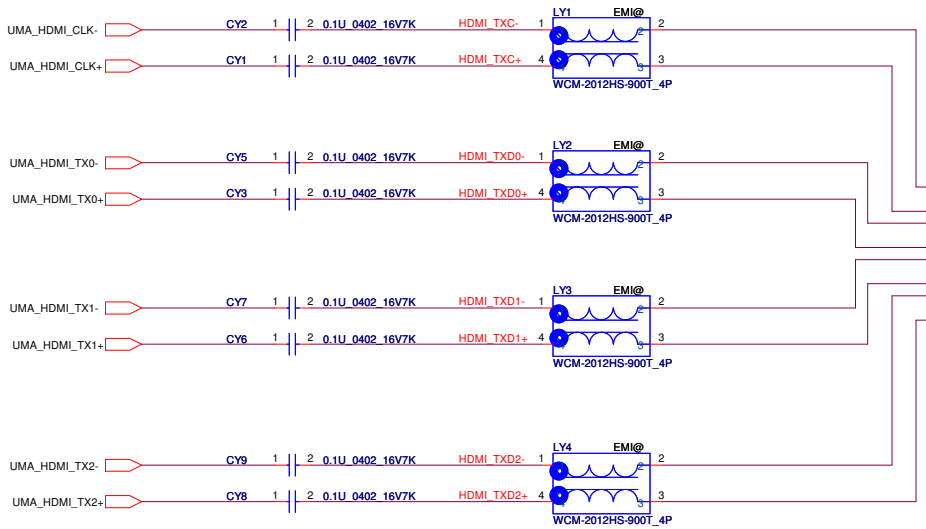


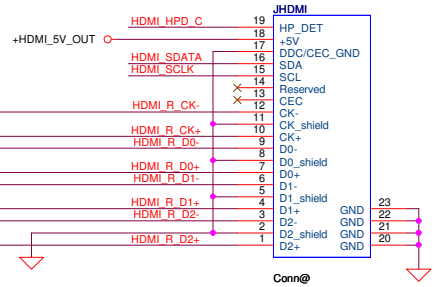


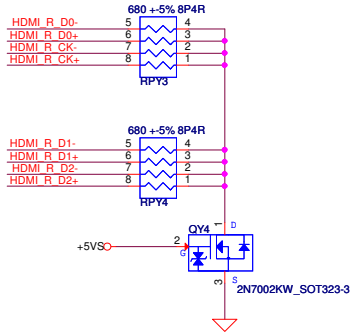




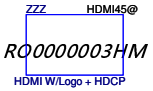
HDMI Connector







HDMI Royalty



HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

please manually load
this virtual material to 45@ BOM

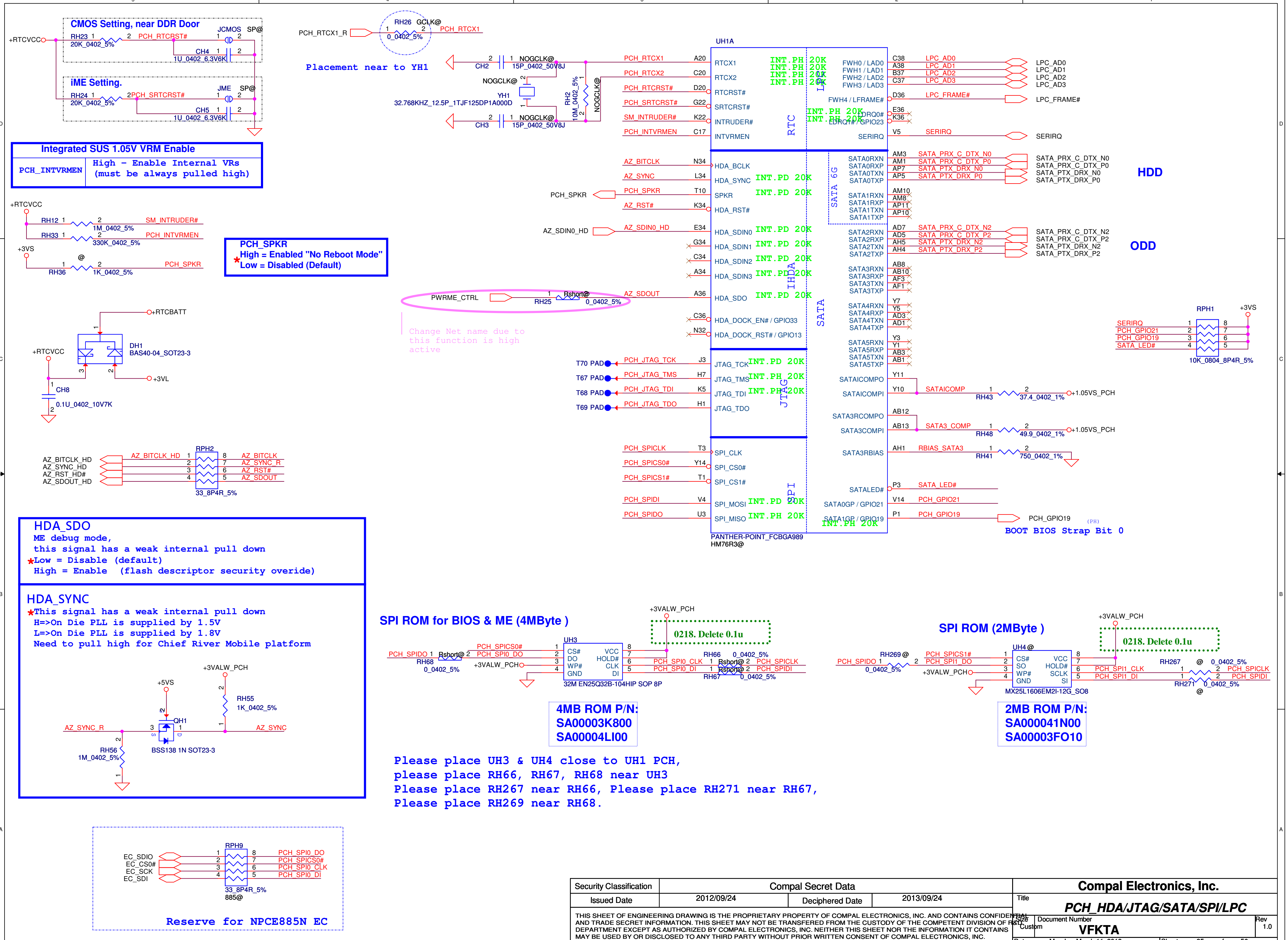
Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

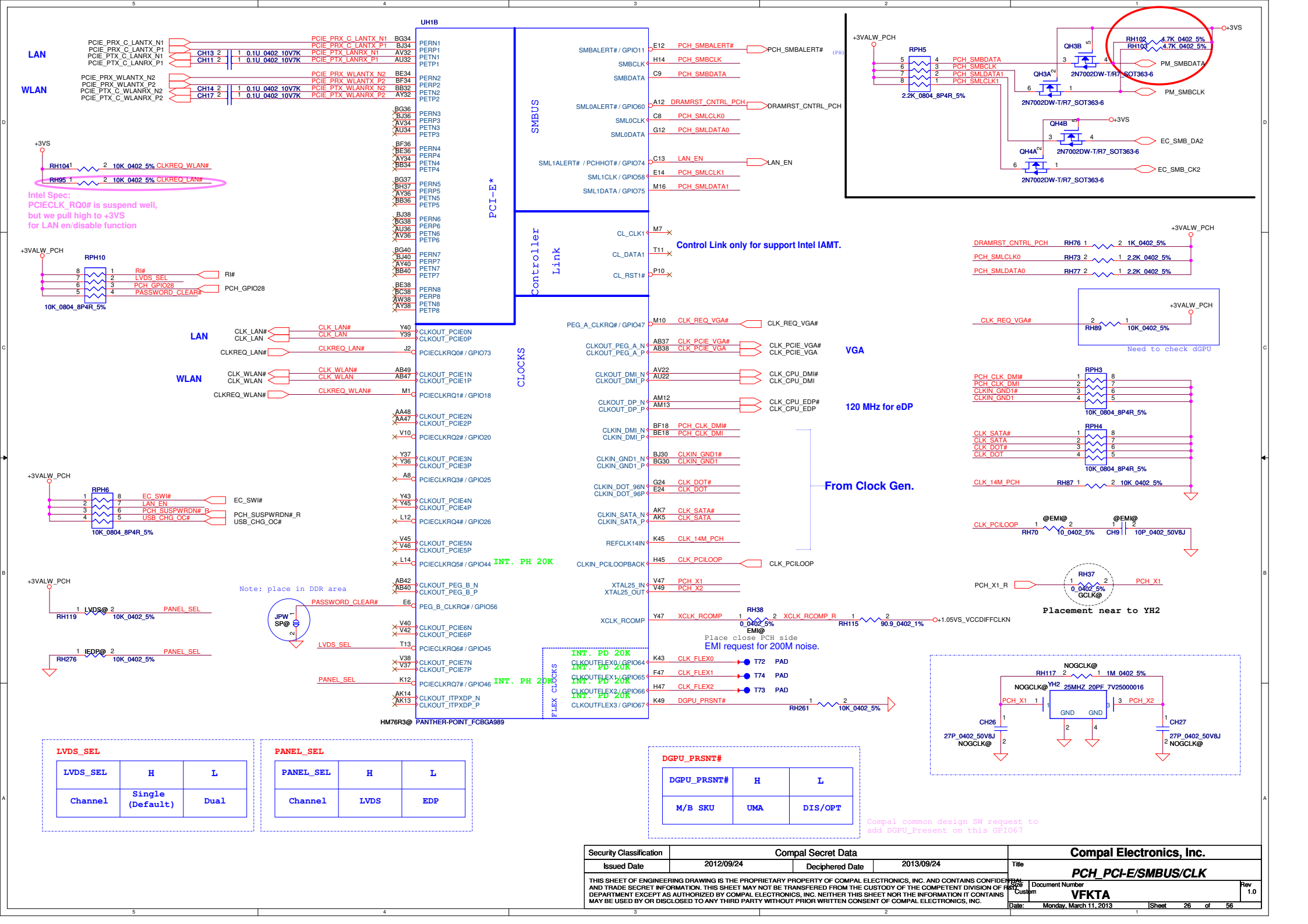
Title: ***HDMI Conn.***

Size: B | Document Number: VFKTA | Rev: 1.0

Date: Monday, March 11, 2013 | Sheet 24 of 56



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title: PCH_HDA/JTAG/SATA/SPI/LPC
Size: Custom	Document Number: VFKTA			Rev 1.0
Date: Monday, March 11, 2013	Sheet 25 of 56			



Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: *PCH_PCI-E/SMBUS/CLK*

Size	Document Number	Rev
Custom	VFKTA	1.0

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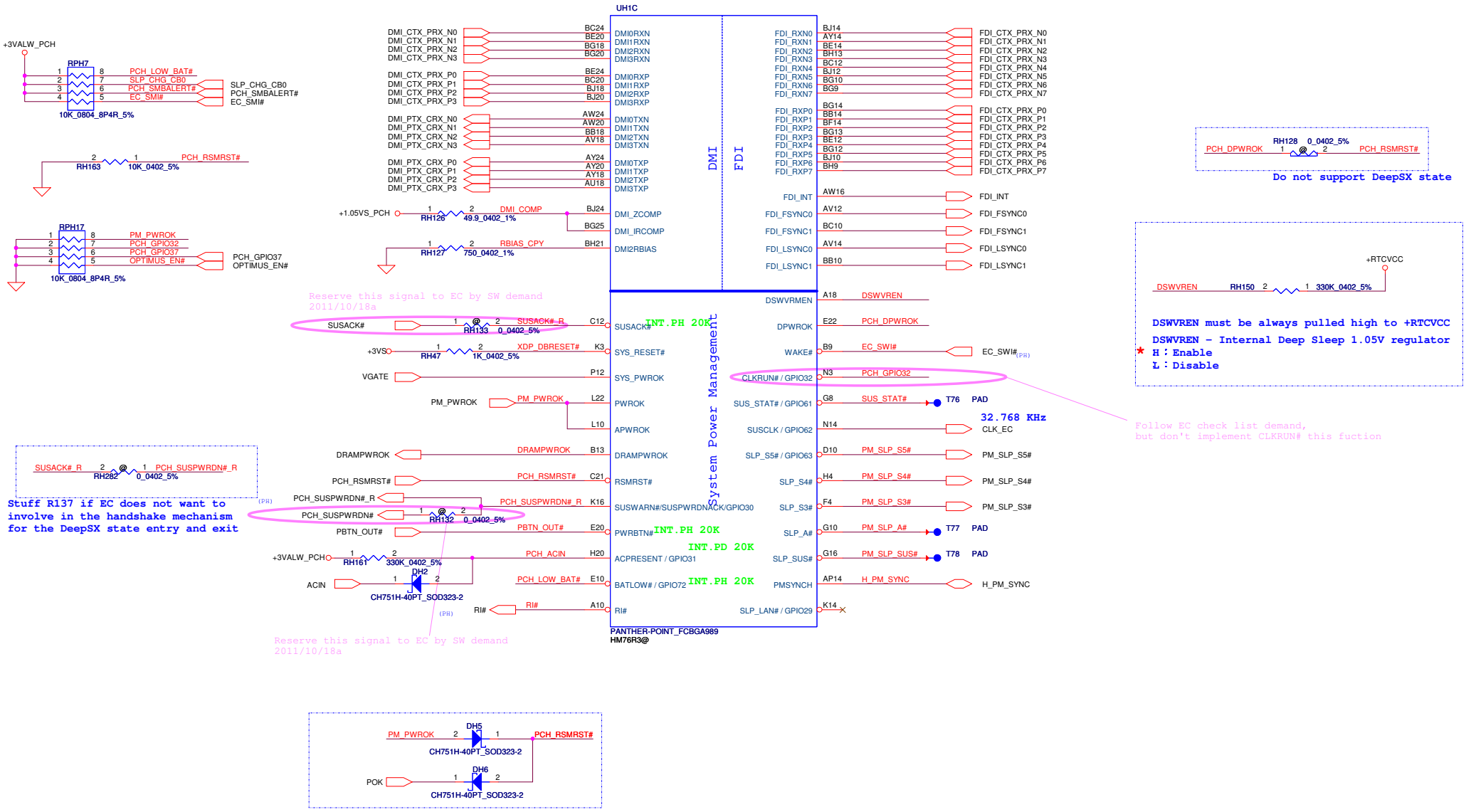
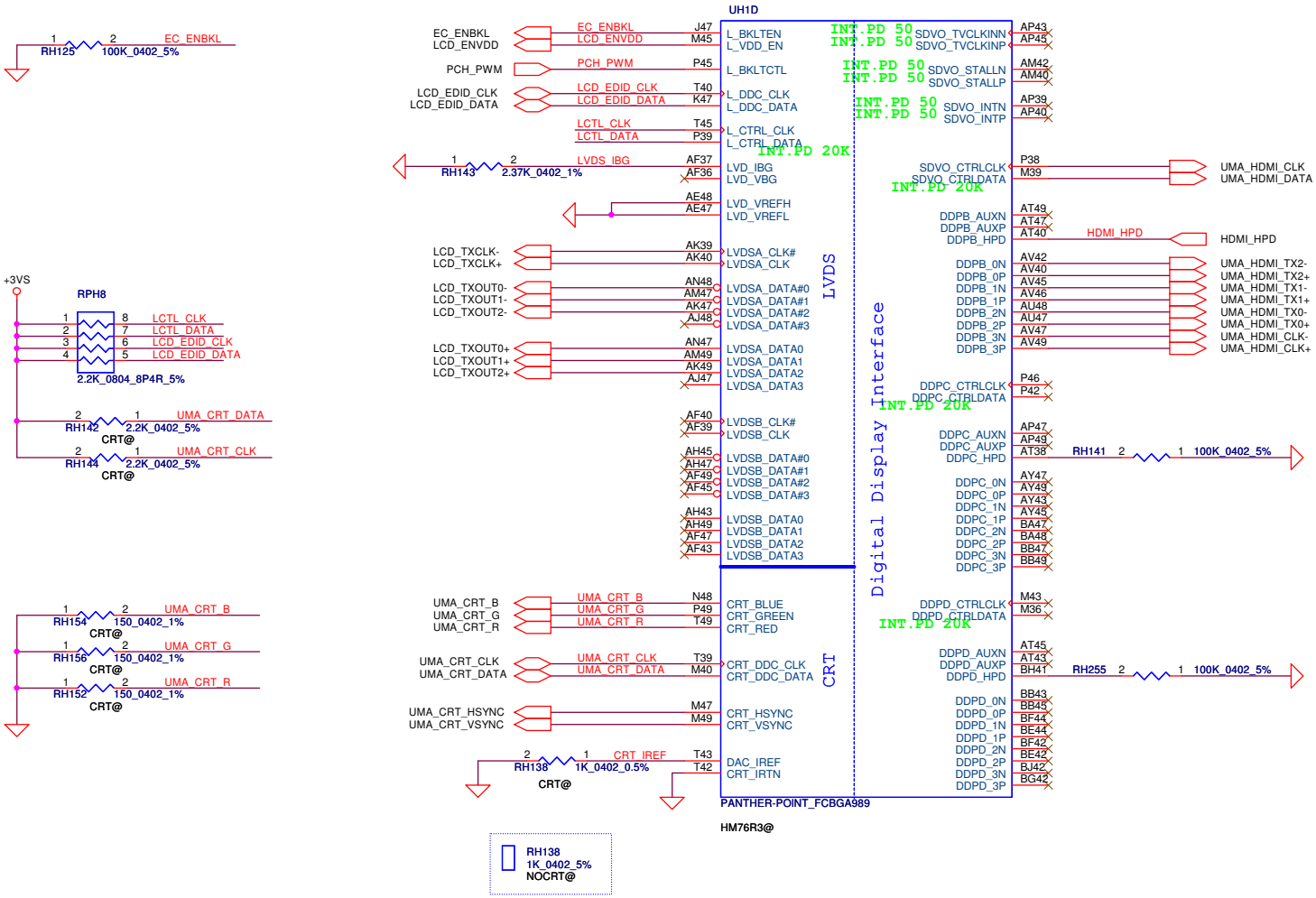


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/24	Deciphered Date 2013/09/24	Title: PCH_DMI/FDI/PM
Size: Custom	Document Number: VFKTA		Rev: 1.0
Date: Monday, March 11, 2013	Sheet 27 of 56		



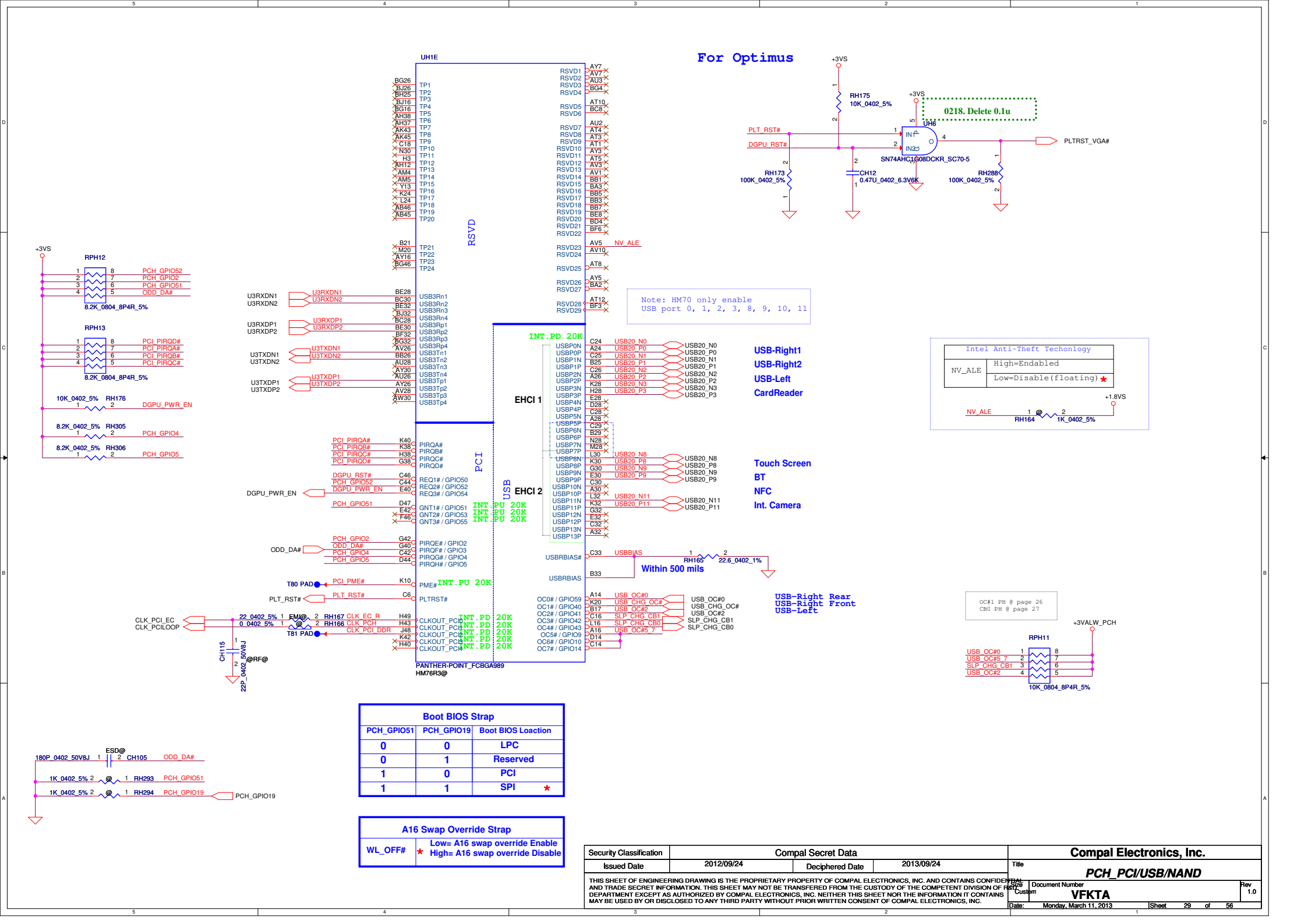
Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

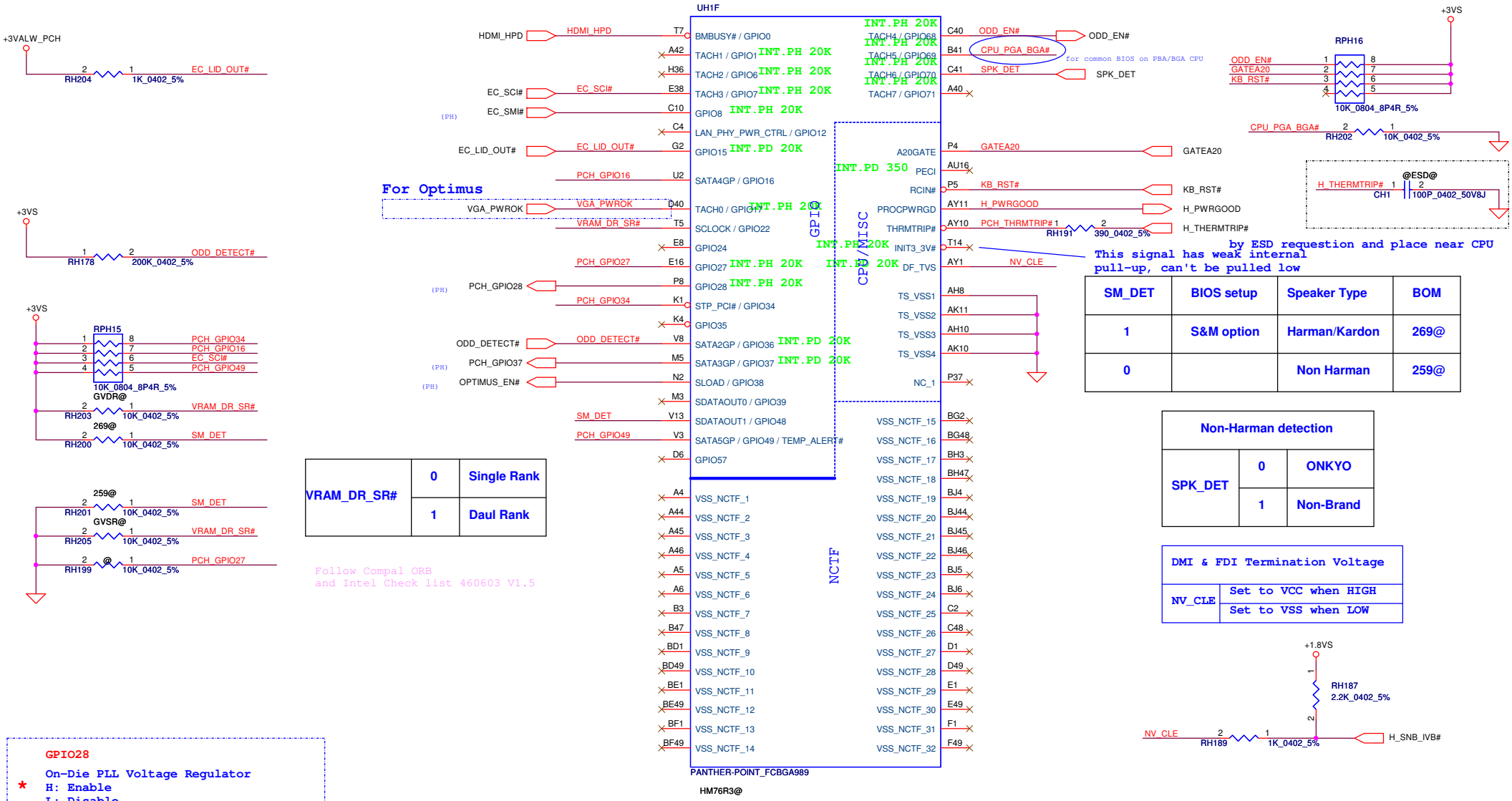
Compal Electronics, Inc.

Title: ***PCH_CRT/LVDS/HDMI***

Size	Document Number	Rev
Custom	VFKTA	1.0

Date: Monday, March 11, 2013 | Sheet 28 of 56


For Optimus
UH1E
RSVD
PCI
USB
EHCI 1
EHCI 2
PANTHER-POINT_FCBGA989
HM76R3@
Note: HM70 only enable
USB port 0, 1, 2, 3, 8, 9, 10, 11
USB-Right1
USB-Right2
USB-Left
CardReader
Touch Screen
BT
NFC
Int. Camera
USB-Right Rear
USB-Right Front
USB-Left
Within 500 mils
0218. Delete 0.1u
SN74AHC1G08DCKR_SC70-5
Intel Anti-Theft Techonlogy
NV_ALE
High=Endabled
Low=Disable(floating) *
Boot BIOS Strap
PCH_GPIO51
PCH_GPIO19
Boot BIOS Loaction
0 0 LPC
0 1 Reserved
1 0 PCI
1 1 SPI *
A16 Swap Override Strap
WL_OFF# * Low= A16 swap override Enable
High= A16 swap override Disable
Security Classification
Compal Secret Data
Issued Date
2012/09/24
Deciphered Date
2013/09/24
Compal Electronics, Inc.
PCH_PCI/USB/NAND
VFKTA
Monday, March 11, 2013
Sheet 29 of 56



VRAM_DR_SR#	0	Single Rank
	1	Daul Rank

Follow Compal ORB
and Intel Check list 460603 V1.5

This signal has weak internal pull-up, can't be pulled low

by ESD requestion and place near CPU

SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

Non-Harman detection		
SPK_DET	0	ONKYO
	1	Non-Brand

DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW

GPIO28

On-Die PLL Voltage Regulator
* H: Enable
L: Disable

GPIO8

Integrated Clock Chip Enable (Removed)
H: Disable
* L: Enable

Integrated clock enable functionality is achieved by soft-strap
The current default is clock enable

OPTIMUS_EN#

OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

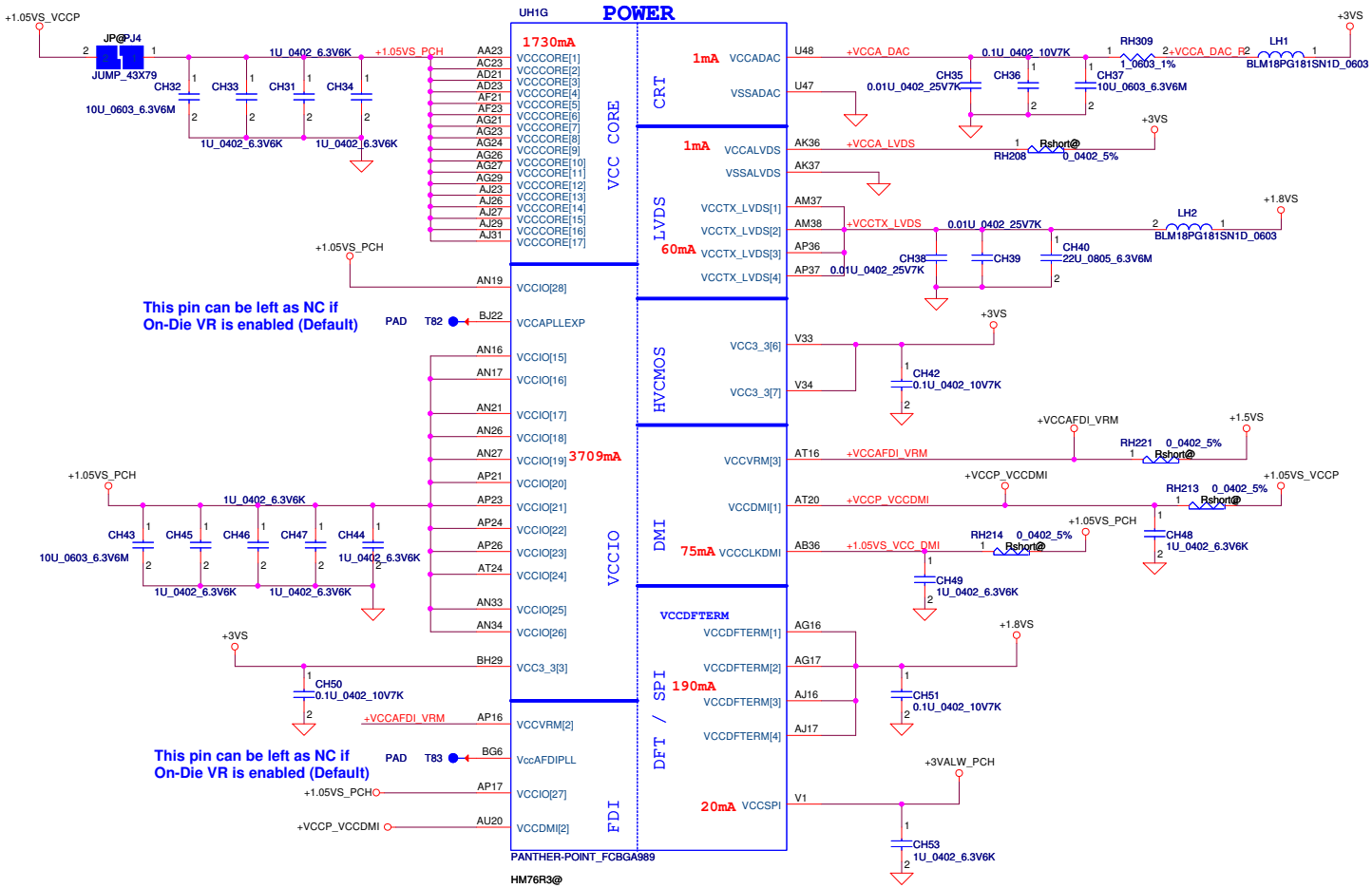
Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: *PCH_CPU/GPIO*

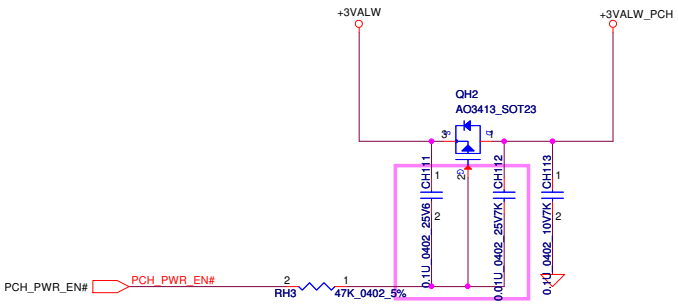
Size	Document Number	Rev
B	VFKTA	1.0

Date: Monday, March 11, 2013 Sheet 30 of 56



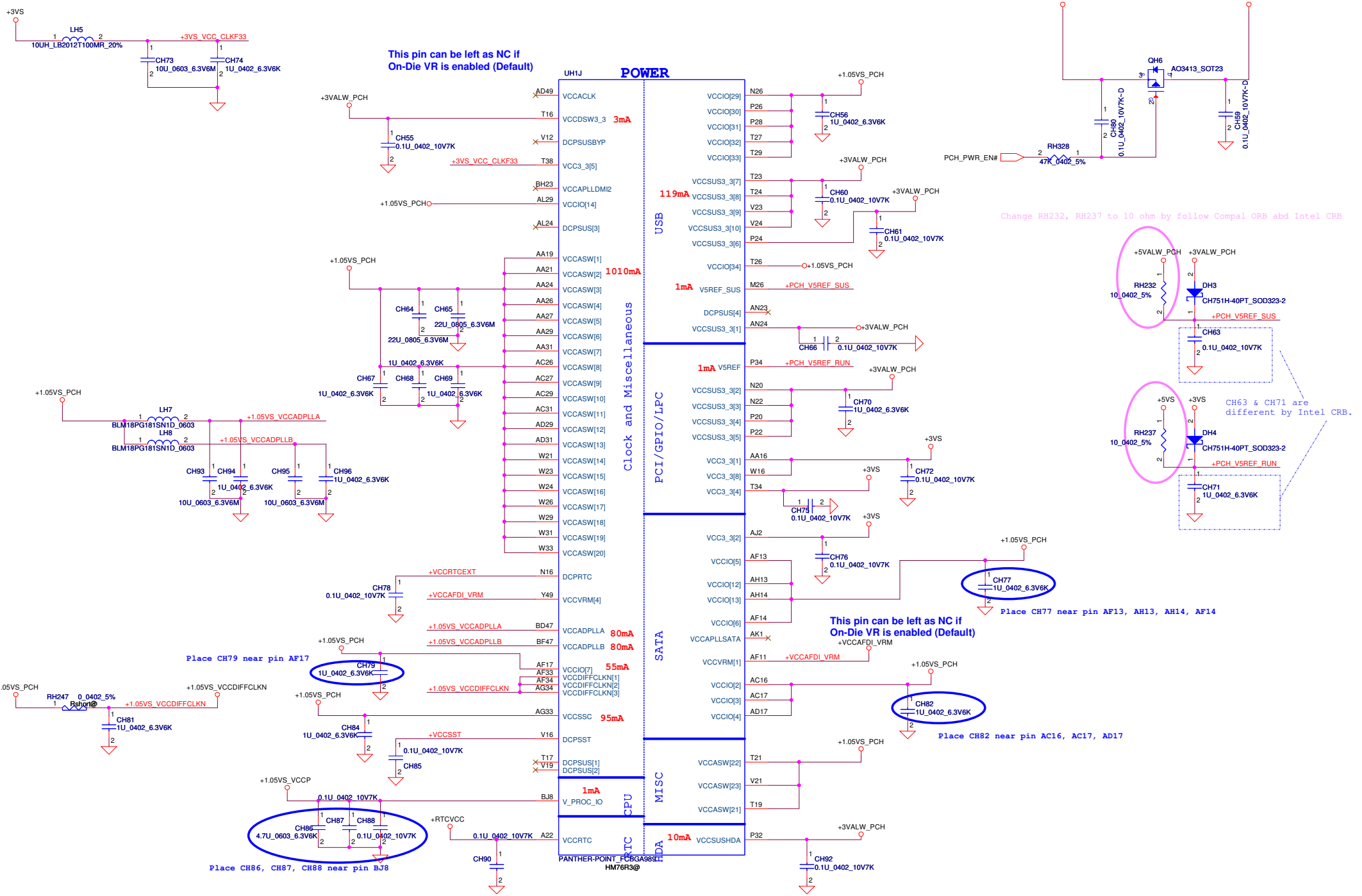
PCH Power Rail Table Refer to PCH EDS R1.0		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

+3VALW to +3VALW_PCH

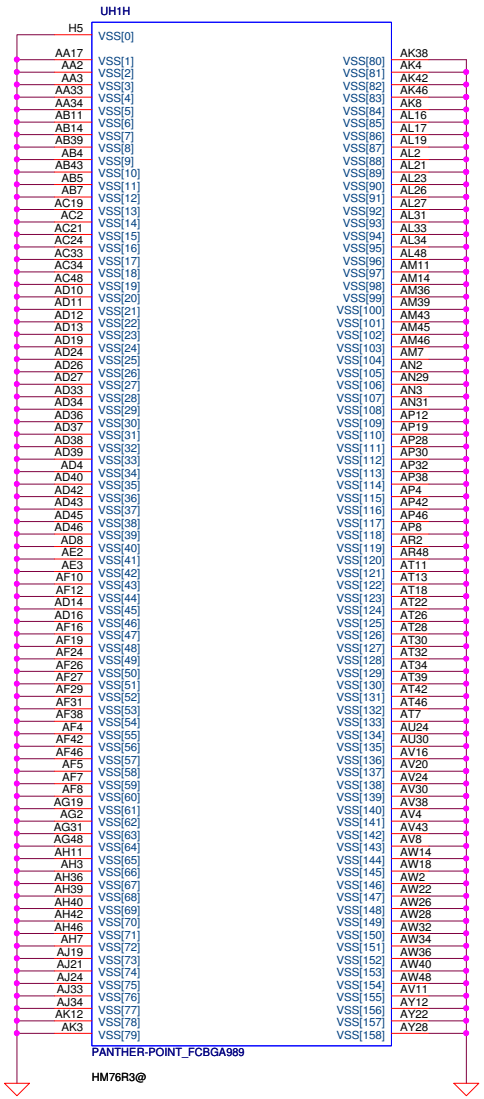


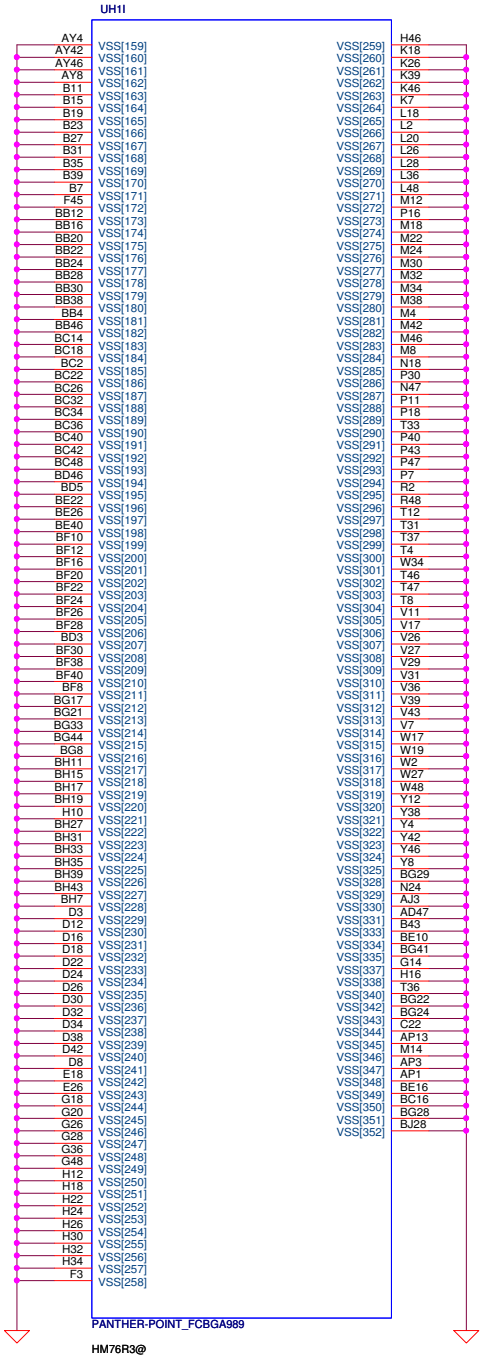
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/24	Deciphered Date 2013/09/24	Title: PCH_POWER-1

Size: Custom	Document Number: VFKTA		Rev: 1.0
Date: Monday, March 11, 2013	Sheet 31 of 56		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/24	Deciphered Date 2013/09/24	Title: PCH_POWER-2
			Size: Custom; Document Number: VFKTA; Rev: 1.0
			Date: Monday, March 11, 2013; Sheet 32 of 56





Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

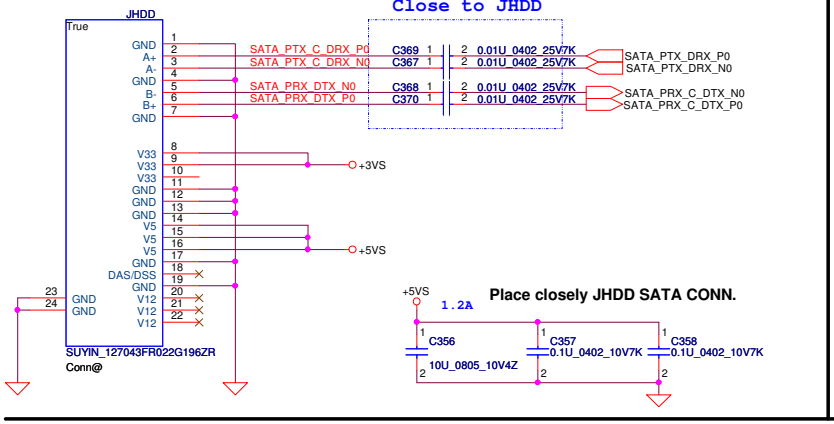
Compal Electronics, Inc.

Title: ***PCH_GND***

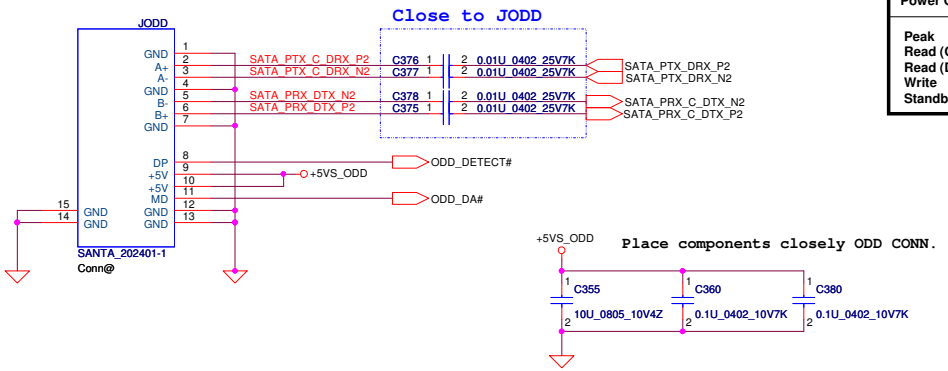
Size	Document Number	Rev
Custom	VFKTA	1.0

Date: Monday, March 11, 2013 Sheet 33 of 56

SATA HDD Conn.

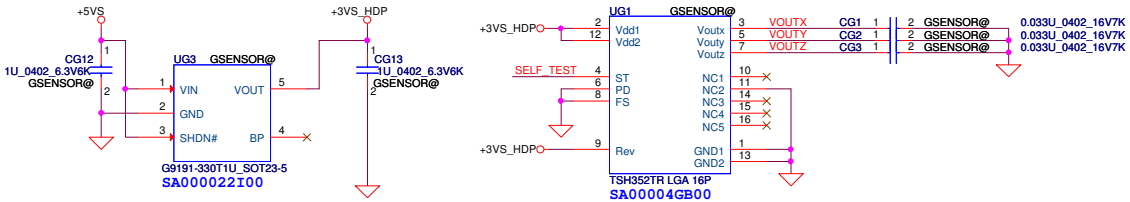


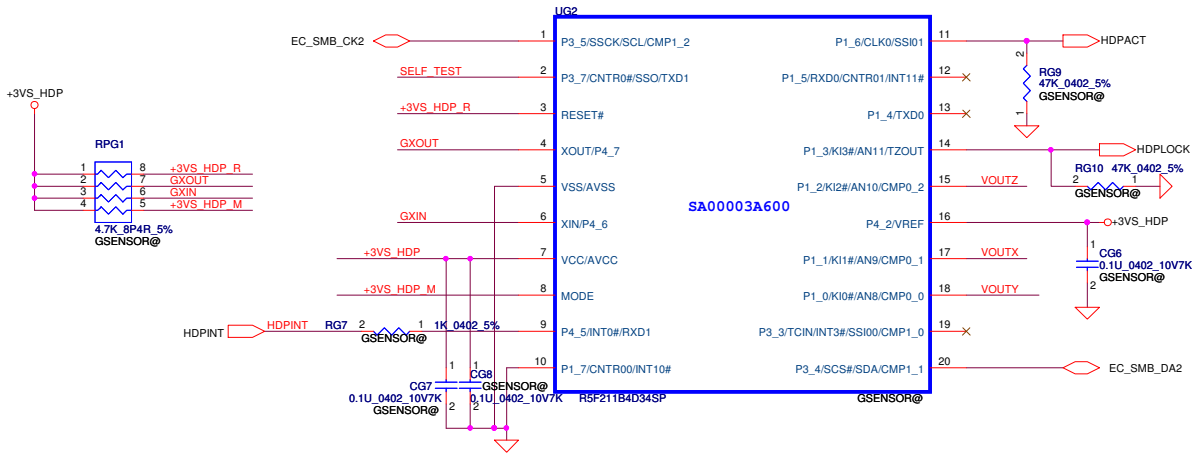
SATA ODD Conn



Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA

G-Sensor





Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: **HDD/ODD/G-Sensor**

Size: | Document Number: **VFKTA** | Rev: 1.0

Date: Monday, March 11, 2013 | Sheet 34 of 56

Slot 1 Half PCIe Mini Card-WLAN

+3V_WLAN 40 mils

0.1U_0402_10V7K CM1 CM2 CM3

0.1U_0402_10V7K 4.7U_0603_6.3V6K

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

From EC — BT_ON — BT_ON — RM27 1K_0402_5% — E51_RXD

For isolate BT_ON and Compal Debug Card.

To EC (Need pull-up +3VL)

To PCH

To PCH

WLAN/ WiFi

To PCH

JWLAN

WLAN_WAKE#

BT_ON — RM24 @0_0402_5% — BT_CTRL_R

CLKREQ_WLAN#

CLK_WLAN#

CLK_WLAN

PCIE_PRX_WLANTX_N2

PCIE_PRX_WLANTX_P2

PCIE_PTX_C_WLANRX_N2

PCIE_PTX_C_WLANRX_P2

+3V_WLAN

E51_TXD

E51_RXD

Debug card using

LOTES_AAA-PCI-049-P06-A

Conn@

+3V_WLAN

To EC

WL_OFF#

PLT_RST#

To PCH

PM_SMBCLK

PM_SMBDATA

USB20_N9

USB20_P9

WiMax/ BT

LED_WIMAX#

LED_WIMAX#

RM6 100K_0402_5% +3VS

+3VALW TO +3V_WLAN for WOWL

+3VALW

RM31 10K_0402_5% WOWL@

To EC WOWL_EN#

47K_0402_5% RM30 WOWL@

RM2 100K_0402_5%

WOWL@ CM9 0.1U_0402_10V7K

Vgs=-4.5V,Id=3A,Rds<97mohm

AO3413_SOT23 QM2

WOWL@ CM10 0.01U_0402_25V7K

If system don't support WOWL

+3V_WLAN

RM1 0_0603_5% NOWOWL@ +3VS

+3VL +1.05VS_VCCP +3VS_DGPU +3VALW

0.1U_0402_10V7K CCL1 GCLK@

0.1U_0402_10V7K CCL3 GCLK@

0.1U_0402_10V7K CCL6 GCLK@

0.1U_0402_10V7K CCL8 GCLK@

for safety request

CCL7 22U_0805_6.3V6M GCLK@

RCL4 120_0603_5% GCLK@

+RTC +RTCGCLK

UCL1 GCLK@

VBAT VDD_RTC_OUT

+3VL +V3.3A

+3VALW VDD

32kHz PCH_RTCX1_R

+3VS_DGPU VDDIO_27M 27MHz

VGA_X1_R RCL3 22_0402_5% VGA_X1

+1.05VS_VCCP VDDIO_25M_A 25MHz_A

VDDIO_25M_B 25MHz_B PCH_X1_R_R

22 ohm for NV chip

CLK_X1 CLK_X2 XTAL_IN XTAL_OUT

GND1 GND2 GND3 GND4

SLG3NB304VTR_TQFN16_2X3

CCL11 2.2U_0402_6.3V6M GCLK@

PCH_X1_R_R RCL1 Rshort@ 0_0402_5% PCH_X1_R

GCLK@ YCL1 25MHZ 12PF X3G025000DK1H-X

CLK_X1 CLK_X2 GND GND

CCL9 18P_0402_50V8J GCLK@

CCL12 18P_0402_50V8J GCLK@

PN: SA000063300

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

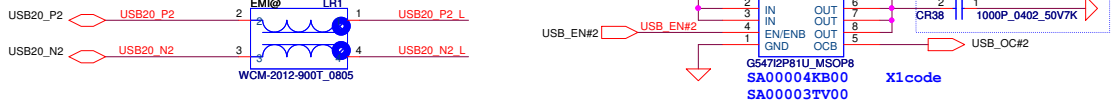
Compal Electronics, Inc.

Title: WLAN/GCLK

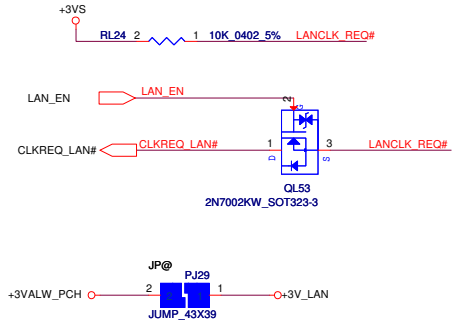
Size | Document Number: VFKTA | Rev: 1.0

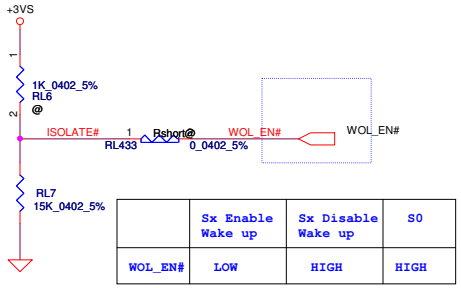
Date: Monday, March 11, 2013 | Sheet 35 of 56

Left USB 2.0 x 1

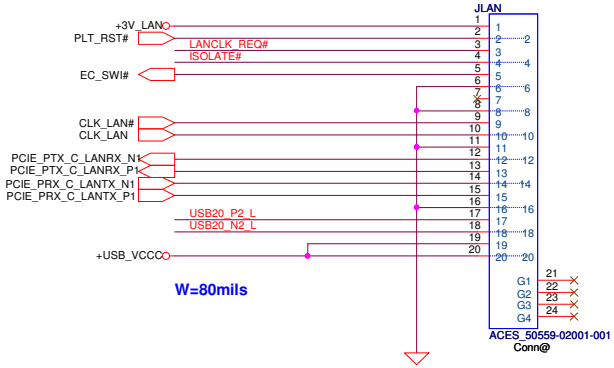


For LAN function





	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

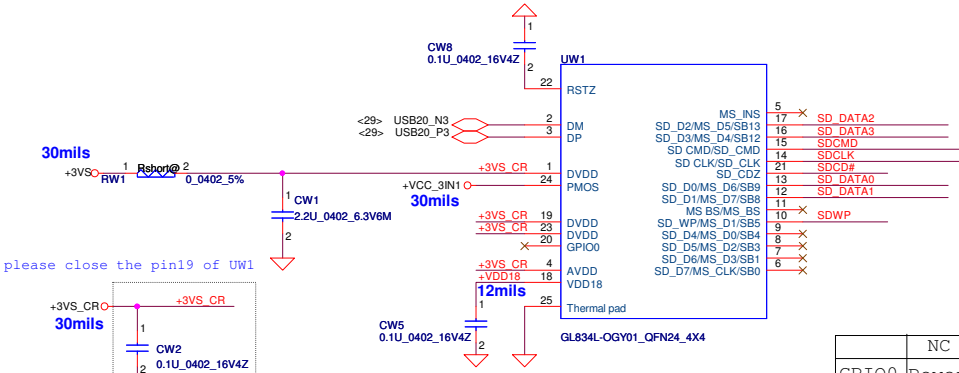


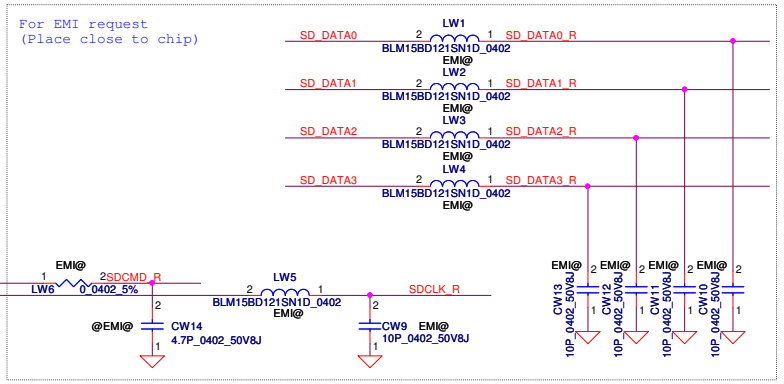
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/12/14	Deciphered Date 2012/12/31	Title: LUSB20/LAN conn.
Size: Custom	Document Number: VFKTA		Rev: 1.0
Date: Monday, March 11, 2013	Sheet 36 of 56		

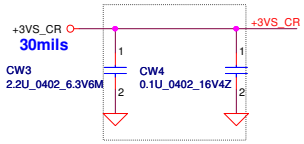




	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

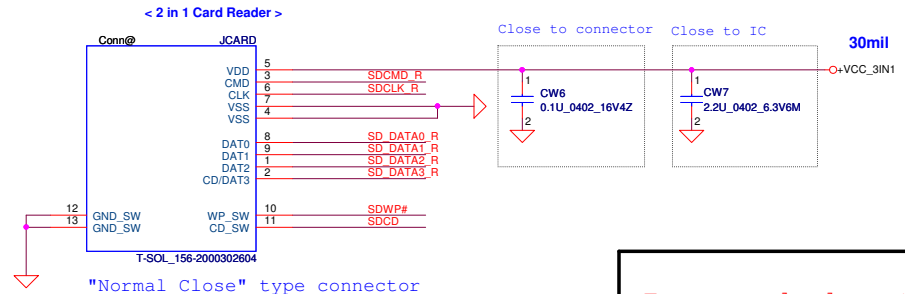
please close the pin19 of UW1

please close the pin4 of UW1



De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket

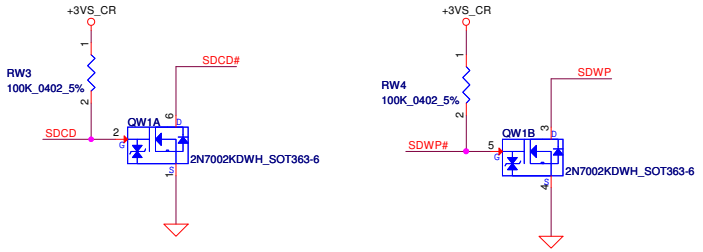
< 2 in 1 Card Reader >



"Normal Close" type connector

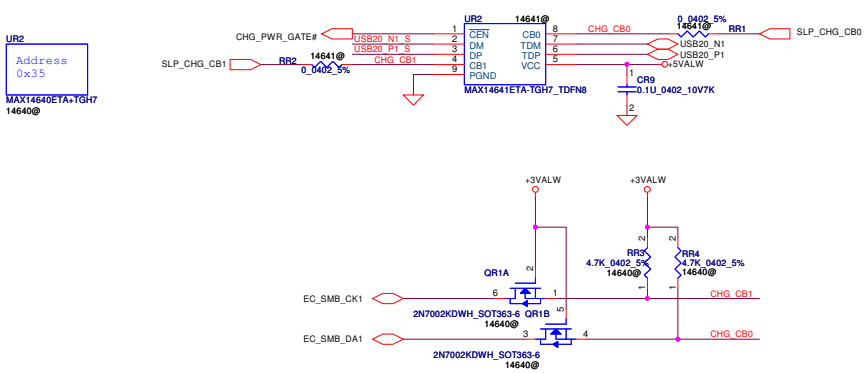
	CD_SW	WP_SW	
		Protect disable	Protect Enable
Card Uninsertion	Close	Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit



Security Classification	Compal Secret Data		
Issued Date	2012/10/26	Deciphered Date	2013/10/26

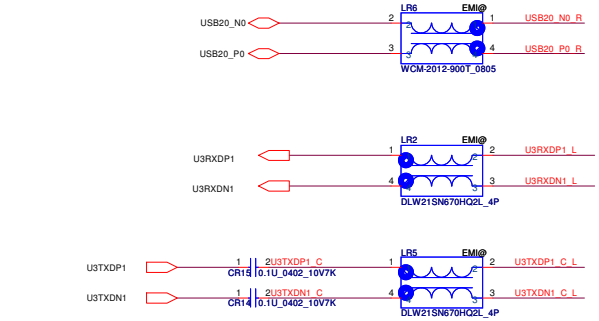
Compal Electronics, Inc.			
Title	USB-CardReader GL834L		
Size: Custom	Document Number: VFKAA		Rev: 1.0
Date: Monday, March 11, 2013	Sheet 37 of 56		



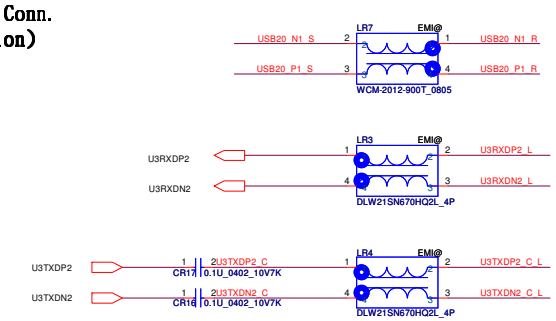
USB Sleep & Charge

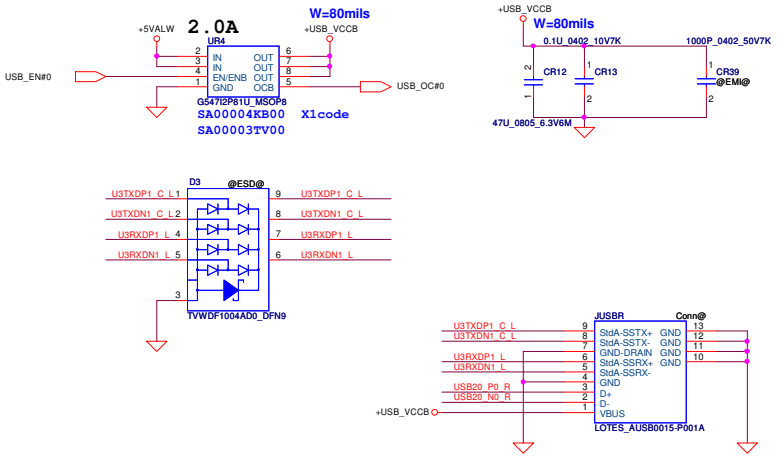
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.

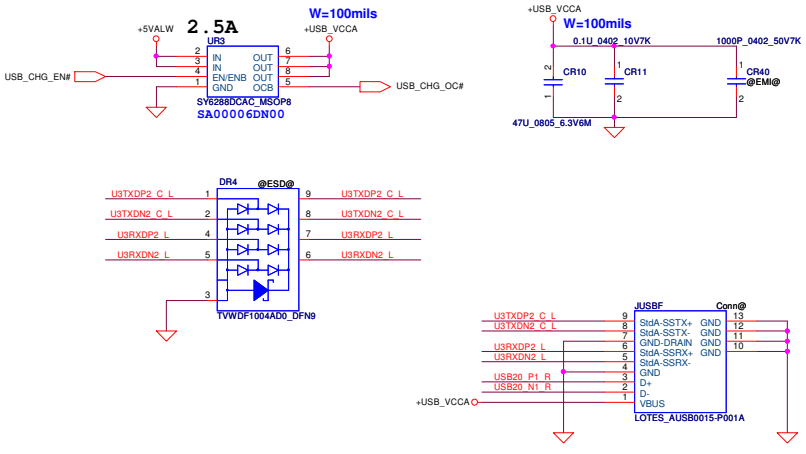
Right rear USB3.0 Conn.



Right front USB3.0 Conn. (Support S&C function)







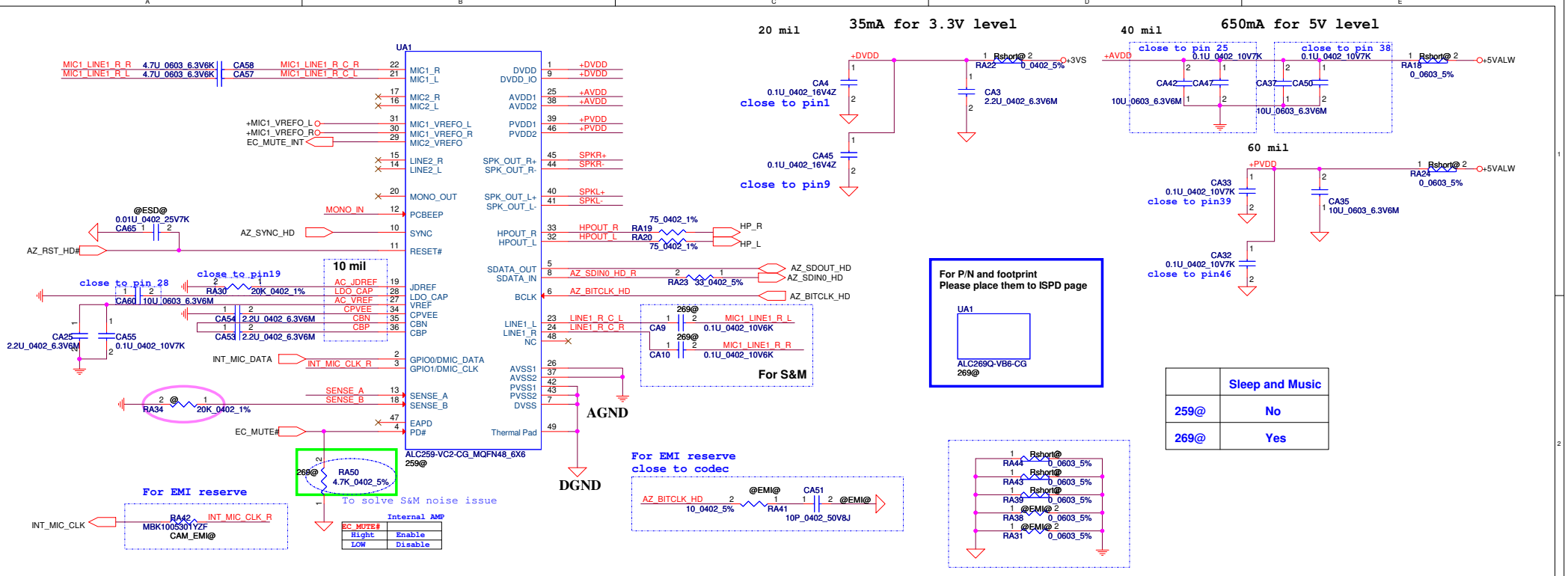
Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

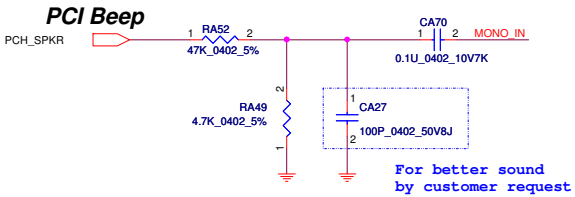
Title: RUSB30/S&C

Size: Custom | Document Number: VFKTA | Rev: 1.0

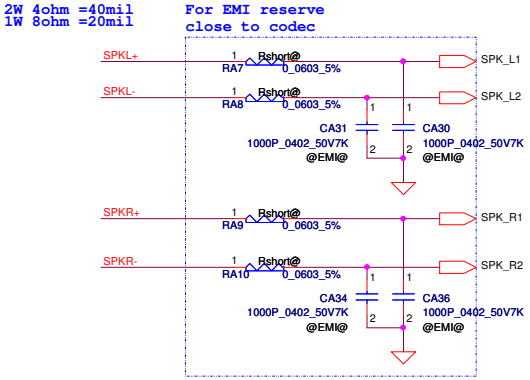
Date: Monday, March 11, 2013 | Sheet 38 of 56



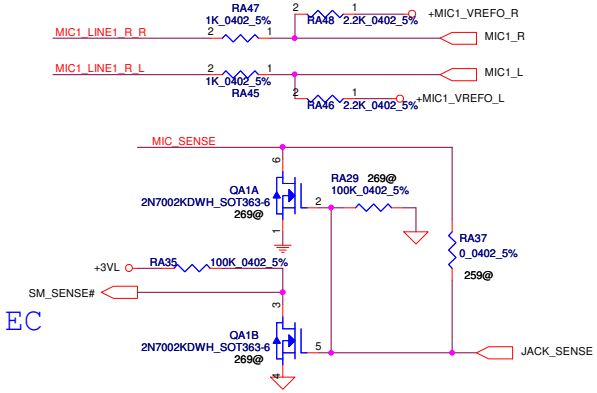
Beep sound



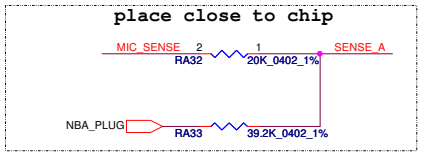
SPK



MIC/LINE IN



place close to chip

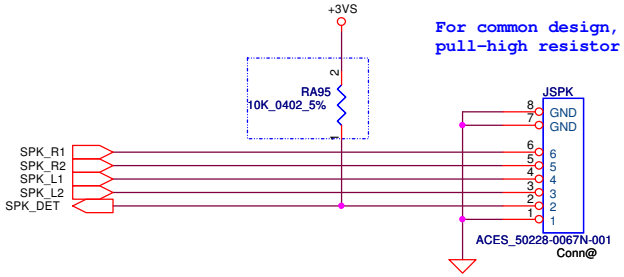


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.	
Title	HDA-ALC259-VC/269-VB
Size: Custom	Document Number
Rev	
Date: Monday, March 11, 2013	Sheet 39 of 56

SPK Conn.



For common design,
pull-high resistor should be placed at connector side.

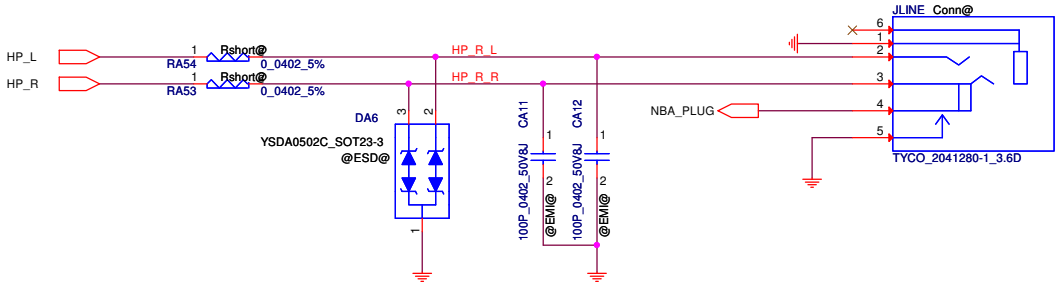
<SM_DET>
Intel : GPIO48
AMD Richland : GPIO173
AMD Kabini :GPIO70

<SPK_DET>
Intel : GPIO70
AMD Richland : GPIO74
AMD Kabini :GPIO62

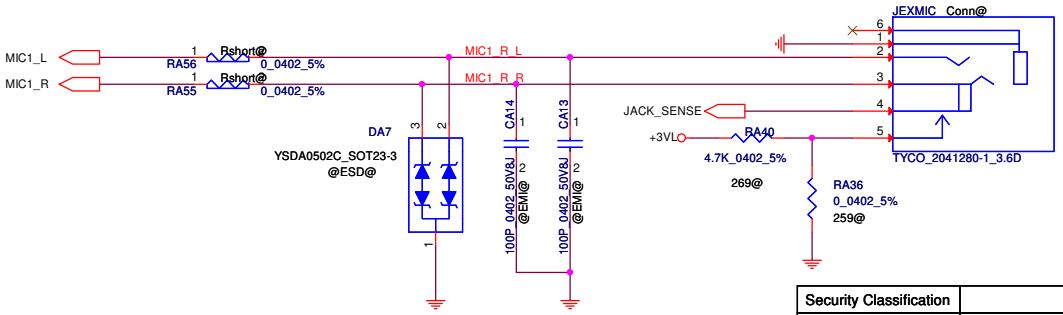
SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

Non-Harman detection		
SPK_DET	0	ONKYO
	1	Non-Brand

HeadPhone/LINE Out JACK



MIC/LINE IN JACK



Compal Electronics, Inc.

Title: AUDIO CONN

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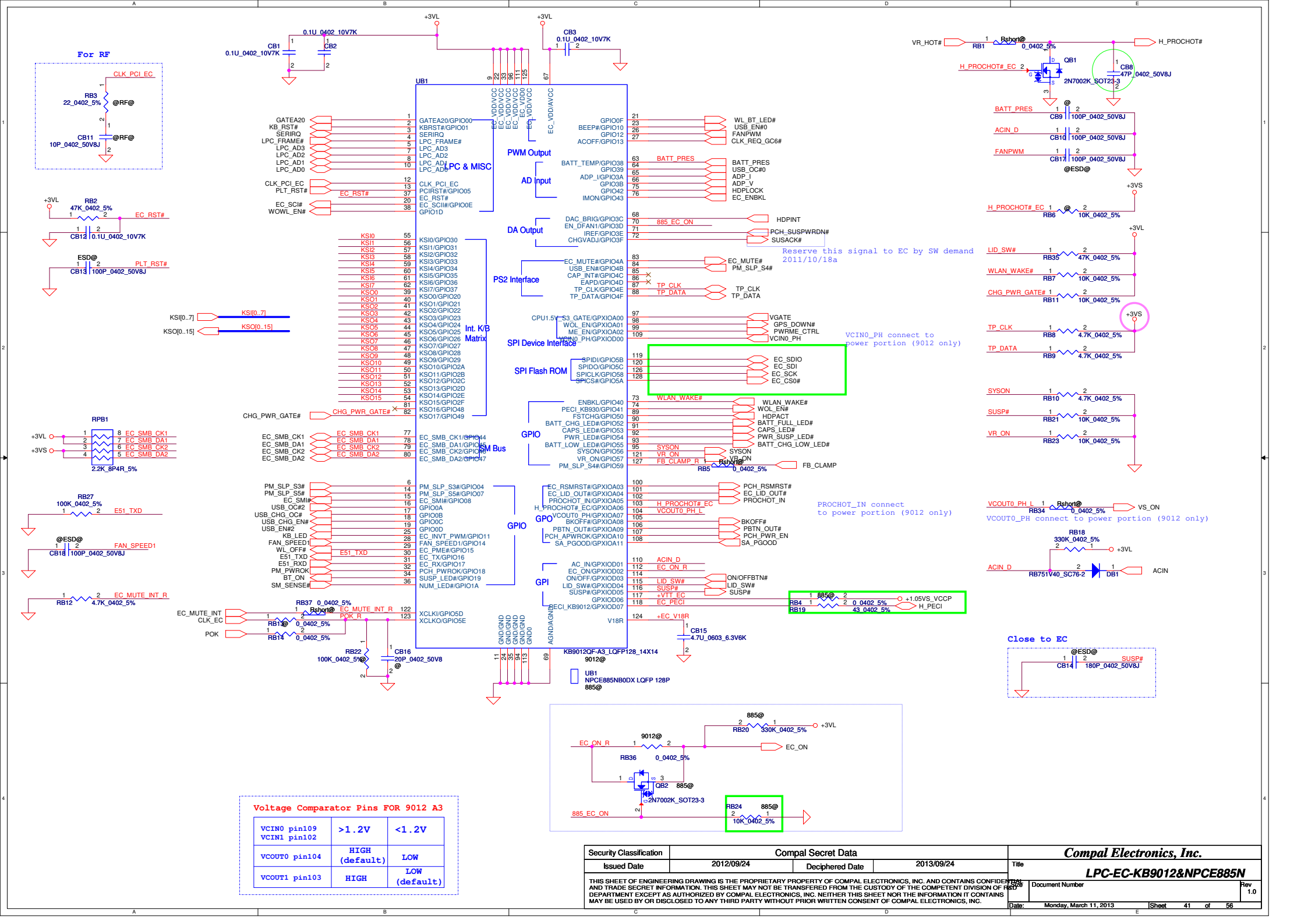
For RF
CLK_PCI_EC
RB3 22_0402_5% @RF@
CB11 10P_0402_50V8J @RF@
UB1
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
PCH_SUSPWRDN#
SUSACK#
Reserve this signal to EC by SW demand 2011/10/18a
VCIN0_PH connect to power portion (9012 only)
PROCHOT_IN connect to power portion (9012 only)
VCOUT0_PH connect to power portion (9012 only)
Close to EC
KB9012QF-A3_LQFP128_14X14
9012@
UB1 NPCE885NB0DX LQFP 128P 885@
Voltage Comparator Pins FOR 9012 A3
VCIN0 pin109 VCIN1 pin102 >1.2V <1.2V
VCOUT0 pin104 HIGH (default) LOW
VCOUT1 pin103 HIGH LOW (default)
Security Classification Compal Secret Data
Issued Date 2012/09/24 Deciphered Date 2013/09/24
Compal Electronics, Inc.
LPC-EC-KB9012&NPCE885N
Document Number Rev 1.0
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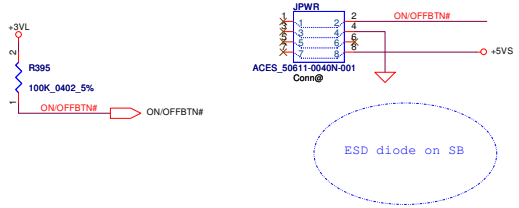
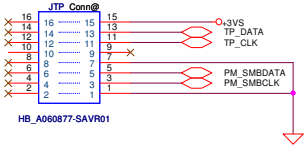
Power Button



Conn.

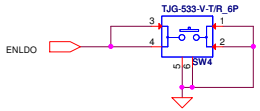
ESD diode on SB

Touchpad Connector

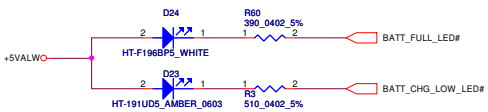


NFC

Battery Reset



BATT CHARGE /FULL LED

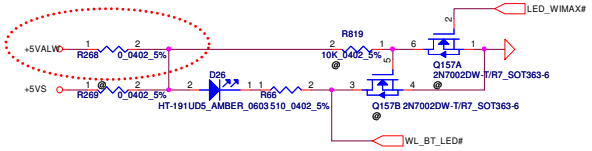


White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED

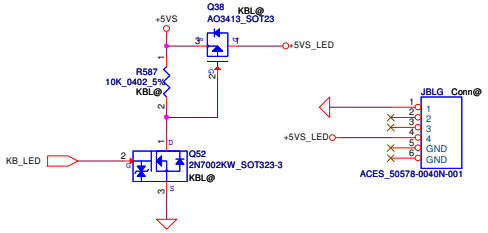
White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN/WiMAX LED

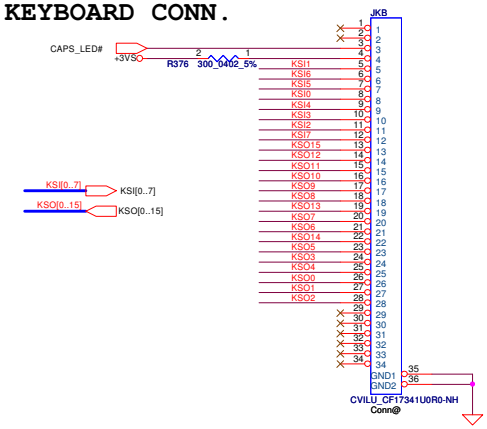


Amber LED bright while Wireless and/or WiMAX turns on.

Keyboard LED

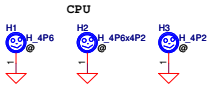


KEYBOARD CONN.

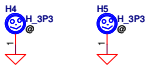


Screw Hole

CPU

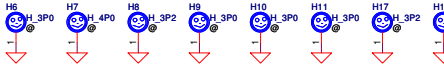


VGA

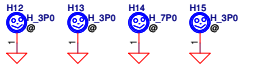


WLAN standoff

PTH



NPTH



PCB Fedical Mark PAD

CPU

(Default)
CPU8
SA00004SX00

UC1 CPUI73537UR1@	UC1 CPUI53337UR1@	UC6 CPUI73537UR3@	UC7 CPUI53337UR3@
SA00006DB40	SA00006D850	????????????	SA00006D880
Ivy Bridge i7 3537U R1	Ivy Bridge i5 3337U R1	Ivy Bridge i7 3537U R3	Ivy Bridge i5 3337U R3
UC1 CPUI33227UR1@	UC1 CPUI32375MR1@	UC4 CPUI33227UR3@	UC5 CPUI32375MR3@
SA00006D970	SA00006ED40	SA00006D960	SA00006ED60
Ivy Bridge i3 3227U R1	Ivy Bridge i3 2375M R1	Ivy Bridge i3 3227U R3	Ivy Bridge i3 2375M R3
UC1 CPUP2117UR1@	UC1 CPUC847R1@	UC8 CPUP2117UR3@	UC9 CPUC847R3@
SA000061230	SA00005VK00	SA000061260	SA00005VK50
Ivy Bridge Pentium 2117U R1	Ivy Bridge Celeron 847 R1	Ivy Bridge Pentium 2117U R3	Ivy Bridge Celeron 847 R3

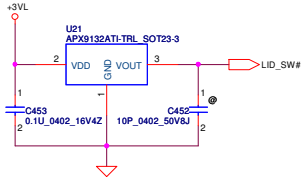
GPU

UV1 N14PGV2R1@
SA00006DO00
N14P-GV2-S-A1 FCBGA

(Default)
N14PGV2R3@
N14P-GV2-S-A1
SA00006DO40

UV1 N14MGLR1@	UV1 N14MGLR3@
SA000069000	SA000069010
N14M-GL-S-A2 FCBGA	N14M-GL-S-A2 FCBGA

Lid SW



ISPD

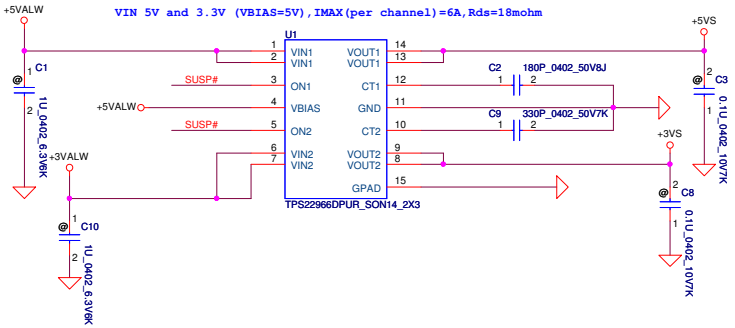
ZZZ
DA8000XE000
PCB LA-9861P

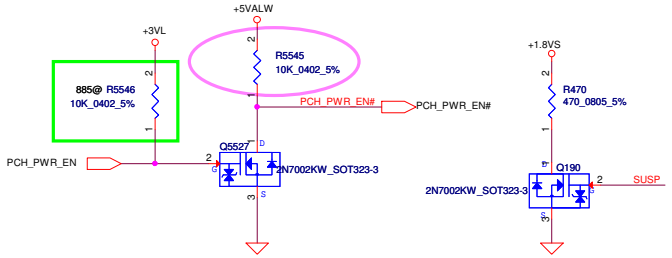
PCH

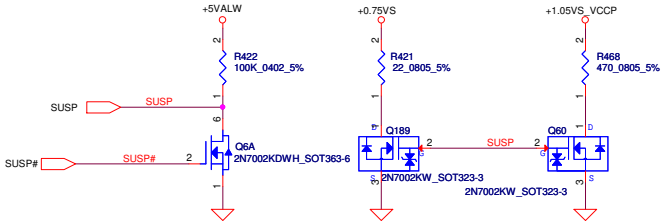
UH1 HM76R1@		(Default)
SA00005FHA0		HM76R3@
BD82HM76 SLJ8E C1		BD82HM76 SLJ8E C1
		SA00005FHE0
UH1 HM70R1@	UH1 HM70R3@	
SA00005MQ50	SA00005MQC0	
BD82HM70 SJTNV C1	BD82HM70 SJTNV C1	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/24	Deciphered Date 2013/09/24	Title: TP/ISPD/KB/LED/Screw
			Size: Document Number: VFKTA Rev: 1.0
			Date: Monday, March 11, 2013 Sheet 42 of 56

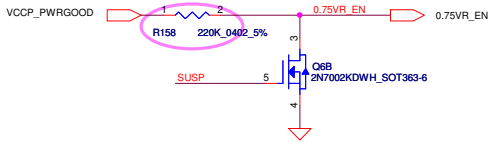
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



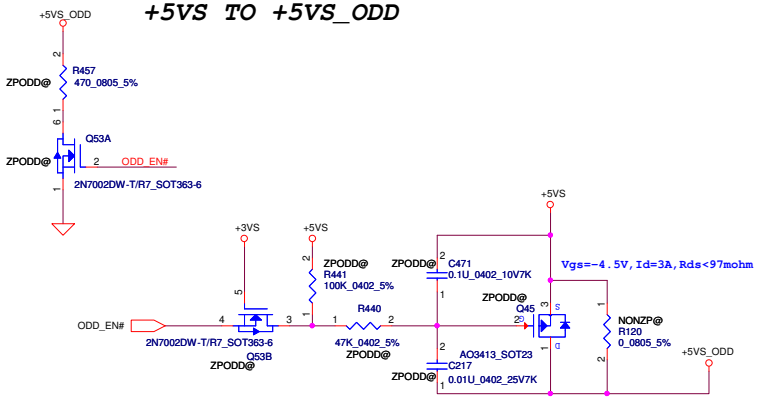




For S3 CPU Power Saving



+5VS TO +5VS_ODD



Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
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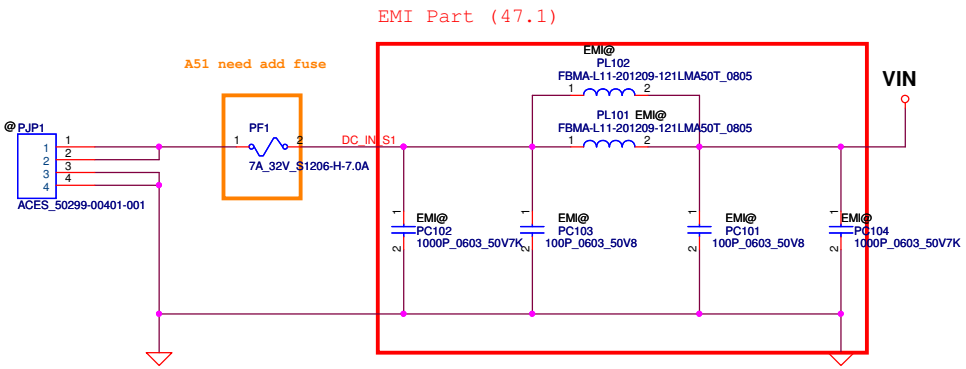
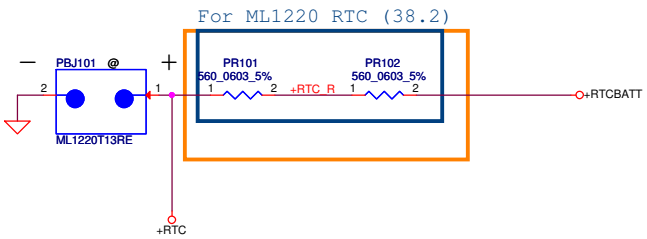




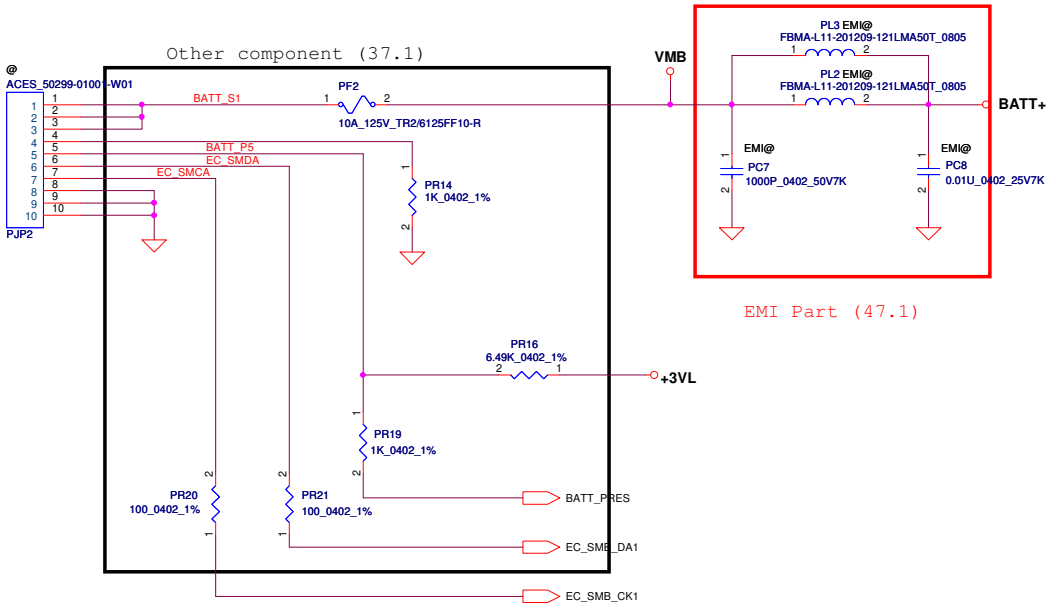
Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

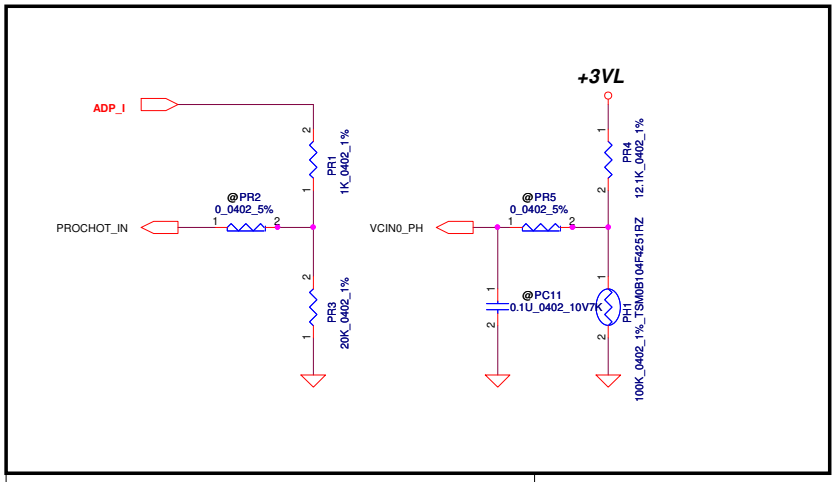
Title: *DCIN/PRECHARGE*

Size: Custom | Document Number: *VFKTA* | Rev: 1.0

Date: | Sheet 44 of 56



OTP (39.7)



PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

	Protect	Recovery
65W	0.752V	0.626V
75W	0.902V	0.722V

	Initial	Protect	Recovery
CPU OTP	65W	93 C	56 C

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: ***BATTERY CONN / OTP***

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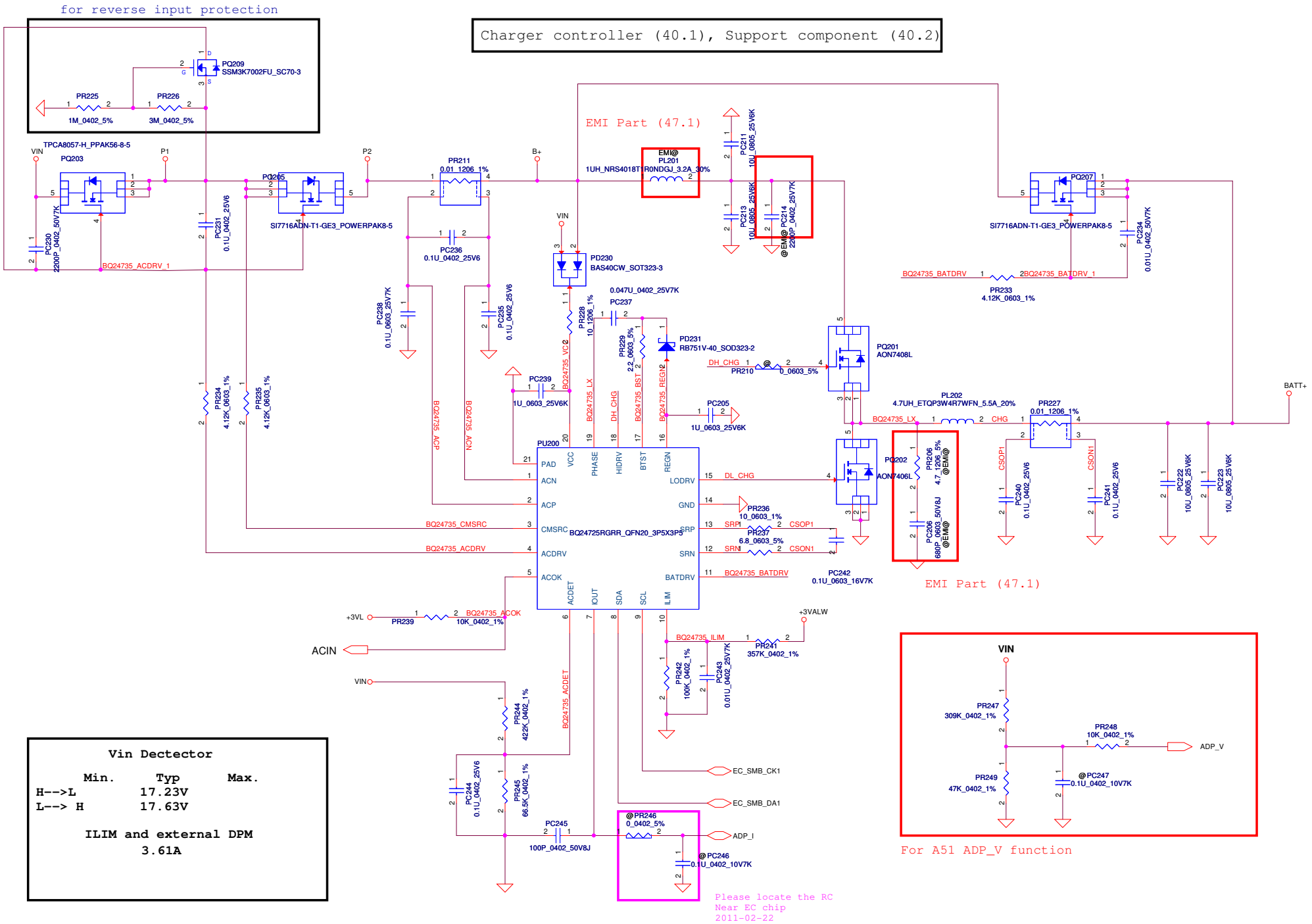
Date: | Sheet 45 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: *CHARGER*

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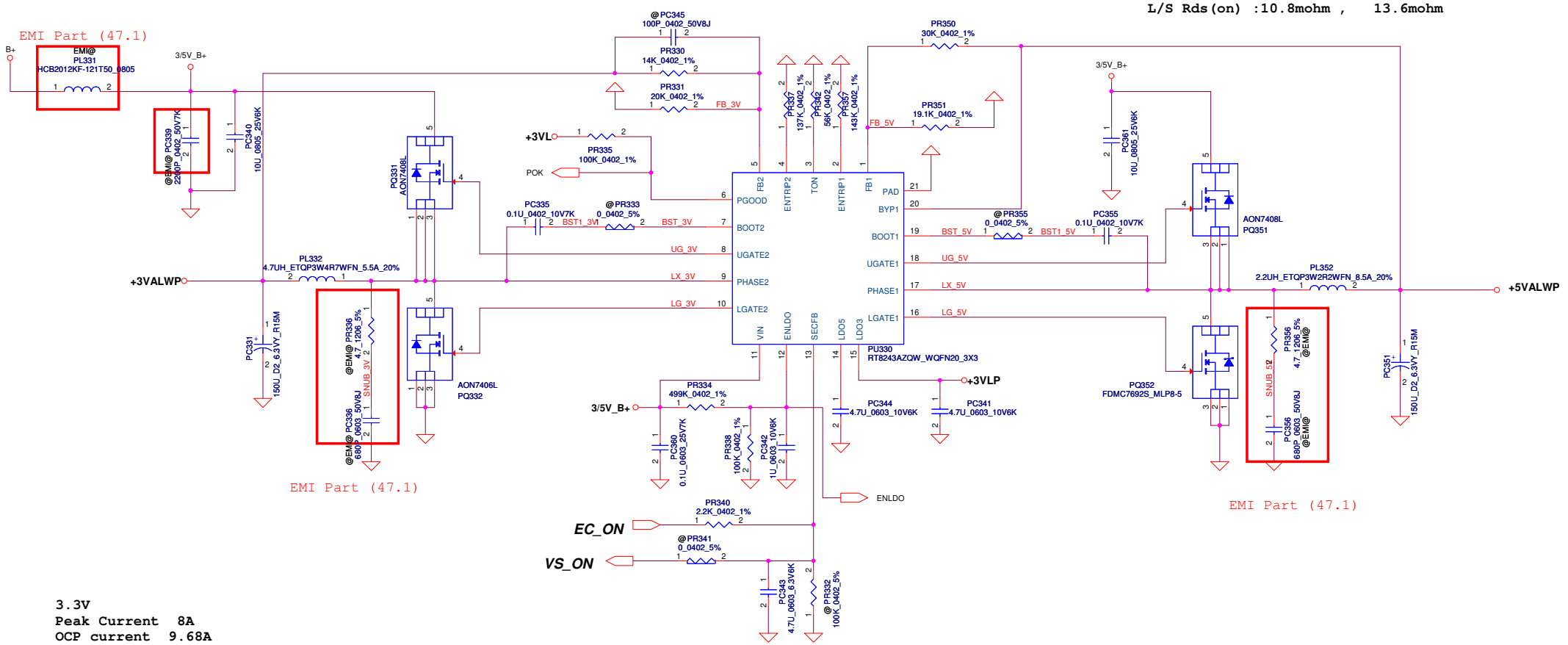
3/5VALW controller (35.1), Support component (35.2)

5V
Peak Current 8.5A
OCP current 10.2A
FSW=390kHz
Delta I=4.29A,ripple=4.29*17m=72.93mV
DCR 15.5mohm+/-15%
ESR 17mohm

	TYP	MAX
H/S Rds(on)	27mohm	34mohm
L/S Rds(on)	10.8mohm	13.6mohm



3.3V
Peak Current 8A
OCP current 9.68A
Delta I=1.28A ,ripple=1.28x15m=19.2mV
FSW=455kHz
DCR 35mohm +/-15%
ESR 15mohm

	TYP	MAX
H/S Rds(on)	27mohm	34mohm
L/S Rds(on)	19mohm	23.5mohm

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: *3VALW/5VALW*

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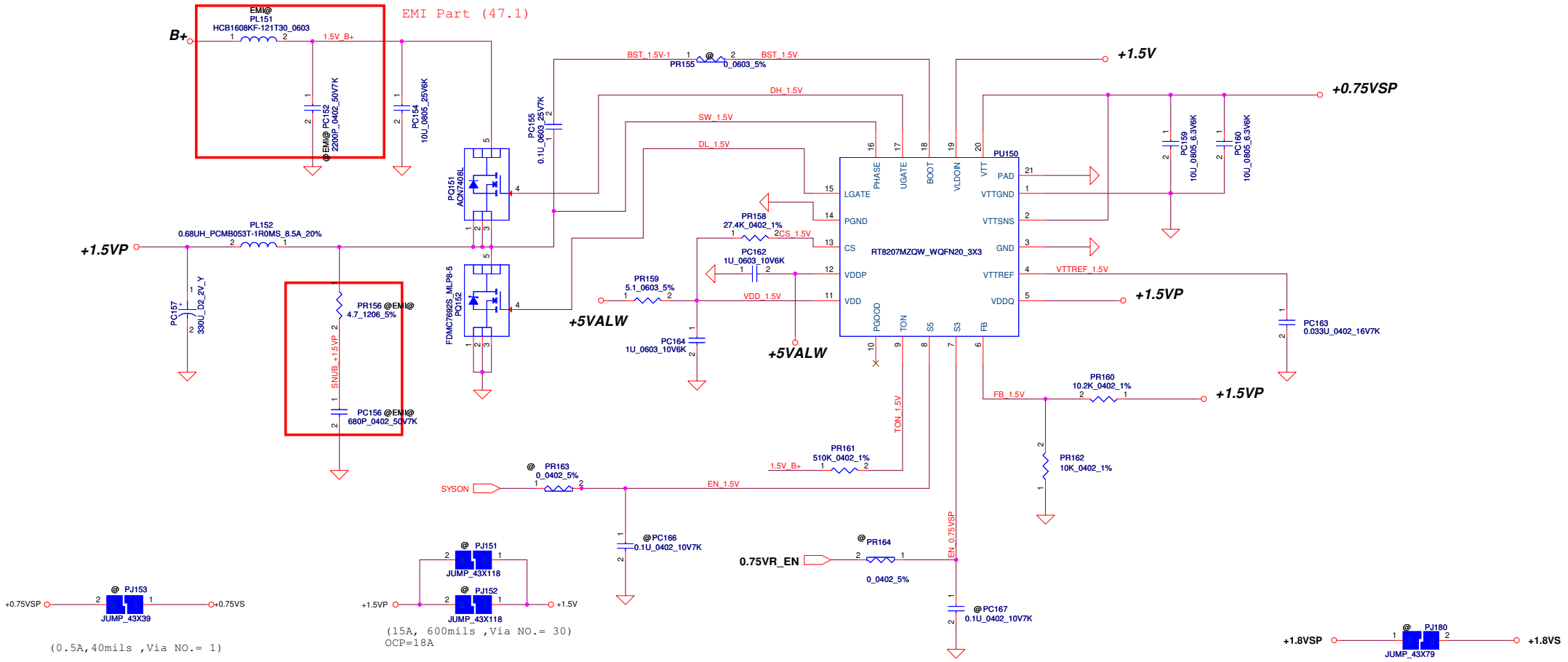
DDR controller (35.3), Support component (35.4)



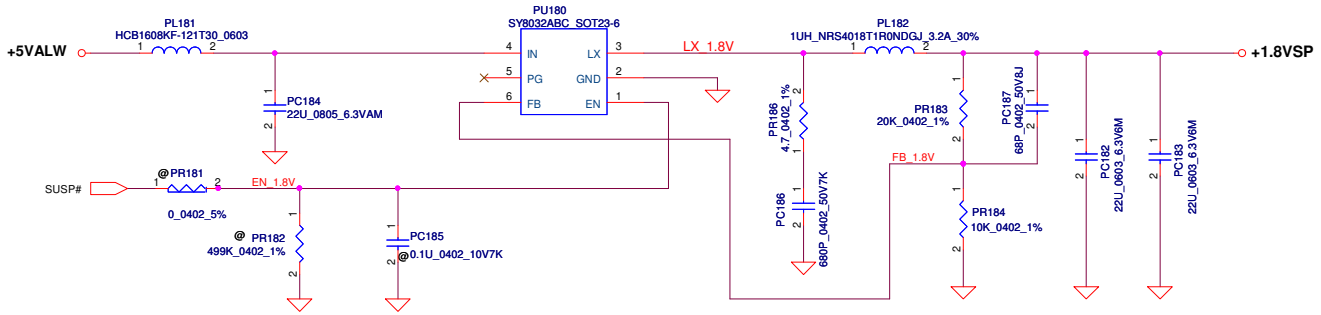
1.5V
Peak Current 16.66A
OCP current 20 A
FSW=495kHz
DCR 12mohm
ESR 10mohm

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:10.8mohm ,	13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

1.8VS controller (35.15), Support component (35.16)



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	1.5VP/0.75VSP/1.8VSP
				Size: Custom	Document Number: VFKTA
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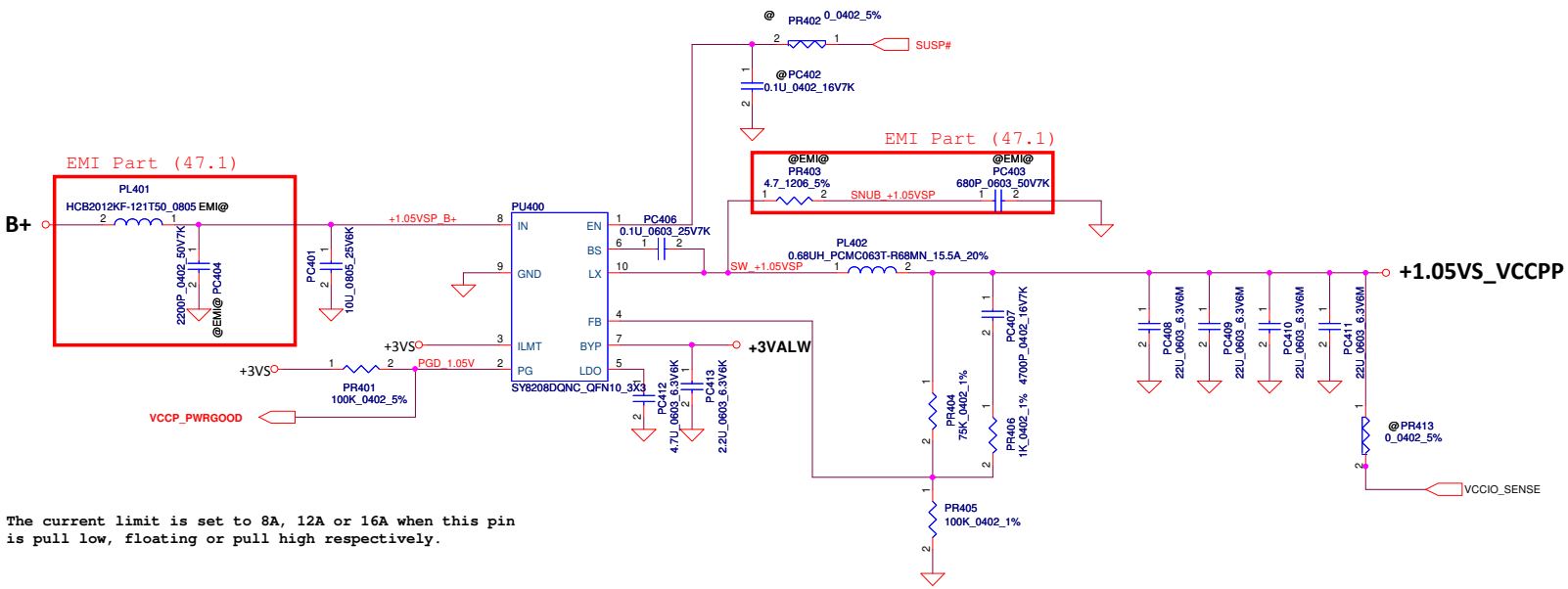
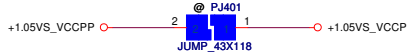
1.05VCCP controller (35.5), Support component (35.6)



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.



(14.37A,680mils ,Via NO.=30)
OCP=17.24A

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: ***+1.05VS_VCCP***

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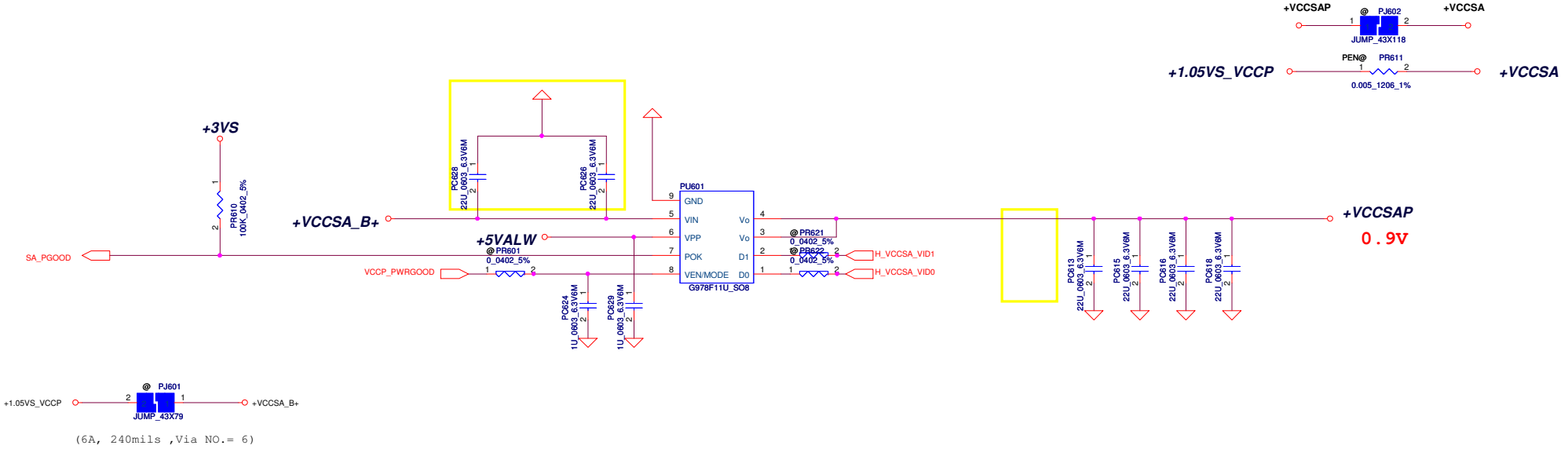
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

VCCSA controller (35.17), Support component (35.18)



(6A, 240mils ,Via NO.= 6)

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title	VCC_SAP	
Size: Custom	Document Number: VFKTA	Rev: 1.0
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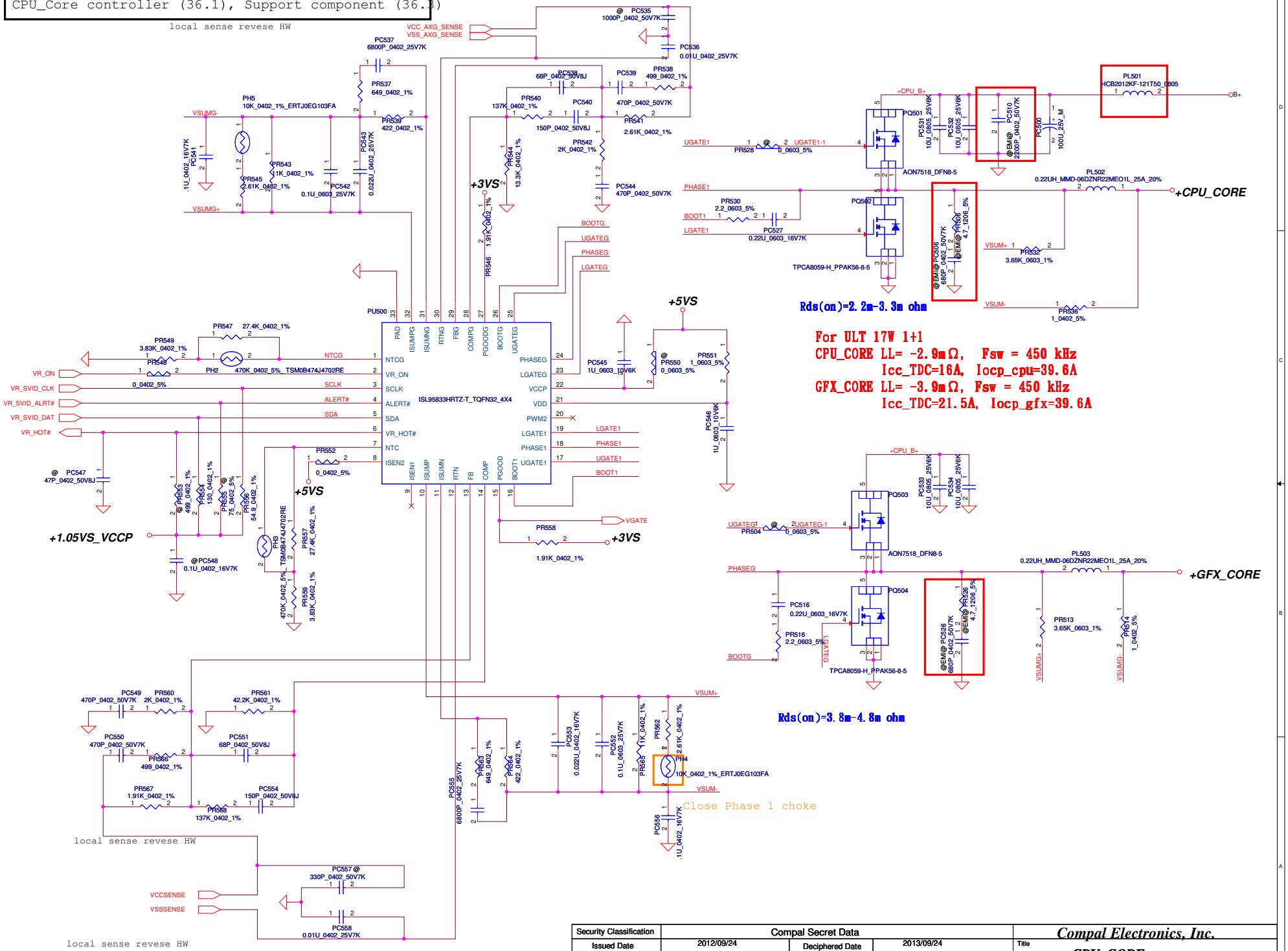
CPU_Core controller (36.1), Support component (36.3)



Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
Custom	VFKTA	1.0

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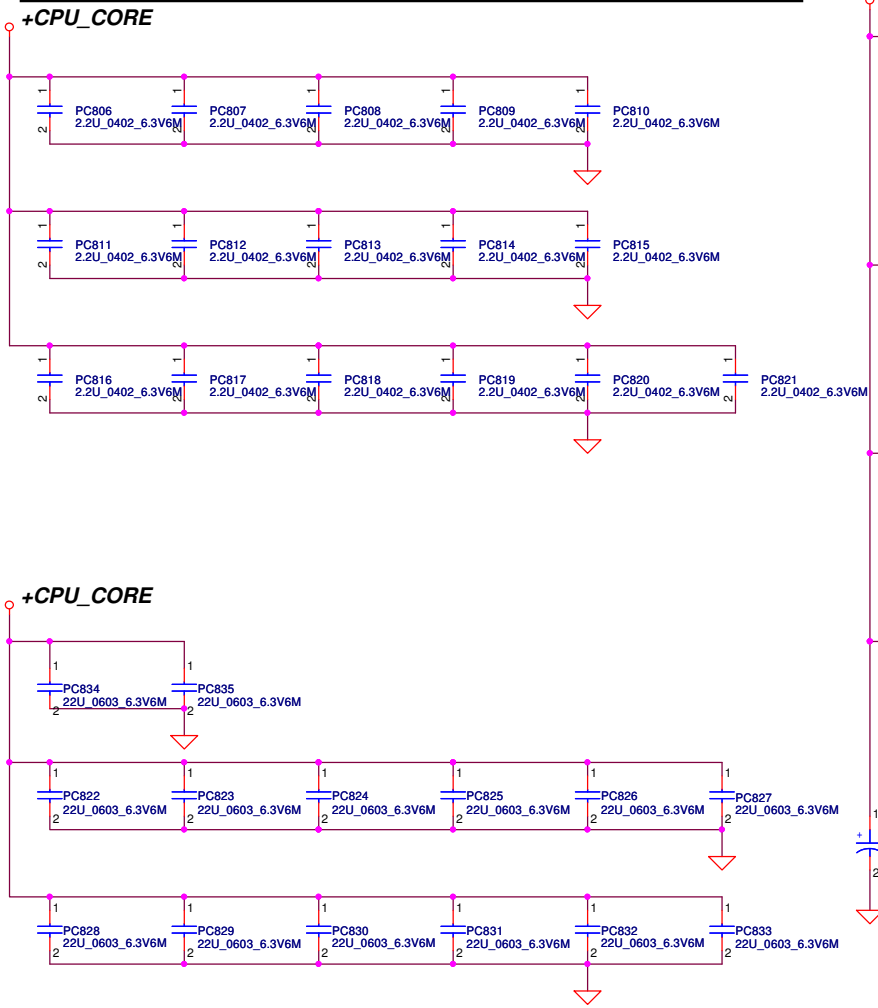
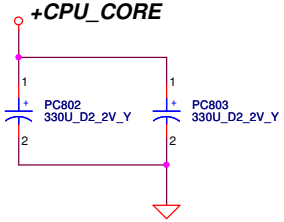
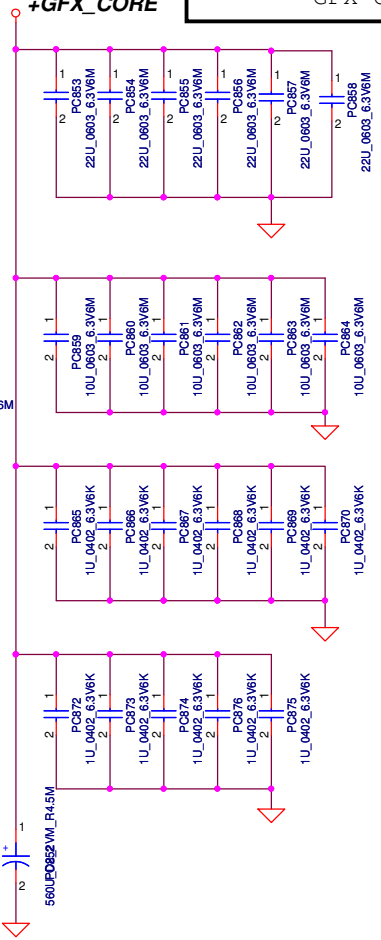
CPU_Core output CAP (Including MLCC) 36.4

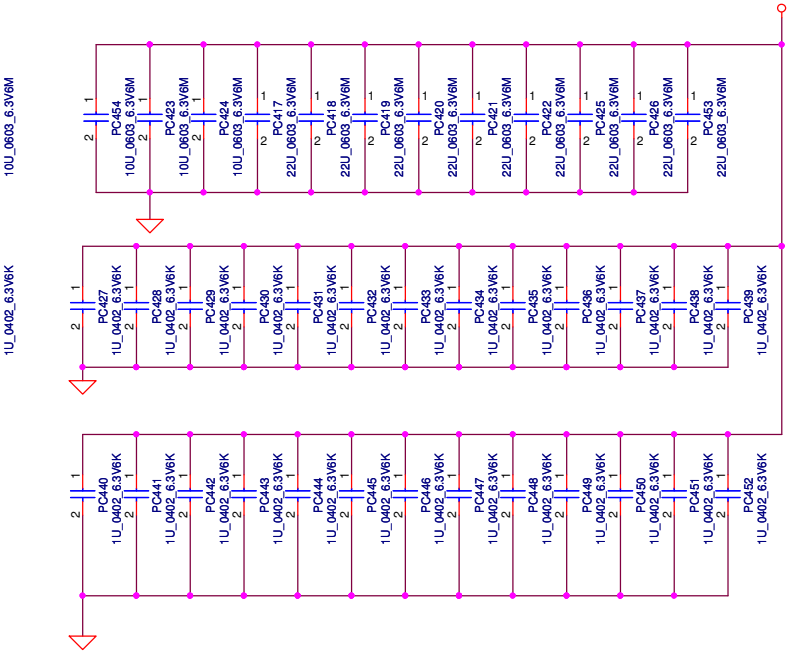




GFX output CAP (Including MLCC) 36.5



VCCP output Cap (Including MLCC) 36.6



Chief River ULV	330uF*9m	22uF	10uF	2.2uF	1uF	470uF	560uF
CPU	2	14		16			
GFX_CORE		6	6		11		1
1.05V_VCCP		9	3		26		1

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

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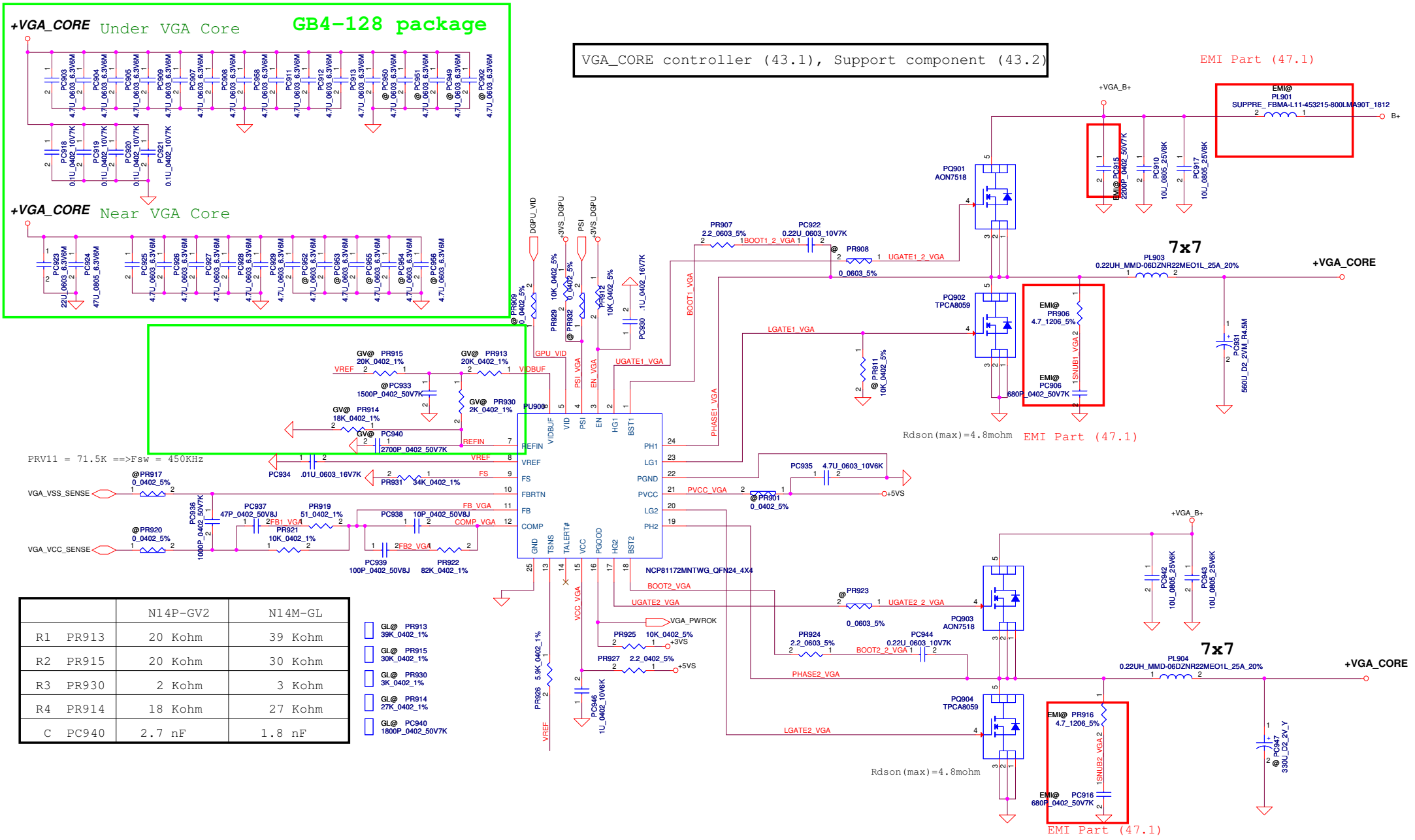

	N14P-GV2	N14M-GL
R1 PR913	20 Kohm	39 Kohm
R2 PR915	20 Kohm	30 Kohm
R3 PR930	2 Kohm	3 Kohm
R4 PR914	18 Kohm	27 Kohm
C PC940	2.7 nF	1.8 nF

GL@ PR913 39K_0402_1%
GL@ PR915 30K_0402_1%
GL@ PR930 3K_0402_1%
GL@ PR914 27K_0402_1%
GL@ PC940 1800P_0402_50V7K

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

Title: +VGA_COREP

Size: Custom | Document Number: VFKTA | Rev: 1.0

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Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	Reson (Why)	
1	EVT--2012/10/24	P45-PWR-BATTERY CONN / OTP	@PD5 / Remove ESD diode	company	For part count reducation	
2	EVT--2012/10/24	P45-PWR-BATTERY CONN / OTP	@PD6 / Remove ESD diode	company	For part count reducation	
3	EVT--2012/10/24	P46-PWR-CHARGER	@PC221 /Remove 10uF capacitor	company	For part count reducation	
4	EVT--2012/10/24	P47-PWR-3VALW/5VALW	PC331 /Reserve	PWR	ME limitation	
5	EVT--2012/10/24	P47-PWR-3VALW/5VALW	@PC354/mount	PWR	ME limitation	
6	EVT--2012/10/24	P47-PWR-3VALW/5VALW	PR337/235K change to 137K	PWR	for RT8243 3V OCP setting	
7	EVT--2012/10/24	P47-PWR-3VALW/5VALW	PR357/156K change to 143K	PWR	for RT8243 5V OCP setting	
8	EVT--2012/10/24	P48-1.5VP/0.75VSP/1.8VSP	PR158/16.2K change to 27.4K	PWR	for RT8207 OCP setting	
9	EVT--2012/10/24	P52-PWR +CPU_CORE DECOUPLING	PC416/ change 560uF	PWR	Based on height and space limitation	
10	EVT--2012/10/24	P52-PWR +CPU_CORE DECOUPLING	PC415/ Remove	PWR	Based on height and space limitation	
11	EVT--2012/10/24	P53-PWR-VGA_COREP	PR929 / Add 10K ohm	HW	Pull high PSI port	
12	EVT--2012/10/24	P53-PWR-VGA_COREP	PR913 / 39k change to 20K(GV)	PWR	For N14 PWM VID setting	
13	EVT--2012/10/24	P53-PWR-VGA_COREP	PR915 / 39k change to 20K(GV) 30K(GL)	PWR	For N14 PWM VID setting	
14	EVT--2012/10/24	P53-PWR-VGA_COREP	PR930 / 1.5k change to 2K(GV) 3K(GL)	PWR	For N14 PWM VID setting	
15	EVT--2012/10/24	P53-PWR-VGA_COREP	PR914 / 30k change to 18K(GV) 24K(GL)	PWR	For N14 PWM VID setting	
16	EVT--2012/10/24	P53-PWR-VGA_COREP	PR904 / 1.5k change to 0K(GV) 3K(GL)	PWR	For N14 PWM VID setting	
17	EVT--2012/10/24	P53-PWR-VGA_COREP	PC940 / Add 2700pF(GV) 1800pF(GL)	PWR	For N14 PWM VID setting	
18	EVT--2012/10/24	P53-PWR-VGA_COREP	PC933 /Reserve	PWR	For N14 PWM VID setting	
19	EVT--2012/10/24	P53-PWR-VGA_COREP	@PC914 /Remove 0.1uF capacitor	company	For part count reducation	
20	EVT--2012/10/24	P53-PWR-VGA_COREP	PR931/71.5K change to 34K	PWR	For NCP81172 Fsw setting	
21	EVT--2012/10/24	P53-PWR-VGA_COREP	PR927/PN change to SD028220B80	PWR	for PN setting error	
22	EVT--2012/10/25	P46-PWR-CHARGER	PQ203/change to TPCA8507	PWR	for design change	MEMO
23	DVT--2012/12/06	P46-PWR-CHARGER	PU200/change to BQ24725RGRR	PWR	for design change	
24	DVT--2012/12/06	P46-PWR-CHARGER	PQ203/ change to TPCA8507	PWR	AON6504 has burnt out issue	
25	DVT--2012/12/06	P47-PWR-3VALW/5VALW	PC534,PC351/Delete	PWR	Based on height and space limitation	
26	DVT--2012/12/06	P47-PWR-3VALW/5VALW	PR335/add 100K ohm	PWR	Pull high +3VL	
27	DVT--2012/12/06	P47-PWR-3VALW/5VALW	PC344/add 4.7U	PWR	for design request	
28	DVT--2012/12/06	P47-PWR-3VALW/5VALW	PC341/change to 4.7U	PWR	for design request	
29	DVT--2012/12/06	P47-PWR-3VALW/5VALW	PC352,PC353/add 150U_D2	PWR	Based on height and space limitation	
30	DVT--2012/12/06	P48-1.5VP/0.75VSP/1.8VSP	PL152/change to 0.68UH	PWR	for design change	
31	DVT--2012/12/06	P49-PWR-1.05VS_VCCP	PL401/change PN	PWR	to integrate PN	
32	DVT--2012/12/06	P49-PWR-1.05VS_VCCP	PR403 PC403/Reserve	EMI	EMI Command	
33	DVT--2012/12/06	P51-CPU_CORE	CPU_CORE(PR5XX,PC5XX)/change solution	PWR	change solution	
34	DVT--2012/12/06	P52-PWR +CPU_CORE DECOUPLING	PC802 PC803/change to 470U	PWR	change solution	
35	DVT--2012/12/06	P54-PWR-VGA_COREP	PR912/add 10K ohm	PWR	pull high +3VS_DGPU	
36	DVT--2012/12/06	P54-PWR-VGA_COREP	PC934/change 0.01U	PWR	For N14 PWM VID setting	
37	DVT--2012/12/06	P54-PWR-VGA_COREP	PL903 PL904/change PN	PWR	have higher loss	
38	DVT--2012/12/06	P45-PWR-BATTERY CONN / OTP	PF2/change PN	company	For cost down	
39	PVT--2013/01/18	P47-PWR-3VALW/5VALW	PC352,PC353/change location to PC331,PC351	PWR	change location	
40	PVT--2013/01/18	P48-1.5VP/0.75VSP/1.8VSP	PC157/change 390U	PWR	for design change	
41	PVT--2013/01/18	P49-PWR-1.05VS_VCCP	PC414 / change 0ohm	PWR	change solution(change to location sense)	
42	PVT--2013/01/18	P52-PWR +CPU_CORE DECOUPLING	PC417,PC418,PC419,PC420,PC421,PC422,PC425/change to 22U	PWR	for 1.05VCCP test	
43	PVT--2013/01/18	P52-PWR +CPU_CORE DECOUPLING	PC426,PC453/add 22U	PWR	for 1.05VCCP test	
44	PVT--2013/01/18	P49-PWR-1.05VS_VCCP	PC407/change 4700P	PWR	for design change	
45	PVT--2013/01/18	P52-PWR +CPU_CORE DECOUPLING	PC416/Delete	PWR	for 1.05VCCP test(change to location sense)	
46	PVT--2013/01/18	P49-PWR-1.05VS_VCCP	PL402/change to 0.68U	PWR	for 1.05VCCP test	
47	PVT--2013/01/18	P51-CPU_CORE	PQ501,PQ503 /change AON7518	PWR	AON7514 EOL	
48	PVT--2013/01/18	P51-CPU_CORE	PR553/Reserve	PWR	change solution	
49	PVT--2013/01/18	P54-PWR-VGA_COREP	PC906 ,PC915,PC916,PR906,PR916/add	EMI	EMI Command	
50	PVT--2013/01/18	P54-PWR-VGA_COREP	PC934/change PN	PWR	change PN	
51	PVT--2013/01/21	P52-PWR +CPU_CORE DECOUPLING	PC802,PC852/change to 560U	PWR	for CPU,GFX Transient	
52	PVT--2013/01/21	P51-CPU_CORE	PQ502,PQ504 /change TPCA8059	PWR	for design change	
53	PVT--2013/01/21	P54-PWR-VGA_COREP	PC947/Reserve	PWR	for VGA Transient(for cost down)	
54	PVT--2013/01/22	P52-PWR +CPU_CORE DECOUPLING	PC802,PC803/change to 330U	PWR	for CPU Transient	
55	Pre-MP--2013/03/04	P49-PWR-1.05VS_VCCP	PR406/add 1k ohm	PWR	for 1.05VCCP test(change to location sense)	
56	Pre-MP--2013/03/04	P53-PWR-VGA_COREP	PR904 PR918 PR928 PC945 remove PR914 change from 24K to 27K	PWR	Remove and change for Richtek solution setting	

Compal Electronics, Inc.

Title: **PIR (PWR)**

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HW PIR (Product Improve Record)

VFKTA LA-9861P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	11/13	39	Add CA39 (SE102104K00)	BOM structure change
2.	11/13	39	Reserve RA31,RA38	EMI request
3.	11/13	41	Change RB36 from 2.2k to 0 ohm and CB50 to @	Design change
4.	11/13	15	Update VGA strap pin all page	Design change
5.	11/21	42	Remove NFC function	Design change
6.	11/21	42	Update CPU config&PN	Design change
7.	11/26	23	change BOM structure C238,C239,C240,C241,C242,C243 to CRT@EMI@	EMI request
8.	11/26	22	Add D92 for LID_SW#_D to isolate the +3VL power rail from LID_SW#	Design change
9.	11/26	24	Add @ to JHDMI Design change	
10.	11/26	37	Change JCARD.10 to SDWP# and JCARD.11 to SDCD.	Design change
	37		Add QW1, RW3, RW4 for normal close type connector.	
11.	11/26	40	Update HDMI power circuit	Design change
12.	11/26	40	Change JSPK from 8 pin to 6 pin (SP02000WS00)	Design change
13.	11/26	40	Remove SPK_DET1 and change SPK_DET0 net name to SPK_DET	Design change
14.	11/26	39	Change RA50 to 269@	Design change
15.	11/26	40	Reverse JSPK to keep same layout routing on MB	Design change
16.	11/27	30	Remove GPIO71 and change SPK_DET1 to SPK_DET	Design change
17.	11/29	30	Add GPIO22 as VRAM_DR_SR# and add RH203, RH205 for BOM control <DIS>	For dual&single rank common bios
18.	11/30	30	Change RH202, RH203 BOM structure to GVDR@ and GVSR@	For dual&single rank common bios
19.	11/30	42	Change H7 to 4P0, Add H19 (3P2N), Change H17, H18 to PTH	ME request
20.	11/30	25	Change UH3 from socket to IC	Design change
21.	11/30	09	Change CC53 to 47U 0805 (SE00000PL00)& add CC50 (SE00000PL00)	For 1206 MLCC Crack issue
	09		Change CC44 to 47U 0805 (SE00000PL00)& add CC40 (SE00000PL00)	
	12		Change CD31 to 47U 0805 (SE00000PL00)	
		38	Change CR10&CR12 to 47U 0805 (SE00000PL00)	
22.	11/30	07	Change RC73 to 0 ohm (do not use short pad on this location)	For debug
23.	11/30	17	Change RV53 pull high to +3VS	Design change
24.	11/30	15	Change RV24 to 4.99K	Strap pin change
25.	11/30	22	Delete D92 and change the netname to BKOFF#	Avoid LCD_INV leak to Touch/B
26.	11/30	23	Add R62 & R63 for CRT undershoot issue	For CRT undershoot issue
27.	11/30	25	Chane UH4, RH269, RH271 to @, change RH267 from shortpad to 0-ohm @.	Design change
28.	11/30	08	Add CC17~CC19 for ESD request	ESD request
29.	11/30	29,41	Move PLT_RST# ESD capacitor (CH104) to EC side (CB13) and mount 0.1uF	ESD request
30.	11/30	05	Change CC63 from @ESD@ to ESD@	ESD request
31.	11/30	41	Change PM_SLP_S4# from pin127 to pin84.	For ENE common code
32.	11/30	41	Change USB_EN#0 from pin84 to pin23.	For ENE common code
33.	11/30	41	Change FB_CLAMP from pin23 to pin127.	For ENE common code
34.	11/30	17	CV57 and CV60 change to 0.01U.	For sequence
35.	11/30	17	RV47 change to 180K.	For sequence
36.	12/03	38	Update USB circuit	For S&C MAX4640 and MAX4641 co-lay circuit
37.	12/04	42	Change H19 to NPTH	Design change
38.	12/04	17	Change QV2 footprint to NC7ST32P5X_SC70-5	For non-A51 part change
39.	12/04	04	Add S&C SMBus address in the table	Design change

HW PIR (Product Improve Record)

QCLA4 LA-8861P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
40.	12/04	41	Add short-pad (RB5) on pin127.	Design change
41.	12/04	13	Reverse DV1, Change DV1, QV8 to OPT@,	
	13		Change FB_CLAMP_MON from pull down to pull high +3VS_DGPU	
42.	12/04	17	Change UV2 PN to SA007320300	Design change
		17	Change UV2, CV58 to OPT@ and change RV50 to @	
43.	12/04	43	Add R5546 put high PCH_PWR_EN to +3VL	Design change
45.	12/05	41	Add CHG_PWR_GATE# pull high 3VL and add RB11 10K.	Design change
46.	12/05	38	S&C IC Pin1 was connected to the EC(GPIO49) Pin82.	Design change

VFKTA LA-9861P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	12/24	17	Change RV43 to 270K	For GC6 timing requirements
2.	12/24	17	Change RV53 to 10K	For GC6 timing requirements
3.	12/24	17	Change RV54 to 33K	For GC6 timing requirements
4.	12/24	17	Change RV50to N14MGL@	N14M-GL doesn't support GC6
5.	12/24	17	Change UV2to N14PGV2@	N14M-GL doesn't support GC6
6.	12/24	17	Change CV58 to @	Cost reduction
7.	12/24	13	Change QV8to N14PGV2@	N14M-GL doesn't support GC6
8.	12/24	13	Change DV1 P/N to SCS00002G00	BOM reduction
9.	01/09	41	Change CB31 to 100P P/NSE071101J80	Design Change
10.	01/09	7,9,25	Change QC3,QC7,QC8,QH1 to SB00000PF00	SB501380020 X1 code
11.	01/15	22	Reserve R267&R266 0 ohm	For EMI cost down
12.	01/15	41	Reserve CB50 1U	Common design
13.	01/15	13	GPIO12 be connected to EC_GPXIOA01(remove EC_DRAMRST_CNTRL_PCH&RC3)	For GPS
14.	01/16	42	Modify JTP pin define	For DFB highlight
15.	01/16	22	Add C17 100P on LED_PWM	For EMI request
16.	01/17	39/42	Add RB12, RB37, connect EC_MUTE_INT from codec to EC	For boot bobo issue
17.	01/17	5/30/42	Reserve CC1,CH1,CB17,CB18,CC35 100P	For ESD
18.	01/17	26	Add RH38 0 ohm on XCLK_RCOMP	For EMI 200M noise

VFKTA LA-9861P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	02/18	06	Swap H_EDP_TXN[0\1] to H_EDP_TXP[0\1]	Design mistake
2.	02/18	22	Change C7 to SE076153K80 (15nF)	for LCD sequence tuning
3.	02/19	05	Delete CC33, CC36, C4; change R1 to short pad	for part count reduce
4.	02/19	07	Change RC73 to short pad	for part count reduce
5.	02/19	09	Delete CC61, CC83; change RC119 to short pad	for part count reduce
6.	02/19	11	Delete CD2, CD15	for part count reduce
7.	02/19	12	Delete CD28, CD46	for part count reduce
8.	02/19	17	Delete CV58	for part count reduce
9.	02/19	22	Change R106 to shortpad	for part count reduce
10.	02/19	23	Delete C250	for part count reduce
11.	02/19	25	Delete CH6, CH100; change RH67, RH68 to short pad	for part count reduce
12.	02/19	26	Delete RH275	for part count reduce
13.	02/19	28	Delete RH254	for part count reduce
14.	02/19	29	Delete CH30, RH287	for part count reduce
15.	02/19	35	Delete CCL2, RCL5, RCL2, net: LAN_X1_R_R, LAN_X1_R	for part count reduce
16.	02/19	36	Delete net: LAN_X1_R	for part count reduce
17.	02/19	37	Change RW1 to shortpad	for part count reduce
18.	02/19	38	Delete CR7, CR8	for part count reduce
19.	02/19	39	Change RA22, RA18, RA24 to short pad	for part count reduce
20.	02/19	41	Delete CB4, CB5, CB50	for part count reduce
21.	02/19	42	Delete SW2, SW3	for part count reduce
22.	02/23	37	Change RW2 to 33Ohm and mount CW9 10PF	for EMI request
23.	03/04	41	Connect RB14 form POK_R to POK and reserve RB13,RB22,CB16	for abnormal shut down power request
24.	03/04	37	Add RW5~RW8 for EMI request and change netname SD_DATAx to SD_DATAx_R on conn side	for EMI request

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