Compal Confidential

PBL01

LA-6733P REV 0.3 Schematic

Intel Sandy Bridge/Cougar Point

DIS

2010-11-02 Rev. 0.3

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: Cover Page		
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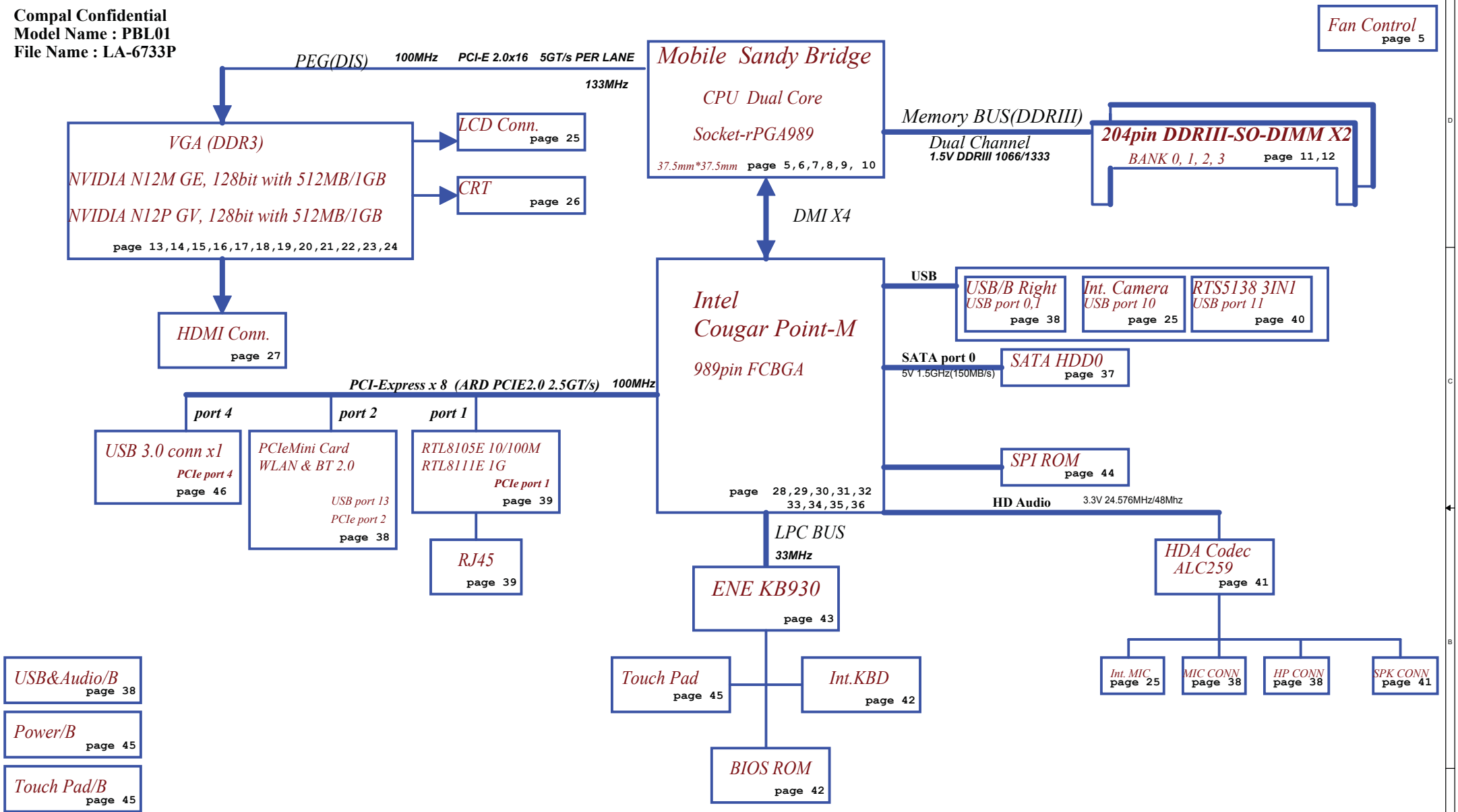
Compal Confidential
Model Name : PBL01
File Name : LA-6733P



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Title: Block Diagrams

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.2

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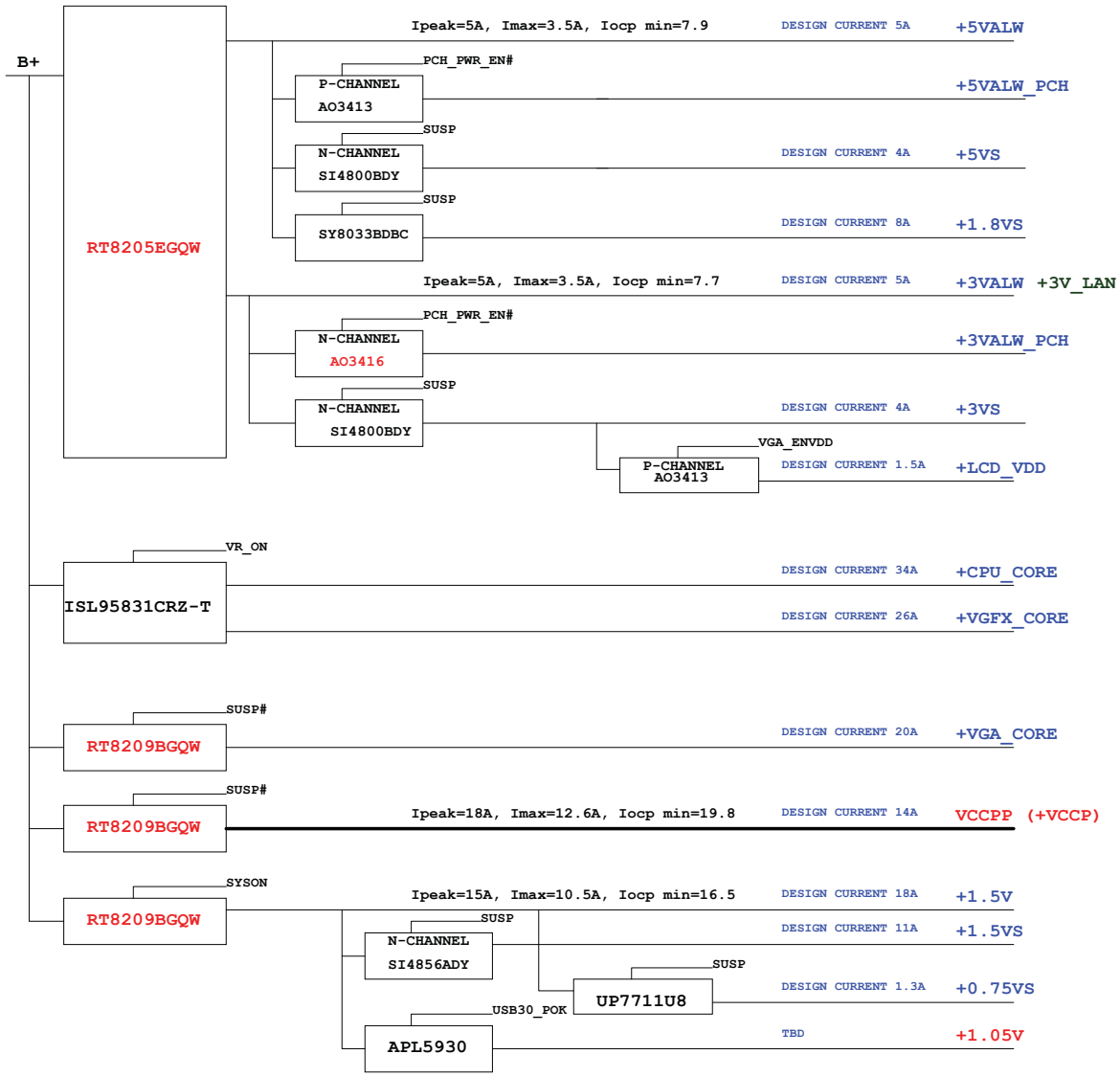

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Title: Power Map

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Power	Device	Address
+3VALW	EC KB930	
+3VL	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB930	
+3VS	GPU Thermal Sensor	
+3VALW	PCH	

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Slot#1--WLAN	

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Title: Notes List

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Terminate DPLL_REF_SSCLK to GND and PLL_REF_SSCLK# to VCCP on Processor if motherboard only supports external graphics.

JCPU1B

MISC
- 32 H_SNB_IVB# → C26 SNB_IVB#
- PAD T1 → TP_SKTOCC# AN34 SKTOCC#

THERMAL
- T5 PAD → H_CATERR# AL33 CATERR#
- 33,43 H_PECI → H_PECI AN33 PECI
- 43 H_PROCHOT# → R58 1 2 H_PROCHOT#_R 56_0402_5% AL32 PROCHOT#
- 33 H_THERMTRIP# → R14 1 2 H_THERMTRIP#_R 0_0402_5% AN32 THERMTRIP#

PWR MANAGEMENT
- 30 H_PM_SYNC → AM34 PM_SYNC
- 33 H_PWRGOOD → H_PWRGOOD AP33 UNCOREPWRGOOD
- PM_SYS_PWRGD_BUF → R79 1 2 PM_DRAM_PWRGD_R 130_0402_5% V8 SM_DRAMPWROK
- BUF_CPU_RST# → AR33 RESET#

CLOCKS
- BCLK A28 / BCLK# A27 → CLK_CPU_DMI 29 / CLK_CPU_DMI# 29
- DPLL_REF_SSCLK A16 / DPLL_REF_SSCLK# A15 → R126 1K_0402_5% / R115 1K_0402_5% → +VCCP → eDP

DDR3 MISC
- SM_DRAMRST# R8 → H_DRAMRST# → H_DRAMRST# 7
- SM_RCOMP[0] AK1 → SM_RCOMP_0 RC42 2 → 1 140_0402_1%
- SM_RCOMP[1] A5 → SM_RCOMP_1 RC43 2 → 1 25.5_0402_1%
- SM_RCOMP[2] A4 → SM_RCOMP_2 RC45 2 → 1 200_0402_1%
- DDR3 Compensation Signals Layout Note:Please these resistors near Processor
- from DDR

JTAG & BPM
- PRDY# AP29 → T9 PAD
- PREQ# AP27 → T10 PAD
- TCK AR26 → T4 PAD
- TMS AR27 → T6 PAD
- TRST# AP30 → T7 PAD
- TDI AR28 → T2 PAD
- TDO AP26 → T3 PAD
- DBR# AL35 → T8 PAD
- BPM#[0] AT28
- BPM#[1] AR29
- BPM#[2] AR30
- BPM#[3] AT30
- BPM#[4] AP32
- BPM#[5] AR31
- BPM#[6] AT31
- BPM#[7] AR32

Sandy Bridge_rPGA_Rev0p61
CONN@

Processor Pullups

+VCCP
- R47 2 1 62_0402_5% H_PROCHOT#
- R50 2 1 10K_0402_5% H_PWRGOOD

Follow DG 0.71

+3VALW
- C85 0.1U_0402_16V4Z
- R104 0_0402_5%
- 30 PWROK
- 30 DRAMPWROK
- U5 74AHC1G08DCKR_SC70-5
- PM_SYS_PWRGD_BUF
- +1.5V_CPU_VDDQ
- R81 200_0402_5%
- @R110 39_0402_5%
- 47,54 SUSP
- @Q5 2N7002_SOT23

Buffered reset to CPU

+3VS
- C84 0.1U_0402_16V4Z
- +VCCP
- R64 75_0402_5%
- R72 43_0402_1%
- U3 SN74LVC1G07DCKR_SC70-5
- 2,3,8,39,43,46 PLT_RST#
- R15 0_0402_5%
- BUFO_CPU_RST#
- BUF_CPU_RST#
- @R73 0_0402_5%

FAN Control Circuit

+5VS
- 1A
- C863 10U_0805_10V4Z
- U58 G996P11U_SO8 (EN, VIN, VOUT, VSET, GND)
- 43 EN_DFAN1
- +FAN1
- 10mil
- C1 10U_0805_10V4Z
- @C864 1000P_0402_50V7K
- JFAN ACES_85204-0300N @
- R3 10K_0402_5%
- +3VS
- FAN_SPEED1 43
- C865@ 0.01U_0402_25V7K

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Title: Sandy Bridge(1/6)-CLK/MISC/JTAG/XDP/FAN

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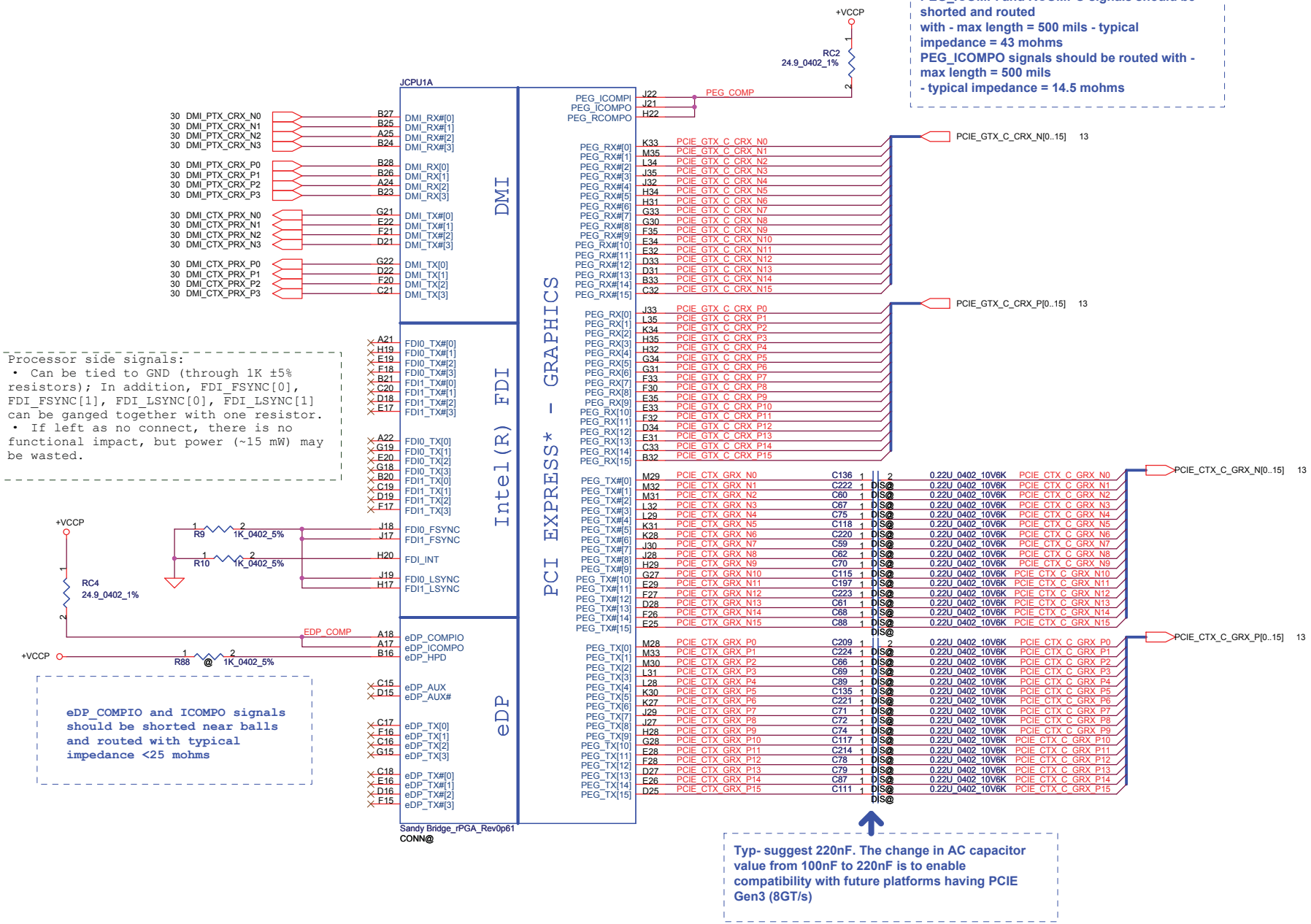

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Compal Electronics, Inc.

Title: Sandy Bridge(2/6)-DMI/FDI/PEG/eDP

Size	Document Number	Rev
Custom	PBL01 LA6733P M/B	0.3

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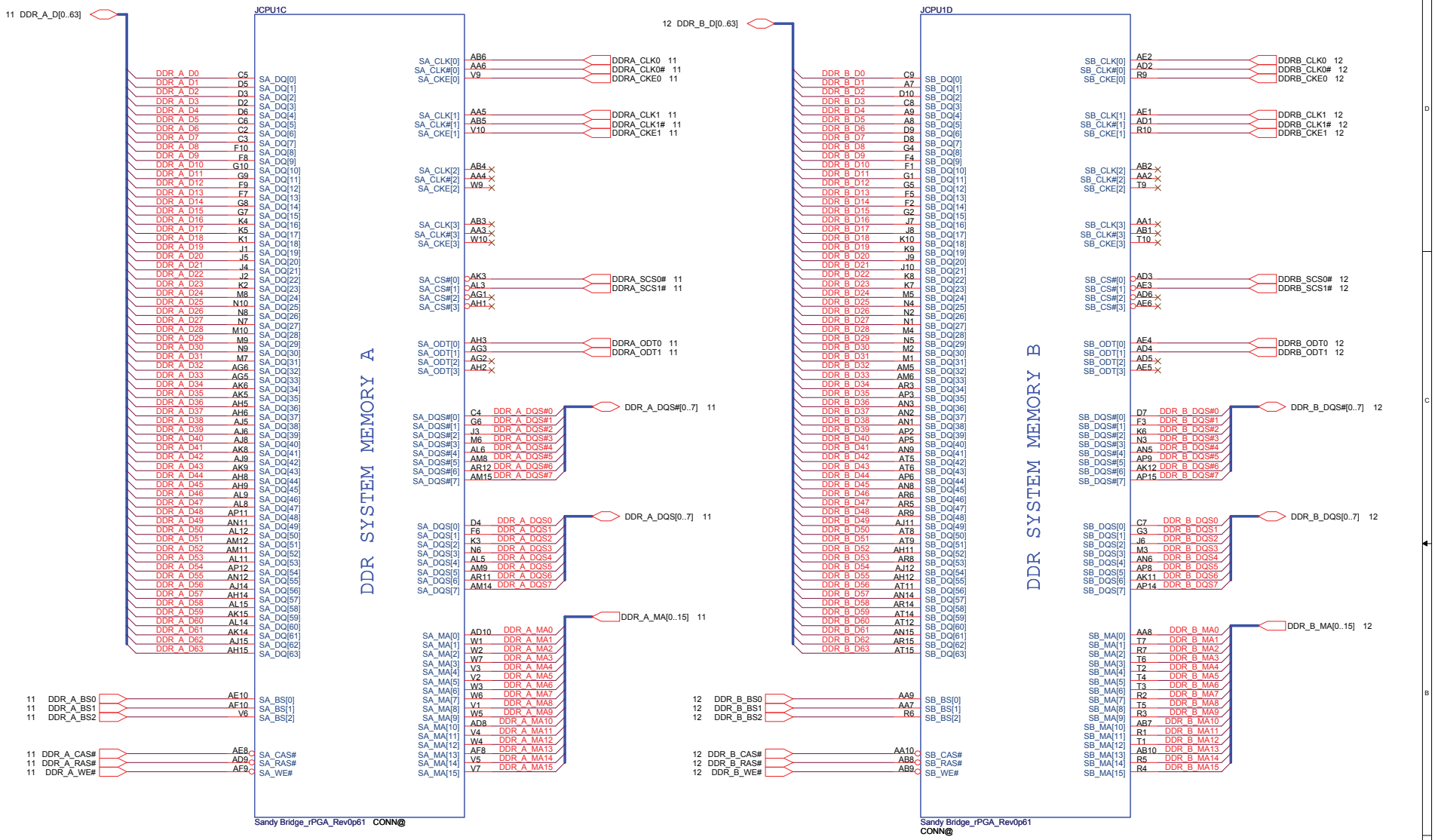

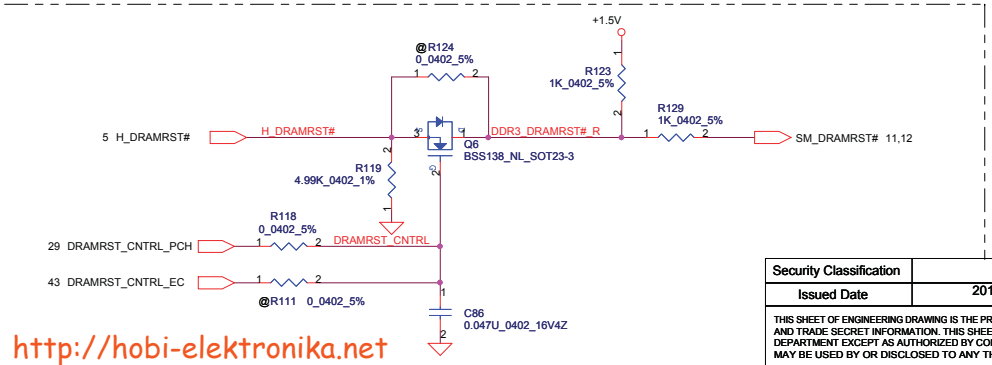

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Compal Electronics, Inc.

Title: Sandy Bridge(3/6)-DDR III

Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.3

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Group1

POWER

+CPU_CORE

JCPU1F

94A

18A

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

Material Note (+VCCP)

330uF/ 9m ohm, number are 4
SGA20331E10 for 330uF
16 * 22uF 0805
10 * 10uF 0805

(Place these capacitors under CPU socket Edge, top layer)

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
- can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

Cap quantity follow 43890_HR_CHKLST_Rev07

Resistors close to VR

Close to CPU

reserve for test
please co-layout with CC172

Sandy Bridge_rPGA_Rev0p61
CONN@

POWER

Group2

JCPU1G

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

Sandy Bridge_rPGA_Rev0p61
CONN@

+V_SM_VREF should have 20 mil trace width

Follow DG 0.71 page 6

(9A,360mils ,Via NO.= 18)

OCP (min)=10.8A

+1.5V_CPU_VDDQ Source

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Title: Sandy Bridge(4/6)-PWR

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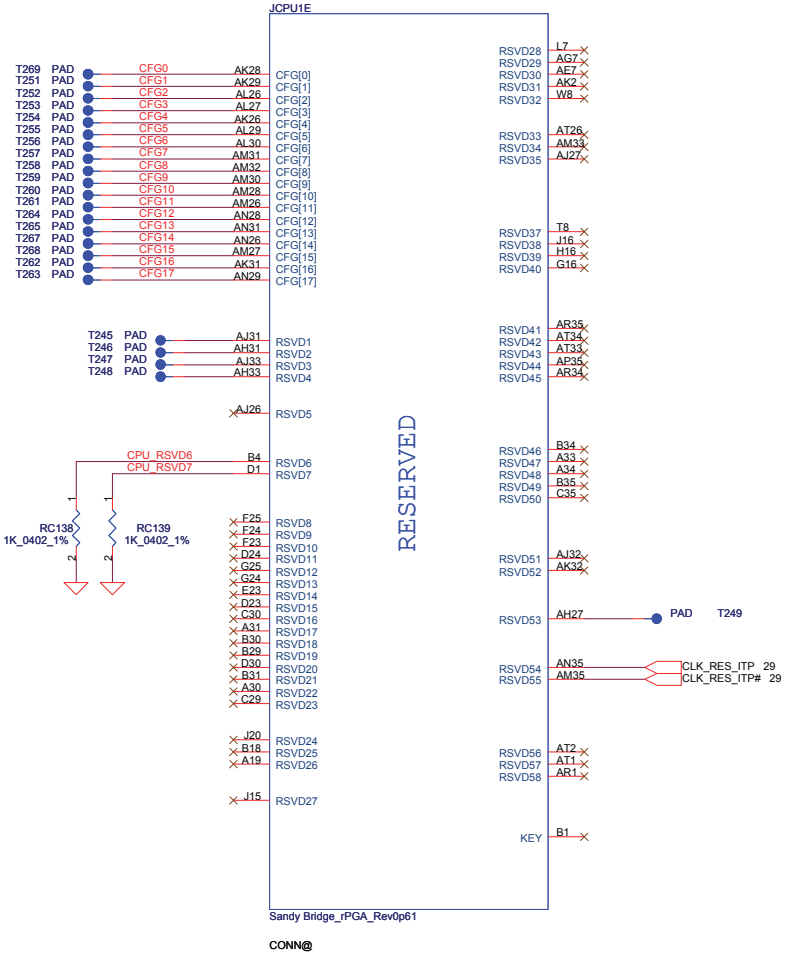
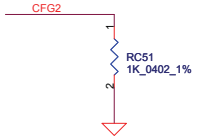
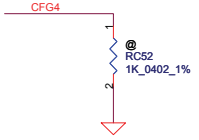
CFG Straps for Processor

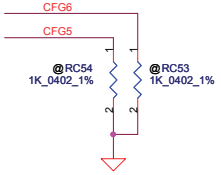




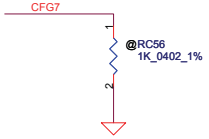
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: Sandy Bridge(5/6) Reserve

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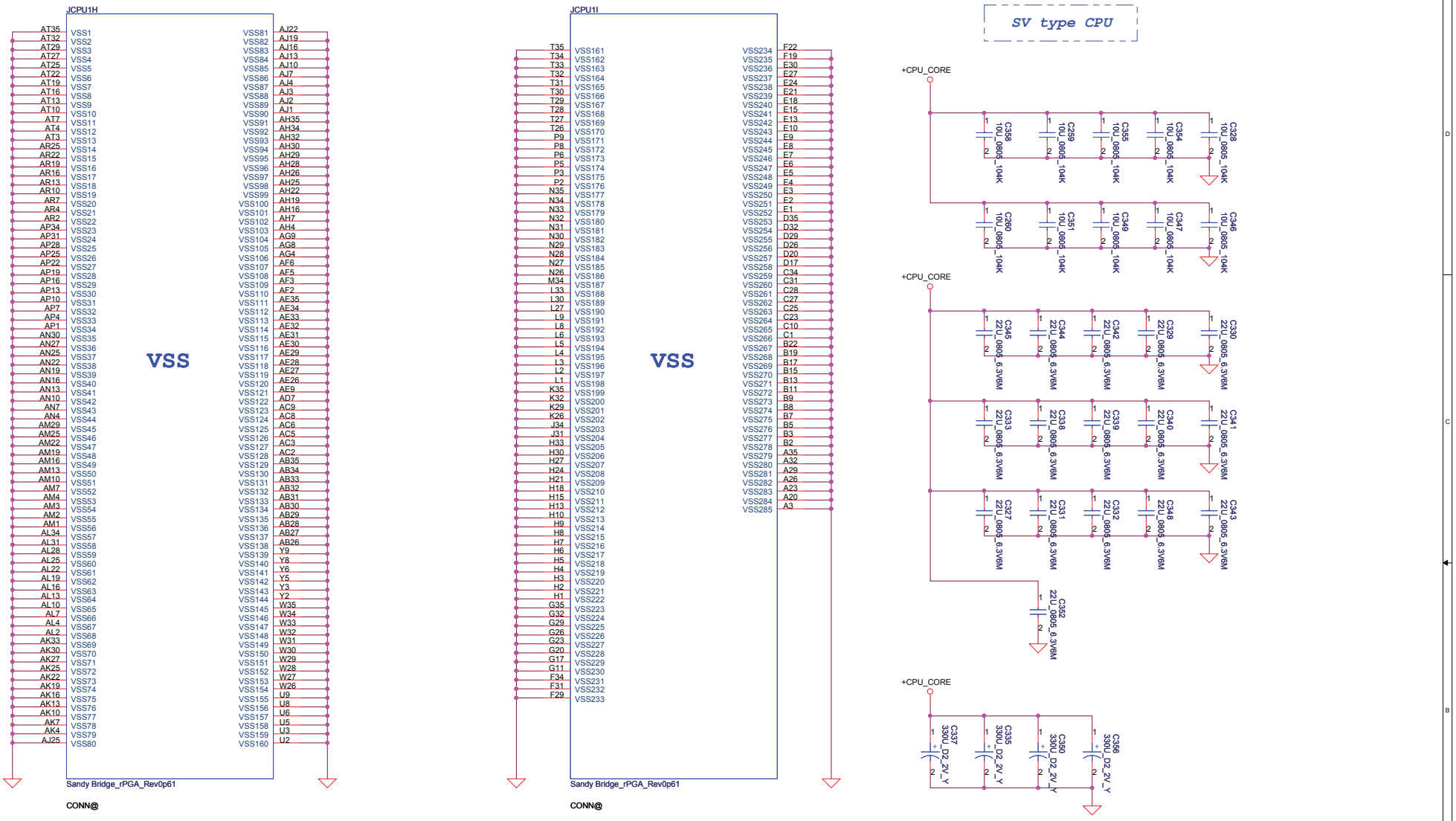

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Title: Sandy Bridge(6/6)-GND

Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.3

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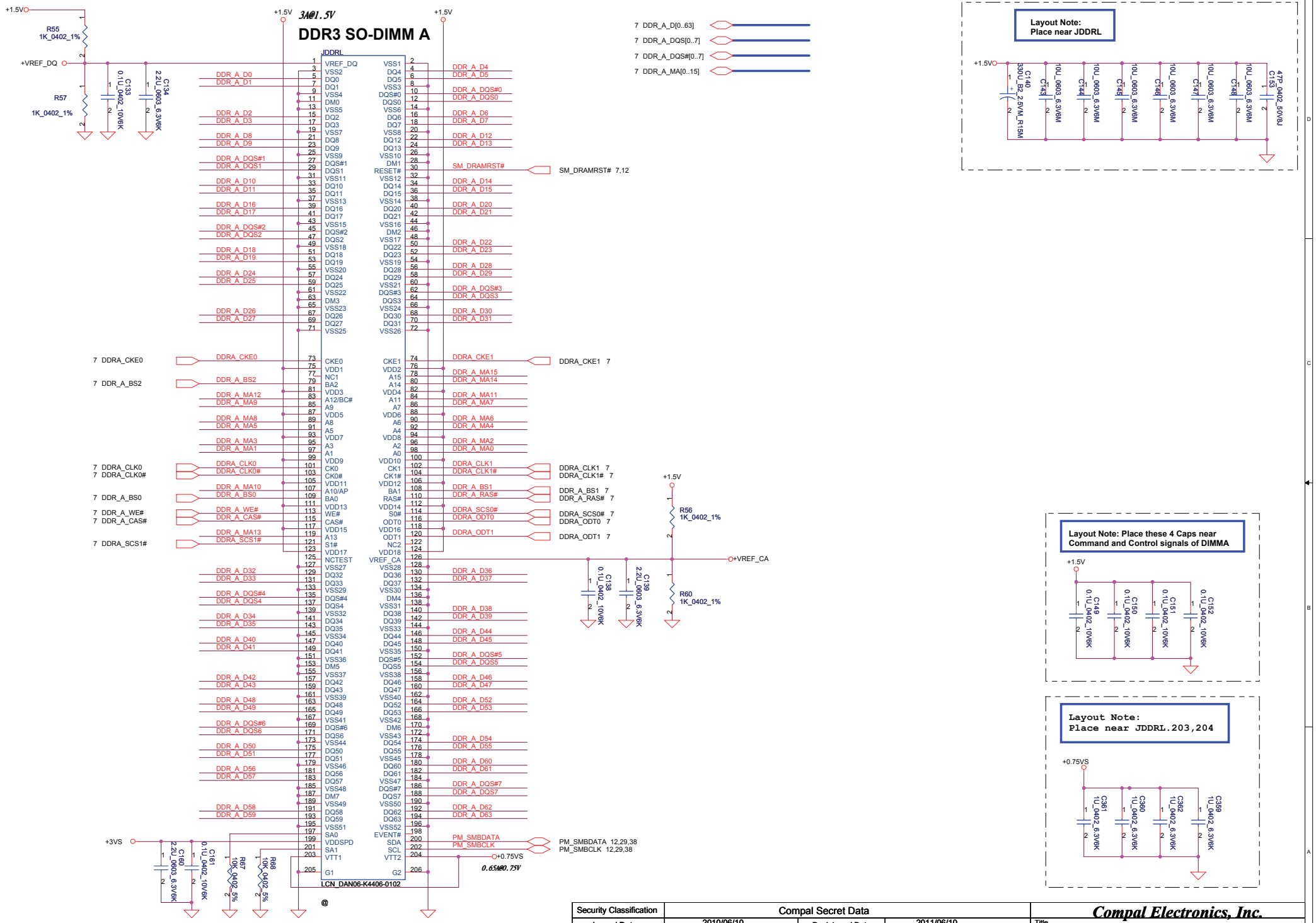
DDR3 SO-DIMM A



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Title: DDRIII-SODIMM0

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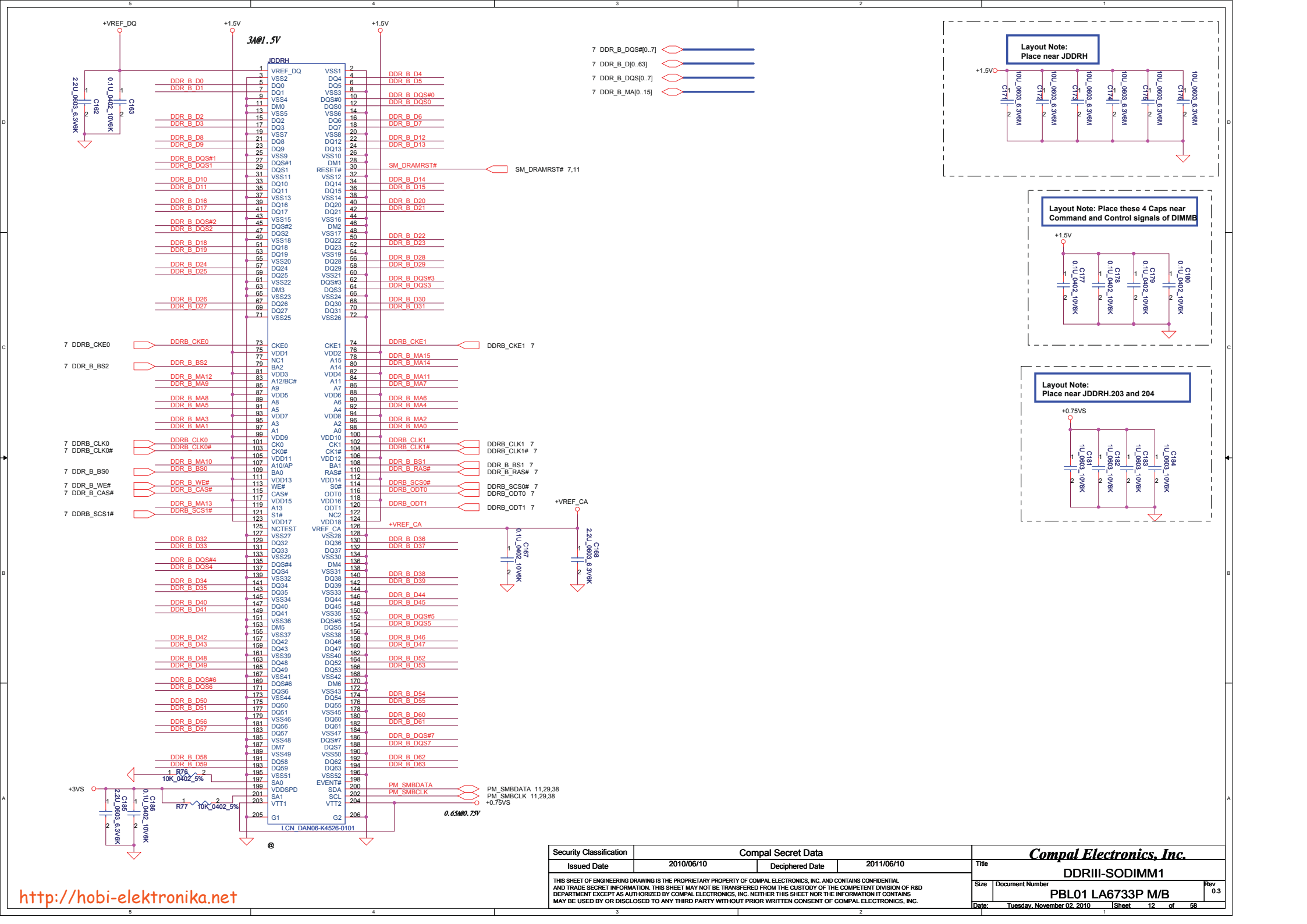
+VREF_DQ
+1.5V
+1.5V
3A@1.5V
JDDRH
LCN_DAN06-K4526-0101
7 DDR_B_DQS#[0..7]
7 DDR_B_D[0..63]
7 DDR_B_DQS[0..7]
7 DDR_B_MA[0..15]
SM_DRAMRST# 7,11
DDRB_CKE1 7
DDRB_CLK1 7
DDRB_CLK1# 7
DDR_B_BS1 7
DDR_B_RAS# 7
DDRB_SCS0# 7
DDRB_ODT0 7
DDRB_ODT1 7
+VREF_CA
PM_SMBDATA 11,29,38
PM_SMBCLK 11,29,38
+0.75VS
+3VS
0.65A@0.75V
@
Layout Note:
Place near JDDRH
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB
Layout Note:
Place near JDDRH.203 and 204
+0.75VS
http://hobi-elektronika.net
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2011/06/10
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Title
DDRIII-SODIMM1
Size
Document Number
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Rev
0.3
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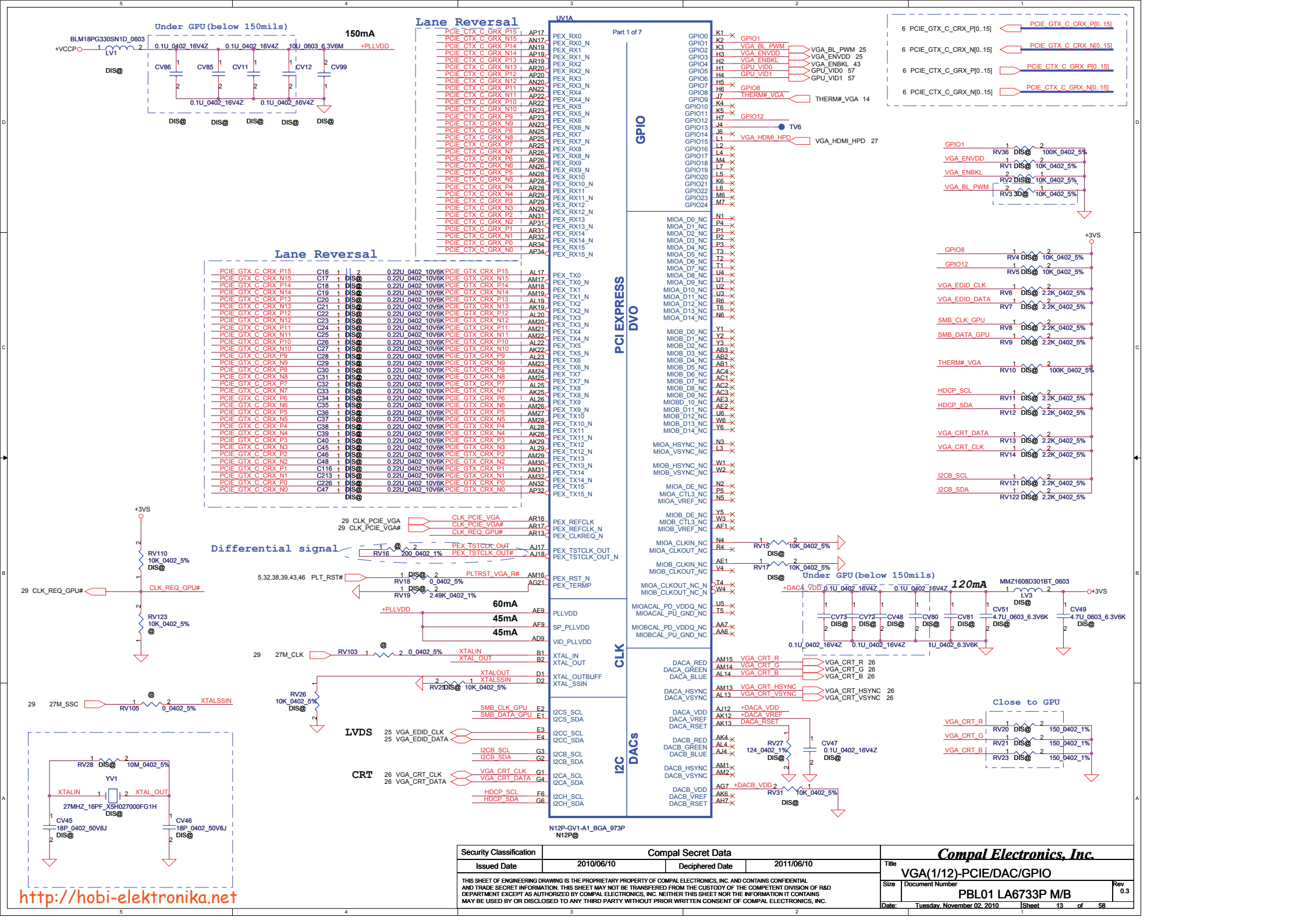
Under GPU(below 150mils)
150mA
BLM18PG330SN1D_0603
+VCCP
LV1
+PLLVDD
0.1U_0402_16V4Z
0.1U_0402_16V4Z
10U_0603_6.3V6M
CV86
CV85
CV11
CV12
CV99
DIS@
Lane Reversal
UV1A
Part 1 of 7
PCIE_CTX_C_GRX_P15
PCIE_CTX_C_GRX_N15
PCIE_CTX_C_GRX_P14
PCIE_CTX_C_GRX_N14
PCIE_CTX_C_GRX_P13
PCIE_CTX_C_GRX_N13
PCIE_CTX_C_GRX_P12
PCIE_CTX_C_GRX_N12
PCIE_CTX_C_GRX_P11
PCIE_CTX_C_GRX_N11
PCIE_CTX_C_GRX_P10
PCIE_CTX_C_GRX_N10
PCIE_CTX_C_GRX_P9
PCIE_CTX_C_GRX_N9
PCIE_CTX_C_GRX_P8
PCIE_CTX_C_GRX_N8
PCIE_CTX_C_GRX_P7
PCIE_CTX_C_GRX_N7
PCIE_CTX_C_GRX_P6
PCIE_CTX_C_GRX_N6
PCIE_CTX_C_GRX_P5
PCIE_CTX_C_GRX_N5
PCIE_CTX_C_GRX_P4
PCIE_CTX_C_GRX_N4
PCIE_CTX_C_GRX_P3
PCIE_CTX_C_GRX_N3
PCIE_CTX_C_GRX_P2
PCIE_CTX_C_GRX_N2
PCIE_CTX_C_GRX_P1
PCIE_CTX_C_GRX_N1
PCIE_CTX_C_GRX_P0
PCIE_CTX_C_GRX_N0
PEX_RX0
PEX_RX0_N
PEX_RX1
PEX_RX1_N
PEX_RX2
PEX_RX2_N
PEX_RX3
PEX_RX3_N
PEX_RX4
PEX_RX4_N
PEX_RX5
PEX_RX5_N
PEX_RX6
PEX_RX6_N
PEX_RX7
PEX_RX7_N
PEX_RX8
PEX_RX8_N
PEX_RX9
PEX_RX9_N
PEX_RX10
PEX_RX10_N
PEX_RX11
PEX_RX11_N
PEX_RX12
PEX_RX12_N
PEX_RX13
PEX_RX13_N
PEX_RX14
PEX_RX14_N
PEX_RX15
PEX_RX15_N
PCI EXPRESS
GPIO
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
VGA_BL_PWM
VGA_ENVDD
VGA_ENBKL
GPU_VID0
GPU_VID1
THERM#_VGA
TV6
VGA_HDMI_HPD
DVO
MIOA_D0_NC
MIOA_D1_NC
MIOA_D2_NC
MIOA_D3_NC
MIOA_D4_NC
MIOA_D5_NC
MIOA_D6_NC
MIOA_D7_NC
MIOA_D8_NC
MIOA_D9_NC
MIOA_D10_NC
MIOA_D11_NC
MIOA_D12_NC
MIOA_D13_NC
MIOA_D14_NC
MIOB_D0_NC
MIOB_D1_NC
MIOB_D2_NC
MIOB_D3_NC
MIOB_D4_NC
MIOB_D5_NC
MIOB_D6_NC
MIOB_D7_NC
MIOB_D8_NC
MIOB_D9_NC
MIOBD_10_NC
MIOB_D11_NC
MIOB_D12_NC
MIOB_D13_NC
MIOB_D14_NC
MIOA_HSYNC_NC
MIOA_VSYNC_NC
MIOB_HSYNC_NC
MIOB_VSYNC_NC
MIOA_DE_NC
MIOA_CTL3_NC
MIOA_VREF_NC
MIOB_DE_NC
MIOB_CTL3_NC
MIOB_VREF_NC
MIOA_CLKIN_NC
MIOA_CLKOUT_NC
MIOB_CLKIN_NC
MIOB_CLKOUT_NC
MIOA_CLKOUT_NC_N
MIOB_CLKOUT_NC_N
MIOACAL_PD_VDDQ_NC
MIOACAL_PU_GND_NC
MIOBCAL_PD_VDDQ_NC
MIOBCAL_PU_GND_NC
CLK
PLLVDD
SP_PLLVDD
VID_PLLVDD
XTAL_IN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN
I2C
DACs
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_HSYNC
DACA_VSYNC
DACA_VDD
DACA_VREF
DACA_RSET
DACB_RED
DACB_GREEN
DACB_BLUE
DACB_HSYNC
DACB_VSYNC
DACB_VDD
DACB_VREF
DACB_RSET
N12P-GV1-A1_BGA_973P
N12P@
6 PCIE_GTX_C_CRX_P[0..15]
6 PCIE_GTX_C_CRX_N[0..15]
6 PCIE_CTX_C_GRX_P[0..15]
6 PCIE_CTX_C_GRX_N[0..15]
Lane Reversal
PCIE_GTX_C_CRX_P15
PCIE_GTX_C_CRX_N15
PCIE_GTX_C_CRX_P14
PCIE_GTX_C_CRX_N14
PCIE_GTX_C_CRX_P13
PCIE_GTX_C_CRX_N13
PCIE_GTX_C_CRX_P12
PCIE_GTX_C_CRX_N12
PCIE_GTX_C_CRX_P11
PCIE_GTX_C_CRX_N11
PCIE_GTX_C_CRX_P10
PCIE_GTX_C_CRX_N10
PCIE_GTX_C_CRX_P9
PCIE_GTX_C_CRX_N9
PCIE_GTX_C_CRX_P8
PCIE_GTX_C_CRX_N8
PCIE_GTX_C_CRX_P7
PCIE_GTX_C_CRX_N7
PCIE_GTX_C_CRX_P6
PCIE_GTX_C_CRX_N6
PCIE_GTX_C_CRX_P5
PCIE_GTX_C_CRX_N5
PCIE_GTX_C_CRX_P4
PCIE_GTX_C_CRX_N4
PCIE_GTX_C_CRX_P3
PCIE_GTX_C_CRX_N3
PCIE_GTX_C_CRX_P2
PCIE_GTX_C_CRX_N2
PCIE_GTX_C_CRX_P1
PCIE_GTX_C_CRX_N1
PCIE_GTX_C_CRX_P0
PCIE_GTX_C_CRX_N0
0.22U_0402_10V6K
Differential signal
29 CLK_PCIE_VGA
29 CLK_PCIE_VGA#
CLK_REQ_GPU#
PEX_REFCLK
PEX_REFCLK_N
PEX_CLKREQ_N
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
PEX_RST_N
PEX_TERMP
5,32,38,39,43,46 PLT_RST#
PLTRST_VGA_R#
RV16 200_0402_1%
RV18 0_0402_5%
RV19 2.49K_0402_1%
60mA
45mA
45mA
+PLLVDD
29 27M_CLK
RV103 0_0402_5%
XTALIN
XTAL_OUT
RV25 10K_0402_5%
29 27M_SSC
RV105 0_0402_5%
XTALSSIN
RV26 10K_0402_5%
SMB_CLK_GPU
SMB_DATA_GPU
I2CS_SCL
I2CS_SDA
LVDS
25 VGA_EDID_CLK
25 VGA_EDID_DATA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
CRT
26 VGA_CRT_CLK
26 VGA_CRT_DATA
I2CA_SCL
I2CA_SDA
HDCP_SCL
HDCP_SDA
I2CH_SCL
I2CH_SDA
+3VS
RV110 10K_0402_5%
RV123 10K_0402_5%
RV28 10M_0402_5%
YV1
27MHZ_16PF_X5H027000FG1H
CV45 18P_0402_50V8J
CV46 18P_0402_50V8J
RV15 10K_0402_5%
RV17 10K_0402_5%
Under GPU(below 150mils)
120mA
MMZ1608D301BT_0603
LV3
+DACA_VDD
CV73
CV72
CV48
CV80
CV81
CV51 4.7U_0603_6.3V6K
CV49 4.7U_0603_6.3V6K
0.1U_0402_16V4Z
1U_0402_6.3V6K
RV27 124_0402_1%
CV47 0.1U_0402_16V4Z
RV31 10K_0402_5%
VGA_CRT_R
VGA_CRT_G
VGA_CRT_B
VGA_CRT_HSYNC
VGA_CRT_VSYNC
Close to GPU
RV20 150_0402_1%
RV21 150_0402_1%
RV23 150_0402_1%
RV36 100K_0402_5%
RV1 10K_0402_5%
RV2 10K_0402_5%
RV3 10K_0402_5%
RV4 10K_0402_5%
RV5 10K_0402_5%
RV6 2.2K_0402_5%
RV7 2.2K_0402_5%
RV8 2.2K_0402_5%
RV9 2.2K_0402_5%
RV10 100K_0402_5%
RV11 2.2K_0402_5%
RV12 2.2K_0402_5%
RV13 2.2K_0402_5%
RV14 2.2K_0402_5%
RV121 2.2K_0402_5%
RV122 2.2K_0402_5%
I2CB_SCL
I2CB_SDA
http://hobi-elektronika.net
Security Classification
Compal Secret Data
Issued Date
2010/06/10
Deciphered Date
2011/06/10
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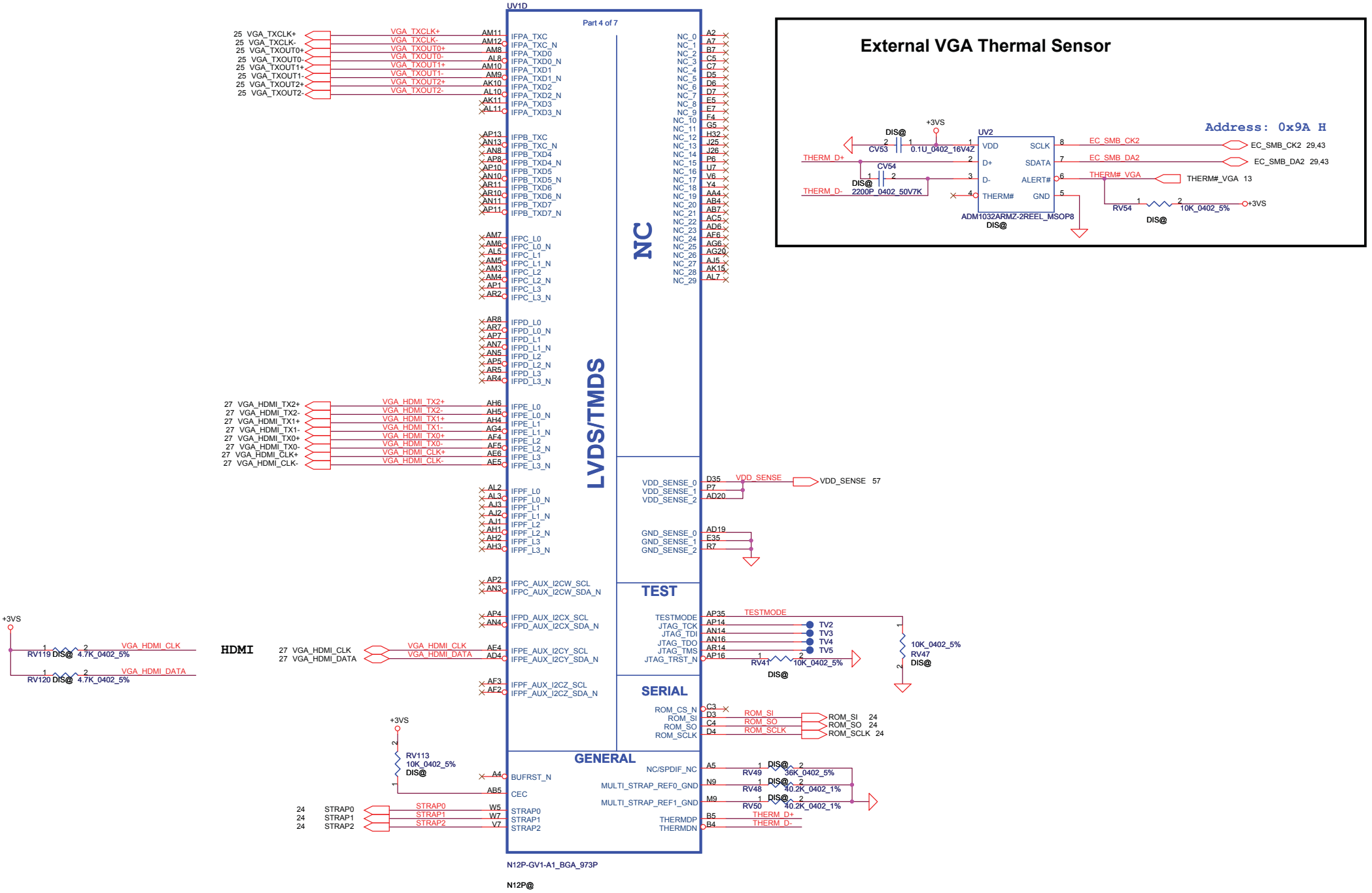
Compal Electronics, Inc.
Title
VGA(1/12)-PCIE/DAC/GPIO
Size
Document Number
PBL01 LA6733P M/B
Rev
0.3
Date: Tuesday, November 02, 2010
Sheet 13 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: VGA(2/12)-LVDS/HDMI/DP/THM

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

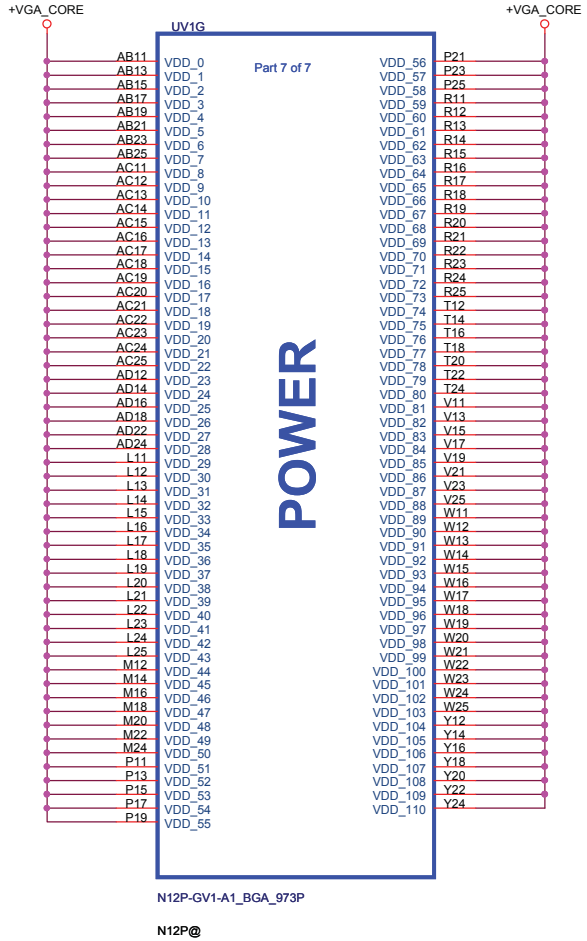
Date: Tuesday, November 02, 2010 | Sheet 14 of 58

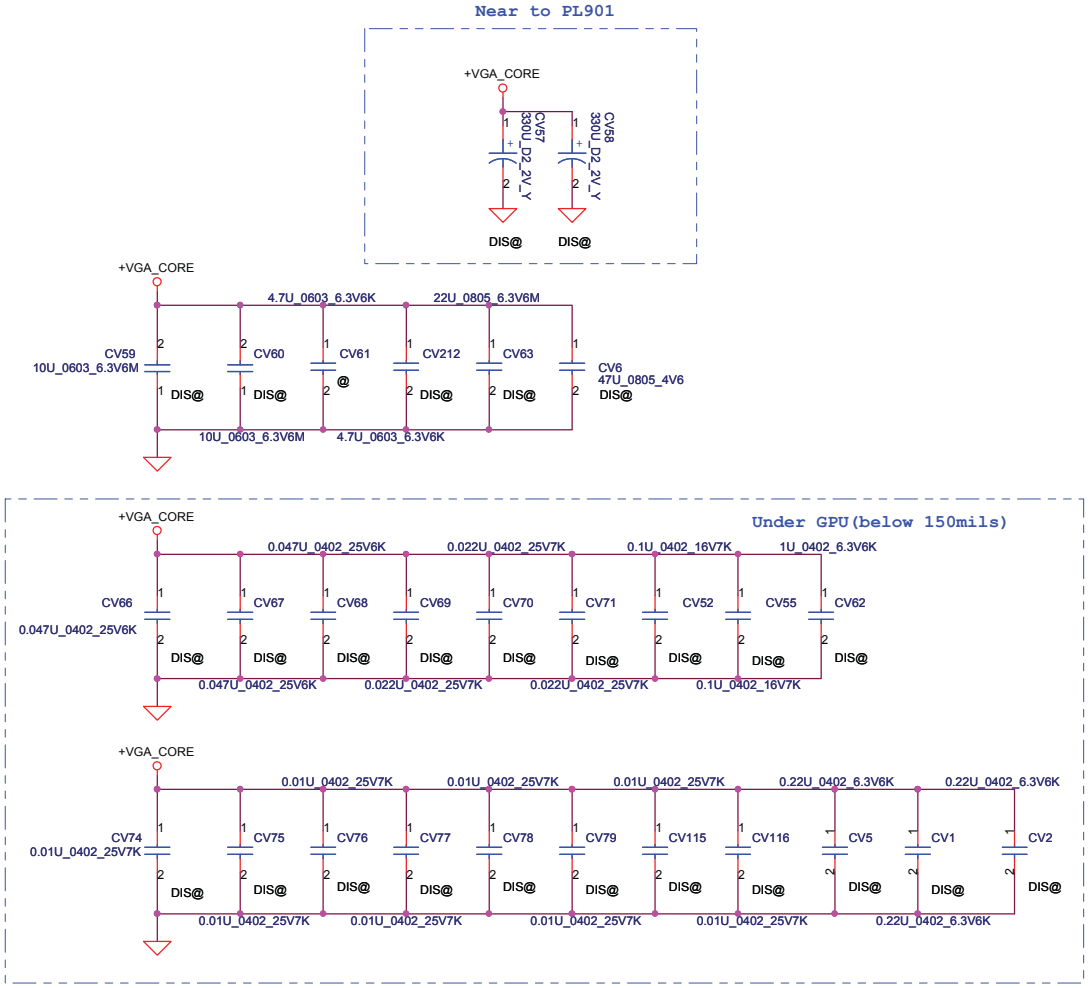
N12M-GE-B Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0			1.0 V
P8-P12			0.85 V

N12P-GV1 Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0(Cold)			0.925 V
P0(Hot)			0.875 V
P8-P12			0.825 V





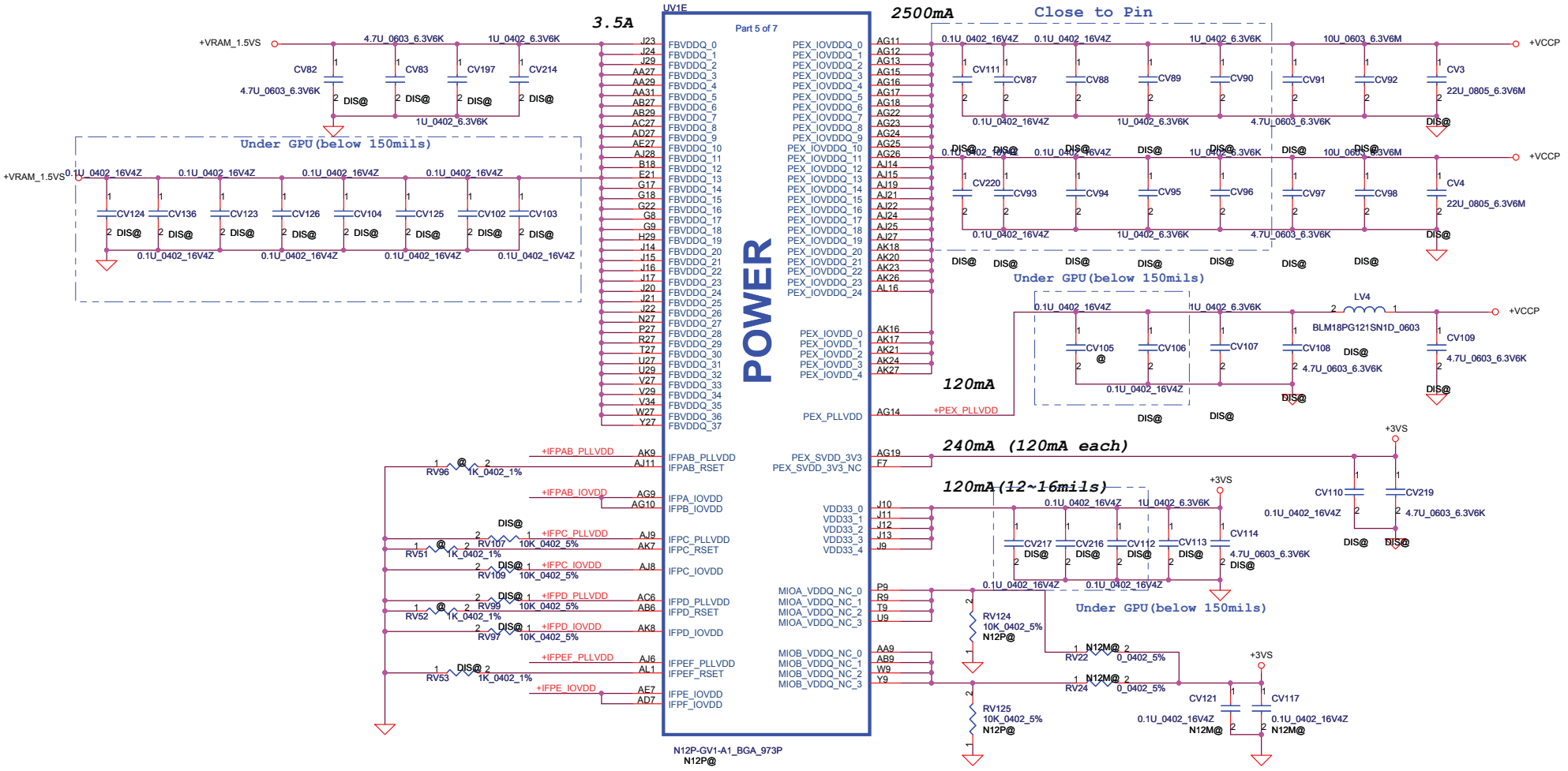
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

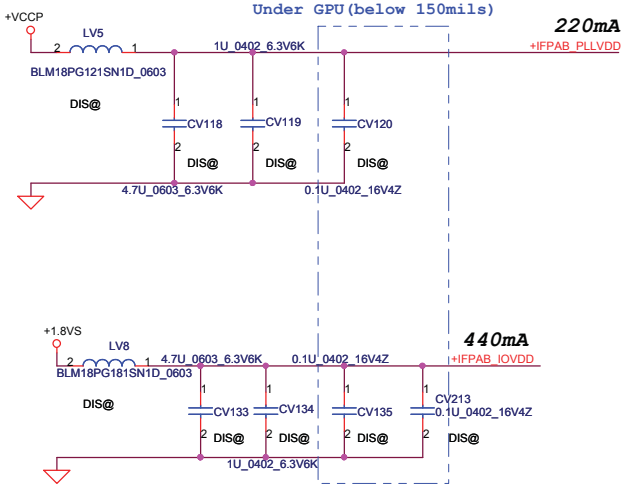
Compal Electronics, Inc.

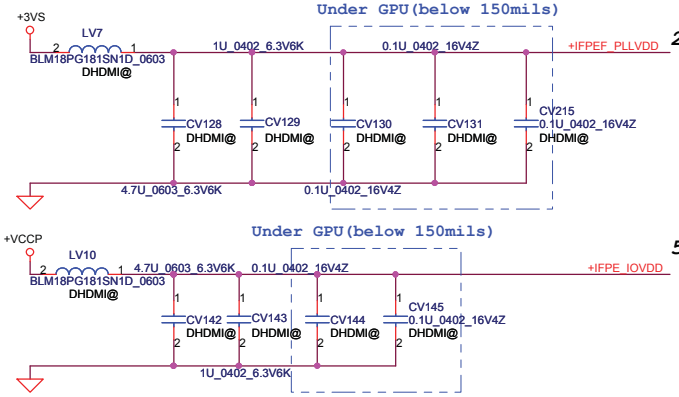
Title: VGA(3/12)-VGA CORE

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, October 26, 2010 | Sheet 15 of 58







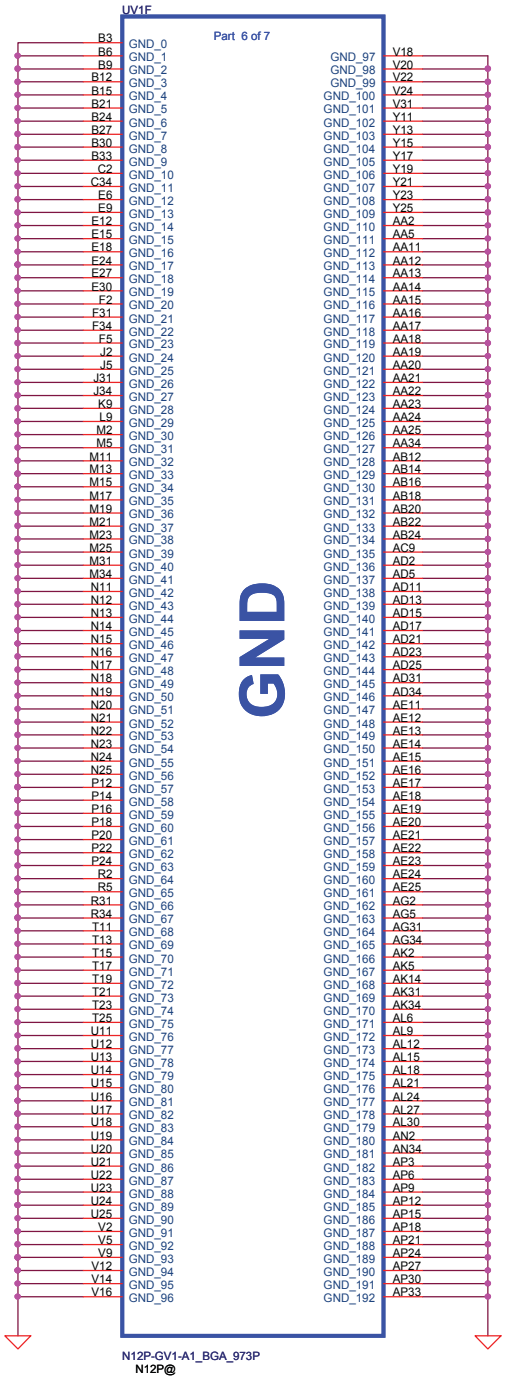
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: VGA(4/12)-POWER

Size: | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, October 26, 2010 | Sheet 16 of 58



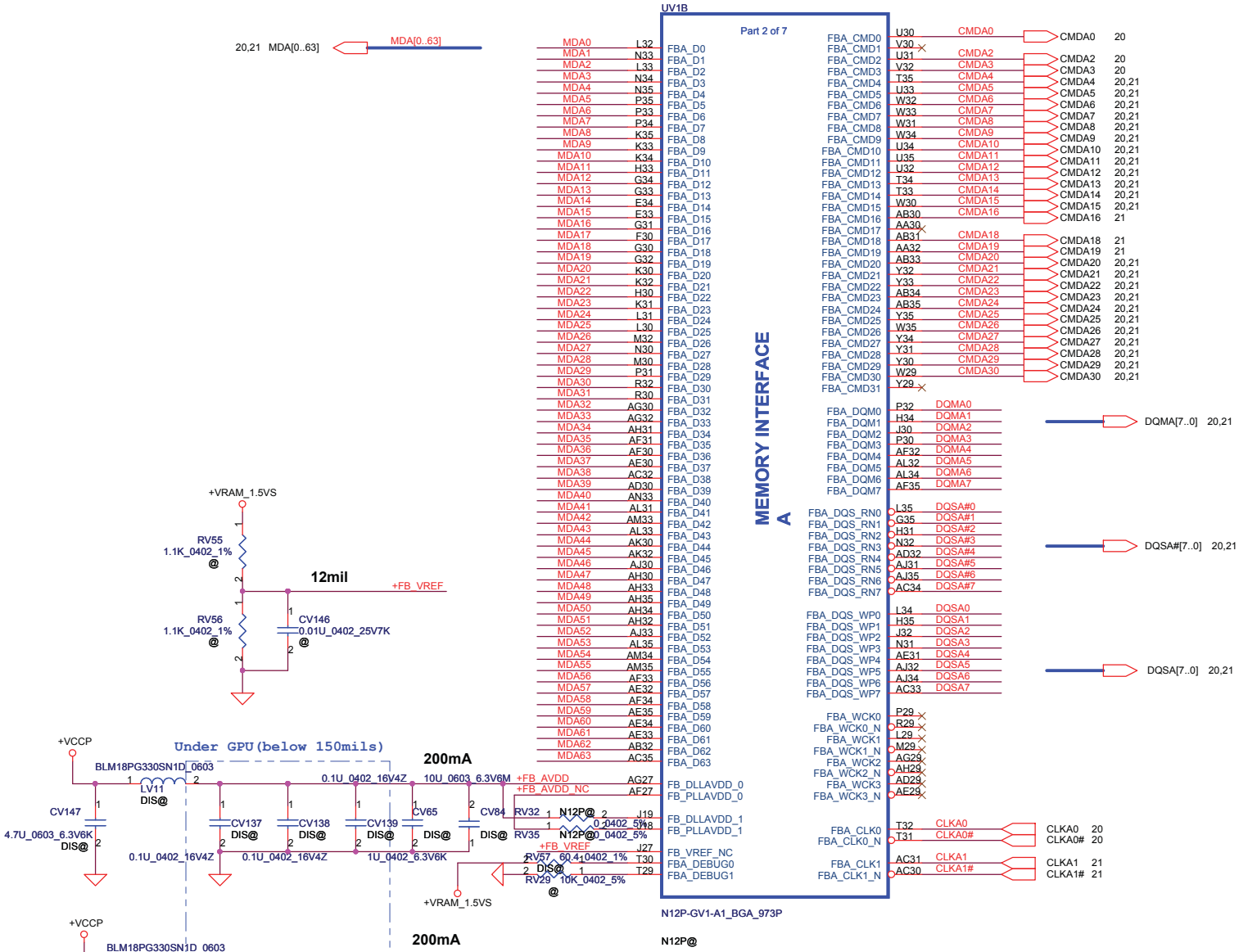
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: VGA(5/12)-GND

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Monday, October 25, 2010 | Sheet 17 of 58



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

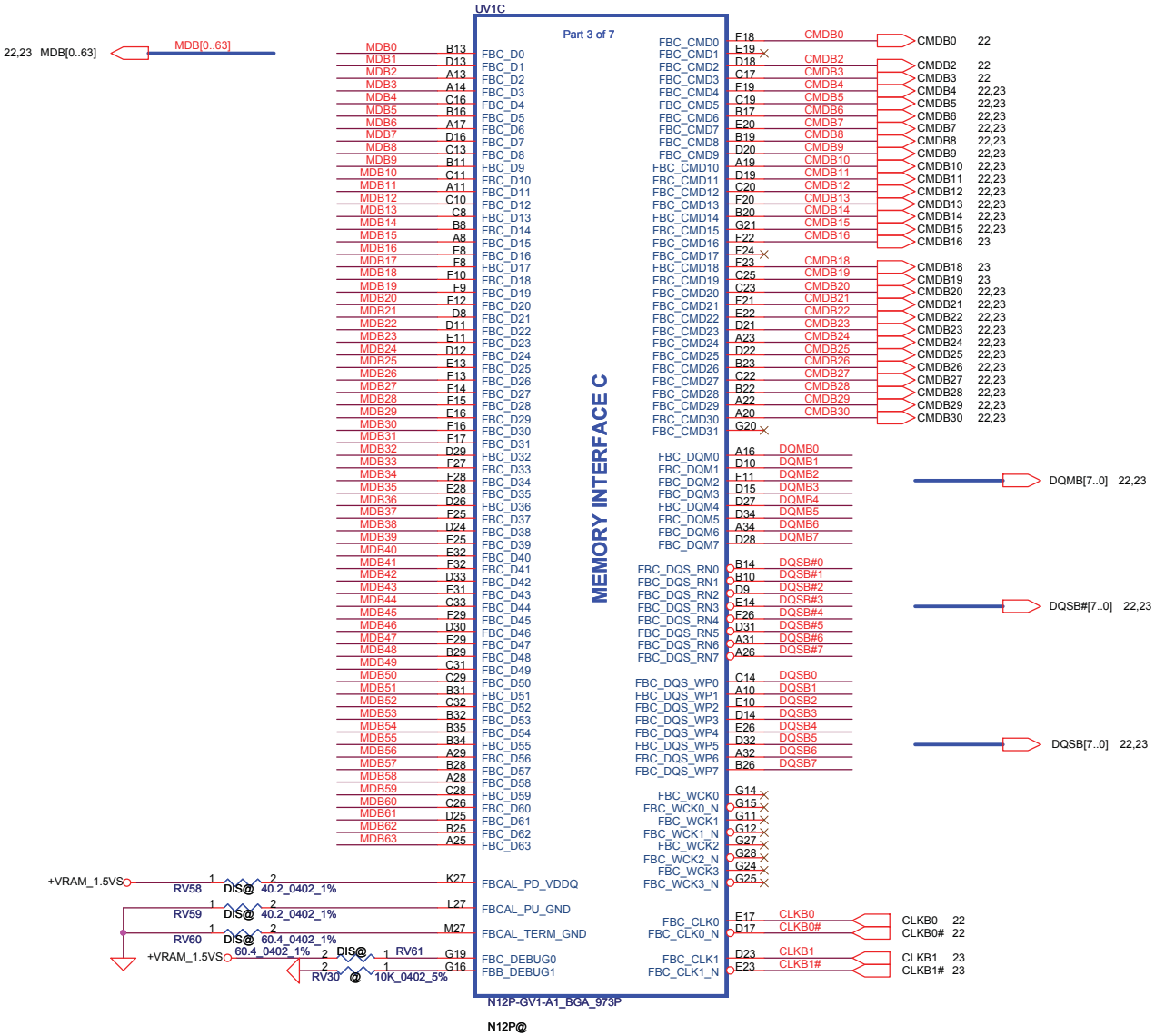
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: VGA(6/12)-MEM Interface A

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, November 02, 2010 | Sheet 18 of 58



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

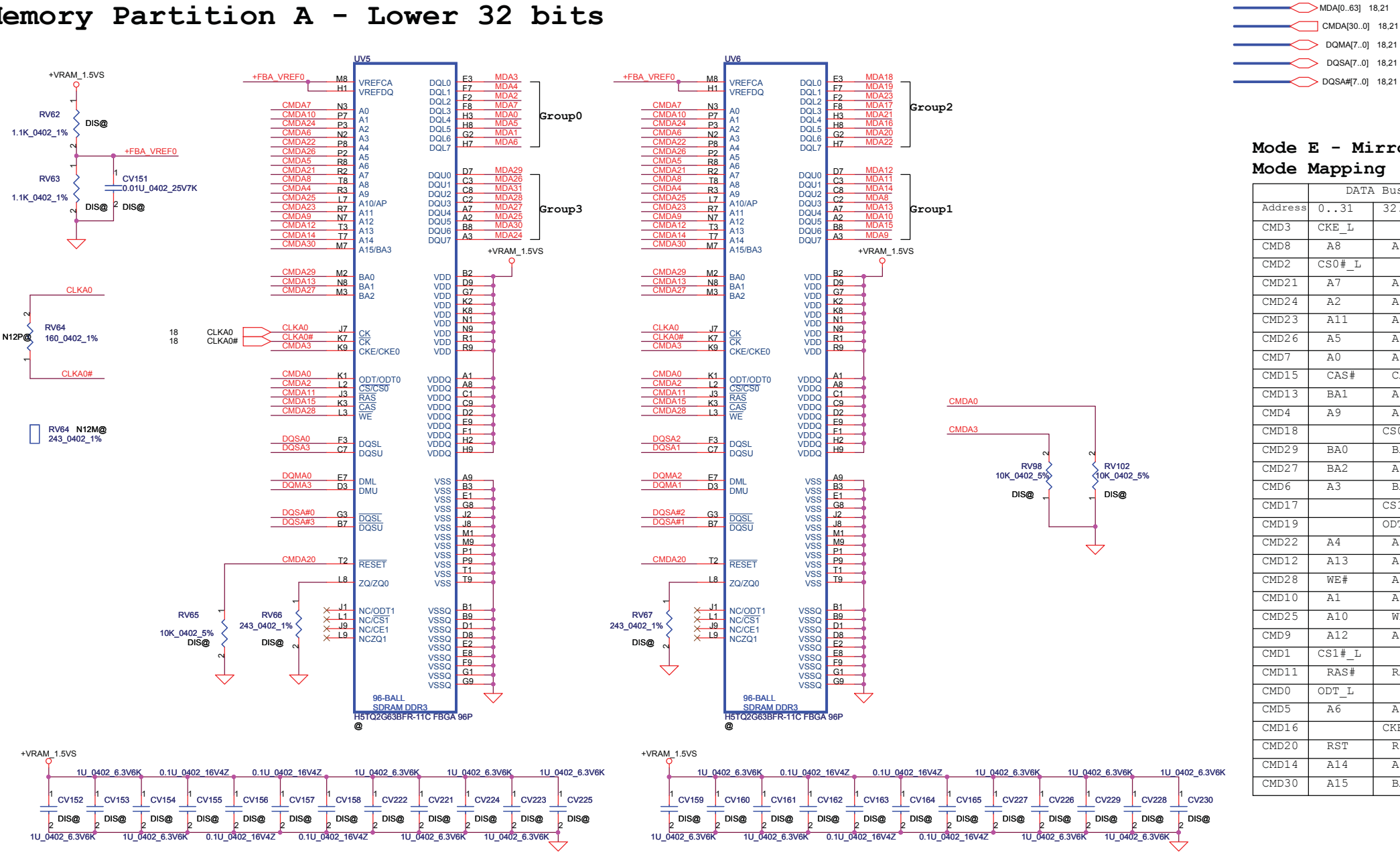
Compal Electronics, Inc.

Title: VGA(7/12)-MEM Interface C

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, November 02, 2010 | Sheet 19 of 58

Memory Partition A - Lower 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: VGA(8/12)-VRAM A Lower

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

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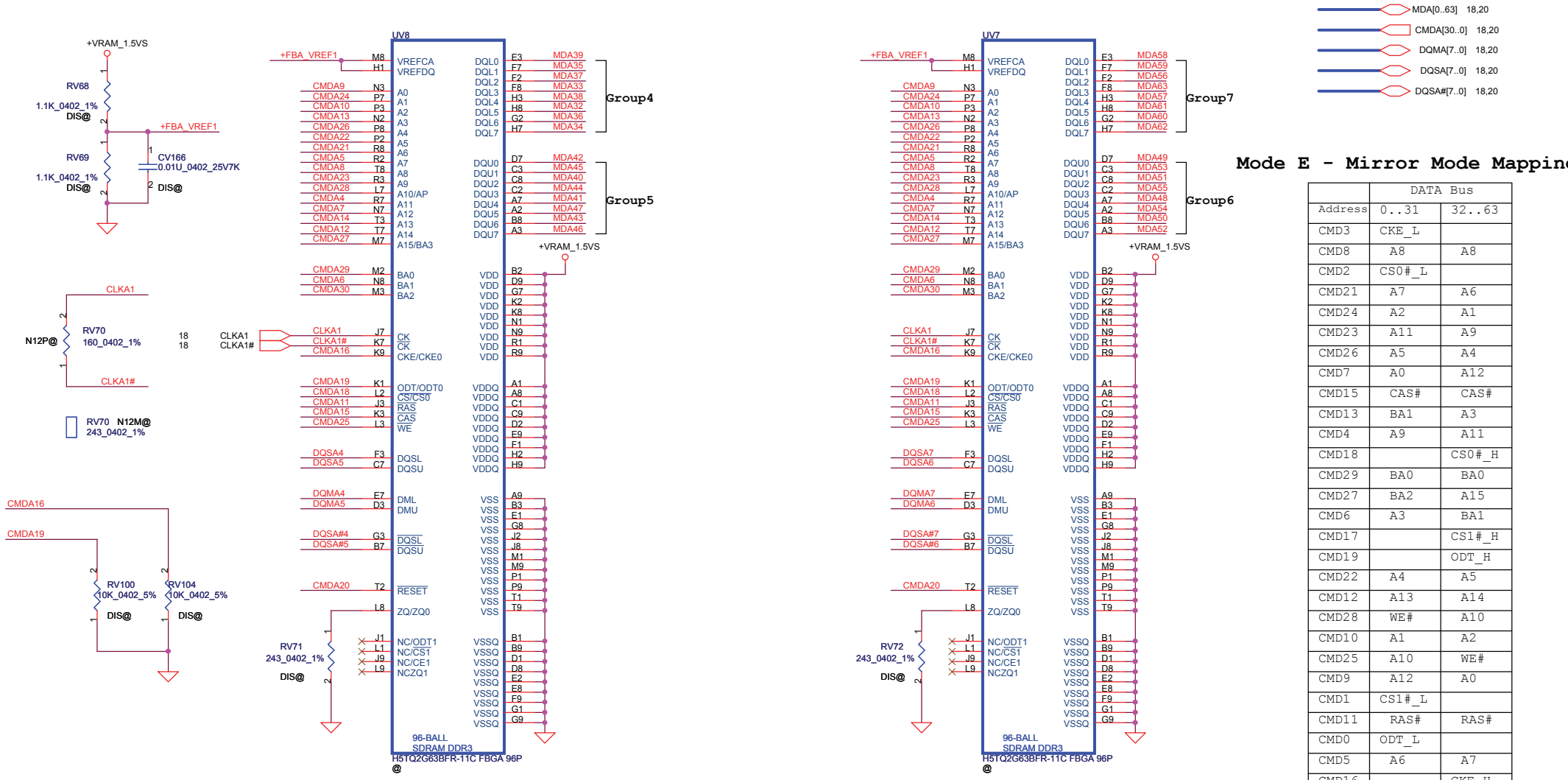
Memory Partition A - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

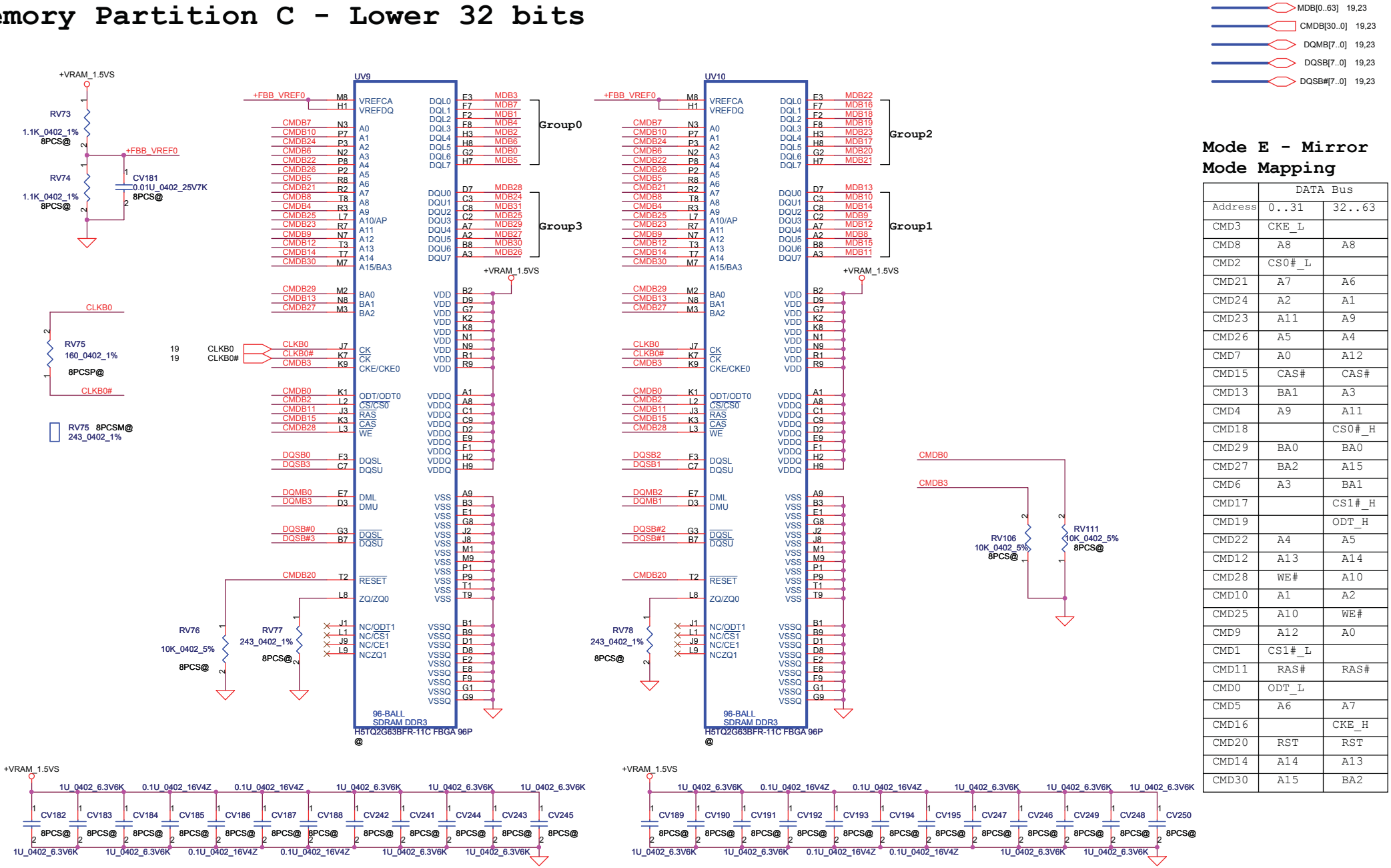
Compal Electronics, Inc.

Title: VGA(9/12)-VRAM A Upper

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, November 02, 2010 | Sheet 21 of 58

Memory Partition C - Lower 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

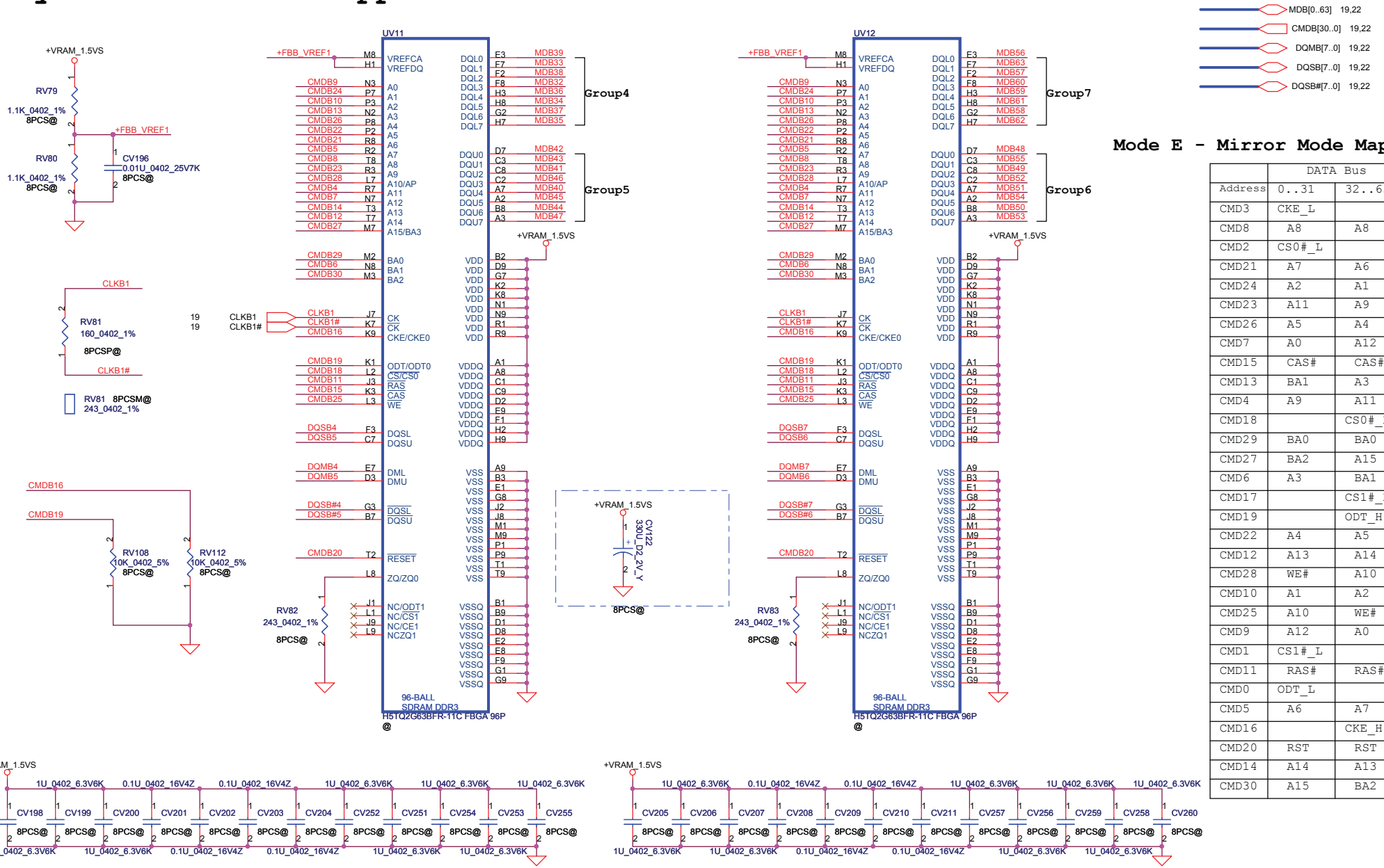
Compal Electronics, Inc.

Title: VGA(10/12)-VRAM C Lower

Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, November 02, 2010 | Sheet 22 of 58

Memory Partition C - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Compal Electronics, Inc.

Title: VGA(11/12)-VRAM C Upper

Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.3

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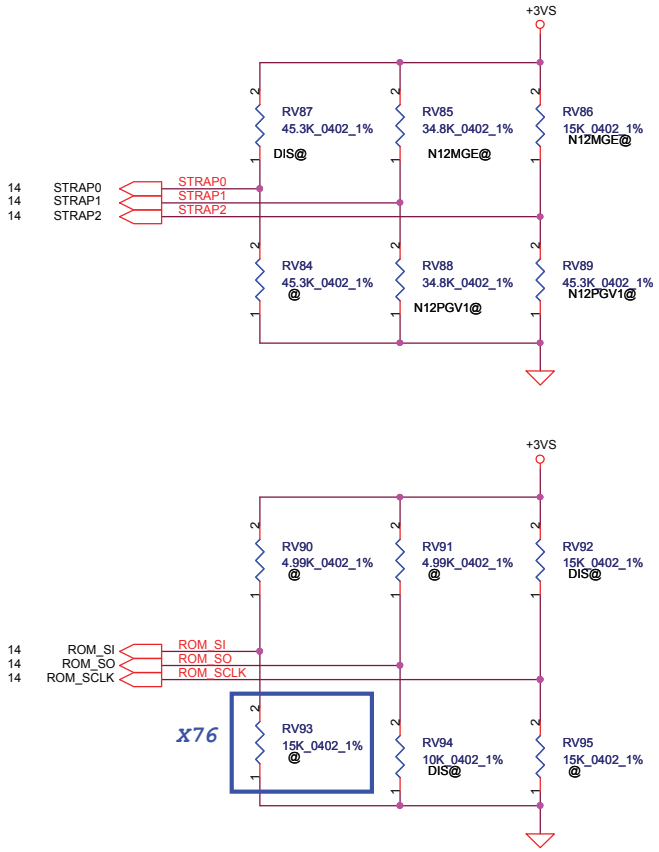


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	DeviceID	ROM_SCLK	STRAP2
N12M-GE		Pull up 15K	Pull up 15K
N12P-GV1		Pull up 15K	Pull down 45K

Hynix H5TQ2G63BFR-12C SA00003VS00	1G	0110	PD 34.8K SD034348280
Samsung K4W2G1646B-HC12 SA00003MQ40	1G	0111	PD 45.3K SD034453280

SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	256MB (Default)
1	Reserved

USER Straps

User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG

3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	3D Device
1	VGA Device (Default)

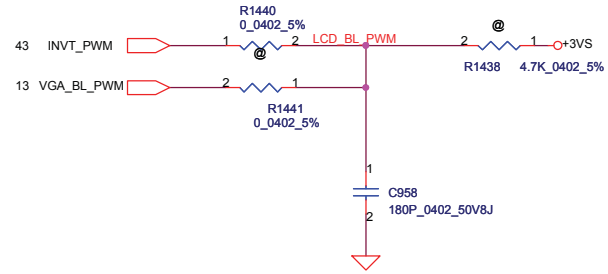
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

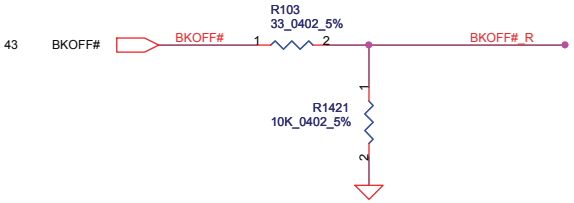
Compal Electronics, Inc.

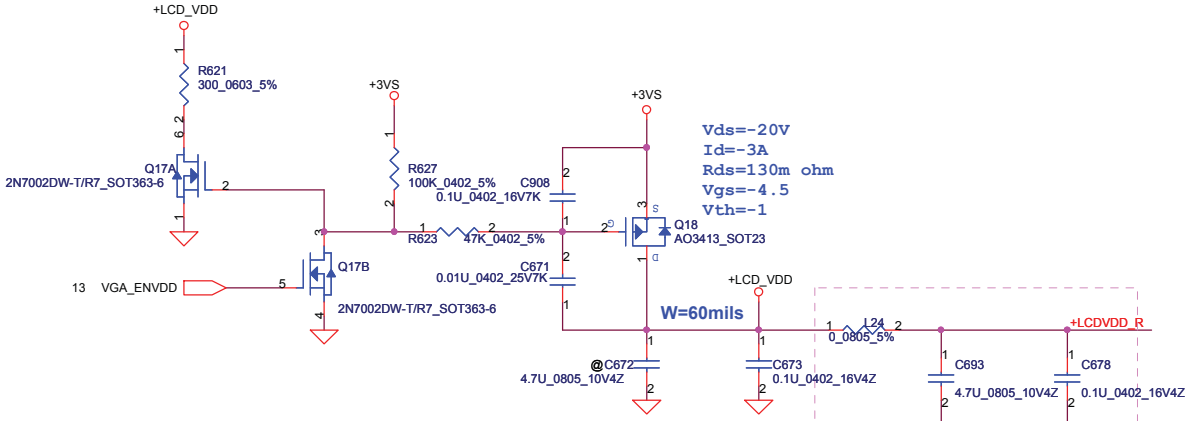
Title: VGA(12/12)-MISC

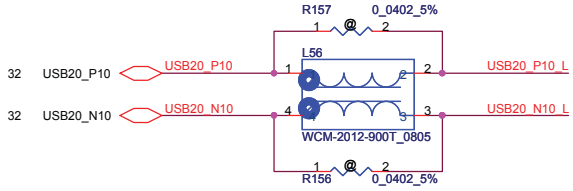
Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.3

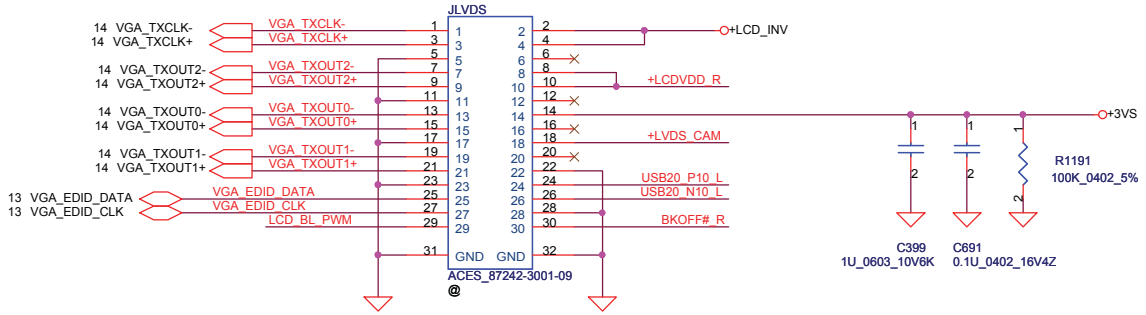
Date: Tuesday, November 02, 2010 | Sheet 24 of 58



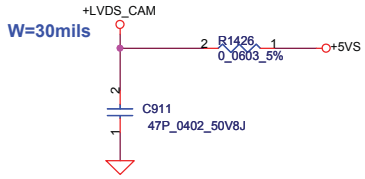


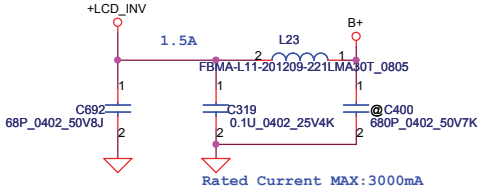






LCD/PANEL BD. Conn.





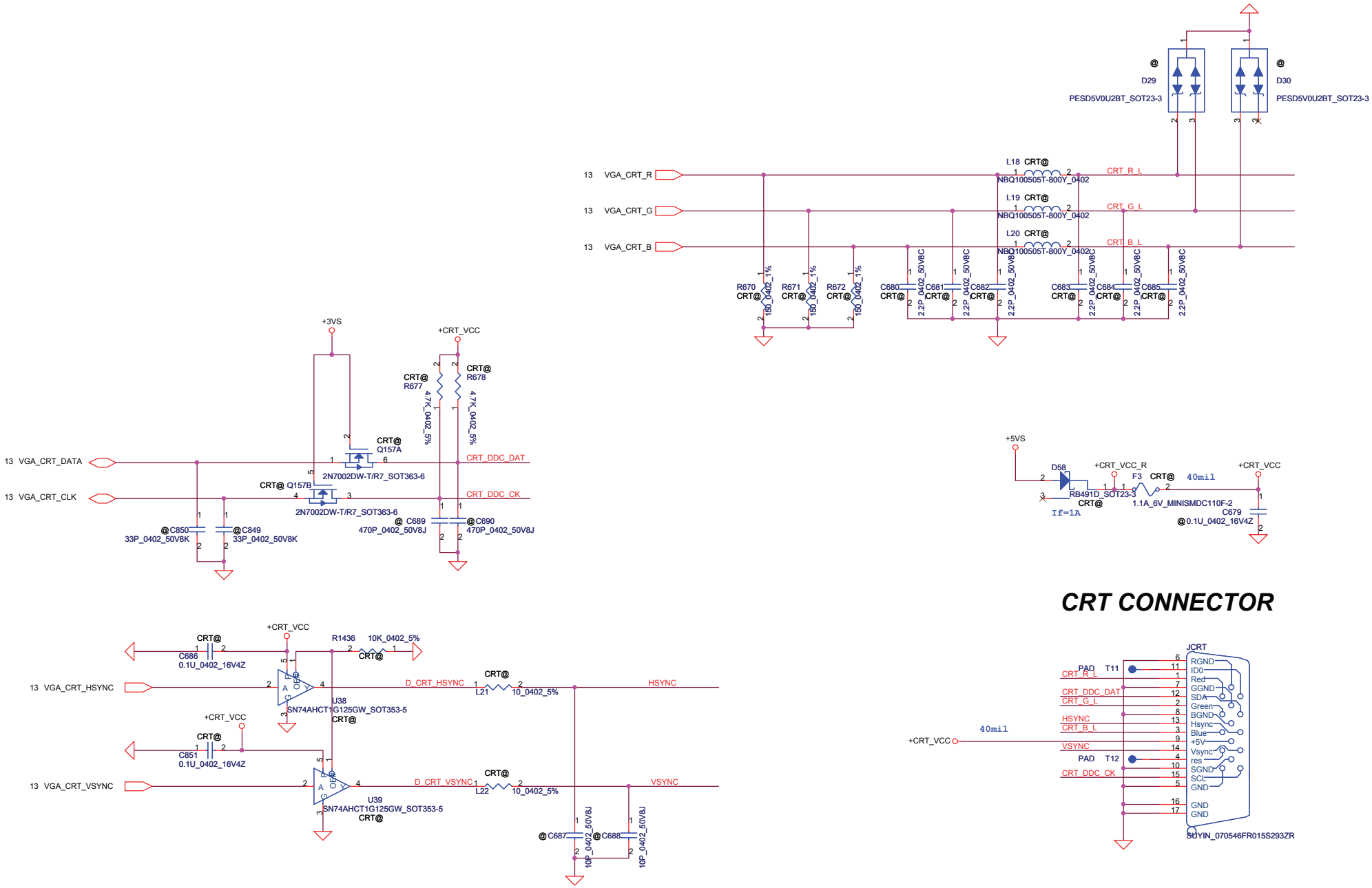
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: LVDS

Size	Document Number	Rev
	PBL01 LA6733P M/B	0.3

Date: Tuesday, November 02, 2010 Sheet 25 of 58



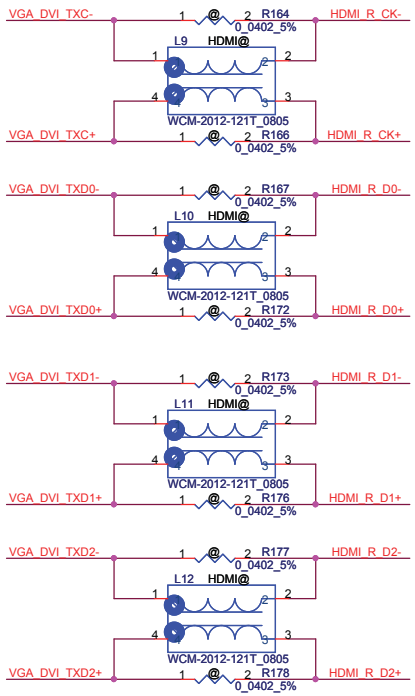
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

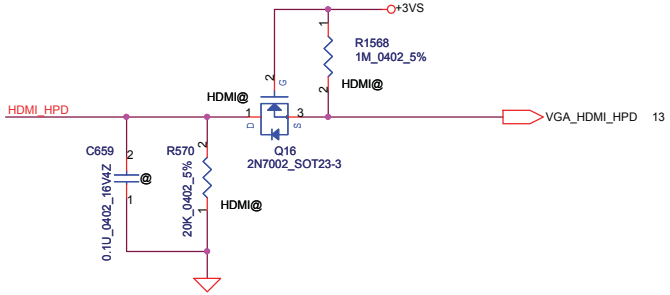
Compal Electronics, Inc.

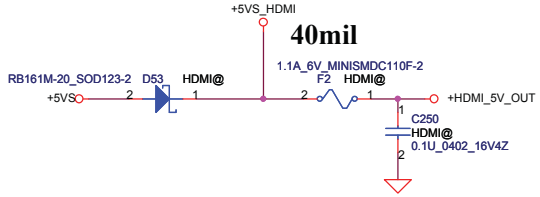
Title: CRT

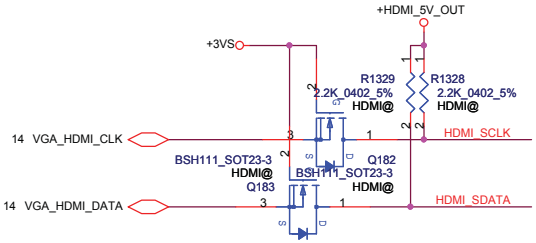
Size	Document Number	Rev
	PBL01 LA6733P M/B	0.3

Date: Tuesday, November 02, 2010 | Sheet 26 of 58

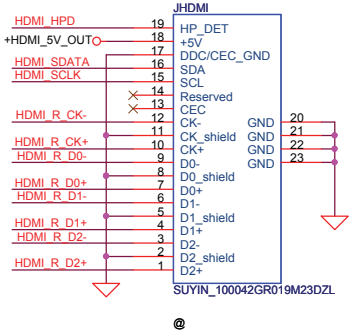


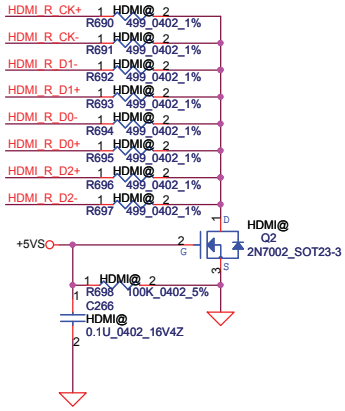






HDMI Connector





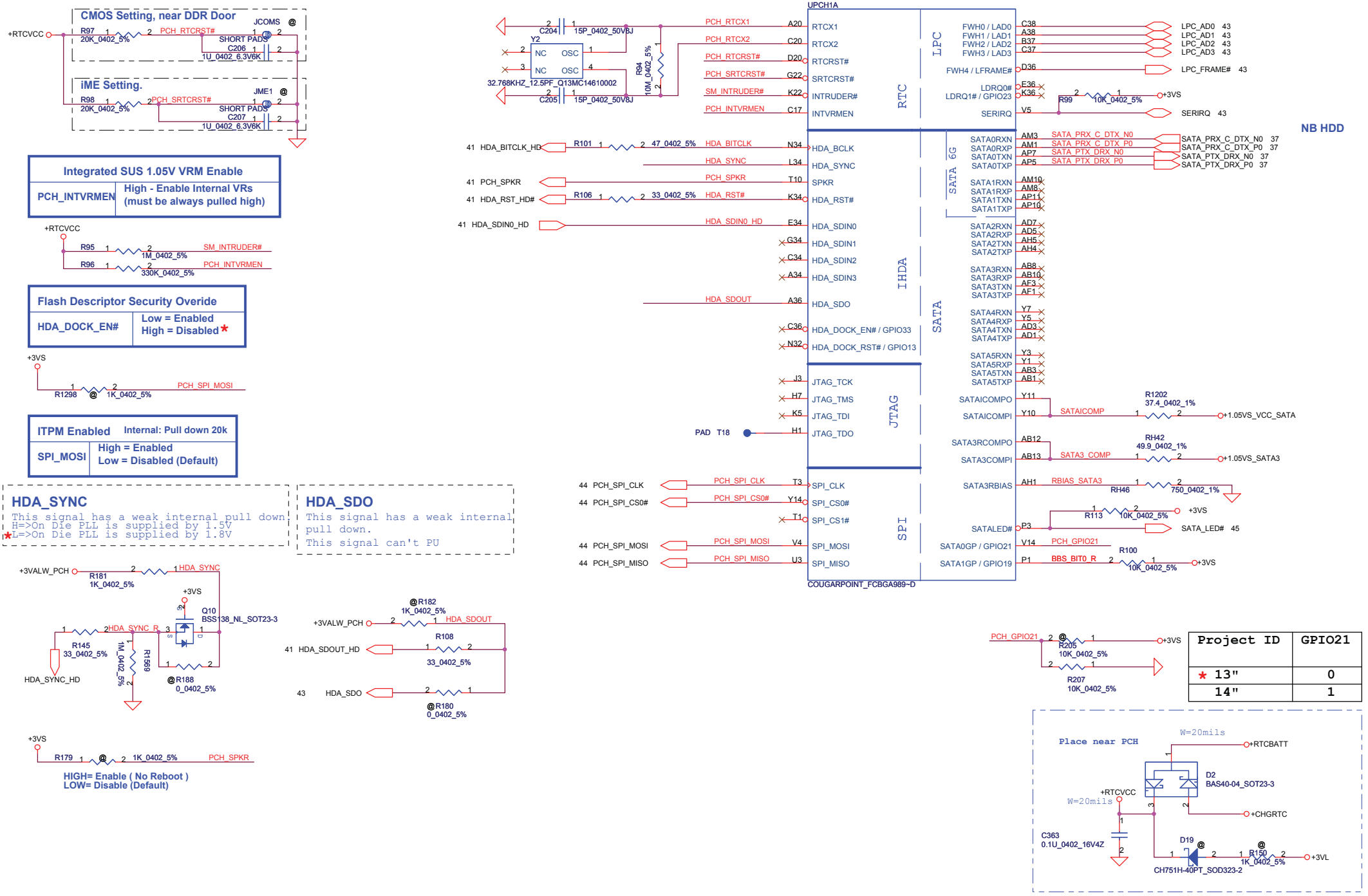
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: HDMI Connector

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, November 02, 2010 | Sheet 27 of 58

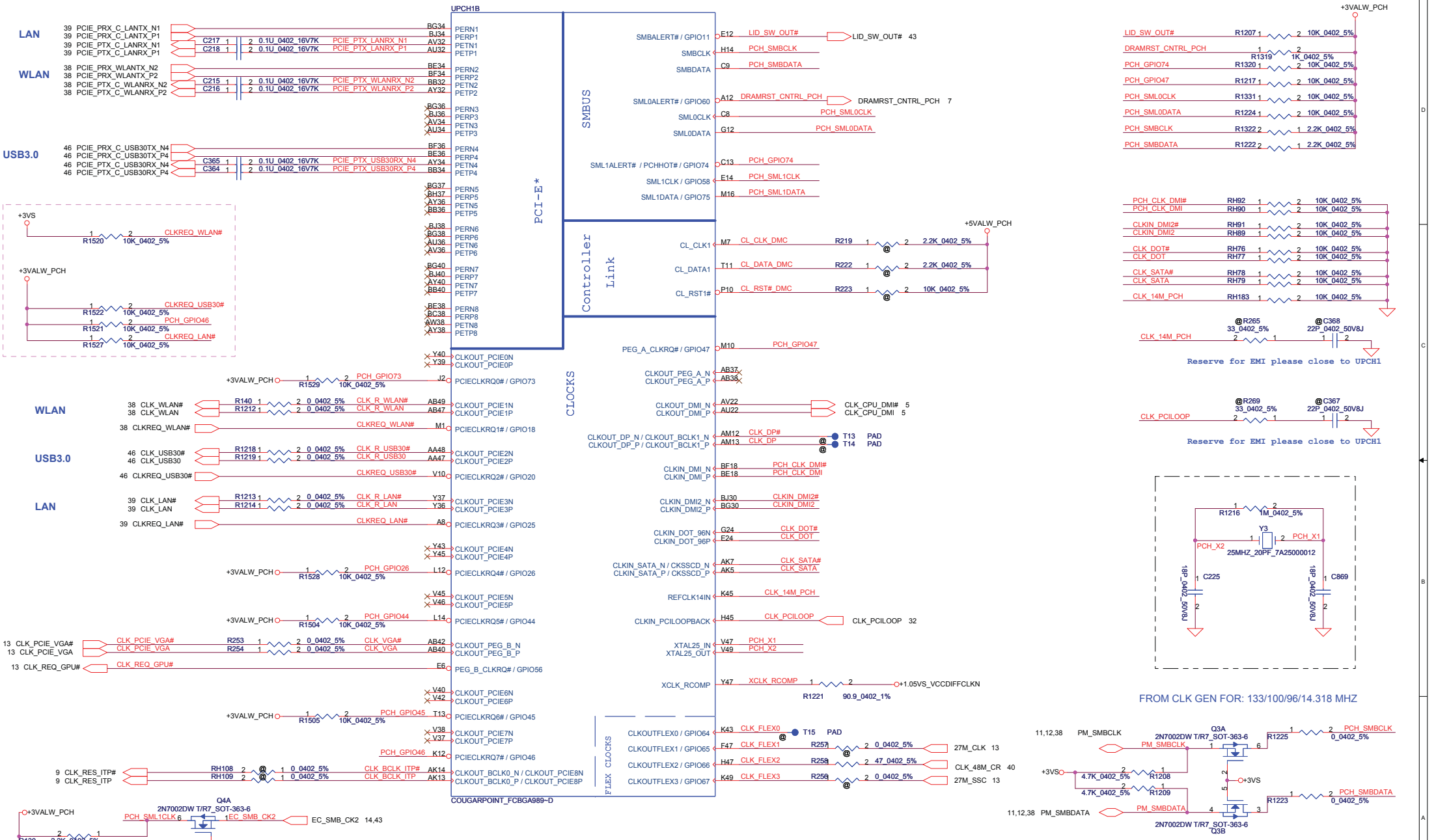


Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: Cougar Point(1/9)-HDA/SATA/XDP/RTC/SPI

Size	Document Number	Rev
Custom	PBL01 LA6733P M/B	0.3
Date: Tuesday, November 02, 2010	Sheet 28 of 58	



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

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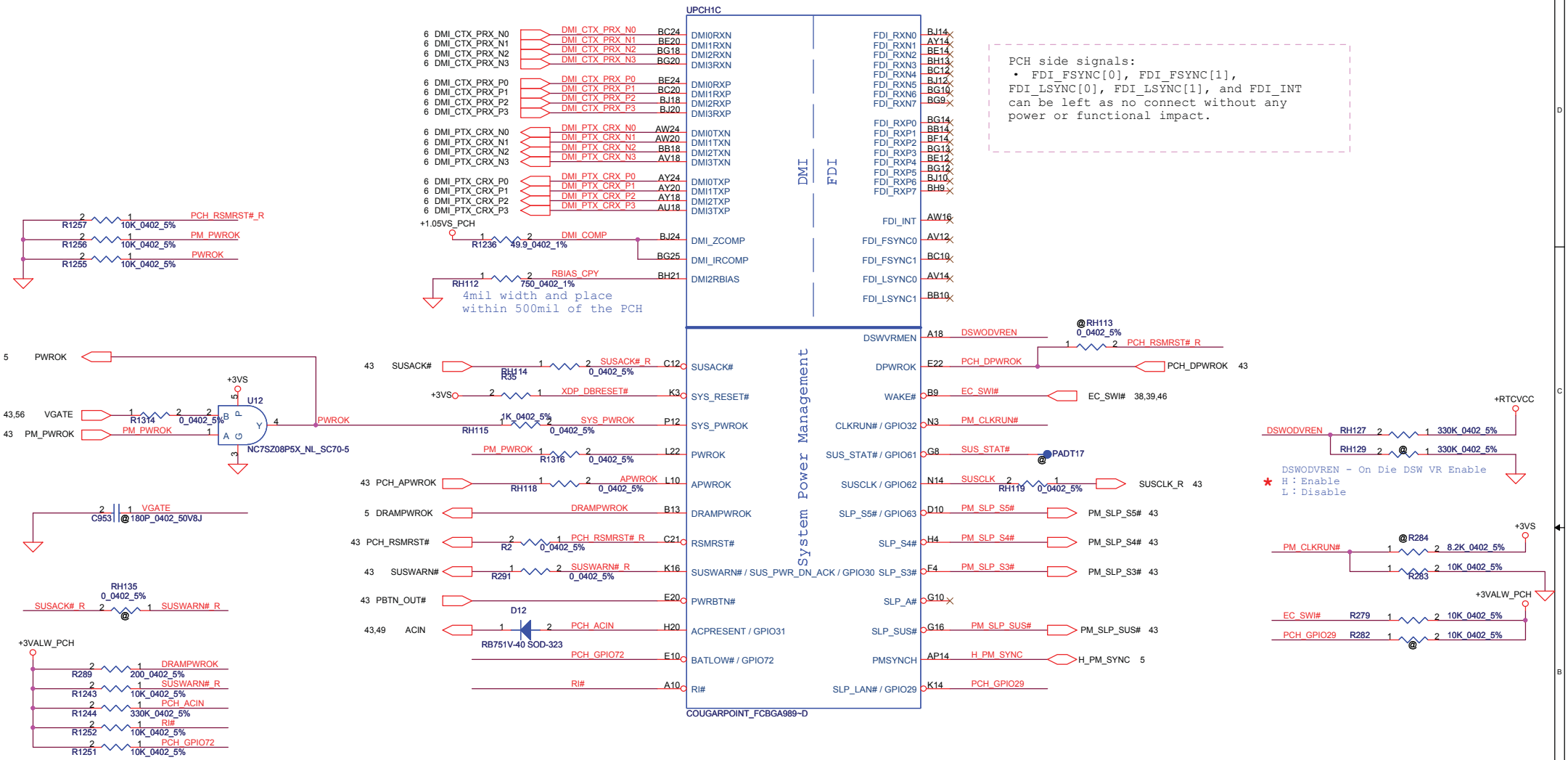
Compal Electronics, Inc.

Title: Cougar Point(2/9)-PCI-E/SMBUS/CLK

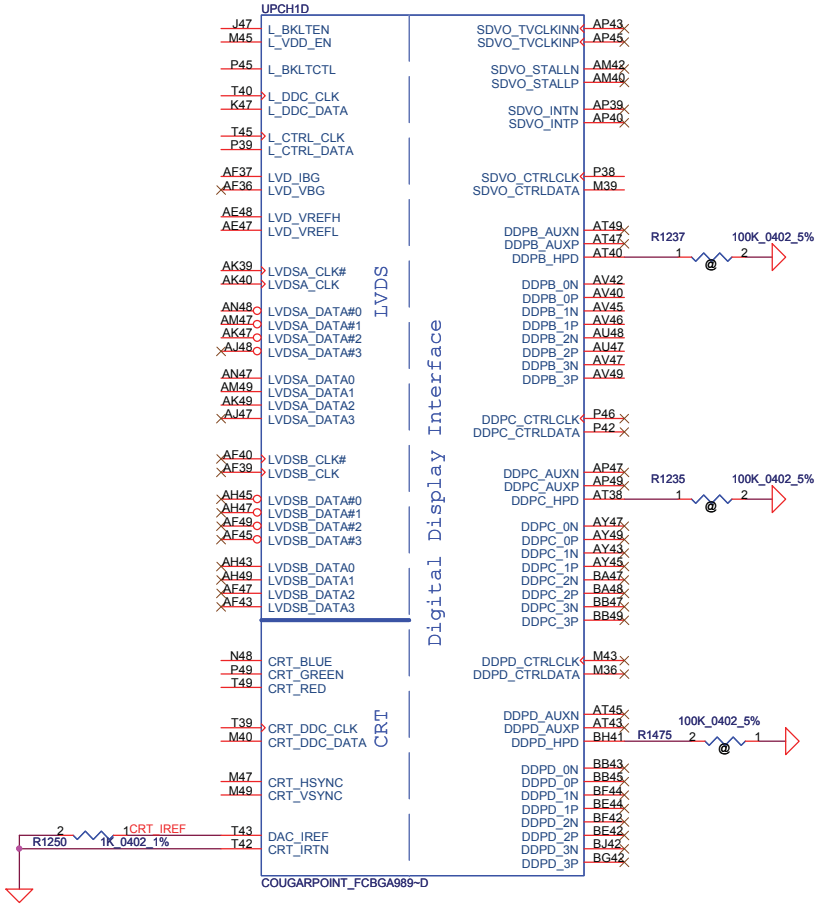
Size	Document Number	Rev
Custom	PBL01 LA6733P M/B	0.3

Date: Tuesday, November 02, 2010 Sheet 29 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.			
Title	Cougar Point(3/9)-DMI/FDI/PWM		
Size: Custom	Document Number: PBL01 LA6733P M/B		Rev: 0.3
Date: Tuesday, November 02, 2010	Sheet 30 of 58		



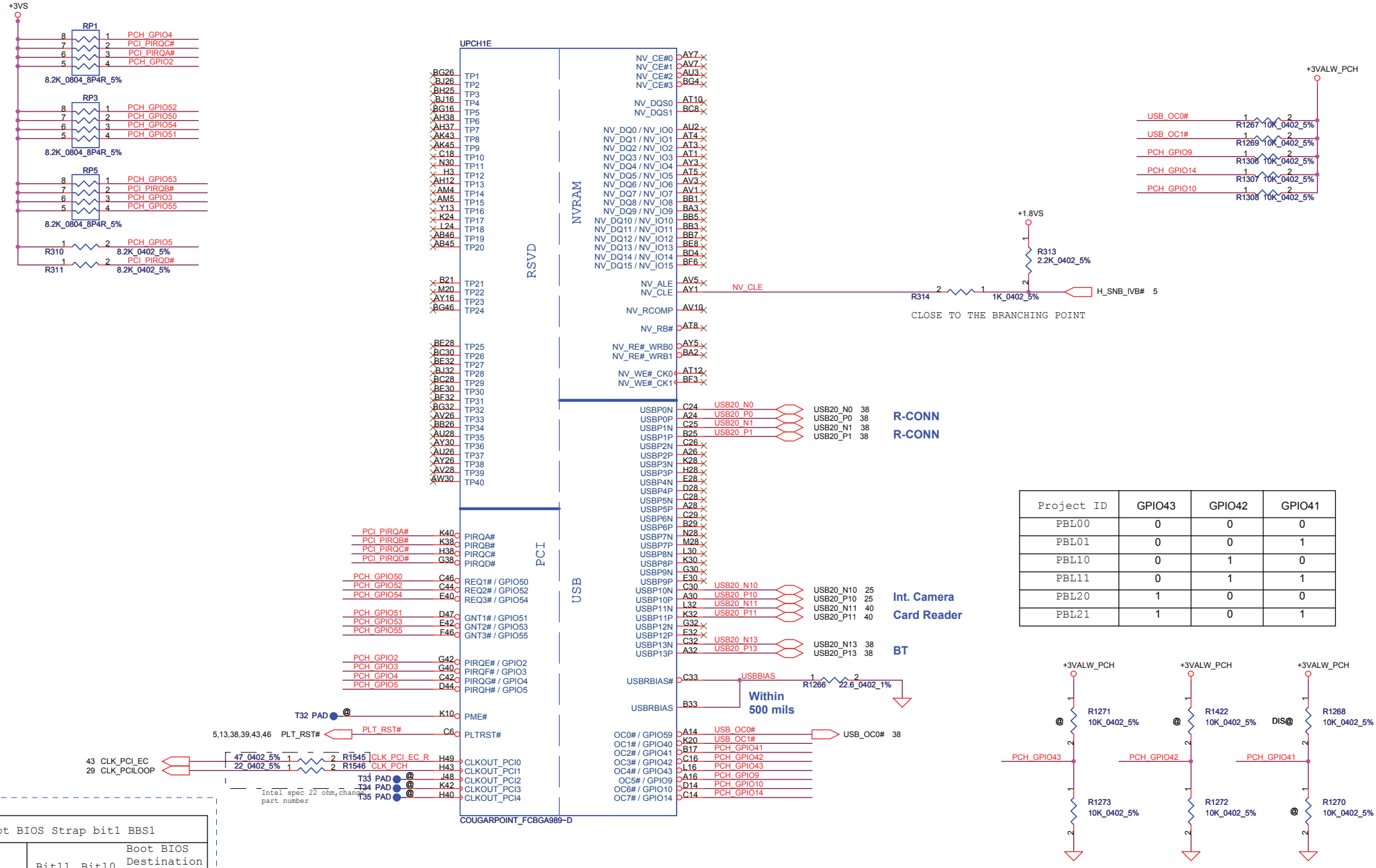
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: Cougar Point(4/9)-CRT/LVDS/HDMI/DP

Size	Document Number	Rev
Custom	PBL01 LA6733P M/B	0.3

Date: Monday, October 25, 2010 Sheet 31 of 58



Project ID	GPIO43	GPIO42	GPIO41
PBL00	0	0	0
PBL01	0	0	1
PBL10	0	1	0
PBL11	0	1	1
PBL20	1	0	0
PBL21	1	0	1

Boot BIOS Strap bit1 BBS1

	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC

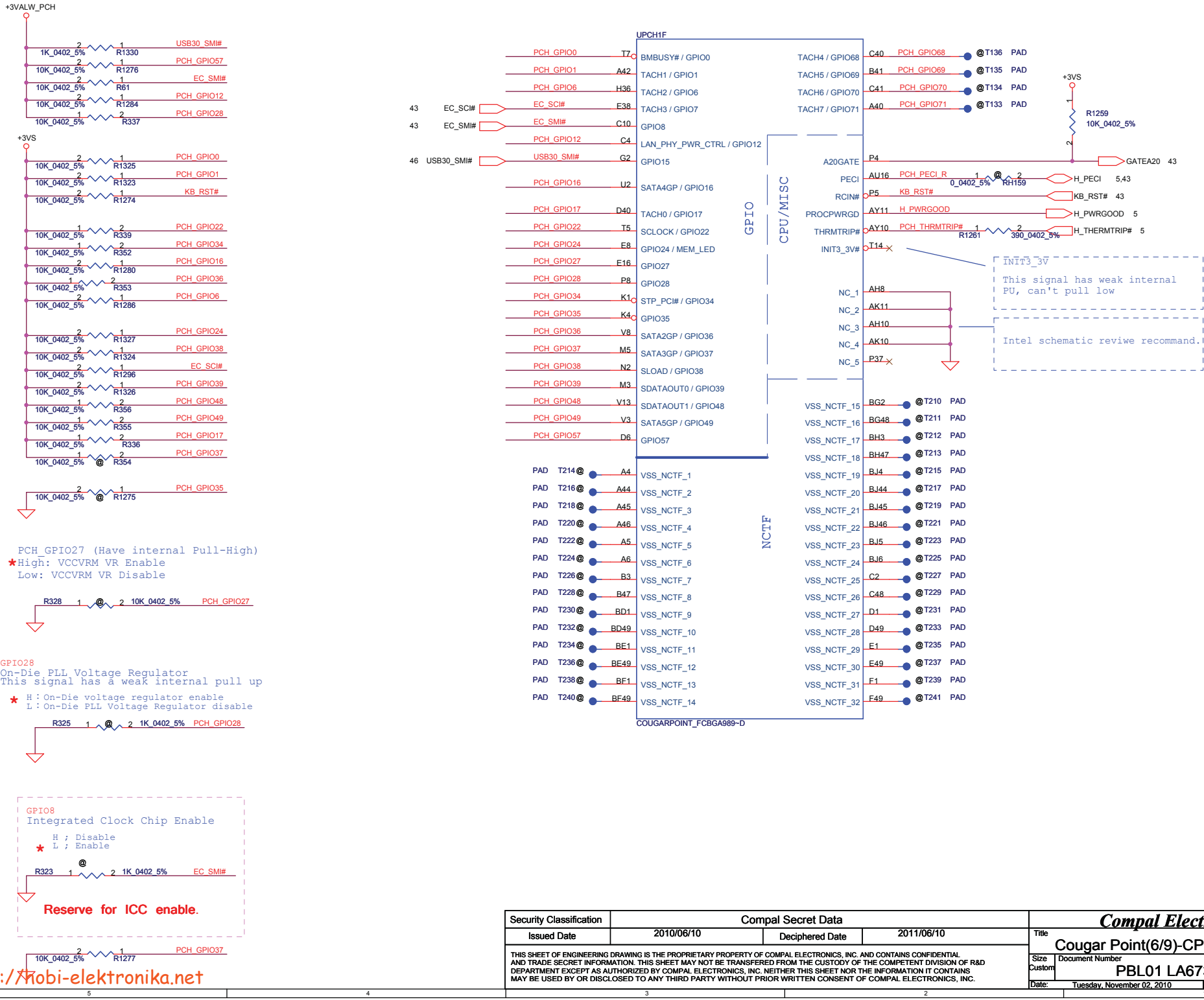
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: Cougar Point(5/9)-USB/PCI/NAND/STRAP

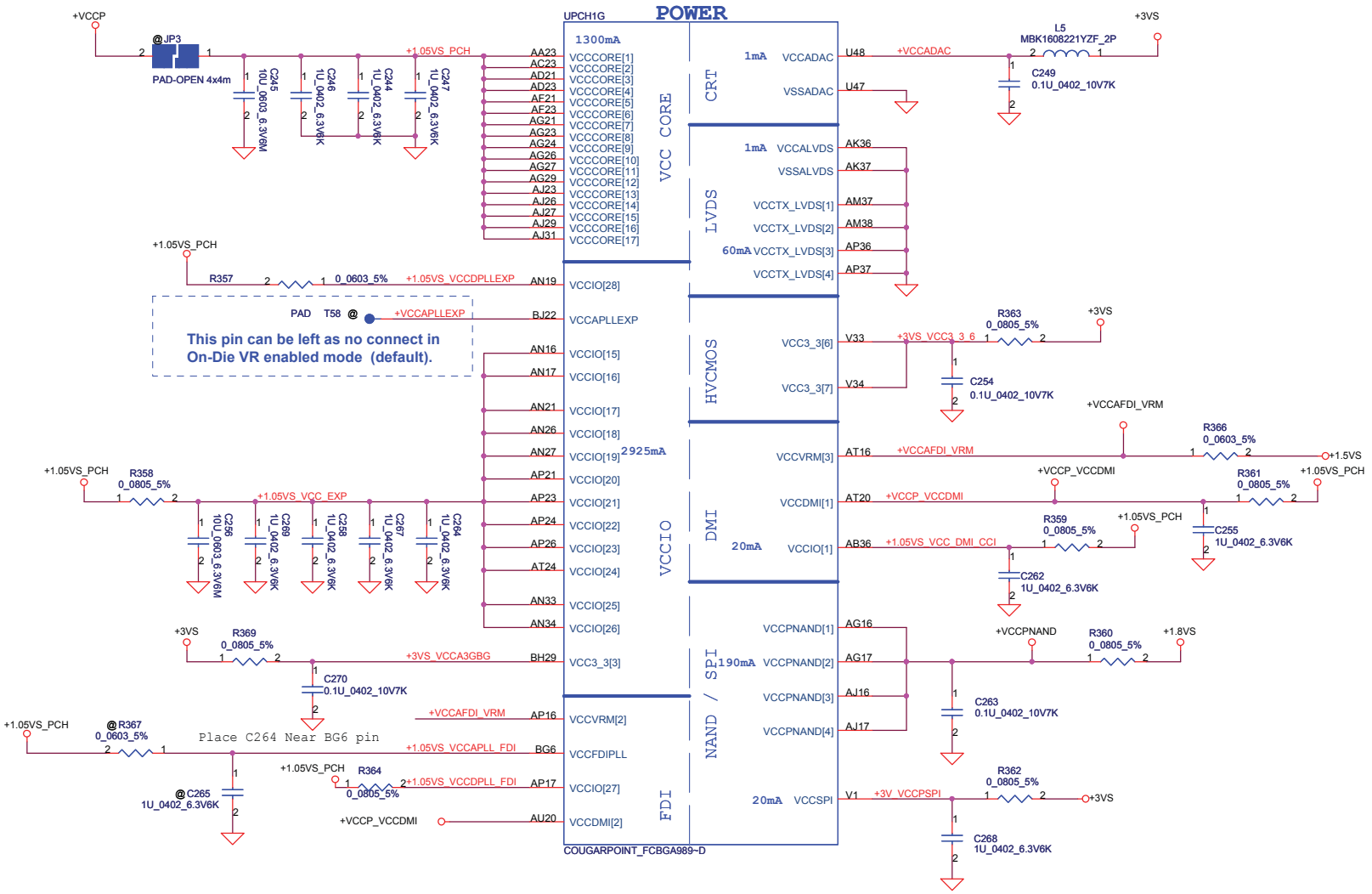
Size	Document Number	Rev
Custom	PBL01 LA6733P M/B	0.3

Date: Tuesday, November 02, 2010 Sheet 32 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.		
Title	Cougar Point(6/9)-CPU/GPIO/MISC	
Size: Custom	Document Number: PBL01 LA6733P M/B	Rev: 0.3
Date: Tuesday, November 02, 2010	Sheet 33 of 58	



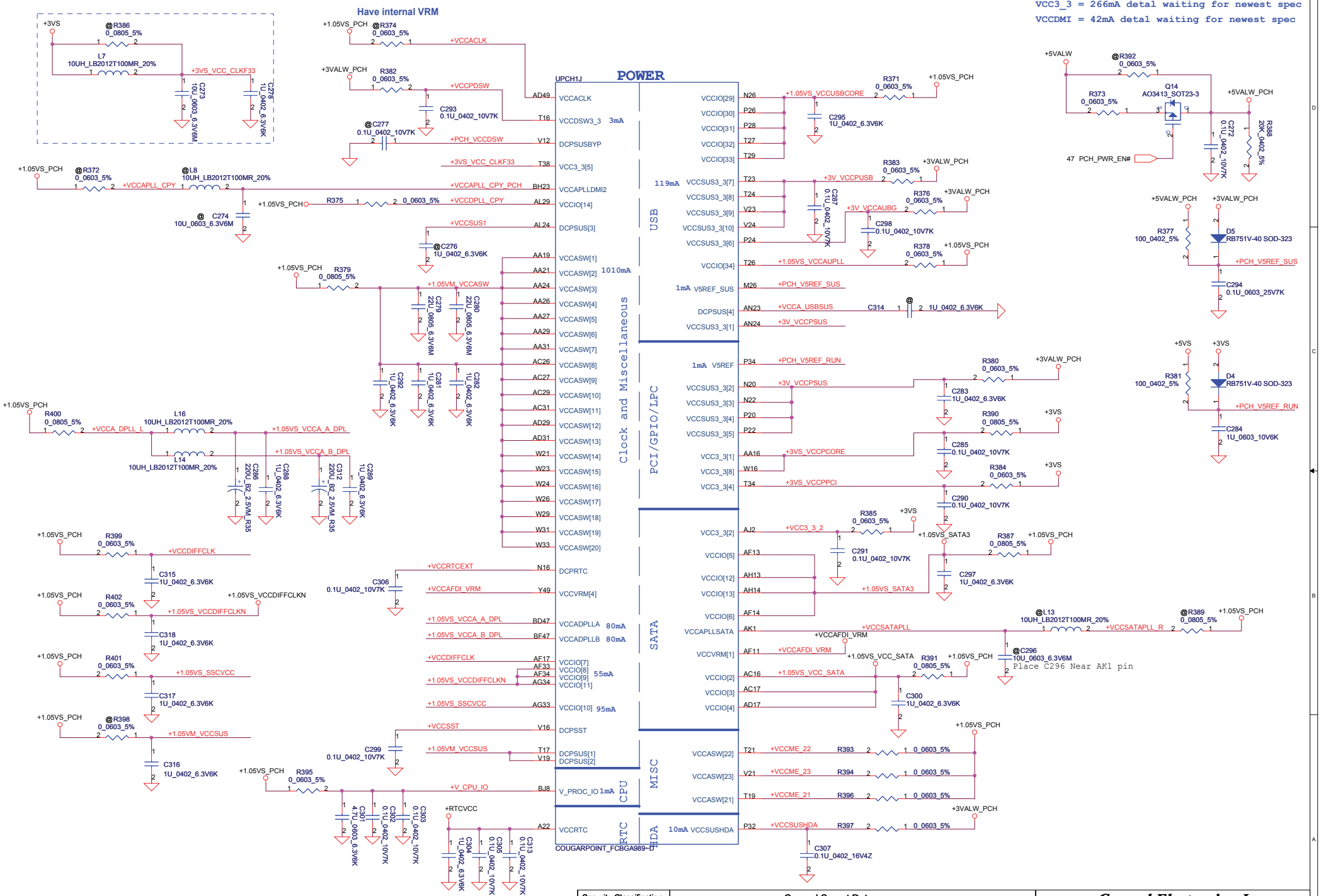
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Compal Electronics, Inc.

Title: Cougar Point(7/9)-PWR1

Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Friday, October 29, 2010 | Sheet 34 of 58



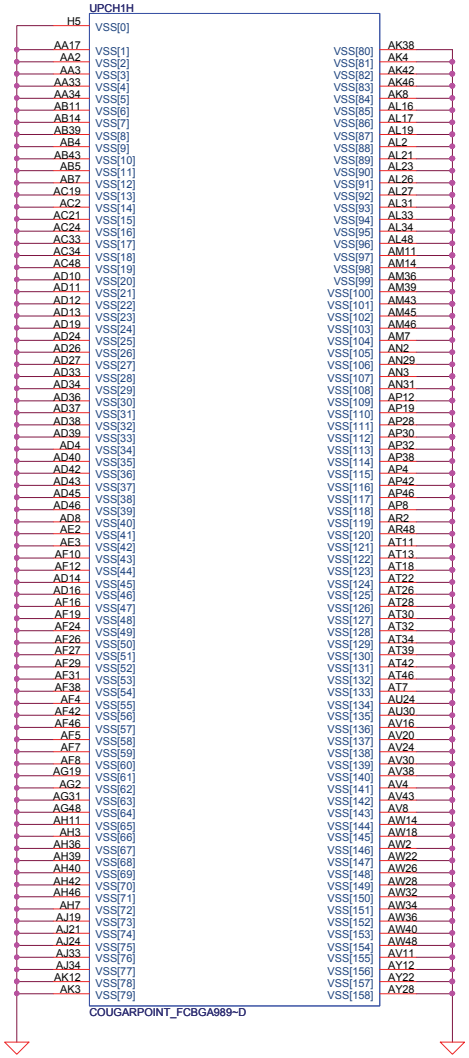
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

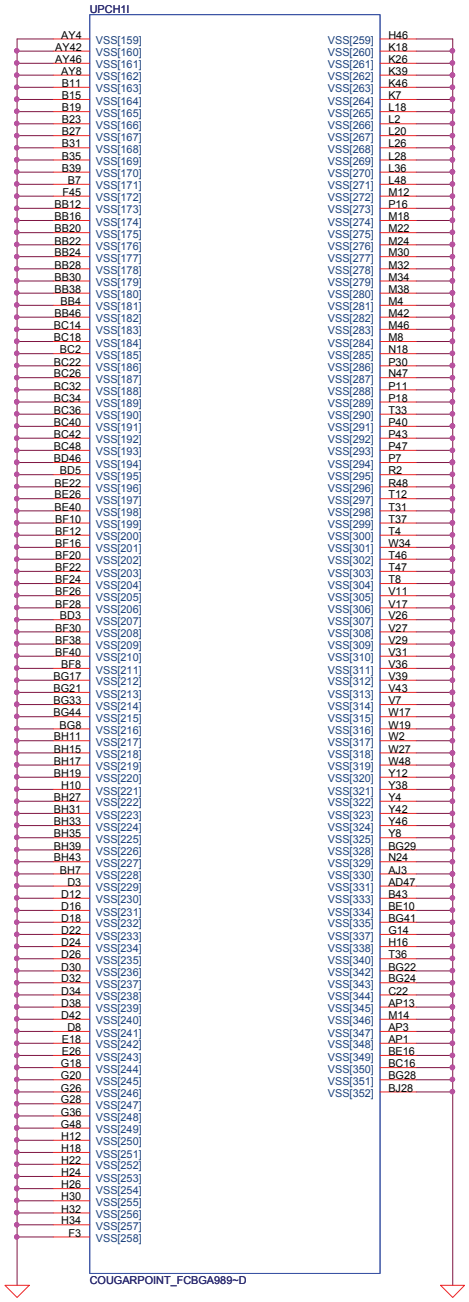
Compal Electronics, Inc.

Title: Cougar Point(8/9)-PWR2

Size	Document Number	Rev
Custom	PBL01 LA6733P M/B	0.3

Date: Tuesday, November 02, 2010 | Sheet 35 of 58





Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

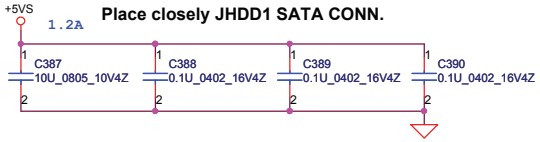
Title: Cougar Point(9/9)-GND

Size	Document Number	Rev
Custom	PBL01 LA6733P M/B	0.3

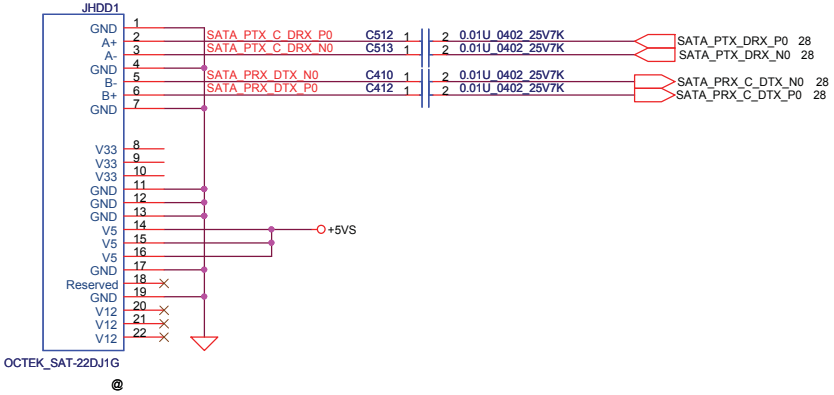
Date: Monday, October 25, 2010 | Sheet 36 of 58

SATA HDD1 Conn.

Place closely JHDD1 SATA CONN.



13.3" HDD



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

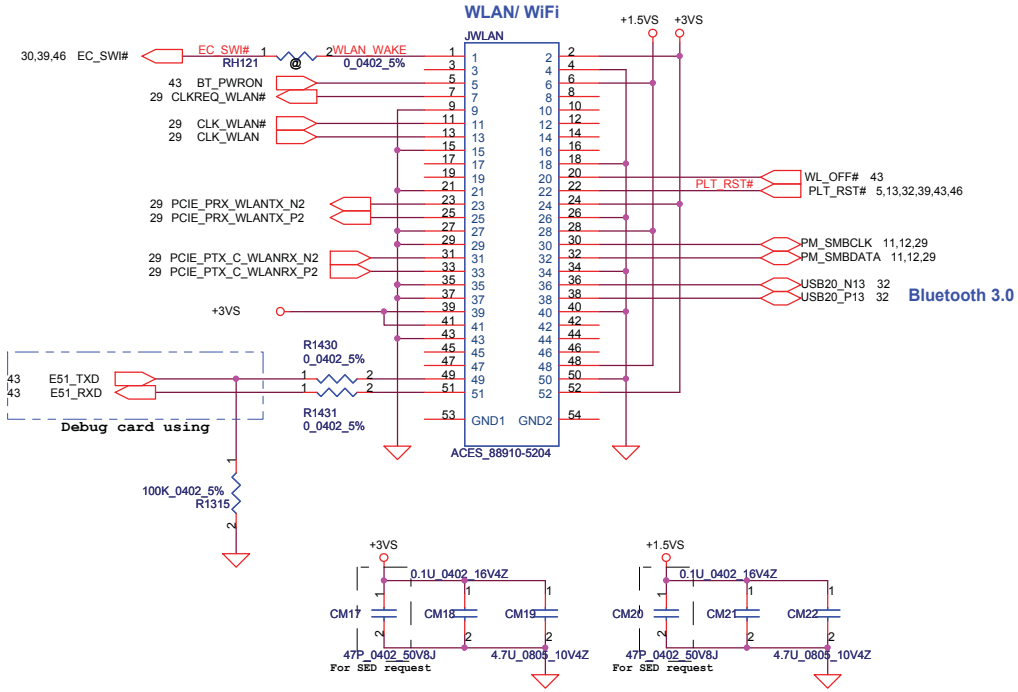
Compal Electronics, Inc.

Title: SATA-HDD

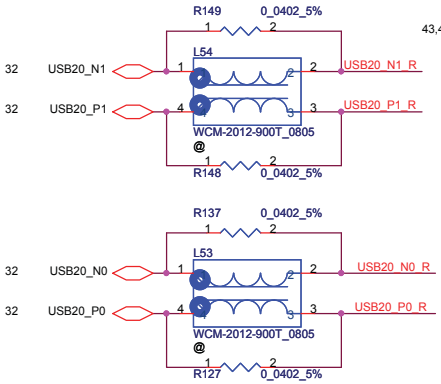
Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

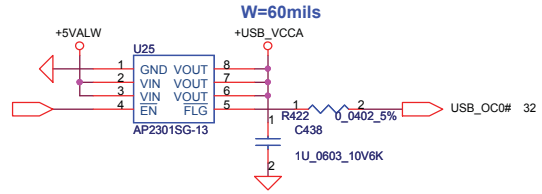
Date: Tuesday, November 02, 2010 | Sheet 37 of 58

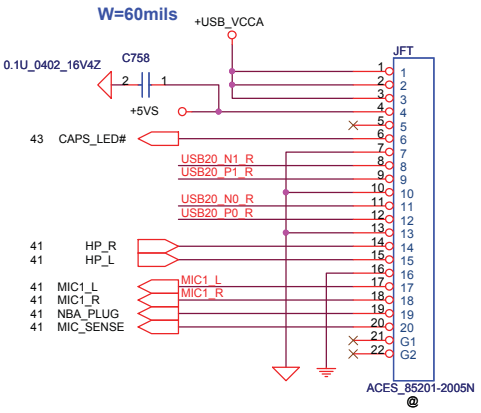
Slot 1 Half PCIe Mini Card-WLAN & BT3.0



Function Board







HeadPhone/LINE Out JACK

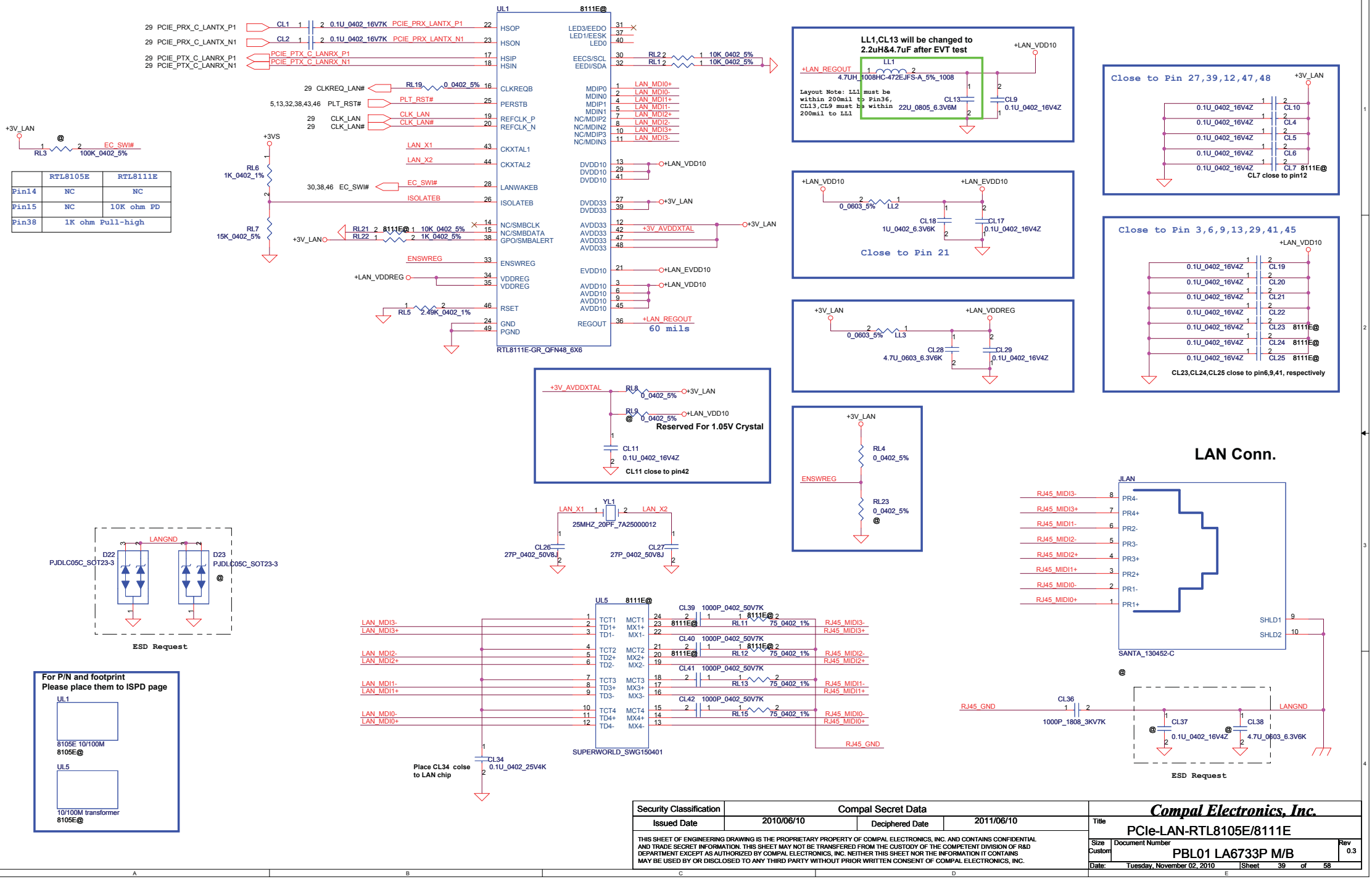
Ext.MIC/LINE IN JACK

Compal Electronics, Inc.

Title: WLAN/USB

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, November 02, 2010 | Sheet 38 of 58



	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

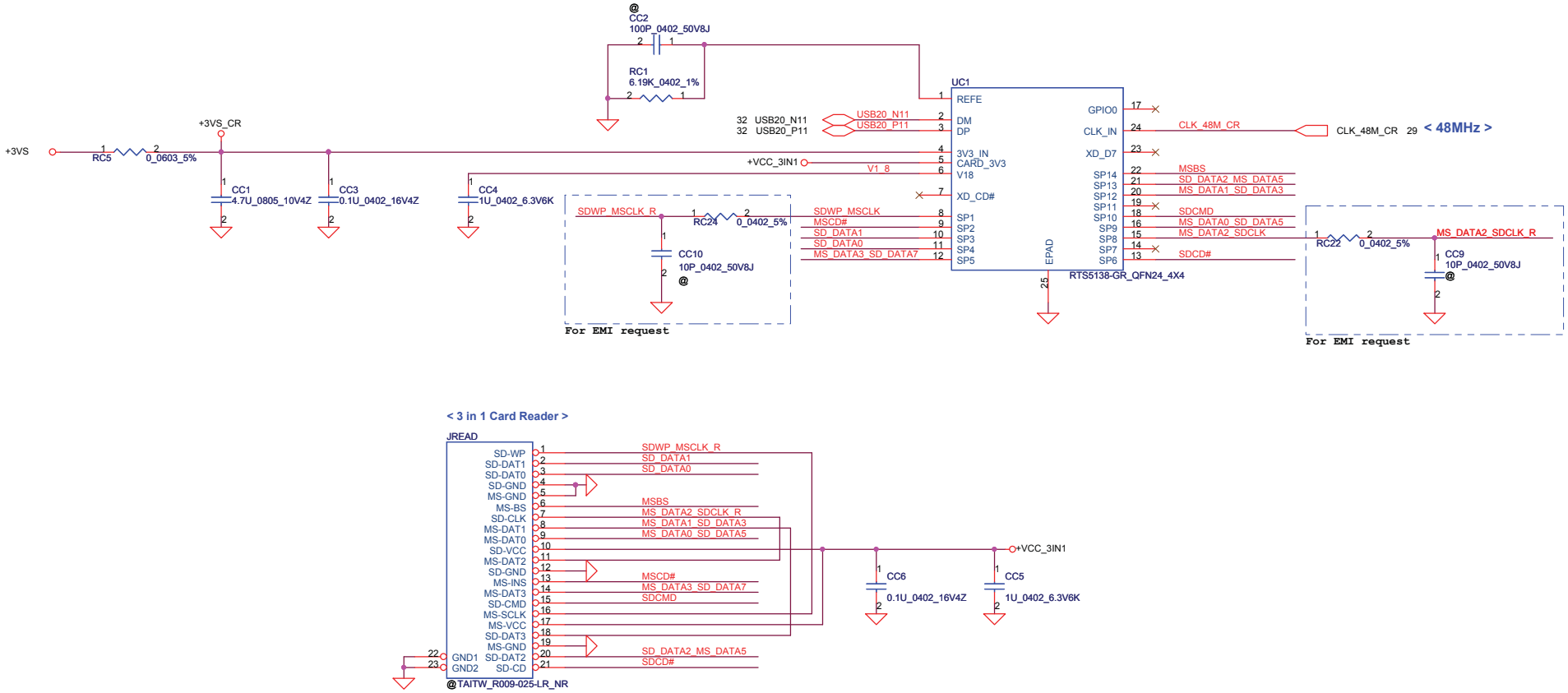
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: PCIe-LAN-RTL8105E/8111E

Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, November 02, 2010 | Sheet 39 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: USB-Card Reader-RTS5138

Size	Document Number	Rev
	PBL01 LA6733P M/B	0.3

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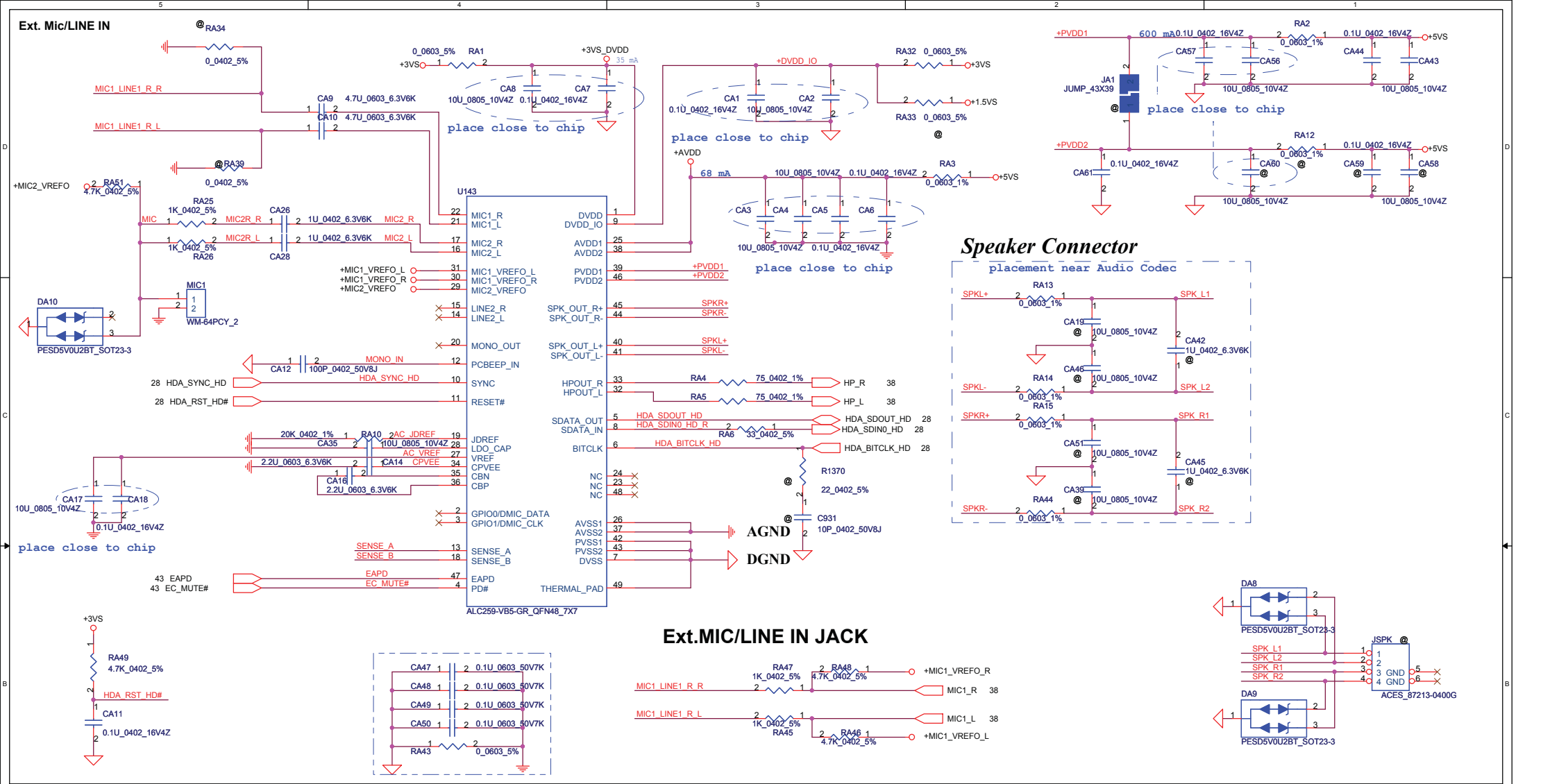
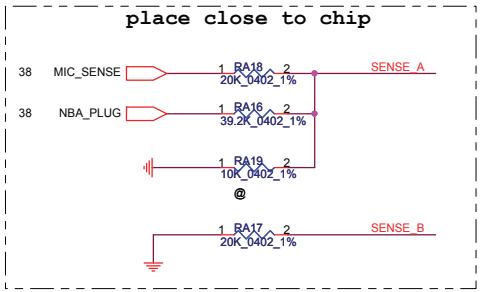
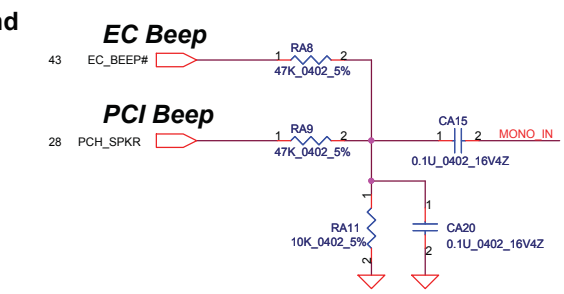


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	





Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.			
Title	HD CODEC ALC259		
Size	Document Number	PBL01 LA6733P M/B	Rev 0.3
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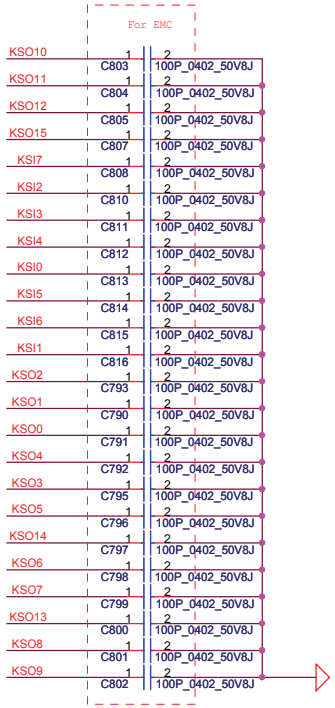
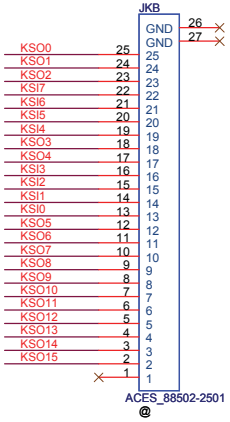
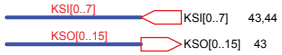
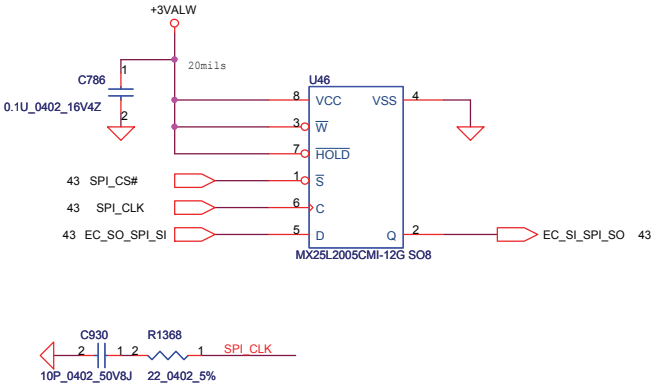
KEYBOARD CONN.



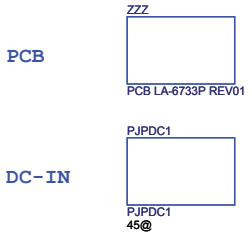




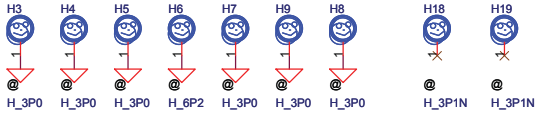
SPI Flash (1MByte*1)



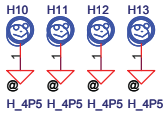
ISPD



Screw Hole

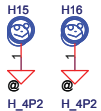


CPU

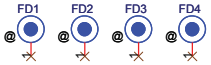


JWLAN

VGA



PCB Fedical Mark PAD



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: KB/PAD/ISPD/LID/ECROM

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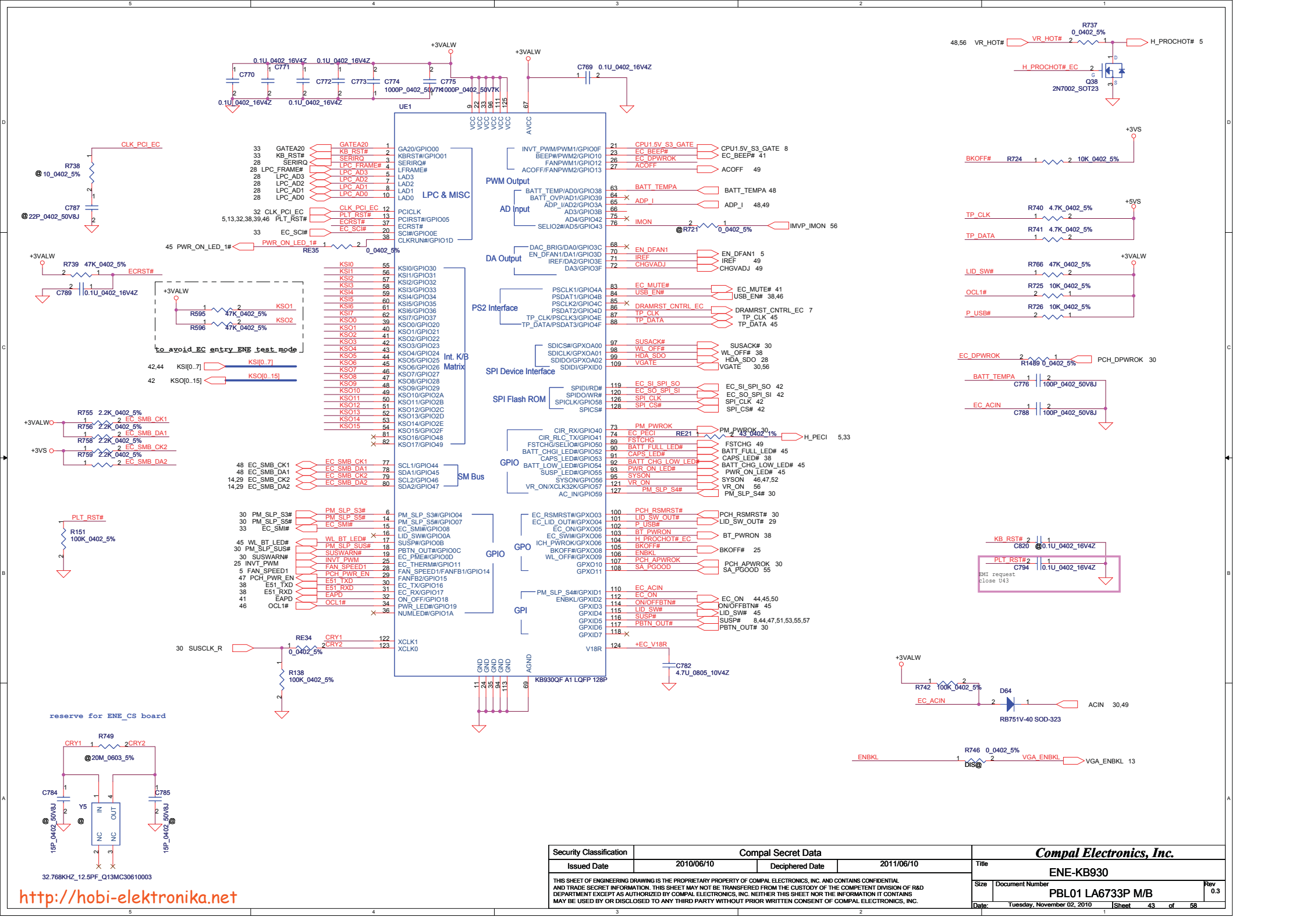

Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title	ENE-KB930	
Size	Document Number	Rev
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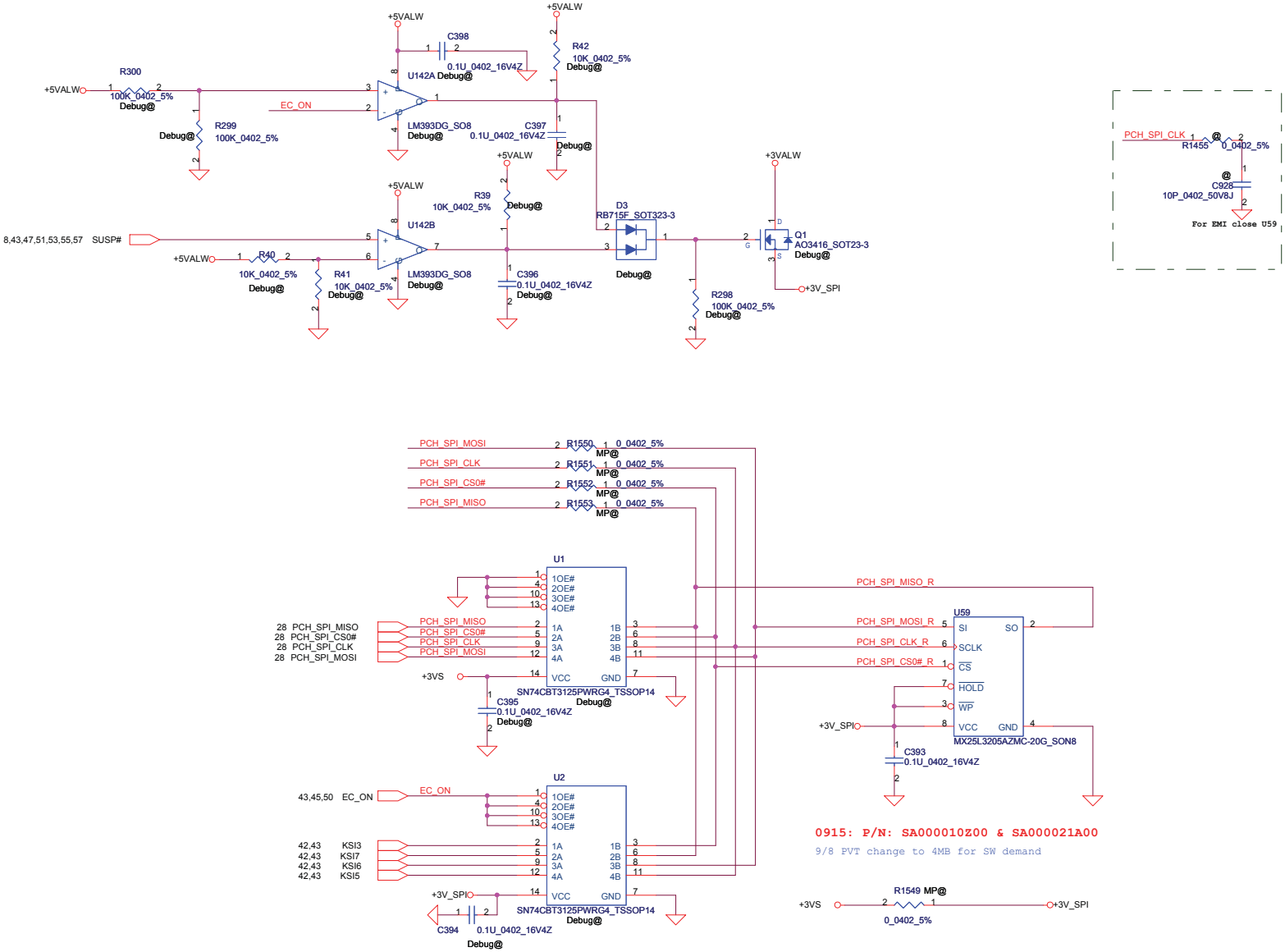
Date: Tuesday, November 02, 2010	Sheet 43 of 58	

SPI ROM For Basic ME ROM size (w/o Braidwood & system BIOS): 4MByte



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

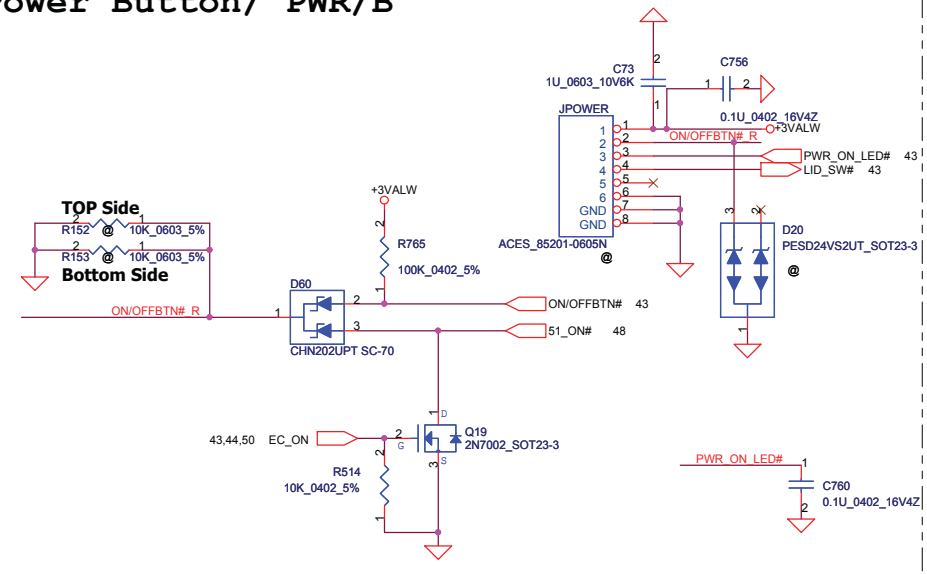
Compal Electronics, Inc.

Title: SBIOS ROM

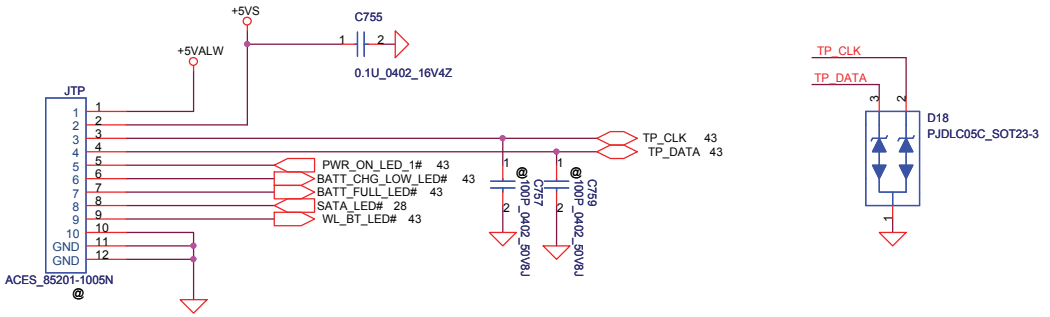
Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

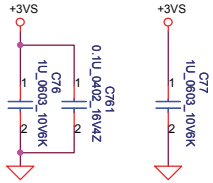
Date: Tuesday, November 02, 2010 | Sheet 44 of 58

Power Button/ PWR/B



Touch/B Connector





Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: PWR/TP/LED

Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, November 02, 2010 | Sheet 45 of 58

+1.5V to +1.05V Transfer

UT2 APL5930KAI-TRG_SO8 — 1A

Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

+3V & +1.05V has power sequence timing:
0.1*VDD(+3V) ~ 0.9*VDD(+1.05V) < 100ms

Close to U102.D7 / Close to U102.P13

Follow Vendor recommend.

+3V:200mA
+1.05V:800mA

CSEL=0 : 24MHz XTAL
CSEL=1 : 48MHz Clock

Place as close as possibile to UU102.N14 and UU102.M14

35mA

UPD720200A:
SMIB Low active

For UPD720200:
SMI high active

W=80mils
W=60mils
2.5A

Close to UU37.6

http://hobi-elektronika.net

Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

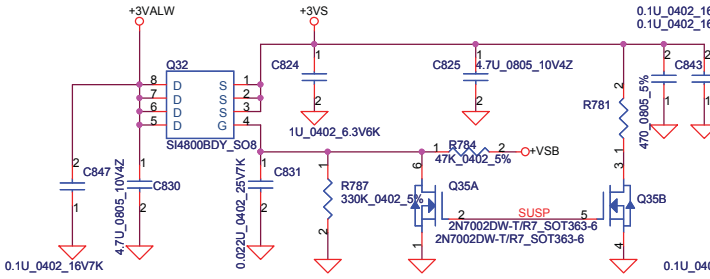
Title: PCIe-USB3.0 UPD720200A

Size: Custom | Document Number: PBL01 LA-6733P M/B | Rev: 0.3

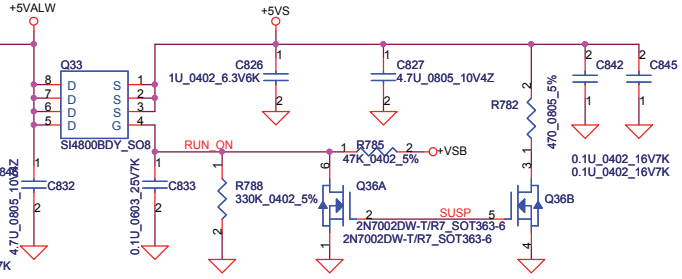
Date: Tuesday, November 02, 2010 | Sheet 46 of 58

+3VALW TO +3VS

Vgs=-0V,Id=9A,Rds=18.5mohm

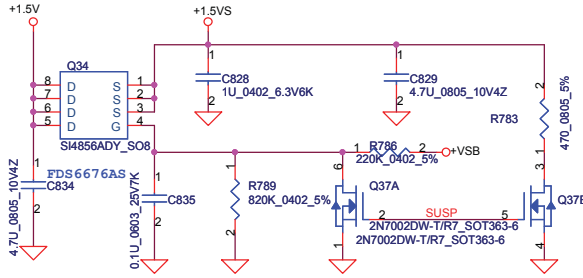


+5VALW TO +5VS



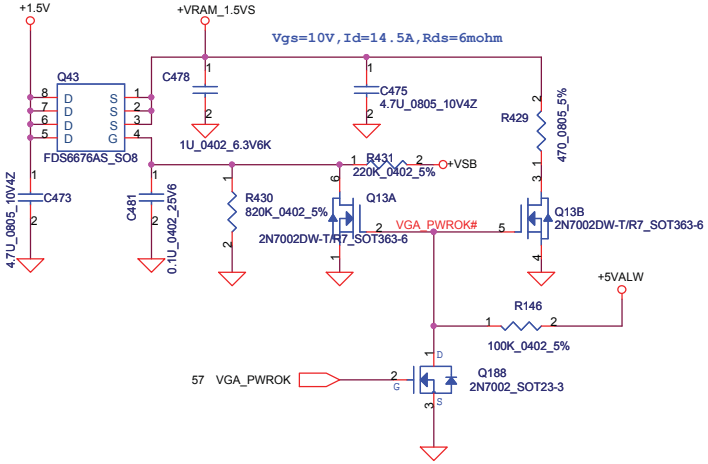
+1.5V to +1.5VS

Vgs=10V,Id=14.5A,Rds=6mohm



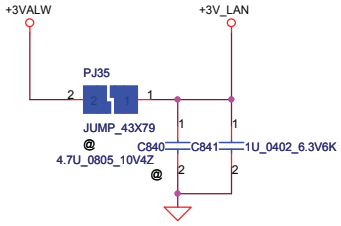
+1.5V to +VRAM_1.5VS

Vgs=10V,Id=14.5A,Rds=6mohm



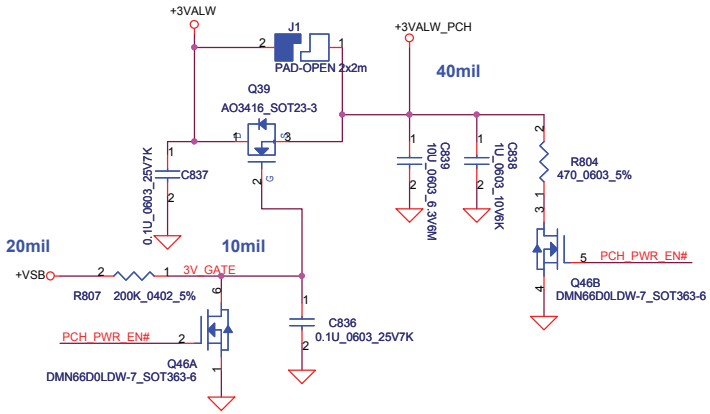
+3VALW TO +3V_LAN

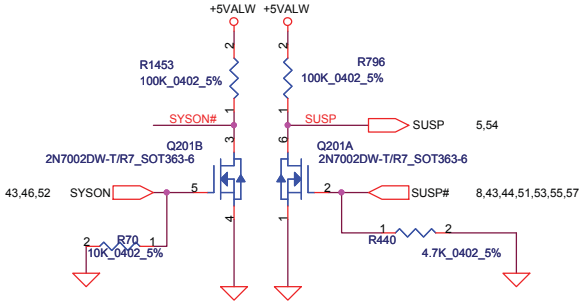
Vgs=-4.5V,Id=3A,Rds<97mohm

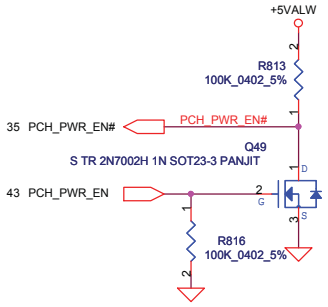


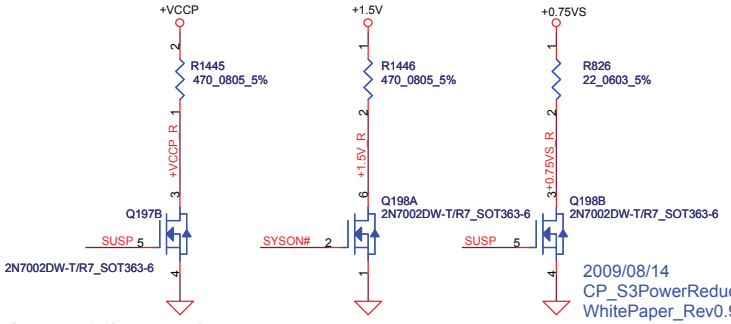
+3VALW TO +3VALW(PCH AUX Power)

Short J1 for PCH VCCSUS3.3









2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

http://hobi-elektronika.net

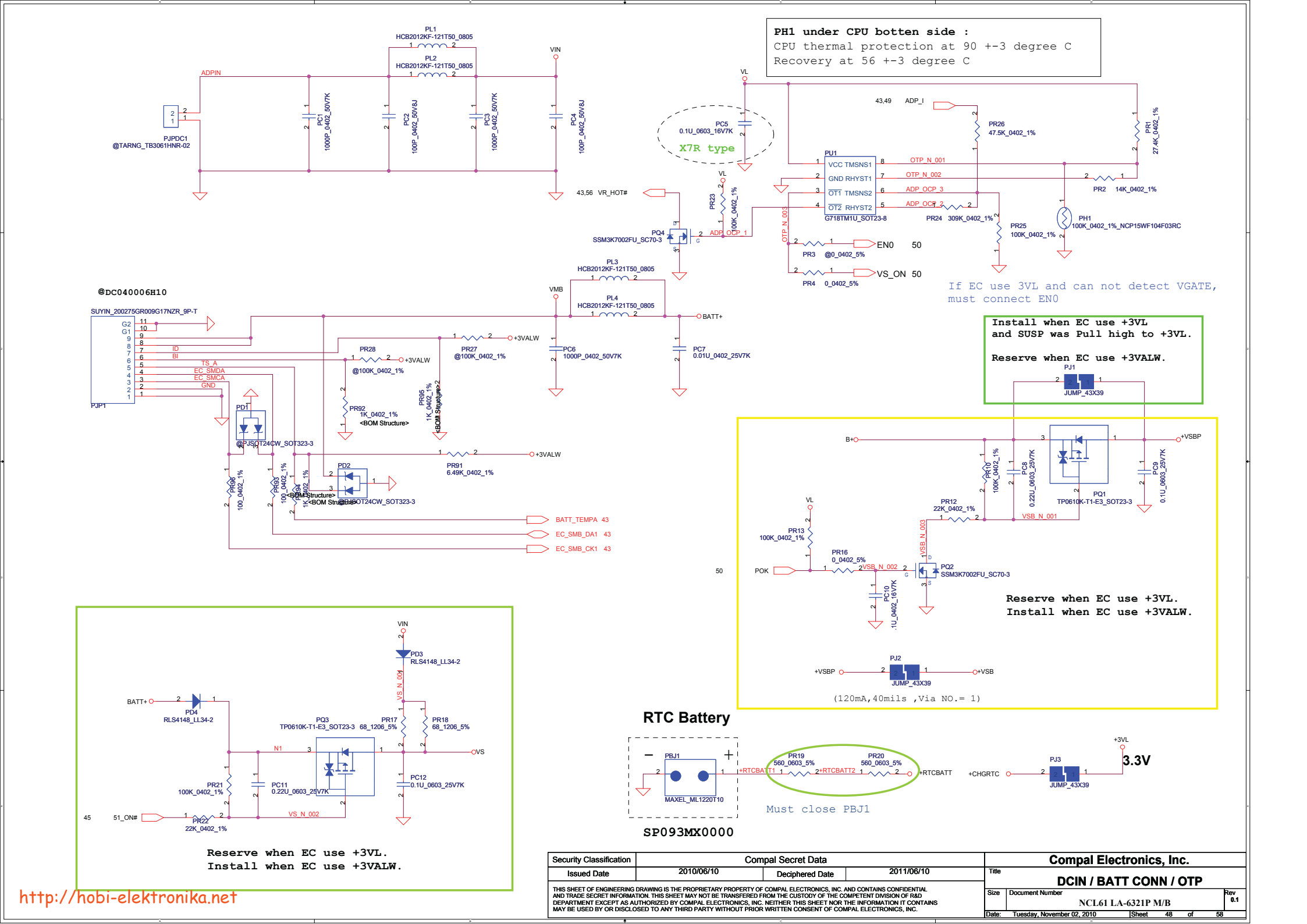
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: DC-DC INTERFACE

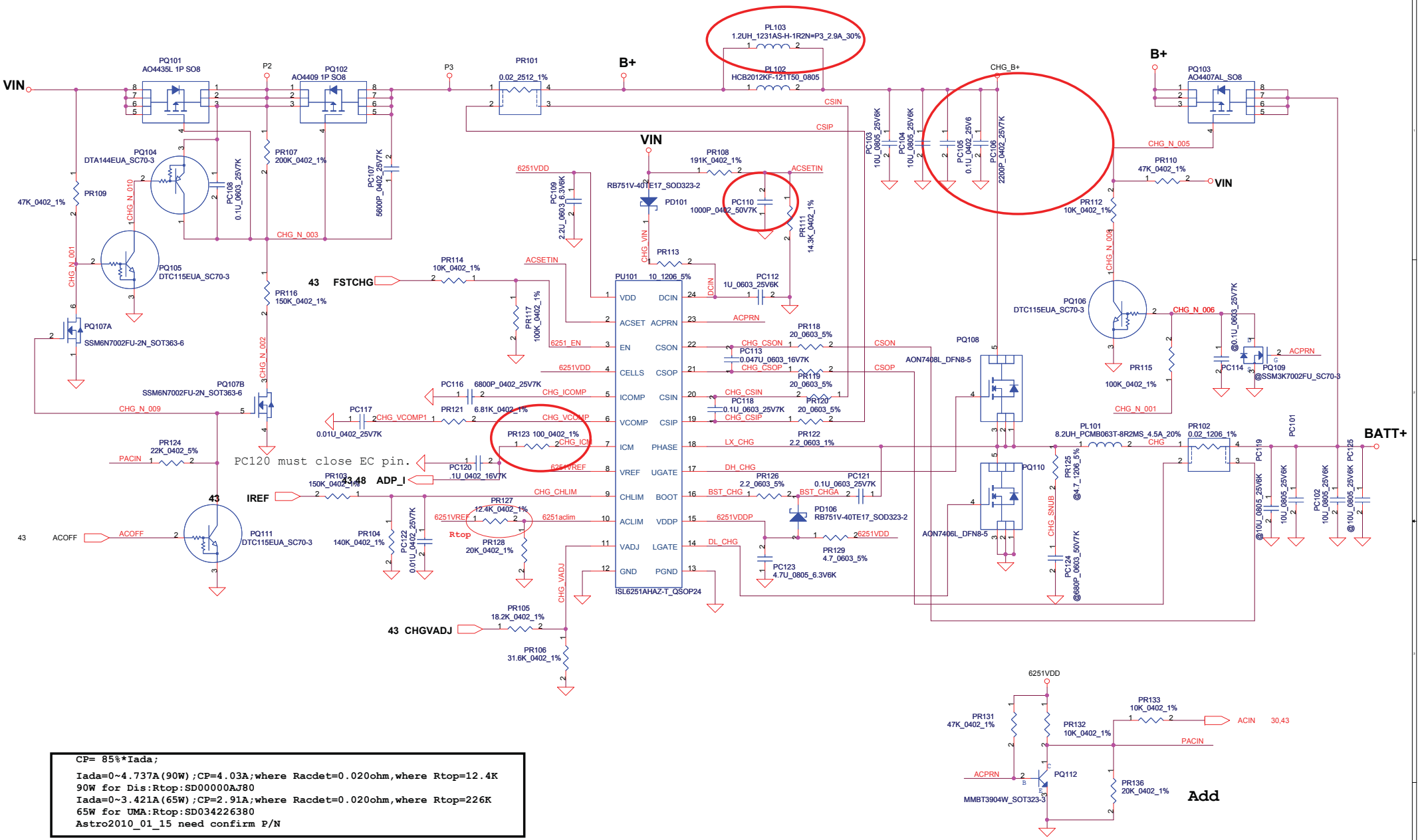
Size | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Tuesday, November 02, 2010 | Sheet 47 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.	
Title	DCIN / BATT CONN / OTP
Size	Document Number: NCL61 LA-6321P M/B
Rev	0.1
Date: Tuesday, November 02, 2010	Sheet 48 of 58




```
CP= 85%*Iada;
Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N
```

```
CP mode
Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A
```

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

Add

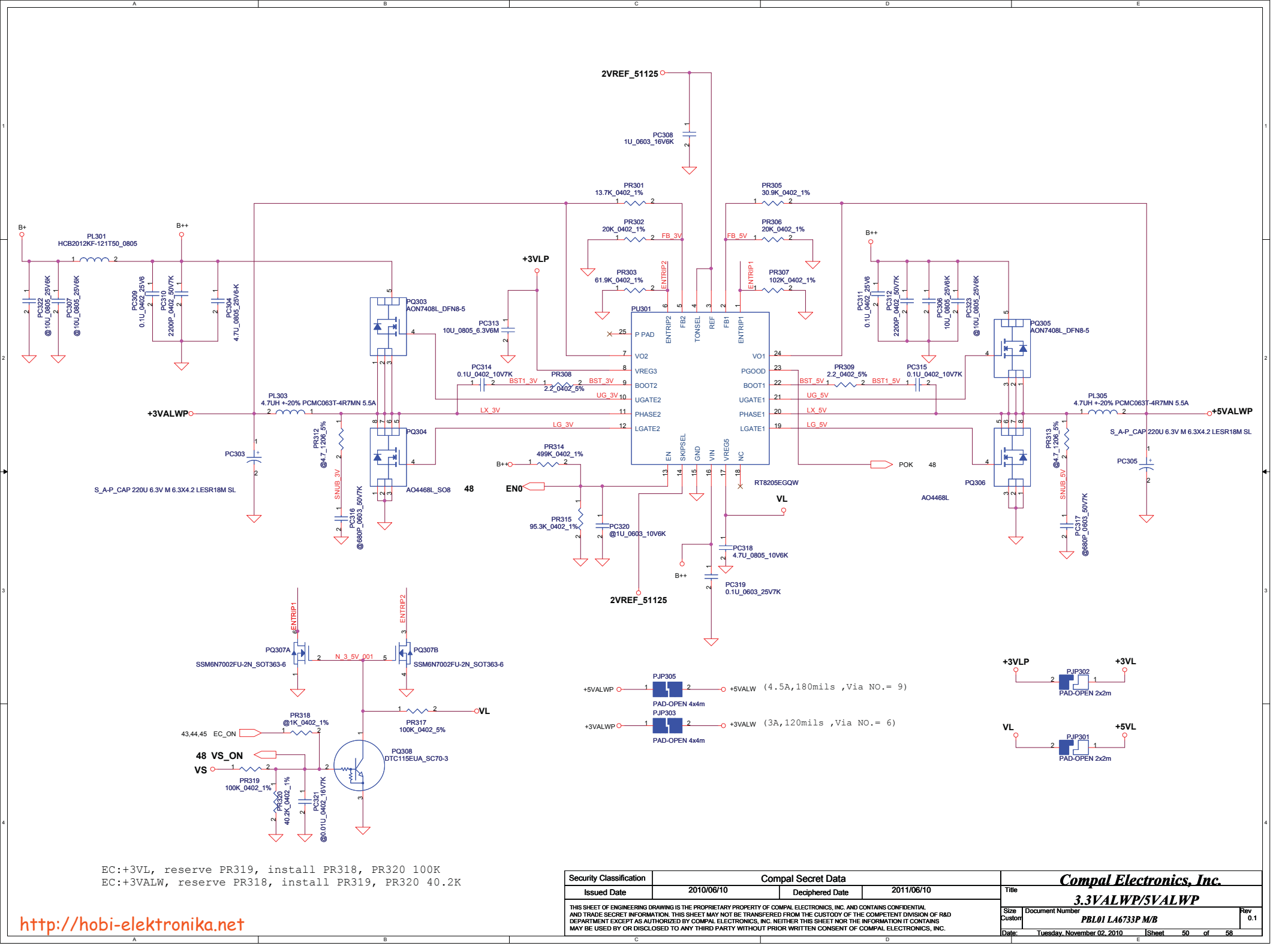
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
	PBL01 LA6732P MB	0.1

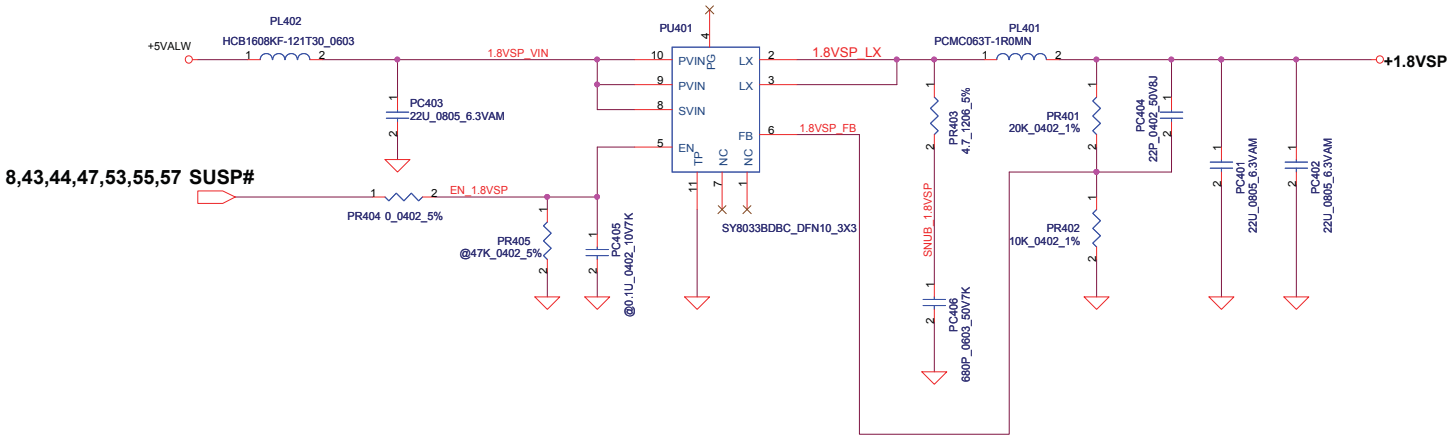
Date: Tuesday, November 02, 2010 Sheet 49 of 58



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size: Custom	Document Number: PBL01 LA6733P M/B		Rev: 0.1
Date: Tuesday, November 02, 2010		Sheet 50 of 58	



<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR401/PR402)=0.6*(1+20K/10K)=1.8V

(2A, 80mils, Via NO.= 4)

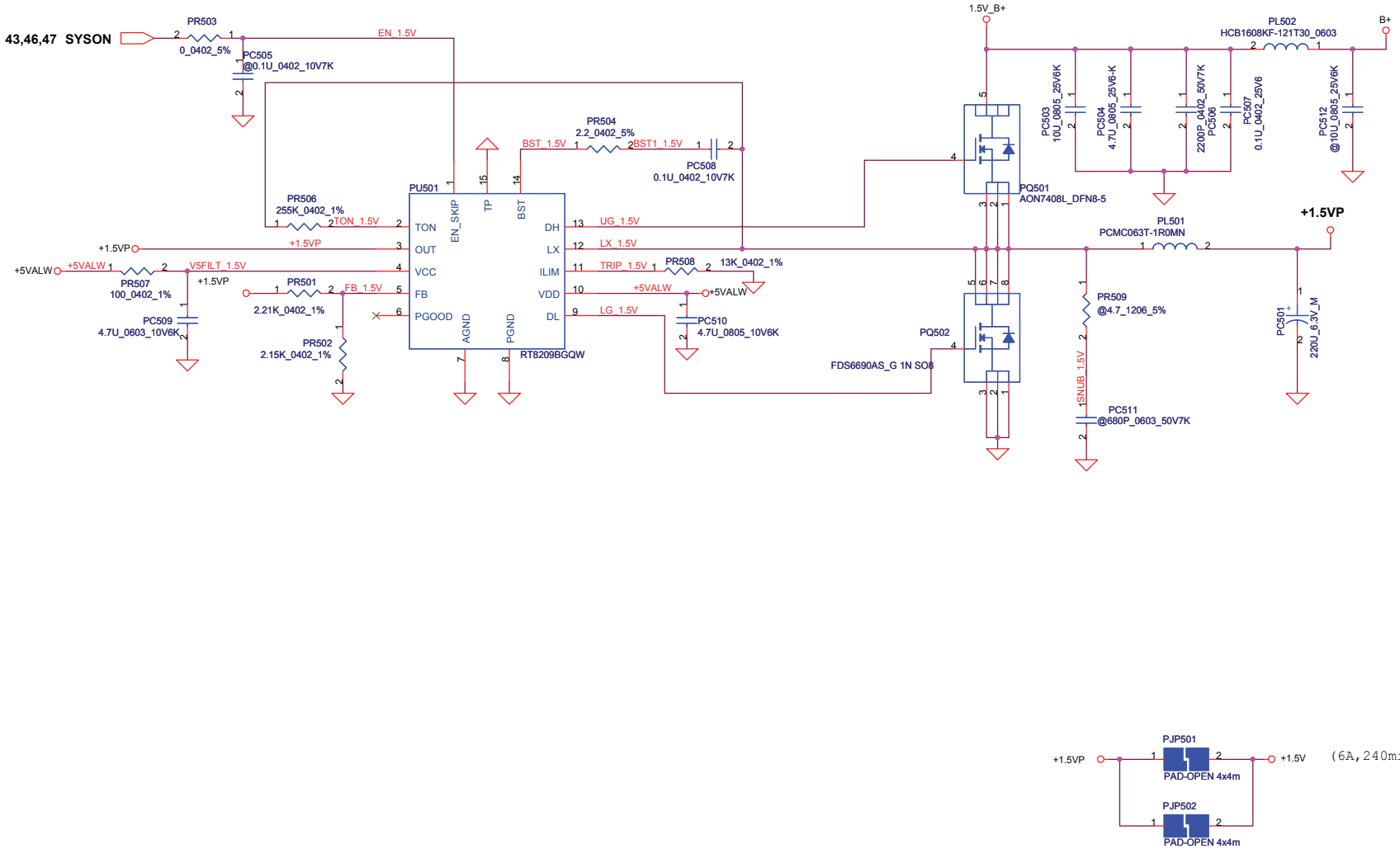
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: **+1.8VSP**

Size	Document Number	Rev
	PBL01 LA6732P MB	0.1

Date: Tuesday, November 02, 2010 Sheet 51 of 58



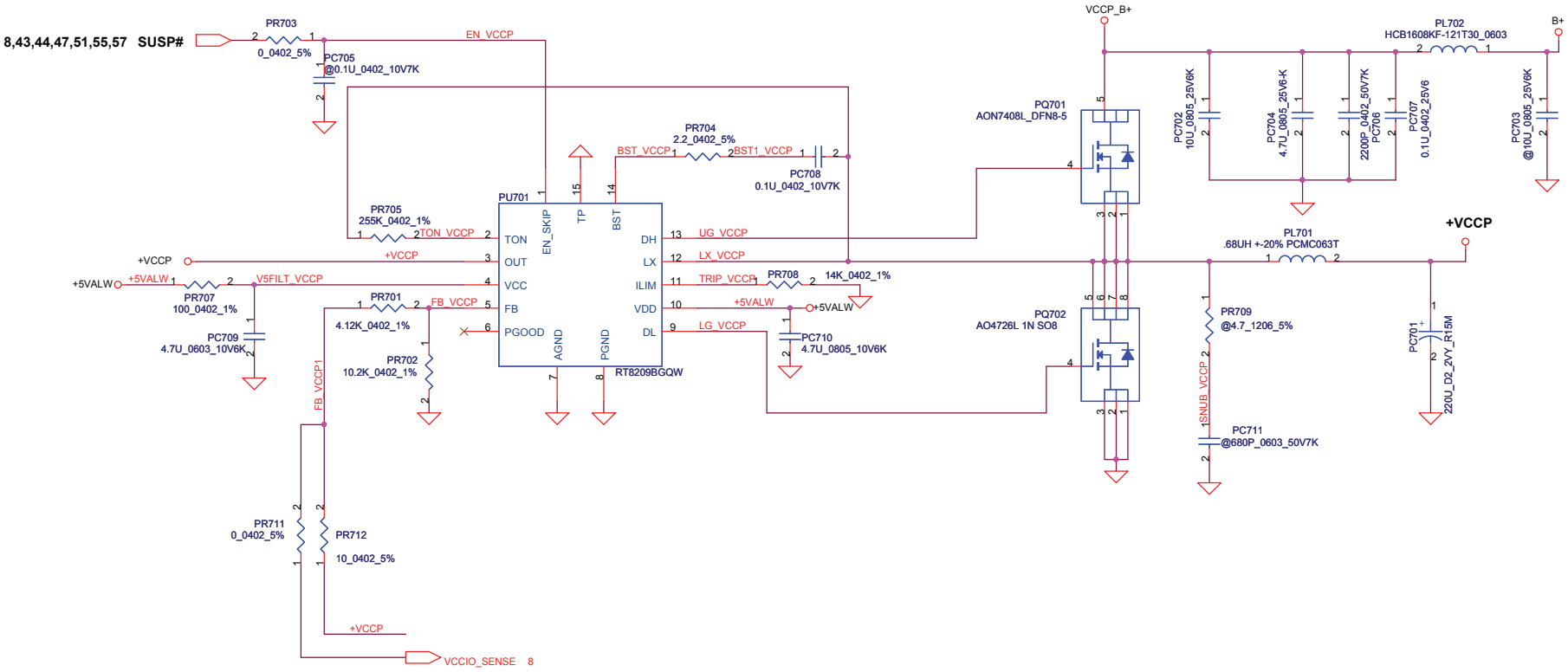
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	PBL01 LA6733P M/B	0.1

Date: Tuesday, November 02, 2010 | Sheet 52 of 58



VSSIO_SENSE connect to GND directly.

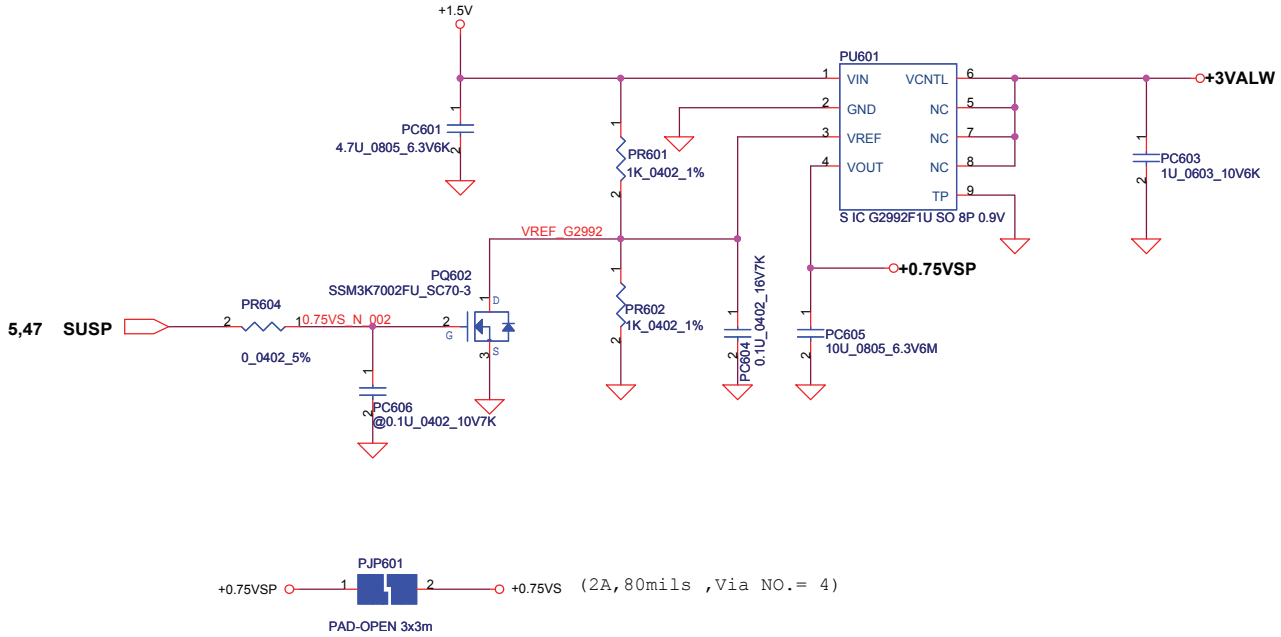
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: PWR+1.05VSP/+VCCPP

Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.1

Date: Tuesday, November 02, 2010 | Sheet 53 of 58



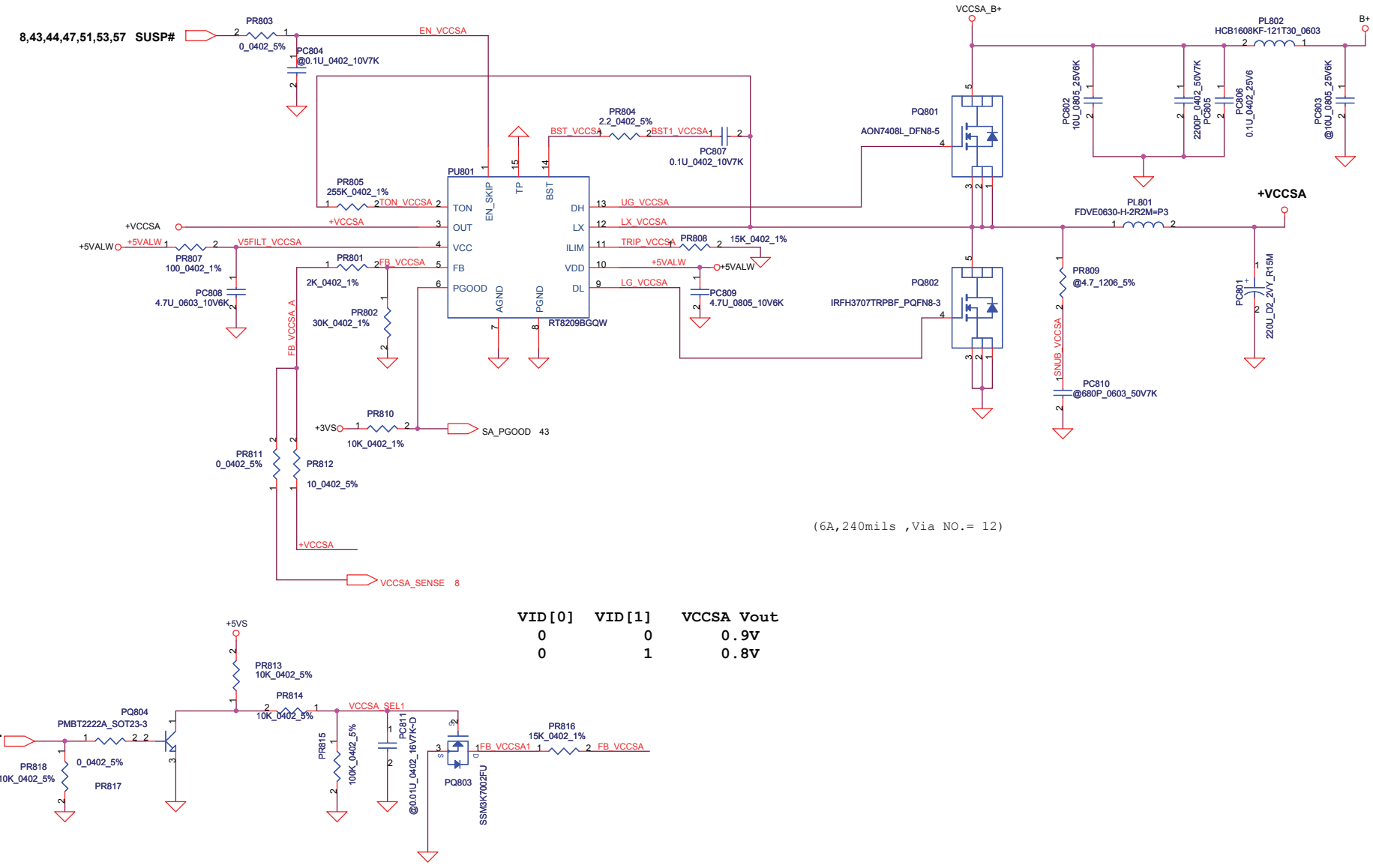
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: **0.75VSP/1.1VSP**

Size	Document Number	Rev
	PBL01 LA6733P M/B	0.1

Date: Tuesday, November 02, 2010 Sheet 54 of 58



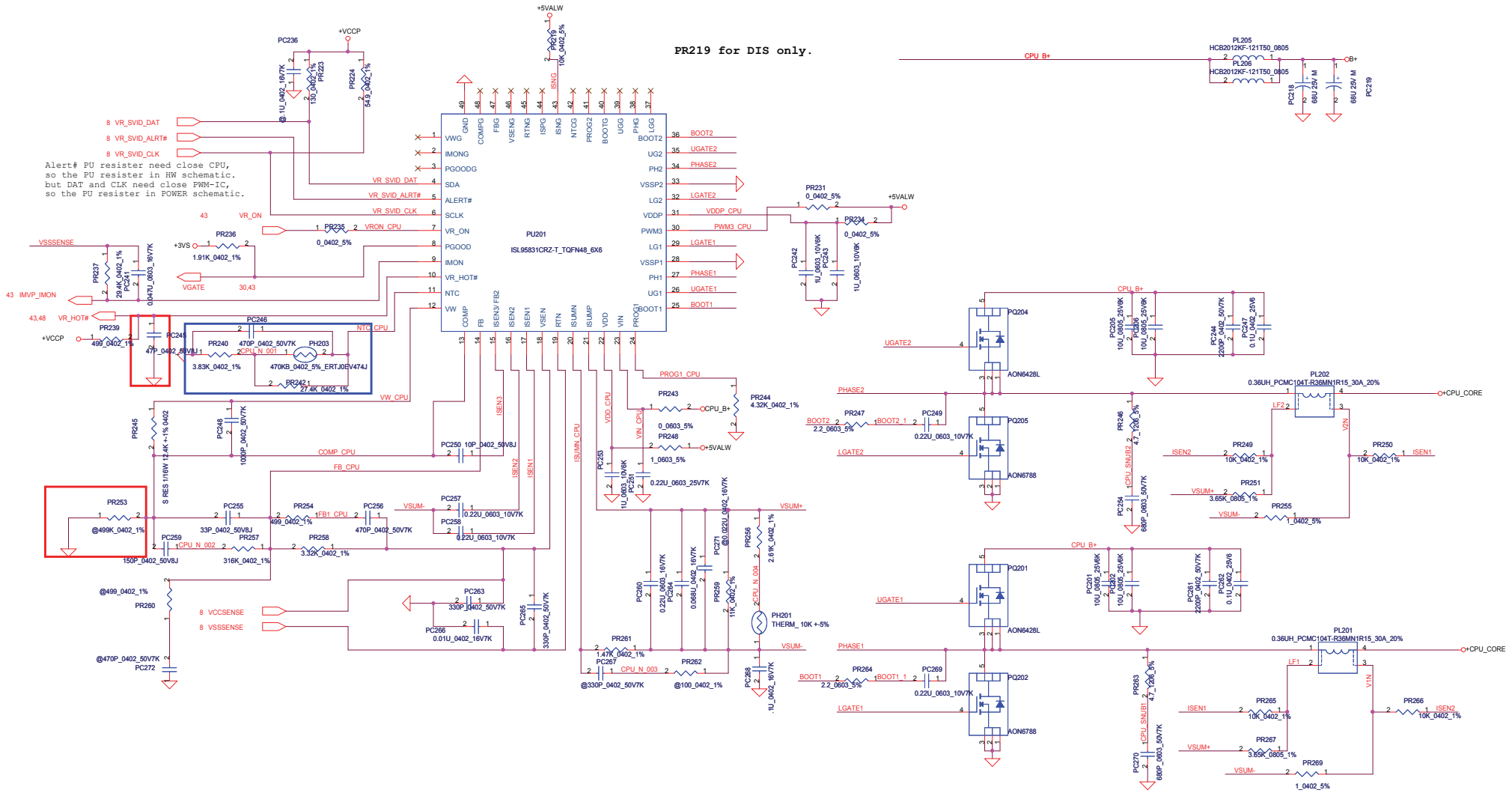
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: PWR+VCCSAP

Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.1

Date: Tuesday, November 02, 2010 | Sheet 55 of 58



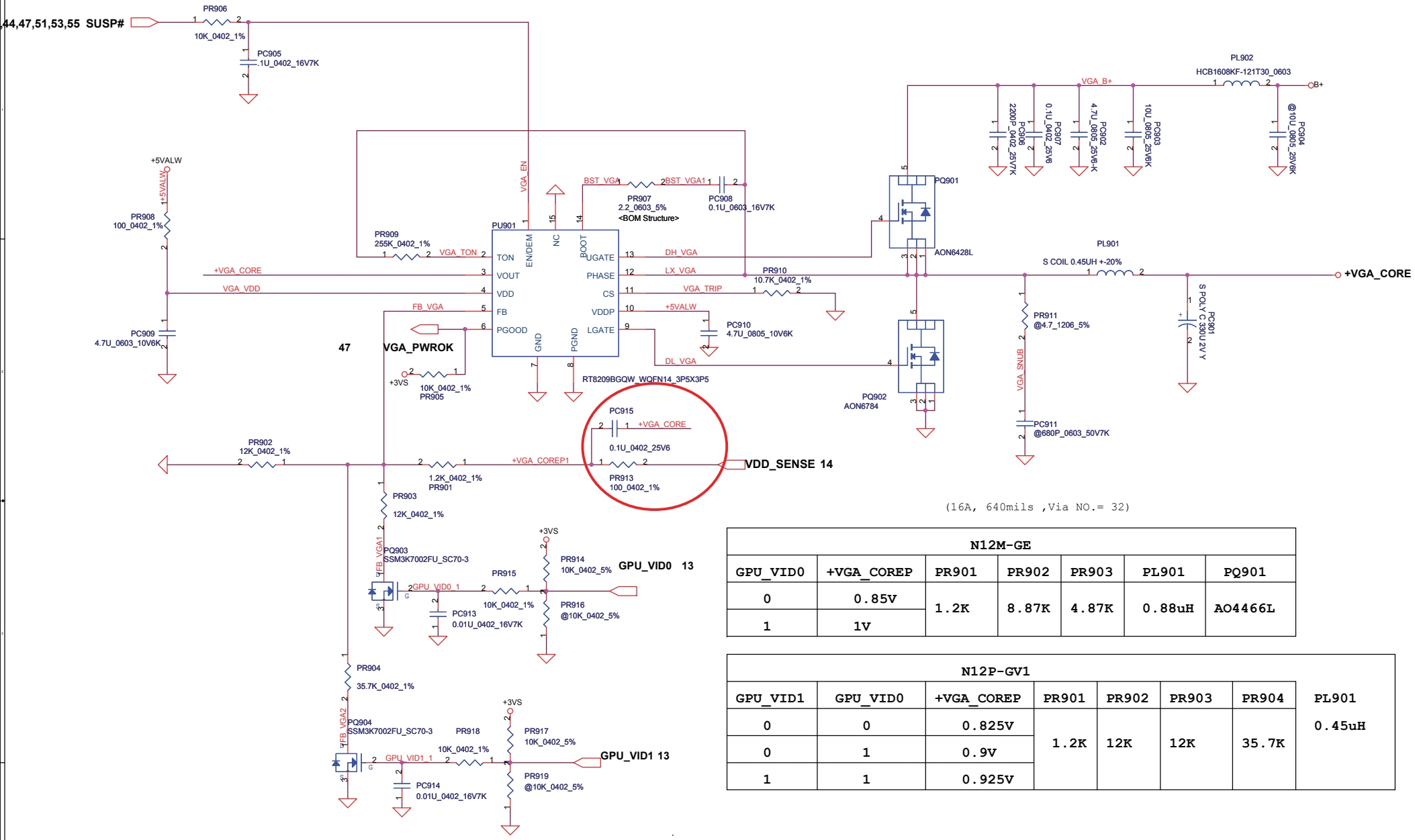
Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size	Document Number	Rev
C	PBL01 LA6733P M/B	0.1

Date: Tuesday, November 02, 2010 Sheet 56 of 58



(16A, 640mils ,Via NO.= 32)

N12M-GE						
GPU_VID0	+VGA_COREP	PR901	PR902	PR903	PL901	PQ901
0	0.85V	1.2K	8.87K	4.87K	0.88uH	AO4466L
1	1V					

N12P-GV1							
GPU_VID1	GPU_VID0	+VGA_COREP	PR901	PR902	PR903	PR904	PL901
0	0	0.825V	1.2K	12K	12K	35.7K	0.45uH
0	1	0.9V					
1	1	0.925V					

Need double confirm with HW
about the voltage level setting
N12P-LP default value is high level

Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: +VGA_COREP

Size | Document Number: PBL01 LA6733P M/B | Rev: 1.0

Date: Tuesday, November 02, 2010 | Sheet 57 of 58

Revision Change: 0.1 to 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	08/12	All	Remove all components about UMA@	From UMA/DIS schematic to DIS only
2	08/12	41	Change RA16 from 5.1K to 39.2K & connect from SENSE_B to SENSE_A	Headphone out can't detect issue
3	08/12	46	Change USB30 from TI to NEC	SPEC request
4	08/12	27	Delet U37 and relate schematic. Q16.1 connect to HDMI connector directly. R570 from 100K to 20K	HDMI Hot Plug issue
5	08/24	41	Change RA9,RA10 to 4.7U	For Audio Precision
6	08/24	29	Change CLKREQ_USB30# Pull-hi from +3VS to +3VALW_PCH	Vendor request
7	08/25	43	Mount R1368 and C930	EMI request
8	08/25	28,29,32	Change R101,R258, and R1545 to 47ohm	EMI request
9	08/25	5	Add R15 between PLT_RST# to U3	EMI request
10	08/25	25	Change C399 to 1U_0603	EMI request
11	08/25	45	Add C760	EMI request
12	08/26	10	Remove C80	DFB issue
13	08/26	45	Change CT31 footprint to B2	DFB issue
14	08/31	45	Add C73,C76,C77, and C761	EMI issue
15	09/01	14	Remove RV33,RV34	ME issue
16	09/02	41	Reserve C931 and R1370	EMI request
17	09/02	43	Remove C208	EMI request

Revision Change: 0.2 to 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	10/08	28	Add R1569	Power consumption
2	10/20	43	Add R725 and pull high +3VALW	For common design
3	10/20	46	Remove DT1	For cost down
4	10/20	27	Remove D17	For cost down
5	10/22	39	Reserve D22, D23	EMI request
6	10/27	43	Add R726 and pull high +3VALW	For common design
7	10/28	43	Add R138 and pull low to GND	EC request

Security Classification	Compal Secret Data		
Issued Date	2010/06/10	Deciphered Date	2011/06/10

Compal Electronics, Inc.

Title: HW PIRI

Size: Custom | Document Number: PBL01 LA6733P M/B | Rev: 0.3

Date: Thursday, October 28, 2010 | Sheet 58 of 58