

Compal Confidential

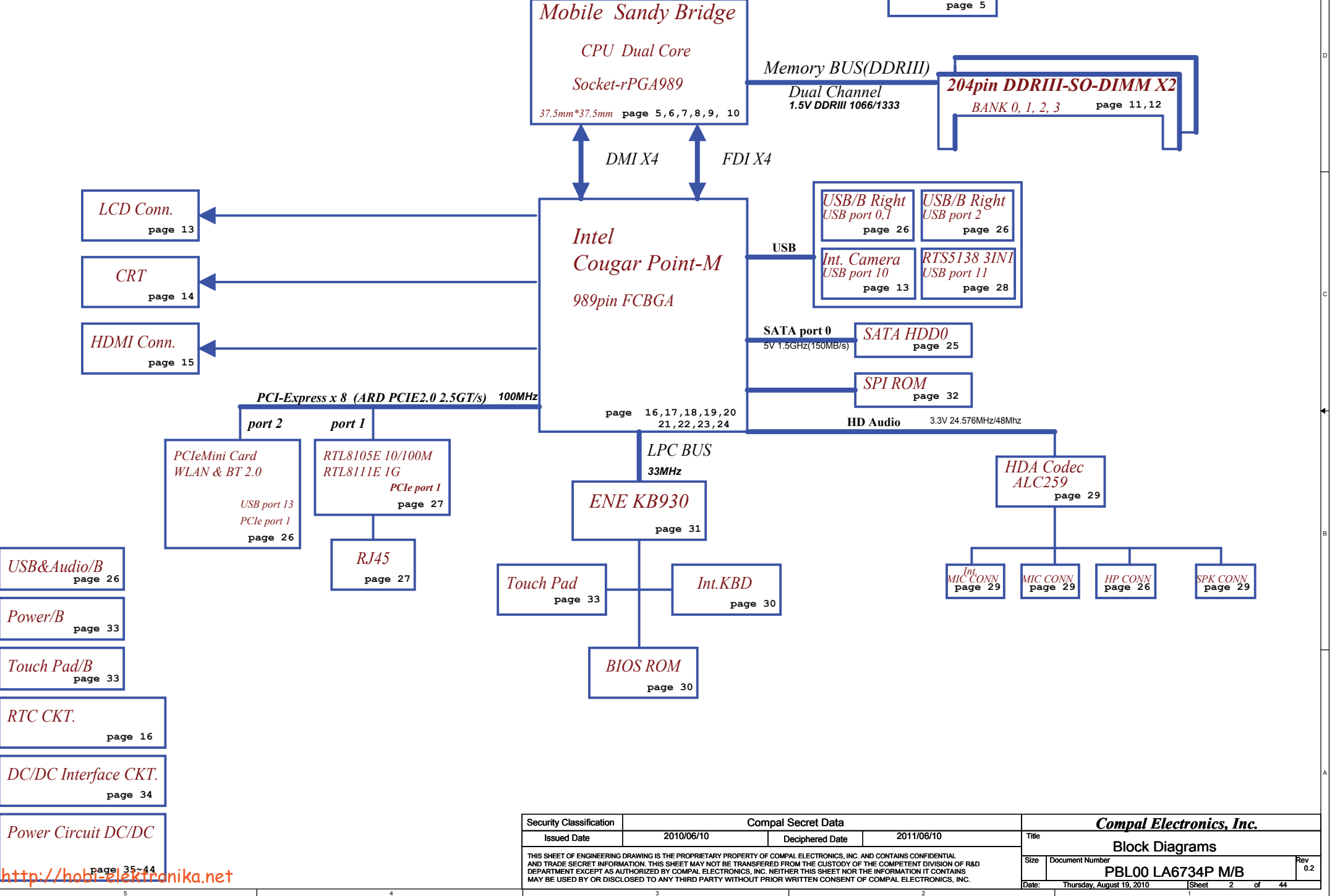
PBL00

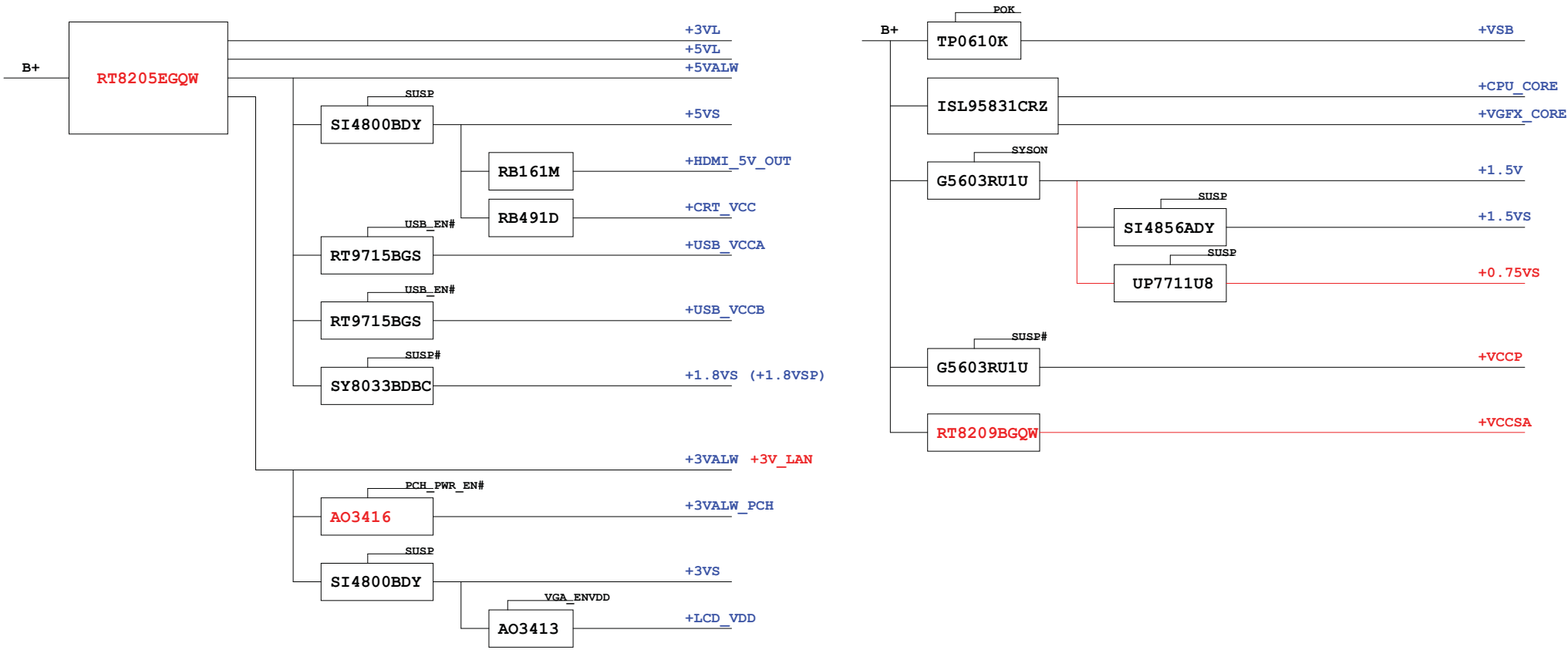
LA-6734P REV 0.2 Schematic

Intel Sandy Bridge/Cougar Point (UMA)

2010-10-28 Rev. 0.2

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

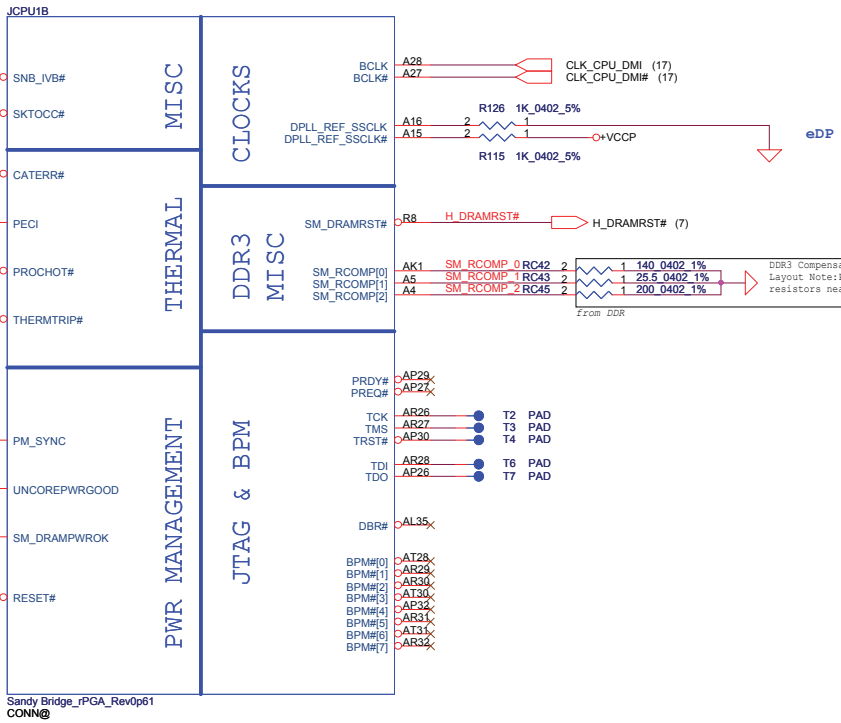
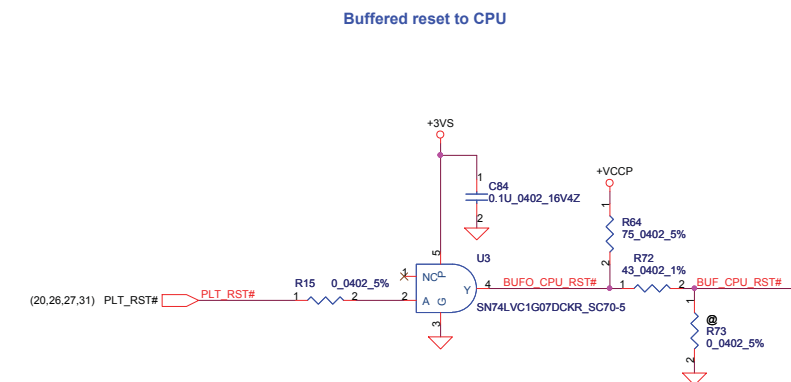
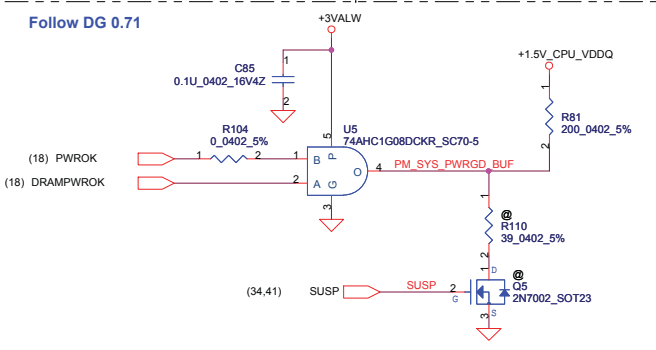
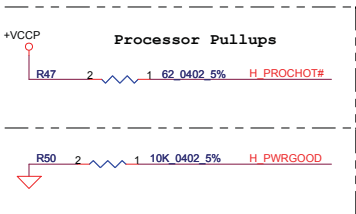
Power	Device	Address	Power	Device	Address
+3VALW	EC KB930		+3VS	EC KB930	
+3VL	Smart Battery	0001 011x b	+3VS	GPU Thermal Sensor	
			+3VALW	PCH	

EC SM Bus2 address

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Slot#1--WLAN	

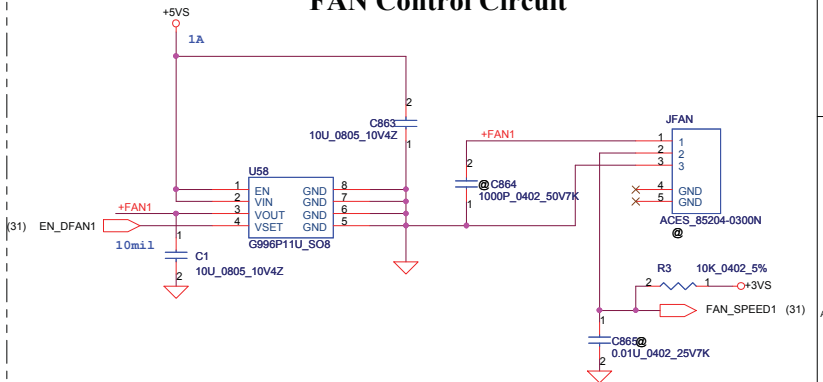
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Issued Date	2010/06/10	Deciphered Date	2011/06/10	Notes List		
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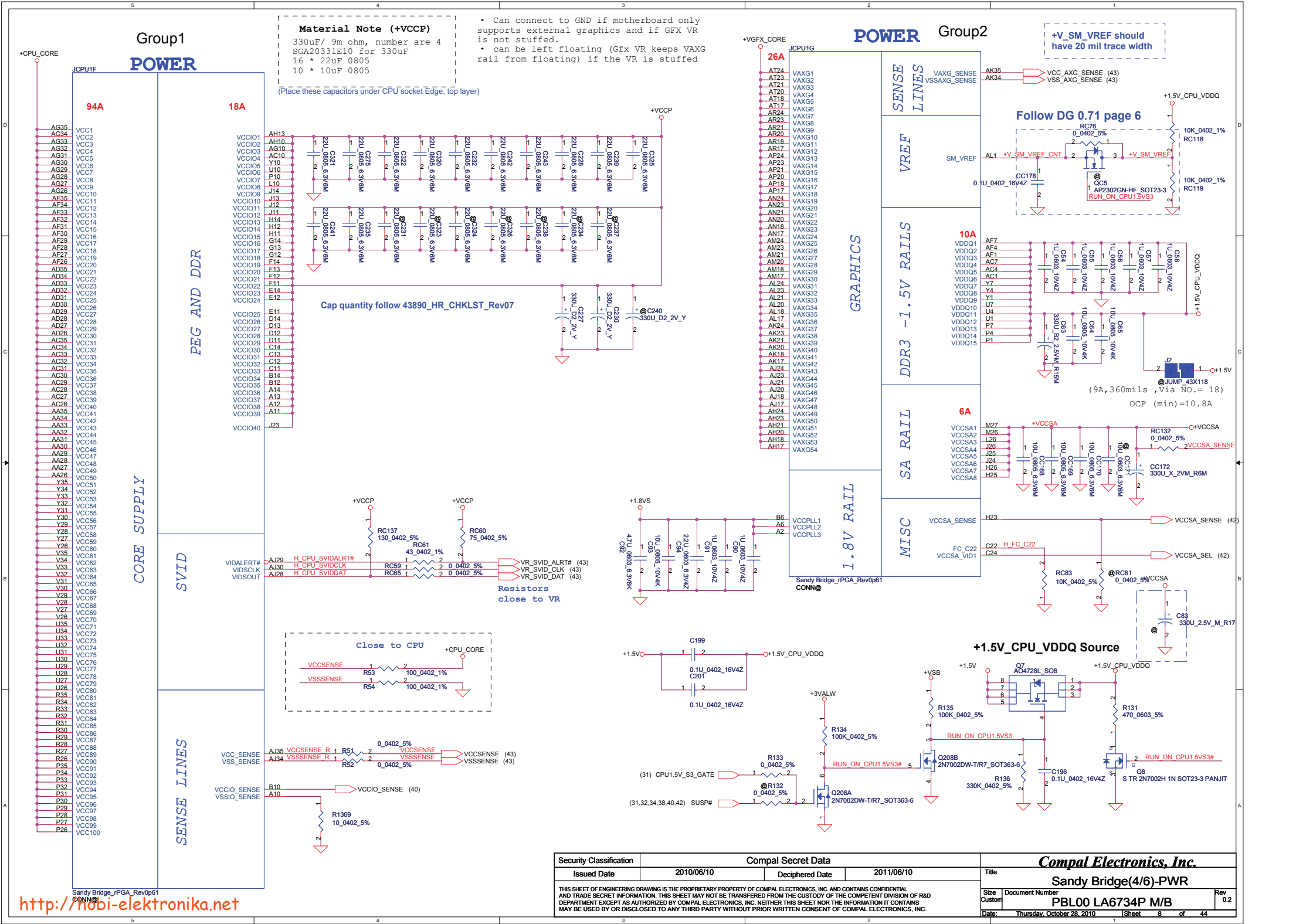


Terminate DPLL_REF_SSCLK to GND and PLL_REF_SSCLK# to VCCP on Processor if motherboard only supports external graphics.

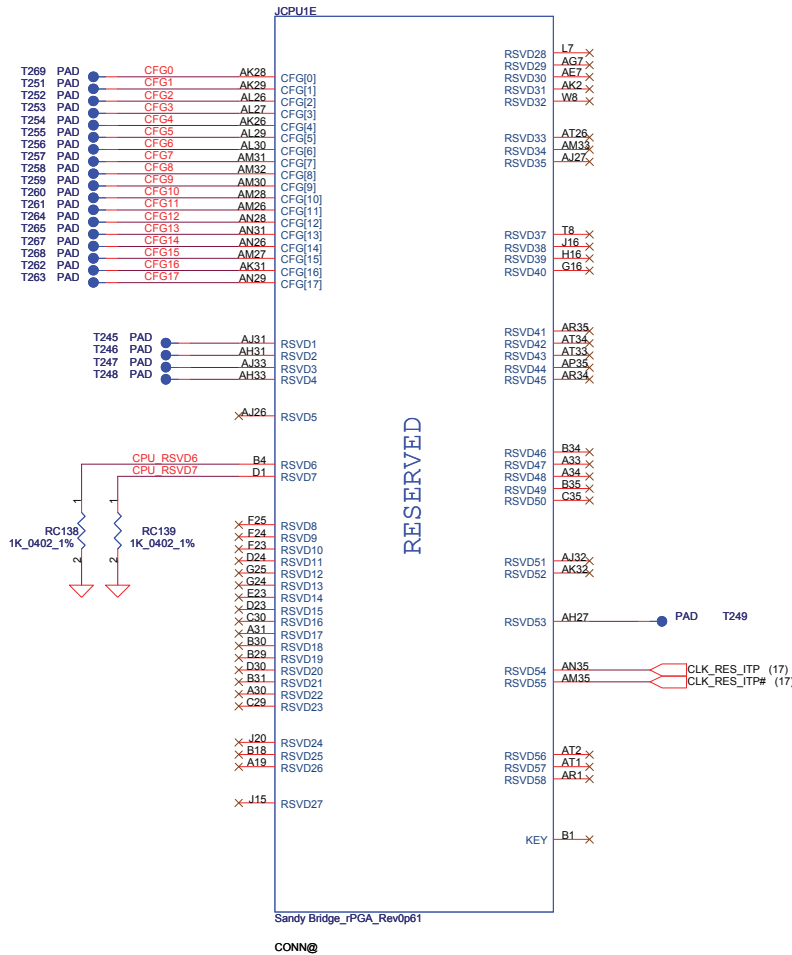
DDR3 Compensation Signals
Layout Note: Please these resistors near Processor

FAN Control Circuit





CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

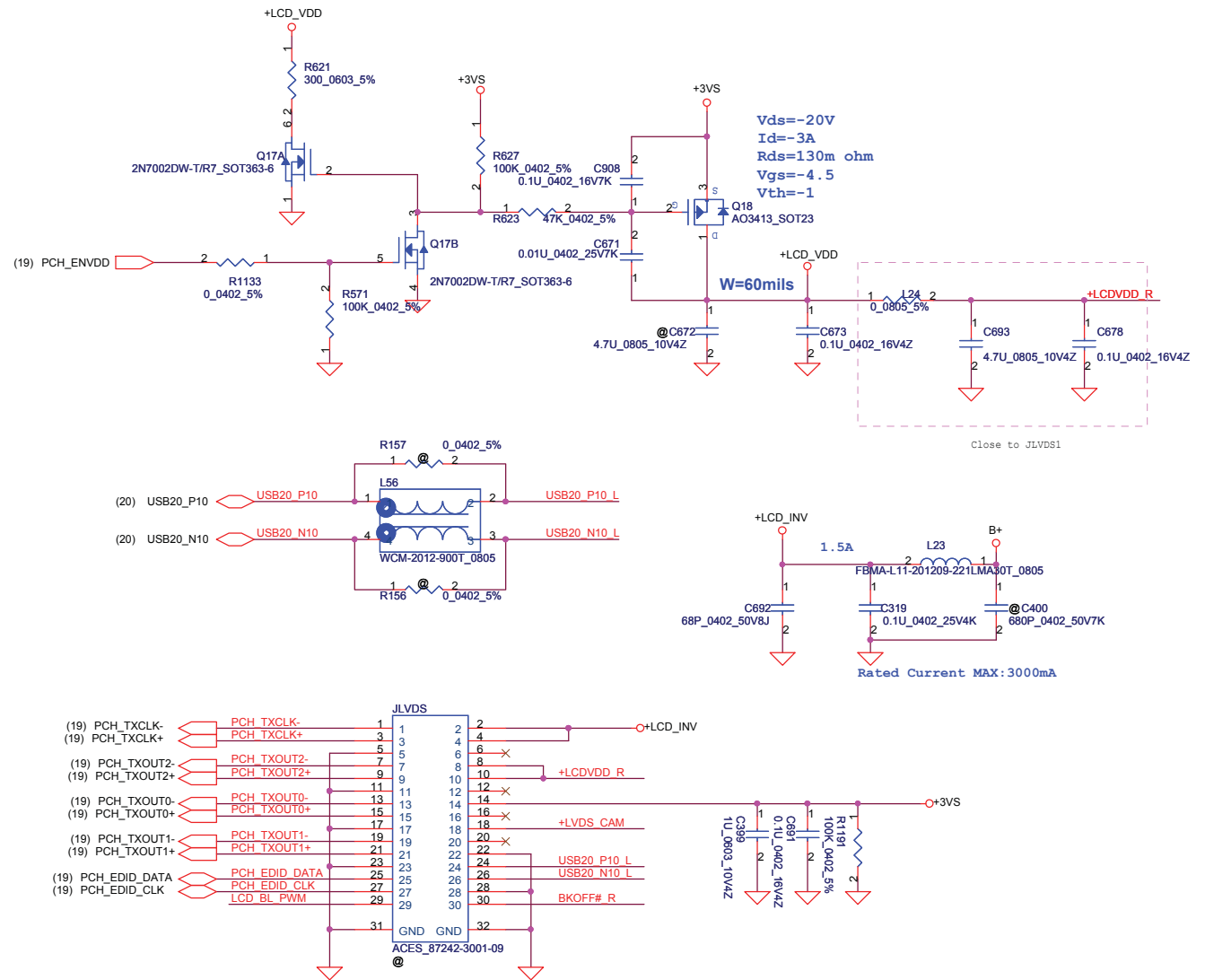
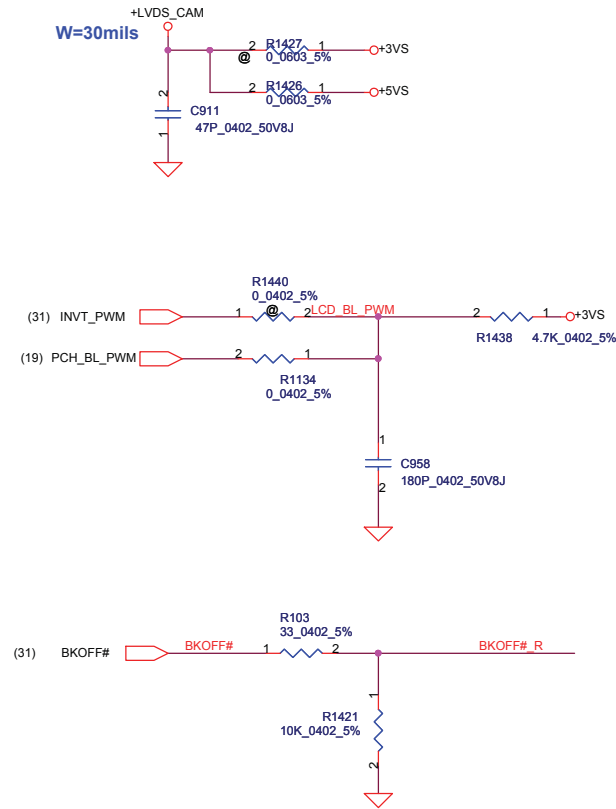
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

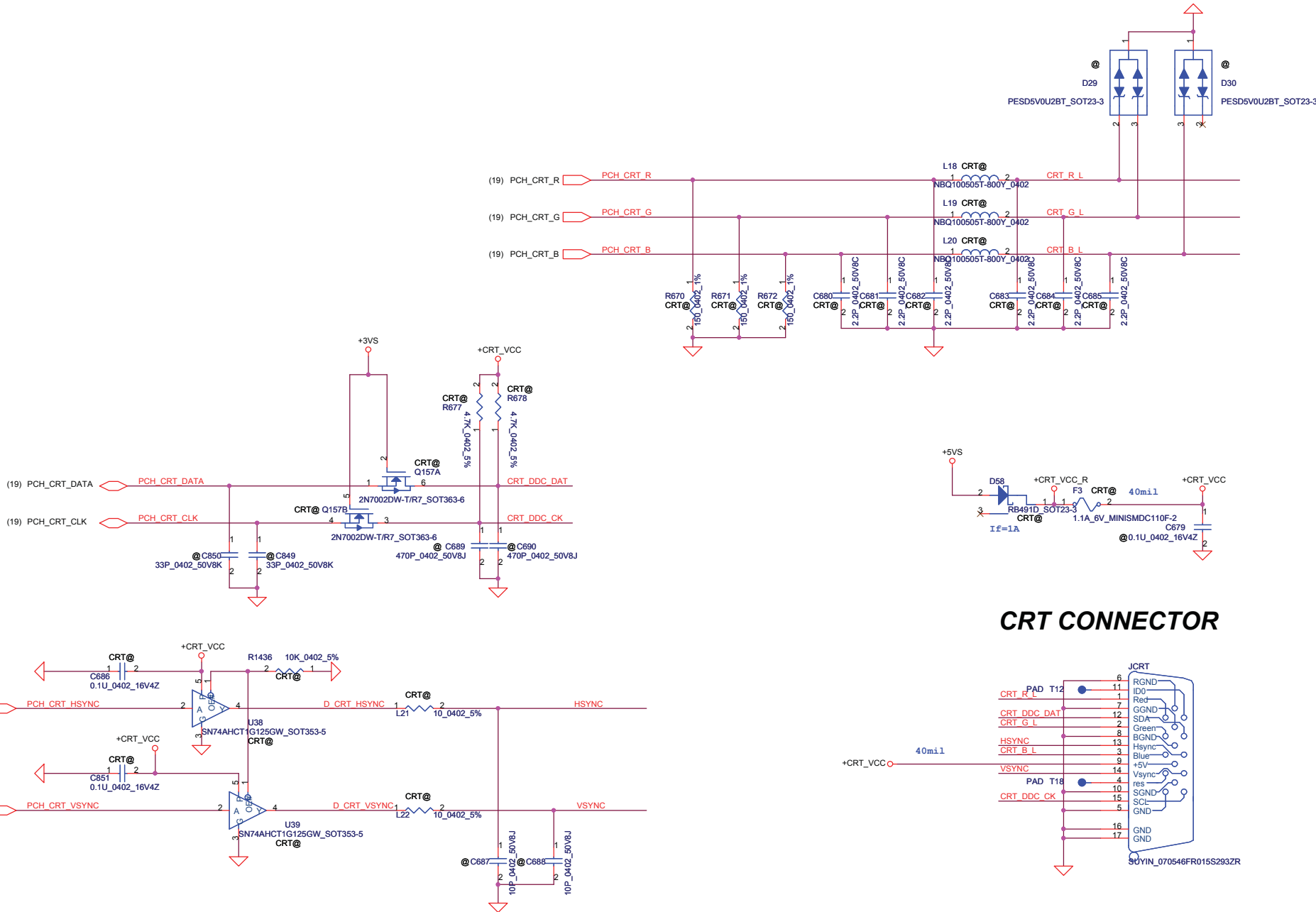
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



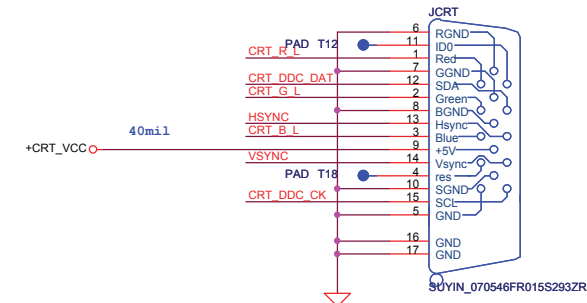
LCD/PANEL BD. Conn.



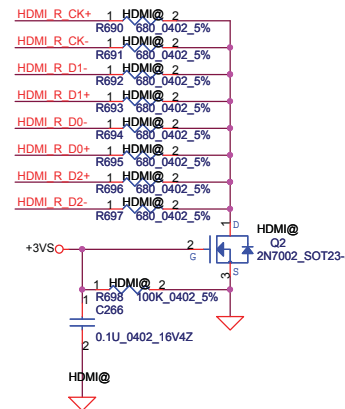
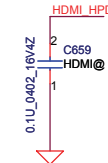
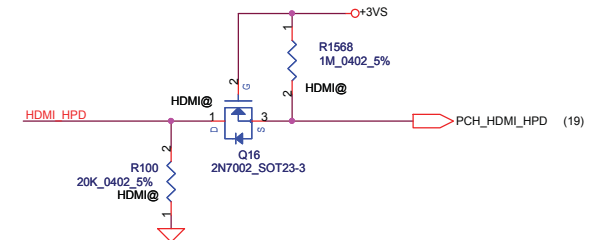
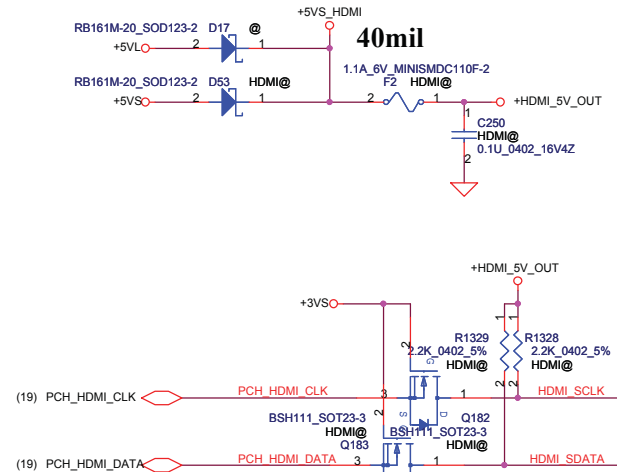
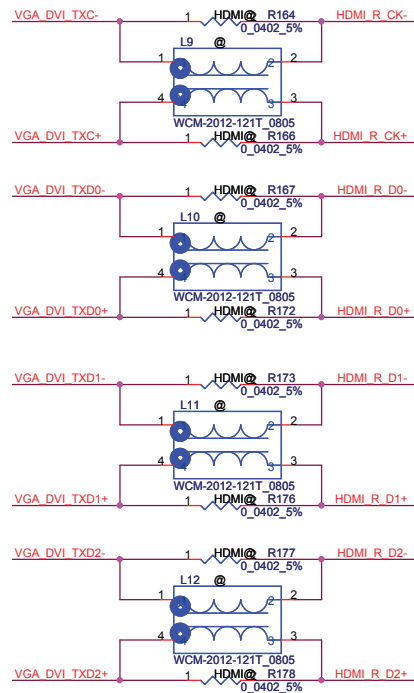
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								Size	Document Number						Rev	
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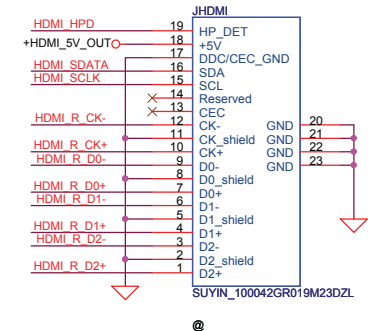
CRT CONNECTOR



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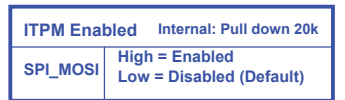
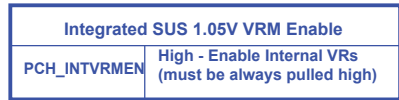
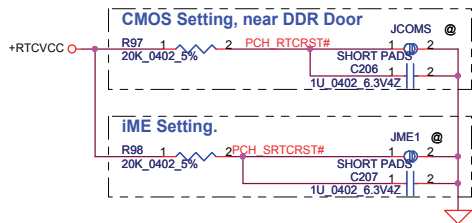


HDMI Connector



(19) PCIE_MTX_GRX_HDMI_P3	HDMI@	CV269	1	2	0.1U_0402_16V7K	VGA DVI TXC+
(19) PCIE_MTX_GRX_HDMI_N3	HDMI@	CV270	1	2	0.1U_0402_16V7K	VGA DVI TXC-
(19) PCIE_MTX_GRX_HDMI_P2	HDMI@	CV271	1	2	0.1U_0402_16V7K	VGA DVI TXD0+
(19) PCIE_MTX_GRX_HDMI_N2	HDMI@	CV272	1	2	0.1U_0402_16V7K	VGA DVI TXD0-
(19) PCIE_MTX_GRX_HDMI_P1	HDMI@	CV273	1	2	0.1U_0402_16V7K	VGA DVI TXD1+
(19) PCIE_MTX_GRX_HDMI_N1	HDMI@	CV274	1	2	0.1U_0402_16V7K	VGA DVI TXD1-
(19) PCIE_MTX_GRX_HDMI_P0	HDMI@	CV275	1	2	0.1U_0402_16V7K	VGA DVI TXD2+
(19) PCIE_MTX_GRX_HDMI_N0	HDMI@	CV276	1	2	0.1U_0402_16V7K	VGA DVI TXD2-

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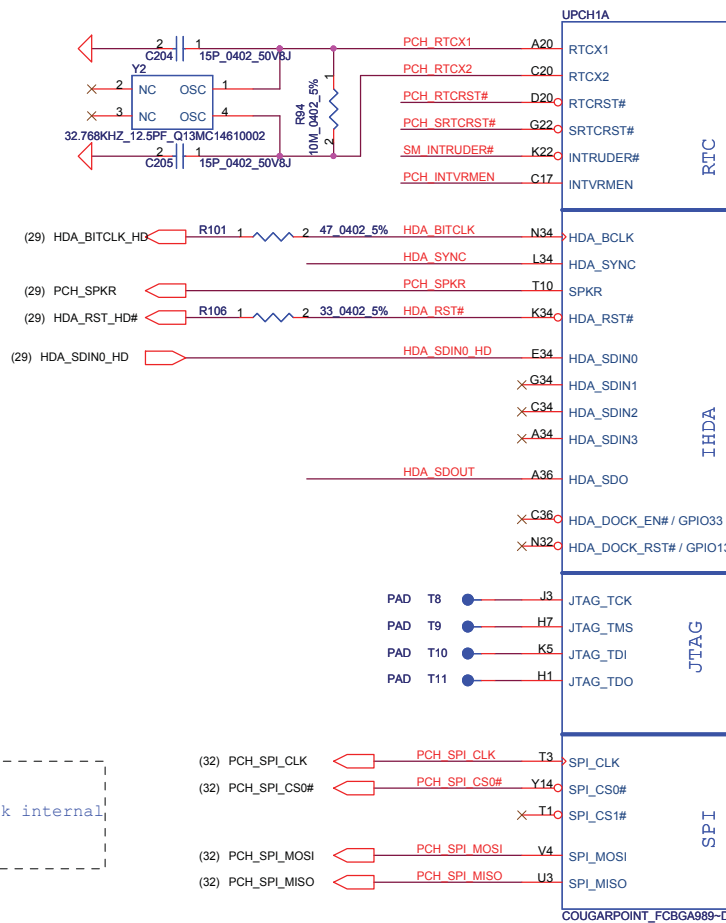
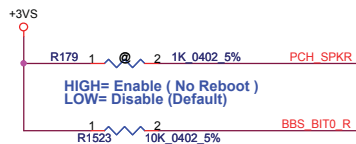
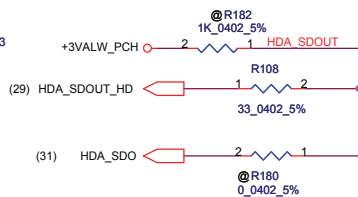
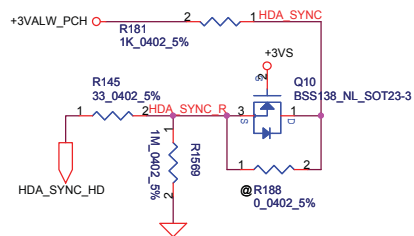


HDA_SYNC

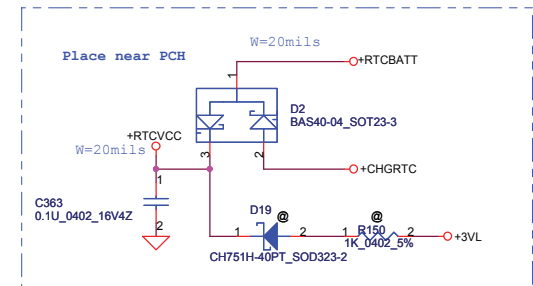
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

HDA_SDO

This signal has a weak internal pull down.
This signal can't PU



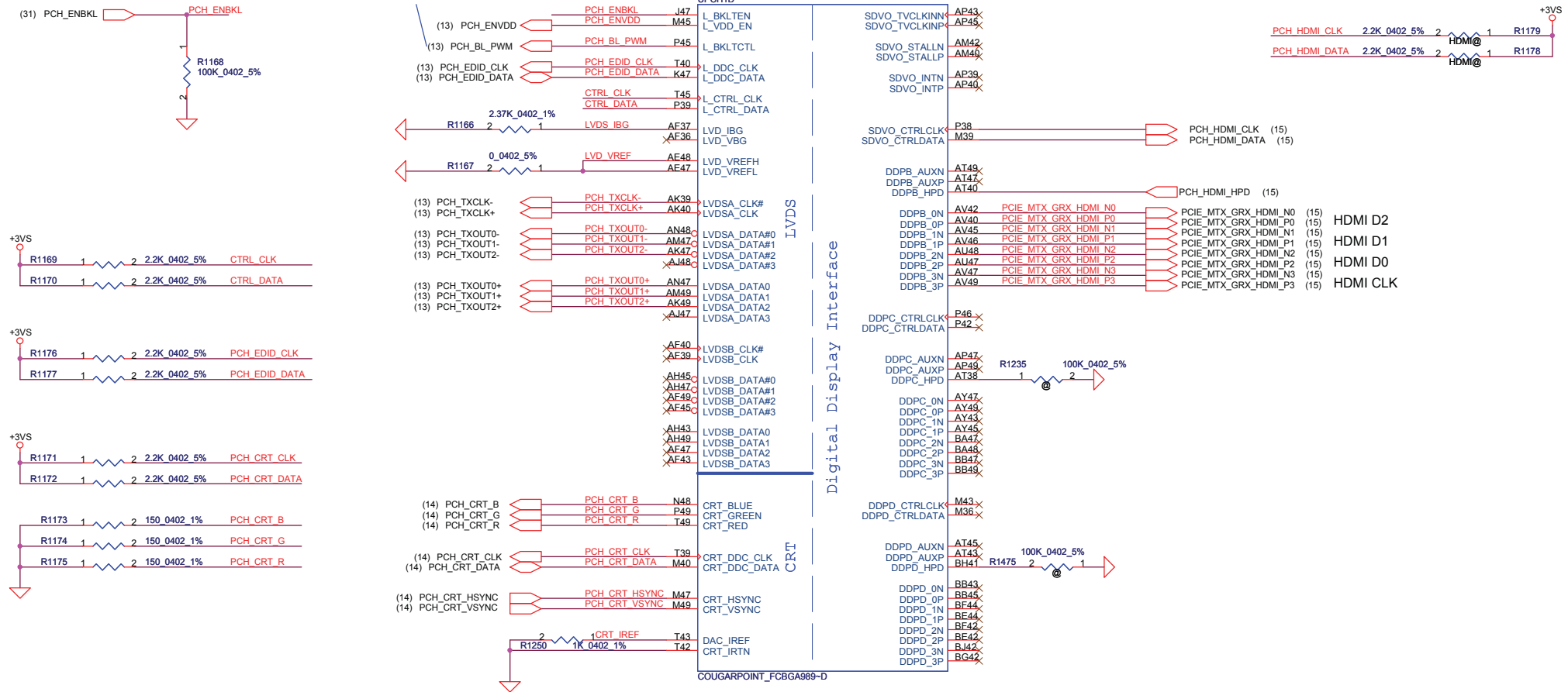
Project ID	GPIO21
★ 13"	0
14"	1



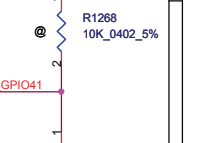
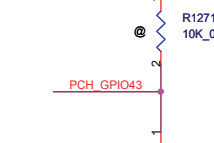
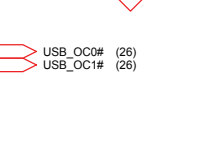
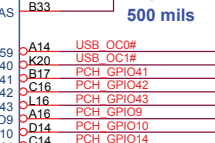
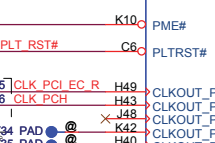
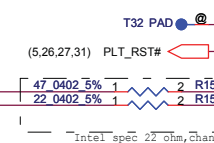
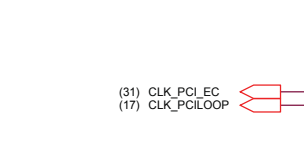
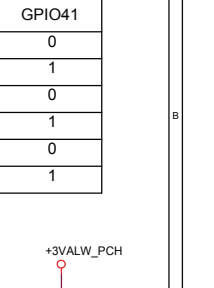
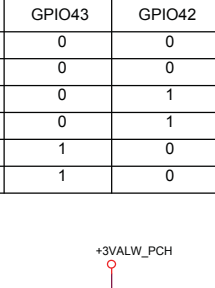
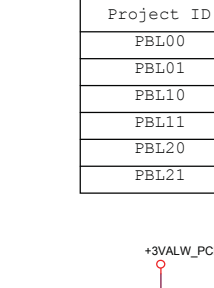
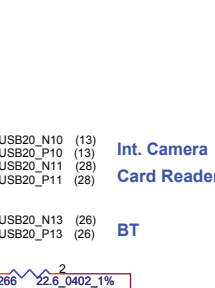
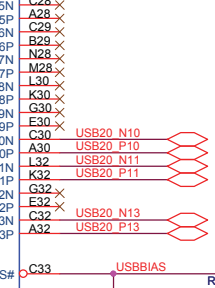
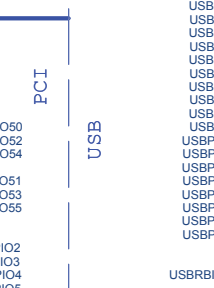
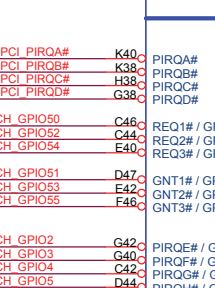
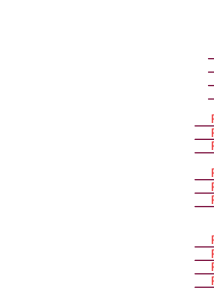
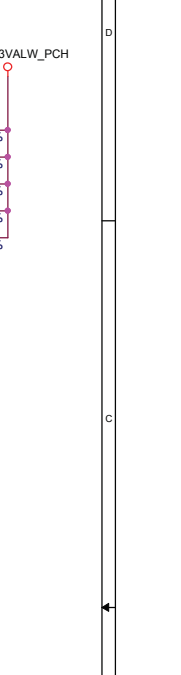
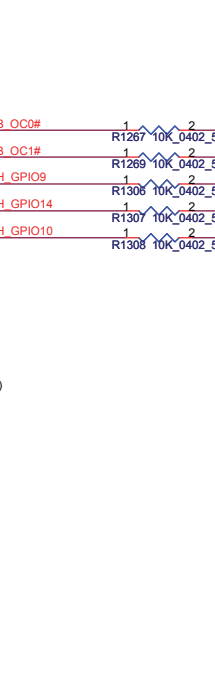
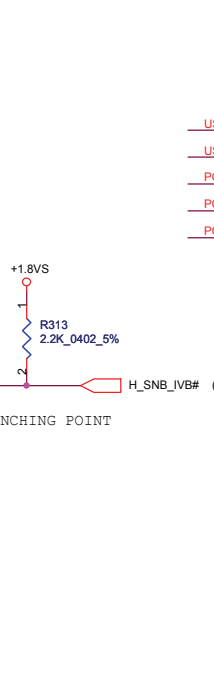
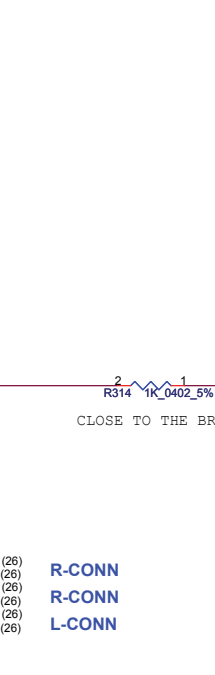
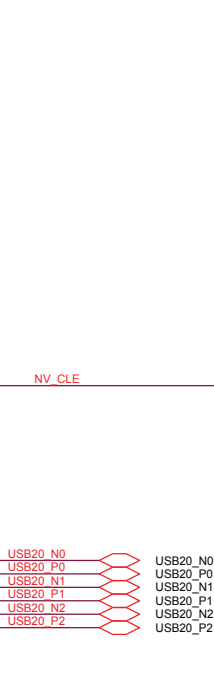
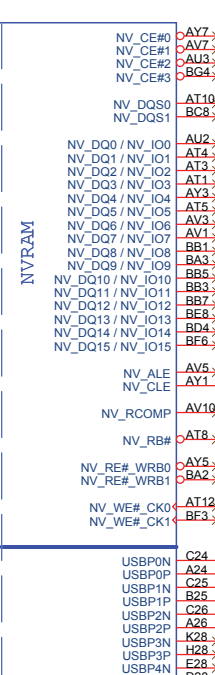
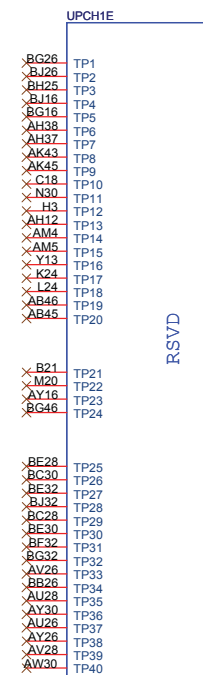
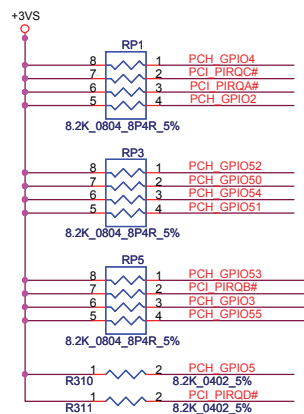
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Pull high at LVDS conn side.



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						Size Custom		Document Number	
Date:		Thursday, October 28, 2010				Sheet 19		of 44	



Boot BIOS Strap bit1 BBS1			
Bit11 Bit10		Boot BIOS Destination	
GNT1# / GPIO51	0 1	Reserved	
	1 0	PCI	
	1 1	SPI	
	0 0	LPC	

Security Classification			
Issued Date		Deciphered Date	
2010/06/10		2011/06/10	

Compal Secret Data			
Issued Date		Deciphered Date	
2010/06/10		2011/06/10	

Compal Secret Data			
Issued Date		Deciphered Date	
2010/06/10		2011/06/10	

Compal Secret Data			
Issued Date		Deciphered Date	
2010/06/10		2011/06/10	

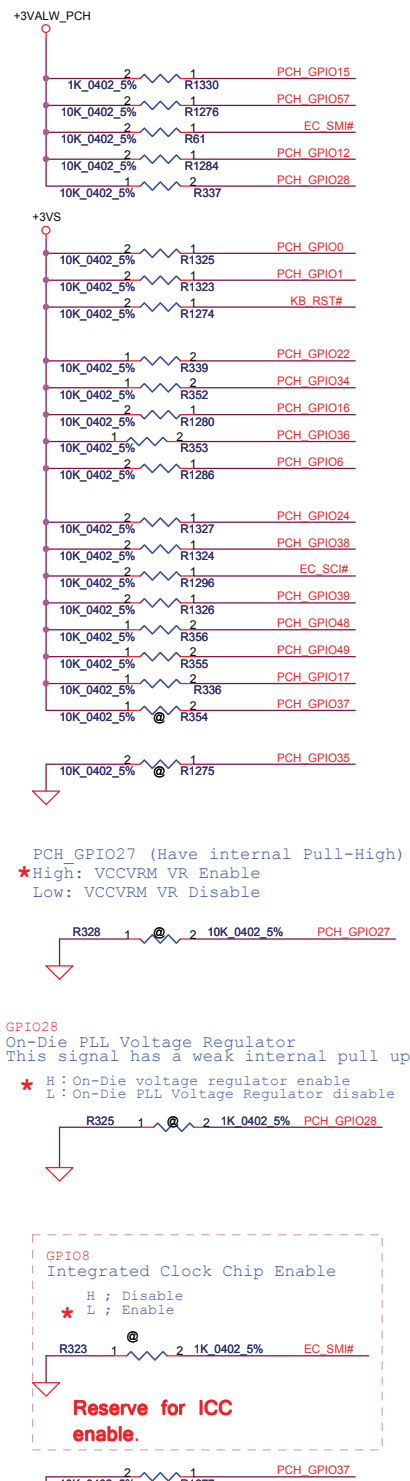
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Issued Date		Deciphered Date	
2010/06/10		2011/06/10	

Compal Secret Data			
Issued Date		Deciphered Date	
2010/06/10		2011/06/10	

Compal Secret Data			
Issued Date		Deciphered Date	
2010/06/10		2011/06/10	

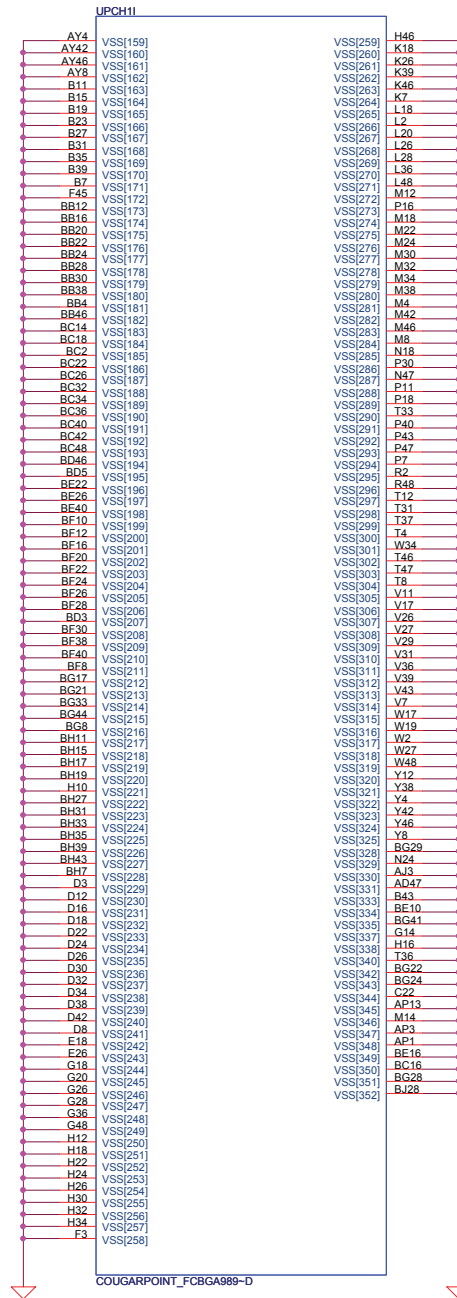
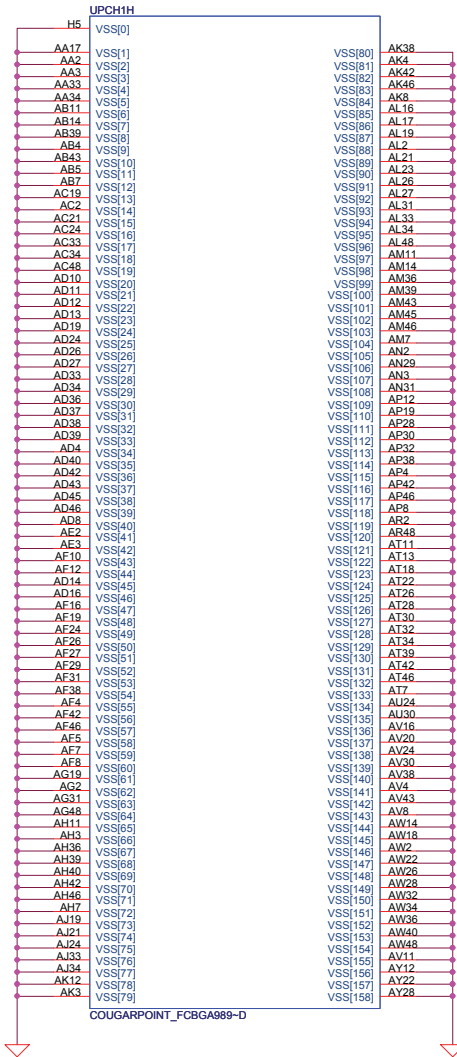
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Issued Date		Deciphered Date	
2010/06/10		2011/06/10	

Compal Secret Data			
Issued Date		Deciphered Date	
2010/06/10		2011/06/10	



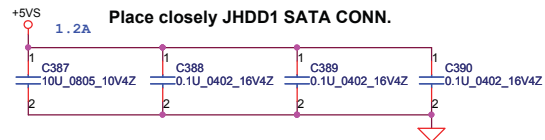
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Issued Date	2010/06/10	Deciphered Date	2011/06/10	Title	
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Size	Custom	Document Number	PBL00 LA6734P M/B	Rev	0.2
Date:	Thursday, October 28, 2010	Sheet	21	of	44



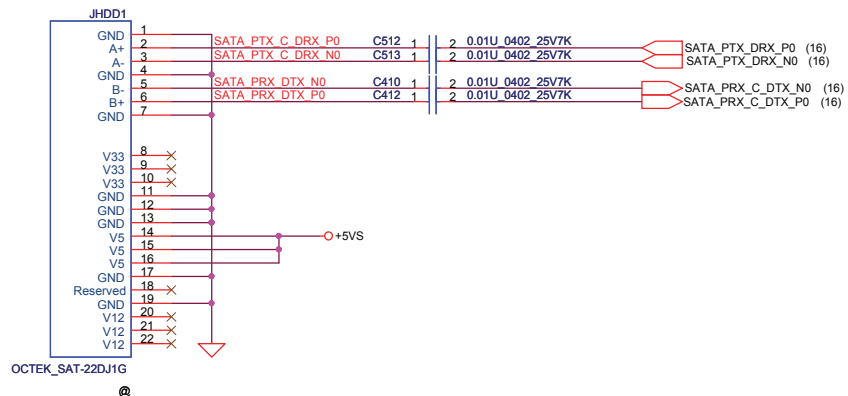


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Issued Date		2010/06/10	Deciphered Date	2011/06/10	Title		Cougar Point(9/9)-GND	
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					Custom	PBL00 LA6734P M/B	0.2	
					Date:	Tuesday, September 07, 2010	Sheet	24 of 44

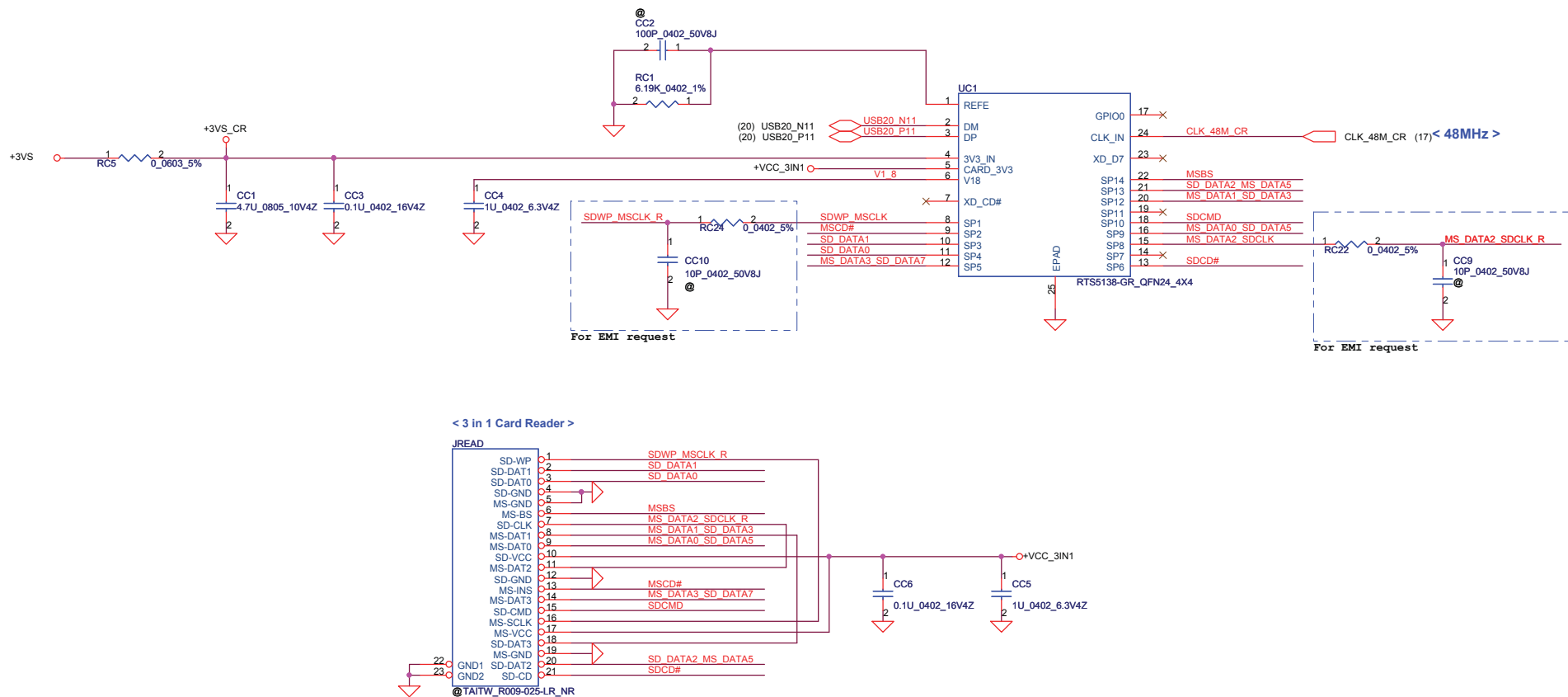
SATA HDD1 Conn.



13.3" HDD

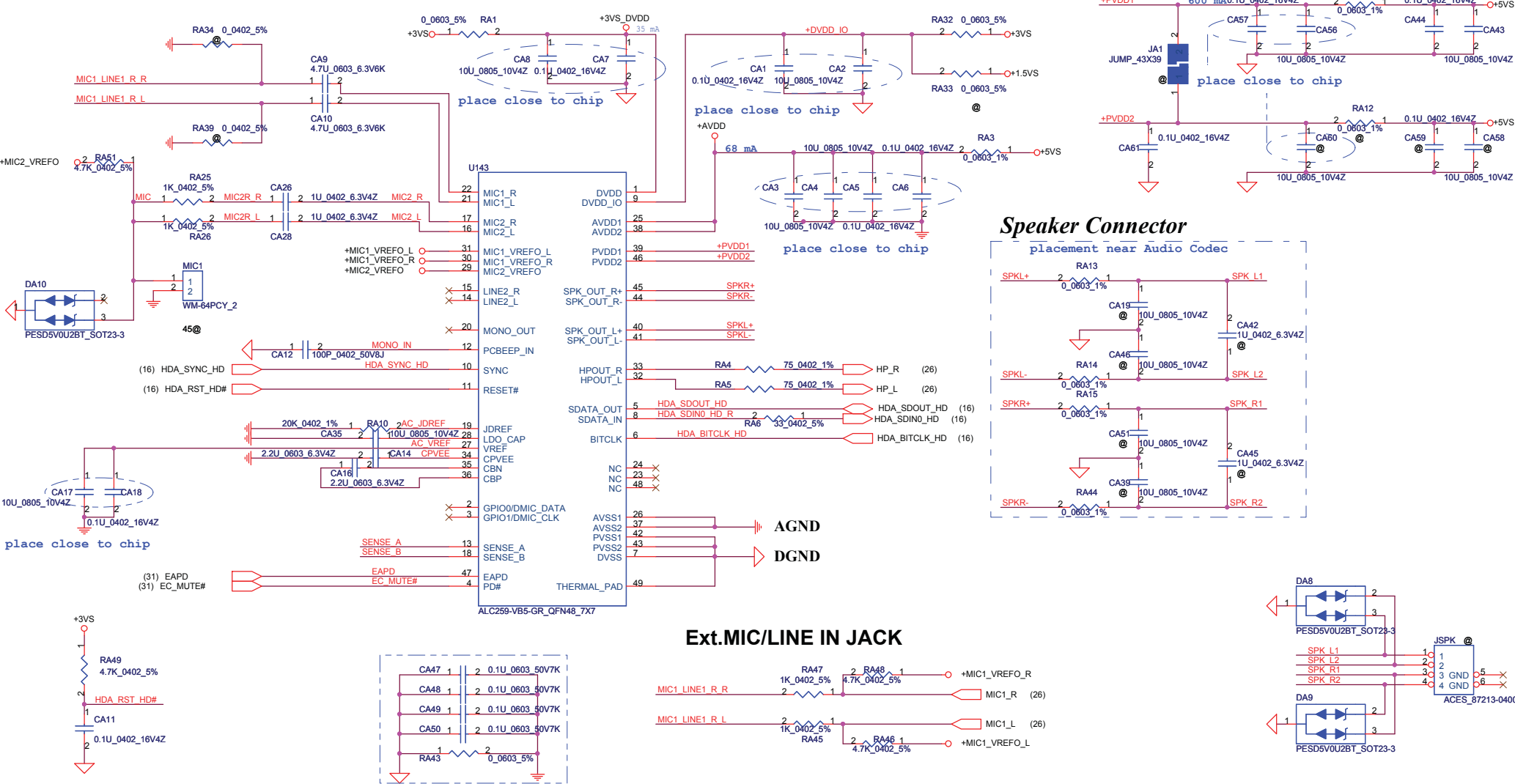


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Issued Date	2010/06/10	Deciphered Date	2011/06/10	Title	SATA-HDD
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				Date:	Thursday, October 28, 2010
				Sheet	25 of 44
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				Document Number	PBL00 LA6734P M/B

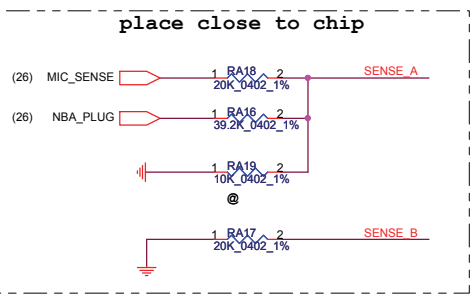


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				Size	Document Number	Rev
				PBL00 LA6734P M/B		
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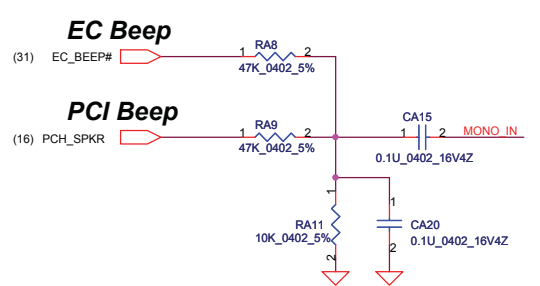
Ext. Mic/LINE IN



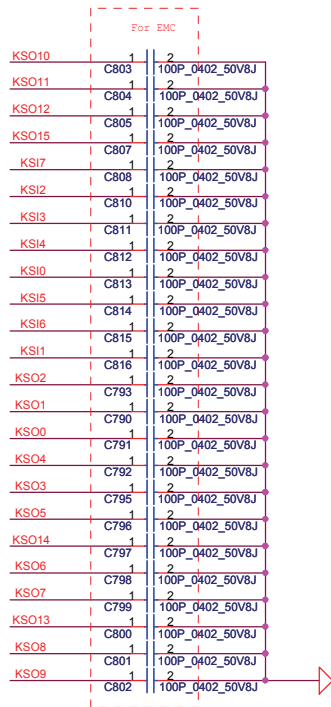
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	



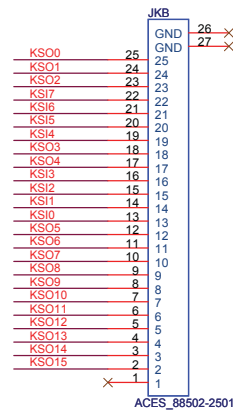
Beep sound



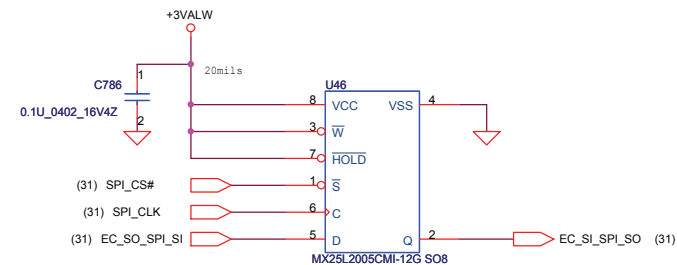
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Issued Date	2010/06/10	Deciphered Date	2011/06/10	Title	
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Size	Document Number	PBL00 LA6734P M/B		Rev 0.2	
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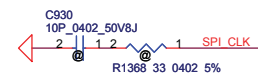
KEYBOARD CONN.



SPI Flash (1MByte*1)

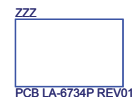


P/N : SA00003GK00 & SA00003GM10

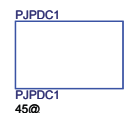


ISPD

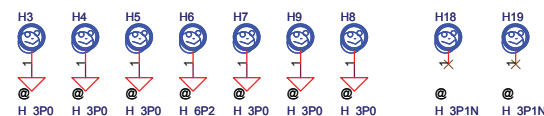
PCB



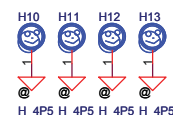
DC-IN



Screw Hole



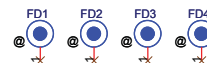
CPU



JWLAN



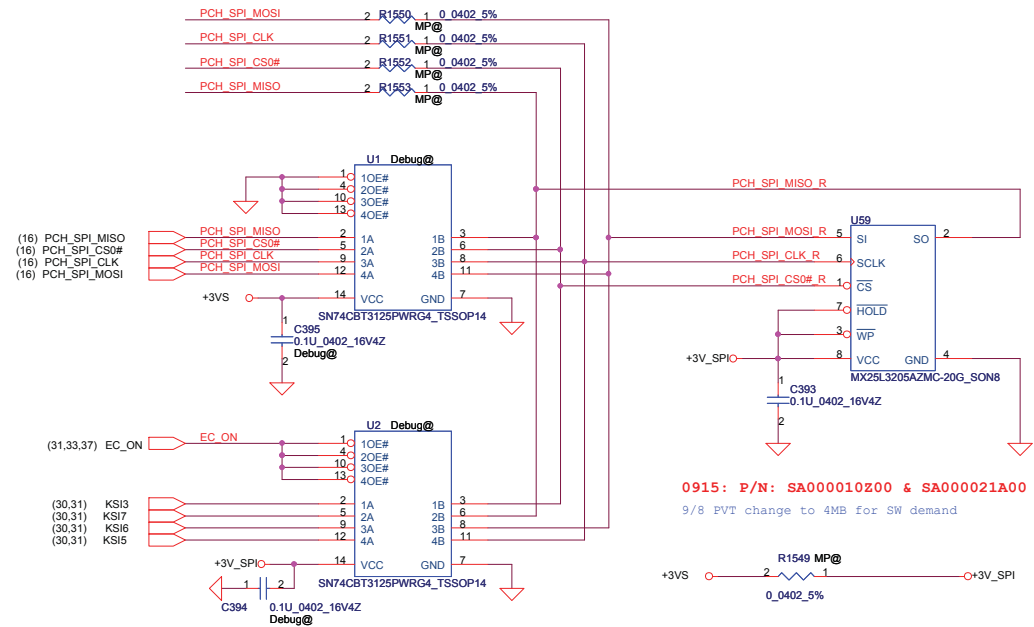
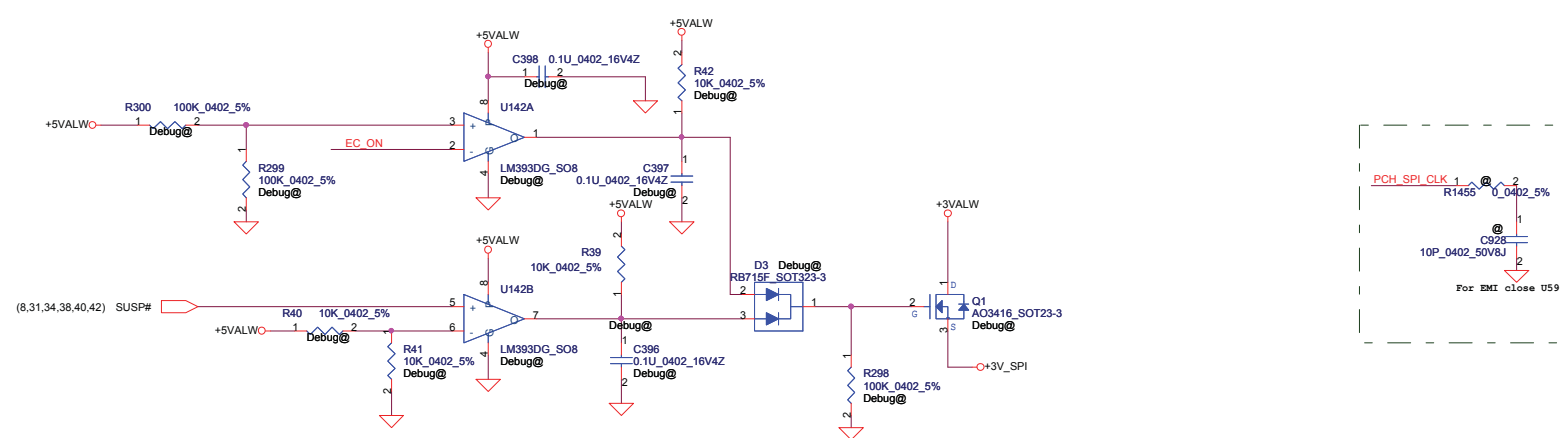
PCB Fedcal Mark PAD



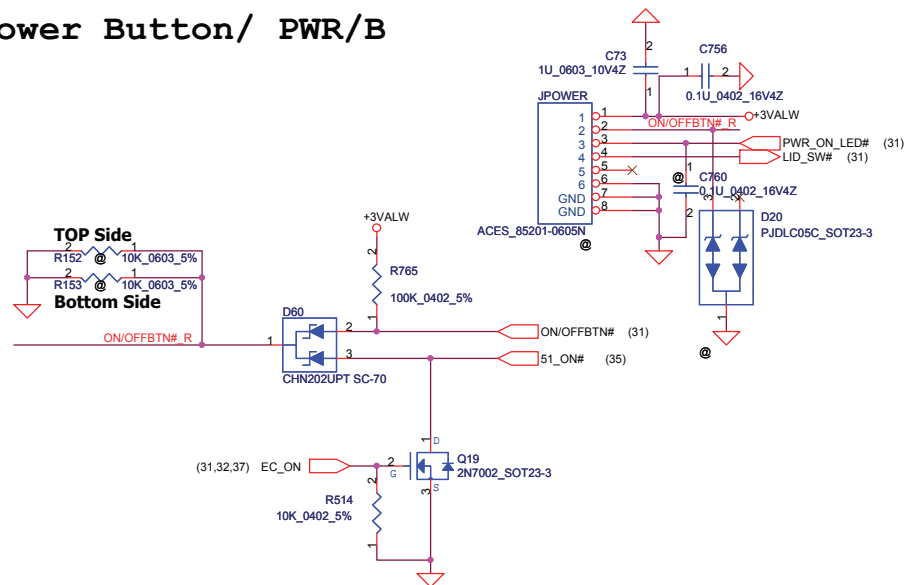
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Size		Document Number			Rev
Date:		Thursday, October 28, 2010			0.2
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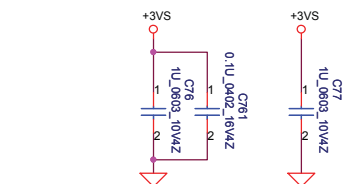
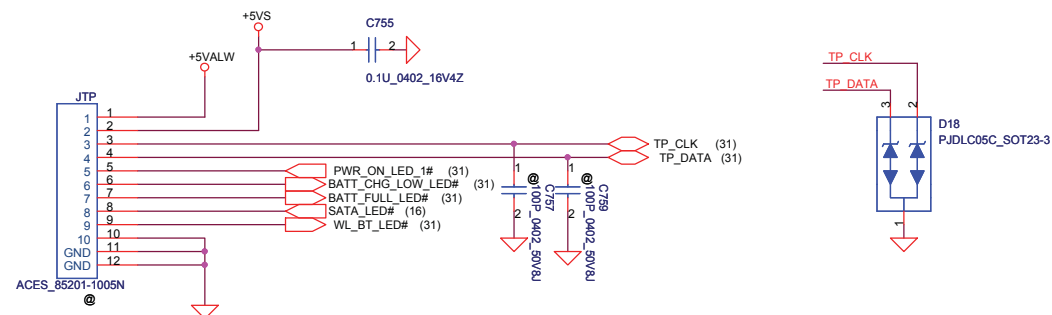
SPI ROM For Basic ME ROM size
(w/o Braidwood & system BIOS):
4MByte



Power Button/ PWR/B

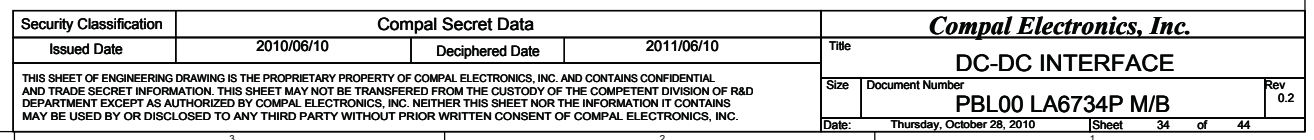


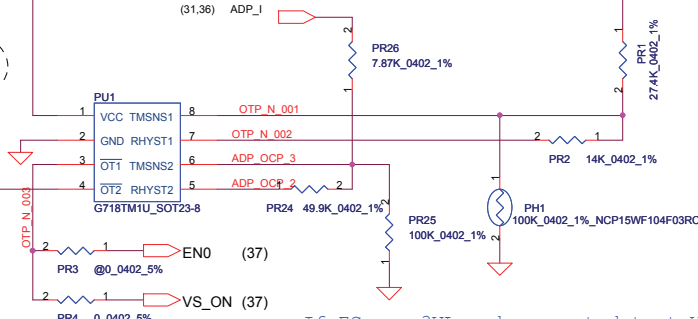
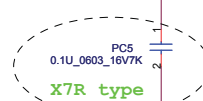
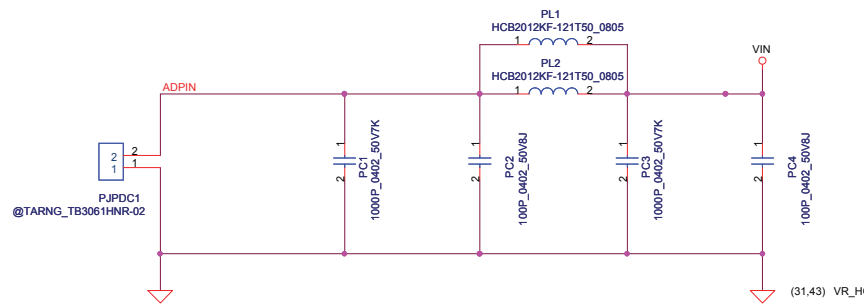
Touch/B Connector



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$V_{gs} = -0V, I_d = 9A, R_{ds} = 18.5m\Omega$

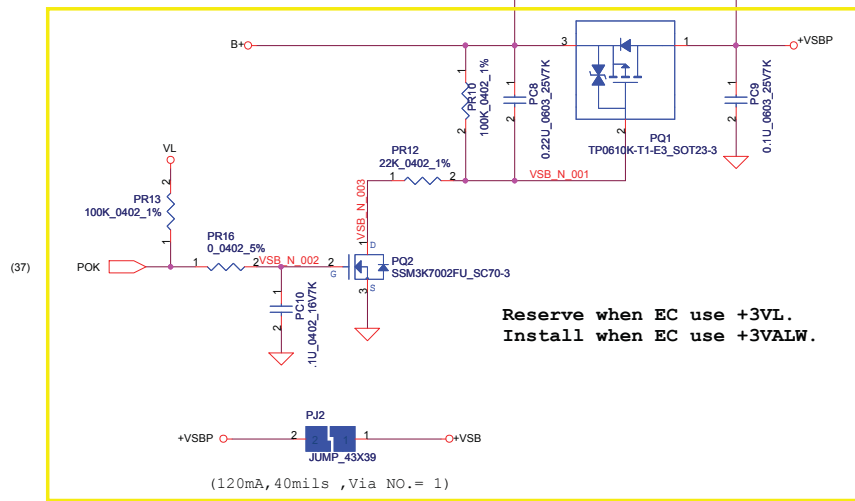
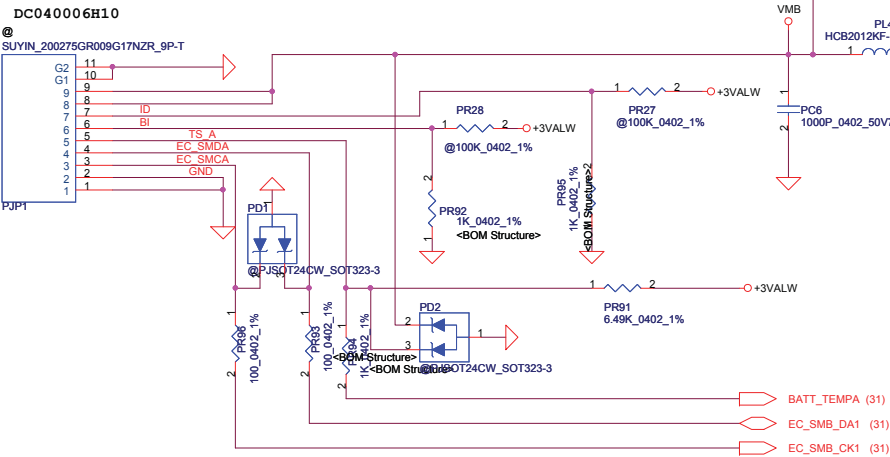




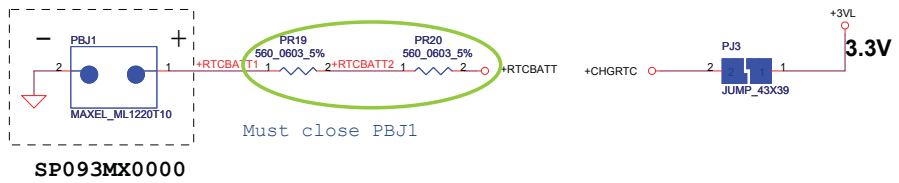
If EC use 3VL and can not detect VGATE,
must connect EN0

Install when EC use +3VL
and SUSP was Pull high to +3VL.

Reserve when EC use +3VALW.



RTC Battery

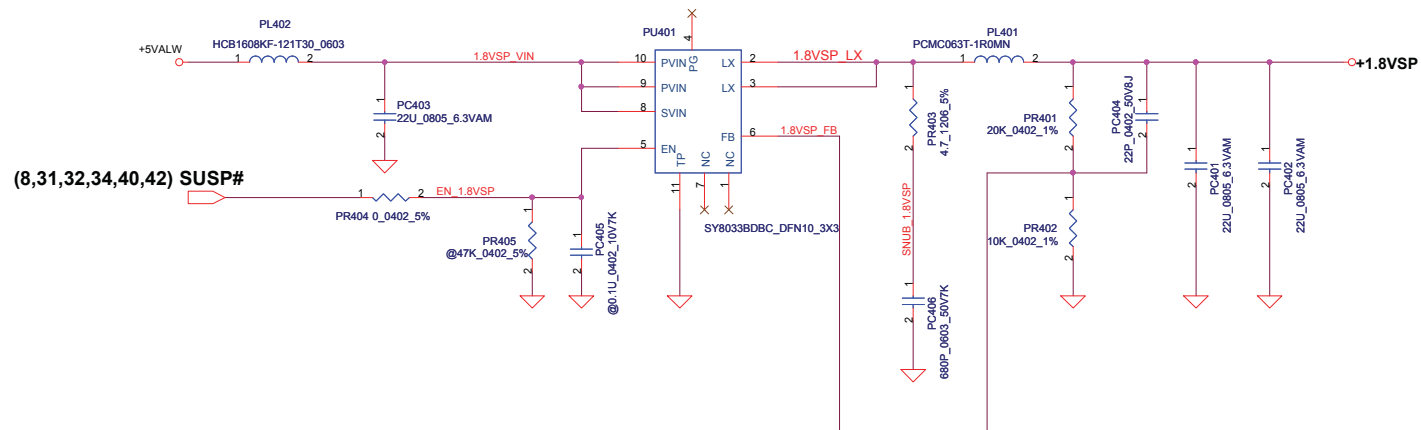


SP093MX0000

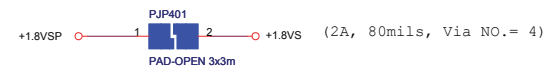
Reserve when EC use +3VL.
Install when EC use +3VALW.

Reserve when EC use +3VL.
Install when EC use +3VALW.

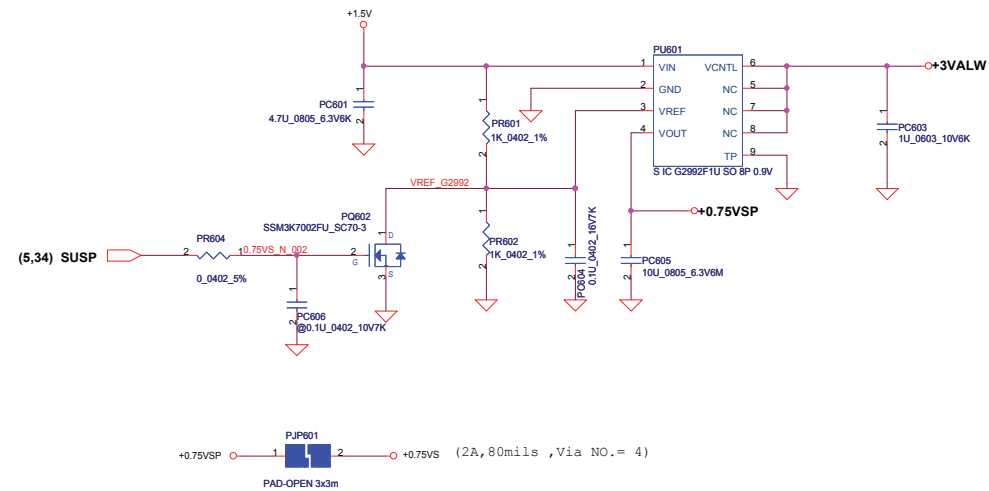
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Size		Document Number		PBL01 LA6733P M/B	
Date		Thursday, October 28, 2010		Sheet	35 of 44



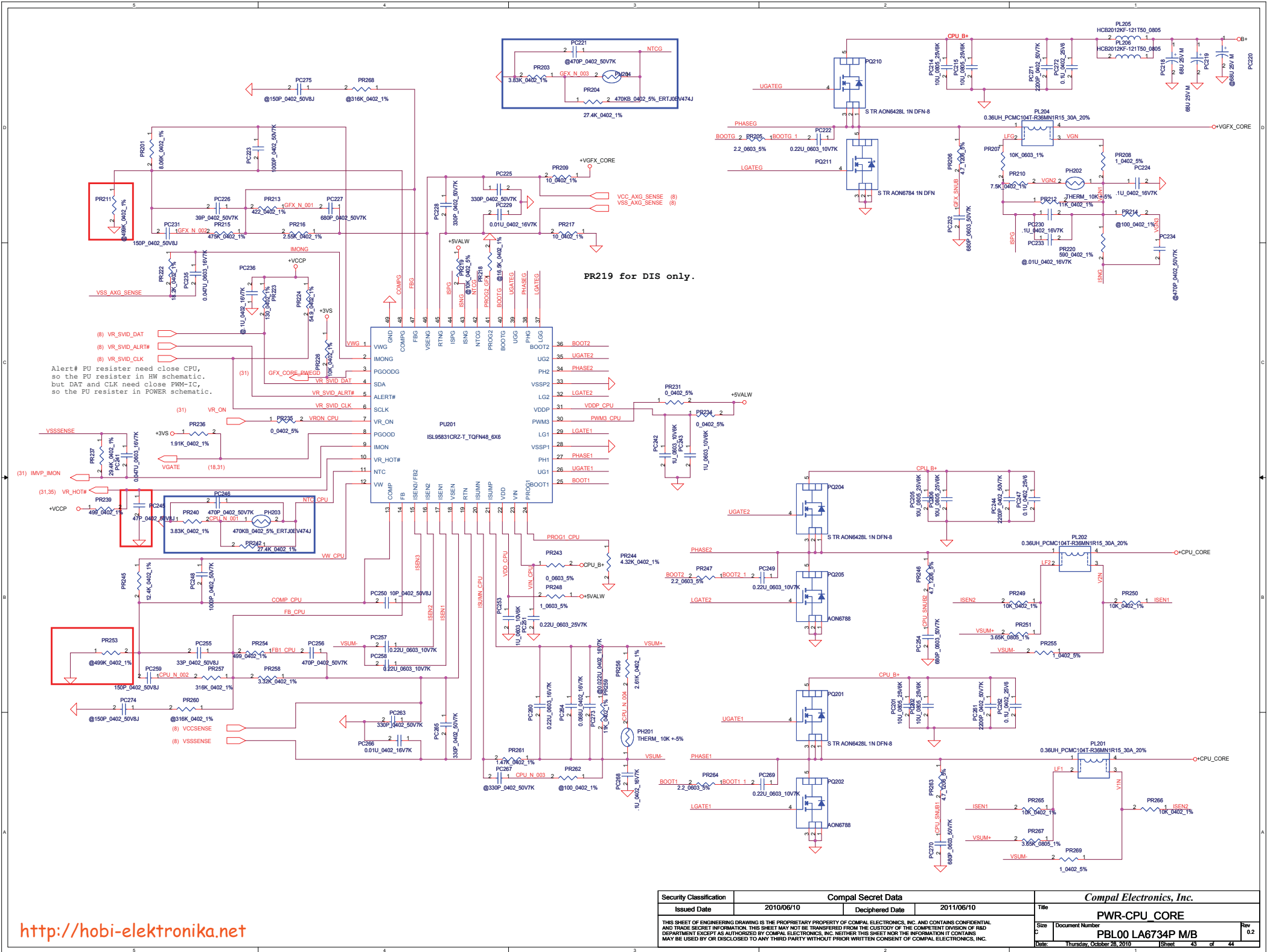
$$\begin{aligned} <V_o=1.8V> \quad V_{FB}=0.6V \\ V_o=V_{FB} * (1+PR401/PR402)=0.6 * (1+20K/10K)=1.8V \end{aligned}$$



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Revision Change: 0.1 to 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	08/12	All	Remove all components about UMA@	From UMA/DIS schematic to DIS only
2	08/12	41	Change RA16 from 5.1K to 39.2K & connect from SENSE_B to SENSE_A	Headphone out can't detect issue
3	08/12	46	Change USB30 from TI to NEC	SPEC request
4	08/12	27	Delet U37 and relate schematic. Q16,i connect to HDMI connector directly. R570 from 100K to 20K	HDMI Hot Plug issue
5	08/24	41	Change RA9,RA10 to 4.7U	For Audio Precision
6	08/24	29	Change CLKREQ_USB30# Pull-hi from +3VS to +3VALW_PCH	Vendor request
7	08/25	43	Mount R1368 and C930	EMI request
8	08/25	28,29,32	Change R101,R258, and R1545 to 47ohm	EMI request
9	08/25	5	Add R15 between PLT_RST# to U3	EMI request
10	08/25	25	Change C399 to 1U_0603	EMI request
11	08/25	45	Add C760	EMI request
12	08/26	10	Remove C80	DFB issue
13	08/26	45	Change CT31 footprint to B2	DFB issue
14	08/31	45	Add C73,C76,C77, and C761	EMI issue
15	09/01	14	Remove RV33,RV34	ME issue
16	09/02	41	Reserve C931 and R1370	EMI request
17	09/02	43	Remove C208	EMI request

Revision Change: 0.2 to 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	10/08	28	Add R1569	Power consumption
2	10/20	43	Add R725 and pull high +3VALW	For common design
3	10/20	46	Remove DT1	For cost down
4	10/20	27	Remove D17	For cost down
5	10/22	39	Reserve D22, D23	EMI request