

Compal Confidential

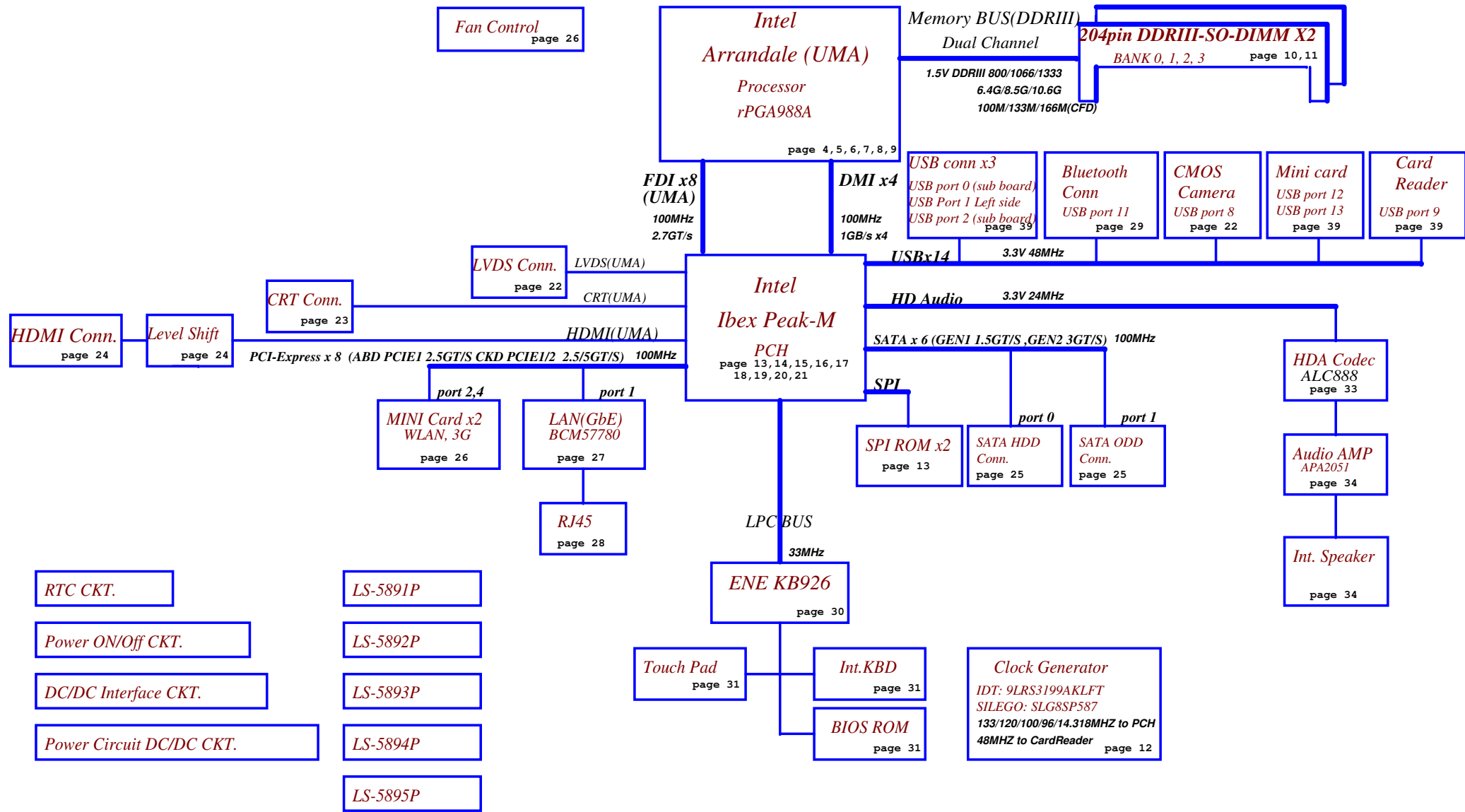
NEW70 / 80 / 90 / 50 <LA-5892P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2010-01-21

REV: 1.0

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Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Project ID / Board ID Table for EC-AD channel

Vcc	3.3V +/- 5%						
Ra/Rc	100K +/- 5%						
	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max	Board ID	Project ID	
0	0	0 V	0 V	0 V	0.1	NEW70	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2	NEW80	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	0.3	NEW90	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	1.0		
4	56K +/- 5%	1.036 V	1.185 V	1.264 V			
5	100K +/- 5%	1.453 V	1.650 V	1.759 V			
6	200K +/- 5%	1.935 V	2.200 V	2.341 V			
7	NC	2.500 V	3.300 V	3.300 V			

Not Used

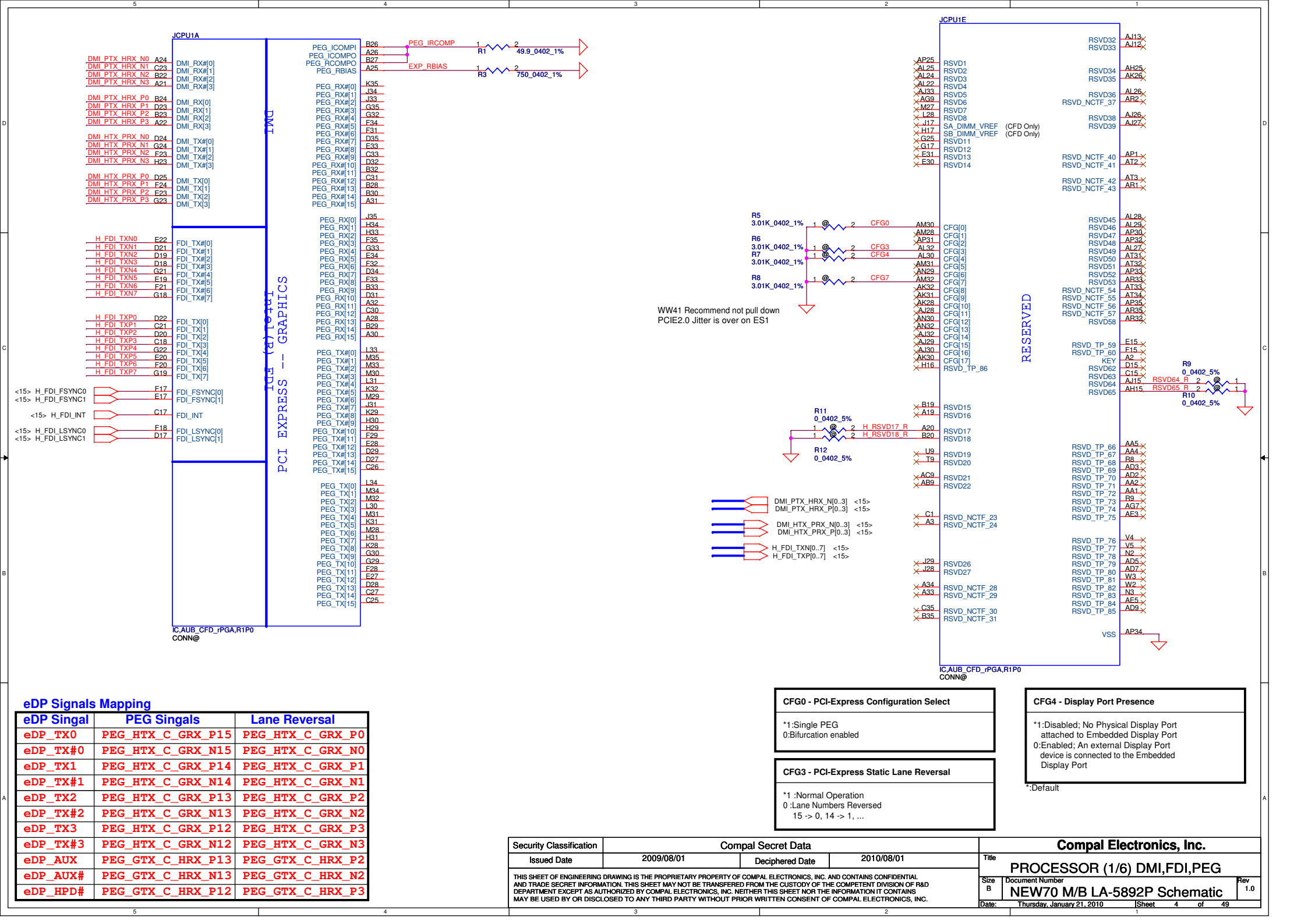
BTO Item	BOM Structure
HDMI	HDMI@
3G	3G@
9050@	NEW90 / NEW50
7080@	NEW70 / NEW80

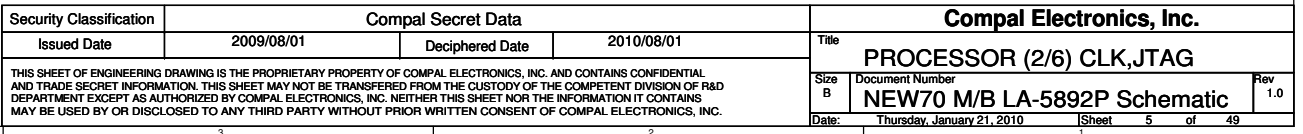
BOM Config

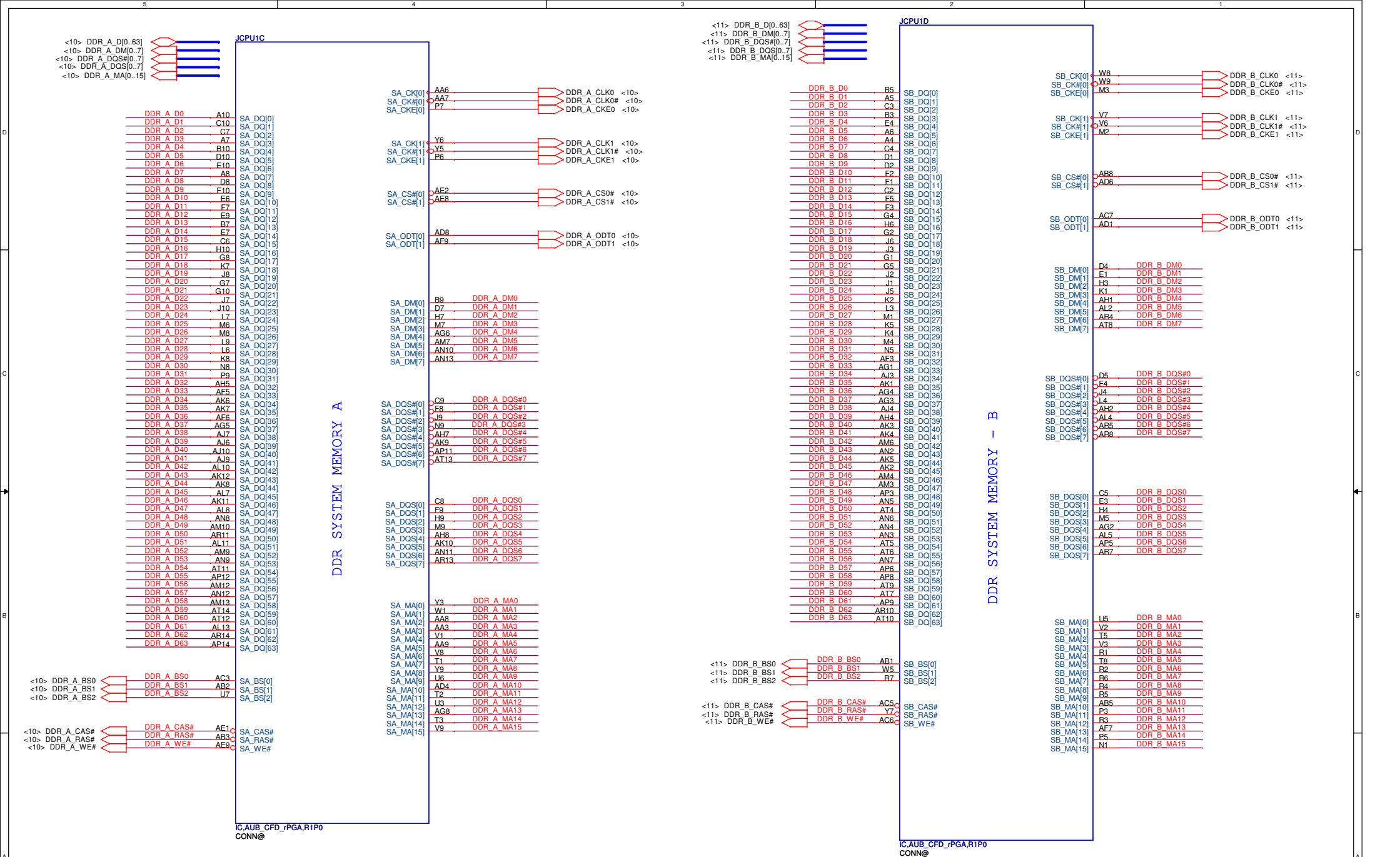
USB Port Table

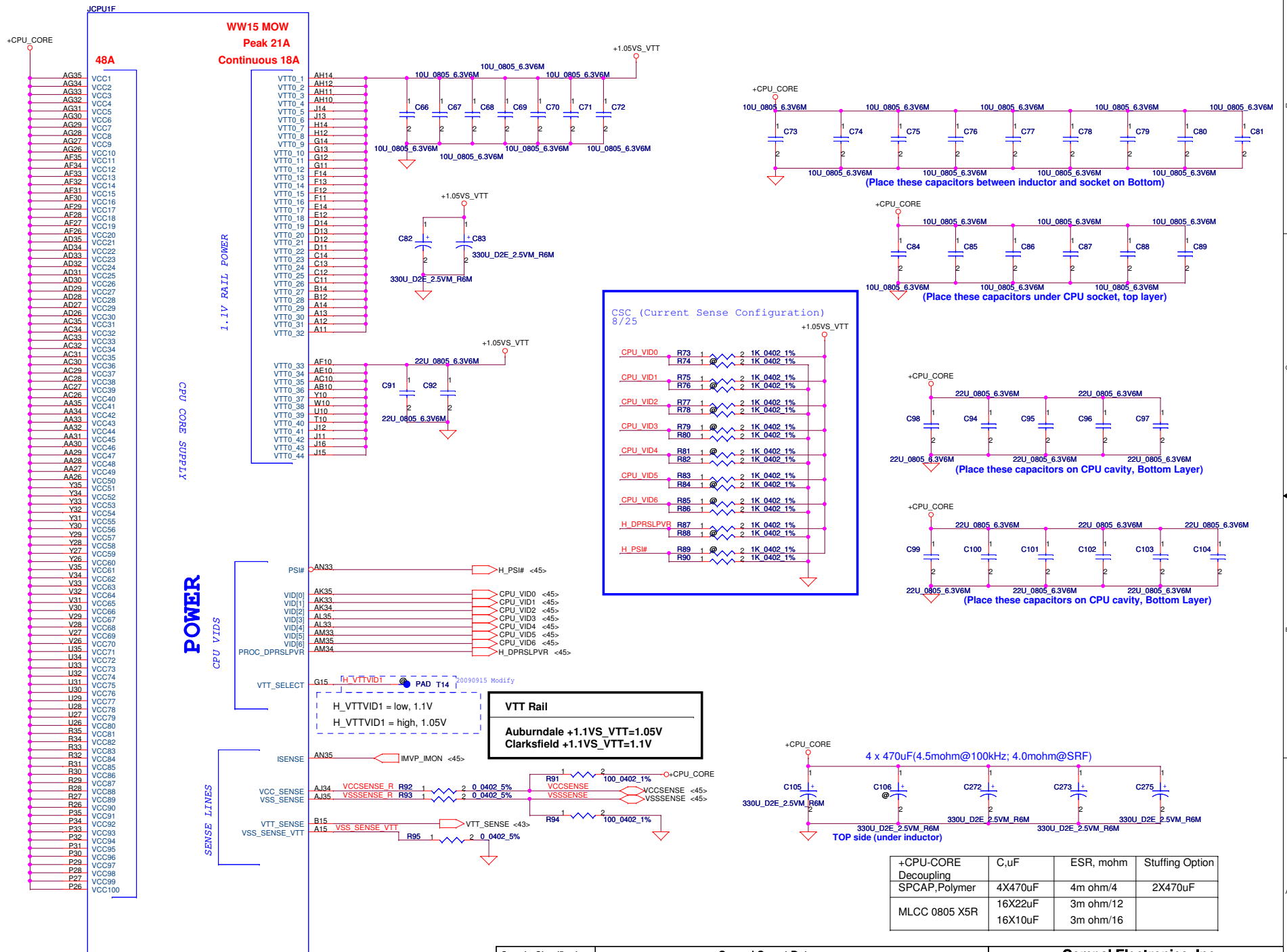
USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 USB	Ext1 USB
		1	Ext3 HS USB	Ext3 HS USB
		2	Ext2 USB	Ext2 USB
	UHCI1	3		
		4		
	UHCI2	5		
		6		
EHCI2	UHCI3	7		
		8	Camera	Camera
		9	Card Reader	Card Reader
	UHCI5	10	SIM CARD	SIM CARD
		11	Blue Tooth	Blue Tooth
	UHCI6	12	1st Min-Card	1st Min-Card
		13	2st Min-Card	2st Min-Card

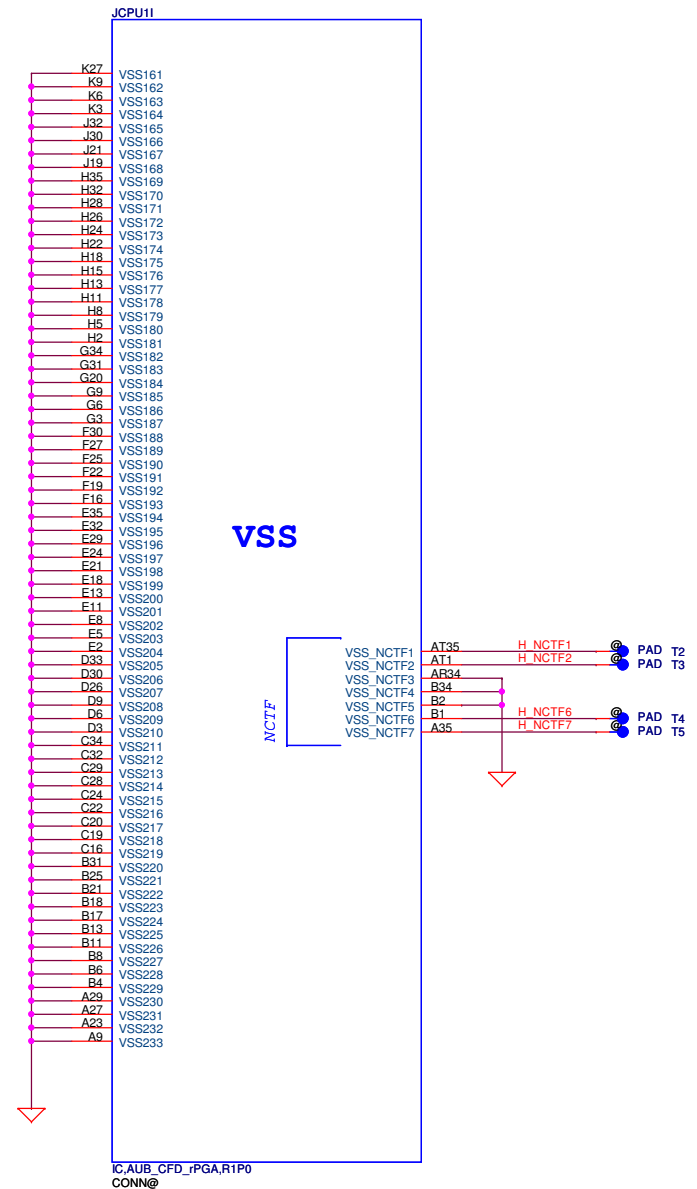
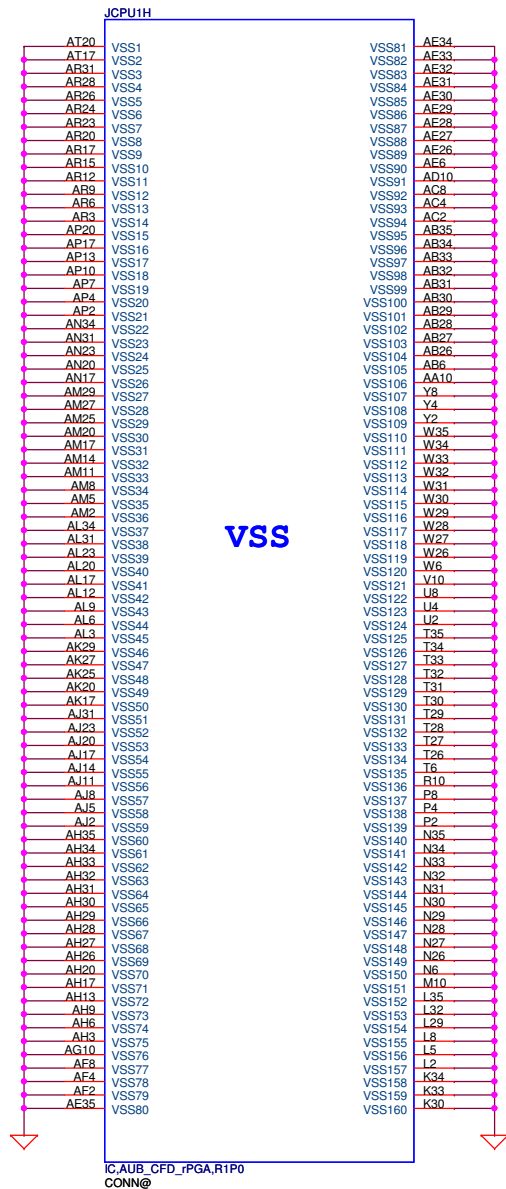
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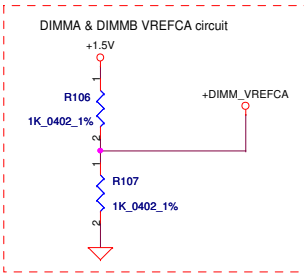
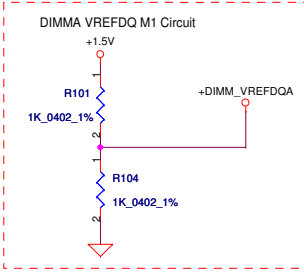




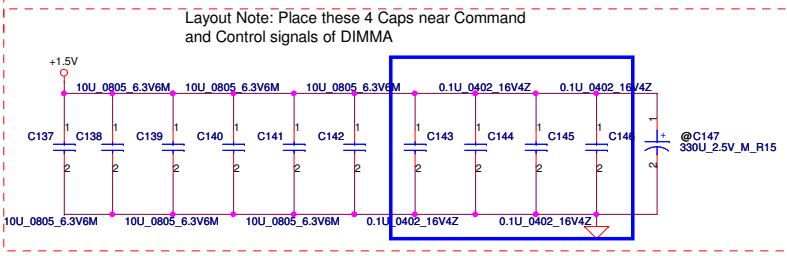




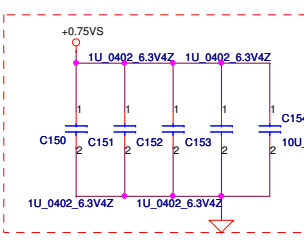
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						Size		Document Number		NEW70 M/B LA-5892P Schematic		Rev 1.0	
						Customer							
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Layout Note:
Place near JDIMM1

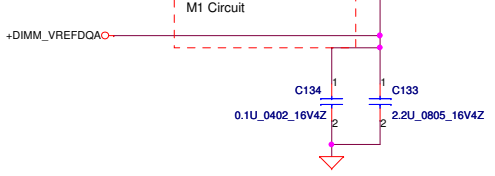
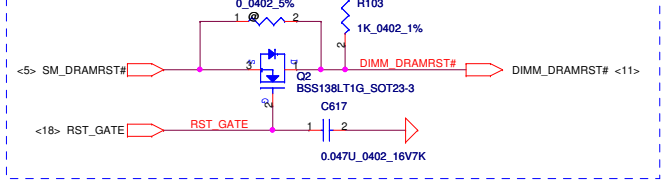


Layout Note:
Place near JDIMM1.203 & JDIMM1.204



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<6> DDR_A_D[0..63]
<6> DDR_A_DM[0..7]
<6> DDR_A_DQS[0..7]
<6> DDR_A_MA[0..15]

#425302
CP_S3PowerReduction
WhitePaper_Rev1.0



<6> DDR_A_CKE0
<6> DDR_A_BS2
<6> DDR_A_BS0
<6> DDR_A_WE#
<6> DDR_A_CAS#
<6> DDR_A_CS1#

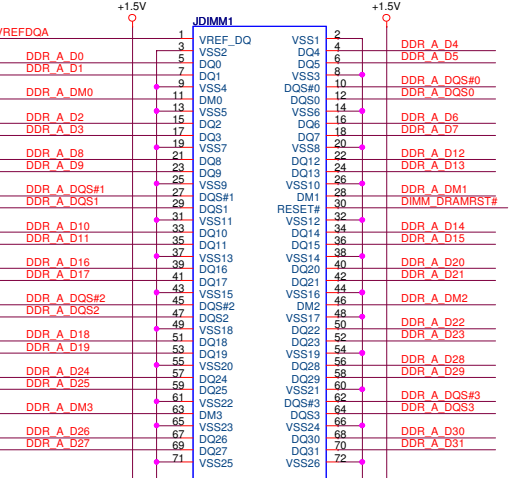
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DDR A D33
DDR A D34
DDR A D35
DDR A D40
DDR A D41
DDR A D42
DDR A D43
DDR A D48
DDR A D49
DDR A D50
DDR A D51
DDR A D56
DDR A D57
DDR A D58
DDR A D59

DDR A D60
DDR A D61
DDR A D62
DDR A D63
DDR A D64
DDR A D65
DDR A D66
DDR A D67
DDR A D68
DDR A D69

DDR A D70
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DDR A D72
DDR A D73
DDR A D74
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DDR A D78
DDR A D79

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DDR A D85
DDR A D86
DDR A D87
DDR A D88
DDR A D89

DDR A D90
DDR A D91
DDR A D92
DDR A D93
DDR A D94
DDR A D95
DDR A D96
DDR A D97
DDR A D98
DDR A D99



DDR A CKE0
DDR A BS2
DDR A BS0
DDR A WE#
DDR A CAS#
DDR A CS1#

DDR A D32
DDR A D33
DDR A D34
DDR A D35
DDR A D40
DDR A D41
DDR A D42
DDR A D43
DDR A D48
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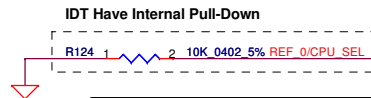
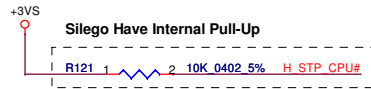
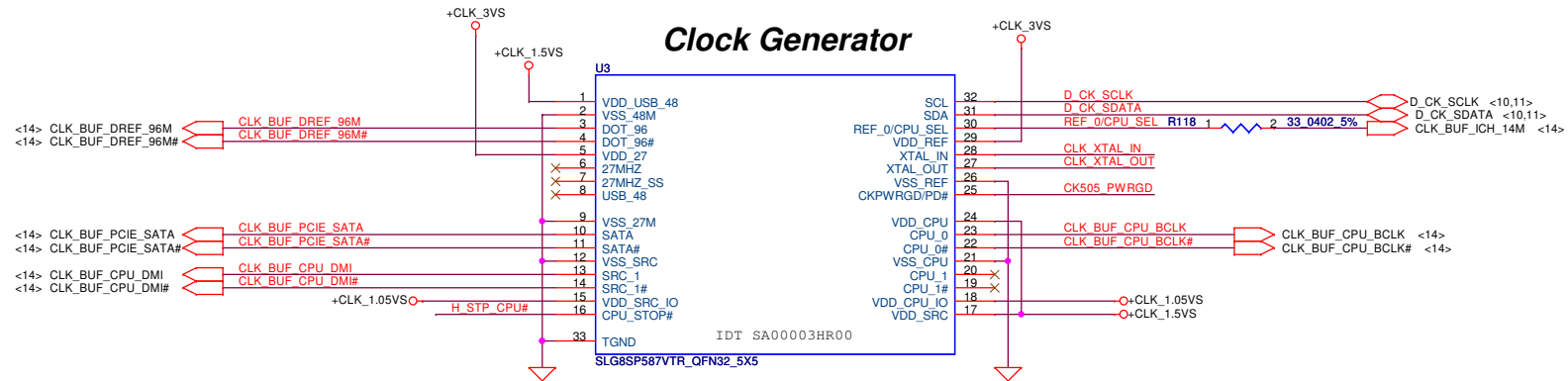
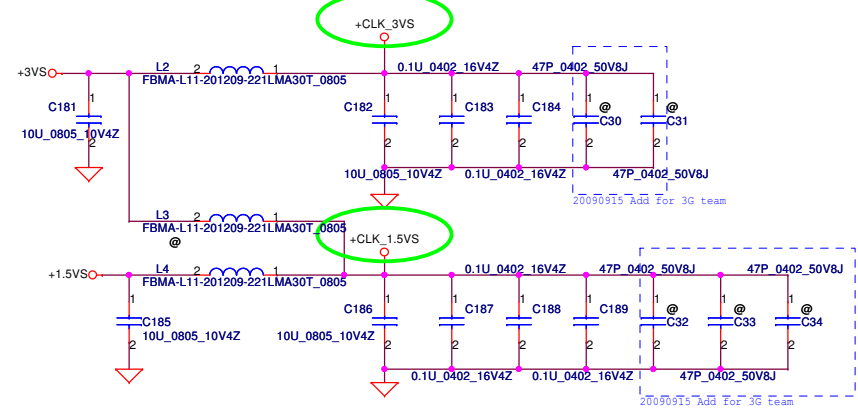
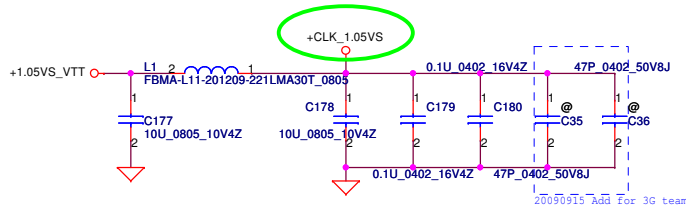
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DDR A D92
DDR A D93
DDR A D94
DDR A D95
DDR A D96
DDR A D97
DDR A D98
DDR A D99

DDR3 SO-DIMM A
Change to Reverse Type
8mm High

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DDRIII-SODIMM SLOT1

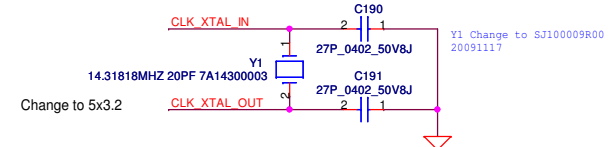
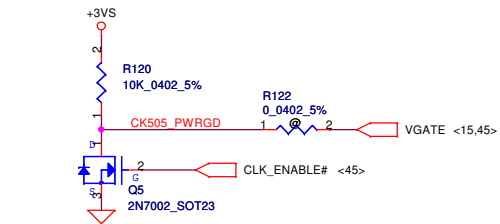
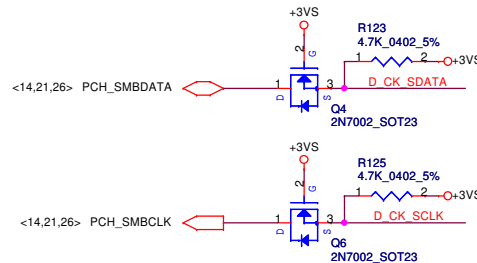
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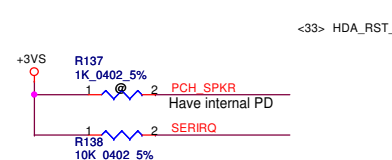
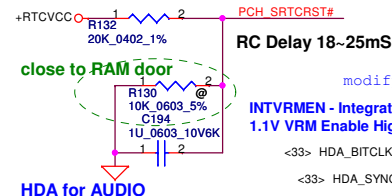
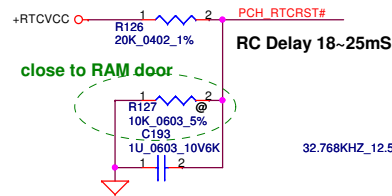
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

IDT: 9LRS3199AKLFT, SA000030P00
 SILEGO: SLG8SP587V(WF), SA00002XY10
 Low Power:
 IDT: 9LVS3199AKLFT, SA00003HR00
 Realtek: RTM890N-631-GRT, SA00003HQ00



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						Size		Document Number		NEW70 M/B LA-5892P Schematic		Rev 1.0	
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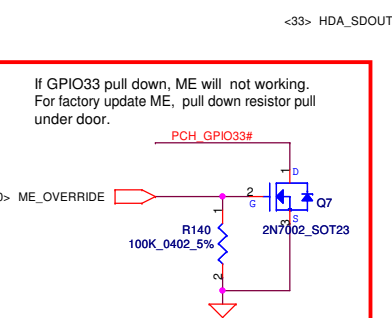
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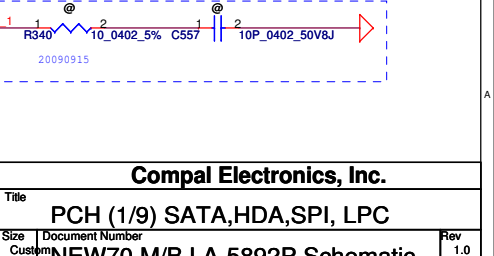
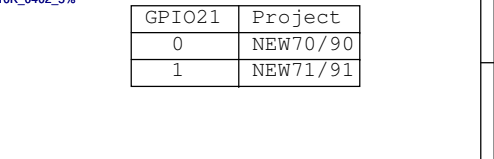
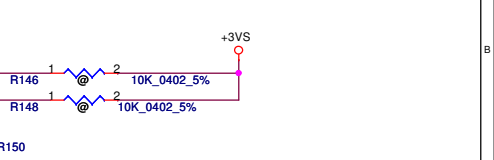
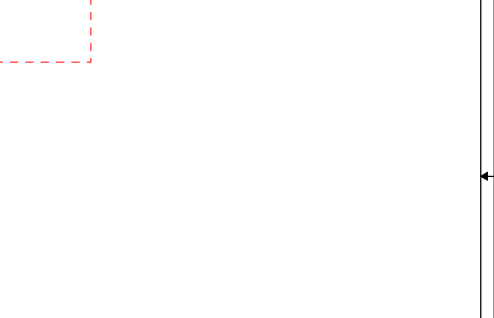
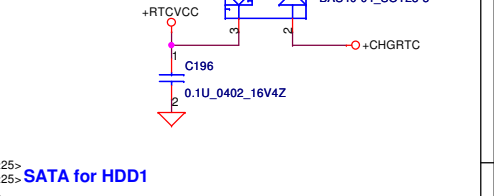
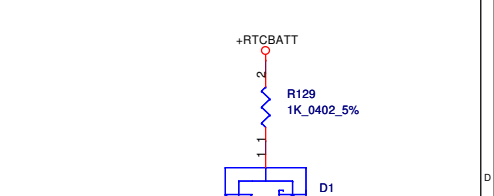
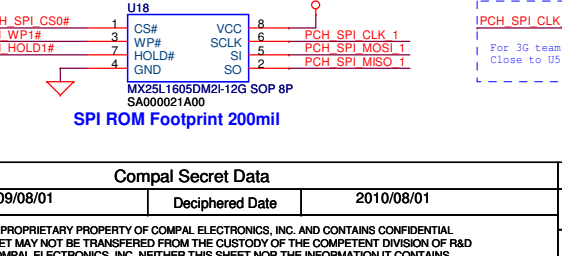
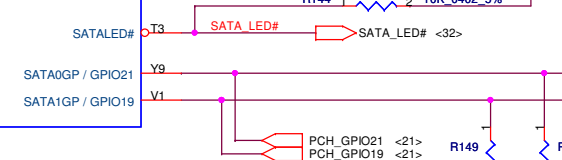
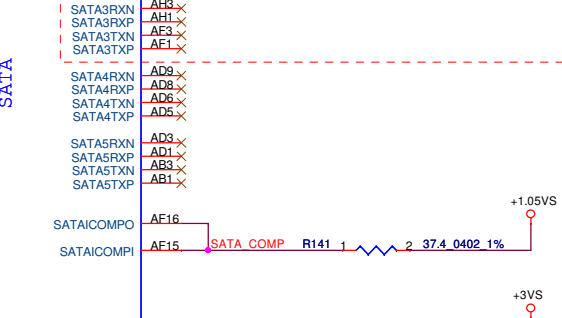
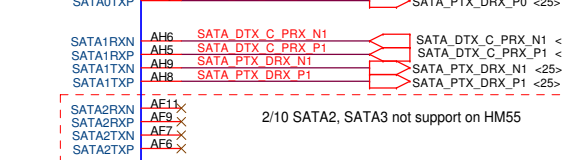
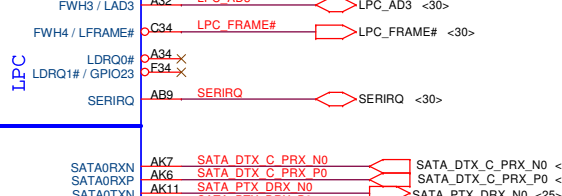
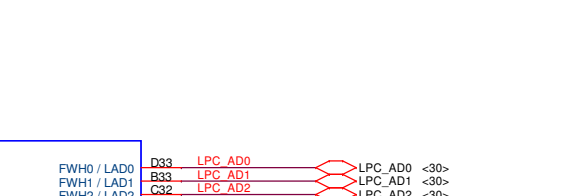
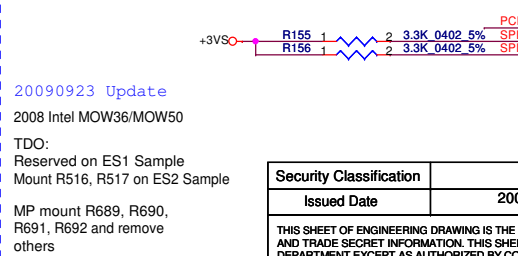
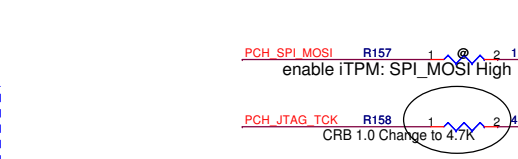
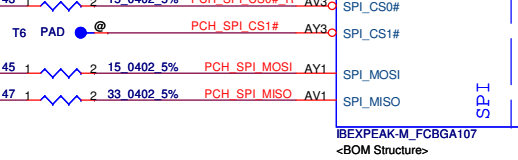
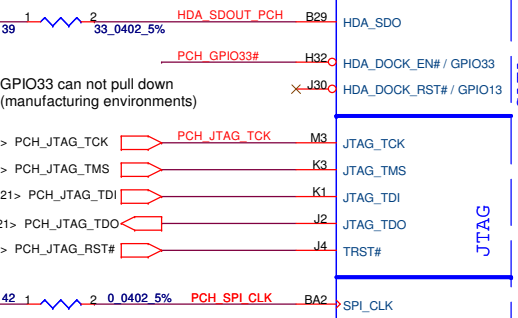
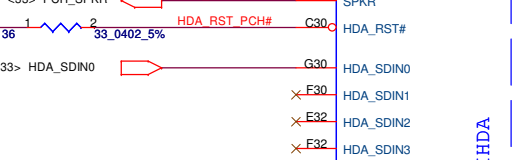
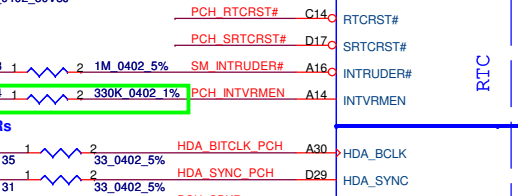
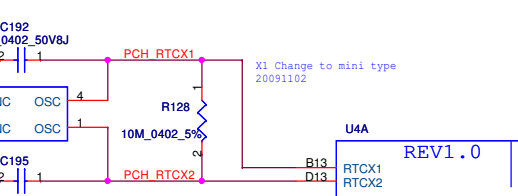
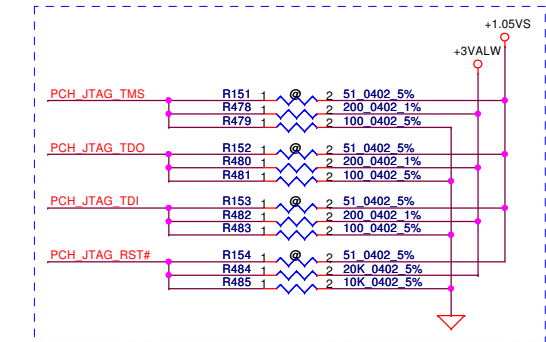
If GPIO33 pull down, ME will not working. For factory update ME, pull down resistor pull under door.

<30> ME_OVERRIDE

GPIO33 has a weak internal pull-up
NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.



GPIO33 has a weak internal pull-up
NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.



20090923 Update

2008 Intel MOW36/MOW50

TDO:
Reserved on ES1 Sample
Mount R516, R517 on ES2 Sample

MP mount R689, R690,
R691, R692 and remove
others

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title				
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				Size	Document Number			Rev
				Custom	NEW70 M/B LA-5892P Schematic			1.0
				Date:	Thursday, January 21, 2010	Sheet 13 of 49		

For PCIE LAN

For Wireless LAN

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<26> PCIE_PTX_C_DRX_N2
<26> PCIE_PTX_C_DRX_P2

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PCIE_DTX_C_PRX_P1 BJ30
PCIE_PTX_DRX_N1 BF29
PCIE_PTX_DRX_P1 BH29

PCIE_DTX_C_PRX_N2 AW30
PCIE_DTX_C_PRX_P2 BA30
PCIE_PTX_DRX_N2 BC30
PCIE_PTX_DRX_P2 BD30

U4B

REV1.0

PCI-E*

Controller

Link

PEG

From CLK BUFFER

Clock Flex

2/10 PCIE7, PCIE8 not support on HM55

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PCH_SMBDATA R181 1 2 2.2K 0402 5%

PCH_GPIO60 R182 1 2 10K 0402 5%
PCH_SML1CLK R183 1 2 2.2K 0402 5%
PCH_SML1DAT R184 1 2 2.2K 0402 5%

PCH_GPIO74 R185 1 2 10K 0402 5%

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PCH_GPIO56 R188 1 2 10K 0402 5%
PCH_GPIO73 R189 1 2 10K 0402 5%

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PCH_GPIO56 R188 1 2 10K 0402 5%
PCH_GPIO73 R189 1 2 10K 0402 5%

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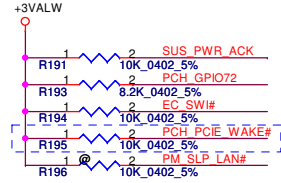
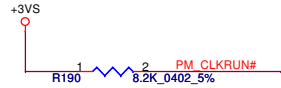
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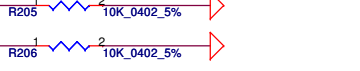
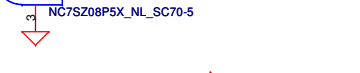
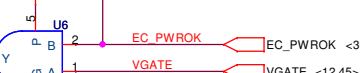
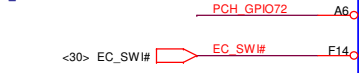
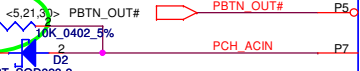
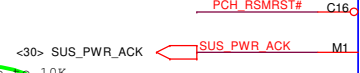
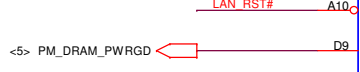
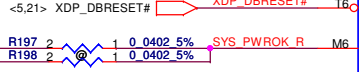
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R195 Change to 10K for W37
20090916



No used Integrated LAN,
connecting LAN_RST# to GND

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DMI HTX PRX N1 BJ22
DMI HTX PRX N2 AW20
DMI HTX PRX N3 BJ20
DMI HTX PRX P0 BD24
DMI HTX PRX P1 BG22
DMI HTX PRX P2 BA20
DMI HTX PRX P3 BG20
DMI PTX HRX N0 BE22
DMI PTX HRX N1 BF21
DMI PTX HRX N2 BD20
DMI PTX HRX N3 BE18
DMI PTX HRX P0 BD22
DMI PTX HRX P1 BH21
DMI PTX HRX P2 BC20
DMI PTX HRX P3 BD18

DMIORXN
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DMI2RXN
DMI3RXN
DMIORXP
DMI1RXP
DMI2RXP
DMI3RXP
DMIOTXN
DMI1TXN
DMI2TXN
DMI3TXN
DMIOTXP
DMI1TXP
DMI2TXP
DMI3TXP

REV1.0

FDI_RXN0
FDI_RXN1
FDI_RXN2
FDI_RXN3
FDI_RXN4
FDI_RXN5
FDI_RXN6
FDI_RXN7
FDI_RXP0
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FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7

FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

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System Power Management

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LAN_RST#
DRAMPWROK
RSMRST#
SUS_PWR_ACK
PBTN_OUT#
ACPRESENT / GPIO31
BATLOW# / GPIO72
RI#

WAKE#
CLKRUN# / GPIO32
SUS_STAT# / GPIO61
SUSCLK / GPIO62
SLP_S5# / GPIO63
SLP_S4#
SLP_S3#
SLP_M#
TP23
PMSYNCH
SLP_LAN# / GPIO29

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PM_SLP_S4# <30>
PM_SLP_S3# <30>
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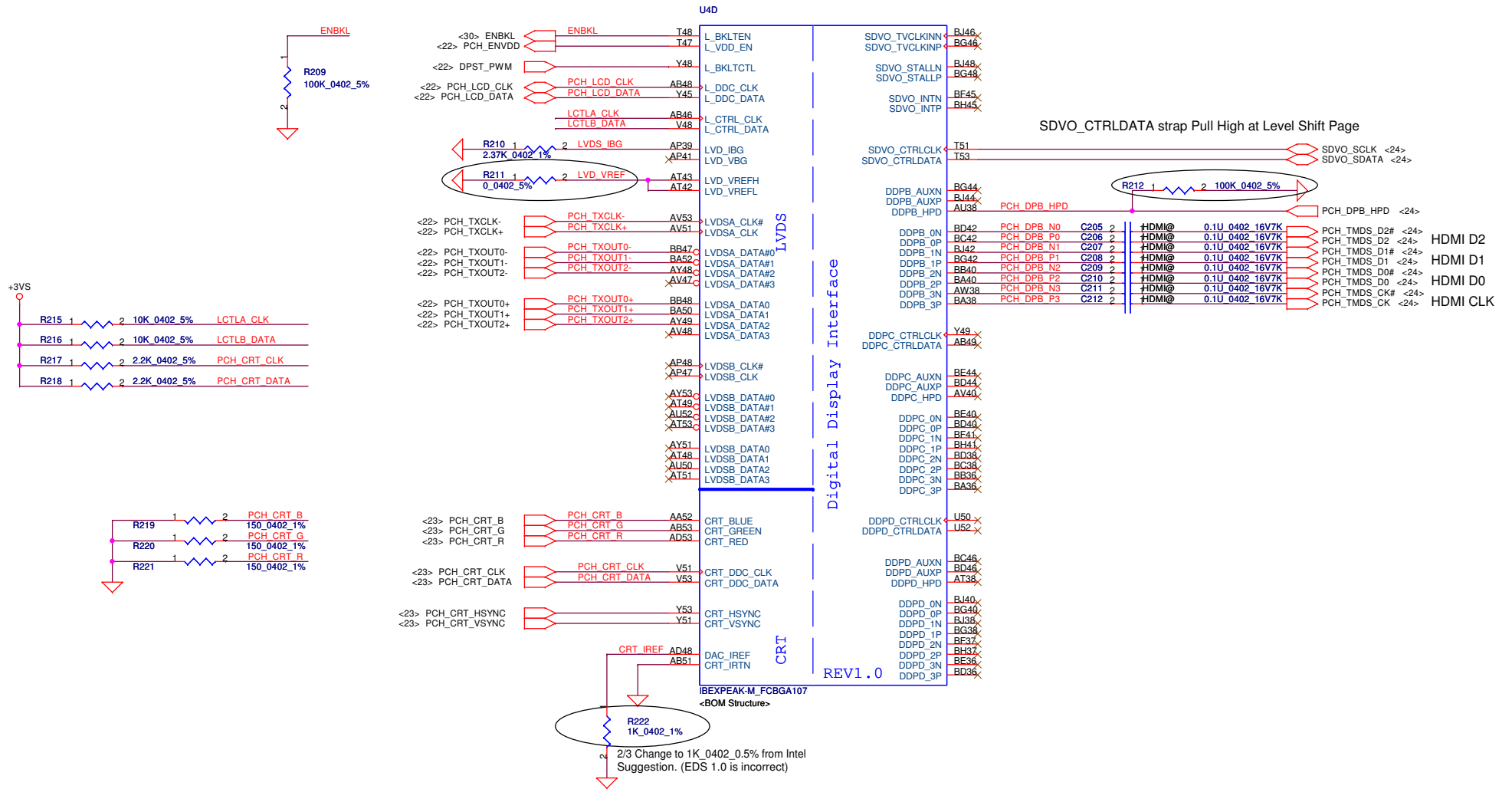
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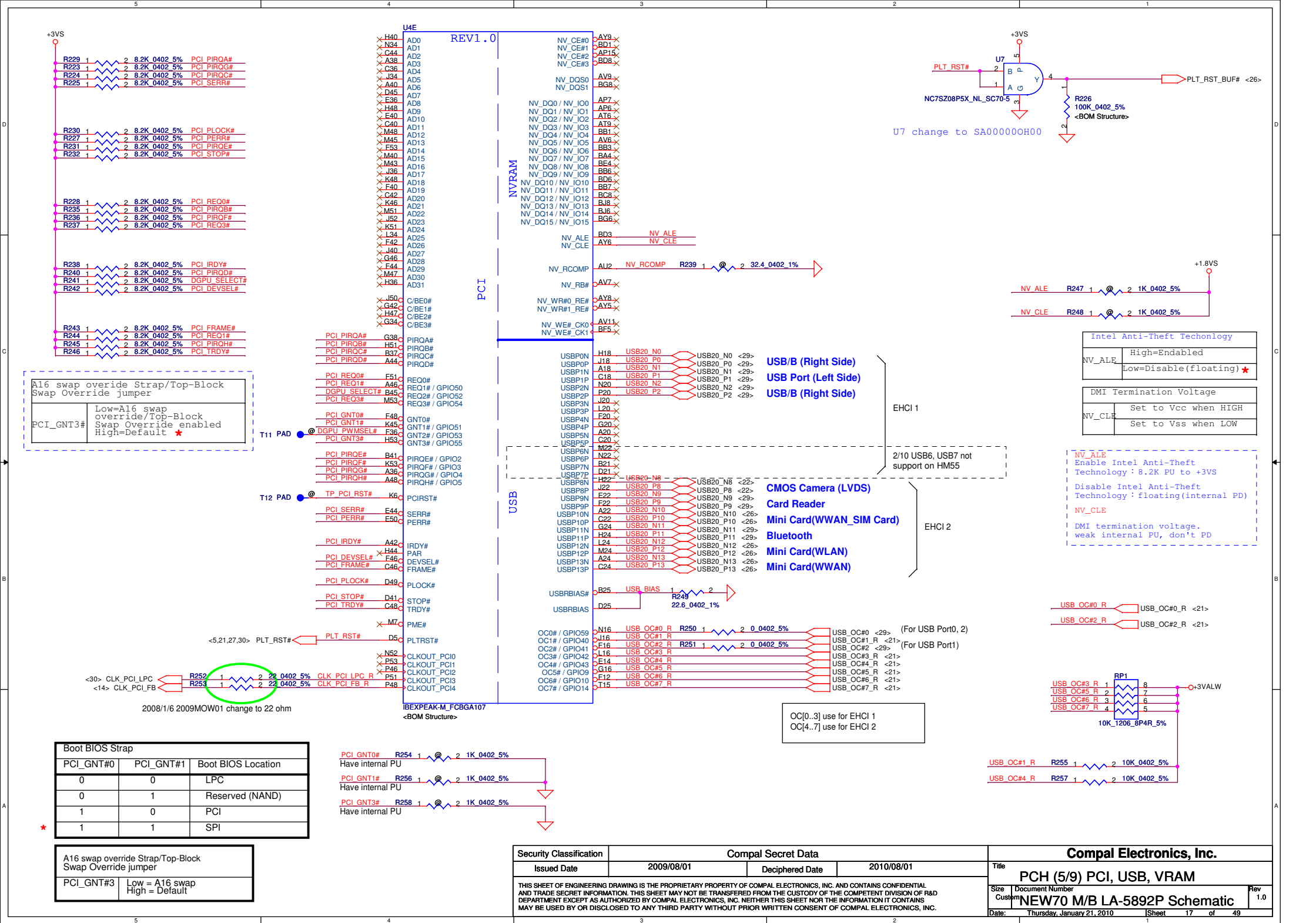
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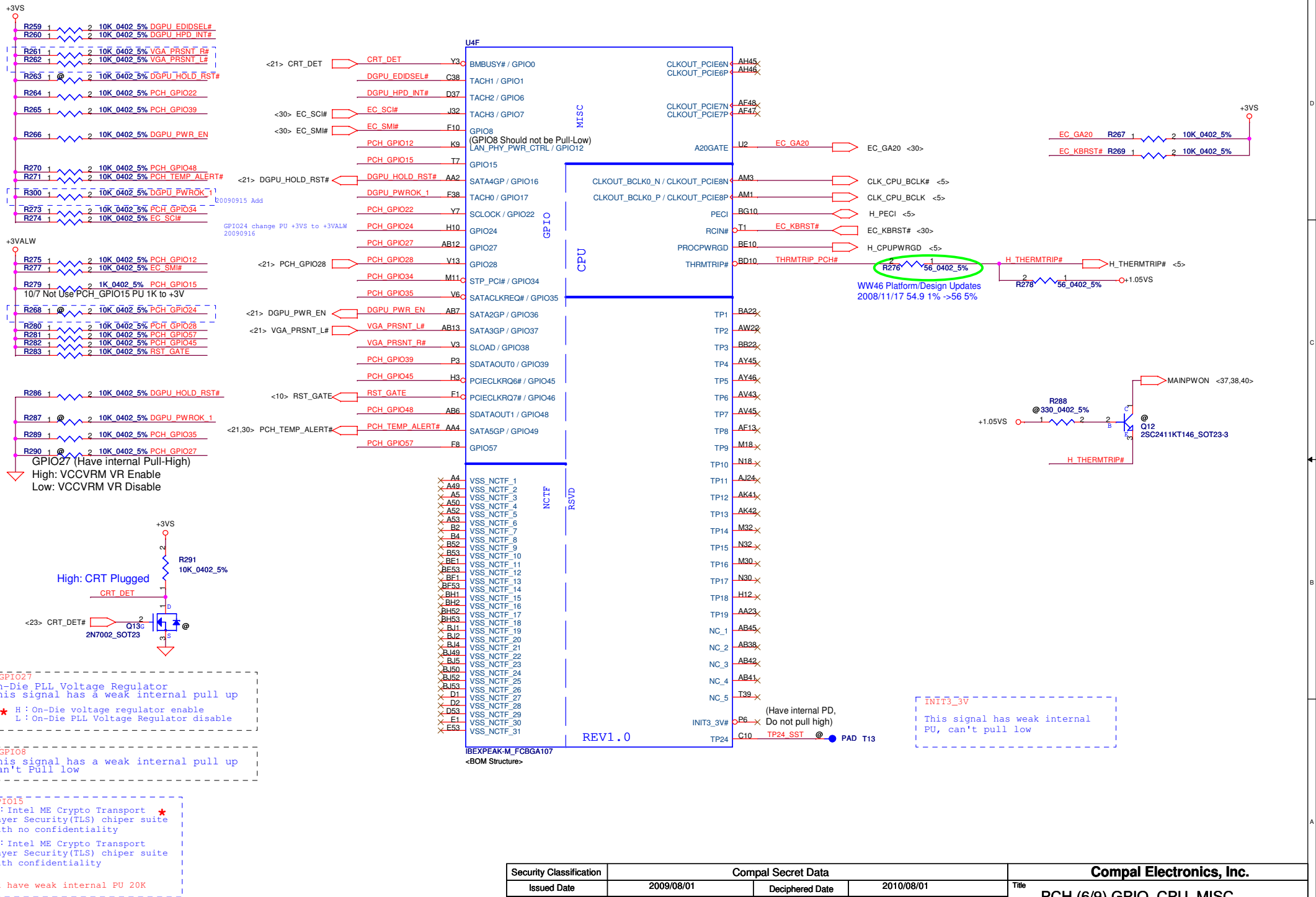
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/08/01				Title			
Deciphered Date				2010/08/01				PCH (3/9) DMI, FDI, PM			
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				NEW70 M/B LA-5892P Schematic				Rev			
				Date: Thursday, January 21, 2010				Sheet 15 of 49			



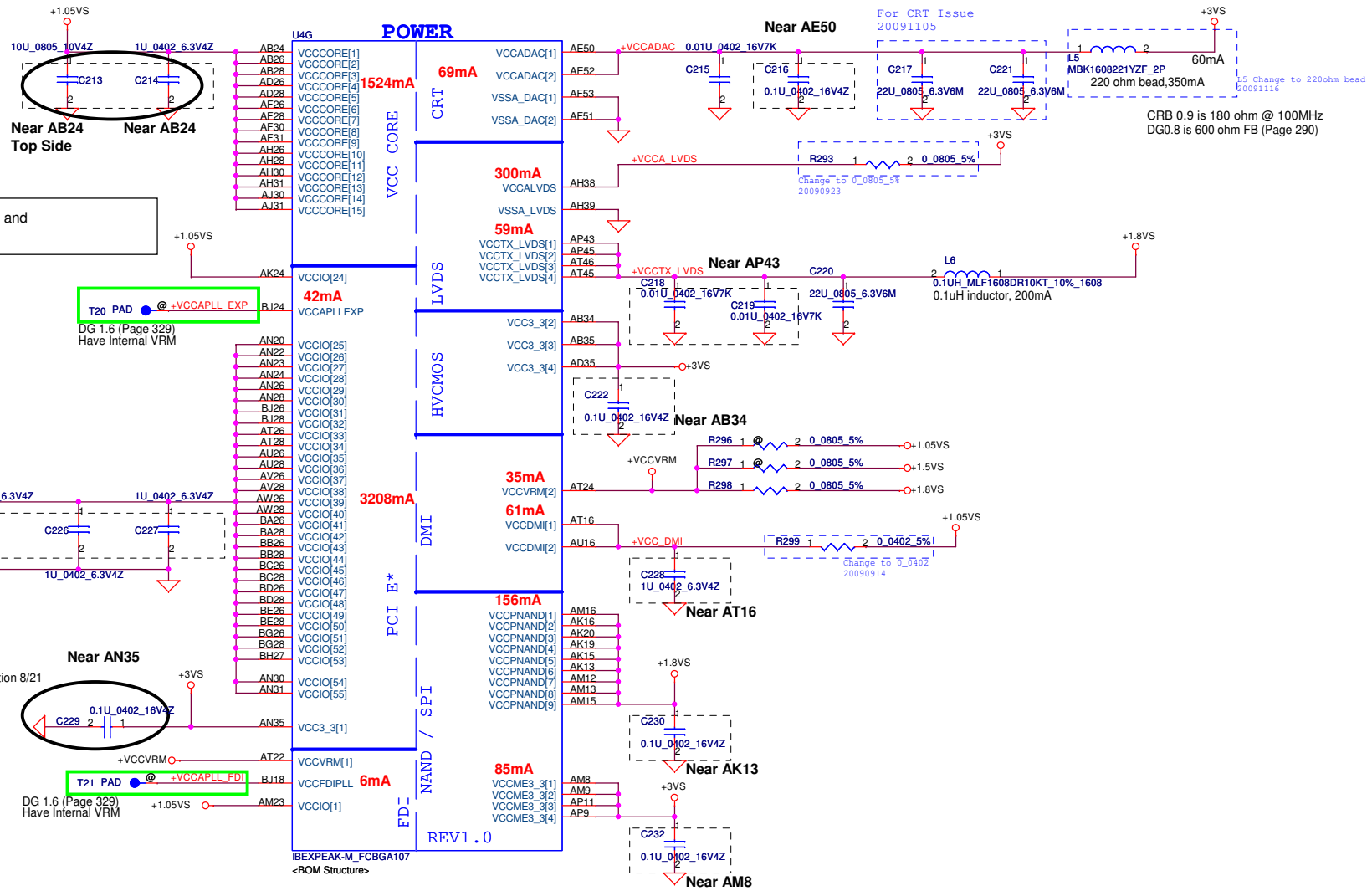
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/08/01		Deciphered Date		2010/08/01		Title	
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										Size	
										Document Number	
										NEW70 M/B LA-5892P Schematic	
										Date	
										Thursday, January 21, 2010	
										Sheet	
										16 of 49	
										Rev	
										1.0	

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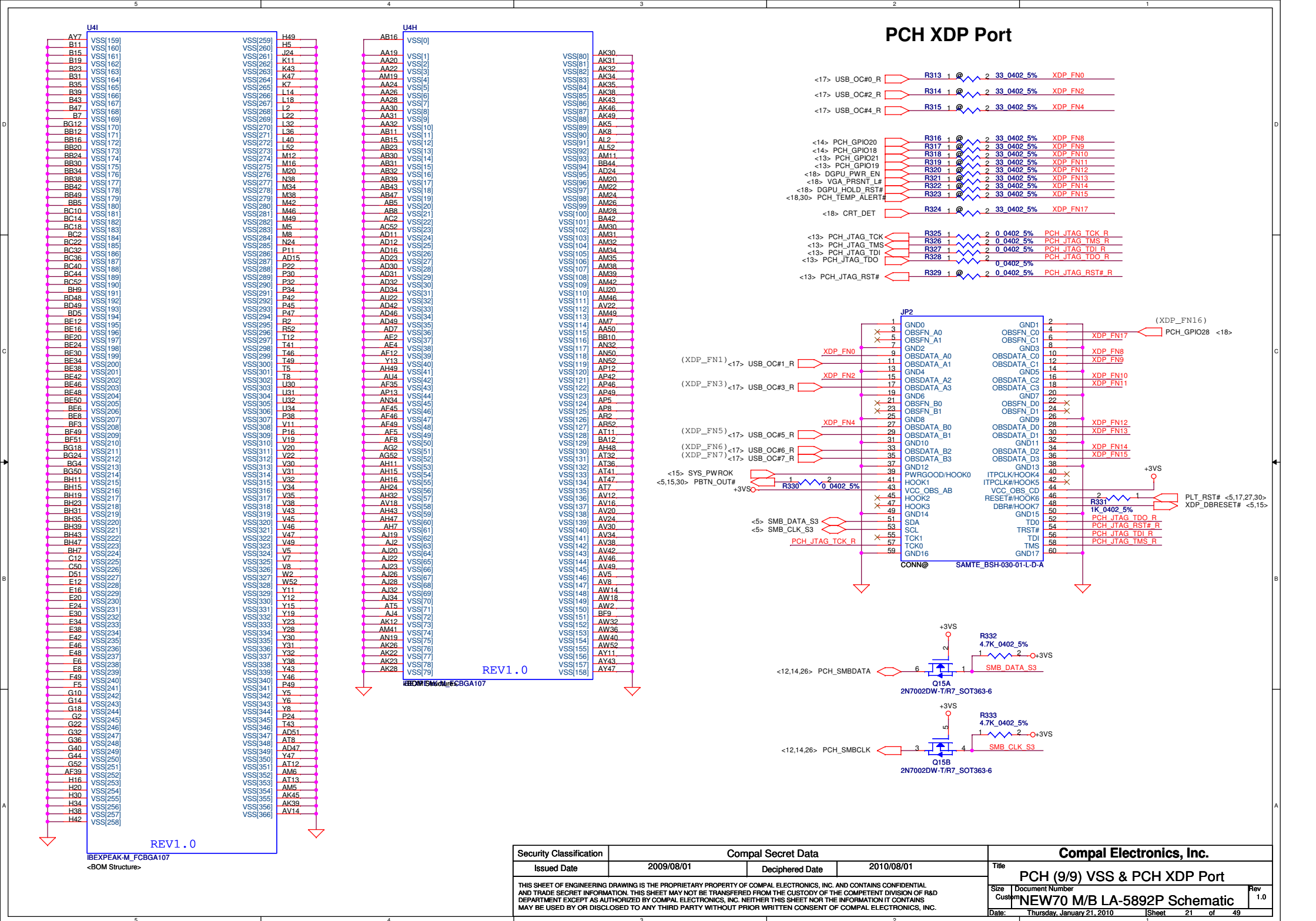




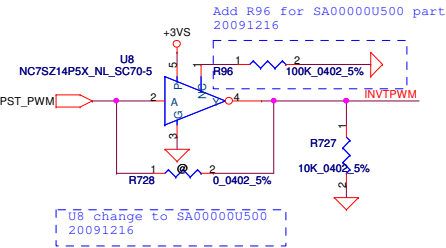
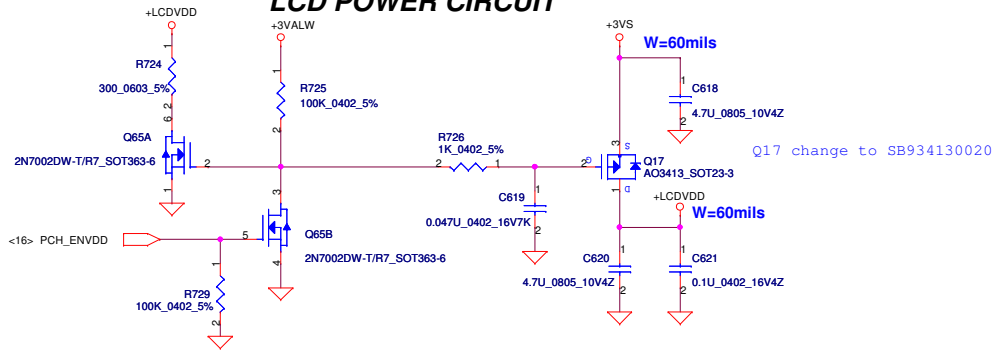
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	PCH (6/9) GPIO, CPU, MISC
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				Date	Thursday, January 21, 2010
				Sheet	18 of 49



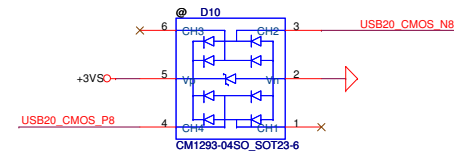
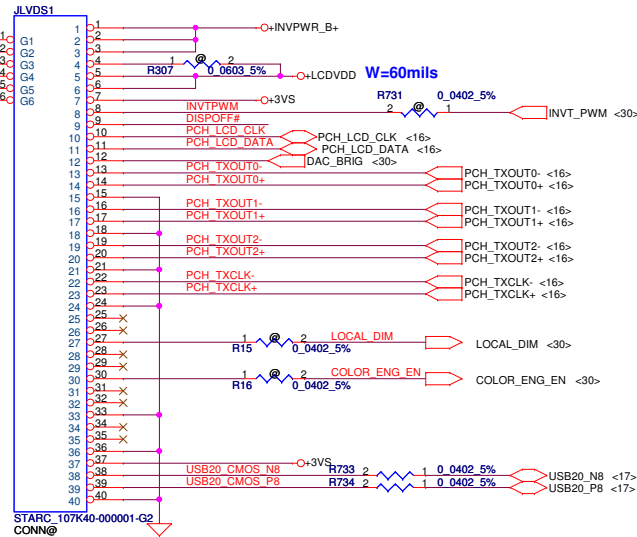
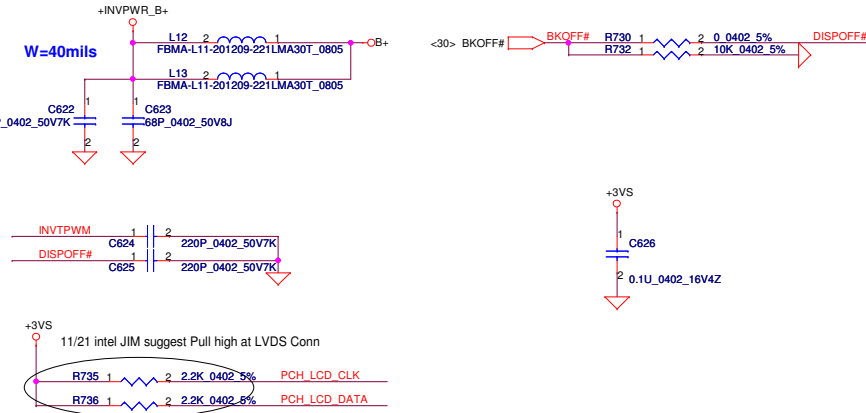
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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title PCH (7/9) PWR	
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				Date	Thursday, January 21, 2010
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LCD POWER CIRCUIT

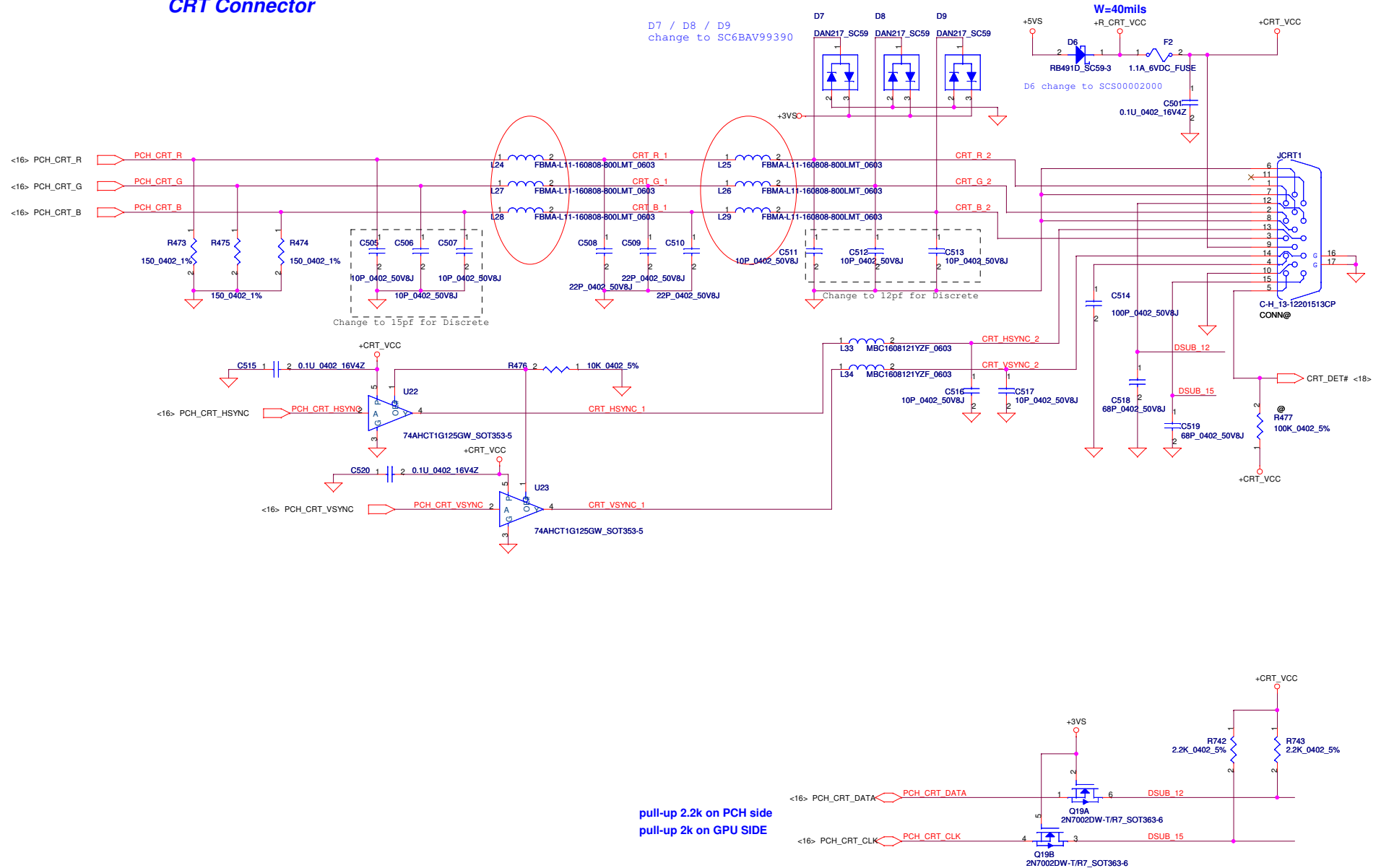


LED PANEL Conn.



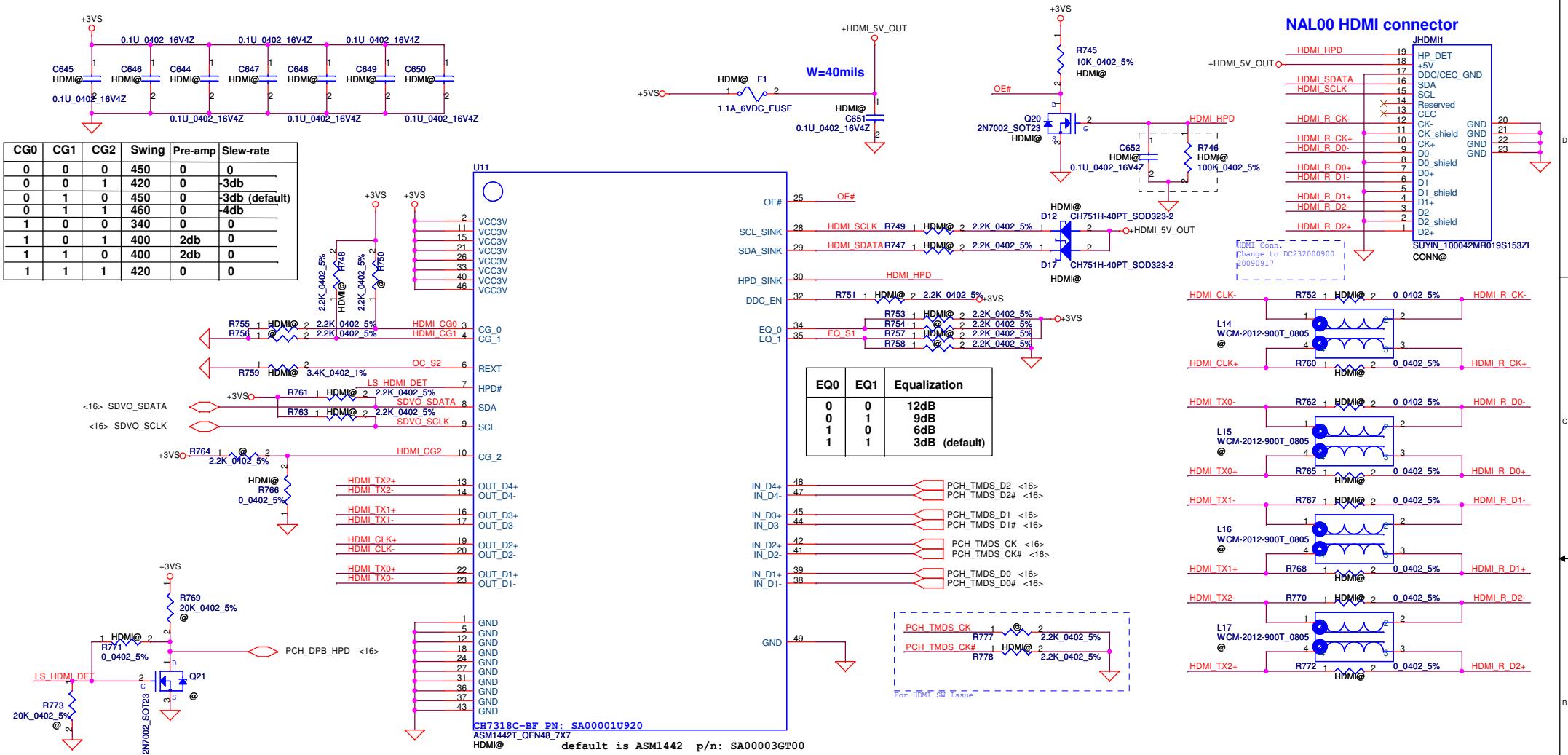
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Issued Date				2009/5/12				Title			
Deciphered Date				2010/04/15				LVDS Connector			
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				Custom NEW70 M/B LA-5892P Schematic				1.0			
Date: Thursday, January 21, 2010				Sheet 22 of 49							

CRT Connector

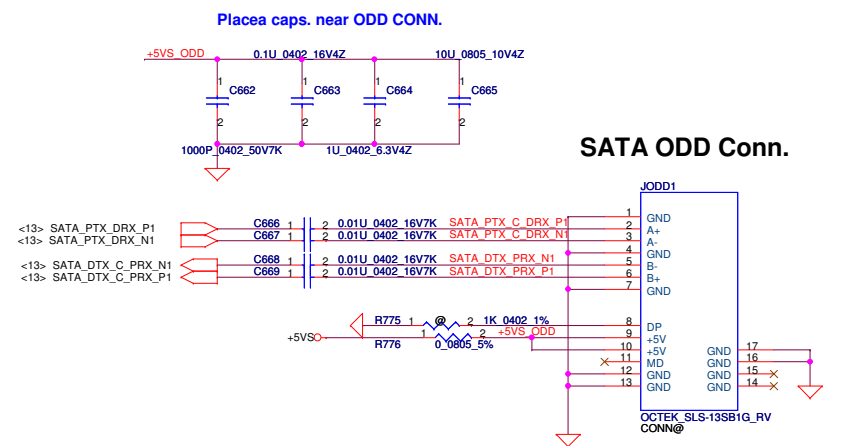
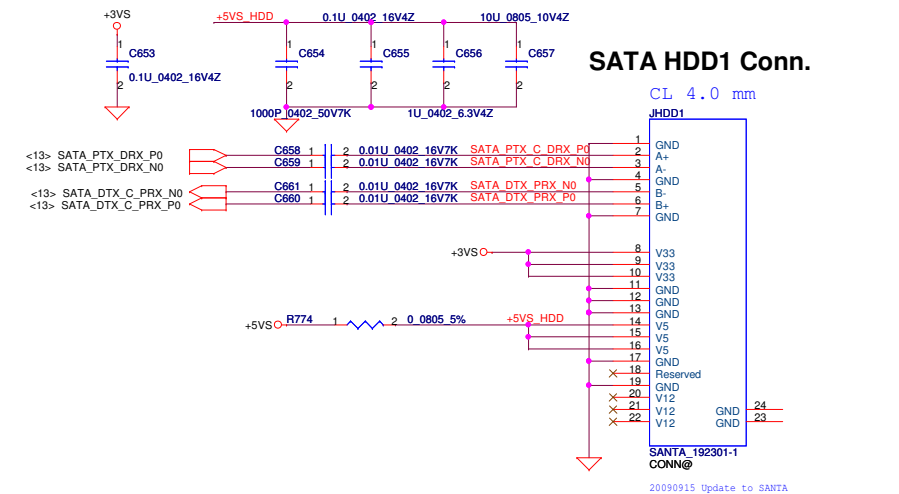
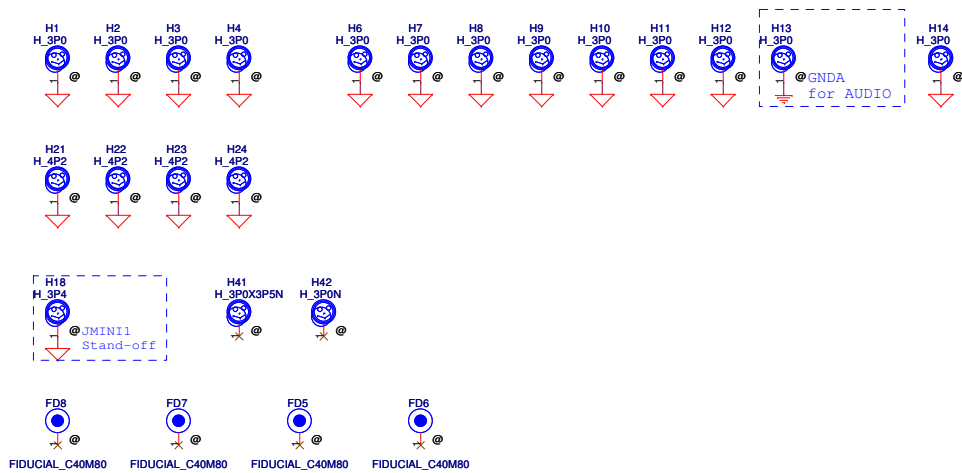


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								2010/04/15			
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Title				NEW70 M/B LA-5892P Schematic				Rev 1.0			
Date				Thursday, January 21, 2010				Sheet 23 of 49			

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

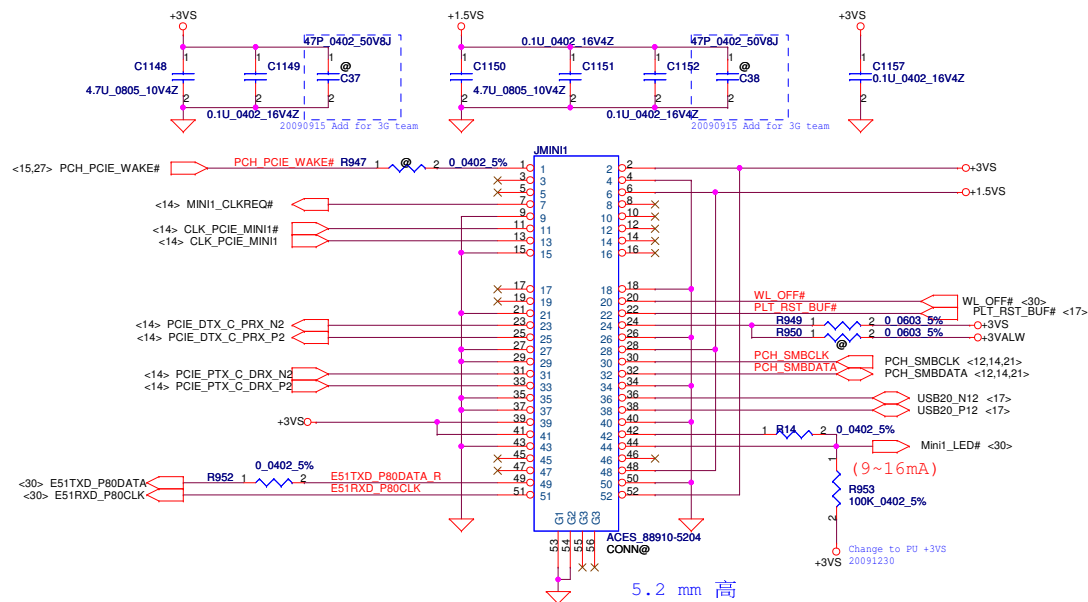


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Issued Date	2009/4/15	Deciphered Date	2010/04/15	Title	
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Size	Custom	Document Number	NEW70 M/B LA-5892P Schematic	Rev	1.0
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								HDD & ODD & Screw Hole		
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								B	NEW70 M/B LA-5892P Schematic	1.0
								Date:	Thursday, January 21, 2010	Sheet 25 of 49

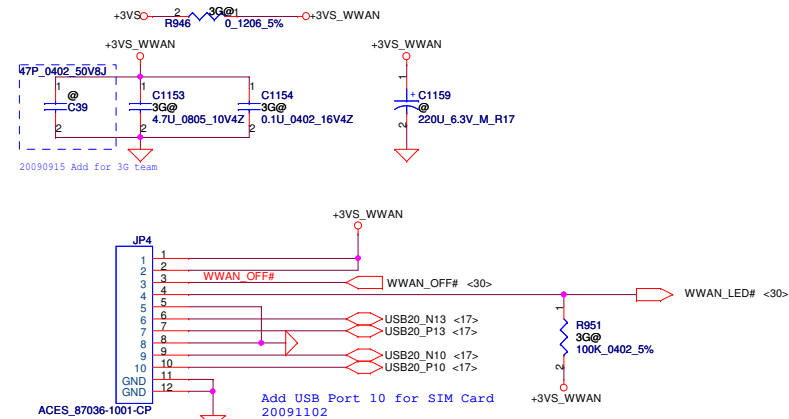
For Wireless LAN



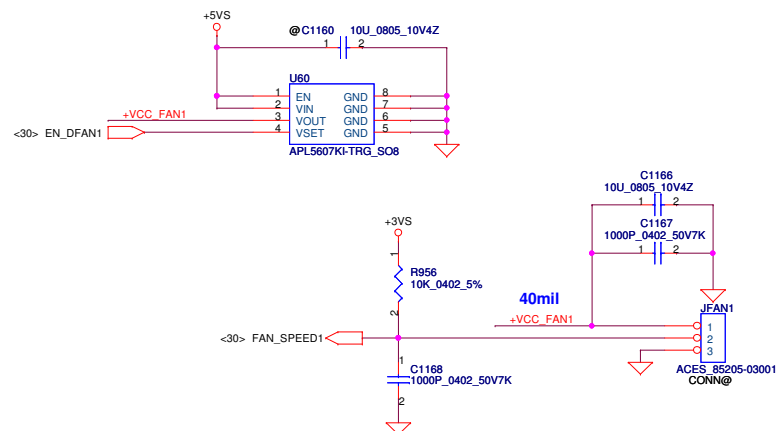
Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

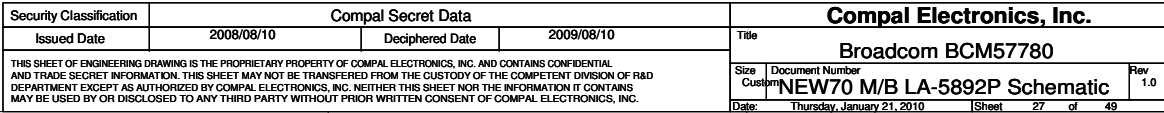
To 3G / GPS Module Connect



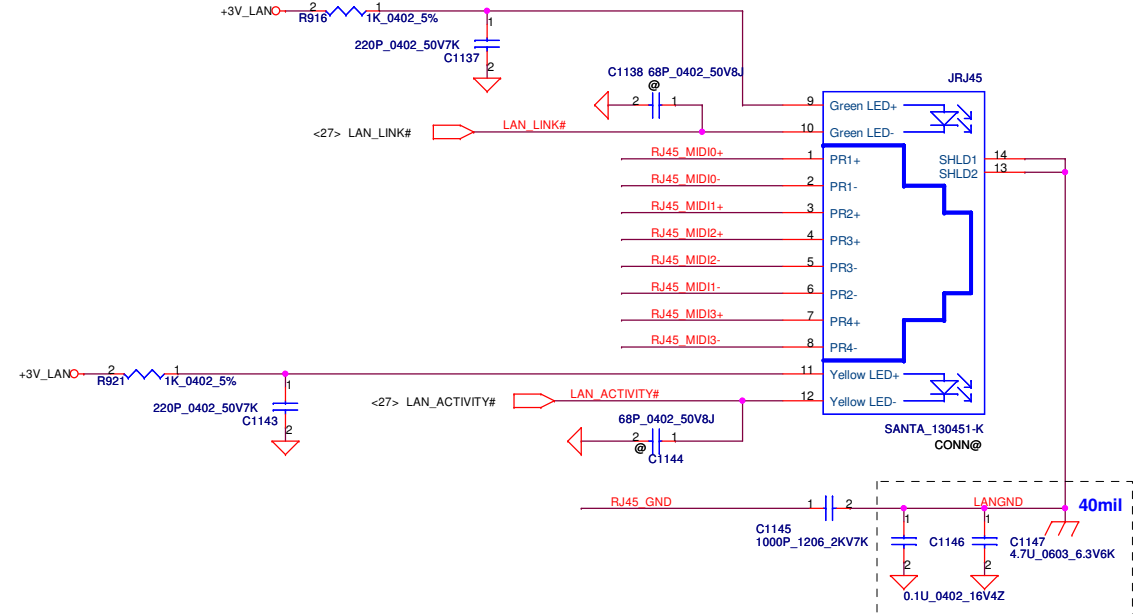
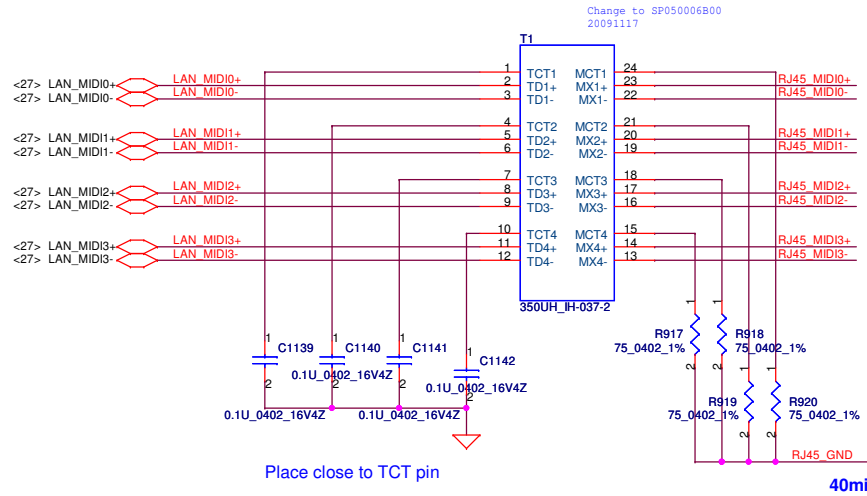
FAN1 Conn



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				NEW70 M/B LA-5892P Schematic	
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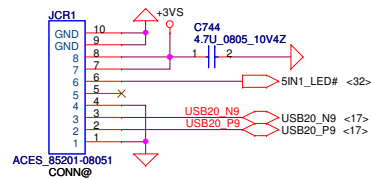


LAN Connector



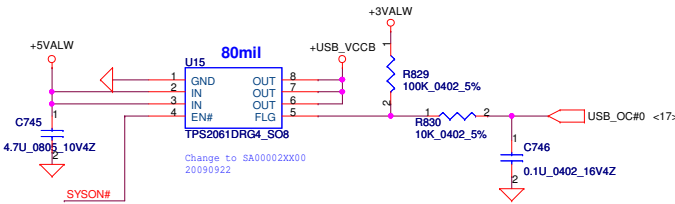
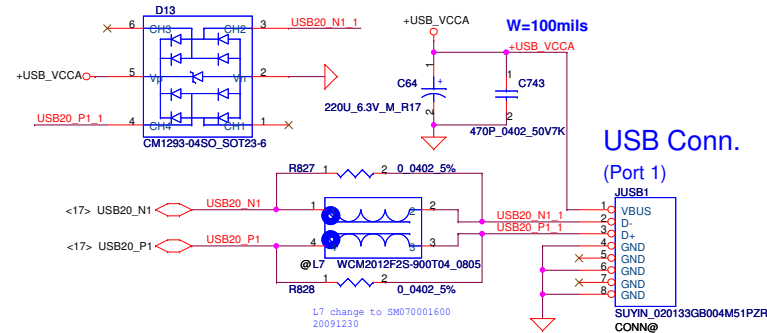
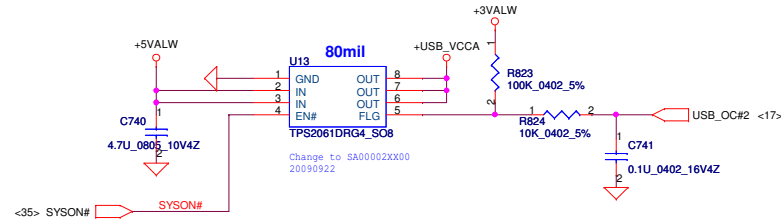
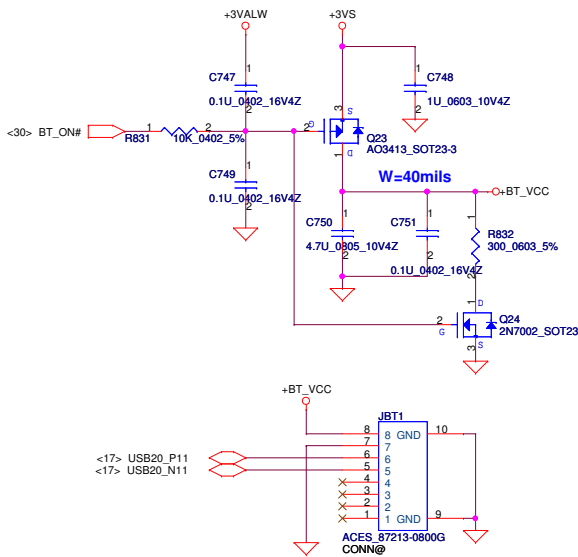
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Issued Date	2008/08/10	Deciphered Date	2009/08/10	Title	
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Size	Customer	Document Number	NEW70 M/B LA-5892P Schematic	Rev	1.0
Date	Thursday, January 21, 2010	Sheet	28	of	49

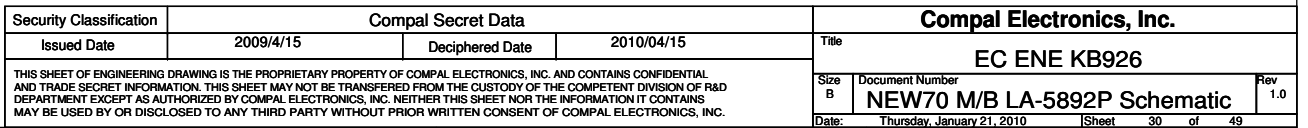
Card Reader Conn.

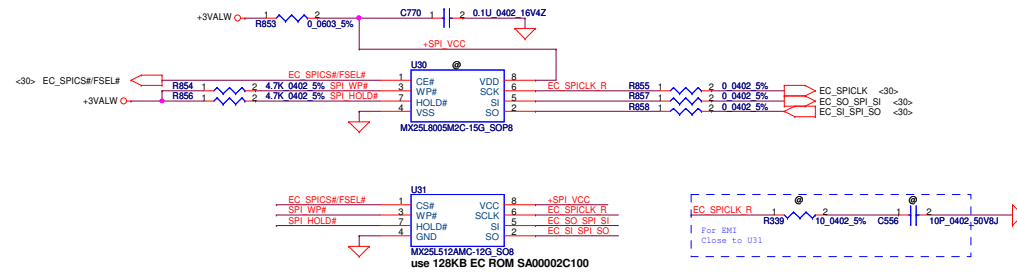
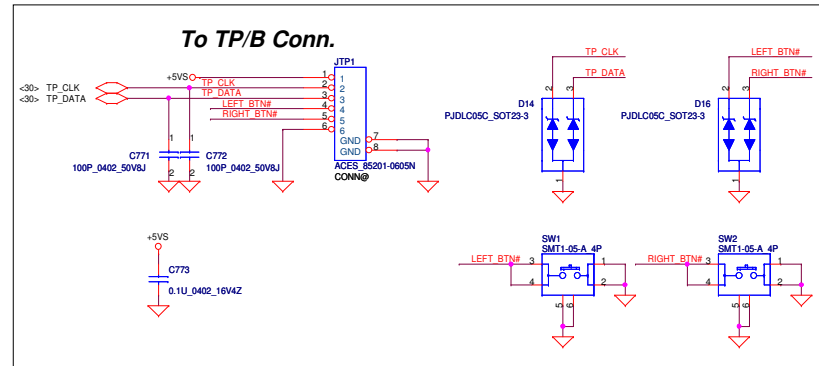
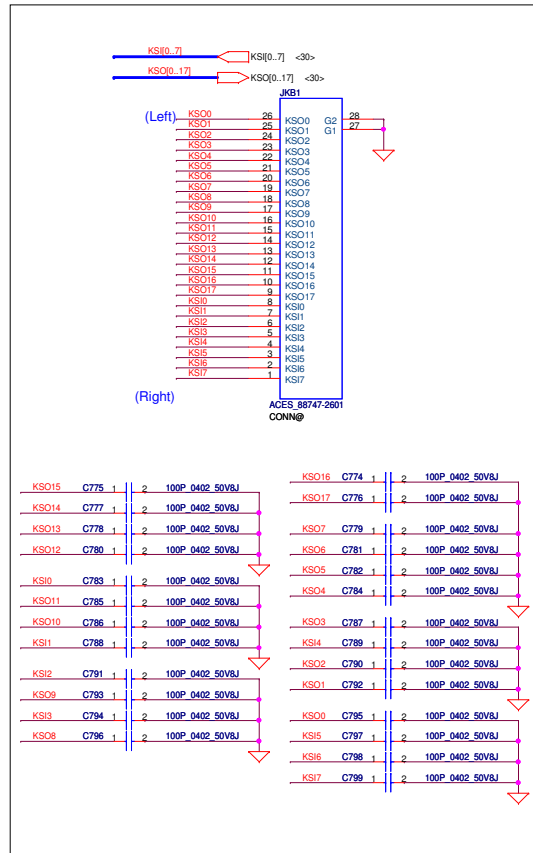


Bluetooth Conn.

Q23 change to SB934130020





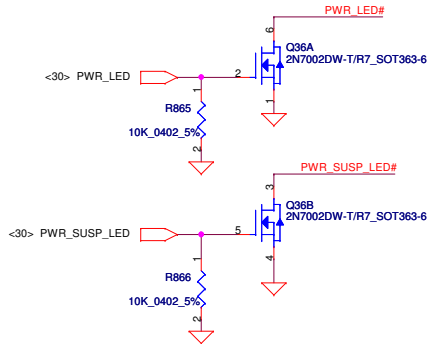
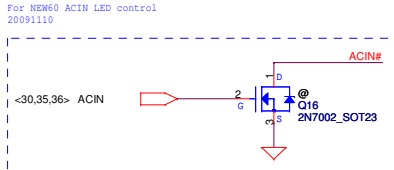
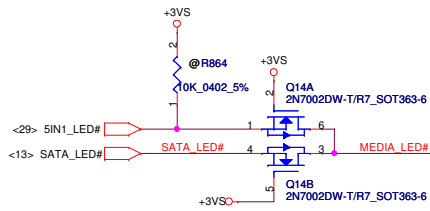
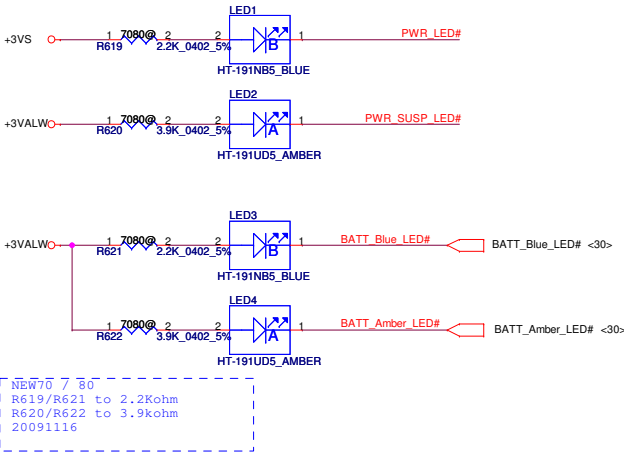
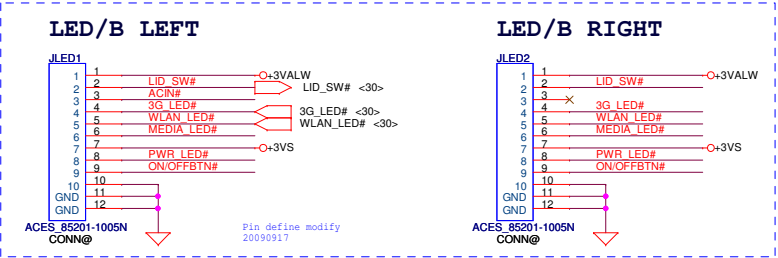
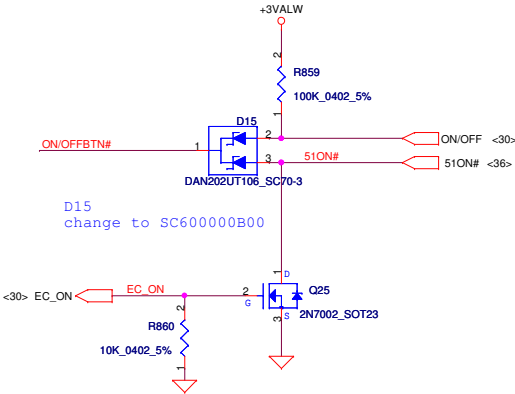


ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

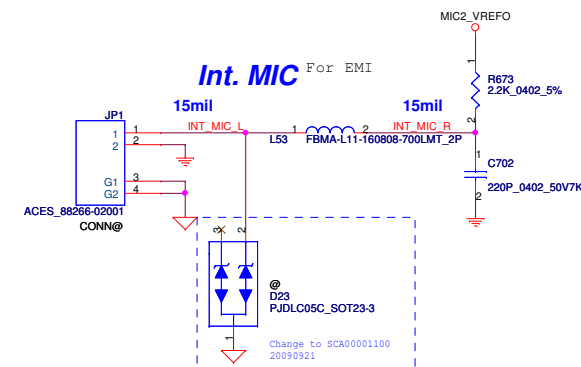
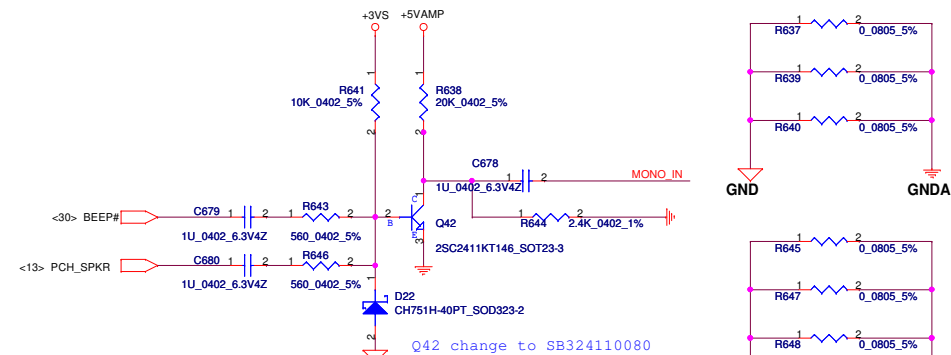
To BTN/B Conn.

	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN#
KSI4	BT_BTN#	Volum down_BTN#
KSI5	Power save_BTN#	

Power Button

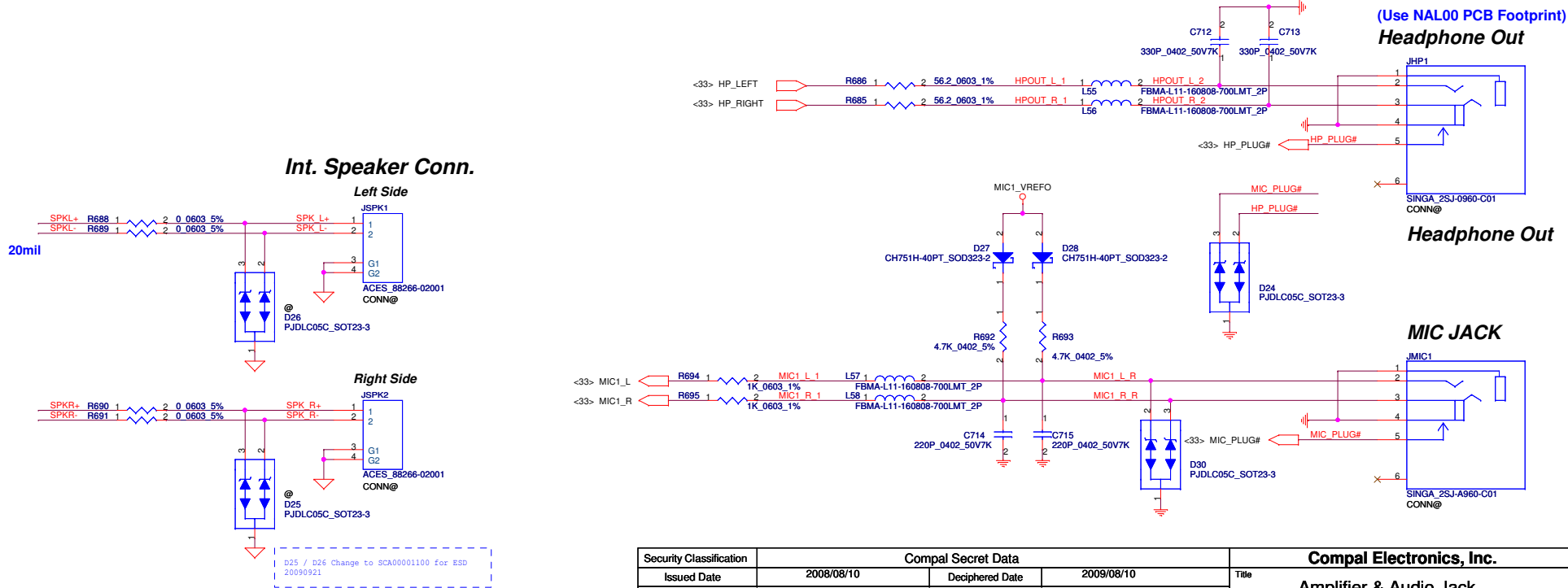
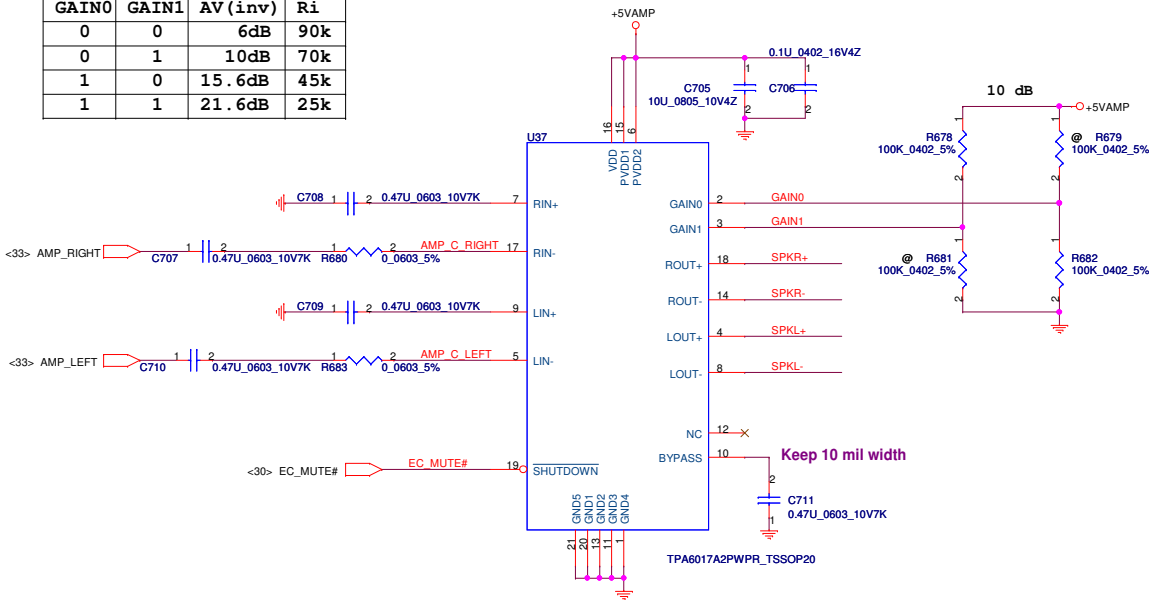


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								NEW70 M/B LA-5892P Schematic			
								Date: Thursday, January 21, 2010			
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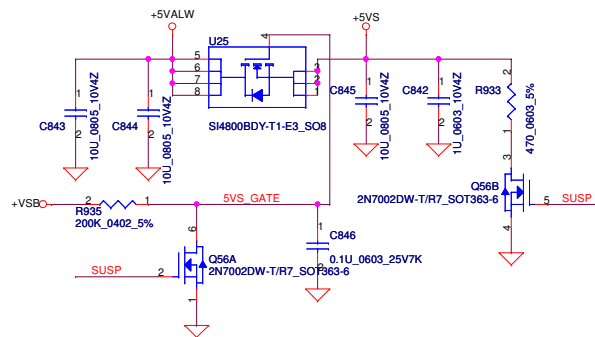
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								Size	Document Number		Rev	
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								Date:	Thursday, January 21, 2010		Sheet	33

GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

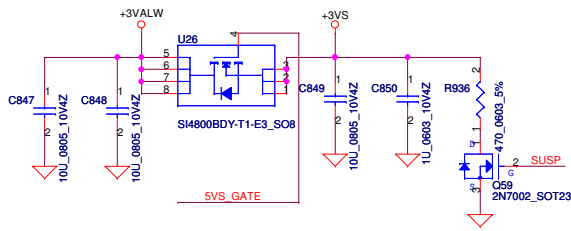


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Title				Amplifier & Audio Jack				Size			
Customer				NEW70 M/B LA-5892P Schematic				Rev			
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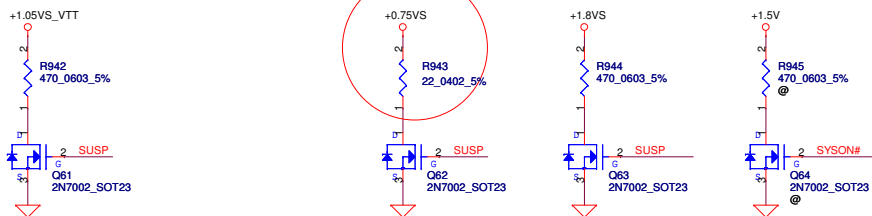
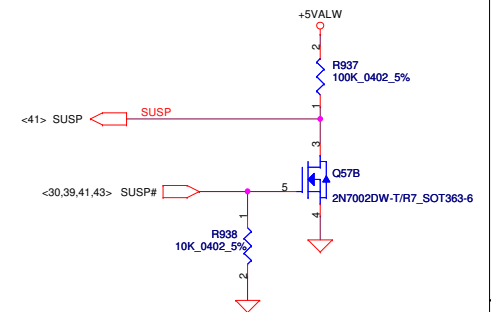
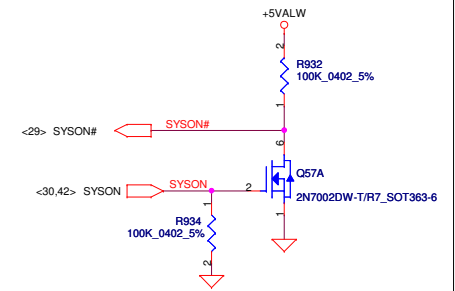
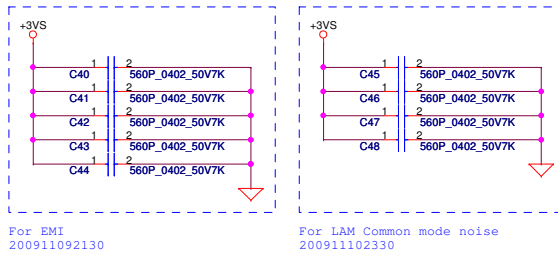
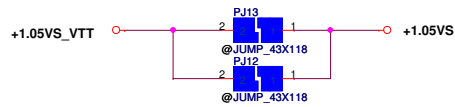
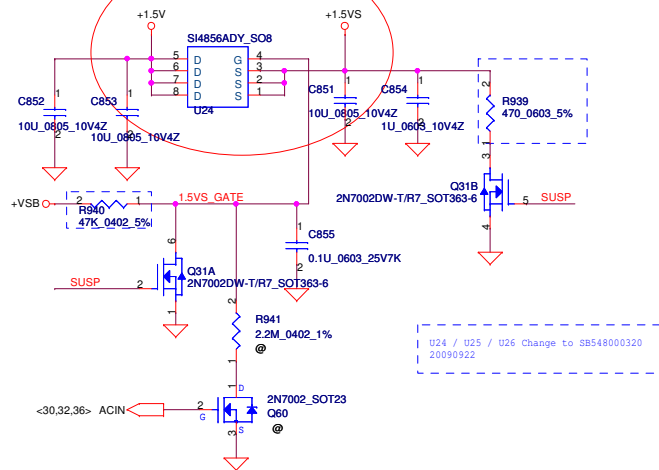
+5VALW TO +5VS



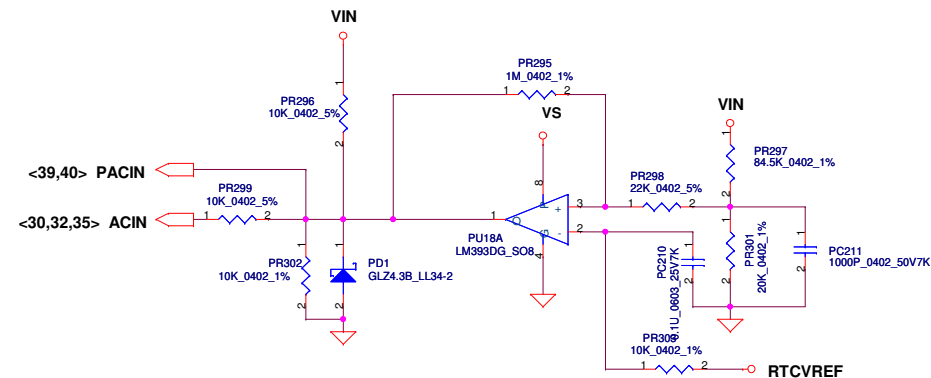
+3VALW TO +3VS



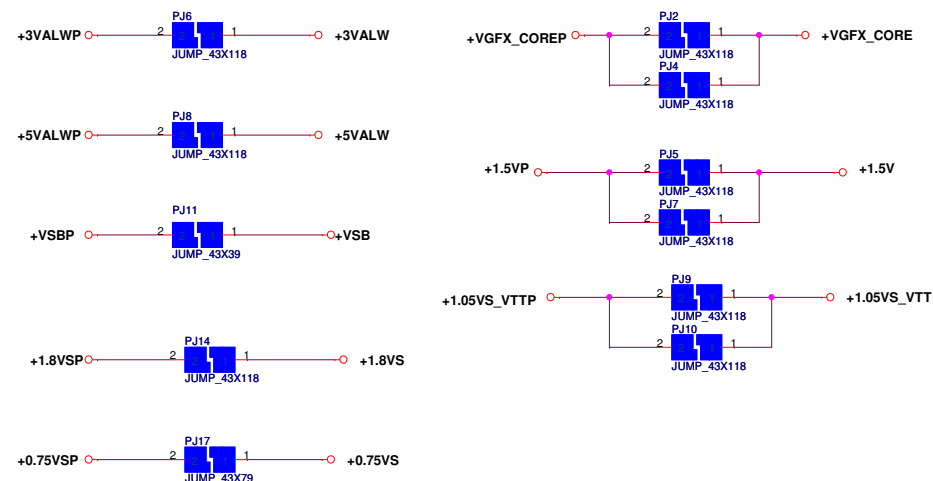
+1.5V to +1.5VS



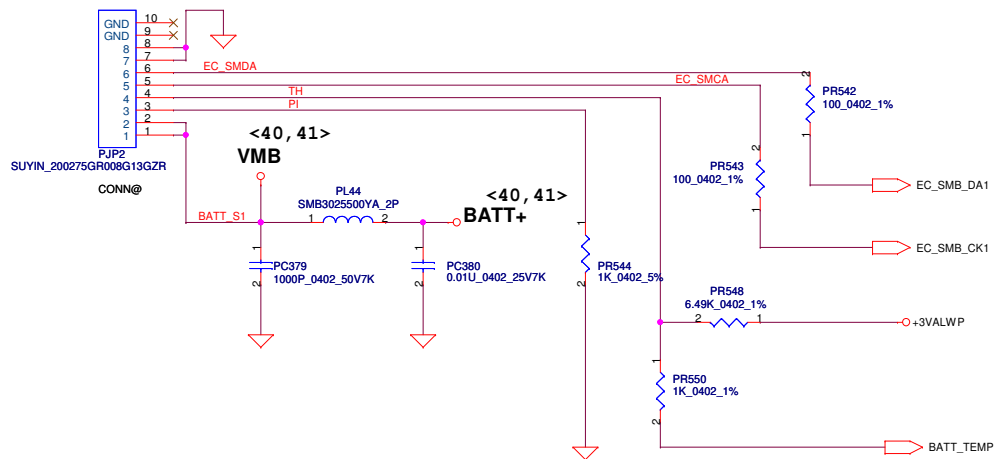
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2009/12/31				2009/12/31				Title			
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Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



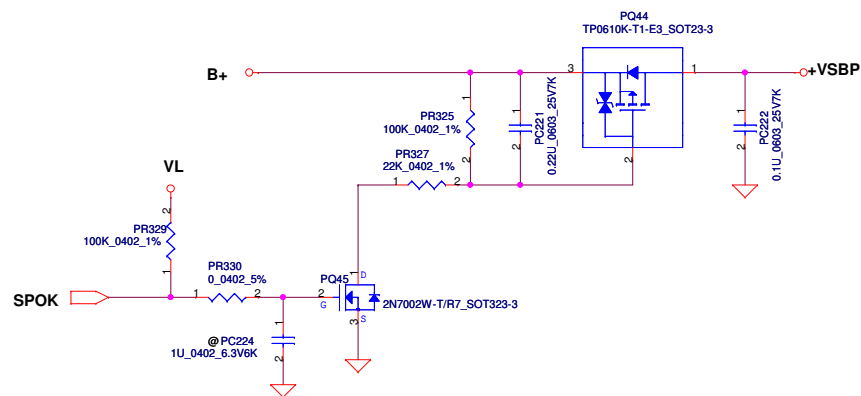
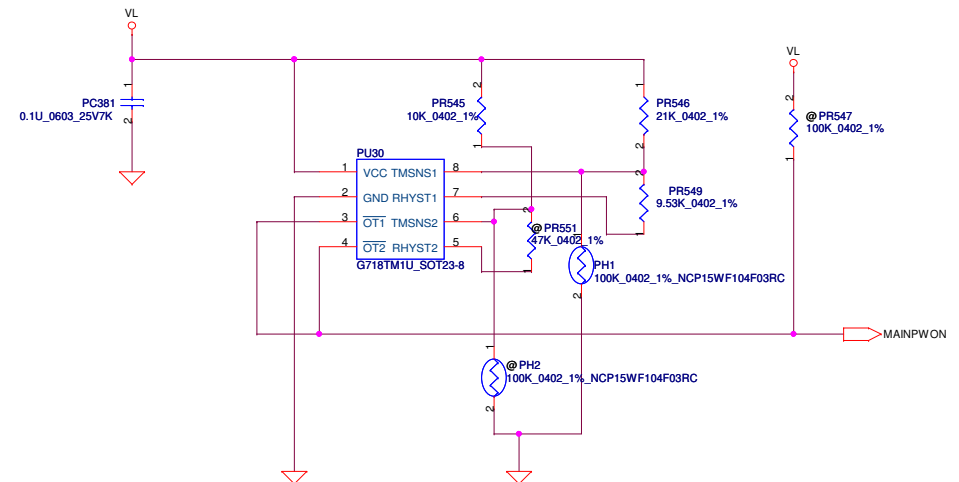
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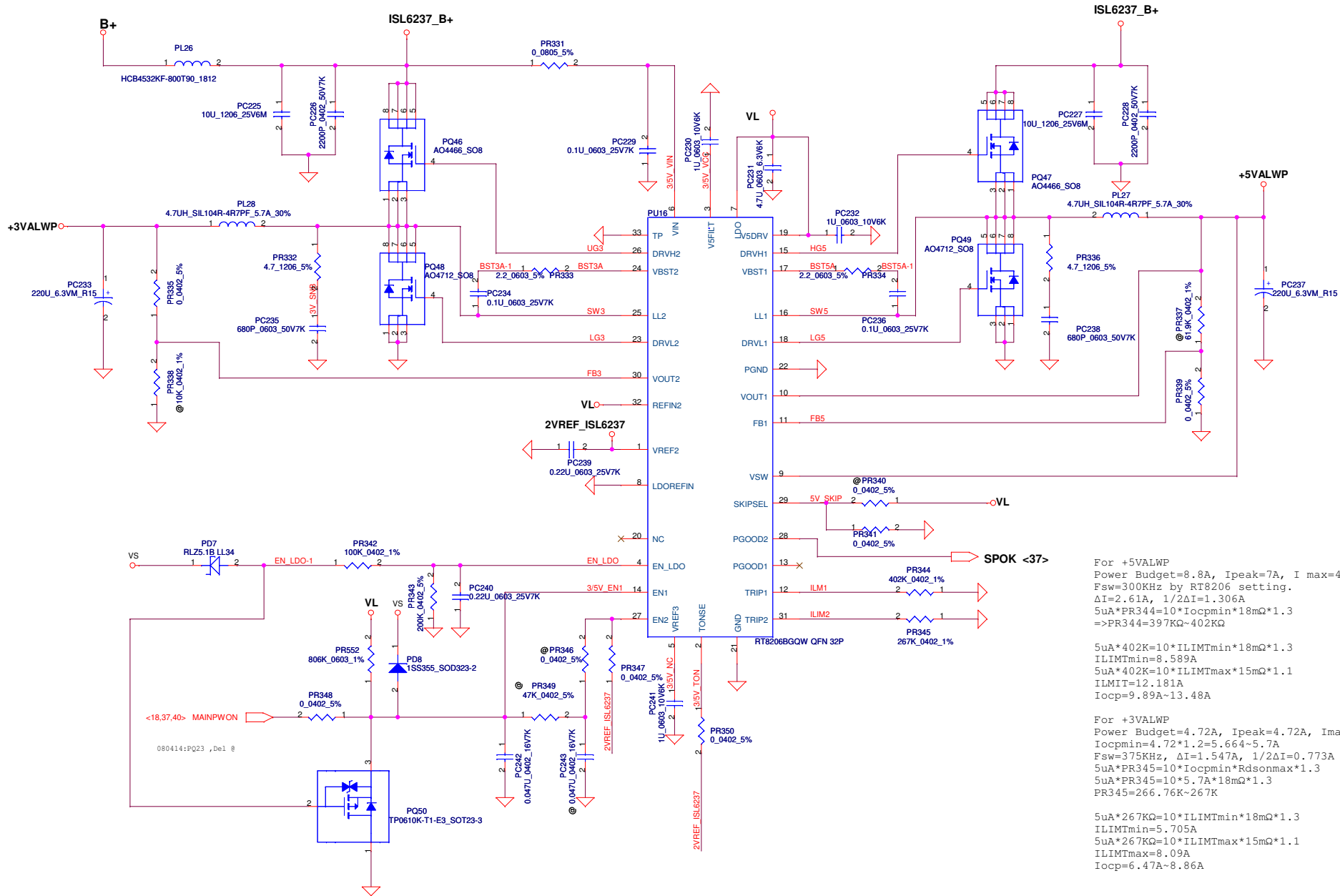
PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C



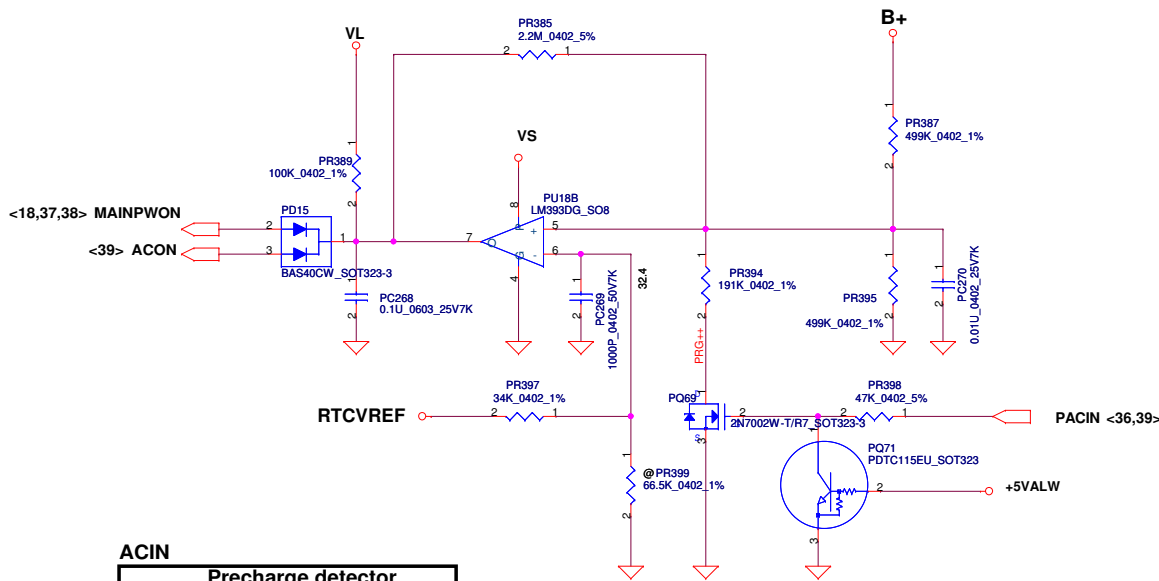
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
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CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

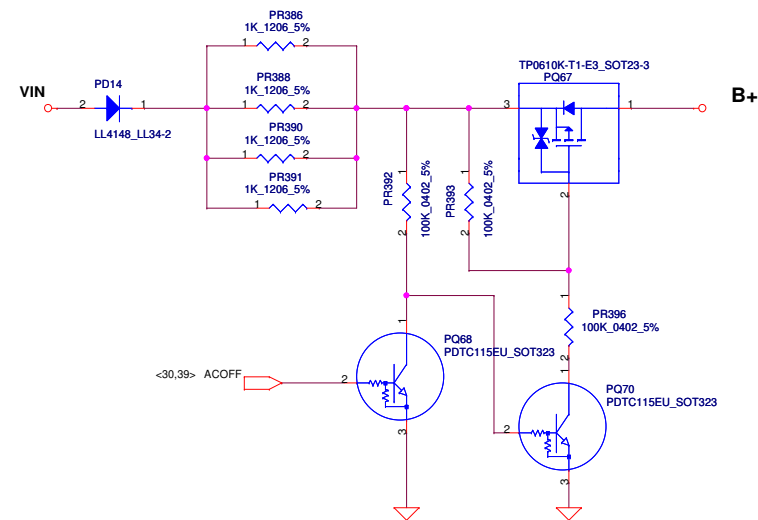


ACIN

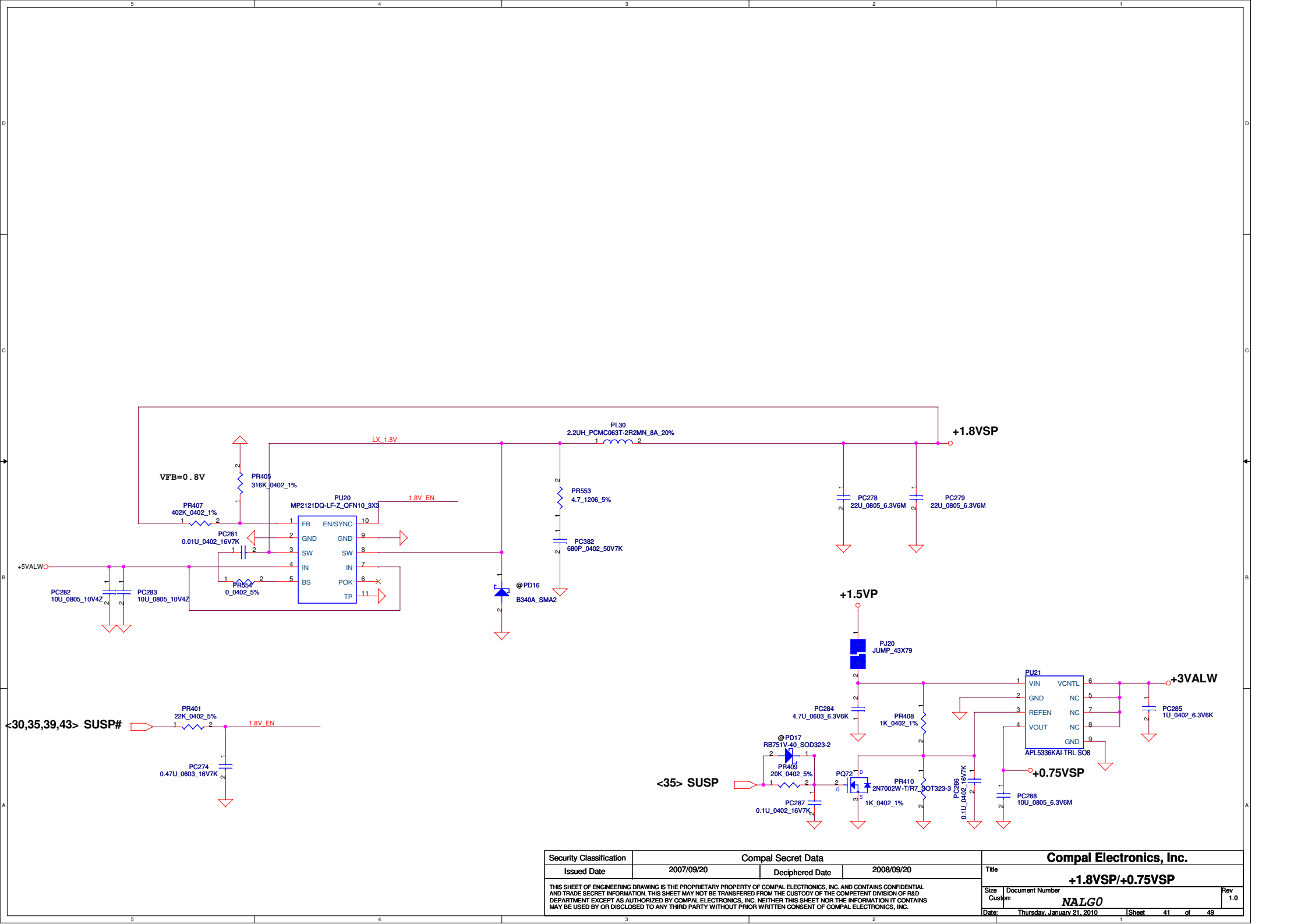
Precharge detector			
Min.	typ.	Max.	
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

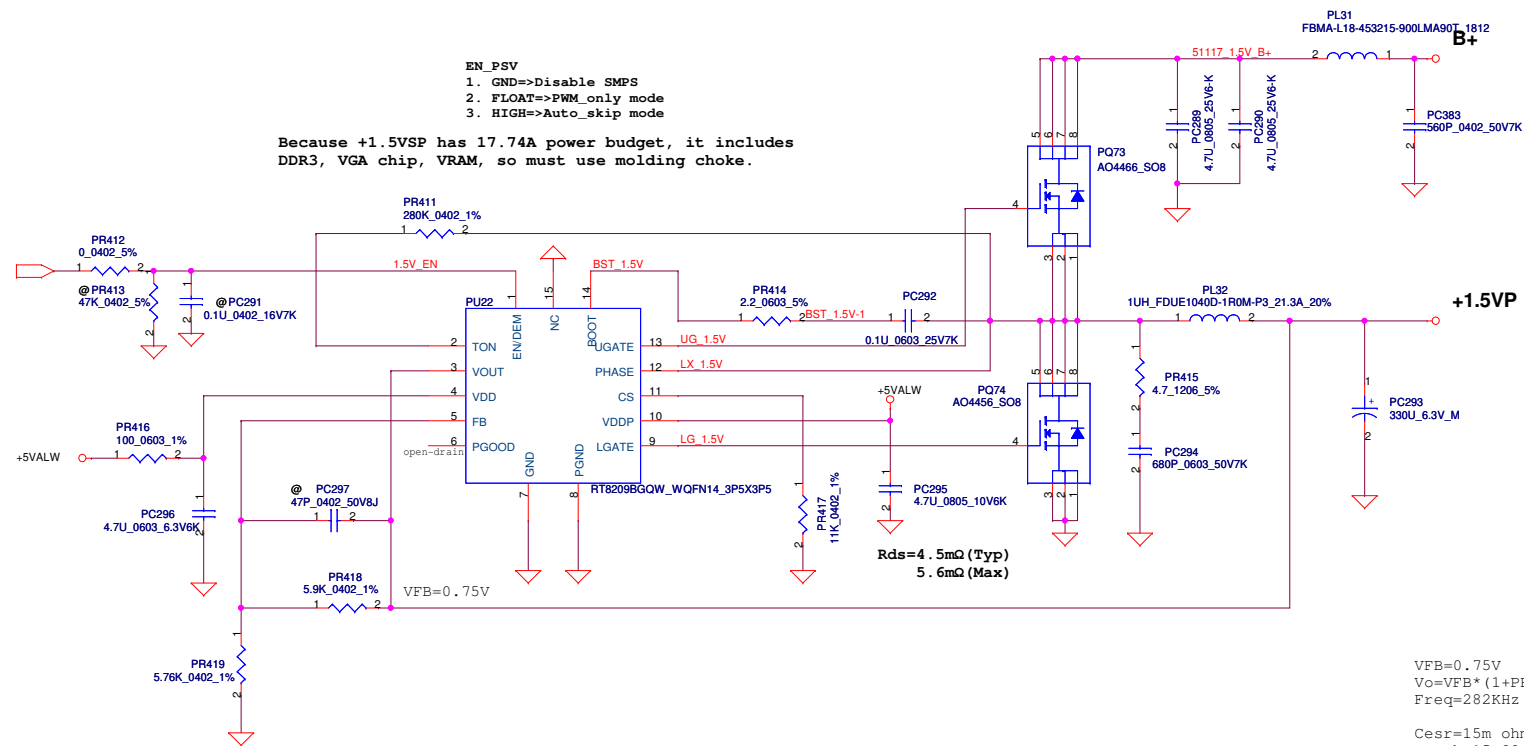
Precharge detector			
Min.	typ.	Max.	
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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<30,35> SYSON



VFB=0.75V
 $V_o = VFB * (1 + PR418 / PR419) = 1.52V$
Freq=282KHz (min) , 300KHz (typ)

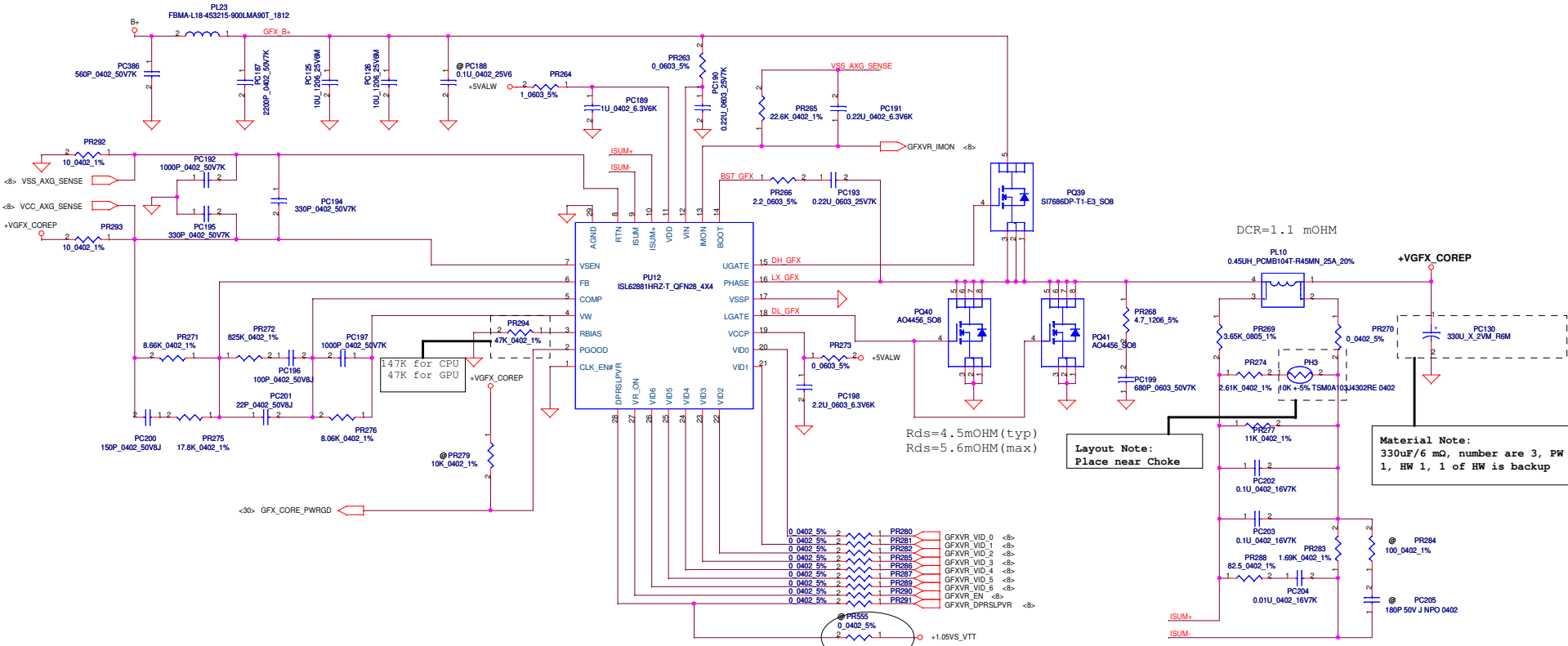
Cesr=15m ohm
Ipeak=15.82A
Iocpmin=18.98A
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * \text{Freq}) = 4.899A$
 $1/2 \Delta I = 2.449A$
Iocp=18.09A~29.13A

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Issued Date		2008/08/10		Title	
		Deciphered Date		1.5VP	
				Size	
				Document Number	
				Custom	
				NALGO	
				Rev	
				1.0	
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				Sheet	
				42 of 49	


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Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCF calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCF Threshold*Rdroop/LL=24.89A

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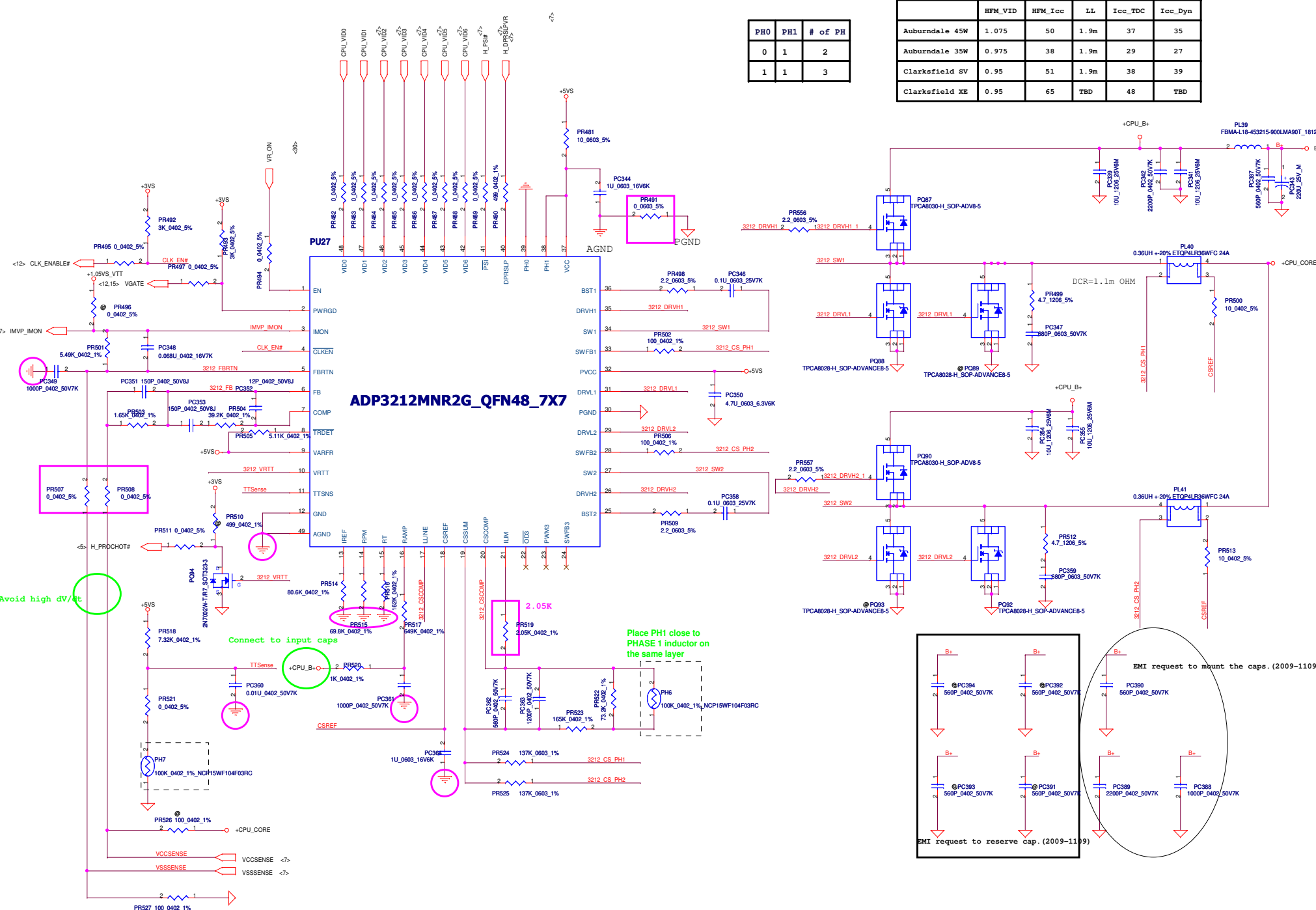


2009-1214 common circiut modify.

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				Size	Document Number	Rev
				NALGO		1.0
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PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Arrandale CPU of UMA SKU only use 1 LS MOS	Arrandale CPU of UMA SKU only use 1 LS MOS	0.1	45	1 pop PQ87,PQ90, un-pop PQ86. 2 Delete PQ89, PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP ADVANCE 4 PC A false)	2009-1019	to DVT
2	BOM unique.	In order to BOM unique for 1SS355, re-link PD8.	0.1	38	Change PD8 from SC1SS355003 to SC100001K00	2009-1019	to DVT
3	CIS link error.	CIS link error.	0.1	45	Chnage PR500 from SD028100A00(S RES I/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1019	to DVT
4	BOM unique.	BOM unique.	0.1	39	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1019	to DVT
5	BOM unique.	BOM unique.	0.1	41	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1019	to DVT
6	BOM unique.	BOM unique.	0.1	45	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1019	to DVT
7	BOM unique.	BOM unique.	0.1	38	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1019	to DVT
8	BOM unique.	BOM unique.	0.1	45	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1019	to DVT
9	BOM unique.	BOM unique.	0.1	43	Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1019	to DVT
10	VTI Power rail commond design.	VTI Power rail commond design.	0.1	43	Change PQ83 from SB00000I900(S TR AON6704L 1N DFN) to SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1019	to DVT
11	Charger, EMI request.	EMI request to add a bead to replace Jump to PASS EMI test.	0.2	39	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)-X63826B011 Delete PQ95 SB00000I900(S TR AON6704L 1N DFN)-OTHERS	2009-1019	to DVT
12	+VSBP, EMI request.	EMI request to add PC221/PC222 to PASS EMI test	0.2	37	Add PL45 SM010018210(S SUPPRE TAI-TECH HCB4532KF-800T90 1812)	2009-1105	to DVT
13	+1.8VSP, BOM error.	+1.8VSP EN delete wrong. Must add PR401 and PC274 for SUSP# enable.	0.2	41	Add PC221 SE000005Z80 S CER CAP .22U 25V K X7R 0603 Add PC222 SE042104K80 S CER CAP .1U 25V K X7R 0603	2009-1105	to DVT
14	+1.5VP, EMI request.	EMI request add snubber for +1.5VP to PASS EMIU test.	0.2	42	Add PR401 SD028220280 S RES I/16W 22K 0402 5% Add PC274 SE026474K80 S CER CAP 0.47U 16V K X7R 0603	2009-1105	to DVT
15	+1.5VP, EMI request.	EMI request add a small cap to reduce high Freq noise. EMI request change boost R to 2.2 ohm.	0.2	42	Add PR415 SD001470B80 S RES I/4W 4.7 +-5% 1206 Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603	2009-1105	to DVT
16	+1.05VS_VTTP EMI request.	EMI request add two small cap to reduce high Freq noise.	0.2	43	Add PC383 SE074561K80 S CER CAP 560P 50V K X7R 0402 Change PR414 from SD013000080 to SD013220B80	2009-1105	to DVT
17	+1.05VS_VTTP EMI request.	EMI request add snubber for +1.05VS_VTTP to PASS EMIU test.	0.2	43	Add PC384 SE074561K80 S CER CAP 560P 50V K X7R 0402 Add PC385 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
18	+1.05VS_VTTP EMI request.	EMI request change boost R to 2.2 ohm.	0.2	43	Add PR465 SD001470B80 S RES I/4W 4.7 +-5% 1206 Add PC332 SE024681J80 S CER CAP 680P 50V J NPO 0603	2009-1105	to DVT
19	+1.05VS_VTTP, HW request.	HW request to increase +1.05VS_VTTP voltage.	0.2	43	Change PR461 from SD013000080 to SD013220B80	2009-1105	to DVT
20	+GFX_COREP, EMI request.	EMI request add a small cap to reduce high Freq noise.	0.2	44	Change PR472 from SD034499180 to SD034649180.	2009-1105	to DVT
21	+GFX_COREP, EMI request.	EMI request add snubber for +1.05VS_VTTP to PASS EMIU test.	0.2	44	Add PC386 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
22	+GFX_COREP, EMI request.	EMI request change boost R to 2.2 ohm.	0.2	44	Add PR268 SD001470B80 S RES I/4W 4.7 +-5% 1206 Add PC199 SE024681J80 S CER CAP 680P 50V J NPO 0603	2009-1105	to DVT
			0.2	44	Change PR266 from SD013000080 to SD013220B80	2009-1105	to DVT

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	+CPU_COREP, EMI request.	EMI request add a small cap to reduce high Freq noise.	0.2	45	Add PC387 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
25	+CPU_COREP, EMI request.	EMI request change boost R to 2.2 ohm.	0.2	45	Change PR498/PR509 from SD013000080 to SD013220B80	2009-1105	to DVT
26	+CPU_COREP, EMI request.	EMI request add snubber for +CPU_COREP to PASS EMIU test.	0.2	45	Add PR499/PR512 SD001470B80 S RES 1/4W 4.7 +-5% 1206 Add PC347/PC359 SE024681J80 S CER CAP 680P 50V J NPO 0603	2009-1105	to DVT
27	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PL40/PL41 from SH000005680 to SH0000012036BM00.	2009-1105	to DVT
28	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PR524/PR525 from SD013120380 to SD013137380.	2009-1105	to DVT
29	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PC362 from SE074391K80 S CER CAP 390P 50V K X7R 0402 to SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
30	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PR501 from SD034536180 S RES 5.36K 0402 1% to SD034549180 S RES 1/16W 5.49K 0402 1%	2009-1105	to DVT
31	+CPU_COREP, EMI request.	+CPU_COREP, EMI request.	0.3	45	Add PC388 SE074102K80 S CER CAP 1000P 50V K X7R 0402	2009-1113	to DVT
32	+CPU_COREP, EMI request.	+CPU_COREP, EMI request.	0.3	45	Add PC389 SE074222K80 S CER CAP 2200P 50V K X7R 0402 Add PC390 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1113	to DVT
33	+CPU_COREP, cost issue.	Beuase SF000000G80 will cost uo, change to SF22004M210.'	0.3	45	Change PC343 from SF000000G80 to SF22004M210.	2009-1113	to DVT
34	+CPU_COREP, IMON issue.	Because Intel update IMON RC time constant, update PC348 to 0.068u to meet spec.	0.3	45	Change PC348 from SE076103K80 S CER CAP .01U 16V K X7R 0402 to SE000003J80 S CER CAP 0.068U 16V K X7R 0402	2009-1113	to DVT
35	+3V/+5V cost issue.	Because Nippon cost up thier OS-CON cap, so we change Nippon cap to Sanyo cap by sourcer request.	0.4	38	Change PC233/PC237 from SF22001M300 S ELE CAP 220U 6.3V M F60(6.3X5.7) PXC to SF22001M200 S ELE CAP 220U 6.3V M B C6 SVPC ESR15	2009-1118	to DVT
36	+1.05VS_VTTP issue.	HW request to increase +1.05VS_VTTP voltage.	0.4	43	Change PR472 from SD034649180 to SD034511180.	2009-1118	to DVT
37	+1.05VS_VTTP issue.	HW request to increase +1.05VS_VTTP voltage.	0.4	43	Chnage PR476 from SD034665180 to SD034649180.	2009-1118	to DVT
38	+0.75VSP power sequence issue.	HW request to adjust power sequence.	0.4	47	change PR409 from SD028000080 S RES 0 0402 5% to SD028200280 S RES 1/16W 20K 0402 5%.	2009-1118	to DVT
39	+1.05VS_VTTP issue.	+1.05VS_VTTP choke unique to +1.5VP.	0.4	43	Change PL38 from SH000008V80 S COIL 1UH +-20% PCMB103E-1R0MS 20A to SH000009U00 S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A	2009-1118	to DVT
40	+1.05VS_VTTP 2nd source issue.	In order to phase in 2nd source, change ISL6268 to APW7138.	0.5	43	Change PU26 from SA00001HT80 S IC ISL6268CAZ-T SSOP 16P to PU999 SA000020600 S IC APW7138NITRL SSOP 16P	2009-1208	to PVT
41	+1.05VS_VTTP 2nd source issue.	APW7138 needn't pop PC335.	0.5	43	Delete PC335 SE075103K80 S CER CAP .01U 25V K X7R 0402 and change location to PC999.	2009-1208	to PVT
42	HDD LED flash issue.	HDD LED will flash when plug in adapter, because +3VS rise a little. HW request add PC224 to solve it.	0.5	37	Add PC224 SE000000K80 S CER CAP 1U 6.3V X5R 0402	2009-1208	to PVT
43	HDD LED flash issue.	If add PC224, must change PR330 from 0 to 1K to avoid SPOK pin fail. that is add a current limit R on SPOK pin.	0.5	37	Chnage PR330 from SD028000080 to SD028100180.	2009-1208	to PVT
44	BOM error.	+1.8VSP choke use wrong material. Unique MP2121 to other project.	0.5	41	Change PL30 from SH000006180 S COIL 2.2UH +-20% PCMC063T -2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A Add PR554 SD028000080 0 0402 5%	2009-1208	to PVT
45	+1.05VS_VTTP issue.	HW request to adjust +1.05VS_VTTP Vout.	0.5	43	Change PR472 from SD034511180 to SD0344999180.	2009-1208	to PVT
46	+VGFX_COREP issue	ISL62881 common circiut update.	0.5	44	Delete PR291 SD028000080. Add PR555 SD028000080.	2009-1208	to PVT

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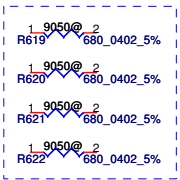
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Sequense issue.	Modify sequense by HW request.	0.6	37	Chnage PR330 from SD028100180 S RES 1/16W 1K +-5% 0402 to SD028000080 S RES 1/16W 0 +-5% 0402.	2010-0112	to Pre-MP
25	Sequense issue.	Modify sequense by HW request.	0.6	37	Delete PC224 SE000000K80 S CER CAP 1U 6.3V K X5R 0402	2010-0112	to Pre-MP
26	EMI issue.	Because EMI has power BB on 250MHz, add HS gate R to solve.	0.6	45	Add PR556/PR557 SD013220B80 S RES 1/10W 2.2 +-5% 0603	2010-0112	to Pre-MP
27	BOM loss update in DVT.	BOM loss update in DVT, change 1.8V choke.	0.6	41	Change PL30 from SH000006180 S COIL 2.2UH +-20% PCMC063T-2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A	2010-0112	to Pre-MP
28	Common circiut update.	GFX_COREP common circiut update.	0.6	44	Add PR291 SD028000080 0 0402 5% Delete PR555 SD028000080 0 0402 5%	2010-0112	to Pre-MP
29	Changer choke issue.	Because Cyntec has quality issue and can't use in MFG, in order to prevent shortage issue, change to Maglayer.	0.6	39	Chnage PL29 from SH000005280 S COIL 10UH +-20% PCMB104T-100MS 6A to SH000009R00 S COIL 10UH +-20% MMD-10DZ-100M-X1 6A	2010-0112	to Pre-MP
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Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1			09 / 30	Q9 / Q15 / Q65 / Q14 / Q36 / Q19 / Q31 / Q56 / Q57 Change to SB000000AR10 Q4/Q5/Q6/Q7/Q13/Q24/Q25/Q59/Q61/Q62/Q63/Q20 Change to SB570020120	
2	DVT		11 / 03	Modify WWAN Mini catd PIN define. X1 / X2 Change to SJ132P7KW10. Add PCH SUSCLK net for remove EC crystal. Remove C147. Add F2 for RF team. Add C670 / C671 / C672 / C673 For INTEL Change C217 to 22U and add C221 22U for CRT issue.	
			11 / 05	Add P80DATA PD 100Kohm(R51) for EC common design. Add C40 / C41 / C42 / C43 / C44 for EMI. Add ACIN#(Q16) for ACIN LED(NEW60) Add C45 / C46 / C47 / C48 for LAN Common mode noise Remove net BT_LED#.	
			11 / 09	Add R14 for MINI1 LED Function.	
			11 / 10	Add D13/D14/D16/D23/D24/D25/D26/D30 for ESD Add R836/C760 R338/C585 for RF. L21 Change to SM010012010 L5 Change to SM01000AX00 Change R619/R621 to 680ohm Change R620/R622 to 3.9kohm Y1 Change to SJ100009R00 R841 Change to 8.2k ohm Update Power SCH Change T1 to SP050006B00 Change PCH P/N to SA00003N7B0 Change R167 to 470 ohm. Update Power SCH	
			11 / 11		
			11 / 16		
			11 / 16		
			11 / 17		
			11 / 18		
			11 / 19		
3	PVT		12 / 07	C259 / C279 / C692 / C693 Change to SE107475K80 0603 type Reserved R15 (net LOCAL_DIM) / R16 (net COLOR_ENG_EN) for LVDS function. Reserved R307 for +LCDVDD. EC Pin36 for WLAN_LED# (output), Pin 17 for MINI1_LED# (input) EC Pin91 for 36_LED#(output) & Pin85 for WWAN_LED# (input) Update Power SCH	
			12 / 09	Update Power SCH Add R96 PD 100K for LVDS Panel issue. Add C674 / C675 / C676 For EMI. Del SW3 Power on SW Update Power SCH US change to SA00000U500 R619 / R621 change to 2.2K SD028220180 for LED Q13 / R477 Change to unpop R171 Change to pop,R172 change to unpop for Board ID. Add R777 / R778 For HDMI Issue.Only pop R778. R751 Change to 2.2K.	
			12 / 10		
			12 / 11		
			12 / 14		
			12 / 16		
			12 / 17		
4	PRE MP		01 / 06	ADD PU R951 / R953 UNPOP D23 for MIC noise issue. UNPOP R827 / R828, ADD L7 SM070001600 for USB. Update Power SCH	
			01 / 11	Change Q9,Q65,Q15,Q14,Q36,Q19,Q31,Q56,Q57 to SB000000DH00 Change LED1 / LED3 to SC591NB5A30 Del L7 Add R827 / R828. Del D26 / D25 Update Power SCH	
			01 / 21		

For NEW50 / NEW90 LED



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