

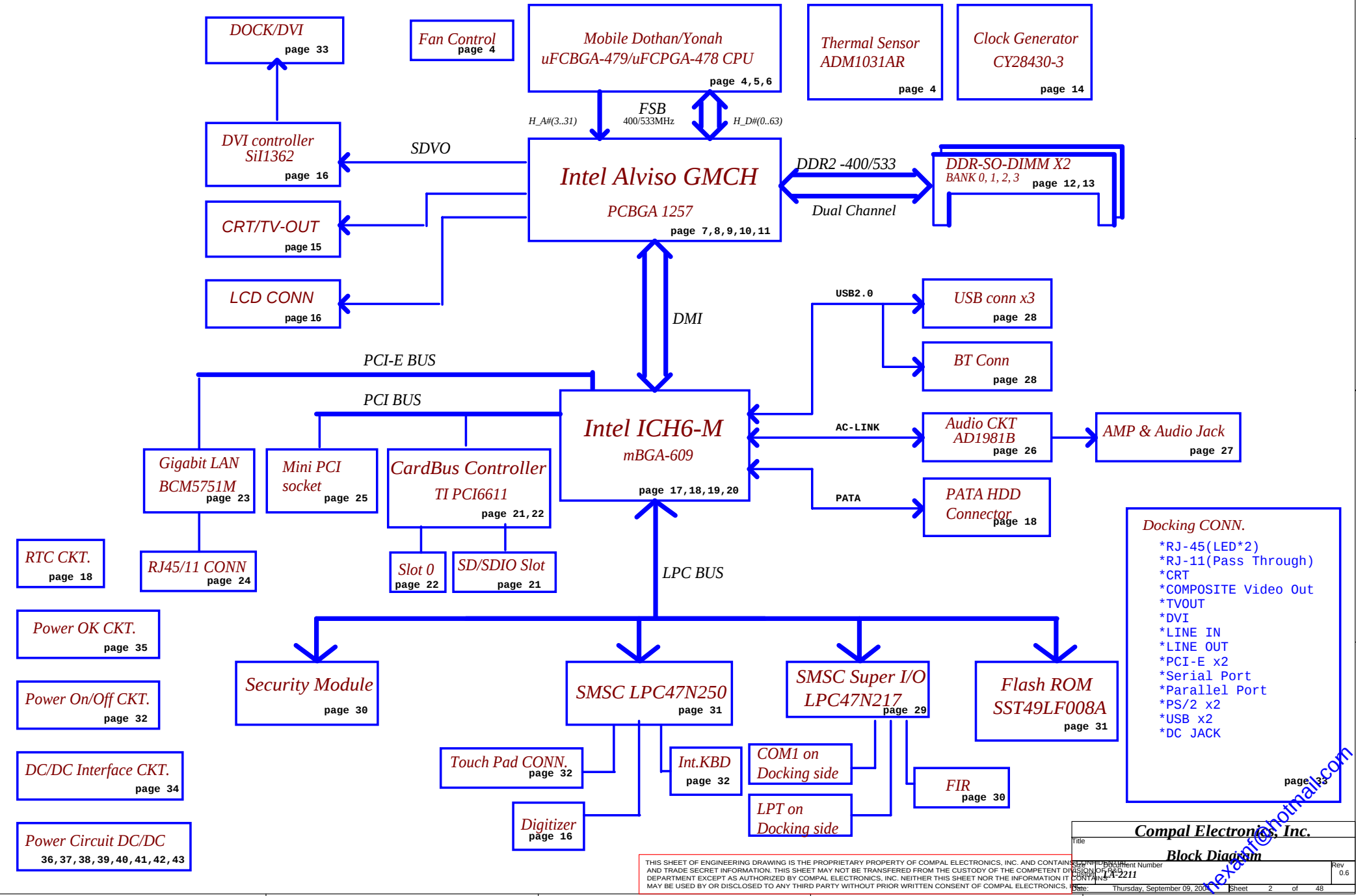
Compal confidential

Schematics Document Mobile Dothan uFCBGA/uFCPGA with Intel Alviso_GM+ICH6-M core logic 2004-09-09 REV:06

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14-2211			
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Heavenly



Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12Vswitched power rail on power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol note:

-  :means digital ground.
-  :means analog ground.
- @ :means reserved.

Internal PCI Devices

DEVICE	PCI Device ID	IDSEL #
LAN	D8	AD24
Azalia	D27	AD11
PCI-E	D28	AD12
USB1.1/2.0	D29	AD13
PCI to PCI (DMI to PCI)	D30	AD14
AC97 MODEM	D30	AD14
AC97 Audio	D30	AD14
PATA/SATA	D31	AD15
LPC I/F	D31	AD15
SMBUS	D31	AD15

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
Mini-PCI	D4	AD20	0	F
CARD BUS	D6	AD22	2	A B C D

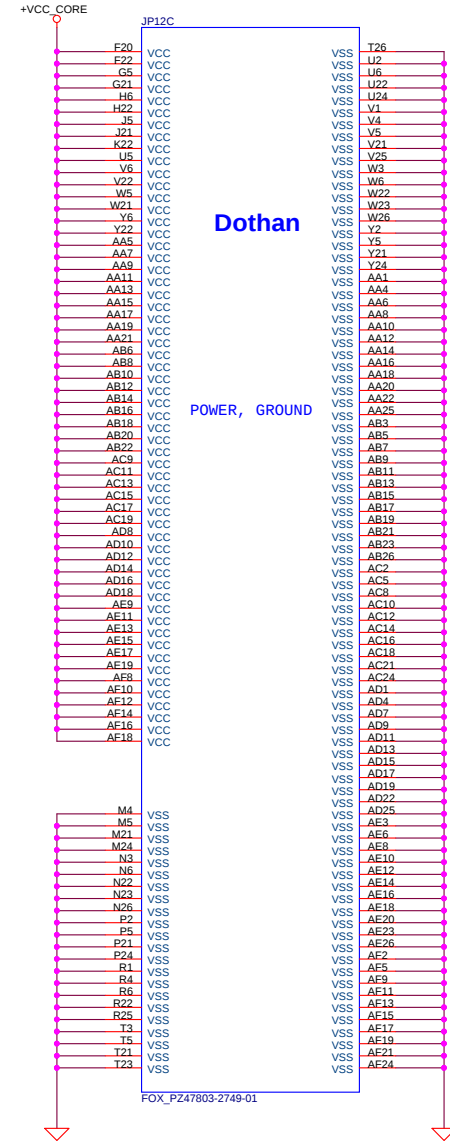
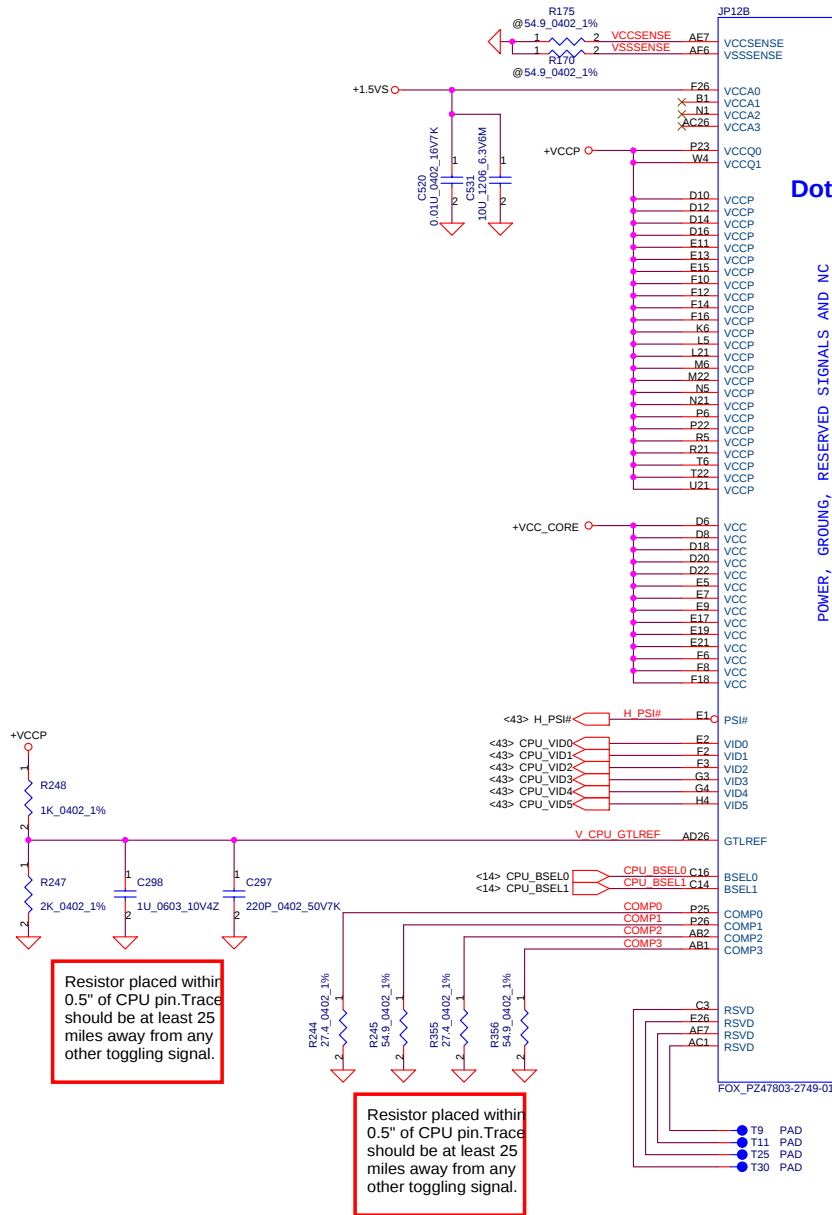
I2C / SMBUS ADDRESSING

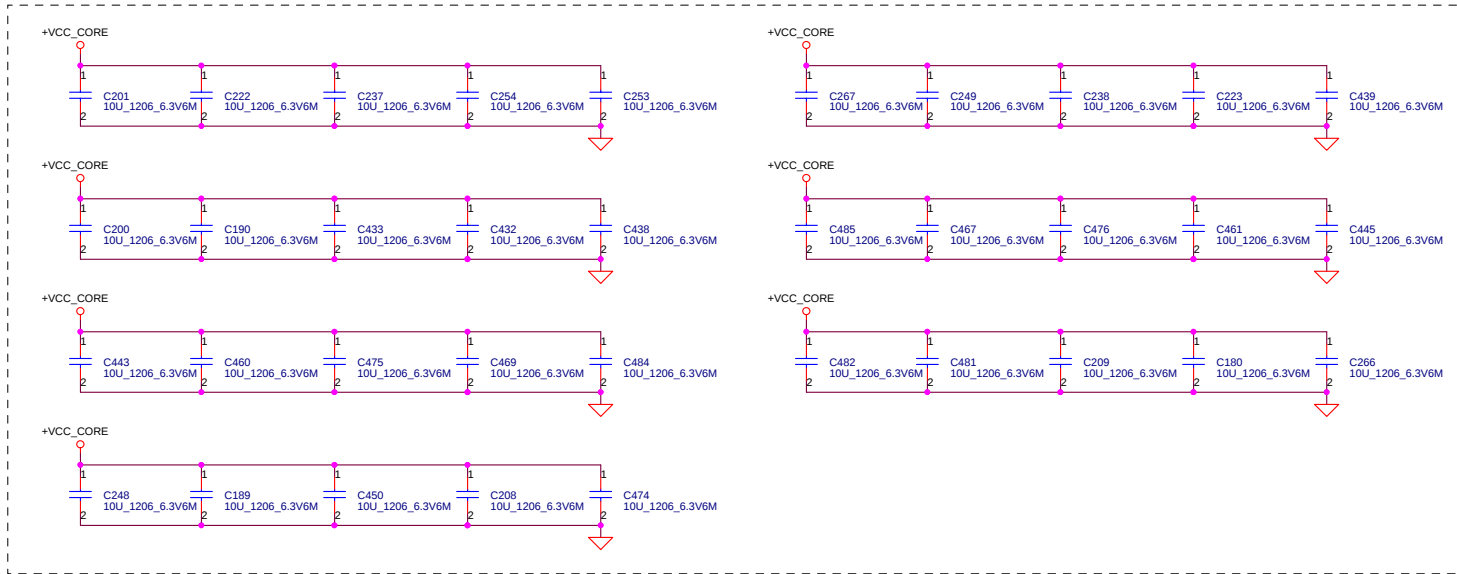
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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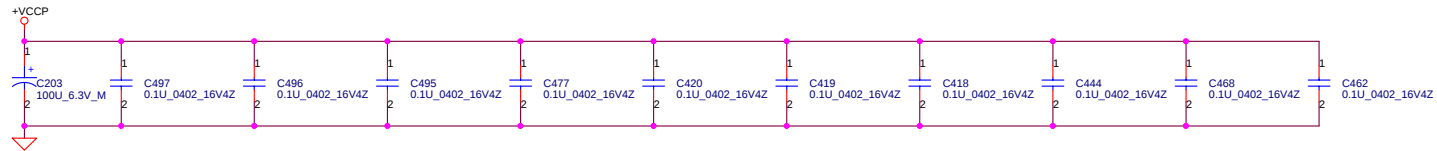
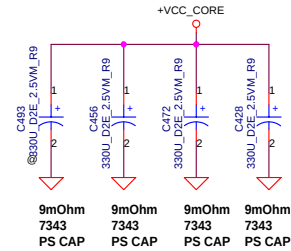
Notes List

Title		Drawing Number		Rev
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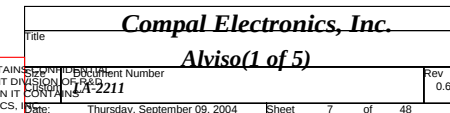


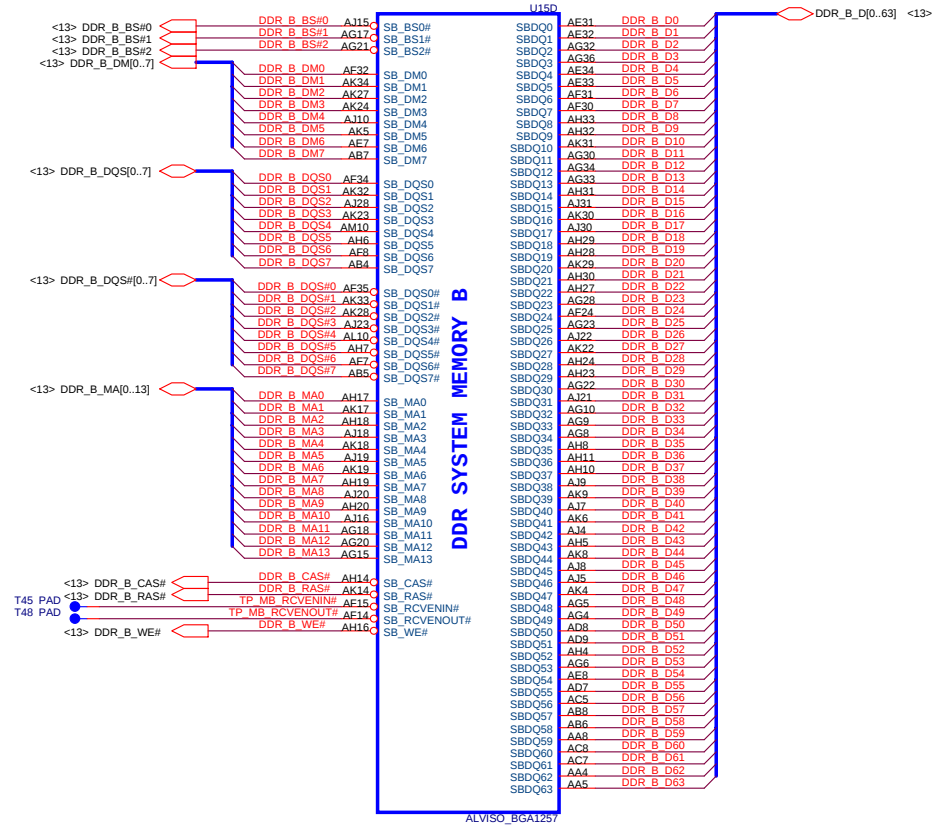


Near VCORE regulator.

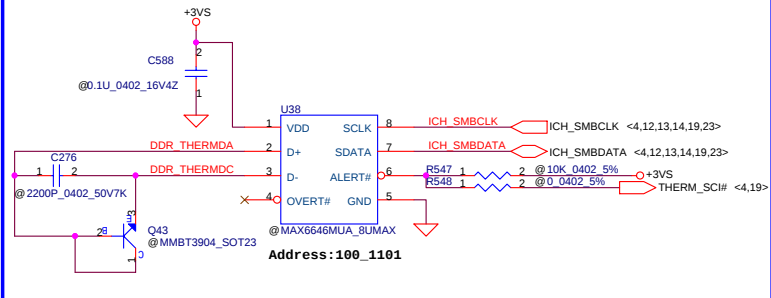


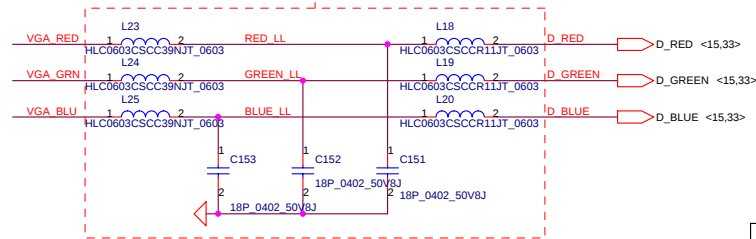
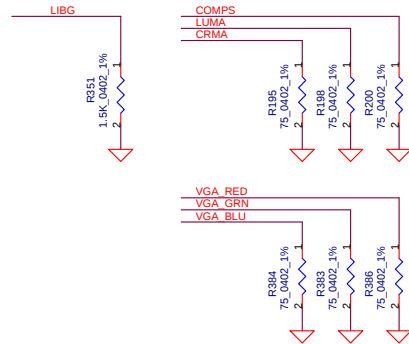
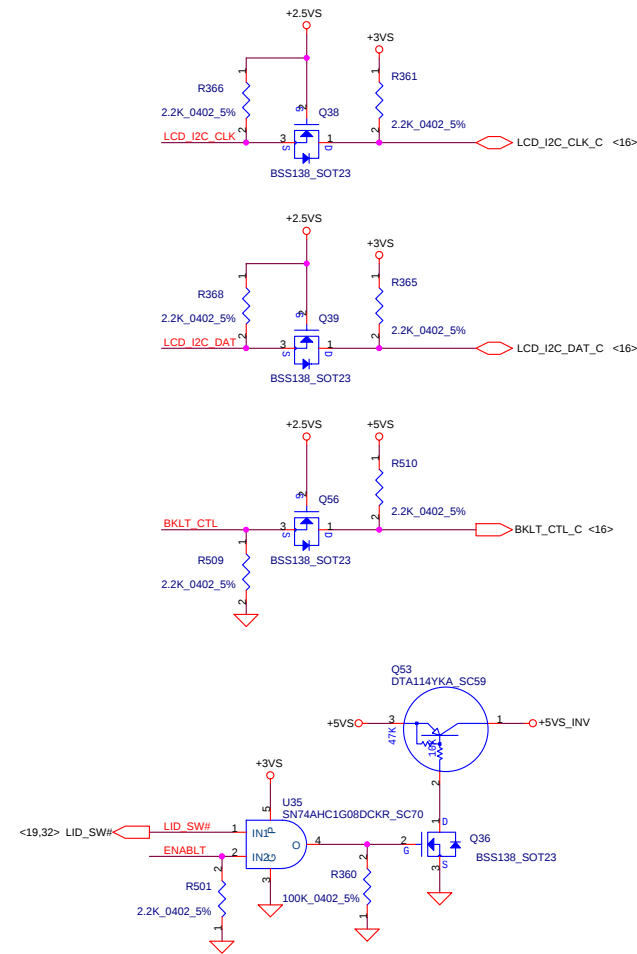
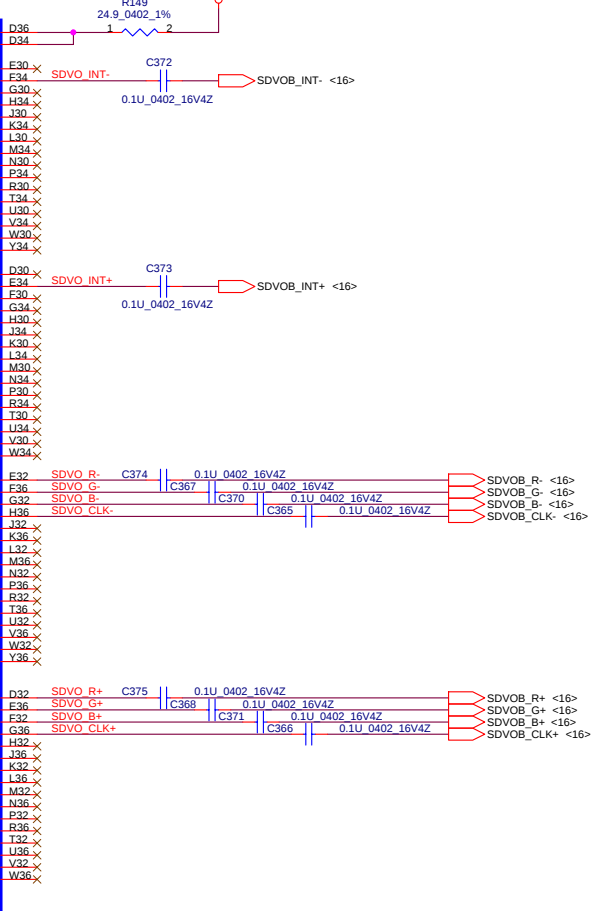
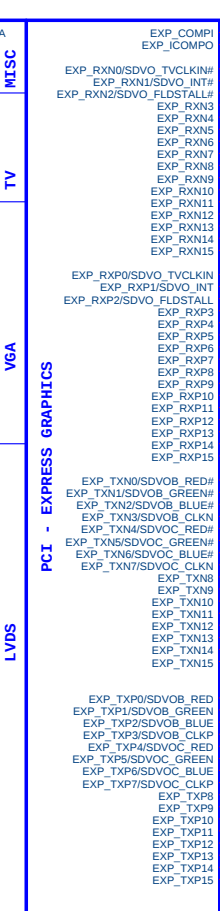
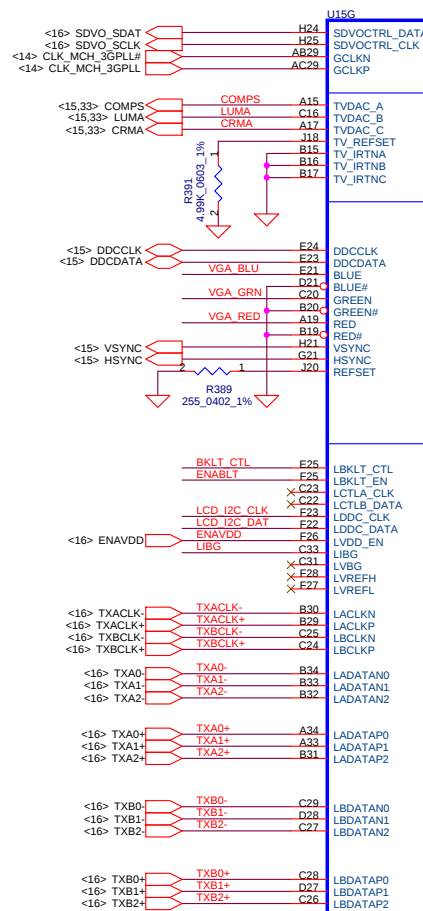
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Reserved thermal CKT and closed to JP34.





Layout Note:
Place these components as close
as possible to Alviso-GM.

 DDR_A_DQS#[0..7]

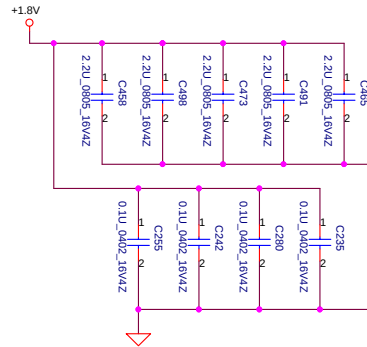
 DDR_A_D[0..63]

 DDR_A_DM[0..7]

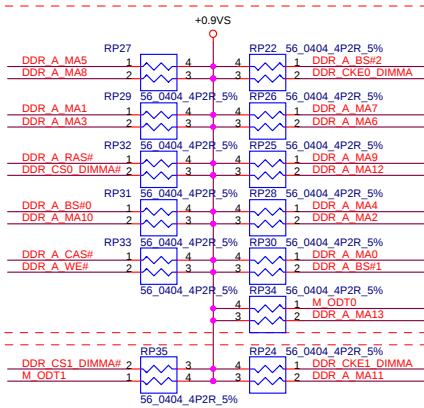
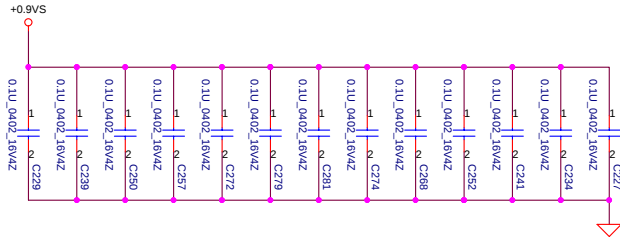
 DDR_A_DQS[0..7]

 DDR_A_MA[0..13]

Layout Note:
Place near JP34

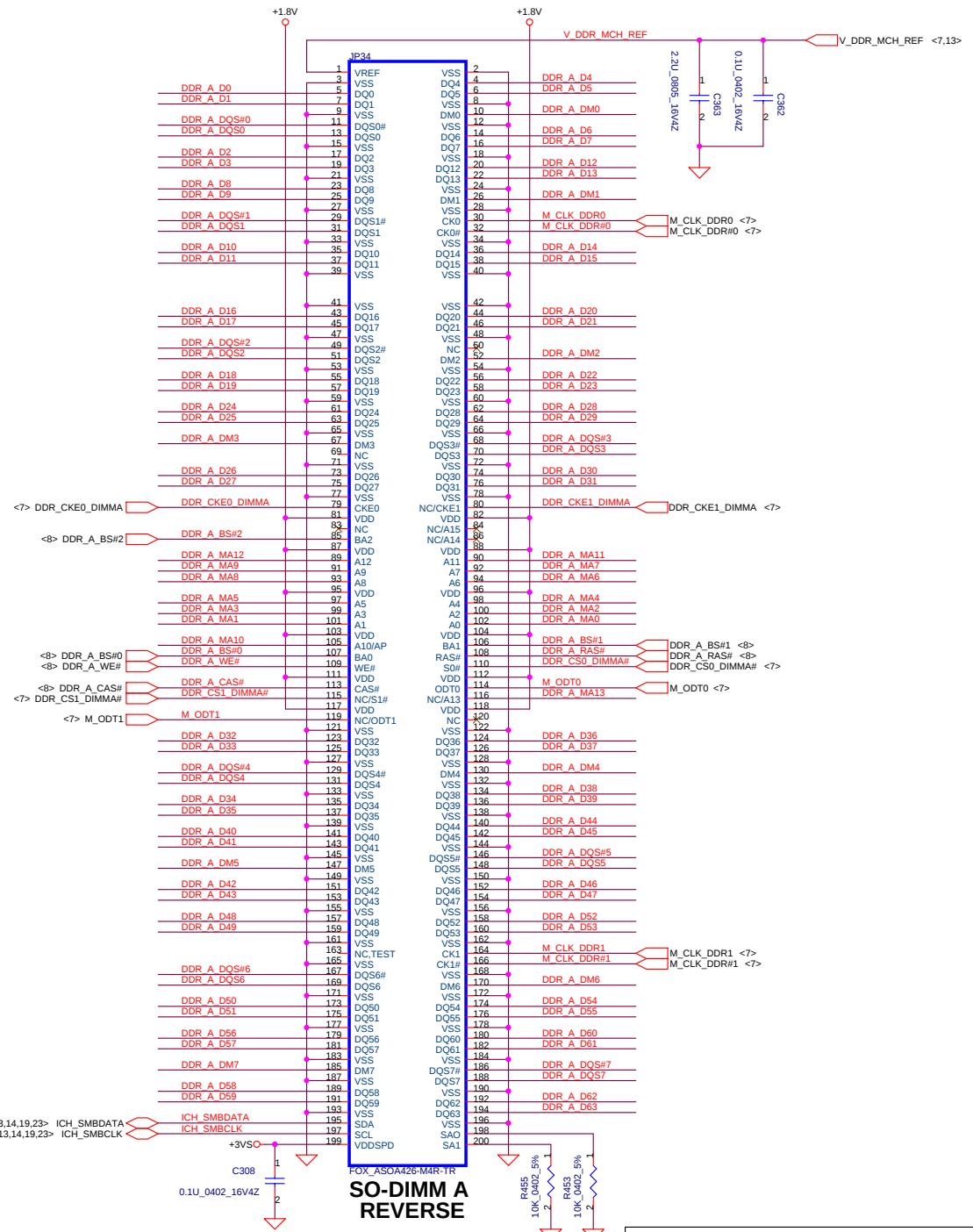


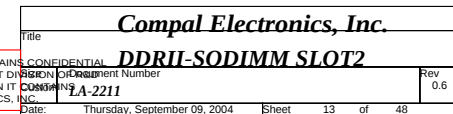
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_VDR_VTT



Layout Note:
Place these resistor closely JP34, all trace length<750 mil

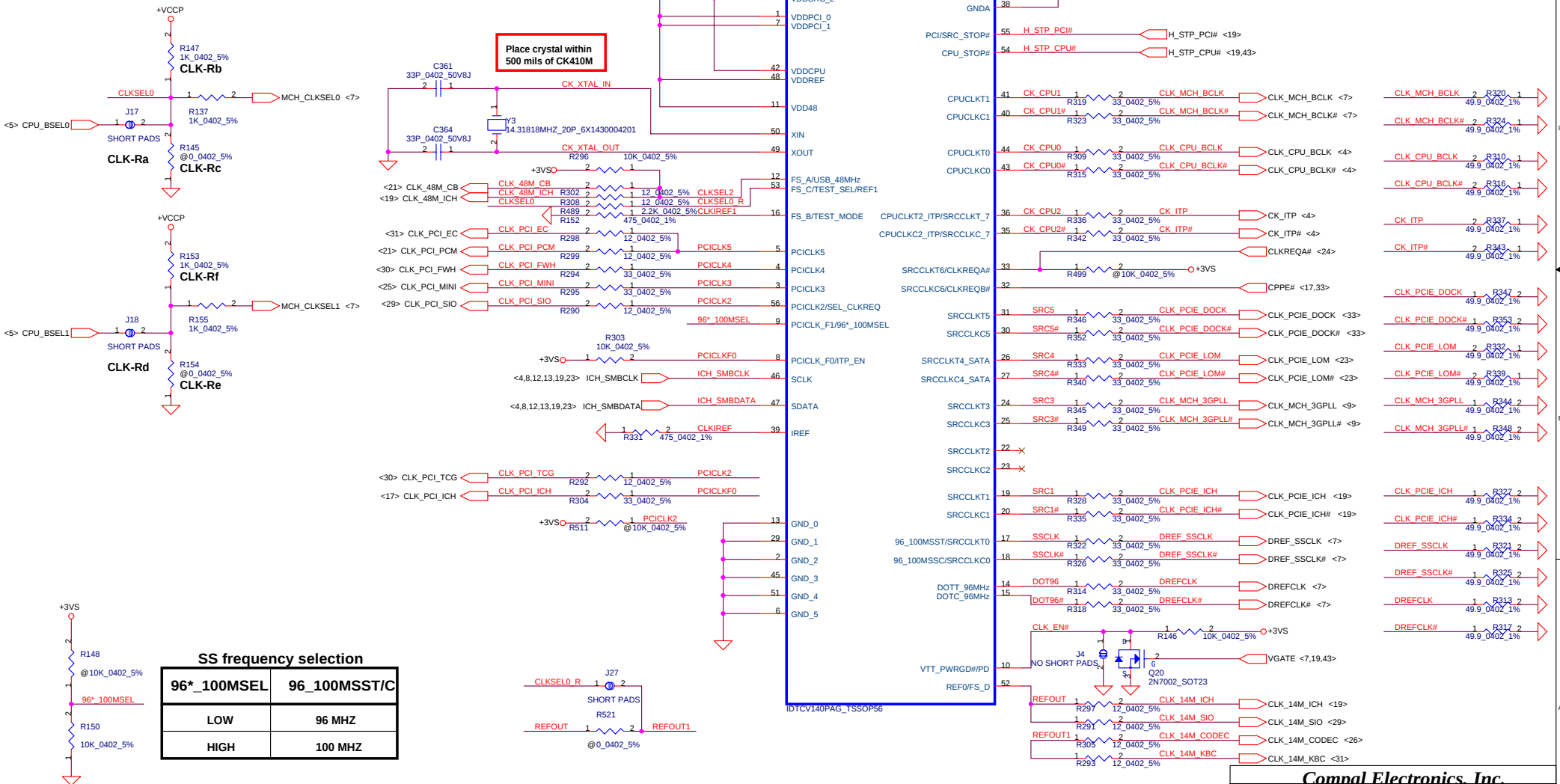
Layout Note:
Place these resistor closely JP34, all trace length Max=1.3"



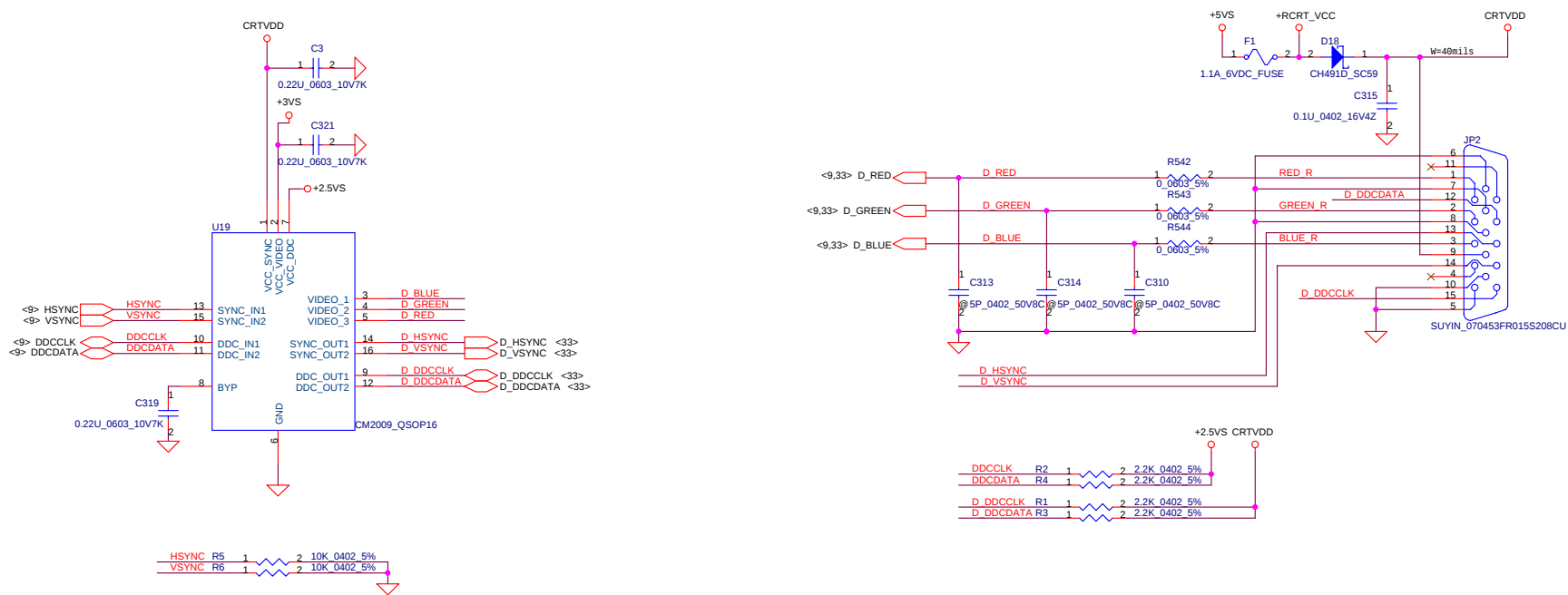


FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
1	0	1	100	100	33.3

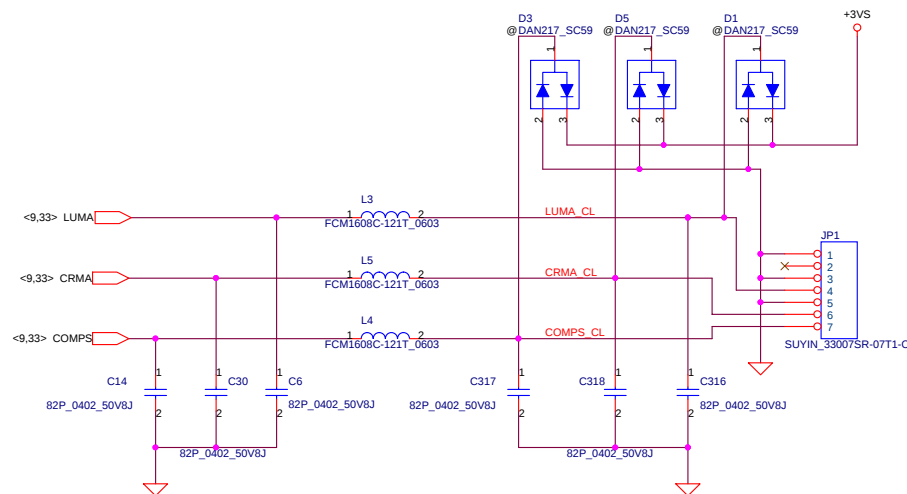
CPU Type	CLK-Ra	CLK-Rb	CLK-Rc	CLK-Rd	CLK-Re	CLK-Rf
Dothan-A PSB400	OPEN	1K Ohm	OPEN	OPEN	0 Ohm	OPEN
Dothan-A PSB533	OPEN	OPEN	0 Ohm	OPEN	0 Ohm	OPEN
Dothan-B	SHORT	1K Ohm	OPEN	0 Ohm	OPEN	1K Ohm



CRT Connector



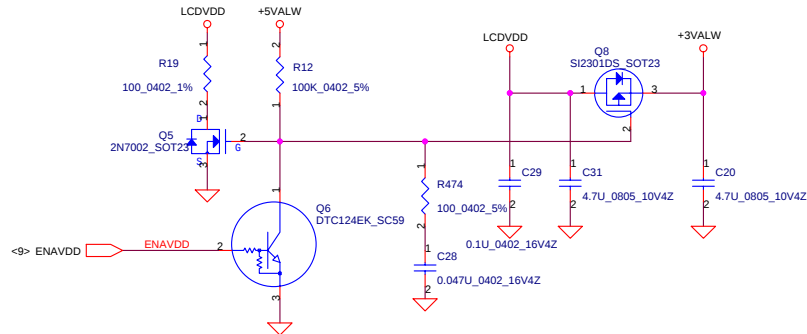
TV-Out Connector



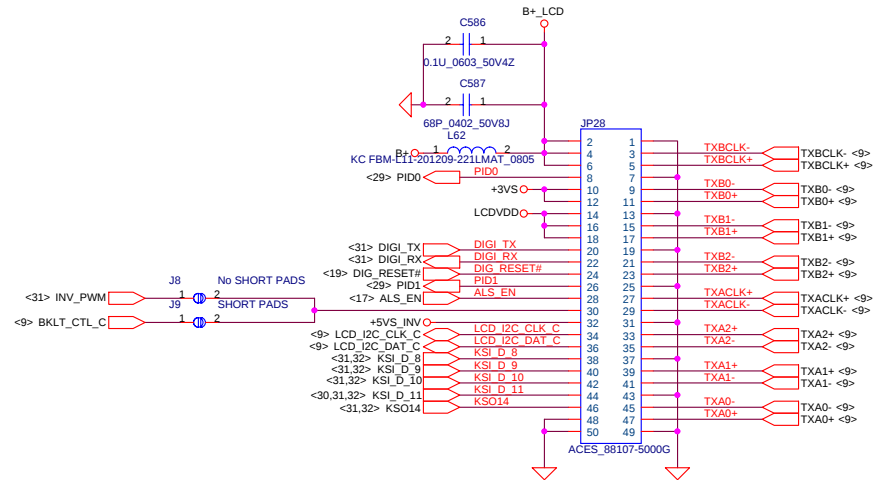
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Title		Compal Electronics, Inc.	
Revision		CRT & TVout Connector	
Drawing Number		LA-2211	
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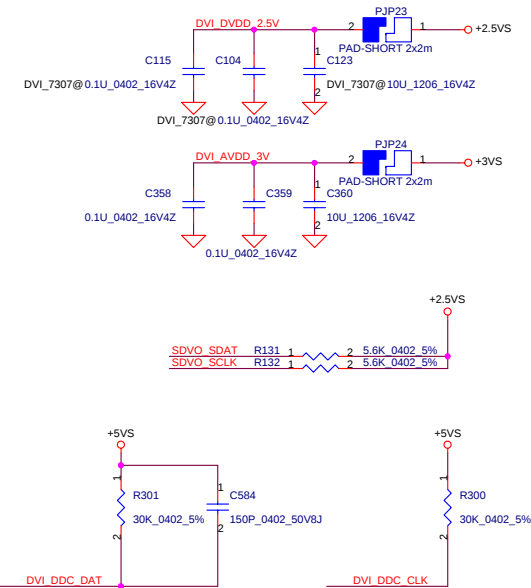
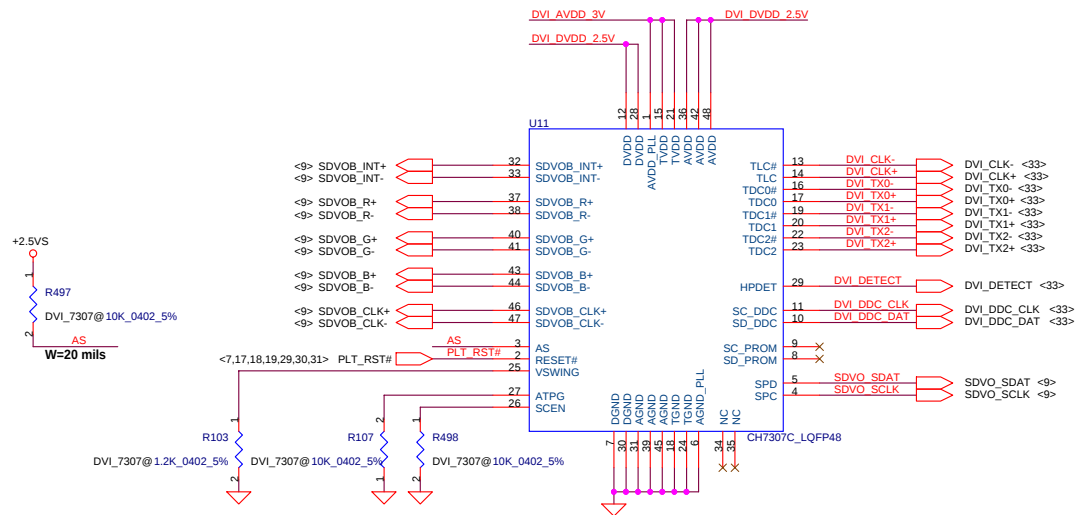
LCD POWER CIRCUIT

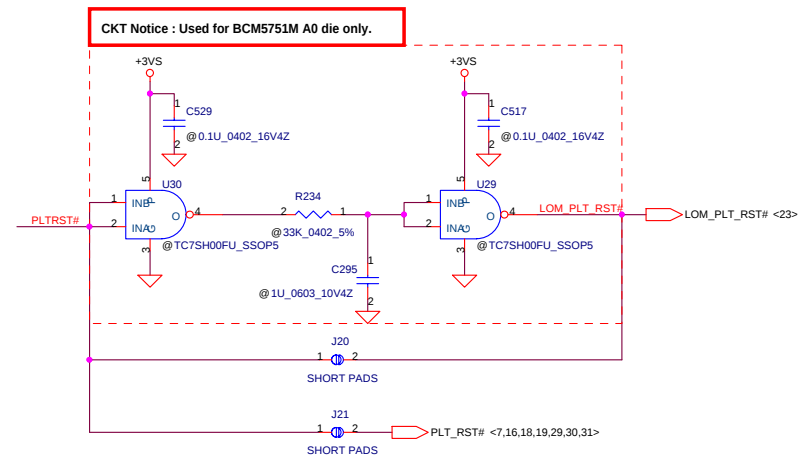
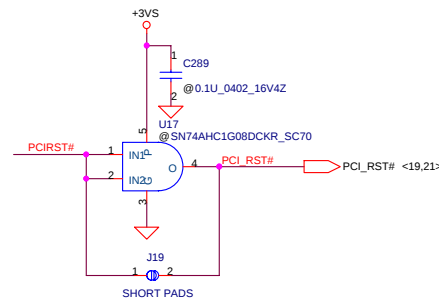
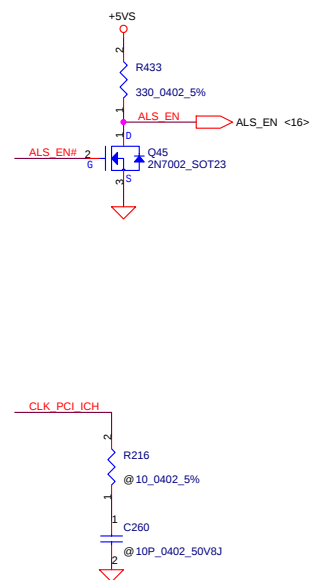
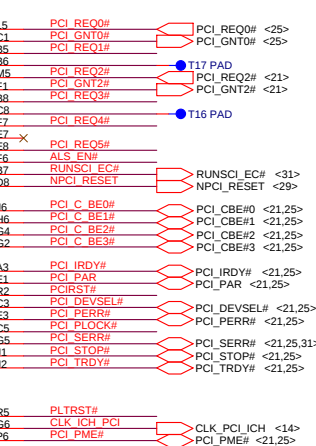
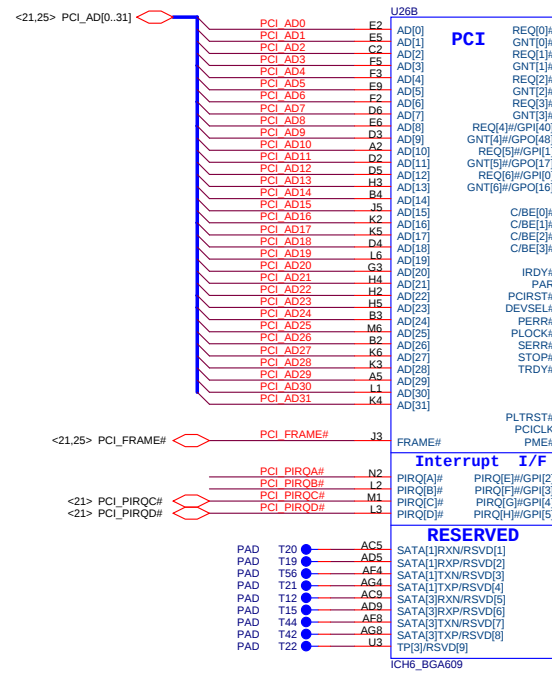
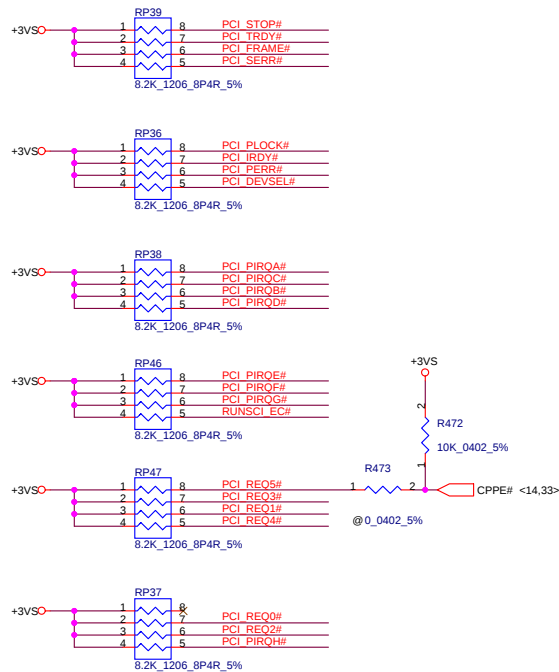


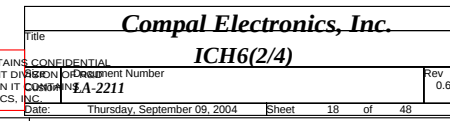
LCD/PANEL BD. CONN.

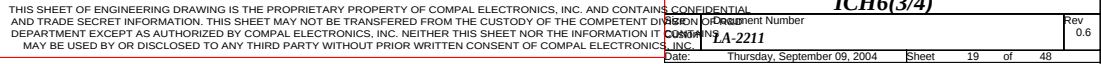


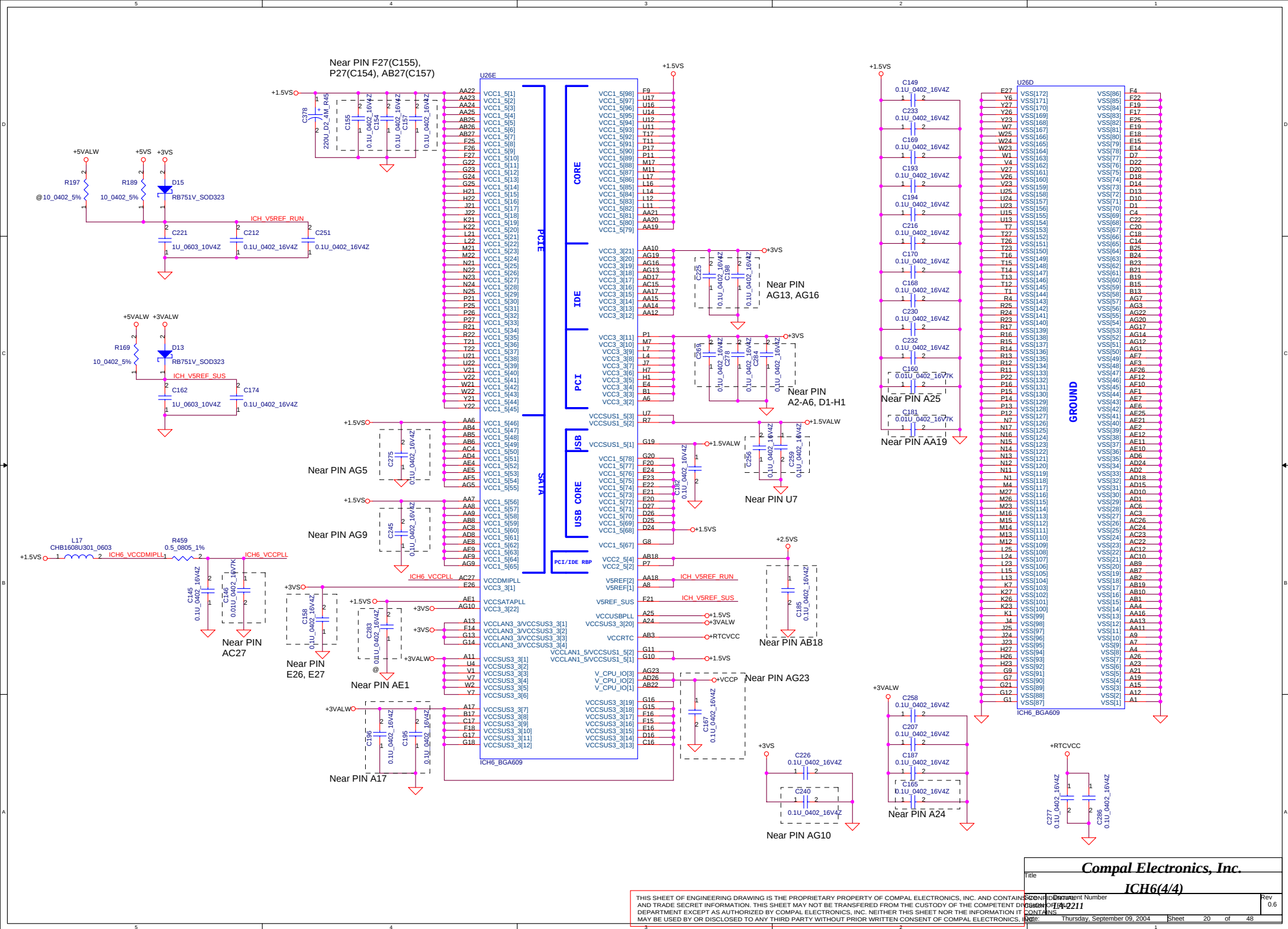
DVI CONTROLLER

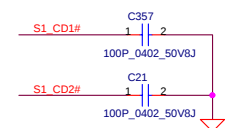
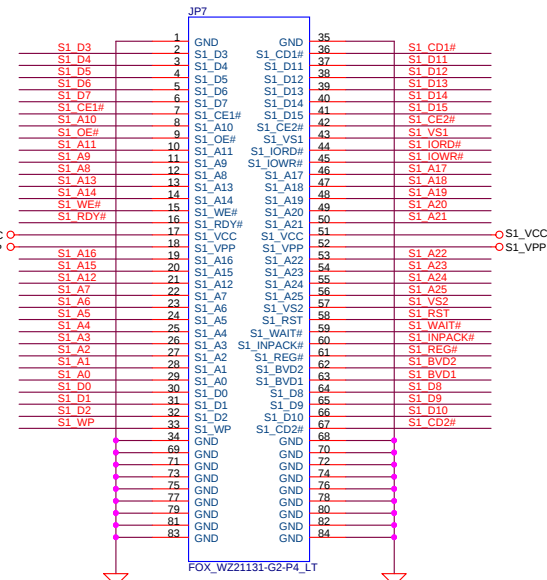


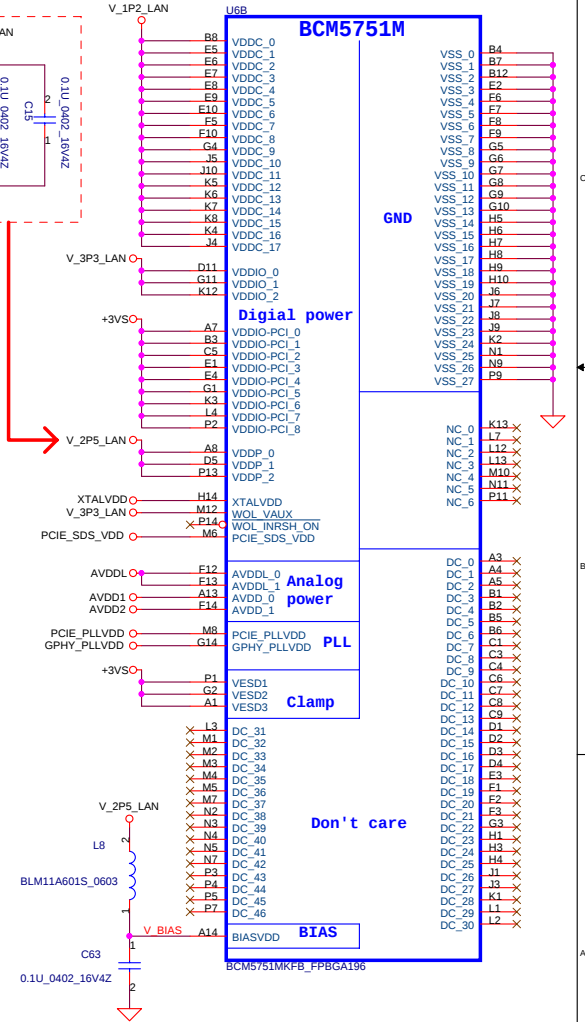
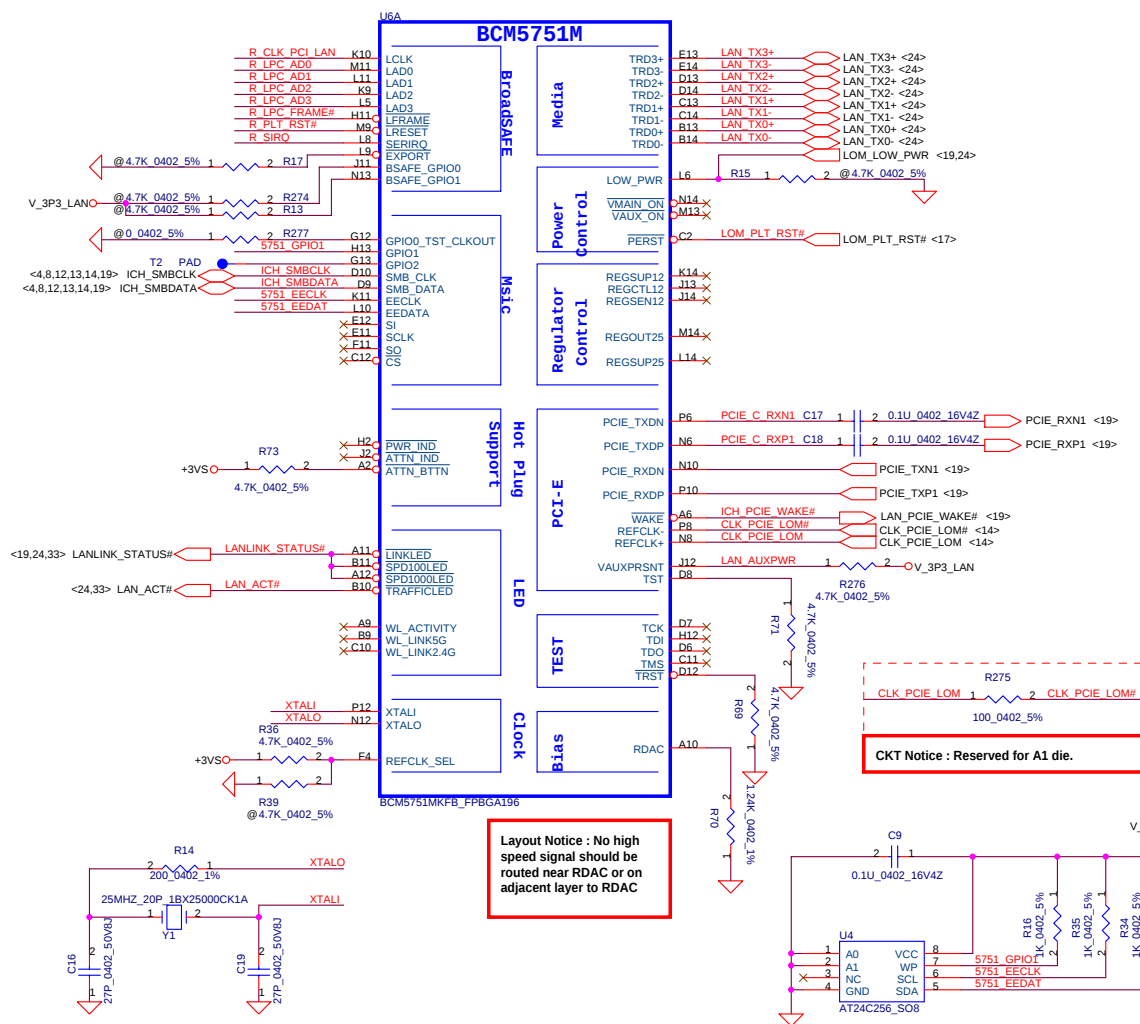
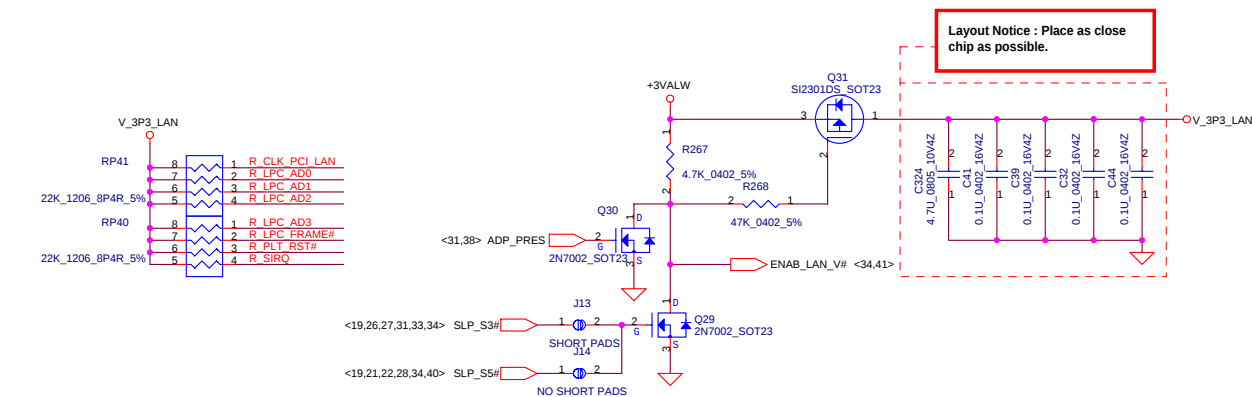


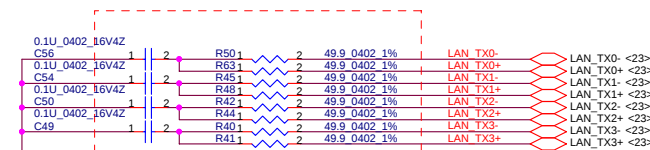
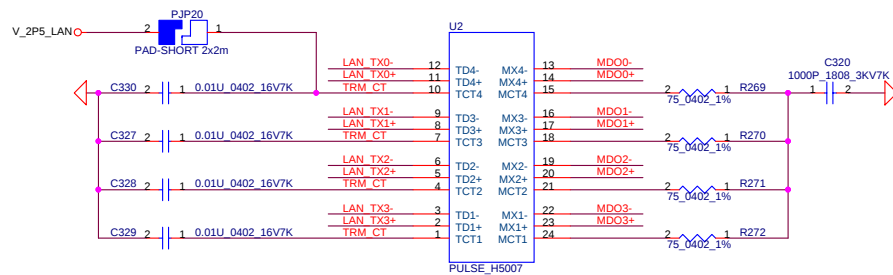




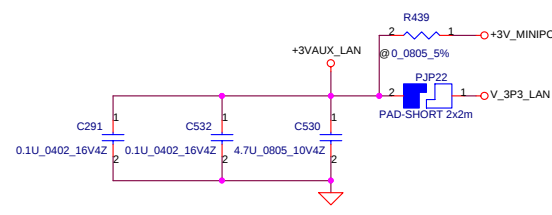
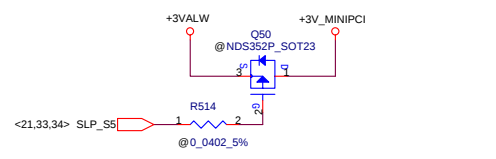
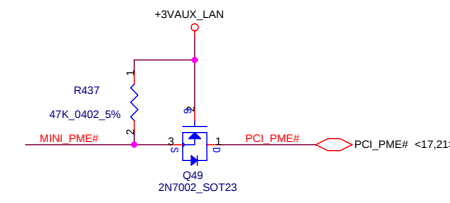
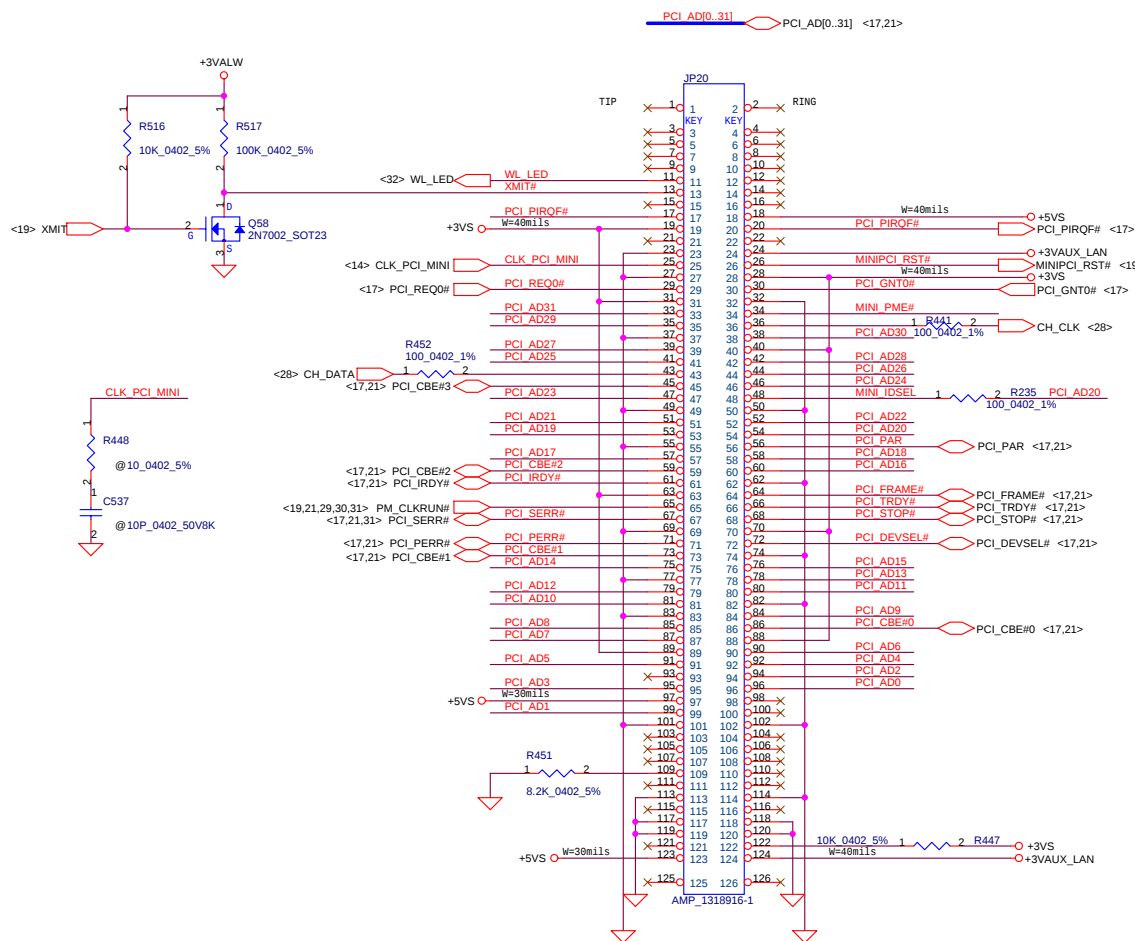
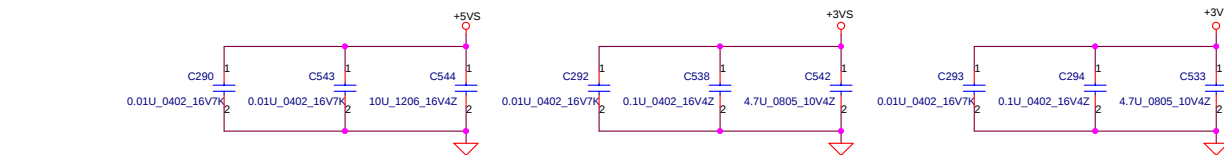


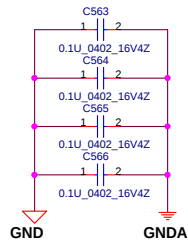
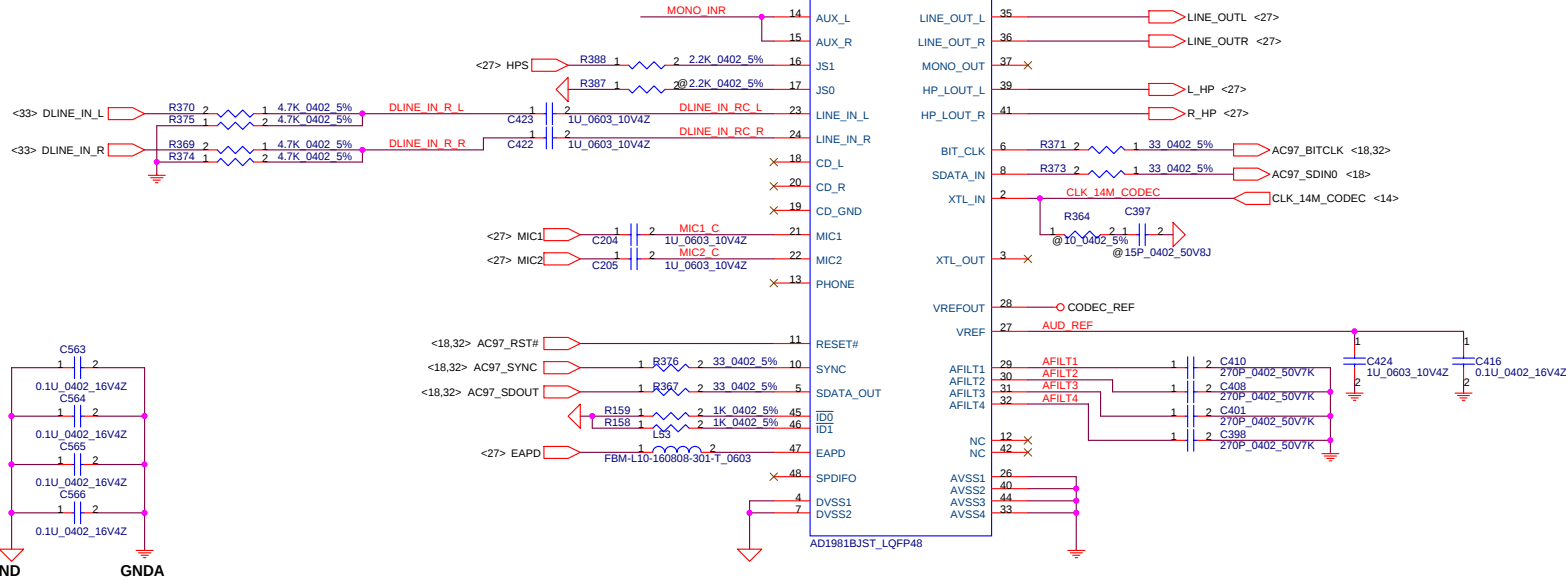
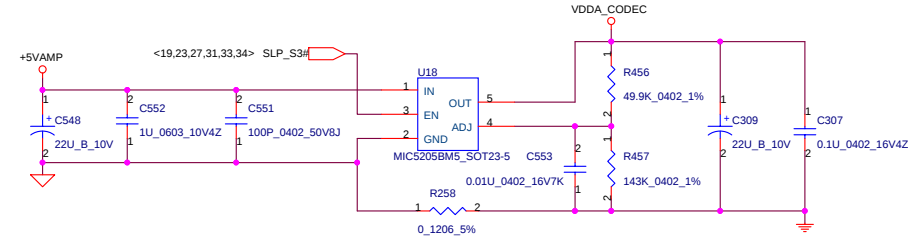
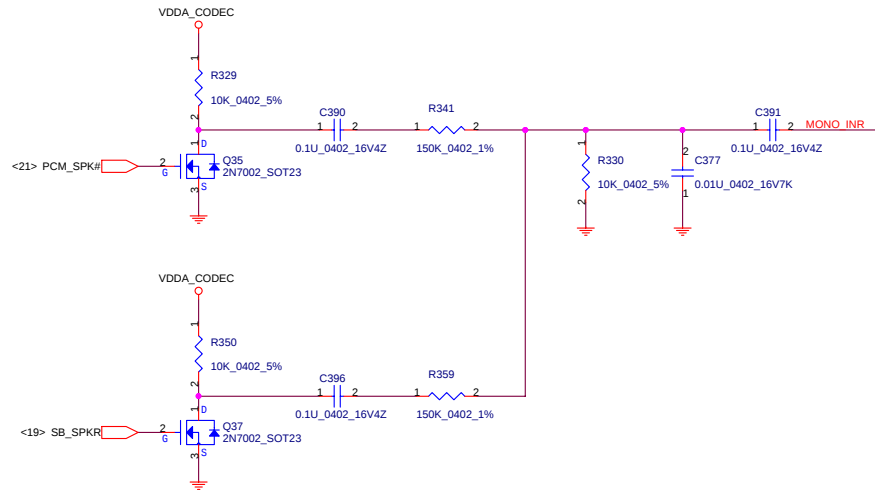






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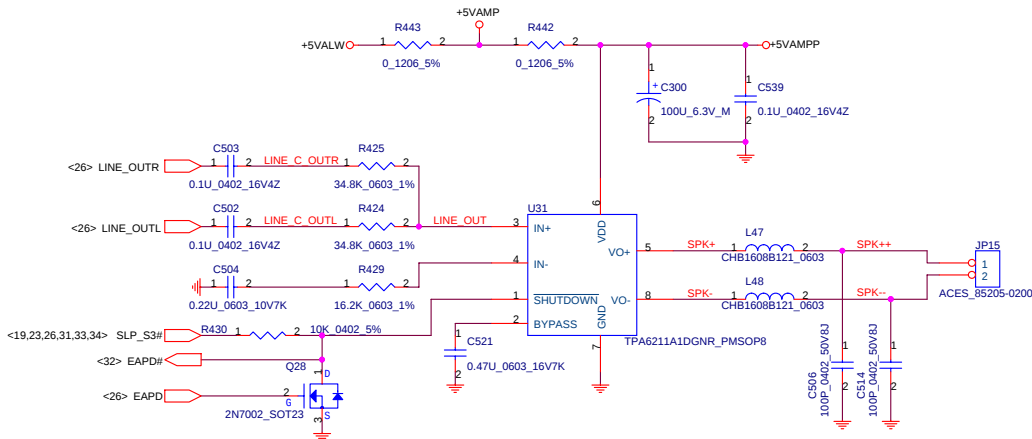




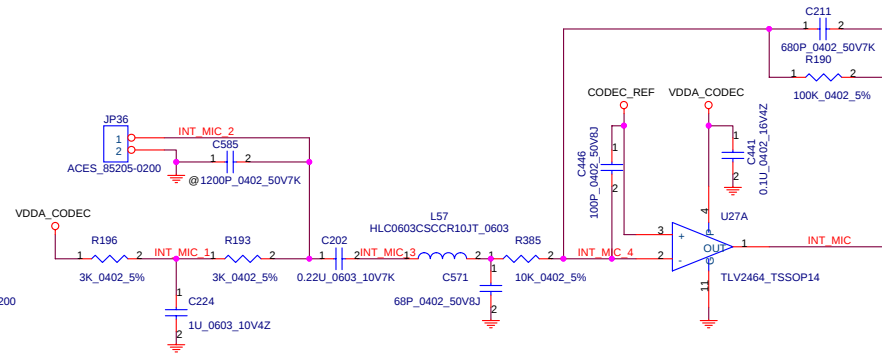
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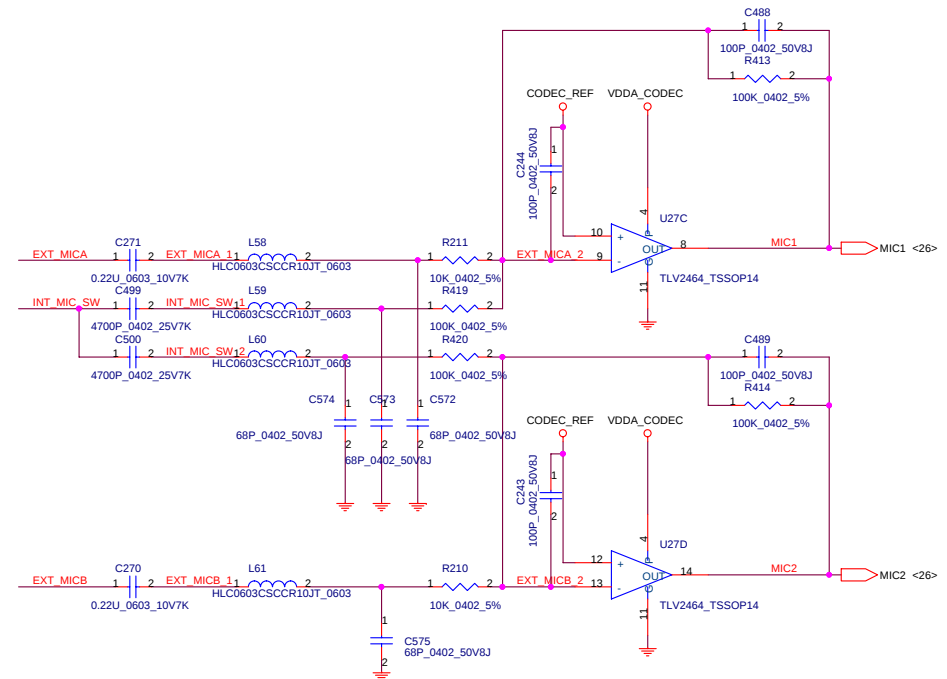
AMP. FOR INTERNAL SPEAKER



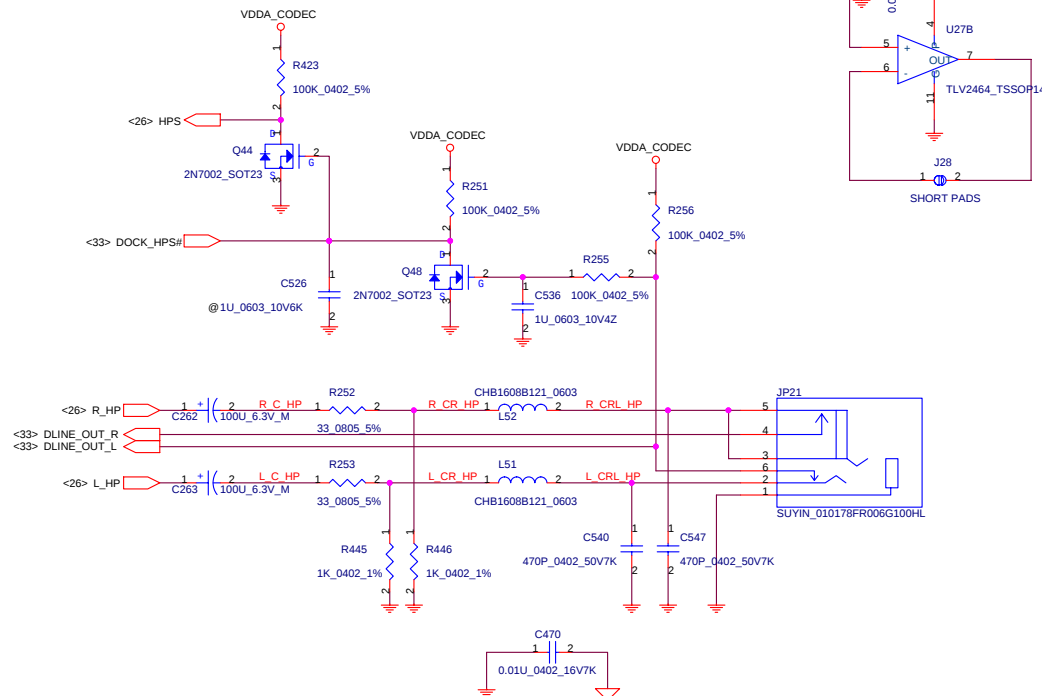
AMP. FOR INTERNAL MICROPHONE



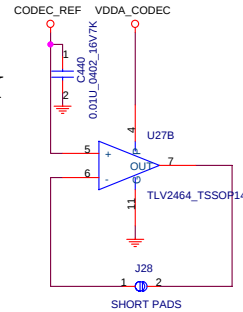
AMP. FOR EXTERNAL MICROPHONE



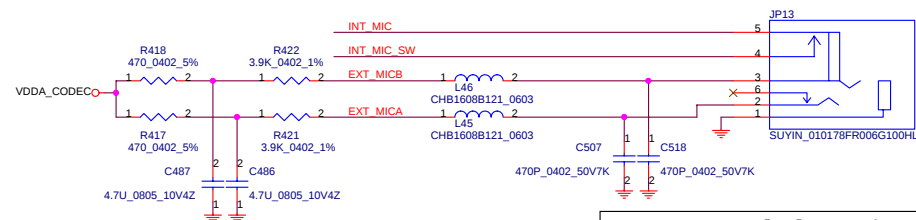
LINE OUT/HEADPHONES AUDIO JACK



UNUSED



EXT. MICIN AUDIO JACK



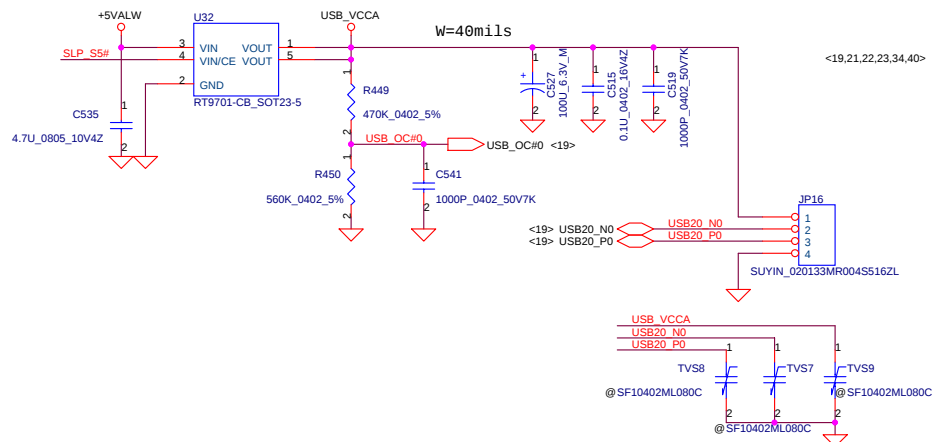
Compal Electronics, Inc.

AMP & Audio Jack

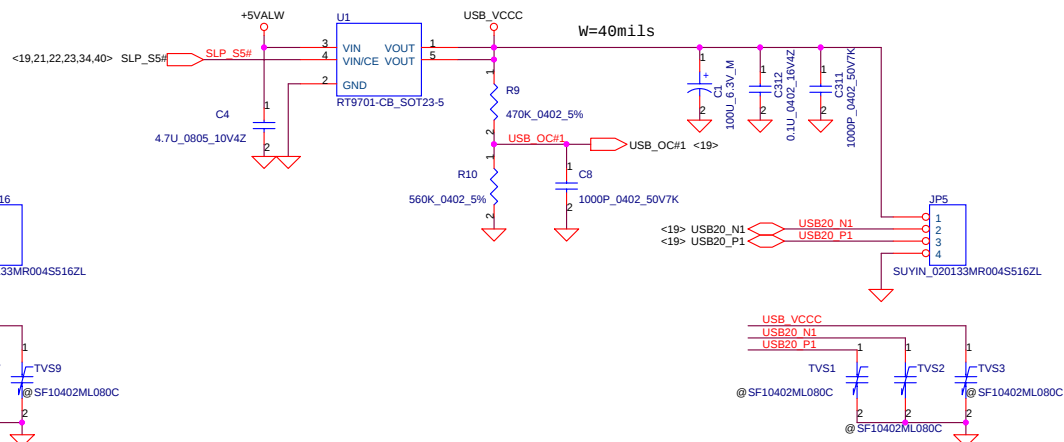
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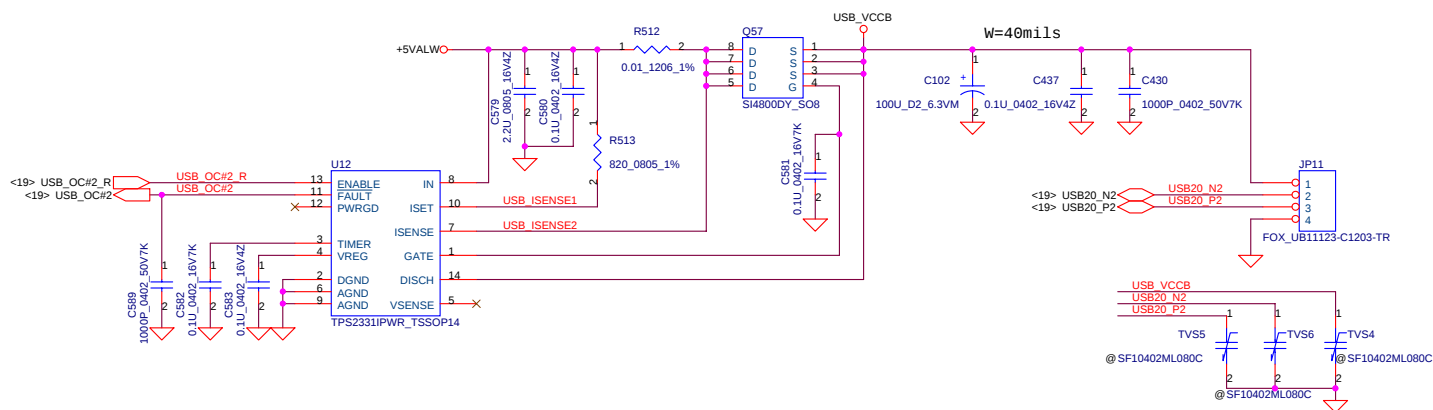
USB CONNECTOR 1



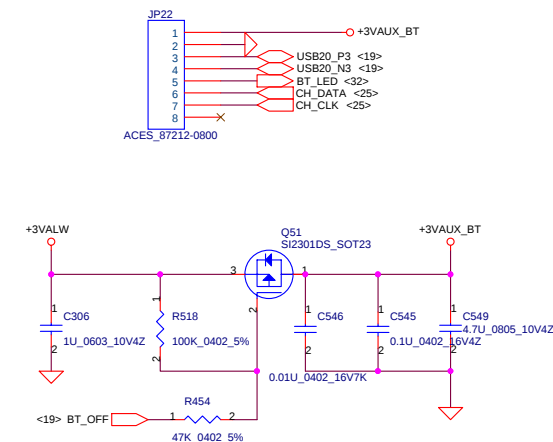
USB CONNECTOR 2



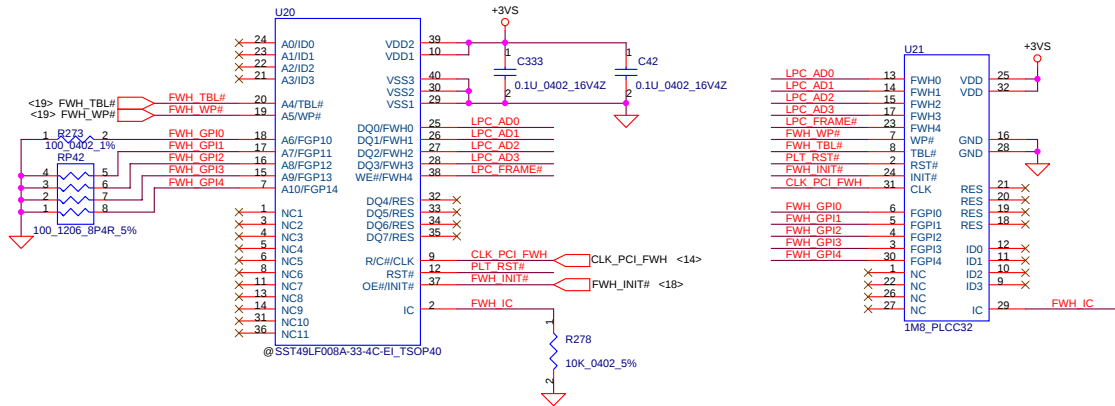
USB CONNECTOR 3



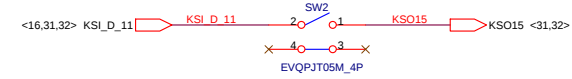
BT Connector



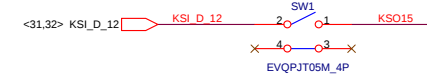
BIOS ROM



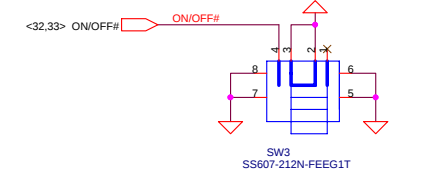
Wireless/BT ON & OFF Button



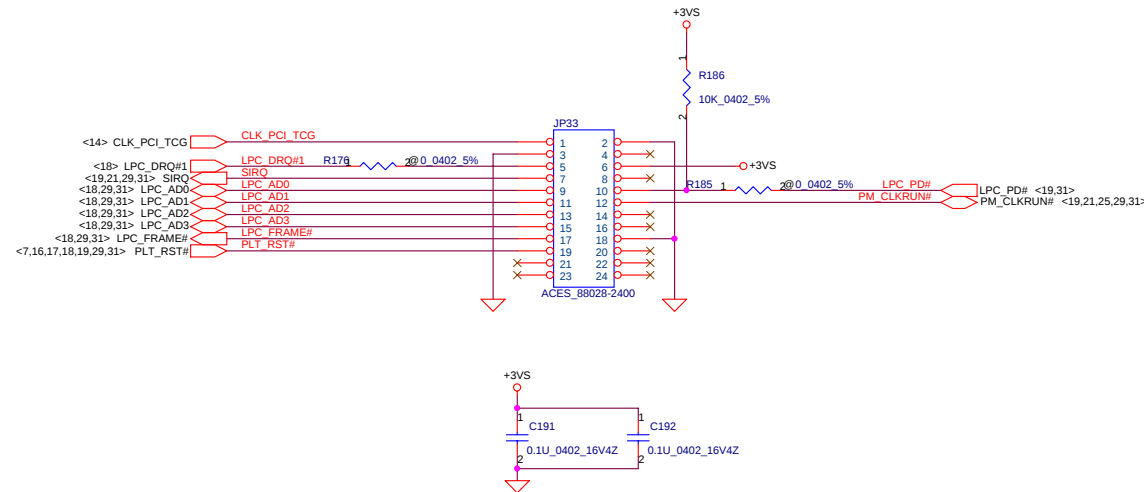
QuickLook Button



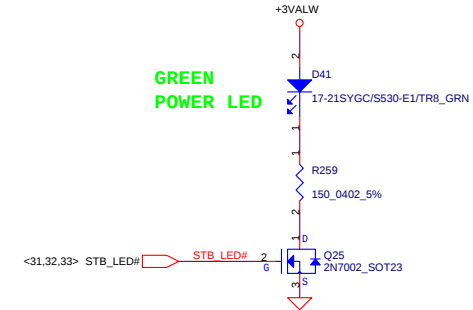
ON/OFF & SLEEP Button



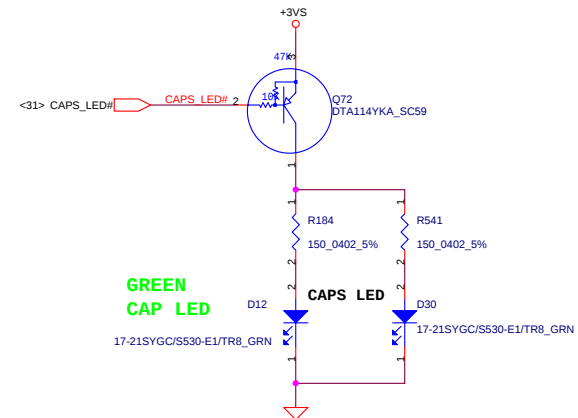
TPM Module

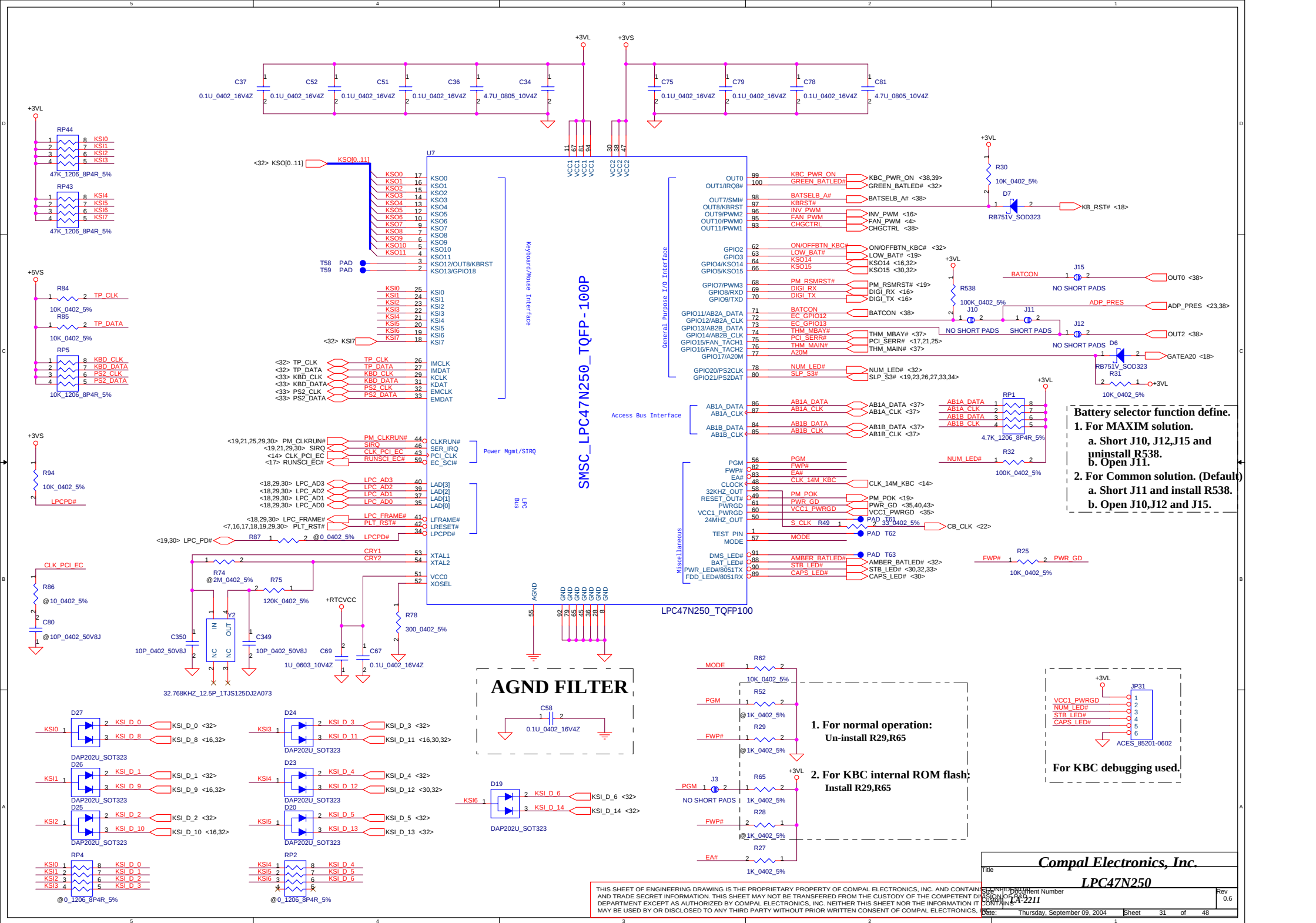


GREEN POWER LED



GREEN CAP LED





FUN BD.

Pinout for the FUN BD. connector (JP9):

Pin	Signal
1	KSI D 8
2	KSI D 9
3	KSI D 10
4	KSI D 13
5	KSO14
6	KSO15
7	LID_SW#
8	EAPD#
9	NUM_LED#
10	NUM_LED#
11	
12	

Power connections: +3VS, +3VALW, +3VAL, +5VS, +3VS.

ACES_87212-1200

FIR & LED BD.

Pinout for the FIR & LED BD. connector (JP18):

Pin	Signal
1	IRRX
2	IRTXOUT
3	IRMODE
4	HDD_LED#
5	IRRX
6	IRTXOUT
7	IRMODE
8	HDD_LED#
9	IRRX
10	IRTXOUT
11	IRMODE
12	HDD_LED#
13	IRRX
14	IRTXOUT
15	IRMODE
16	HDD_LED#
17	IRRX
18	IRTXOUT
19	IRMODE
20	HDD_LED#
21	IRRX
22	IRTXOUT
23	IRMODE
24	HDD_LED#
25	IRRX
26	IRTXOUT
27	IRMODE
28	HDD_LED#
29	IRRX
30	IRTXOUT
31	IRMODE
32	HDD_LED#
33	IRRX
34	IRTXOUT
35	IRMODE
36	HDD_LED#
37	IRRX
38	IRTXOUT
39	IRMODE
40	HDD_LED#

Power connections: +3VS, +5VS, +3VALW, +3VAL, +5VS, +3VS, +3VL.

ACES_85203-2002

10-Pin Connector

Pinout for the 10-pin connector:

Pin	Signal
1	BT_LED
2	WL_LED
3	STB_LED#
4	PANEL_FLIP#
5	GREEN_BATLED#
6	
7	
8	
9	
10	

Power connections: +5VS, +3VL, +3VS.

ACES_85203-2002

The schematic diagram illustrates the MDC Conn. circuit. It features a JP25 connector, an ACES_88018-3010 chip, and various power and signal connections. The chip is connected to a +3VALW supply and a +3VS supply. The chip's pins are connected to various components, including capacitors (C12, C13, C7, C5, C10, C22), resistors (R402), and other chips (AC97_SYNC, AC97_RST#, AC97_BITCLK, AC97_SDIN1, AC97_BITCLK). The chip is also connected to a +3VALW supply and a +3VS supply. The chip's pins are connected to various components, including capacitors (C12, C13, C7, C5, C10, C22), resistors (R402), and other chips (AC97_SYNC, AC97_RST#, AC97_BITCLK, AC97_SDIN1, AC97_BITCLK). The chip is also connected to a +3VALW supply and a +3VS supply.

Power button

The diagram shows a power button circuit. It starts with a 3V_L supply connected to a 100K_0402_5% resistor (R22). The other end of R22 is connected to a 1U_0603_10V4Z capacitor (C23) and the input of a 5V SN74LVC14APWLE_TSSOP14 inverter (U5F). The output of U5F is connected to a 100K_0402_5% resistor (R26) and the gate of a 2N7002_SOT23 MOSFET (Q70). The source of Q70 is connected to ground, and the drain is connected to a 100K_0402_5% resistor (R536) and the input of a 100K_0402_5% resistor (R8). The other end of R8 is connected to a 3V_ALW supply. The output of the circuit is ON/OFFBTN#.

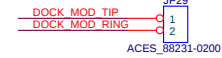
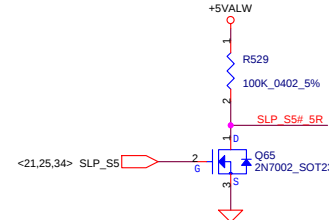
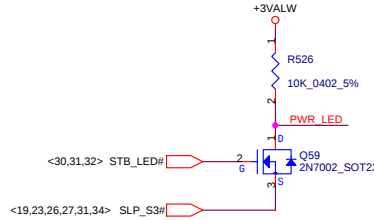
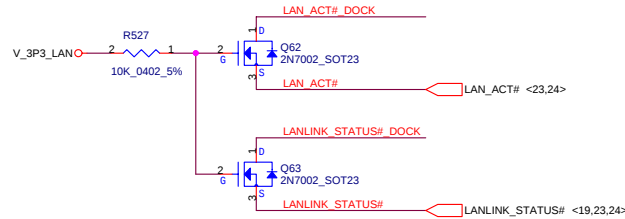
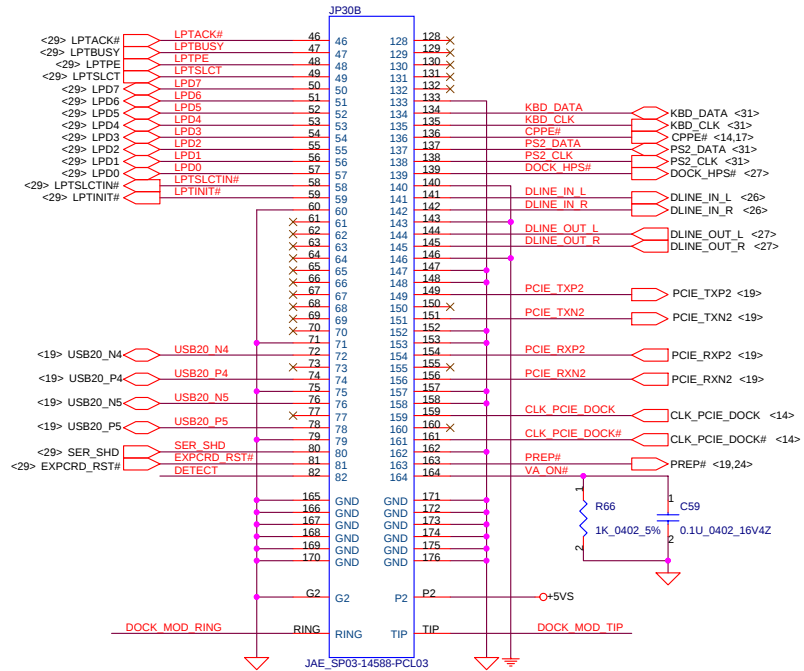
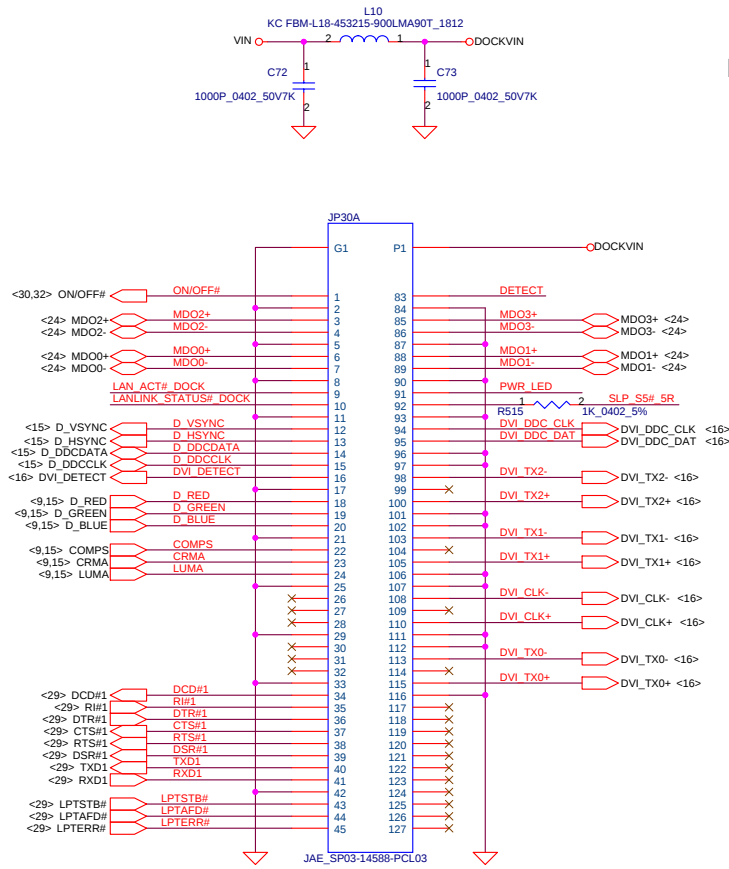
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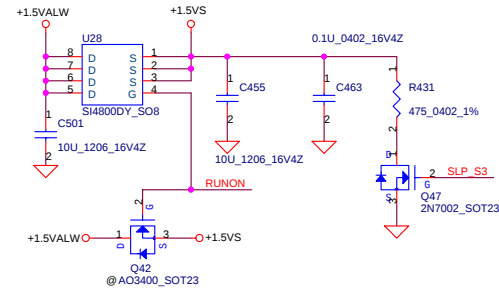
TP BD.

Compal Electronics MDC/KBD/ON C	
Title	SECURITY DOCUMENT NUMBER
DATE	DATE
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DATE	DATE
Thursday, September 09, 2004	Sheet

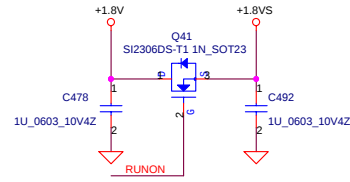
DOCK CONN. 184PIN



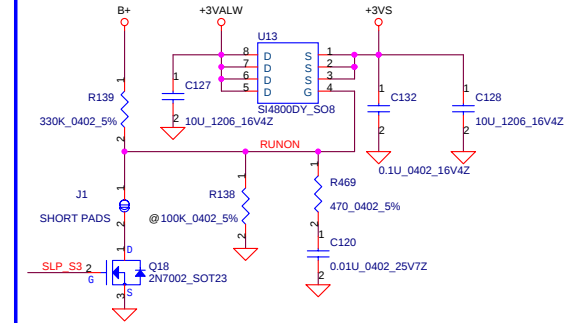
+1.5VALW to +1.5VS Transfer



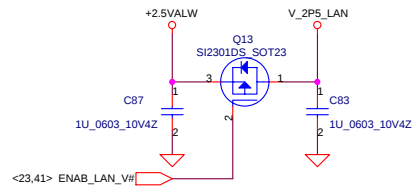
+1.8V to +1.8VS Transfer



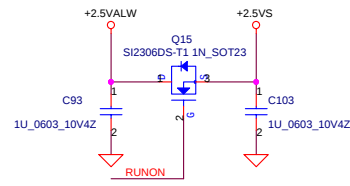
+3VALW to +3VS Transfer



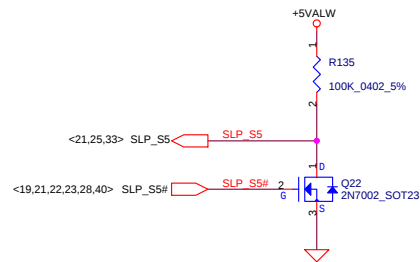
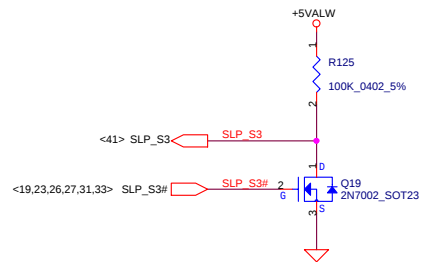
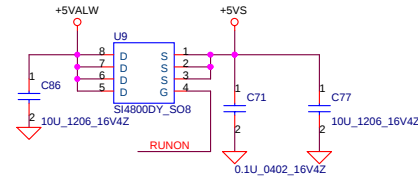
+2.5VALW to V_2P5_LAN Transfer



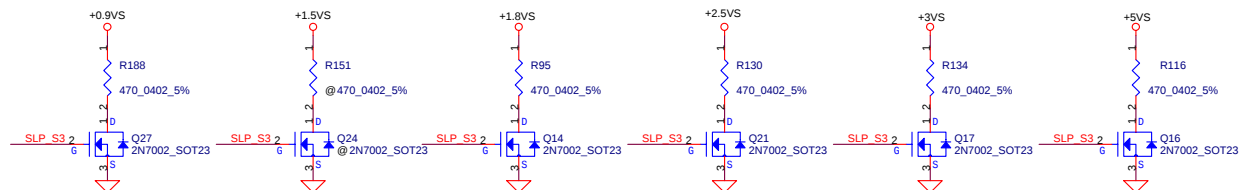
+2.5VALW to +2.5VS Transfer



+5VALW to +5VS Transfer



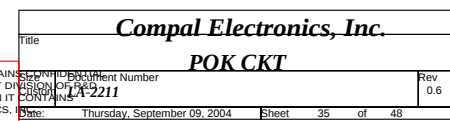
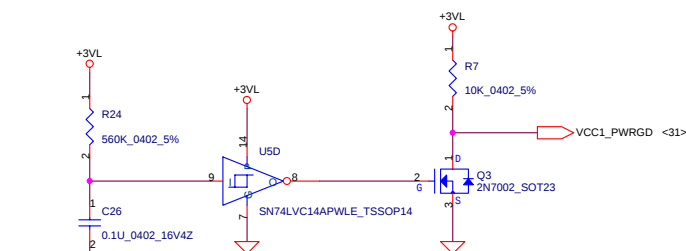
Discharge circuit



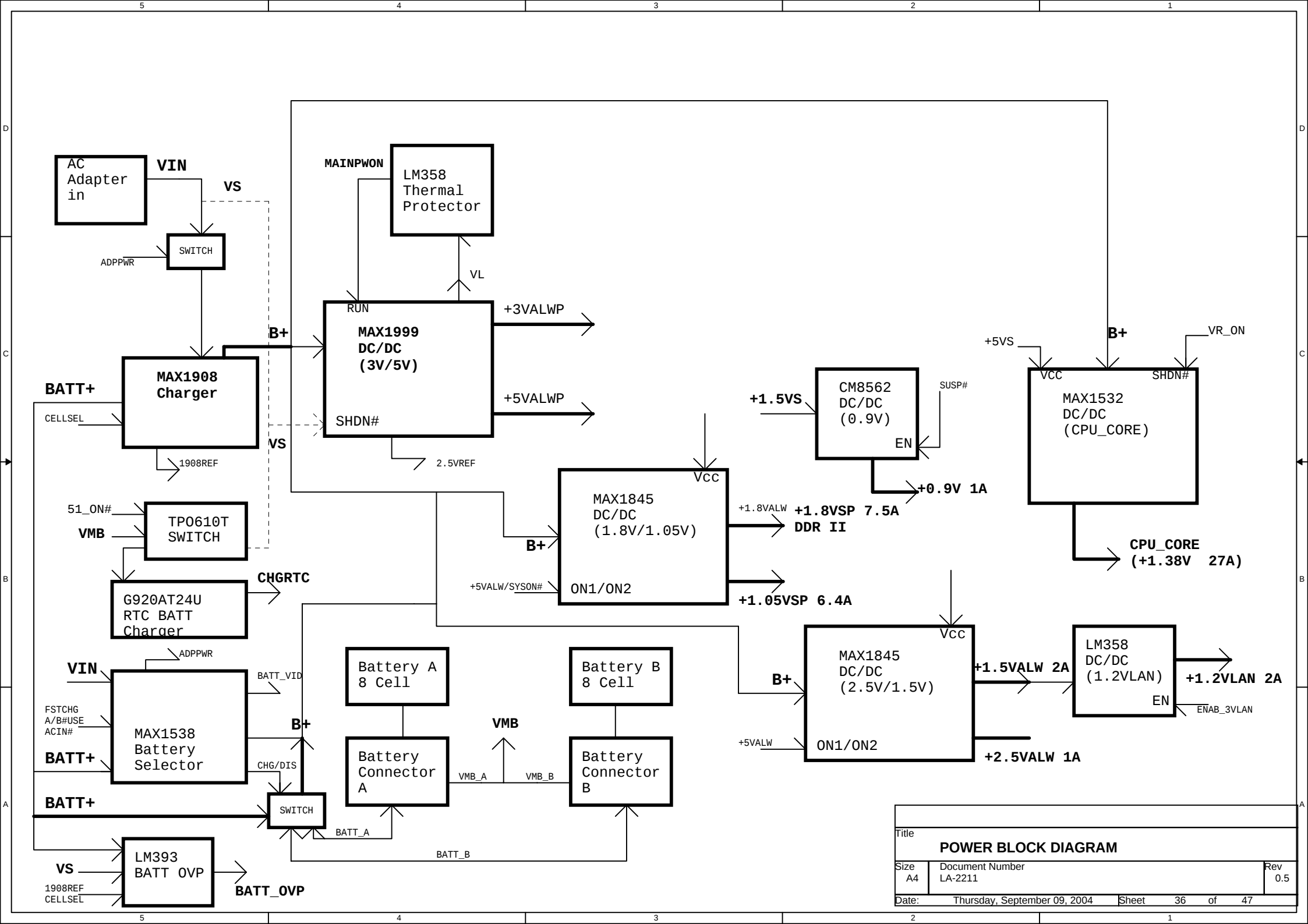
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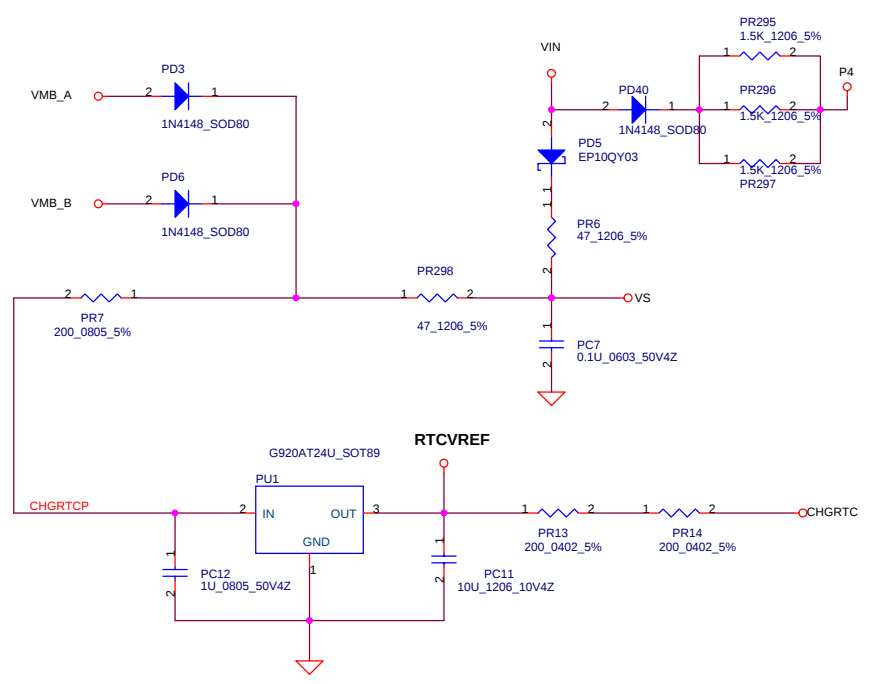
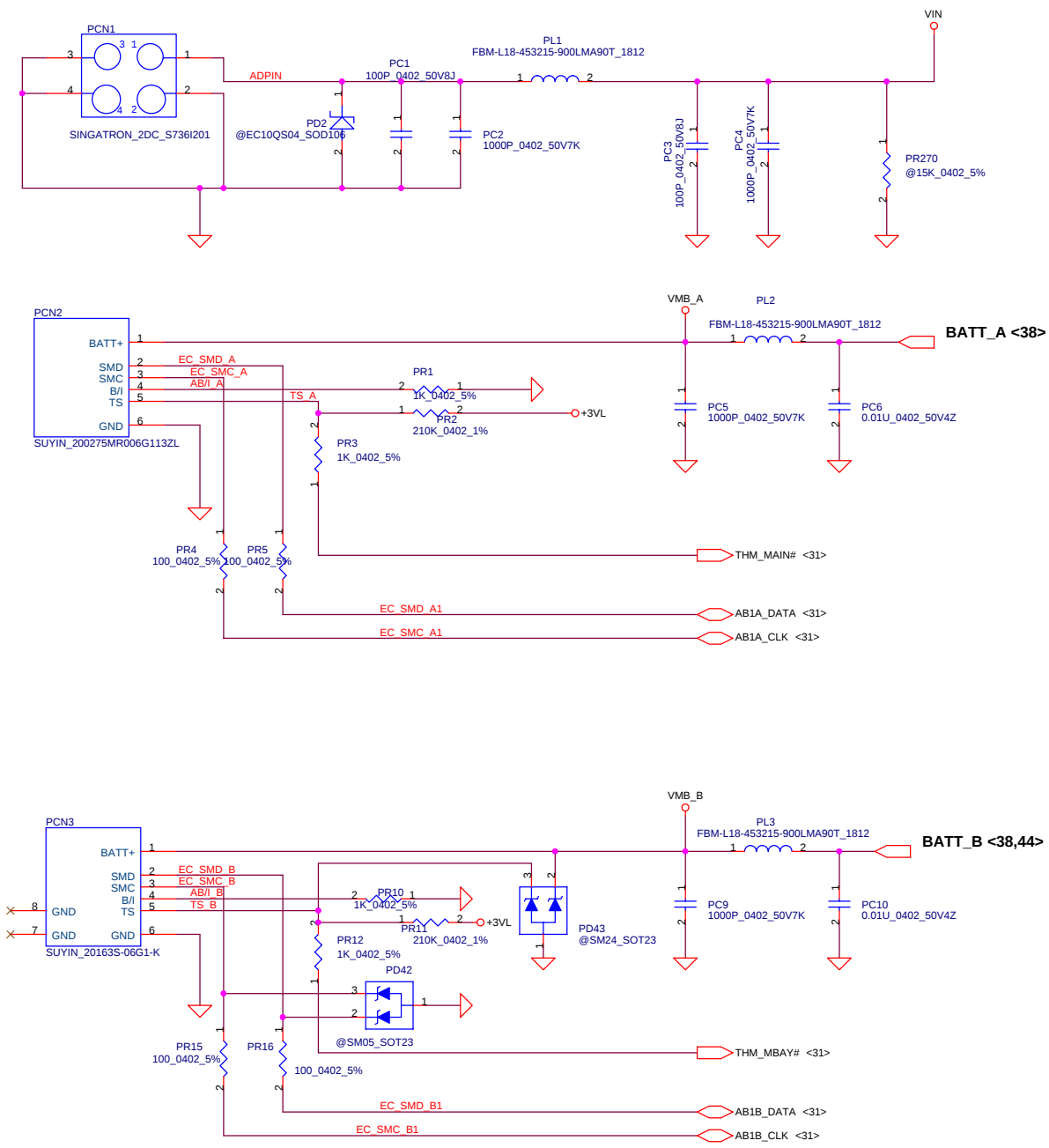
Title	DC/DC Circuits	Rev	0.6
Document Number	LA-2211	Sheet	34 of 48
Date	Thursday, September 09, 2004		

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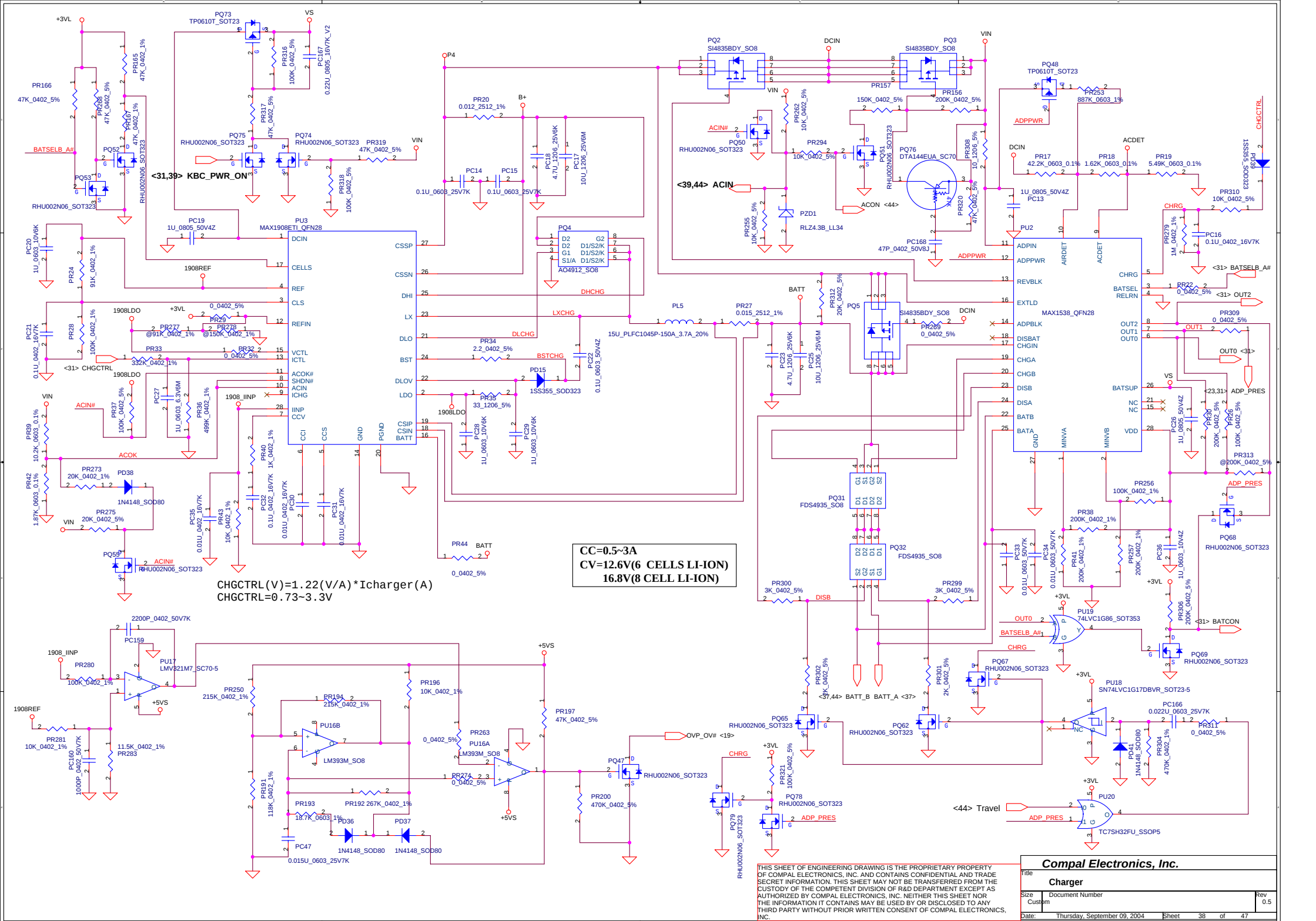
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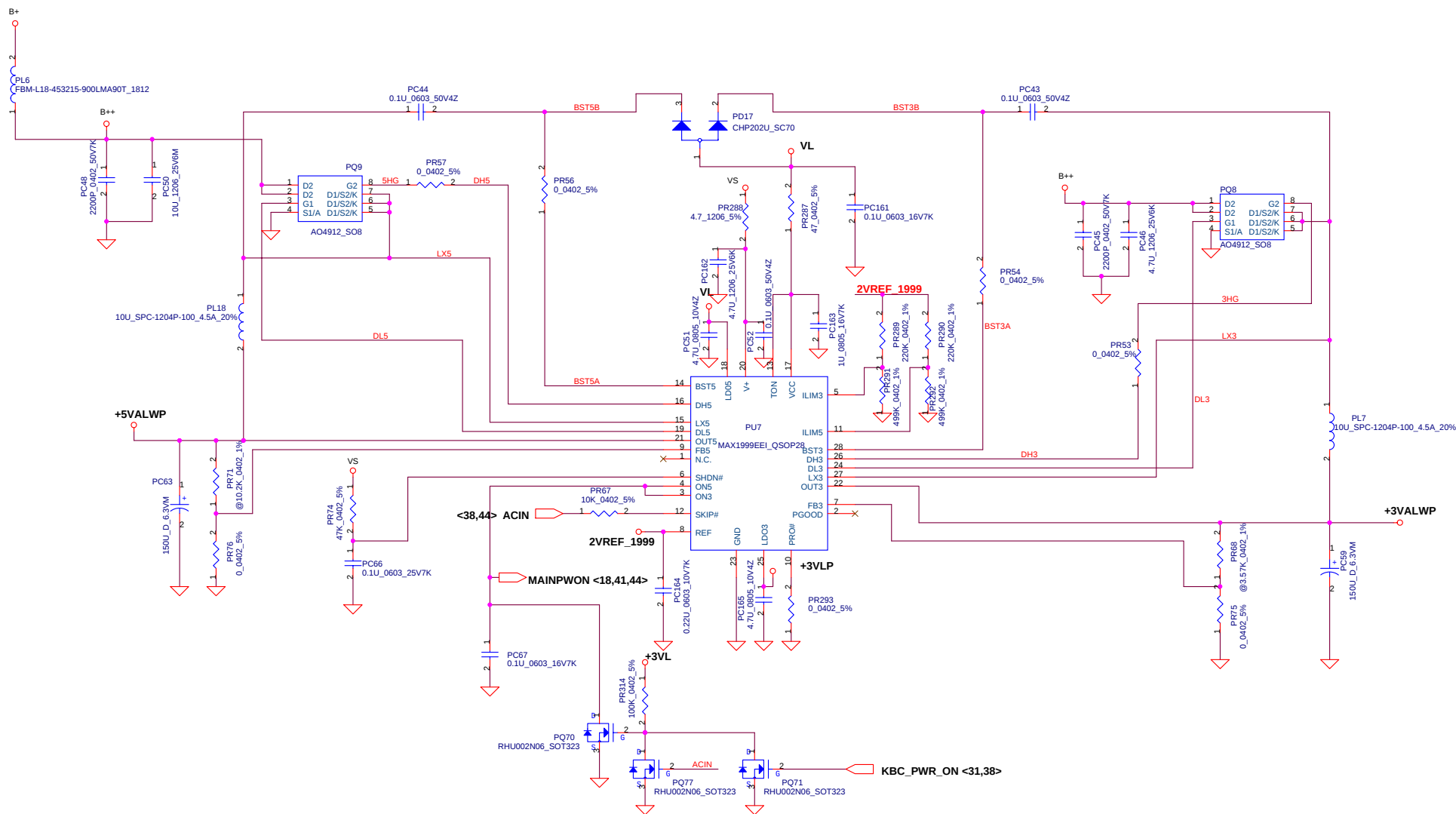


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Title	BATTERY CONN		
Document Number	37 of 47		
Date	Thursday, September 09, 2004	Sheet	37 of 47

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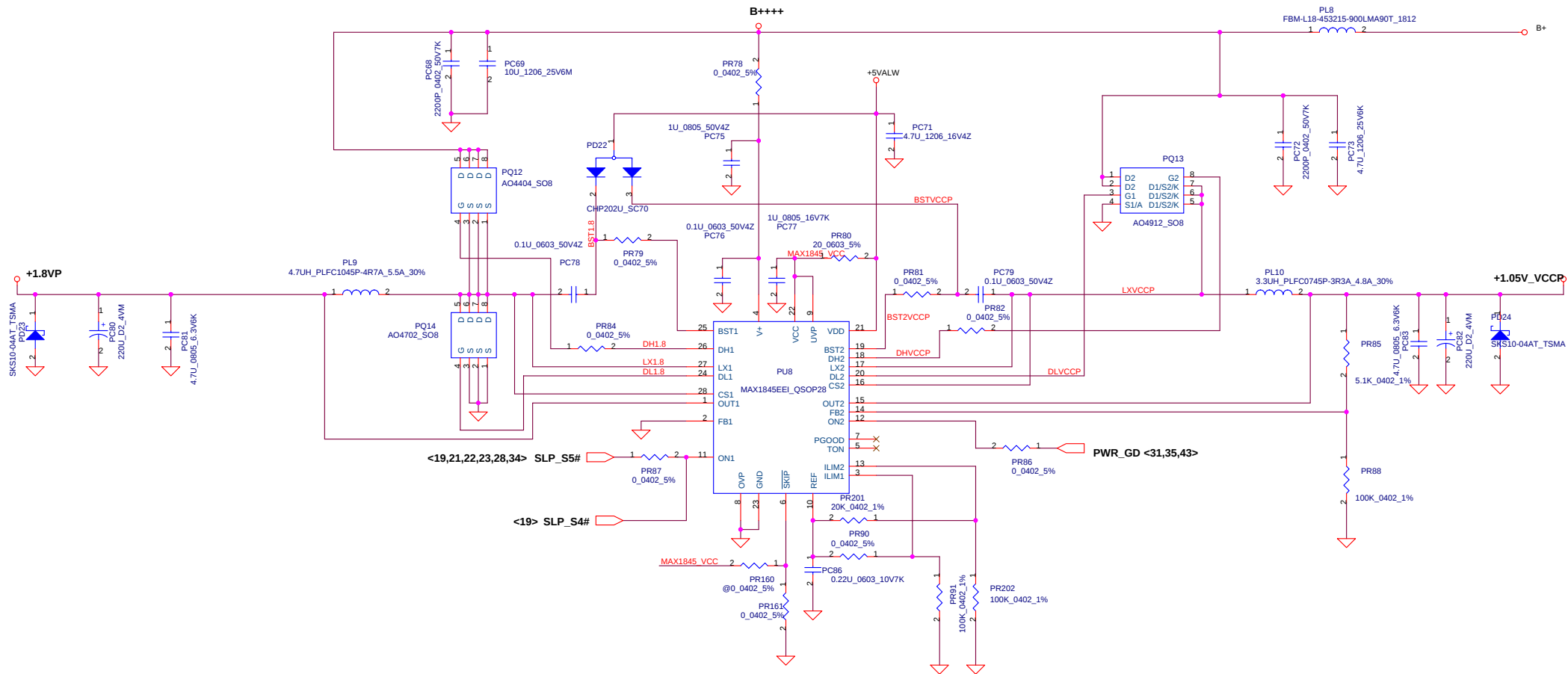


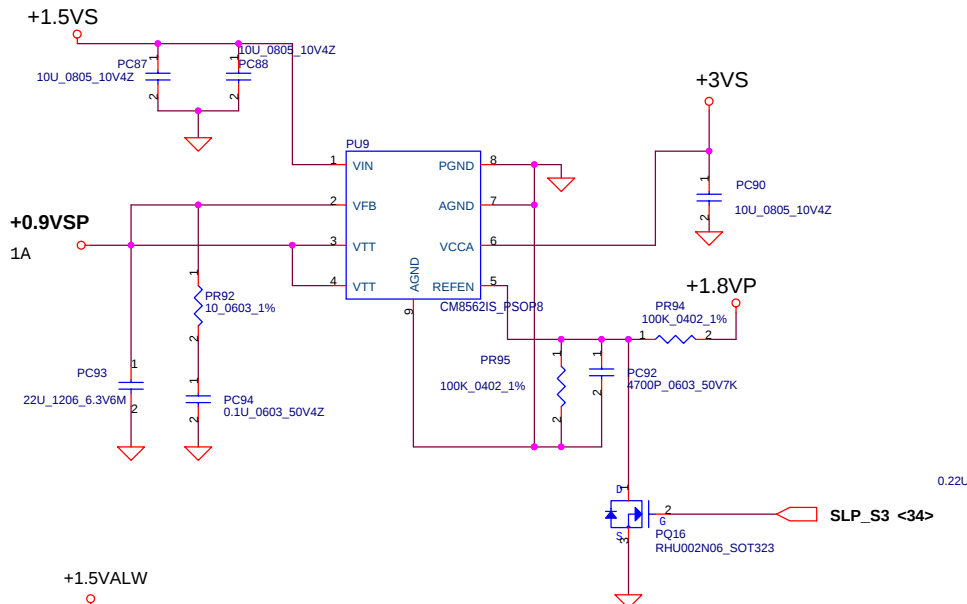
+3.3V/+5V



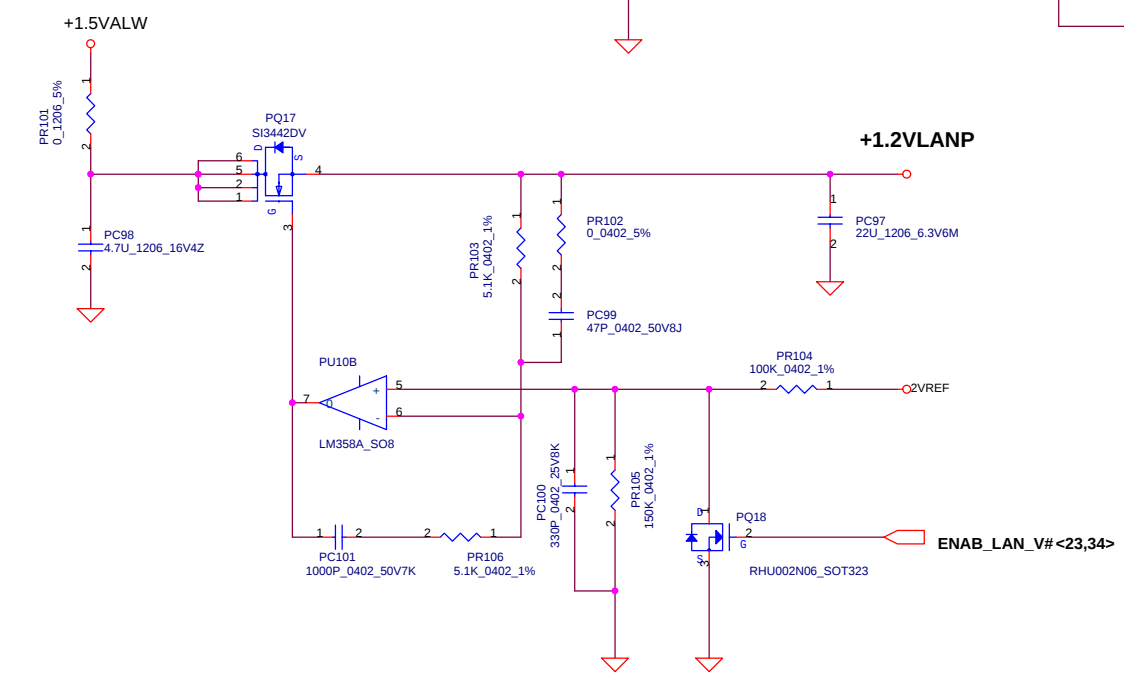
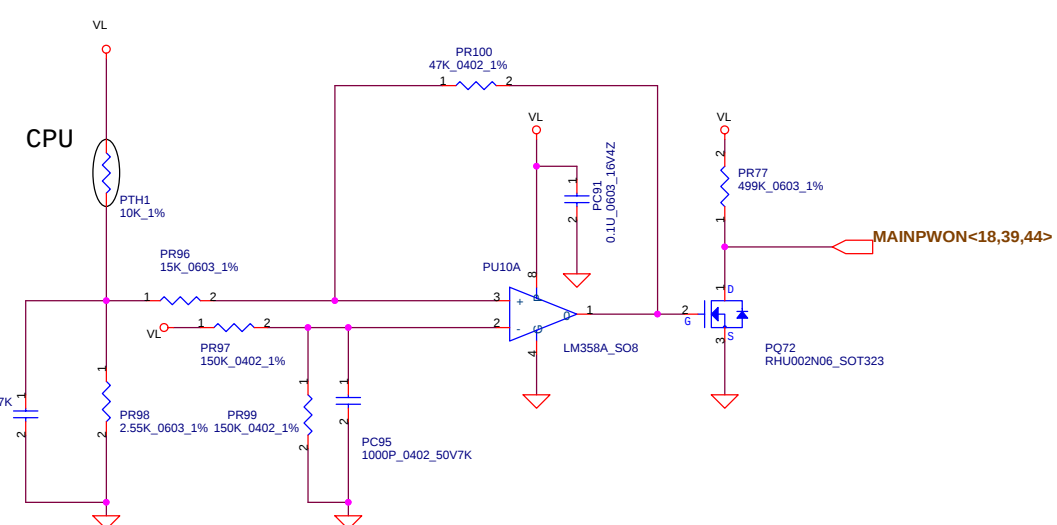
Compal Electronics, Inc.		
Title	3.3V / 5V	Rev
Document Number	3.3V / 5V	0.1
Date	Thursday, September 09, 2004	Sheet 39 of 47

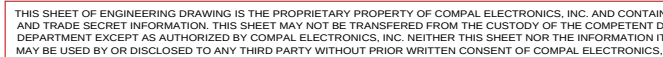
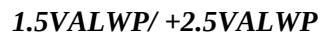
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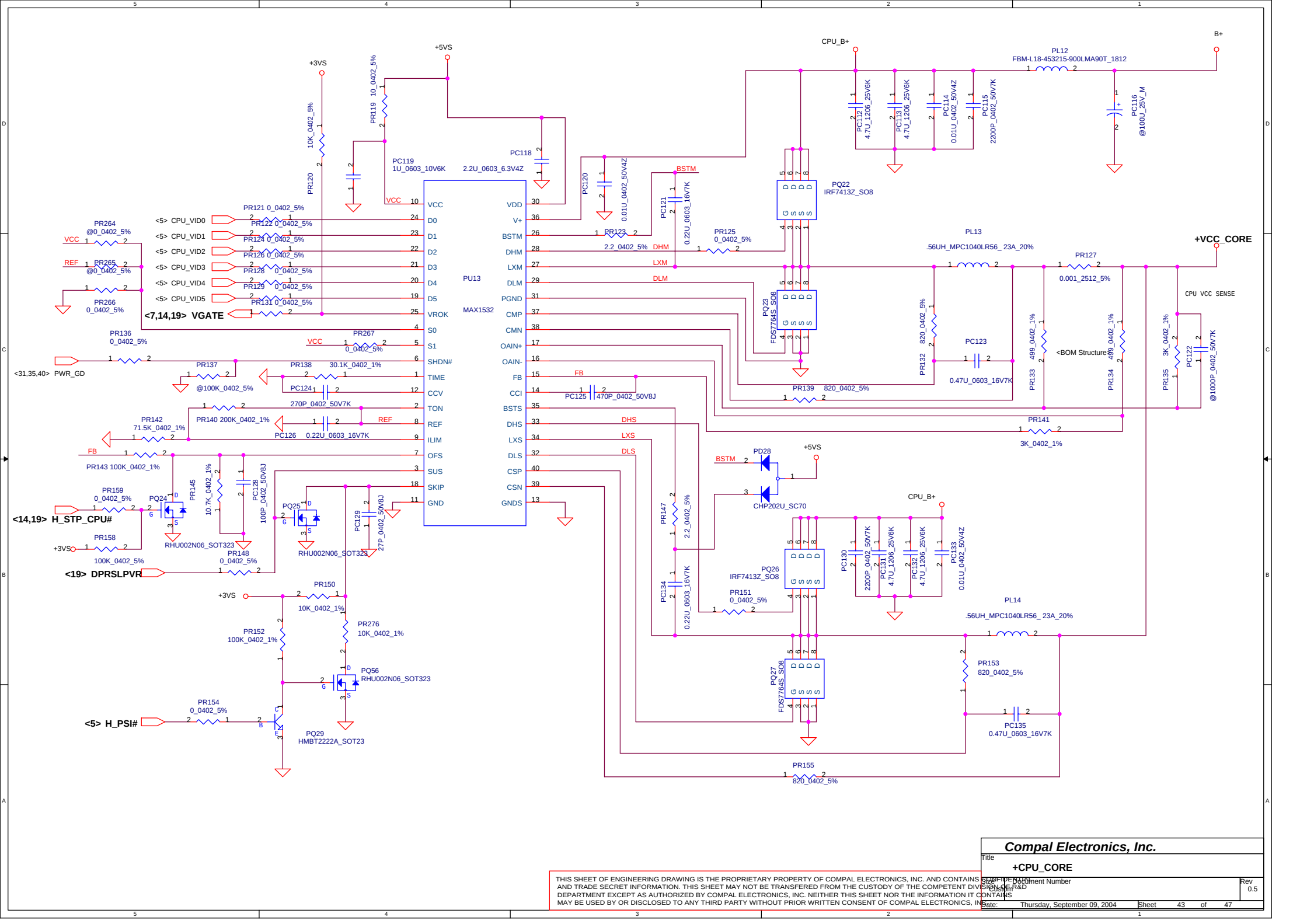




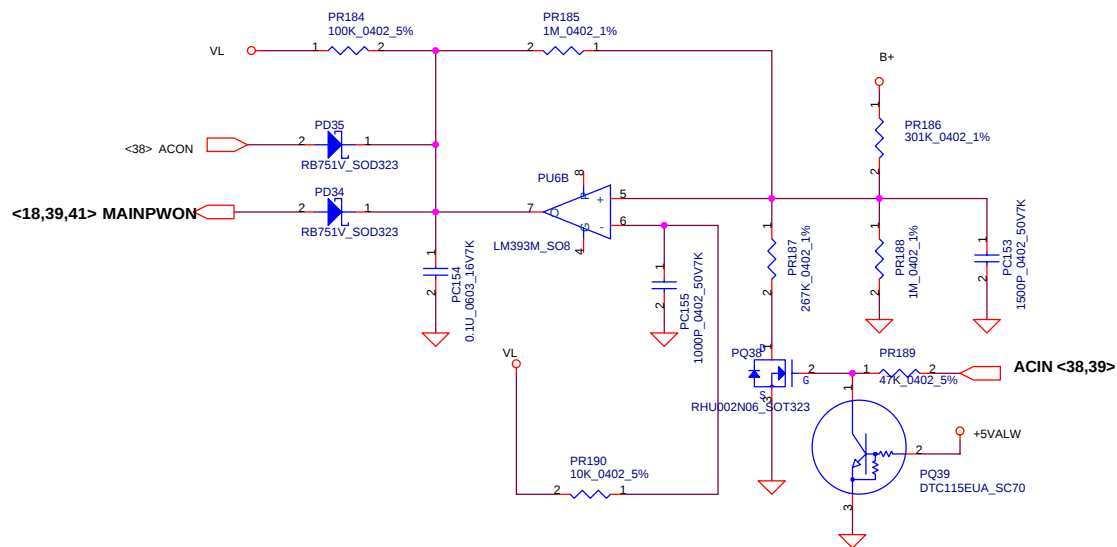
PH1 under BATT botten side :
 CPU thermal protection at 90 $\pm$ 3 degree C
 Recovery at 43 $\pm$ 3 degree C







Compal Electronics, Inc.			
Title			
+CPU_CORE			
Sheet			
Revision			
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0.5			



Title		Rev	
BATT OVP		0.5	
DIVISION OF REGIMENT NUMBER			
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Version Change List (P. I. R. List) for Power Circuit

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Title			
Changed-List History-1			
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	LA-2211		0.5
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Version Change List (P. I. R. List) for EE Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut-In Date
1	26	AGND	03/22/2004 (DB2)	HP	Link AGND and GND with capacitor	changeR460,R461,R462,R463 from 0_0402_5% to C563,C564,C565,C566 0.1U_0402_16V4Z	DB2(0.3)
2	16	SiI1362	03/22/2004 (DB2)	HP	Follow SiI1362 demo circuit	changeR117 from 100_0402_5% to 1k_0402_5% changeR105 from 300_0402_5% to 1k_0402_5%	DB2(0.3)
3	16	SiI1362	03/23/2004 (DB2)	HP	Follow SiI1362 data sheet recommend	Add R493,R494,R495,R496 300_0402_1% Add C567,C568,C569,C570 0.1U_0402_16V4Z	DB2(0.3)
4	27	Microphone circuit	03/23/2004 (DB2)	HP	To improve frequency response	Add L57,L58,L59,L60,L61 HLC0603CSCCR10JT_0603 Add C571,C572,C573,C574,C575 68P_0402_50V8J	DB2(0.3)
5	32	Trackpoint CONN	03/23/2004 (DB2)	Compal	Change trackpoint connector from pitch1.0mm to 0.5mm	change JP14 from ACES_85203-0802 to ACES_87153-0801L	DB2(0.3)
6	23	V_1P2_LAN	04/01/2004 (DB2)	Compal	V_1P2_LAN ripple over spec	change L8,L29,L30,L32,L33 from 0_0603_5% to BLM11A601S_0603	DB2(0.3)
7	4	ADM1031	04/02/2004 (DB2)	Compal	Can't read DDRII temprature	link Q43 pin1 from GND to Q43 pin2	SI1(0.4)
8	23	ATTN_BTTN#	04/08/2004 (DB2)	HP	Per Broadcom, this signal should be pulled up to +3VS.	Delete R72 layout pad and change R73.1 from GND to +3VS.	SI1(0.4)
9	16	CH7307	04/08/2004 (DB2)	CHrontle	Recommendation from Chrontle.	1. Pin25 VSWING for CH7307 should be added 1.2K ohm to GND. 2. Pin 26, 27 should be GND as 10K ohm. 3. Pin3 AS should be pull up as 1K ohm.	SI1(0.4)
10	29, 33	SER_SHD	04/08/2004 (DB2)	HP	Add active high signal SER_SHD to GPIO47 on U8 pin 31 that connects to pin 80 on docking connector JP30B. Add Pull down to this signal. This is used to control serial port transceiver in dock.		SI1(0.4)
11	34	PWR on fail	04/19/2004 (DB2)	Compal	System can't boot reliably.	1. Change Q15 from SI2301 to SI2306. 2. Change Q15.2 control signal from SLP_S3 to RUNON. 3. Change R139 from 100K_0402_5% to 330K_0402_5%.	SI1(0.4)
12	29	MAX3243	04/28/2004 (DB2)	Compal	Delete COM port components.	Delete U33,C558,C559,C561,C560,C562,R468,RP50.	SI1(0.4)
13	9	White screen	04/28/2004 (DB2)	Compal	LCD has white screen when system power on or resume from S3/S4.	1. Exchange U35.3 and U35.5 2. Add a 2.2K_0402_5% pull down resistor on U35.2	SI1(0.4)
14	14, 19 23, 24	LAN PWR down	04/29/2004 (DB2)	HP	Support LAN controller power down feature when LAN cable do not installed.	1. Delete R499 10K_0402_5%. 2. Add R502,R505,R507 0_0402_5%. 3. Delete R15 4.7K_0402_5%. 4. Add U36,U37 SN74LVC1G17DBVR. 5. Add Q54 2N7002. 6. Add C576,C577 0.1U_0402_16V4Z. 7. Add D32 RB751V. 8. Add R503 100K_0402_5%. 9. Add R504 120K_0402_5%. 10. Add R506 10K_0402_5%.	SI1(0.4)

Version Change List (P. I. R. List) for EE Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut-In Date
15	21	TI Flash media IO	04/30/2004 (DB2)	HP	Solve TI Flash media IO work around circuit.	Add D33,D34 RB751V.	SI1(0.4)
16	19	LANLINK_STATUS#	04/30/2004 (DB2)	HP	Change this signal from pin M3 of U26B to pin C25 of U26C.	1. Add R508 10K 0402_5%. 2. Add Q55 2N7002.	SI1(0.4)
17	21,22	Change power rail	05/12/2004 (DB2)	HP	PCMCIA interface don't support S3 or S5 wake up feature.	Change all of components power rail to main power plane.	SI1(0.4)
18	28	USB+PWR switcher	05/21/2004 (DB2)	Compal	Change USB power switcher from MIC2044 to TPS2330.		SI1(0.4)
19	27	Microphone pre-amp	05/26/2004 (DB2)	HP	Per HP's requirement change microphone pre-amp from MAX4492 to TLV2464A.		SI1(0.4)
20	21,22	Change power rail	05/27/2004 (DB2)	HP	Going back and forth for waking up support for PCMCIA interface.	Change all of components power rail to resume power plane.	SI1(0.4)
21	21,22	Change power rail	07/05/2004 (SI1)	HP	PCMCIA interface don't support S3 or S5 wake up feature.	1. Reserved some component layout pads for +3V/+5V. 2. Add R530 and R537 for supporting PCMCIA power rail with main power rail.	SI1-B(0.5)
22	19,31 32,35	S5 power consumption	07/05/2004 (SI1)	HP	To reduce power consumption on S5. The specification is under 50 mW.	1. Add isolation circuit. (R532,R533,D37,D38) 2. Change some component's power rail from +3VALW to +3VL (R223,R218[V_3P3_LAN],U7,RP44,RP43,R65,R28,R27,JP31 RP1,R32,R31,R30,U5,R22,R24,R7)	SI1-B(0.5)
23	28	USB+PWR switcher	07/20/2004 (SI1)	Compal	To solve voltage droop issue when cradle plugged in USB port.	1. Change C582 from 1000pF to 0.1uF. 2. Add C581 0.1uF. 3. Change C102 to 100uF Low ESR capacitor.	SI2(0.6)
24	31	Wrong voltage level on FWP#.	07/22/2004 (SI1)	Compal	To solve wrong voltage on FWP# when system is powered off.	Delete R28.	SI2(0.6)
25	27	OTS#133751	07/22/2004 (SI1)	Compal	When mute is off, the mute button LED remains on (very dim though).	Change R430 from 100K ohm to 10K ohm.	SI2(0.6)
26	18	ICH_RTCRST# timing	08/22/2004 (SI1)	Intel	Intel changed component's value.	1. Change R230 from 180K ohm to 20K ohm. 2. Change C287 from 0.1uF to 1uF.	SI2(0.6)
27	14	R511	08/03/2004 (SI1)	Compal	For supporting CY28442 on SI2.	Delete R511.	SI2(0.6)
28	27	R429, C504	08/03/2004 (SI1)	HP	Follow Lloyd Daniel's suggestion, change R429 to 16.2K ohm and change C504 to 0.22uF.	change R429 to 16.2K ohm and change C504 to 0.22uF.	SI2(0.6)
29	30	Power LED active error.	08/03/2004 (SI1)	Compal	Swap D41.1 with D41.4 for solving LED active error on SI1-B unit.		SI2(0.6)
30	16,26 32	Modify EMI solution	08/03/2004 (SI1)	Compal		1. Add FBM-L11-201209-221LMAT on L62 and delete R466. 2. Add 0.1u (C586) / 68p (C587) capacitors at B+_LCD. 3. Add CHB2012U121 on L36. 4. Remove CP1~CP7	SI2(0.6)
31	30	Delete sleep button function	08/10/2004 (SI1)	HP	Sleep LED is no longer required.	Delete D40 & R261.	SI2(0.6)
32	30	Add additional R & LED for CAP. function	08/10/2004 (SI1)	Compal	For solving CAP LED bright issue. This requirement was coming from ME team.	1. Add R541 150 ohm. 2. Add green LED 17-21SYGC/S530-E1/TR8.	SI2(0.6)

Compal Electronics, Inc.		
Title		
Changed-List EE History-2		
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Version Change List (P. I. R. List) for EE Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut-In Date
33	30	Power Button	08/10/2004 (SI1)	Compal	Change powr button from 2-way to 1-way.	From SS056-Pt213BBT-PA2 to SS607-212N-FEEG1T.	SI2(0.6)
34	19	OTS#137561	08/19/2004 (SI1)	Compal	I found this issue was caused by ICH_PCIE_WAKE# signal generated again. Because V_3P3_LAN disappeared before +3VALW under battery mod. This is wrong.	1. Change R532 from 10K ohm to 1K ohm. 2. Delete D37. 3. Add a additional MOS Q71 (BSS138). 4. Connection Q71.2 with V_3P3_LAN. 5. Connection Q71.3 with D37.1. 6. Connection Q71.1 with D37.2.	SI2(0.6)
35	15	RGB rise/fall time.	08/23/2004 (SI1)	Compal	RGB rise/fall time out of specification issue.	Short L54,L55,L56.	SI2(0.6)
36	18	RTC Accuracy	08/27/2004 (SI1)	Compal	To improve RTC accuracy.	1. Change Y4 to 32.768 KHz +-10 ppm. 2. Change C516 and C528 to 18pF.	SI2(0.6)
37	16	DVI CKT	08/31/2004 (SI1)	HP	Remove any components that associate with Silicon Image controller for DVI.		SI2(0.6)
38	4	ADM1032	09/02/2004 (SI1)	Compal	Change thermal sensor to ADM1032 and reserve a thermal sensor CKT (MAX6646) on page 8.		SI2(0.6)