

COMPAL CONFIDENTIAL

MODEL NAME : *Biathlon (IBM 15R)*
COMPAL P/N : *HEL00*
PCB NO : *LA-3091P*
Revision : *1.0*

IBM 15R Schematics Document
uFCBGA/uFCPGA Mobile Dothan
Alviso 915+ ICH6-M
2 Channel DDR2

2005-12-20
REV : 1.0

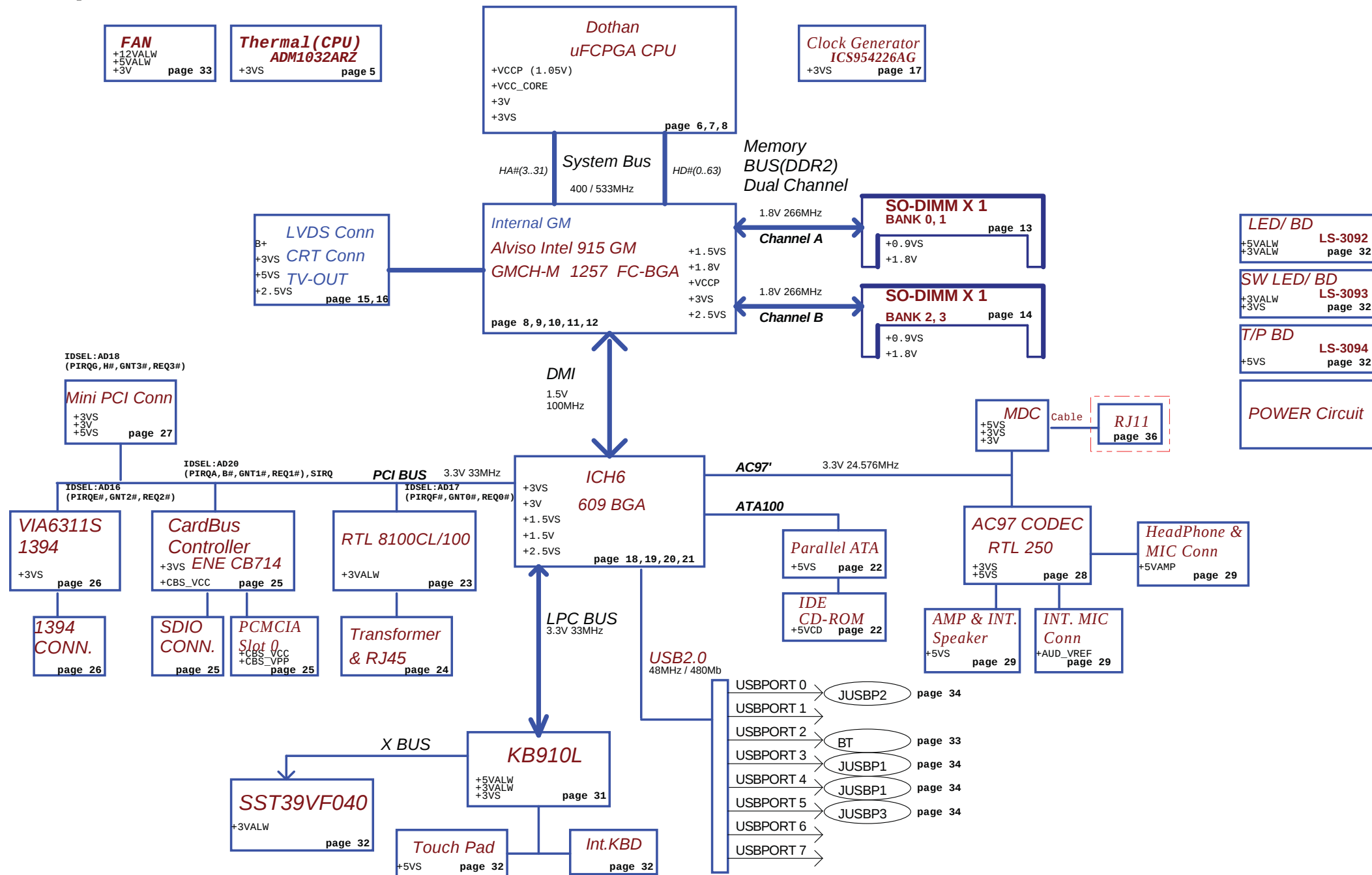
SW LED/B
LS-3093P

M/B LA-3091P

TP/B
LS-3094P

LED/B
LS-3092P

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Bithlon LA3091 Schematic	
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				Custom	LA-3091
				Date	Tuesday, January 30, 2006
				Sheet	1 of 44
				Rev	1.0



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						LA-3091		1.0	
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I2C / SMBUS ADDRESSING

External PCI Devices

DEVICE	IDSEL #	REQ / GNT #	PIRQ
LAN	AD17	0	F
CARD BUS	AD20	1	A
Cardreader			B
1394	AD16	2	E
Wireless LAN(MINI PCI)	AD18	3	G,H

@ Depop
1@ IBM 15R (UMA)
2@ (Discrete)

Power Managment table

Signal State	+12VALW +5VALW +3VALW	+12V +5V +3V +1.8V	+CPU_CORE +VCCP +5VS +3VS +2.5VS +1.8VS +1.25VS +1.5VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Ceramic Capacitor Spec
Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NP0	C0G		BJ	CH	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+ -0.05PF	+ -0.1PF	+ -0.25PF	+ -0.5PF	+ -1PF	+ -2%	+ -3%	+ -5%

K	M	N	P	Q	V	X	Z	
+ -10%	+ -20%	+ -30%	+100, -0%	+30, -10%	+20, -10%	+40, -20%	+80, -20%	

SMBUS Control Table

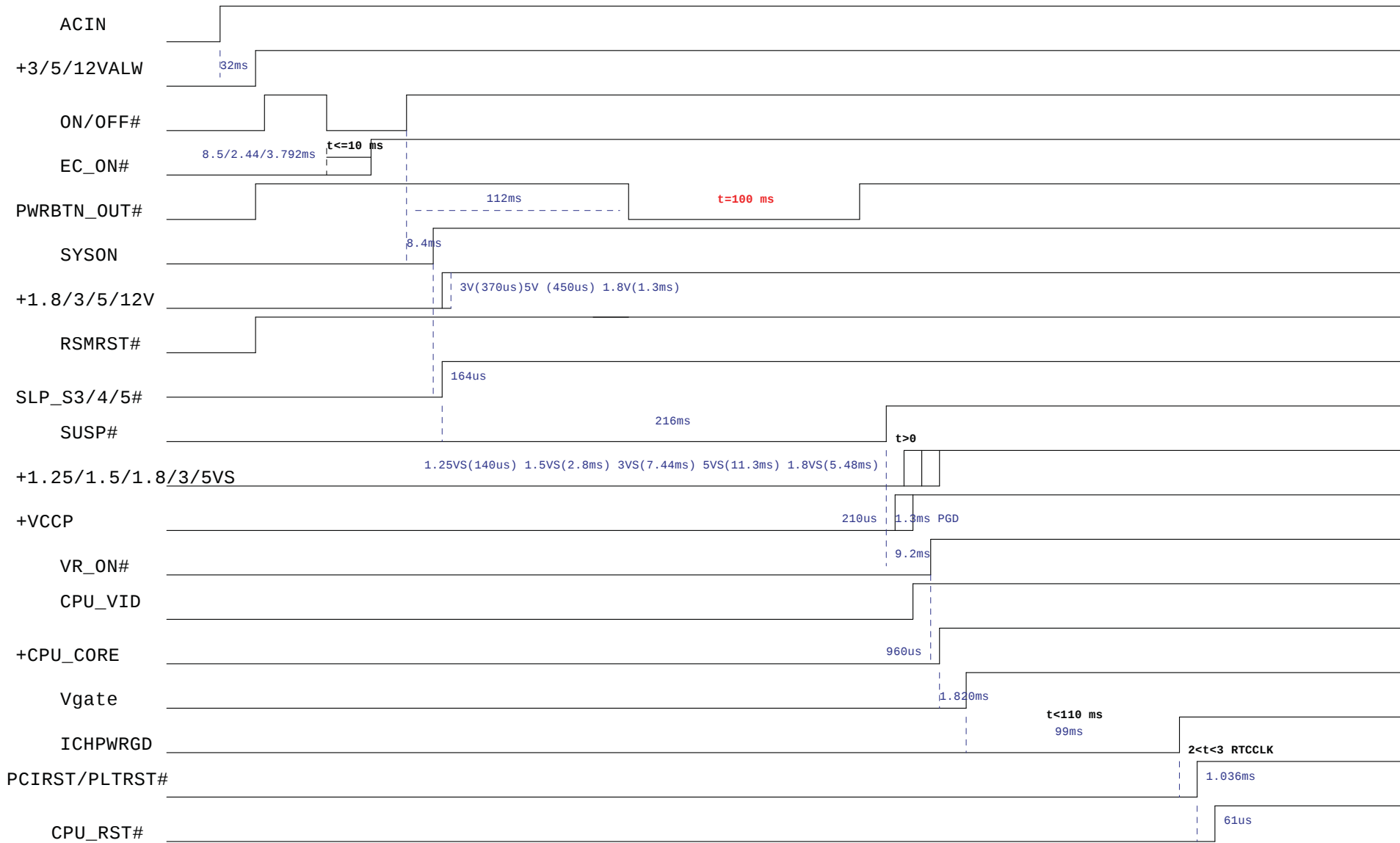
	SOURCE	BATT	SERIAL EEPROM	THERMAL SENSOR CPU (ADM1032)	Intel PCI WLAN	SO-DIMM1 SO-DIMM2	CLK CHIP	LCD
SMB_EC_CK1 SMB_EC_DA1	KB910L PU +5VALW	✓	✓					
SMB_EC_CK2 SMB_EC_DA2	KB910L PU +5VALW			✓	✓			
ICH_SMBCLK ICH_SMBDATA	ICH6-M PU +3VALW					✓	✓ PU +3VS	
LCD_CLK LCD_DAT	Alviso GM-GP PU +2.5VS							✓ PU +3VS

	PCB Rev	Data
EVT-Build	0.1	
DVT-Build	0.2	
PVT-Build		
MP-Build		

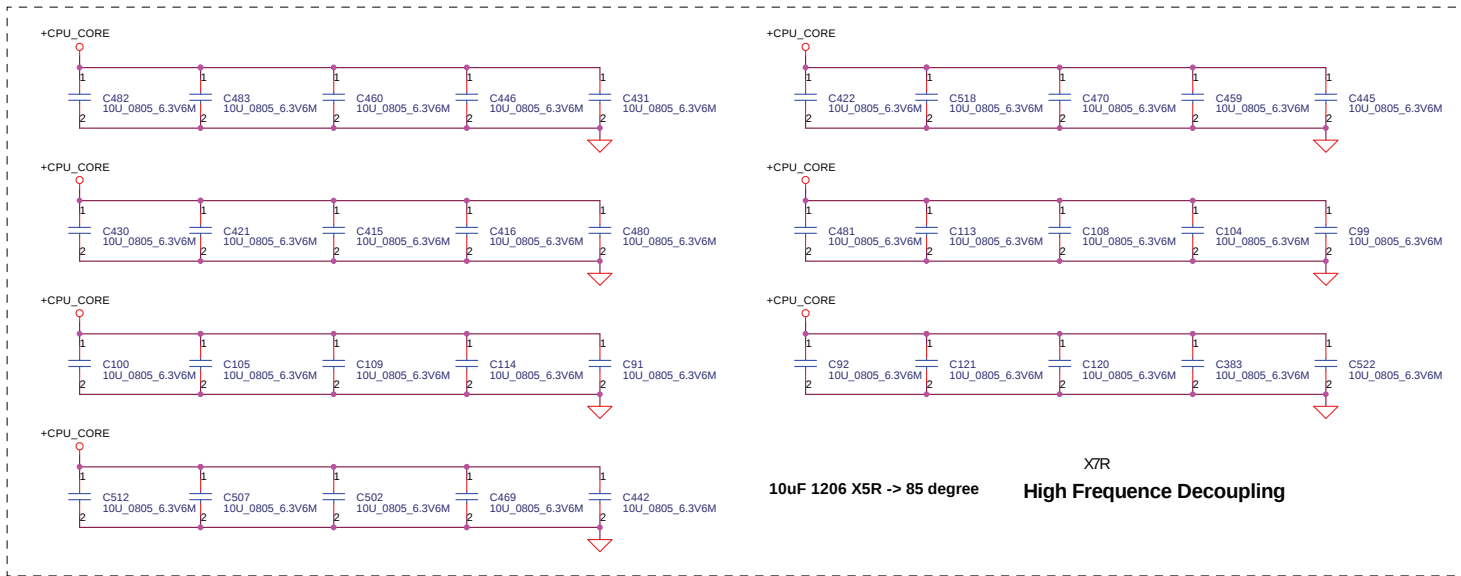
SCHEMATICS VERSION LIST

VERSION	ISSUE DATE	REMARK
0.1		EVT-Build
0.2		DVT-Build
		PVT-Build
		MP-Build

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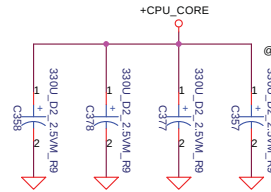


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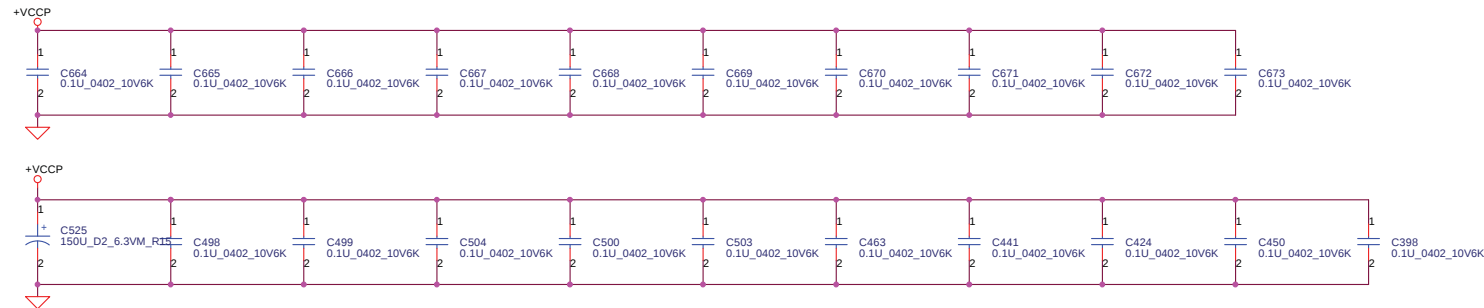
10uF 1206 X5R -> 85 degree
X7R
High Frequency Decoupling

Near VCORE regulator.



ESR <= 3m ohm
Capacitor > 880 uF

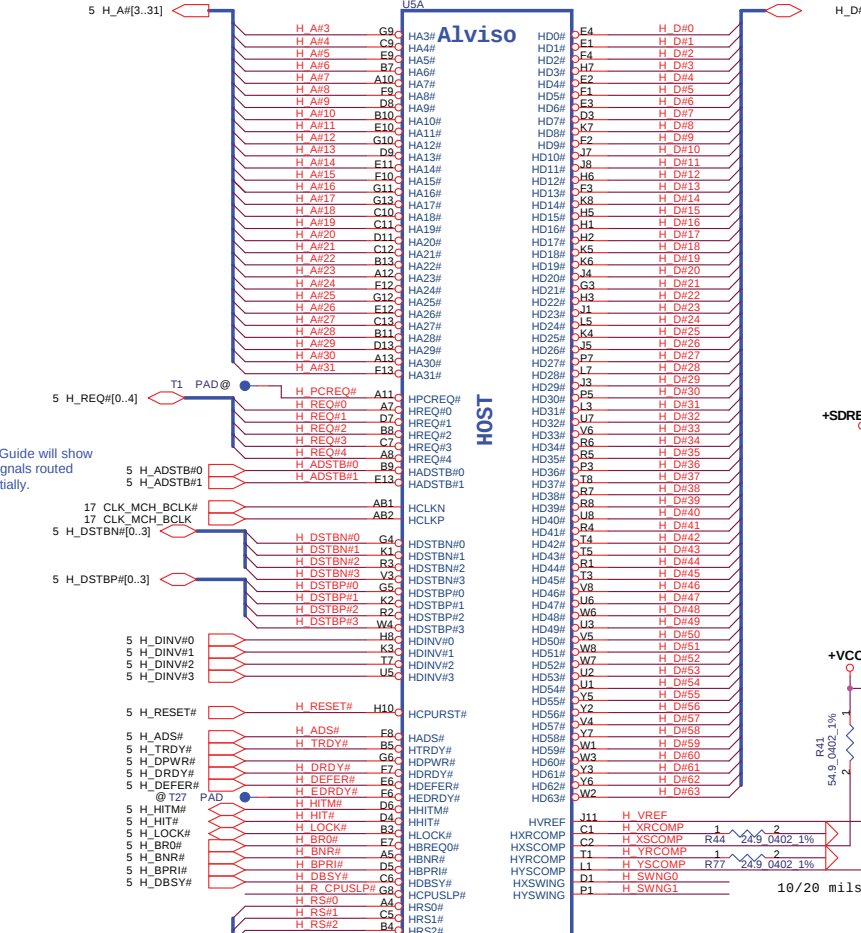
Vcc-core Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	3X330uF	9m ohm/3	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



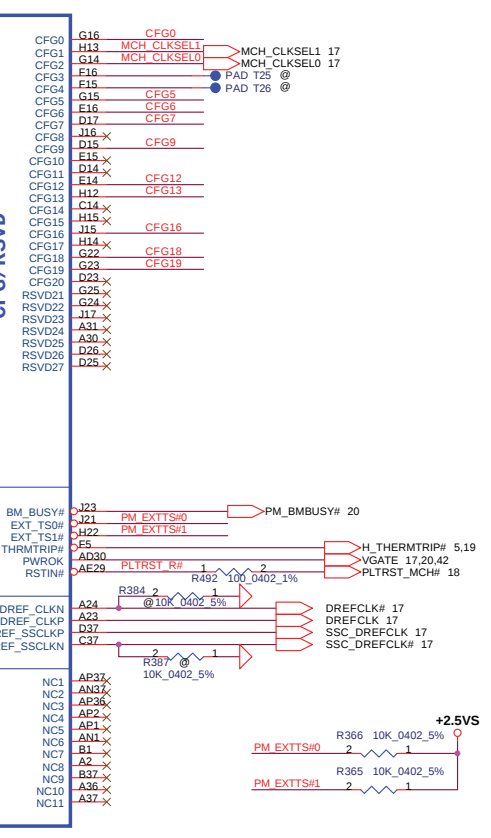
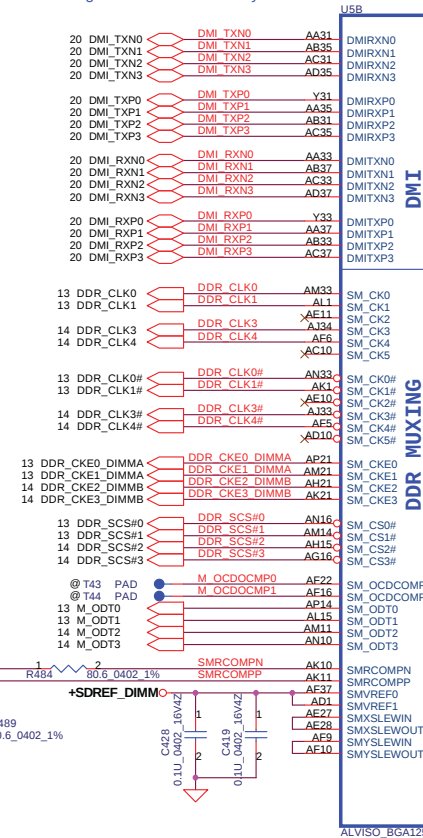
Layout Guide will show these signals routed differentially.

Layout Guide will show these signals routed differentially.

Alviso CFG[17:3] has internal pull-up

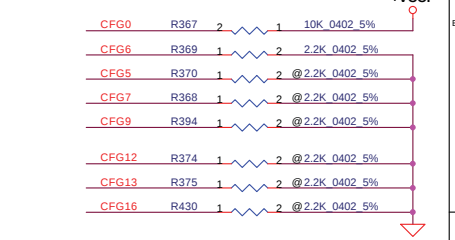


Layout Note:
H_XRCOMP & H_YRCOMP trace width and spacing is 10/20

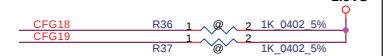


CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V

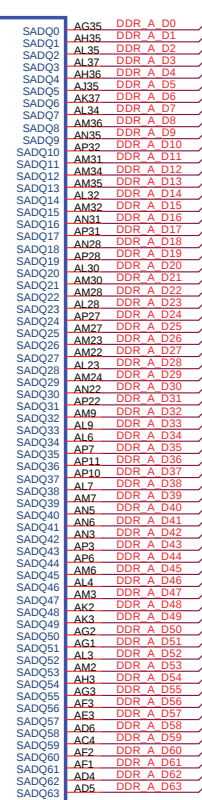
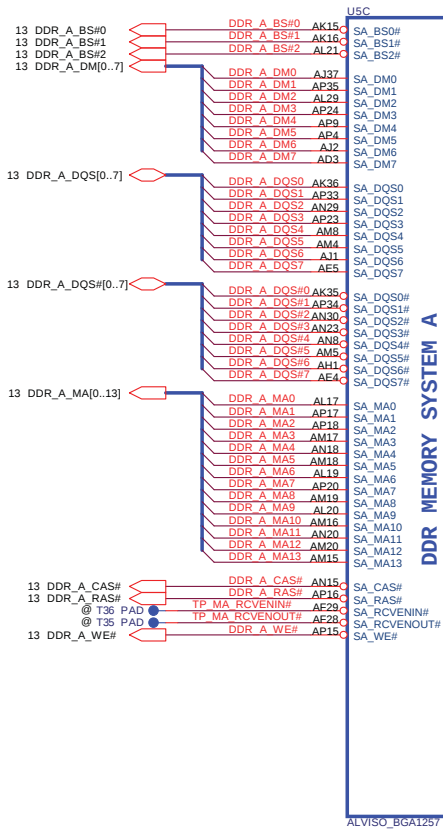
CFG[17:3] have internal pull-up



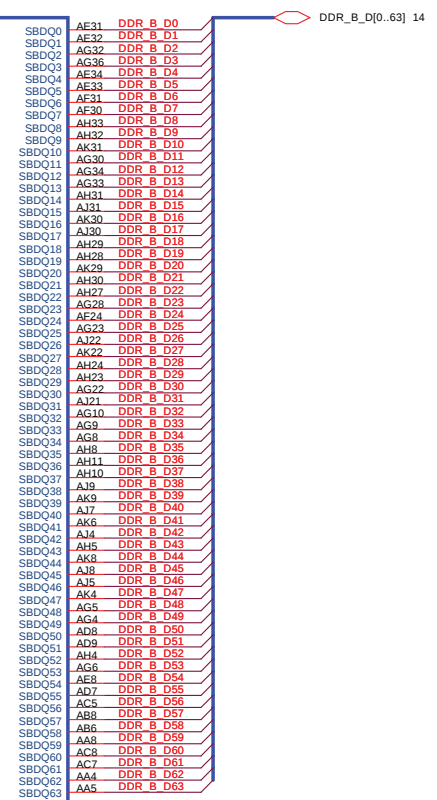
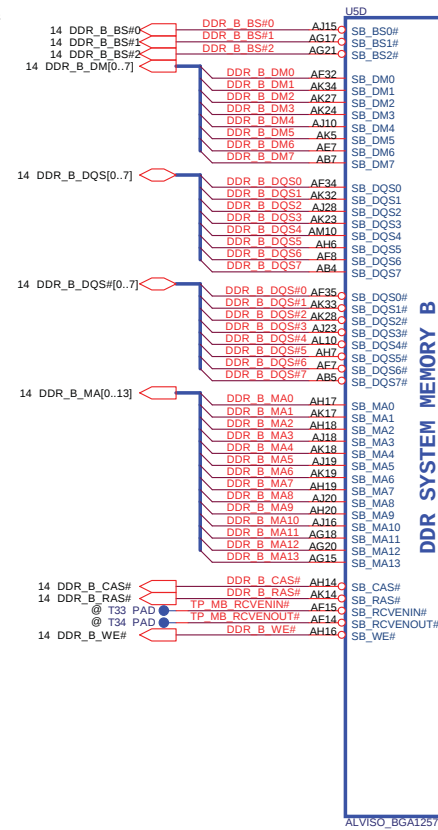
CFG[19:18] have internal pull-down
3.5 k reserve for choose



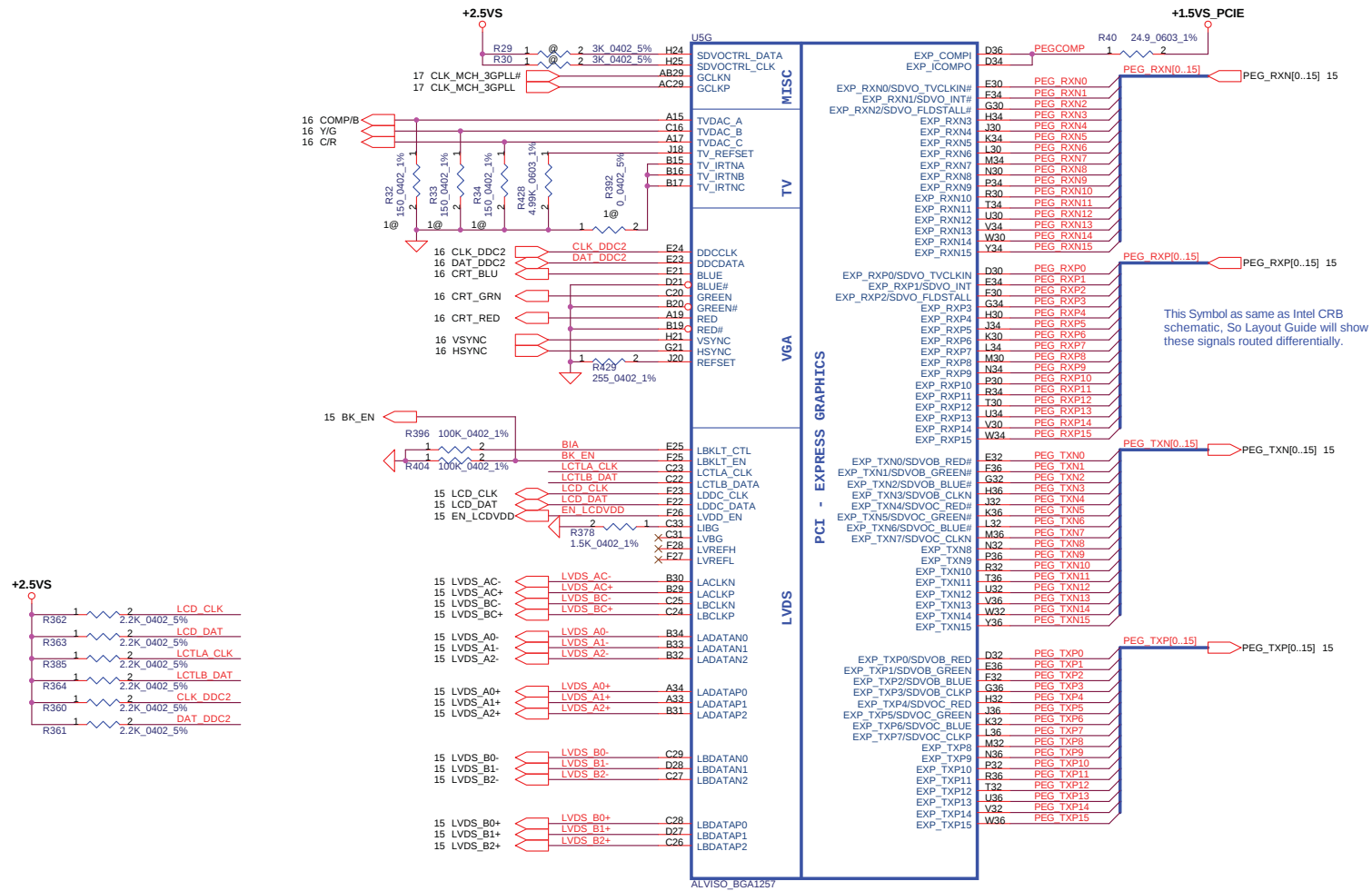
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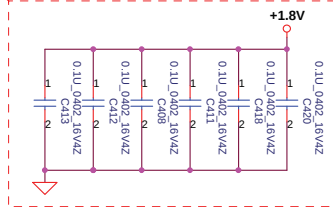
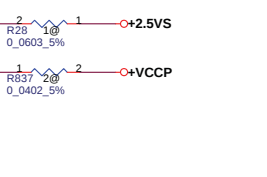
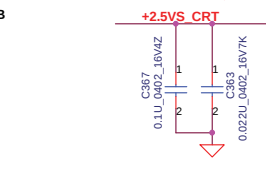
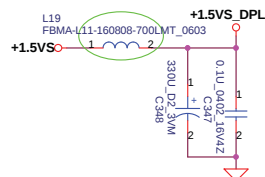
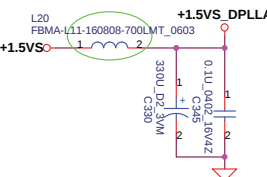
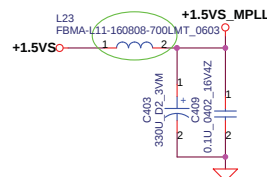
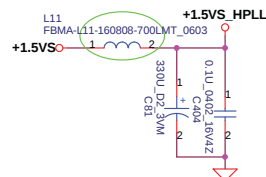
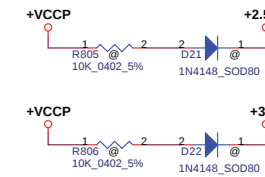
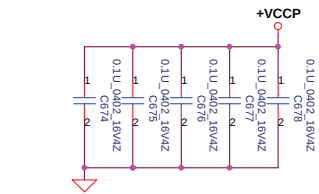
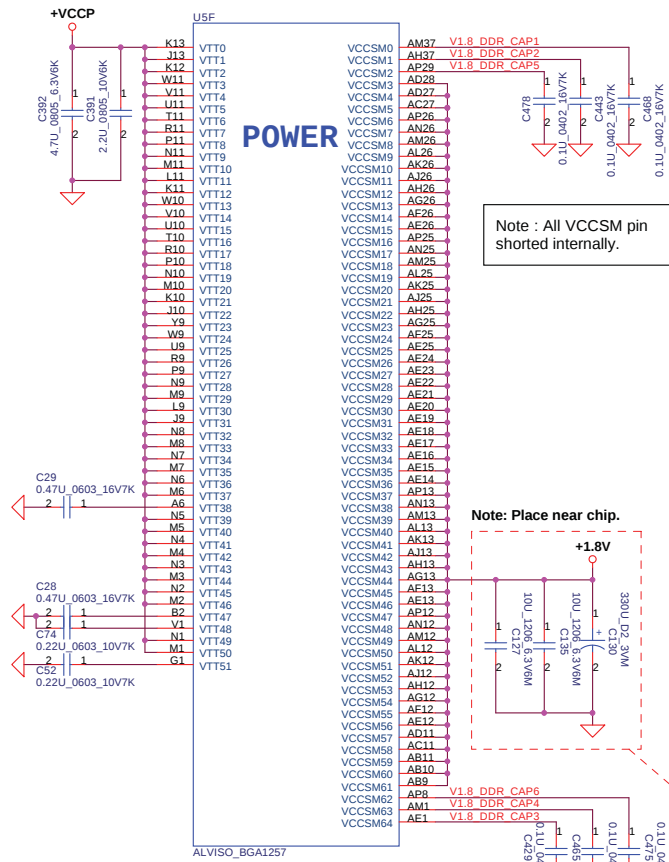
This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.



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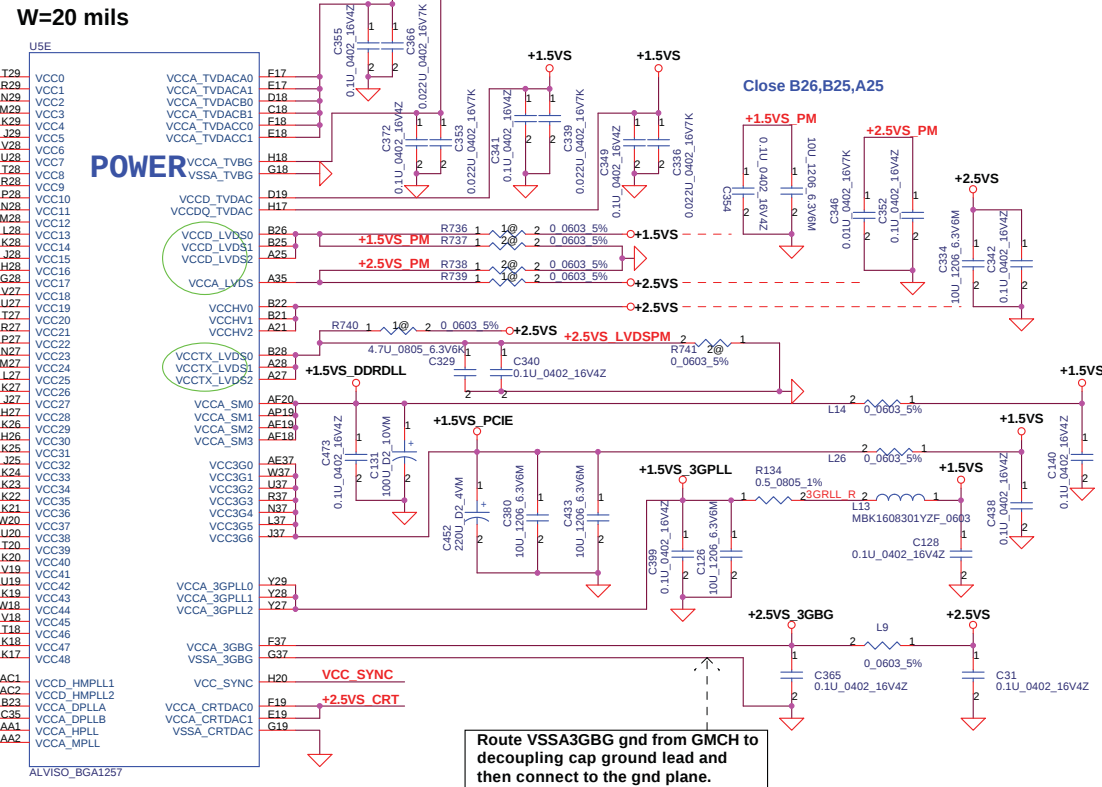


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		Size		Document Number				Rev	
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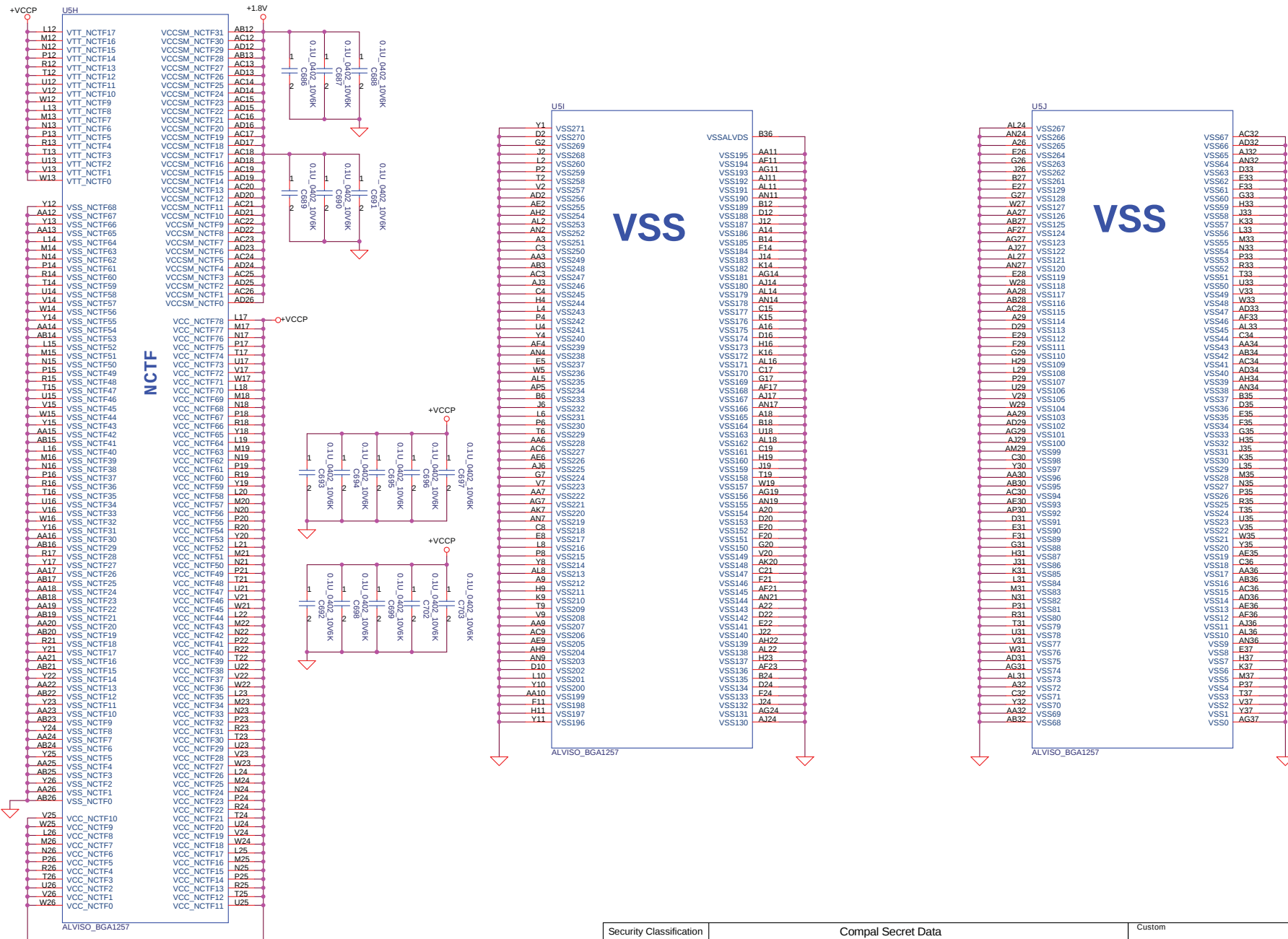


Note : C330, C348 No stuff for Ext. VGA. Stuff for Int. VGA.

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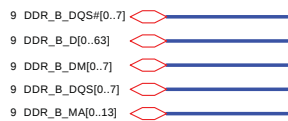


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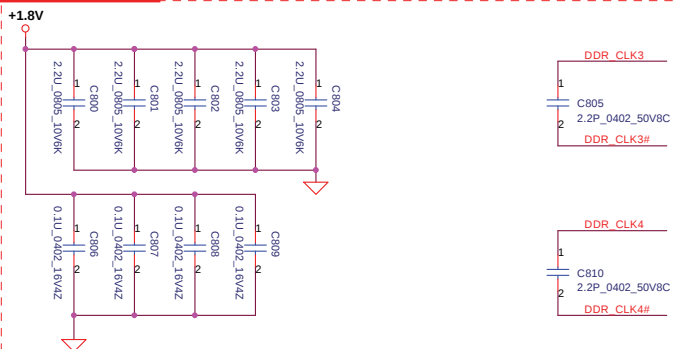


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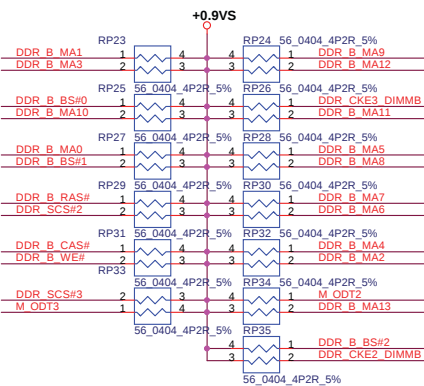
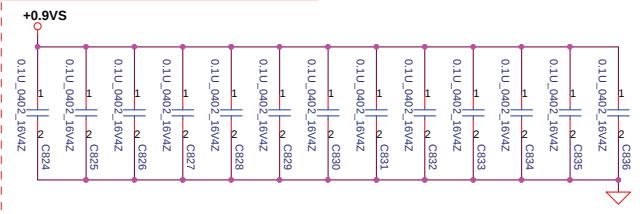




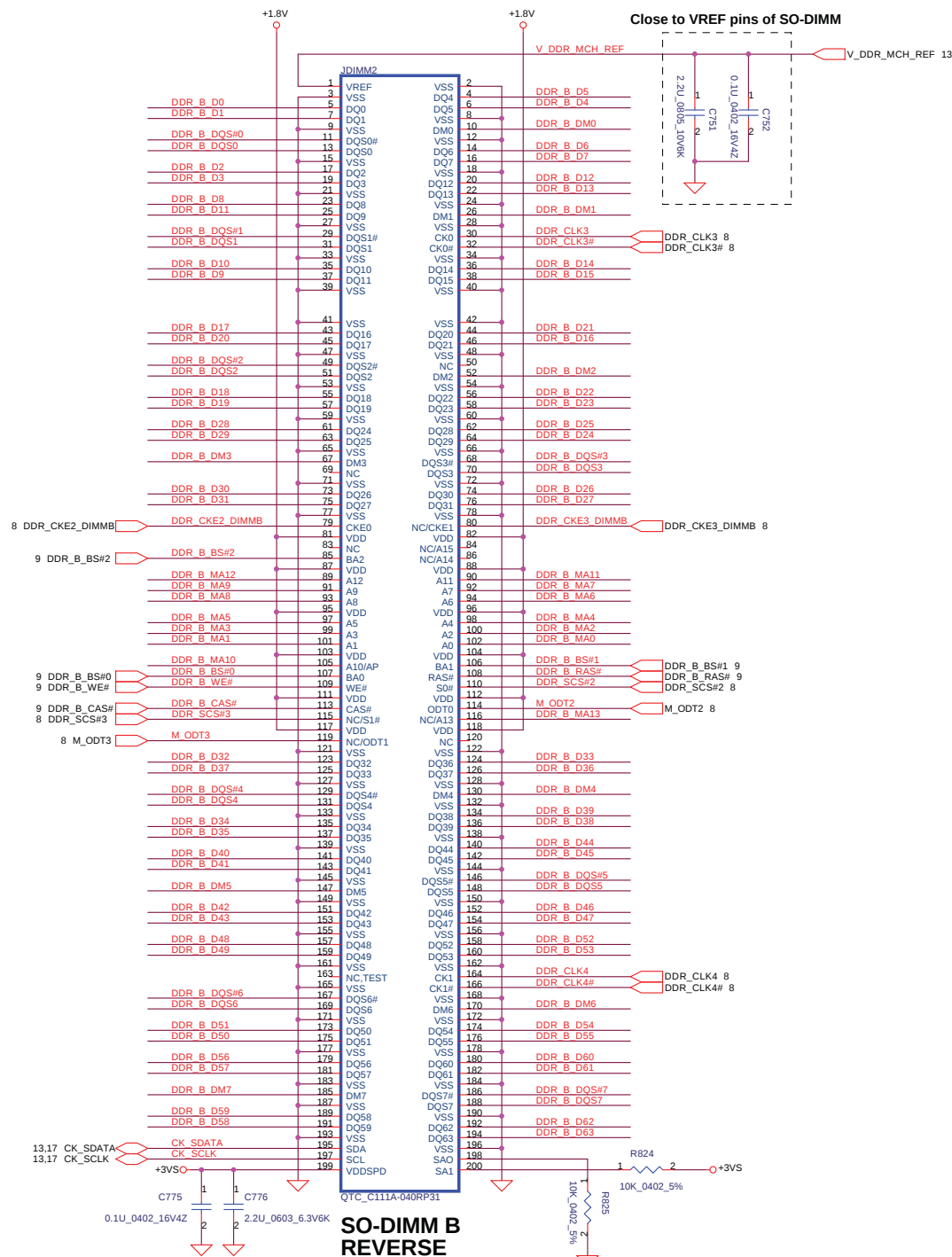
Layout Note:
Place near JDIMM2



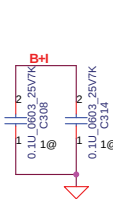
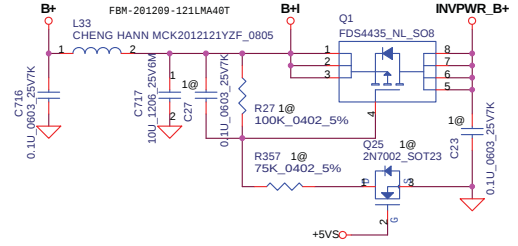
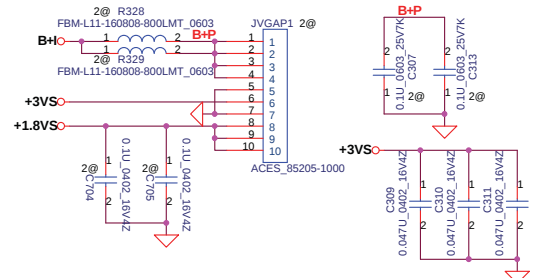
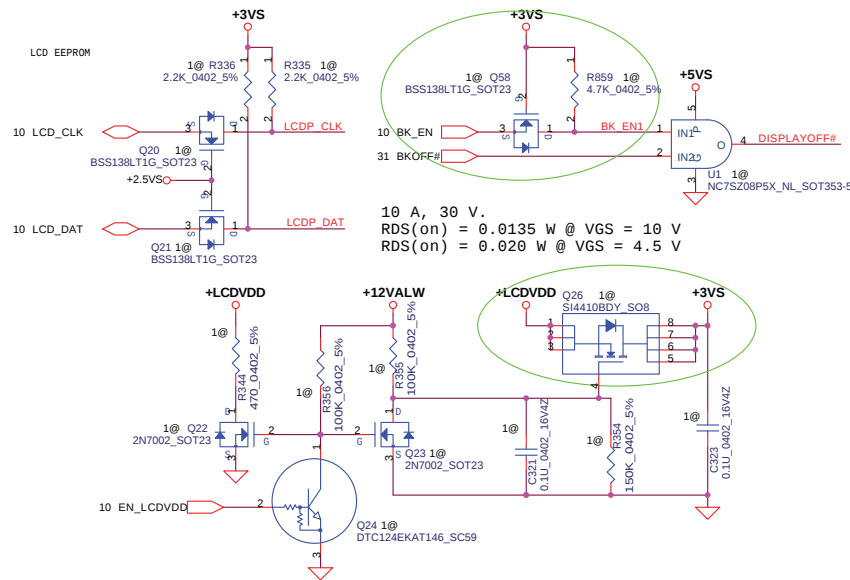
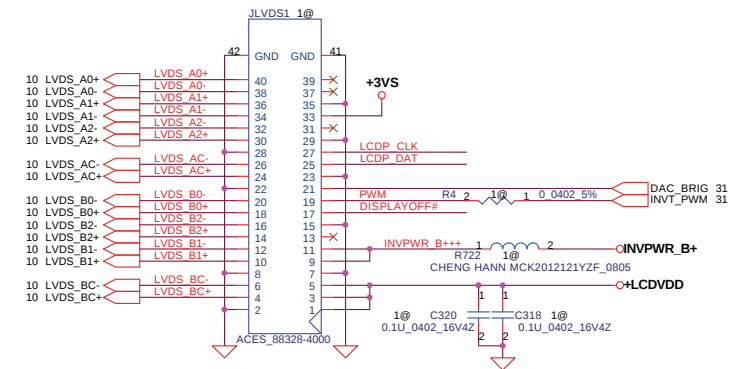
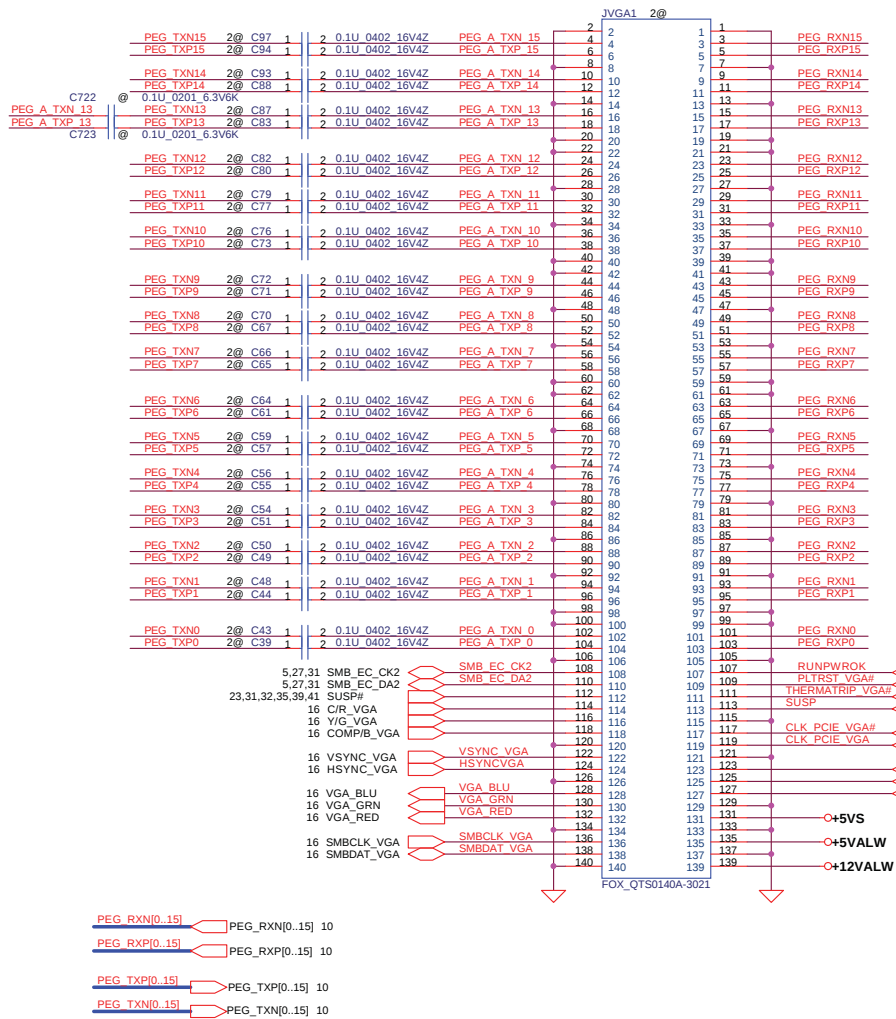
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JDIMM2, all trace length Max=1.5"

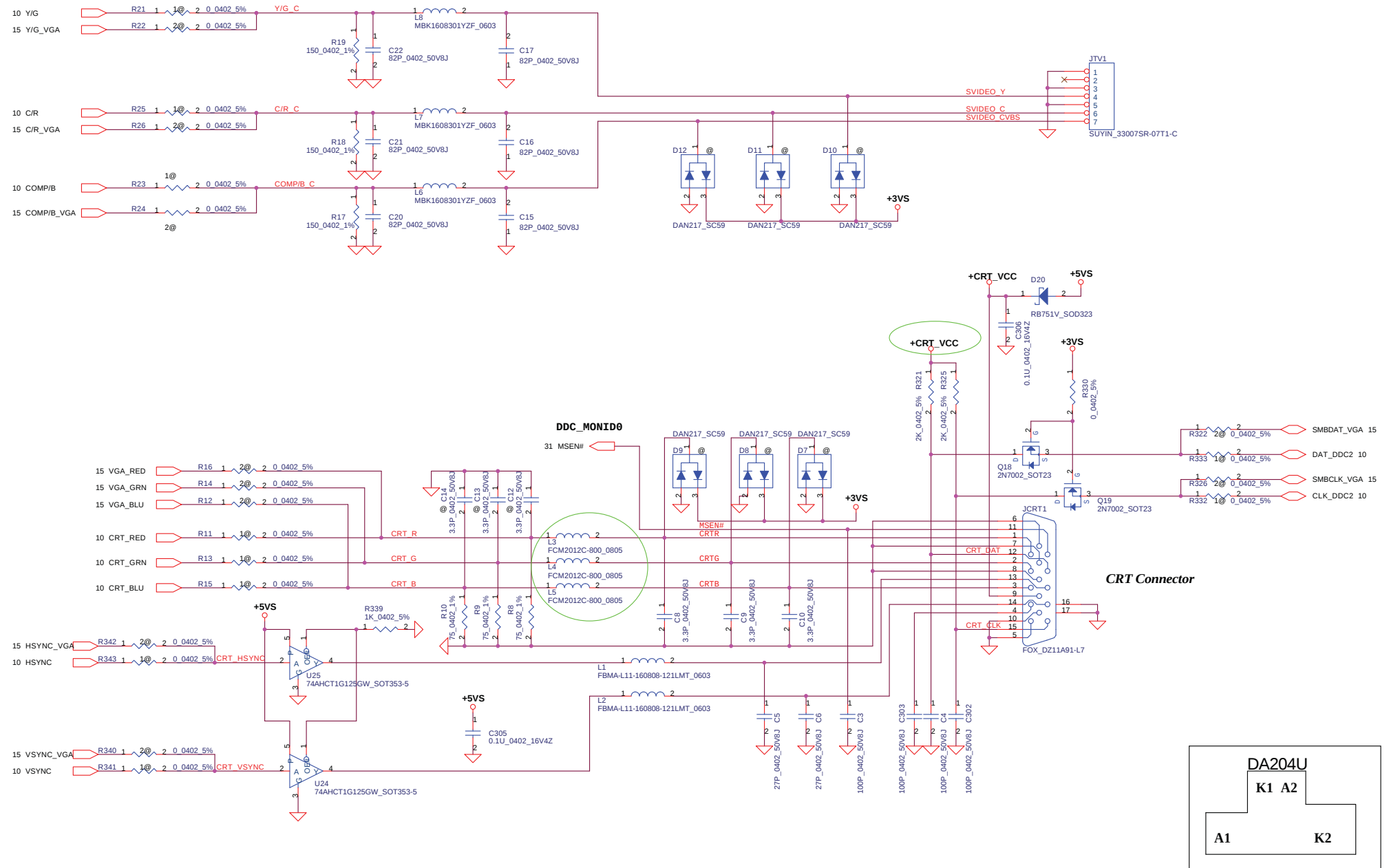


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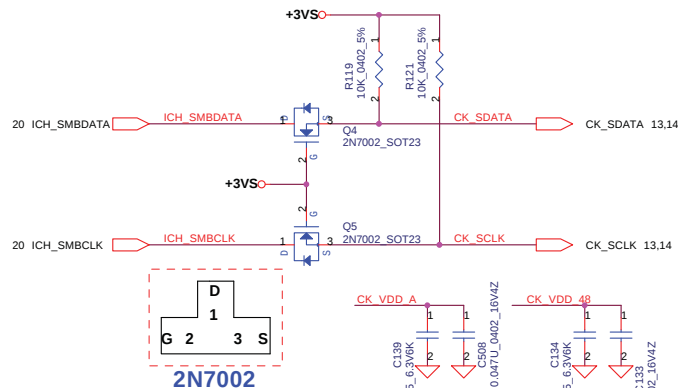


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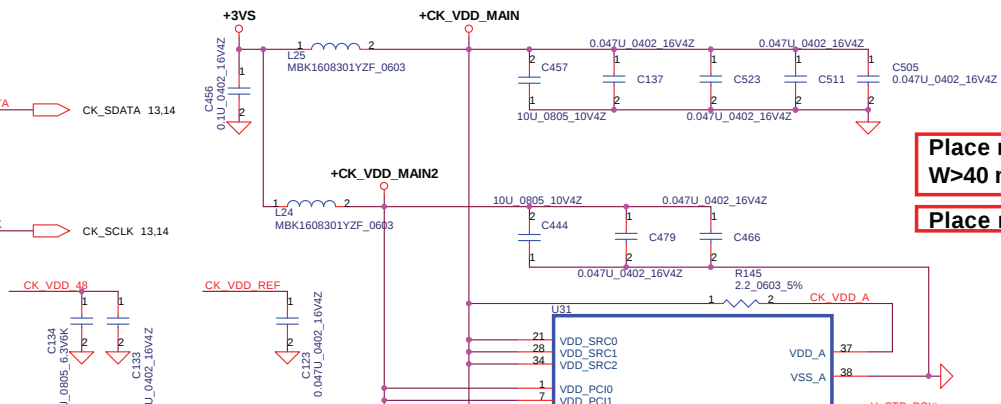
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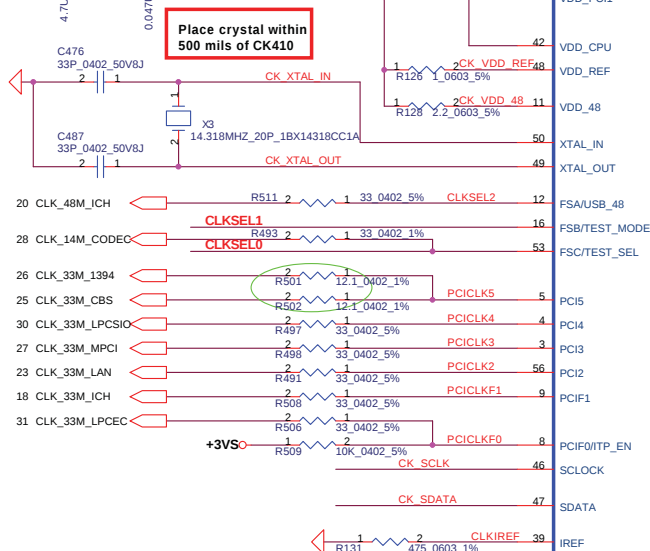
0 0 1 for Dothan-A 533Mhz
1 0 1 for Dothan-A 400Mhz

FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
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Table : ICS 954201 / Cypress CY28411

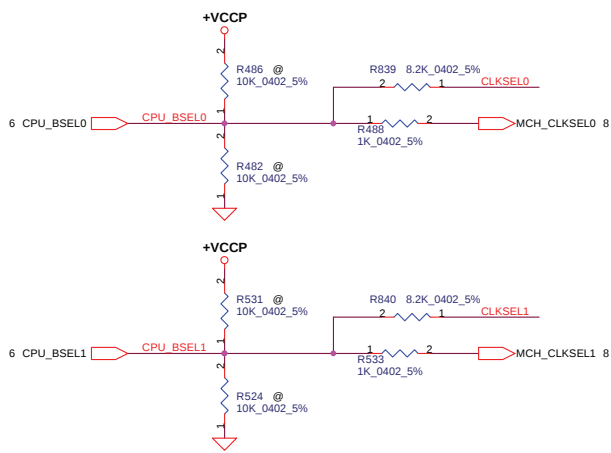
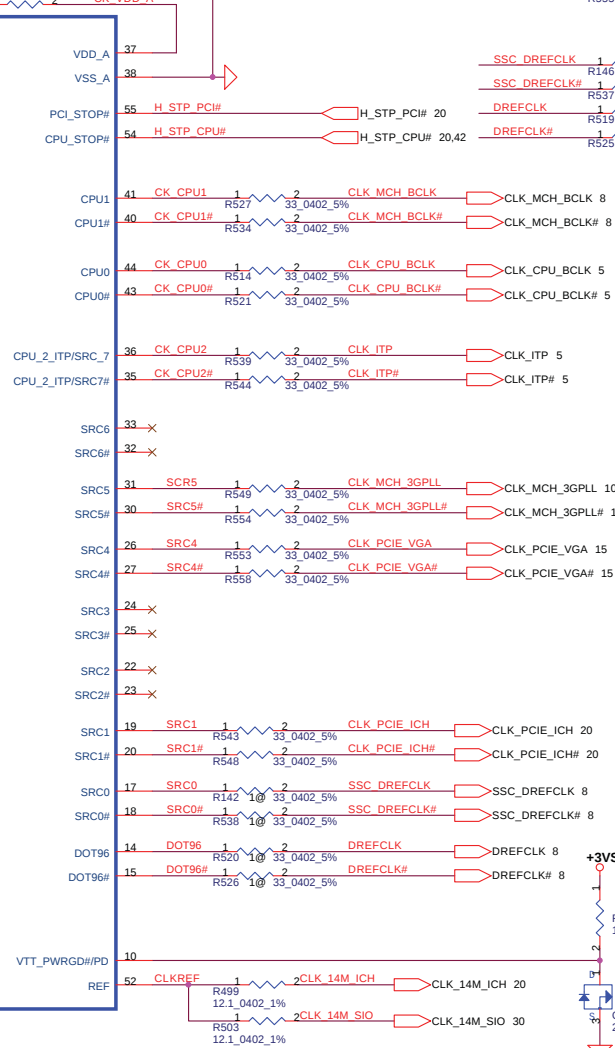
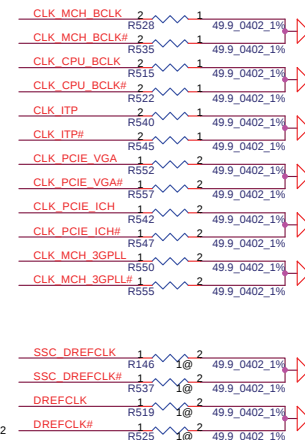


Place crystal within
500 mils of CK410



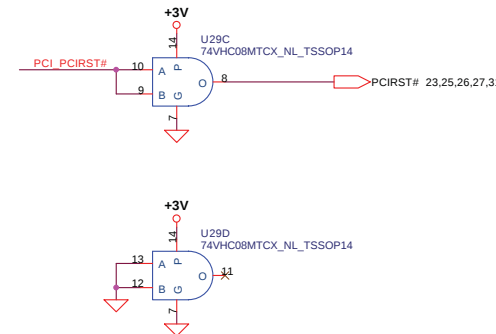
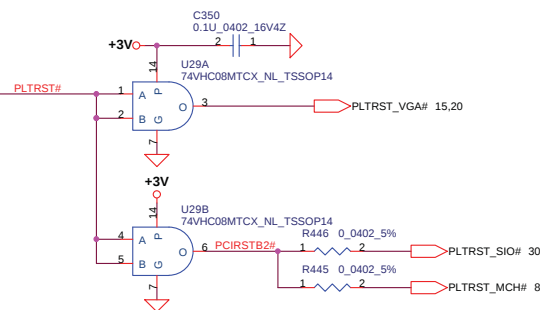
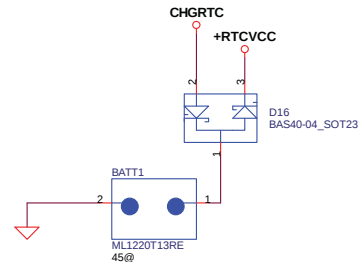
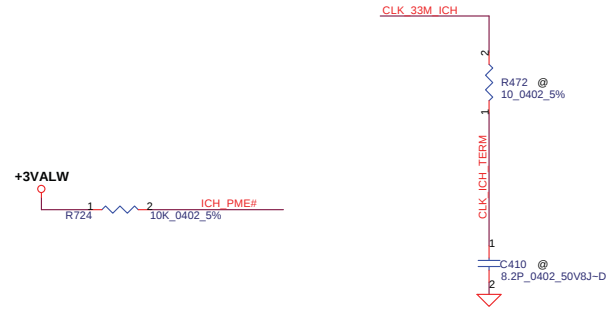
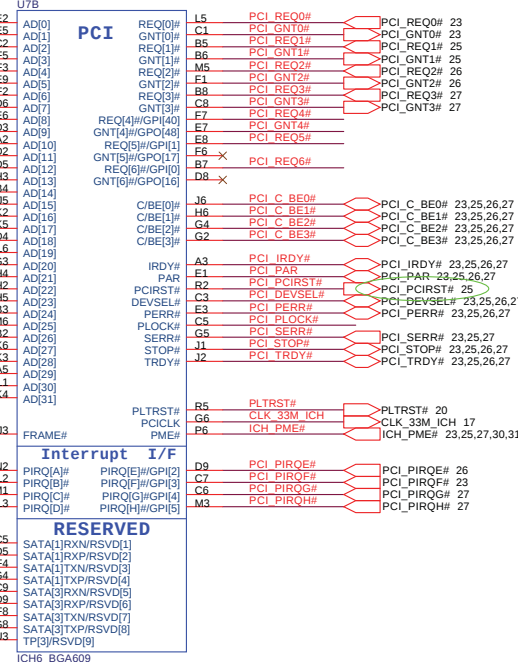
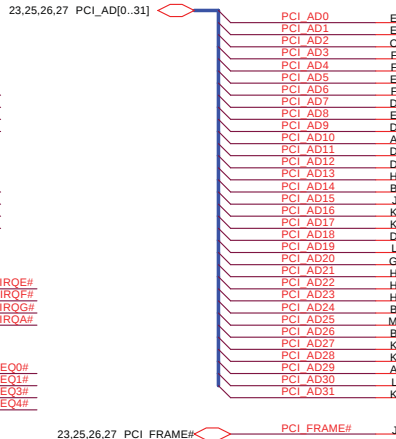
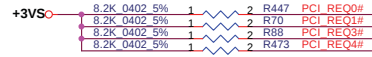
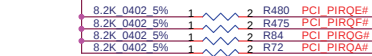
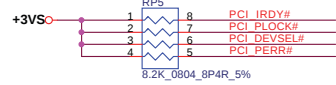
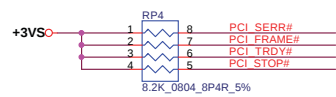
Place near each pin
W>40 mil

Place near CK410M



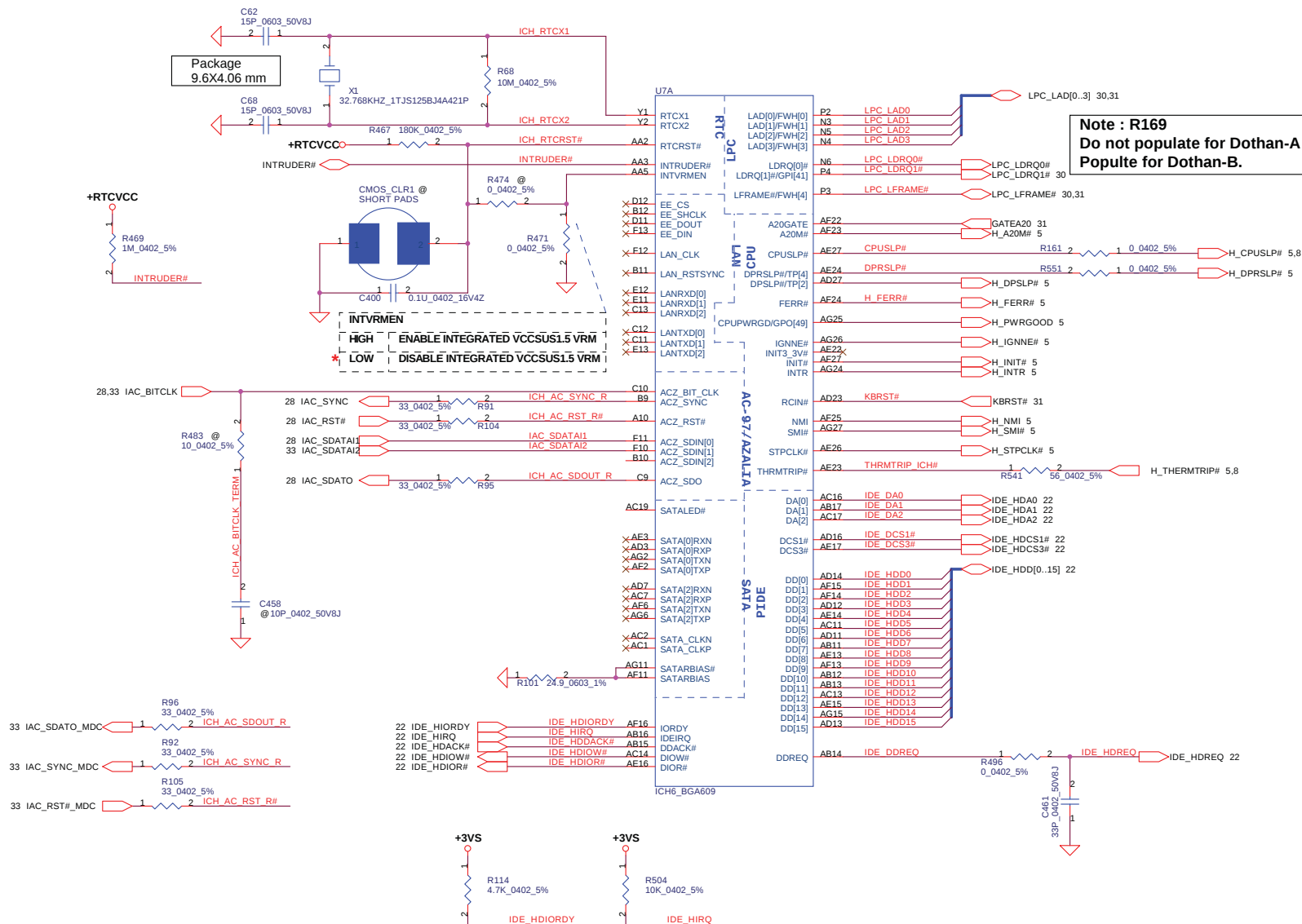
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Title Clock Generator			
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Size LA-3091		Rev 1.0	Date Tuesday, January 10, 2006
Sheet 18		of 44	

<http://www.compall.com.tw>

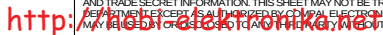


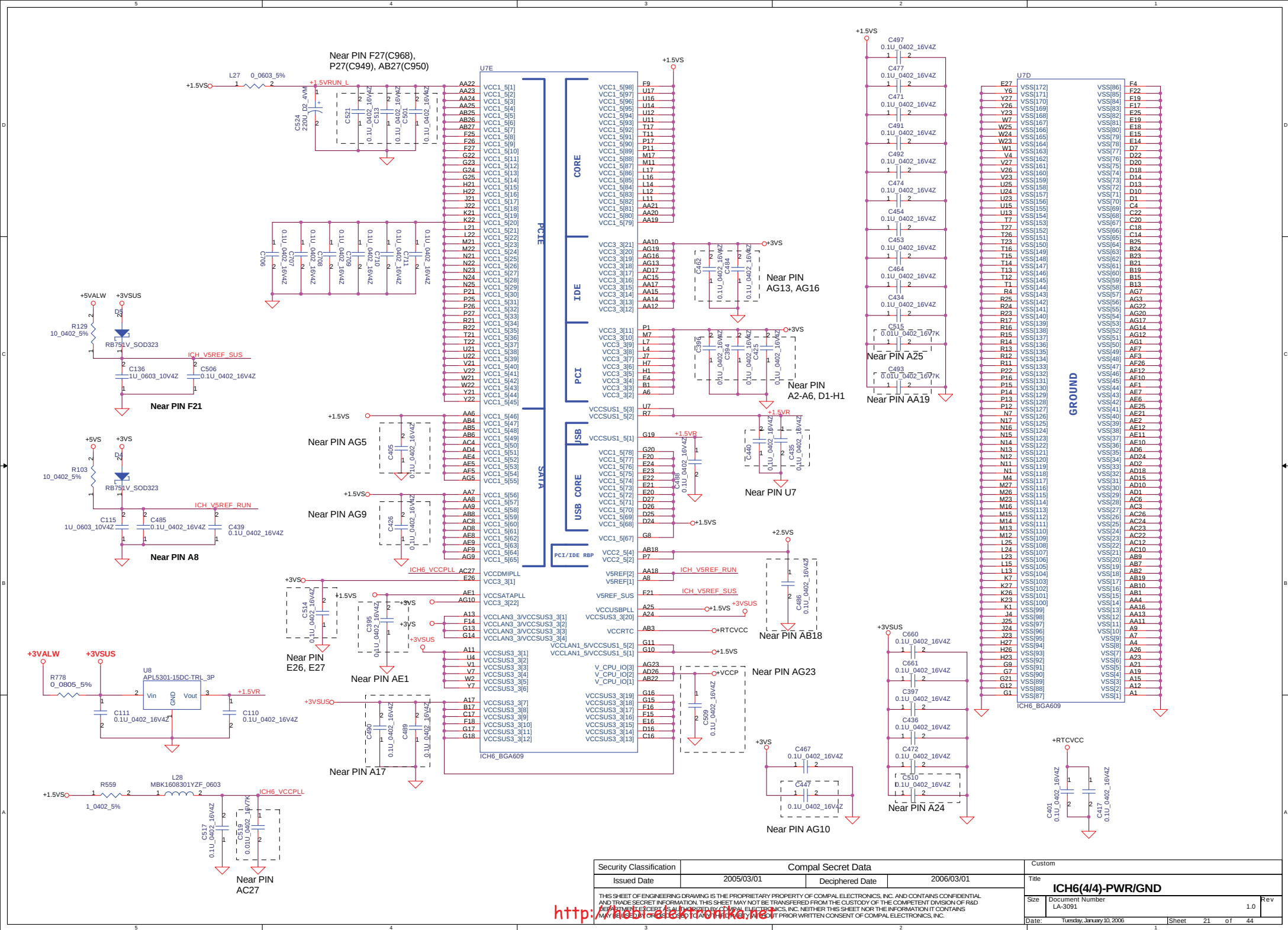
Note : R169
Do not populate for Dothan-A
Populte for Dothan-B.

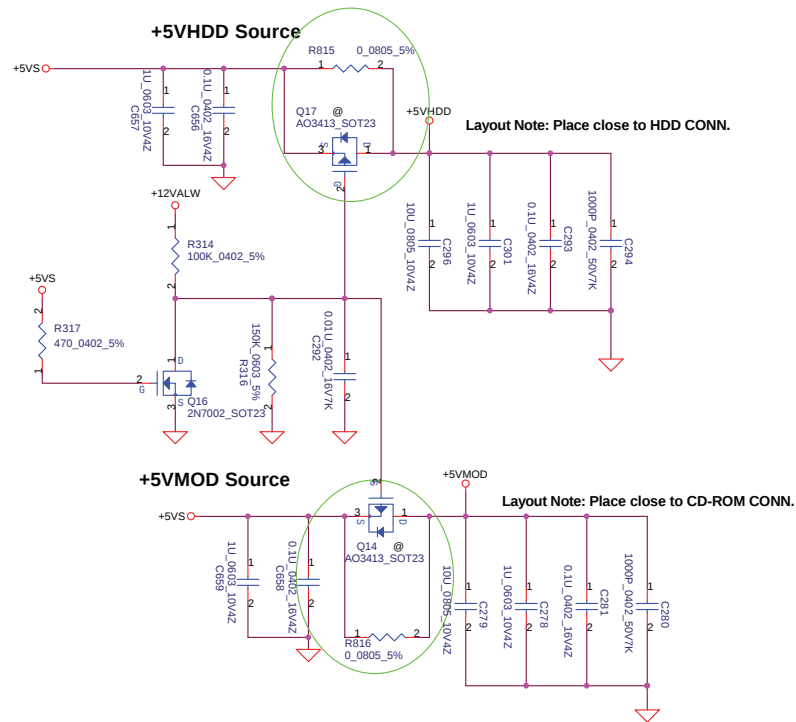
Note :
R161 Populte zero ohm for Dothan-A,
no stuff for Dothan-B.
R551 no stuff for Dothan-A,
Populte zero ohm for Dothan-B.
Stuff R546 for Dothan B, no stuff R352 for Dothan A

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Date: Tuesday, January 10, 2006				Sheet	19 of 44

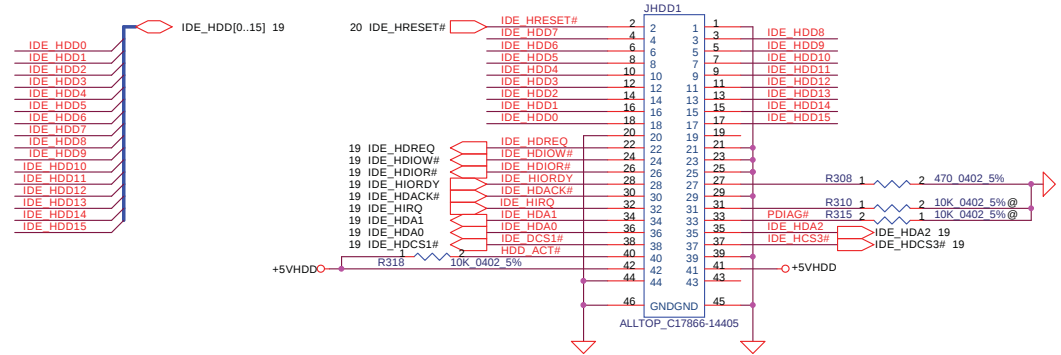
<http://www.compall.com.tw>





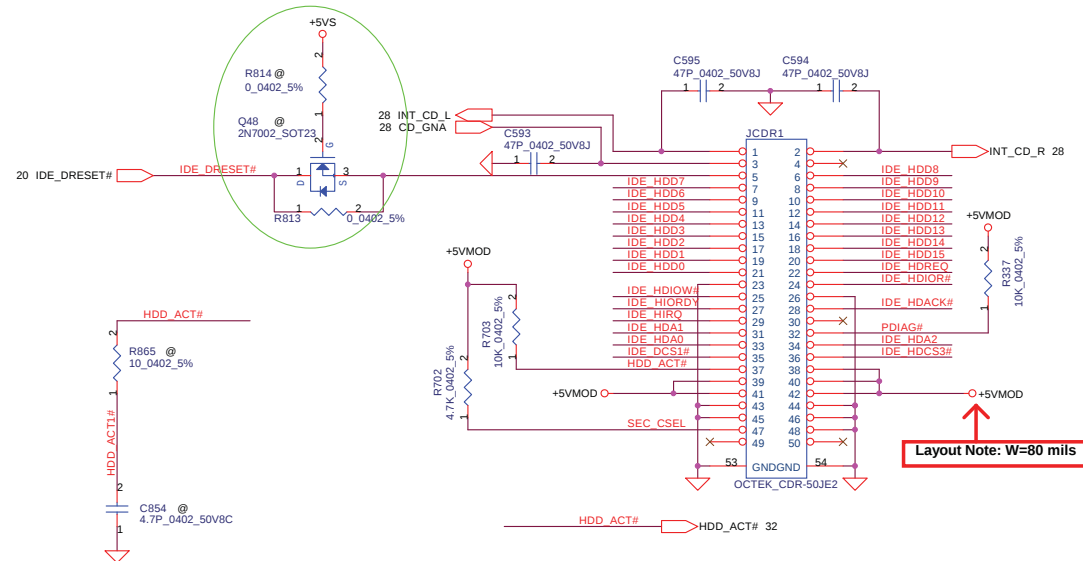


HDD Connector



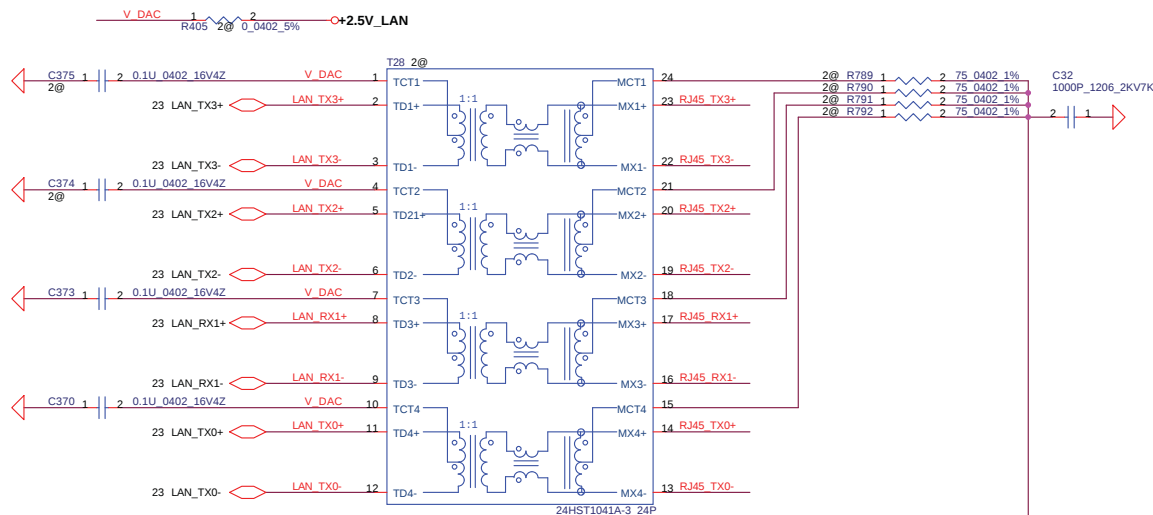
IRQ how to assign

CD-ROM Connector



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Size	Document Number LA-3091	Rev	1.0
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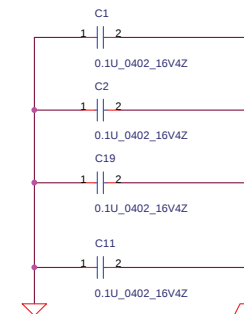
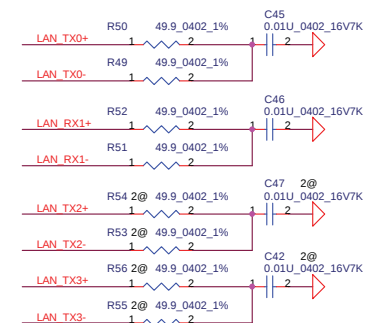
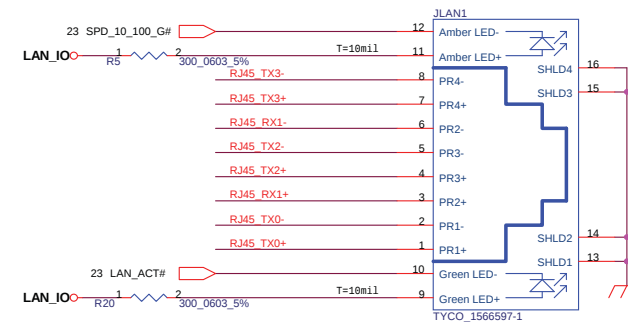
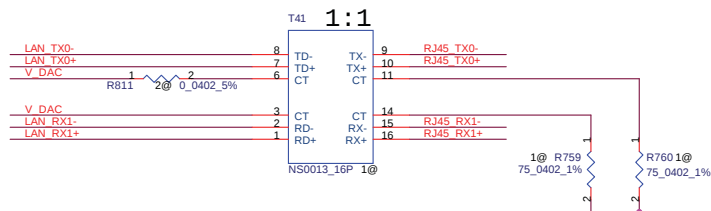
RTL8110SBL used the 24HST1041A-3_24P

RTL8100CL used the 24ST0023-3_24P

Layout Note

24HST1041A-3 pls close to conn.

Termination plane should be copied to chassis ground and also depends on safety concern

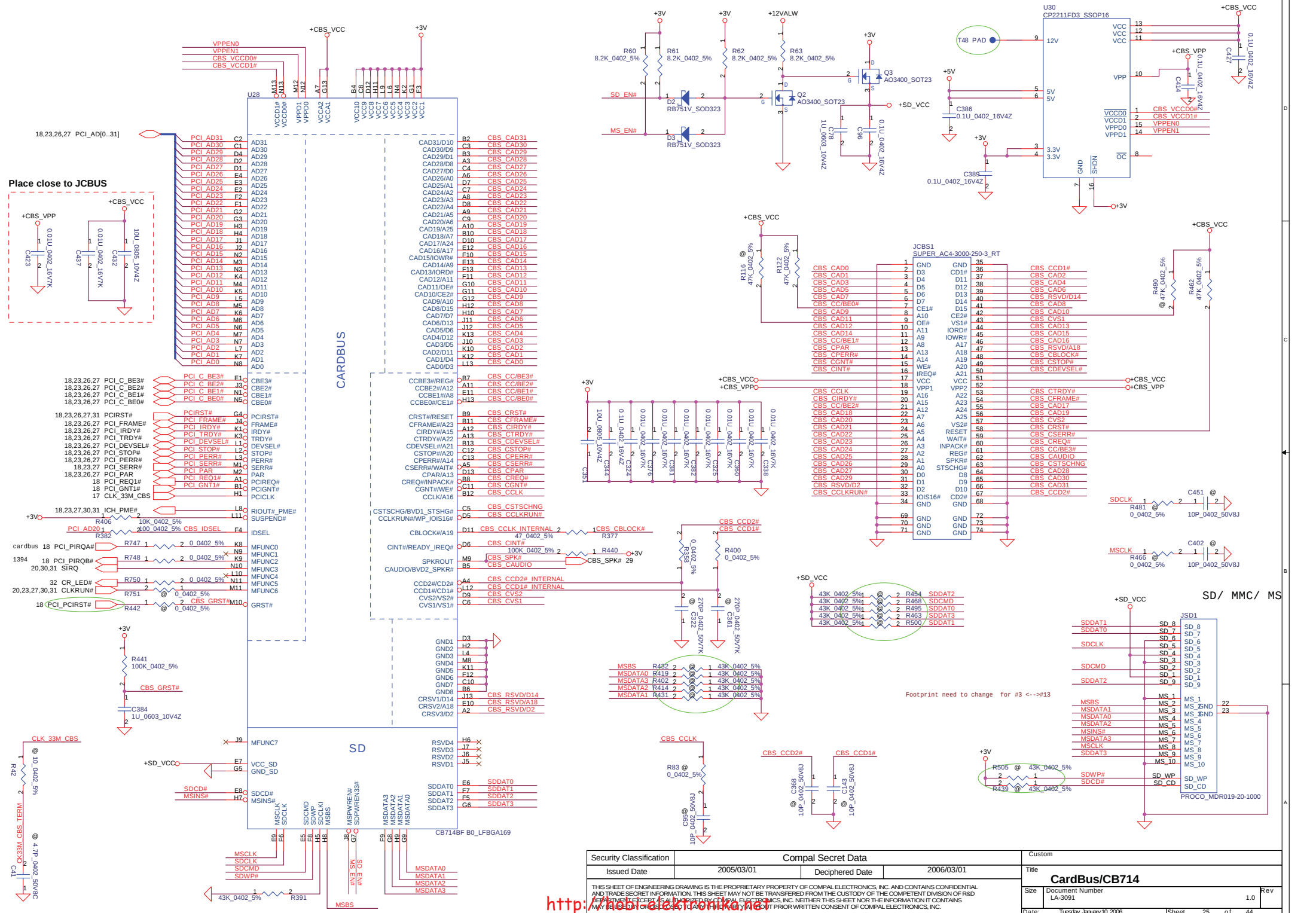


Termination plane should be copied to chassis ground and also depends on safety concern

Please close to LAN IC

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								Size		Document Number		1.0		Rev	
								Date:		Tuesday, January 10, 2006		Sheet		24 of 44	

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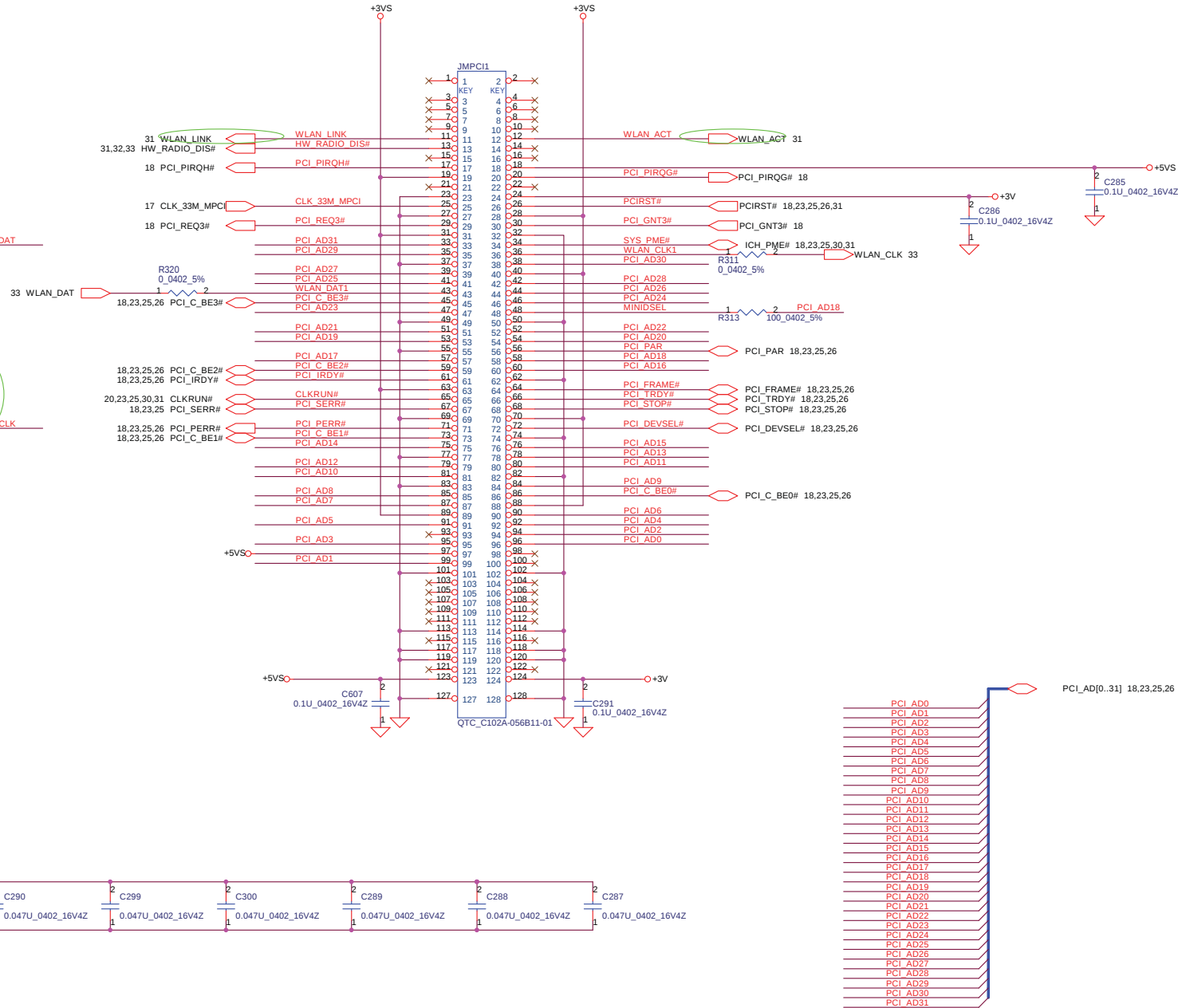
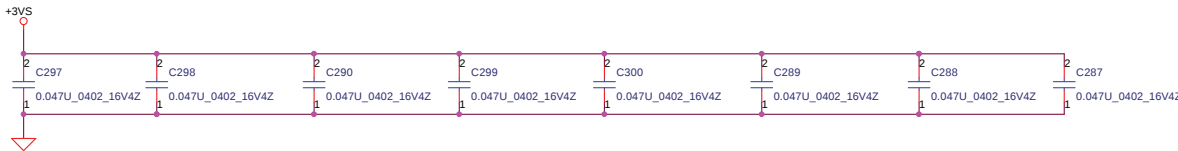
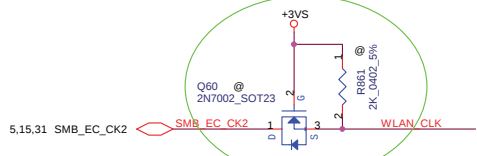
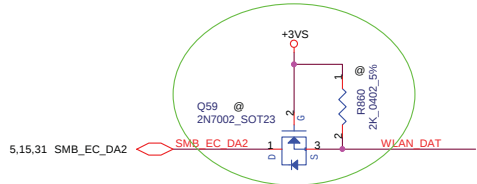


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Date:		Tuesday, January 10, 2006		Sheet		25		of		44	

Intel WLAN HW Spec

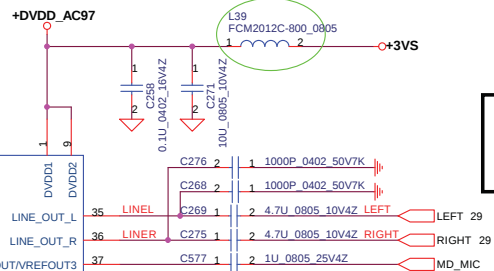
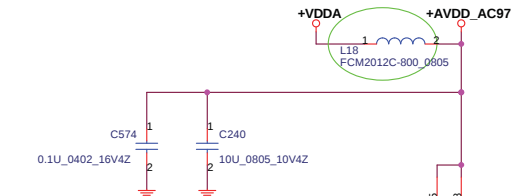
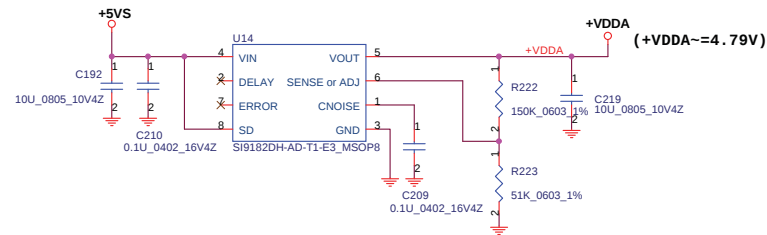
Pin36:
Channel_Clk/BT_PRIORITY

Pin43:
Channel_Data_11b_activity

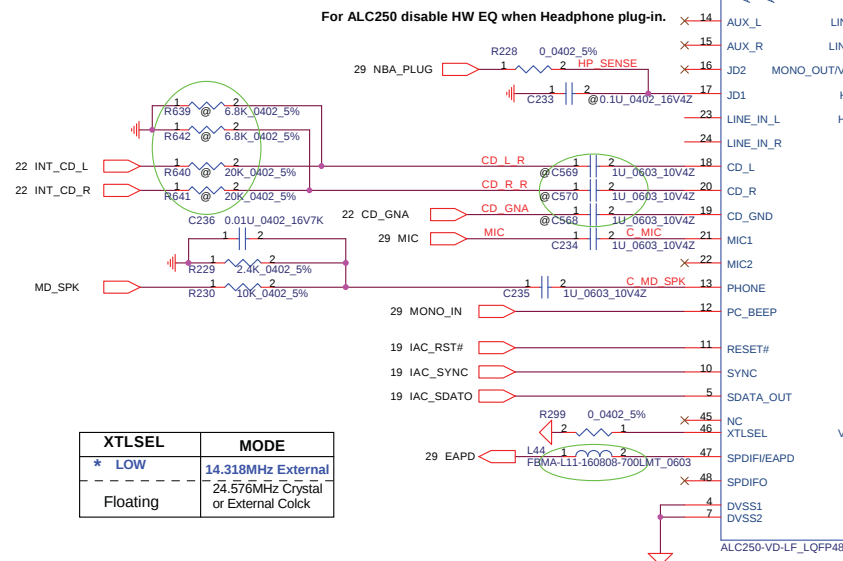


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Size	Document Number	Rev		Date	
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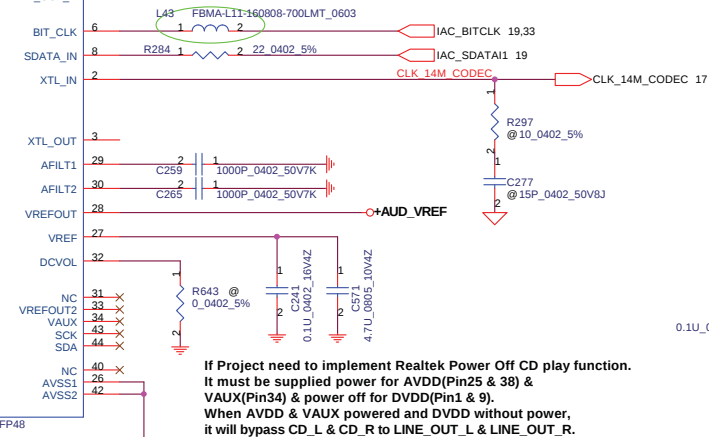
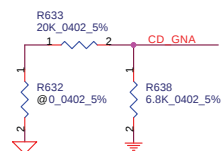
AC97 Codec



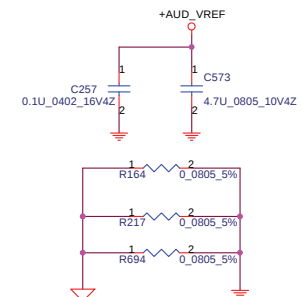
When Project need implement Headphone channel output from Audio Codec pin 39 & 41, it must have another driver to support JD function to change signal path from LINE_OUT_L & LINE_OUT_R to HP_OUT_L & HP_OUT_R when headphone insert.

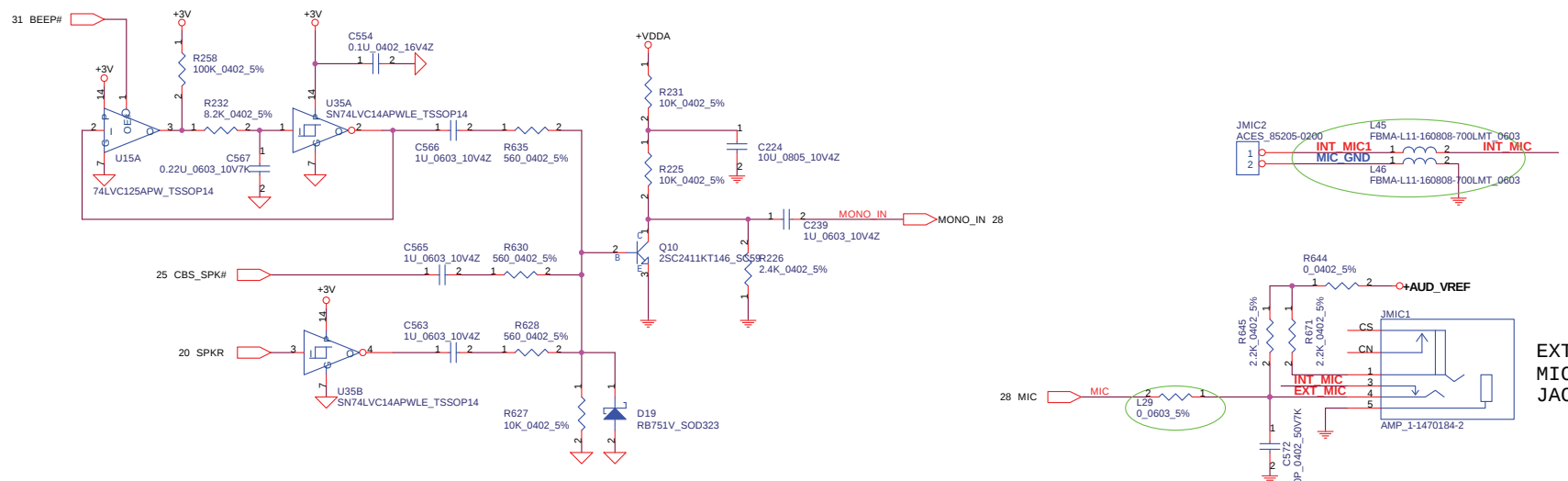
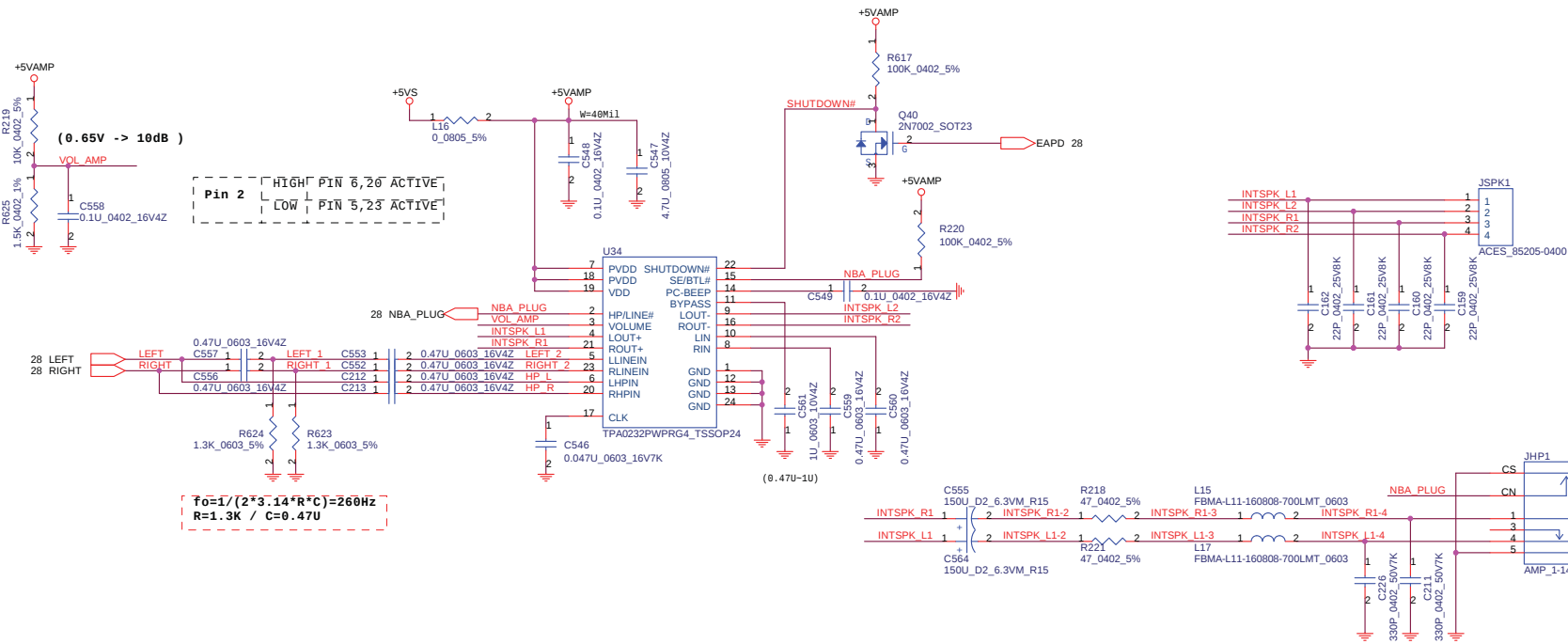


XTLSEL	MODE
* LOW	14.318MHz External
Floating	24.576MHz Crystal or External Colck



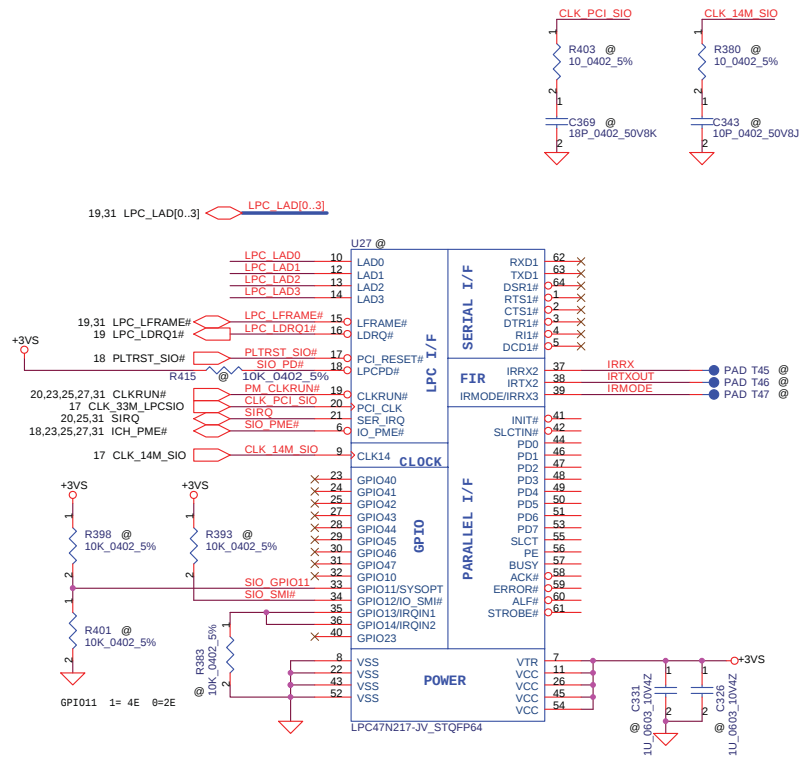
MODE	SHUT DOWN	POWER OFF CD Play	NORMAL	NORMAL
DVDD(1/9)	0	0	1	1
VAUX(34)	0	1	0	1





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		LA-3091							
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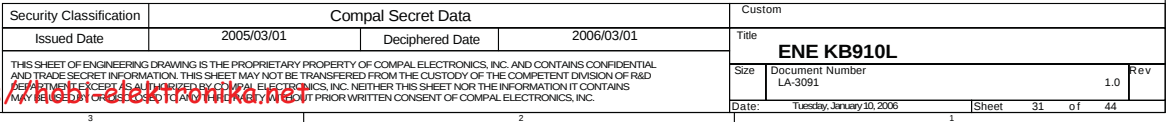


FIR Module

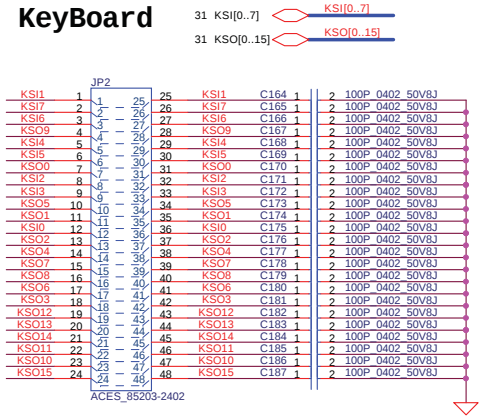
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Issued Date		2005/03/01		Deciphered Date		2006/03/01		Title			
								SUPER I/O and FIR			
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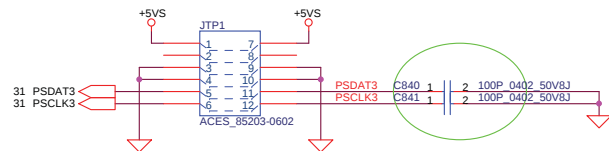
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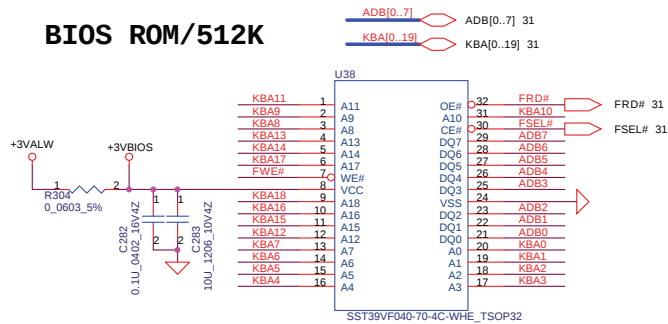
KeyBoard



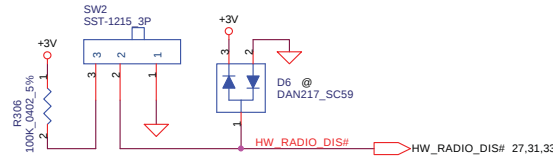
T/P



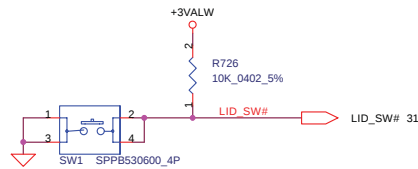
BIOS ROM/512K



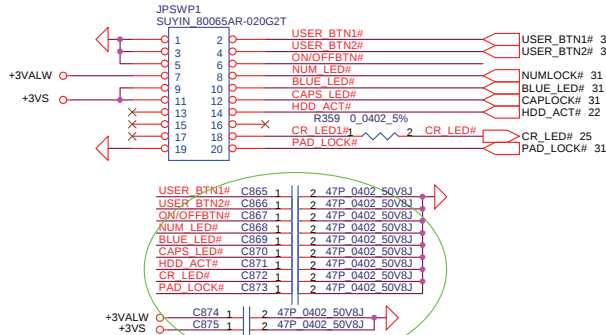
Killer switch



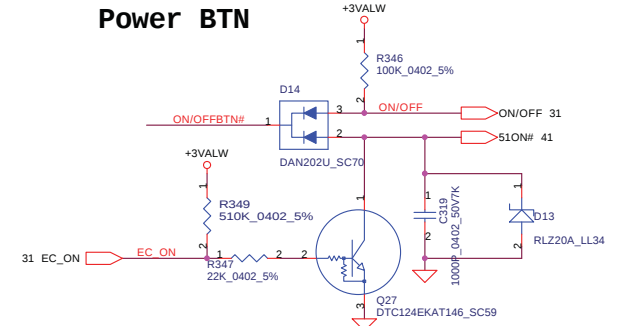
LID Switch



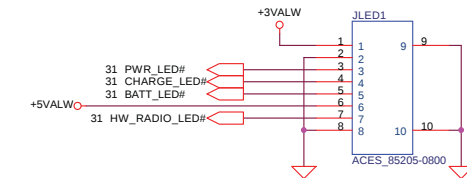
SW Board



Power BTN



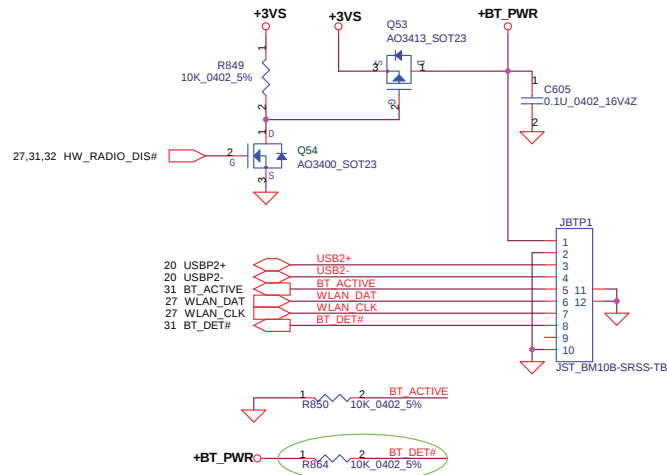
LED Board



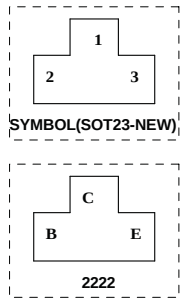
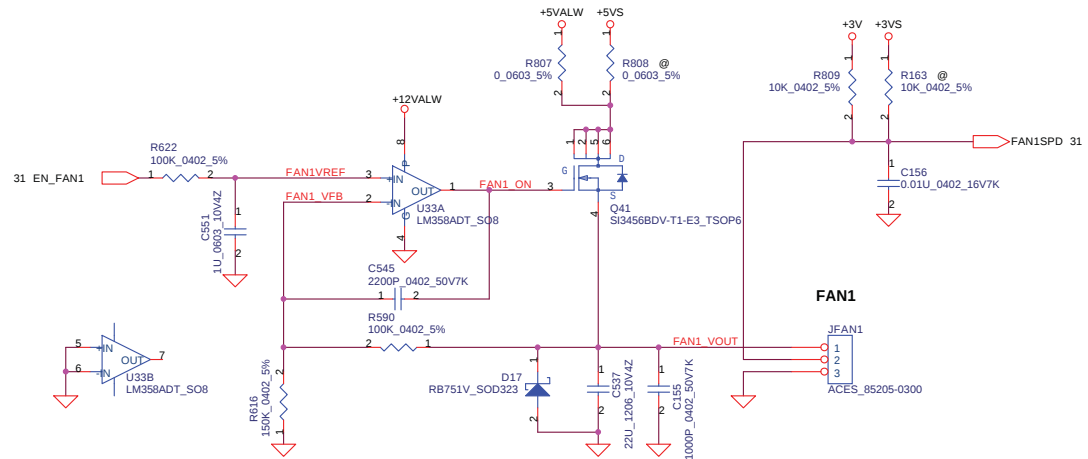
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				LA-3091	1.0
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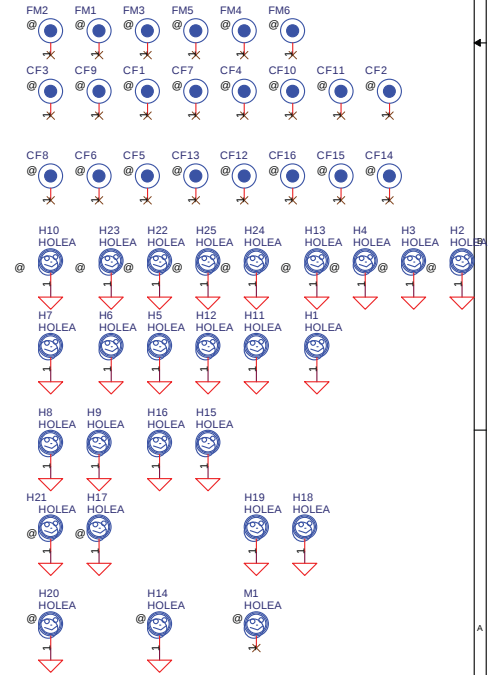
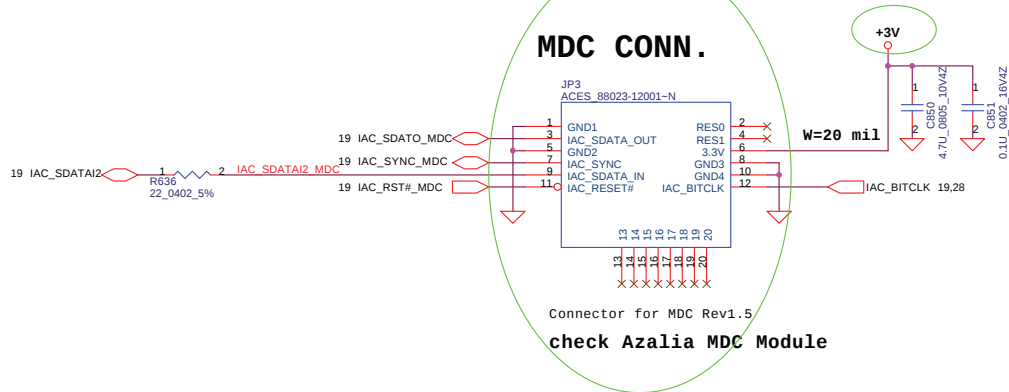
Blue Tooth



FAN1 Control and Tachometer

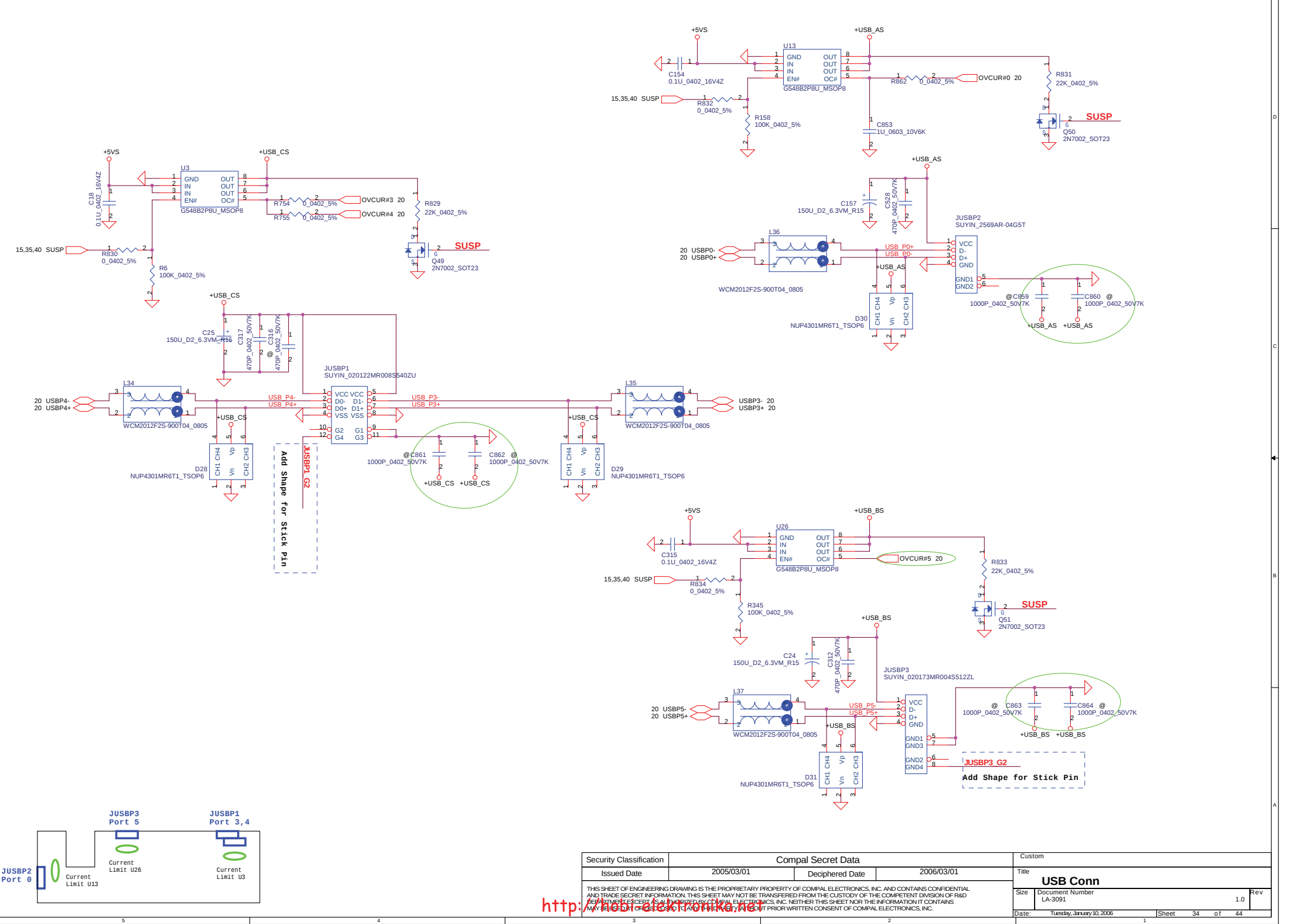


MDC CONN.



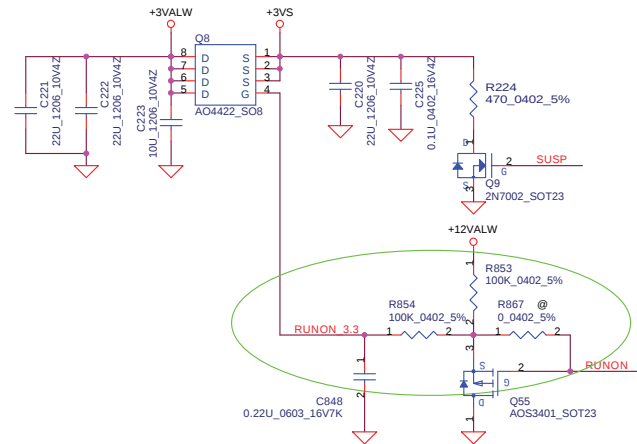
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				MDC / Blue Tooth / Fan	
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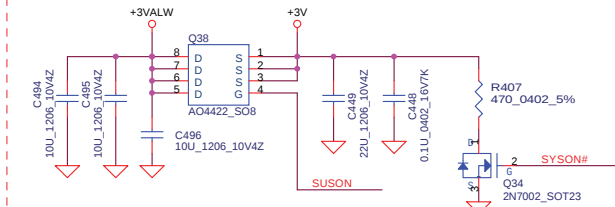


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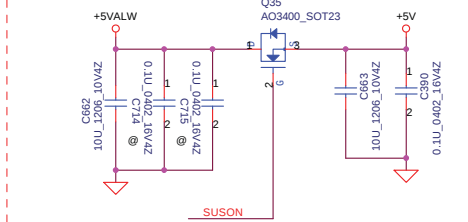
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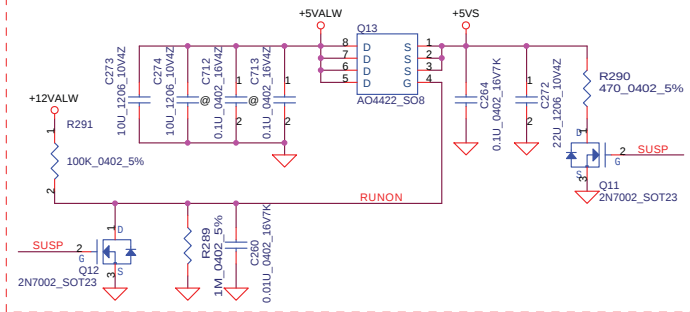
+3VALW to +3V Transfer



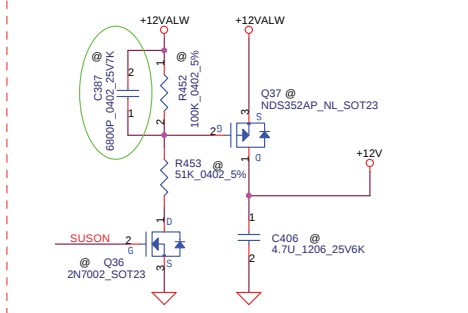
+5VALW to +5V Transfer



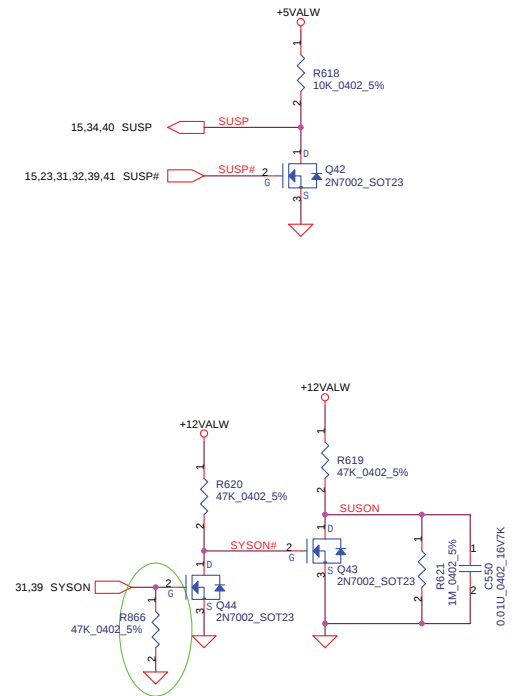
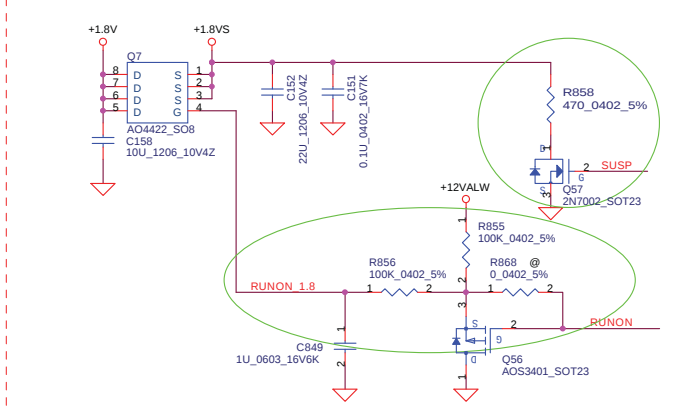
+5VALW to +5VS Transfer



+12VALW to +12V Transfer

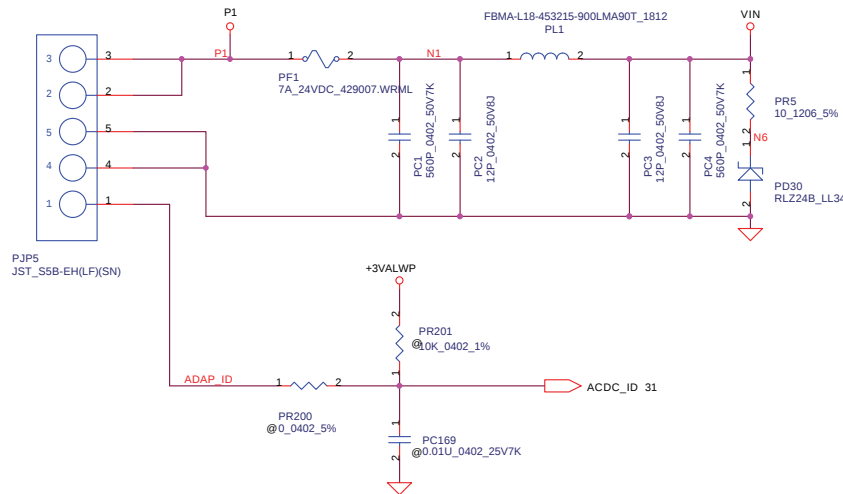


+1.8V to +1.8VS Transfer

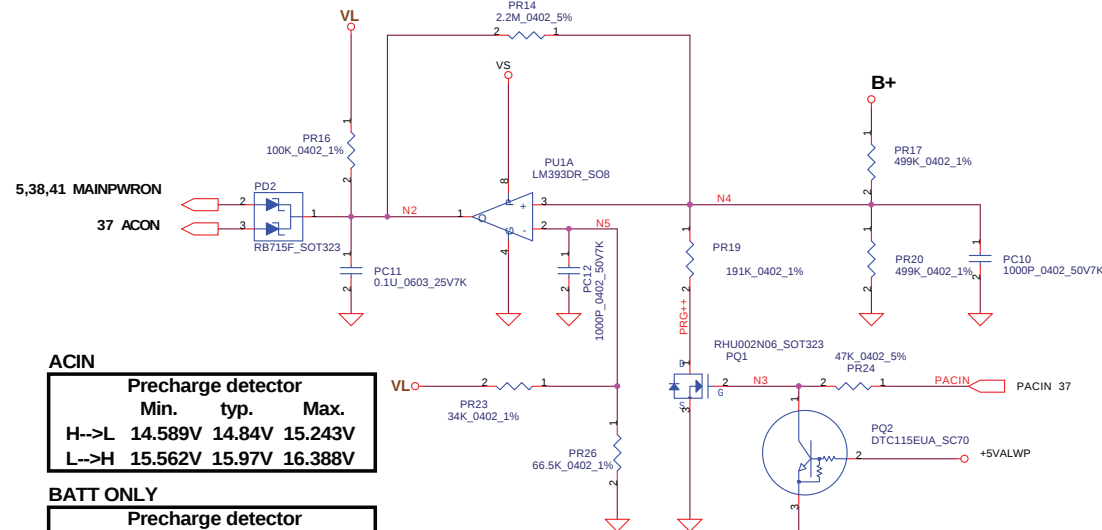
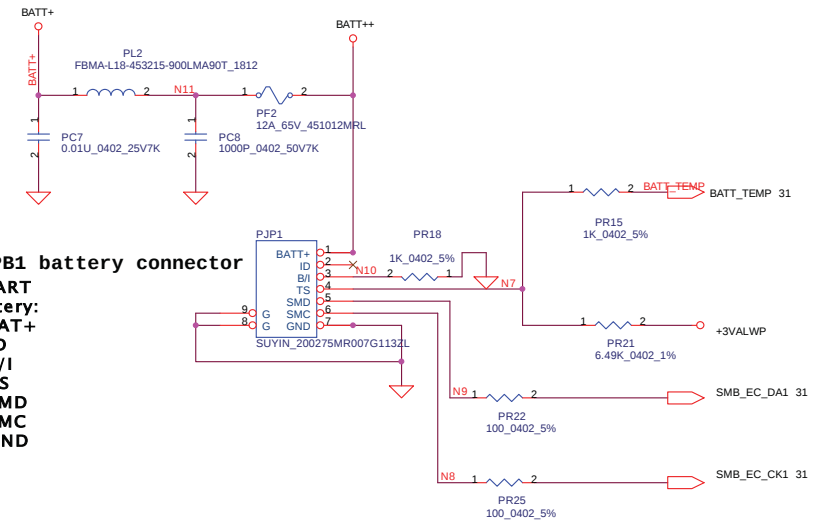


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<http://www.backhome.net>



PJPB1 battery connector
SMART
Battery:
1.BAT+
2.ID
3.B/I
4.TS
5.SMD
6.SMC
7.GND

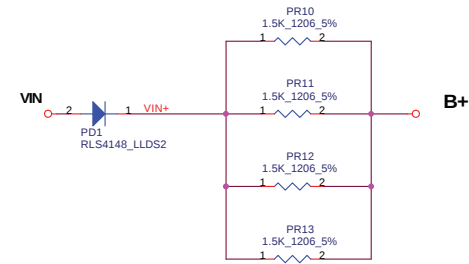


ACIN

Precharge detector			
Min.	typ.	Max.	
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

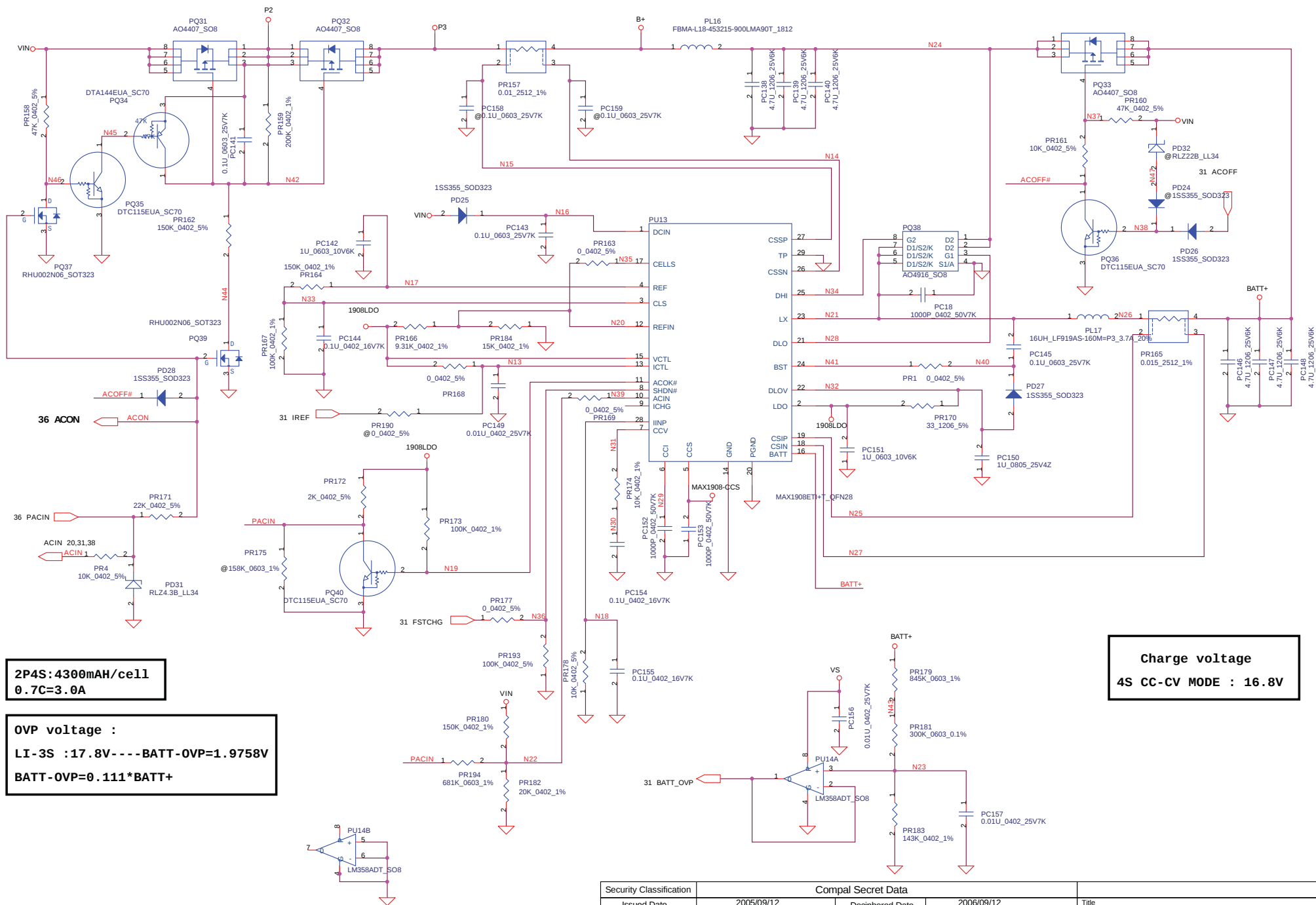
BATT ONLY

Precharge detector			
Min.	typ.	Max.	
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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2006/09/12				2006/09/12				DCIN & DETECTOR & Precharge			
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<http://icn.electronics.com>

I_{adp}=0~3A(65W)

2P4S:4300mAh/cell
0.7C=3.0A

OVP voltage :

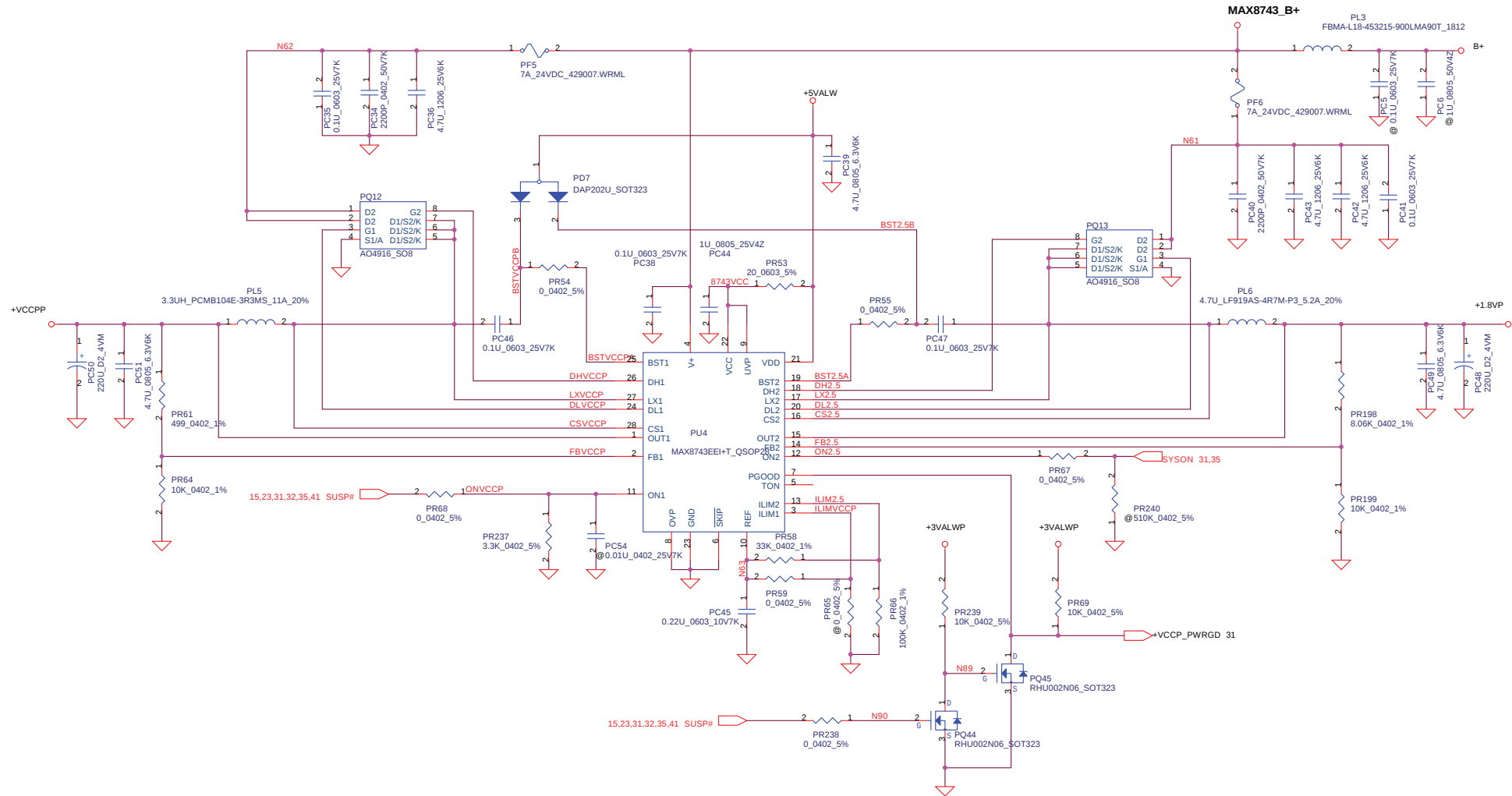
LI-3S :17.8V---BATT-OVP=1.9758V

BATT-OVP=0.111*BATT+

Charge voltage
4S CC-CV MODE : 16.8V

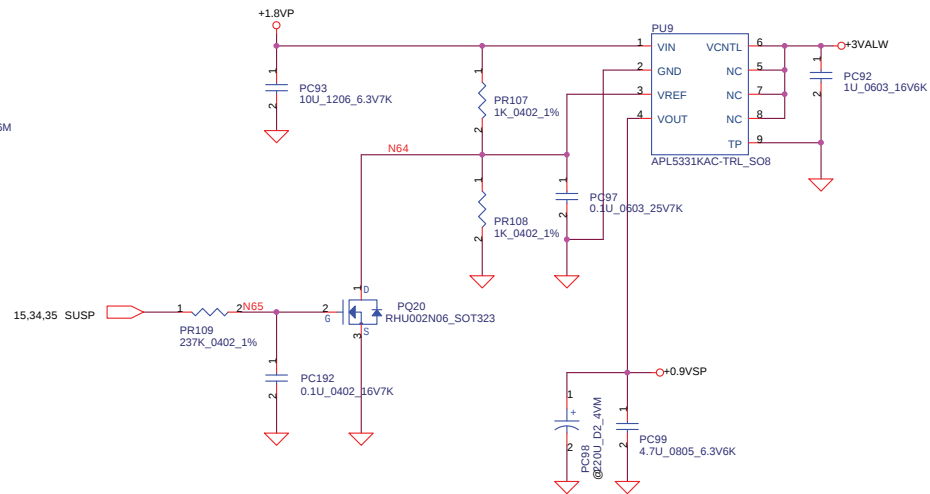
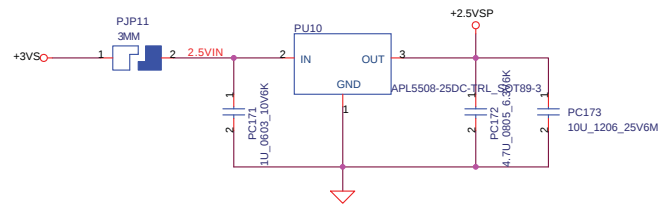
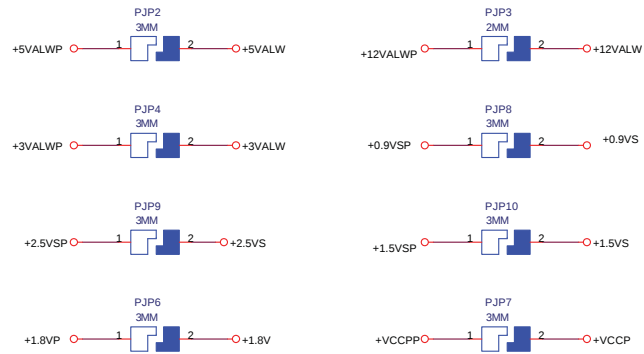
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+1.8VP / +VCCPP



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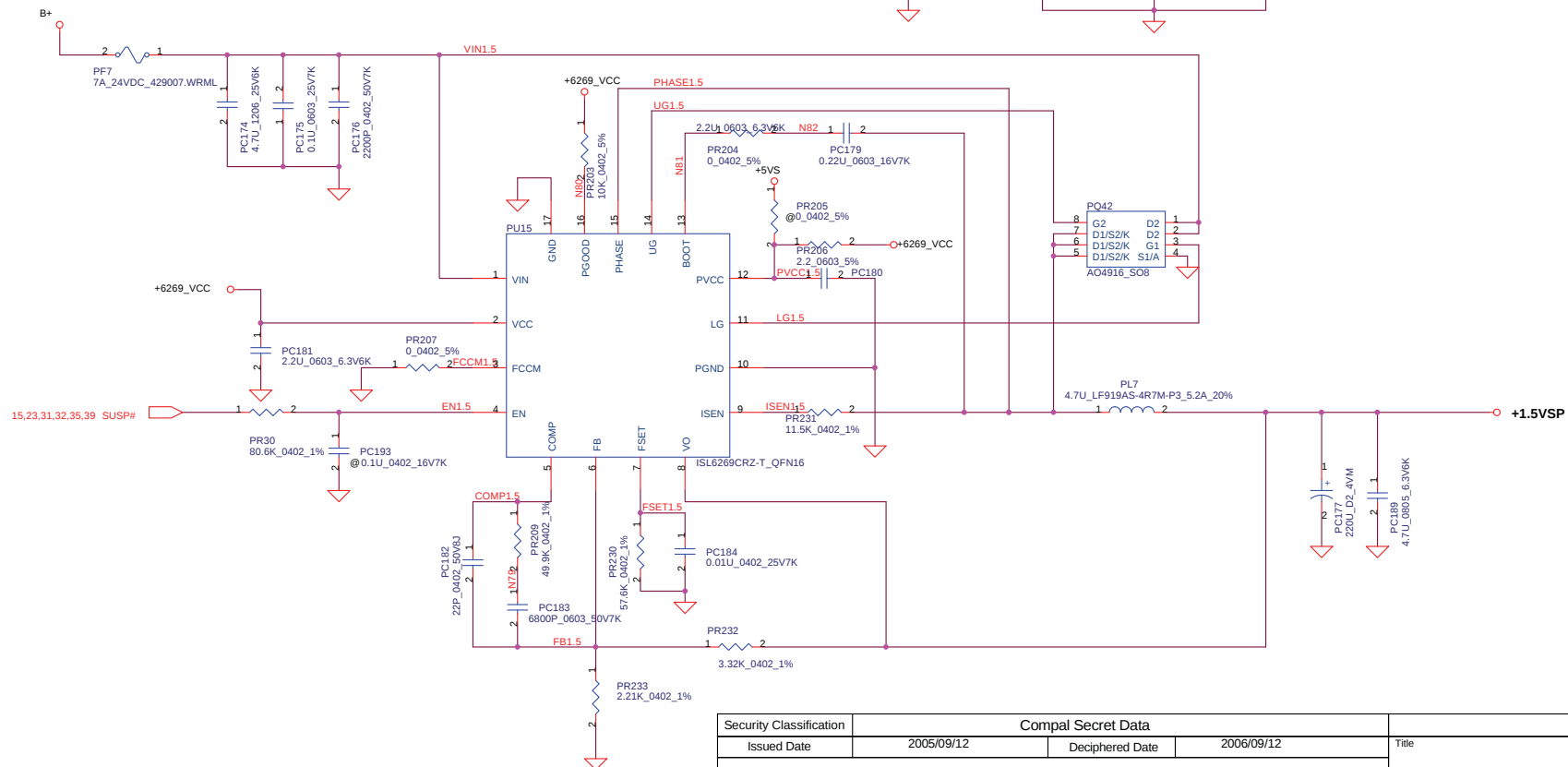
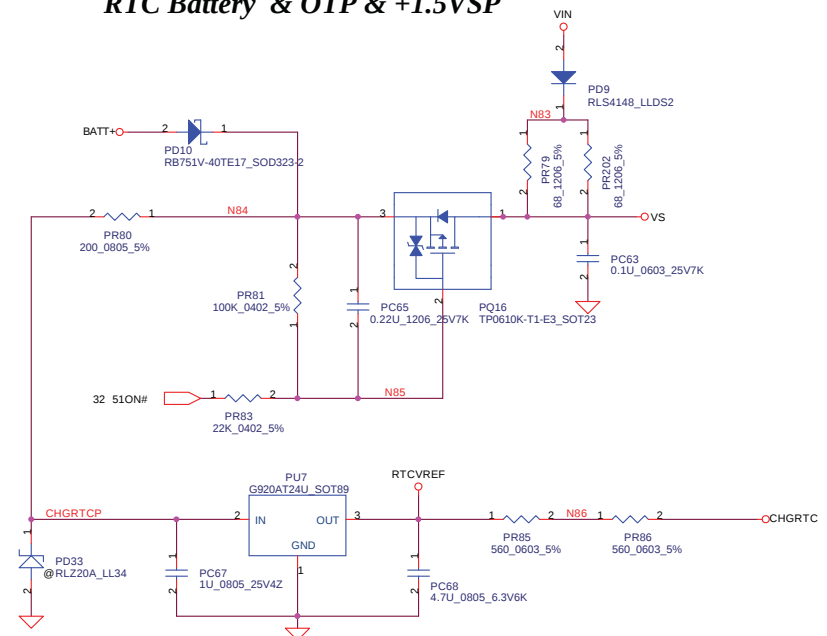
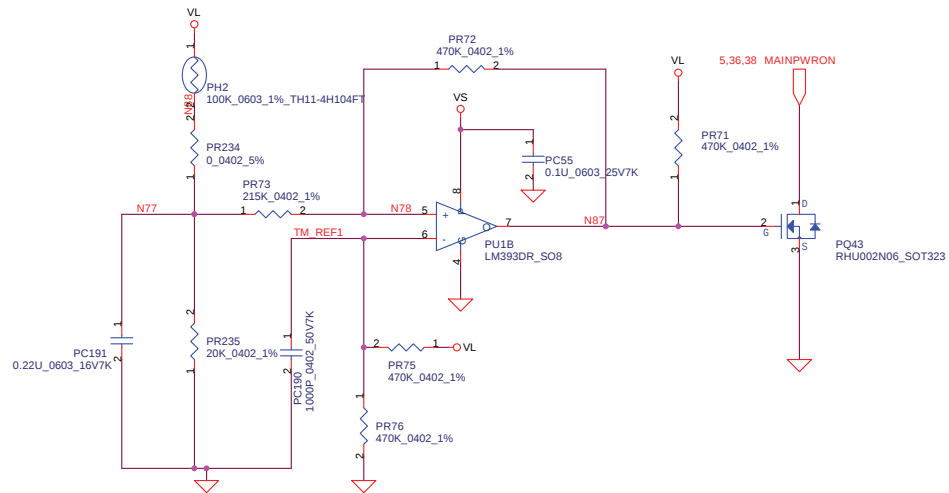
+0.9VSP / +2.5VSP



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				+0.9VSP / +2.5VP					
				Size		Document Number		Rev	
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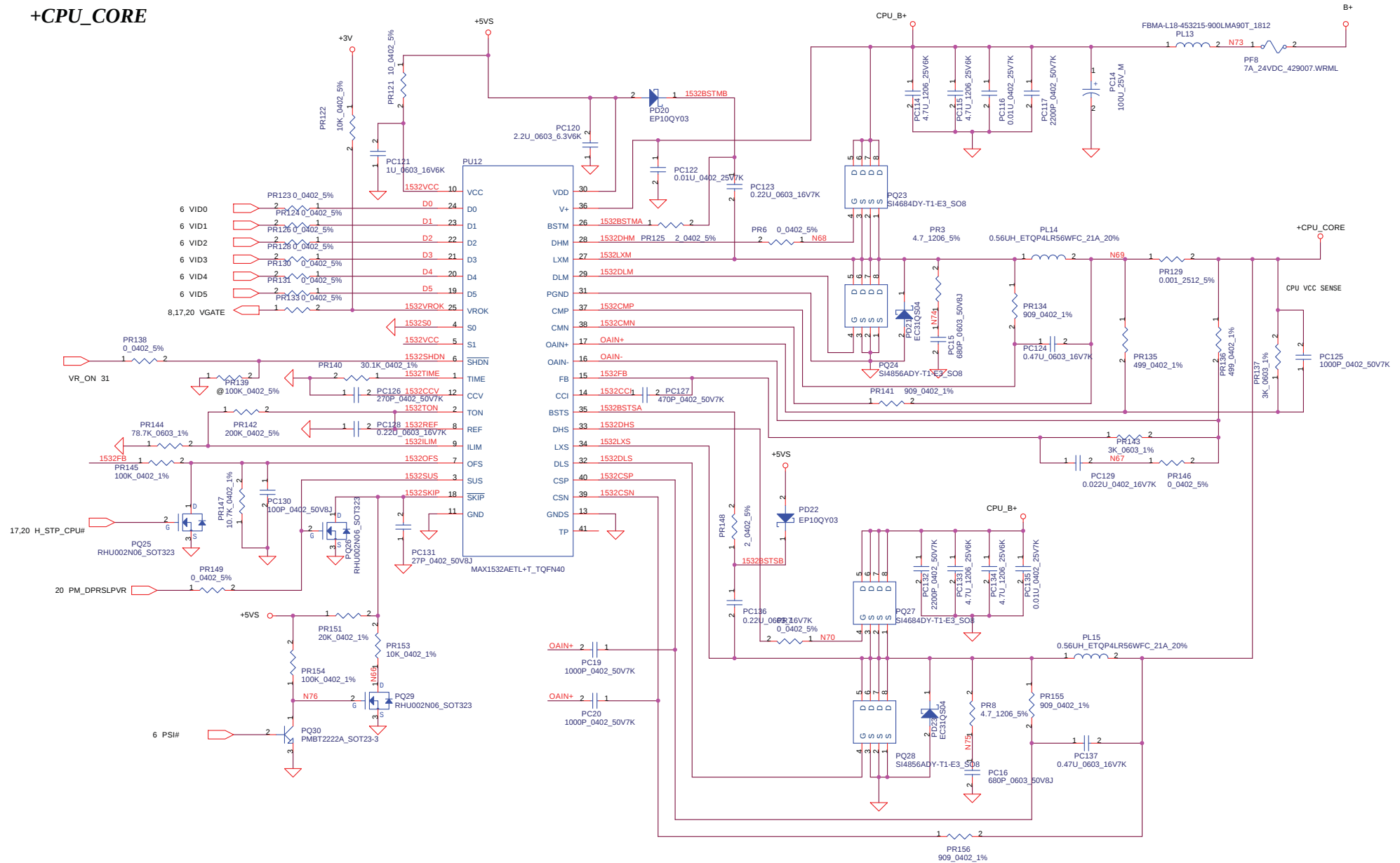
PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C

RTC Battery & OTP & +1.5VSP



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+CPU_CORE



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Version change list (P.I.R. List)

Item	Reason for change	Modify List	PG#	Rev.	Phase
1	Solve NB thermal issue	Add C855 S CER CAP 4.7U 6.3V K X5R 0805 Change C393 to S CER CAP 4.7U 6.3V K X5R 0805	11	0.2	EVT to DVT
2	Avoid +LCDVDD voltage transfer loss from +3.3V to +3.1V	Change Q26 to S TR SI4410DY-T1-A 1N S0-8	15		
3	Avoid can't turn on LCD	Change U1 to S IC NC7SZ08P5X_NL SC70 5P AND Add Q58 S TR BSS138LT1G 1N SOT23 W/D Add R859 S RES 1/16W 4.7K +-5% 0402	15		
4	Fix R G B rising time fail	Change L3,L4,L5 to S SUPPRE_ TAI-TECH FCM2012CF-800T06 0805	16		
5	Common Clock Generator Design	Change U31 to S IC ICS954226AGLFT TSSOP 56P CLK GEN	17		
6	Correct can't power on when adapter plug-in	Remove Q47 S TR 2N7002 1N SOT-23 only for BOM	20		
7	Avoid TP short when plug-in	Delete JTP1 pin2 net from +5VS	32		
8	Fine tune +3VS power sequence	Add R853,R854 S RES 1/16W 100K +-5% 0402 C848 S CER CAP .22U 16V K X7R 0603 Q55 S TR A03401L 1P SOT23	36		
9	Fine tune +1.8VS power sequence	Add R855,R856 S RES 1/16W 100K +-5% 0402 C849 S CER CAP 1U 16V K X5R 0603 TAIYO Q56 S TR A03401L 1P SOT23	36		
10	Add +1.8VS dis-charge circuit	Add R858 S RES 1/16W 470 +-5% 0402 Q57 S TR 2N7002 1N SOT-23	36		
11	Change MDC module from V1.0 to V1.5	Change JP3 from S H-CONN ACES 88021-30011 30P P0.8 to S H-CONN FOXCON QT8A0121-6011-8F 12P P.8	34		
12	Change NB L material to reduce Voltage lose	Change L11,L19,L20L23 from S SUPPRE_ CHENG-HANN MBK1608301YZF 0603 to S SUPPRE_ KC FBMA-L11-160808-700LMT 0603	11	0.3	DVT to PVT & SVT
13	Reduce USB over current signal nosie	Add C856,C858 S CER CAP 1U 10V K X5R 0603	20		
14	Fix ODD can't detect issue	Remove Q17,Q14 only fro BOM and delete D27,R813 Add R813 S RES 1/16W 0 +-5% 0402	22		
15	Eliminate LAN ISOLATE# voltage leakage	Add Q61 S TR A03413 1P SOT23-3 R43 S RES 1/16W 1K +-1% 0402 R46 S RES 1/16W 15K +-1% 0402	23		
16	Fix MS/SD can't detect issue	Remove R454,R468,R495,R463,R500,R505,R439 S RES 1/16W 43K +-5% 0402 fro SD Remove R432,R419,R402,R414,R431 S RES 1/16W 43K +-5% 0402 for MS Delete U30 pin9 link to +12V	25		
17	Fix SPK niose issue	Remove R639,R642,R640,R641,C569,C568,C570 Change R851 to L44 S SUPPRE_ KC FBMA-L11-160808-700LMT 0603 Change L18,L39 to S SUPPRE_ TAI-TECH FCM2012CF-800T06 0805 Change R285 to L44 S SUPPRE_ KC FBMA-L11-160808-700LMT 0603	28		
18	Fix SPK niose issue	Add C162,C161,C160,C159 S CER CAP 22P 25V K NPO 0402 Add L45,L46 S SUPPRE_ KC FBMA-L11-160808-700LMT 0603 Deletet C844 S CER CAP 220P 50V K X7R 0402 Change L29 to S RES 1/10W 0 +-5% 0603	29		
19	Fix MDC can't wake up on ring issue	Change JP3 pin6 link to +3V	33		
20	Delete USB Conn	Delete JUSBP4,D32,L38,C839	34		
21	Eliminate SYSON voltage surge issue	Add R866 S RES 1/16W 47K +-5% 0402	35		
22	Fix USB can't detect issue	Delete L40,L41,L42	34	1.0	SVT to MP v2.0
23	Avoid CRT voltage leakage to +5VS	Change R321 and R325 link to +CRT_VCC (original link to +5VS)	16		MP v2.0 to MP v3.0

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Version change list (P.I.R. List)

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Item	Reason for change	Modify List	PG#		B.Ver#	Phase
1	Adjust 0.9VSP power sequence	Add PR109 237K_0402_1% and PC192 0.1U_0402_16V delay 0.9VSP.	41	2005.10.23		
2	Adjust 1.5VSP power sequence	Add PR30 80.6K_0402_1% and PC193 0.1U_0402_16V delay 1.5VSP.	42	2005.10.23		
3	Improve 1.8VP、VCCP、1.5VSP transient response	Change PC50、PC48、PC177 from 150u 6.3v to 220u 4v	40 B42	2005.10.23		
4	To solve susp# leakage from +3valwp	Delete PD3	39	2005.12.01		
5	To avoid +VCC_PWRGD trun on beofre +VCCP turn on.	Add PQ44、PQ45 RHU002N06_SOT323, PR238 0_0402_5%, PR239 10K_0402_5%	39	2005.12.01		
6	Adjust 1.5v back to A-test status.	Delete PC193 at BOM.	41 B42	2005.12.01		
7						
8						
9						
10						
11						
12						
13						

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				LA-3091	Rev
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