Project Code:KEX00

MB Serial Number: LA-4651

BOM:46160336L01

PCB PN:DAA00000Y00

KEX00----LA-4651

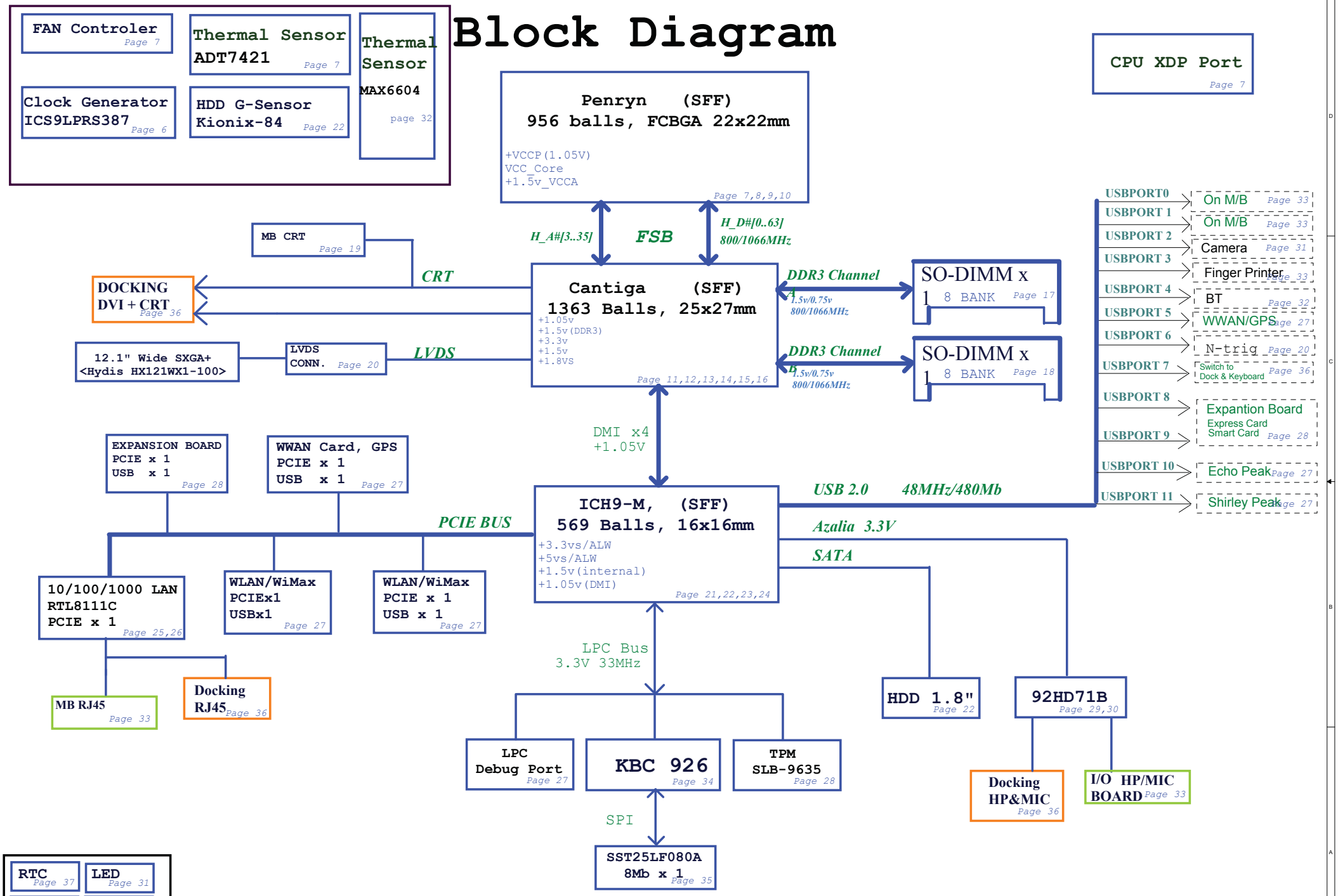
Montevina Platform,
SFF,DDR3Penryn + Cantiga +ICH9

2008-08-04

REV: X0.2

Title: Cover Sheet		
Size: Custom	Document Number: Bradstreet	Rev: 0.01
Date: Monday, August 04, 2008	Sheet 1 of 45	

Block Diagram



http://hobi-elektronika.net

Title	Block Diagram	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 2 of 45	

Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	B+	+5VALW +3VALW +3V_LAN [1]	+1.5V_MEM V_DDR_REF	+5VS +3VS +1.8VS +1.5VS +0.75VTT +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4 AC Pluged	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC+Battery removed	X	X	X	X

NOTE:
1. S3 state, if without AC ON, +3V_LAN will be switched off.

SMBUS Control Table

	SOURCE	CLK GEN	CPU THERMAL	SODIMM A & B	G-SENSOR	WLAN/WWAN EXPRESS CARD	ALS	THERMAL SENSOR ICH9,Cantiga SO-DIMM A&B	THERMAL SENSOR CHARGER	BATT-1	BATT-2	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	X	X	Y	X	Y	X	X	X	Y	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	Y	X	X	X	X	Y	Y	Y	X	X
ICH_SMB_CLK ICH_SMB_DATA	ICH9M	Y	X	Y	X	Y	X	X	X	X	X	X
EDID_CLK EDID_DATA	Cantiga	X	X	X	X	X	X	X	X	X	X	Y

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
CLK GEN	D2	1101 0010
CPU THERMAL	4C	0100 1100
SODIMM A	A0	1100 0000
SODIMM B	A4	1100 0100
G-SENSOR	30	0011 0000
ALS	72	0111 0010
THERMAL SENSOR (ICH9)	30	0011 0000
THERMAL SENSOR (Cantiga)	32	0011 0010
THERMAL SENSOR (So-Dimm A)	34	0011 0100
THERMAL SENSOR (LED LCD)	36	0011 0110
THERMAL SENSOR (Charger)	38	0011 1000
THERMAL SENSOR (Battery A)	TBD	TBD
THERMAL SENSOR (Battery B)	TBD	TBD
WLAN	TBD	TBD
WWAN	TBD	TBD
EXPRESS CARD	TBD	TBD

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

Debug@ : for LPC debug card, 80 port.

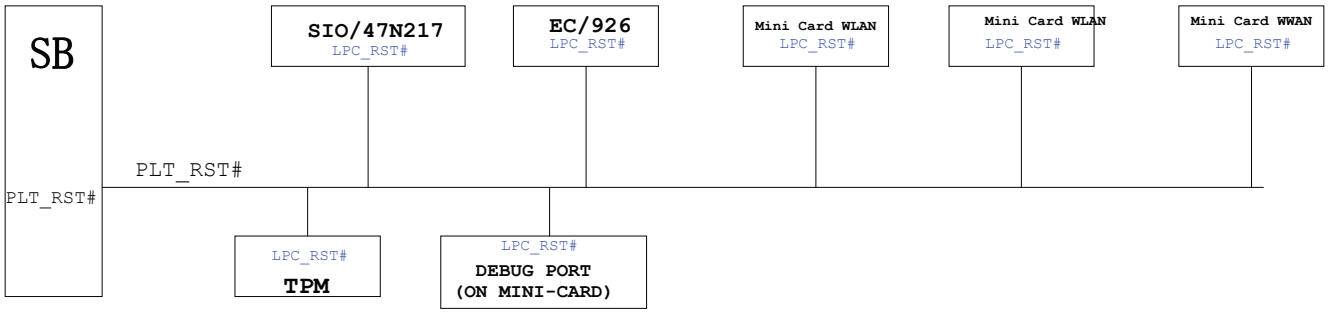
XDP@ : Reserve for CPU XTP debug.

MP@ : Should been staffed while in MP phase.

PCB 05P LA-4651P REV0 M/B

LPC BUS ADDRESSING/TOPOLOGY

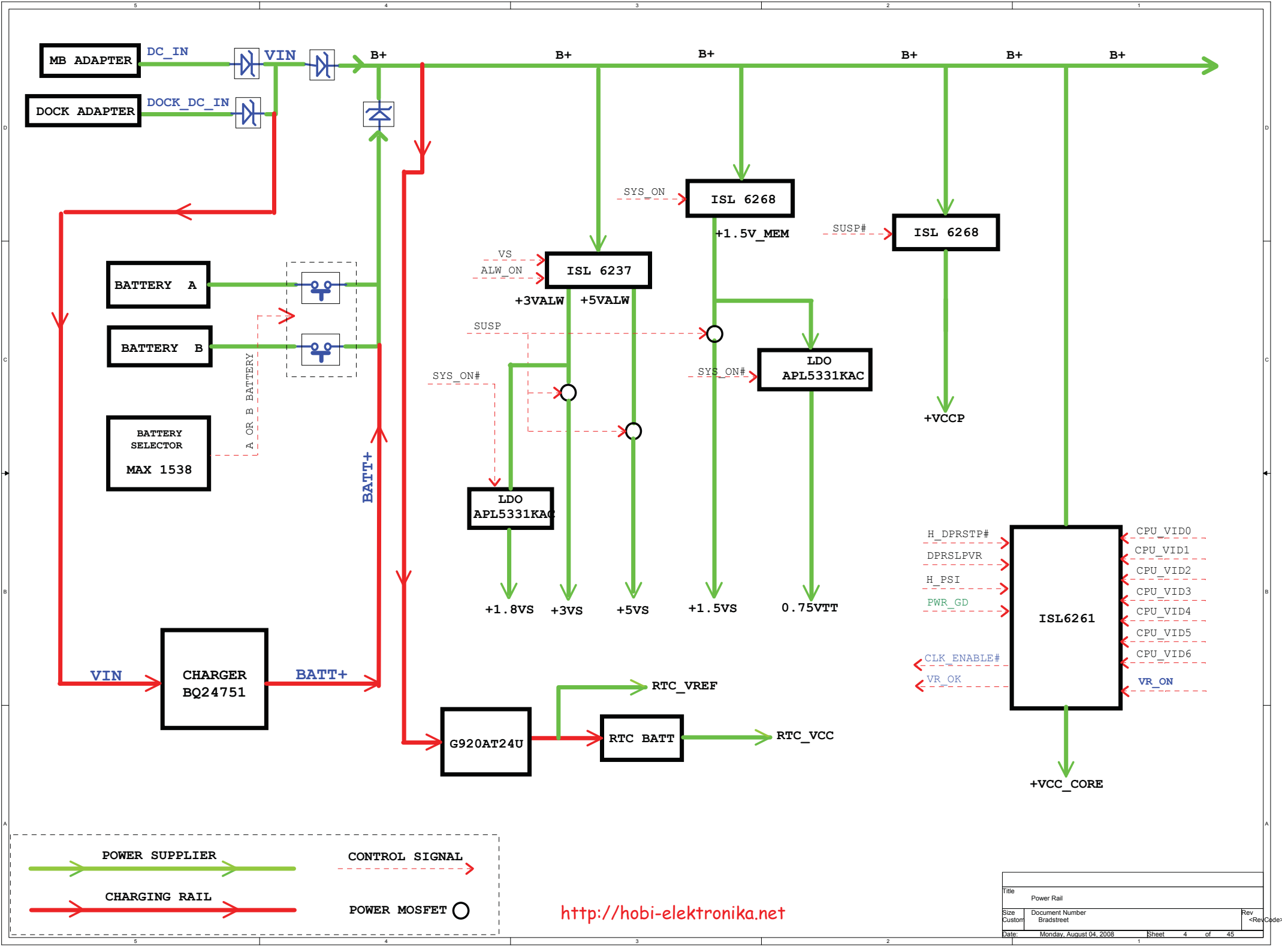
DEVICE	HEX	ADDRESS
SIO LPC47N217	2EH	0010 1110
TPM SLB9635TT1.2	4EH	0100 1110
Mini debug port	80	1000 0000

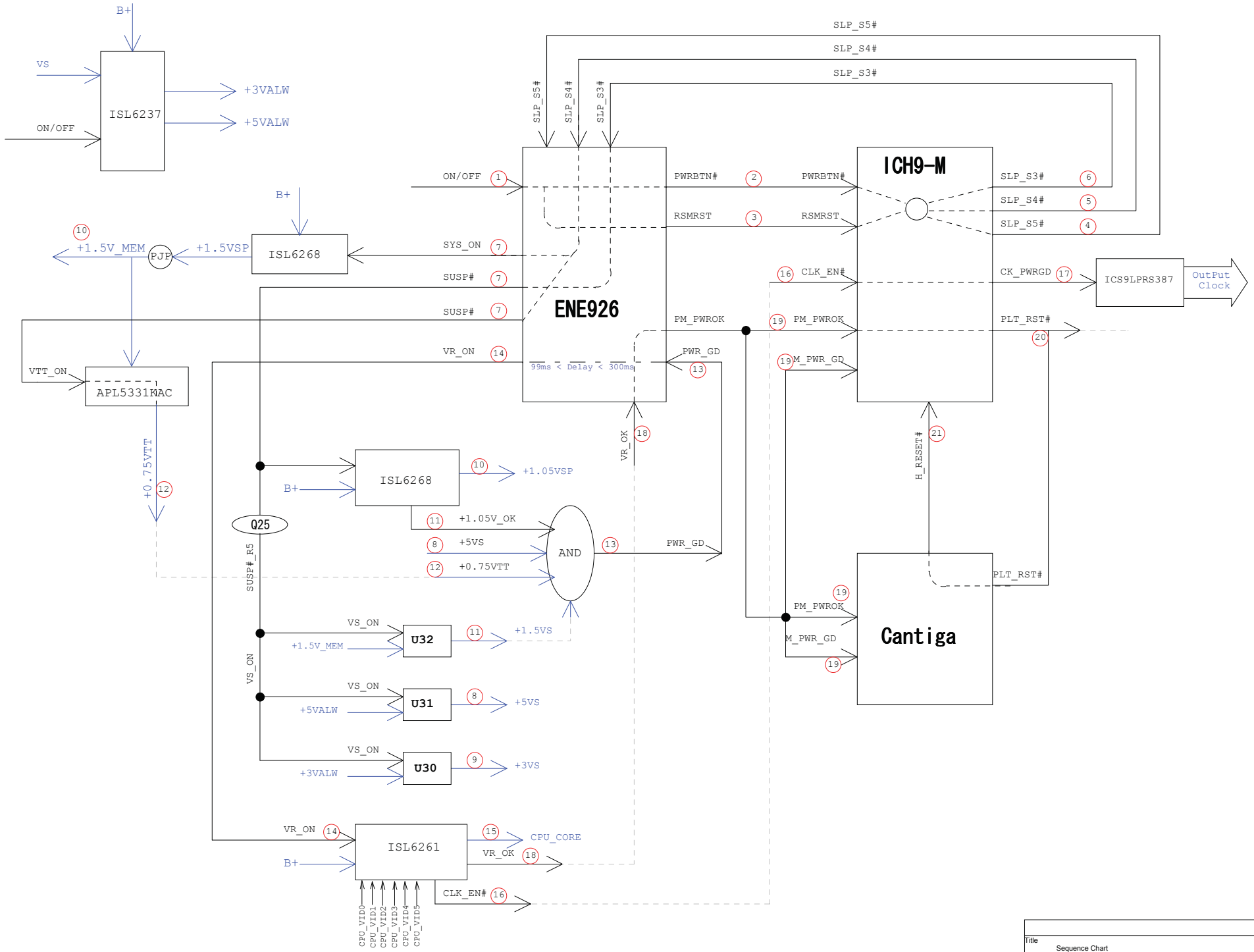


http://hobi-elektronika.net

ME Connector List Version:
Bradstreet connector list071210.xls

Title: Schematic Infomation			
Size: Custom	Document Number: Bradstreet		Rev: 0.01
Date: Monday, August 04, 2008	Sheet 3 of 45		


MB ADAPTER
DC_IN
VIN
DOCK ADAPTER
DOCK_DC_IN
B+
BATTERY A
BATTERY B
A OR B BATTERY
BATTERY SELECTOR
MAX 1538
BATT+
VIN
CHARGER
BQ24751
BATT+
SYS_ON
ISL 6268
+1.5V_MEM
SUSP#
ISL 6268
+VCCP
VS
ALW_ON
ISL 6237
+3VALW
+5VALW
SUSP
SYS_ON#
SYS_ON#
LDO
APL5331KAC
LDO
APL5331KAC
+1.8VS
+3VS
+5VS
+1.5VS
0.75VTT
G920AT24U
RTC_VREF
RTC BATT
RTC_VCC
H_DPRSTP#
DPRSLPVR
H_PSI
PWR_GD
CLK_ENABLE#
VR_OK
ISL6261
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPU_VID6
VR_ON
+VCC_CORE
POWER SUPPLIER
CHARGING RAIL
CONTROL SIGNAL
POWER MOSFET
http://hobi-elektronika.net
Title
Power Rail
Size
Custom
Document Number
Bradstreet
Rev
<RevCode>
Date:
Monday, August 04, 2008
Sheet
4
of
45



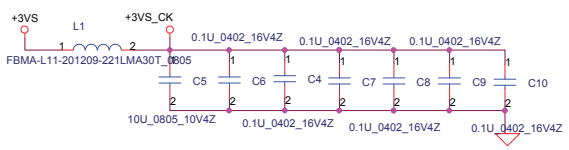
http://hobi-elektronika.net

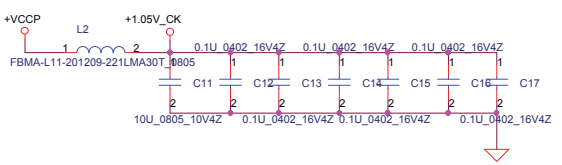
Title	Sequence Chart	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 5 of 45	

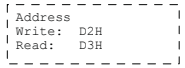
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	1	166	100	33.3
0	1	0	200	100	33.3
0	0	0	266	100	33.3

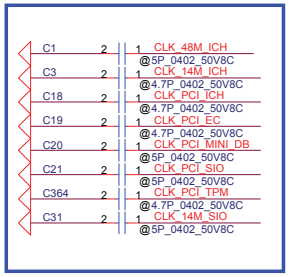
FSB Frequency Selet:

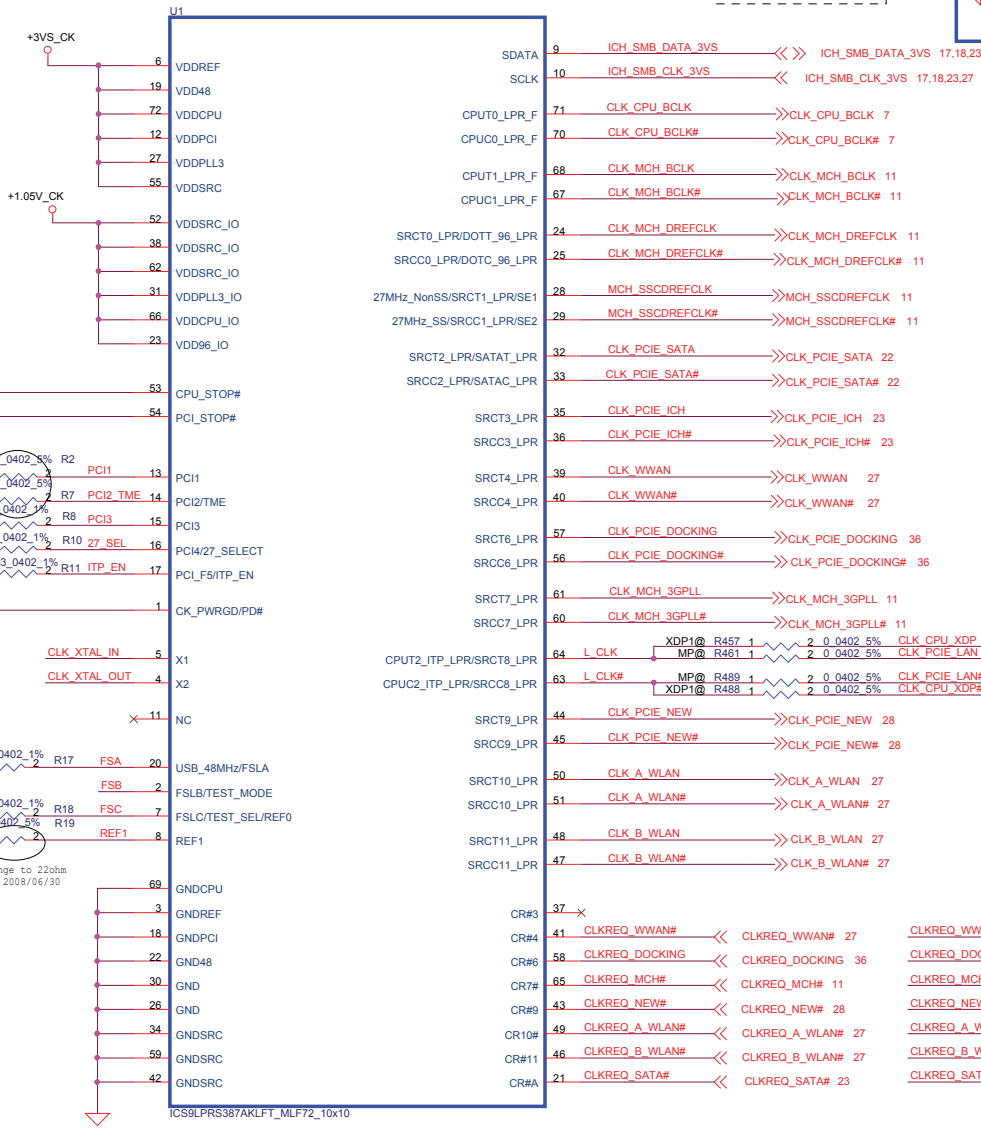
CPU Driven (Default) *	Stuff	R6	R14	R24			
	No Stuff	R1	R9	R12	R16	R20	R27
667MHz	Stuff	R1	R12	R27			
	No Stuff	R6	R14	R24	R9	R16	R20
800MHz	Stuff	R9	R12	R27			
	No Stuff	R6	R14	R24	R1	R16	R20
1066MHz	Stuff	R9	R16	R27			
	No Stuff	R6	R14	R24	R1	R12	R20

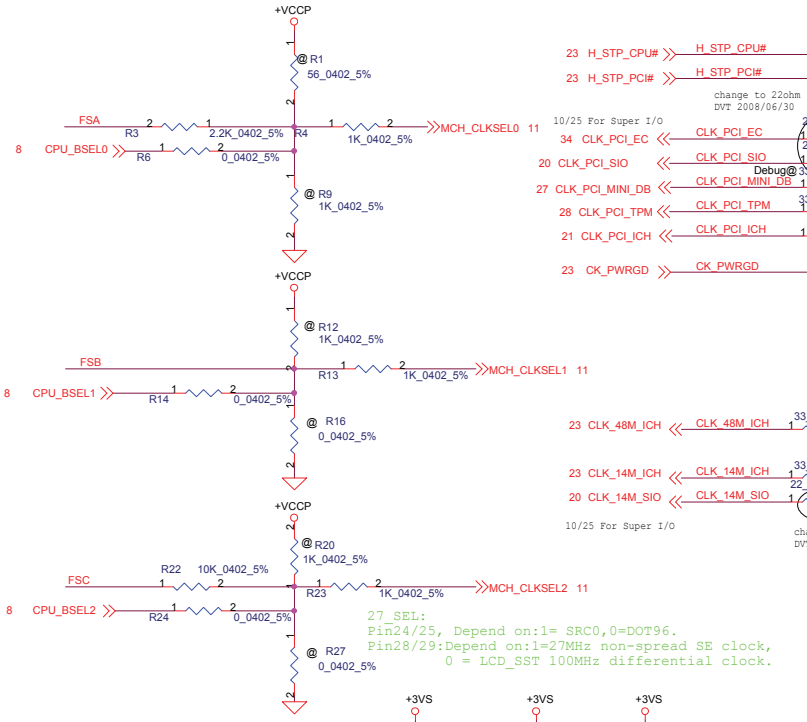




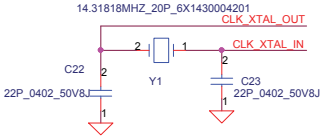


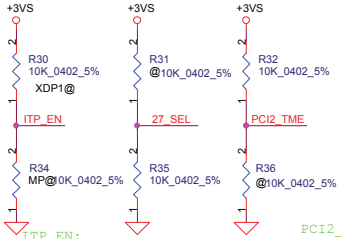






27_SEL:
Pin24/25, Depend on:1= SRC0,0=DOT96.
Pin28/29:Depend on:1=27MHz non-spread SE clock,
0 = LCD_SST 100MHz differential clock.

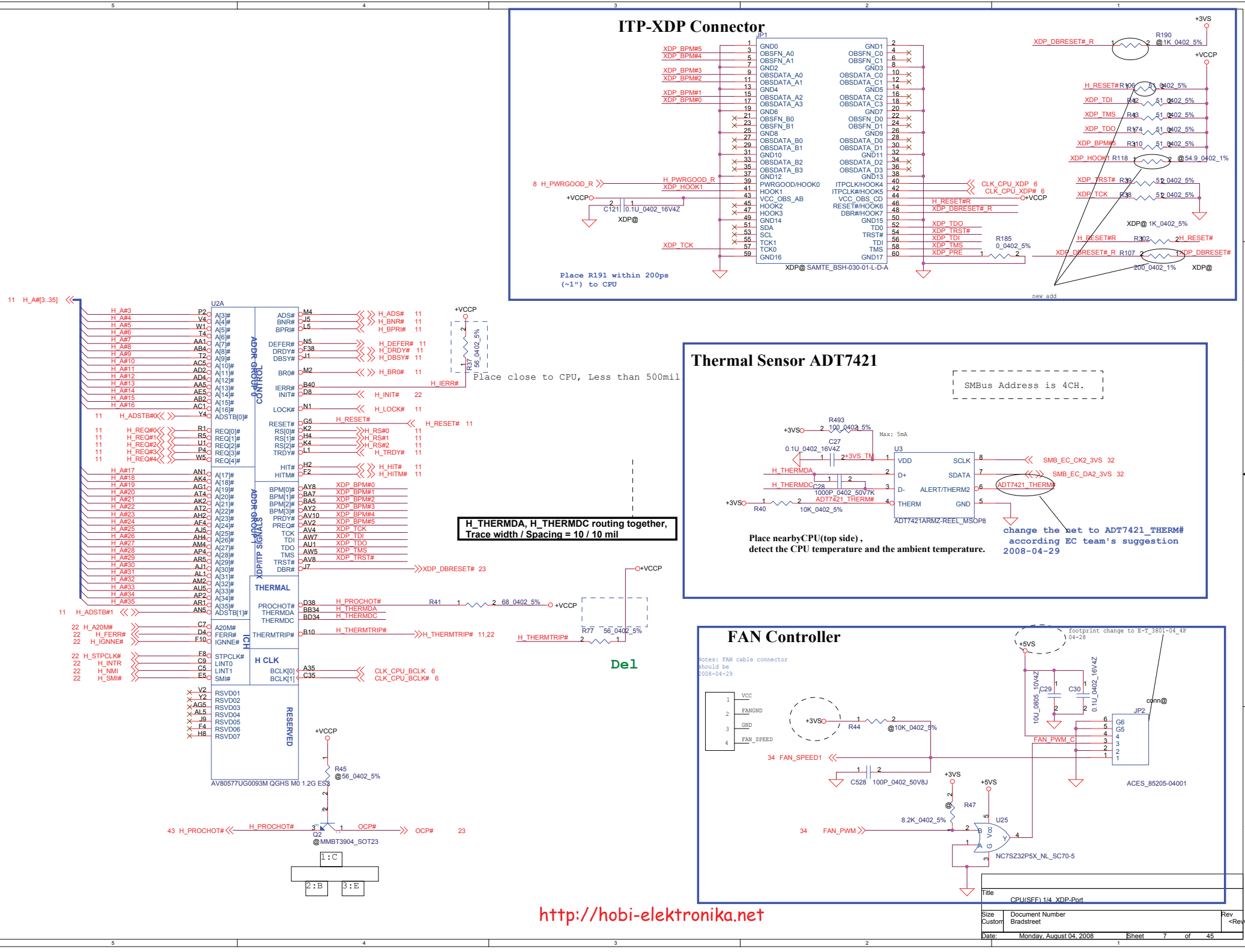


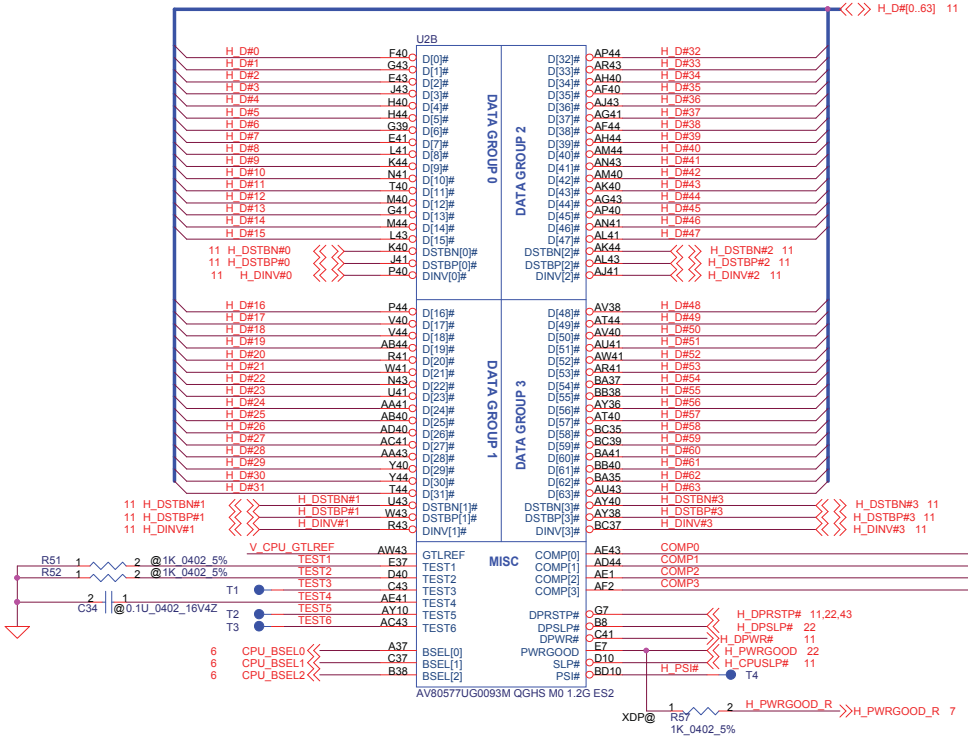


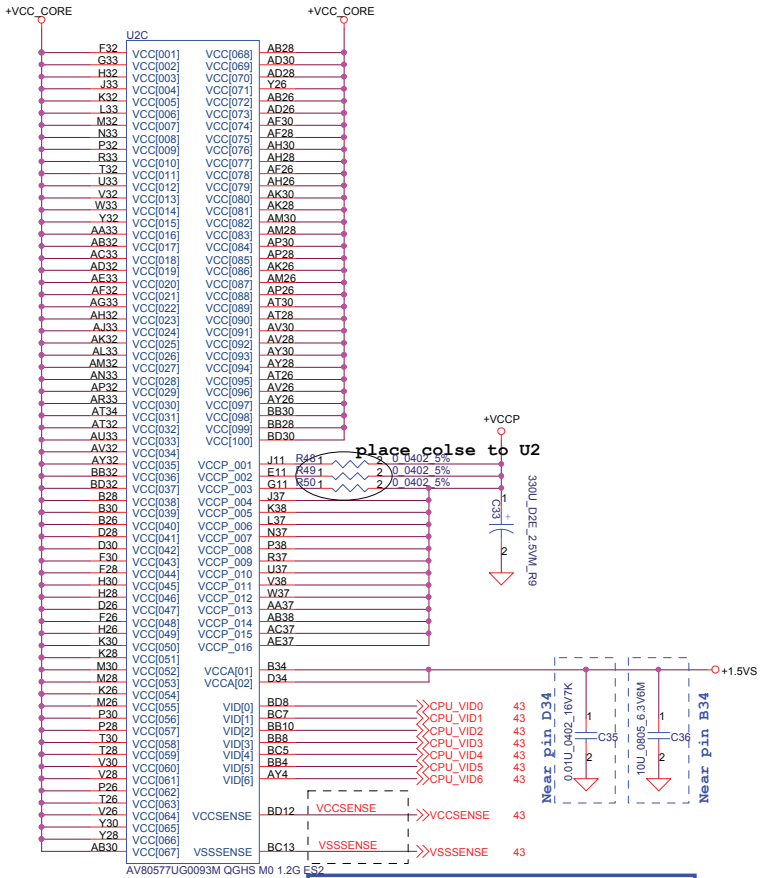
ITP_EN:
0 =SRC8/SRC8#
1 = ITP/ITP#

PCI2_TME:
0=Overclocking of CPU and SRC NOT allowed
1=Overclocking of CPU and SRC NOT allowed

Title	Clock Gen		
Size: Custom	Document Number: Bradstreet		Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 6	of 45	


ITP-XDP Connector
JP1
XDP_BPM#5
XDP_BPM#4
XDP_BPM#3
XDP_BPM#2
XDP_BPM#1
XDP_BPM#0
XDP_TCK
8 H_PWRGOOD_R
H_PWRGOOD_R
XDP_HOOK1
+VCCP
C121 0.1U_0402_16V4Z
XDP@
GND0 OBSFN_A0 OBSFN_A1 GND2 OBSDATA_A0 OBSDATA_A1 GND4 OBSDATA_A2 OBSDATA_A3 GND6 OBSFN_B0 OBSFN_B1 GND8 OBSDATA_B0 OBSDATA_B1 GND10 OBSDATA_B2 OBSDATA_B3 GND12 PWRGOOD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 GND14 SDA SCL TCK1 TCK0 GND16
GND1 OBSFN_C0 OBSFN_C1 GND3 OBSDATA_C0 OBSDATA_C1 GND5 OBSDATA_C2 OBSDATA_C3 GND7 OBSFN_D0 OBSFN_D1 GND9 OBSDATA_D0 OBSDATA_D1 GND11 OBSDATA_D2 OBSDATA_D3 GND13 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 GND15 TD0 TRST# TDI TMS GND17
XDP@ SAMTE_BSH-030-01-L-D-A
CLK_CPU_XDP 6
CLK_CPU_XDP# 6
+VCCP
H_RESET#R
XDP_DBRESET#_R
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_PRE
R185 0_0402_5%
Place R191 within 200ps (~1") to CPU
+3VS
XDP_DBRESET#_R
R190 @1K_0402_5%
+VCCP
H_RESET# R106 51_0402_5%
XDP_TDI R42 51_0402_5%
XDP_TMS R43 51_0402_5%
XDP_TDO R174 51_0402_5%
XDP_BPM#5 R310 51_0402_5%
XDP_HOOK1 R118 @54.9_0402_1%
XDP_TRST# R39 51_0402_5%
XDP_TCK R38 51_0402_5%
XDP@ 1K_0402_5%
H_RESET#R R302 H_RESET#
XDP_DBRESET#_R R107 XDP_DBRESET#
200_0402_1% XDP@
new add
11 H_A#[3..35]
U2A
H_A#3 H_A#4 H_A#5 H_A#6 H_A#7 H_A#8 H_A#9 H_A#10 H_A#11 H_A#12 H_A#13 H_A#14 H_A#15 H_A#16
11 H_ADSTB#0
11 H_REQ#0 H_REQ#1 H_REQ#2 H_REQ#3 H_REQ#4
H_A#17 H_A#18 H_A#19 H_A#20 H_A#21 H_A#22 H_A#23 H_A#24 H_A#25 H_A#26 H_A#27 H_A#28 H_A#29 H_A#30 H_A#31 H_A#32 H_A#33 H_A#34 H_A#35
11 H_ADSTB#1
22 H_A20M#
22 H_FERR#
22 H_IGNNE#
22 H_STPCLK#
22 H_INTR
22 H_NMI
22 H_SMI#
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
ICH
RESERVED
ADS# BNR# BPRI# DEFER# DRDY# DBSY# BR0# IERR# INIT# LOCK# RESET# RS[0]# RS[1]# RS[2]# TRDY# HIT# HITM# BPM[0]# BPM[1]# BPM[2]# BPM[3]# PRDY# PREQ# TCK TDI TDO TMS TRST# DBR#
H_ADS# 11
H_BNR# 11
H_BPRI# 11
H_DEFER# 11
H_DRDY# 11
H_DBSY# 11
H_BR0# 11
H_IERR#
H_INIT# 22
H_LOCK# 11
H_RESET#
H_RESET# 11
H_RS#0 11
H_RS#1 11
H_RS#2 11
H_TRDY# 11
H_HIT# 11
H_HITM# 11
XDP_BPM#0 XDP_BPM#1 XDP_BPM#2 XDP_BPM#3 XDP_BPM#4 XDP_TCK XDP_TDI XDP_TDO XDP_TMS XDP_TRST#
XDP_DBRESET# 23
PROCHOT# THERMDA THERMDC THERMTRIP#
H_PROCHOT# H_THERMDA H_THERMDC H_THERMTRIP#
H_THERMTRIP# 11,22
R41 1 2 68_0402_5%
+VCCP
R77 56_0402_5%
H_THERMTRIP#
Del
BCLK[0] BCLK[1]
CLK_CPU_BCLK 6
CLK_CPU_BCLK# 6
RSVD01 RSVD02 RSVD03 RSVD04 RSVD05 RSVD06 RSVD07
AV80577UG0093M QGHS M0 1.2G ES2
+VCCP
R45 @56_0402_5%
43 H_PROCHOT#
H_PROCHOT#
Q2 @MMBT3904_SOT23
OCP#
OCP# 23
1:C 2:B 3:E
+VCCP
R56 56_0402_5%
Place close to CPU, Less than 500mil
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil
Thermal Sensor ADT7421
SMBus Address is 4CH.
+3VS
R493 100_0402_5%
Max: 5mA
C27 0.1U_0402_16V4Z
+3VS_TM
H_THERMDA
H_THERMDC
C28 1000P_0402_50V7K
ADT7421_THERM#
R40 10K_0402_5%
U3
VDD D+ D- THERM SCLK SDATA ALERT/THERM2 GND
ADT7421ARMZ-REEL_MSOP8
SMB_EC_CK2_3VS 32
SMB_EC_DA2_3VS 32
ADT7421_THERM#
Place nearbyCPU(top side) , detect the CPU temperature and the ambient temperature.
change the net to ADT7421_THERM# according EC team's suggestion 2008-04-29
FAN Controller
Notes: FAN cable connector should be 2008-04-29
footprint change to E-T_3801-04_4P 04-28
VCC FANGND GND FAN_SPEED
+3VS
R44 @10K_0402_5%
34 FAN_SPEED1
C528 100P_0402_50V8J
+5VS
R47 8.2K_0402_5%
34 FAN_PWM
U25
NC7SZ32P5X_NL_SC70-5
+5VS
10U_0805_10V4Z
C29
C30 0.1U_0402_16V4Z
FAN_PWM_C
JP2
conn@
ACES_85205-04001
Title
CPU(SFF) 1/4 XDP-Port
Size Custom
Document Number Bradstreet
Rev <RevCode>
Date: Monday, August 04, 2008
Sheet 7 of 45
http://hobi-elektronika.net



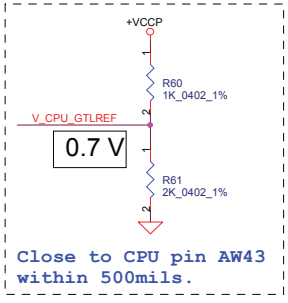


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

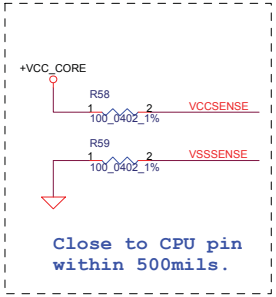
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 3.5 mils.

Length match within 25 mils.
Z0=27.4 ohm
2008-04-07



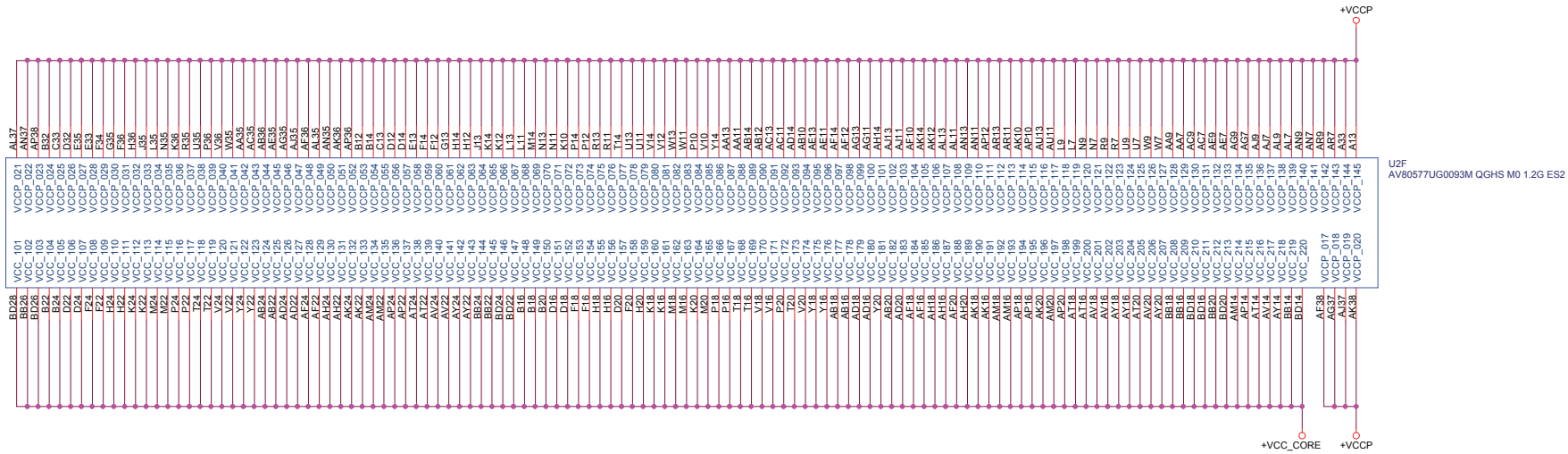
Close to CPU pin AW43 within 500mils.



Close to CPU pin within 500mils.

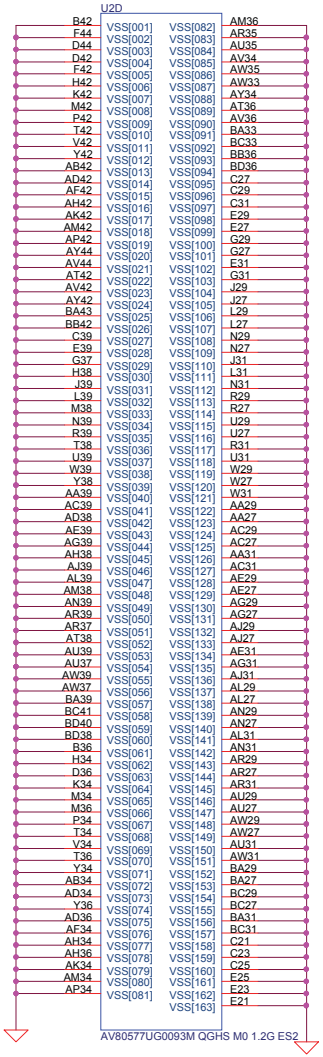
http://hobi-elektronika.net

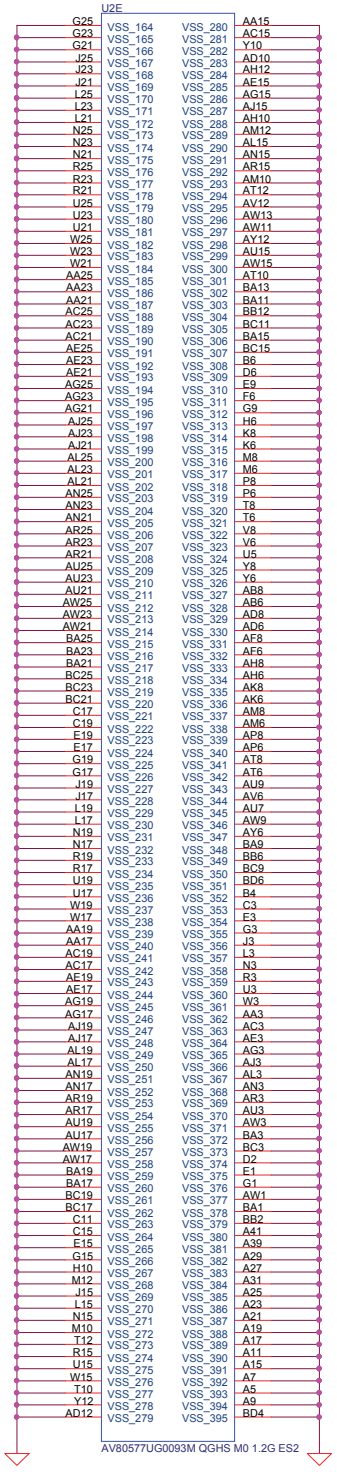
Title	CPU(SFF) 2/4	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 8 of 45	

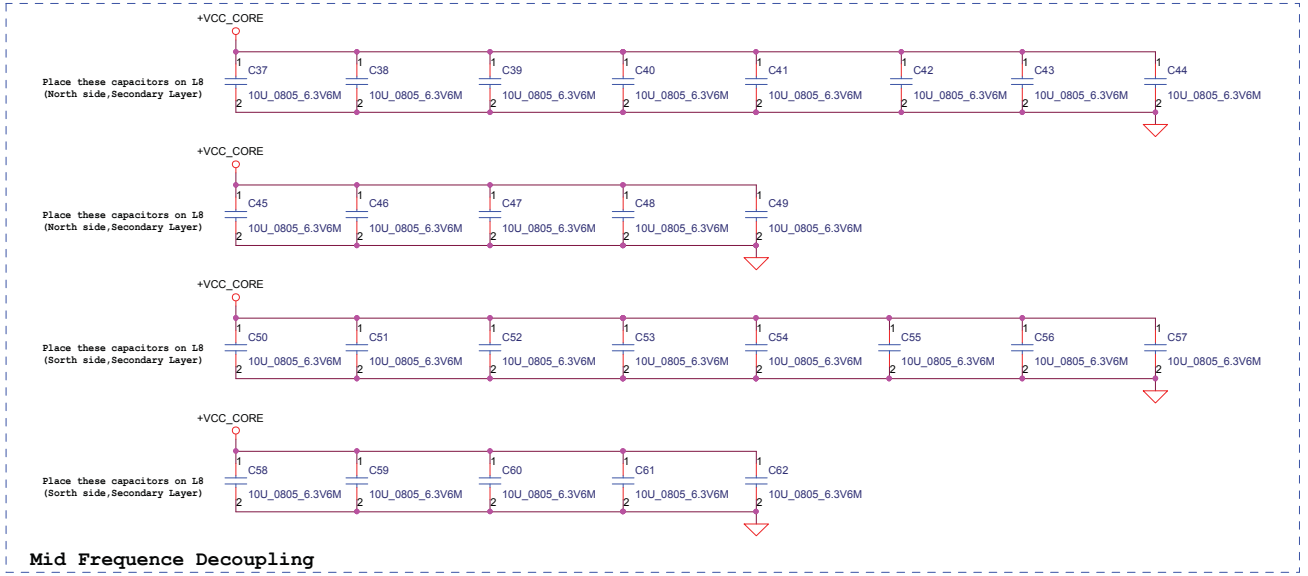


http://hobi-elektronika.net

Title	CPU(SFF) 3/4		
Size	Document Number		Rev
Custom	Bradstreet		<RevCode>
Date:	Monday, August 04, 2008	Sheet 9 of 45	

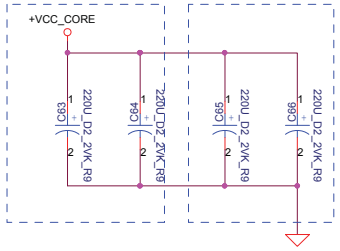


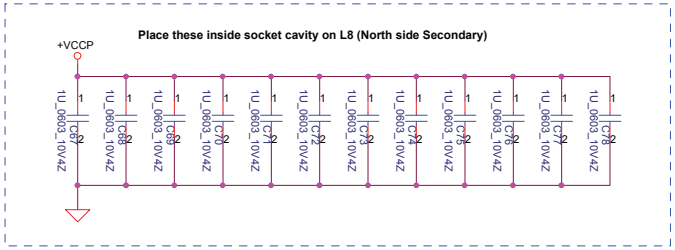




Near CPU CORE regulator

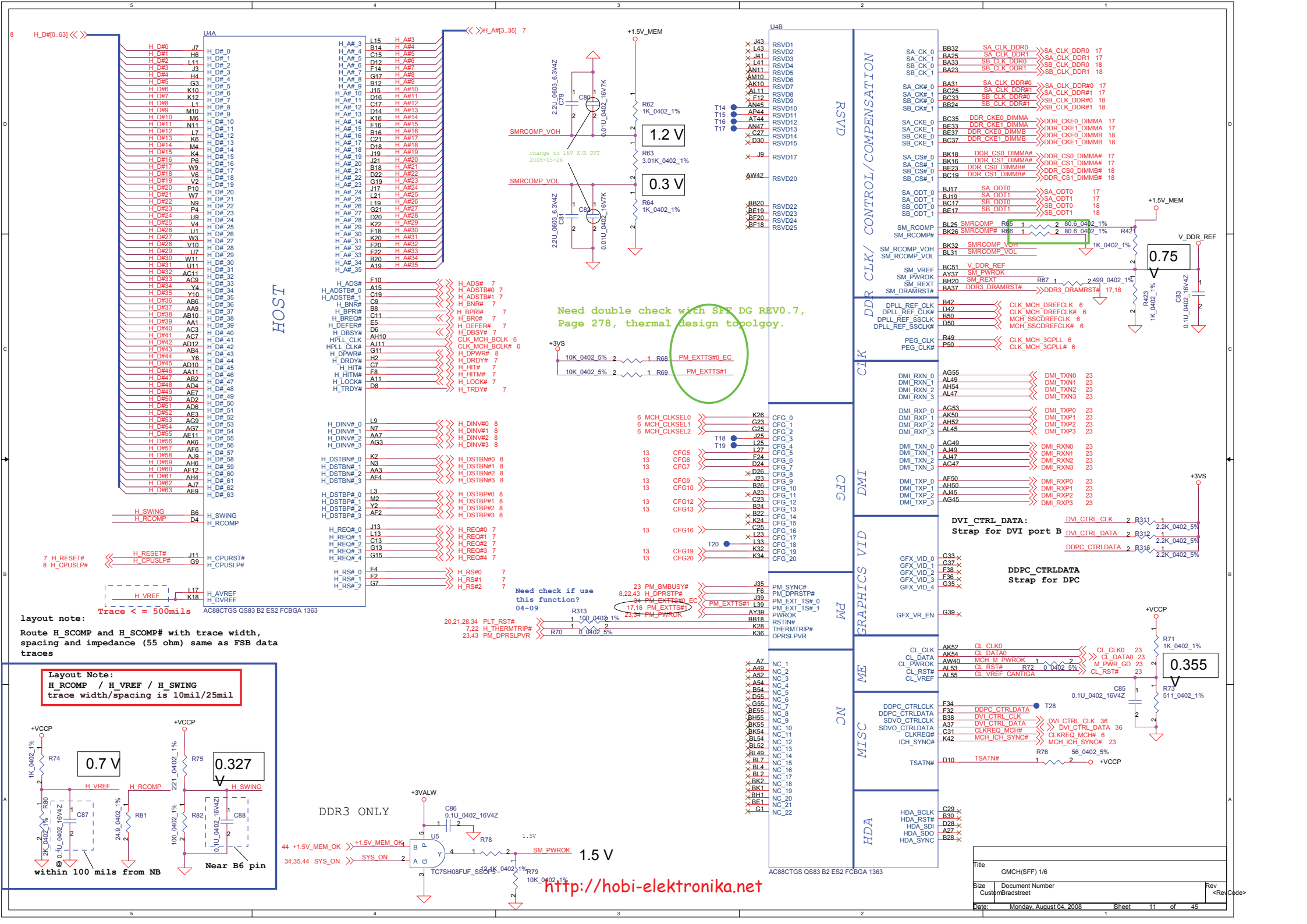
ESR <= 1.5m ohm

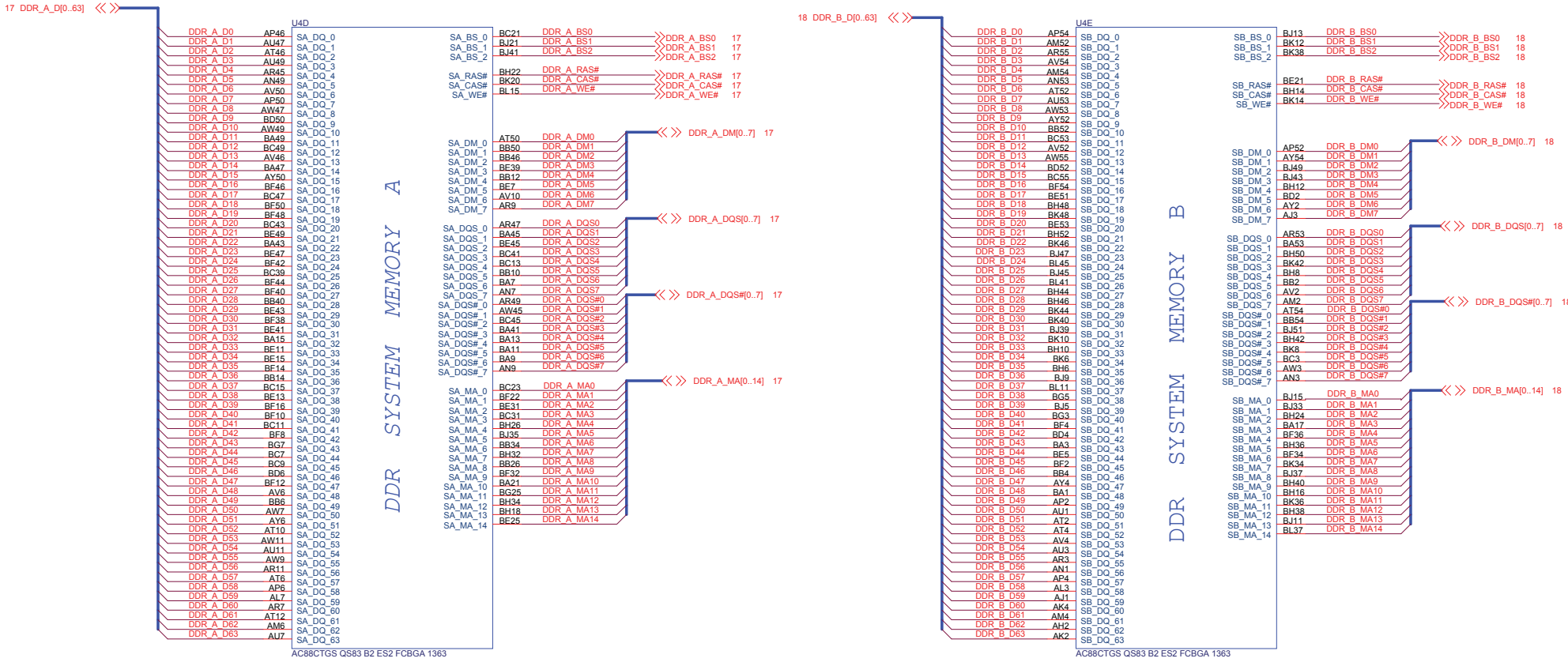




http://hobi-elektronika.net

Title	CPU(SFF) 4/4		
Size	Document Number		Rev
Custom	Bradstreet		<RevCode>
Date:	Monday, August 04, 2008	Sheet 10 of 45	


U4A
HOST
AC88CTGS QS83 B2 ES2 FCBGA 1363
U4B
RSVD
CLK/ CONTROL/COMPENSATION
DDR
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA
1.2 V
0.3 V
0.75 V
0.355 V
0.7 V
0.327 V
1.5 V
Need double check with SFF DG REV0.7, Page 278, thermal design topolgoy.
Need check if use this function? 04-09
DVI_CTRL_DATA: Strap for DVI port B
DDPC_CTRLDATA Strap for DPC
DDR3 ONLY
Trace < = 500mils
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
Layout Note: H_RCOMP / H_VREF / H_SWING trace width/spacing is 10mil/25mil
within 100 mils from NB
Near B6 pin
http://hobi-elektronika.net
Title GMCH(SFF) 1/6
Size Custom
Document Number Bradstreet
Rev <RevCode>
Date: Monday, August 04, 2008
Sheet 11 of 45



Title	GMCH(SFF) 2/6	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 12 of 45	

LCD require the
PWM frequency typical 280Hz,(200 to 350Hz),
Need confirm with Intel what's the frequency
of this signal output.
(8/21)

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

Ice update 11-01

Ref to SFF DG P196

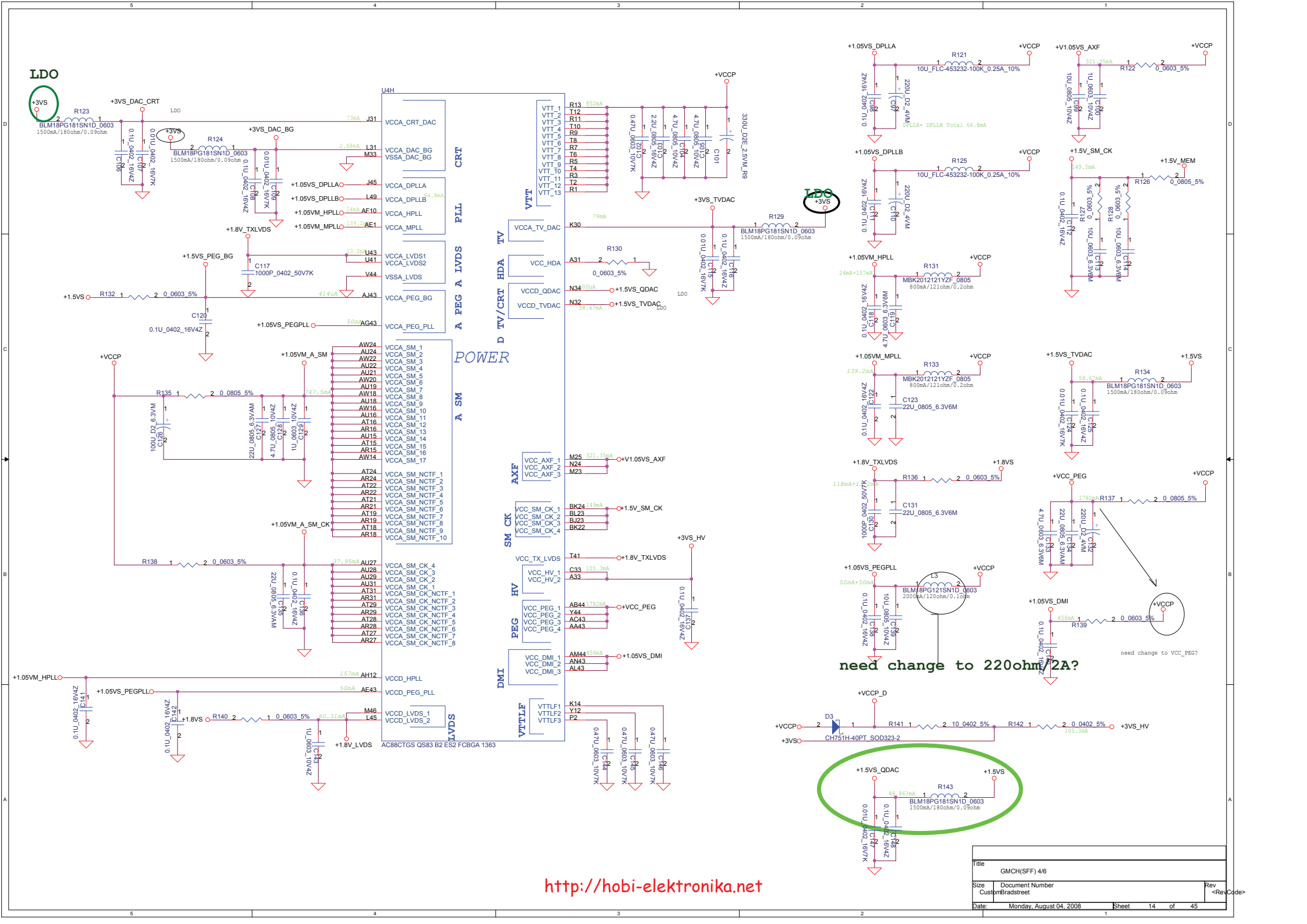
Close to pin D32 and keep 30mil space to other part/trace.

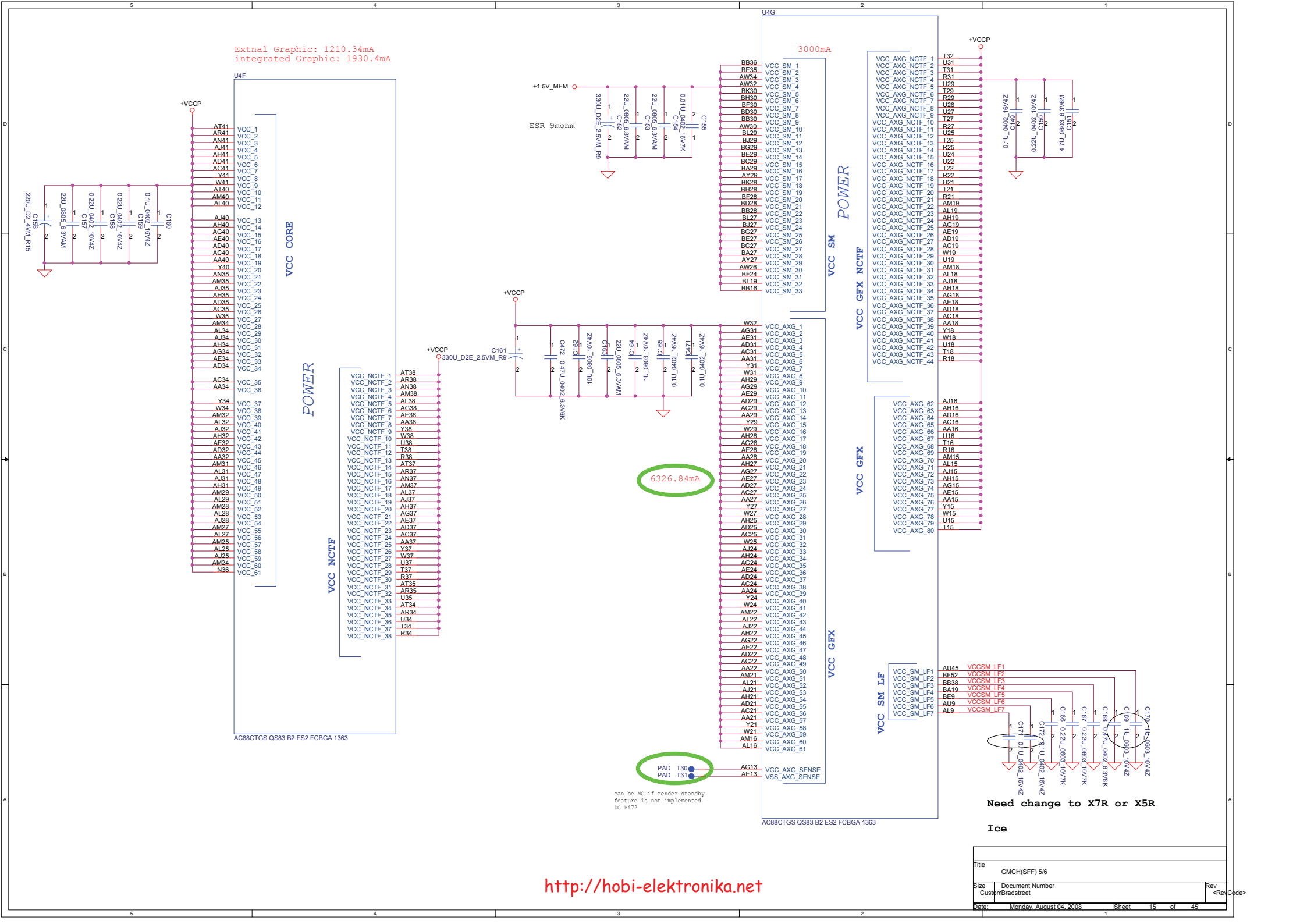
Change from SD00000328L

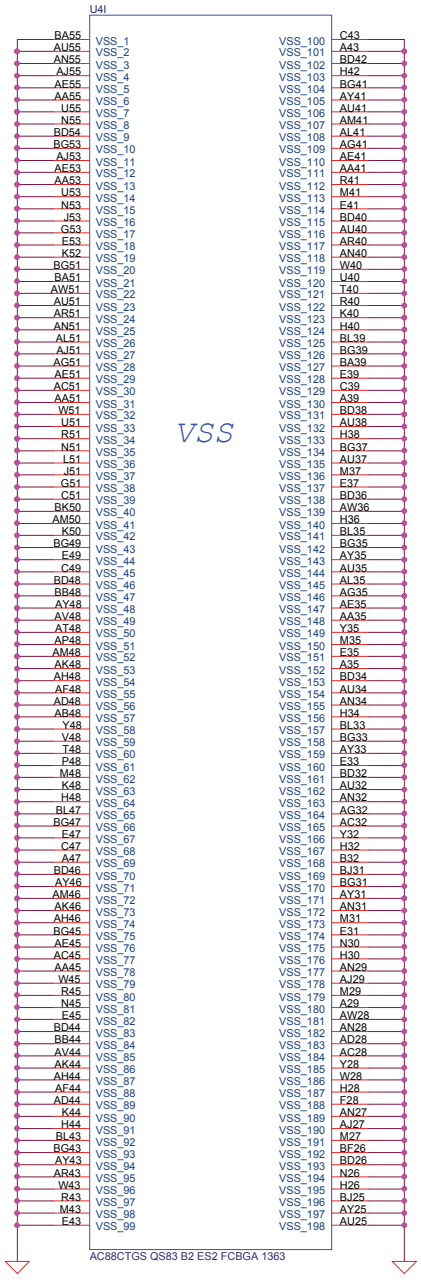
Place near Cantiga Pin.J29,G29,F30

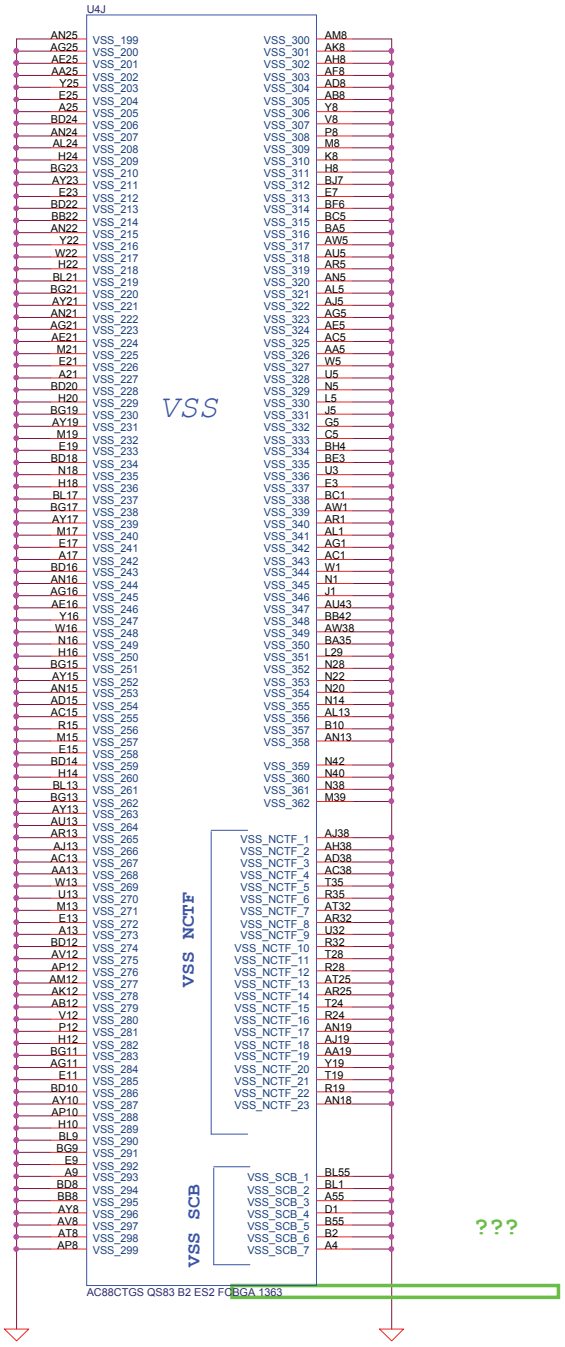
2008-04-09

Title	GMCH(SFF) 3/6
Size: Custom	Document Number: Bradstreet
Rev	<RevCode>
Date:	Monday, August 04, 2008
Sheet	13 of 45


LDO
+3VS
+3VS_DAC_CRT
+3VS_DAC_BG
R123
R124
BLM18PG181SN1D_0603
1500mA/180ohm/0.09ohm
U4H
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
CRT
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
PLL
+1.8V_TXLVDS
+1.5VS_PEG_BG
C117
1000P_0402_50V7K
R132
0_0603_5%
C120
0.1U_0402_16V4Z
VCCA_LVDS1
VCCA_LVDS2
VSSA_LVDS
VCCA_PEG_BG
VCCA_PEG_PLL
A PEG A LVDS
+1.05VS_PEGPLL
+VCCP
+1.05VM_A_SM
R135
0_0805_5%
100U_D2_6.3VM
22U_0805_6.3VAM
4.7U_0805_10V4Z
1U_0603_10V4Z
C126
C127
C128
C129
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCCA_SM_6
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
VCCA_SM_10
VCCA_SM_11
VCCA_SM_12
VCCA_SM_13
VCCA_SM_14
VCCA_SM_15
VCCA_SM_16
VCCA_SM_17
VCCA_SM_NCTF_1
VCCA_SM_NCTF_2
VCCA_SM_NCTF_3
VCCA_SM_NCTF_4
VCCA_SM_NCTF_5
VCCA_SM_NCTF_6
VCCA_SM_NCTF_7
VCCA_SM_NCTF_8
VCCA_SM_NCTF_9
VCCA_SM_NCTF_10
A SM
POWER
+1.05VM_A_SM_CK
R138
0_0603_5%
22U_0805_6.3VAM
0.1U_0402_16V4Z
C135
C136
VCCA_SM_CK_4
VCCA_SM_CK_3
VCCA_SM_CK_2
VCCA_SM_CK_1
VCCA_SM_CK_NCTF_1
VCCA_SM_CK_NCTF_2
VCCA_SM_CK_NCTF_3
VCCA_SM_CK_NCTF_4
VCCA_SM_CK_NCTF_5
VCCA_SM_CK_NCTF_6
VCCA_SM_CK_NCTF_7
VCCA_SM_CK_NCTF_8
+1.05VM_HPLL
+1.05VS_PEGPLL
+1.8VS
R140
0_0603_5%
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS_1
VCCD_LVDS_2
LVDS
+1.8V_LVDS
AC88CTGS QS83 B2 ES2 FCBGA 1363
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT
330U_D2E_2.5VM_R9
VCCA_TV_DAC
VCC_HDA
VCCD_QDAC
VCCD_TVDAC
TV
HDA
TV/CRT
D
+3VS_TVDAC
R129
BLM18PG181SN1D_0603
1500mA/180ohm/0.09ohm
R130
0_0603_5%
+1.5VS_QDAC
+1.5VS_TVDAC
LDO
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
AXF
+V1.05VS_AXF
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
SM CK
+1.5V_SM_CK
VCC_TX_LVDS
+1.8V_TXLVDS
+3VS_HV
VCC_HV_1
VCC_HV_2
HV
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
PEG
+VCC_PEG
VCC_DMI_1
VCC_DMI_2
VCC_DMI_3
DMI
+1.05VS_DMI
VTTLF1
VTTLF2
VTTLF3
VTTLF
+1.05VS_DPLLA
R121
10U_FLC-453232-100K_0.25A_10%
220U_D2_4VM
DPLLA+ DPLLB Total 64.8mA
+1.05VS_DPLLB
R125
10U_FLC-453232-100K_0.25A_10%
+1.5V_SM_CK
+1.5V_MEM
R126
0_0805_5%
R127
0_0603_5%
R128
0_0603_5%
+1.05VM_HPLL
R131
MBK2012121YZF_0805
800mA/121ohm/0.2ohm
+1.05VM_MPLL
R133
MBK2012121YZF_0805
800mA/121ohm/0.2ohm
C123
22U_0805_6.3V6M
+1.5VS_TVDAC
R134
BLM18PG181SN1D_0603
1500mA/180ohm/0.09ohm
+1.8V_TXLVDS
+1.8VS
R136
0_0603_5%
C131
22U_0805_6.3V6M
+VCC_PEG
R137
0_0805_5%
+1.05VS_PEGPLL
L3
BLM18PG121SN1D_0603
2000mA/120ohm/0.15ohm
+1.05VS_DMI
R139
0_0603_5%
need change to VCC_PEG?
need change to 220ohm 2A?
+VCCP_D
D3
CH751H-40PT_SOD323-2
R141
10_0402_5%
R142
0_0402_5%
+1.5VS_QDAC
+1.5VS
R143
BLM18PG181SN1D_0603
1500mA/180ohm/0.09ohm
http://hobi-elektronika.net
Title
GMCH(SFF) 4/6
Size
Custom
Document Number
Bradstreet
Rev
<RevCode>
Date:
Monday, August 04, 2008
Sheet
14
of
45

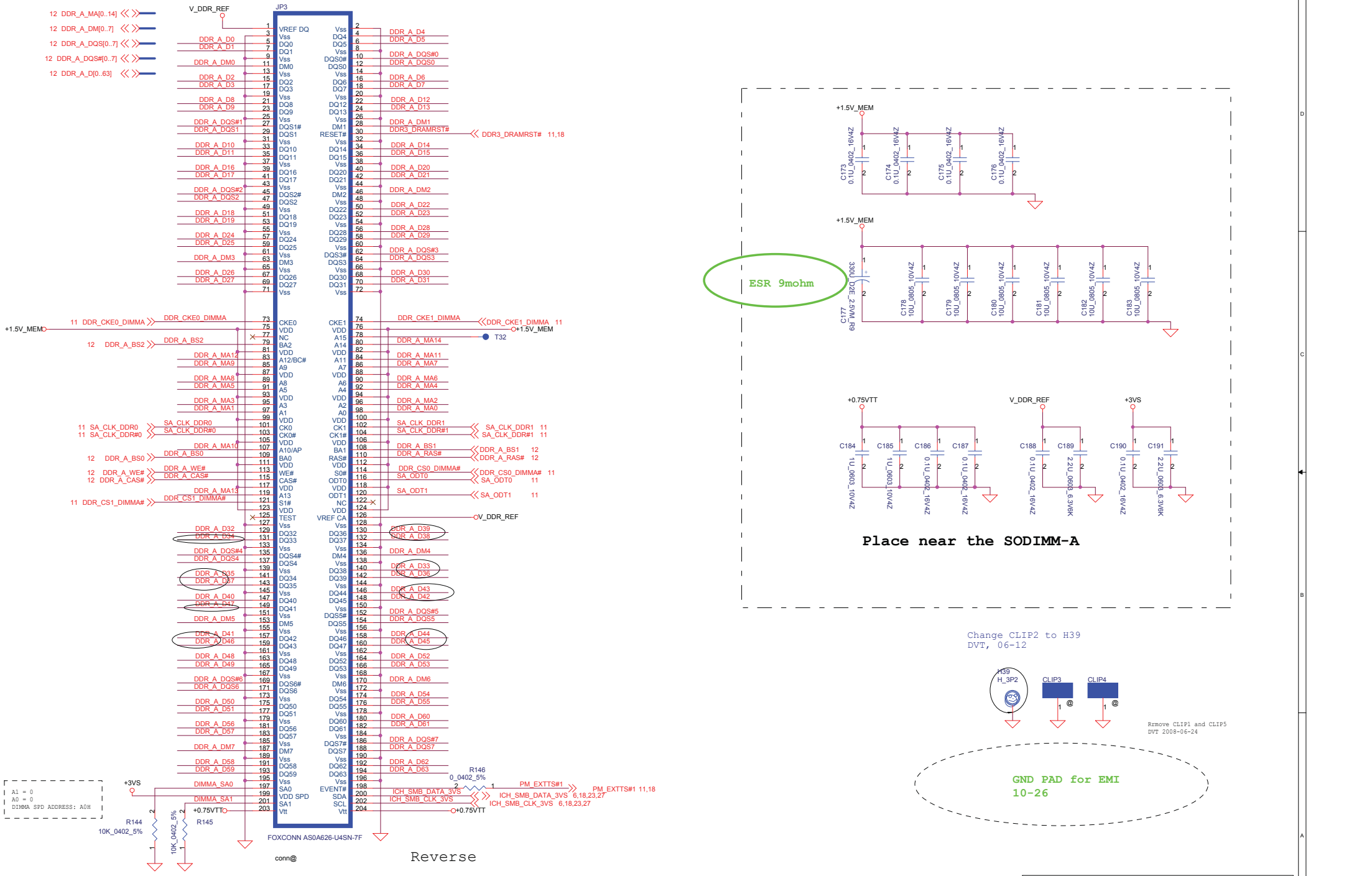

Extnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA
U4F
+VCCP
VCC CORE
POWER
VCC NCTF
AC88CTGS QS83 B2 ES2 FCBGA 1363
+1.5V_MEM
ESR 9mohm
330U_D2E_2.5VM_R9
22U_0805_6.3VAM
22U_0805_6.3VAM
0.01U_0402_16V7K
U4G
3000mA
VCC SM
POWER
VCC GFX NCTF
VCC GFX
VCC SM LF
6326.84mA
PAD T30
PAD T31
can be NC if render standby feature is not implemented
DG P472
AC88CTGS QS83 B2 ES2 FCBGA 1363
Need change to X7R or X5R
Ice
http://hobi-elektronika.net
Title
GMCH(SFF) 5/6
Size
Custom
Document Number
Bradstreet
Rev
<RevCode>
Date:
Monday, August 04, 2008
Sheet
15
of
45

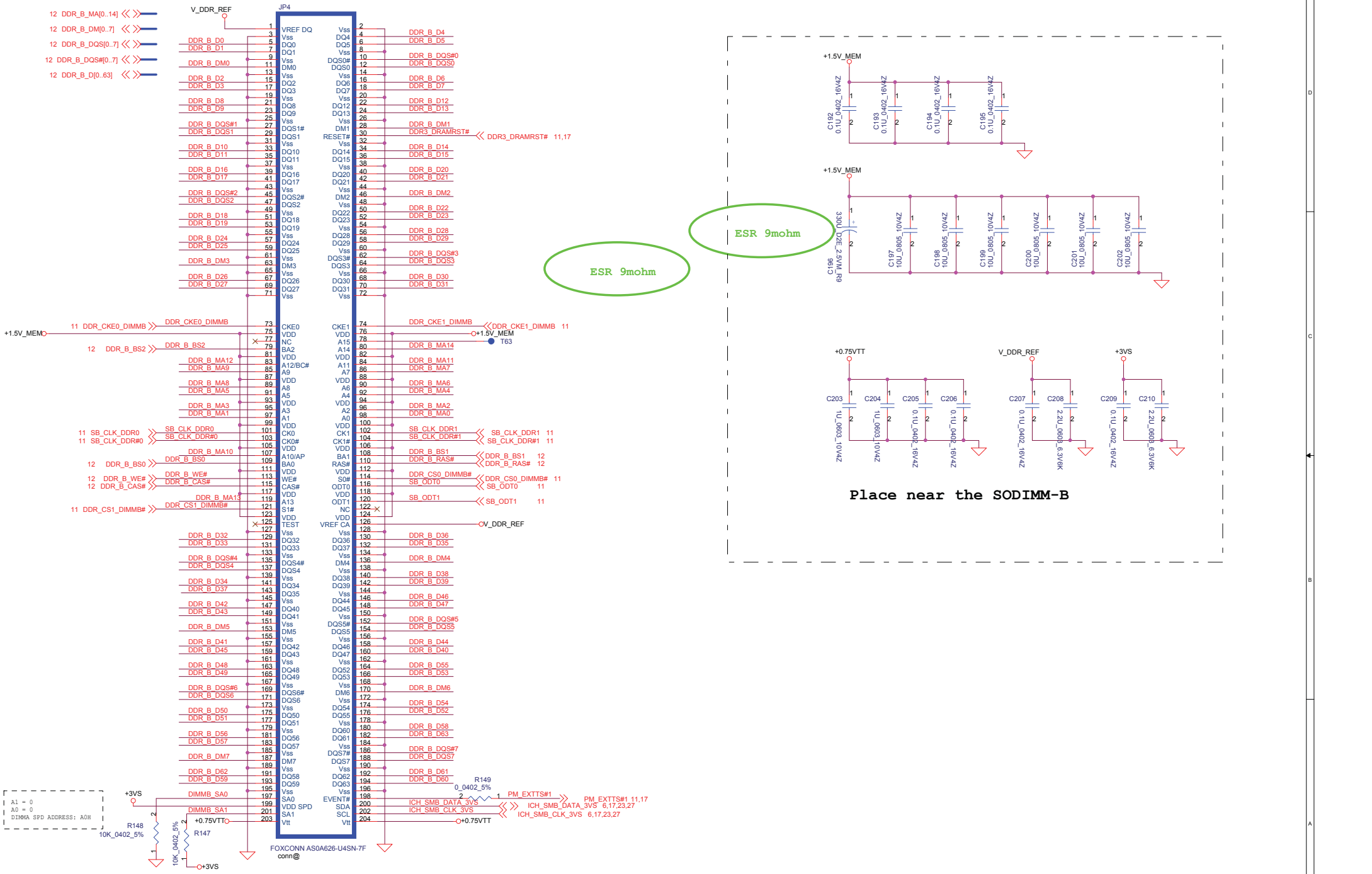




http://hobi-elektronika.net

Title	GMCH(SFF) 6/6	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 16 of 45	


JP3
V_DDR_REF
12 DDR_A_MA[0..14]
12 DDR_A_DM[0..7]
12 DDR_A_DQS[0..7]
12 DDR_A_DQS#[0..7]
12 DDR_A_D[0..63]
FOXCONN AS0A626-U4SN-7F
conn@
Reverse
A1 = 0
A0 = 0
DIMMA SPD ADDRESS: A0H
R144 10K_0402_5%
R145 10K_0402_5%
R146 0_0402_5%
ESR 9mohm
Place near the SODIMM-A
Change CLIP2 to H39
DVT, 06-12
H39 H_3P2
CLIP3
CLIP4
Rrmove CLIP1 and CLIP5
DVT 2008-06-24
GND PAD for EMI
10-26
http://hobi-elektronika.net
Title
Memory Channel - A
Size
Custom
Document Number
Bradstreet
Rev
<RevCode>
Date: Monday, August 04, 2008
Sheet 17 of 45


JP4
V_DDR_REF
FOXCONN AS0A626-U4SN-7F
conn@
ESR 9mohm
ESR 9mohm
+1.5V_MEM
+0.75VTT
V_DDR_REF
+3VS
Place near the SODIMM-B
A1 = 0
A0 = 0
DIMMA SPD ADDRESS: A0H
R148
10K_0402_5%
R147
R149
0_0402_5%
http://hobi-elektronika.net
Title
Memory Channel - B
Size
Custom
Document Number
Bradstreet
Rev
<RevCode>
Date:
Monday, August 04, 2008
Sheet
18
of
45

CRT

+3vs, Decoupling Capacitors for PI3512.

C212 C213 C214 C215 0.1U_0402_16V4Z

Need change to same net with LAN switch/USB switch

defult 0, need add pull down R? 04/25

U6 PI3V512QE_QSOP24

34 DOCKEN_VGA	DOCKEN_VGA	SEL
13 D_RED	D_RED	YA
13 D_GREEN	D_GREEN	YB
13 D_BLUE	D_BLUE	YC
13 CRT_HSYNC	CRT_HSYNC	YD
13 CRT_VSYNC	CRT_VSYNC	YE

VDD, GND

A0	CRT_R_MB	
B0	CRT_G_MB	
C0	CRT_B_MB	
D0	CRT_HSYNC_MB	
E0	CRT_VSYNC_MB	
A1	CRT_R_DOCK	36
B1	CRT_G_DOCK	36
C1	CRT_B_DOCK	36
D1	CRT_HSYNC_DOCK	36
E1	CRT_VSYNC_DOCK	36

DOCKEN_VGA	0: TO MB ★
	1: TO DOCK

L YN to IN0
H YN to IN1

R150 10K_0402_5%

DOCKEN_VGA DOCKEN_VGA# Q4 2N7002W-7-F_SOT323-3

R151 2.2K_0402_5% R152 2.2K_0402_5%

CRT_DDC_CLK CRT_DDC_DATA

U7 SN74CBTD3306CPWR_TSSOP8

13 CRT_DDC_DATA — CRT_DDC_DATA — DOCKEN_VGA DOCKEN_VGA# — 3VDDCDA 3VDDCDA_DOCK — 3VDDCDA_DOCK 36

C216 0.1U_0402_16V4Z

U8 SN74CBTD3306CPWR_TSSOP8

13 CRT_DDC_CLK — CRT_DDC_CLK — DOCKEN_VGA DOCKEN_VGA# — 3VDDCCL 3VDDCCL_DOCK — 3VDDCCL_DOCK 36

C217 0.1U_0402_16V4Z

1.1A 6V UL/CSA/TUV

D4 RB491D_SC59-3

C218 0.1U_0402_16V4Z R154 2.2K_0402_5% R155 2.2K_0402_5%

need 47onh25%/0.3ohm/100mA Bead
SM01000C600

FBMA-L11-201209-170LMT L4 L6 L8

CRT_R_MB CRT_G_MB CRT_B_MB — CRT_R_MB_MID CRT_G_MB_MID CRT_B_MB_MID — CRTR CRTG CRTB

R266 R319 R320 0_0603_5%

C219 0.1U_0402_16V4Z

D5 D6 D7 @ DAN217_SC59-3

R156 150_0402_1% R157 R158

C223 C224 C225 C226 C227 C228 C229 C230 C231 10P_0402_25V8K

P6-GND P11-NC P7-GND P12-3VDDCDA P8-GND P13-HSYNC P9-CRTVCC P14-VSYNC P10-GND P15-3VDDCCL
P1-R P2-G P3-B

CRT Footprint

JP5 SUYIN_070112FR015S222XU

3VDDCDA CRTR CRTG CRTB CRT_HSYNC_MB_C CRT_VSYNC_MB_C 3VDDCCL

C220 47P_0402_50V8J @ C221 47P_0402_50V8J @ C222 conn@ 100P_0402_50V8J

Follow ME advice change PN to DC060001300
2008-04-01,
change PCB FT to SUYIN_070546FR015S2307R_15P,
same with JAL70(A58)
DVT, 0619

will update to 47ohm/100MHz bead.

U35 U36 74AHCT1G125GW_SOT353-5

CRT_HSYNC_MB CRT_HSYNC_MB_C C252 R360 1K_0402_5%

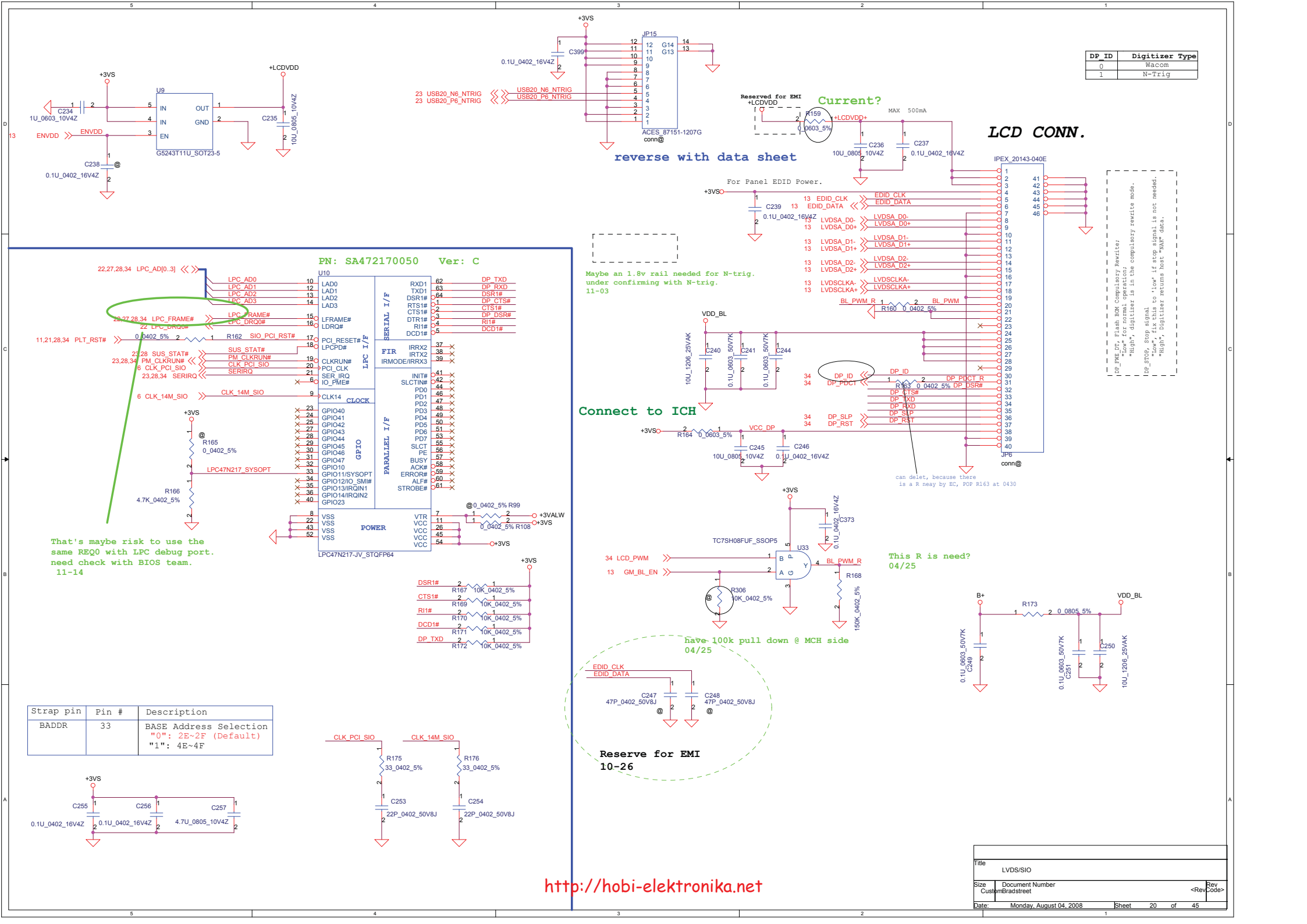
CRT_VSYNC_MB CRT_VSYNC_MB_C C374

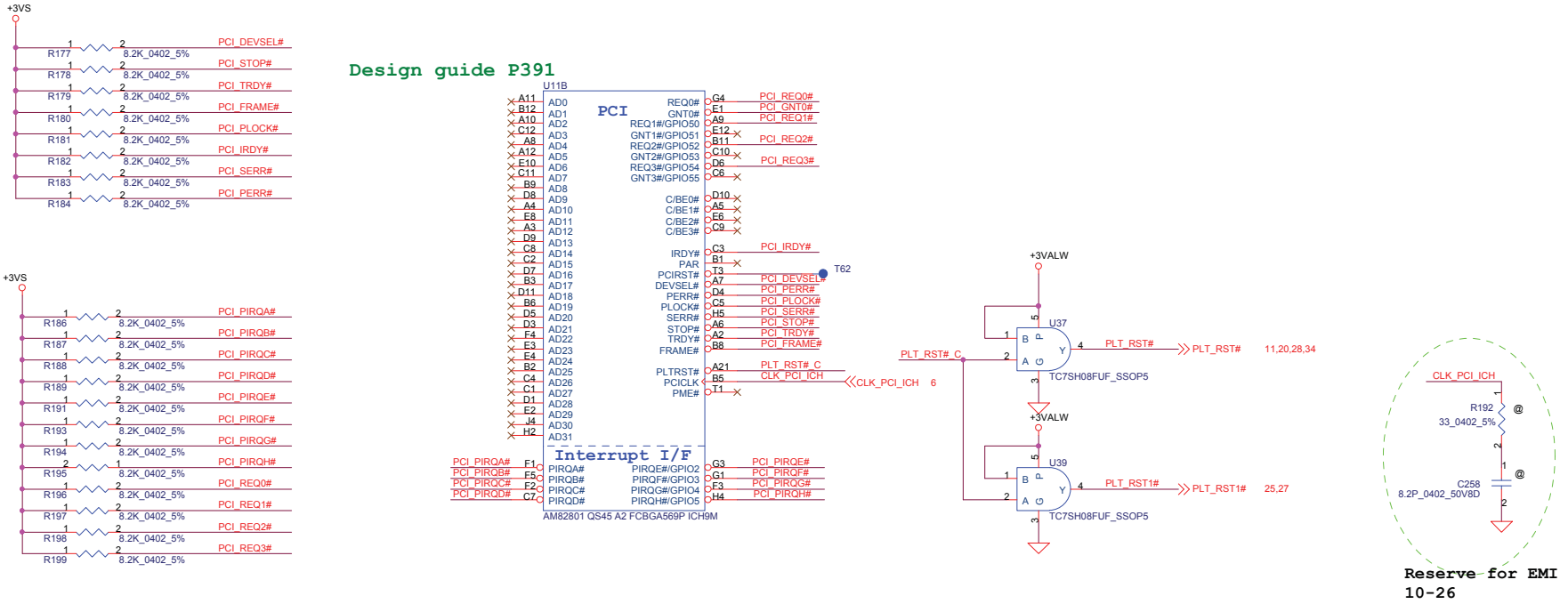
C232 C233 0.1U_0402_16V4Z D9 D8 DAN217_SC59-3

CRT_VSYNC_MB_C CRT_HSYNC_MB_C

http://hobi-elektronika.net

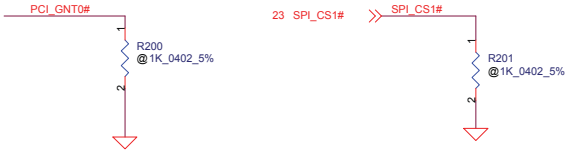
Title	CRT/BlueTooth/Camera		
Size	Document Number		Rev
Custom	Bradstreet		<RevCode>
Date:	Monday, August 04, 2008	Sheet 19 of 45	


+3VS
U9
IN
IN
EN
OUT
GND
G5243T11U_SOT23-5
C234
1U_0603_10V4Z
ENVDD
C238
0.1U_0402_16V4Z
+LCDVDD
C235
10U_0805_10V4Z
C399
0.1U_0402_16V4Z
JP15
ACES_87151-1207G
conn@
23 USB20_N6_NTRIG
23 USB20_P6_NTRIG
USB20_N6_NTRIG
USB20_P6_NTRIG
Reserved for EMI
+LCDVDD
R159
0_0603_5%
+LCDVDD+
MAX 500mA
Current?
C236
10U_0805_10V4Z
C237
0.1U_0402_16V4Z
LCD CONN.
reverse with data sheet
IPEX_20143-040E
For Panel EDID Power.
C239
0.1U_0402_16V4Z
13 EDID_CLK
13 EDID_DATA
EDID_CLK
EDID_DATA
LVDSA_D0-
LVDSA_D0+
LVDSA_D1-
LVDSA_D1+
LVDSA_D2-
LVDSA_D2+
LVDSCLKA-
LVDSCLKA+
BL_PWM_R
R160 0_0402_5%
BL_PWM
DP_FWR_DT, Flash BOM Compulsory Rewrite;
"Low", For normal operation
"High", digitizer is in the compulsory rewrite mode.
DP_STOP, Stop signal
"Low", fix this to 'low' if stop signal is not needed.
"High", Digitizer returns host "NAK" data.
Maybe an 1.8v rail needed for N-trig.
under confirming with N-trig.
11-03
VDD_BL
C240
10U_1206_25VAK
C241
0.1U_0603_50V7K
C244
0.1U_0603_50V7K
34 DP_ID
34 DP_PDCT
DP_ID
R163 0_0402_5% DP_PDCT_R
DP_DSR#
DP_CTS#
DP_TXD
DP_RXD
DP_SLP
DP_RST
Connect to ICH
34 DP_SLP
34 DP_RST
R164 0_0603_5%
VCC_DP
C245
10U_0805_10V4Z
C246
0.1U_0402_16V4Z
JP6
conn@
can delet, because there
is a R neay by EC, POP R163 at 0430
PN: SA472170050 Ver: C
U10
LPC47N217-JV_STQFP64
22,27,28,34 LPC_AD[0..3]
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
22,27,28,34 LPC_FRAME#
22 LPC_DRQ0#
LPC_FRAME#
LPC_DRQ0#
11,21,28,34 PLT_RST#
0_0402_5%
R162
SIO_PCI_RST#
23,28 SUS_STAT#
23,28,34 PM_CLKRUN#
6 CLK_PCI_SIO
23,28,34 SERIRQ
SUS_STAT#
PM_CLKRUN#
CLK_PCI_SIO
SERIRQ
6 CLK_14M_SIO
CLK_14M_SIO
LPC I/F
CLOCK
SERIAL I/F
FIR
PARALLEL I/F
GPIO
POWER
DP_TXD
DP_RXD
DSR1#
DP_CTS#
CTS1#
DP_DSR#
RI1#
DCD1#
@0_0402_5% R99
0_0402_5% R108
+3VALW
+3VS
That's maybe risk to use the
same REQ0 with LPC debug port.
need check with BIOS team.
11-14
R165
0_0402_5%
LPC47N217_SYSOPT
R166
4.7K_0402_5%
DSR1#
CTS1#
RI1#
DCD1#
DP_TXD
R167 10K_0402_5%
R169 10K_0402_5%
R170 10K_0402_5%
R171 10K_0402_5%
R172 10K_0402_5%
TC7SH08FUF_SSOP5
U33
34 LCD_PWM
13 GM_BL_EN
R306
10K_0402_5%
BL_PWM_R
R168
150K_0402_5%
C373
0.1U_0402_16V4Z
This R is need?
04/25
have 100k pull down @ MCH side
04/25
EDID_CLK
EDID_DATA
C247
47P_0402_50V8J
C248
47P_0402_50V8J
Reserve for EMI
10-26
B+
R173
0_0805_5%
VDD_BL
C249
0.1U_0603_50V7K
C251
0.1U_0603_50V7K
C250
10U_1206_25VAK
Strap pin | Pin # | Description
BADDR | 33 | BASE Address Selection
"0": 2E~2F (Default)
"1": 4E~4F
C255
0.1U_0402_16V4Z
C256
0.1U_0402_16V4Z
C257
4.7U_0805_10V4Z
CLK_PCI_SIO
CLK_14M_SIO
R175
33_0402_5%
R176
33_0402_5%
C253
22P_0402_50V8J
C254
22P_0402_50V8J
DP_ID | Digitizer Type
0 | Wacom
1 | N-Trig
http://hobi-elektronika.net
Title
LVDS/SIO
Size
Custom
Document Number
Bradstreet
Rev
<RevCode>
Date: Monday, August 04, 2008
Sheet 20 of 45



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



Title	ICH9M(SFF) 1/4	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 21 of 45	

ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH_RSVD	HDA_SDOUT_CODEC	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	NormalOperation(Default)
1	1	Set PCIE port config bit1

XOR CHAIN ENTRANCE STRAP:RSVD

CMOS signal need take care the sequense
ICH=>IMVP=>MCH=>CPU

need updated FT,
Temp FT:JUMP_43X34

what's means?
11-14

near ICH

Follow Schematic Check List,
8.2k pull up.
2007-11-22

placed within 2" from ICH9M

Within 500 mils

change to 16V X7R
2008-05-26

Place near HDD
SATA connector.

Those decoupling capacitors need
place near the SATA connector

pin 1 and pi4 change

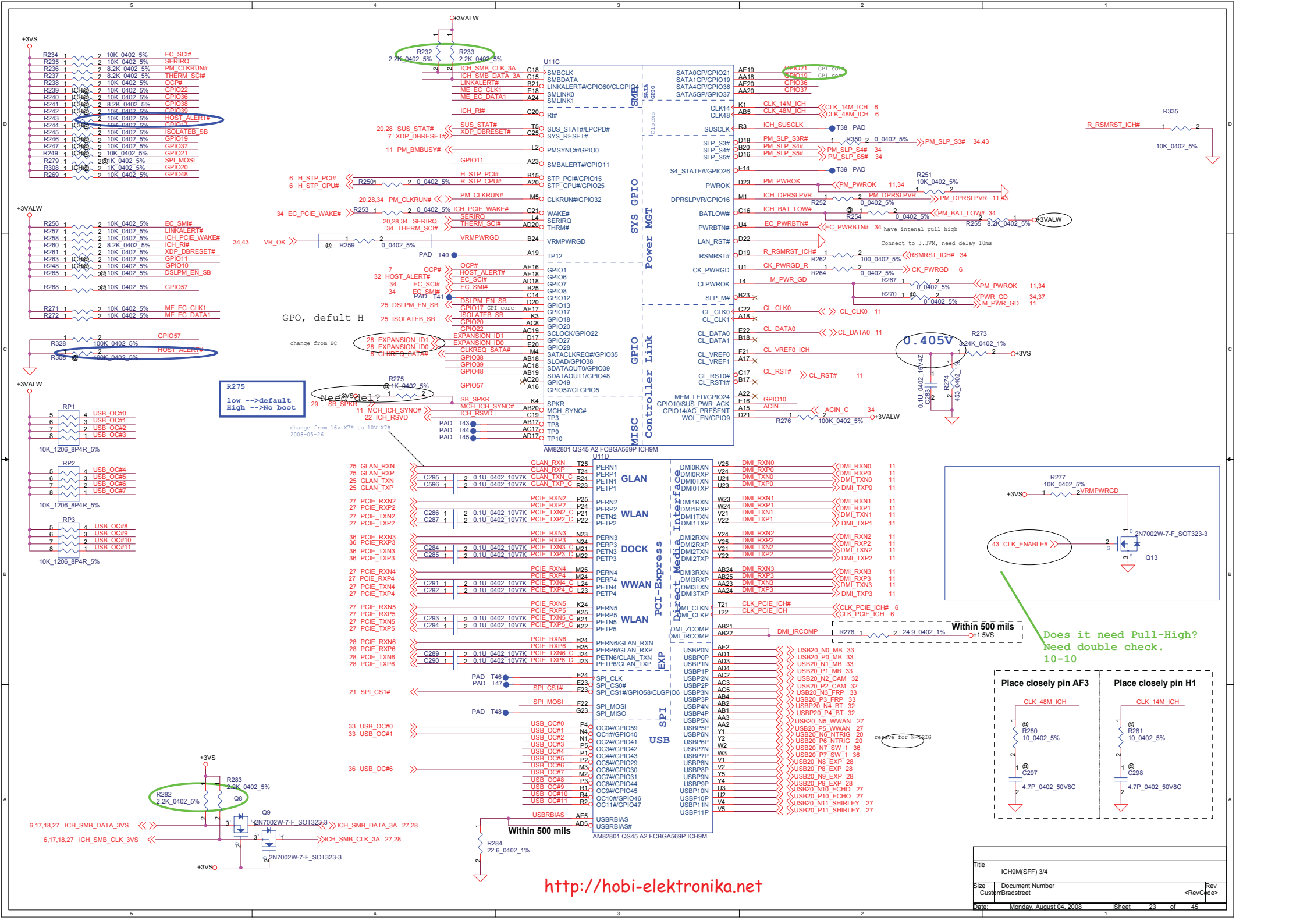
G-Sensor

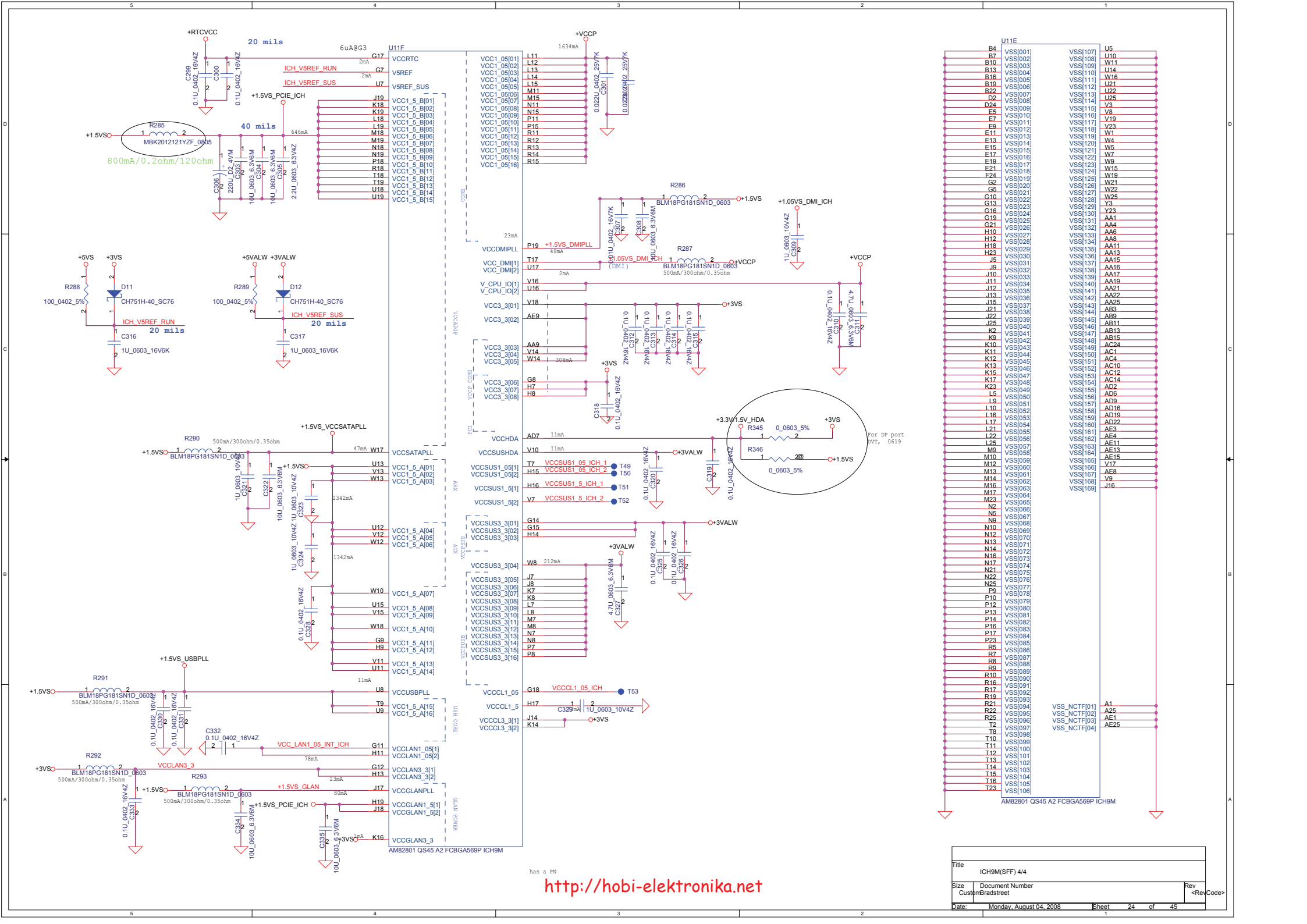
SM BUS Addr. 0011 000

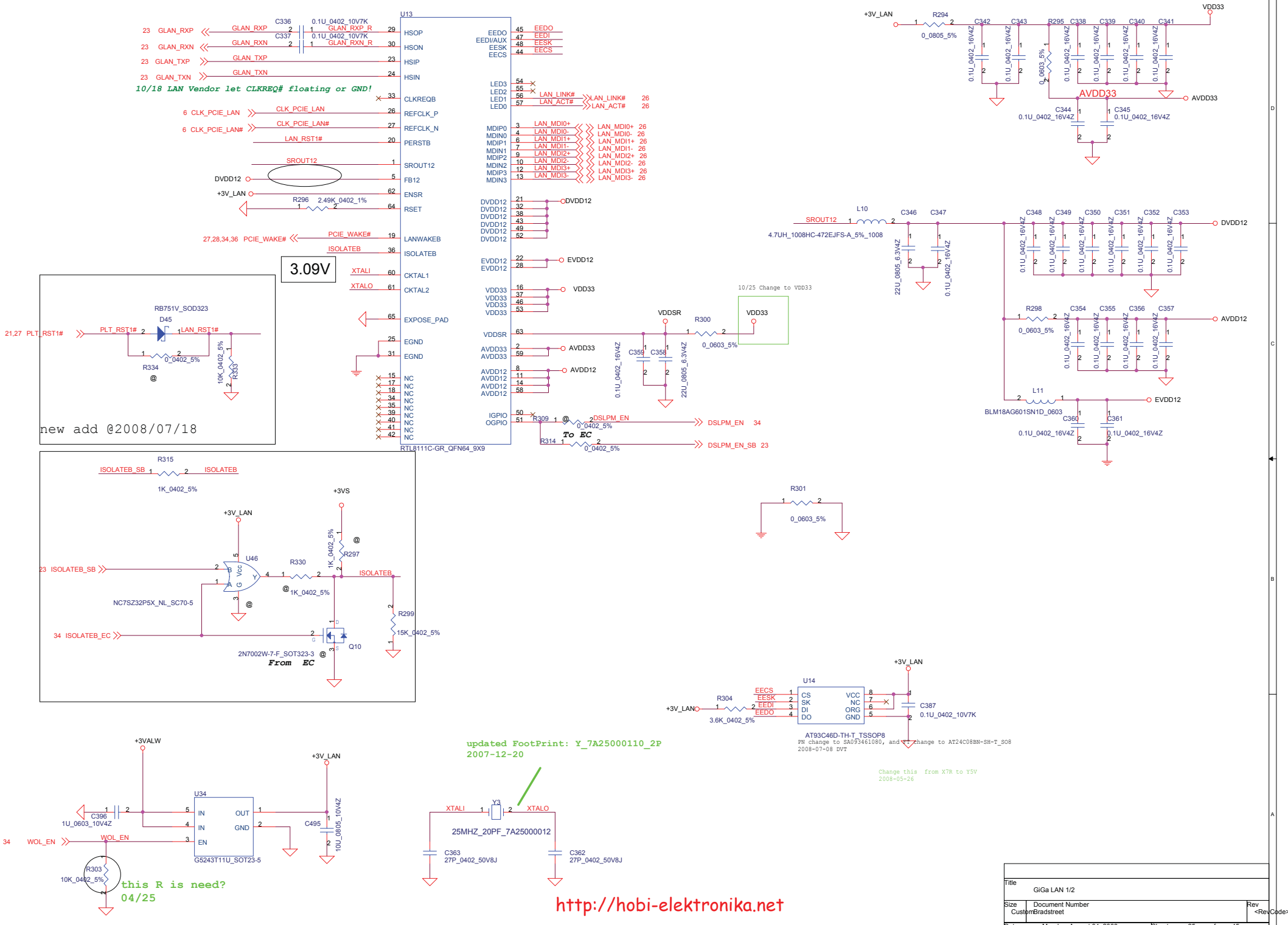
SM BUS Addr: 0011 0000

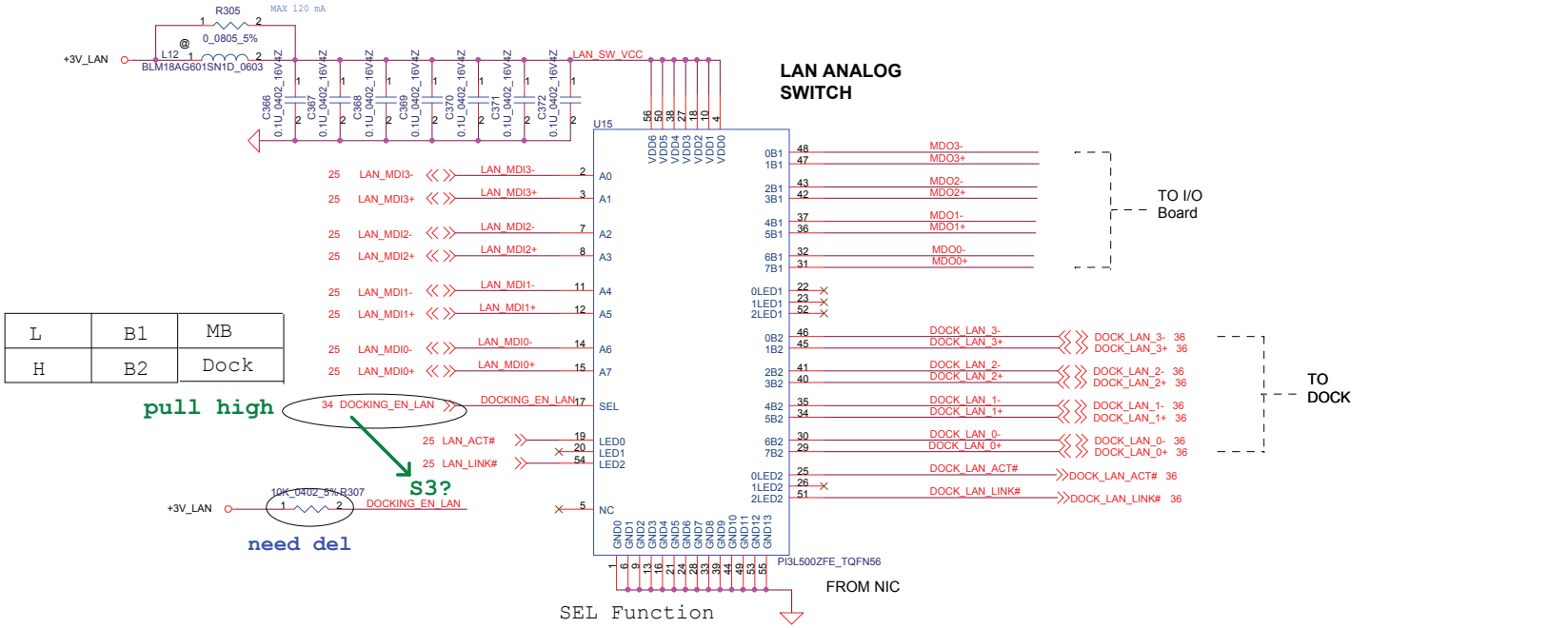
http://hobi-elektronika.net

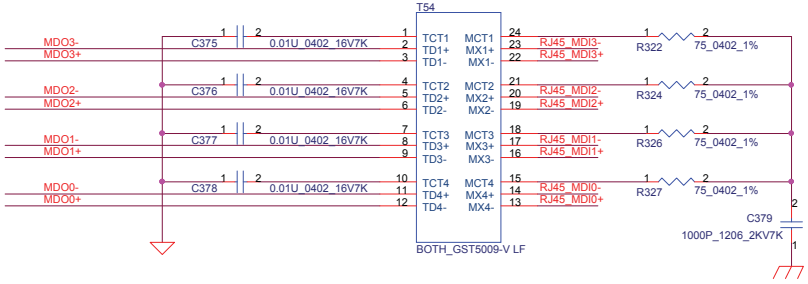
Title	ICH9M(SFF) 2/4 , G-Sensor
Size	Custom
Document Number	Bradstreet
Rev	<RevCode>
Date:	Monday, August 04, 2008
Sheet	22 of 45

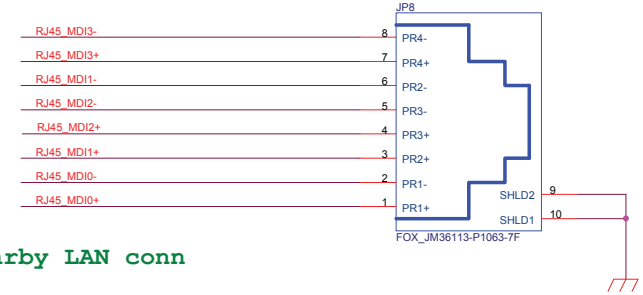

+3VS
+3VALW
R234 10K_0402_5% EC_SCI#
R235 10K_0402_5% SERIRQ
R236 8.2K_0402_5% PM_CLKRUN#
R237 8.2K_0402_5% THERM_SCI#
R238 10K_0402_5% OCP#
R239 10K_0402_5% GPIO22
R240 10K_0402_5% GPIO36
R241 8.2K_0402_5% GPIO38
R242 10K_0402_5% GPIO39
R243 10K_0402_5% HOST_ALERT1#
R244 10K_0402_5% GPIO17
R245 10K_0402_5% ISOLATEB_SB
R246 10K_0402_5% GPIO19
R247 10K_0402_5% GPIO37
R249 10K_0402_5% GPIO21
R279 1K_0402_5% SPI_MOSI
R308 1K_0402_5% GPIO20
R269 10K_0402_5% GPIO48
R256 10K_0402_5% EC_SMI#
R257 10K_0402_5% LINKALERT#
R258 10K_0402_5% ICH_PCIE_WAKE#
R260 8.2K_0402_5% ICH_RI#
R261 10K_0402_5% XDP_DBRESET#
R263 10K_0402_5% GPIO11
R248 10K_0402_5% GPIO10
R265 10K_0402_5% DSLPM_EN_SB
R268 10K_0402_5% GPIO57
R271 10K_0402_5% ME_EC_CLK1
R272 10K_0402_5% ME_EC_DATA1
R328 100K_0402_5% GPIO57
R358 100K_0402_5% HOST_ALERT1#
GPO, defult H
change from EC
R275
low -->default
High -->No boot
Need del?
change from 16v X7R to 10V X7R
2008-05-26
RP1 USB_OC#0 USB_OC#1 USB_OC#2 USB_OC#3
RP2 USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7
RP3 USB_OC#8 USB_OC#9 USB_OC#10 USB_OC#11
10K_1206_8P4R_5%
R232 2.2K_0402_5%
R233 2.2K_0402_5%
U11C
SMBCLK SMBDATA LINKALERT#/GPIO60/CLGPIO2 SMLINK0 SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP12
GPIO1 GPIO6 GPIO7 GPIO8 GPIO12 GPIO13 GPIO17 GPIO18 GPIO20 GPIO22
SCLOCK/GPIO22
GPIO27 GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3 TP8 TP9 TP10
SMB
SATA GPIO
GPIO
SYS
Power MGT
Clocks
GPIO
Controller Link
MISC
SATA0GP/GPIO21 SATA1GP/GPIO19 SATA4GP/GPIO36 SATA5GP/GPIO37
CLK14 CLK48
SUSCLK
SLP_S3# SLP_S4# SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0 CL_CLK1
CL_DATA0 CL_DATA1
CL_VREF0 CL_VREF1
CL_RST0# CL_RST1#
MEM_LED/GPIO24
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
WOL_EN/GPIO9
AM82801 QS45 A2 FCBGA569P ICH9M
U11D
PERN1 PETN1 PETP1 GLAN
PERN2 PETN2 PETP2 WLAN
PERN3 PETN3 PETP3 DOCK
PERN4 PETN4 PETP4 WWAN
PERN5 PETN5 PETP5 WLAN
PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP
PCI-Express
EXP
SPI_CLK SPI_CS0# SPI_CS1#/GPIO58/CLGPIO6 SPI_MOSI SPI_MISO
SPI
OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8#/GPIO44 OC9#/GPIO45 OC10#/GPIO46 OC11#/GPIO47
USB
USBRBIAS USBRBIAS#
DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_CLKN DMI_CLKP
DMI_ZCOMP DMI_IRCOMP
Direct Media Interface
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P
AM82801 QS45 A2 FCBGA569P ICH9M
R335 10K_0402_5%
R251 10K_0402_5%
R252 0_0402_5%
R254 0_0402_5%
R255 8.2K_0402_5%
R262 100_0402_5%
R264 0_0402_5%
R267 0_0402_5%
R270 0_0402_5%
R273 3.24K_0402_1%
R274 453_0402_1%
0.405V
C263 0.1U_0402_16V4Z
R276 100K_0402_5%
R277 10K_0402_5%
R278 24.9_0402_1%
Within 500 mils
Does it need Pull-High?
Need double check.
10-10
2N7002W-7-F_SOT323-3
Q13
Q8
Q9
R283 2.2K_0402_5%
R282 2.2K_0402_5%
R284 22.6_0402_1%
reserve for N-TRIG
Place closely pin AF3
Place closely pin H1
R280 10_0402_5%
R281 10_0402_5%
C297 4.7P_0402_50V8C
C298 4.7P_0402_50V8C
http://hobi-elektronika.net
Title ICH9M(SFF) 3/4
Size Custom
Document Number Bradstreet
Rev <RevCode>
Date: Monday, August 04, 2008
Sheet 23 of 45


+RTCVCC
20 mils
6uA@G3
U11F
VCCRTC
V5REF
V5REF_SUS
ICH_V5REF_RUN
ICH_V5REF_SUS
+1.5VS_PCIE_ICH
+1.5VS
R285
MBK2012121YZF_0805
800mA/0.2ohm/120ohm
40 mils
646mA
+VCCP
1634mA
+1.05VS_DMI_ICH
R286
R287
BLM18PG181SN1D_0603
500mA/300ohm/0.35ohm
+5VS
+3VS
+5VALW
+3VALW
R288
R289
D11
D12
CH751H-40_SC76
100_0402_5%
ICH_V5REF_RUN
ICH_V5REF_SUS
20 mils
C316
C317
1U_0603_16V6K
+1.5VS_VCCSATAPLL
R290
47mA
+1.5VS_USBPLL
R291
11mA
R292
R293
VCCLAN3_3
+1.5VS_GLAN
80mA
VCC_LAN1_05_INT_ICH
78mA
23mA
+3VS
VCCSUS1_05_ICH_1
VCCSUS1_05_ICH_2
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
VCCCL1_05_ICH
+3.3V1.5V_HDA
R345
R346
0_0603_5%
For DP port
DVT, 0619
AM82801 QS45 A2 FCBGA569P ICH9M
U11E
VSS_NCTF[01]
VSS_NCTF[02]
VSS_NCTF[03]
VSS_NCTF[04]
AM82801 QS45 A2 FCBGA569P ICH9M
has a PN
http://hobi-elektronika.net
Title
ICH9M(SFF) 4/4
Size
Custom
Document Number
Bradstreet
Rev
<RevCode>
Date:
Monday, August 04, 2008
Sheet
24
of
45


U13
RTL8111C-GR_QFN64_9X9
HSOP
HSON
HSIP
HSIN
CLKREQB
REFCLK_P
REFCLK_N
PERSTB
SROUT12
FB12
ENSR
RSET
LANWAKEB
ISOLATEB
CKTAL1
CKTAL2
EXPOSE_PAD
EGND
NC
EEDO
EEDI/AUX
EESK
EECS
LED3
LED2
LED1
LED0
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
DVDD12
EVDD12
VDD33
VDDSR
AVDD33
AVDD12
IGPIO
OGPIO
GLAN_RXP
GLAN_RXN
GLAN_TXP
GLAN_TXN
CLK_PCIE_LAN
CLK_PCIE_LAN#
LAN_RST1#
PCIE_WAKE#
ISOLATEB
XTALI
XTALO
LAN_LINK#
LAN_ACT#
LAN_MDI0+
LAN_MDI0-
LAN_MDI1+
LAN_MDI1-
LAN_MDI2+
LAN_MDI2-
LAN_MDI3+
LAN_MDI3-
DSLPM_EN
DSLPM_EN_SB
10/18 LAN Vendor let CLKREQ# floating or GND!
3.09V
10/25 Change to VDD33
To EC
From EC
new add @2008/07/18
updated FootPrint: Y_7A25000110_2P
2007-12-20
this R is need?
04/25
Change this from X7R to Y5V
2008-05-26
AT93C46D-TH-T_TSSOP8
PN change to SA093461080, and change to AT24C08BN-SH-T_SO8
2008-07-08 DVT
http://hobi-elektronika.net
Title
GiGa LAN 1/2
Size
Custom
Document Number
Bradstreet
Rev
<RevCode>
Date:
Monday, August 04, 2008
Sheet
25
of
45

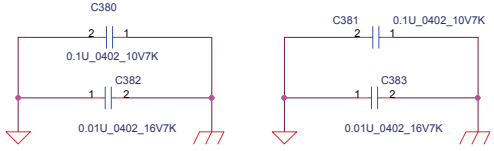




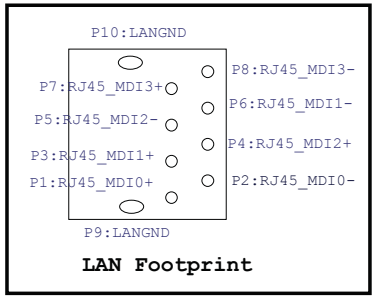


Please nearby LAN conn

USE DC234000B00 PCB Footprint, FOX_JM36113-P1063-7F_8P, same with EFL31
2008-03-18



Realtek reference circuit for EMI!

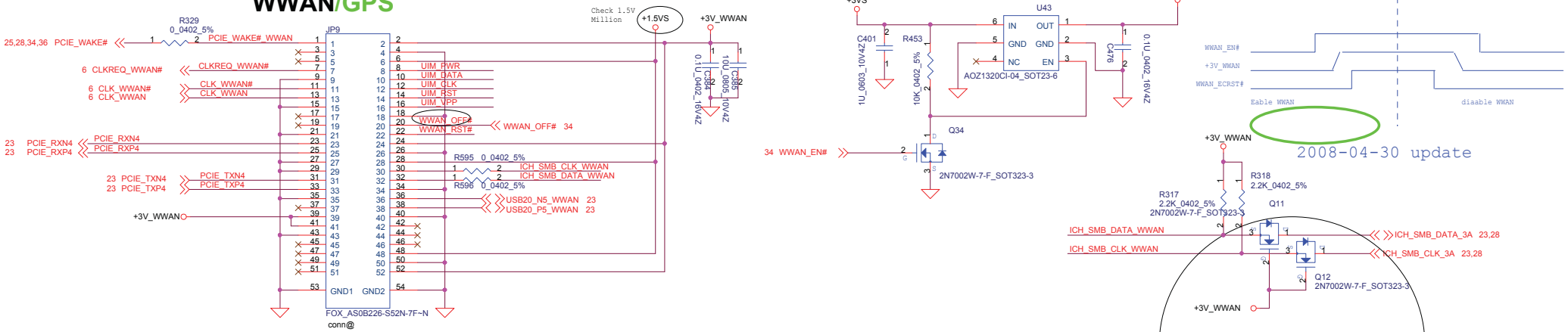


http://hobi-elektronika.net

Title	GiGa LAN 2/2		
Size	Document Number		Rev
Custom	Bradstreet		<RevCode>
Date:	Monday, August 04, 2008	Sheet 26 of 45	

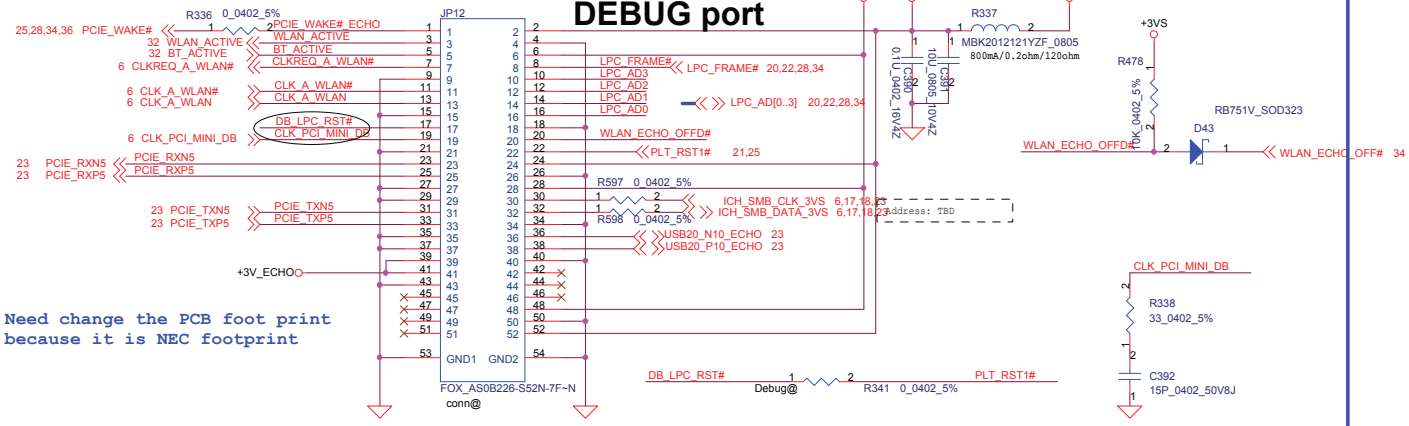
DVT, need study,0619

WWAN/GPS

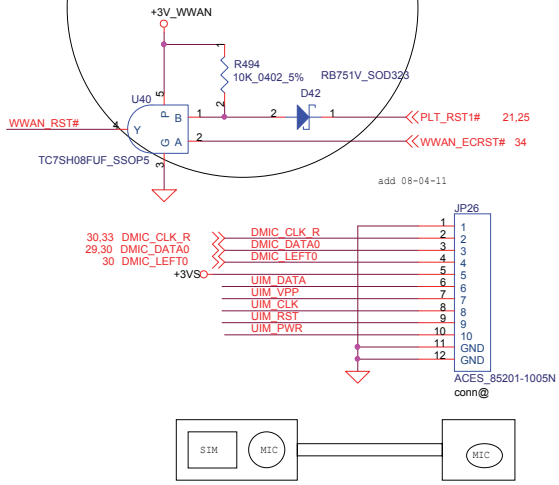


2008-04-30 update

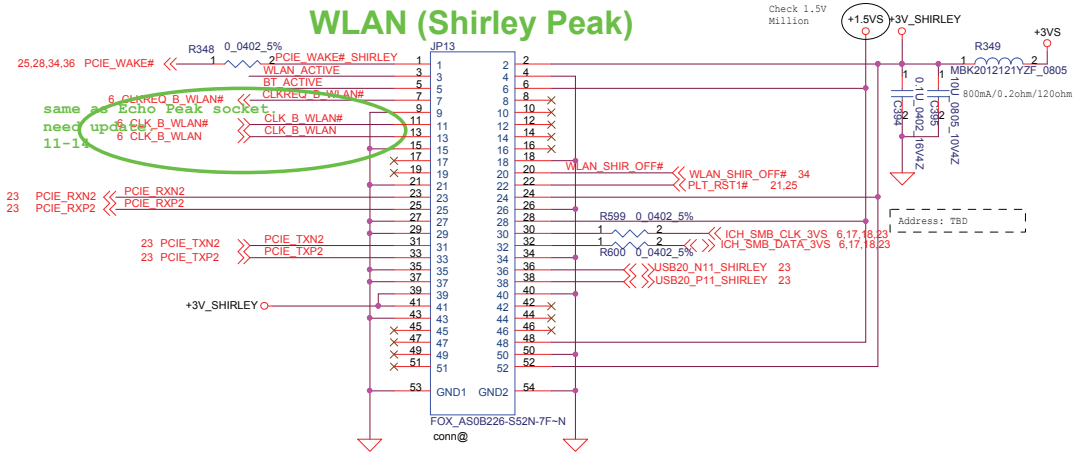
WLAN/WiMax (Echo Peak)/ DEBUG port



Need change the PCB foot print because it is NEC footprint



WLAN (Shirley Peak)



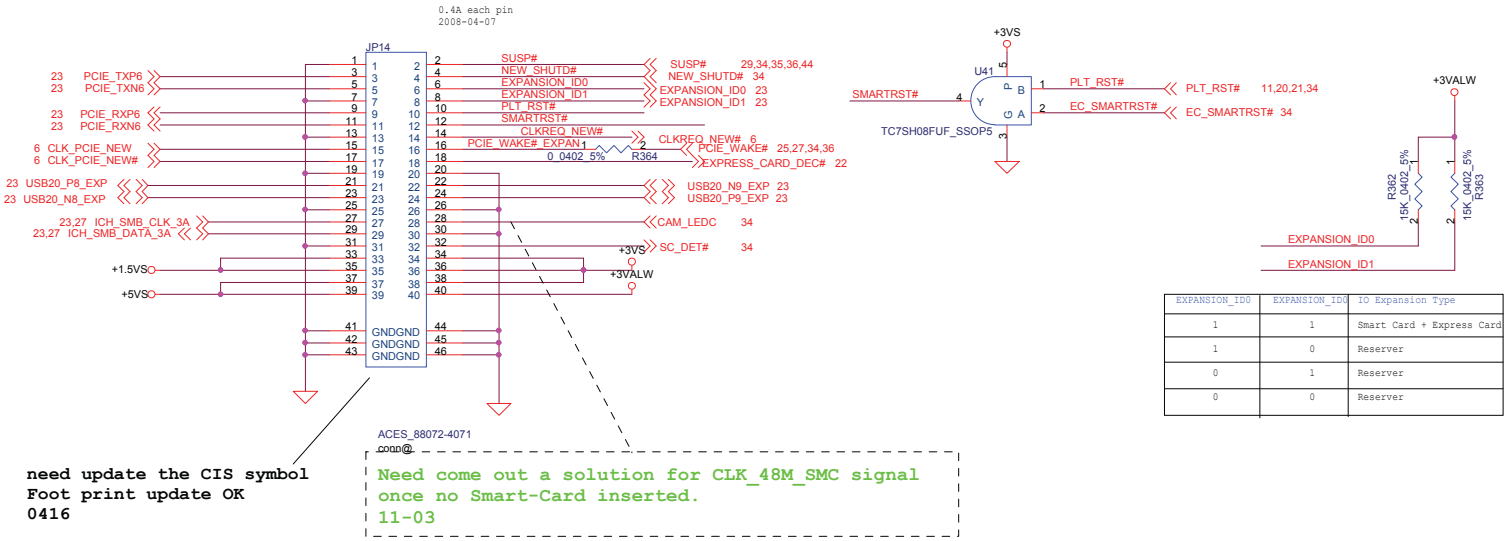
same as Echo Peak socket
need update
11-14

need move to LED board, and the
corlor of LED need modify, also the dim adjustment circuit need been added.
11-12

Title	MINI-Card, Debug	
Size	Document Number	Rev
Custom	Bradstreet	<RevCode>
Date: Monday, August 04, 2008	Sheet 27 of 45	

Expansion Board Conn

del 48MHZ termination R&C
2008-03-21

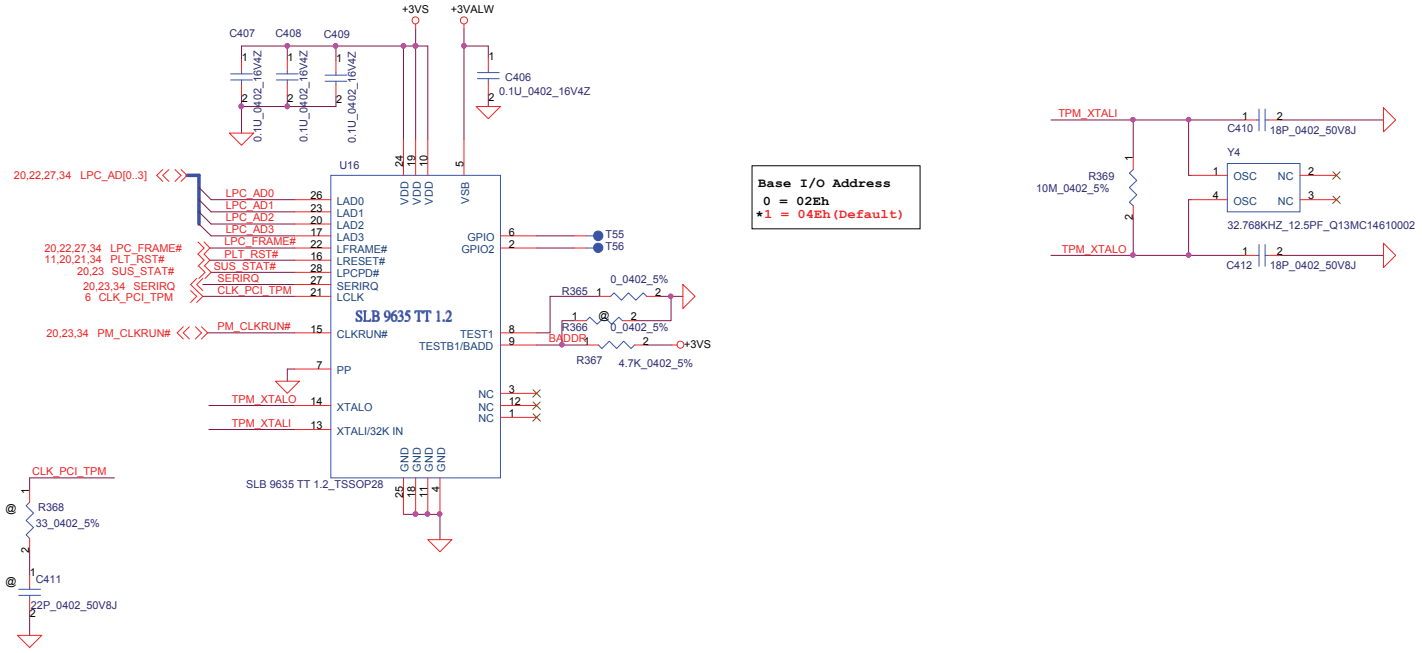


EXPANSION_ID0	EXPANSION_ID0	IO Expansion Type
1	1	Smart Card + Express Card
1	0	Reserver
0	1	Reserver
0	0	Reserver

need update the CIS symbol
Foot print update OK
0416

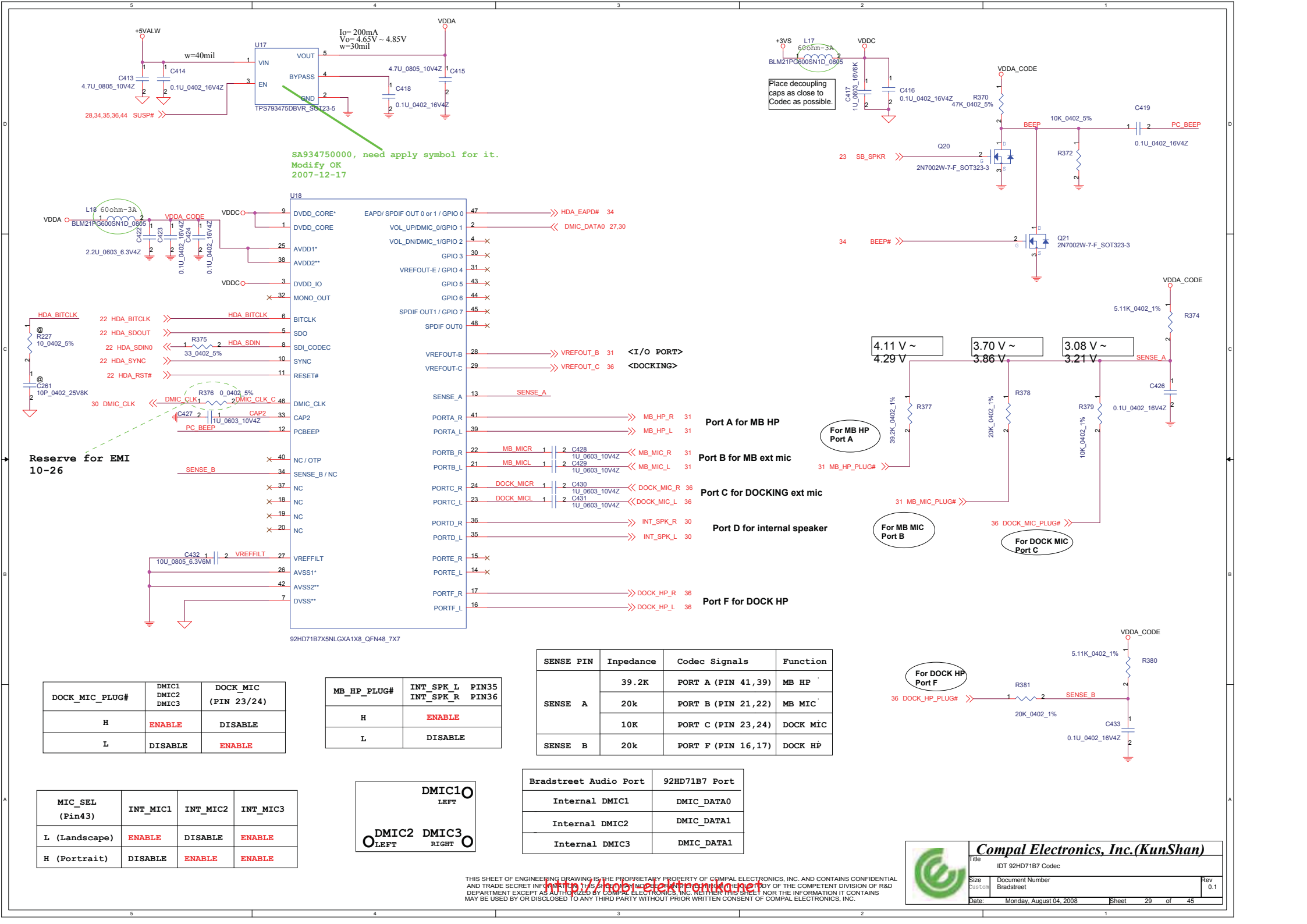
Need come out a solution for CLK_48M_SMC signal
once no Smart-Card inserted.
11-03

TPM



http://hobi-elektronika.net

Title	Expansion, TPM		
Size	Document Number		Rev
Custom	Bradstreet		<RevCode>
Date:	Monday, August 04, 2008	Sheet 28 of 45	



DOCK_MIC_PLUG#	DMIC1 DMIC2 DMIC3	DOCK_MIC (PIN 23/24)
H	ENABLE	DISABLE
L	DISABLE	ENABLE

MB_HP_PLUG#	INT_SPK_L PIN35 INT_SPK_R PIN36
H	ENABLE
L	DISABLE

SENSE PIN	Inpedance	Codec Signals	Function
SENSE A	39.2K	PORT A (PIN 41,39)	MB HP
	20k	PORT B (PIN 21,22)	MB MIC
	10K	PORT C (PIN 23,24)	DOCK MIC
SENSE B	20k	PORT F (PIN 16,17)	DOCK HP

MIC_SEL (Pin43)	INT_MIC1	INT_MIC2	INT_MIC3
L (Landscape)	ENABLE	DISABLE	ENABLE
H (Portrait)	DISABLE	ENABLE	ENABLE

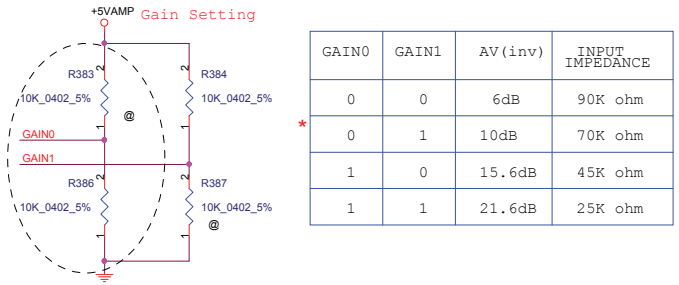
Bradstreet Audio Port	92HD71B7 Port
Internal DMIC1	DMIC_DATA0
Internal DMIC2	DMIC_DATA1
Internal DMIC3	DMIC_DATA1

Compal Electronics, Inc.(KunShan)

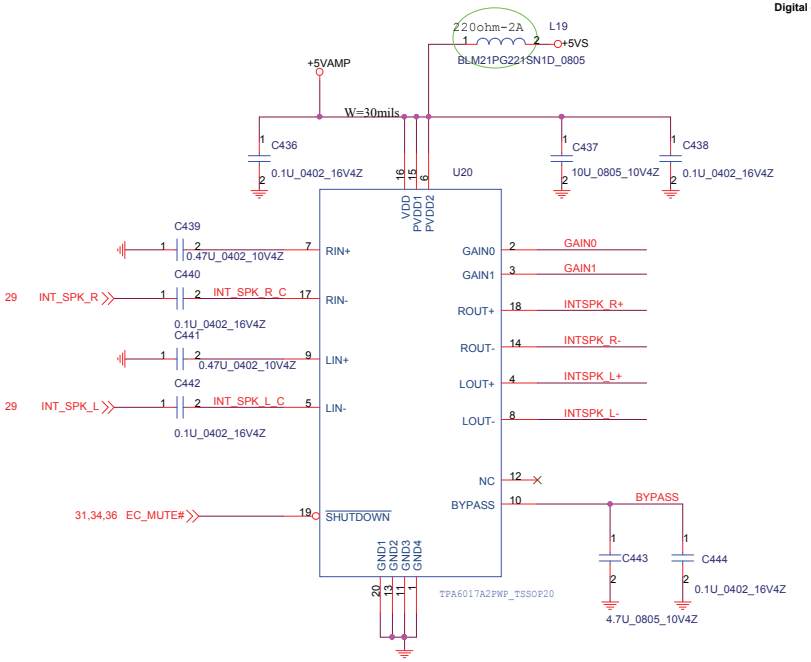
Title: IDT 92HD71B7 Codec

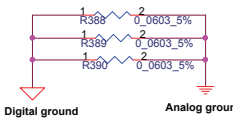
Size: Custom | Document Number: Bradstreet | Rev: 0.1

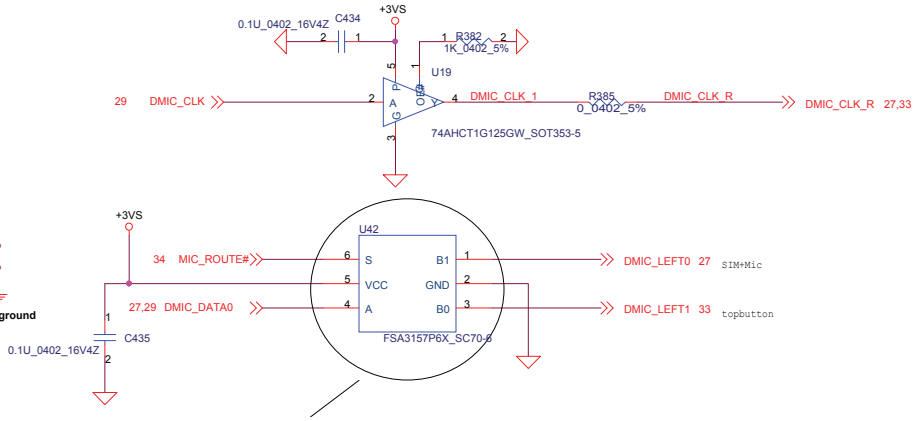
Date: Monday, August 04, 2008 | Sheet 29 of 45



GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm



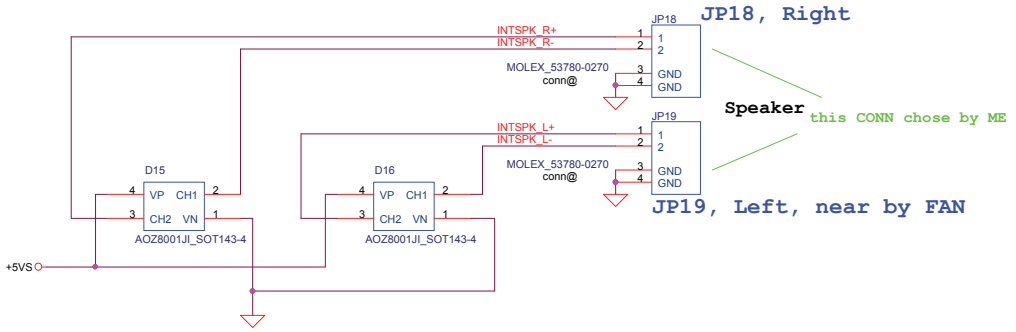




Change to SA731157010
2008-05-26

SEL	
0	B0
1	B1 *

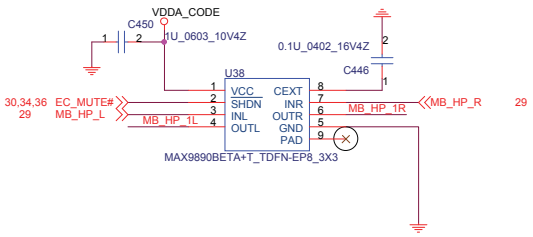
this CONN chose by ME

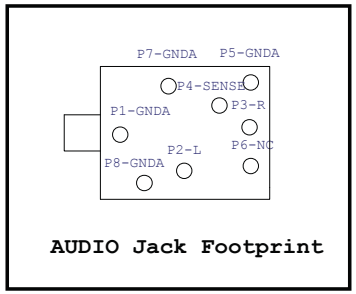


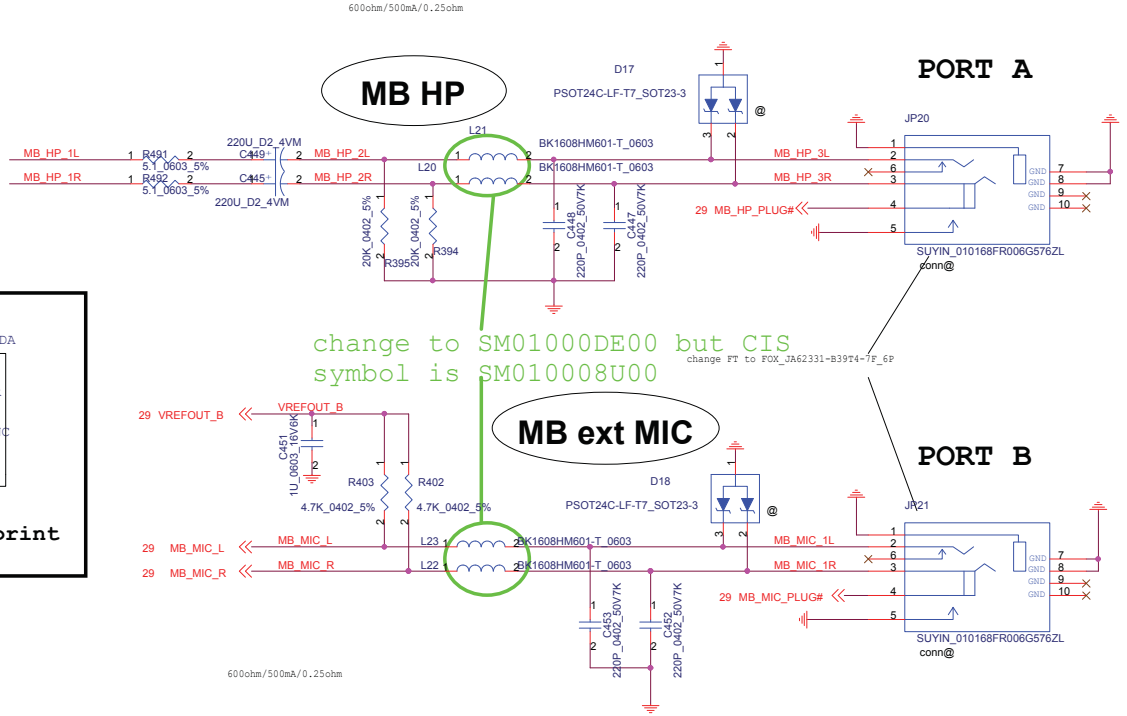
http://hobi-elektronika.net

Compal Electronics, Inc.(KunShan)		
Title: IDT 92HD71B7 Amp&Jack		
Size: Custom	Document Number: Bradstreet-	Rev: 0.01
Date: Monday, August 04, 2008	Sheet 30 of 45	

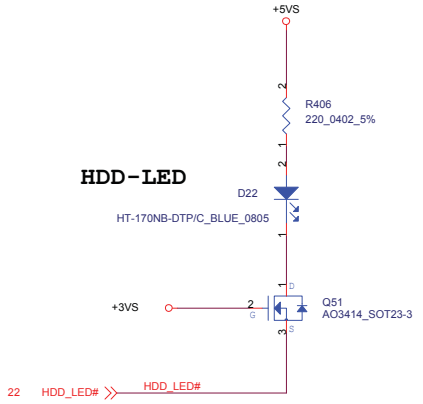
AUDIO JACK







LED

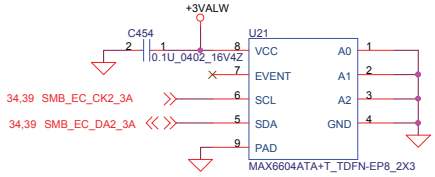


Follow Bill command to delete the LED brightless controller circuit.
1-19

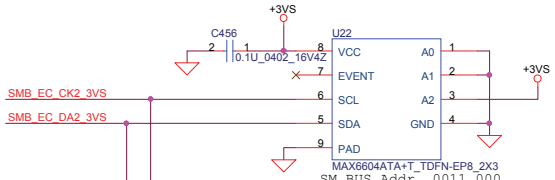
Need double check the signal type.

Title: LED		
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 31 of 45	

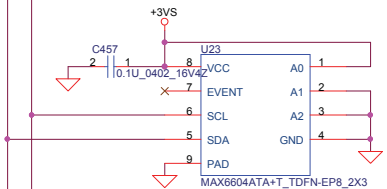
Thermal Sensor



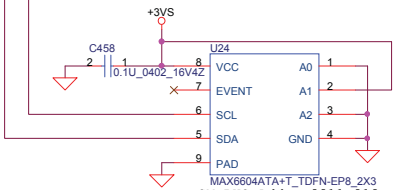
SM BUS Addr. 0011 000
Thermal Sensor for charger



SM BUS Addr. 0011 000
Thermal Sensor for ICH-9M

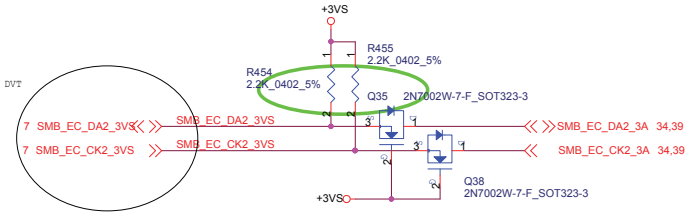


SM BUS Addr. 0011 001
Thermal Sensor for Cantiga



SM BUS Addr. 0011 010
Thermal Sensor for SO-DIMMs

DVT

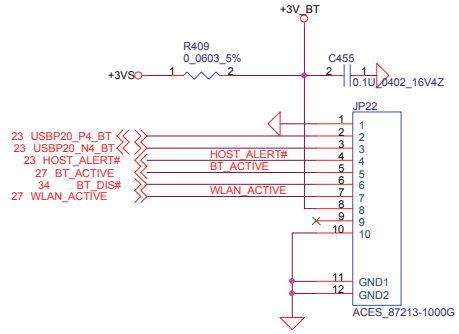


Blue Tooth

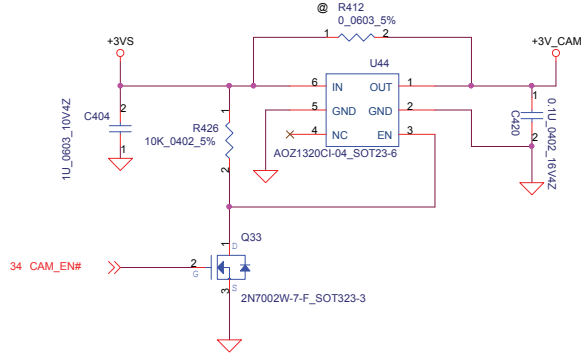
USI BT solution

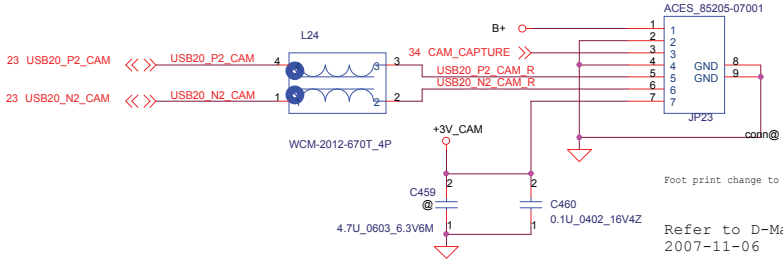
Delete +3V_BT power switch.
2007-11-15

	MB signal		new BT signal
1	GND	1	GND
2	USB+	2	USB+
3	USB-	3	USB-
4	HOST_ALERT#	4	BT_ACTIVE(PIO5)
5	BT_ACTIVE	5	BT_Priority/Ch_Clk(PIO4)
6	HW_RADIO_DIS#	6	HW_RADIO_DIS#(PIO3)
7	WLAN_ACTIVE	7	WLAN_ACTIVE/Ch_Data(PIO6)
8	+3.3V	8	+3.3V
9	NC	9	LED(PIO7)
10	GND	10	GND



Camera





Foot print change to MOLEX_53398-0571_5P

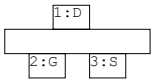
Refer to D-Max GD-5253 SPEC.
2007-11-06

http://hobi-elektronika.net

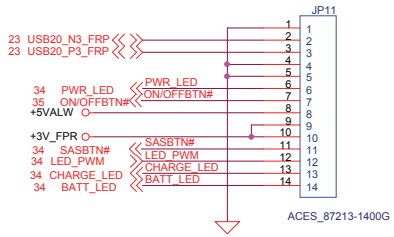
Title	Thermal Sensor		
Size	Document Number		Rev
Custom	Bradstreet		<RevCode>
Date:	Monday, August 04, 2008	Sheet 32 of 45	

Finger Printer

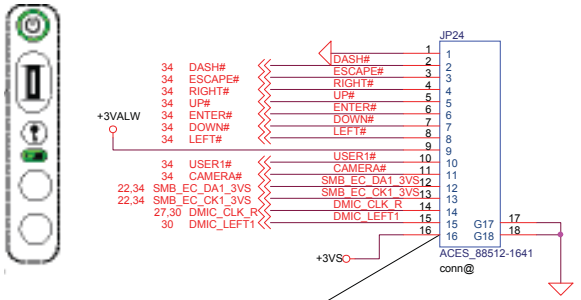
change to LCD MOS?

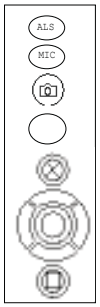


Side button

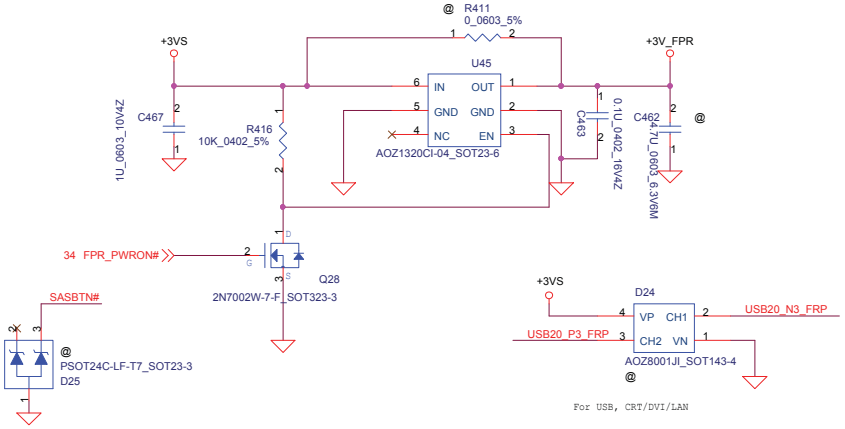


Top side Board Connect to M/B

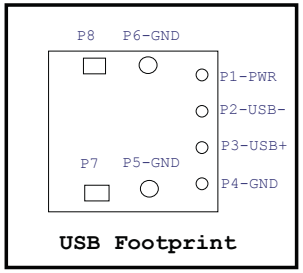




change JP24 to SP01000R700 ACES_88512-1641_16P
0619, DVT
change JP11 to SP02000H800 ACES_87213-1400G_14P
06/26 DVT

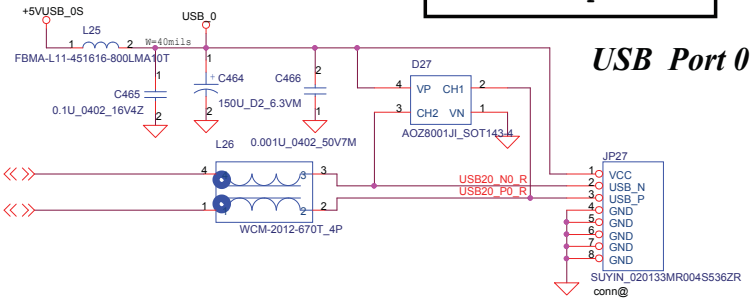


For USB, CRT/DVI/LAN



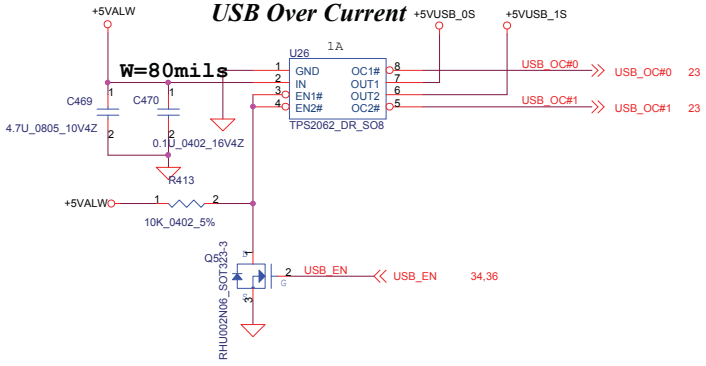
USB Footprint

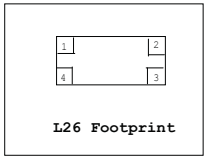
USB Port 0



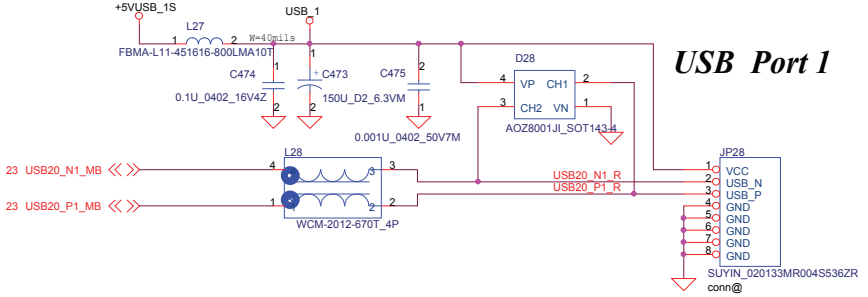
USB ON MB

USB Over Current



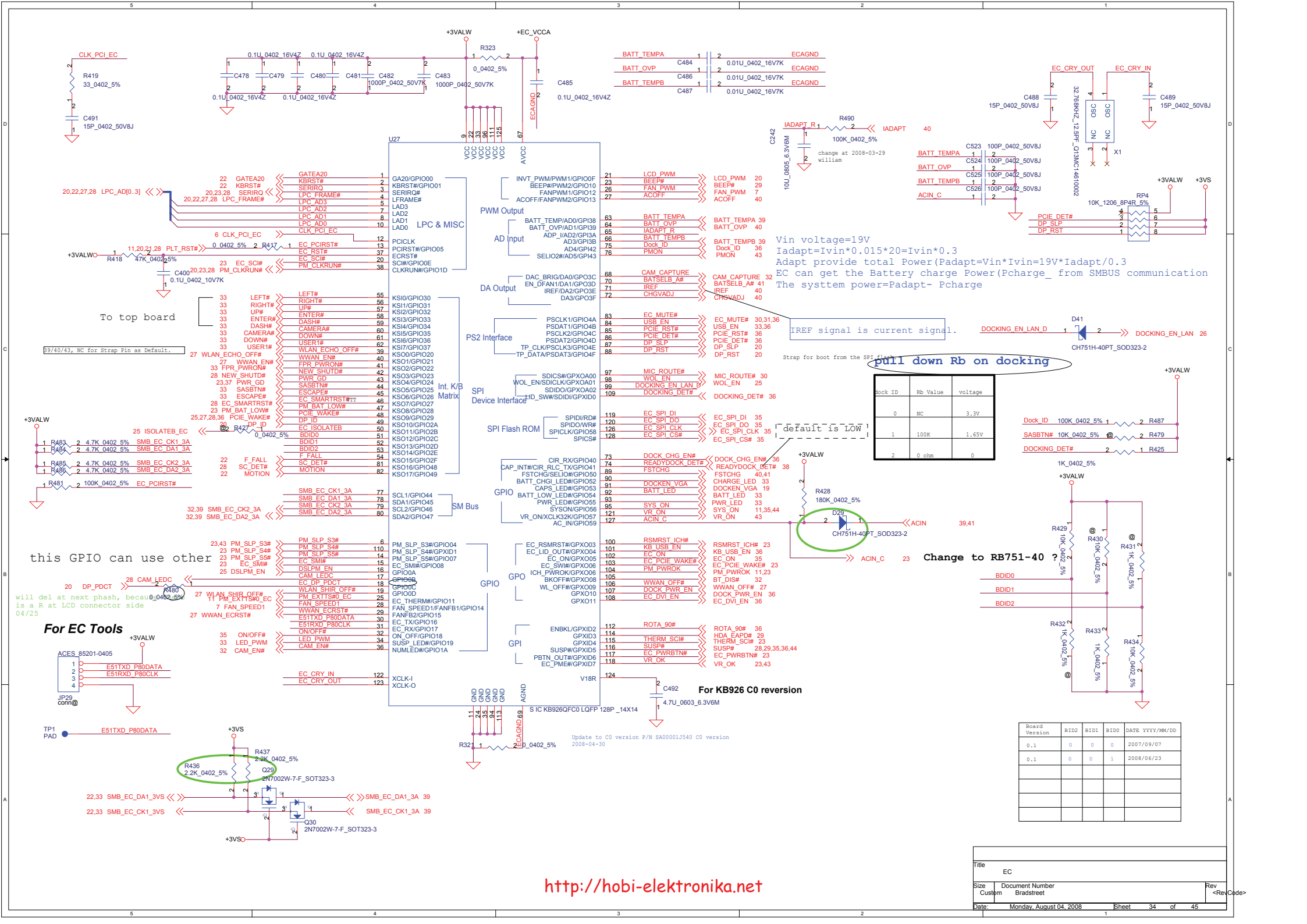


USB Port 1



http://hobi-elektronika.net

Title	FRP/IO/BTN/Wireless-SW	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 33 of 45	

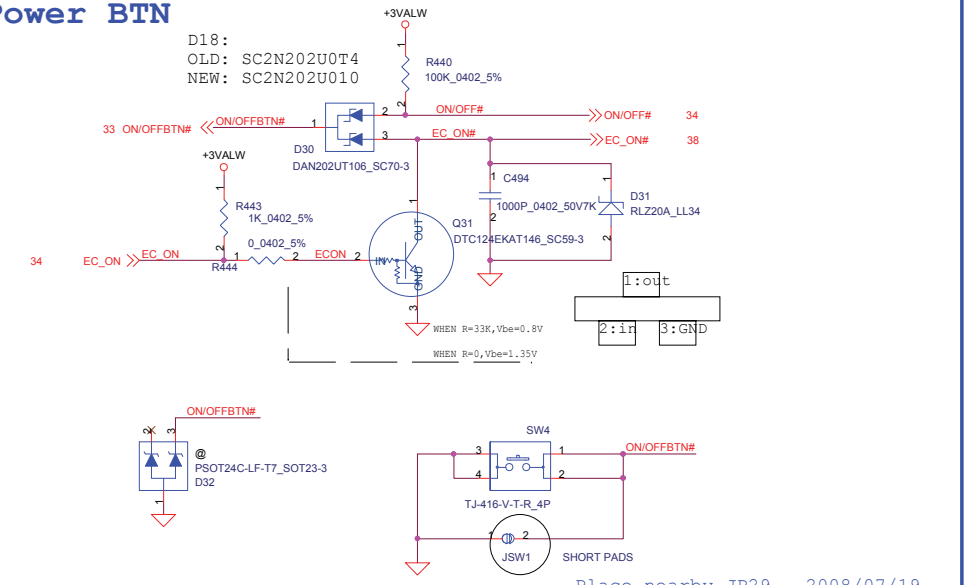


Dock ID	Rb Value	voltage
0	NC	3.3V
1	100K	1.65V
2	0 ohm	0

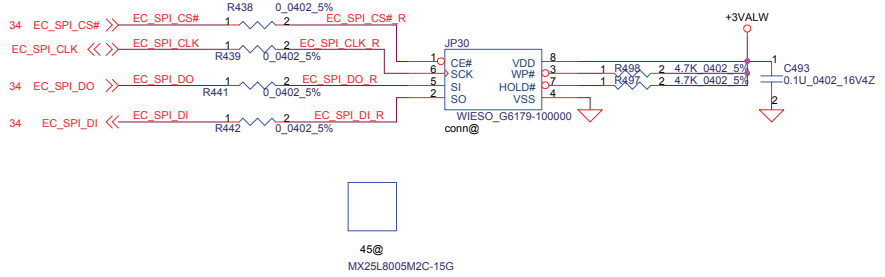
Board Version	BID2	BID1	BID0	DATE YYYY/MM/DD
0.1	0	0	0	2007/09/07
0.1	0	0	1	2008/06/23

Title	EC		
Size	Document Number		Rev
Custom	Bradstreet		<RevCode>
Date:	Monday, August 04, 2008	Sheet	34 of 45

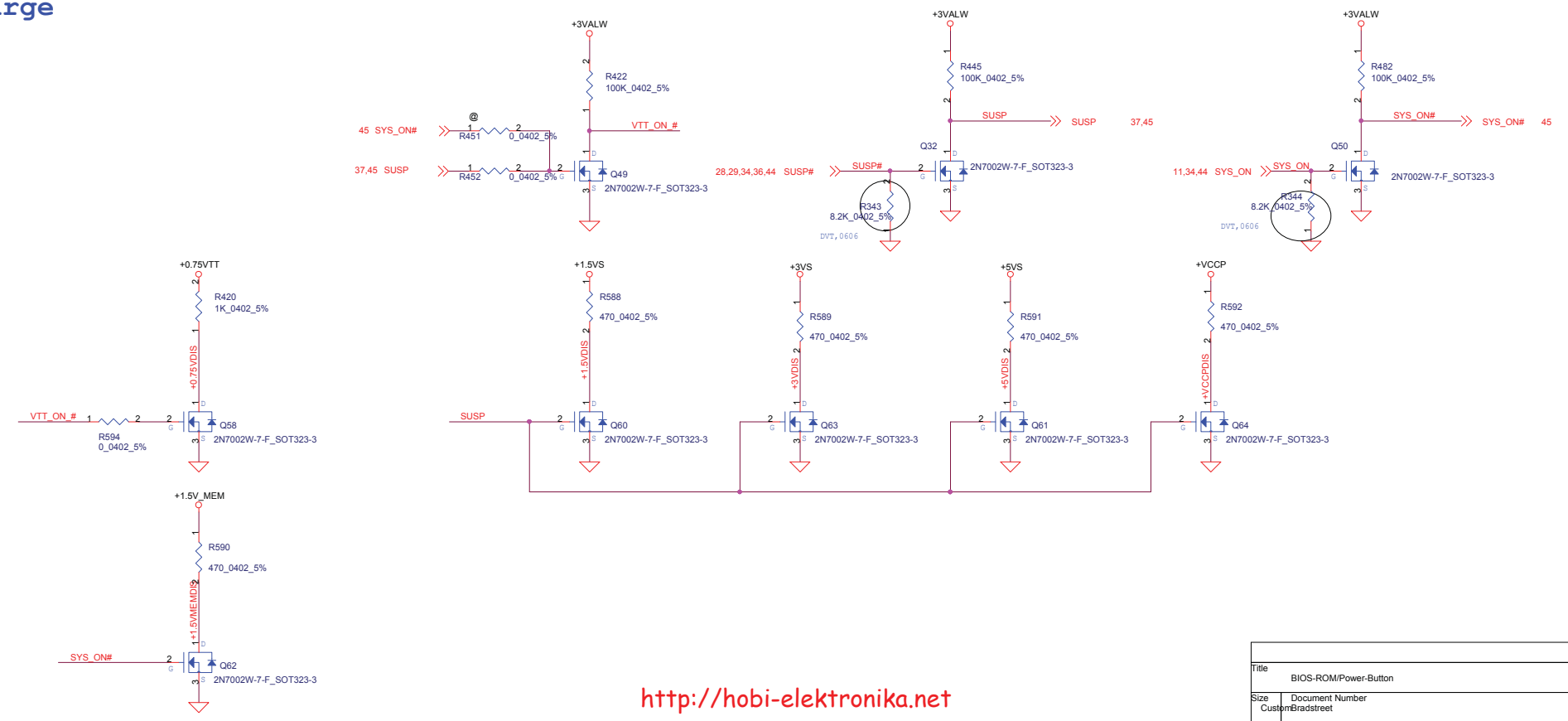
Power BTN



BIOS-ROM/SPI



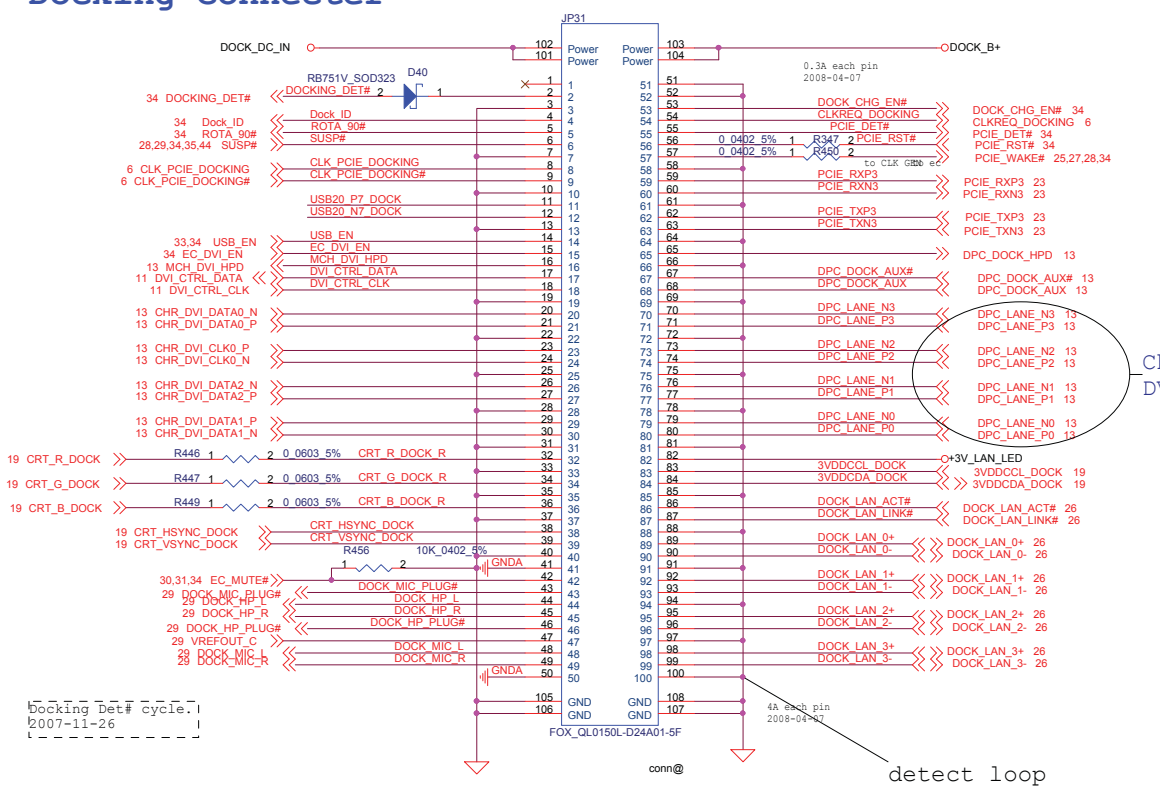
Discharge



http://hobi-elektronika.net

Title	BIOS-ROM/Power-Button	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 35 of 45	

Docking Connecter



Docking Det# cycle.
2007-11-26

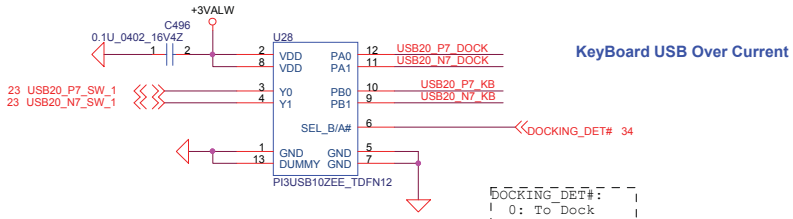
detect loop

Change the pin assignment
DVT, 0619

KeyBoard Connecter

Dock ON, ----------"0"
UN-PLUG,--------"1"
Pull high on Docking

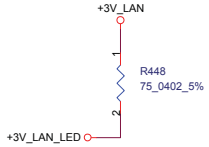
ESD DIODE will add on the Docking bridge board.

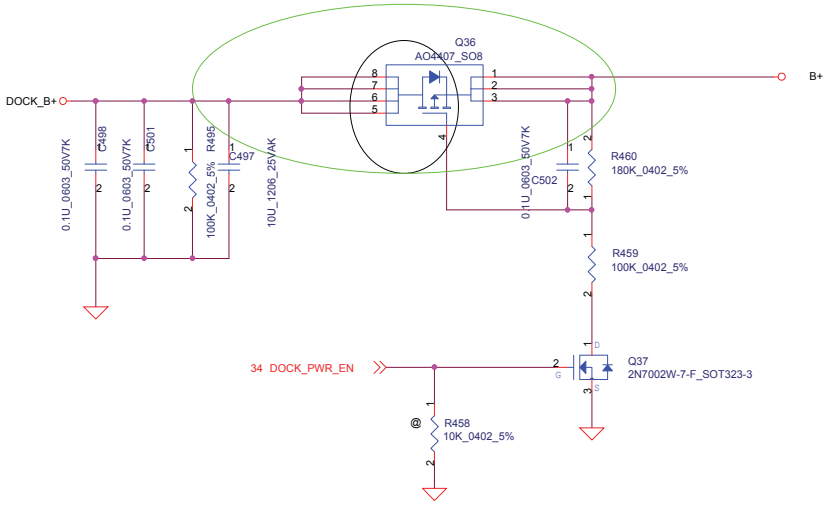


KeyBoard USB Over Current

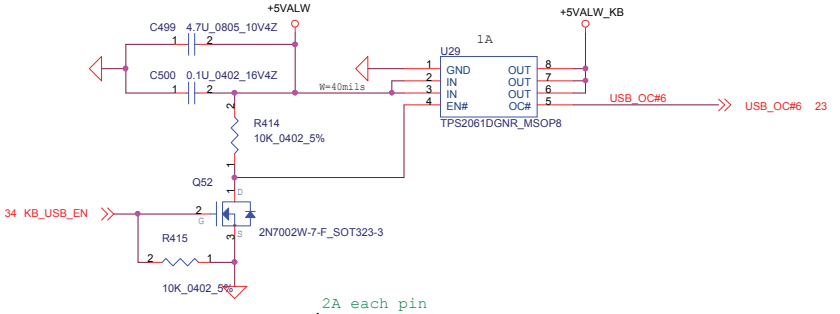
DOCKING_DET#:
0: To Dock
1: To KeyBoard
Default = 1

Add pull high?
12-26





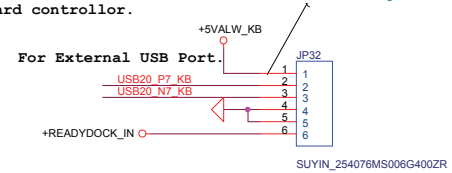
need change follow power's
suggestion
2007/12/19

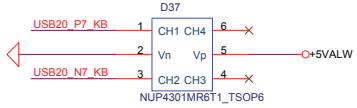


For Keyboard controllor.

2A each pin

For External USB Port.



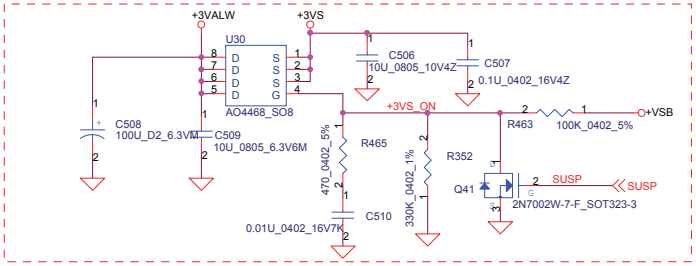


Pogo Connector

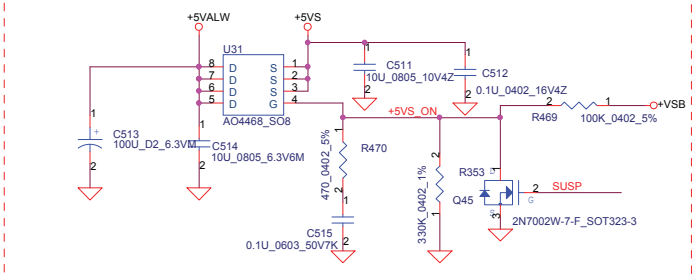
http://hobi-elektronika.net

Title: Dock Conn/Keyboard Conn			
Size: Custom	Document Number: Bradstreet		Rev: <RevCode>
Date: Monday, August 04, 2008		Sheet 36 of 45	

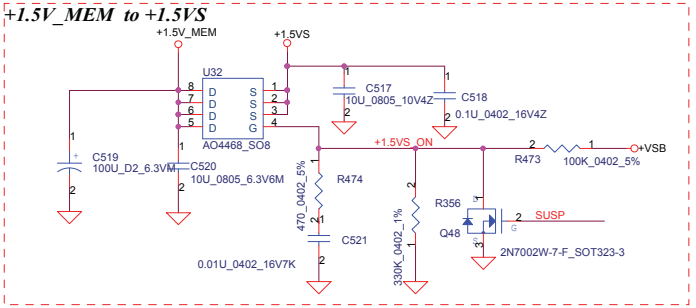
+3VALW to +3VS Transfer



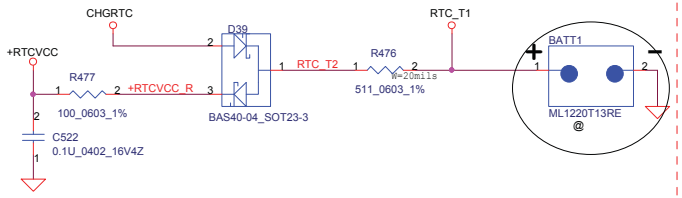
+5VALW to +5VS Transfer



+1.5V_MEM to +1.5VS

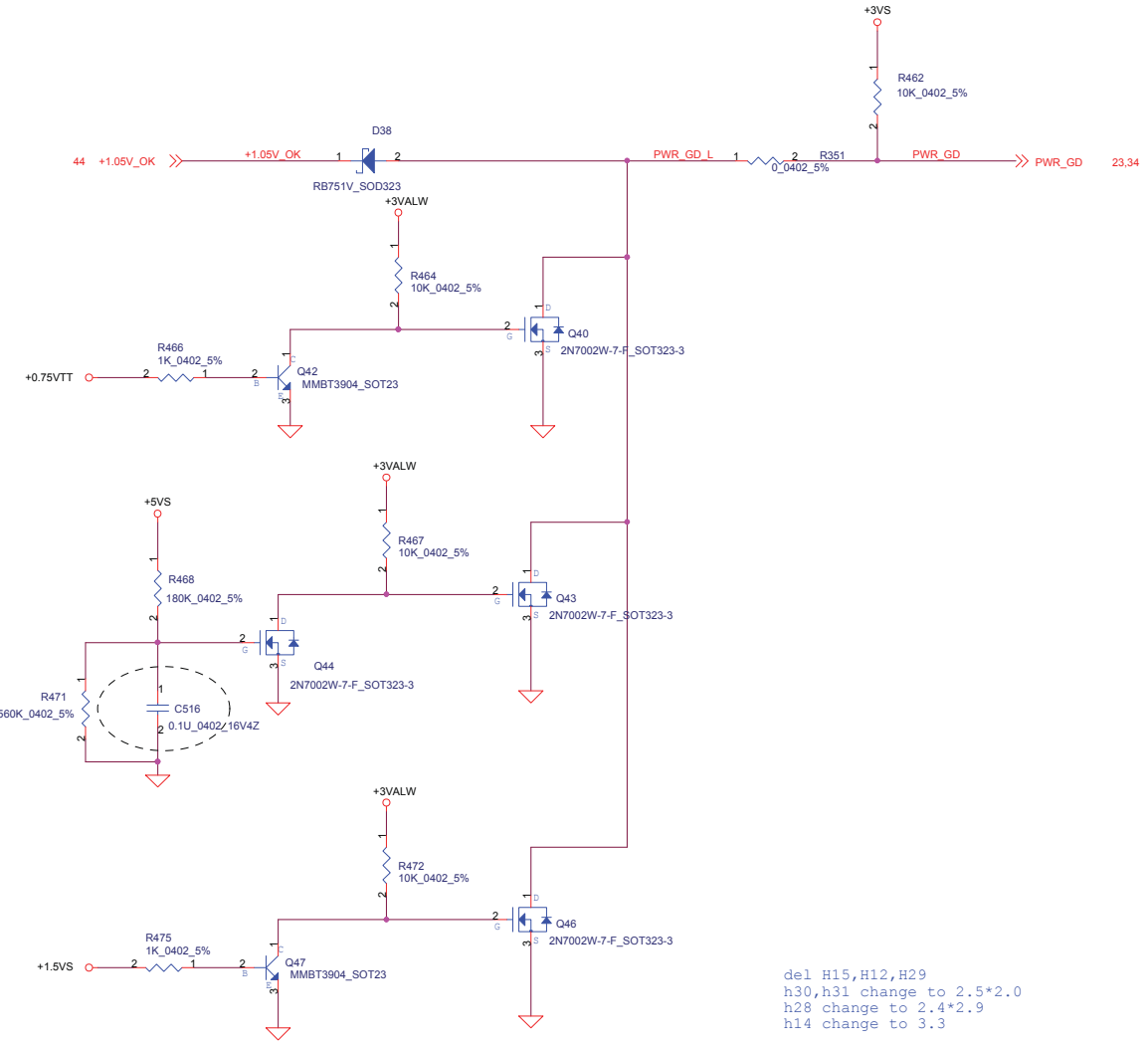


RTC



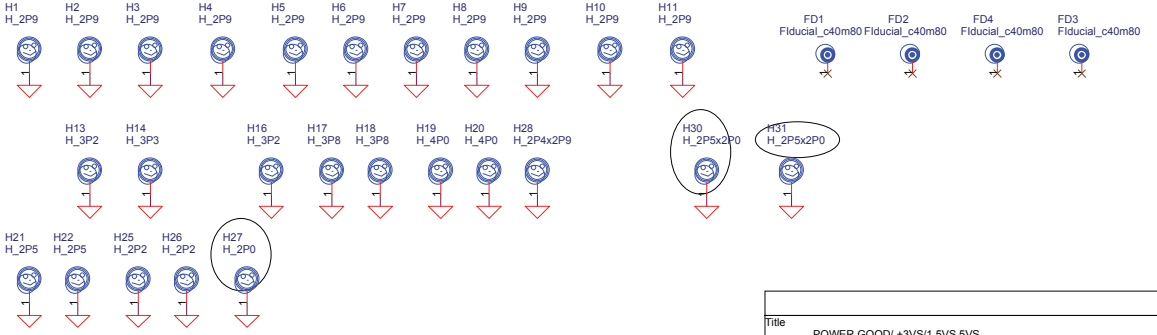
need update CIS symbol,
right now symbol is
MAXELL_ML1220T13RE_2P,
same with IGT30

35,45



del H15,H12,H29
h30,h31 change to 2.5*2.0
h28 change to 2.4*2.9
h14 change to 3.3

DVT, 06-12



http://hobi-elektronika.net

Title	POWER GOOD/ +3VS/1.5VS.5VS	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 37 of 45	

080315:DCjack P/N TBD

071031 ??update into SM010018210
(071010 Circuit PL1 ,PL2,PL3 SM010008E10)
080422: PL1 into SM010020720 for height limit
080712:PL1,PL3 from SM010020720 to SM010016410

DC301001M80

PJPDC1
SINGA_2DW-0005-B03
conn@

080416: Modify: PJP2---PJPDC1

DC_IN_S1 — PL1 — DC_IN_S2
FBMA-L11-322513-151LMA50T_1210

PC1 1000P_0402_50V7K
PC2 100P_0402_50V8J
PC3 1000P_0402_50V7K
PC4 100P_0402_50V8J

DC_IN
DOCK_DC_IN
B540C_SMC PD1
B540C_SMC PD2
VIN

+READYDOCK_IN
PD15 EC31QS04
PR190 340K_0402_1%
PR189 100K_0402_5%
PR128 100K_0402_5%
+3VALW
READYDOCK_DET#
PQ36 2N7002W-T/R7_SOT323-3
PQ37 2N7002W-T/R7_SOT323-3
PR198 100K_0402_5%
38W/50W#_Select 40

08-03-25 add reday docking ,I=2A, P=38W
080718:Ready dock ,CP=1.8A

BATT_A — PD3 RLS4148_LL34-2
BATT_B — PD5 RLS4148_LL34-2
PD4 RLS4148_LL34-2
1538VCC
PQ1 TP0610K-T1-E3_SOT23-3
PR1 68_1206_5%
PR2 68_1206_5%
PR3 200_0603_5%
CHGRTCP
N1
VS
PR4 100K_0402_1%
PC5 0.22U_1206_25V7K
PC6 0.1U_0603_25V7K
35 EC_ON#
PR5 22K_0402_1%

080319:update PJ1 into PJP15
080410:PD2 pop,
080410:update ready dock diode into small size SC11QS04000
080416: Modify: PR128 Pin1
+3.3VALW into +3VALW
080418: Del PJP15

RTCVREF
PR6 200_0603_5%
PR7 560_0603_5%
PR8 560_0603_5%
3.3V
PU1 G920AT24U_SOT89-3
OUT IN GND
N2
CHGRTC
PC7 10U_0805_10V4Z
PC8 1U_0805_25V4Z

PJP16 JUMP_43X118 — +3VALWP — +3VALW
(4.5A,180mils ,Via NO.= 9)

PJP17 JUMP_43X118 — +5VALWP — +5VALW
(4A,160mils ,Via NO.= 8)

PJP5 JUMP_43X39 — +VSBP — +VSB
(120mA,20mils ,Via NO.= 1)

PJP7 JUMP_43X118
PJP9 JUMP_43X118 — +1.05VSP — +VCCP
(8A,320mils ,Via NO.=16)

080409 William update by Power bugdet_Rev0.8 from Million.

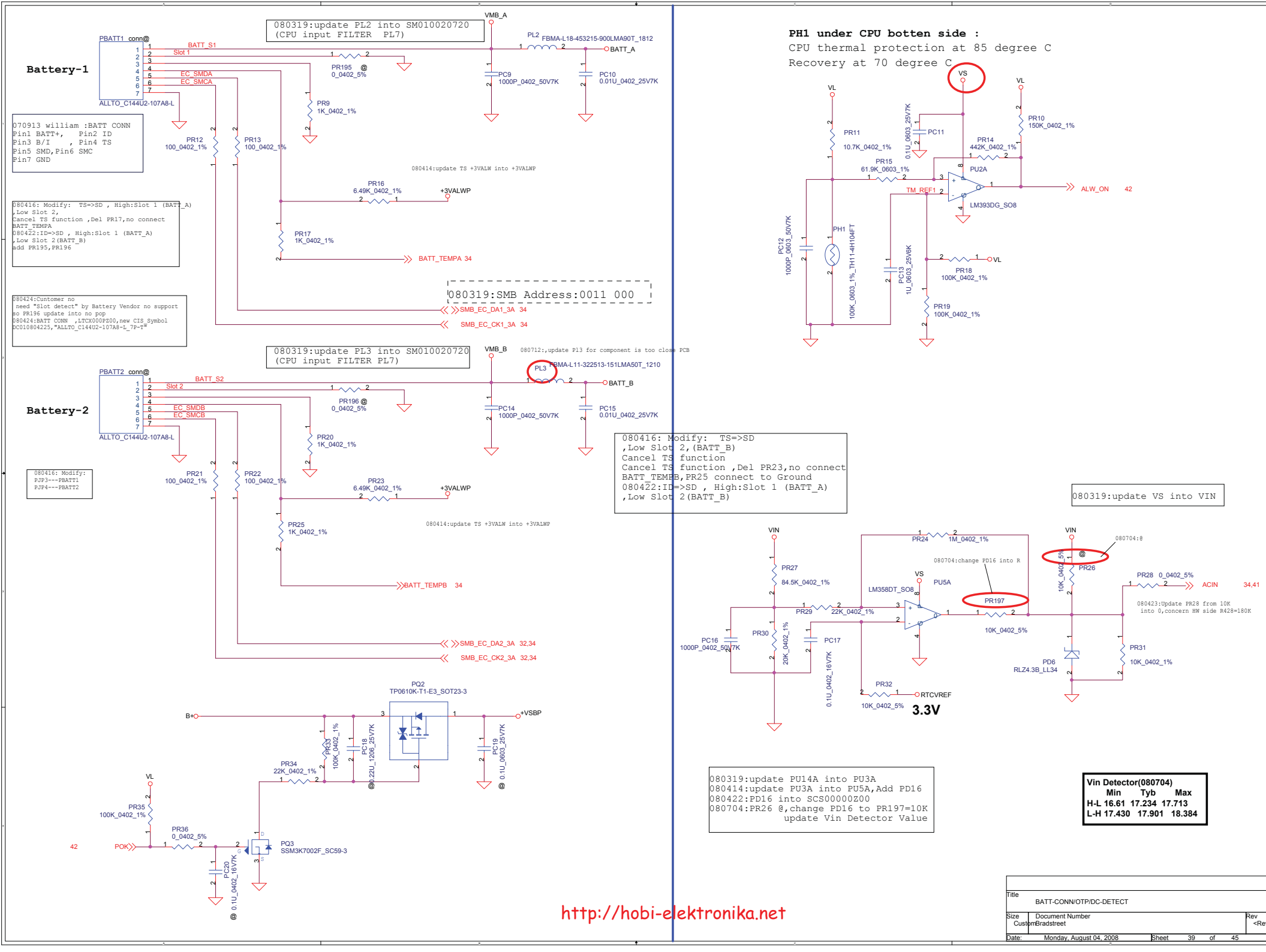
PJP18 JUMP_43X79 — +1.8VSP — +1.8VS
(1A,40mils ,Via NO.= 2)

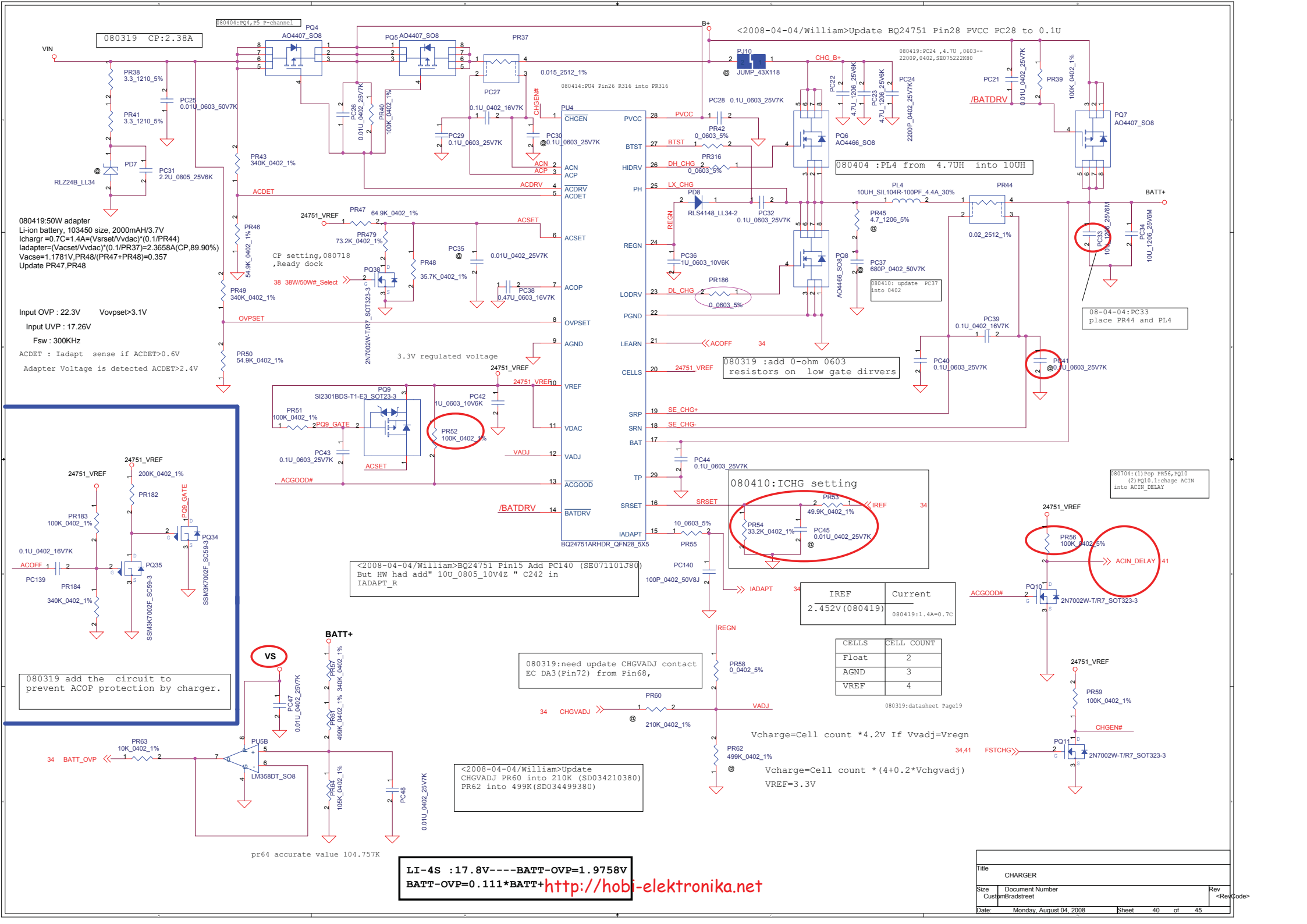
PJP6 JUMP_43X79 — +0.75VTTP — +0.75VTT
(1A,40mils ,Via NO.= 2)

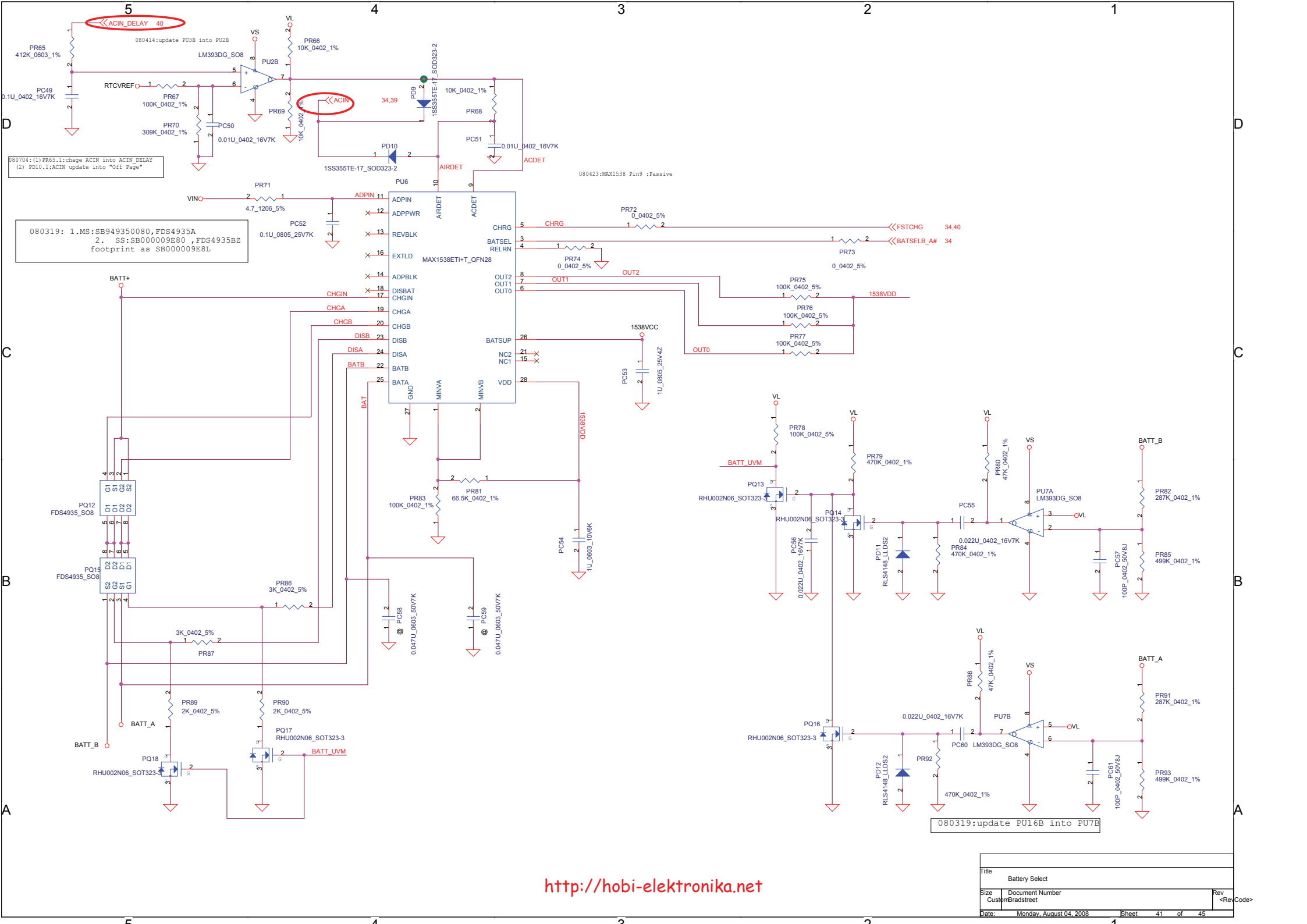
PJP10 JUMP_43X118
PJP8 JUMP_43X118 — +1.5VP — +1.5V_MEM
(8.0A,320mils ,Via NO.=16)

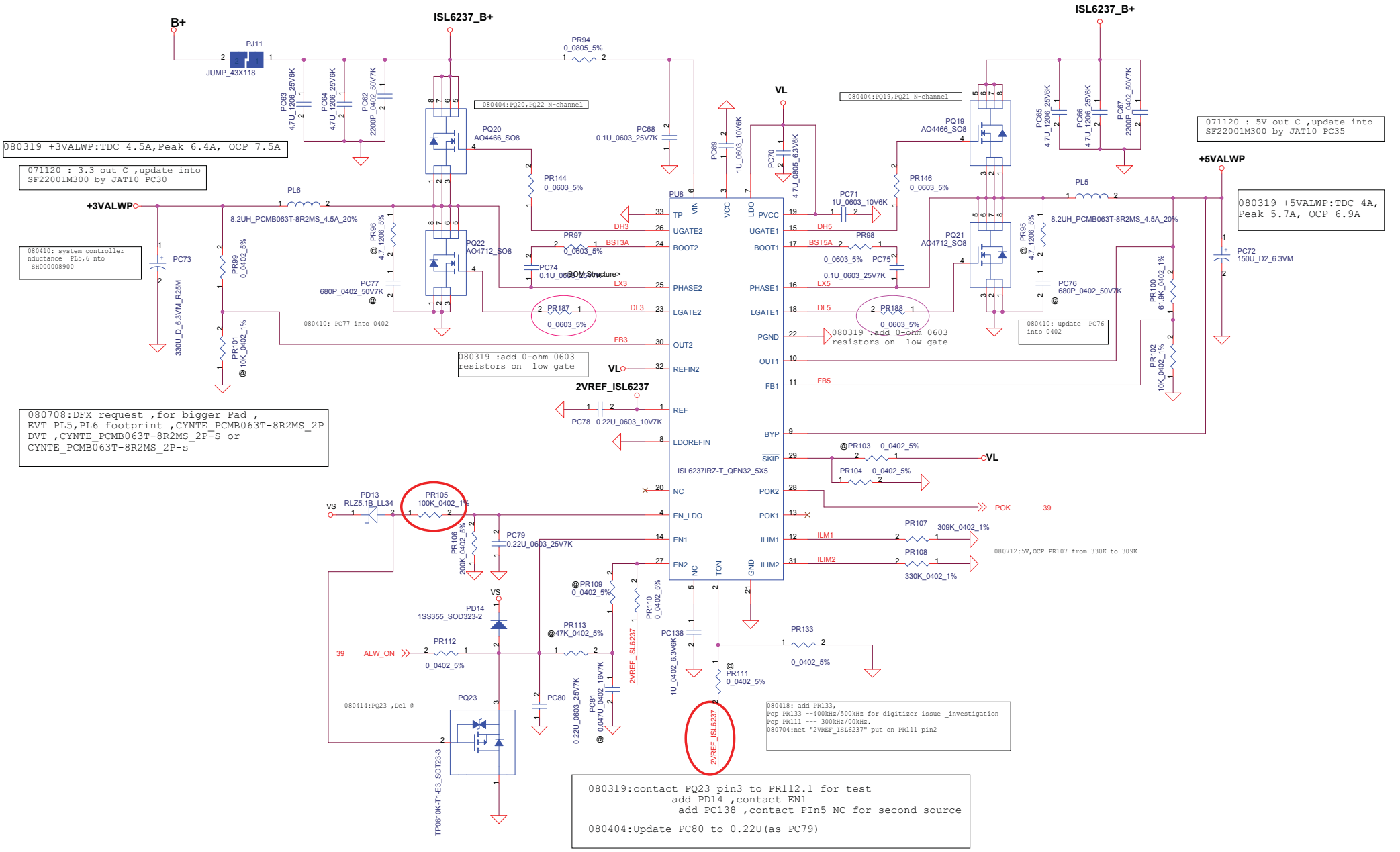
080319:update PJ. into PJP add PJP10,Del@

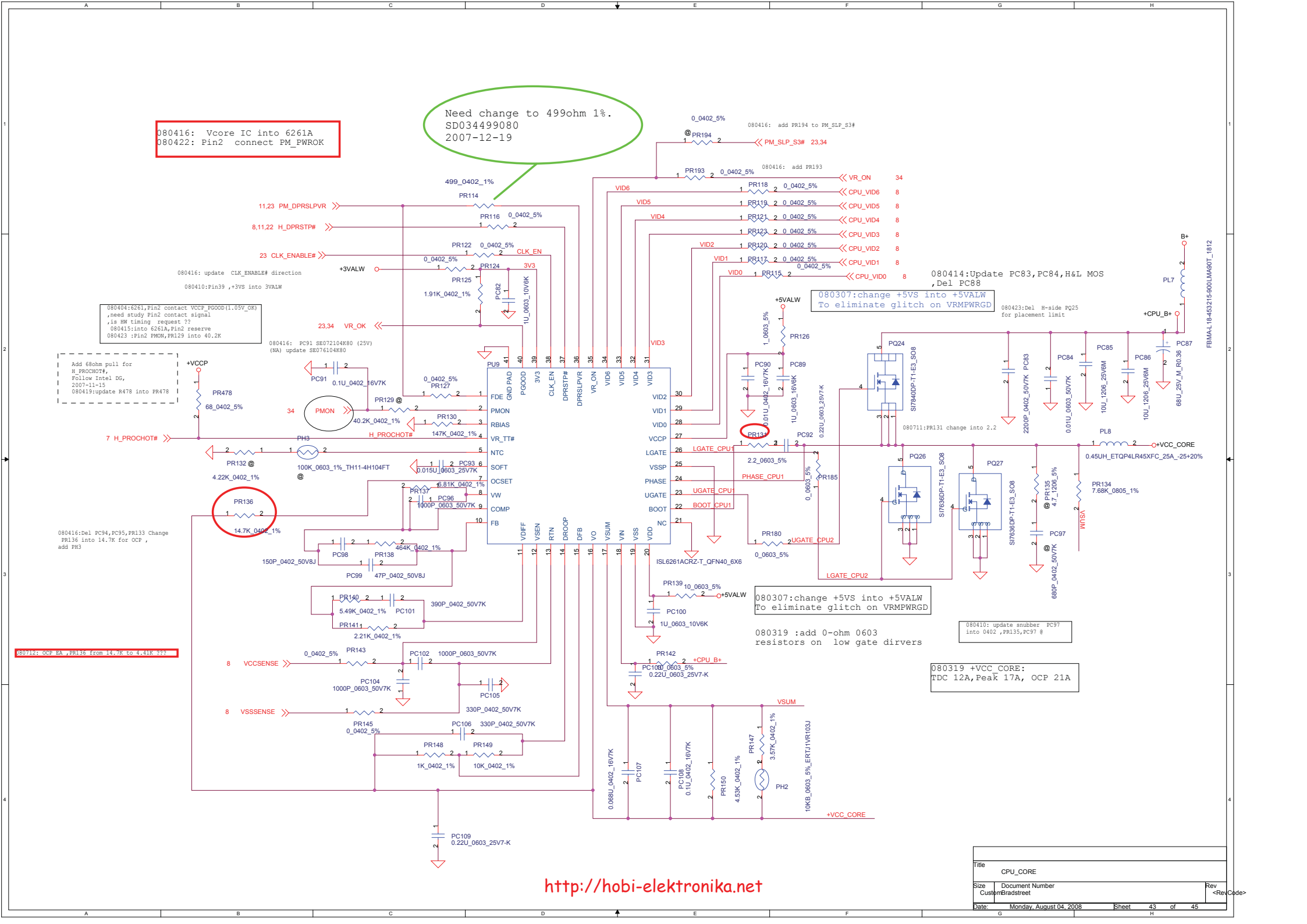
Title	DC-IN	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 38 of 45	

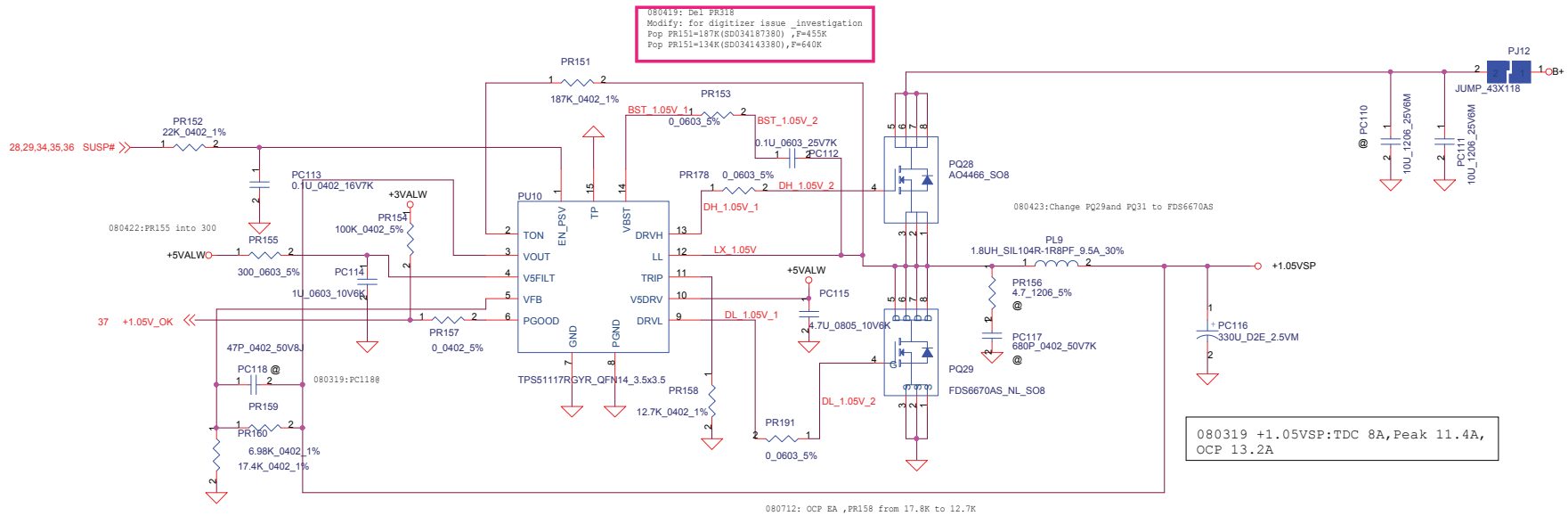

Battery-1
080319:update PL2 into SM010020720
(CPU input FILTER PL7)
PBATT1 conn@
ALLTO_C144U2-107A8-L
BATT_S1
Slot 1
EC_SMDA
EC_SMCA
VMB_A
PL2 FBMA-L18-453215-900LMA90T_1812
BATT_A
PR195 @ 0_0402_5%
PC9 1000P_0402_50V7K
PC10 0.01U_0402_25V7K
PR9 1K_0402_1%
PR12 100_0402_1%
PR13 100_0402_1%
070913 william :BATT CONN
Pin1 BATT+, Pin2 ID
Pin3 B/I , Pin4 TS
Pin5 SMD,Pin6 SMC
Pin7 GND
080414:update TS +3VALW into +3VALWP
PR16 6.49K_0402_1%
+3VALWP
080416: Modify: TS=>SD , High:Slot 1 (BATT_A)
,Low Slot 2,
Cancel TS function ,Del PR17,no connect
BATT_TEMPA
080422:ID=>SD , High:Slot 1 (BATT_A)
,Low Slot 2(BATT_B)
add PR195,PR196
PR17 1K_0402_1%
BATT_TEMPA 34
080319:SMB_Address:0011 000
SMB_EC_DA1_3A 34
SMB_EC_CK1_3A 34
080424:Cuntomer no
need "Slot detect" by Battery Vendor no support
so PR196 update into no pop
080424:BATT CONN ,LTCX000PZ00,new CIS Symbol
DC010804225,"ALLTO_C144U2-107A8-L_7P-T"
Battery-2
080319:update PL3 into SM010020720
(CPU input FILTER PL7)
PBATT2 conn@
ALLTO_C144U2-107A8-L
BATT_S2
Slot 2
EC_SMDB
EC_SMCB
VMB_B
080712:,update PL3 for component is too close PCB
PL3 FBMA-L11-322513-151LMA50T_1210
BATT_B
PR196 @ 0_0402_5%
PC14 1000P_0402_50V7K
PC15 0.01U_0402_25V7K
PR20 1K_0402_1%
PR21 100_0402_1%
PR22 100_0402_1%
080416: Modify:
PJP3---PBATT1
PJP4---PBATT2
PR23 6.49K_0402_1%
+3VALWP
080414:update TS +3VALW into +3VALWP
PR25 1K_0402_1%
BATT_TEMPB 34
080416: Modify: TS=>SD
,Low Slot 2,(BATT_B)
Cancel TS function
Cancel TS function ,Del PR23,no connect
BATT_TEMPB,PR25 connect to Ground
080422:ID=>SD , High:Slot 1 (BATT_A)
,Low Slot 2(BATT_B)
SMB_EC_DA2_3A 32,34
SMB_EC_CK2_3A 32,34
PQ2
TP0610K-T1-E3_SOT23-3
B+
+VSBP
PR33 100K_0402_1%
PC18 @0.22U_1206_25V7K
PC19 @ 0.1U_0603_25V7K
PR34 22K_0402_1%
VL
PR35 100K_0402_1%
PR36 0_0402_5%
42
POK
PQ3
SSM3K7002F_SC59-3
PC20 @ 0.1U_0402_16V7K
PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C
VS
VL
PR11 10.7K_0402_1%
PC11 0.1U_0603_25V7K
PR10 150K_0402_1%
PR14 442K_0402_1%
PR15 61.9K_0603_1%
PU2A
LM393DG_SO8
TM_REF1
ALW_ON 42
PC12 1000P_0603_50V7K
PH1
100K_0603_1%_TH11-4H104FT
PC13 1U_0603_25V6K
PR18 100K_0402_1%
PR19 100K_0402_1%
080319:update VS into VIN
VIN
PR24 1M_0402_1%
PR27 84.5K_0402_1%
080704:change PD16 into R
PU5A
LM358DT_SO8
PR197
PR29 22K_0402_1%
PR30 20K_0402_1%
PC16 1000P_0402_50V7K
PC17 0.1U_0402_16V7K
10K_0402_5%
PR26
080704:0
PR28 0_0402_5%
ACIN 34,41
080423:Update PR28 from 10K
into 0,concern HW side R428=180K
PD6 RLZ4.3B_LL34
PR31 10K_0402_1%
PR32 10K_0402_5%
RTCVREF
3.3V
080319:update PU14A into PU3A
080414:update PU3A into PU5A,Add PD16
080422:PD16 into SCS00000Z00
080704:PR26 @,change PD16 to PR197=10K
update Vin Detector Value
Vin Detector(080704)
Min Tyb Max
H-L 16.61 17.234 17.713
L-H 17.430 17.901 18.384
http://hobi-elektronika.net
Title
BATT-CONN/OTP/DC-DETECT
Size Custom
Document Number Bradstreet
Rev <RevCode>
Date: Monday, August 04, 2008
Sheet 39 of 45

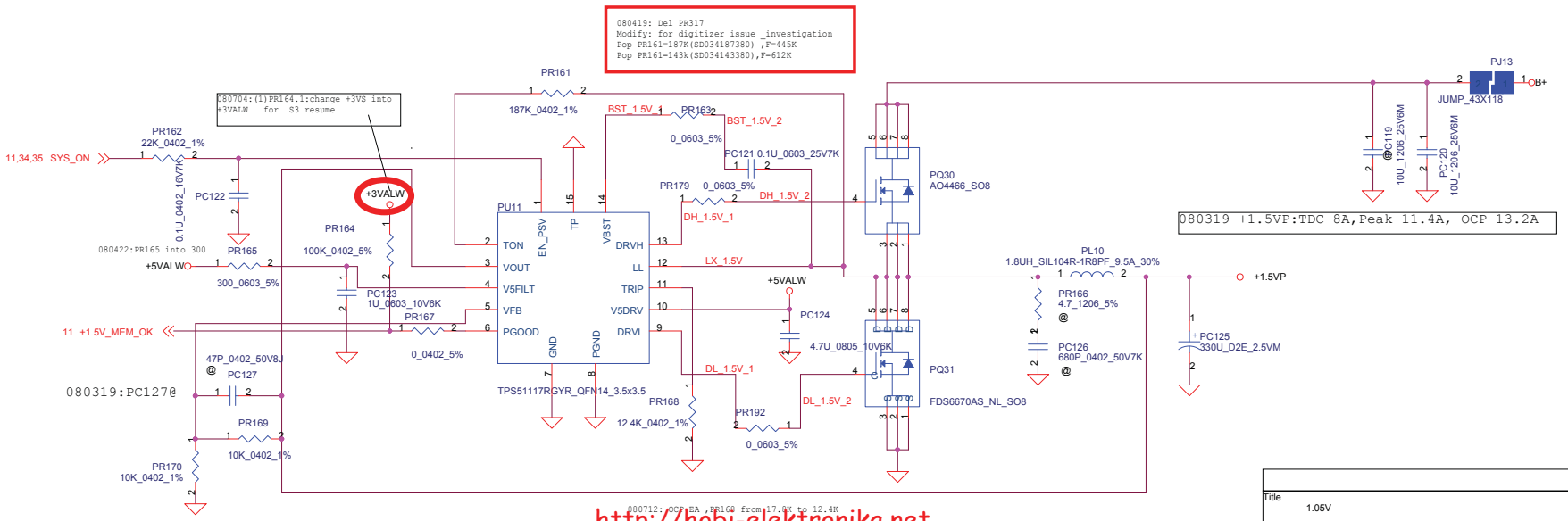

080319 CP:2.38A
080404:PQ4,P5 P-channel
PQ4 AO4407_SO8
PQ5 AO4407_SO8
VIN
PR38 3.3_1210_5%
PR41 3.3_1210_5%
PC25 0.01U_0603_50V7K
PD7 RLZ24B_LL34
PC31 2.2U_0805_25V6K
PR43 340K_0402_1%
PR46 54.9K_0402_1%
PR49 340K_0402_1%
PR50 54.9K_0402_1%
ACDET
OVPSET
080419:50W adapter
Li-ion battery, 103450 size, 2000mAH/3.7V
Ichargr =0.7C=1.4A=(Vsrset/Vvdac)*(0.1/PR44)
Iadapter=(Vacset/Vvdac)*(0.1/PR37)=2.3658A(CP,89.90%)
Vacse=1.1781V,PR48/(PR47+PR48)=0.357
Update PR47,PR48
Input OVP : 22.3V Vovpset>3.1V
Input UVP : 17.26V
Fsw : 300KHz
ACDET : Iadapt sense if ACDET>0.6V
Adapter Voltage is detected ACDET>2.4V
PR37
0.015_2512_1%
PC27 0.1U_0402_16V7K
PC26 0.01U_0402_25V7K
PR40 100K_0402_1%
PC29 0.1U_0603_25V7K
PC30 @0.1U_0603_25V7K
CHGEN#
ACN
ACP
ACDRV
080414:PU4 Pin26 R316 into PR316
PU4
CHGEN
PVCC
BTST
HIDRV
PH
LX_CHG
REGN
LODRV
PGND
LEARN
CELLS
SRP
SRN
BAT
TP
SRSET
IADAPT
ACDRV
ACDET
ACSET
ACOP
OVPSET
AGND
VREF
VDAC
VADJ
ACGOOD
BATDRV
BQ24751ARHDR_QFN28_5X5
24751_VREF
PR47 64.9K_0402_1%
PR479 73.2K_0402_1%
PR48 35.7K_0402_1%
PC35 @ 0.01U_0402_25V7K
PC38 0.47U_0603_16V7K
PQ38 2N7002W-T/R7_SOT323-3
38 38W/50W#_Select
CP setting,080718
,Ready dock
3.3V regulated voltage
PQ9 SI2301BDS-T1-E3_SOT23-3
PR51 100K_0402_1%
PQ9_GATE
PR52 100K_0402_1%
PC42 1U_0603_10V6K
PC43 0.1U_0603_25V7K
ACSET
ACGOOD#
/BATDRV
<2008-04-04/William>Update BQ24751 Pin28 PVCC PC28 to 0.1U
B+
PJ10 JUMP_43X118
CHG_B+
PC28 0.1U_0603_25V7K
PC22 4.7U_1206_25V6K
PC23 4.7U_1206_25V6K
PC24 2200P_0402_25V7K
080419:PC24 ,4.7U ,0603--
2200P,0402,SE075222K80
PC21 0.01U_0402_25V7K
PR39 100K_0402_1%
/BATDRV
PQ7 AO4407_SO8
PQ6 AO4466_SO8
PR42 0_0603_5%
PR316 0_0603_5%
080404 :PL4 from 4.7UH into 10UH
PD8 RLS4148_LL34-2
PC32 0.1U_0603_25V7K
PC36 1U_0603_10V6K
PR186 0_0603_5%
PL4 10UH_SIL104R-100PF_4.4A_30%
PR44 0.02_2512_1%
PR45 4.7_1206_5%
PQ8 AO4466_SO8
PC37 680P_0402_50V7K
080410: update PC37 into 0402
BATT+
PC33 10U_1206_25V6M
PC34 10U_1206_25V6M
08-04-04:PC33 place PR44 and PL4
PC39 0.1U_0402_16V7K
PC40 0.1U_0603_25V7K
PC41 @0.1U_0603_25V7K
080319 :add 0-ohm 0603 resistors on low gate dirvers
080410:ICHG setting
PR53 49.9K_0402_1%
IREF
PR54 33.2K_0402_1%
PC45 0.01U_0402_25V7K
PC44 0.1U_0603_25V7K
SRSET
10_0603_5%
PR55
PC140 100P_0402_50V8J
IADAPT
080704:(1)Pop PR56,PQ10
(2)PQ10.1:chage ACIN into ACIN_DELAY
24751_VREF
PR56 100K_0402_5%
ACIN_DELAY 41
PQ10 2N7002W-T/R7_SOT323-3
ACGOOD#
IREF Current
2.452V(080419) 080419:1.4A=0.7C
CELLS CELL COUNT
Float 2
AGND 3
VREF 4
080319:datasheet Page19
<2008-04-04/William>BQ24751 Pin15 Add PC140 (SE071101J80)
But HW had add" 10U_0805_10V4Z " C242 in
IADAPT_R
080319:need update CHGVADJ contact
EC DA3(Pin72) from Pin68,
PR58 0_0402_5%
PR60 @ 210K_0402_1%
CHGVADJ
VADJ
Vcharge=Cell count *4.2V If Vvadj=Vregn
PR62 499K_0402_1%
Vcharge=Cell count *(4+0.2*Vchgvadj)
VREF=3.3V
24751_VREF
PR59 100K_0402_1%
CHGEN#
PQ11 2N7002W-T/R7_SOT323-3
FSTCHG
24751_VREF
200K_0402_1%
PR182
PR183 100K_0402_1%
PQ9_GATE
PQ34 SSM3K7002F_SC59-3
0.1U_0402_16V7K
ACOFF
PC139
PQ35 SSM3K7002F_SC59-3
PR184 340K_0402_1%
080319 add the circuit to
prevent ACOP protection by charger.
VS
BATT+
PC47 0.01U_0402_25V7K
PR63 10K_0402_1%
BATT_OVP
PU5B LM358DT_SO8
PR64 105K_0402_1%
PR61 499K_0402_1%
PR67 340K_0402_1%
PC48 0.01U_0402_25V7K
pr64 accurate value 104.757K
LI-4S :17.8V----BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+
http://hobi-elektronika.net
Title CHARGER
Size Custom
Document Number Bradstreet
Rev <RevCode>
Date: Monday, August 04, 2008
Sheet 40 of 45


ACIN_DELAY 40
080414:update PU3B into PU2B
PR65 412K_0603_1%
PC49 0.1U_0402_16V7K
RTCVREF
PR67 100K_0402_1%
PR70 309K_0402_1%
PC50 0.01U_0402_16V7K
LM393DG_SO8
PU2B
VS
VL
PR66 10K_0402_1%
PR69 10K_0402_1%
ACIN
34,39
PD9 1SS355TE-17_SOD323-2
PR68 10K_0402_1%
PC51 0.01U_0402_16V7K
ACDET
PD10 1SS355TE-17_SOD323-2
AIRDET
080704:(1)PR65.1:chage ACIN into ACIN_DELAY
(2) PD10.1:ACIN update into "Off Page"
080423:MAX1538 Pin9 :Passive
PU6
PR71 4.7_1206_5%
VIN
ADPIN
PC52 0.1U_0805_25V7K
ADPPWR
REVBLK
EXTLD
MAX1538ETI+T_QFN28
ADPBLK
DISBAT
CHGIN
CHGA
CHGB
DISB
DISA
BATB
BATA
GND
MINVA
MINVB
CHRG
BATSEL
RELRN
BATSUP
NC2
NC1
VDD
PR72 0_0402_5%
CHRG
FSTCHG 34,40
PR73 0_0402_5%
BATSELB_A# 34
PR74 0_0402_5%
OUT2
OUT1
OUT0
PR75 100K_0402_5%
PR76 100K_0402_5%
PR77 100K_0402_5%
1538VDD
1538VCC
PC53 1U_0805_25V4Z
080319: 1.MS:SB949350080,FDS4935A
2. SS:SB000009E80 ,FDS4935BZ
footprint as SB000009E8L
BATT+
BAT
PQ12 FDS4935_SO8
PQ15 FDS4935_SO8
PR81 66.5K_0402_1%
PR83 100K_0402_1%
PC54 1U_0603_10V6K
PR86 3K_0402_5%
3K_0402_5%
PR87
PC58 @ 0.047U_0603_50V7K
PC59 @ 0.047U_0603_50V7K
PR89 2K_0402_5%
PR90 2K_0402_5%
BATT_A
BATT_B
PQ17 RHU002N06_SOT323-3
PQ18 RHU002N06_SOT323-3
BATT_UVM
PR78 100K_0402_5%
PR79 470K_0402_1%
PQ13 RHU002N06_SOT323-3
PQ14 RHU002N06_SOT323-3
PR80 47K_0402_1%
PU7A LM393DG_SO8
PC55 0.022U_0402_16V7K
PR84 470K_0402_1%
PC56 0.022U_0402_16V7K
PD11 RLS4148_LLDS2
PC57 100P_0402_50V8J
PR82 287K_0402_1%
PR85 499K_0402_1%
PR88 47K_0402_1%
PU7B LM393DG_SO8
PC60 0.022U_0402_16V7K
PQ16 RHU002N06_SOT323-3
PR92 470K_0402_1%
PD12 RLS4148_LLDS2
PC61 100P_0402_50V8J
PR91 287K_0402_1%
PR93 499K_0402_1%
080319:update PU16B into PU7B
http://hobi-elektronika.net
Title
Battery Select
Size
Custom
Document Number
Bradstreet
Rev
<RevCode>
Date:
Monday, August 04, 2008
Sheet
41
of
45

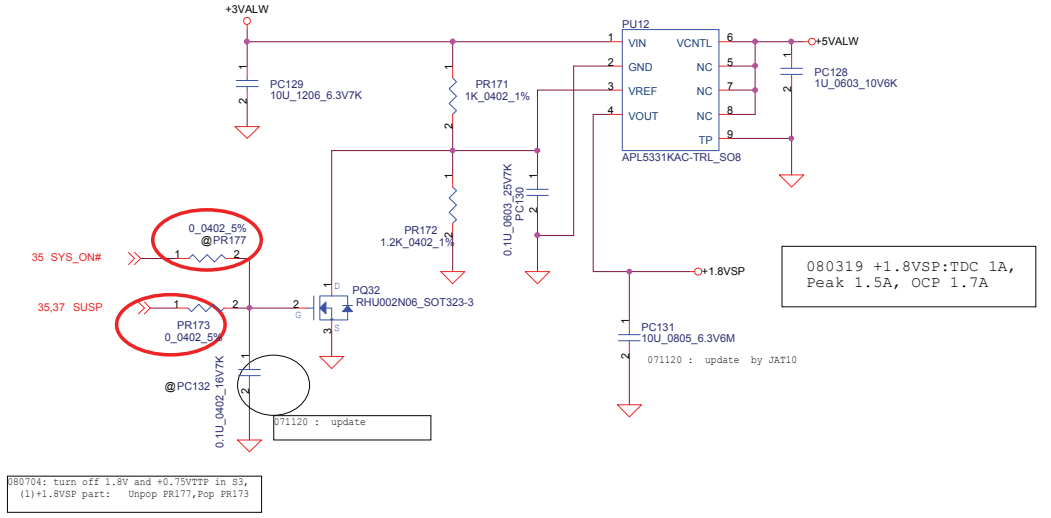

B+
ISL6237_B+
VL
+3VALWP
+5VALWP
2VREF_ISL6237
080319 +3VALWP:TDC 4.5A,Peak 6.4A, OCP 7.5A
071120 : 3.3 out C ,update into SF22001M300 by JAT10 PC30
071120 : 5V out C ,update into SF22001M300 by JAT10 PC35
080319 +5VALWP:TDC 4A, Peak 5.7A, OCP 6.9A
080404:PQ20,PQ22 N-channel
080404:PQ19,PQ21 N-channel
080319 :add 0-ohm 0603 resistors on low gate
080410: update PC76 into 0402
080410: PC77 into 0402
080708:DFX request ,for bigger Pad , EVT PL5,PL6 footprint ,CYNTE_PCMB063T-8R2MS_2P DVT ,CYNTE_PCMB063T-8R2MS_2P-S or CYNTE_PCMB063T-8R2MS_2P-s
ISL6237IRZ-T_QFN32_5X5
080712:5V,OCP PR107 from 330K to 309K
080414:PQ23 ,Del @
080418: add PR133, Pop PR133 --400kHz/500kHz for digitizer issue _investigation Pop PR111 --- 300kHz/00kHz. 080704:net "2VREF_ISL6237" put on PR111 pin2
080319:contact PQ23 pin3 to PR112.1 for test
add PD14 ,contact EN1
add PC138 ,contact PIn5 NC for second source
080404:Update PC80 to 0.22U(as PC79)
http://hobi-elektronika.net
Title 3VALW/5VALW
Size Custom
Document Number Bradstreet
Rev <RevCode>
Date: Monday, August 04, 2008
Sheet 42 of 45

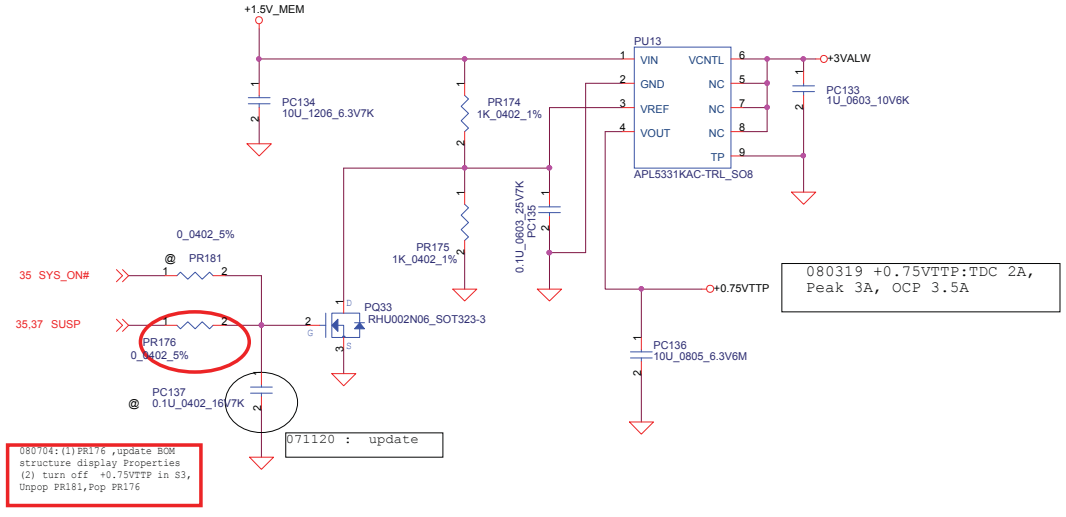

080416: Vcore IC into 6261A
080422: Pin2 connect PM_PWROK
Need change to 499ohm 1%.
SD034499080
2007-12-19
080414:Update PC83,PC84,H&L MOS ,Del PC88
080307:change +5VS into +5VALW To eliminate glitch on VRMPWRGD
080319 :add 0-ohm 0603 resistors on low gate dirvers
080319 +VCC_CORE: TDC 12A,Peak 17A, OCP 21A
080712: OCP EA ,PR136 from 14.7K to 4.41K ???
080416:Del PC94,PC95,PR133 Change PR136 into 14.7K for OCP , add PH3
080410: update snubber PC97 into 0402 ,PR135,PC97 @
http://hobi-elektronika.net
Title CPU_CORE
Size Custom
Document Number Bradstreet
Rev <RevCode>
Date: Monday, August 04, 2008
Sheet 43 of 45





Title	1.05V	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 44 of 45	





Title	<Title>	
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, August 04, 2008	Sheet 45 of 45	

Change List ~ 1

Items	Page	Title	Date	Request Owner	Issue Description and Solution Description	Version
1	P7	CPU thermal sensor SMBus	2008/05/14	Compal/Kaberl	change CPU thermal(U3) sensor to SMB_EC2 follow Compal common design	X 0.2
2	P8/14	change C33 C101 PN	2008/05/14	Compal/Ice	change the C33 C101 from SGA19331D20 to SGA19331D10 becasue the high limitation	X 0.2
3	P35	add pull down at SUSP# and SYSON	2008/05/14	Compal/Ice	VS power will auto up when plug AC adapter, it will cause the LED auto flash, so add pull down R343 and R344 to discharge the power on SUSP# and SYSON	X 0.2
4	P23	ICH GPIO10 pull up Resistor	2008/06/06	Compal/Ice	the power of ICH GPIO10 is SUSPEND, so the pull high R should be +3VALW, change R248 pull high to +3VALW	X 0.2
5	P7	update Fan schematic	2008/06/06	Compal/Ice	change FAN schematic based the FAN type,Del Q1,R4,C32,D1,R95,add U25	X 0.2
6	P34	EC GPIO	2008/06/14	Compal/Kaber	change EC GPIO to follow Compal common design pin 39 to WLAN_ECHO_OFF#, pin62 to USER1#, add D43,Pin 34 => LED_PWM Pin 27 =>AC_OFF Pin 68 => CAM_CAPTURE	X 0.2
7	P34	EC GPIO	2008/06/26	Montion/ID	delet USER button 2 because ID change	X 0.2
8	P23	power switch	2008/06/27	Compal ice	change FPR,WWAN,and Camera power control swith to AO1320,For WWAN, add U43,Q34, CAM add U44,C404, FPR, add U45	X 0.2
9	P34	DOCK_CHG_EN#	2008/06/27	power william	this signal is high active,so change it from DOCK_CHG_EN# to DOCK_CHG_EN	X 0.2
10	P34	EC_DVI_EN#	2008/06/27	Compal/Ice	this signal is high active,so change it from EC_DVI_EN# to EC_DVI_EN	X 0.2
11	P34	DC-DC MOS Gate voltage	2008/06/27	Compal/Ice	U30,U31,U32 gate is pull high to +VSB, it is 19V and may destroy the DC-DC Mos, so add R352,R353,R354 to reduce gate voltage	X 0.2
12	P23	ICH PCIE port	2008/07/01	BIOS/Nash	if disable port 0, the other ports will also be disabled, follow BIOS suggestion, exchange port 1 and port 5	X 0.2
13	P34	PM_SLP_S3#	2008/07/01	Compal/Ice	Add a 0 ohm Resistor on the net PM_SLP_S3# for HW signal test, add R350	X 0.2
14	P13	MCH_DVI_HPD	2008/07/03	Compal/Ice	reserve 0 ohm Resistor R96 on the net MCH_DVI_HPD for the new leve shift of DVI	X 0.2
15	P23	ICH PCIE port	2008/07/16	BIOS/Nash	follow BIOS/Motion suggestion, change port 1 to GLAN, and port3 to dock	X 0.2
16	P23	Add NEW_SHUTD#	2008/07/16	Motion	follow customer require add NEW_SHUTD# for save the power	X 0.2
17	P13	ICH GPIO	2008/07/17	Compal/Ice	because the GPIO power is +3vs, but EXPRESS_DET# need pull high to 3VALW, so change EXPRESS_DET# to GPIO56, and GPIO48 change pull high to +3VS	X 0.2

Title	<Title>	
Size: Custom	Document Number <Doc>	Rev <RevCode>
Date: Monday, August 04, 2008	Sheet 46 of 46	