

LA-1811

Compal confidential

Schematics Document

**DT TRANSPORT or Prescott uFCPGA
with ATI-RC300M+SB200 core logic**

2003-09-01

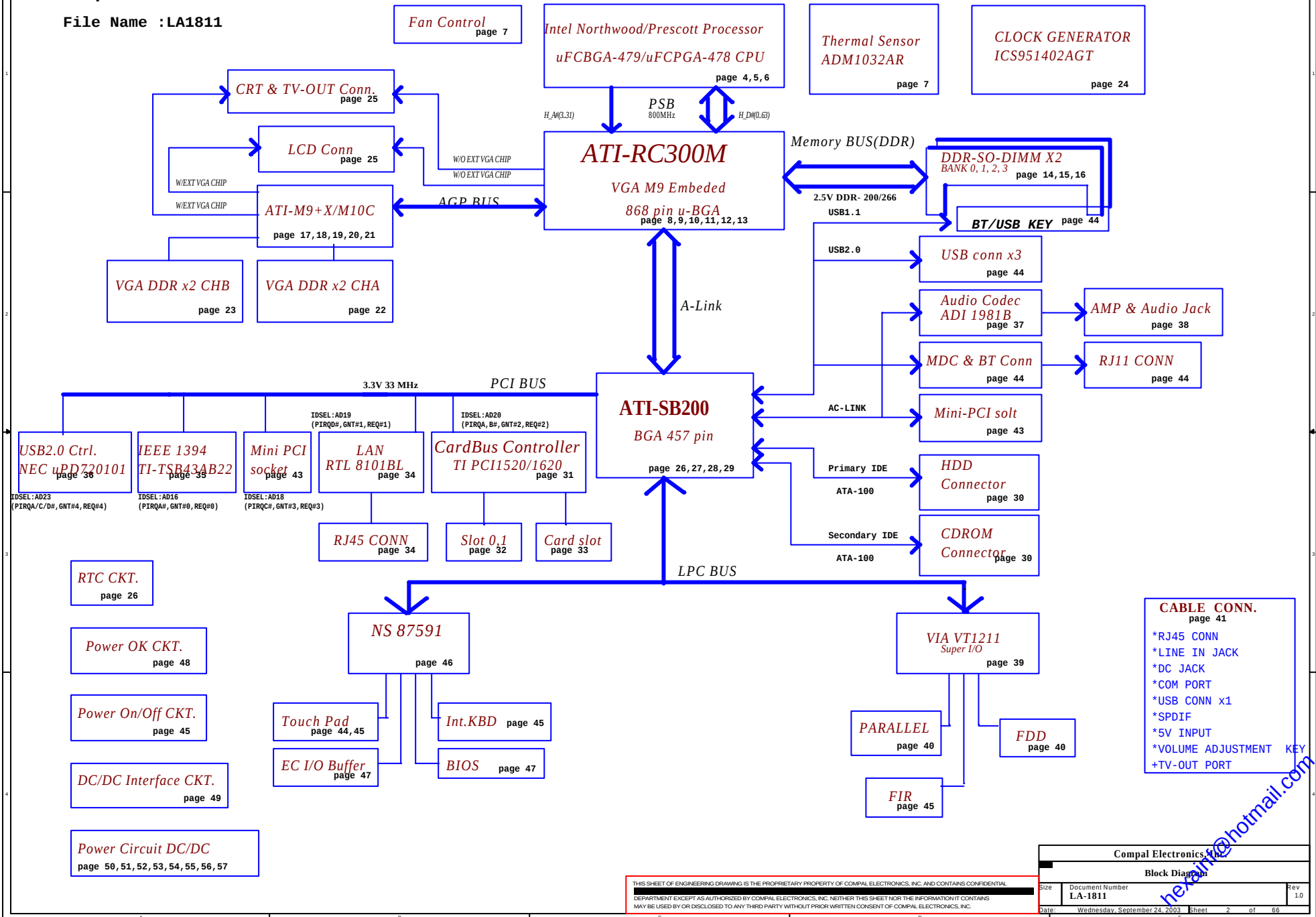
REV:1.0

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL
INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.	
Cover Sheet	
Size	Document Number
	LA-1811
Date	Wednesday, September 24, 2003
Sheet	1 of 66
Rev	1.0

Compal confidential

File Name :LA1811



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
Block Diagram		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 2 of 66

Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCVID	The voltage for Processor VID select	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.2VS_VGA	1.2V I/O power rail for ATI-VGA M9+X/M10P.	ON	OFF	OFF
+1.5VS	1.5V I/O power rail for ATI-RS300M/RC300M NB AGP.	ON	OFF	OFF
+1.8VS	1.8V switched power rail for ATI-RS300M/RC300M NB.	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V system power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V system power rail for SB,LAN,CardReader and HUB.	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V system power rail .	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
AGP BUS	AGP_DEVSEL	N/A	A
SOUTHBRIDGE	AD31 (INT.)	N/A	N/A
USB	AD30 (INT.)	N/A	D
AC97	AD31 (INT.)	N/A	B
ATA 100	AD31 (INT.)	N/A	A
ETHERNET	AD24(INT.)	N/A	C
1394	AD16	0	A
LAN	AD19	1	D
CARD BUS	AD20	2	A,B
Wireless LAN(MINI PCI)	AD18	3	C
EXT USB	AD23(EXT.)	4	A,C,D

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

NAGP@ : means just build when no external AGP VGA chip build in (UMA).

M10@ : means build VGA M10

M9@ : means build VGA M9+X

M9-M10@ : means build VGA M9 or M10

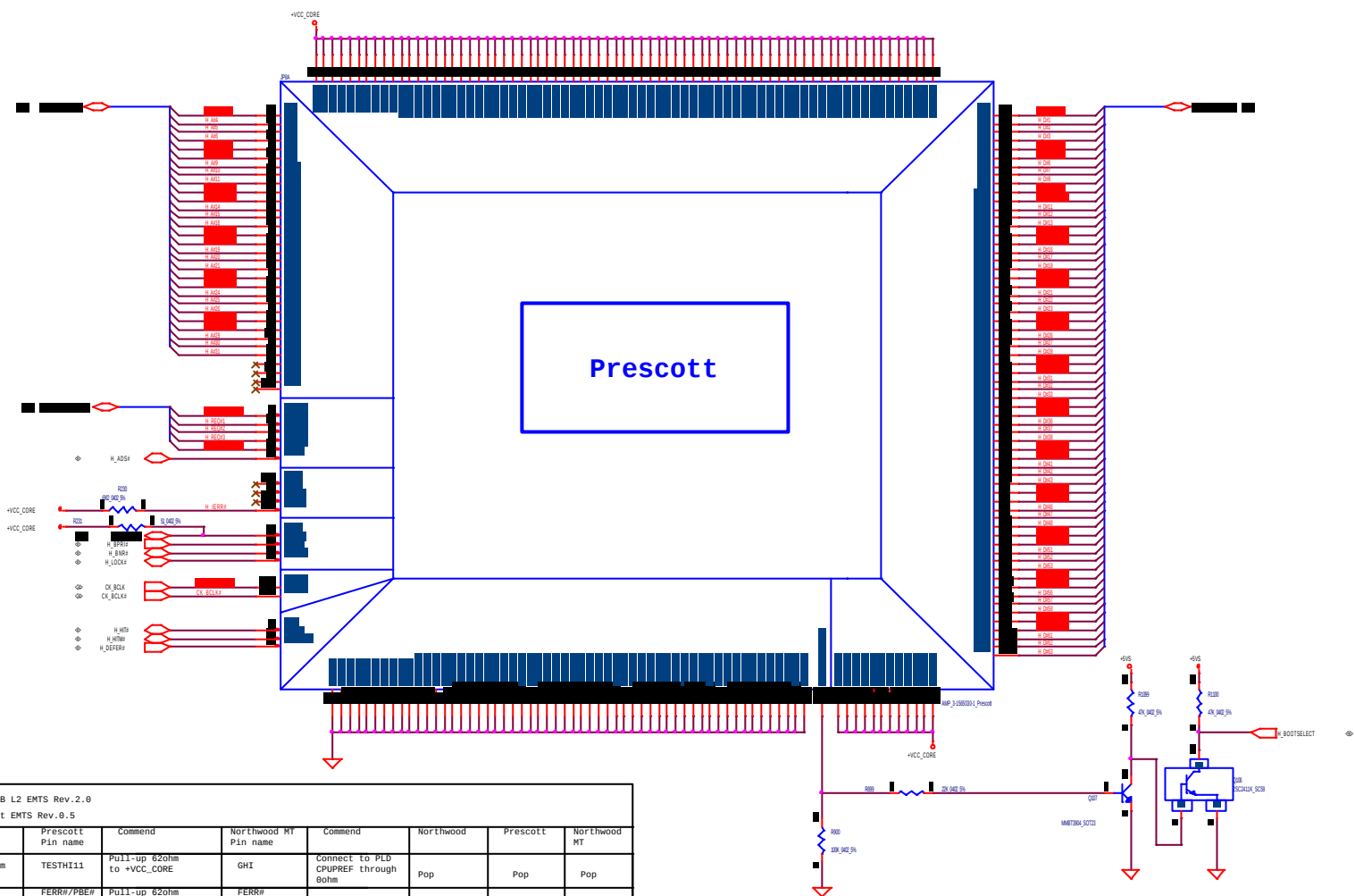
1520@ : means build Cardbus PCI1520

1620@ : means build Cardbus PCI1620

ATI@ : means build ATI SB USB2.0 related to turn on the function .

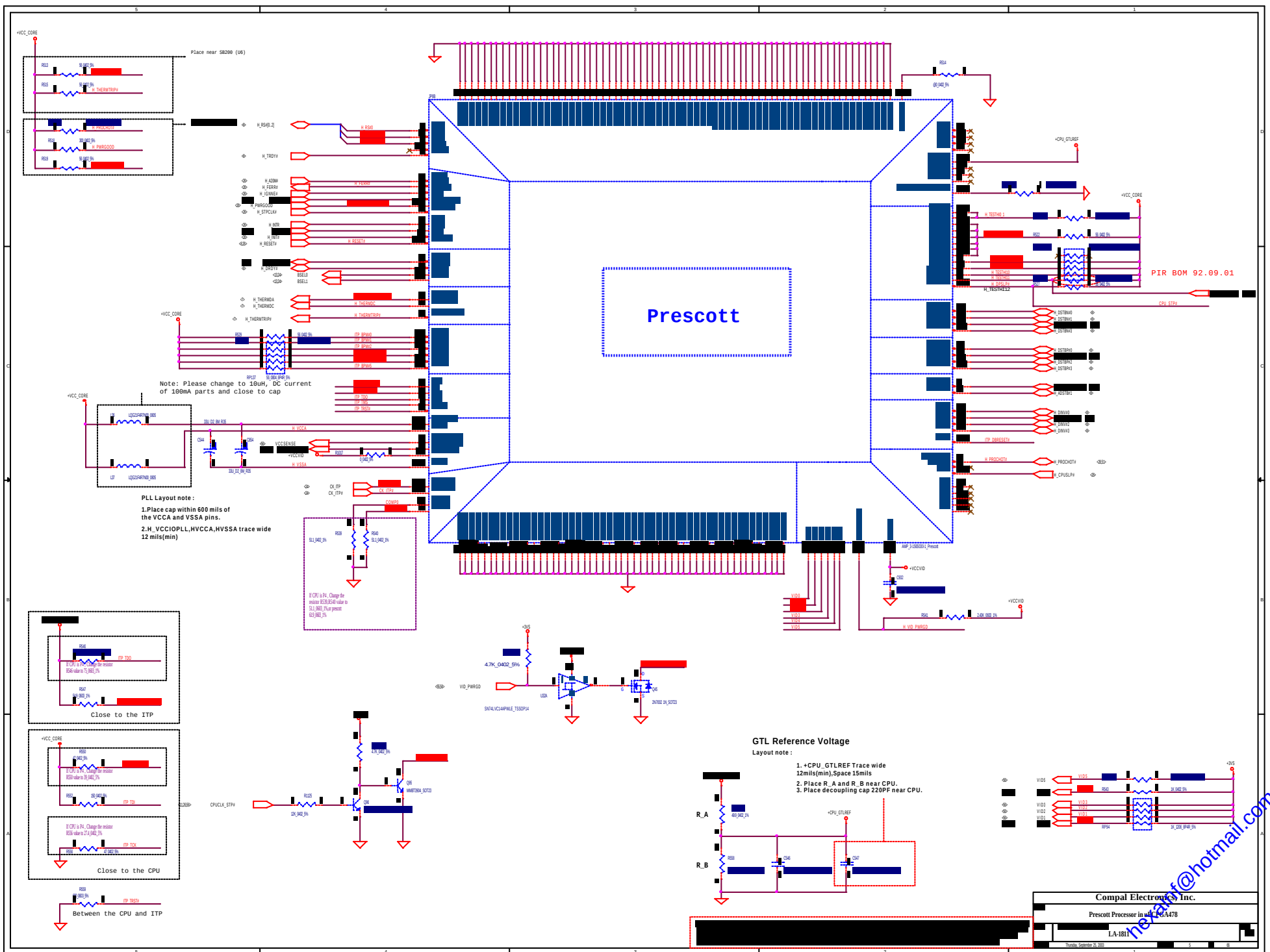
NEC@ : means build NEC USB2.0 related to turn on the function .

AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS



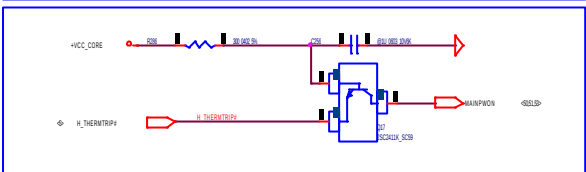
Reference Intel document
Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0
Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5

Pin number	Northwood Pin name	Comment	Prescott Pin name	Comment	Northwood Pin name	Comment	Northwood	Prescott	Northwood MT
A6	TESTHI11	Pull-up 200ohm to +VCC_CORE	TESTHI11	Pull-up 620ohm to +VCC_CORE	GHI	Connect to PLD CPUPREF through 80hm	Pop	Pop	Pop
B6	FERR#	Pull-up 620ohm to +VCC_CORE	FERR#/PBE#	Pull-up 620ohm to +VCC_CORE	FERR#	Pull-up 620ohm to +VCC_CORE	Pop	Pop	Pop
AA28	ITPCLKOUT0	Pull-up 560hm to +VCC_CORE	TESTHI6	Pull-up 620hm to +VCC_CORE	ITPCLKOUT0	Pull-up 560hm to +VCC_CORE	Pop	Pop	Pop
AB22	ITPCLKOUT1	Pull-up 560hm to +VCC_CORE	TESTHI7	Pull-up 620hm to +VCC_CORE	ITPCLKOUT1	Pull-up 560hm to +VCC_CORE	Pop	Pop	Pop
AD2	NC	float	VIDPWRGD	Pull-up 2.43K ohm to +VCCVID	NC	float	Depop	Pop	Depop
AD3	NC	float	VIDS	Pull-up 1Kohm to +3VRUN & connect to PWRIC	NC	float	Depop	Pop	Depop
AP3	NC	float	VCCVIDLB	Connect to +VCCVID	NC	float	Depop	Pop	Depop
AE23	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter			
AD20	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter			
AD1	VSS	Connect to GND	BOOTSELECT	CPU determine	VSS	Connect to GND	Pop	Depop	Pop
AE26	VSS	Connect to GND	OPTIMIZED/COMPAT#	float	VSS	Connect to GND	Pop	Depop	Pop
AD25	TESTHI12	Pull-up 200ohm to +VCC_CORE	TESTHI12	Pull-up 620hm to +VCC_CORE	DPSLP	Connect to PLD through 80hm	Pop	Pop	Pop



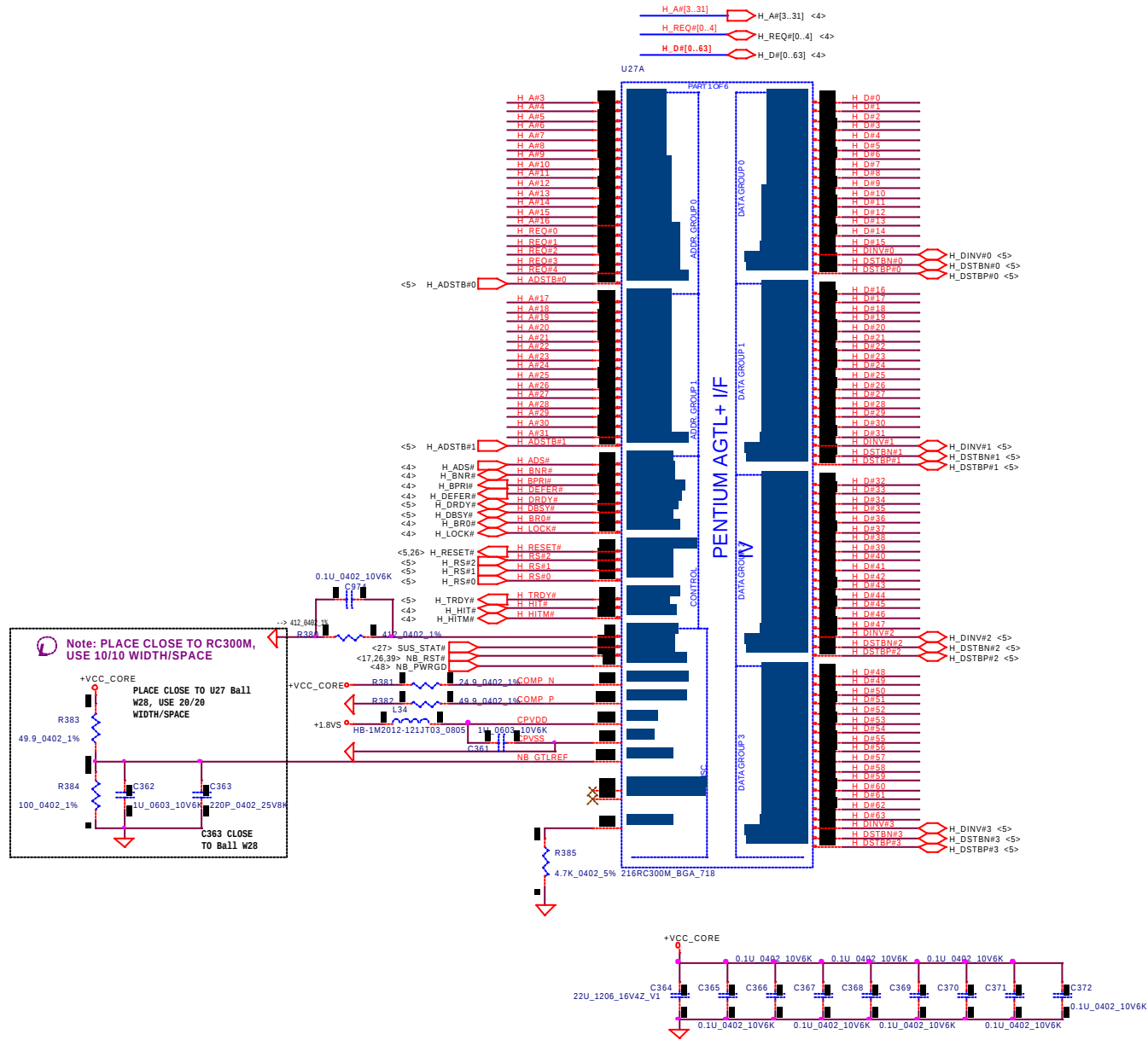
Thermal Sensor ADM1032AR

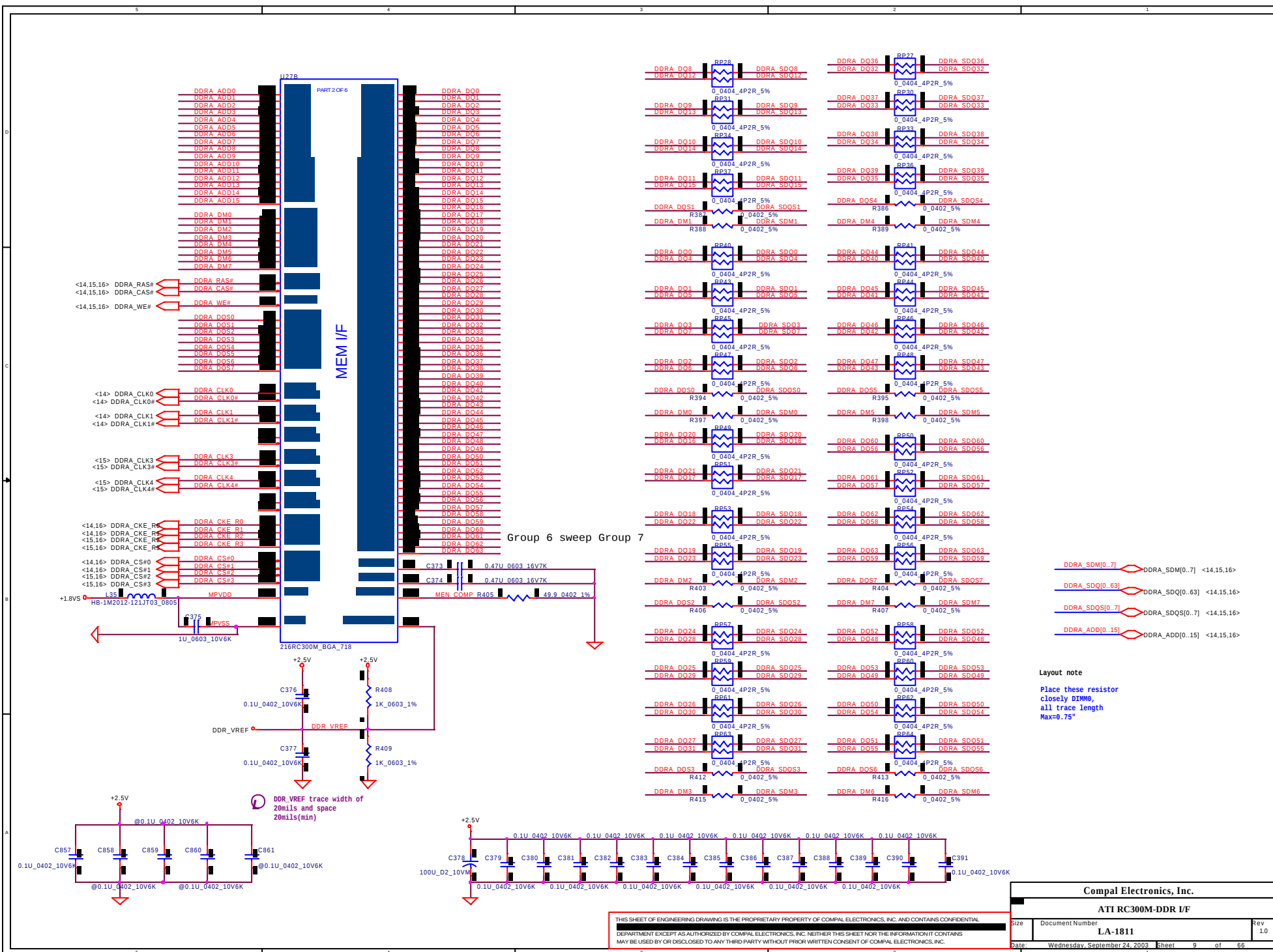
The diagram illustrates the internal circuitry of the Thermal Sensor ADM1032AR. Key components include a 100k pull-up resistor on the CS pin, a 100nF capacitor on the CS pin, and a 100k pull-down resistor on the SDA pin. The sensor is connected to a 3.3V supply and ground. The output pins are labeled THERMADA, THERMDC, CS_SMC_2, and CS_SMC_1. The address is 1001_100X.



FAN CONN.1

The diagram shows a fan speed control circuit. The fan motor (FAN1) is connected to a 5V supply through a 10k resistor. The speed sensor (FAN123456789) is connected to the fan motor. The speed controller (FAN123456789) is connected to the speed sensor. The speed feedback circuit (FAN123456789) is connected to the speed controller. A red circle highlights the feedback loop components, including the 10k resistor, the 100nF capacitor, and the 10k resistor.





<13,26> A_AD[0..31] A_AD[0..31]
<13,26> A_CBE#[0..3] A_CBE#[0..3]

A_AD0
A_AD1
A_AD2
A_AD3
A_AD4
A_AD5
A_AD6
A_AD7
A_AD8
A_AD9
A_AD10
A_AD11
A_AD12
A_AD13
A_AD14
A_AD15
A_AD16
A_AD17
A_AD18
A_AD19
A_AD20
A_AD21
A_AD22
A_AD23
A_AD24
A_AD25
A_AD26
A_AD27
A_AD28
A_AD29
A_AD30
A_AD31

A_CBE#0
A_CBE#1
A_CBE#2
A_CBE#3

<13,26> A_PAR
<26> A_STROBE#
<26> A_ACAT#
<26> A_END#
<17,26,31,35,36> PCI_PIRQA#
<26> A_DEVSEL#
<26> A_OFF#
<26> A_SBRREQ#
<26> A_SBGNT#

A_PAR
A_STROBE#
A_ACAT#
A_END#
A_DEVSEL#
A_OFF#
A_SBRREQ#
A_SBGNT#

AGP_GNT#
AGP_REQ#
AGP8X_DET#
AGPREF_8X

AGP_COMP
AGP8X_DET#

AGP8X_DET#

AGP8X_DET#

AGP8X_DET#

AGP8X_DET#

AGP8X_DET#

AGP8X_DET#

AGP8X_DET#

AGP8X_DET#

AGP8X_DET#

AGP8X_DET#

PCI Bus 0 / A-Link I/F
PCI BUS 1 / AGP Bus (GPIO , TMD5 , ZVPort)

	8X(M9+M10@)	4X(NAGP@)
Ra	169_0402_1%	52.1_0402_1%
Rb	324_0402_1%	1K_0402_1%
Rc	100_0402_1%	1K_0402_1%

AGP_AD0
AGP_AD1
AGP_AD2
AGP_AD3
AGP_AD4
AGP_AD5
AGP_AD6
AGP_AD7
AGP_AD8
AGP_AD9
AGP_AD10
AGP_AD11
AGP_AD12
AGP_AD13
AGP_AD14
AGP_AD15
AGP_AD16
AGP_AD17
AGP_AD18
AGP_AD19
AGP_AD20
AGP_AD21
AGP_AD22
AGP_AD23
AGP_AD24
AGP_AD25
AGP_AD26
AGP_AD27
AGP_AD28
AGP_AD29
AGP_AD30
AGP_AD31

AGP_SSSTB
AGP_SSSTB#
AGP_ADSTB0#
AGP_ADSTB1#
AGP_ADSTB2#
AGP_ADSTB3#

AGP_CBE#0
AGP_CBE#1
AGP_CBE#2
AGP_CBE#3

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

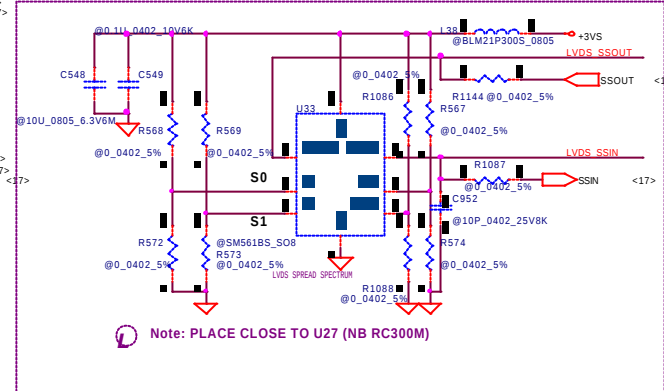
AGP_IRDY#
AGP_TRDY#
AGP_STOP#
AGP_PAR#
AGP_FRAME#
AGP_DEVSEL#
AGP_DBI_HI/PIPE#
AGP_DBI_LO#
AGP_RBF#

AGPAND LVDS MUXED SIGNALS

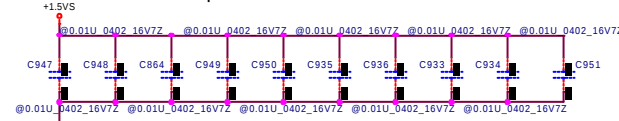
AGP_SBA2 R560 NAPG@0_0402_5% ENABLTH# <17,25>
AGP_SBA3 R561 NAPG@0_0402_5% ENAVDD <17,25,46>
AGP_SBA4 R562 NAPG@0_0402_5% AGP_STP# <17,27>
AGP_SBA5 R563 NAPG@0_0402_5% AGP_BUSY# <17,27>
AGP_SBA6 R564 @0_0402_5% LVDS_SSOUT
AGP_SBA7 R565 @0_0402_5% LVDS_SSIN
AGP_SBA1 R994 NAPG@0_0402_5% DDC_DAT <17,25>
AGP_SBA0 R995 NAPG@0_0402_5% DDC_CLK <17,25>

AGP_AD[0..31] AGP_AD[0..31] <17>
AGP_SBA[0..7] AGP_SBA[0..7] <17>
AGP_CBE#[0..3] AGP_CBE#[0..3] <17>
AGP_ST[0..2] AGP_ST[0..2] <17>

PIR BOM 92.06.23



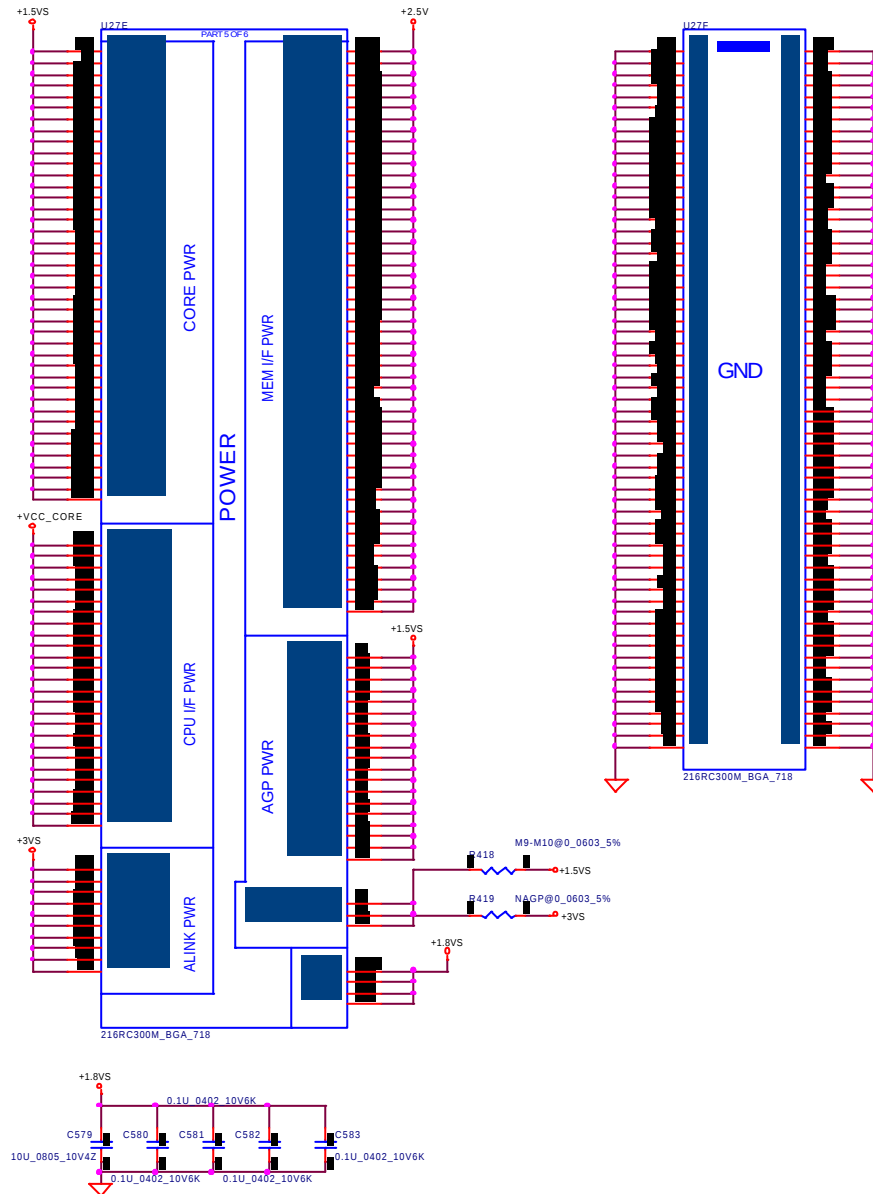
ATI request



Note: PLACE CLOSE TO U27 (NB RC300M)

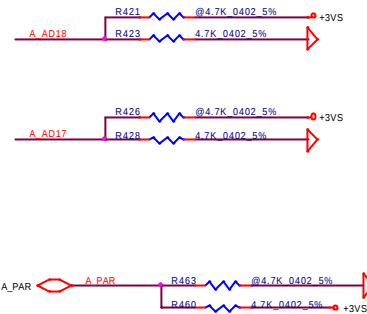
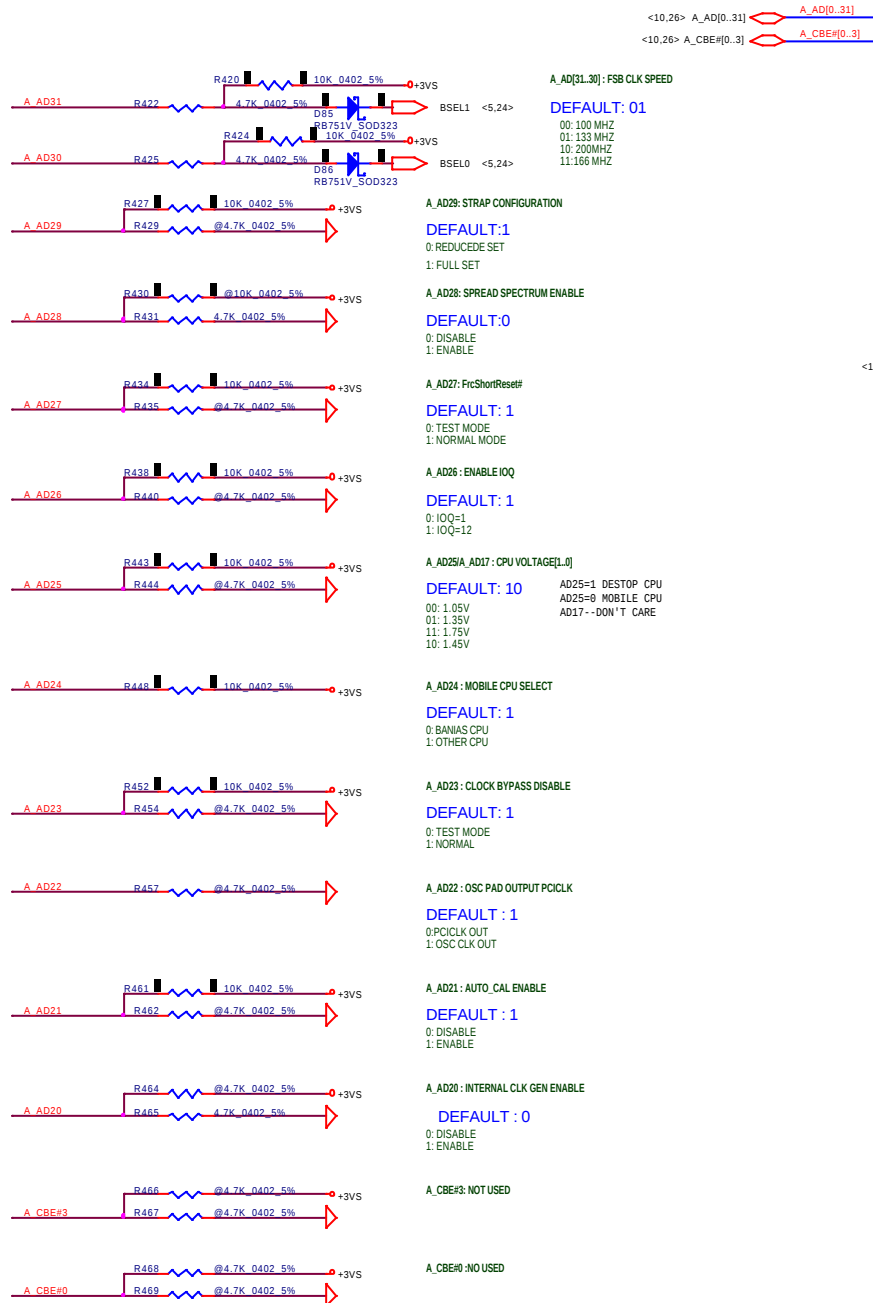
Compal Electronics, Inc.		
ATI RC300M-AGP, ALINK BUS		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 10 of 66

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
ATI RC300M-POWER		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 12 of 66



A_AD18: ENABLE PHASE CALIBRATION

DEFAULT: 0

0: DISABLE

1: ENABLE

A_AD25/A_AD17: CPU VOLTAGE[L0]

DEFAULT: 0

00: 1.05V

01: 1.35V

11: 1.75V

10: 1.45V

PAR: EXTENDED DEBUG MODE

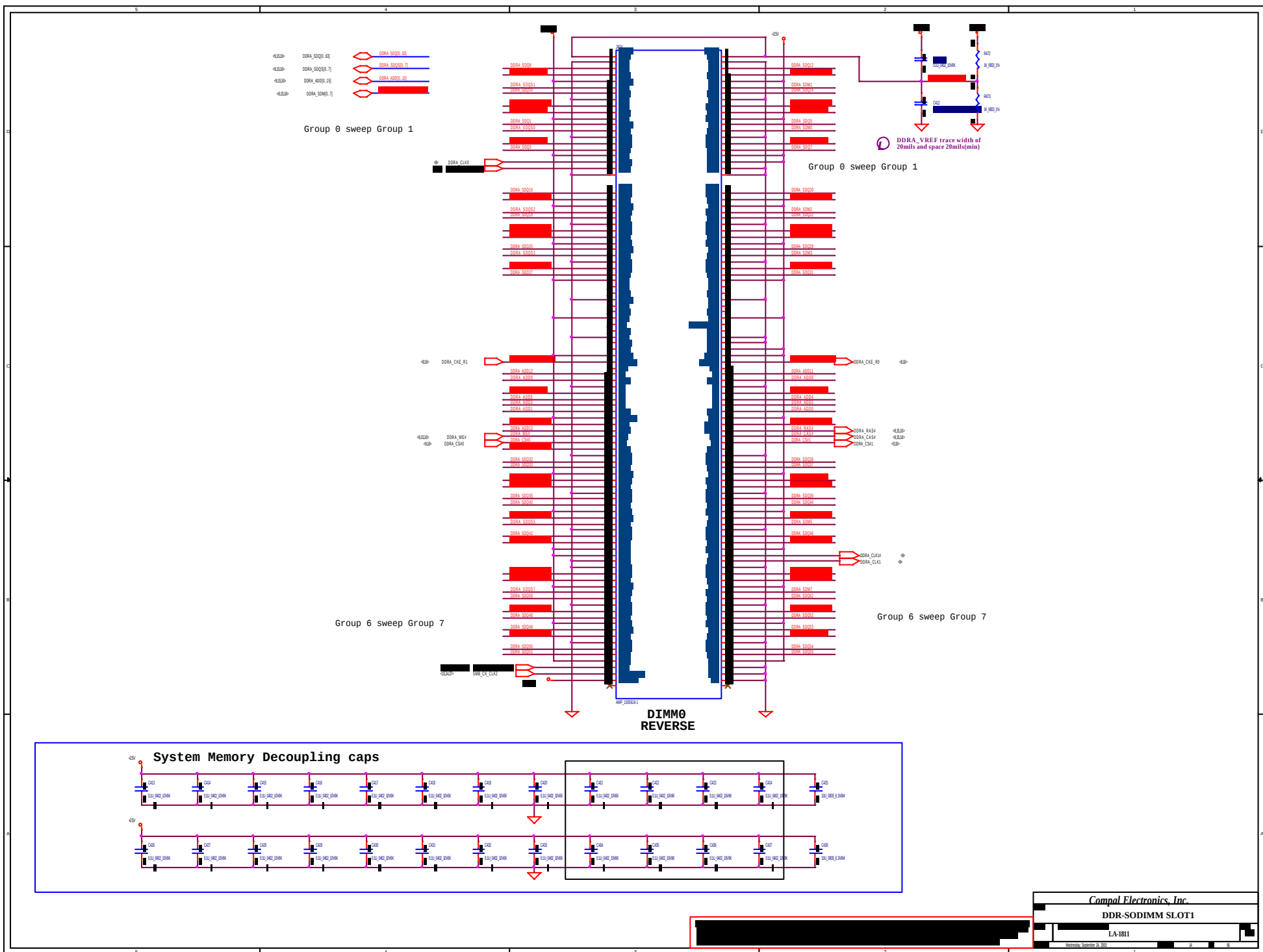
DEFAULT: 1

0: DEBUG MODE

1: NORMAL

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
ATI RC300M-SYSTEM STRAP		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 13 of 66



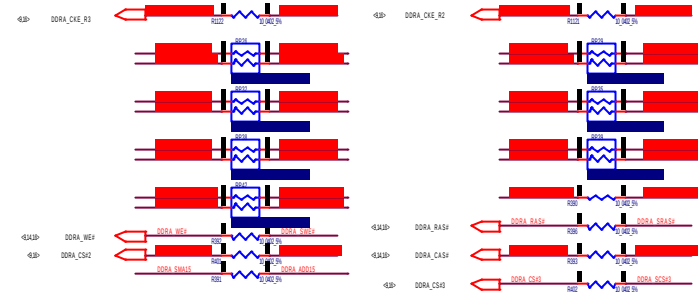
<LA3P> DDR4_SQ[0..15] DDR4_SQ[0..15]
 <LA3P> DDR4_SQ[0..15] DDR4_SQ[0..15]
 <LA3P> DDR4_ADD[0..15] DDR4_ADD[0..15]

Group 0 sweep Group 1

◇ DDR4_CLK3
 ◇ DDR4_CLK9

Group 0 sweep Group 1

DDR4_VREF trace width of
 20mils and space
 20mils(min)

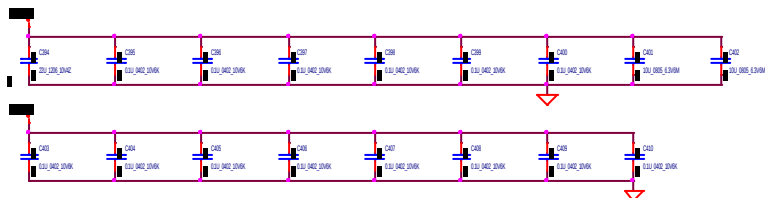


Group 6 sweep Group 7

<LA2D> SMB_CLK[0..15]
 <LA2D> SMB_CLK[0..15]

DIMM1
 STANDARD

System Memory Decoupling caps

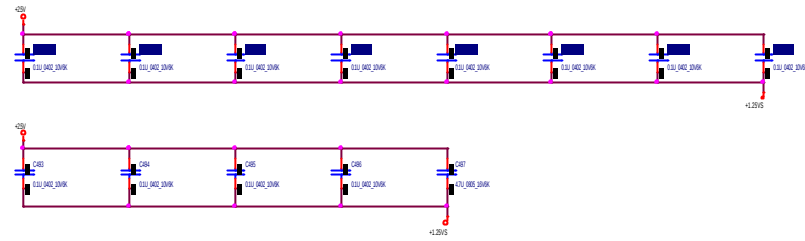
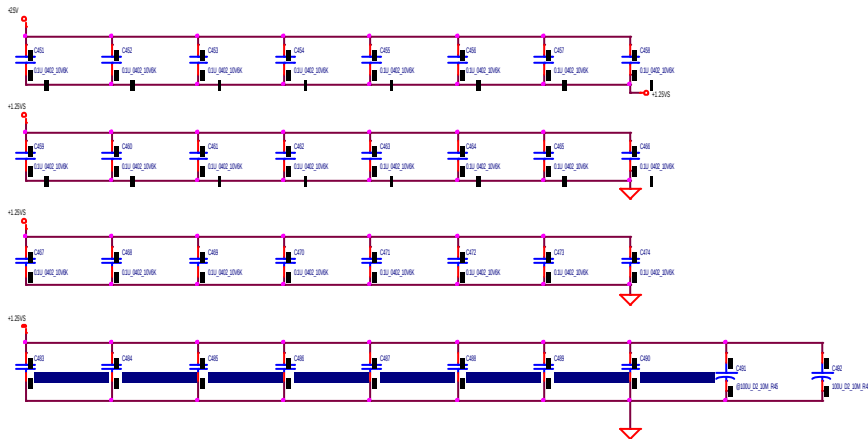
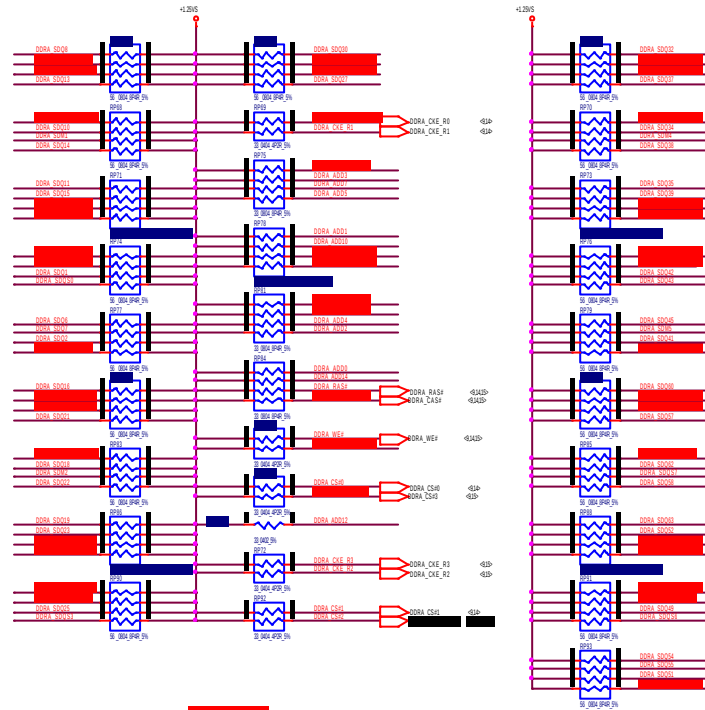


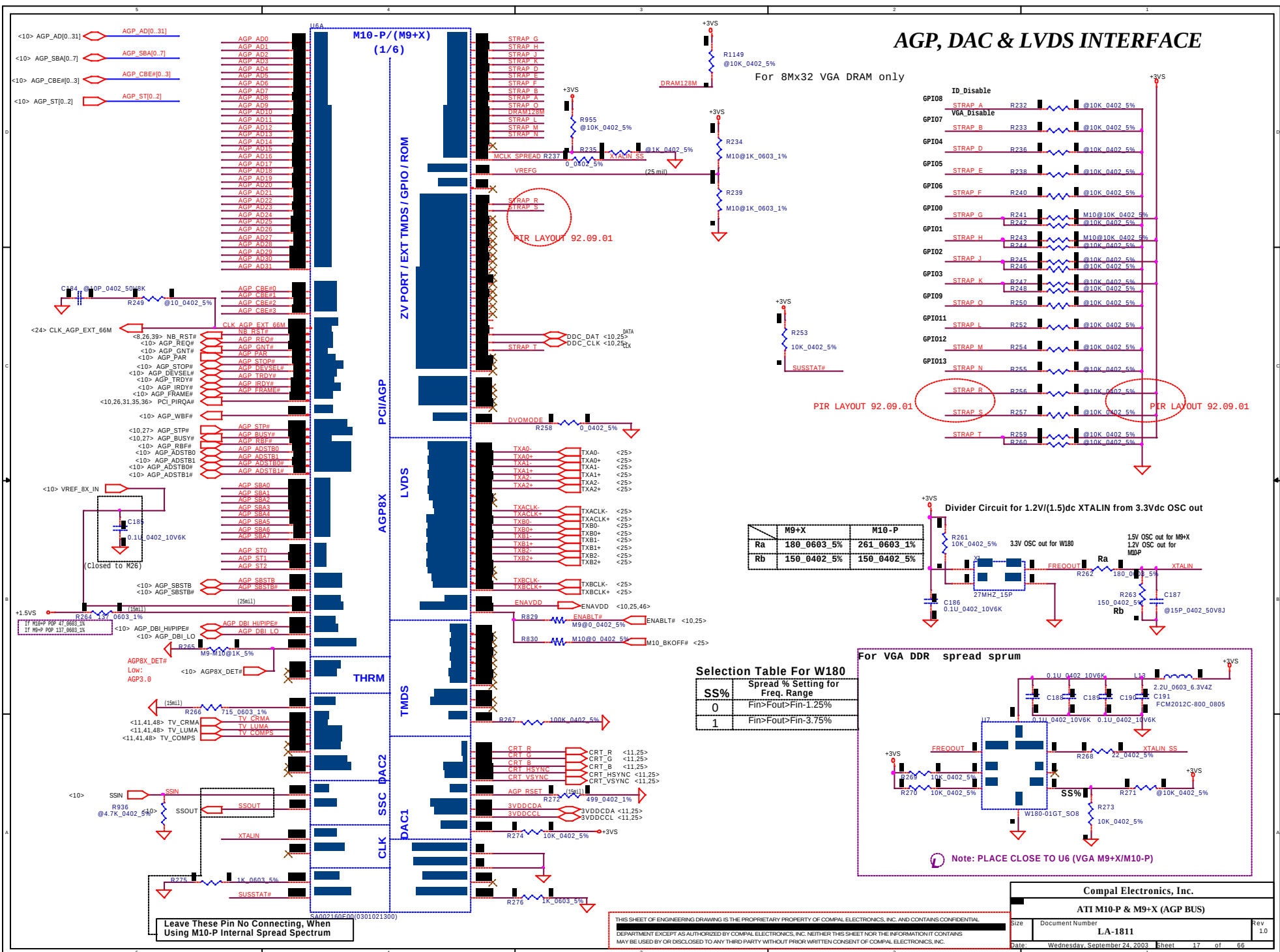
Compal Electronics, Inc.

DDR-SODIMM SLOT2

LA-1811

DDR Termination resistors & Decoupling caps





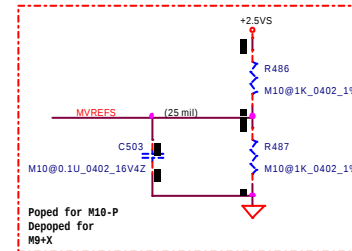
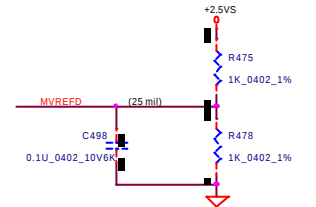
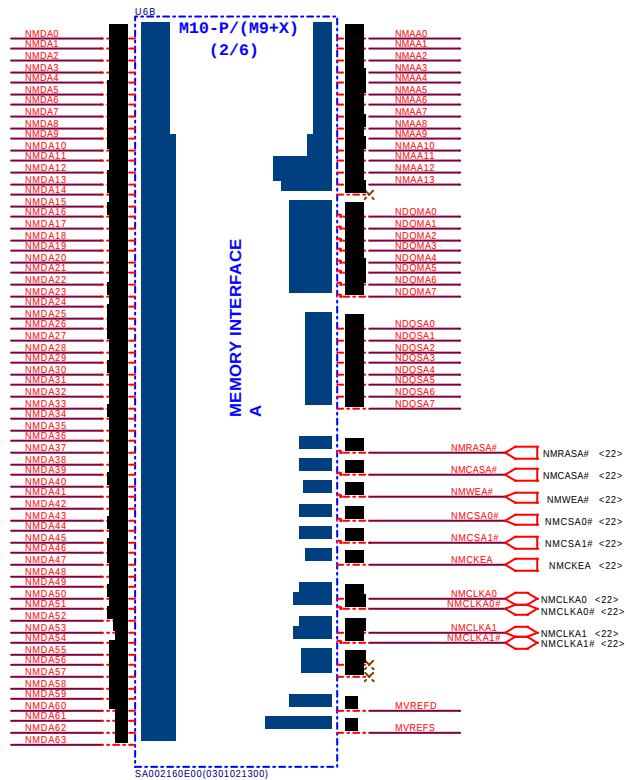
MEMORY INTERFACE A

<22> NMDA[0..63]  NMDA[0..63]

<22> NMAA[0..13]  NMAA[0..13]

<22> NDQMA[0..7]  NDQMA[0..7]

<22> NDQSA[0..7]  NDQSA[0..7]

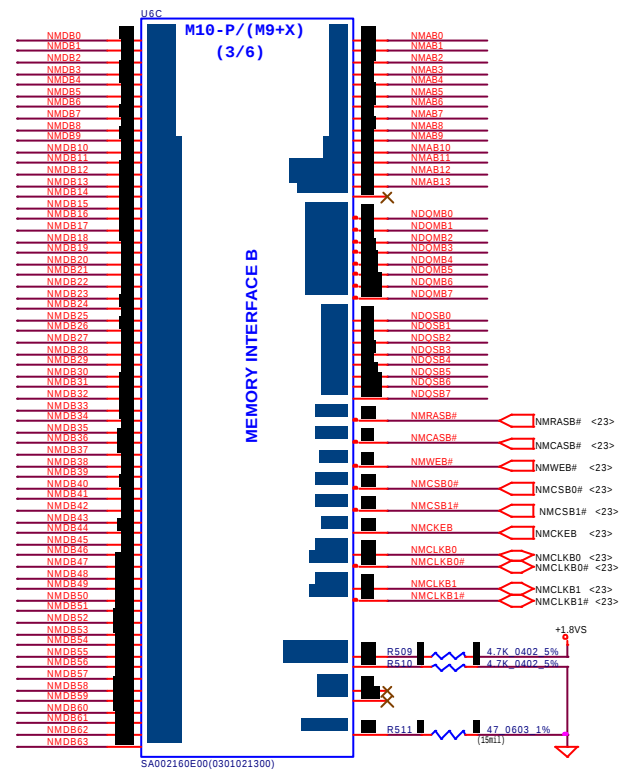


THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
ATI M10-P/M9+X DDR-A		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 18 of 66

MEMORY INTERFACE B

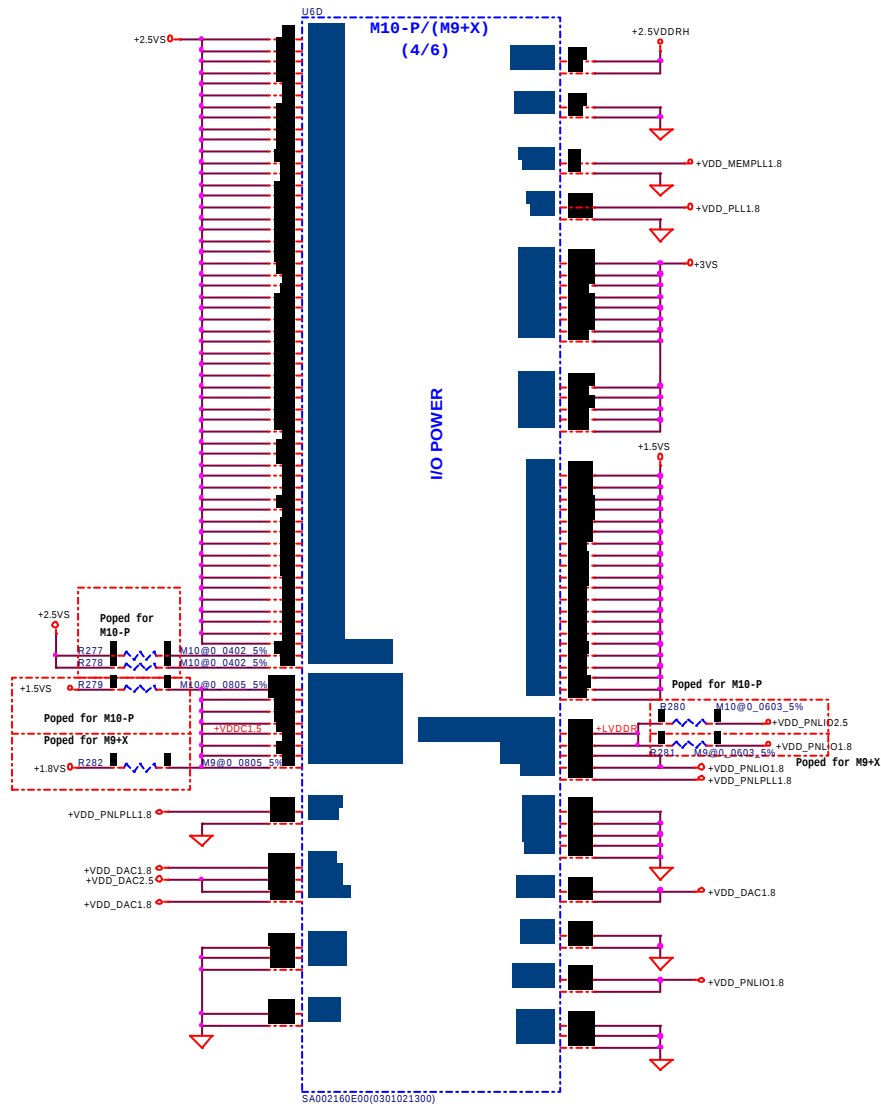
<23> NMDB[0..63] NMAB[0..63]
<23> NMAB[0..13] NMAB[0..13]
<23> NDQMB[0..7] NDQMB[0..7]
<23> NDQSB[0..7] NDQSB[0..7]



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
ATI M10-P/M9+X DDR-B			
Size	Document Number	Rev	
	LA-1811	1.0	
Date	Wednesday, September 24, 2003	Sheet	19 of 66

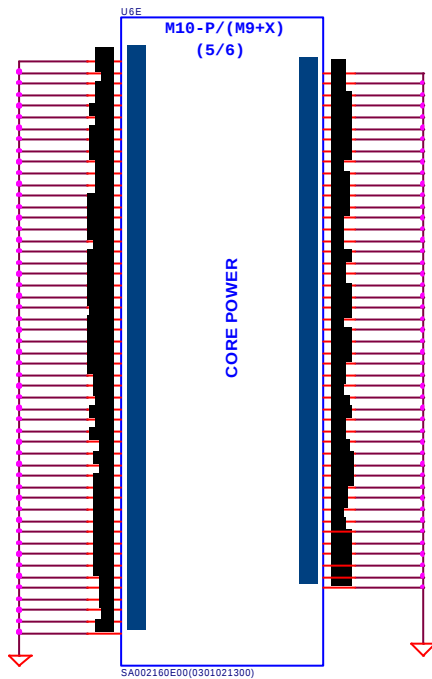
POWER INTERFACE



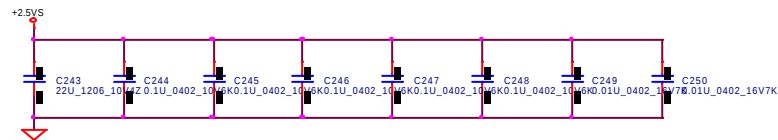
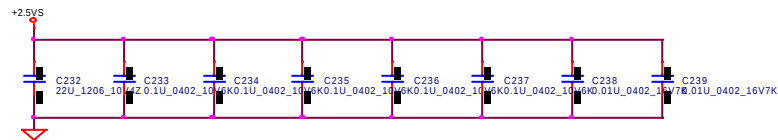
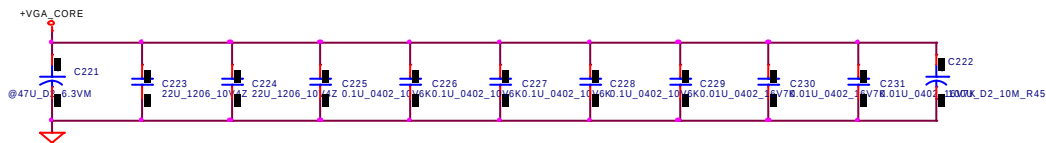
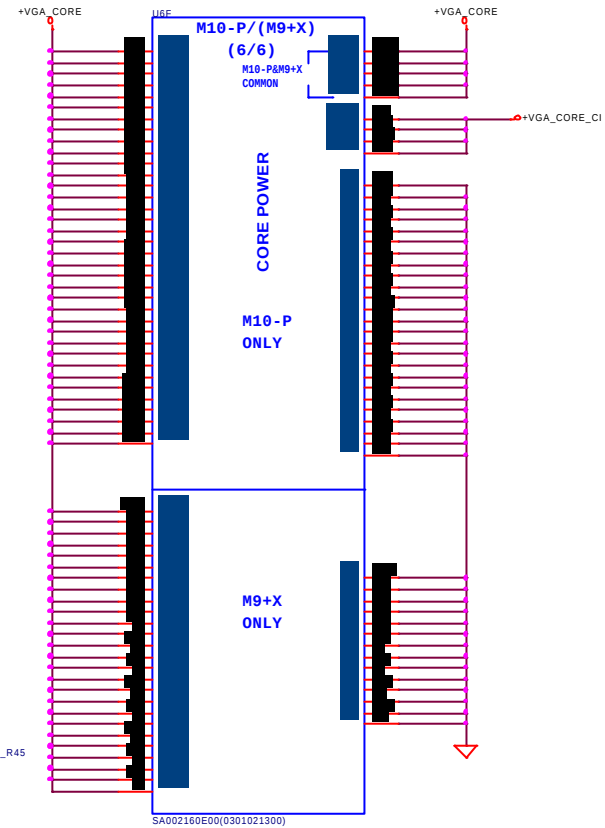
As close as possible to related pin

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE KEPT SECRET AND NOT DISCLOSED TO ANY OTHER PERSON OR ORGANIZATION WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NO PART OF THIS SHEET OR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

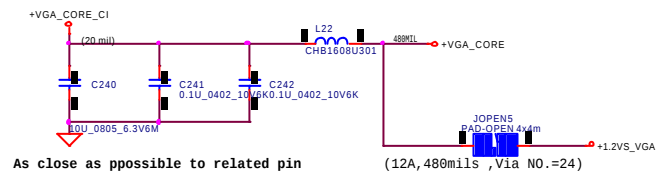
Compal Electronics, Inc.			
ATI M10-P/M9+X POWER-A			
Size	Document Number	Rev	
	LA-1811	1.0	
Date	Wednesday, September 24, 2003	Sheet	20 of 66



POWER INTERFACE



As close as possible to related pin



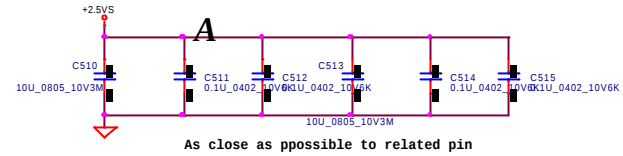
As close as possible to related pin

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

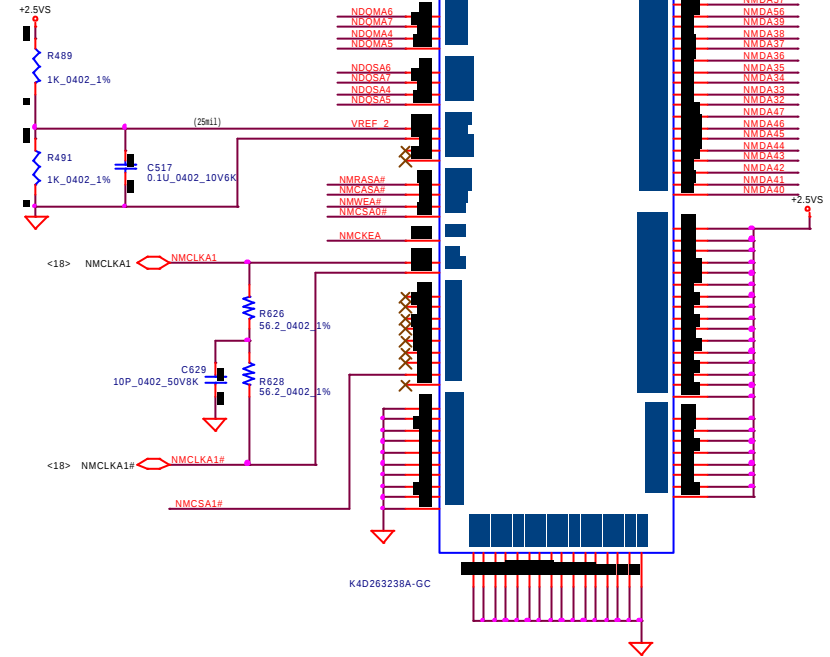
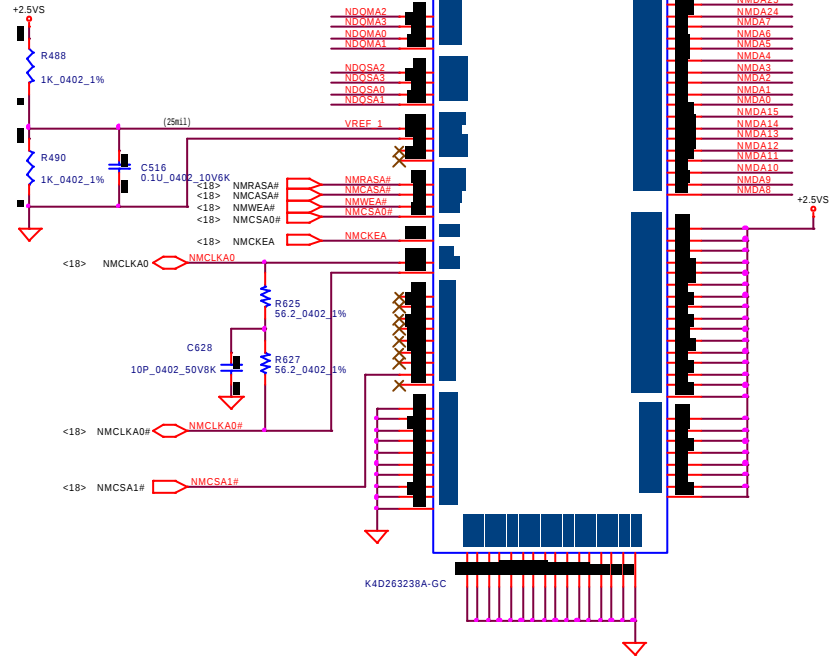
Compal Electronics, Inc.		
ATI M10-P/M9+X POWER-B		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 21 of 66

VGA DDR FOR CHANNEL

A



- <18> NMAA[0..13] NMAA[0..13]
- <18> NMDA[0..63] NMDA[0..63]
- <18> NDQMA[0..7] NDQMA[0..7]
- <18> NDQSA[0..7] NDQSA[0..7]

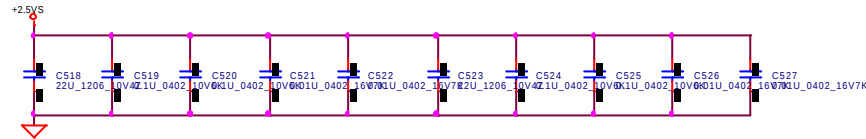


THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

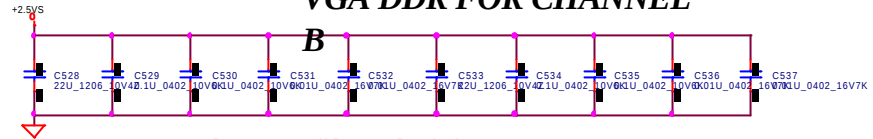
Compal Electronics, Inc.		
VGA DDR FOR CHANNEL A		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 22 of 66

VGA DDR FOR CHANNEL

B

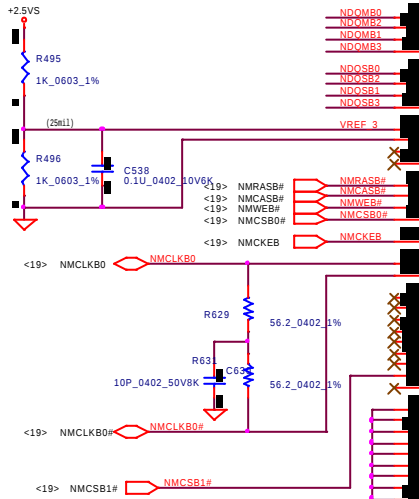


As close as possible to related pin

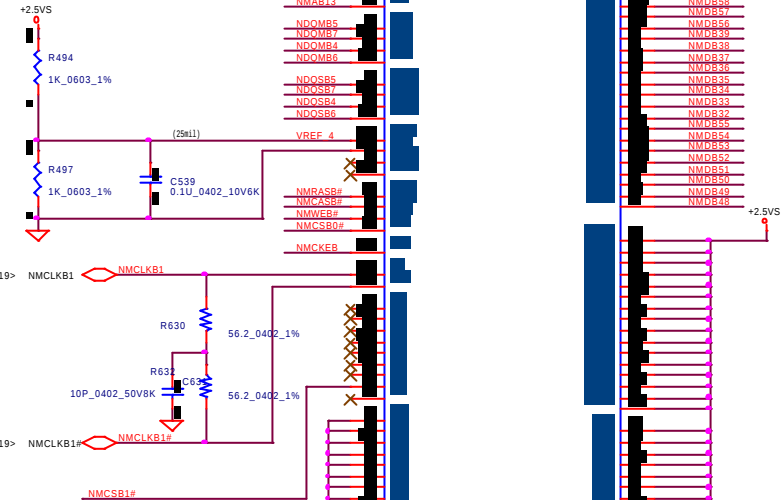


As close as possible to related pin

<19> NMAB[0..13] NMAB[0..13]
 <19> NMDB[0..63] NMDB[0..63]
 <19> NDQMB[0..7] NDQMB[0..7]
 <19> NDQSB[0..7] NDQSB[0..7]



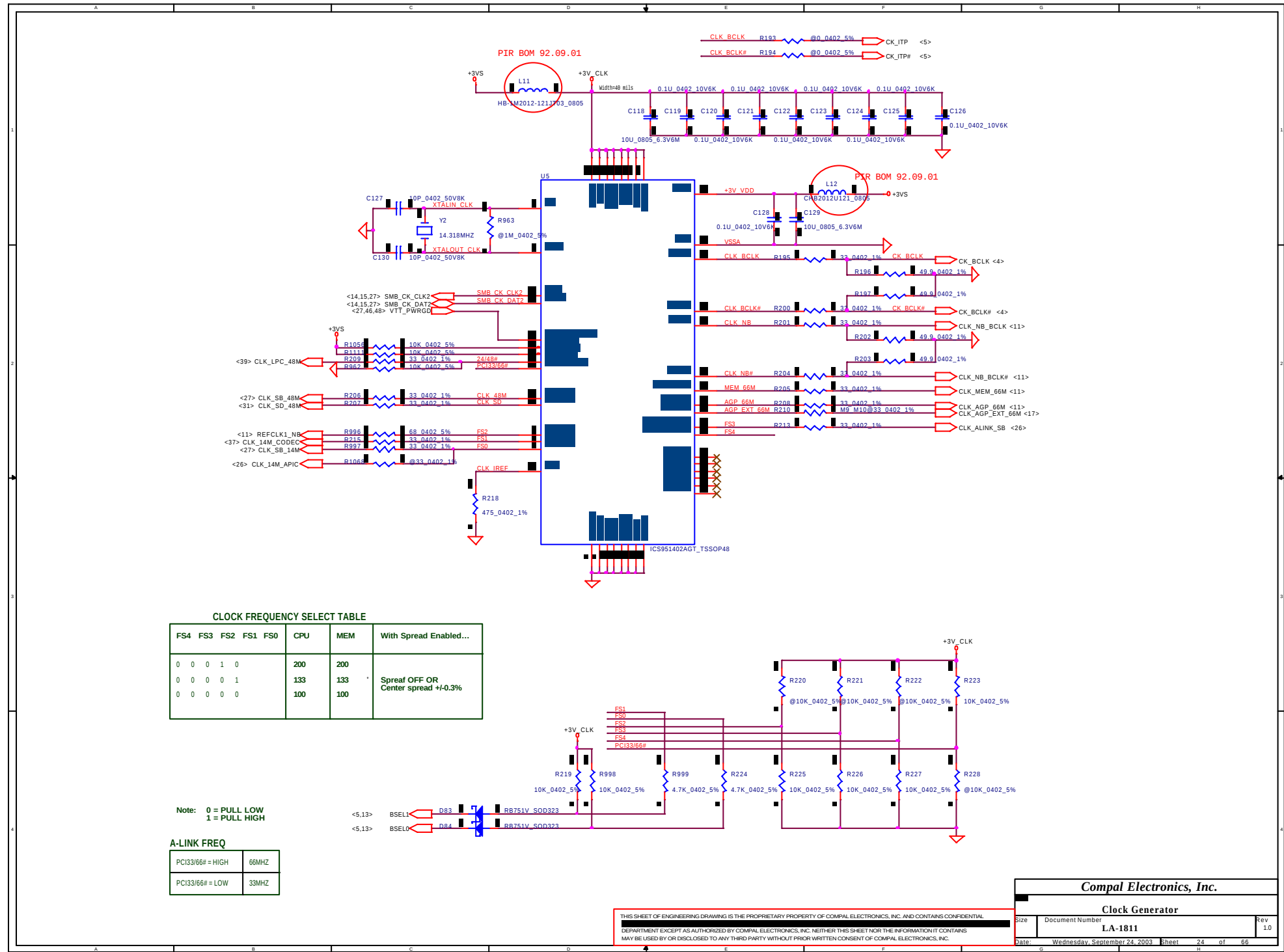
K4D263238A-GC



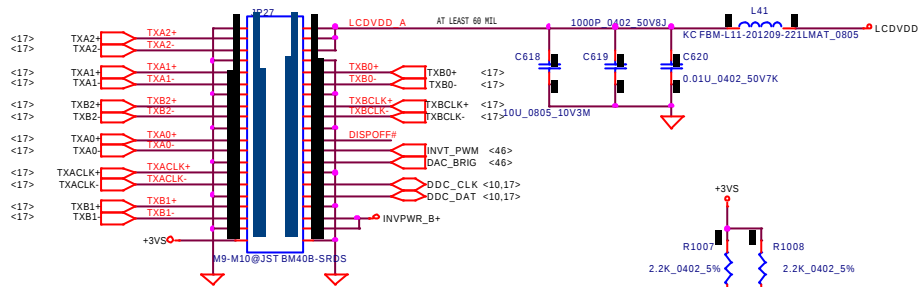
K4D263238A-GC

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED IN ANY MANNER WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

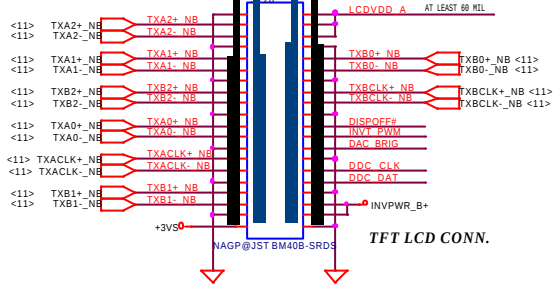
Compal Electronics, Inc.		
VGA DDR FOR CHANNEL B		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 23 of 66



LCD CONN



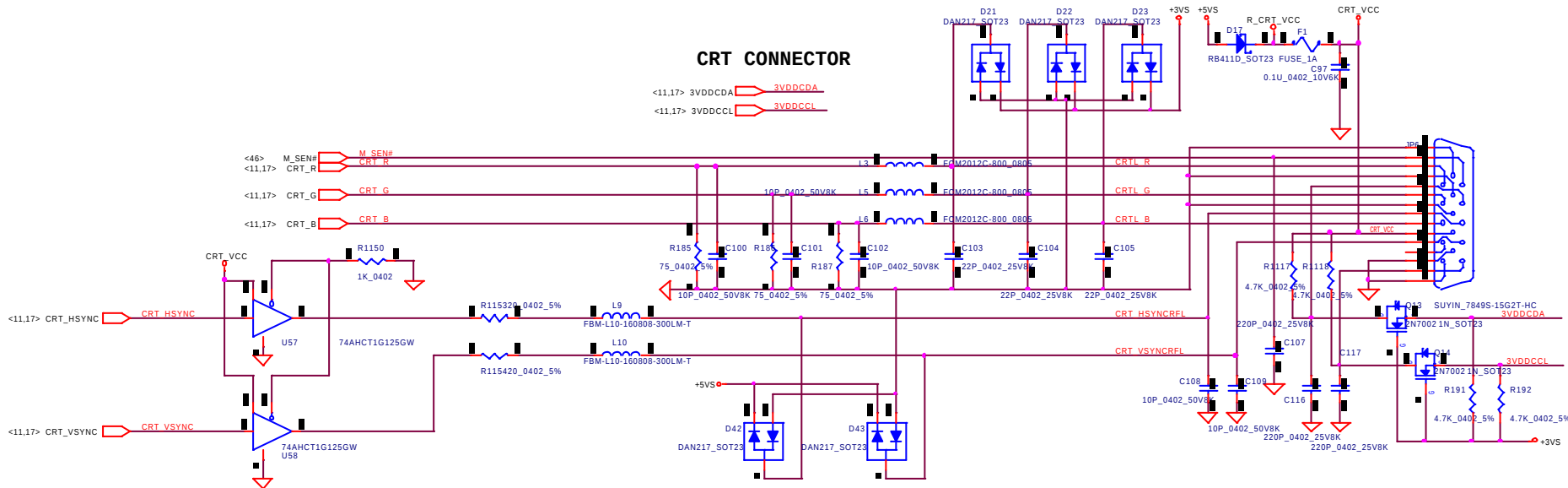
TFT LCD CONN.



TFT LCD CONN.

CRT CONNECTOR

<11,17> 3VDDCDA 3VDDCDA
<11,17> 3VDDCCL 3VDDCCL

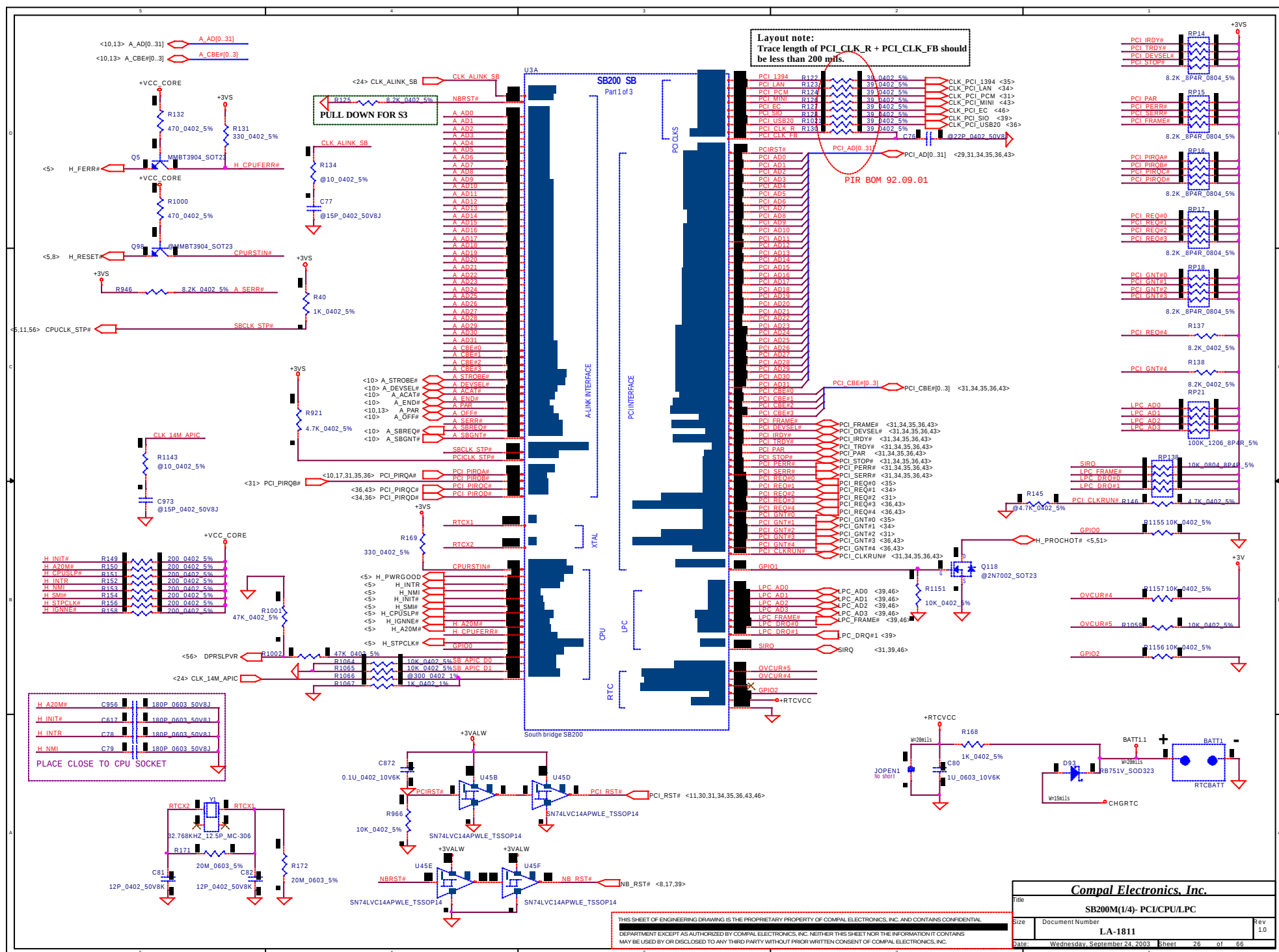


Compal Electronics, Inc.

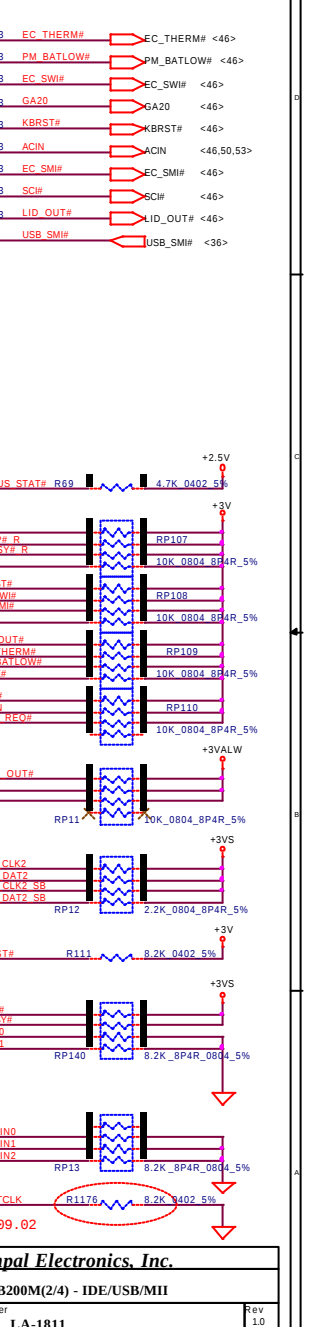
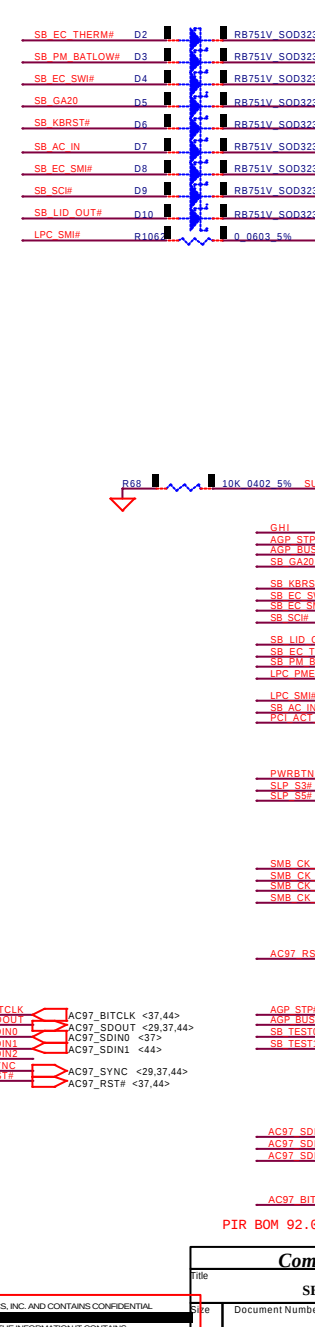
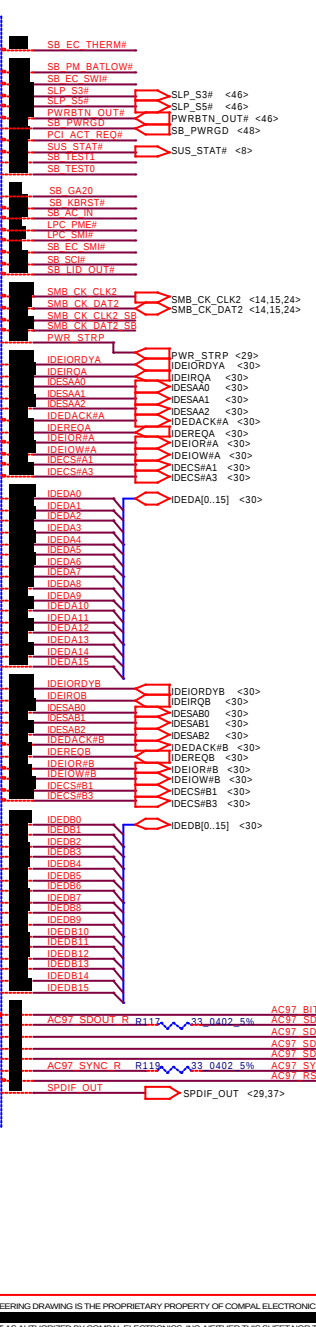
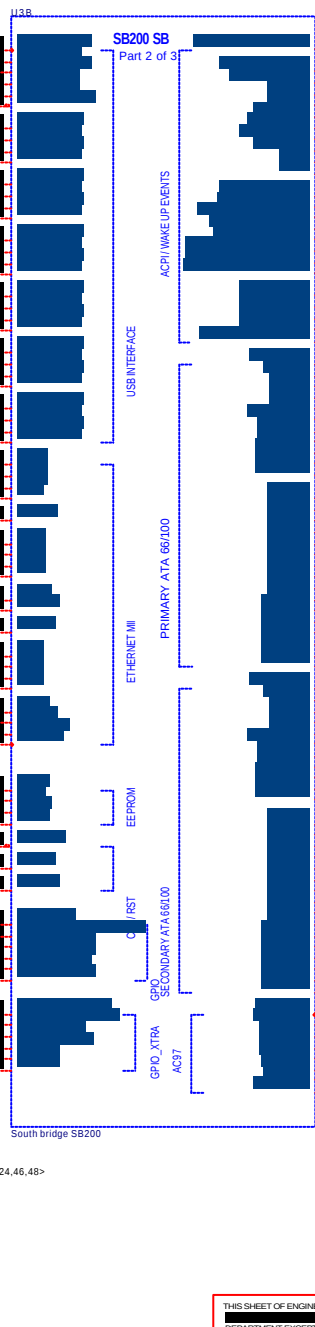
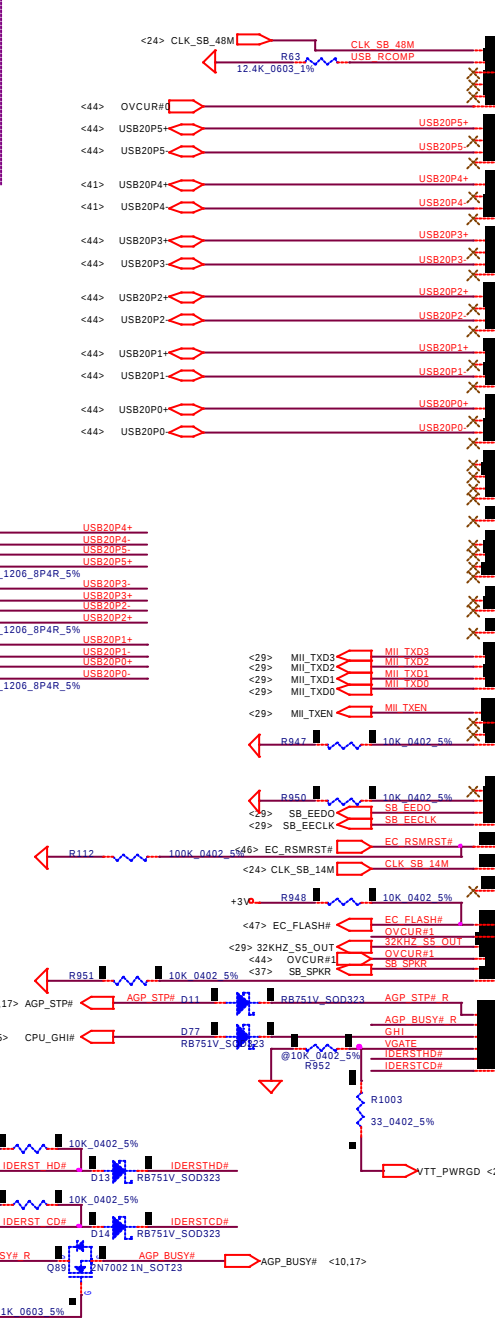
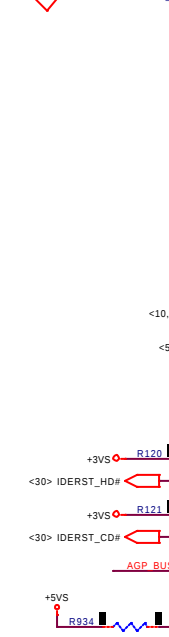
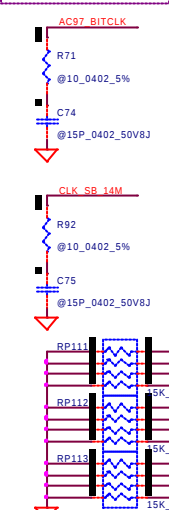
LCD,CRT,TV-OUT & Inverter BD CONN.

Size Document Number
LA-1811
Date Wednesday, September 24, 2003 Sheet 25 of 66

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE KEPT AS A SECRET AND NOT DISCLOSED TO ANY OTHER PERSON OR ORGANIZATION WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

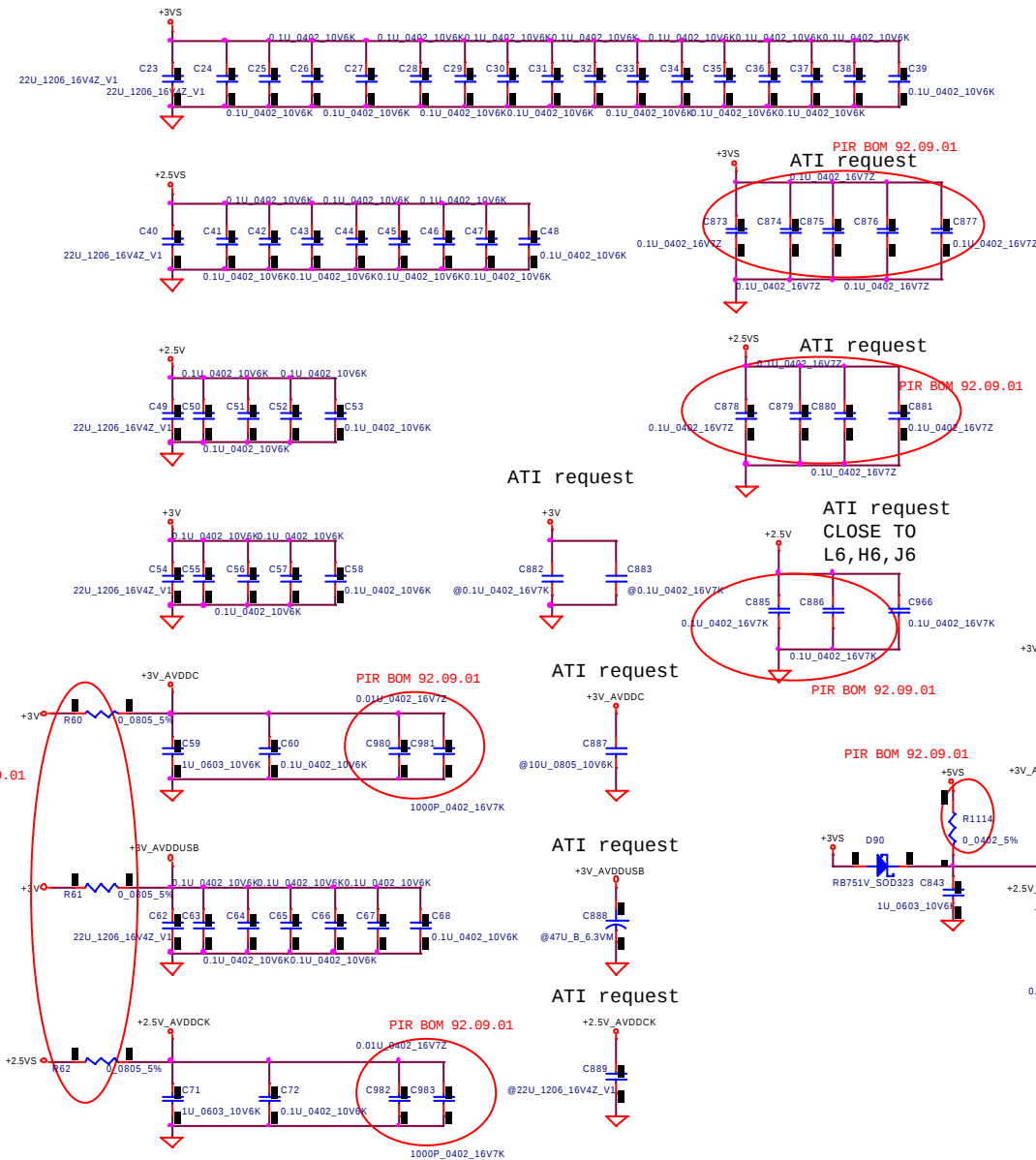


Note: Place close to U3 (ATI SB) For ATI USB2.0 only.



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
SB200M(2/4) - IDE/USB/MI		
File	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 27 of 66



PIR BOM 92.09.01

PIR BOM 92.09.01

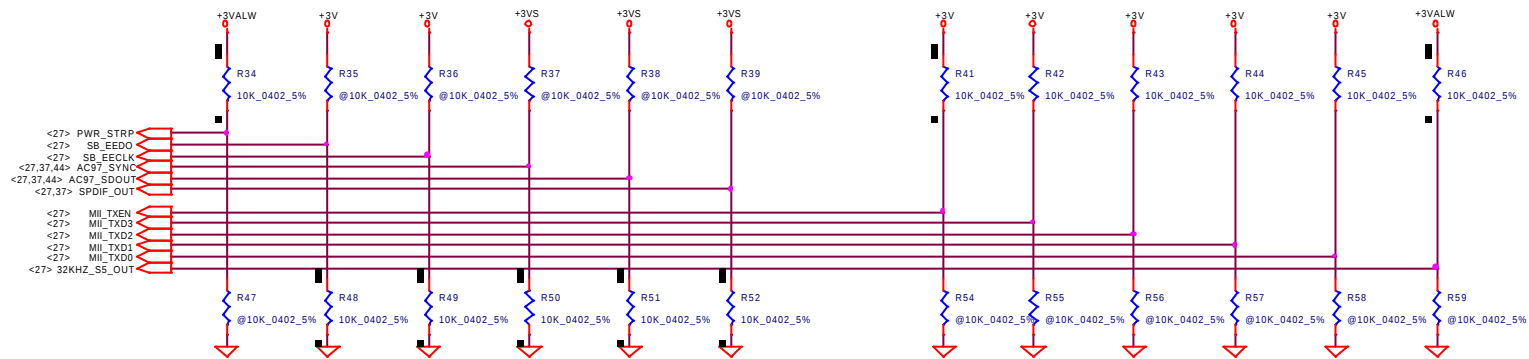
PIR BOM 92.09.01

PIR BOM 92.09.01

PIR BOM 92.09.01

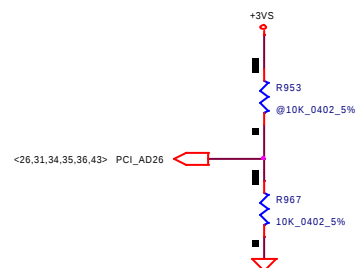
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE KEPT SECRET AND NOT DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
File		SB200M(3/4) - PWR	
Size	Document Number	Rev	
	L.A-1811	1.0	
Date:	Wednesday, September 24, 2003	Sheet	28 of 66



REQUIRED SYSTEM STRAPS

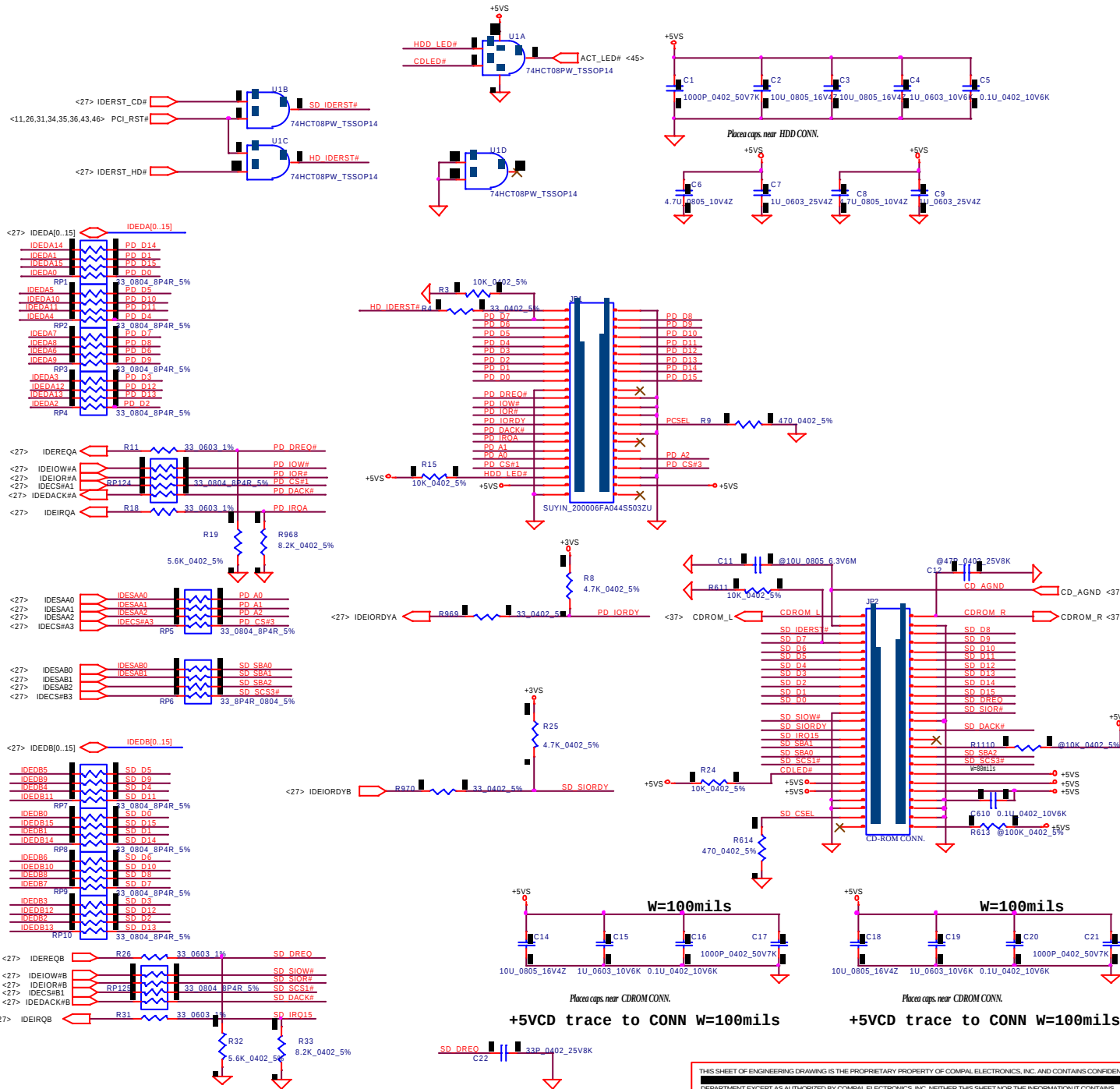
	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLYCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 20MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC)
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (P#)	HI SPEED A-LINK DEFAULT	SIO 40MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQ SETTING		32KHZ INPUT TO SB200 (EXT RTC)



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL
 INFORMATION. IT IS TO BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
SB200M(4/4) - STRAPS			
Size	Document Number	Rev	
	LA-1811	1.0	
Date:	Wednesday, September 24, 2003	Sheet	29 of 66

HDD/CD-ROM Module



Compal Electronics, Inc.		
HDD & CDROM Connector		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 30 of 66

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

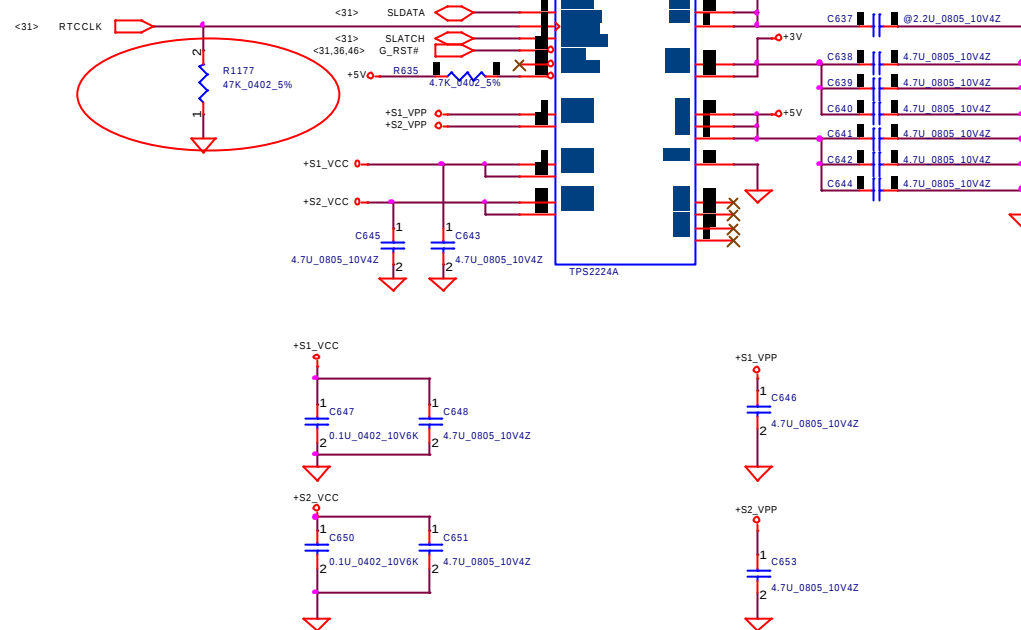
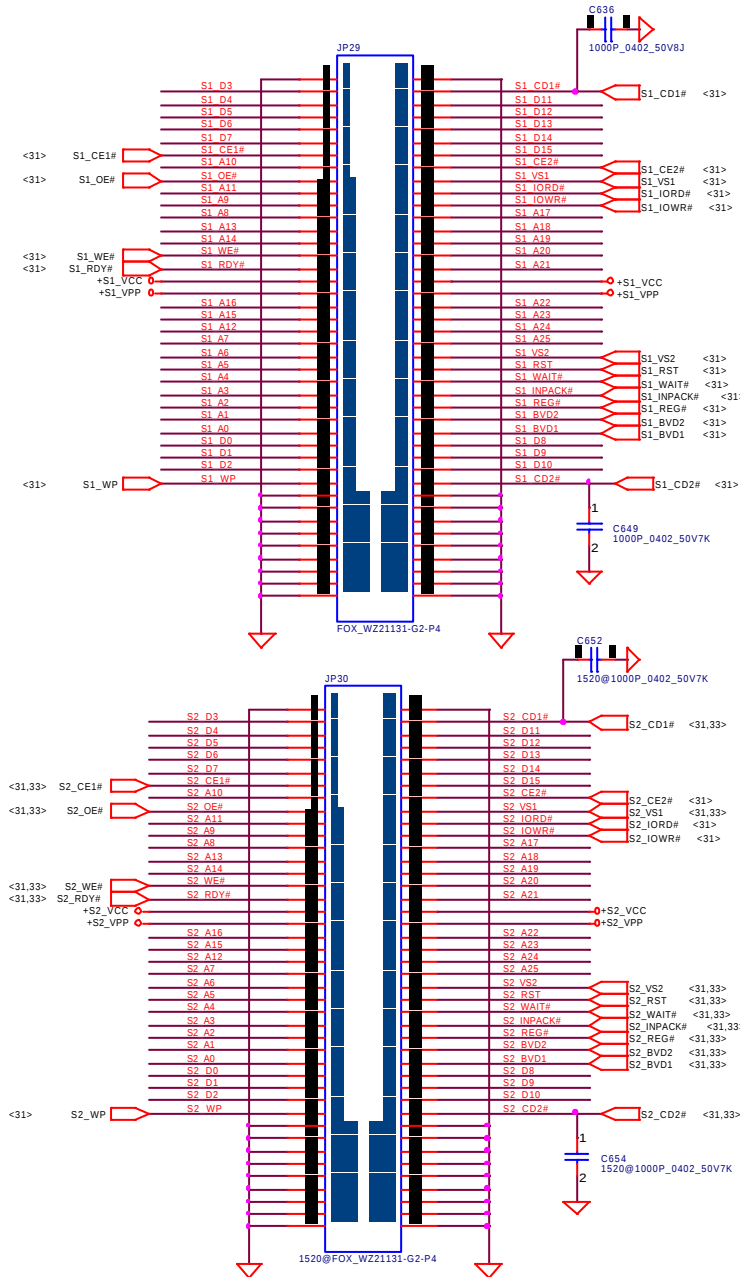
CARDBUS

SOCKET

<31> S1_D[0..15] S1_D[0..15]
 <31> S1_A[0..25] S1_A[0..25]
 <31,33> S2_D[0..15] S2_D[0..15]
 <31,33> S2_A[0..25] S2_A[0..25]

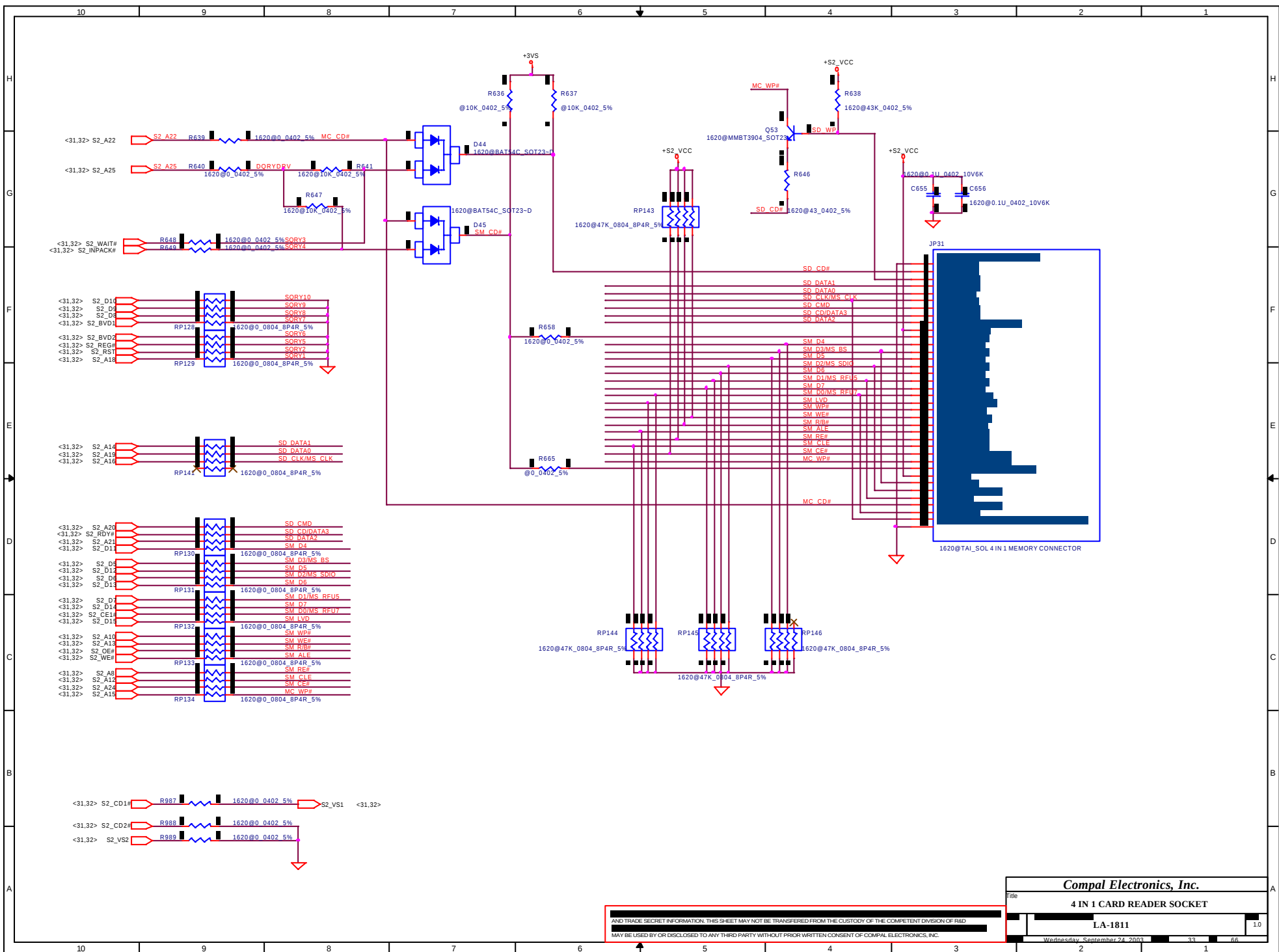
PCMCIA POWER CTRL.

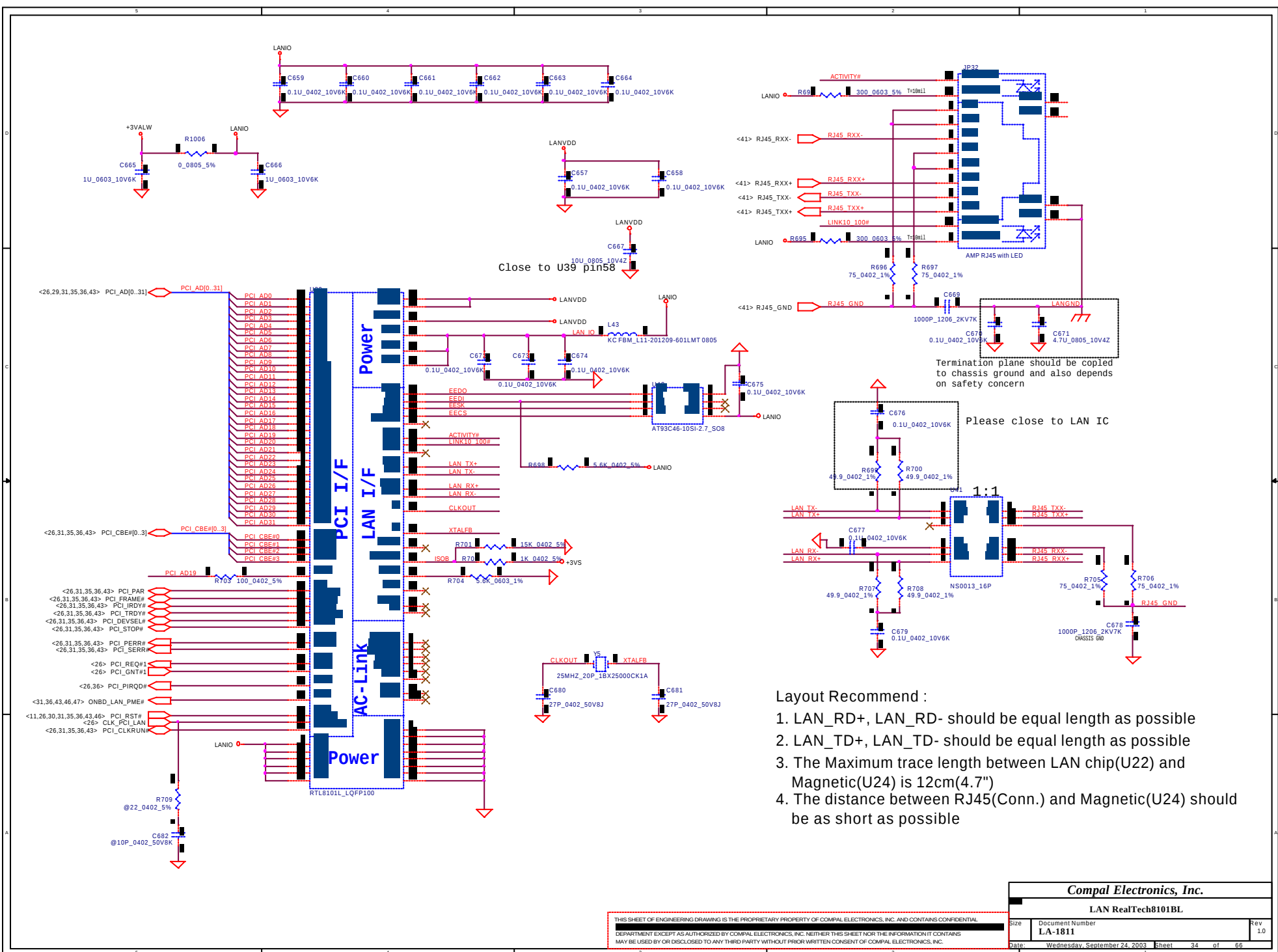
PIR BOM & LAYOUT 92.09.01

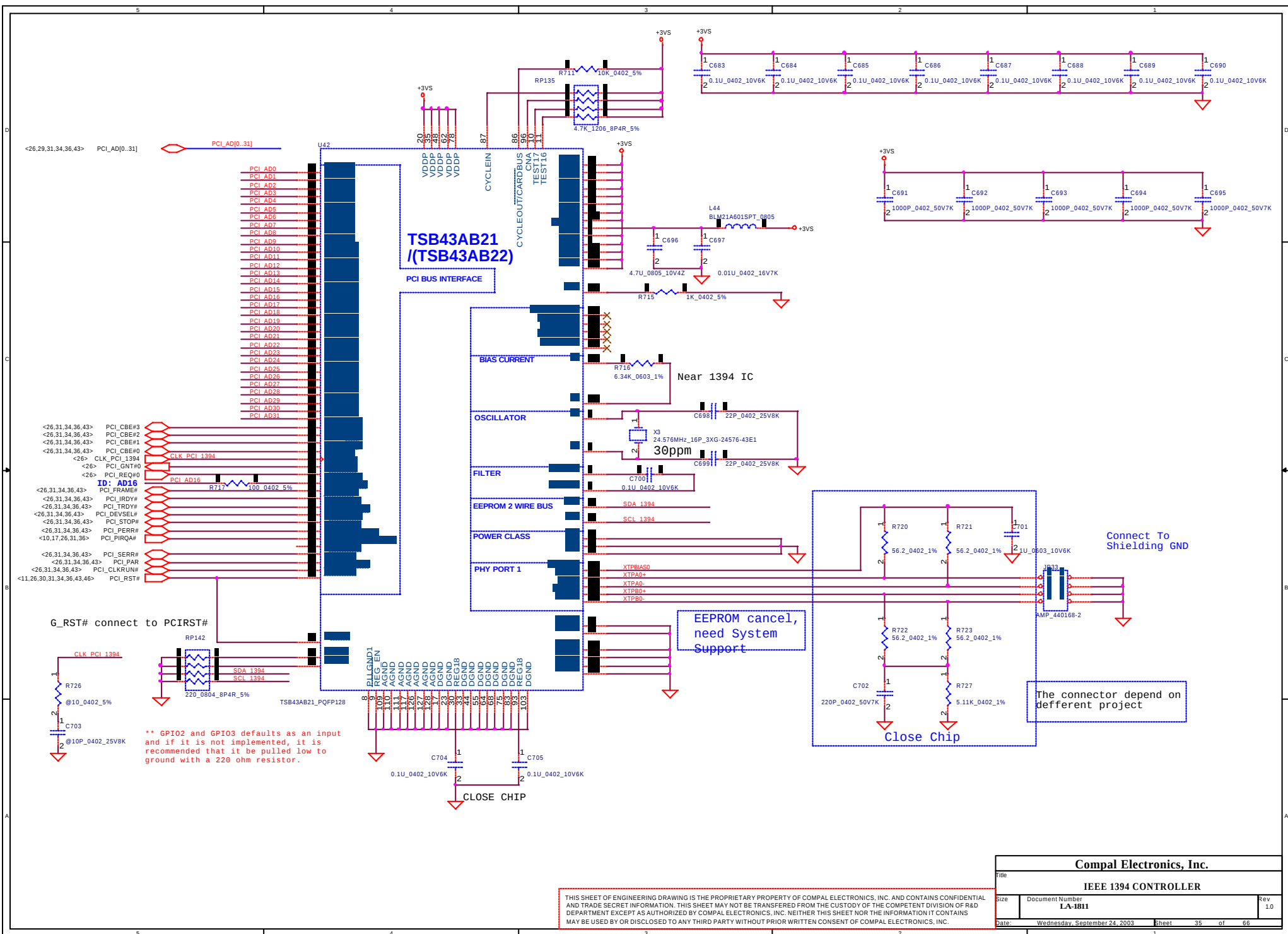


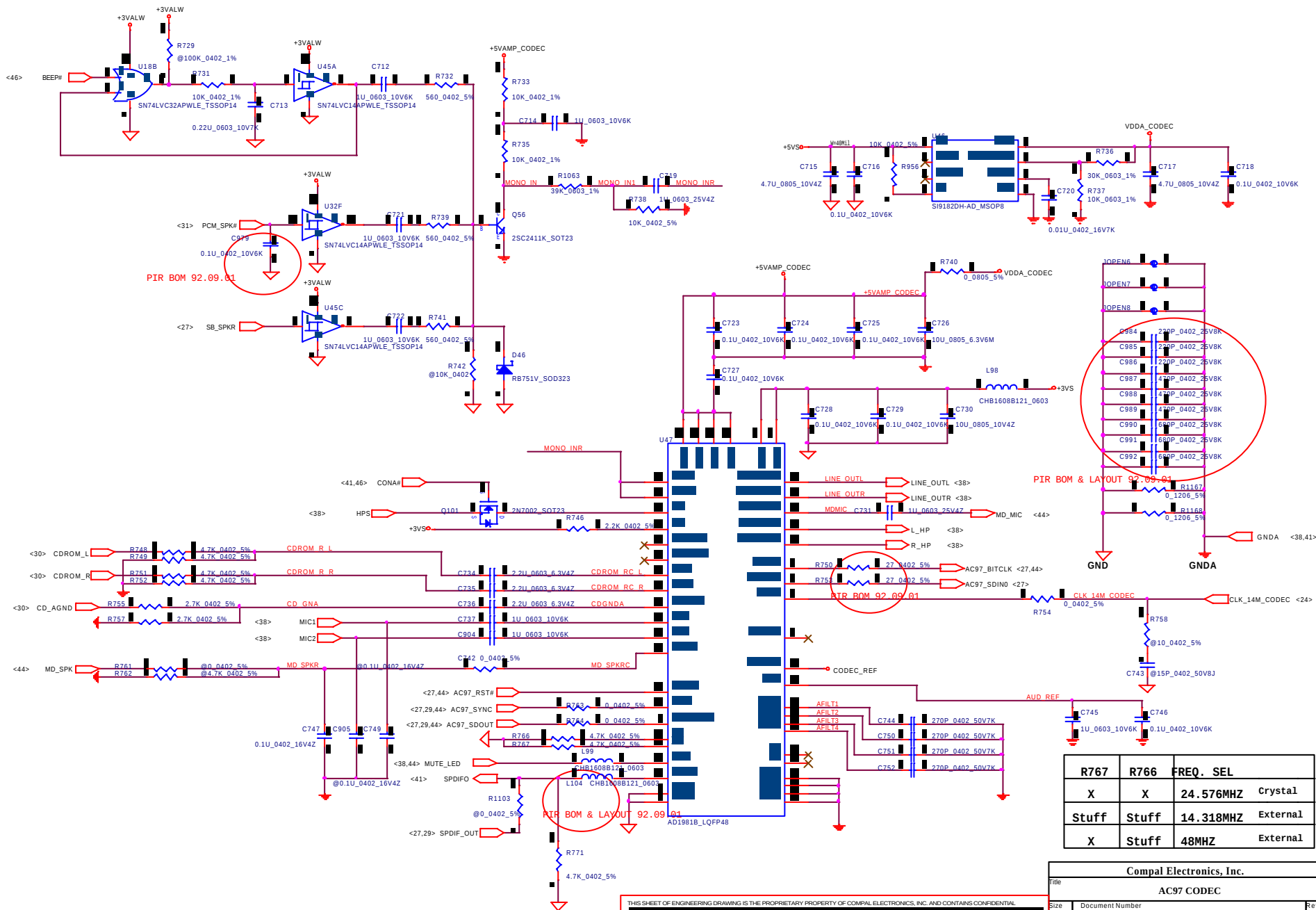
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
Title			
CARD BUS SOCKET			
Size	Document Number	Rev	
	LA-1811	1.0	
Date	Wednesday, September 24, 2003	Sheet	32 of 66

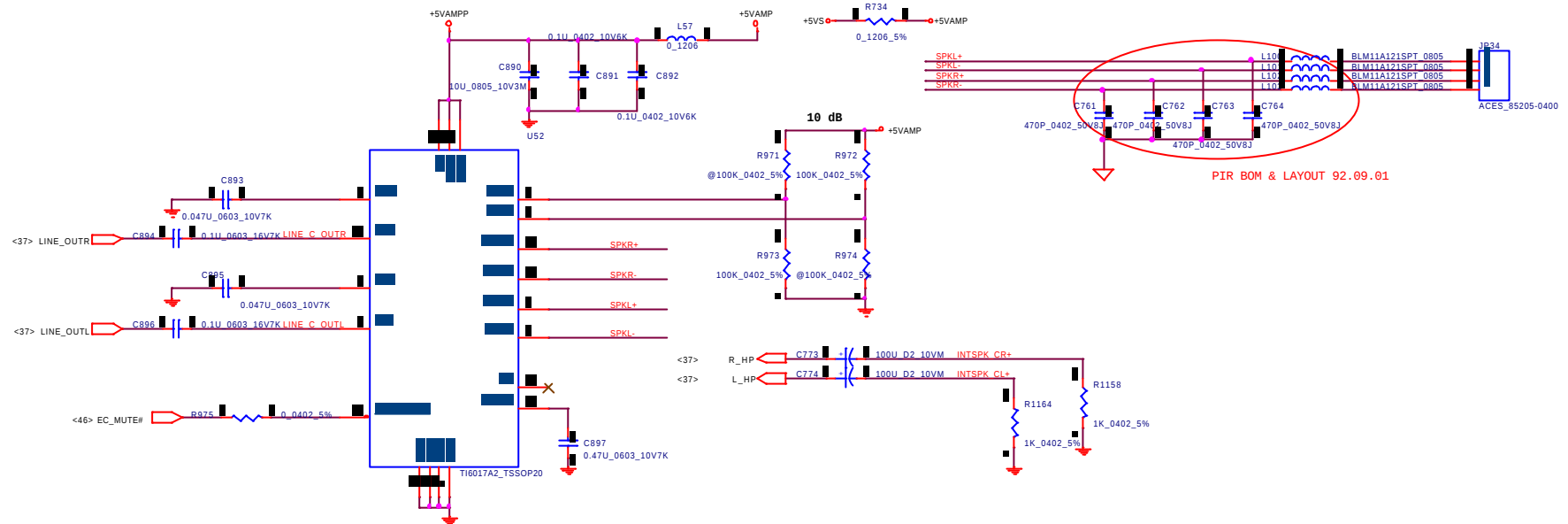




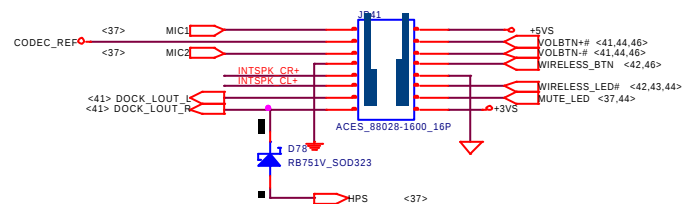




THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



AUDIO CONNECTOR



Gain Settings		
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

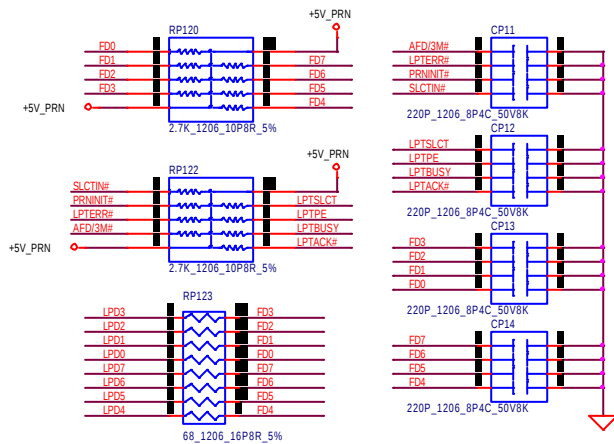
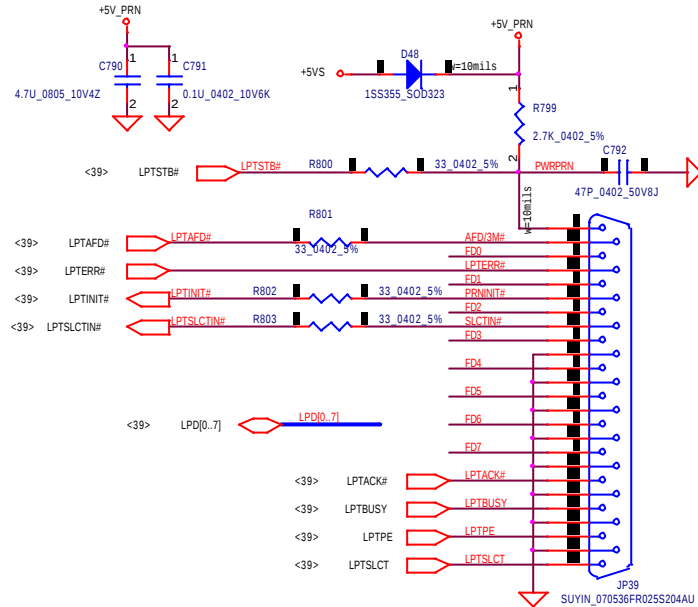
HEADPHONE OUT/LINE OUT

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE KEPT SECRET AND NOT DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

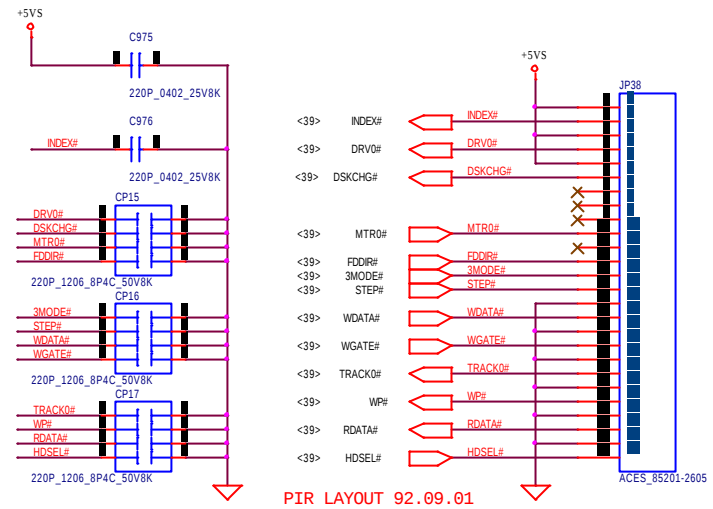
Compal Electronics, Inc.		
AMP & Audio Jack		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 38 of 66

Wednesday, September 24, 2003

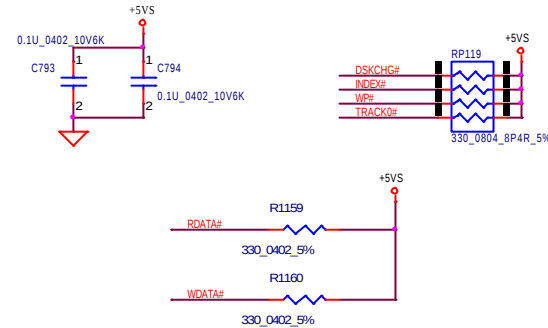
Parallel Port



FDD CONN.



PIR LAYOUT 92.09.01



Compal Electronics, Inc.

File: Parallel port and FDD

Size: B Document Number LA-1811

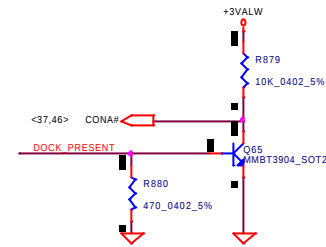
Date: Wednesday, September 24, 2003

Sheet 40 of 66

Rev 1.0

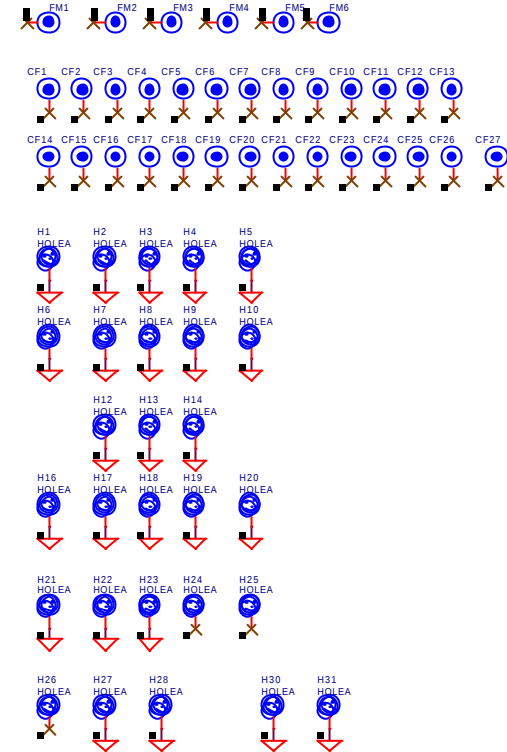
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

SPR 36 PIN For X7

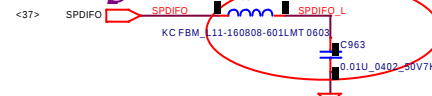


EMI Clip PAD

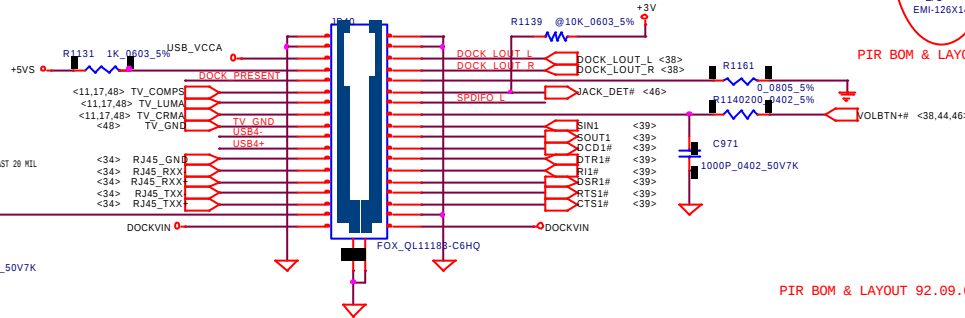
PIR BOM & LAYOUT 92.09.01



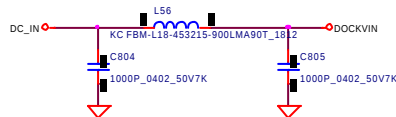
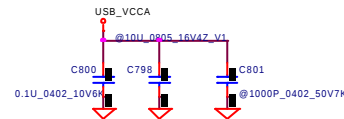
PIR BOM & LAYOUT 92.09.01



Note: PLACE CLOSE TO SPR PORT (JP40)

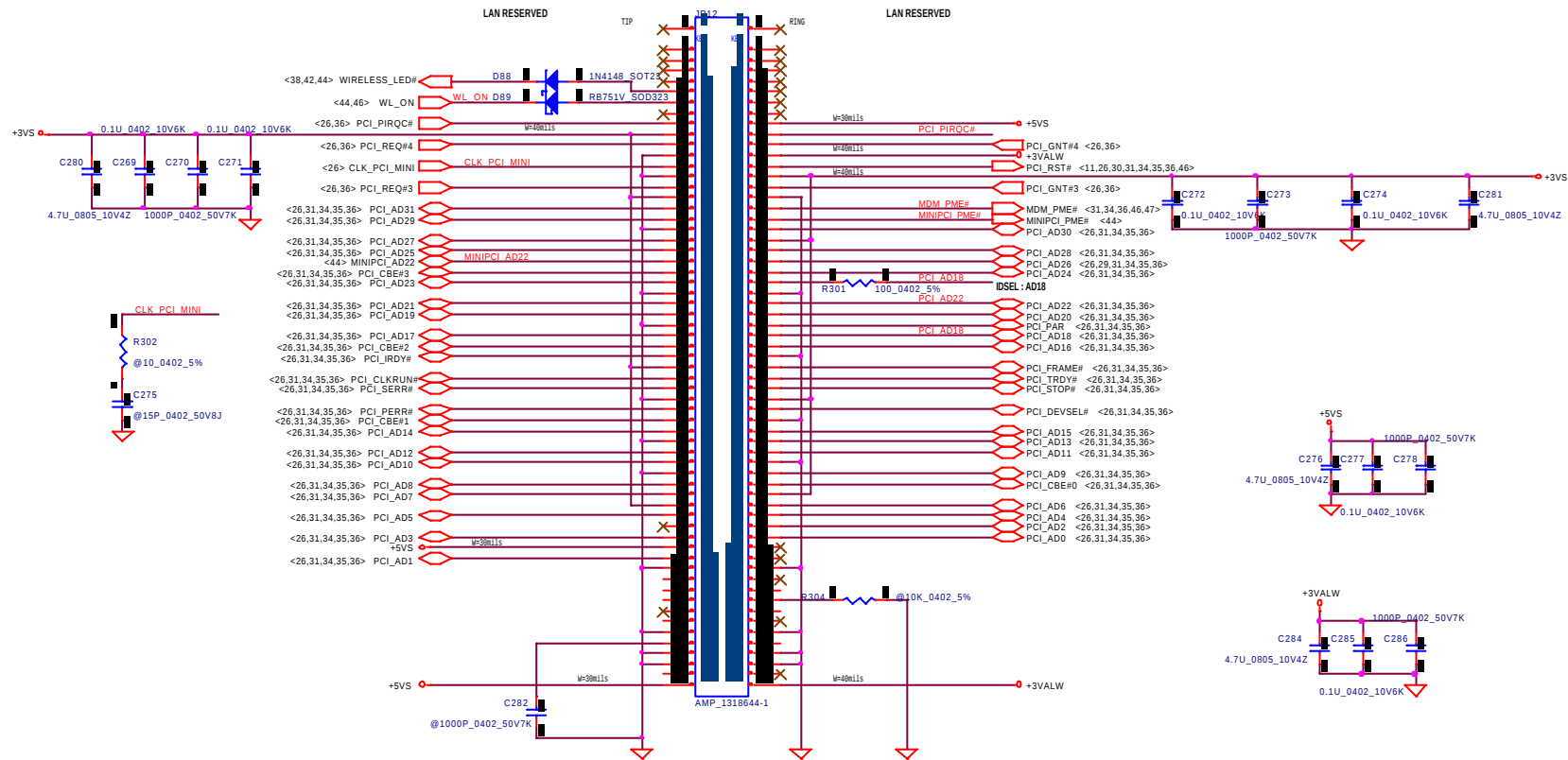


Note: PLACE CLOSE TO SPR PORT (JP40)



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
SPR Connector		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 41 of 66

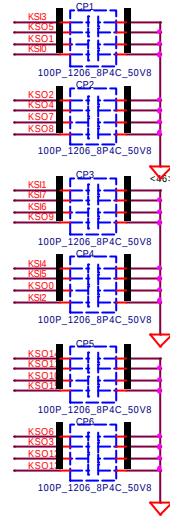
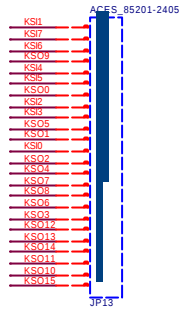


THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE KEPT SECRET AND NOT DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

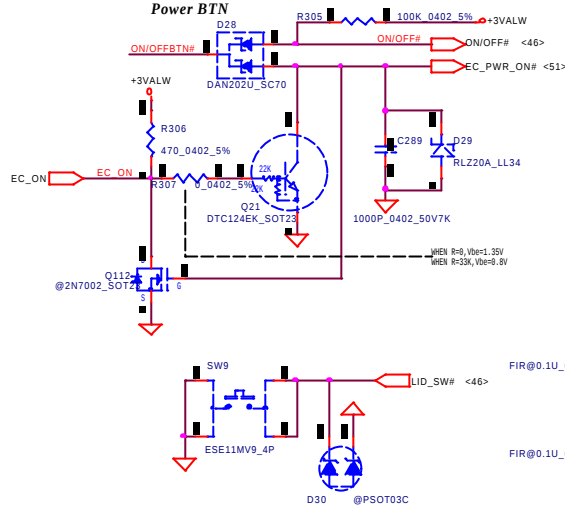
Compal Electronics, Inc.		
Mini PCI Slot		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 43 of 66

INT_KBD CONN.

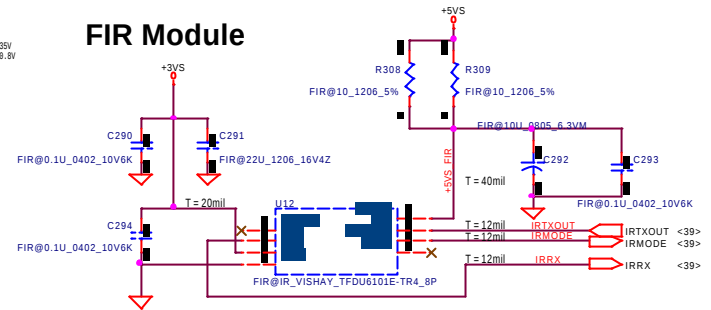
KS1[0..7] <KS1[0..7] <42,46>
KS0[0..15] <KS0[0..15] <46>



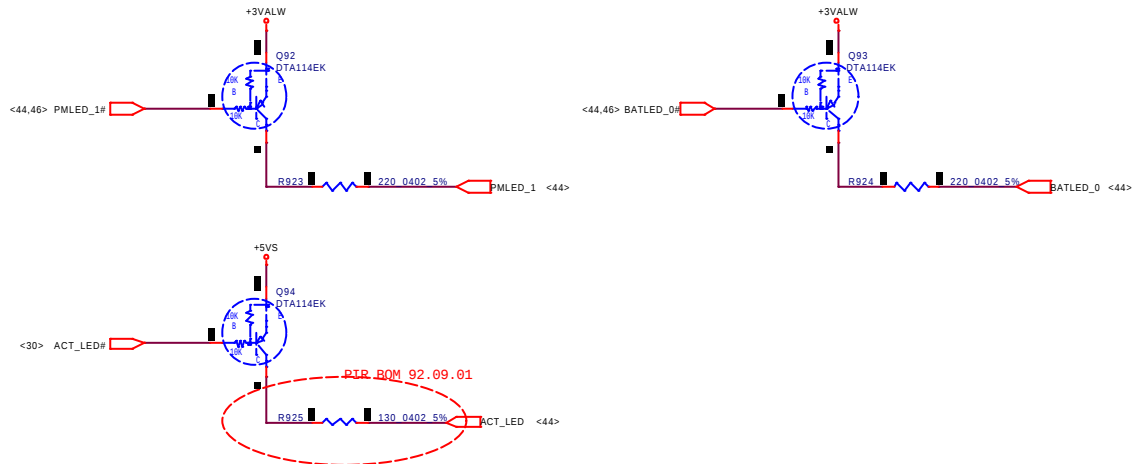
Power BTN



FIR Module

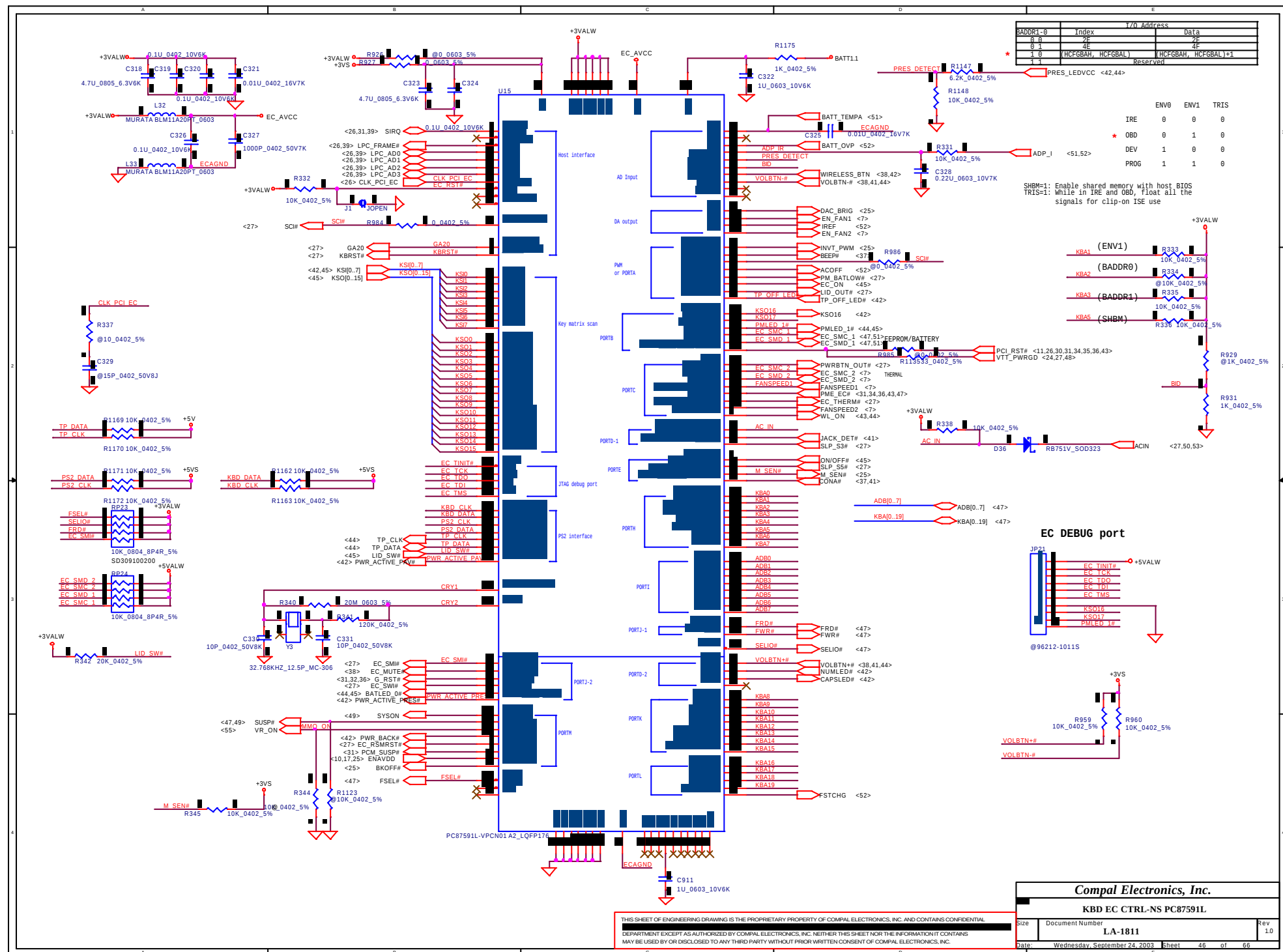


Touch Pad & Status LED Conn.



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
KBD,ON/OFF,T/P,LED & FIR		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 45 of 66

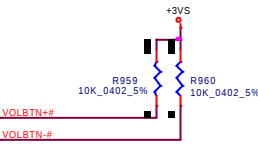
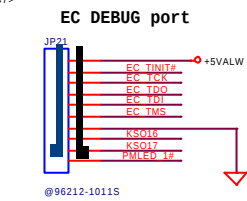


Y/N Address		
BADDR1-0	Index	Data
0 0	2E	2E
0 1	4F	4F
1 0	(HCFG8AH, HCFG8AL)	(HCFG8AH, HCFG8AL)+1
1 1	Reserved	

	ENV0	ENV1	TRIS
IRE	0	0	0
OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

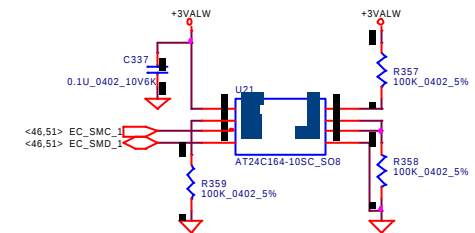
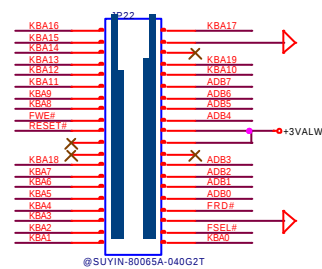
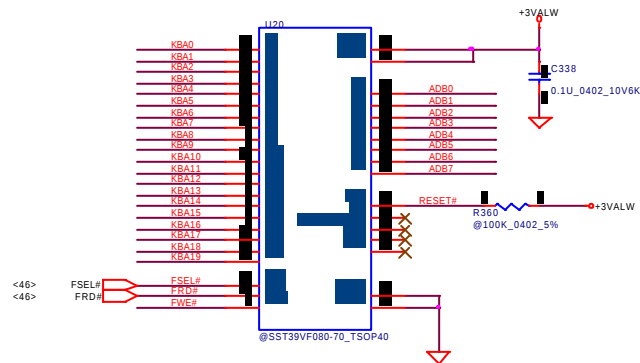
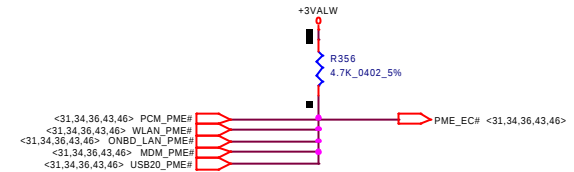
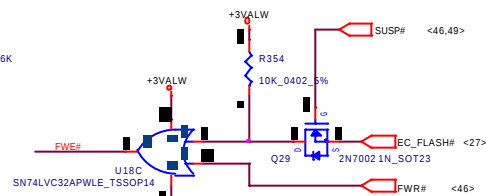
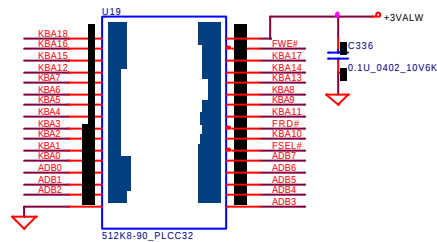
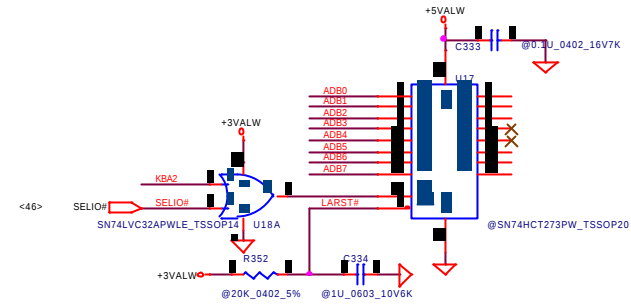
KBA1 (ENV1)	R333	10K_0402_5%
KBA2 (BADDR0)	R334	@10K_0402_5%
KBA3 (BADDR1)	R335	10K_0402_5%
KBA5 (SHBM)	R336	10K_0402_5%



Compal Electronics, Inc.		
KBD EC CTRL-NS PC87591L		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	
Sheet	46	of 66

<46> ADB[0..7] ADB[0..7]
<46> KBA[0..19] KBA[0..19]

OUTPUT

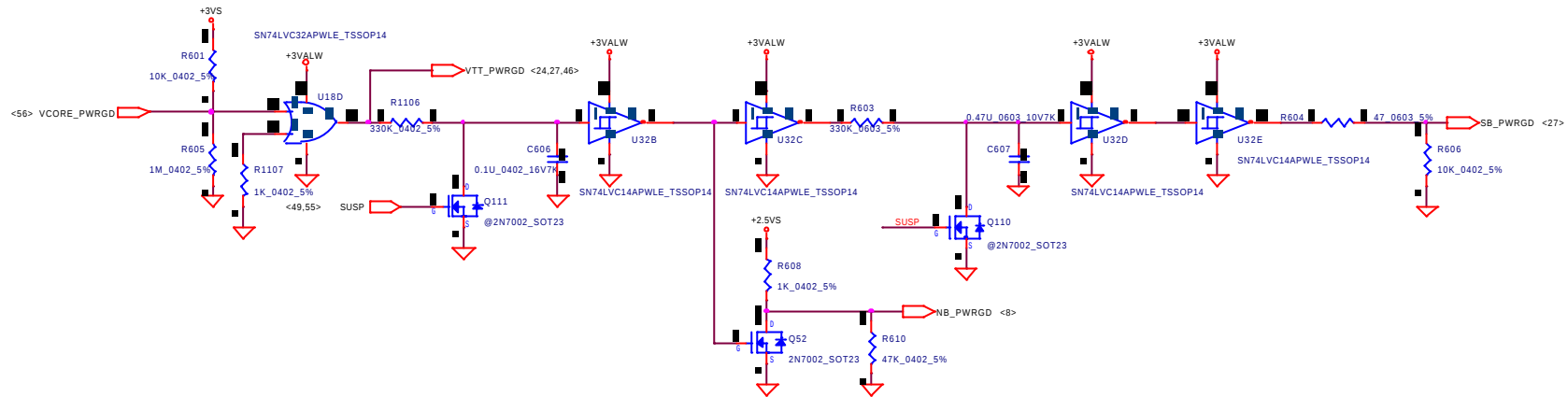


Compal Electronics, Inc.

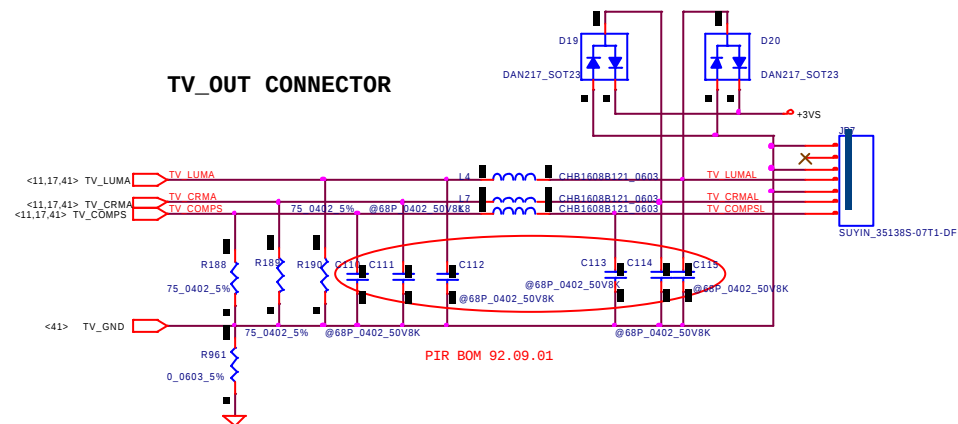
BIOS & EC I/O Port

Size	Document Number	Rev
	LA-1811	1.0
Date:	Wednesday, September 24, 2003	Sheet 47 of 66

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



TV_OUT CONNECTOR



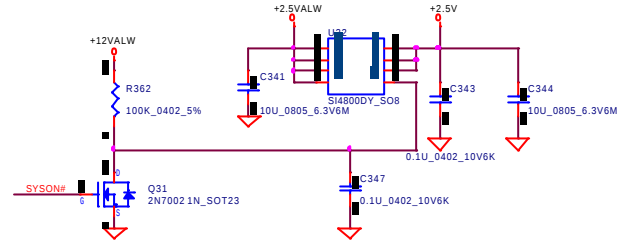
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

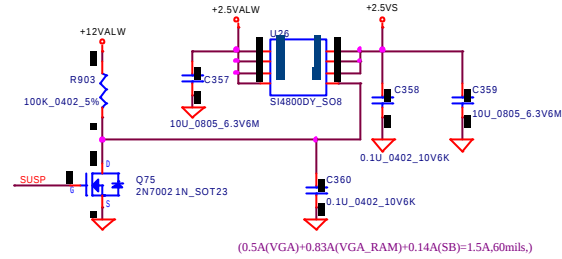
POWER GOOD & P/S2 CKT

Size	Document Number	Rev
	LA-1811	1.0
Date:	Wednesday, September 24, 2003	Sheet 48 of 66

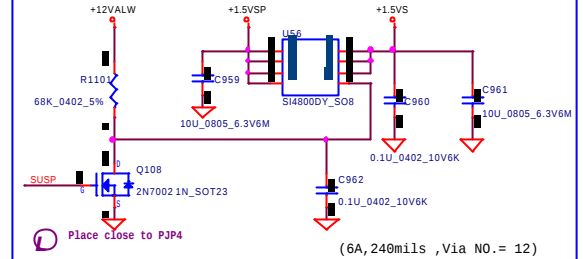
+2.5VALW to +2.5V Transfer



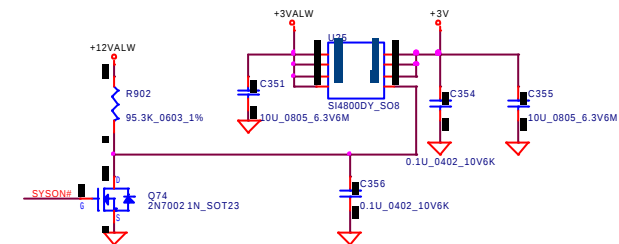
+2.5V to +2.5VS Transfer



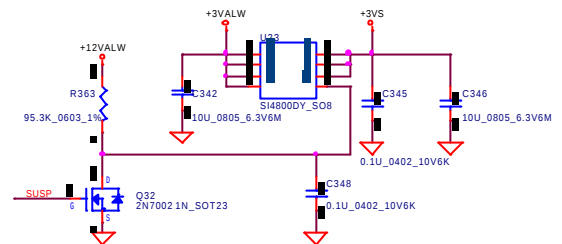
+1.5VSP to +1.5VS Transfer



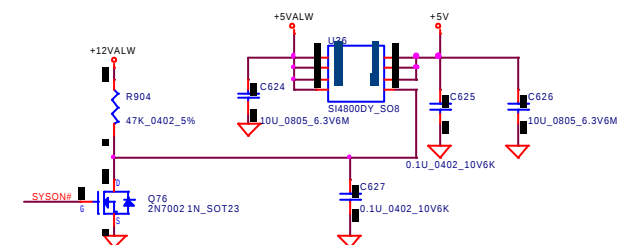
+3VALW to +3V Transfer



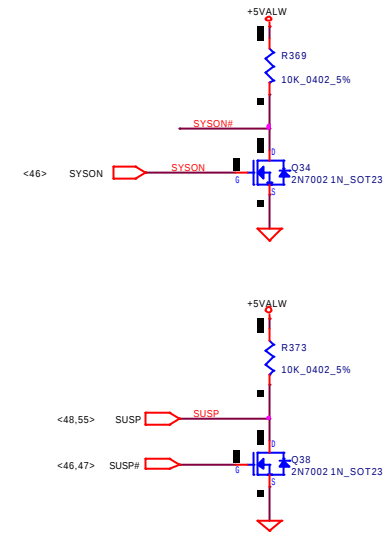
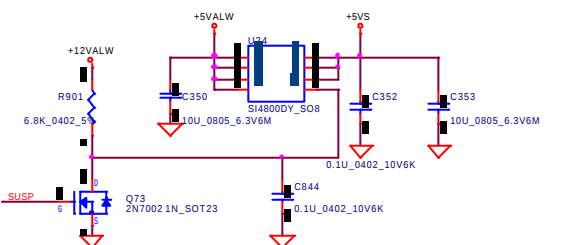
+3VALW to +3VS Transfer



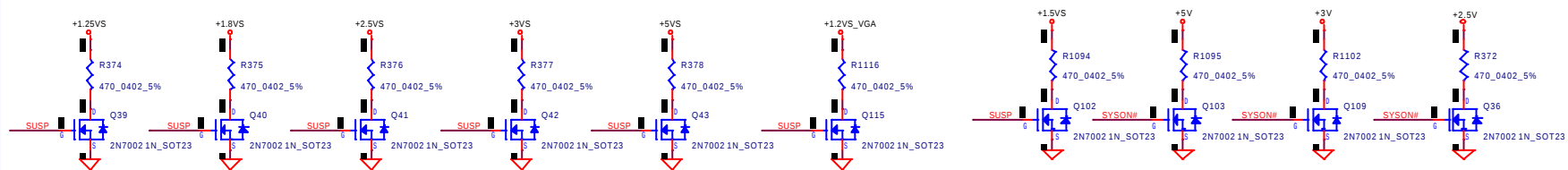
+5VALW to +5V Transfer



+5VALW to +5VS Transfer



Discharge circuit

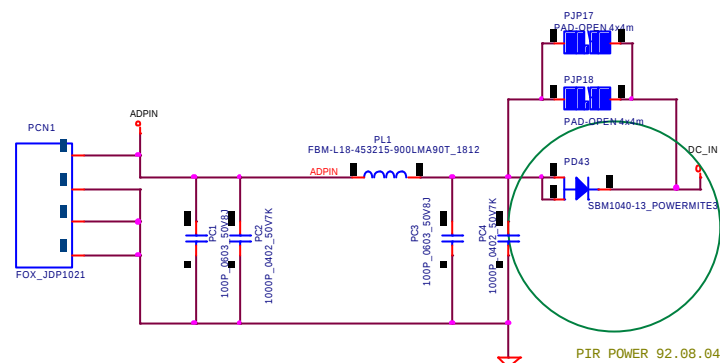


Compal Electronics, Inc.

DC/DC Circuits

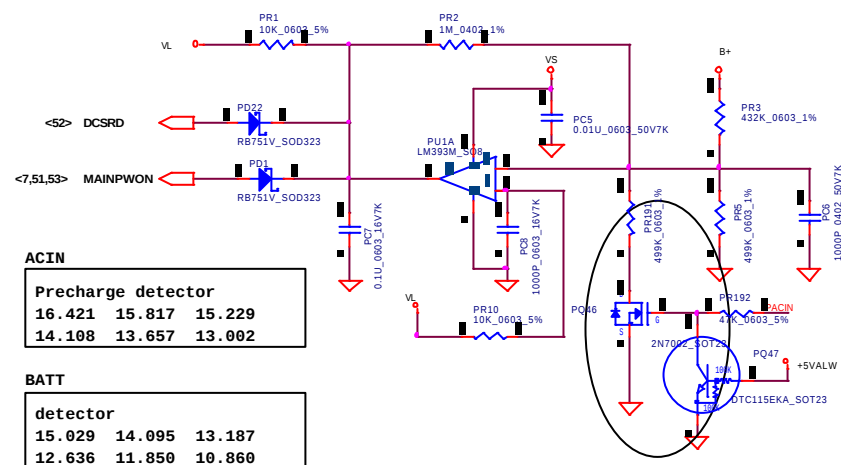
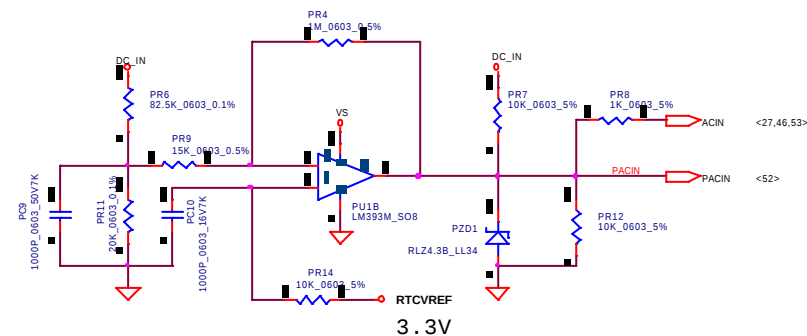
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE KEPT SECRET AND NOT DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Size Document Number LA-1811 Rev 1.0 Date Wednesday, September 24, 2003 Sheet 49 of 66



Vin Detector

17.788	17.438	17.090
17.277	16.928	16.585



ACIN

16.421	15.817	15.229
14.108	13.657	13.002

BATT

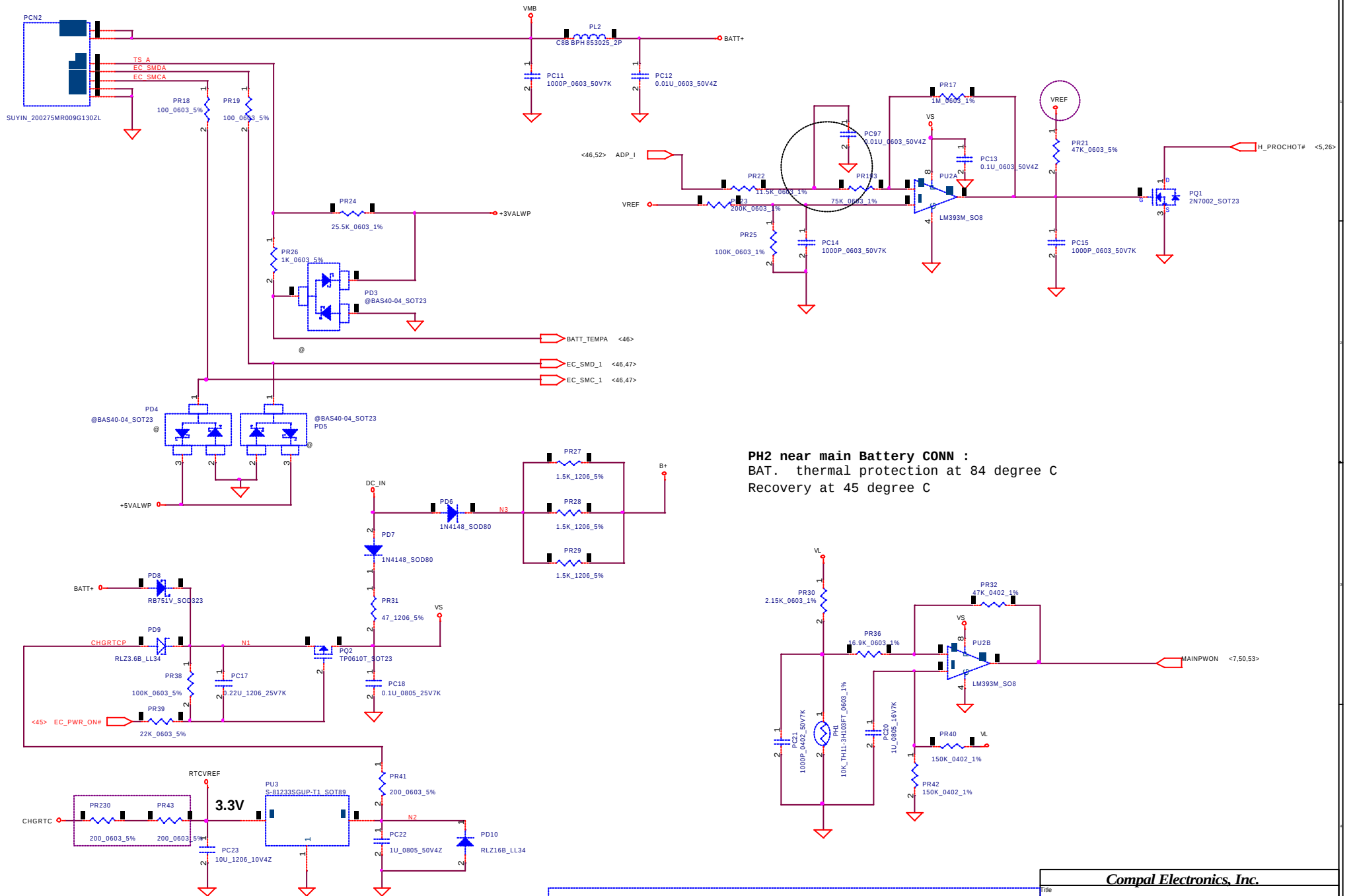
15.029	14.095	13.187
12.636	11.850	10.860

Compal Electronics, Inc.

Detector

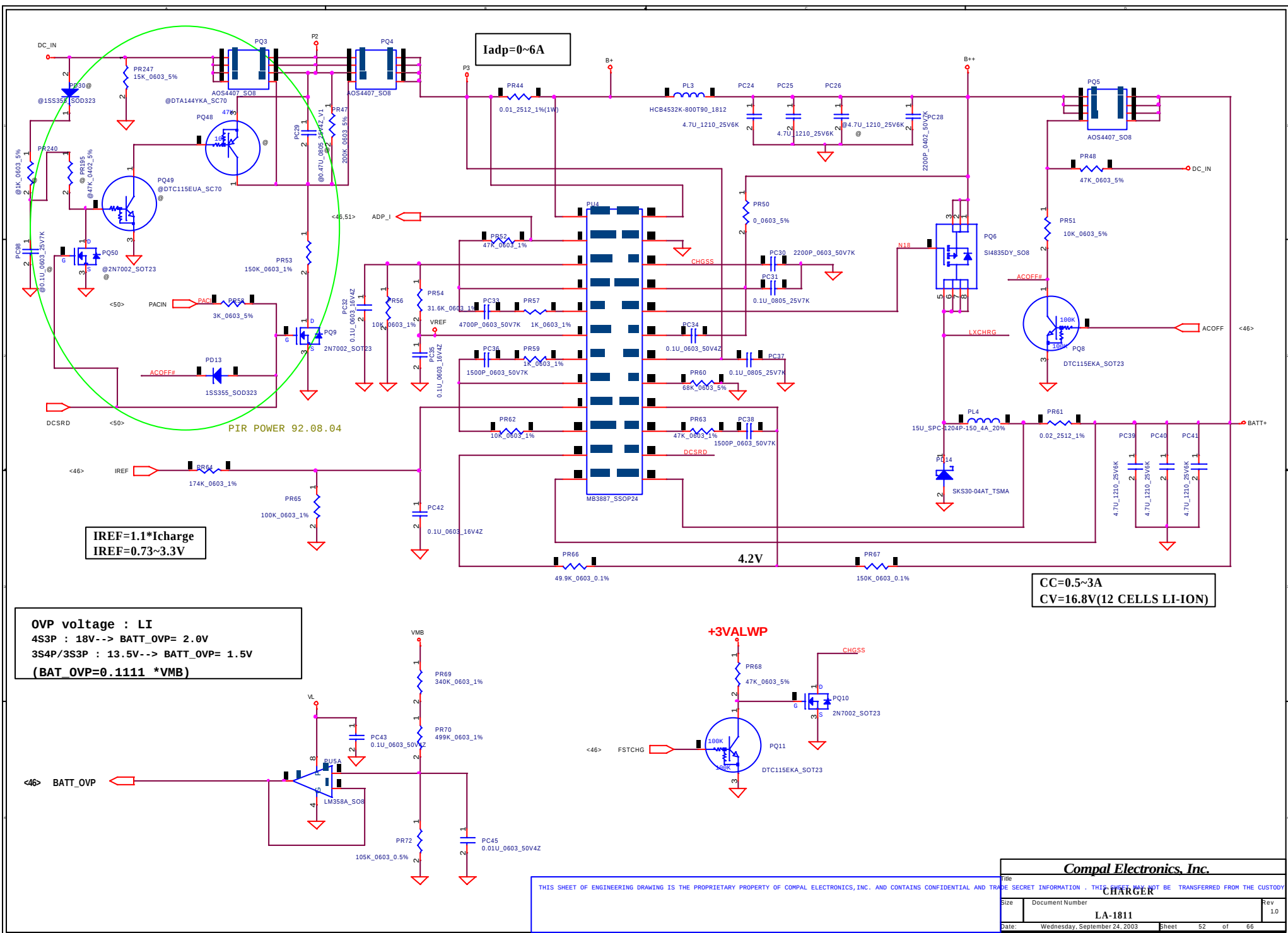
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

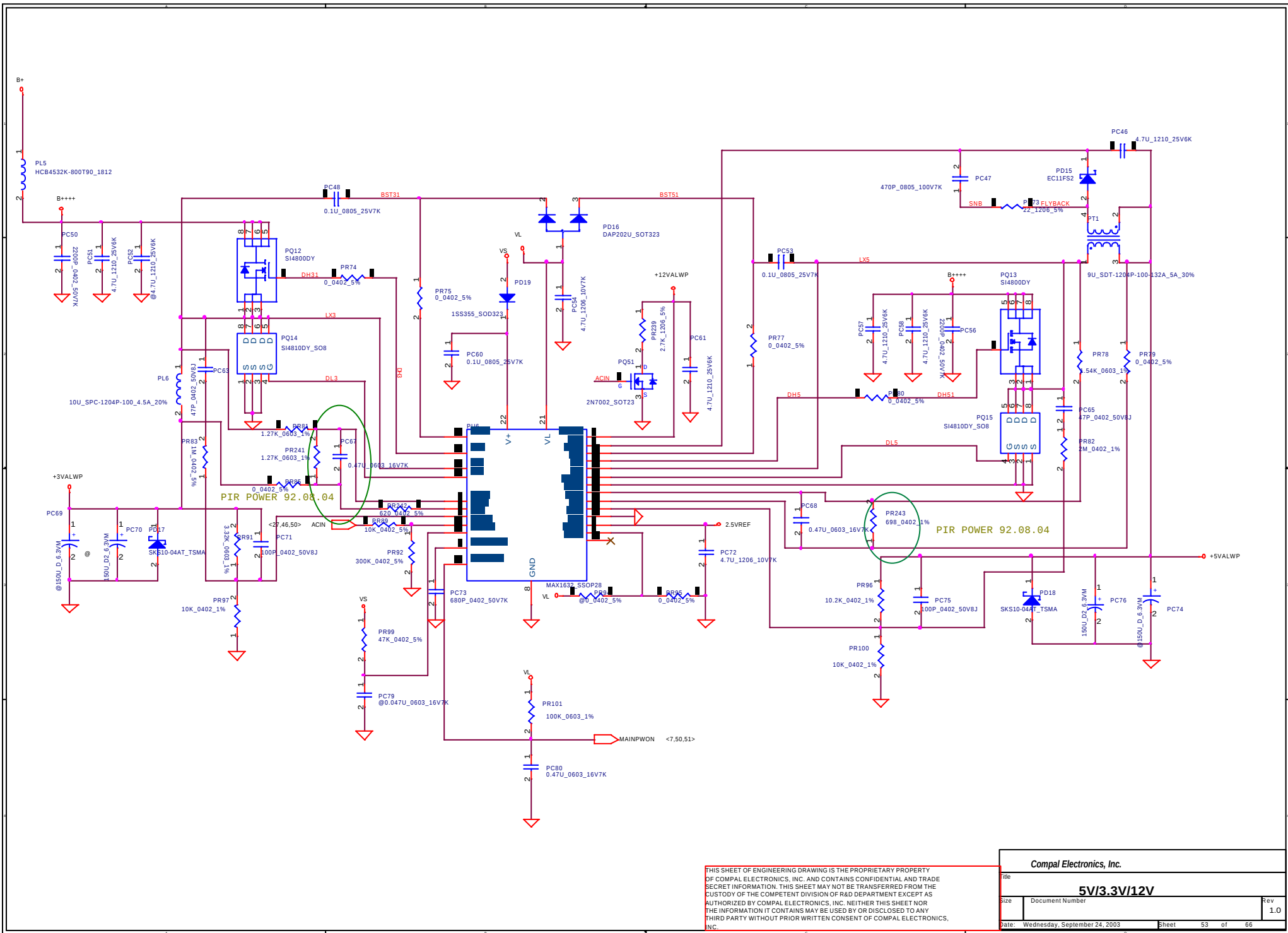
Size	Document Number	Rev
		1.0
Date	Wednesday, September 24, 2003	Sheet 50 of 66

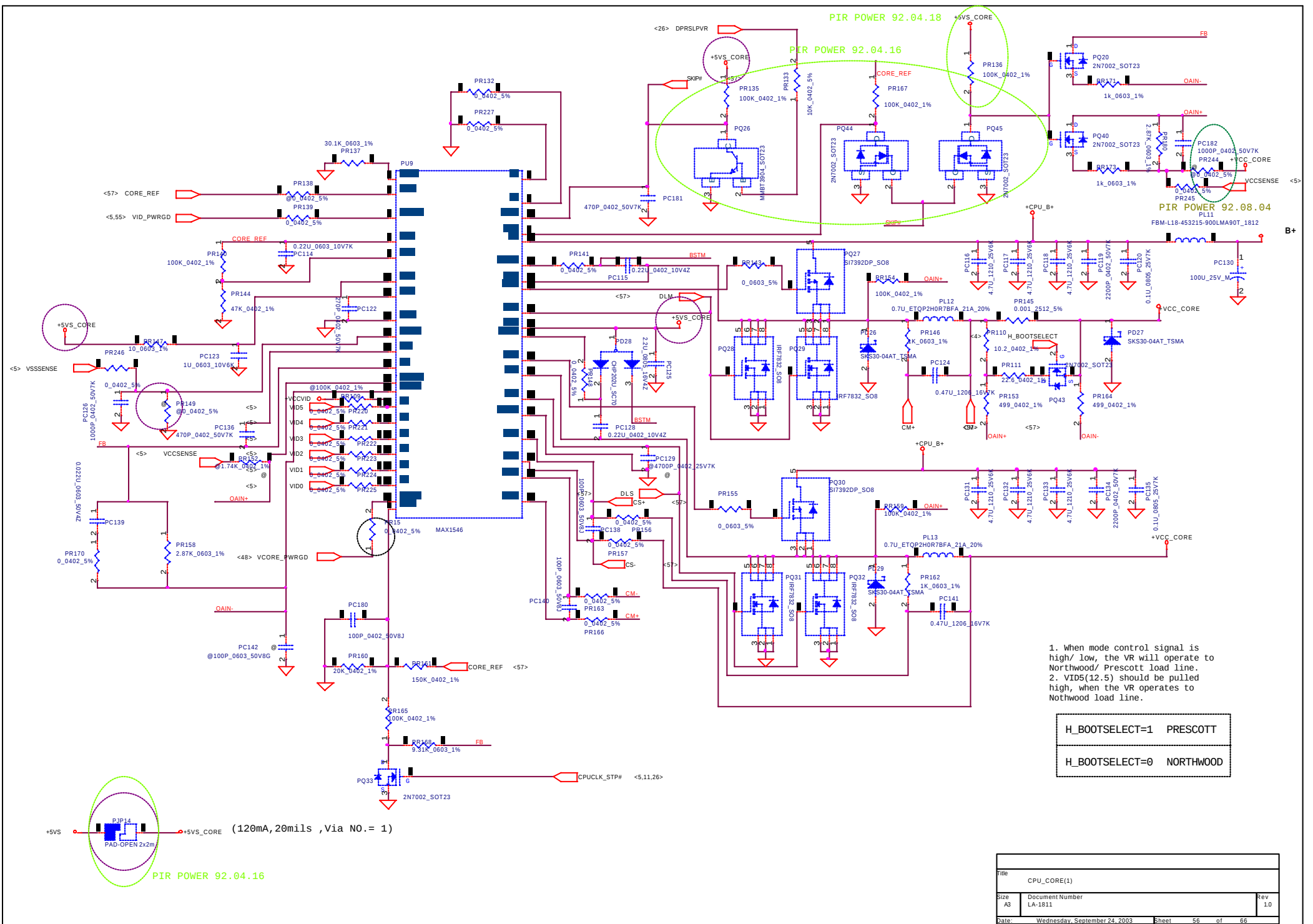


THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DI

Compal Electronics, Inc.			
Title		BATTERY CONN / OTP	
Size	Document Number	LA-1811	
Date	Wednesday, September 24, 2003	Sheet	51 of 66
Rev	1.0		







Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
------	-------	-------	------	------------------	-------------------	----------------------	------

Compal Electronics, Inc.			
Changed-List History-1			
Size	Document Number		Rev
	LA-1811		1.0
Date:	Wednesday, September 24, 2003	Sheet	58 of 66

BHR60 from DB-1 to DB-2 STEP LA-1811 REV:0.1 -> 0.2 Modify <92.03.17.~92.03.24. >

1.Add an independent power source for VGA chip because of ATI request . <Page 12> 92.03.17.

-Add U53(SI9185),C913,R1023,C912,C914 and related net . (Modify CKT,BOM&Layout)

2.Modify the Audio related schematic for Customer request . <Page 37> 92.03.17.

-Add Q101(2N7002);Del R948(2.2K_0402_5%);Modify R746(2.2K_0402_5%) . (Modify CKT,BOM&Layout)

3.Change the USB2.0 Controller chip from ATI to NEC and modify the net for Customer request . <Page 26,27,36,44> 92.03.18.

-Add U54(NEC_uPD720101F1-EA8),R1024~R1047,R1049,R1051,R1053,R1054,C915~C929, U55(AT24C02),RP147,RP148,R102,R1059,R1062;Del RP127 . (Modify CKT,BOM&Layout)

-Add R1048,R1050,R1052 . (Modify CKT&Layout)

4.Modify the Audio related schematic for Customer request . <Page 37,38> 92.03.20.

-Add R1063(39K_0603_1%);Del R768(0_1206_5%) . (Modify CKT,BOM&Layout)

-Change C894,C896 from 1U_0603_10V6K to 0.1U_0603_16V7K . (Modify CKT&BOM)

-Change R974 from @100K_0402_5% to 100K_0402_5% . (Modify CKT&BOM)

-Change R972 from 100K_0402_5% to @100K_0402_5% . (Modify CKT&BOM)

-Change JP41.3 from GND A to +5VAMP . (Modify CKT&Layout)

5.Modify the MiniPCI and BlueTooth conn related schematic for Customer request . <Page 43,44> 92.03.21.

-Add R1083,R1084,R1085(@0_0402_5%) . (Modify CKT&Layout)

-Change R300 from 100_0402_5% to @100_0402_5% . (Modify CKT&BOM)

6.Modify the USB2.0 related for Compal ATI/NEC Dual Layout request . <Page 27,44> 92.03.21.

-Add R1069,R1070,R1072,R1073,R1074,R1076,R1077,R1078,R1092,R1093(NEC@0_0402_5%) . (Modify CKT,BOM&Layout)

-Change R976,R977,R978,R979,R982,R983 from 0_0402_5% to ATI@0_0402_5% and the net . (Modify CKT,BOM&Layout)

-Add R1071,R1075,R1090,R1091(ATI@0_0402_5%) . (Modify CKT&Layout)

7.Add De-coupling capacitor for AGP power pins on RC300M and VGA chip because of ATI request . <Page 10> 92.03.21.

-Add C937~C946,C862,C863,C865~C871(0.1U_0402_10V6K) . (Modify CKT,BOM&Layout)

8. Reserve the SMBus1/2 swap Resistors for ATI request . <Page 27> 92.03.23.

-Add RP150(0_0404_4P2R_5%) . (Modify CKT,BOM&Layout)

-Add RP149(@0_0404_4P2R_5%) . (Modify CKT&Layout)

9. Add the power source +5V and +1.5VS discharge circuit for ATI request . <Page 49> 92.03.23.

-Add R1094,R1095(470_0402_5%),Q102,Q103(2N7002 1N_SOT23) . (Modify CKT,BOM&Layout)

10. Modify the ON1 related to speed up the power sequence for ATI request . <Page 48,54> 92.03.23.

-Add R1096,R1097(10K_0402_5%),Q1043(2N7002 1N_SOT23),Q105(DTC124EK_SC59); Del PR113(47K),PC183(0.1U) . (Modify CKT,BOM&Layout)

11. Modify power source CAP.'s value by Brian . <Page 26,49> 92.03.24.

-Change C347,C360 from 0.1U_0402_10V6K to 3900P_0402_50V7K;C356,C348 from 0.01U_0402_16V7K to 2200P_0402_25V7K . (Modify CKT&BOM)

-Add C956(180P_0603_50V8J) . (Modify CKT,BOM&Layout)

12. Del Via Hole on schematic for ME modify . <Page 41> 92.03.24.

-Del H15(H_C374D295),H29(H_C197D91) . (Modify CKT,BOM&Layout)

13.Modify the MiniPCI and BlueTooth conn related for Customer request . <Page 43,44> 92.03.24.

-Change R1083,R1084 from @0_0402_5% to 100_0402_5% . (Modify CKT&BOM)

-Add C957(10U_0805_10V3M),C958(0.1U_0402_10V6K) . (Modify CKT,BOM&Layout)

14.Swap the USB20*P3* and USB20*P5* for Customer request . <Page 44> 92.03.24.

-Modify R1079~R1082,JP43,R980,R981's connection . (Modify CKT&Layout)

15.Modify the schematic after rev0.1 debug by Brian . <Page 12,17,26,29> 92.03.24.

-Change R1010 from @0_0603_5% to 0_0603_5%;R1011 from 0_0603_5% to @0_0603_5%; Q15 from 2SC2411K_SOT23 to @2SC2411K_SOT23;R145 from 4.7K_0402_5% to @4.7K_0402_5%; R146 from @4.7K_0402_5% to 4.7K_0402_5%;R967 from @10K_0402_5% to 10K_0402_5%; R833 from @0_0402_5% to 0_0402_5% . (Modify CKT&BOM)

16.Modify the schematic H_BOOTSELECT related by Power Team . <Page 04> 92.03.25.

-Add Q106(2SC2411K_SC59),Q107(MMBT3904_SOT23),R1099,R1100(47K_0402_5%) . (Modify CKT,BOM&Layout)

-Change R899 from 0_0402_5% to 22K_0402_5%;R900 from @0_0402_5% to 100K_0402_5% . (Modify CKT&BOM)

17.Add a power transfer circuit to fix +1.5VS leakage issue . <Page 49> 92.03.25.

-Add U56(SI4800DY_SO8),Q108(2N7002 1N_SOT23),R1101(100K_0402_5%),C960(0.1U_0402_10V6K), C961(10U_1206_6.3V6M),C962(3900P_0402_50V7K) . (Modify CKT,BOM&Layout)

18. Modify power source Resistor and CAP.'s value for power sequence . <Page 49> 92.03.26.

-Change C347,C360,C962 from 3900P_0402_50V7K to 0.1U_0402_10V6K;C356,C348 from 2200P_0402_25V7K to 0.1U_0402_10V6K;C627,C844 from 1000P_0402_50V7K to 0.1U_0402_10V6K . (Modify CKT&BOM)

-Change R903,R362 from 100K_0402_5% to 91K_0402_5% . (Modify CKT&BOM)

-Change R902,R363 from 100K_0402_5% to 95.3K_0603_1% . (Modify CKT,BOM&Layout)

19. Modify the ON1 related to speed up the power sequence for ATI request by Brian/James/CT . <Page 48,54> 92.03.26.

-Del R1096,R1097(10K_0402_5%),Q1043(2N7002 1N_SOT23),Q105(DTC124EK_SC59) . (Modify CKT,BOM&Layout)

20. Add the power source +3VS discharge circuit by Brian . <Page 49> 92.03.26.

-Change Q42 from @2N7002 1N_SOT23 to 2N7002 1N_SOT23 . (Modify CKT&BOM)

21. Change the Resistor's value for ATI recommend . <Page 17 > 92.03.26.

-Change R264 from 169_0603_1% to 2N7002 1N_SOT23 . (Modify CKT&BOM)

22. Correct material layout footprint and pin define . <Page 26,34 > 92.03.26.

-Change Y1,Y3 PCB Footprint and JP32 pin define . (Modify CKT&Layout)

23. Add the power source +3V discharge circuit for ATI request . <Page 49> 92.03.27.

-Add R1102(470_0402_5%),Q109(2N7002 1N_SOT23) . (Modify CKT,BOM&Layout)

24. Change the power sequence related part's power source by Brian . <Page 5,37,48> 92.03.27.

-Change U32's power source from +3VS to +3VALW . (Modify CKT&Layout)

25. Modify the power sequence related schematic for timing by Brian . <Page 48> 92.03.27.

-Change R605 from 1M_0402_5% to @1M_0402_5%;C606 from 1U_0603_10V6K to @1U_0603_10V6K . (Modify CKT&BOM)

-Add Q110(2N7002_SOT23) . (Modify CKT,BOM&Layout)

26. Modify the SPDIF related schematic for Customer request . <Page 37,41> 92.03.28.

-Add R1103(0_0402_5%),C963(0.01U_0402_50V7K) . (Modify CKT,BOM&Layout)

27. Modify the NEC USB2.0 Controller Chip related schematic for Customer request . <Page 36> 92.03.28.

-Add Y7(30MHZ_30PPM),R1105(100_0402_5%),C964(12P_0402_50V8J),C965(10P_0402_50V8K) . (Modify CKT,BOM&Layout)

-Add R1104(@0_0402_5%) . (Modify CKT&Layout)

-Change R1024 from 0_0402_5% to @0_0402_5% . (Modify CKT&BOM)

28. Update the material's Layout Footprint for error correction . <Page 36> 92.03.28.

-Update JP29,JP14,SW1,SW3~SW8,JP40,Q65 . (Modify CKT&Layout)

29. Modify the related schematic after Brian Review <Page 7,24,26,29,30,39,43,45> 92.03.31.

-Del R288(56_0402_5%) . (Modify CKT,BOM&Layout)

30. Modify the related schematic after Layout check <Page 44> 92.03.31.

-Modify JP16(RJ11 Conn.),5 and JP16.6 from GND to NC . (Modify CKT&Layout)

31. Update the material's Layout Footprint for error correction . <Page 41> 92.04.02.

-Update JP40 . (Modify CKT&Layout)

32. Modify the schematic for cost down . <Page 10,12,26,37> 92.04.04.

-Change to @(R1005,D79~D82,U53,C912,C913,R1023,Q98,R769,R771.) . (Modify CKT&BOM)

---PLEASE SEE NEXT PAGE

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL

INFORMATION. NO PART OF THIS SHEET OR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

H/W2 EE Dept. PIR SHEET(1)

Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	Sheet 59 of 66

BHR60 from DB-2 to SI-1 STEP LA-1811 REV:0.3 -> 0.4 EE Modify

<92.04.08.~92.04.18.>

1. J33 Connector JP33 Pin define sequence error. <Page 35> 92.04.08.

-Change JP33 sequence JP33.4->JP33.1, JP33.3->JP33.2, JP33.2->JP33.3, JP33.1->JP33.4. (Modify EE Circuit)

2.LED Circuit to Power Button(PRES)modify . <Page 42, Page 46> 92.04.09.

-Move Q66.1-R883-D56 -> Q62.1-R883-D56(PRES). (Modify EE Circuit)

-Rename Q62.2 net PWR_BACK# change to PWR_ACTIVE# connect to EC U15.119. (Modify EE Circuit)

3.Add +1.2VS_VGA Discharge Circuit. <Page 49> 92.04.09.

-Add +1.2VS_VGA Discharge Circuit(R1116 , Q115 to SUSP). (Modify EE Circuit)

4.Add 3VDDCDA & 3VDDCCL pull hing CRT_VCC circuit. <Page 25> 92.04.09.

-Add Q13.1-R1117 to +CRT_VCC & Q14.1-R1118 to CRT_VCC. (Modify EE Circuit)

5.PCMCIA U37 NET S1_CE2# & S1_CE1# Sweep. <Page 31> 92.04.09.

6. MDC(JP17) Net AC97_SData_In1/AC97_SData_In2 to AC97_Data_In. <Page 44> 92.04.10.

-Update BOM add R326. (Modify EE Circuit)

7. Change NB DDR Bus Net for basic on AT1 NB DDR Bus Layout rule. <Page 9, 14, 15, 16> 92.04.11.

-Add R1122(DDRA_CKE_R3), R1121(DDRA_CKE_R2). (Modify EE Circuit)

-Del R399(DDRA_CS#0), R400(DDRA_CS#2). (Modify EE Circuit)

8. Check BOM USB OUVUR R893&R895 470K change to 330K. <Page 44> 92.04.12.

9. Add SUSP# pull Down. <Page 46> 92.04.14.

-Add EC U15.115 to SUSP# pull Down @R1123 to GND. (Modify EE Circuit)

10. Add CPUCLK_STP# pull High Circuit. <Page 26, 5> 92.04.14.

-BOM Q113 -> @ , Add R1124 to Q113.1 & Q113.3. (Modify EE Circuit)

-Add CPUCLK_STP# pull High @R1126 to +3VS . (Modify EE Circuit)

-Add CPUCLK_STP# serial resistor R1125 to Q96.2. (Modify EE Circuit)

11. Change BOM R585 75 -> 0 & R996 33 -> 68(REFCLK1_NB). <Page 11, 24> 92.04.15.

12. SIO Circuit All Power Plan +3V -> +3VS. <Page 39> 92.04.15.

13. Add NEC USB Corstralor U54.P19(SRMOD) pull Low. <Page 36> 92.04.16.

-Add USB Constralor U54.P19(SRMOD) pull Low R1127 to GND. (Modify EE Circuit)

-Update BOM R1046 -> @. (Modify EE Circuit)

14. Add @R1132 pull High +3V(RTS1#) & @RP153 pull High +3V(CTS1#/DSR1#/DCD1#/RI1#). <Page 39> 92.04.16.

15. Change BOM C364, C23, C24, C40, C798 47U -> 22U. <Page 8,28,41> 92.04.17.

16. Change BOM R380 430 -> 412(U27.A9/CPU_RSET#). <Page 8> 92.04.17.

17. Change BOM D57 HSMG-C170 -> 12-21SYGC/S530-E1, R1014 @ -> Del @. <Page 42> 92.04.17.

18. Change BOM C191 4.7U -> 2.2U. <Page 17> 92.04.17.

19. Change BOM C202,C931 10U -> 2.2U. <Page 20> 92.04.17.

20. Change BOM R636 100K-> @10K, R637 100K-> @10K, R665 -> @. <Page 33> 92.04.17.

21. Change MC_CD# - D44.3(SA_A25) -> D45.2, D44.2(SA_A22). <Page 33> 92.04.17.

22. Add R1135 -> VTT_PWRGD(U15.165). <Page 46> 92.04.18.

23. Add R1136, Q116, R1137, R1138 for pull High +3VS(CARD_LED#). <Page 42> 92.04.18.

24. Change BOM Q67 -> @, R884 -> @(CARD_LED#). <Page 42> 92.04.18.

25. Change BOM C966 22U -> 0.1U. <Page 18> 92.04.18.

26. Change BOM C916 -> @, C917 -> @. <Page 36> 92.04.18.

27. Change BOM R1019 -> @(U47.17 JS1) pull High. <Page 37> 92.04.18.

28. Change BOM R264 47 -> 137(U6.PM27 AGPTST). <Page 17> 92.04.18.

BHR60 from DB-2 to SI-1 STEP LA-1811 REV:0.3 -> 0.4 Layout Modify

<92.04.08.~92.04.18.>

1.FDD Connector JP38 PCB Footprint error. <Page 40> 92.04.09.

-Check JP38 ACES_85201-2605_26P. (Modify Layout)

2.Power Switch U53 PCB Footprint error. <Page 12> 92.04.09.

-Change U53 SI9185_MLP33-8->MSOP8. (Modify Layout)

3.Crystal Y4 PCB Footprint error. <Page 11> 92.04.09.

-Change Y4 Y_TXC_6X1430004201_20P->KDS_DSX840GA. (Modify Layout)

4.USB Key Connector JP46 Part error. <Page 44> 92.04.09.

-Change JP46 S W-CONN ACES_85205-0400_4P P1.25(ACES_85205-0400_4P)->S H-CONN ACES_85201-0405_4P P1.0(ACES_85201-0405_4P). (Modify Layout)

5. Change BOM & Layout LED D57 Footprint . <Page 42> 92.04.15.

-Change D57 HSMG-C170 to LED_12-21SYGC_S530-E1_TR8. (Modify Layout)

6. Change Layout Keyboard Connector JP13 Footprint. <Page 45> 92.04.15.

-Change JP13 ACES_85201-2402_24P -> ACES_85201_2405_24P. (Modify Layout)

7. Change Layout FrontSideboard Connector JP42 Footprint. <Page 44> 92.04.15.

-Change JP42 ACES_85201-1402_14P -> ACES_85201_1405_14P. (Modify Layout)

----PLEASE SEE NEXT PAGE

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL

INFORMATION. IT IS TO BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
H/W2 EE Dept. PIR SHEET(2)			
Size	Document Number		Rev
	LA-1811		1.0
Date	Wednesday, September 24, 2003		Sheet 60 of 66

BHR60 from DB-2 to SI-1 STEP LA-1811 REV:0.3 -> 0.4 EE Modify

<92.04.08.~92.04.18. >

29. Change U13.P1 <-> U13.P5, U14.P1 <-> U14.P5. <Page 43> 92.04.21.

30. Change R994.1 - AGP_DEVSEL# -> AGP_SBA1(DDC_DAT), R995.1 AGP_IRDY# -> AGP_SBA0(DDC_CLK). <Page 10> 92.04.21.

31. Add CLK_14M_APIC Terminate R,C @R1143 10/@C973 15P. <Page 26> 92.04.21.

32. Change SPR JP40 33,34 DOCKVIN -> GND , JP35,36 GND -> DOCKVIN. . <Page 41> 92.04.21.

33. Change BOM Q65 DTC124EK_SC59 -> MMBT3904_SOT23. <Page 41> 92.04.21.

34. Del @R1104, @R1089, @C953(CLK_SB_48M). <Page 36> 92.04.21.

35. Add @R1142 pull High(DOCK_LOUT_R). <Page 38> 92.04.21.

36. Add C971 & R1140 for VOLBTN+#, R1141 & C972 for VOLBTN-#, R1131 pull High +5VS, @R1139 pull High +3V. <Page 41> 92.04.21.

37. Add R520 @ -> Del @(JP8.AE26 COMPAT#). <Page 5> 92.04.23.

38. Change BOM R539, R540 61.9 -> 51.1 (JP8.L24/P1 COMP0/COMP1). <Page 5> 92.04.23.

39. Change BOM R553 100 -> 49.9, R558 169 -> 100. <Page 5> 92.04.23.

40. Change BOM R383 100 -> 49.9, R384 169 -> 100. <Page 8> 92.04.23.

41. Add R1001 @4.7K -> Del @, 100K pull Low(DPRSLPVR). <Page 26> 92.04.23.

42. Change BOM R40 @ -> Del @, R53 -> @. <Page 29> 92.04.23.

43. Change BOM R792 -> @, R795 @ -> Del @. <Page 39> 92.04.23.

44. Change BOM R230 -> @. <Page 4> 92.04.23.

45. EMI add R1144 for SSOUT. <Page 10> 92.04.24.

46. EMI change D73, D74, D75, D76 part. <Page 38> 92.04.24.

47. Add C974 pull Low for +NB_AGP. <Page 17> 92.04.24.

48. Change BOM R623 10K -> 0. <Page 25> 92.04.28.

49. Change BOM R622, R619 10K ->@. <Page 25> 92.04.28.

BHR60 SI STEP LA-1811 REV:0.4 EE MEN <92.04.28. >

1. Change C781 SE077106M00 -> SE054106Z10. <Page 39> 92.04.28.

2. Change C963 -> @. <Page 41> 92.04.28.

3. Change C974 -> @. <Page 17> 92.04.28.

4. Change C742 -> (SD028000000) 0 Ohm. <Page 37> 92.04.28.

5. Add R771 -> (SD028470100) 4.7K Ohm. <Page 37> 92.04.28.

6. Add C747 -> (SE070104Z00) 0.1U. <Page 37> 92.04.28.

7. DEL R761,R762 <Page 37> 92.04.28.

BHR60 from DB-2 to SI-1 STEP LA-1811 REV:0.3 -> 0.4 Layout Modify

<92.04.08.~92.04.18. >

---PLEASE SEE NEXT PAGE

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS
MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
H/W2 EE Dept. PIR SHEET(2)			
Size	Document Number	Rev	
	LA-1811	1.0	
Date	Wednesday, September 24, 2003	Sheet	61 of 66

BHR60 from SI-1 to DB(15.4") LA-1811 REV:0.4 -> 0.5 HW PIR
<92.05.07.~92.05.30. >

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Prevent CPUCLK_STP# abnormal state happened	5 26 29	Change R1125 from 4.7K to 12K Delete R1126 Change R40 from 10K to 1K	0.5
2		Prevent power leakage	7	Change the power of U8 from +3VS to +3VALW	0.5
3		Power saving	7	Change the power of Fans from +5VALW to +5VS	0.5
4		ATI recommendation	8	Add C374	0.5
5		Add VGA DRAM size detect function	17	Add R1149 for 128MB VGA DRAM (un-populate for 64MB)	0.5
6		Add CSI# for Hynix 8Mx32 VGA DRAM	18, 19, 22, 23	Add Nets: NMCSA1# and NMCSB1#	0.5
7		Change M9+X VGA_CORE from +1.5VS to individual power source	21	Delete JOPEN3	0.5
8		Delete useless components	5 25 27	Delete R538 Delete C96 Delete Q114, Add R1145	0.5
9		Solve power leakage from CRT	25	Change R619-1 and R622-1 net from +5VS to CRT_VCC	0.5
10		Prevent DPRSLPVR abnormal state happened	26	Change R1001 from 100K to 47K, R1002 from 0 to 47K	0.5
11		Using rechargeable RTC battery for HP's request	26	Delete D66, D71 and D72; Add D91 (BAS40-04, the same as LA-1761 D30); Change BATT1 from CR1220 to ML1220 (the same as LA-1761 BATT1)	0.5
12		Prevent +5V drop while plug SPR for HP's request	41	Change JP40.3, C798.1, C800.1 and C801.1 net from +5V to USB_VCCA; Change C798 from 22u to @10u; Change C801 from 1000p to @1000p	0.5
13		Enhance brightness of blue LEDs	42, 45 44	Delete Q67, R883, R884, R942 and R943; Add Q117 and R1146; Change R881, R882, R885, R888, R889, R890, R925 and R1136 to 220 Change JP42.2 from BATLED_0 to BATLED_0#; Change JP42.7 from N.C. to +5VALW; Change JP42.12 from PAV_GND to PAV_LEDVCC; Change JP42.13 from PMLED_1 to PMLED_1#; Change JP42.14 from PAV_GND to +5VS; Change JP45.7 from PRES_GND to PRES_LEDVCC; Change JP45.8 from PRES_GND to +5VS	0.5
14		Solve PWR_ACTIVE LED function fail issue	42 46	Change power from +3VS to +5V for PWR_ACTIVE LED (D52 and D56) Add R1147 and R1148; Change U15.76 net from N.C. to PWR_ACTIVE_PRES#; Change U15.87 net from N.C. to PRES_DETECT; Change U15.119 net from PWR_ACTIVE# to PWR_ACTIVE_PAV#	0.5
15		Solve M10 can't power up issue	49	Change R1101 from 100K to 56K; Change R901 from 91K to 27K	0.5
16		Add discharge components	49	Add R372, R1095, R1102, Q36, Q103 and Q109	0.5
17		Material change for ME's request	44	Change JP47 from ACES_88231_0200 to MOLEX_53398_0290 (the same as LA-1761 JP2)	0.5
18		Using NEC USB2.0 to support BT for HP's request	44	Change R1082.2 net from USB3+ to USB5+; Change R1081.2 net from USB3- to USB5-	0.5
19		Increase MONO_IN voltage level	37	Change R738 from 2.4K to 10K	0.5
20		Decrease Audio AMP Gain	38	Change R971 from 100K to @100K; Change R973 from @100K to 100K	0.5

Update with Item23

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
H/W2 EE Dept. PIR SHEET(2)		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	
Sheet	62	of 66

BHR60 from SI-1 to DB(15.4") LA-1811 REV:0.4 -> 0.5
HW PIR <92.05.07.~92.05.30. >

BHR60 from DB to SI LA-1811 REV:0.5 -> 0.6
HW PIR <92.06.20.~92.07.03. >

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
21		RTL8101L no need transistor for 3.3V to 2.5V anymore REALTEK recommendation	34	Delete Q55, R944 and C868 Change R704 from 5.6K_0402_5% to 5.6K_0402_1%	0.5
22		Connector Spec. change for ME's request	44	Change PCB Footprint from SUYIN_020167MR004SX012R_4P to suyn_020167mr004s11zu_4p for JP18, JP19 and JP20	0.5
23		Solve Tr and Tf of H-sync/V-sync over Spec issue for high resolution CRT	25	Delete Q68, Q64, R619, R620, R621 and R612; Add U57, U58 and R1150	0.5
24		Delete useless components with BOM	10 24	Delete R574, R1066 and C952 Delete R210 for UMA only	0.5
25		Add SB to control H_PROCHOT# for HP's request	26	Add Q118 and R1151	0.5
26		Add components for EMI	37 40 40	Add R1152 Add L65 - L78 Add L79 - L97	0.5
27		Solve DOS cold-boot shunt down issue	7	Delete C256	0.5
28		Decrease overshoot & undershoot	25	Add R1153 and R1154	0.6
29		Change SB GPIO0 and GPIO2 pull-down to GND	26	Delete RP126; Add R1155- R1157	0.6
30		Only 0603 size in SAP for 5.6K_1%	34	Change component size of R704 from 0402 to 0603	0.6
31		The pin-definition of FDD conn. was error on rev0.5 M/B	40	Correct the pin-definition for JP38	0.6
32		VIA recommendation	40	Change RP119 from 1K to 330; Delete RP121; Add R7 and R7	0.6
33		Enhance brightness of Docking LEDs	41	Change R880 from 10K to 470	0.6
34		To support wake-up function with TP	44	Change TP power from +5VS to +5V	0.6
35		Delete useless components	5 12 17 20 24 25 26 27 29 37 38 39	Delete RS35, RS36, R991 and R992 Delete U53, C912-C914, D79-D82, R954, R1010-R1012 and R1023 Delete Q15 and R251 Delete R1022 Delete R211 and R216 Delete C93-C95 and C930 Delete Q113, R1124 and D91; Add D93 Delete RP149, RP150, R1145 and Q114 Delete R53 Delete L45, R1019, Y6, R756, C740 and C741 Delete R1142 Delete RP153 and R1132	0.6
36		To improve RTC accuracy	26	Change Y1 from +/-20ppm to +/-10ppm	0.6
37		Solve Cardbus controller can't reset well issue	31	Delete R905, R941 and C906; Connect U37.C11 to G_RST#	0.6
38		Add components for EMI	37 40	Add L98 and L99 Add C975, C976, CP15-CP17	0.6
39		Improve Audio quality	37 38 41	Delete C753-C756; Add R1165-R1168 and C979 Add R1158 and R1164; Exchange the nets of JP41.2 and JP41.3 Add R1161	0.6
40		Add components for ID & ME	42	Add D92	
41		Modify +5V power-up timing to lead +3V	49	Change R904 from 91K to 47K	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS TO BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
H/W2 EE Dept. PIR SHEET(2)		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	
Sheet	63	of 66

BHR60 from SI-1 to PV LA-1811 REV:0.6 -> 0.7
HW PIR <92.07.03.~92.08.08.>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
42		Correct Y1 and Y3 pin-out	26	Using pin-1 and pin-2 of these crystals	0.7
			46		
43		ATI Product Advisory, refer to PA_2181XP0T1	44	Delete R65, R66, R67, R70, R72, R75, R79, R82, R86, R89, R94 and R95	0.7
44		Solve CD-ROM audio noise issue	30	Delete C11	0.7
45		Solve audio noise issue	37	Change R733.1 from +5VS to +5VAMP_CODEC	0.7
46		For EM I	38	Add L100, L101, L102 and L103	0.7
47		For FIR detect	39	Add R1173(no fir) and R1174(with FIR)	0.7
48		ATI recommendation	27	Change RP12 from 10K to 2.2K	0.7
			46	Add R1175	
49		Delete useless components	46	Delete D69 and D70	0.7
50		To support wake-up function with TP	46	Delete RP154; Add R1169, R1170, R1171 and R1172	0.7
51		Solve M10 can't power up issue	49	---Delete C844----- Charge R901 from 27K to 6.8K	0.7
52		Improve Tr and Tf of H-sync/V-sync for high resolution CRT	25	Decrease the R _{L,C} value	0.7
53		Modify brightness of LEDs	42	Change Transistors from BJT to PMOS and Resistors value for Pav; Change Resistors value for Pre.	0.7
			45		
54		Fast power on for battery only	45	Change R306 from 100K to 470; Delete Q112	0.7
55		Improve contact		Move JP2(CD-ROM conn.) right 0.65mm	0.7
56		Correct Caps. LED and Numl. LED placement		Exchange the placement of these LEDs	0.7
57		Solve audio noise issue		Cut the bridge between AGND and DGND in GND1 layer	0.7
58		Reserve for EM I	37	Add JOPEN6, JOPEN7 and JOPEN8	0.7
59		Improve USB2.0 signal quality	36	Change R1027, R1029, R1030, R1031, R1032, R1033, R1034 and R1035 to 42.2	0.7
60		Reserve VRAM detect function for ATI recommendation	17	Connect R256/R257 to ZV_DATA0/ZV_DATA1, and pull-up to +3VS	1.0
61		For EM I	38	Change C761-C764 to 470µF and pull-down to D-GND; Change L100-L103 to MOK2012221YZT(ZA)	1.0
			48	Delete C110-C115	
			36	Change L89, R1079 & R1080 to CHB1608U301	
			7	Add C855, C856, C897 and C898	
			24	Change L11 & L12 to MBV2012301YZT	
			26	Change RC1 clock dumping resistors to 39 ohm	
			28	Add C872-C881, C880-C883; Change R60-R62 to MBV2012301YZT	
			37	Delete R769 & R770; Add C884-C892 & L104	
			41	Add L105	
			25	Add C893 & C894	
62		Reduce GH1 # "LOW" voltage level	5	Change R627 to 300 ohm	1.0
63		Fix "Pop" sound during boot up	37	Add C979	1.0
64		For PCBA skew reducing	42 45	Change R885, R888, R890, R1136 and R925 to 130	1.0
65		TI recommendation	32	Add R1177	1.0
66		Solve audio L/R swap issue	37	Change R750 & R753 to 27 ohm	1.0
			44	Delete R327 & C305	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION.
DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
H/W2 EE Dept. PIR SHEET(2)		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003 Sheet 64 of 66	

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	54, 55, 56, 57	wrong layout pad	03/25/2003	Compal	wrong layout pad	change to correct layout pad on PU7, PU8, PU9, PU10, PU11, PU16 and PQ24	0.2
2	56	DPRSLPVR	03/25/2003	Compal	Reserve two resistors for voltage of Deep-sleeper mode	Reserver PR231, PR232, PR233, PR234 for deeper-sleeper mode voltage setting	0.3
3	56	CPU VR-Cont.	03/25/2003	Compal	Reserve a jumper for power consumption measurement	Add PJP14	0.3
4	57	CPU VR-Cont.	03/25/2003	Compal	Change the netname +5VS_CORE for power consumption measurement	Change Netname of +5VS_CORE	0.3
5	51	RTC charger	03/25/2003	Compal	use two resistors for RTC charger protection	Add PR230	0.3
6	55	1.2VS_VGA	03/25/2003	Compal	re-layout 1.2V_VGA requested by ME	re-located both PL10 and PQ21, PQ23 as well as 1.2VS_VGA related power circitry	0.3
7	55	1.2VS_VGA	03/26/2003	Compal	Reserve a jumper for power consumption measurement	Add PJP15	0.3
8	55	+1.25VSP	03/26/2003	Compal	Change power time-sequence of 1.25VSP input power	Change VD, and VDD of PU16 from +2.5VALWP to +2.5VS; Connect PR235.2 to +2.5VS add a resistor PR235 for Stand/By pin for test	0.3
9	54	+1.5VALWP	03/27/2003	Compal	Reserve Force PWM function of 1.5V/2.5V and add a PR236 for SUSP# signal	Add PR237, PR238 for force PWM function control, and add PR236 for SUSP# signal	0.3
10	54	+1.5VALWP	04/16/2003	Compal	change 1.5V time sequence	Change power time-sequence of 1.5VSP input power	0.4
11	56	CPU DPRSLPVR	04/16/2003	Compal	Change DPRSLPVR design	Add two transistor PQ44, PQ45 for voltage of Deep-sleeper mode	0.4
12	54 55 56	PWR JUMP	04/16/2003	Compal	For DFX issue	Change power JUMP SIZE to follow new jump role	0.4
13	56	CPU DPRSLPVR	04/18/2003	Compal	Change DPRSLPVR design	Reserve DPRSLPVR function and add a PR136 for +5VS_CORE signal	0.4
14	50	Vin DETECTOR	04/30/2003	Compal	to make ACIN to enable to pull low	Change PR8 form 10k_0603 to 0K_0603	0.4
15	50	Precharge	04/30/2003	Compal	BOM error	Change PR1 from 10k_0603 to 100k_0603	0.4
16	51	Battery OTP	04/30/2003	Compal	To change feekbeck time	Change PC20 from .22u to 1u ;PR40&PR42 from 100k to 150k; PC80 from 1u to .47u	0.4
17	51		04/30/2003	Compal	change component	Change PU3 from S-81233SGUP-T1 to S-812C33AUA-C2N	0.4
18	52	Battery_OVP	04/30/2003	Compal	To avoide the BATT_OVP output to oscillate	Delet PC44&PR71	0.4
19	53	5V/3.3V/12V	04/30/2003	Compal	BOM error	Change PD16 from EC31Q04 to EC11FS2	0.4
20	53	5V/3.3V/12V	04/30/2003	Compal	To improve the 3V output ripple Voltage	Delet PC77	0.4

Compal Electronics, Inc.		
Title		
Changed-List History-1		
Size	Document Number	Rev
	LA-1811	1.0
Date	Wednesday, September 24, 2003	
Sheet	65	of 66

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
------	-------	-------	------	------------------	-------------------	----------------------	------

Compal Electronics, Inc.			
Title			
Changed-List History-1			
Size	Document Number		
	LA-1811		
	Rev 1.0		
Date:	Wednesday, September 24, 2003	Sheet	66 of 66