

LAGUNA

REV : X00

@ : Depop Component

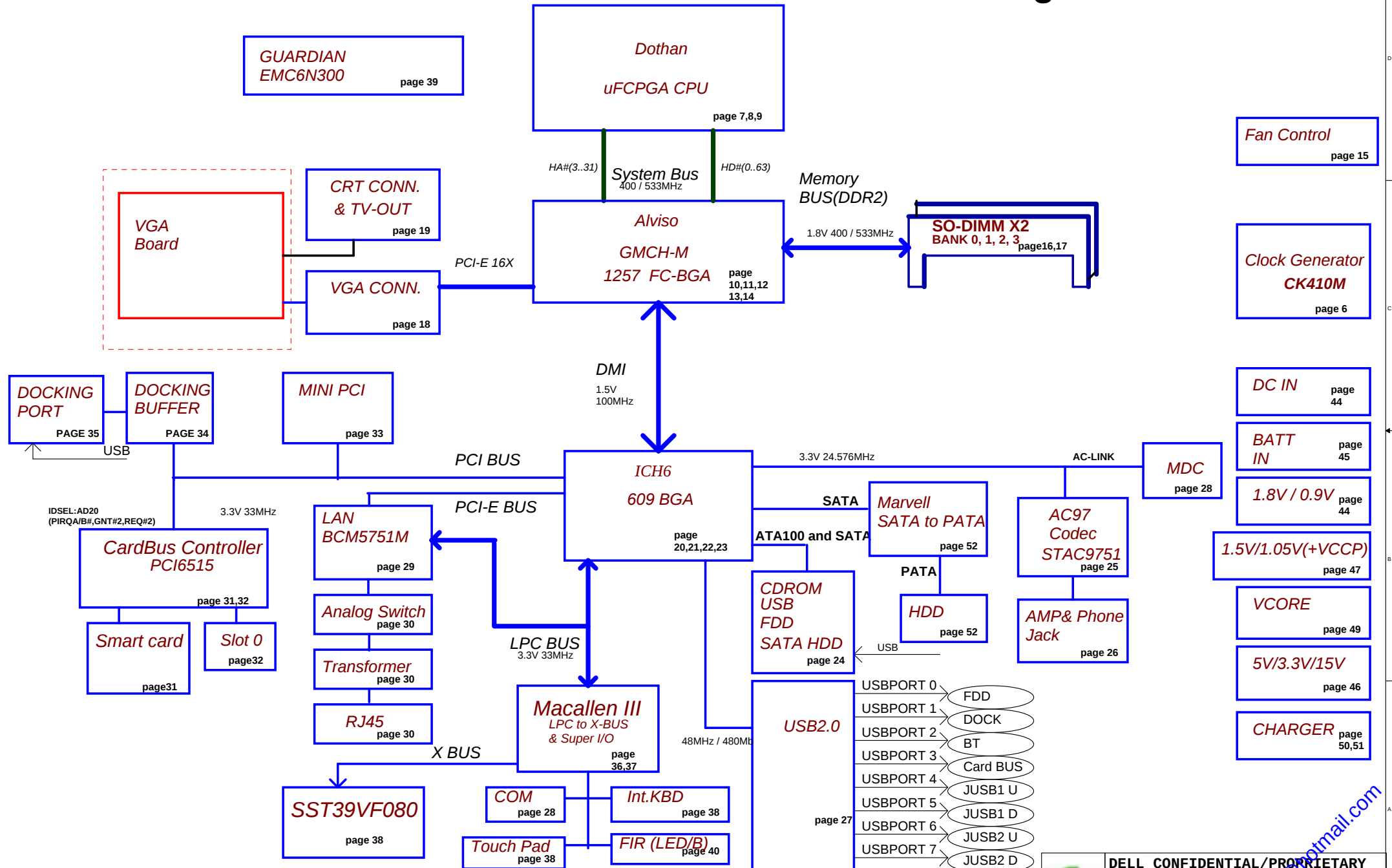
PRELIMINARY

Dothan Schematic with Capture CIS and Function field

uFCPGA Dothan
02-07-2004
REV: 0.3

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		DELL CONFIDENTIAL/PROPRIETARY	
Title			
Cover Sheet			
Size	Document Number Board Number LA2111		Rev 0.3
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PM TABLE

State \ power plane	+3VALW +5VALW	+3VSUS +5VSUS +1.8VSUS +1.5VSUS	+5VRUN +RTC_CELL +3VRUN +0.9V_DDR_VTT +2.5VRUN +1.8VRUN +1.5VRUN +VCC_CORE +VCCP +15V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

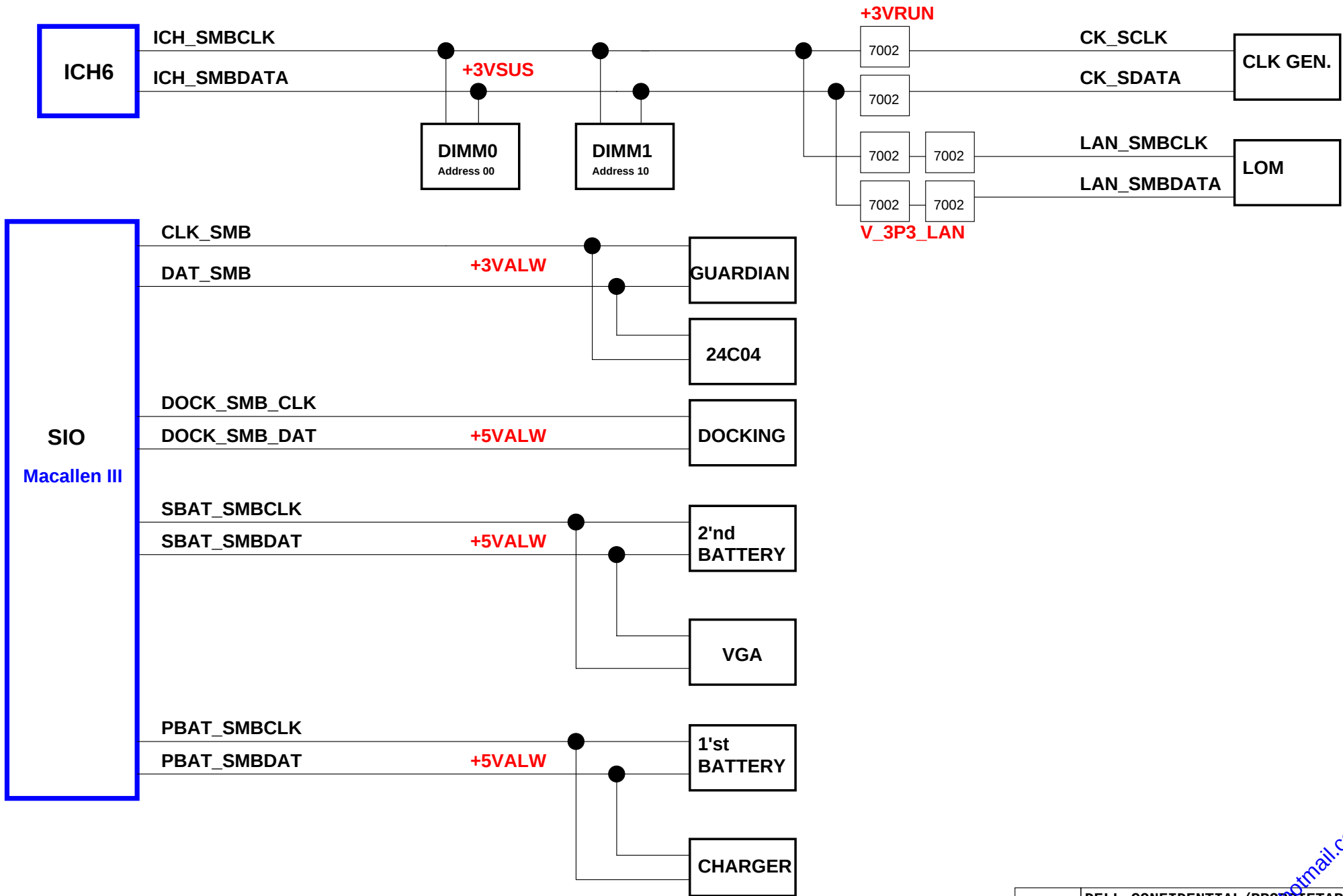
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	D,C
DOCK	AD24	0	A
MINI PCI	AD19	3	D,B

USB TABLE

USB PORT#	DESTINATION
0	FDD (module bay)
1	DOCK
2	MPCI (BlueTooth)
3	NEW Connector
4	USB Port 1(Top)
5	USB Port 1(Bottom)
6	USB Port 2(Top)
7	USB Port 2(Bottom)

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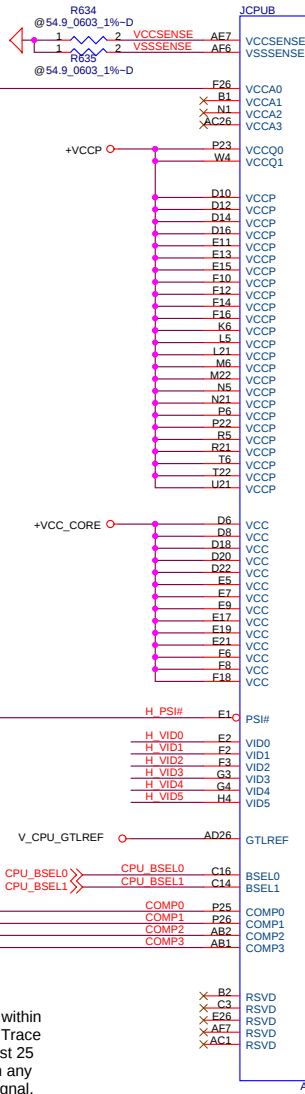
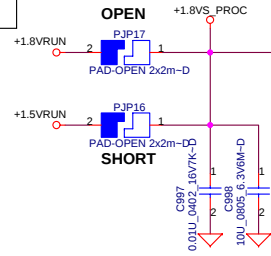
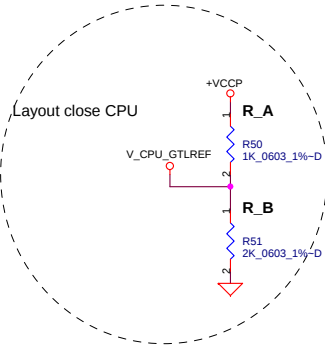
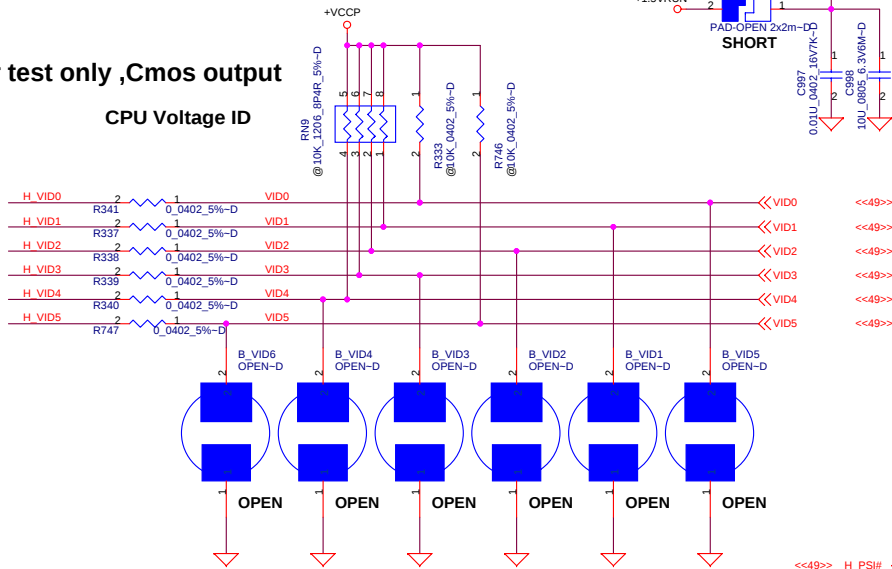


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Dothan-A2 w/ 533Mhz supports both 1.5V and 1.8V.
Dothan-B step w/533Mhz supports only 1.5V

For test only ,Cmos output

CPU Voltage ID



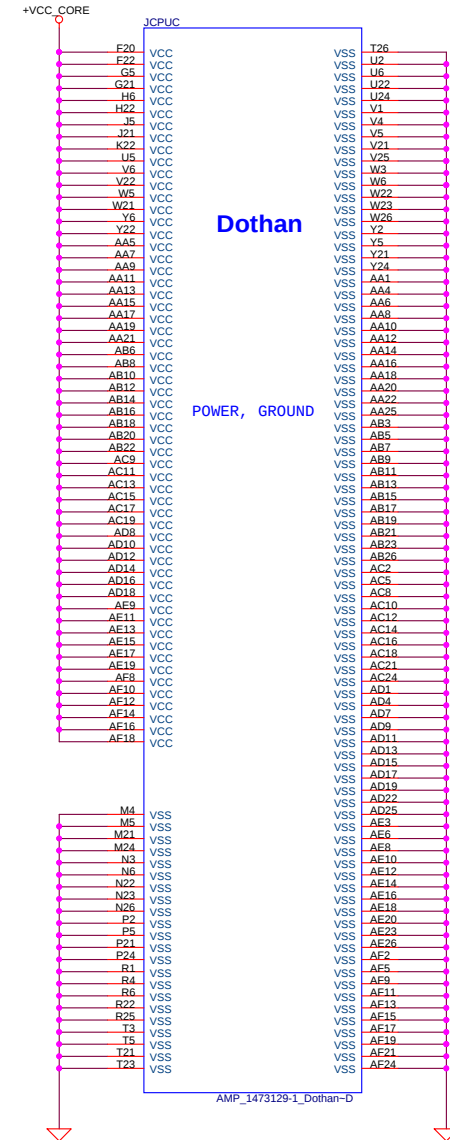
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 miles away from any other toggling signal.

Dothan

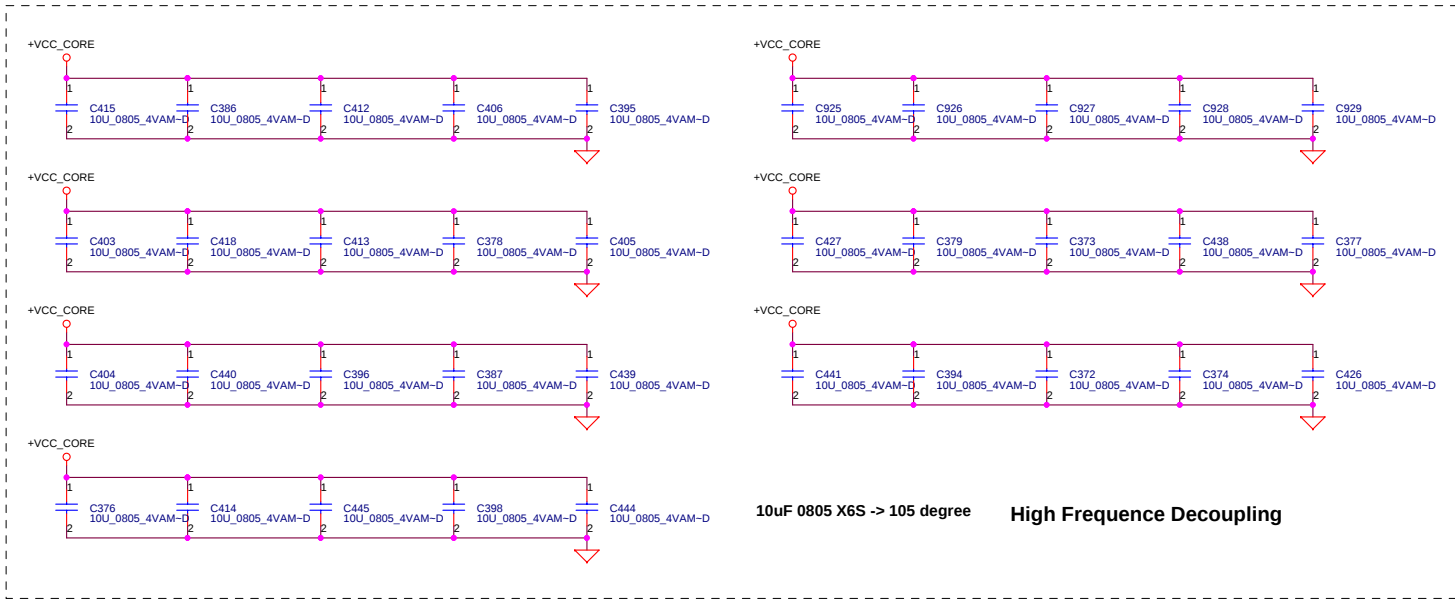
POWER, GROUND, RESERVED SIGNALS AND NC

Dothan

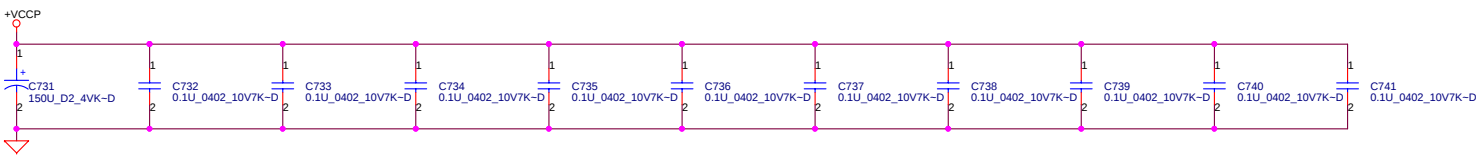
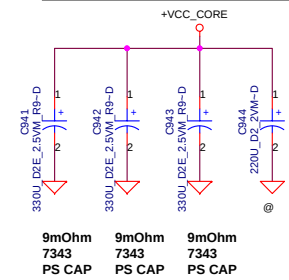
POWER, GROUND



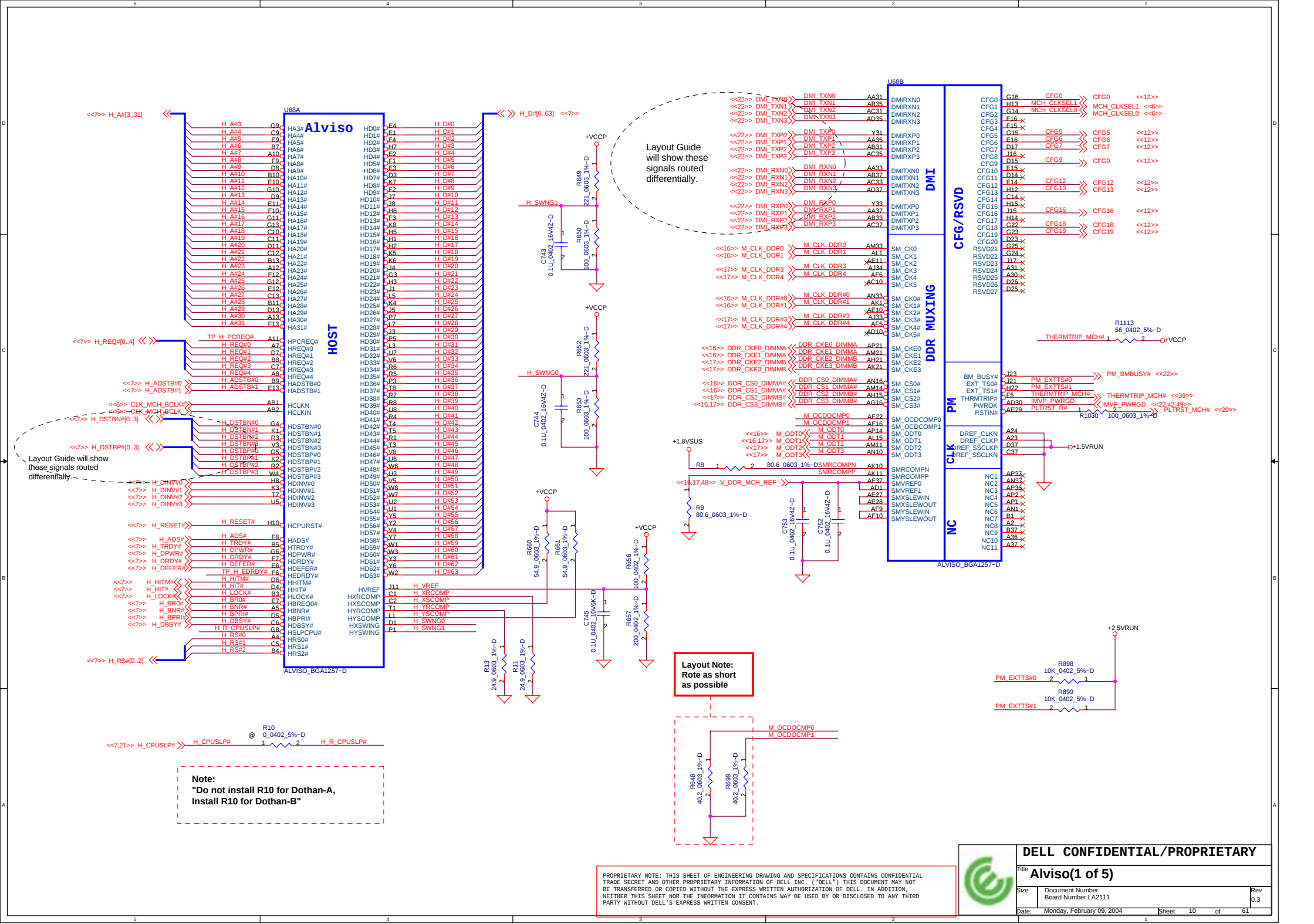
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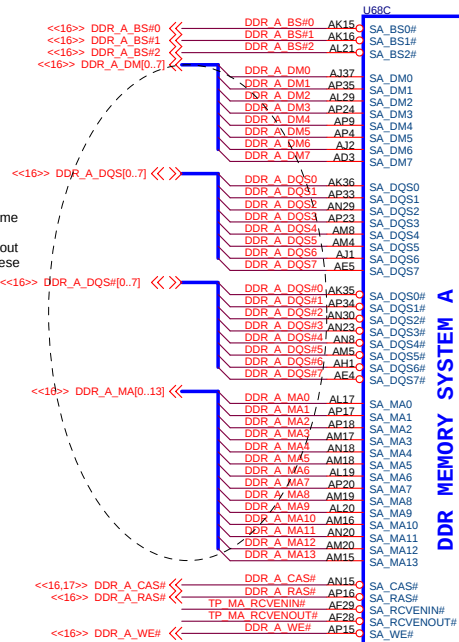
Near VCORE regulator.



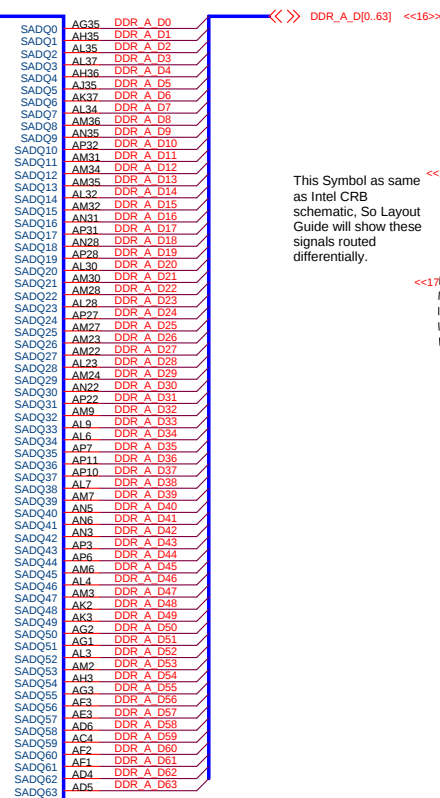
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This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.



ALVISO_BGA1257-D



This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.

DDR SYSTEM MEMORY B

ALVISO_BGA1257-D

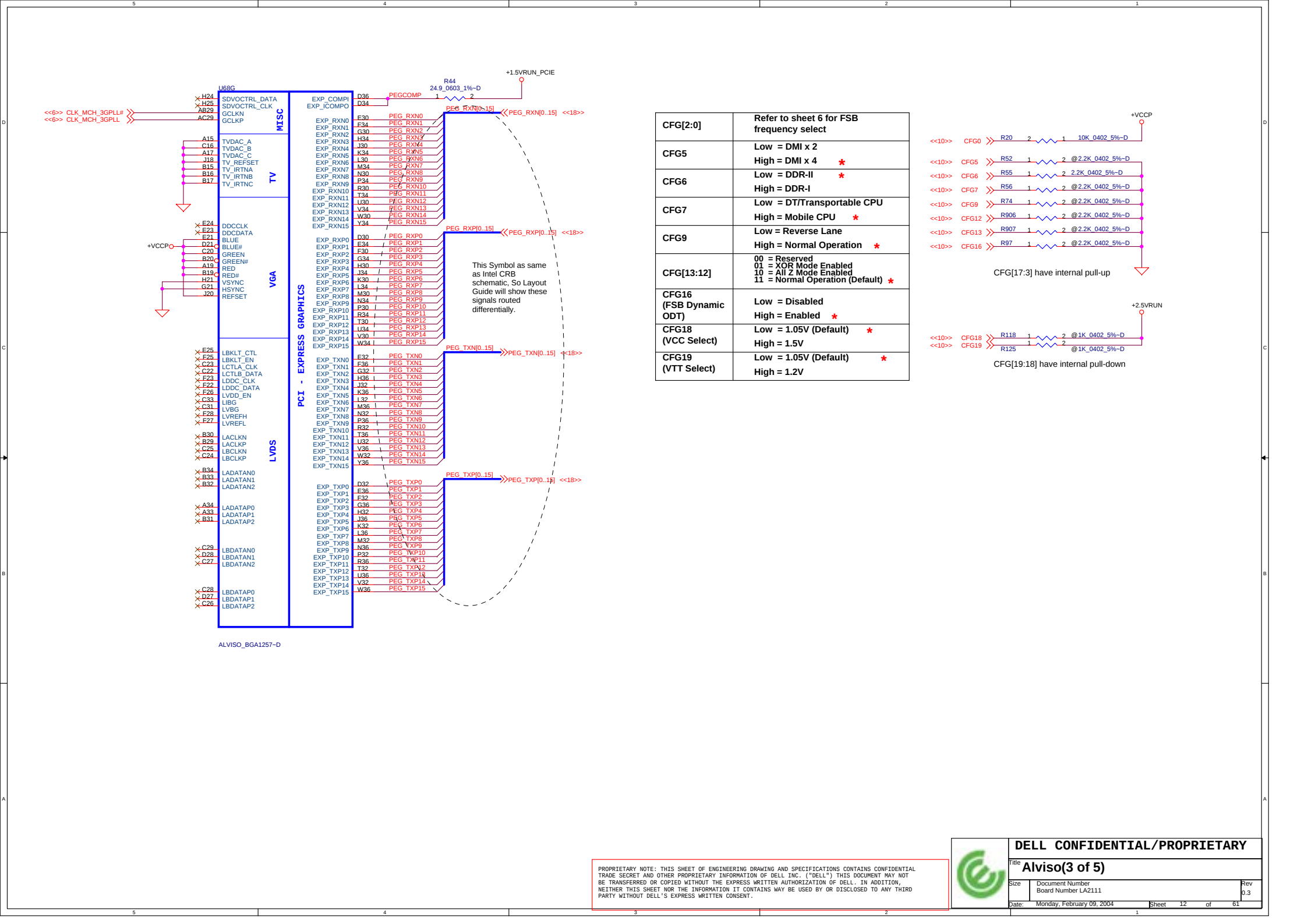


DELL CONFIDENTIAL/PROPRIETARY

Title Alviso(2 of 5)

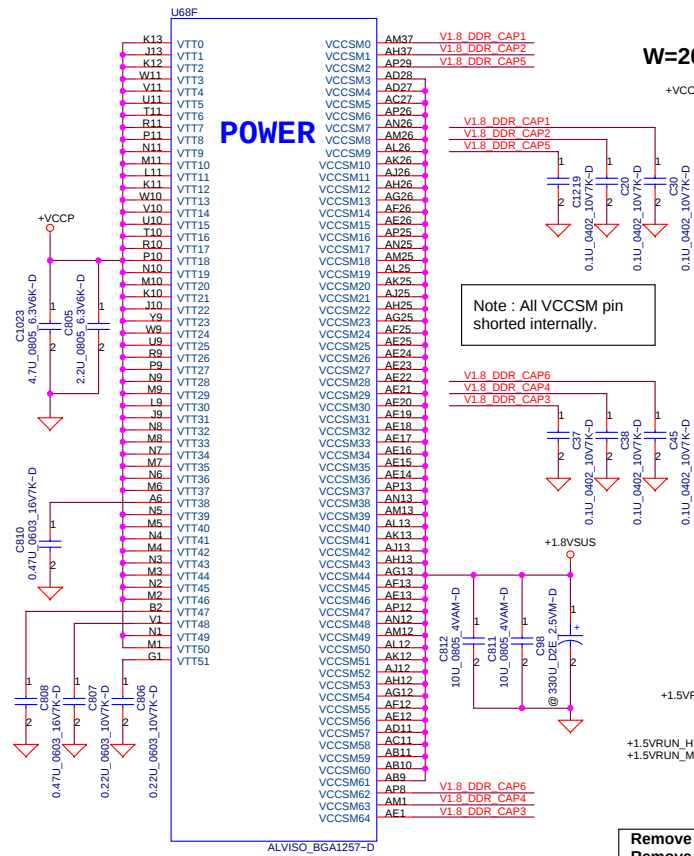
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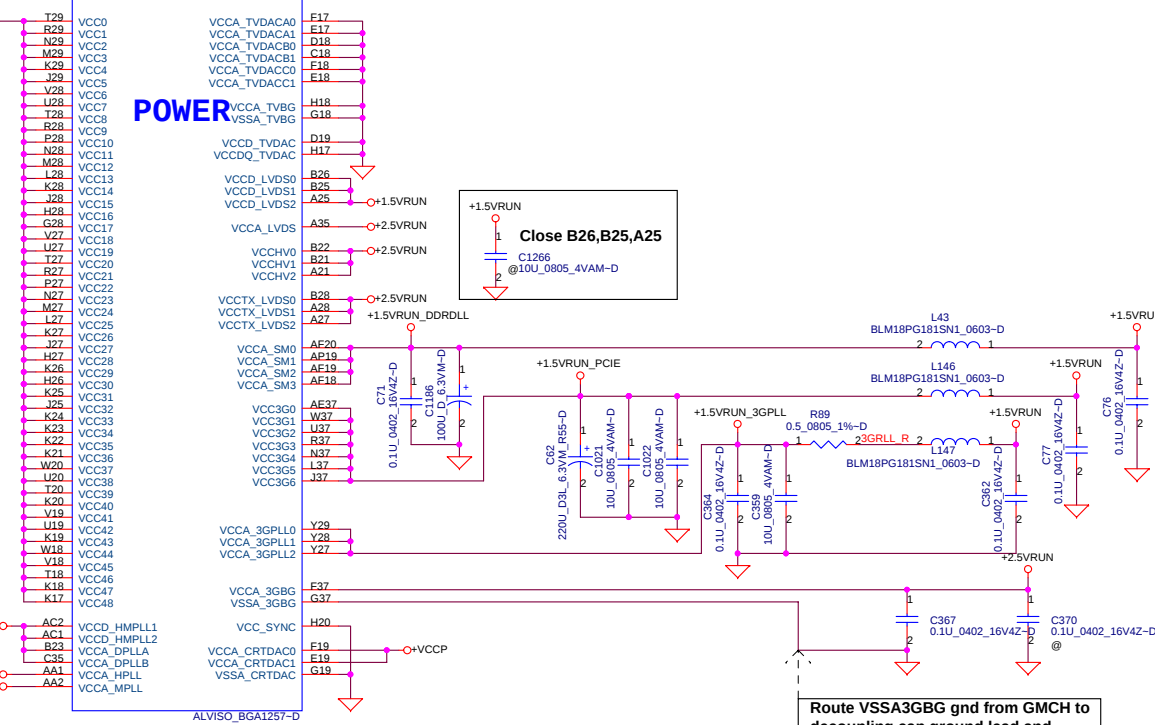
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POWER



W=20 mils

POWER

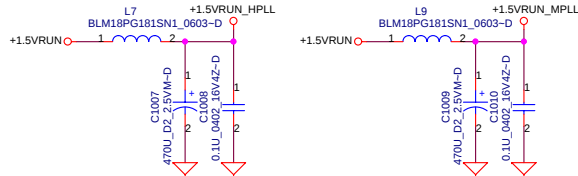


Note : All VCCSM pin shorted internally.

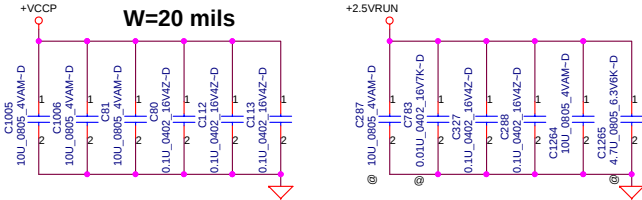
Close B26,B25,A25
C1266
@10U_0805_4VAM-D

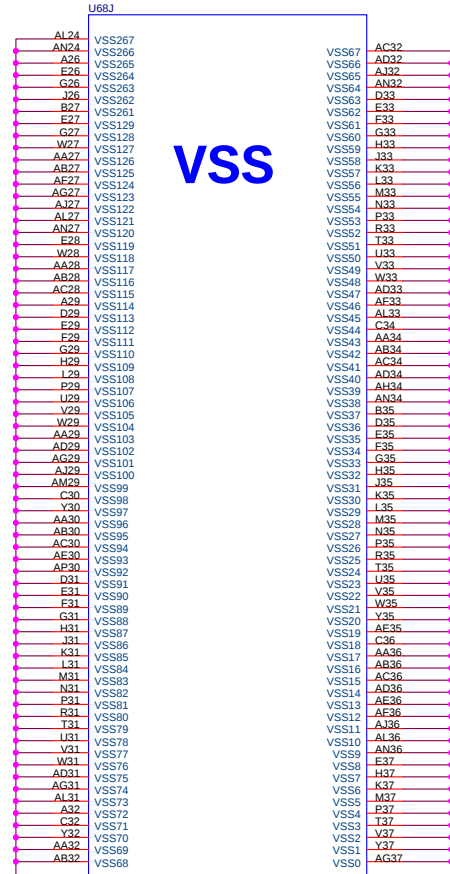
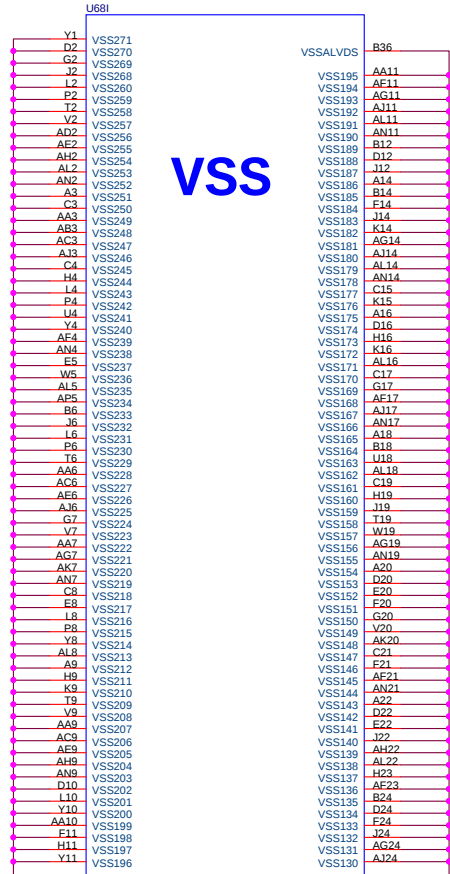
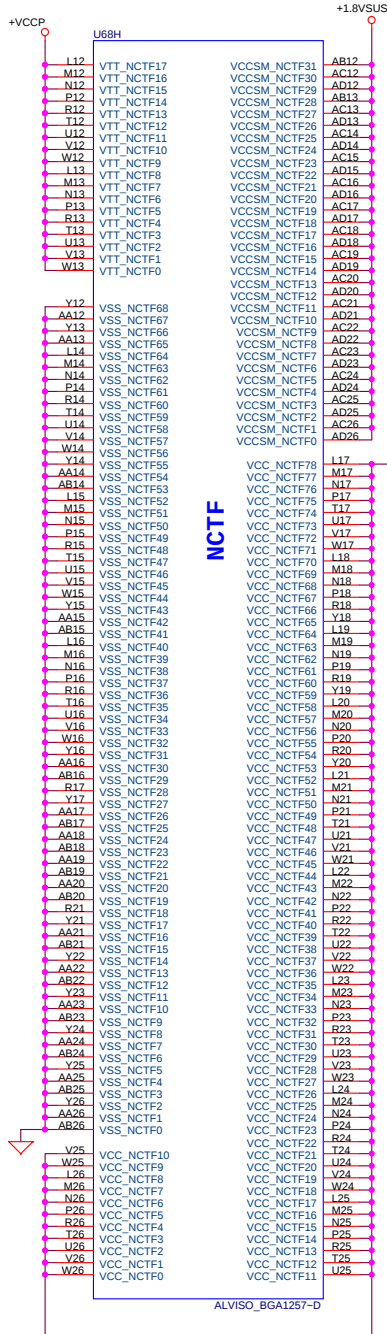
Route VSSA3GBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

Remove L6, C48, C51, Connect DPLL directly to +1.5vrun
Remove L29, C47, C8, Connect DPLLA directly to +1.5vrun
Steven-01/09/2004



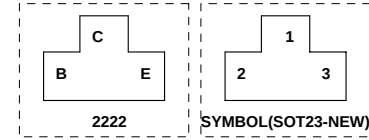
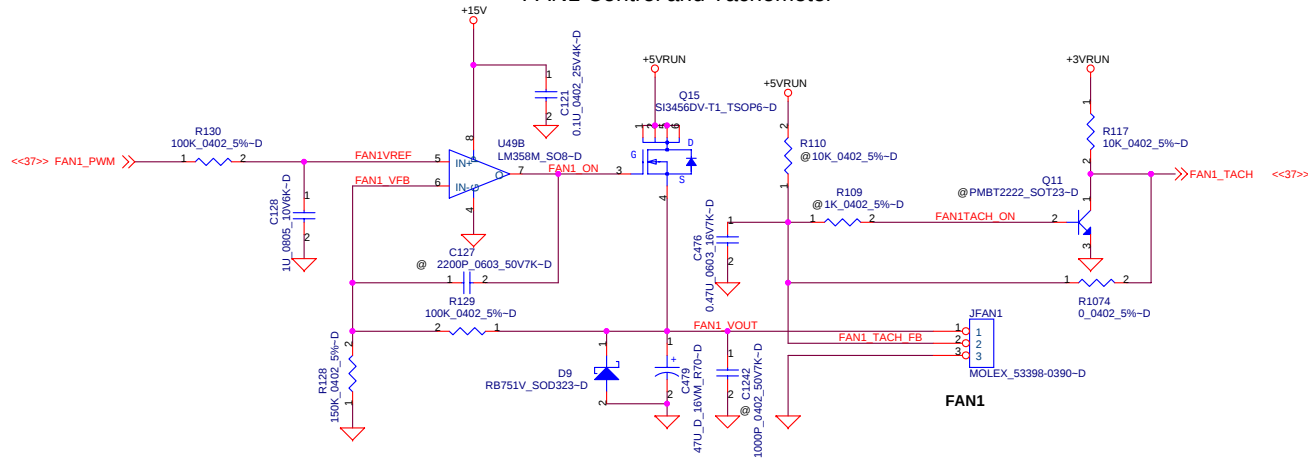
W=20 mils



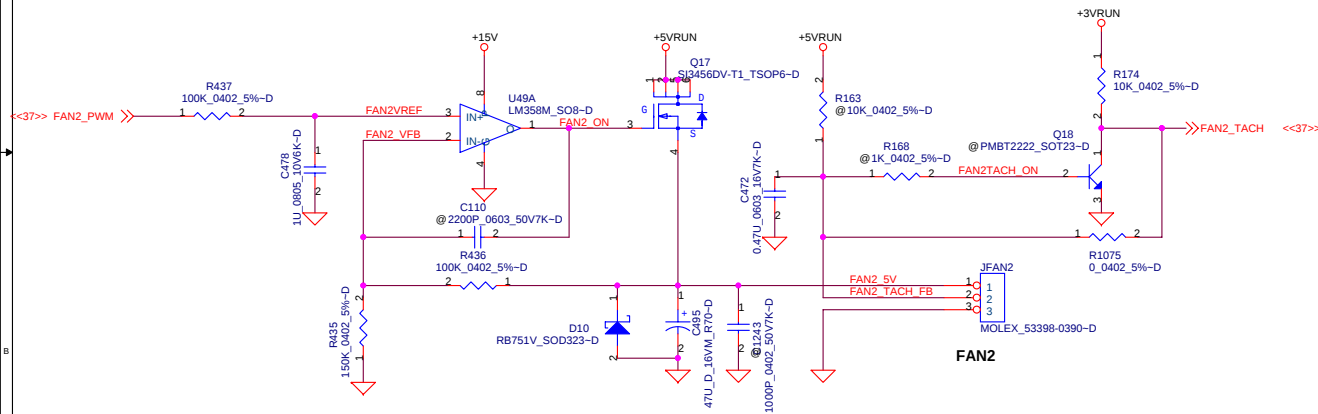


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FAN1 Control and Tachometer



FAN2 Control and Tachometer

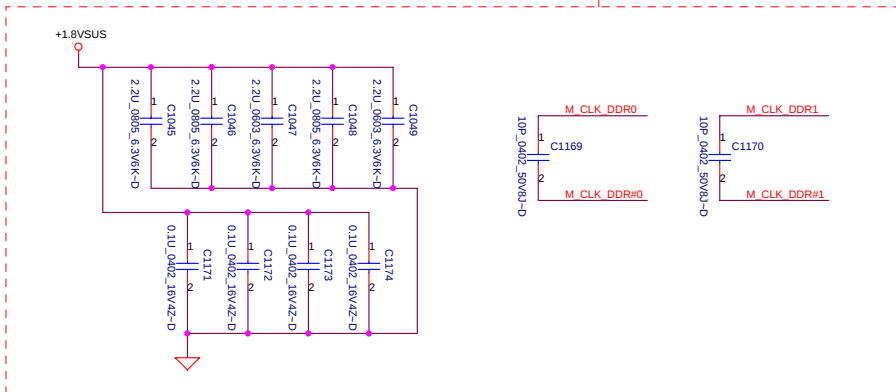


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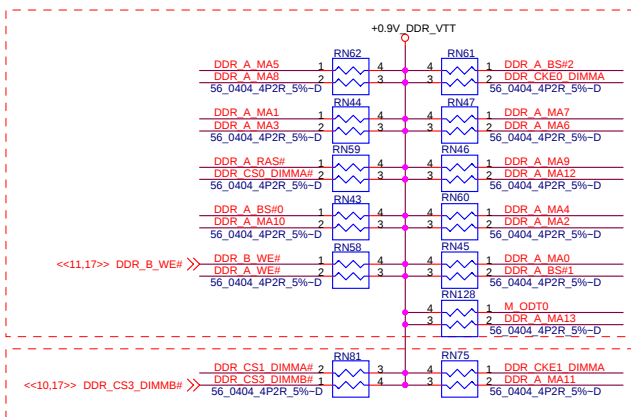
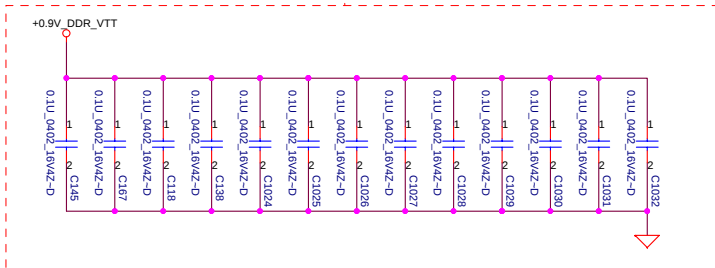
DELL CONFIDENTIAL/PROPRIETARY			
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<<11>> DDR_A_DQS#[0..7] << >>
 <<11>> DDR_A_D[0..63] << >>
 <<11>> DDR_A_DM[0..7] << >>
 <<11>> DDR_A_DQS[0..7] << >>
 <<11>> DDR_A_MA[0..13] << >>

Layout Note:
Place near JDIM1

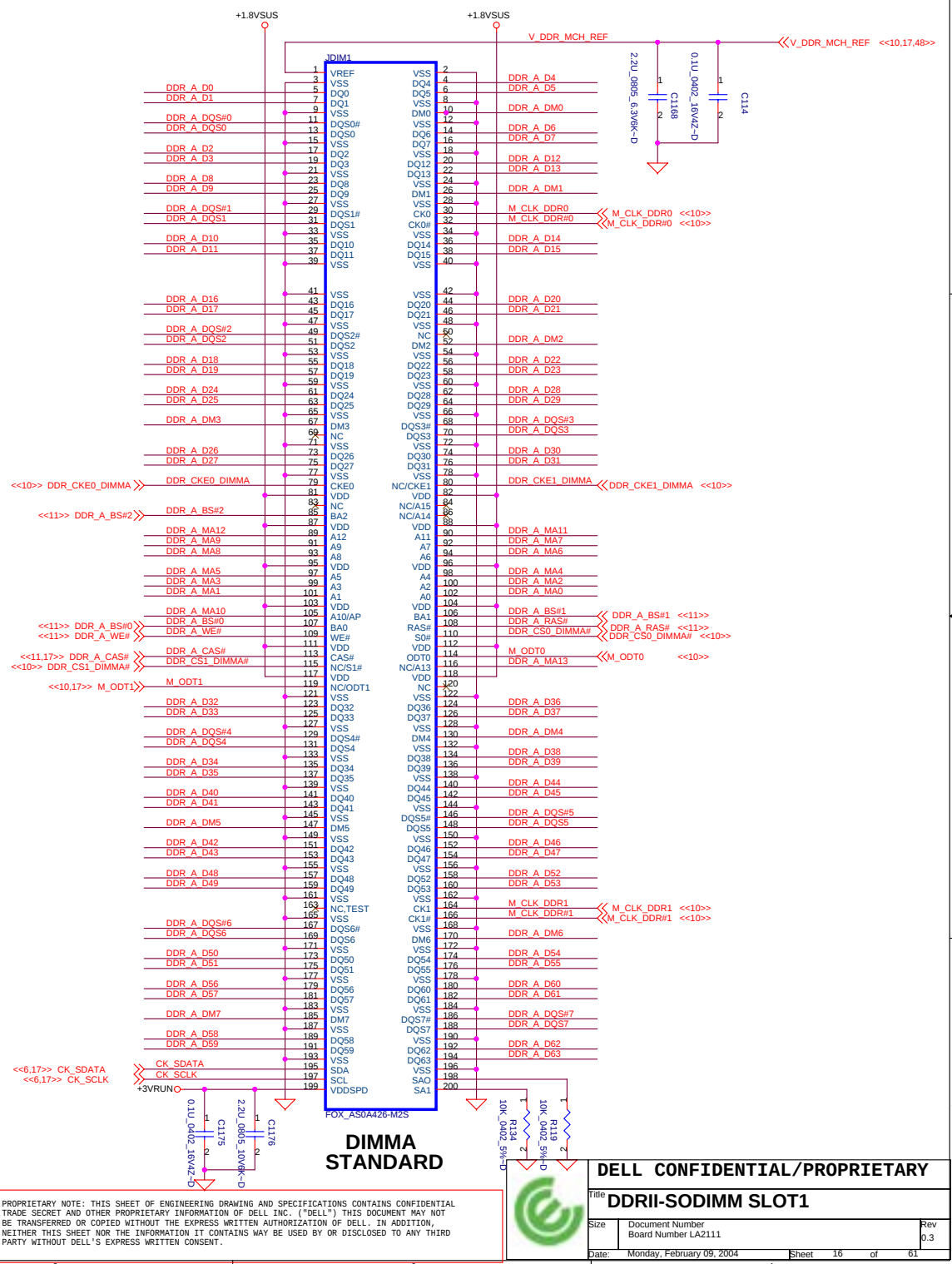


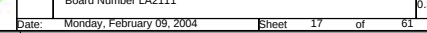
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

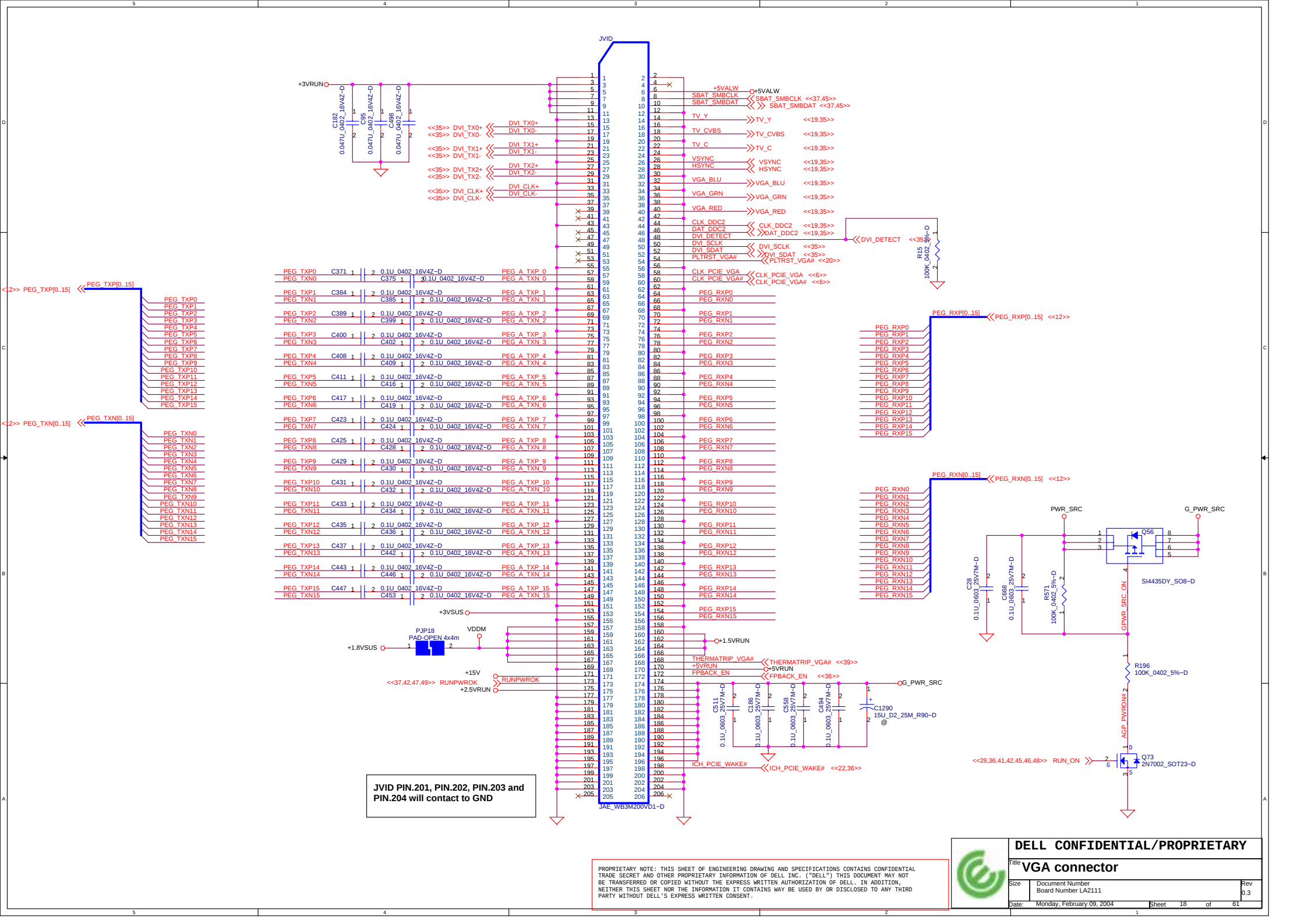


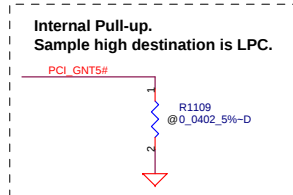
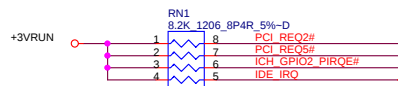
Layout Note:
Place these resistor closely DIMM0,all trace length<750 mil

Layout Note:
Place these resistor closely DIMM0,all trace length Max=1.3"



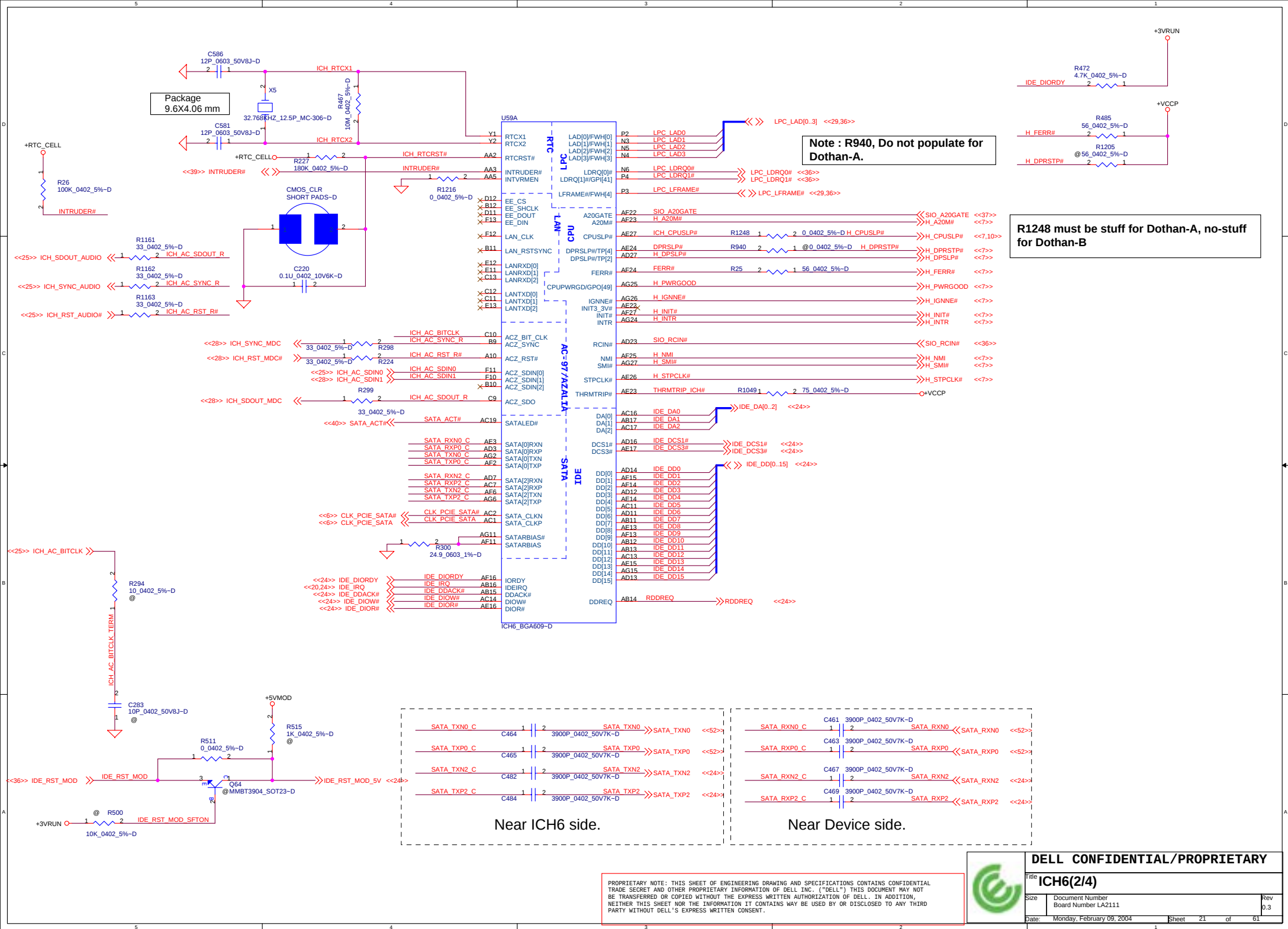


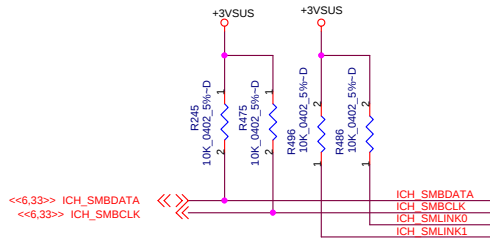




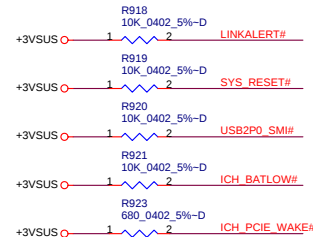
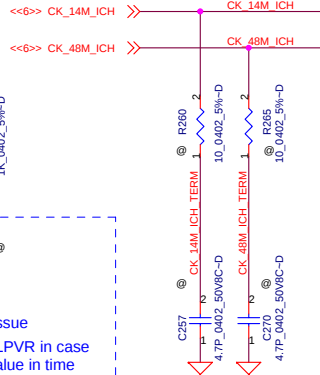
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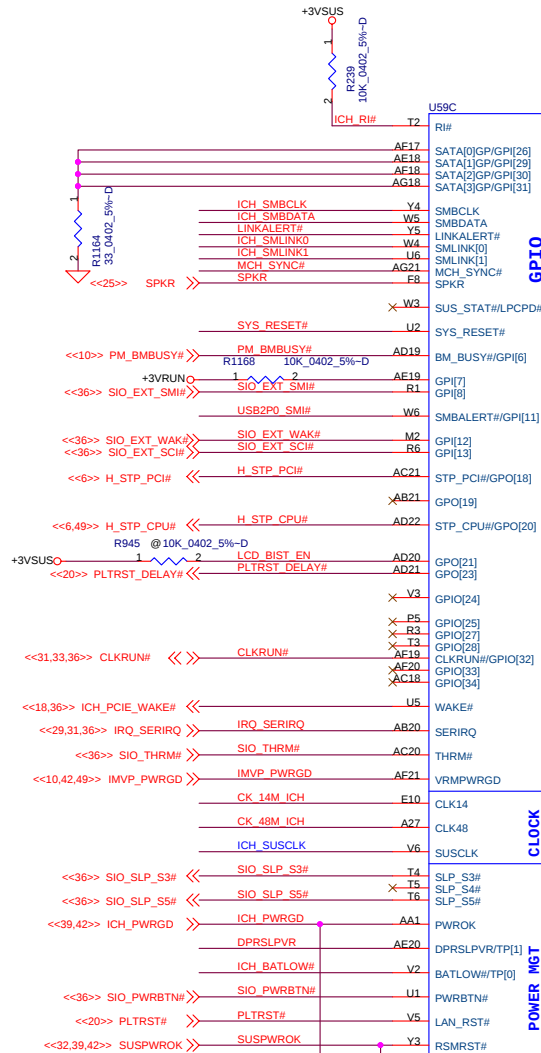
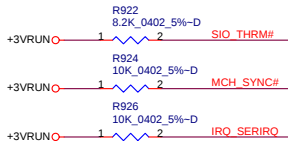




(PCI Express Wake Event)

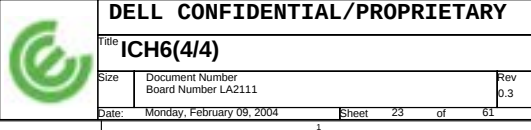


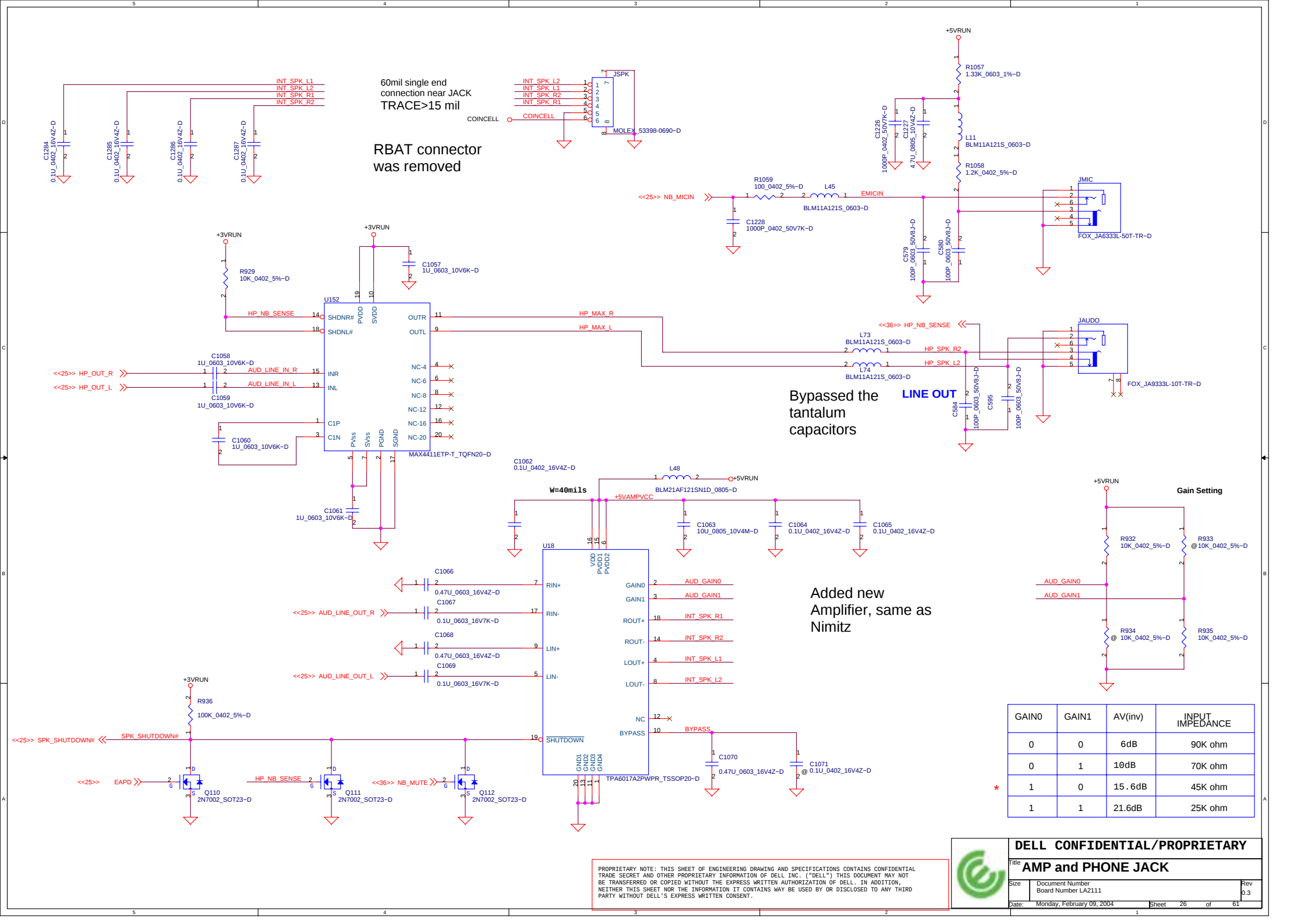
Check List suggest pop 10/16



CLOCK

POWER MGT





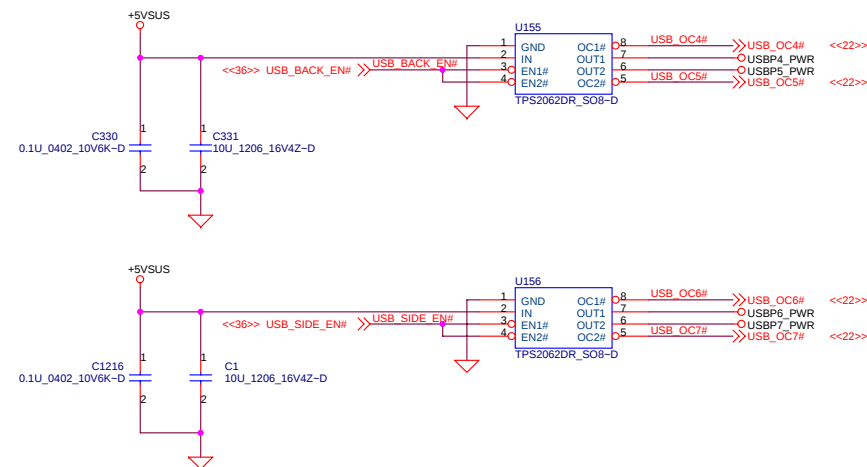
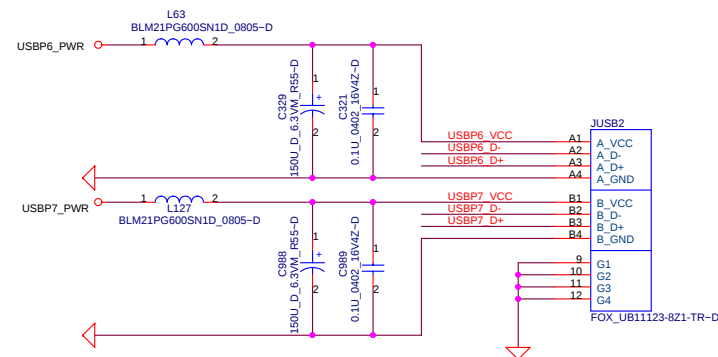
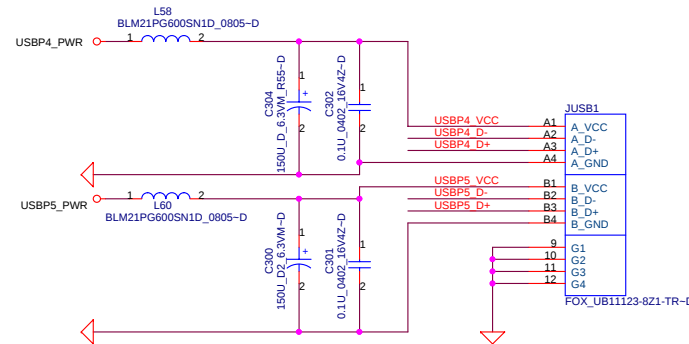
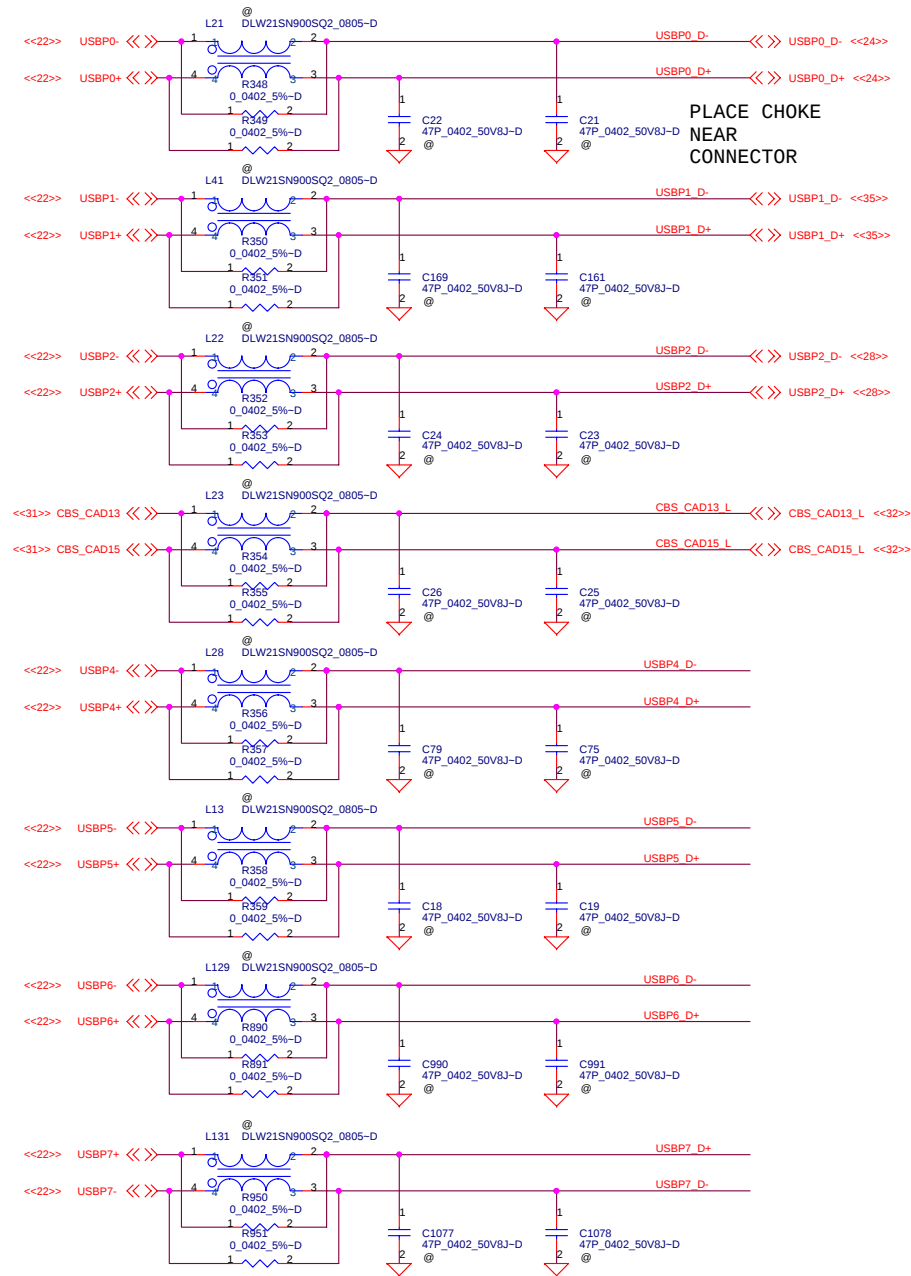
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Title **AMP and PHONE JACK**

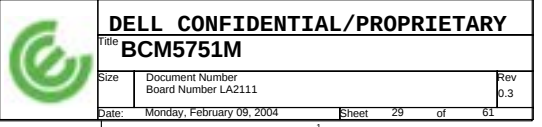
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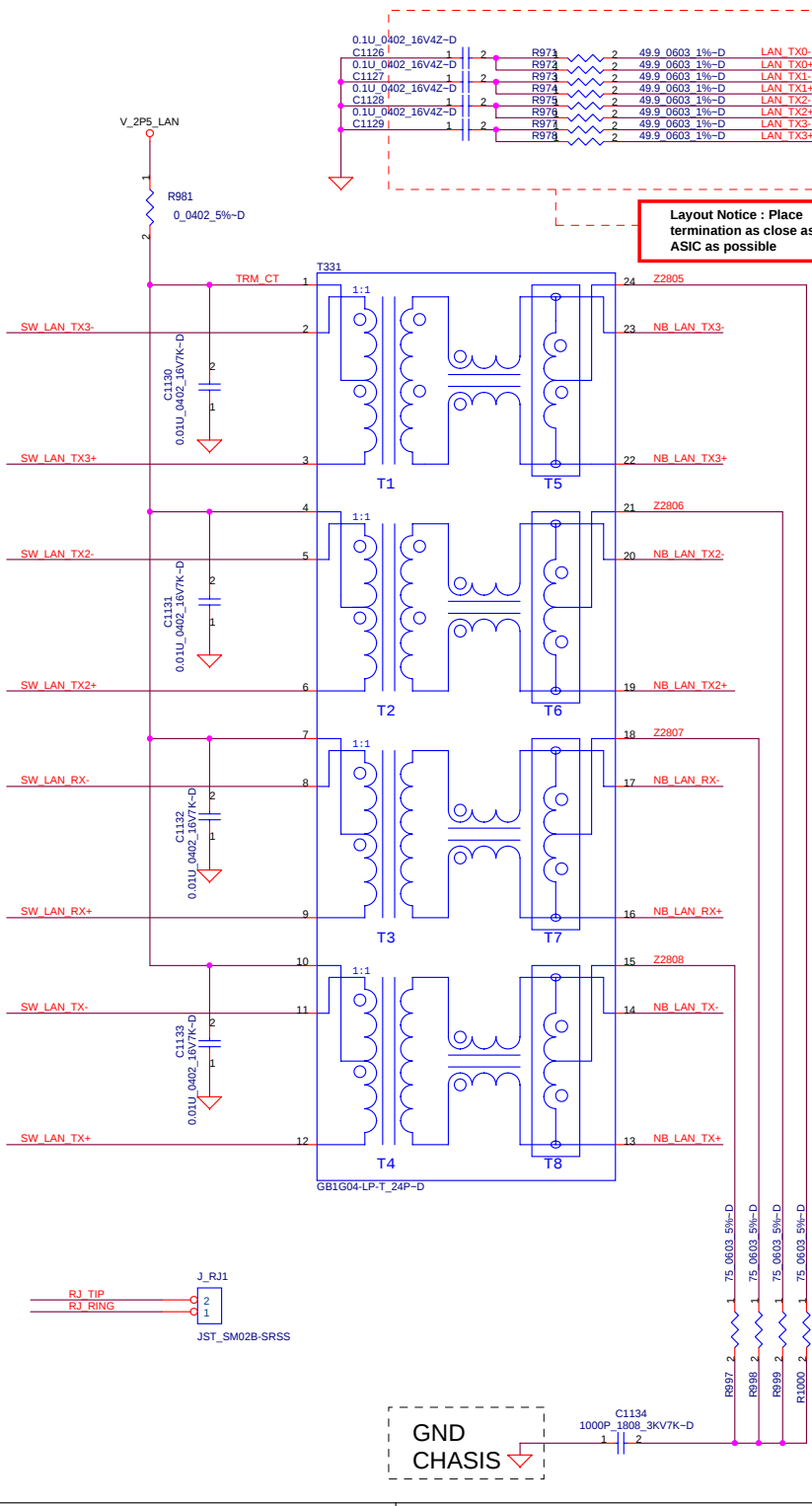


USB PORT#	DESTINATION
0	FDD (module bay)
1	DOCK
2	MPCI (BlueTooth)
3	NEW Connector
4	USB Port 1(Top)
5	USB Port 1(Bottom)
6	USB Port 2(Top)
7	USB Port 2(Bottom)

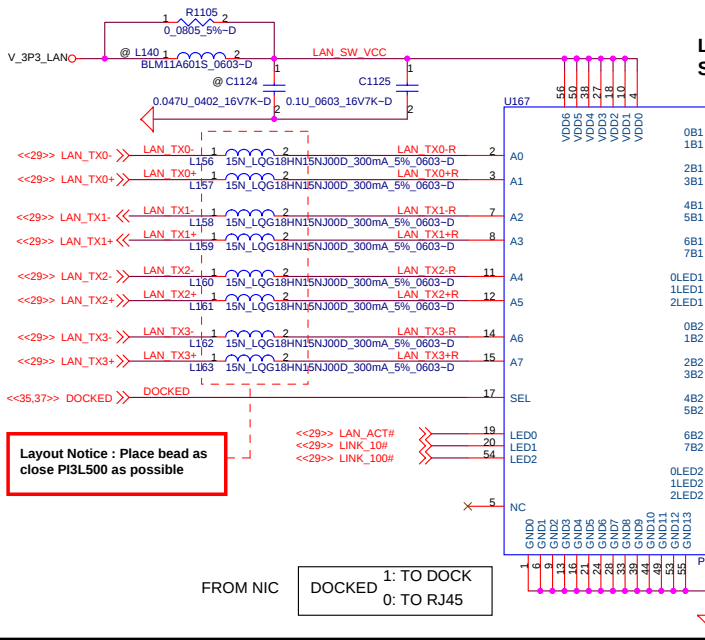
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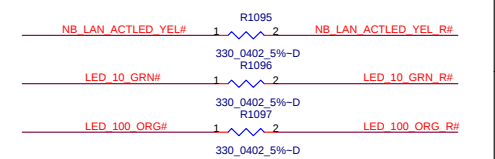
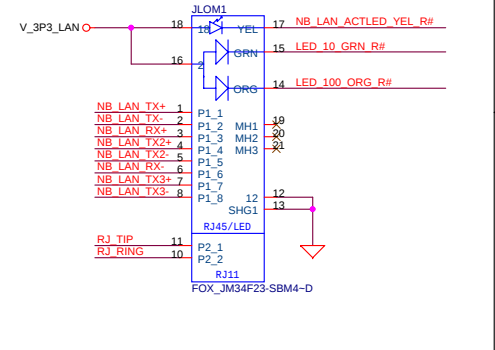




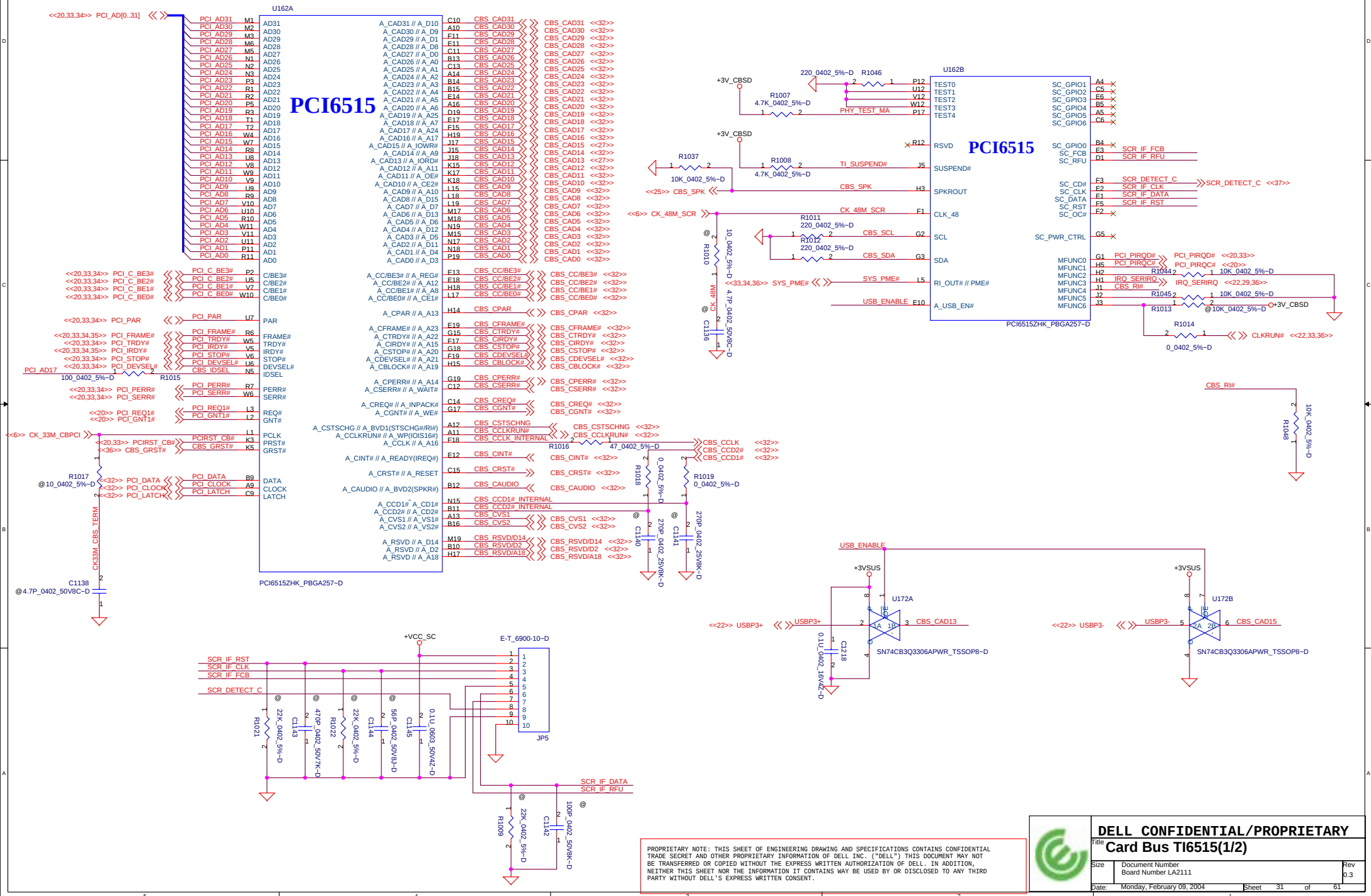
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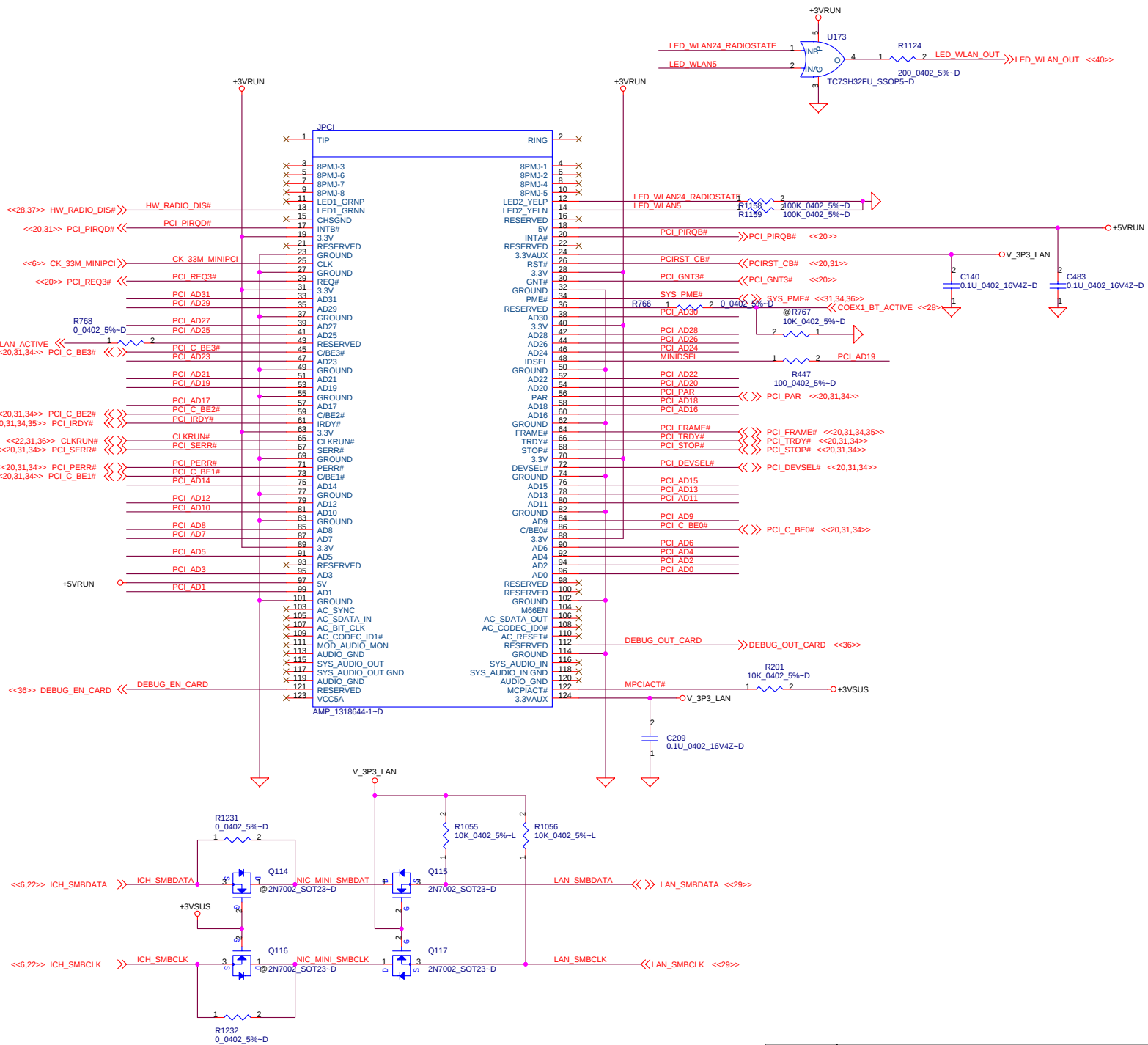
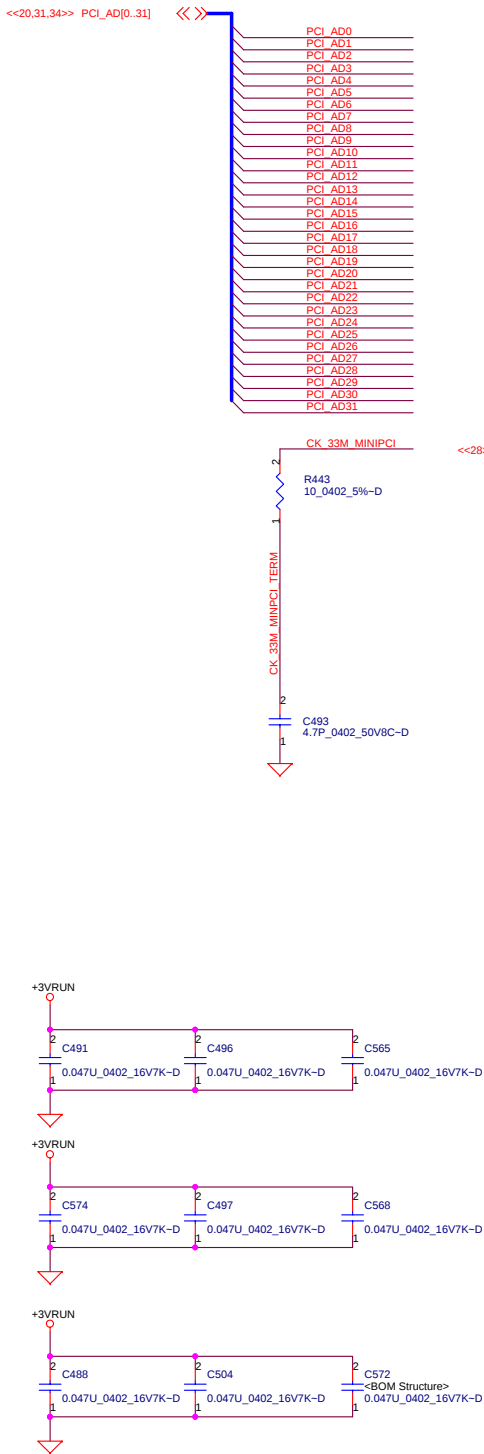


Layout Notice : Place bead as close as possible to the PI3L500

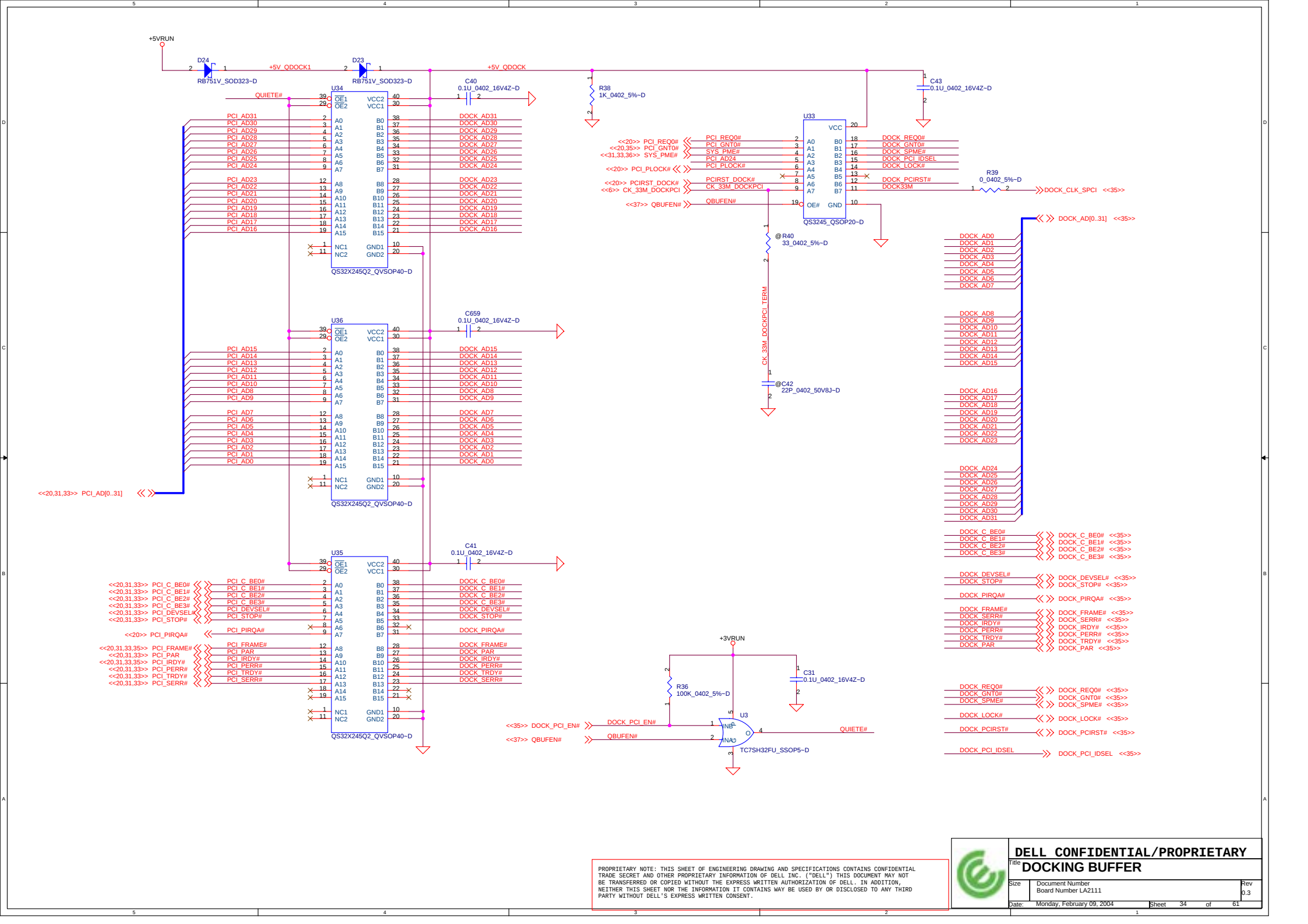


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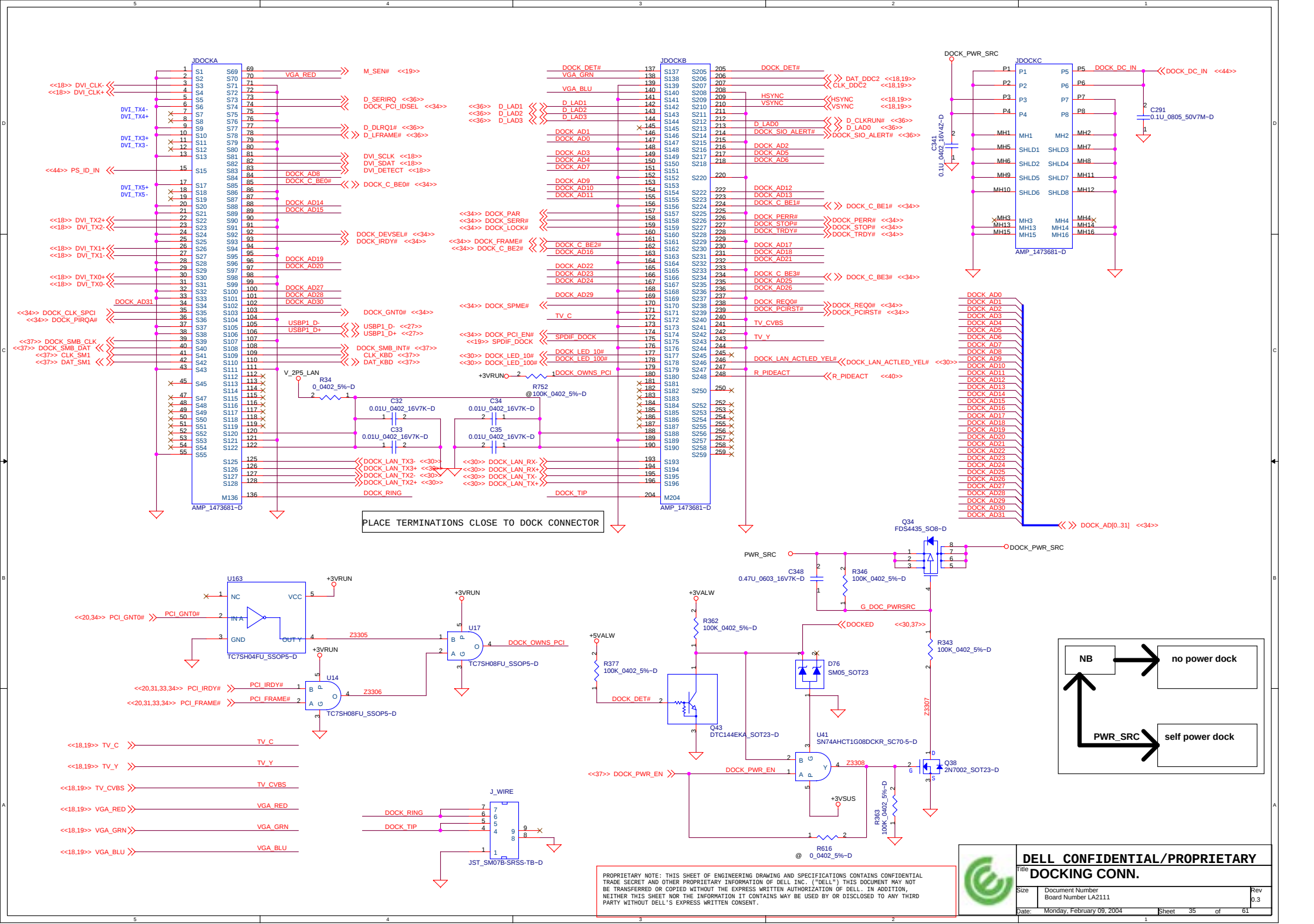
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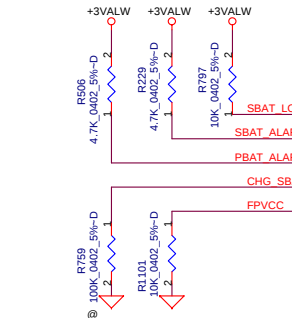
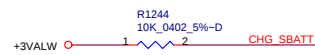
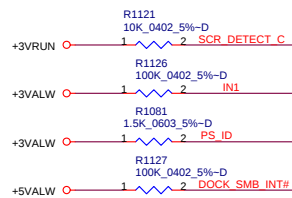
DELL CONFIDENTIAL/PROPRIETARY

Title **DOCKING BUFFER**

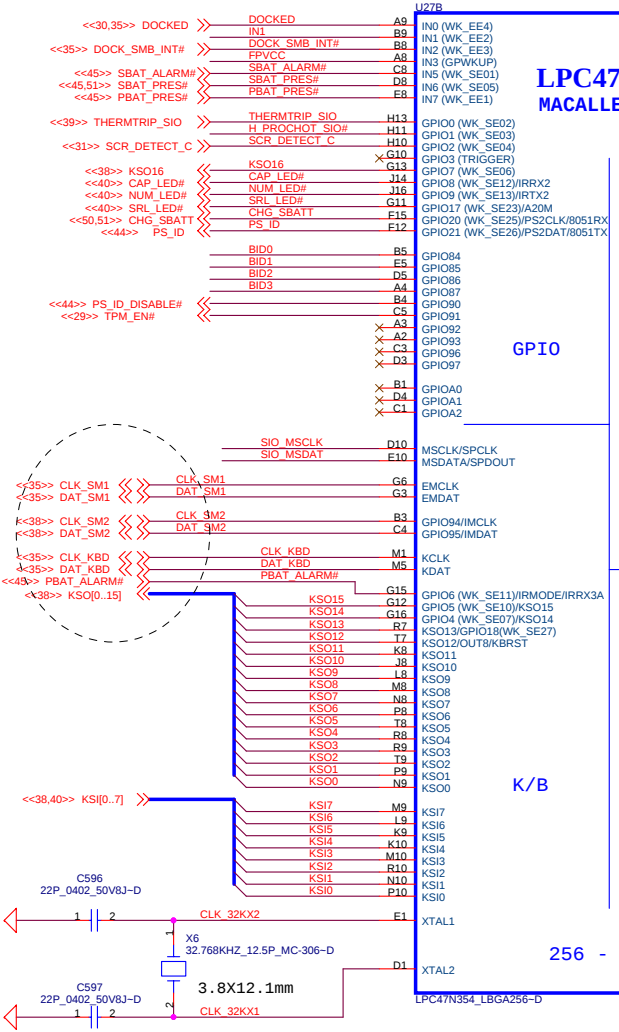
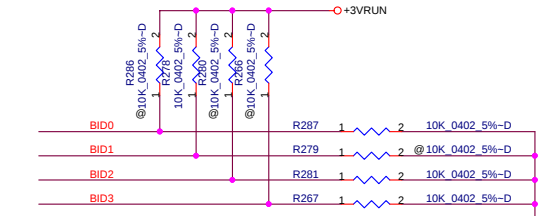
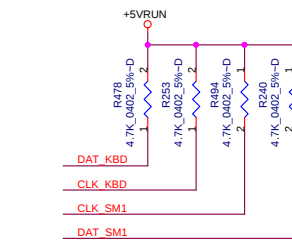
Size	Document Number Board Number LA2111	Rev 0.3
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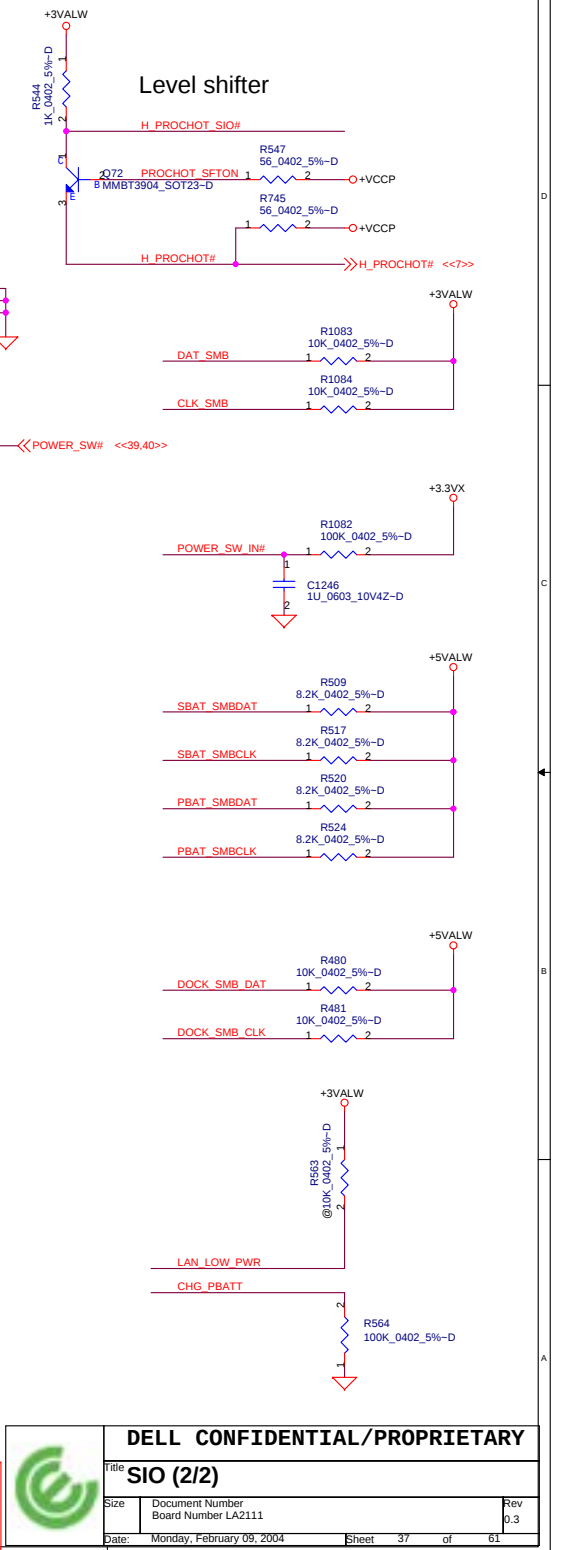


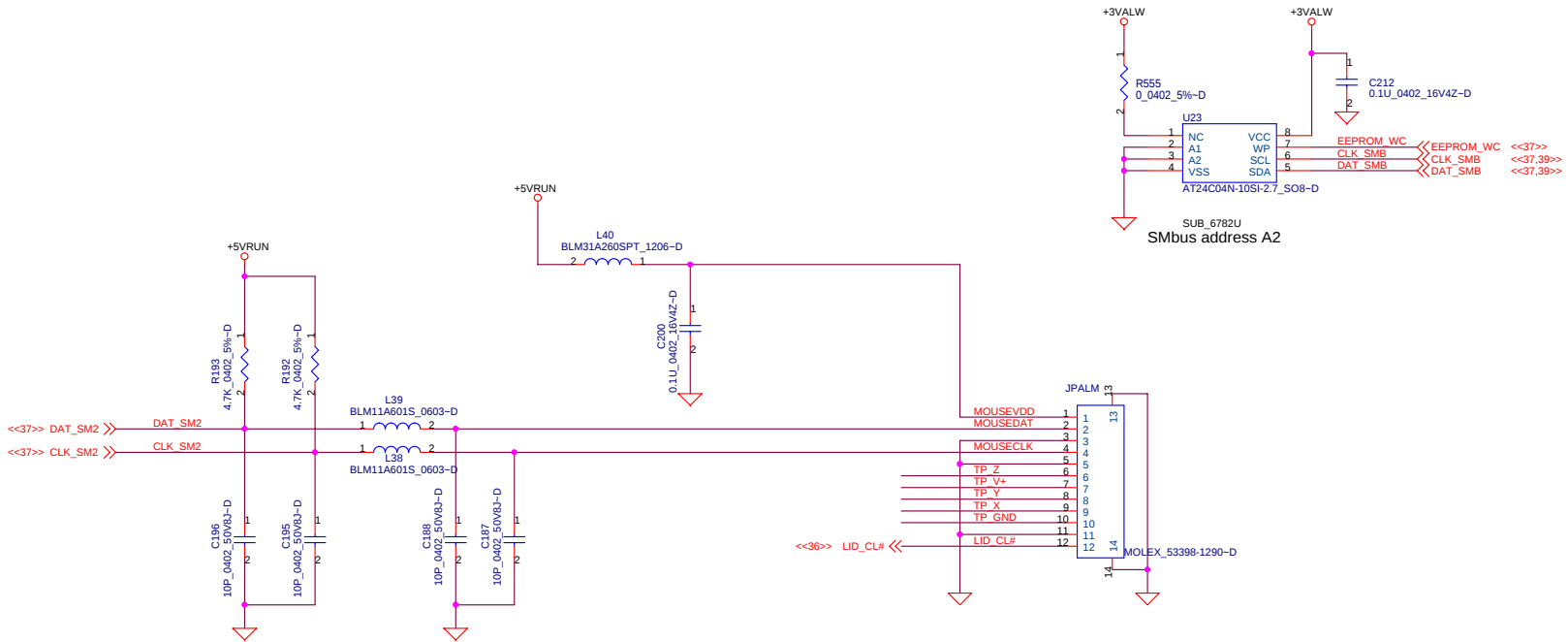
For SMSC issue, add schematic at bring-up.
Bill 10/31
For layout space, change to 0402 0 ohm.
Bill 11/04
Macallen III rev A IMCLK/IMDAT pair did not work properly. MacIII RevB has solved this issue. Delete R1198 - R1203 and connect directly.
Steven 01/09/2004



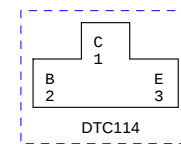
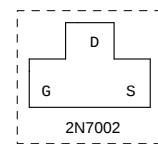
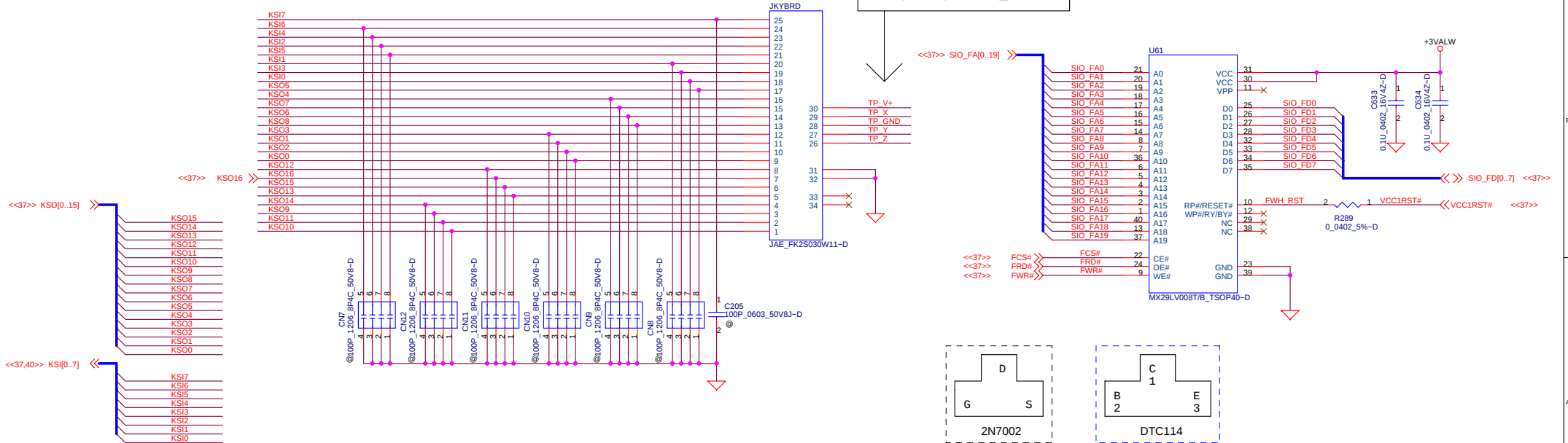
BID3	BID2	BID1	BID0	REV
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0	0	0	1	M01
0	0	1	0	X00

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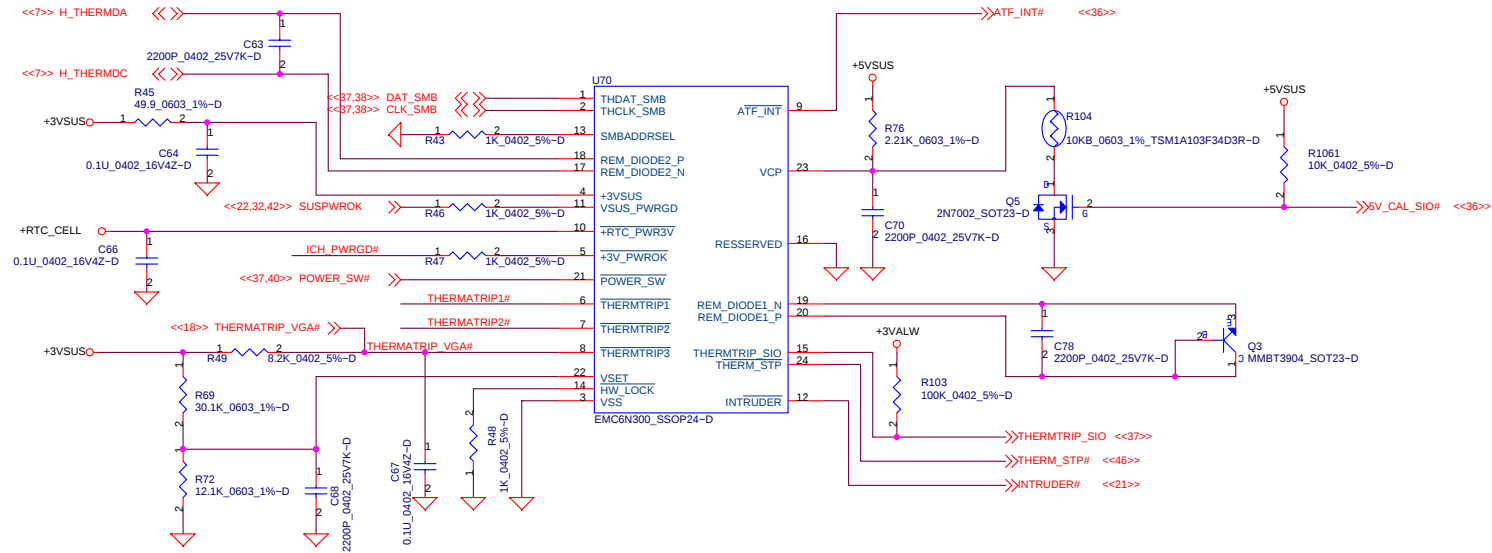
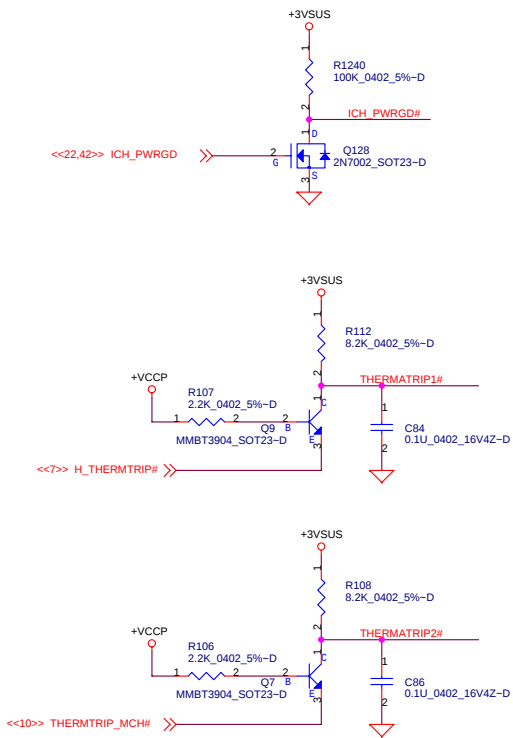




Keep no nosie coupled,
Especially the TP_GND

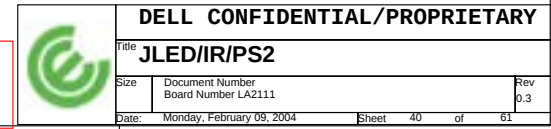
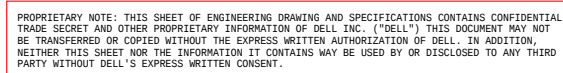
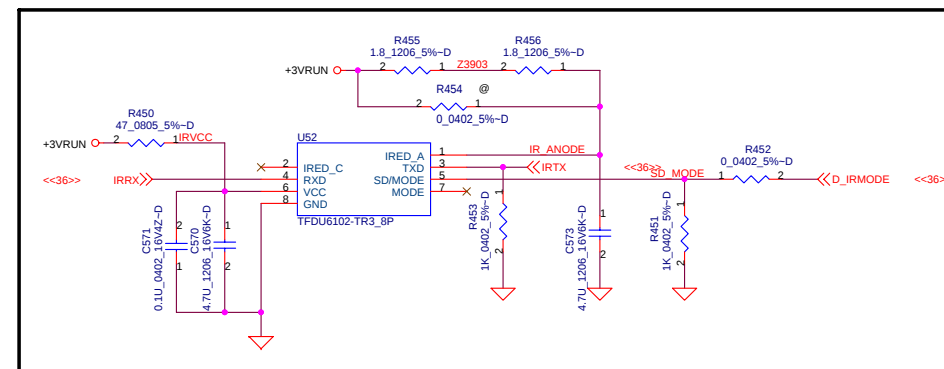
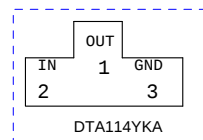


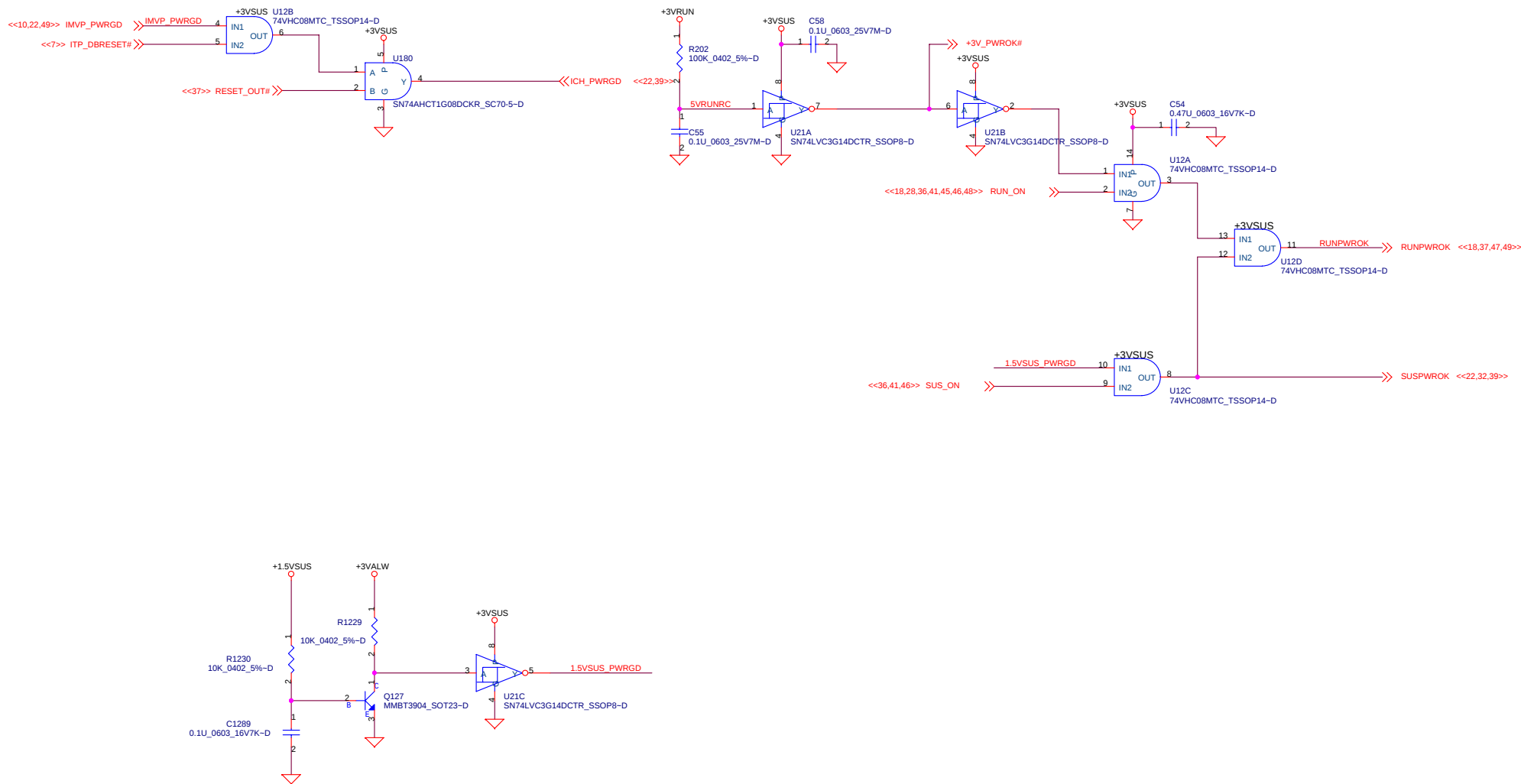
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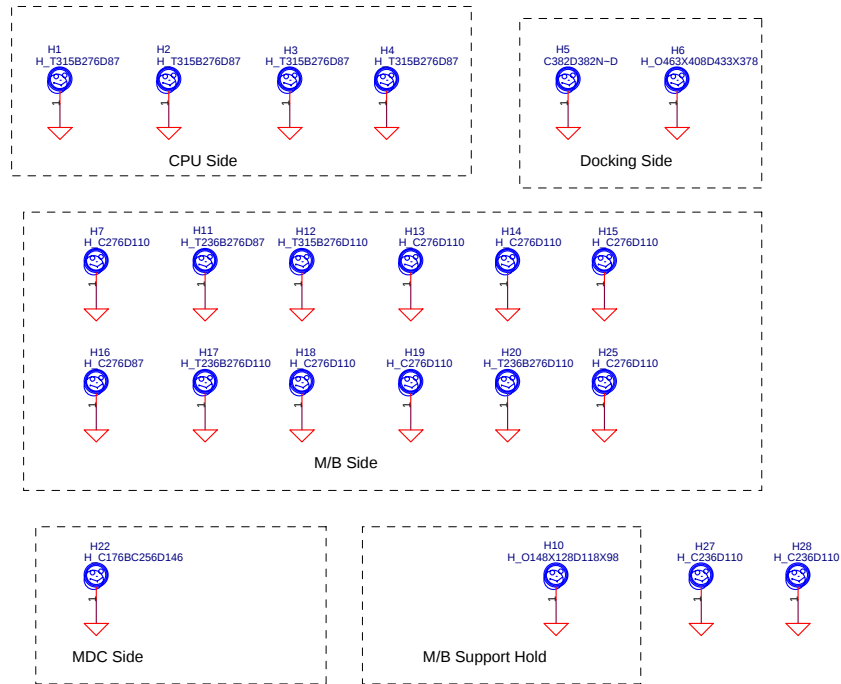
DELL CONFIDENTIAL/PROPRIETARY			
Title		Thermtrip	
Size	Document Number	Rev	
	Board Number LA2111	0.3	
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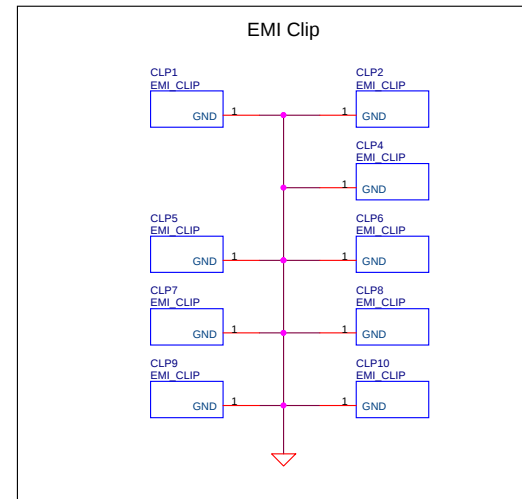
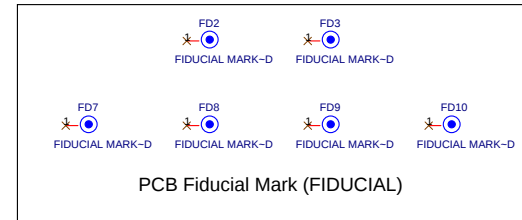
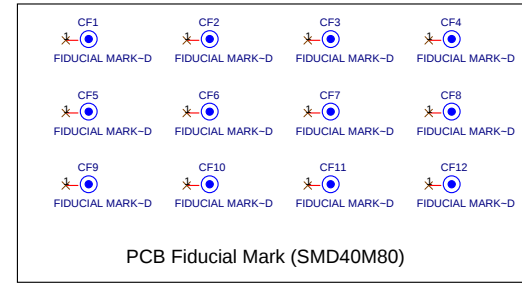


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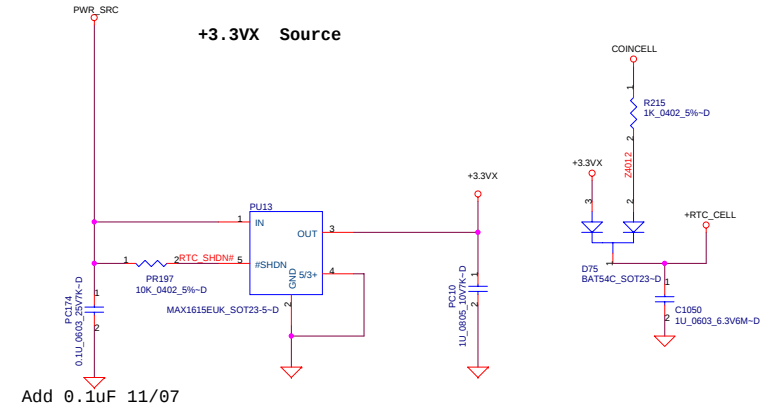
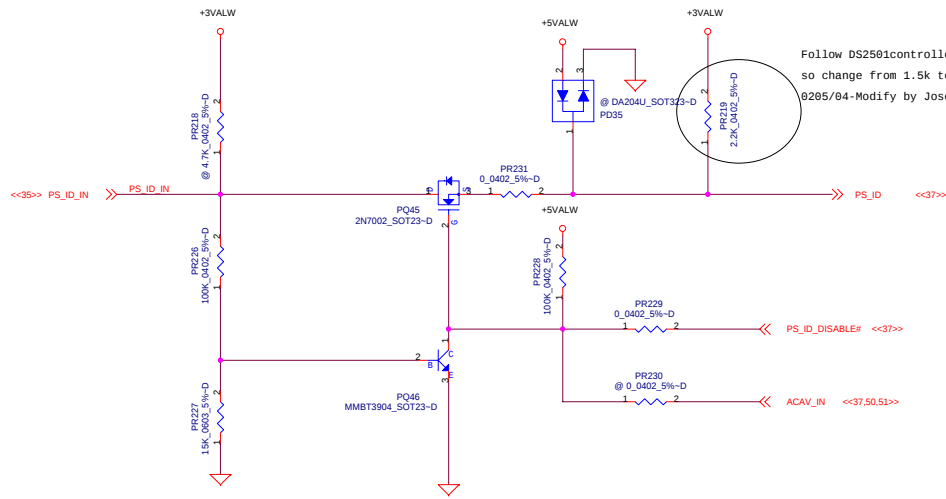
				DELL CONFIDENTIAL/PROPRIETARY			
Title				Power Sequence			
Size		Document Number		Board Number		Rev	
		Monday, February 09, 2004		Sheet 42		of 61	
						0.3	



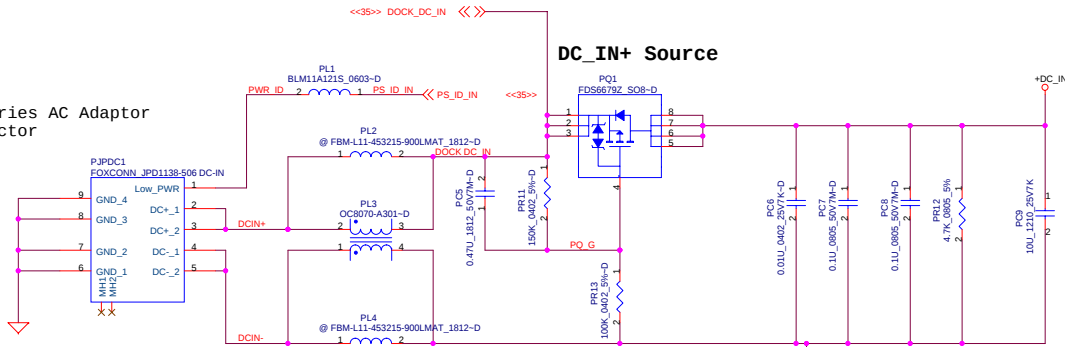
Fiducial Mark



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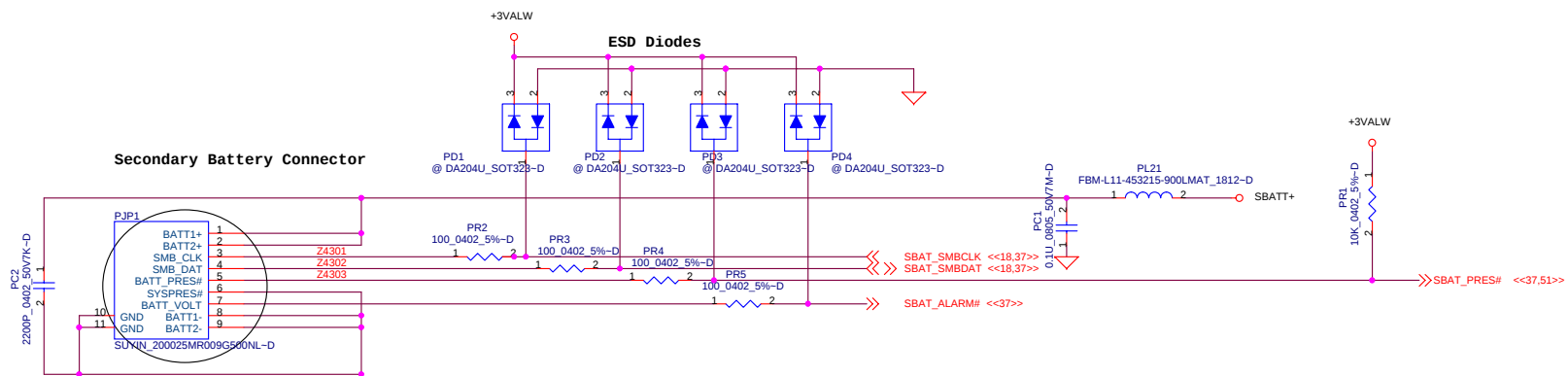


Z-series AC Adaptor Connector

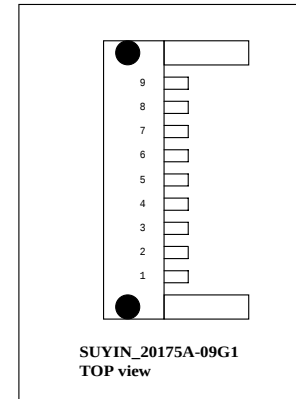
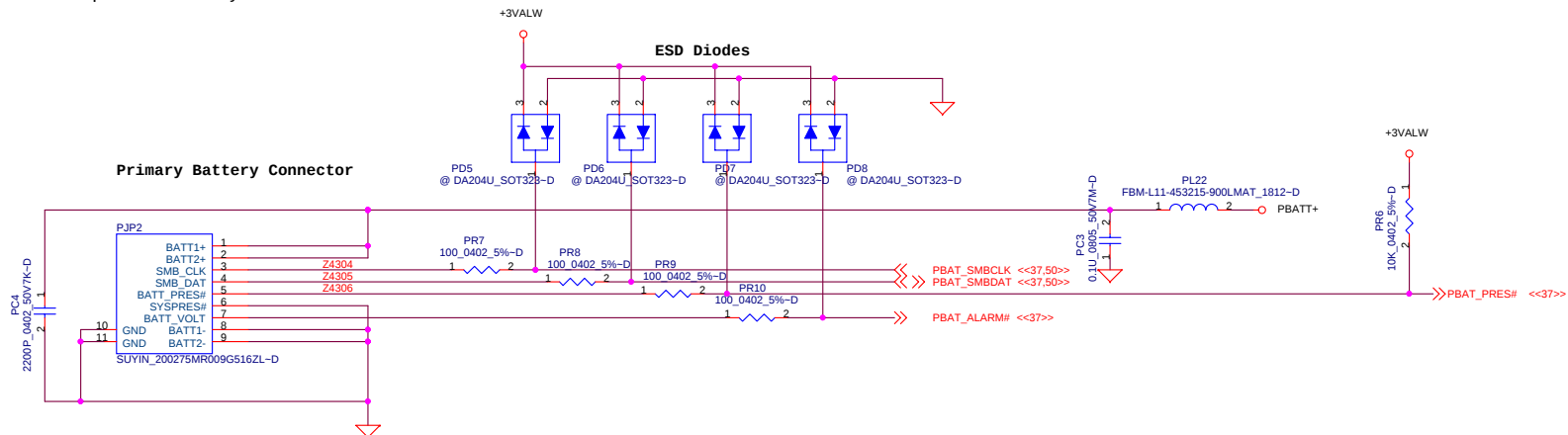


THE POINT
NOTE: *THE POINT LOCATED AT PS MODULE

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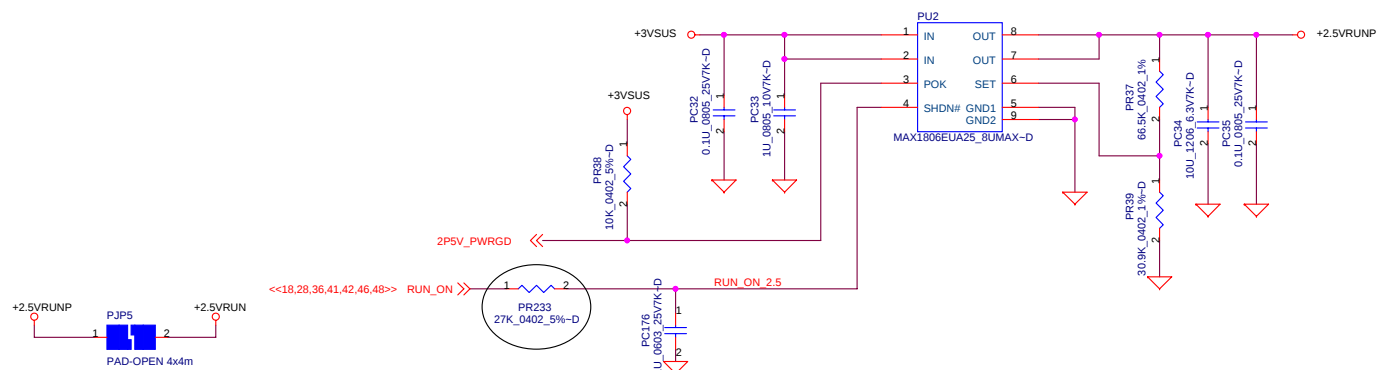


Update PJP1 symbol -01/29/2004



+2.5VRUN

$$R1=R2 * (Vo / 0.8 - 1), R2:25K\sim 100K.$$



Add Delay schematic, the value wait change.
12/16 Change to PWR materials

Change PR233 to achieve proper 1ms powerup delay.
Modify PR233 from 10 k to 27k by Joseph. -02/05

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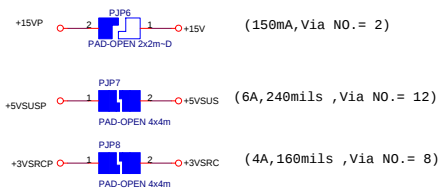
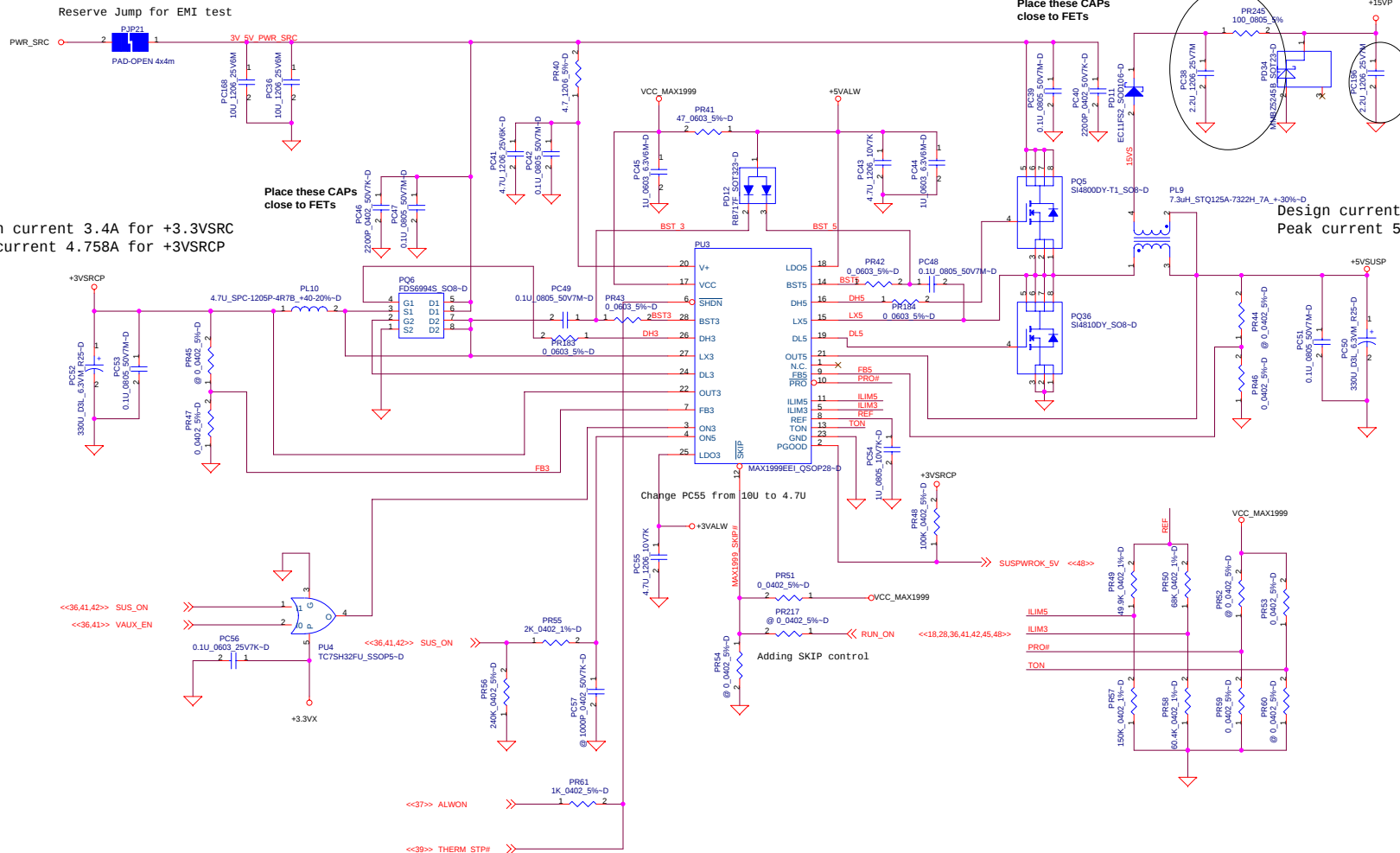
DELL CONFIDENTIAL/PROPRIETARY			
Title Battery Conn./+2.5V			
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DC/DC +3V/ +5V/ +15V

Modify by Joseph 01/28/04

Design current 3.4A for +3.3VSRCP
Peak current 4.758A for +3.3VSRCP

Design current 4A for +5VSUS
Peak current 5.7A for +5VSUS



+3VSRCP:
 $OCF = (((I_{lim3} / 10) / \text{Low-side MOSFET } R_{ds(on)} + 0.5 * I_L) * (+1.07))$
 $I_{lim3} = REF(60.4K / 60.4K + 68K) = 0.94V$
 Low side MOSFET $R_{ds(on)} = 22.75m \text{ ohms at } 100C$
 $I_L = ((V_{in} - V_o) / L) * T_{on} = ((19.5 - 3.3) / 4.7u) * ((1/300K) * 3.3/19.5) = 1.944 A$
 OCP TYP: 5.1A

+5VSUS
 $OCF = (((I_{lim5} / 10) / \text{Low-side MOSFET } R_{ds(on)} + 0.5 * I_L) * (+1.07))$
 $I_{lim5} = REF(150K / 150K + 49.9K) = 1.5V$
 Low side MOSFET $R_{ds(on)} = SI4810DY = 25m \text{ ohms at } 100C$
 $I_L = ((V_{in} - V_o) / L) * T_{on} = ((19.5 - 5) / 7.3u) * ((1/200K) * 5/19.5) = 2.546 A$
 OCP TYP: 7.273A

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+1.5VSUSP / +VCCP_1P05VP

Reserve Jump for EMI test

PJP22
PAD-OPEN 4x4mm

1.5V VCCP_PWR_SRC

Design current 5A for +VCCP_1P05VP
Peak current 7.124A for +VCCP_1P05VP

+VCCP_1P05VP

Change PC74 to ESR= 9m ohms

Design current 3A for +1.5VSUSP
Peak current 4.034A for +1.5VSUSP

12/10 Modify PL12 for high limitation

+1.5VSUSP

12/12 Depopulate PD30, PD31

12/18 Delete PR232 not need.

<<48>> SUSPWOK_1P8V

12/12 New VCCP powergood solution

+1.5VSUSP

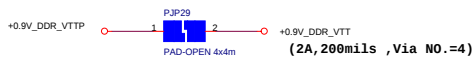
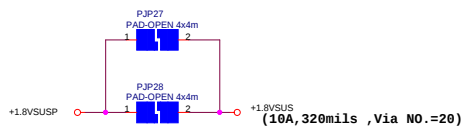
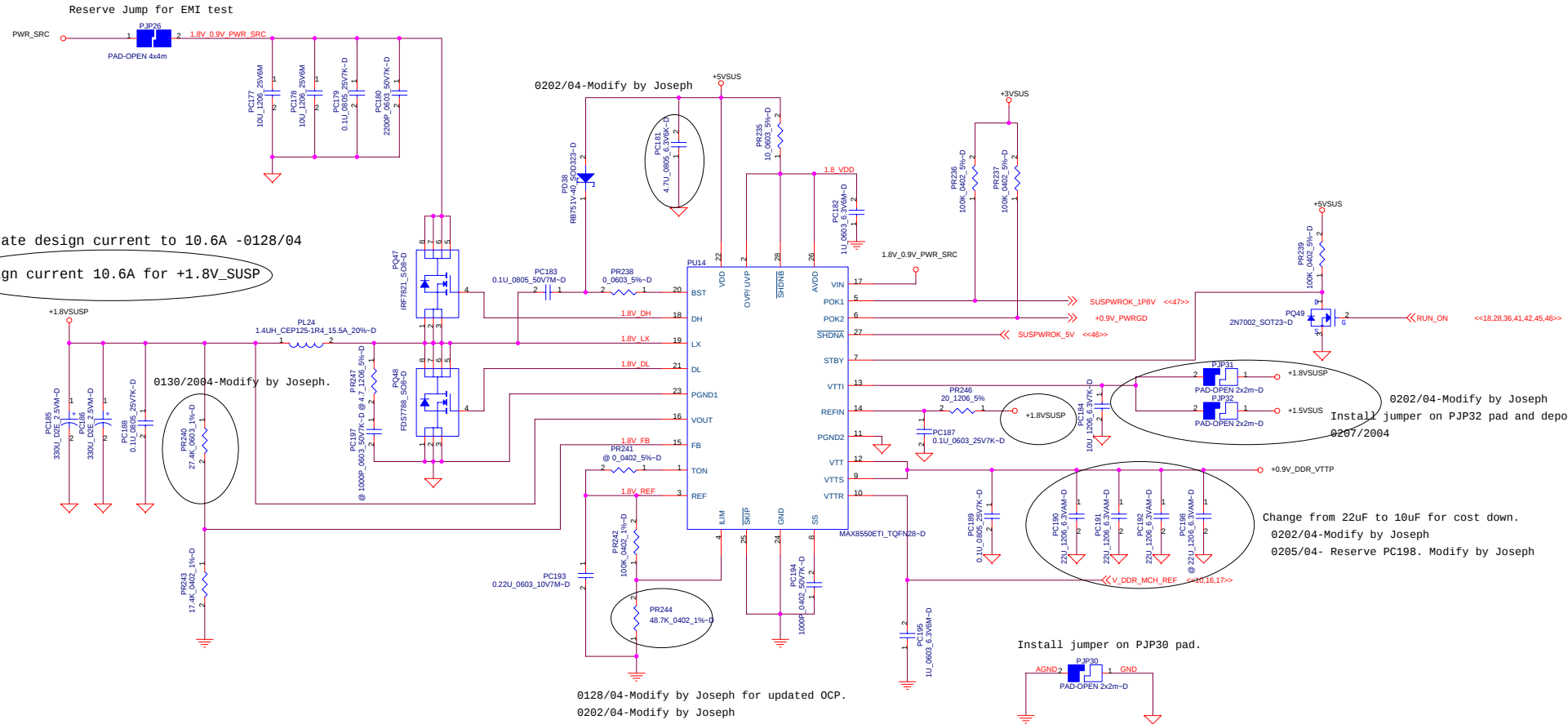
OCp: (((Ilim2 / 10) / Low-side MOSFET Rds(on) + 0.5 * IL)
Ilim2=REF(80.6K/80.6K+100K)=0.8925 V
Low side MOSFET Rds(on): 22.75m ohms at 100C
IL=((Vin-Vo) / L) * Ton=((19.5-1.5) / 5u) * ((1/255K) * 1.5/19.5)=1.23 A
OCp TYP: 4.462A

+VCCP_1P05VP

OCp: (((Ilim1 / 10) / Low-side MOSFET Rds(on) + 0.5 * IL)
Ilim1=REF(90.9K/90.9K+150K)=0.754V
Low side MOSFET Rds(on): FDS6676SS=0.01125 at 100C
IL=((Vin-Vo) / L) * Ton=((19.5-1.05) / 1.5u) * ((1/345K) * 1.05/19.5)=1.92 A
OCp TYP: 7.66 A

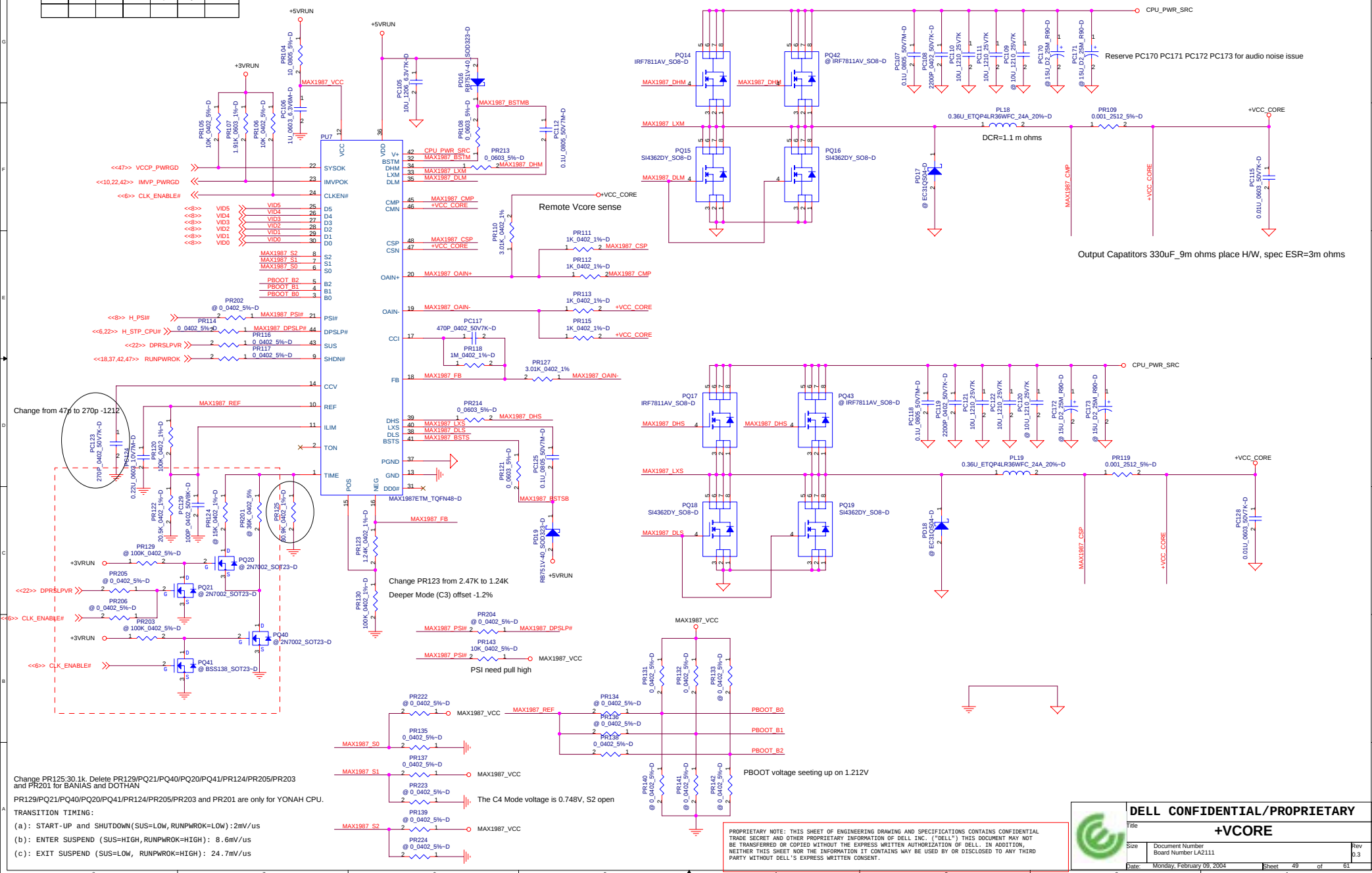
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+1.8VSUSP/ +0.9V_DDR_VTT
DDR2 Termination



```
+1.8VVSUP
OCP: (((Ilim / 10) / Low-side MOSFET Rds(on) + 0.5 * IL)
Ilim=REF(53.6k/53.6k+100k)=0.6979 V
Low side MOSFET Rds(on):6.5m ohms at 100C
IL=((Vin-Vo) / L)*Ton=((19.5-1.0) / 1.4u) * ((1/450k) * 1.8/19.5))=2.59A
OCP TYP: 11.37A
```

V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	1	1	1	0	1.484
0	1	1	0	0	1	1.308
1	0	1	1	1	1	0.956
1	1	1	1	0	0	0.748



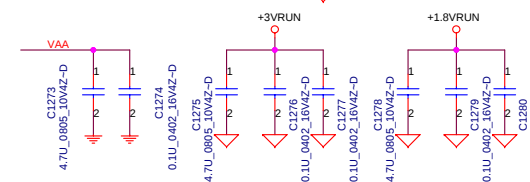
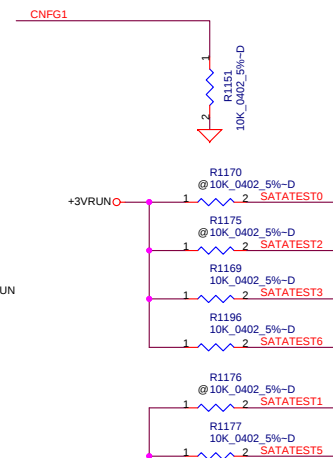
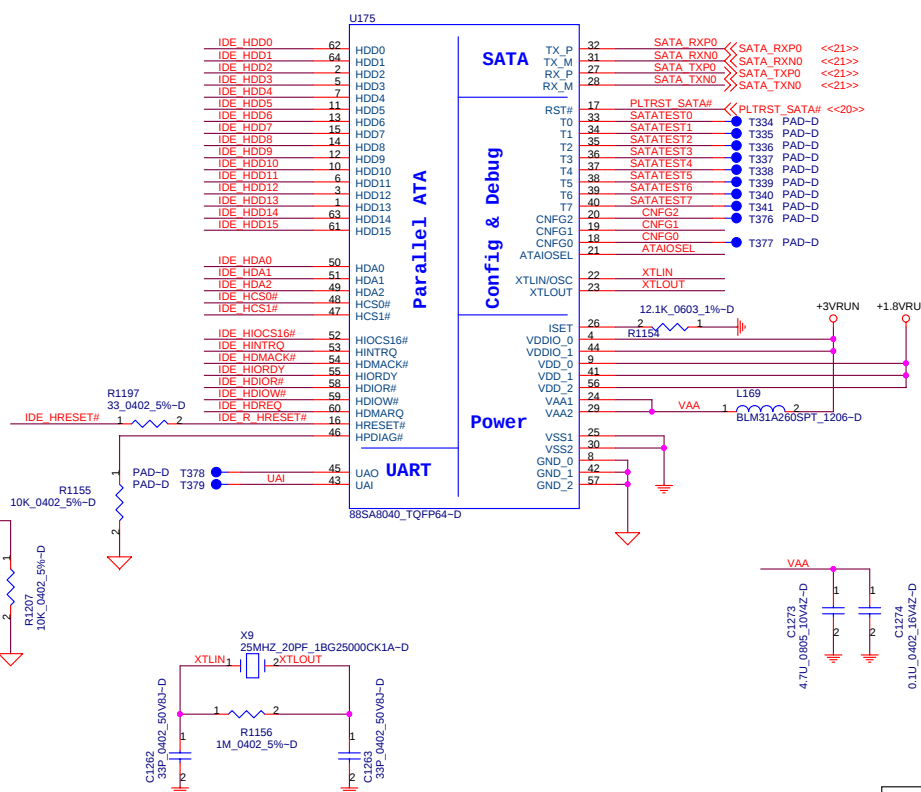
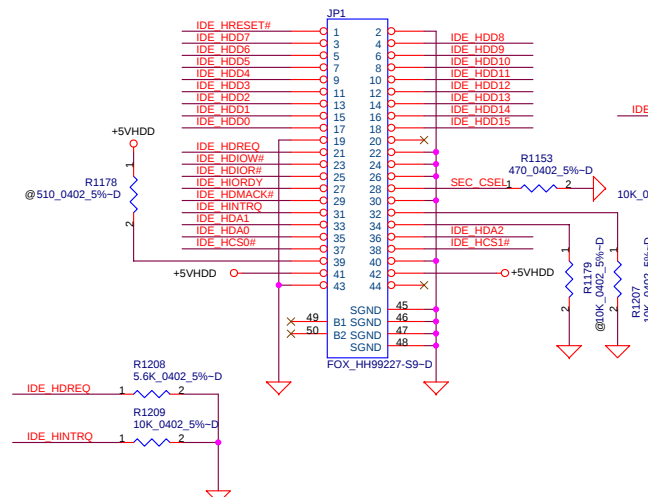
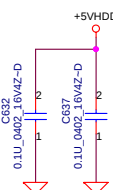
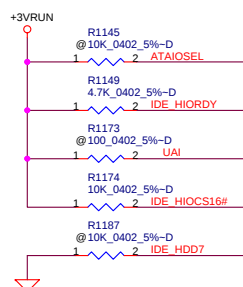
	SATATEST3	SATATEST4	
	0	0	20MHz
*	0	1	25MHz
	1	0	30MHz
	1	1	40MHz

Pin Name	Pin No.	Int. PUI/PD	Settings
SATATEST0	33	PD	NC
SATATEST1	34	PU	NC
SATATEST2	35	PD	NC
SATATEST3	36	PD	1
SATATEST4	37	PD	NC
SATATEST5	38	PU	0
SATATEST6	39	PD	NC
SATATEST7	40	PD	NC
CFG0	20	PD	NC
CFG1	19	PU	0
CFG2	18	PD	NC

PU / PD is internal pull-up or pull-down 100Kohm

Sets maximum transfer rate and UDMA mode

	CNFG2	CNFG1	CNFG0	NOTE
*	0	0	0	Device Mode 100MB/s
	0	0	1	Device Mode 133MB/s
	0	1	0	Device Mode 150MB/s
	1	0	0	Host Mode 100MB/s
	1	0	1	Host Mode 133MB/s
	1	1	0	Host Mode 150MB/s
	0	1	1	Reserved
	1	1	1	Reserved



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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	13	H/W	12/10	Bill	Power drop issue.	L43, L146 and L147 material change from BLM11A601S to BLM21PG600SN1D(3000mA).	0.2
2	20	H/W	12/10	Bill	VGA and LOM PLTRST# delay.	U25 Pin1 & Pin2 net name change to "PLTRST_DELAY#"	0.2
3	22	H/W	12/10	Bill	VGA and LOM PLTRST# delay.	U59 Pin AD21 add net name "PLTRST_DELAY#"	0.2
4	29	H/W	12/10	Bill	LOM isolation LRESET and PERST.	U164 Pin.M9 change net name to "PLTRST#".	0.2
5	32	M/E	12/11	Bill	Cardbus connector change.	Cardbus connector change to FOXCONN QT600806-7121.	0.2
6	39	H/W	12/11	CS	Populate Q9	Needed for full guardian.	0.2
7	10, 22, 42	H/W	12/11	CS	Delete R22 and connect IMVP_PWRGD directly to MCH and ICH	Resistor not needed.	0.2
8	42	H/W	12/11	CS	Delete R1228	Not used.	0.2
9	42	H/W	12/11	CS	Change U12 pin 10 to 1.5VSUS_PWRGD. Eliminate the need for U42D.	Simplifying the SUSPWROK logic, and this gate can be removed.	0.2
10	42	H/W	12/11	CS	Delete R753, C922, U67, R21, and C921	Not used.	0.2
11	42	H/W	12/11	CS	Change R1229 voltage to +3VALW	This will eliminate the glitch at the output of 1.5VSUS_PWRGD (U21 pin 5).	0.2
12	42	H/W	12/11	CS	Delete R1190, C1281, R1188, Q124, R1189, Q123, and R1195.	We are now using SUSPWROK_1P8V signal to enable the 1.5V rail.	0.2
13	9	H/W	12/11	CS	Remove C944 capacitor at +VCC_CORE.	Delete C944	0.2
14	33	H/W	12/11	CS	Add a No-Pop 0-ohm resistor connecting pin 3 of Q114 to Pin 3 of Q115. This is for future testing of the SMBUS to the LOM without the isolation. There is a push on the Dell side to remove this Isolation.	Add R1231	0.2
15	33	H/W	12/11	CS	Add a No-Pop 0-ohm resistor connecting pin 3 of Q116 to Pin 3 of Q117. This is for future testing of the SMBUS to the LOM without the isolation. There is a push on the Dell side to remove this Isolation.	Add R1232	0.2
16	13	H/W	12/11	GF	No stuff C287 and C1265. Change C1264 to 10uF	Modify OK.	0.2
17	21	H/W	12/11	GF	Can we delete some 0-ohm ser. Resistors on CPU interface?	Modify OK.	0.2
18	19	H/W	12/11	CS	Add a NO POP 0-Ohm resistor between pin 1 and pin 8 of L57 for a ground connection when L57 is removed.	Add R1233	0.2
19	38	M/E	12/12	Bill	Change JPLAM cconnector.	Change Pin define and connector library.	0.2
20	40	M/E	12/12	Bill	Change JLED1 and JSW1 cconnector.	Change Pin define and connector library.	0.2

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	19	H/W	12/12	Bill	Remove Q125, Q126, U176, U177, R1222 and R1223 for Docking connector shift-up 1mm.	Layout space issue, delete that component and add R1234, R1235, R1236 and R1237 for isolation int. GFX.	0.2
22	42	H/W	12/12	Bill	Delete R1132, R1131, R1130, Q122, Q121, C1254, and U174 and use VCCP_PWRGD generated by MAX1845.	Using new MAX1845 solution with Diode between PG00D and ON1 for VCCP Powergood.	0.2
23	36	H/W	12/12	CS	Add a No Pop 100K-ohm pulldown resistor to VAUX_EN signal for potential SMSC floating pins on power down. Nimitz team recommended this pulldown for safety.	Add R1238	0.2
24	36	H/W	12/12	CS	Add a 0-ohm resistor in parallel with R228 connected to +3.3VX.	Add R1239	0.2
25	36	H/W	12/12	CS	No Pop R228. Change Macallan VCC0 voltage from +RTC_CELL to +3.3VX per D'05 recommendation.. CMOS settings are now stored in ICH6, thus the RTC rail doesn't need to power this signal.	No pop R228	0.2
26	37	H/W	12/12	CS	Change R1082 pullup voltage to +3.3VX	Modify it.	0.2
27	40	M/E	12/15	Bill	M/E request change JLED1 connector.	Connector change to MOLEX_53398-0690.	0.2
28	30	H/W	12/15	PN	R971-978 should be 0603 package.	Change from 0402 package to 0603 package.	0.2
29	7	H/W	12/15	CS	Change R1160 to 54.9 ohms per Intel.	Change from 220 Ohm to 54.9 Ohm.	0.2
30	7	H/W	12/15	CS / GF	Change R17 to 200 ohms per Intel.	Change from 330 Ohm to 220 Ohm.	0.2
31	19	H/W	12/16	GF	Move D4, D5, D6 back to +3vrun	Modify done	0.2
32	39	H/W	12/17	CS	Invert ICH_PWRGD signal with a 7002 FET and a 100K pullup to +3VSUS. Name the signal ICH_PWRGD# and connect it to pin 1 of R47.	Modify done	0.2
33	43	M/E	12/17	Bill	Add 2 screw on HDD side	Add H27, H28	0.2
34	33	H/W	12/17	CS	No Pop Q114 and Q116.	Following Azeda and using only one level of isolation for SMBUS.	0.2
35	28	M/E	12/17	Bill	Change BT connector.	Change Pin define, to be change to 9 pin connector.	0.2
36	41	H/W	12/18	Bill	RUN_ENABLE singal reserve voltage issue.	Add R1242 no pop.	0.2
37	28	H/W	12/18	Bill	Swap JBT pin define.	For layout route easy, change pin define.	0.2
38	20	H/W	12/18	CS	U164 pin M9 PLTRST# signal should be buffered here for sufficient signal drive strength.	Add U179, R1243	0.2
39	20	H/W	12/18	CS	Regulatory team has reported damage to FETs in the Dock area, want to ensure proper rating of near 3KV.	Q43 change to DTC144EKA_S0T23	0.2

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40	38	H/W	12/18	Bill	Remove BIOS debug connector.	For layout space issue, delete it.	0.2
41	39	H/W	12/19	Bill	Delete R1241 and signal "+3V_PWR0K#" same as Tobago, Sullivan, Azeda	Modify Done	0.2
42	37	H/W	12/21	CS	No Pop R1202 and R1203, Populate R1198, R1199, R1200, and R1201	Modify Done	0.2
43	37	H/W	12/21	Bill	Change Board ID	R286 no stuff, R287 stuff.	0.2
44	38	M/E	12/21	Bill	Change JPLAM connector to Molex_53398-1290.	For M/E request, change it.	0.2
45	31	M/E	12/21	Bill	Change JP5 connector to Molex_53398-0990.	For M/E request, change Samrt-Card connector.	0.2
46	29	H/W	12/24	PN	Dell LOM team requests to make notation 0.5W capacity on R1051	Change to 1210 Size	0.2
47	37	H/W	12/24	CS	U27 GPIO20 is actually an open drain signal, so CHG_SBATT should be pulled high.	Add Pop resister R1244, non-pop R759.	0.2
48	13	H/W	12/24	Bill	Add +VCCP_CRT and +1.5VRUN_TV.	For layout easy control.	0.2
49	26	H/W	12/24	Bill	Change Audio jack location.	Audio jack from JP8 change to JAUD0, JAUDI0D change to JM1C	0.2
50	19	H/W	12/24	Bill	JVGA connector footprint error.	Footprint change, change pin 16, 17 to NC, Pin 17, 18 to GND.	0.2
51	43	M/E	12/24	Bill	Add screw H24	For M/E request add H24.	0.2
52	27	H/W	12/24	Bill	Change USBP7 pair for layout issue.	Exchange USBP7+/USBP7- and USBP7_D+/USBP7_D-.	0.2
53	52	M/E	12/24	Bill	Change HDD connector.	Change HDD same Nimiz.	0.2
54	29/22	H/W	12/24	Bill	Change net name for PCIE pair.	Add net name singal easy control for PCIE.	0.2
55	35	H/W	12/25	Bill	R616 add @.	Same as LBK.	0.2
56	6/10/12 13/19	H/W	12/29	Bill	Int. GFX disable.	No stuff R1071, R1072R1133, R1134, R1135, R1136, R1137, R1138, R1139, R1140, R1141, R1142, R1210, L8, C201, C207, C245, R1234, R1235, R1236, R1237. Stuff R1211, R1212, R1213, R1214.	0.2
57	13	H/W	12/29	Bill	Change Inductor	Change L6, L9, L29, L7 from BLM11A601S to BLM18PG181SN1.	0.2
58	13	H/W	01/02	GF	Change Inductor	Change L43, L146, L147 from BLM21PG600SN1D to BLM18PG181SN1.	0.3
59	37	H/W	01/02	Bill	Change Board ID	R279, R286 no stuff, R278, R287 stuff.	0.3
60	43	EMI	01/02	Bill	Add EMI Clip	Add EMI Clip 7 pcs.	0.3
61	13	H/W	01/02	Bill	Change R1212 pin 2 to GND.	Follow Intel check list, change VCC_SYNC to GND for int. GFX disable.	0.3
62	37	H/W	01/05	PN	Change R1121 pu-high to +3VRUN	Modify.	0.3
63	10	H/W	01/06	GF	Remove R1213 and connect DREFCLK directly to +1.5vrun	Modify.	0.3

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64	10	H/W	01/06	GF	Remove R1214 and connect DREFCLK# directly to GND	Modify.	0.3
65	6	H/W	01/06	GF	Remove R178 and connect DREF_SSCLKP directly to +1.5vrun	Modify.	0.3
66	12	H/W	01/06	GF	Remove R1071, R1072, R1118, R1119	Modify.	0.3
67	12	H/W	01/06	GF	Remove R1133, R1134, R1135	Modify.	0.3
68	12	H/W	01/06	GF	Remove R1064, R1065, R1066. Connect TV_YR, TV_CVBS_R, TV_C_R directly to ground	Modify.	0.3
69	12	H/W	01/06	GF	Remove R1062.Connect pin J18 directly to gnd.	Modify.	0.3
70	12	H/W	01/06	GF	Remove R1136-R1140.	Modify.	0.3
71	12	H/W	01/06	GF	Connect Alviso pins blue/blue#, red/red#, green/green# directly to +vccp	Modify.	0.3
72	12	H/W	01/06	GF	Remove R1063, connect directly to +vccp.	Modify.	0.3
73	12	H/W	01/06	GF	Remove R1141, R1142. Connect these pins directly to gnd.	Modify.	0.3
74	12	H/W	01/06	GF	Remove R1067, R1068, R1069	Modify.	0.3
75	13	H/W	01/06	GF	Remove L164-L168, C1229-C1240.	Modify.	0.3
76	13	H/W	01/06	GF	Connect Alviso pins F17, E17, D18,C18, F18, E18, H18, D19, H17 directly to gnd. (VCCA_TVDAC A,B,C and VCCA_TVBG)	Modify.	0.3
77	13	H/W	01/06	GF	Remove R1210. Connect directly to gnd.	Modify.	0.3
78	13	H/W	01/06	GF	Remove L8, C201, C207, C245. Connect pins E19 and F19 directly to +VCCP	Modify.	0.3
79	13	H/W	01/06	GF	Remove R1192, R1191, D80, D79	Modify.	0.3
80	42	H/W	01/06	CS	Delete R24	Modify.	0.3
81	42	H/W	01/06	CS	Delete All 4 instances of U42	Modify.	0.3
82	42	H/W	01/06	CS	Add a single 5-pin AND gate to replace U42A.(Or an unused AND gate if nearby) Connect RESET_OUT# to the second input pin.	Modify.	0.3
83	42	H/W	01/06	CS	Delete R23	Modify.	0.3
84	42	H/W	01/06	CS	Delete R1225 and R1227	Modify.	0.3
85	42	H/W	01/06	CS	Connect RUN_ON to pin 2 of U12.	Modify.	0.3

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86	41	H/W	01/06	CS	Delete R1194	Modify.	0.3
87	27	H/W	01/06	CS	Populate 0-0hm Resistors or USB filters instead of the Inductors (No POP L21, L41 L22, L23, L28, L13, L129, and L131 Populate R348 - 359 ad R890, R891, R950, and R951) Please do this for M01 board build and for X00 Schematic	Modify.	0.3
88	27	H/W	01/06	CS	Remove L59, L62, L61, and L128 and replace all with 0-0hm resistors for M01 Build and for X00 Schematic	Modify.	0.3
89	7	H/W	01/09	Steven	Del T332, T333 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
90	10	H/W	01/09	Steven	Del T380, T381, T300, T6 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
91	11	H/W	01/09	Steven	Del T2, T3, T4, T5 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
91	19	H/W	01/09	Steven	Del T375 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
92	21	H/W	01/09	Steven	Del T155 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
93	28	H/W	01/09	Steven	Del T280 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
94	36	H/W	01/09	Steven	Del T255, T259, T342, T344, T345, T346, T347, T348, T349, T350, T351, T352, T353, T354, T355, T356, T357, T358, T359, T360, T361, T362, T363, T364 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
95	37	H/W	01/09	Steven	Del T366, T367, T368, T370, T372, T373, T257, T258, T343, T365, T369, T374 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
96	37	H/W	01/09	CS	Delete R1198, R1199, R1200, R1201, R1202, R1203 and connect directly. Macallan III rev A IMCLK/IMDAT pair did not work properly. MacIII RevB has solved this issue.	Modify.	0.3
97	12	H/W	01/09	GF	Remove R1215 from schematic.	Modify.	0.3
98	13	H/W	01/09	GF	Remove L29, C47, C8, Connect DPLLA directly to +1.5vrun Remove L6, C48, C51, Connect DPLLB directly to +1.5vrun	Modify.	0.3
99	13	H/W	01/09	GF	Change C811 to the same component as C812.	Modify.	0.3
100	13	H/W	01/09	GF	No stuff C783 to support ext. vga.	Modify.	0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
101	18	H/W	01/09	CS	Add an 15U 25V De-pop capacitor C1290 in G_PWR_SRC for improve this power plane stability	Modify.	0.3
102	18	H/W	01/12	CF	Add a no stuff cap. for add a CPU bulk decoupling pads back to layout.	Modify.	0.3
103	7	H/W	01/13	CF	Remove C450, C452 non-use item for saving layout space	Modify.	0.3
104	43	H/W	01/17	CF	Delete H23 from M/B.	Modify.	0.3
105	16, 17	H/W	01/19	Bill	DDR termination swap.	For layout routing easy, swap pin define.	0.3
106	6	H/W	01/27	GF	Change BOM to support Dothan 533Mhz	No stuff R65, pop. R66.	0.3
107	29	H/W	01/27	PN	Change C1111 from 10uF to 22uF (1206)	Modify.	0.3
108	8	H/W	01/27	GF	Short PJP16 and open PJP17 for X00 build.	Modify.	0.3
109	29	H/W	01/27	PN	Populate R1180 to allow activating TPM mode.	Modify.	0.3
110	32	H/W	01/28	GF	changing C1201, C1202 to be the same as 0402 package as C1203 to save board space.	Modify.	0.3
111	10	H/W	01/28	GF	Intel recommends pop C745 with 0.1uf cap.	Modify.	0.3
112	36	H/W	01/28	CS	Populate R1238 for eliminate glitch..	Modify.	0.3
113	15	H/W	01/29	CS	C479 and C495 change to 47UF like Nimitz for cost savings.	Modify.	0.3
114	29	H/W	01/29	PN	V.2P5 LAN needs bigger bulk caps, add 2 more 22uF caps C1291, C1292	Modify.	0.3
115	29	H/W	01/30	PN	L155 replaced by 0 ohm resistor (R1245, 00hm 0603), C1215 and C1135 nopop.	Modify.	0.3
116	29	H/W	01/30	PN	L149, C1209 nopop.	Modify.	0.3
117	40	H/W	02/02	CS	no pop R454	Modify.	0.3
118	40	H/W	02/02	CS	Change U52 from the discontinued TFDU6101E to the new TFDU6102.	Modify.	0.3
119	20	H/W	02/02	CS	Add a no pop 33-ohm resistor (R1246) to PLTRST_LOM# and connect to PCIRSTB2# for pop option.	Modify.	0.3
120	20	H/W	02/02	CS	Add a no pop 33-ohm resistor (R1247) to PLTRST_VGA# and connect to PCIRSTB2# for pop option.	Modify.	0.3
121	41	H/W	02/02	CS	Q55 change to DI4810.-02/02	Modify.	0.3
122	29	H/W	02/02	CS	Removed F14 connect from L151 Pin 1	Modify.	0.3
123	42	H/W	02/02	CS	Change R1230 from 330 to 1K	Modify.	0.3

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124	43	H/W	02/02	CS	Change H6 to H_0463X408D433X378 Change H10 to H_0148X128D118X98	Modify.	0.3
125	16	H/W	02/02	CS	change C1047, C1049 to 0603 size for avoid highlimit issue in DIMM region.	Modify.	0.3
126	16	H/W	02/02	GF	Change C1048, C1046, C1045 and C1168 voltage rating to 6.3V for saving cost.	Modify.	0.3
127	17	H/W	02/02	GF	Change C143, C153, C1042-C1044 and C1177 voltage rating for save cost	Modify.	0.3
128	43	H/W	02/03	Steven	Add 3 EMI clip.	Modify.	0.3
129	29	H/W	02/04	PN	Pop R1102. Depop R1103, R1104	Modify.	0.3
130	21	H/W	02/04	GF	Populate R1248	Modify.	0.3
131	20	H/W	02/04	CS	Add a 0 ohm series termination R1251 between the ICH and U25A. This way we can go back to the original M00 design	Modify.	0.3
132	29	H/W	02/04	PN	L149 and C1209 and connect U164 pin F14.	Modify.	0.3
133	6	H/W	02/04	CS	Move SATA clock pair to SRC4 pair on CK410. and connect PCIE_VGA clock to SRC3, PCIE_LOM clock to SRC1	Modify.	0.3
134	21	H/W	02/04	CS	Follow Issue list 1648 to remove the note of R940.	Modify.	0.3
135	21	H/W	02/04	CS	Follow Issue list 1646 to remove the note of R1248.	Modify.	0.3
136	20	H/W	02/05	GF	Add a pop resister R1252	Modify.	0.3
137	21	H/W	02/05	Steven	Correct the Note of R940 and R1248.	Modify.	0.3
138	20,22,28	H/W	02/05	Steven	SWAP RN118, RN117, RN6, RN130, RN121, RN1, RN120, RN131, C13, C14 pin connect for layout routing.	Modify.	0.3
139	43	H/W	02/06	ME	Modify H1, H2, H3, H4, H12, H20 as ME request	Modify.	0.3
140	41	H/W	02/06	CS	Change R605 to 100K for proper voltage level during low battery charge state.	Modify.	0.3
141	35	H/W	02/07	CS	Add D76 in Q43 DOCKED for protection ESD damage.	Modify.	0.3
142	41	H/W	02/07	CS	Change Q55 to DI4800 for cost saving.	Modify.	0.3
143	41	H/W	02/07	Steven	Add a no-pop Q131 3456 parallel with Q55 for this build.	Modify.	0.3
144	43	H/W	02/07	Steven	Remove a no use EMI clip CLP3	Modify.	0.3
145	30	H/W	02/07	Steven	Change RJ1 connector from 5PIN to 2PIN.	Modify.	0.3
146	41	H/W	02/07	ME	Change smart card connector as ME request.	Modify.	0.3

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Version Change List (P. I. R. List) for Power Circuit

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1	P47	+1.5VSUSP / +VCCP_1P05VP	12/09/2003	Dell	PL12 choke had height limitation on secondary side	Change PL12 from CDRH125 4.4uH_5A to SIL1035 5uH_5.5A	0.1
2	P48	+1.8VSUSP/ +0.9V_DDR_VTT	12/09/2003	Compal	Change SC1486 to SC1486A for DDR2 (REFIN threshold voltage change from 0.8V to 0.5V)	Change PU6 from SC1486 to SC1486A version	0.1
3	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Add a diode between the PU5 PGOOD signal and ON1 signal, so that when ON1 is low, PGOOD is low. And when ON1 is high, PGOOD is released and can go high.	This is a new VCCP powergood solution. Changing to match Azeda.	0.1
4	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Change PR232 pull-up voltage to +3VSUS.	Change PR232 pull-up voltage from +5VSUS to +3VSUS.	0.1
5	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Change MAX1845_PWRGD signal name to VCCP_PWRGD	Implementing new powergood solution for VCCP.	0.1
6	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Depopulate PD30 and PD31	Don't use for cost down	0.1
7	P49	+VCORE	12/12/2003	Dell	Change PC123 from 47pF to 270pF	Improve noise immunity with a reduction in the transient response speed.	0.1
8	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Change SUSPWOK_1.5V signal to SUSPWOK_1P8V.	To match other D'05 platforms, this change will also reduce the amount of logic gates for power sequencing circuitry.	0.1
9	P45	Battery Conn./+2.5V	12/16/2003	Compal	Change to Power materials	Change C1288 to PC176, R1224 to PR233.	0.1
10	P47	+1.5VSUSP / +VCCP_1P05VP	12/18/2003	Dell	Delete PR232, not needed	Deleted because PR105 had existed.	0.1
11	P50	Charger	01/08/2004	Dell	Add PD37, PR234 to fix MAX1535A Charger issue when Battery undervoltage is detected. Will waiting MAX1535B and delete it.	Add PD37, PR234	X00
12	P48	+1.8VSUSP/ +0.9V_DDR_VTT	01/27/2004	Dell	Implement MAX8550 regulator	Delete SC1486A regulator and adding MAX8550 Regulator for DDR2 power source.	X01
13	P46	+3.3V/+5V/+15V	01/28/2004	Dell	Adding +15V current limit	Add PC196 PR245 and Change PC38	X01
14	P47	+1.5VSUSP / +VCCP_1P05VP	02/02/2004	Dell	Change PC74 ESR from SER 15m to 9 m ohms.	Change PC74 from 330u_15m to 330u_9m.	X01
15	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/02/2004	Dell	Adding PJP31, PJP32 Jump, +1.8VSUS or 1.5VRUN input voltage for VTTI of Max8550	Adding PJP31, PJP32 Jump.	X01
16	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/02/2004	Dell	Modify +1.8VSUS Regulator OCP	Change PR244 from 53.6K to 48.7K.	X01
17	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/02/2004	Dell	Modify Bypass capacitor Power supply for DL Gate driver of MAX8550	Change PC181 from 1uF to 4.7uF.	X01
18	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/05/2004	Dell	Reserve PC198 for the future cost down.	Add @ PC198.	X01
19	P44	+DCIN	02/05/2004	Dell	Change PR219 to 2.2Kohms per AC Adapter group recommendation.	Change PR219 from 1.5K to 2.2K ohms.	X01
20	P45	Battery Conn./+2.5V	02/05/2004	Dell	Change PR233 to achieve proper 1ms powerup delay.	Change PR233 from 10k to 27kohms.	X01
21	P50	Charger	02/05/2004	Dell	Add note to +VCHGR rail - "Maximum Battery Charge current = 6.2A when system off"	Add note to Charger circuit	X01
22	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/06/2004	Compal	Change 1.8V Regulator switch frequency from 450k to 300kHz	depopulate PR241	X01
23	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/07/2004	Dell	Install jumper on PJP32 pad to connect to 1.5VSUS	PopPJP32 pad and depop PJP31.	X01

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