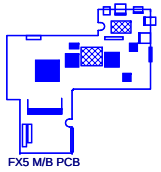
FX5 SAPPORO-INTEGRATED

REV : A00

POWER

- SYSTEM RESET CIRCUIT — PG 39
- RUN POWER SW — PG 46
- BATT CHARGER — PG 40
- AC/BATT CONNECTOR — PG 41
- CPU VR — PG 44
- DC/DC — PG 45 — +3.3V_SUS/+5V_SUS/+15V_SUS
- REGULATOR — PG 42 — VCC_NB & +1.2V_ALW_SUS
- REGULATOR — PG 43 — +1.8V_SUS/+0.9V_DDR_VTT +1.5V_RUN



AMD S1
Turion 64 Rev.F Dual-Core/
Dual-Core 35W
(638 S1g1 socket)
PG 3,4,5,6

- DDR2-SODIMM1 PG 7,8 — 667/800 MHZ DDR II
- DDR2-SODIMM2 PG 7,8 — 667/800 MHZ DDR II
- HT_LINK

CLOCK
SLG84605TTR
PG 18

FAN & THERMAL
EMC4001
PG 35

RS690T
465 FCBGA
PG 9,10,11,12,13

- DDR2-MEMORY DEVICE 8MX16X4 84-PIN FBGA PG 13 — 400 MHZ DDR II
- Panel CONN. PG 19 — LVDS
- TVout CONN. PG 20 — TVOUT
- CRT CONN. PG 20 — VGA
- A_LINK
- PCIEx1 — MINI-CARD WWAN PG 26
- PCIEx2 — MINI-CARD x2 WLAN & WPAN PG 25
- PCIEx1 — EXPRESS-CARD R5538 PG 27

SB600
549 BGA
PG 14,15,16,17

- CD-ROM PG 24 — IDE
- SATA - HDD PG 24 — SATA
- IHDA
- USB2.0 (P6)
- USB2.0 (P4)
- USB2.0 (P9)
- USB2.0 (P7) — BlueTooth PG 38
- USB2.0 (P0,P1)(EXT SIDE)
- USB2.0 (P2,P3)(EXT BACK) — External USBX4 PG 28
- USB2.0 (P8) (GX2) — External USB PG 28
- 33MHz PCI
- USB2.0 (P5)
- SPI
- LPC

AUDIO/AMP
PG 33,34

MDC
PG 27

S/PDIF

Digital MIC | **Camera**
PG 34

Audio Jacks | **SNIFFER**
PG 34

SIO
MEC5025
128KB Flash
TMKBC
128 Pins VTQFP
PG 29

BC

SIO
ECE5021
128 Pins VTQFP
PG 30

1394
8-in-1 Card Reader
R5C833
PG 21,22,23

BCM 4401 (B0)
PG 36

USER INTERFACE
PG 38

RJ45/Magnetics
PG 37

SPI — **FLASH** PG 31

BC — PS/2 — **Touchpad/ Keyboard** PG32

CIR
PG 32

QUANTA COMPUTER

Title	Schematic Block Diagram1	
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14-17	SB600
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19	LCD Conn. & CK-SSCD
20	CRT&TV CONN
21-23	8-IN-1 CARD READER
24	SATA (HDD&CD_ROM)
25	MINI-PCI
26	WWAN
27	Express Card & Smart Card
28	USB
29	SIO (MEC5025)
30	SIO (ECE5011)
31	FLASH,RTC&KC
32	TP&CIR
33	Audio CODEC(STAC9205)&AMP
34	AUDIO CONN Digital MIC/Camera
35	FAN & Thermal
36	LAN (BCM4401)
37	LAN JACK
38	SWITCH&LED
39	System Reset Circuit
40	Charger
41	DCIN,BATT CONNECTOR
42	+1.2V_ALW_SUS,+NB_VCORE
43	+1.8V_SUS,+0.9V_DDR_VTT,+1.5V_RUN
44	VHCORE(MAX8774)
45	+3.3V_ALW,+5V_ALW
46	RUN Power Switch
48	EMI CAP & SCREW HOLE
49	SMBUS BLOCK
50	POWER BLOCK
51	Chipset Power Block

PCI Device	IDSEL	REQ# / GNT# - PIRQ (S/Y)
Cardbus (OZ601)	AD17	N/A
Docking	AD24	N/A
MediaCard & 1394 (R5C832)	AD17	REQ1# / GNT#1 - PIRQC# (Media Card), PIRQD# (1394) & SERIRQ.
LOM (4401)	AD16	REQ0# / GNT#0 - PIRQB#.

PCI-E	Destination (S/Y)
Lane0	MINI CARD-3 WWAN
Lane1	MINI CARD-1 WLAN
Lane2	MINI CARD-2 WPAN
Lane3	EXPRESS CARD

Power States

Power Rail	Control Signal	S0/M0	S3/M1	S3/M1	S4/M1	S3/ M-off	S4/ M-off	S5/ M-off
+15V_ALW								
+5V_ALW								
+3.3V_ALW								
+1.2V_ALW_SUS								
+5V_SUS								
+3.3V_SUS								
+1.8V_SUS								
+0.9V_DDR_VTT								
+5V_RUN								
+1.2V_RUN								
+1.8V_RUN								
+3.3V_RUN								
+2.5V_RUN								
+VCC_VCRE								
+NB_VCORE								
+LCDVCC								
+3.3V_WLAN								
+3.3V_LAN								

IC Chips	USB Port#	Destination (S/Y)
SB600	0	Right side Pair Top as viewed in the front
	1	Right side Pair Bot. as viewed in the front
	2	Rear Side Top
	3	Rear Side Bottom
	4	Left side Pair Tot as viewed in the front
	5	Camera
	6	Express Card
	7	3rd Mini Card USB(WPAN)
	8	Left side Pair Bot. as viewed in the front
	9	WWAN

PM Table

State \ Power Plan	+15V_ALW +5V_ALW +3.3V_ALW +1.2V_ALW_SUS	+5V_SUS +3.3V_SUS +1.8V_SUS +0.9V_DDR_VTT	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.5V_RUN +1.2V_RUN +VCC_CORE +NB_CORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4 on battery	OFF	OFF	OFF

QUANTA COMPUTER

Title	Index, DNI, Power & Ground	
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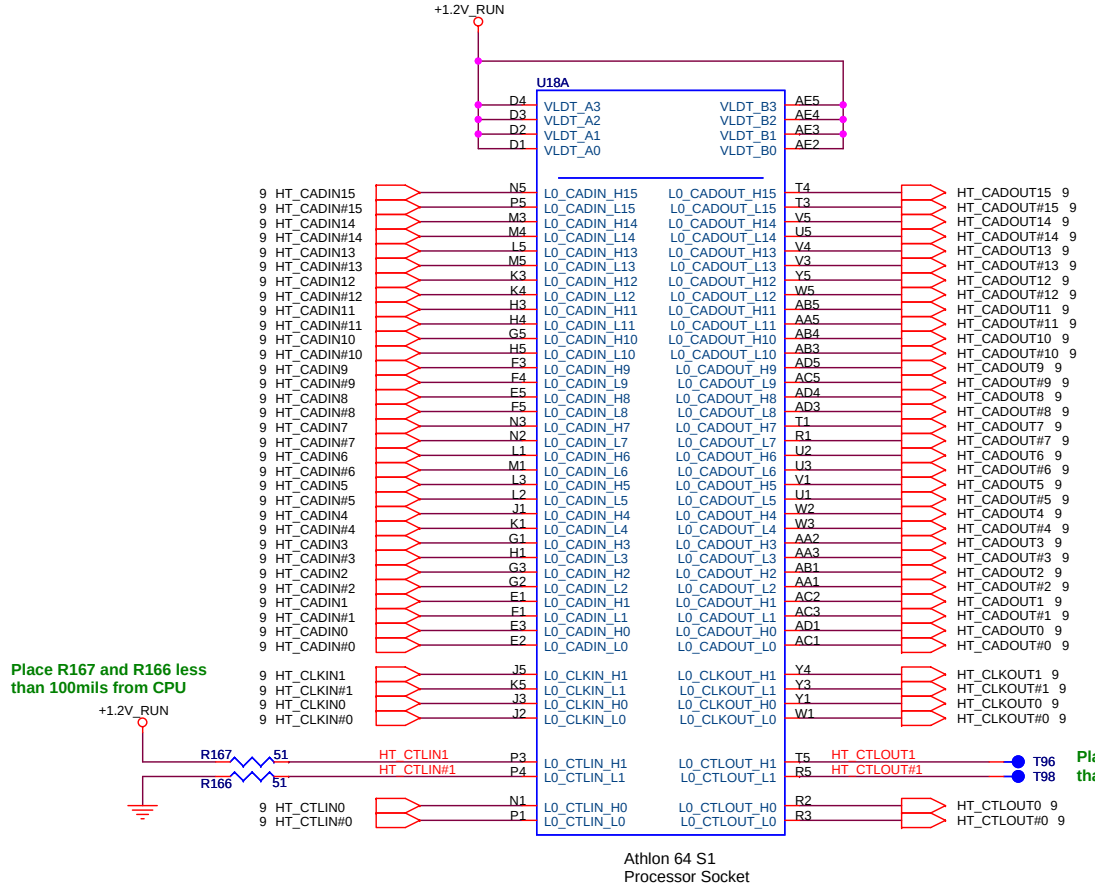
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



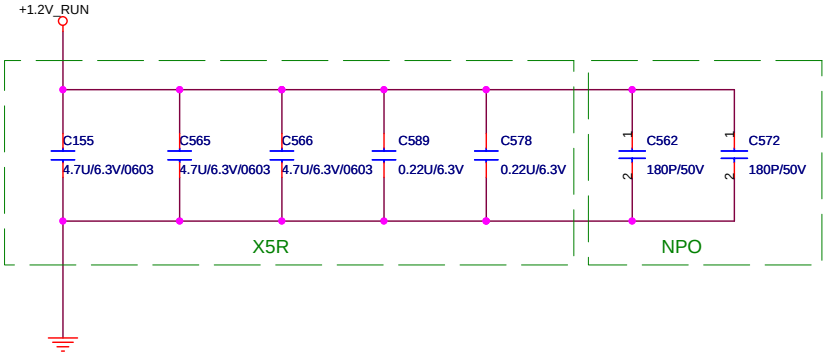
Athlon 64 S1
Processor Socket

Place R167 and R166 less than 100mils from CPU

Place T96 and T98 less than 100mils from CPU

LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



QUANTA COMPUTER

Title	ATHLON64 HT I/F	
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Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

Place Capacitors for +0.9V_CPU_M_VREF_SUS < 1" from the RS690T. +0.9V_CPU_M_VREF_SUS trace length < 6", trace width > 15mils and 20mils spacing from any adjacent signals in X, Y, Z directions.

CPU_VTT_SUS_SENSE should be routed as 10mils and 10mils spacing from any adjacent signals in X, Y, Z directions.

PLACE THEM CLOSE TO CPU WITHIN 1"

+1.8V_SUS
C700 0.1U/10V
R579 1K/F
R577 *0_0603_NC
+V_DDR_VREF
+0.9V_CPU_M_VREF_SUS
C694 0.1U/10V
C683 1N/50V
R578 1K/F
43 CPU_VTT_SUS_SENSE
C647 *470P/50V_NC
R231 39.2/F
R235 39.2/F
M_ZN
M_ZP
+0.9V_DDR_VTT

U18B

W17 MEMVREF
Y10 VTT_SENSE
AE10 MEMZN
AF10 MEMZP

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10

7,8 DDR_CS3_DIMMA# V19 MA0_CS_L3
7,8 DDR_CS2_DIMMA# J22 MA0_CS_L2
7,8 DDR_CS1_DIMMA# V22 MA0_CS_L1
7,8 DDR_CS0_DIMMA# T19 MA0_CS_L0

MA0_CLK_H2 Y16 M_CLK_DDR1 7
MA0_CLK_L2 AA16 M_CLK_DDR#1 7
MA0_CLK_H1 E16 M_CLK_DDR0 7
MA0_CLK_L1 F16 M_CLK_DDR#0 7

7,8 DDR_CS3_DIMMB# Y26 MB0_CS_L3
7,8 DDR_CS2_DIMMB# J24 MB0_CS_L2
7,8 DDR_CS1_DIMMB# W24 MB0_CS_L1
7,8 DDR_CS0_DIMMB# U23 MB0_CS_L0

MB0_CLK_H2 AF18 M_CLK_DDR3 7
MB0_CLK_L2 AF17 M_CLK_DDR#3 7
MB0_CLK_H1 A17 M_CLK_DDR2 7
MB0_CLK_L1 A18 M_CLK_DDR#2 7

7,8 DDR_CKE3_DIMMB H26 MB_CKE1
7,8 DDR_CKE2_DIMMB J23 MB_CKE0
7,8 DDR_CKE1_DIMMA J20 MA_CKE1
7,8 DDR_CKE0_DIMMA J21 MA_CKE0

MB0_ODT1 W23 M_ODT3 7,8
MB0_ODT0 W26 M_ODT2 7,8
MA0_ODT1 V20 M_ODT1 7,8
MA0_ODT0 U19 M_ODT0 7,8

7,8 DDR_A_MA[0..15]

DDR_A_MA15 K19 MA_ADD15
DDR_A_MA14 K20 MA_ADD14
DDR_A_MA13 V24 MA_ADD13
DDR_A_MA12 K24 MA_ADD12
DDR_A_MA11 L20 MA_ADD11
DDR_A_MA10 R19 MA_ADD10
DDR_A_MA9 L19 MA_ADD9
DDR_A_MA8 L22 MA_ADD8
DDR_A_MA7 L21 MA_ADD7
DDR_A_MA6 M19 MA_ADD6
DDR_A_MA5 M20 MA_ADD5
DDR_A_MA4 M24 MA_ADD4
DDR_A_MA3 M22 MA_ADD3
DDR_A_MA2 N22 MA_ADD2
DDR_A_MA1 N21 MA_ADD1
DDR_A_MA0 R21 MA_ADD0

MB_ADD15 J25 DDR_B_MA15
MB_ADD14 J26 DDR_B_MA14
MB_ADD13 W25 DDR_B_MA13
MB_ADD12 L23 DDR_B_MA12
MB_ADD11 L25 DDR_B_MA11
MB_ADD10 U25 DDR_B_MA10
MB_ADD9 L24 DDR_B_MA9
MB_ADD8 M26 DDR_B_MA8
MB_ADD7 L26 DDR_B_MA7
MB_ADD6 N23 DDR_B_MA6
MB_ADD5 N24 DDR_B_MA5
MB_ADD4 N25 DDR_B_MA4
MB_ADD3 N26 DDR_B_MA3
MB_ADD2 P24 DDR_B_MA2
MB_ADD1 P26 DDR_B_MA1
MB_ADD0 T24 DDR_B_MA0

DDR_B_MA[0..15] 7,8

7,8 DDR_A_BS2 K22 MA_BANK2
7,8 DDR_A_BS1 R20 MA_BANK1
7,8 DDR_A_BS0 T22 MA_BANK0

MB_BANK2 K26 DDR_B_BS2 7,8
MB_BANK1 T26 DDR_B_BS1 7,8
MB_BANK0 U26 DDR_B_BS0 7,8

7,8 DDR_A_RAS# T20 MA_RAS_L
7,8 DDR_A_CAS# U20 MA_CAS_L
7,8 DDR_A_WE# U21 MA_WE_L

MB_RAS_L U24 DDR_B_RAS# 7,8
MB_CAS_L V26 DDR_B_CAS# 7,8
MB_WE_L U22 DDR_B_WE# 7,8

DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket

U18C

7 DDR_B_D[0..63]

DDR_B_D63 AD11 MB_DATA63
DDR_B_D62 AE11 MB_DATA62
DDR_B_D61 AE14 MB_DATA61
DDR_B_D60 AE14 MB_DATA60
DDR_B_D59 Y11 MB_DATA59
DDR_B_D58 AB11 MB_DATA58
DDR_B_D57 AC12 MB_DATA57
DDR_B_D56 AE13 MB_DATA56
DDR_B_D55 AE15 MB_DATA55
DDR_B_D54 AF16 MB_DATA54
DDR_B_D53 AC18 MB_DATA53
DDR_B_D52 AF19 MB_DATA52
DDR_B_D51 AD14 MB_DATA51
DDR_B_D50 AC14 MB_DATA50
DDR_B_D49 AE18 MB_DATA49
DDR_B_D48 AD18 MB_DATA48
DDR_B_D47 AD20 MB_DATA47
DDR_B_D46 AC20 MB_DATA46
DDR_B_D45 AF23 MB_DATA45
DDR_B_D44 AF24 MB_DATA44
DDR_B_D43 AF20 MB_DATA43
DDR_B_D42 AE20 MB_DATA42
DDR_B_D41 AD22 MB_DATA41
DDR_B_D40 AC22 MB_DATA40
DDR_B_D39 AE25 MB_DATA39
DDR_B_D38 AD26 MB_DATA38
DDR_B_D37 AA25 MB_DATA37
DDR_B_D36 AA26 MB_DATA36
DDR_B_D35 AE24 MB_DATA35
DDR_B_D34 AD24 MB_DATA34
DDR_B_D33 AA23 MB_DATA33
DDR_B_D32 AA24 MB_DATA32
DDR_B_D31 G24 MB_DATA31
DDR_B_D30 G23 MB_DATA30
DDR_B_D29 D26 MB_DATA29
DDR_B_D28 C26 MB_DATA28
DDR_B_D27 G26 MB_DATA27
DDR_B_D26 G25 MB_DATA26
DDR_B_D25 E24 MB_DATA25
DDR_B_D24 E23 MB_DATA24
DDR_B_D23 C24 MB_DATA23
DDR_B_D22 B24 MB_DATA22
DDR_B_D21 C20 MB_DATA21
DDR_B_D20 B20 MB_DATA20
DDR_B_D19 C25 MB_DATA19
DDR_B_D18 D24 MB_DATA18
DDR_B_D17 A21 MB_DATA17
DDR_B_D16 D20 MB_DATA16
DDR_B_D15 D18 MB_DATA15
DDR_B_D14 C18 MB_DATA14
DDR_B_D13 D14 MB_DATA13
DDR_B_D12 C14 MB_DATA12
DDR_B_D11 A20 MB_DATA11
DDR_B_D10 A19 MB_DATA10
DDR_B_D9 A16 MB_DATA9
DDR_B_D8 A15 MB_DATA8
DDR_B_D7 A13 MB_DATA7
DDR_B_D6 D12 MB_DATA6
DDR_B_D5 E11 MB_DATA5
DDR_B_D4 G11 MB_DATA4
DDR_B_D3 B14 MB_DATA3
DDR_B_D2 A14 MB_DATA2
DDR_B_D1 A11 MB_DATA1
DDR_B_D0 C11 MB_DATA0

AA12 MA_DATA63 DDR_A_D63
AB12 MA_DATA62 DDR_A_D62
AA14 MA_DATA61 DDR_A_D61
AB14 MA_DATA60 DDR_A_D60
W11 MA_DATA59 DDR_A_D59
Y12 MA_DATA58 DDR_A_D58
AD13 MA_DATA57 DDR_A_D57
AB13 MA_DATA56 DDR_A_D56
AD15 MA_DATA55 DDR_A_D55
AB15 MA_DATA54 DDR_A_D54
AB17 MA_DATA53 DDR_A_D53
Y17 MA_DATA52 DDR_A_D52
Y14 MA_DATA51 DDR_A_D51
W14 MA_DATA50 DDR_A_D50
W16 MA_DATA49 DDR_A_D49
AD17 MA_DATA48 DDR_A_D48
Y18 MA_DATA47 DDR_A_D47
AD19 MA_DATA46 DDR_A_D46
AD21 MA_DATA45 DDR_A_D45
AB21 MA_DATA44 DDR_A_D44
AB18 MA_DATA43 DDR_A_D43
AA18 MA_DATA42 DDR_A_D42
AA20 MA_DATA41 DDR_A_D41
Y20 MA_DATA40 DDR_A_D40
AA22 MA_DATA39 DDR_A_D39
Y22 MA_DATA38 DDR_A_D38
W21 MA_DATA37 DDR_A_D37
W22 MA_DATA36 DDR_A_D36
AA21 MA_DATA35 DDR_A_D35
AB22 MA_DATA34 DDR_A_D34
AB24 MA_DATA33 DDR_A_D33
Y24 MA_DATA32 DDR_A_D32
H22 MA_DATA31 DDR_A_D31
H20 MA_DATA30 DDR_A_D30
F22 MA_DATA29 DDR_A_D29
E21 MA_DATA28 DDR_A_D28
J19 MA_DATA27 DDR_A_D27
H24 MA_DATA26 DDR_A_D26
F22 MA_DATA25 DDR_A_D25
F20 MA_DATA24 DDR_A_D24
C23 MA_DATA23 DDR_A_D23
B22 MA_DATA22 DDR_A_D22
F18 MA_DATA21 DDR_A_D21
E18 MA_DATA20 DDR_A_D20
E20 MA_DATA19 DDR_A_D19
D22 MA_DATA18 DDR_A_D18
C19 MA_DATA17 DDR_A_D17
G18 MA_DATA16 DDR_A_D16
G17 MA_DATA15 DDR_A_D15
C17 MA_DATA14 DDR_A_D14
F14 MA_DATA13 DDR_A_D13
E14 MA_DATA12 DDR_A_D12
H17 MA_DATA11 DDR_A_D11
E17 MA_DATA10 DDR_A_D10
E15 MA_DATA9 DDR_A_D9
H15 MA_DATA8 DDR_A_D8
E13 MA_DATA7 DDR_A_D7
C13 MA_DATA6 DDR_A_D6
H12 MA_DATA5 DDR_A_D5
H11 MA_DATA4 DDR_A_D4
G14 MA_DATA3 DDR_A_D3
H14 MA_DATA2 DDR_A_D2
E12 MA_DATA1 DDR_A_D1
G12 MA_DATA0 DDR_A_D0

DDR_A_D[0..63] 7

DDR_B_DM7 AD12 MB_DM7
DDR_B_DM6 AC16 MB_DM6
DDR_B_DM5 AF22 MB_DM5
DDR_B_DM4 AB26 MB_DM4
DDR_B_DM3 E25 MB_DM3
DDR_B_DM2 A22 MB_DM2
DDR_B_DM1 B16 MB_DM1
DDR_B_DM0 A12 MB_DM0

Y13 MA_DM7 DDR_A_DM7
AB16 MA_DM6 DDR_A_DM6
Y19 MA_DM5 DDR_A_DM5
AC24 MA_DM4 DDR_A_DM4
F24 MA_DM3 DDR_A_DM3
E19 MA_DM2 DDR_A_DM2
C15 MA_DM1 DDR_A_DM1
E12 MA_DM0 DDR_A_DM0

7 DDR_B_DM[0..7]
DDR_A_DM[0..7] 7

DDR_B_DQS7 AE12 MB_DQS_H7
DDR_B_DQS#7 AE12 MB_DQS_L7
DDR_B_DQS6 AE16 MB_DQS_H6
DDR_B_DQS#6 AD16 MB_DQS_L6
DDR_B_DQS5 AF21 MB_DQS_H5
DDR_B_DQS#5 AF22 MB_DQS_L5
DDR_B_DQS4 AC25 MB_DQS_H4
DDR_B_DQS#4 AC26 MB_DQS_L4
DDR_B_DQS3 F26 MB_DQS_H3
DDR_B_DQS#3 F26 MB_DQS_L3
DDR_B_DQS2 A24 MB_DQS_H2
DDR_B_DQS#2 A23 MB_DQS_L2
DDR_B_DQS1 D16 MB_DQS_H1
DDR_B_DQS#1 C16 MB_DQS_L1
DDR_B_DQS0 C12 MB_DQS_H0
DDR_B_DQS#0 B12 MB_DQS_L0

W12 MA_DQS_H7 DDR_A_DQS7
W13 MA_DQS_L7 DDR_A_DQS#7
Y15 MA_DQS_H6 DDR_A_DQS6
W15 MA_DQS_L6 DDR_A_DQS#6
AB19 MA_DQS_H5 DDR_A_DQS5
AB20 MA_DQS_L5 DDR_A_DQS#5
AD23 MA_DQS_H4 DDR_A_DQS4
AC23 MA_DQS_L4 DDR_A_DQS#4
G22 MA_DQS_H3 DDR_A_DQS3
G21 MA_DQS_L3 DDR_A_DQS#3
C22 MA_DQS_H2 DDR_A_DQS2
C21 MA_DQS_L2 DDR_A_DQS#2
G16 MA_DQS_H1 DDR_A_DQS1
G15 MA_DQS_L1 DDR_A_DQS#1
G13 MA_DQS_H0 DDR_A_DQS0
H13 MA_DQS_L0 DDR_A_DQS#0

DDR: DATA
Athlon 64 S1
Processor Socket

To SODIMM socket B (Far)
To SODIMM socket A (near)

7 DDR_B_DQS[0..7]
DDR_B_DQS0
DDR_B_DQS1
DDR_B_DQS2
DDR_B_DQS3
DDR_B_DQS4
DDR_B_DQS5
DDR_B_DQS6
DDR_B_DQS7

7 DDR_B_DQS#[0..7]
DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
DDR_B_DQS#6
DDR_B_DQS#7

7 DDR_A_DQS[0..7]
DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7

7 DDR_A_DQS#[0..7]
DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7

QUANTA COMPUTER

Title	ATHLON64 DDRII MEMORY	
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ATHLON Control and Debug

The AMD SI feature has errata, and will not be mplemented.

R195 *300_NC, R194 *300_NC, R193 300 — +1.8V_SUS — CPU_SID_R, CPU_SIC_R

for CPU rev.F.
If for rev.G , populate R195, R194 and depopulate R193.

18 CPU_CLK — C185 3900p_25V — CPU_CLKIN_SC_P
18 CPU_CLK# — C183 3900p_25V — CPU_CLKIN_SC_N
R232 169/F_0603

1.Keep trace to resistor less then 600mils from cpu and trace to ac caps less than 1250mils
2.CPUCLK and CPUCLK# mismatch <35mils.

+3.3V_SUS, +1.8V_SUS — SB this pin is 3.3V,need it level-shift.

R523 *10K_NC, R520 10K, R521 4.7K
Q42 MMST3904-7-F, *MMST3904-7-F_NC, Q61
CPU_PROCHOT# — EC_CPU_PROCHOT# 29

SB600 ONLY

14 CPU_PWRGD — R213 680 — CPU_PWRGD
11,14 LDT_STOP# — R270 680, C827 *0.1U/10V_NC — LDT_STOP#
14 LDT_RST# — R218 680 — LDT_RST#

Note:Place R218 on the Top of the board that is acessible, and that shorting across this resistor will toggle the Hyper Transport reset signal.

R685 *0_NC
R699 0, R700 *0_NC
D39 RB751V40T1G
U38 NL17SZ17DFT2G
R686 20K/F
C814 47P/50V
LDT_STOP# R — R708 *680_NC

Checkferrite bead with an approximate impedance of 35 , a maximum DC resistance of 40 m , and a current rating of at least 500 mA.

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG. This trace should be kept at least 20 mil from all other signal.

+2.5V_RUN — BLM18PG330SN1D_0603 L58 — +2.5V_CPU_VDDA_RUN
C623 100U/6.3V/3528, C608 4.7U/6.3V/0603, C634 0.22U/6.3V, C635 3300P_50V

Place R168 and R165 < 1.5". Route CPU_HTREF1/0 with 5mils trace width and 10mils spacing from other signals in X, Y, Z directions

+1.2V_RUN — R168 44.2/F, R165 44.2/F — CPU_HTREF1, CPU_HTREF0

To Power: 44 CPU_VDD_RUN_FB_H, 44 CPU_VDD_RUN_FB_L
43 CPU_VDDIO_SUS_FB_H, 43 CPU_VDDIO_SUS_FB_L — CPU_VDDIO_SUS_FB_H, CPU_VDDIO_SUS_FB_L
T110, T115, T120, T124
C632 470/P50V/X7R

Place C625< 100mils from CPU.
35 H_THERMDC, 35 H_THERMDA — C625 470P/50V/NPO

U18D

VDDA2, VDDA1
PRESET_L, PWROK, LDTSTOP_L
SIC, SID
HT_REF1, HT_REF0
VDD_FB_H, VDD_FB_L
VDDIO_FB_H, VDDIO_FB_L
CLKIN_H, CLKIN_L
DBRDY
TMS, TCK, TRST_L, TDI
TEST25_H, TEST25_L, TEST19, TEST18, TEST13, TEST9, TEST17, TEST16, TEST15, TEST14, TEST12, TEST7, TEST6, TEST5, TEST4, TEST3, TEST2
RSVD0, RSVD1, RSVD2, RSVD3, RSVD4, RSVD5, RSVD6, RSVD7
MISC

LDT_RST# — CPU_PWRGD — LDT_STOP#
CPU_SIC_R, CPU_SID_R
CPU_CLKIN_SC_P, CPU_CLKIN_SC_N
CPU_DBRDY, CPU_TMS, CPU_TCK, CPU_TRST#, CPU_TDI
CPU_TEST25_H_BYPASSCLK_H, CPU_TEST25_L_BYPASSCLK_L, CPU_TEST19_PLLTEST0, CPU_TEST18_PLLTEST1
CPU_TEST17_BP3, CPU_TEST16_BP2, CPU_TEST15_BP1, CPU_TEST14_BP0, CPU_TEST12_SCANSHIFTENB
CPU_TEST07_ANALOG_T, CPU_TEST6_DIECRACKMON, H_THERMDC, H_THERMDA, CPU_TEST3_GATE0, CPU_TEST2_DRAIN0
CPU_RSVD_MA0_CLK3_P, CPU_RSVD_MA0_CLK3_N, CPU_RSVD_MA0_CLK0_P, CPU_RSVD_MA0_CLK0_N
CPU_RSVD_MB0_CLK3_P, CPU_RSVD_MB0_CLK3_N, CPU_RSVD_MB0_CLK0_P, CPU_RSVD_MB0_CLK0_N

+1.8V_SUS — R527 300, R210 300
THERMTRIP_L — H_THERMTRIP# — H_THERMTRIP# 35
PROCHOT_L — CPU_PROCHOT# — H_THERMTRIP# 35
VID5, VID4, VID3, VID2, VID1, VID0 — 44
CPU_PRESENT_L — CPU_PRESENT#
PSI_L — CPU_PSI# 44 — T31

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports “skipmode, or diode emulation mode”. PSI_L is asserted by the processor during the C3 and S1 states.

DBREQ_L — CPU_DBREQ#
TDO — CPU_TDO

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

TEST29_H — CPU_TEST29_H_FBCLKOUT_P — R546 80.6/F
TEST29_L — CPU_TEST29_L_FBCLKOUT_N

TEST24 — CPU_TEST24_SCANCLK1 — T39
TEST23 — CPU_TEST23_TSTUPD — T126
TEST22 — CPU_TEST22_SCANSHIFTEN — T47
TEST21 — CPU_TEST21_SCANEN — T127
TEST20 — CPU_TEST20_SCANCLK2 — T37
TEST28_H — CPU_TEST28_H_PLLCHRZ_P — T99
TEST28_L — CPU_TEST28_L_PLLCHRZ_N — T121
TEST27 — CPU_TEST27_SINGLECHAIN — T42
TEST26 — CPU_TEST26_BURNIN# — T35
TEST10 — CPU_TEST10_ANALOGOUT — T119
TEST8 — CPU_TEST08_DIG_T — T34

RSVD8 — CPU_MA_RESET# — T131
RSVD9 — CPU_MB_RESET# — T136
RSVD10 — CPU_RSVD_VIDSTRB1 — T30
RSVD11 — CPU_RSVD_VIDSTRB0 — T32
RSVD12 — CPU_RSVD_VDDNB_FB_P — T100
RSVD13 — CPU_RSVD_VDDNB_FB_N — T101
RSVD14 — CPU_RSVD_CORE_TYPE — T102
RSVD15 — CPU_RSVD_15 — T148
RSVD16 — CPU_RSVD_16 — T145
RSVD17 — CPU_RSVD_17 — T149
RSVD18 — CPU_RSVD_18 — T113
RSVD19 — CPU_RSVD_19 — T130
RSVD20 — CPU_RSVD_20 — T143

AMD NPT S1 SOCKET
Processor Socket

+1.8V_SUS

CPU_TEST27_SINGLECHAIN — R216 *300_NC
CPU_TEST26_BURNIN# — R206 300
CPU_PRESENT# — R516 1K/F
CPU_TEST25_H_BYPASSCLK_H — R566 510/F

CPU_TEST21_SCANEN — R541 300
CPU_TEST20_SCANCLK2 — R209 *300_NC
CPU_TEST24_SCANCLK1 — R212 *300_NC
CPU_TEST22_SCANSHIFTEN — R221 *300_NC
CPU_TEST12_SCANSHIFTENB — R536 *300_NC
CPU_TEST15_BP1 — R530 *300_NC
CPU_TEST14_BP0 — R540 *300_NC

CPU_TEST25_L_BYPASSCLK_L — R535 510/F
CPU_TEST19_PLLTEST0 — R542 300
CPU_TEST18_PLLTEST1 — R575 300

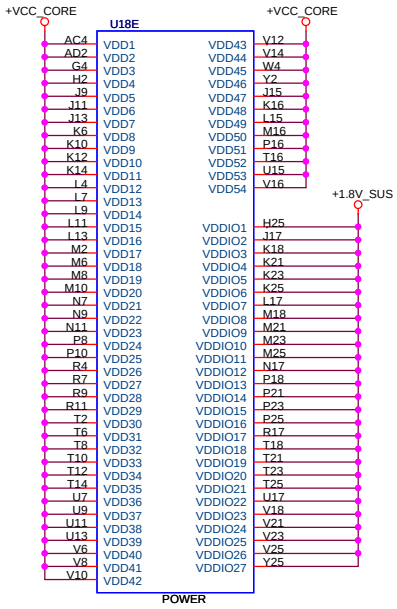
HDT CONNECTOR

+1.8V_SUS
R549, R223, R547, R544, R568 *220_NC
JHDT1 *HDT conn_NC
CPU_DBREQ#, CPU_DBRDY, CPU_TCK, CPU_TMS, CPU_TDI, CPU_TRST#, CPU_TDO
GND, Resreved, DBREQ_L, DBRDY, TCK, TMS, TDI, TRST_L, TDO, VDDIO, RESET_L

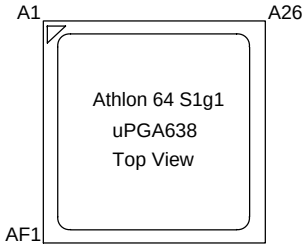
+3.3V_RUN — R589 *4.7K_NC
+1.8V_RUN — R587 *4.7K_NC
Q48 *MMST3904_NC
CPU_RESET# — LDT_RST#

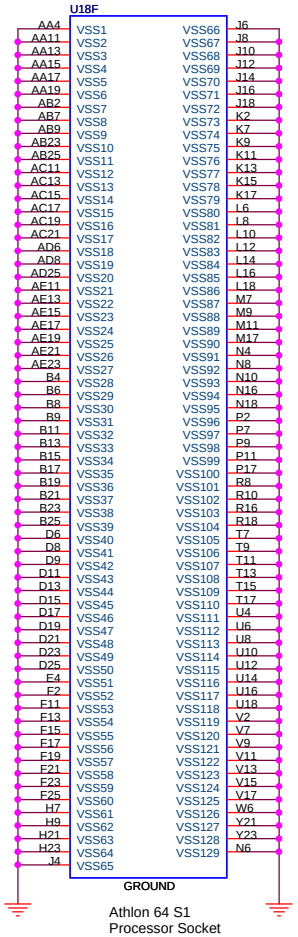
QUANTA COMPUTER

Title	ATHLON64 CTRL & DEBUG	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 5 of 61	



Athlon 64 S1
Processor Socket

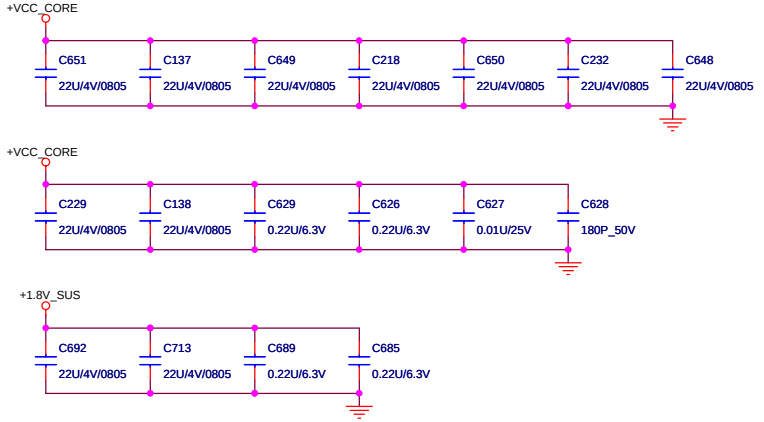




Athlon 64 S1
Processor Socket

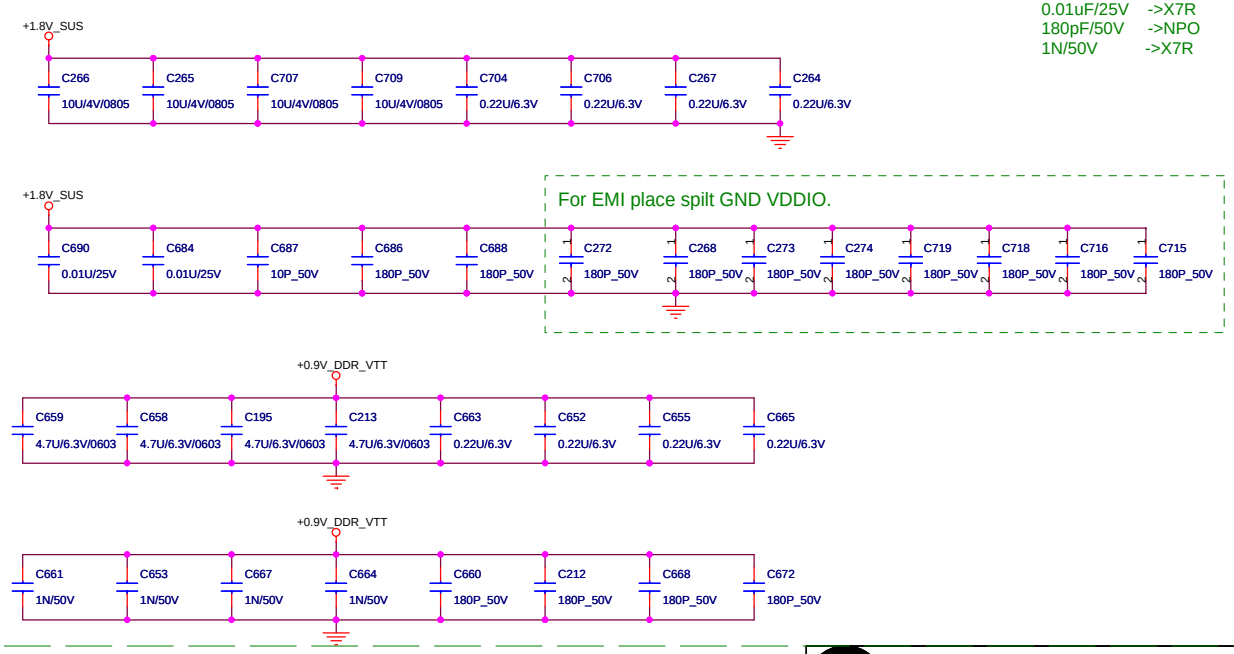
BOTTOMSIDE DECOUPLING

22uF/4V/0805->X6S
0.22uF/6.3V ->X5R
0.01uF/25V ->X7R
180pF/50V ->NPO



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

10U/4V/0805->X6S
4.7U/6.3V/0603->X5R
0.22uF/6.3V ->X5R
0.01uF/25V ->X7R
180pF/50V ->NPO
1N/50V ->X7R



PROCESSOR POWER AND GROUND

QUANTA COMPUTER

Title	ATHLON64 PWR & GND	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 6 of 61	

A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

JDIM1

PC5300 DDR2 SDRAM SO-DIMM (200P)

FOX_AS0A426-N2RN-7F

BOT

JDIM2

PC5300 DDR2 SDRAM SO-DIMM (200P)

Tyco-292406-4

CLOCK 0,1
CKE 0,1

CLOCK 2,3
CKE 2,3

SMbus address A0

SMbus address A4

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

Title	DDRII SODIMMX2
Size	Document Number FX5
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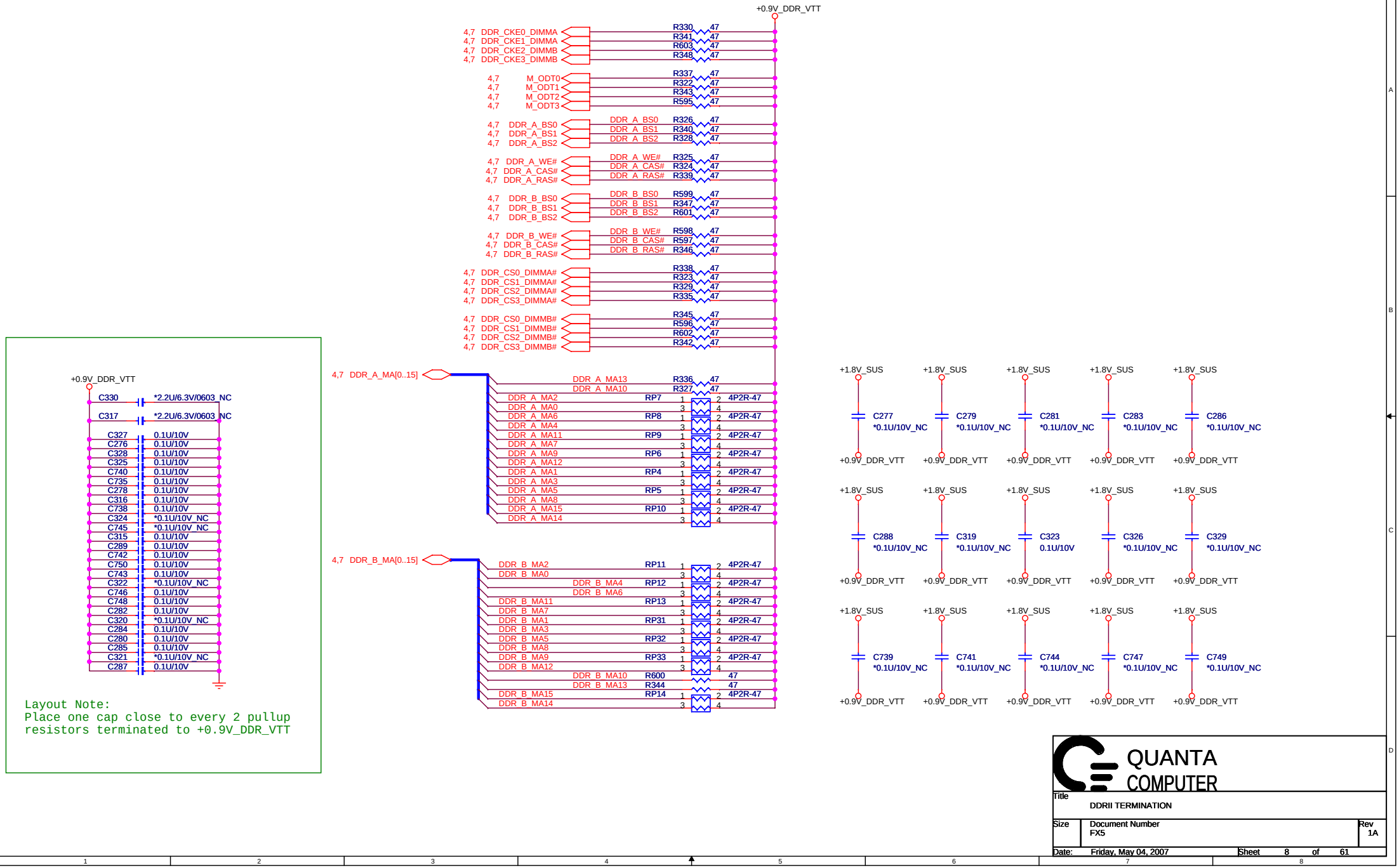
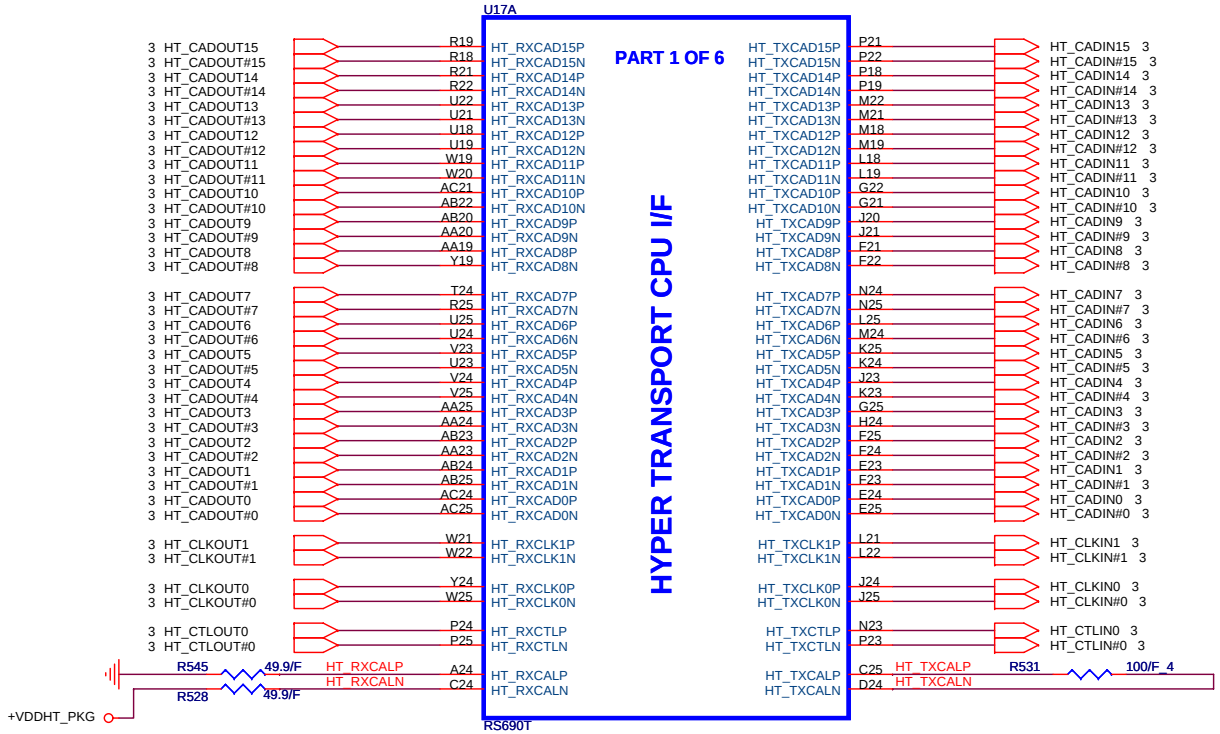
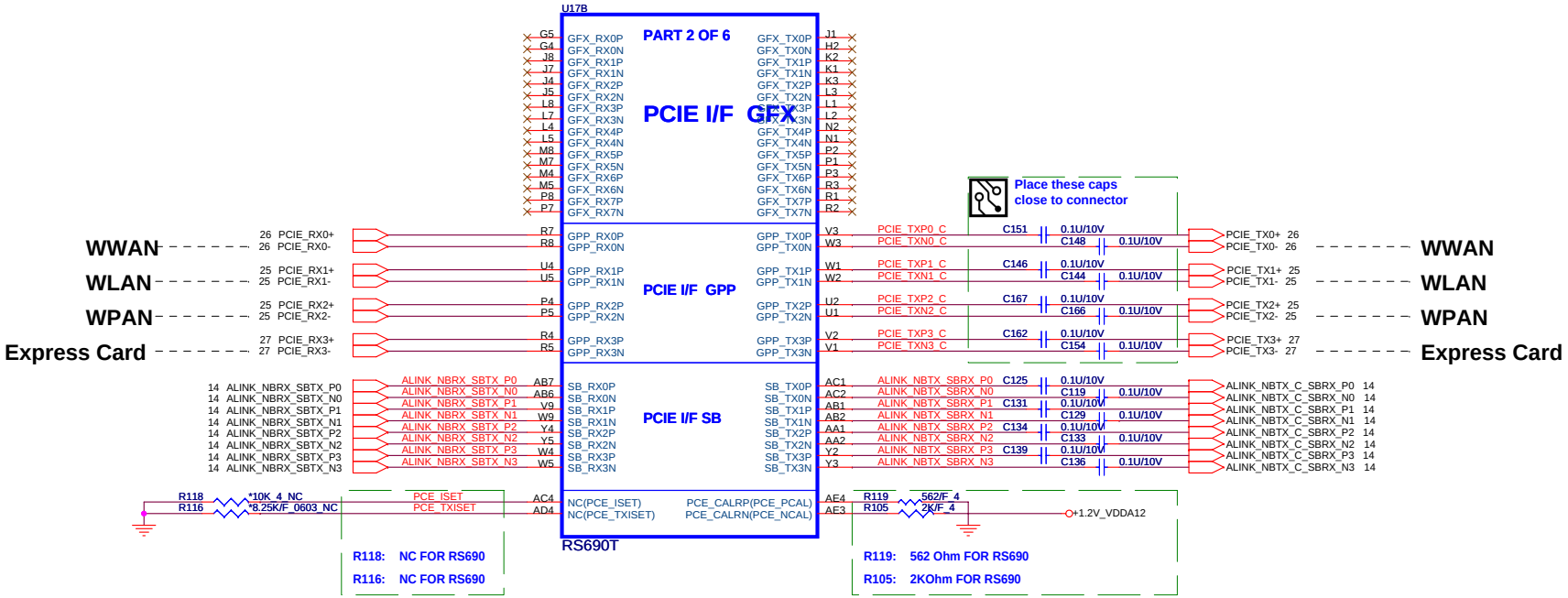
QUANTA COMPUTER


+0.9V_DDR_VTT
4,7 DDR_CKE0_DIMMA R330 47
4,7 DDR_CKE1_DIMMA R341 47
4,7 DDR_CKE2_DIMMB R603 47
4,7 DDR_CKE3_DIMMB R348 47
4,7 M_ODT0 R337 47
4,7 M_ODT1 R322 47
4,7 M_ODT2 R343 47
4,7 M_ODT3 R595 47
4,7 DDR_A_BS0 DDR_A_BS0 R326 47
4,7 DDR_A_BS1 DDR_A_BS1 R340 47
4,7 DDR_A_BS2 DDR_A_BS2 R328 47
4,7 DDR_A_WE# DDR_A_WE# R325 47
4,7 DDR_A_CAS# DDR_A_CAS# R324 47
4,7 DDR_A_RAS# DDR_A_RAS# R339 47
4,7 DDR_B_BS0 DDR_B_BS0 R599 47
4,7 DDR_B_BS1 DDR_B_BS1 R347 47
4,7 DDR_B_BS2 DDR_B_BS2 R601 47
4,7 DDR_B_WE# DDR_B_WE# R598 47
4,7 DDR_B_CAS# DDR_B_CAS# R597 47
4,7 DDR_B_RAS# DDR_B_RAS# R346 47
4,7 DDR_CS0_DIMMA# R338 47
4,7 DDR_CS1_DIMMA# R323 47
4,7 DDR_CS2_DIMMA# R329 47
4,7 DDR_CS3_DIMMA# R335 47
4,7 DDR_CS0_DIMMB# R345 47
4,7 DDR_CS1_DIMMB# R596 47
4,7 DDR_CS2_DIMMB# R602 47
4,7 DDR_CS3_DIMMB# R342 47
4,7 DDR_A_MA[0..15]
DDR_A_MA13 R336 47
DDR_A_MA10 R327 47
DDR_A_MA2 RP7 4P2R-47
DDR_A_MA0
DDR_A_MA6 RP8 4P2R-47
DDR_A_MA4
DDR_A_MA11 RP9 4P2R-47
DDR_A_MA7
DDR_A_MA9 RP6 4P2R-47
DDR_A_MA12
DDR_A_MA1 RP4 4P2R-47
DDR_A_MA3
DDR_A_MA5 RP5 4P2R-47
DDR_A_MA8
DDR_A_MA15 RP10 4P2R-47
DDR_A_MA14
4,7 DDR_B_MA[0..15]
DDR_B_MA2 RP11 4P2R-47
DDR_B_MA0
DDR_B_MA4 RP12 4P2R-47
DDR_B_MA6
DDR_B_MA11 RP13 4P2R-47
DDR_B_MA7
DDR_B_MA1 RP31 4P2R-47
DDR_B_MA3
DDR_B_MA5 RP32 4P2R-47
DDR_B_MA8
DDR_B_MA9 RP33 4P2R-47
DDR_B_MA12
DDR_B_MA10 R600 47
DDR_B_MA13 R344 47
DDR_B_MA15 RP14 4P2R-47
DDR_B_MA14
+0.9V_DDR_VTT
C330 *2.2U/6.3V/0603_NC
C317 *2.2U/6.3V/0603_NC
C327 0.1U/10V
C276 0.1U/10V
C328 0.1U/10V
C325 0.1U/10V
C740 0.1U/10V
C735 0.1U/10V
C278 0.1U/10V
C316 0.1U/10V
C738 0.1U/10V
C324 *0.1U/10V_NC
C745 *0.1U/10V_NC
C315 0.1U/10V
C289 0.1U/10V
C742 0.1U/10V
C750 0.1U/10V
C743 0.1U/10V
C322 *0.1U/10V_NC
C746 0.1U/10V
C748 0.1U/10V
C282 0.1U/10V
C320 *0.1U/10V_NC
C284 0.1U/10V
C280 0.1U/10V
C285 0.1U/10V
C321 *0.1U/10V_NC
C287 0.1U/10V
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
+1.8V_SUS
C277 *0.1U/10V_NC
C279 *0.1U/10V_NC
C281 *0.1U/10V_NC
C283 *0.1U/10V_NC
C286 *0.1U/10V_NC
C288 *0.1U/10V_NC
C319 *0.1U/10V_NC
C323 0.1U/10V
C326 *0.1U/10V_NC
C329 *0.1U/10V_NC
C739 *0.1U/10V_NC
C741 *0.1U/10V_NC
C744 *0.1U/10V_NC
C747 *0.1U/10V_NC
C749 *0.1U/10V_NC
QUANTA COMPUTER
Title
DDRII TERMINATION
Size
Document Number
FX5
Rev
1A
Date: Friday, May 04, 2007
Sheet 8 of 61



QUANTA COMPUTER

Title	RS690T-HT LINK0 I/F	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 9 of 61	



Title	RS690T-PCIE LINK I/F
Size	Document Number FX5
Rev	1A
Date:	Friday, May 04, 2007
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Close RST690T.

R539,R537,R532 close to NB

R552,R517,R514 close to NB

Workaround ciecuit for RS690T
A11 pop R236 and depop R556
A12 Pop R556 and depop R236

RS690: LVDDR18A=3.3V
RS485: LVDDR18A=1.8V

Place C113 < 100mils from CPU

FOR RS690 ONLY

Close to Pin B23

RS690T

LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

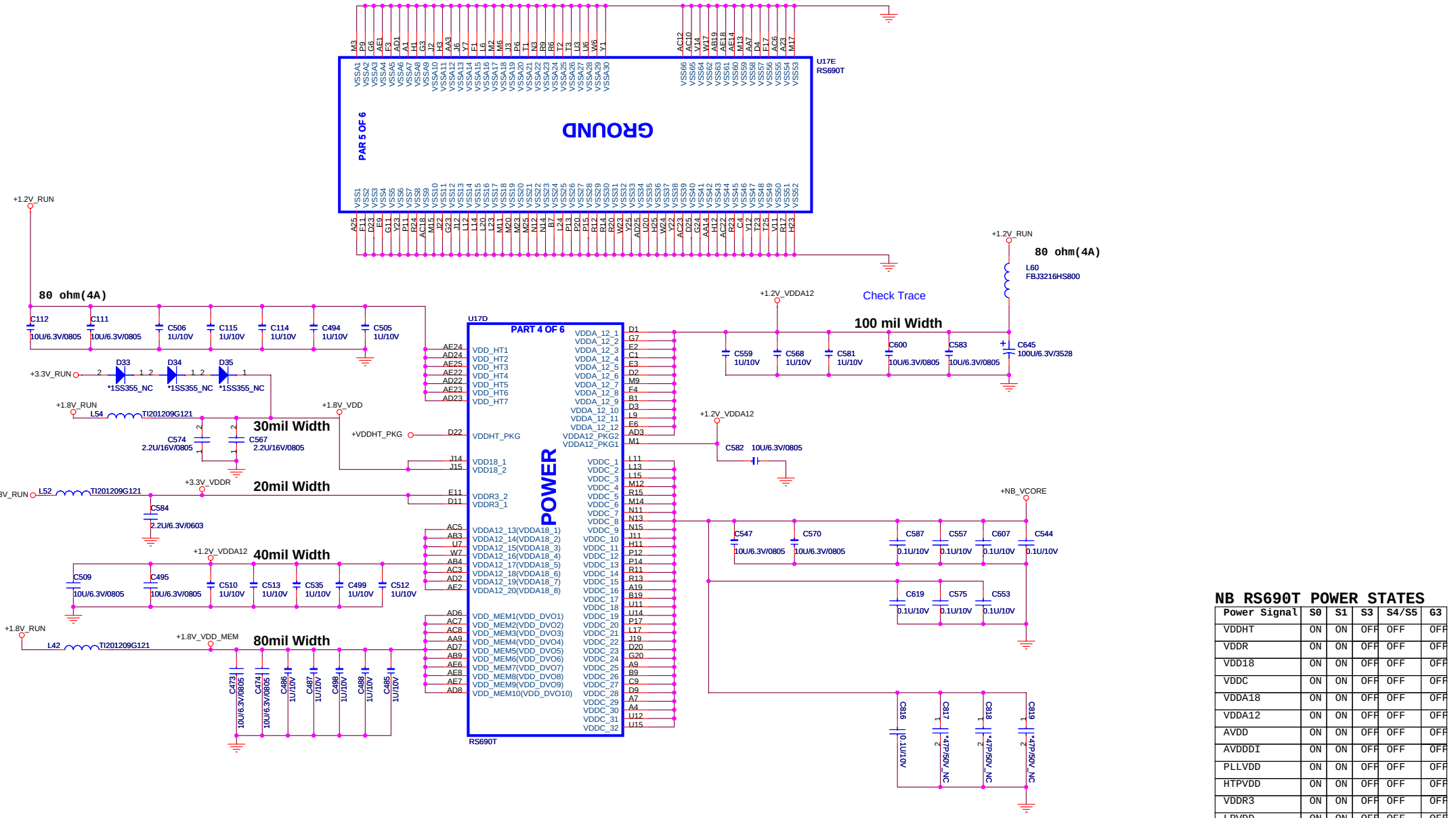
	PU by internal	PD by external
DFT_GPIO0	Side-Port Memory Disable	Side-Port Memory Enable (Default)
DFT_GPIO1	Bypassing EEPROM, use default values	Using EEPROM Strapping
DFT_GPIO[4:2]	Set PCI-E GPP mode to Conf. E	Select PCI-E GPP mode
DFT_GPIO5	Use default values	Use the memory data bus for debug bus output

by default

(289)

QUANTA COMPUTER

Title	RS690T-LVDS	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 11 of 61	

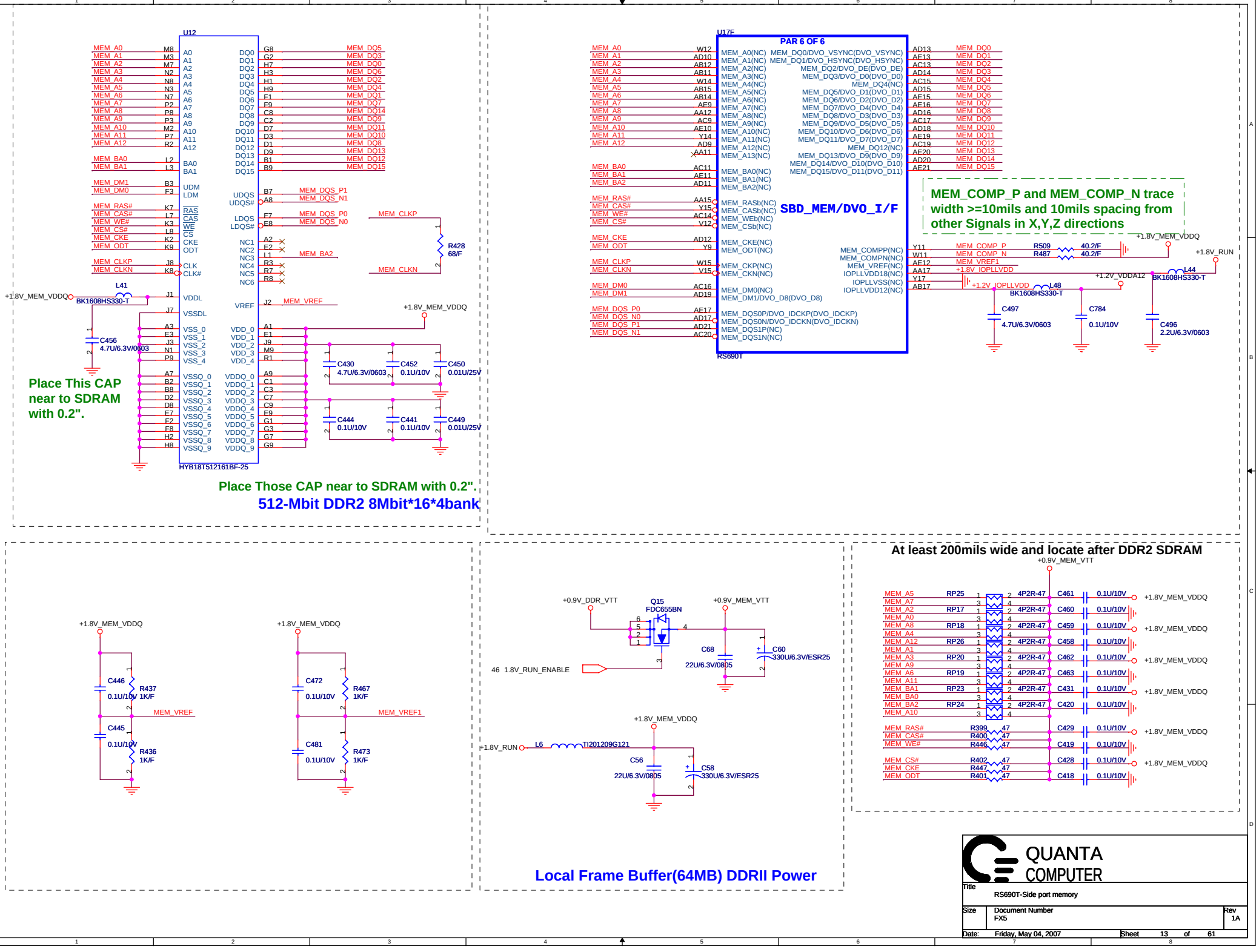


NB RS690T POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

QUANTA COMPUTER

Title	RS690T-POWER	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 12 of 61	


U12
HYB18T512161BF-25
L41
BK1608HS330-T
+1.8V_MEM_VDDQ
C456
4.7U/6.3V/0603
Place This CAP near to SDRAM with 0.2".
Place Those CAP near to SDRAM with 0.2".
512-Mbit DDR2 8Mbit*16*4bank
U17F
PAR 6 OF 6
SBD_MEM/DVO_I/F
RS690T
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
+1.8V_RUN
+1.2V_VDDA12
+1.2V_IOPLLVDD
L48
L44
BK1608HS330-T
C497
4.7U/6.3V/0603
C784
0.1U/10V
C496
2.2U/6.3V/0603
At least 200mils wide and locate after DDR2 SDRAM
+0.9V_MEM_VTT
+0.9V_DDR_VTT
Q15
FDC655BN
C68
22U/6.3V/0805
C60
330U/6.3V/ESR25
1.8V_RUN_ENABLE
L6
TI201209G121
C56
C58
Local Frame Buffer(64MB) DDRII Power
QUANTA COMPUTER
Title
RS690T-Side port memory
Size
Document Number
FX5
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1A
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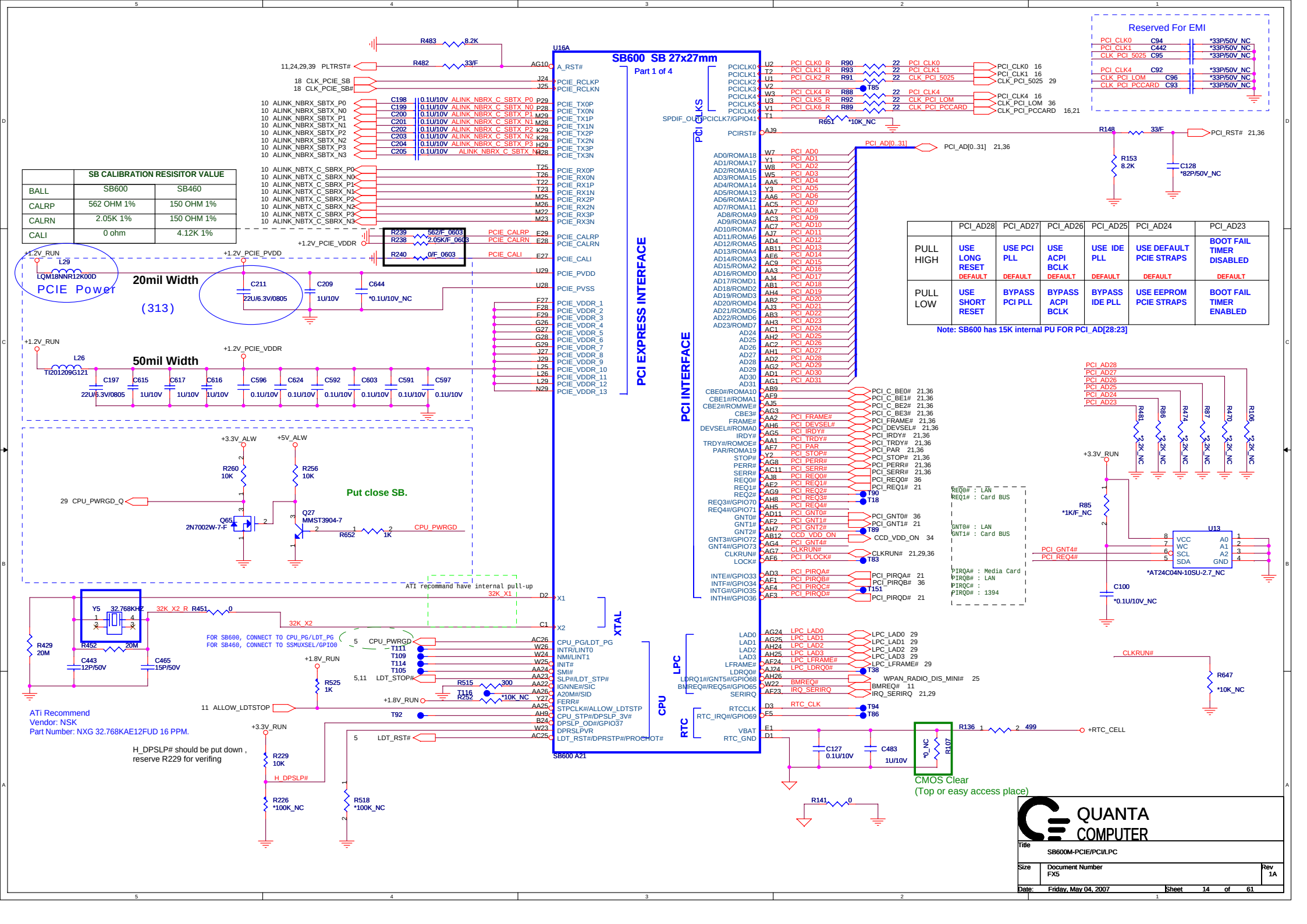
SB600 SB 27x27mm
Part 1 of 4
U16A
SB600 A21
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
LPC
CPU
RTC
Reserved For EMI
SB CALIBRATION RESISITOR VALUE
BALL | SB600 | SB460
CALRP | 562 OHM 1% | 150 OHM 1%
CALRN | 2.05K 1% | 150 OHM 1%
CALI | 0 ohm | 4.12K 1%
PCIE Power
(313)
20mil Width
50mil Width
Put close SB.
ATi recommand have internal pull-up
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
H_DPSLP# should be put down , reserve R229 for verifing
CMOS Clear
(Top or easy access place)
PULL HIGH
PULL LOW
PCI_AD28 | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23
USE LONG RESET DEFAULT | USE PCI PLL DEFAULT | USE ACPI BCLK DEFAULT | USE IDE PLL DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | BOOT FAIL TIMER DISABLED DEFAULT
USE SHORT RESET | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | USE EEPROM PCIE STRAPS | BOOT FAIL TIMER ENABLED
Note: SB600 has 15K internal PU FOR PCI_AD[28:23]
QUANTA COMPUTER
Title: SB600M-PCIE/PCI/LPC
Size: Document Number: FX5
Rev: 1A
Date: Friday, May 04, 2007
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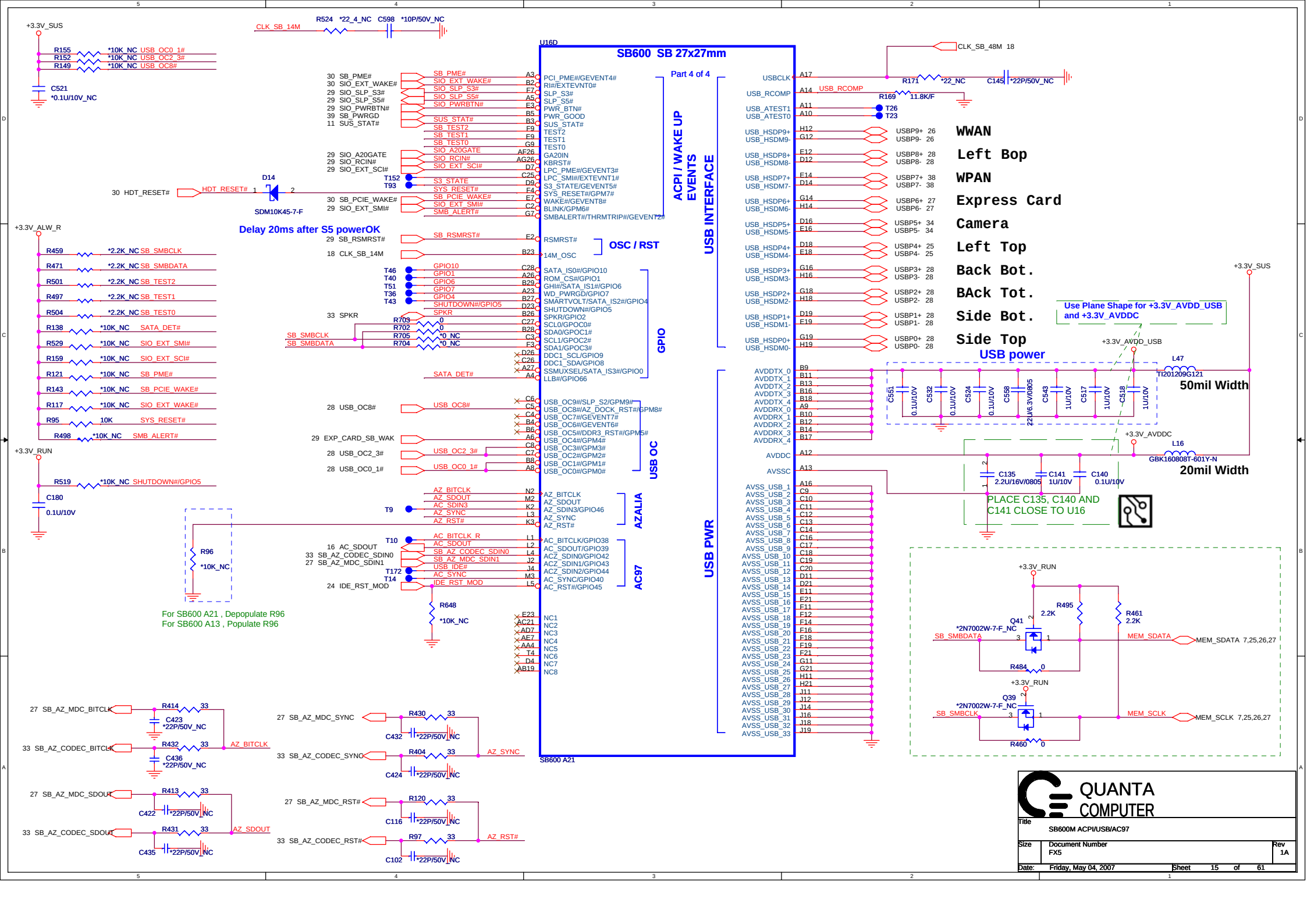
SB600 SB 27x27mm
Part 4 of 4
U16D
SB600 A21
ACPI / WAKE UP EVENTS
USB INTERFACE
GPIO
USB OC
AZALIA
AC97
USB PWR
OSC / RST
Delay 20ms after S5 powerOK
WWAN
Left Bop
WPAN
Express Card
Camera
Left Top
Back Bot.
BAck Tot.
Side Bot.
Side Top
USB power
Use Plane Shape for +3.3V_AVDD_USB and +3.3V_AVDDC
50mil Width
20mil Width
PLACE C135, C140 AND C141 CLOSE TO U16
For SB600 A21 , Depopulate R96
For SB600 A13 , Populate R96
QUANTA COMPUTER
Title
SB600M ACPI/USB/AC97
Size
Document Number
FX5
Rev
1A
Date:
Friday, May 04, 2007
Sheet
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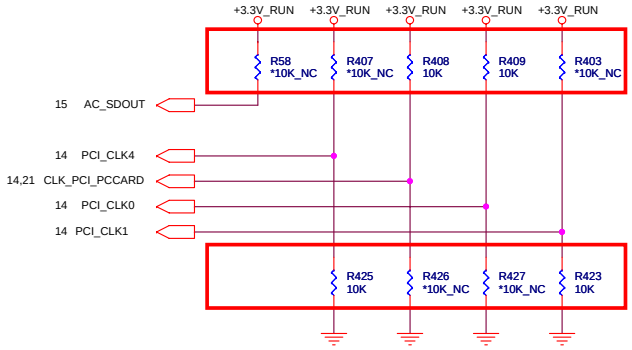
of
61

REQUIRED STRAPS

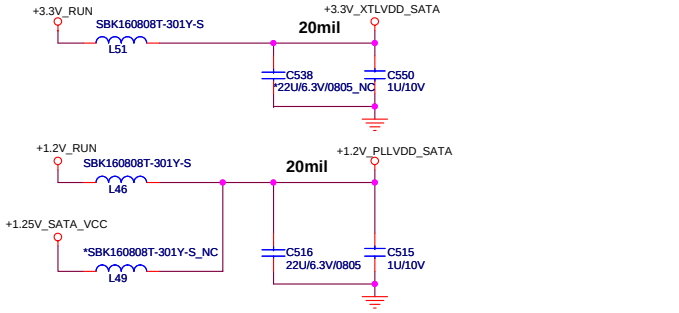
15K internal PU for RTC_CLK
,External PU/PD is not required.
SB600 has 15K internal PD for AC_SDOUT

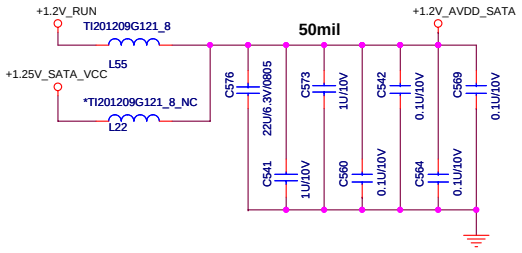


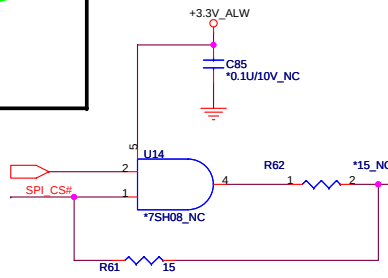
CLK_PCI_PCCARD

	AC_SDOUT	RTC_CLK	PCI_CLK4		PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	H, H = PCI ROM H, L = SPI ROM DEFAULT L, H = LPC ROM L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	

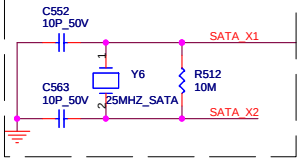
SATA Power

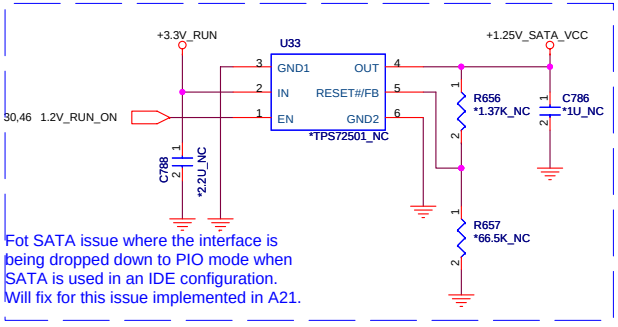






SATA clock Option

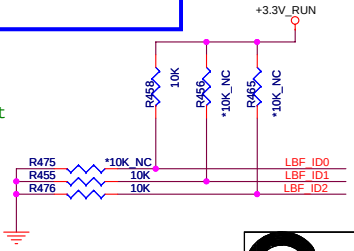


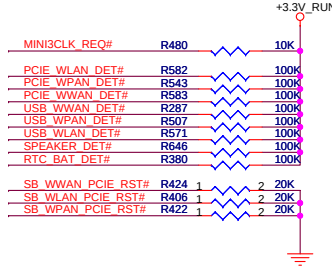


Fot SATA issue where the interface is being dropped down to PIO mode when SATA is used in an IDE configuration. Will fix for this issue implemented in A21.

Local Frame Buffer Strapping List

	LBF_ID2	LBF_ID1	LBF_ID0
Hyanix	0 R476	0 R455	0 R475
Qimonda	0 R476	0 R455	1 R458
Samsung	0 R476	1 R456	0 R475





QUANTA COMPUTER

Title	SB600M HDD/POWER
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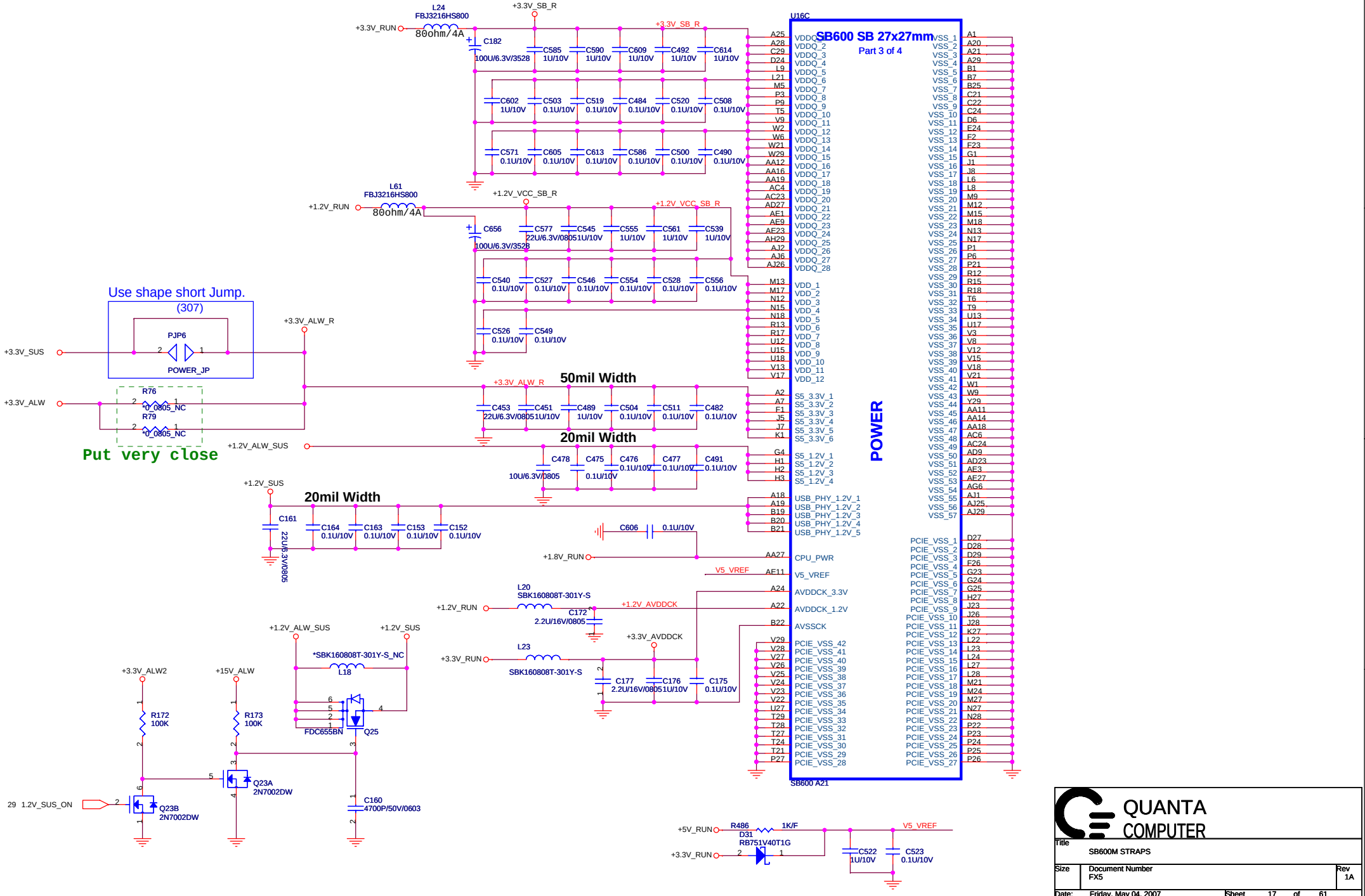
L24
FBJ3216HS800
+3.3V_RUN
80ohm/4A
+3.3V_SB_R
C182
100U/6.3V/3528
C585 1U/10V
C590 1U/10V
C609 1U/10V
C492 1U/10V
C614 1U/10V
C602 1U/10V
C503 0.1U/10V
C519 0.1U/10V
C484 0.1U/10V
C520 0.1U/10V
C508 0.1U/10V
C571 0.1U/10V
C605 0.1U/10V
C613 0.1U/10V
C586 0.1U/10V
C500 0.1U/10V
C490 0.1U/10V
L61
FBJ3216HS800
+1.2V_RUN
80ohm/4A
+1.2V_VCC_SB_R
C656
100U/6.3V/3528
C577 22U/6.3V/0805
C545 1U/10V
C555 1U/10V
C561 1U/10V
C539 1U/10V
C540 0.1U/10V
C527 0.1U/10V
C546 0.1U/10V
C554 0.1U/10V
C528 0.1U/10V
C556 0.1U/10V
C526 0.1U/10V
C549 0.1U/10V
U16C
SB600 SB 27x27mm
Part 3 of 4
VDDQ_1 A25
VDDQ_2 A28
VDDQ_3 C29
VDDQ_4 D24
VDDQ_5 L9
VDDQ_6 L21
VDDQ_7 M5
VDDQ_8 P3
VDDQ_9 P9
VDDQ_10 T5
VDDQ_11 V9
VDDQ_12 W2
VDDQ_13 W6
VDDQ_14 W21
VDDQ_15 W29
VDDQ_16 AA12
VDDQ_17 AA16
VDDQ_18 AA19
VDDQ_19 AC4
VDDQ_20 AC23
VDDQ_21 AD27
VDDQ_22 AE1
VDDQ_23 AE9
VDDQ_24 AE23
VDDQ_25 AH29
VDDQ_26 AJ2
VDDQ_27 AJ6
VDDQ_28 AJ26
VDD_1 M13
VDD_2 M17
VDD_3 N12
VDD_4 N15
VDD_5 N18
VDD_6 R13
VDD_7 R17
VDD_8 U12
VDD_9 U15
VDD_10 U18
VDD_11 V13
VDD_12 V17
S5_3.3V_1 A2
S5_3.3V_2 A7
S5_3.3V_3 F1
S5_3.3V_4 J5
S5_3.3V_5 J7
S5_3.3V_6 K1
S5_1.2V_1 G4
S5_1.2V_2 H1
S5_1.2V_3 H2
S5_1.2V_4 H3
USB_PHY_1.2V_1 A18
USB_PHY_1.2V_2 A19
USB_PHY_1.2V_3 B19
USB_PHY_1.2V_4 B20
USB_PHY_1.2V_5 B21
CPU_PWR AA27
V5_VREF AE11
AVDDCK_3.3V A24
AVDDCK_1.2V A22
AVSSCK B22
PCIE_VSS_42 V29
PCIE_VSS_41 V28
PCIE_VSS_40 V27
PCIE_VSS_39 V26
PCIE_VSS_38 V25
PCIE_VSS_37 V24
PCIE_VSS_36 V23
PCIE_VSS_35 V22
PCIE_VSS_34 U27
PCIE_VSS_33 T29
PCIE_VSS_32 T28
PCIE_VSS_31 T27
PCIE_VSS_30 T24
PCIE_VSS_29 T21
PCIE_VSS_28 P27
VSS_1 A1
VSS_2 A20
VSS_3 A21
VSS_4 A29
VSS_5 B1
VSS_6 B7
VSS_7 B25
VSS_8 C21
VSS_9 C22
VSS_10 C24
VSS_11 D6
VSS_12 E24
VSS_13 F2
VSS_14 F23
VSS_15 G1
VSS_16 J1
VSS_17 J8
VSS_18 L6
VSS_19 L8
VSS_20 M9
VSS_21 M12
VSS_22 M15
VSS_23 M18
VSS_24 N13
VSS_25 N17
VSS_26 P1
VSS_27 P6
VSS_28 P21
VSS_29 R12
VSS_30 R15
VSS_31 R18
VSS_32 T6
VSS_33 T9
VSS_34 U13
VSS_35 U17
VSS_36 V3
VSS_37 V8
VSS_38 V12
VSS_39 V15
VSS_40 V18
VSS_41 V21
VSS_42 W1
VSS_43 W9
VSS_44 Y29
VSS_45 AA11
VSS_46 AA14
VSS_47 AA18
VSS_48 AC6
VSS_49 AC24
VSS_50 AD9
VSS_51 AD23
VSS_52 AE3
VSS_53 AE27
VSS_54 AG6
VSS_55 AJ1
VSS_56 AJ25
VSS_57 AJ29
PCIE_VSS_1 D27
PCIE_VSS_2 D28
PCIE_VSS_3 D29
PCIE_VSS_4 F26
PCIE_VSS_5 G23
PCIE_VSS_6 G24
PCIE_VSS_7 G25
PCIE_VSS_8 H27
PCIE_VSS_9 J23
PCIE_VSS_10 J26
PCIE_VSS_11 J28
PCIE_VSS_12 K27
PCIE_VSS_13 L22
PCIE_VSS_14 L23
PCIE_VSS_15 L24
PCIE_VSS_16 L27
PCIE_VSS_17 L28
PCIE_VSS_18 M21
PCIE_VSS_19 M24
PCIE_VSS_20 M27
PCIE_VSS_21 N27
PCIE_VSS_22 N28
PCIE_VSS_23 P22
PCIE_VSS_24 P23
PCIE_VSS_25 P24
PCIE_VSS_26 P25
PCIE_VSS_27 P26
POWER
SB600 A21
Use shape short Jump.
(307)
PJP6
POWER_JP
+3.3V_SUS
+3.3V_ALW_R
+3.3V_ALW
R76
0_0805_NC
R79
0_0805_NC
Put very close
50mil Width
C453 22U/6.3V/0805
C451 1U/10V
C489 1U/10V
C504 0.1U/10V
C511 0.1U/10V
C482 0.1U/10V
+1.2V_ALW_SUS
20mil Width
C478 10U/6.3V/0805
C475 0.1U/10V
C476 0.1U/10V
C477 0.1U/10V
C491 0.1U/10V
+1.2V_SUS
20mil Width
C161 22U/6.3V/0805
C164 0.1U/10V
C163 0.1U/10V
C153 0.1U/10V
C152 0.1U/10V
C606 0.1U/10V
+1.8V_RUN
V5_VREF
L20
SBK160808T-301Y-S
+1.2V_RUN
C172
2.2U/16V/0805
+1.2V_AVDDCK
L23
+3.3V_RUN
SBK160808T-301Y-S
+3.3V_AVDDCK
C177 2.2U/16V/0805
C176 1U/10V
C175 0.1U/10V
+1.2V_ALW_SUS
+1.2V_SUS
*SBK160808T-301Y-S_NC
L18
FDC655BN
Q25
+3.3V_ALW2
+15V_ALW
R172 100K
R173 100K
Q23A 2N7002DW
Q23B 2N7002DW
29 1.2V_SUS_ON
C160 4700P/50V/0603
+5V_RUN
+3.3V_RUN
R486 1K/F
D31 RB751V40T1G
V5_VREF
C522 1U/10V
C523 0.1U/10V
QUANTA COMPUTER
Title
SB600M STRAPS
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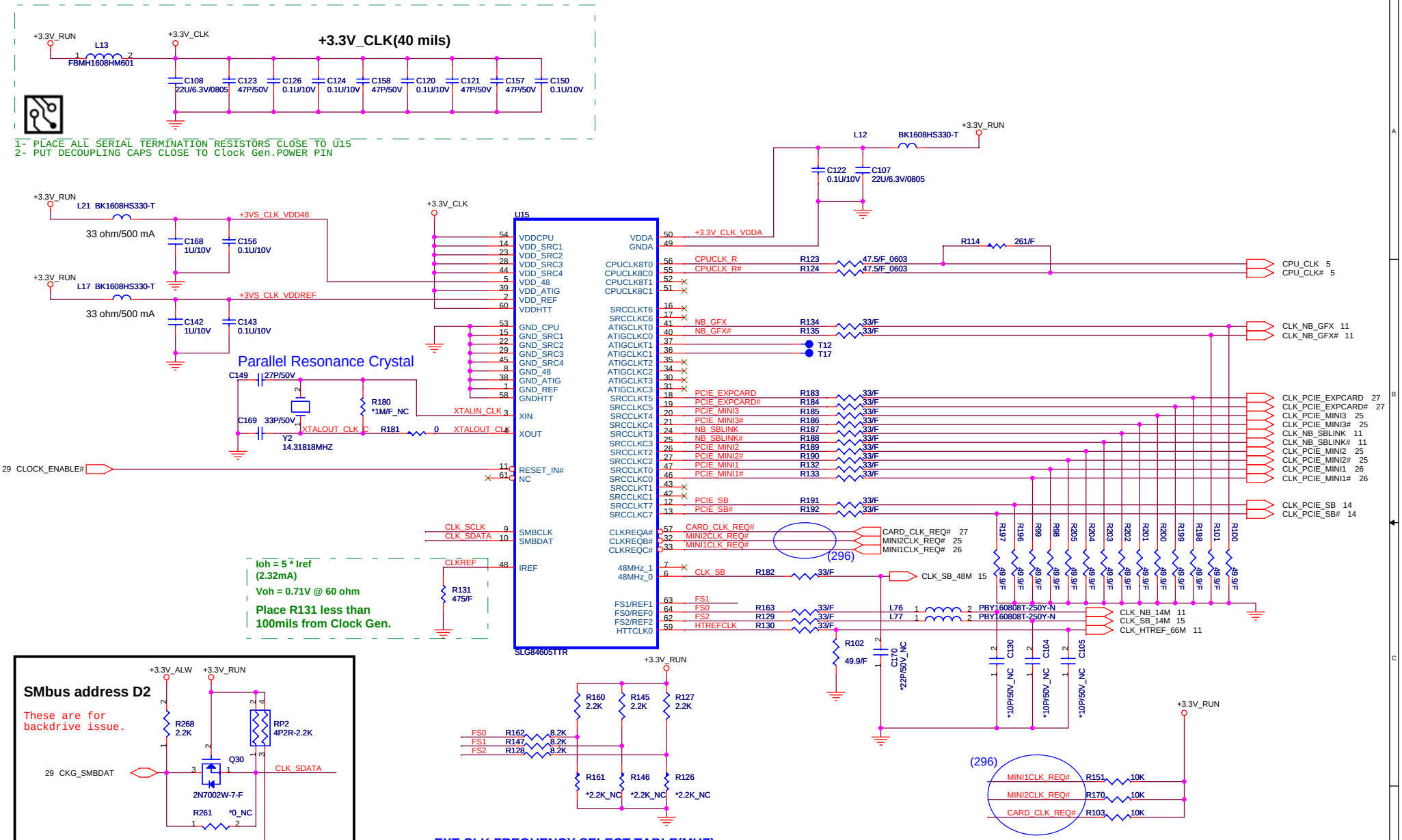

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Title	CLOCK GENERATOR
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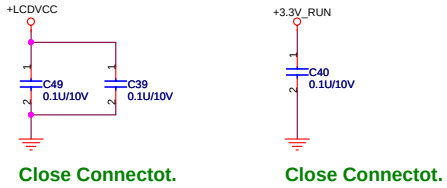
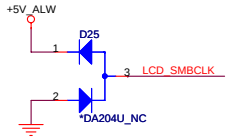
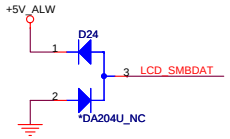


Close Connectot.

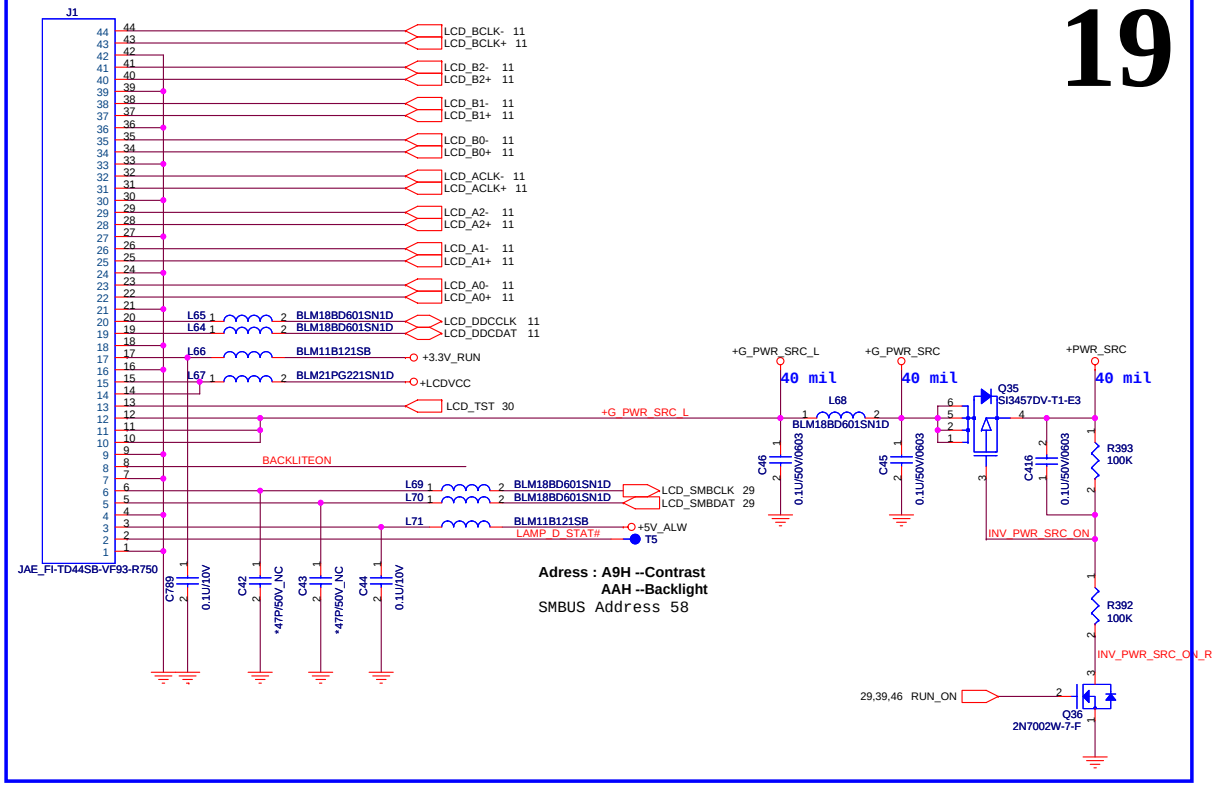
Close Connectot.



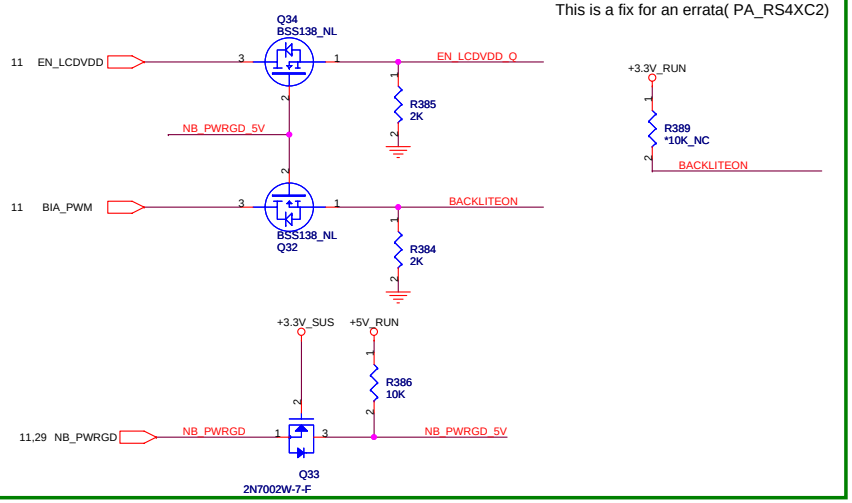
Close Connectot.

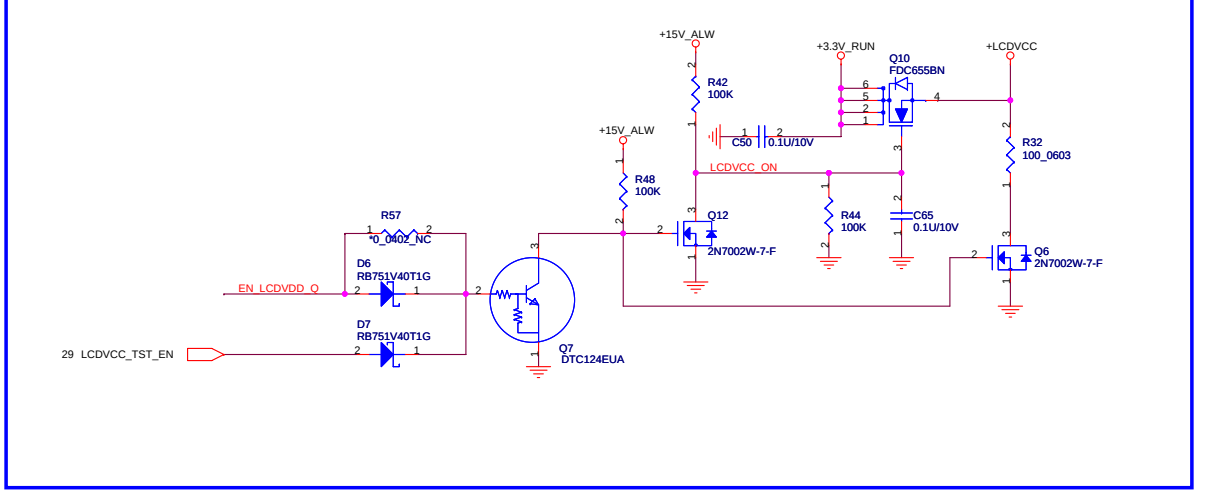


Close Connectot.



This is a fix for an errata(PA_RS4XC2)





QUANTA COMPUTER

Title	LCD CONN&CK-SSCD	
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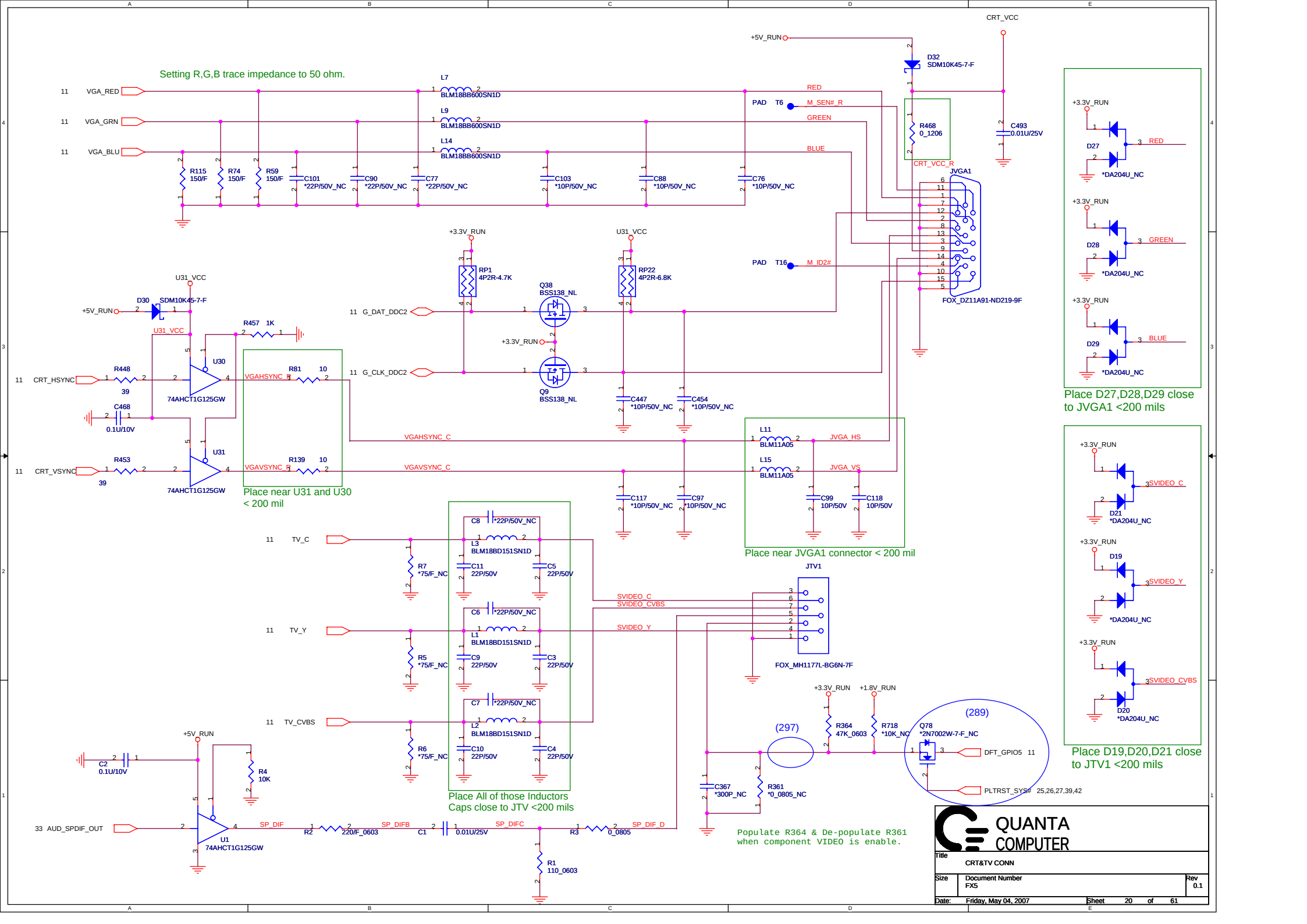
Setting R,G,B trace impedance to 50 ohm.
VGA_RED
VGA_GRN
VGA_BLU
L7 BLM18BB600SN1D
L9 BLM18BB600SN1D
L14 BLM18BB600SN1D
R115 150/F
R74 150/F
R59 150/F
C101 *22P/50V_NC
C90 *22P/50V_NC
C77 *22P/50V_NC
C103 *10P/50V_NC
C88 *10P/50V_NC
C76 *10P/50V_NC
RED
GREEN
BLUE
PAD T6
M_SEN# R
CRT_VCC
+5V_RUN
D32 SDM10K45-7-F
R468 0_1206
C493 0.01U/25V
CRT_VCC_R
JVGA1
FOX_DZ11A91-ND219-9F
PAD T16
M_ID2#
+3.3V_RUN
U31_VCC
RP1 4P2R-4.7K
RP22 4P2R-6.8K
Q38 BSS138_NL
Q9 BSS138_NL
11 G_DAT_DDC2
11 G_CLK_DDC2
D30 SDM10K45-7-F
R457 1K
R448 39
R453 39
U30
U31
74AHCT1G125GW
11 CRT_HSYNC
11 CRT_VSYNC
C468 0.1U/10V
R81 10
R139 10
VGAHSYNC_R
VGAVSYNC_R
VGAHSYNC_C
VGAVSYNC_C
C447 *10P/50V_NC
C454 *10P/50V_NC
C117 *10P/50V_NC
C97 *10P/50V_NC
L11 BLM11A05
L15 BLM11A05
JVGA_HS
JVGA_VS
C99 10P/50V
C118 10P/50V
Place near U31 and U30 < 200 mil
Place near JVGA1 connector < 200 mil
11 TV_C
11 TV_Y
11 TV_CVBS
C8 *22P/50V_NC
C6 *22P/50V_NC
C7 *22P/50V_NC
L3 BLM18BD151SN1D
L1 BLM18BD151SN1D
L2 BLM18BD151SN1D
R7 *75/F_NC
R5 *75/F_NC
R6 *75/F_NC
C11 22P/50V
C9 22P/50V
C10 22P/50V
C5 22P/50V
C3 22P/50V
C4 22P/50V
SVIDEO_C
SVIDEO_CVBS
SVIDEO_Y
JTV1
FOX_MH1177L-BG6N-7F
Place All of those Inductors Caps close to JTV <200 mils
+3.3V_RUN
+1.8V_RUN
R364 47K_0603
R718 *10K_NC
Q78 *2N7002W-7-F_NC
(289)
(297)
DFT_GPIO5 11
PLTRST_SYS# 25,26,27,39,42
C367 *300P_NC
R361 *0_0805_NC
Populate R364 & De-populate R361 when component VIDEO is enable.
C2 0.1U/10V
R4 10K
U1 74AHCT1G125GW
33 AUD_SPDIF_OUT
SP_DIF
SP_DIFB
SP_DIFC
SP_DIF_D
R2 220/F_0603
C1 0.01U/25V
R3 0_0805
R1 110_0603
D27 *DA204U_NC
D28 *DA204U_NC
D29 *DA204U_NC
Place D27,D28,D29 close to JVGA1 <200 mils
D21 *DA204U_NC
D19 *DA204U_NC
D20 *DA204U_NC
Place D19,D20,D21 close to JTV1 <200 mils
QUANTA COMPUTER
Title CRT&TV CONN
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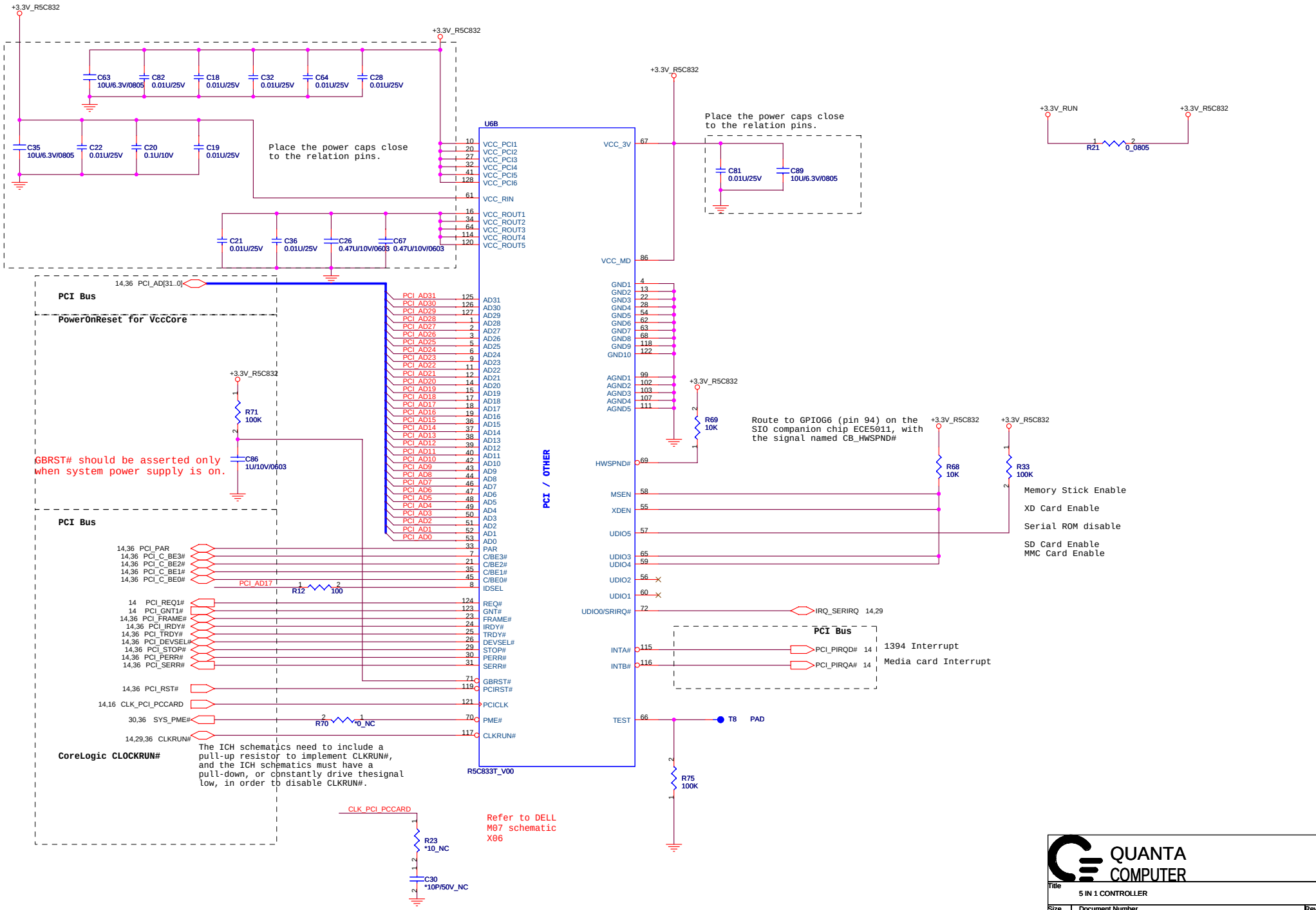
+3.3V_R5C832
C63 10U/6.3V/0805
C82 0.01U/25V
C18 0.01U/25V
C32 0.01U/25V
C64 0.01U/25V
C28 0.01U/25V
C35 10U/6.3V/0805
C22 0.01U/25V
C20 0.1U/10V
C19 0.01U/25V
Place the power caps close to the relation pins.
C21 0.01U/25V
C36 0.01U/25V
C26 0.47U/10V/0603
C67 0.47U/10V/0603
U6B
VCC_PCI1
VCC_PCI2
VCC_PCI3
VCC_PCI4
VCC_PCI5
VCC_PCI6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
C81 0.01U/25V
C89 10U/6.3V/0805
Place the power caps close to the relation pins.
+3.3V_RUN
R21 0_0805
14,36 PCI_AD[31..0]
PCI Bus
PowerOnReset for VccCore
R71 100K
C86 1U/10V/0603
GBRST# should be asserted only when system power supply is on.
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PCI / OTHER
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND2
AGND3
AGND4
AGND5
R69 10K
HWSPND#
Route to GPIOG6 (pin 94) on the SIO companion chip ECE5011, with the signal named CB_HWSPND#
R68 10K
R33 100K
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
IRQ_SERIRQ 14,29
Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable
PCI Bus
INTA#
INTB#
PCI_PIRQD# 14
PCI_PIRQA# 14
1394 Interrupt
Media card Interrupt
14,36 PCI_PAR
14,36 PCI_C_BE3#
14,36 PCI_C_BE2#
14,36 PCI_C_BE1#
14,36 PCI_C_BE0#
C/BE3#
C/BE2#
C/BE1#
C/BE0#
PAR
IDSEL
PCI_AD17
R12 100
14 PCI_REQ1#
14 PCI_GNT1#
14,36 PCI_FRAME#
14,36 PCI_IRDY#
14,36 PCI_TRDY#
14,36 PCI_DEVSEL#
14,36 PCI_STOP#
14,36 PCI_PERR#
14,36 PCI_SERR#
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
14,36 PCI_RST#
14,16 CLK_PCI_PCCARD
30,36 SYS_PME#
14,29,36 CLKRUN#
GBRST#
PCIRST#
PCICLK
PME#
CLKRUN#
R70 *0_NC
CoreLogic CLOCKRUN#
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive thesignal low, in order to disable CLKRUN#.
R5C833T_V00
TEST
T8 PAD
R75 100K
CLK_PCI_PCCARD
R23 *10_NC
C30 *10P/50V_NC
Refer to DELL M07 schematic X06
QUANTA COMPUTER
Title
5 IN 1 CONTROLLER
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80 mils

+3.3V_R5C832

+3.3V_RUN_PHY

L8
BLM18PG181SN1D

C74 10U/6.3V/0805
C73 0.1U/10V
C37 0.01U/25V
C47 1000P/50V

modify

Place these caps as close to the U6 as possible.

U6A

AVCC_PHY1 98
AVCC_PHY2 106
AVCC_PHY3 110
AVCC_PHY4 112

AS CLOSE AS POSSIBLE TO R5C832

TPBIAS0 113

C54 0.33U/16V/0603
C57 0.01U/25V
R31 56.2/F_0603
R34 56.2/F_0603

TPBN0 104 TPB0N
TPBP0 105 TPB0P
TPAN0 108 TPA0N
TPAP0 109 TPA0P

R36 56.2/F_0603
R45 56.2/F_0603
C66 270P/25V
R37 5.11K/F

Circuit area : As small as possible.

*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

Place these caps as close to the U6 as possible.

C83 22P/50V
1394_XI 94 XI
Y1 24.576MHz/7.2pF/50ppm
C84 27P/50V
1394_XO 95 XO
R73 0

RICOH_FILO
C79 *0.01U/25V_NC
96 FIL0

RICOH_REXT
R49 10K/F
101 REXT

RICOH_VREF
C71 0.01U/25V
100 VREF

IEEE1394/SD

97 RSV

R5C833T_V00

MDIO17 87 XD_DATA7 XD_DATA7 23
MDIO16 92 XD_DATA6 XD_DATA6 23
MDIO15 89 XD_DATA5 XD_DATA5 23
MDIO14 91 XD_DATA4 XD_DATA4 23
MDIO13 90 SD/XD/MS_DATA3 SD/XD/MS_DATA3 23
MDIO12 93 SD/XD/MS_DATA2 SD/XD/MS_DATA2 23
MDIO11 81 SD/XD/MS_DATA1 SD/XD/MS_DATA1 23
MDIO10 82 SD/XD/MS_DATA0 SD/XD/MS_DATA0 23

MDIO05 75 XD_WP# 23
MDIO08 88 SD/XD/MS_CMD SD/XD/MS_CMD 23
MDIO19 83 XD_ALE 23
MDIO18 85 XD_CLE 23
MDIO02 78 XD_CE# 23

MDIO03 77 MDIO03 MDIO03 23
MDIO00 80 SD_CD# SD_CD# 23
D12 1SS355
MDIO01 79 R_MS_INS# MS_INS# 23
D13 1SS355

MDIO09 84 SD/XD/MS_CLK 23
MDIO04 76 MC_PWR_CTRL_0 23
MDIO06 74 T7 PAD
MDIO07 73

+3.3V_R5C832
R108 *10K_NC
close to the Chip
XD_CDSW# 23

L45 *DLW21HN121SQ2_NC
L50 *DLW21HN121SQ2_NC

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

CON2
FOX_UV31413-WSU0D-7F

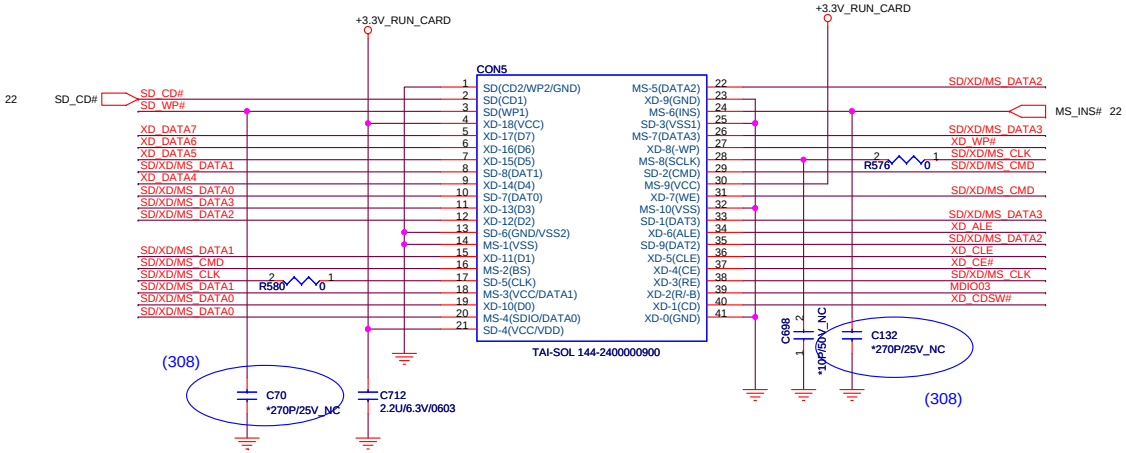
TPB0N R496 0_0805 TPB0-
TPB0P R502 0_0805 TPB0+
TPA0N R510 0_0805 TPA0-
TPA0P R505 0_0805 TPA0+

+3.3V_R5C832

SD/XD/MS_DATA3 R500 *2.7K_NC
SD/XD/MS_DATA2 R511 *2.7K_NC
SD/XD/MS_DATA1 R526 *2.7K_NC
SD/XD/MS_DATA0 R533 *2.7K_NC
SD/XD/MS_CMD R548 *2.7K_NC

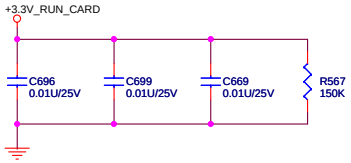
QUANTA COMPUTER

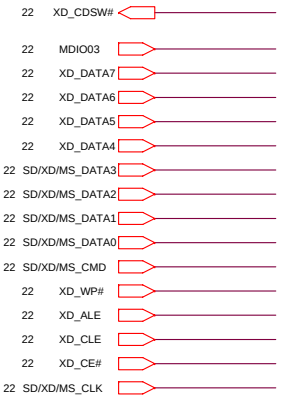
Title	IEEE 1394	
Size	Document Number FX5	Rev 0.1
Date: Friday, May 04, 2007	Sheet 22 of 61	

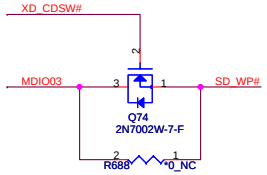


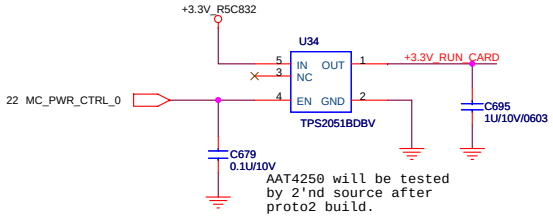
Close pin 4

8 IN1 CARD READER





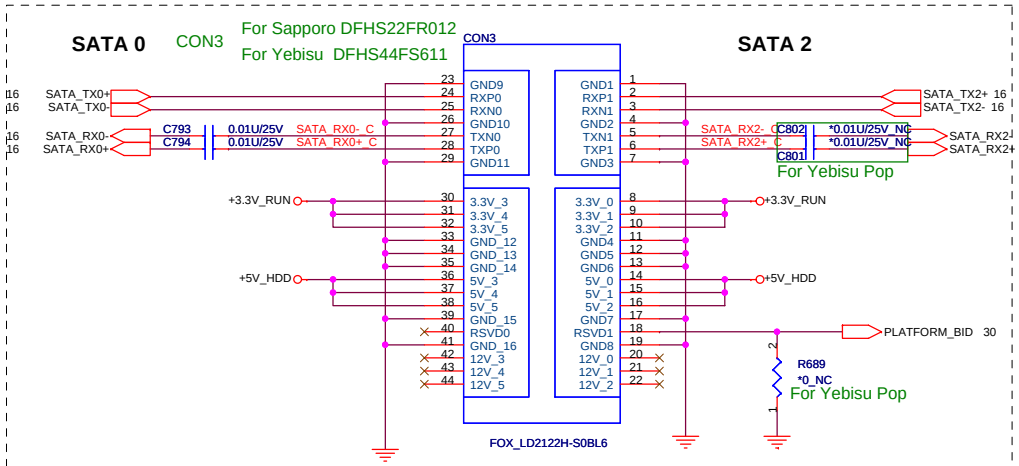


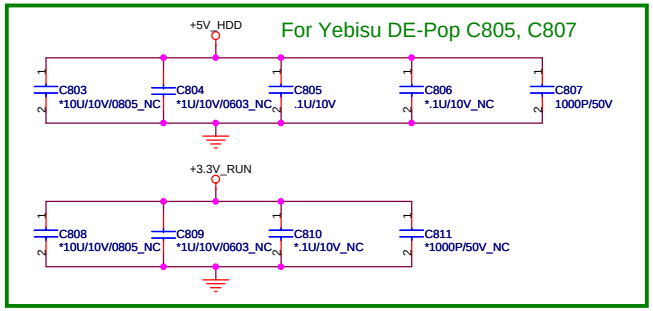


AAT4250 will be tested
by 2'nd source after
proto2 build.

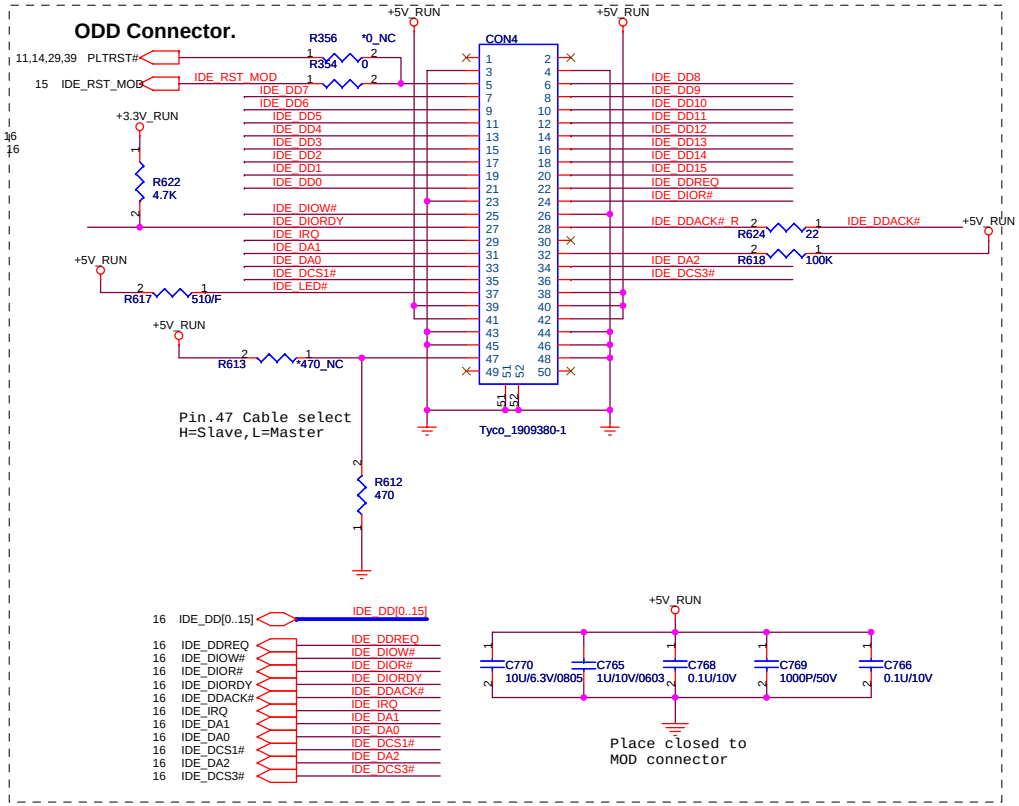
QUANTA COMPUTER

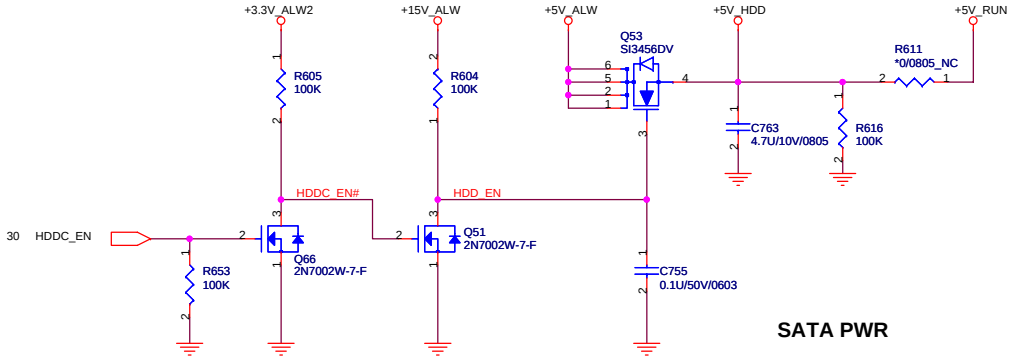
Title	CARD READER CONN	
Size	Document Number FX5	Rev 0.1
Date: Friday, May 04, 2007	Sheet 23 of 61	

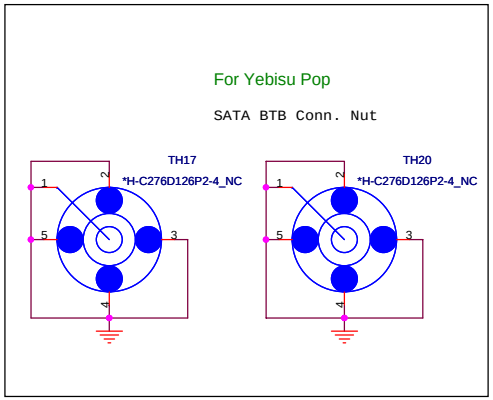




	FX5 (Sapporo)	GX2 (Yebisu)
R689	X	V
C801	X	V
C802	X	V
C805	V	X
C807	V	X



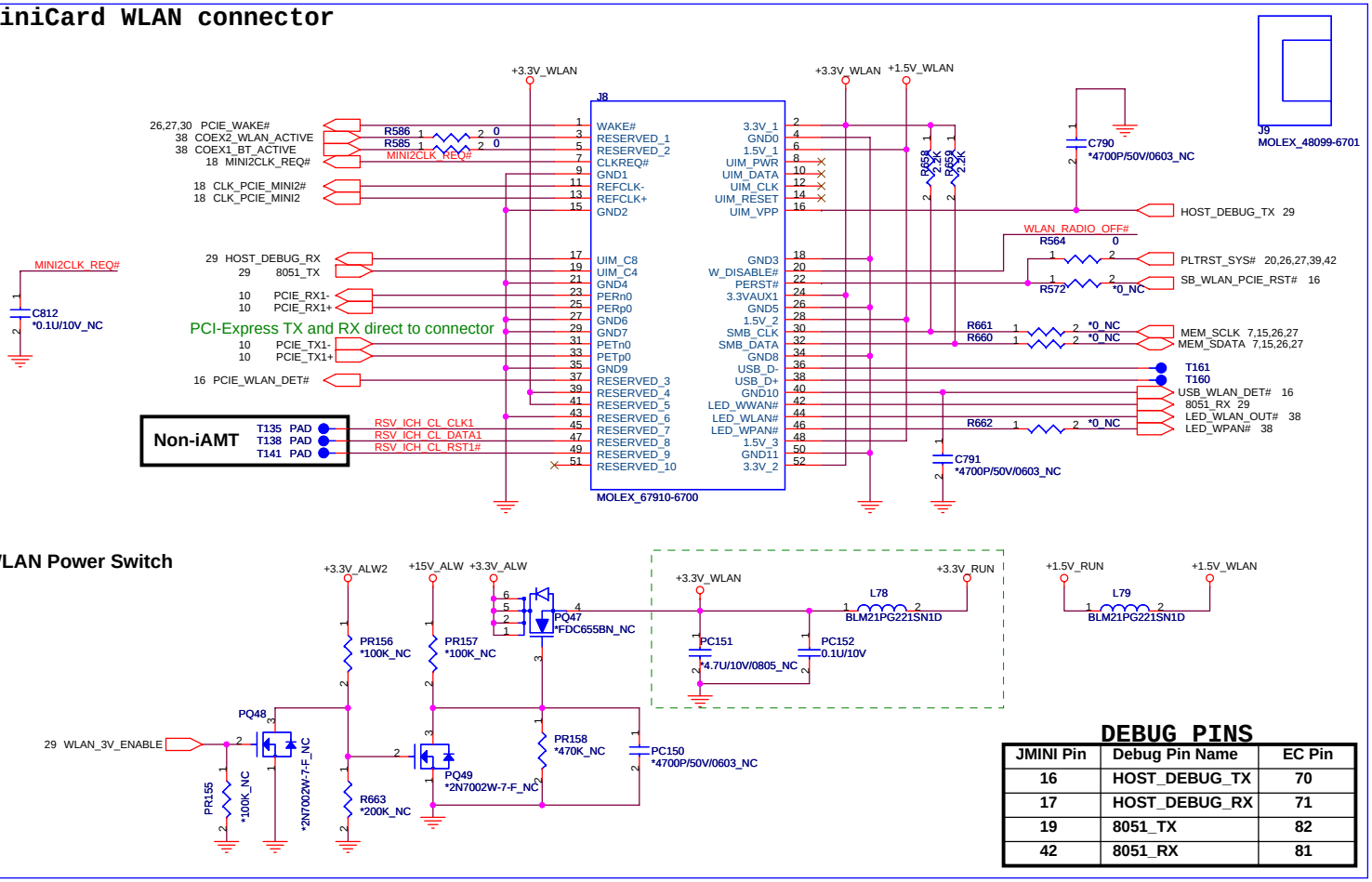


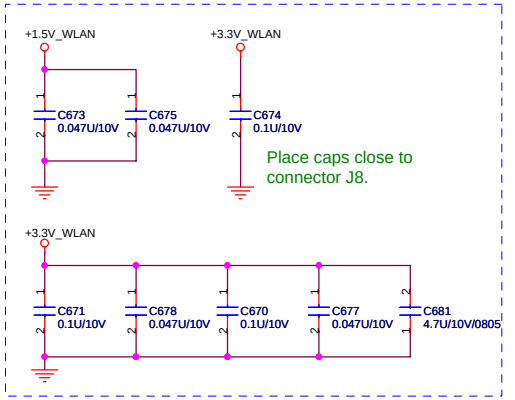


QUANTA COMPUTER

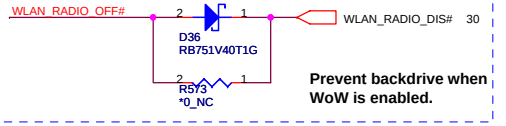
Title	SATA (HDD&CD_ROM)	
Size	Document Number FX5	Rev 0.1
Date: Friday, May 04, 2007	Sheet 24 of 61	

MiniCard WLAN connector





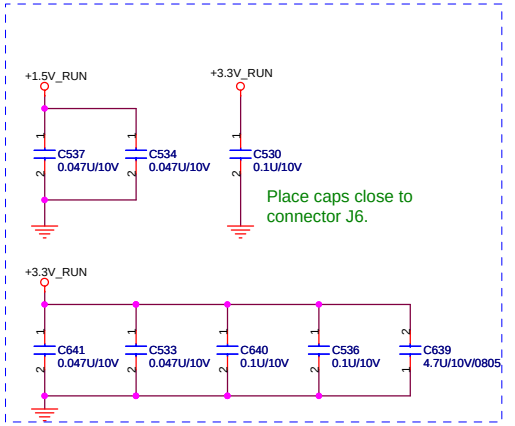
Suport for WoW

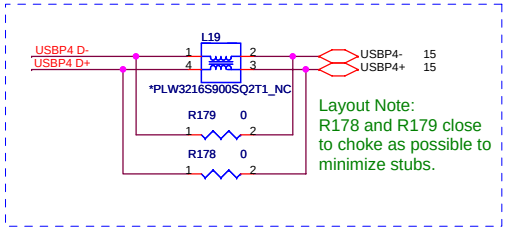


WLAN Power Switch

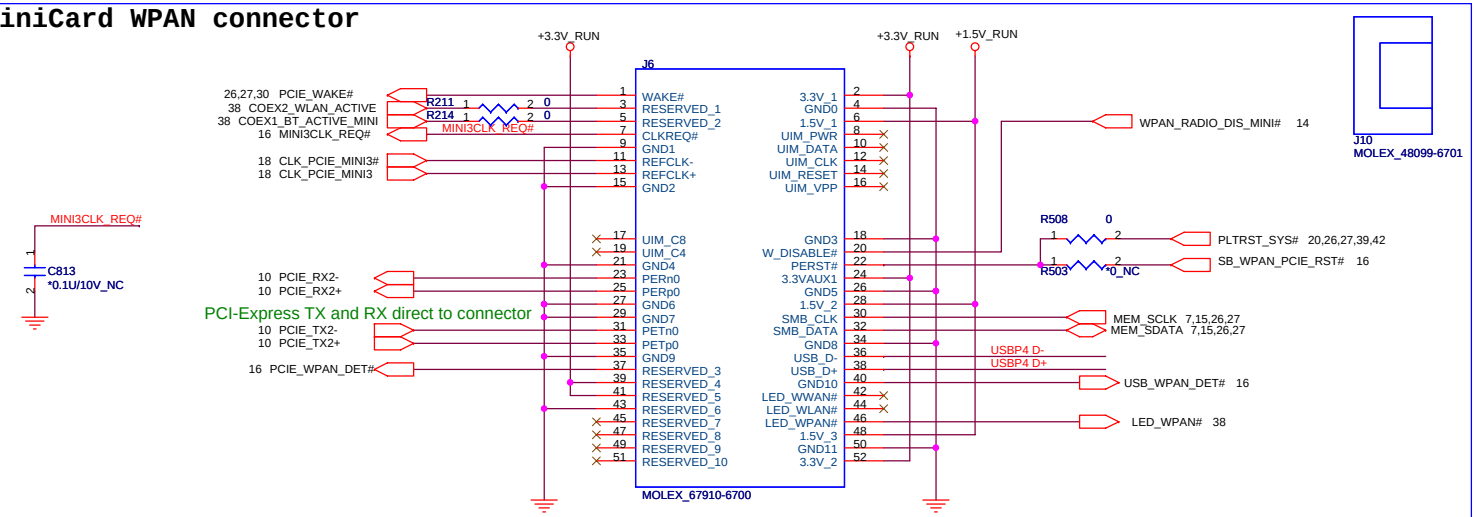
DEBUG_PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



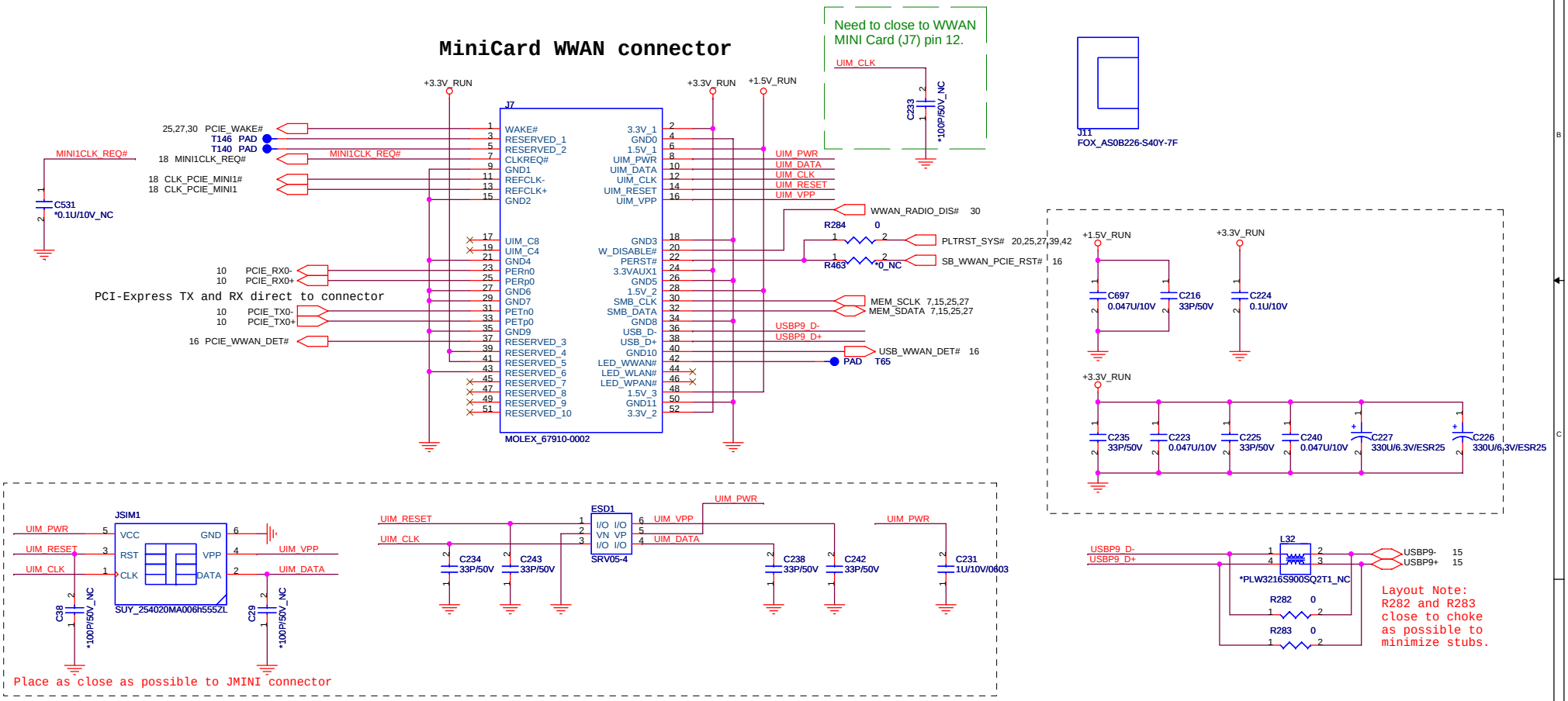


MiniCard WPAN connector



QUANTA COMPUTER			
Title: MINI-PCI			
Size	Document Number: FX5		Rev: 0.1
Date: Friday, May 04, 2007		Sheet 25 of 61	

MiniCard WWAN connector



Title	WWAN	
Size	Document Number FX5	Rev 0.1
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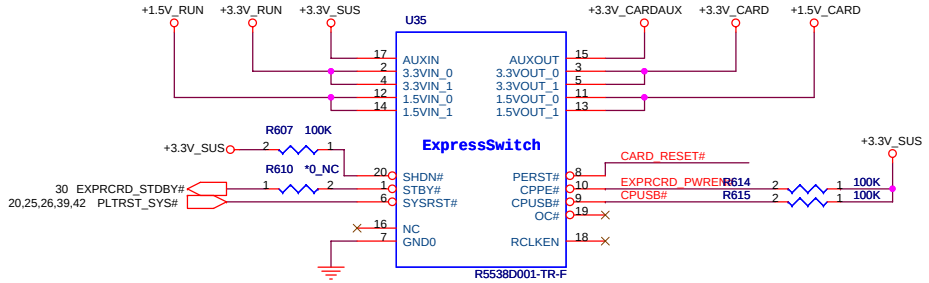
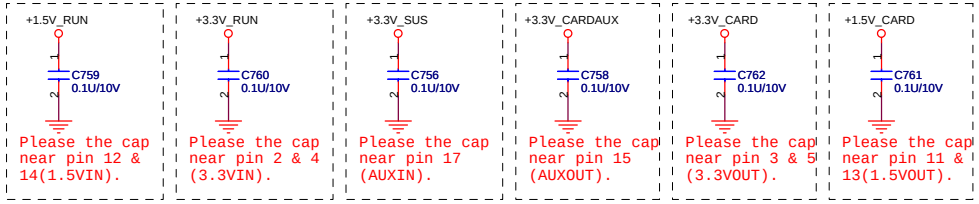
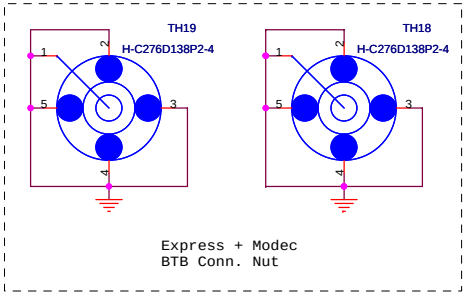
QUANTA COMPUTER

Express Card Power Switch

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

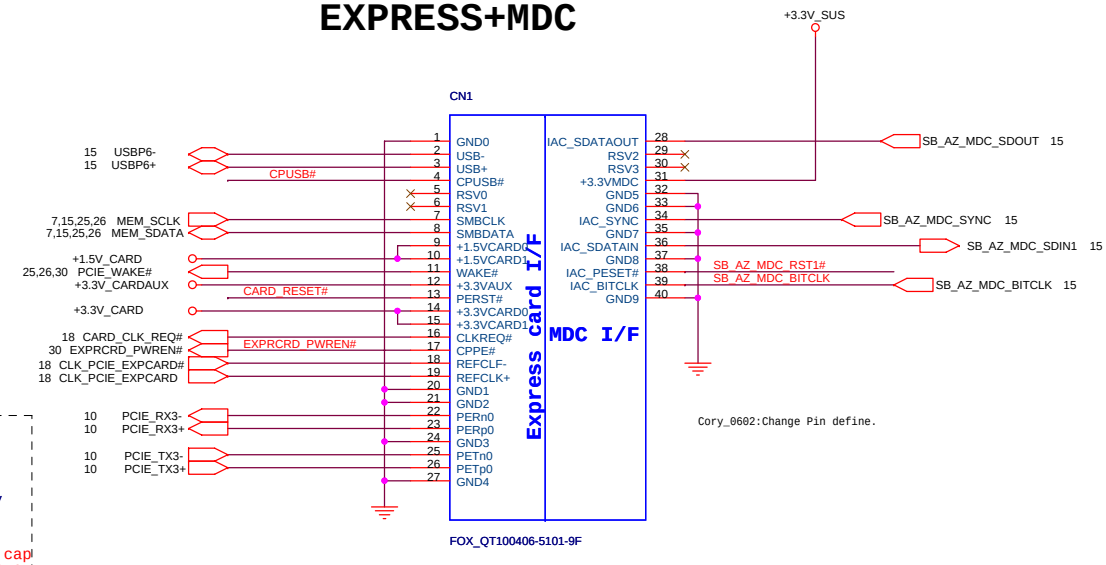




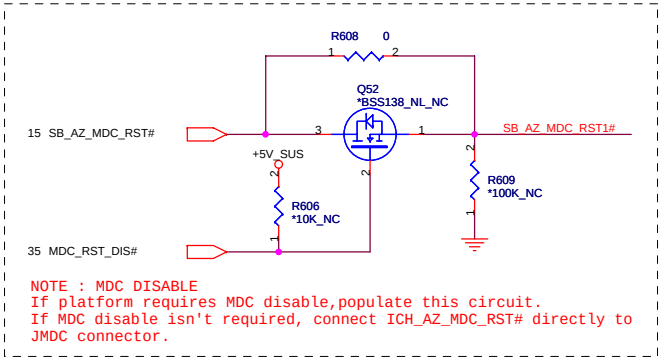


PCI-Express TX and RX direct to connector.

EXPRESS+MDC



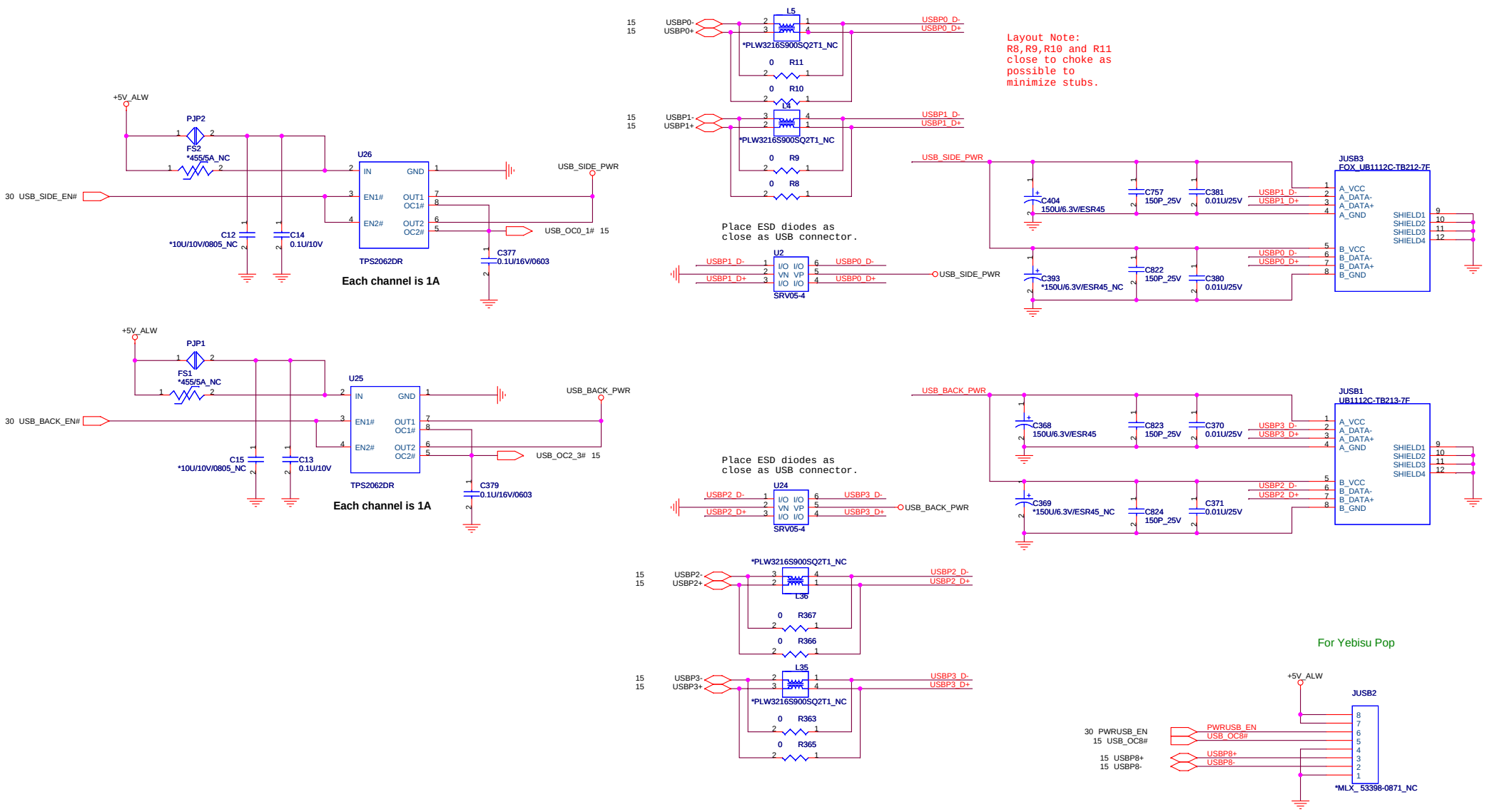
Cory_0602:Change Pin define.



NOTE : MDC DISABLE
If platform requires MDC disable,populate this circuit.
If MDC disable isn't required, connect ICH_AZ_MDC_RST# directly to JMDC connector.

QUANTA COMPUTER

Title	ExpressCard/SmartCard	
Size	Document Number FX5	Rev 0.1
Date: Friday, May 04, 2007	Sheet 27 of 61	



QUANTA COMPUTER

Title	USB & Flash	
Size	Document Number FX5	Rev 0.1
Date: Friday, May 04, 2007	Sheet 28 of 61	

MEC5025 EC-08
128 PIN VTQFP

USIO2

	GPIO4	GPIO5
Intel	0	0
AMD	0	1
TBD	1	0
Parker	1	1

Place these caps close to MEC5025.

Place close to pin 58.

Place cap close to pin 121.

Populate for flash corruption issue.

1 = Enabled.
0 = Disabled

Flash Recovery.

Low = Write Protected.

Flash Write Protect bottom 4K of internal bootblock flash.

Not Stuff 0 ohm when doing Flash recovery.

For MEC5025 Rev.C: C417=22uF and populate workaround circuit.
For MEC5025 Rev.D: C417=4.7uF and depopulate workaround circuit.

Debug Serial Port
Flash Recovery Port.

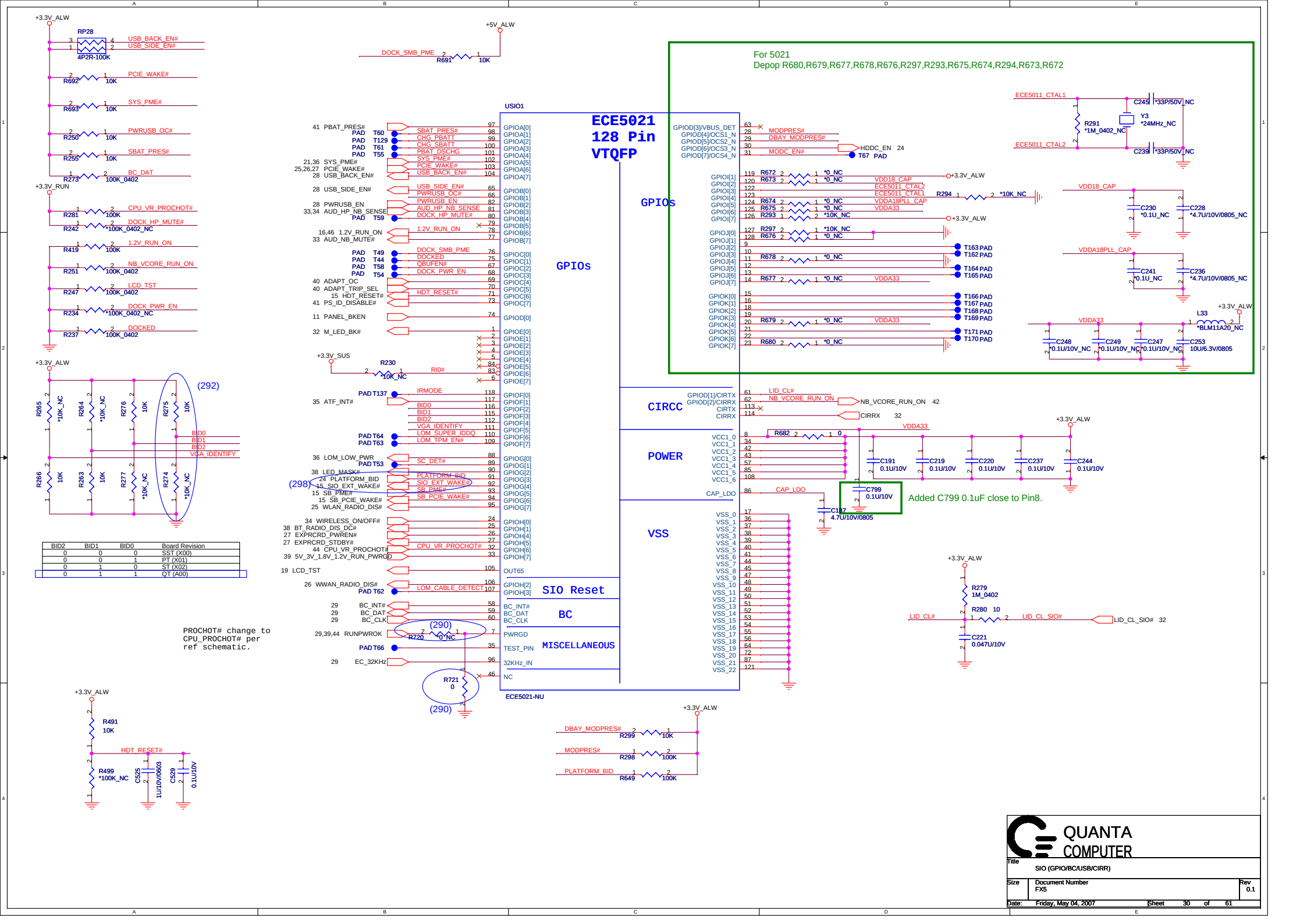
32KHz Clock.

External Work Around Circuit.

MEC5025
LQFP128-16X16-4-FX2
Rev 0.01 (11/09/05)

QUANTA COMPUTER

Title	Ultra I/O Controller MEC5025	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 29 of 61	


ECE5021
128 Pin
VTQFP
USIO1
GPIOs
GPIOs
CIRCC
POWER
VSS
SIO Reset
BC
MISCELLANEOUS
ECE5021-NU
For 5021
Depop R680,R679,R677,R678,R676,R297,R293,R675,R674,R294,R673,R672
Added C799 0.1uF close to Pin8.
PROCHOT# change to
CPU_PROCHOT# per
ref schematic.
QUANTA
COMPUTER
SIO (GPIO/BC/USB/CIRR)
FX5
Friday, May 04, 2007
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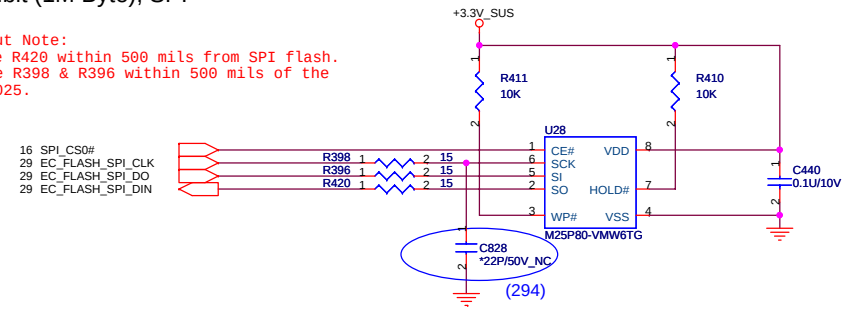
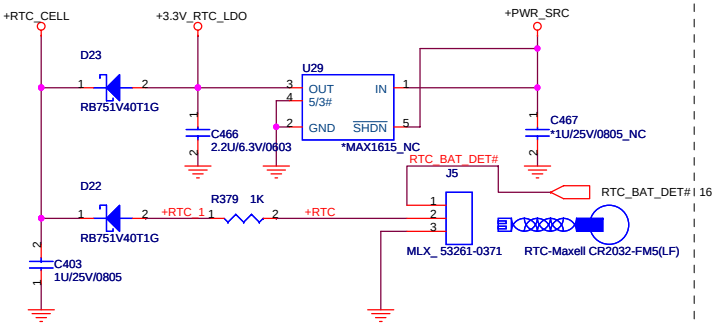
8Mbit (1M Byte), SPI

Layout Note:
Place R420 within 500 mils from SPI flash.
Place R398 & R396 within 500 mils of the MEC5025.



RTC BATTERY



QUANTA COMPUTER

Title	FLASH, RTC & KC	
Size	Document Number FX5	Rev 0.1
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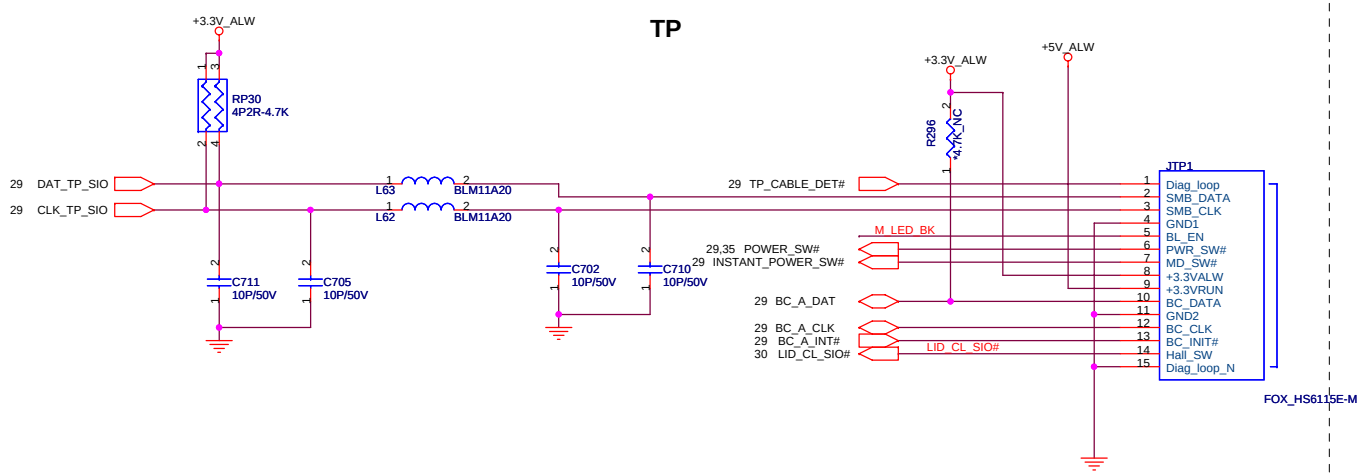
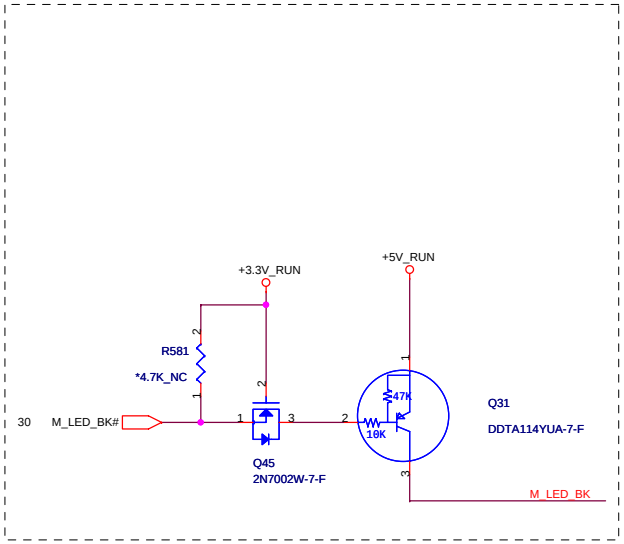
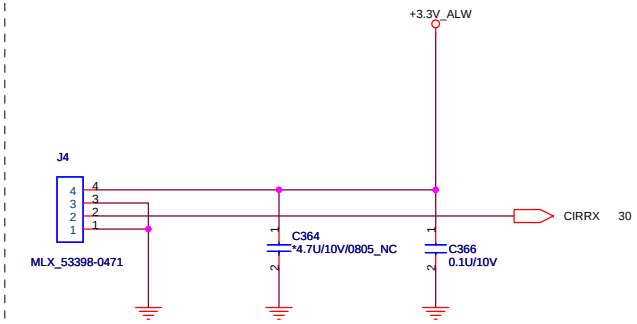
TP





CIR



QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number FX5	Rev 0.1
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INTERNAL SPEAKER AMP

AZALIA (HD) CODEC

Package 1206 for THD+N performance for Vista Logo requirements.

U23 MAX9789A TQFN 32PIN

U22 STAC9205 LQFP 48PIN

For TPA6040A,pop R642,depop R643.

Layout Note: Place close to pin 9.

Layout Note: Place close U23.

Layout Note: Place close to pin 18.

For TPA6040A,pop C775,depop R635.

For TPA6040A,pop C356,depop R357.

FB_60ohm+-25%_100MHz_3A_0.05ohm DC

EMI Request

GAIN2	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

For tuning.

Close to pin 6.

Close to pin 5.

Layout Note: Close to Pin 13.

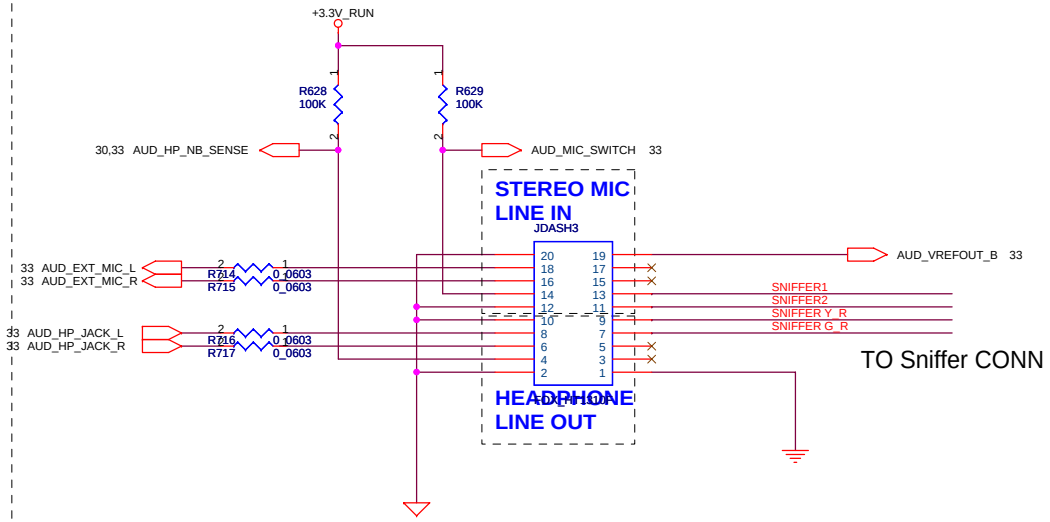
Close to U22.

will support QFN package.

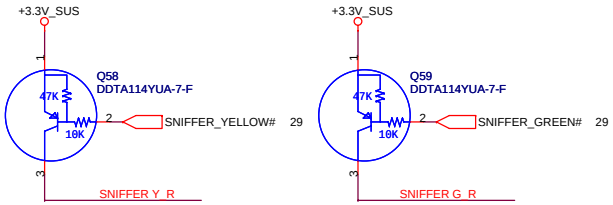
QUANTA COMPUTER

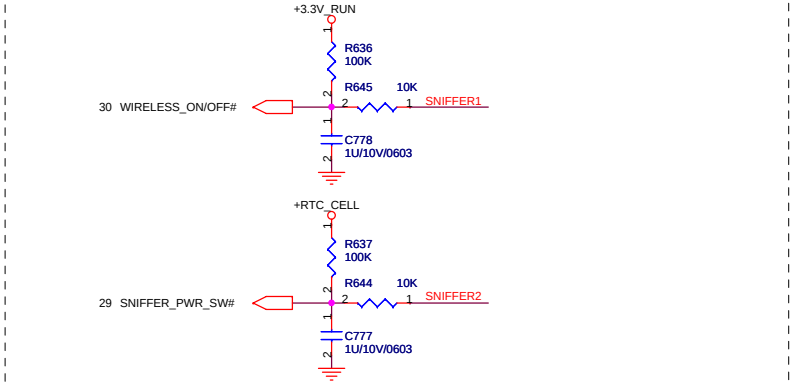
Title	Azelia CODEC(STAC9205)	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 33 of 61	

Audio Connect and Sniffer

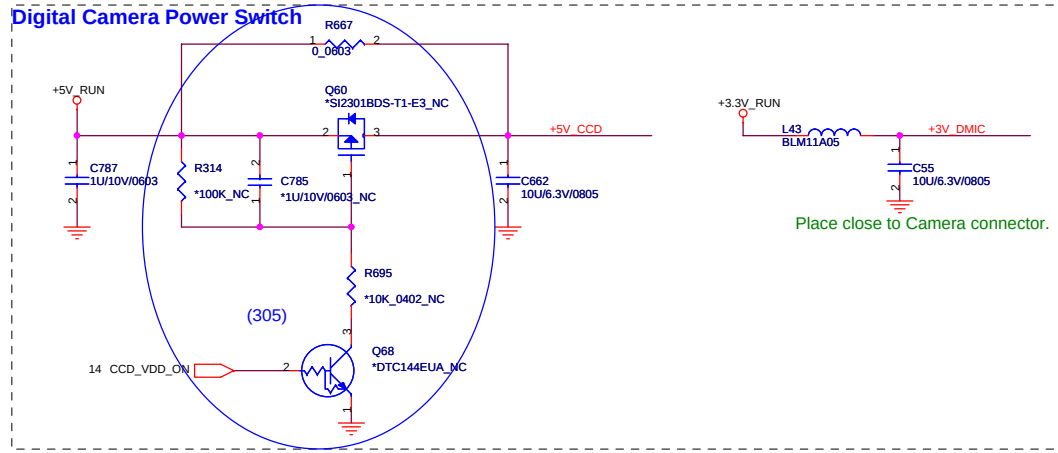


Sniffer LED

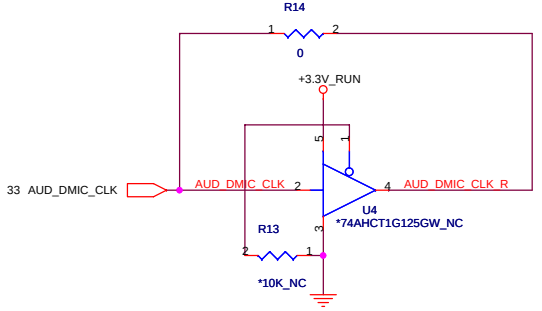


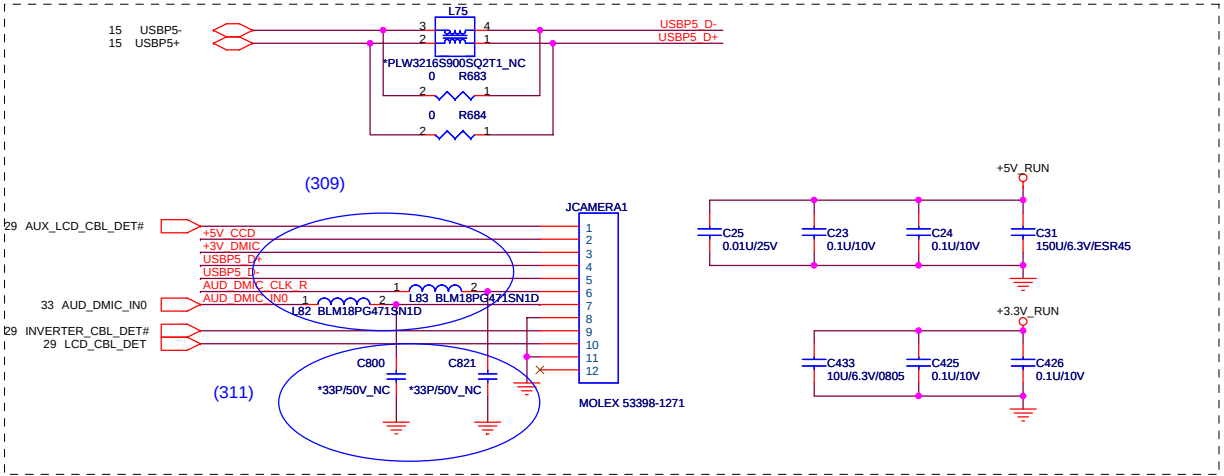


Digital Camera Power Switch



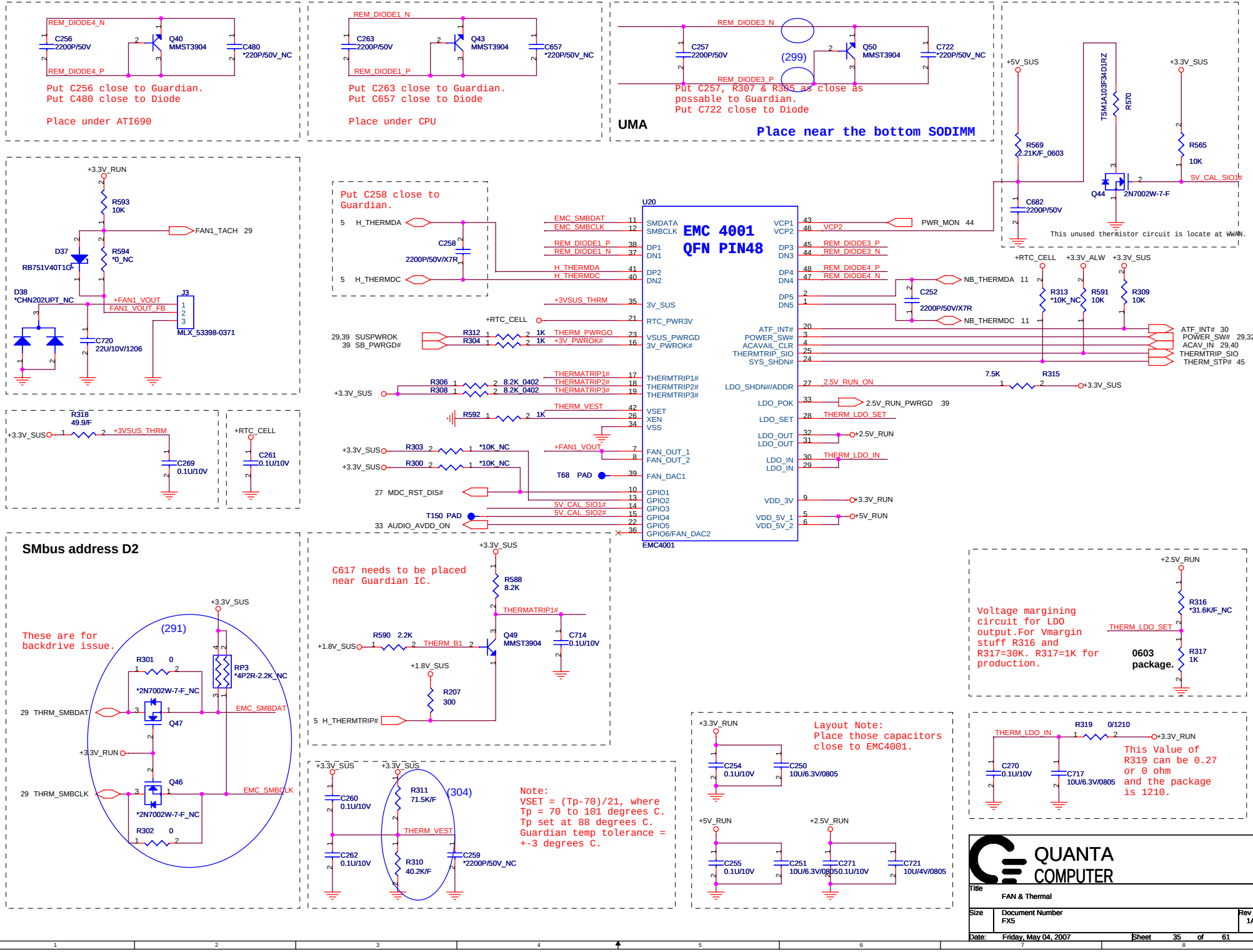
Place close to Camera connector.

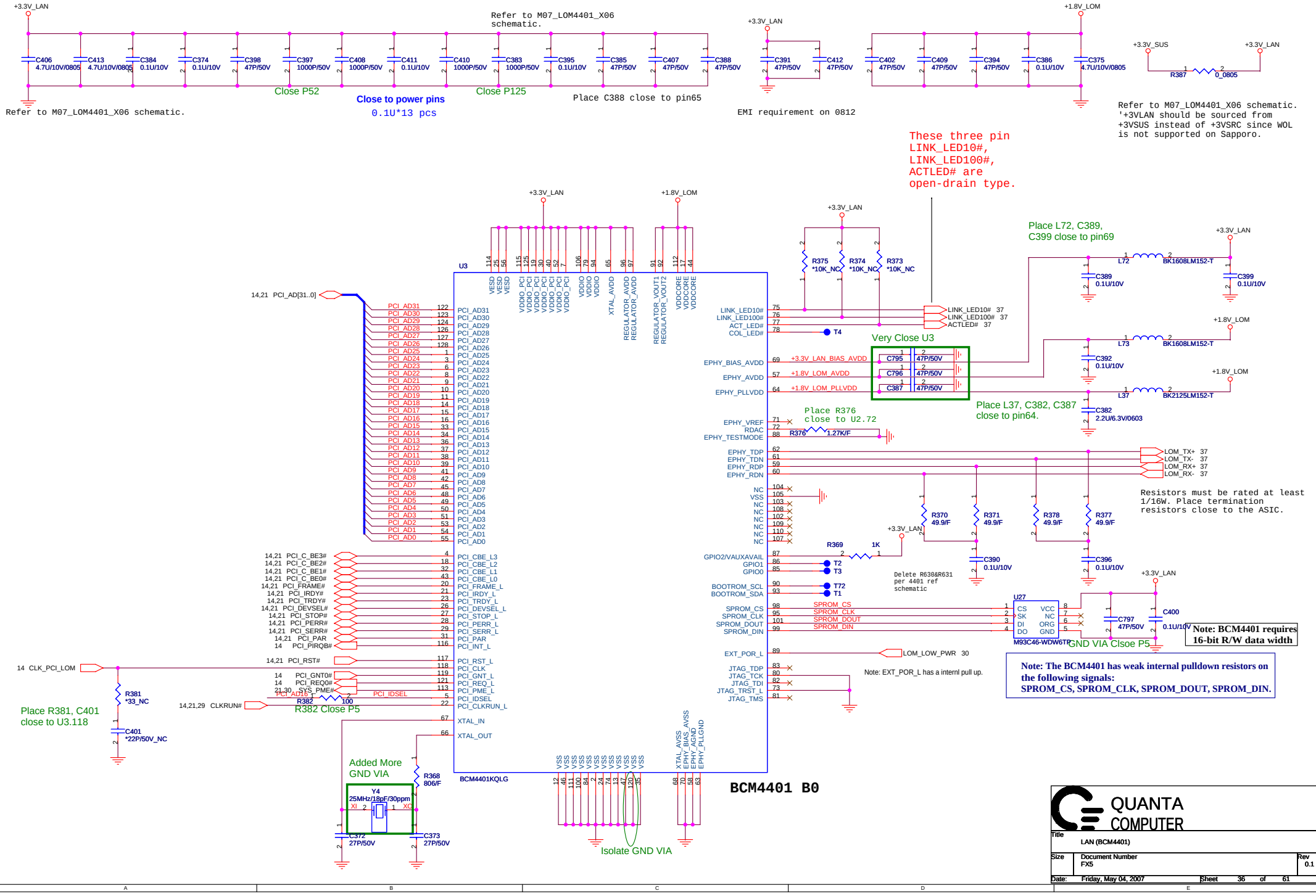




QUANTA COMPUTER

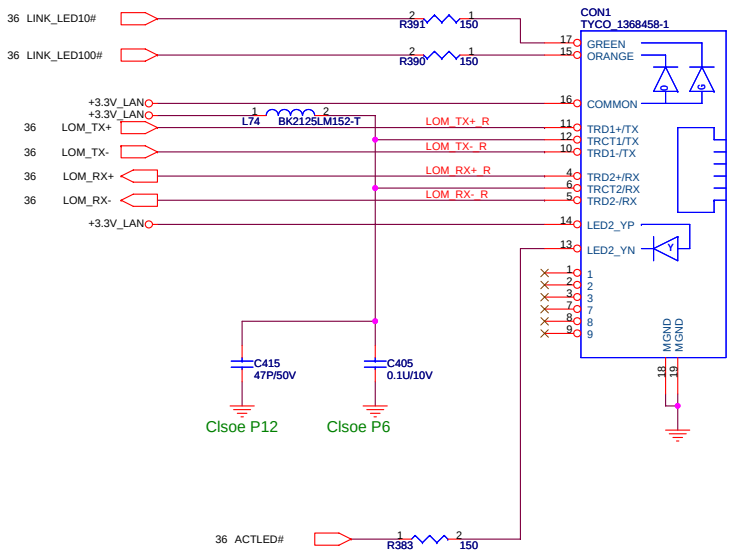
Title	AUDIO CONN Digital MIC/Camera	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 34 of 61	


REM_DIODE4_N
C256 2200P/50V
Q40 MMST3904
C480 *220P/50V_NC
REM_DIODE4_P
Put C256 close to Guardian.
Put C480 close to Diode
Place under ATI690
REM_DIODE1_N
C263 2200P/50V
Q43 MMST3904
C657 *220P/50V_NC
REM_DIODE1_P
Put C263 close to Guardian.
Put C657 close to Diode
Place under CPU
REM_DIODE3_N
C257 2200P/50V
(299)
Q50 MMST3904
C722 *220P/50V_NC
REM_DIODE3_P
Put C257, R307 & R335 as close as possable to Guardian.
Put C722 close to Diode
UMA
Place near the bottom SODIMM
+5V_SUS
TSM1A103F34D1RZ
R570
+3.3V_SUS
R569 2.21K/F_0603
R565 10K
5V_CAL_SIO1#
Q44 2N7002W-7-F
C682 2200P/50V
This unused thermistor circuit is locate at WWAN.
+3.3V_RUN
R593 10K
FAN1_TACH 29
D37 RB751V40T1G
R594 *0_NC
D38 *CHN202UPT_NC
+FAN1_VOUT
FAN1_VOUT_FB
J3
MLX_53398-0371
C720 22U/10V/1206
Put C258 close to Guardian.
5 H_THERMDA
C258 2200P/50V/X7R
5 H_THERMDC
U20
EMC 4001
QFN PIN48
EMC_SMBDAT
EMC_SMBCLK
REM_DIODE1_P
REM_DIODE1_N
H_THERMDA
H_THERMDC
+3VSUS_THRM
+RTC_CELL
29,39 SUSPWROK
39 SB_PWRGD#
R312 1K
R304 1K
THERM_PWRGO
+3V_PWROK#
SMDATA
SMBCLK
DP1
DN1
DP2
DN2
3V_SUS
RTC_PWR3V
VSUS_PWRGD
3V_PWROK#
VCP1
VCP2
PWR_MON 44
REM_DIODE3_P
REM_DIODE3_N
REM_DIODE4_P
REM_DIODE4_N
NB_THERMDA 11
NB_THERMDC 11
C252 2200P/50V/X7R
+RTC_CELL
+3.3V_ALW
+3.3V_SUS
R313 *10K_NC
R591 10K
R309 10K
ATF_INT# 30
POWER_SW# 29,32
ACAV_IN 29,40
THERM_STP# 45
ATF_INT#
POWER_SW#
ACAVAIL_CLR
THERMTRIP_SIO
SYS_SHDN#
R315 7.5K
2.5V_RUN_ON
+3.3V_SUS
LDO_SHDN#/ADDR
LDO_POK
2.5V_RUN_PWRGD 39
LDO_SET
THERM_LDO_SET
LDO_OUT
+2.5V_RUN
THERM_LDO_IN
R306 8.2K_0402
R308 8.2K_0402
THERMATRIP1#
THERMATRIP2#
THERMATRIP3#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
R592 1K
THERM_VEST
VSET
XEN
VSS
R303 *10K_NC
R300 *10K_NC
+FAN1_VOUT
FAN_OUT_1
FAN_OUT_2
T68 PAD
FAN_DAC1
27 MDC_RST_DIS#
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6/FAN_DAC2
5V_CAL_SIO1#
5V_CAL_SIO2#
T150 PAD
33 AUDIO_AVDD_ON
VDD_3V
VDD_5V_1
VDD_5V_2
+3.3V_RUN
+5V_RUN
EMC4001
R318 49.9/F
+3VSUS_THRM
C269 0.1U/10V
C261 0.1U/10V
SMbus address D2
(291)
These are for backdrive issue.
R301 0
RP3 *4P2R-2.2K_NC
*2N7002W-7-F_NC
29 THRM_SMBDAT
EMC_SMBDAT
Q47
29 THRM_SMBCLK
EMC_SMBCLK
Q46
R302 0
C617 needs to be placed near Guardian IC.
R588 8.2K
THERMATRIP1#
+1.8V_SUS
R590 2.2K
THERM_B1
Q49 MMST3904
C714 0.1U/10V
R207 300
5 H_THERMTRIP#
C260 0.1U/10V
C262 0.1U/10V
R311 71.5K/F
(304)
THERM_VEST
R310 40.2K/F
C259 *2200P/50V_NC
Note:
VSET = (Tp-70)/21, where
Tp = 70 to 101 degrees C.
Tp set at 88 degrees C.
Guardian temp tolerance = +-3 degrees C.
Layout Note:
Place those capacitors close to EMC4001.
C254 0.1U/10V
C250 10U/6.3V/0805
C255 0.1U/10V
C251 10U/6.3V/0805
C271 0.1U/10V
C721 10U/4V/0805
Voltage margining circuit for LDO output.For Vmargin stuff R316 and R317=30K. R317=1K for production.
R316 *31.6K/F_NC
R317 1K
0603 package.
R319 0/1210
C270 0.1U/10V
C717 10U/6.3V/0805
This Value of R319 can be 0.27 or 0 ohm and the package is 1210.
QUANTA COMPUTER
Title
FAN & Thermal
Size
Document Number
FX5
Rev
1A
Date: Friday, May 04, 2007
Sheet 35 of 61



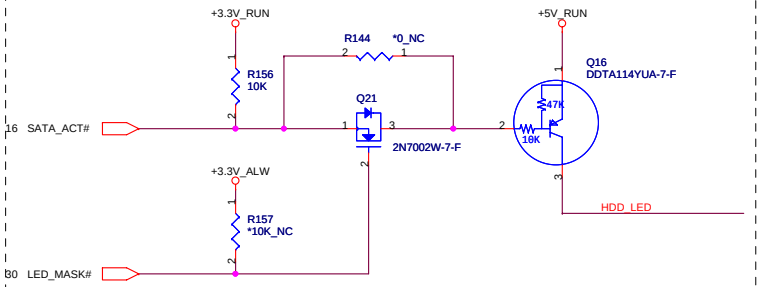
QUANTA COMPUTER

Title	LAN (BCM4401)	
Size	Document Number FX5	Rev 0.1
Date: Friday, May 04, 2007	Sheet 36 of 61	

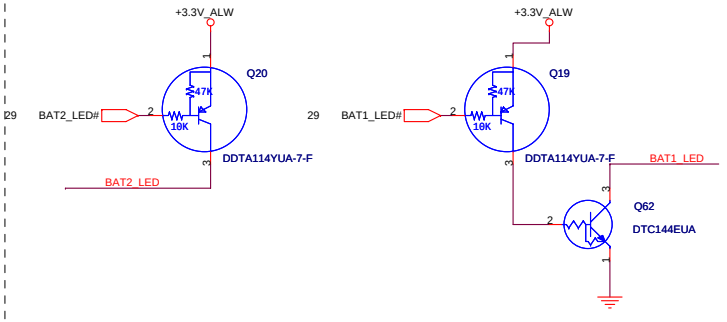


Title	LAN Jack	
Size	Document Number FX5	Rev 0.1
Date: Friday, May 04, 2007	Sheet 37 of 61	

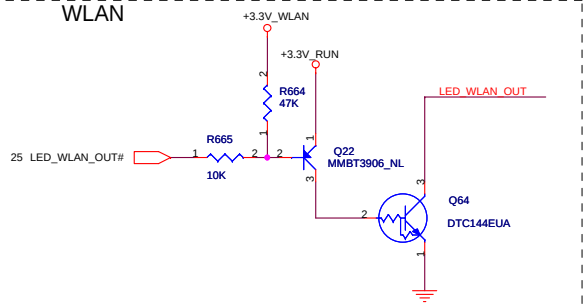
HDD activity LED.



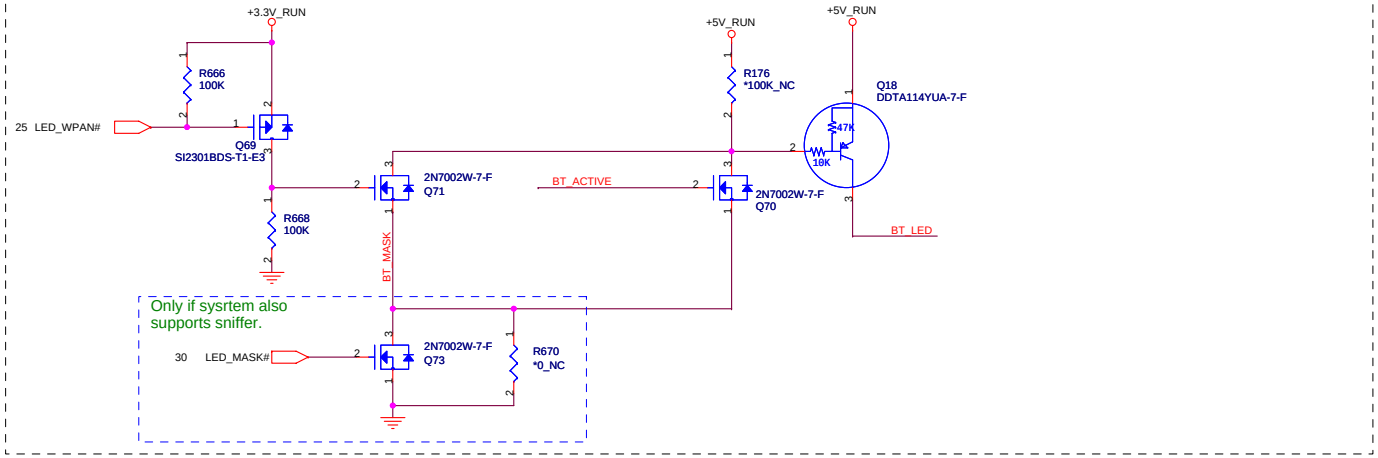
Battery status.



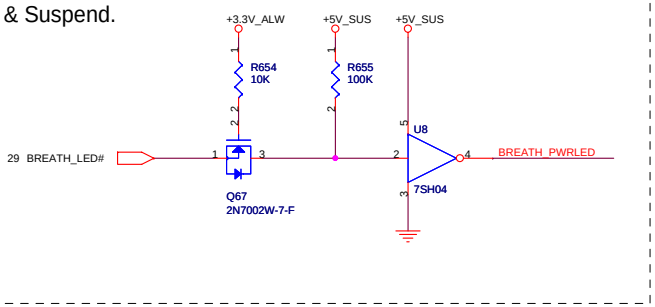
WLAN



BT

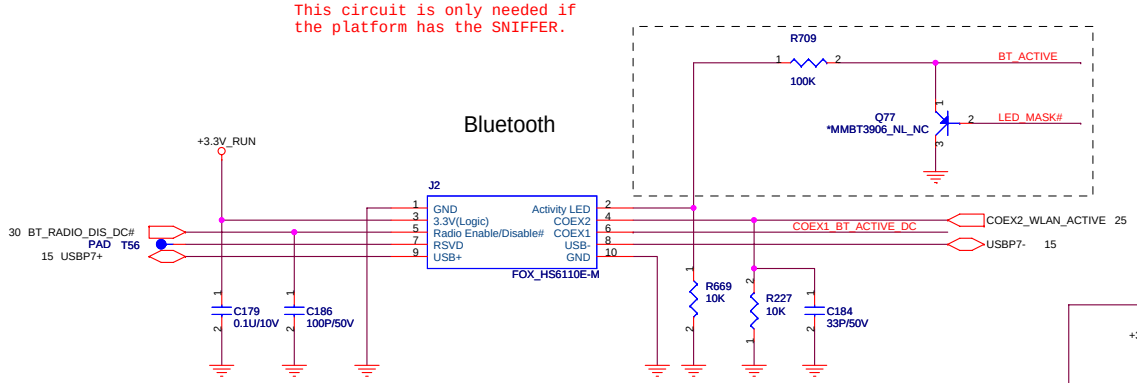


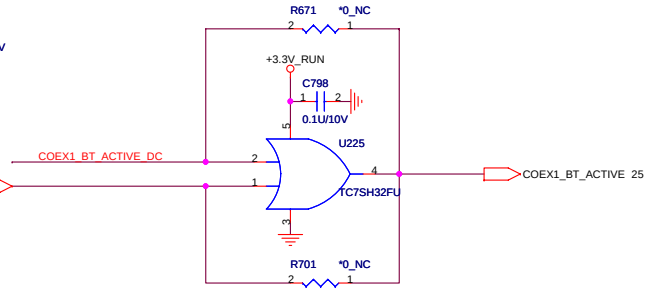
Power & Suspend.

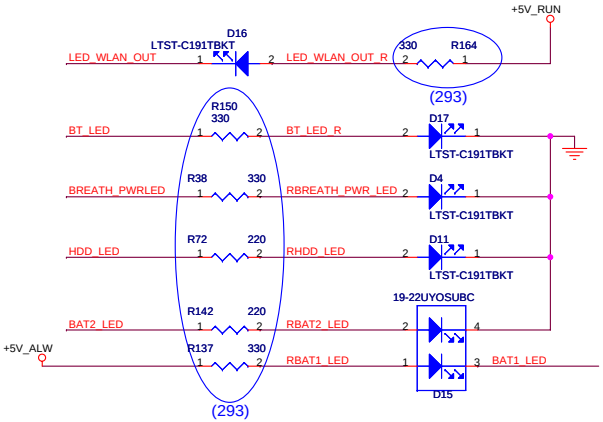


This circuit is only needed if the platform has the SNIFFER.

Bluetooth

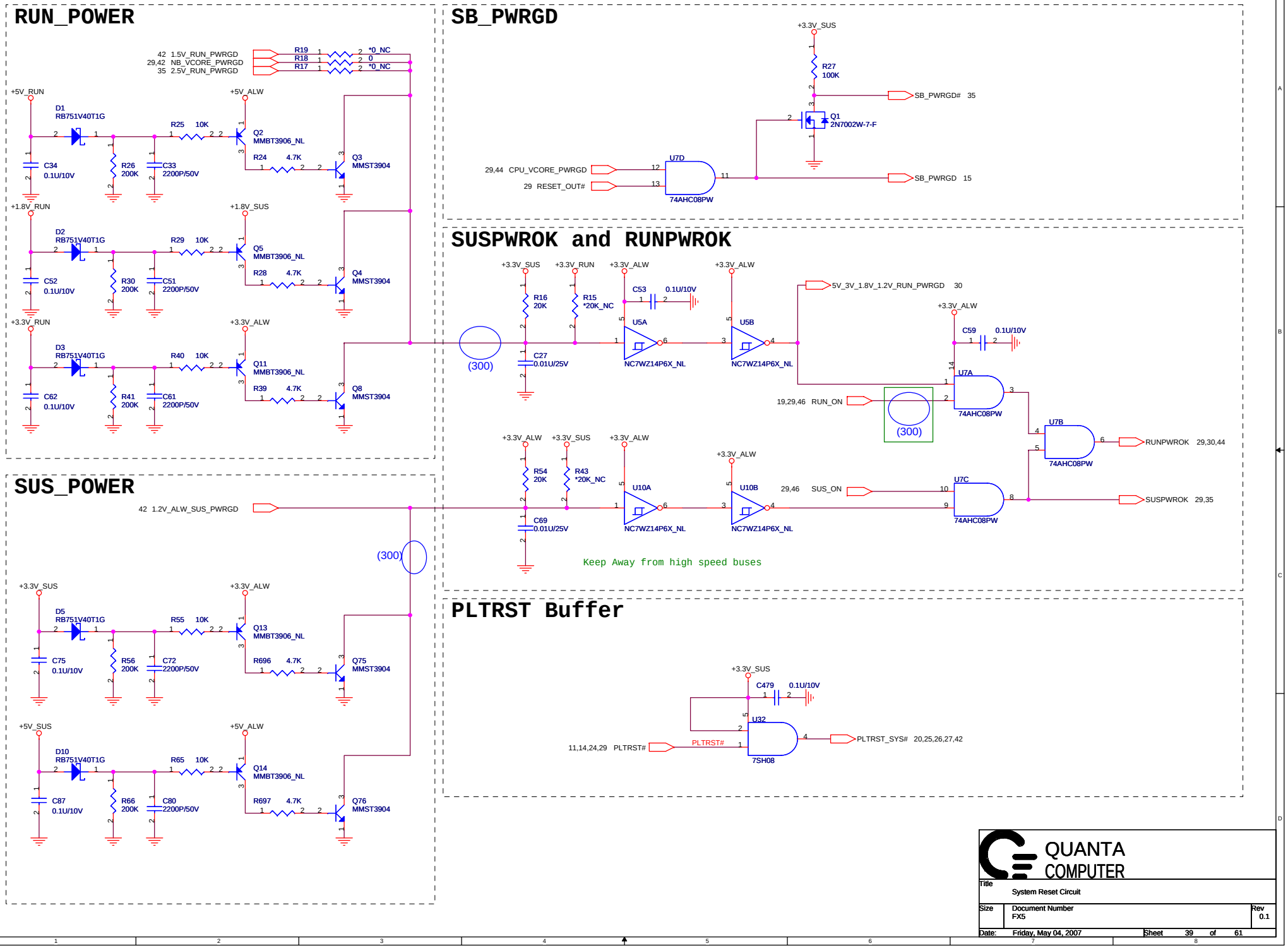






QUANTA COMPUTER

Title	SWITCH & LED	
Size	Document Number FX5	Rev 0.1
Date: Friday, May 04, 2007	Sheet 38 of 61	


RUN_POWER
42 1.5V_RUN_PWRGD
29,42 NB_VCORE_PWRGD
35 2.5V_RUN_PWRGD
R19 *0_NC
R18 0
R17 *0_NC
+5V_RUN
+5V_ALW
D1 RB751V40T1G
R25 10K
Q2 MMBT3906_NL
R24 4.7K
Q3 MMST3904
C34 0.1U/10V
R26 200K
C33 2200P/50V
+1.8V_RUN
+1.8V_SUS
D2 RB751V40T1G
R29 10K
Q5 MMBT3906_NL
R28 4.7K
Q4 MMST3904
C52 0.1U/10V
R30 200K
C51 2200P/50V
+3.3V_RUN
+3.3V_ALW
D3 RB751V40T1G
R40 10K
Q11 MMBT3906_NL
R39 4.7K
Q8 MMST3904
C62 0.1U/10V
R41 200K
C61 2200P/50V
SUS_POWER
42 1.2V_ALW_SUS_PWRGD
(300)
+3.3V_SUS
+3.3V_ALW
D5 RB751V40T1G
R55 10K
Q13 MMBT3906_NL
R696 4.7K
Q75 MMST3904
C75 0.1U/10V
R56 200K
C72 2200P/50V
+5V_SUS
+5V_ALW
D10 RB751V40T1G
R65 10K
Q14 MMBT3906_NL
R697 4.7K
Q76 MMST3904
C87 0.1U/10V
R66 200K
C80 2200P/50V
SB_PWRGD
+3.3V_SUS
R27 100K
SB_PWRGD# 35
Q1 2N7002W-7-F
29,44 CPU_VCORE_PWRGD
29 RESET_OUT#
U7D
74AHC08PW
SB_PWRGD 15
SUSPWROK and RUNPWROK
+3.3V_SUS
+3.3V_RUN
+3.3V_ALW
R16 20K
R15 *20K_NC
C53 0.1U/10V
U5A
U5B
NC7WZ14P6X_NL
C27 0.01U/25V
5V_3V_1.8V_1.2V_RUN_PWRGD 30
C59 0.1U/10V
U7A
74AHC08PW
19,29,46 RUN_ON
U7B
RUNPWROK 29,30,44
SUSPWROK 29,35
R54 20K
R43 *20K_NC
U10A
U10B
29,46 SUS_ON
U7C
C69 0.01U/25V
Keep Away from high speed buses
PLTRST Buffer
C479 0.1U/10V
U32
7SH08
11,14,24,29 PLTRST#
PLTRST_SYS# 20,25,26,27,42
QUANTA COMPUTER
Title
System Reset Circuit
Size
Document Number
FX5
Rev
0.1
Date: Friday, May 04, 2007
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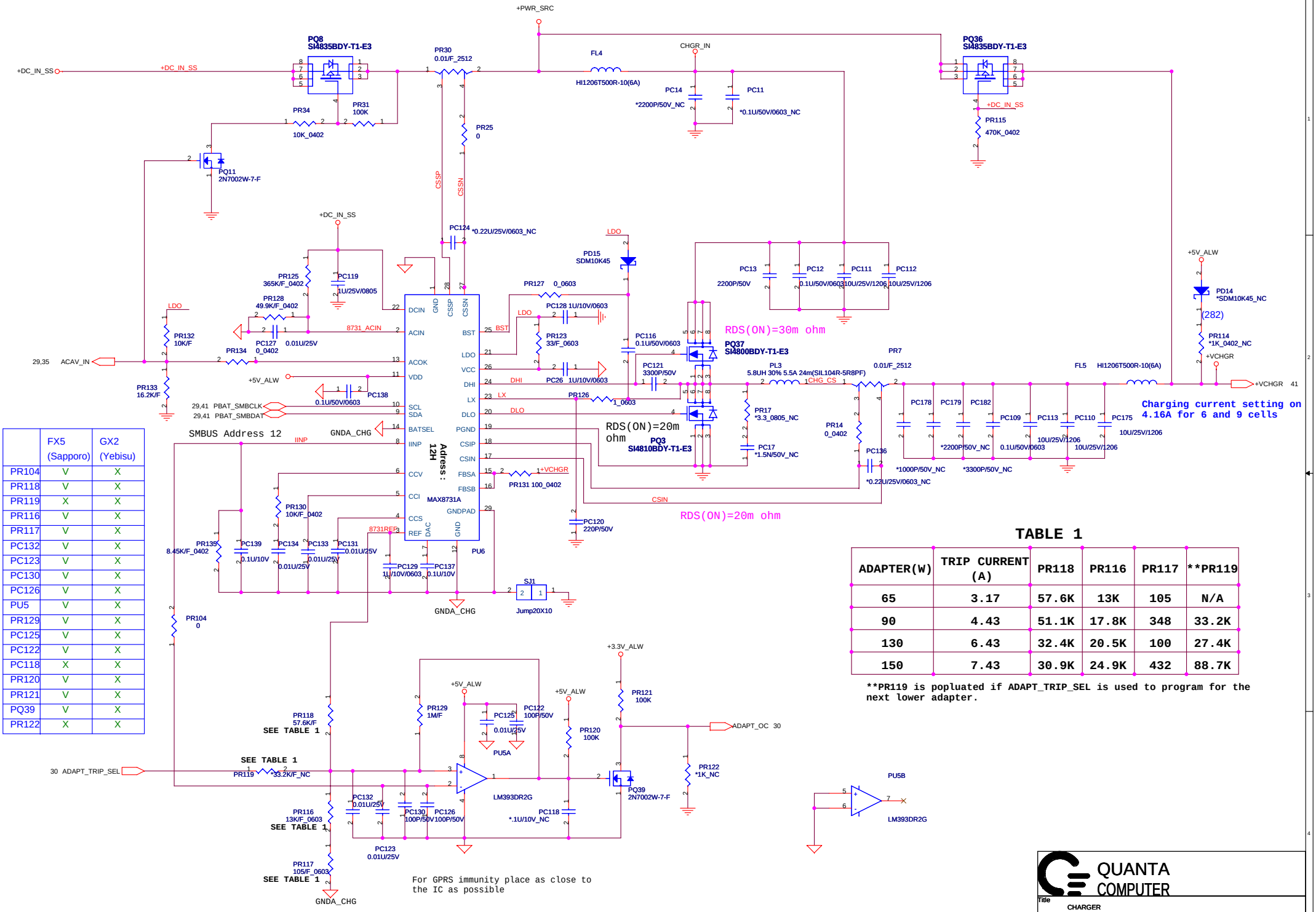


	FX5 (Sapporo)	GX2 (Yebisu)
PR104	V	X
PR118	V	X
PR119	X	X
PR116	V	X
PR117	V	X
PR132	V	X
PR123	V	X
PC130	V	X
PC126	V	X
PU5	V	X
PR129	V	X
PC125	V	X
PC122	V	X
PR118	X	X
PR120	V	X
PR121	V	X
PQ39	V	X
PR122	X	X

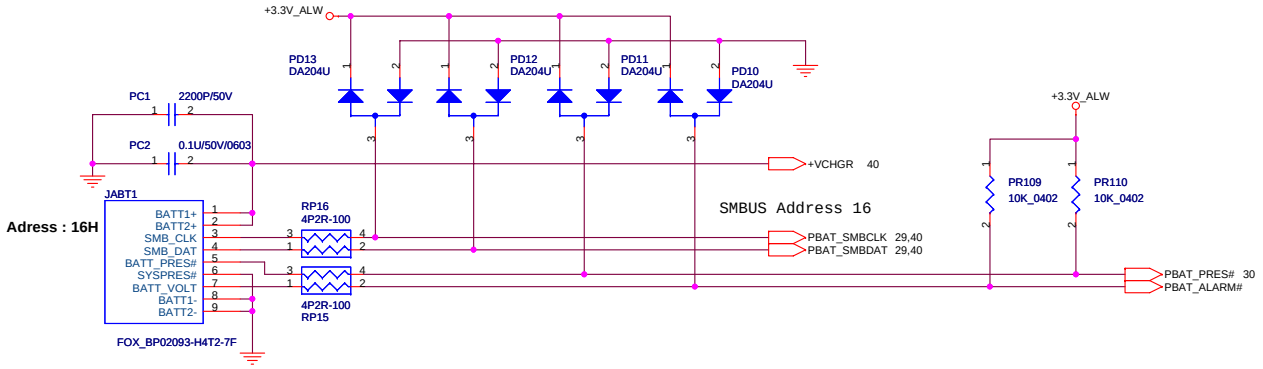
TABLE 1

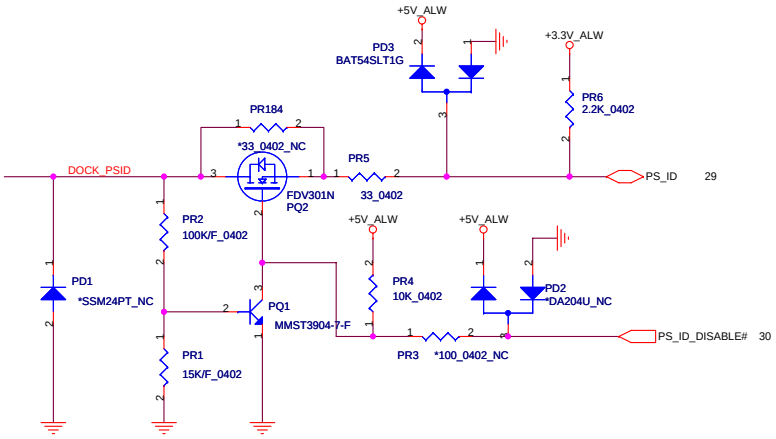
ADAPTER(W)	TRIP CURRENT (A)	PR118	PR116	PR117	**PR119
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

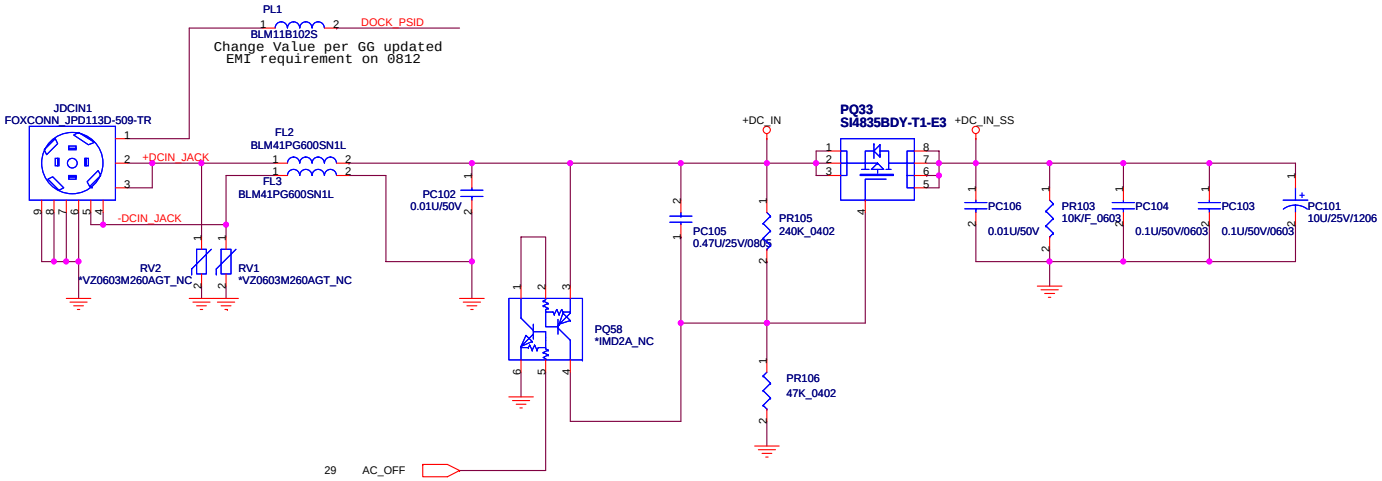
**PR119 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

QUANTA COMPUTER

Title	CHARGER	
Size	Document Number FX5	Rev 1A
Date: 2005/4/21	Sheet 40 of 61	

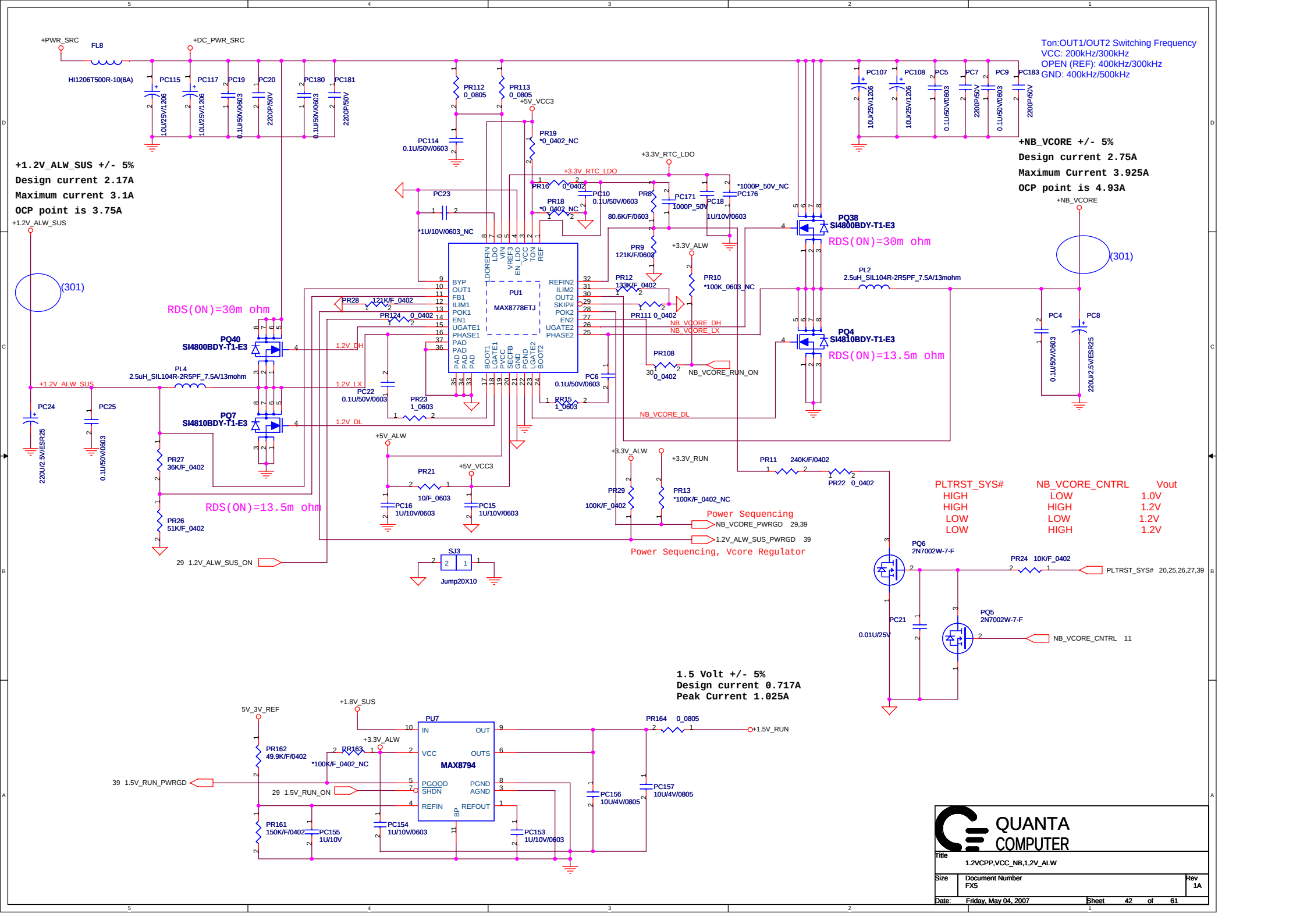




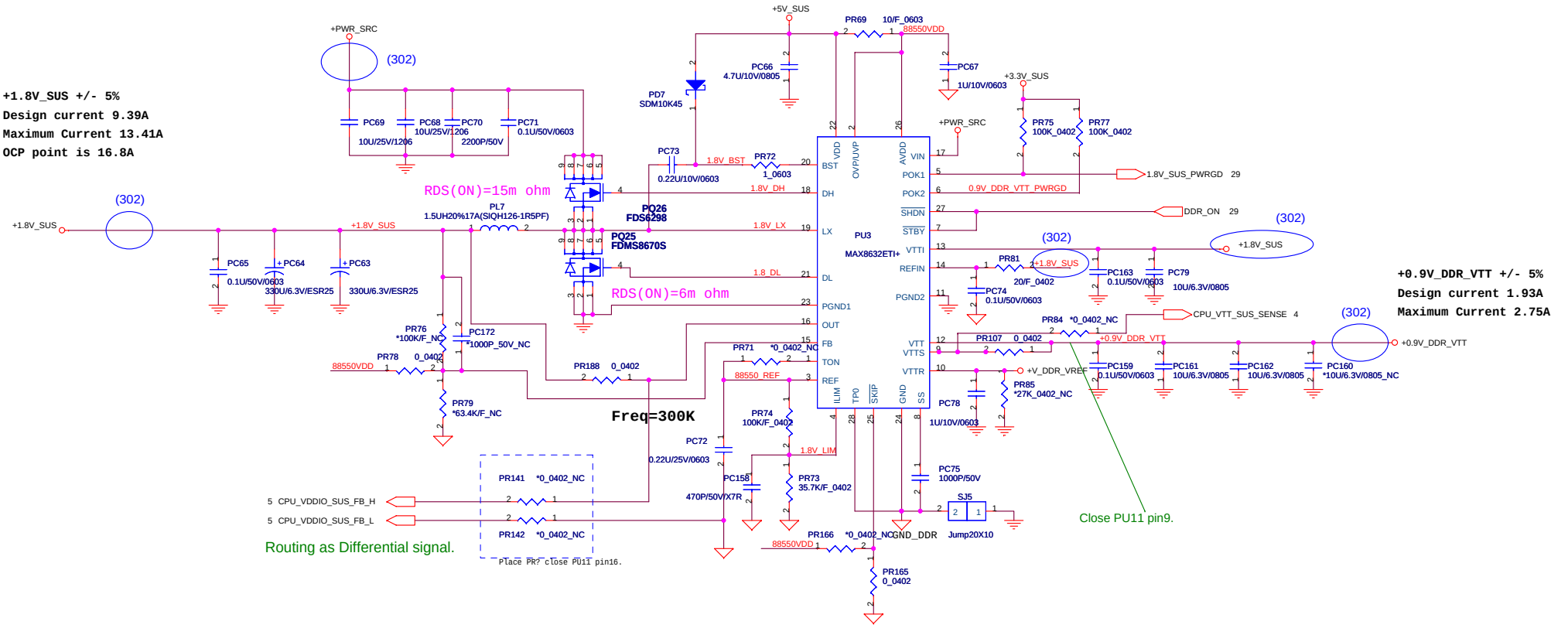


QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number FX5	Rev 1A
Date: 2005/4/21	Sheet 41 of 61	


Ton:OUT1/OUT2 Switching Frequency
VCC: 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz
+1.2V_ALW_SUS +/- 5%
Design current 2.17A
Maximum current 3.1A
OCP point is 3.75A
+NB_VCORE +/- 5%
Design current 2.75A
Maximum Current 3.925A
OCP point is 4.93A
RDS(ON)=30m ohm
RDS(ON)=13.5m ohm
MAX8778ETJ
PU1
PQ38 SI4800BDY-T1-E3
PQ4 SI4810BDY-T1-E3
PQ40 SI4800BDY-T1-E3
PQ7 SI4810BDY-T1-E3
PL2 2.5uH_SIL104R-2R5PF_7.5A/13mohm
PL4 2.5uH_SIL104R-2R5PF_7.5A/13mohm
PLTRST_SYS# NB_VCORE_CNTRL Vout
HIGH LOW 1.0V
HIGH HIGH 1.2V
LOW LOW 1.2V
LOW HIGH 1.2V
Power Sequencing
Power Sequencing, Vcore Regulator
1.5 Volt +/- 5%
Design current 0.717A
Peak Current 1.025A
MAX8794
PU7
QUANTA COMPUTER
1.2VCPP,VCC_NB,1,2V_ALW
FX5
Friday, May 04, 2007
Sheet 42 of 61

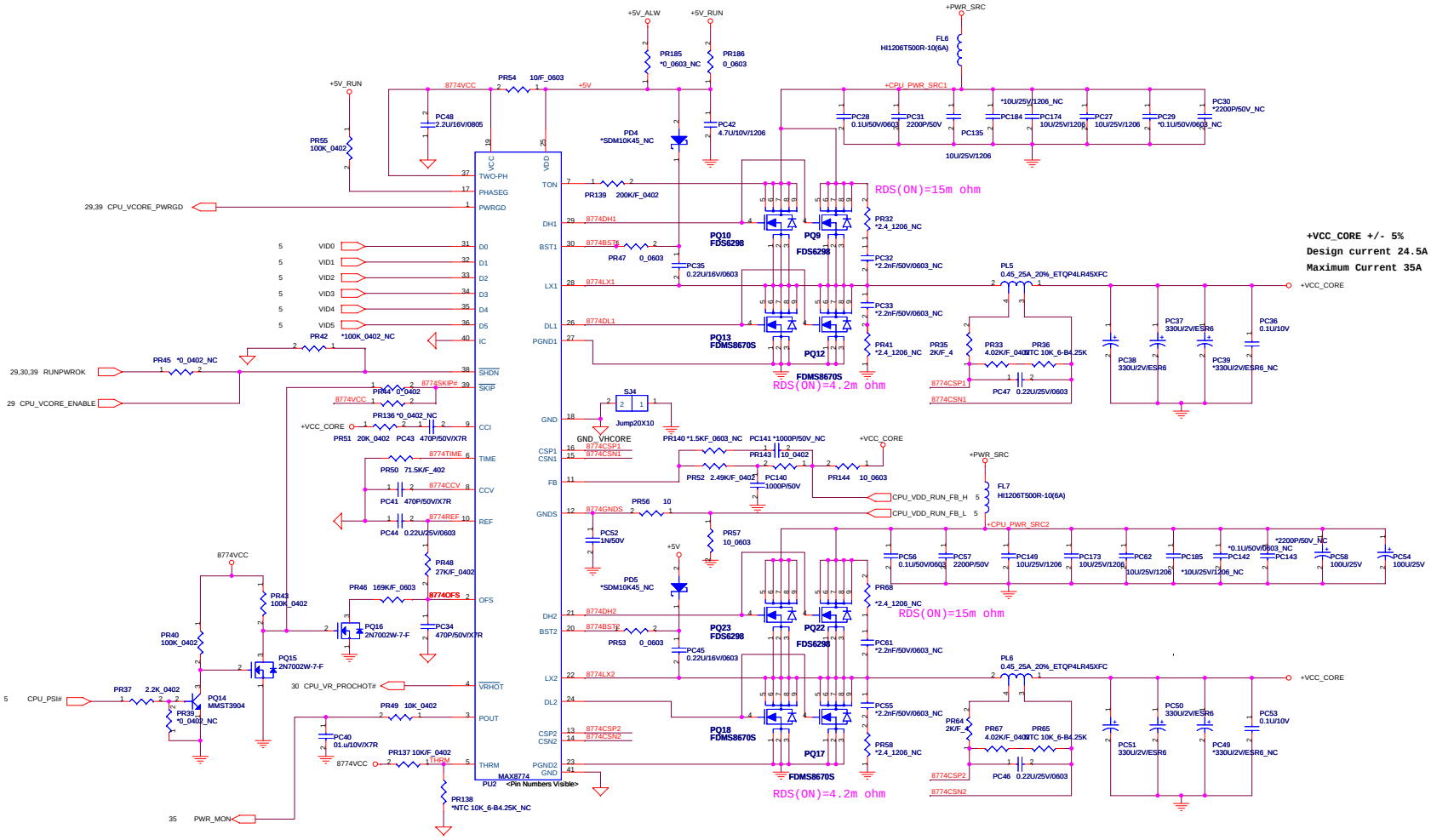
+1.8V_SUS +/- 5%
Design current 9.39A
Maximum Current 13.41A
OCP point is 16.8A



+0.9V_DDR_VTT +/- 5%
Design current 1.93A
Maximum Current 2.75A

QUANTA COMPUTER

Title	1.8V_SUS,1.5V_RUN,0.9V_VTT	
Size	Document Number FX5	Rev 3A
Date: 2005/4/21	Sheet 43 of 61	



D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	0	1	1	1	1.3750V
0	0	1	0	0	0	1.3500V
0	0	1	0	0	1	1.3250V
0	0	1	0	1	0	1.3000V
0	0	1	0	1	1	1.2750V
0	0	1	1	0	0	1.2500V
0	0	1	1	0	1	1.2250V
0	0	1	1	1	0	1.2000V
0	0	1	1	1	1	1.1750V
0	1	0	0	0	0	1.1500V
0	1	0	0	0	1	1.1250V
0	1	0	0	1	0	1.1000V
0	1	0	0	1	1	1.0750V
0	1	0	1	0	0	1.0500V
0	1	0	1	0	1	1.0250V
0	1	0	1	1	0	1.0000V
0	1	0	1	1	1	0.9750V
0	1	1	0	0	0	0.9500V
0	1	1	0	0	1	0.9250V
0	1	1	0	1	0	0.9000V
0	1	1	0	1	1	0.8750V
0	1	1	1	0	0	0.8500V
0	1	1	1	0	1	0.8250V
0	1	1	1	1	0	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7625V
1	0	0	0	0	1	0.7500V
1	0	0	0	1	0	0.7375V
1	0	0	0	1	1	0.7250V
1	0	0	1	0	0	0.7125V
1	0	0	1	0	1	0.7000V
1	0	0	1	1	0	0.6875V
1	0	0	1	1	1	0.6750V
1	0	1	0	0	0	0.6625V
1	0	1	0	0	1	0.6500V
1	0	1	0	1	0	0.6375V
1	0	1	0	1	1	0.6250V
1	0	1	1	0	0	0.6125V
1	0	1	1	0	1	0.6000V
1	0	1	1	1	0	0.5875V
1	0	1	1	1	1	0.5750V
1	1	0	0	0	0	0.5625V
1	1	0	0	0	1	0.5500V
1	1	0	0	1	0	0.5375V
1	1	0	0	1	1	0.5250V
1	1	0	1	0	0	0.5125V
1	1	0	1	0	1	0.5000V
1	1	0	1	1	0	0.4875V
1	1	0	1	1	1	0.4750V
1	1	1	0	0	0	0.4625V
1	1	1	0	0	1	0.4500V
1	1	1	0	1	0	0.4375V
1	1	1	0	1	1	0.4250V
1	1	1	1	0	0	0.4125V
1	1	1	1	0	1	0.4000V
1	1	1	1	1	0	0.3875V
1	1	1	1	1	1	0.3750V

QUANTA COMPUTER

Title	VHCORE (MAX8774)	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 44 of 61	

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

Place these CAPs close to FETs

Ton:OUT1/OUT2 Switching Frequency
VCC: 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

No Install for ISL6236
Install 10 ohm for MAX8778

Place these CAPs close to FETs

5 Volt +/- 5%

Design Current: 7.34 A
Maximum current:10.49A
OCP point is 13.1A

3.3 Volt +/- 5%
Design Current:7.98A
Maximum current:11.4A
OCP point is 13.8A

RDS(ON)=17m ohm

RDS(ON)=7.25m ohm

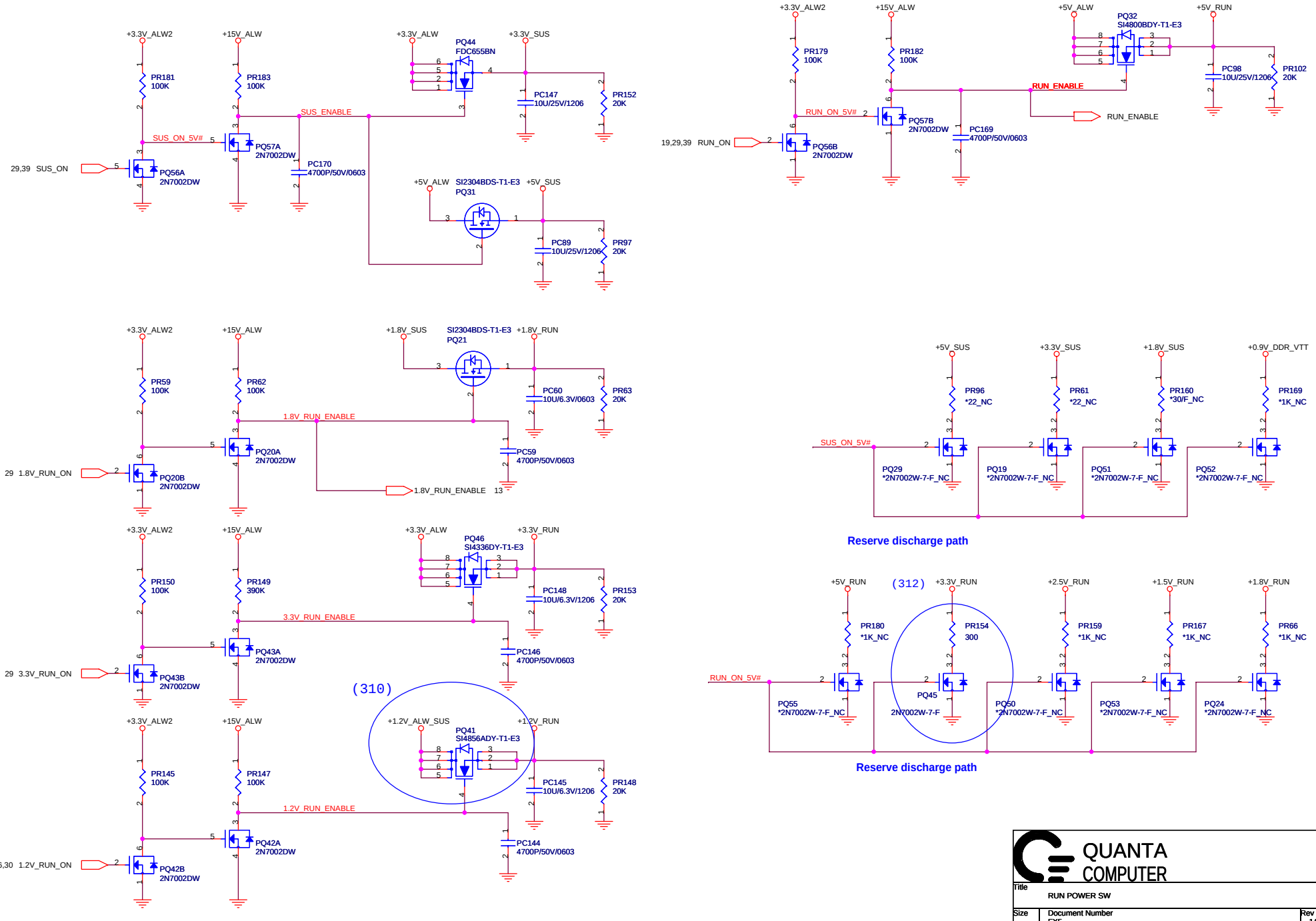
For DELL MO8 schematic (94)

LDO = 5V (LDOREFIN = GND) or
LDOREFIN RANGE: 0.3V to 2V
LDO = 2x LDOREFIN

REFIN2: DYNAMIC 0 to 2V
REFIN2 = RTC: 1.05V Fixed
REFIN2 = VCC: 3.3V Fixed

Title	3VALW,5V,3V, power on
Size	Document Number FX5
Rev	1A
Date:	Friday, May 04, 2007
Sheet	45 of 61

QUANTA COMPUTER



QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number FX5	Rev 1A
Date: Friday, May 04, 2007	Sheet 46 of 61	

PV5 FDJM6003 GND
PV4 FDJM6003 GND
PV3 FDJM6003 GND
PV2 FDJM6003 GND
PV1 FDJM6003 GND
PV7 *FDJM6003_NC GND
PV8 FDJM6003 GND
PV6 *FDJM6003_NC GND
PV9 FDJM6003 GND
PV10 FDJM6003 GND
PV11 FDJM6003 GND

TH6 H-TC354BE354X354D126P2-4
TH5 H-TC217BE354X354D126P2-4
TH4 H-TC256BE354X354D126P2-4
TH1 H-E354X354D126P2-4
TH2 H-TC217BC236D126P2-4
TH3 H-E354X354D126P2-4
TH16 H-TC354BE354X354D126P2-4
TH21 H-TC354BE354X354D126P2-4
TH22 H-E354X354D126P2-4
TH15 H-TC236BE354X354D126P2-4
TH12 H-TC217BC256D126P2-4
TH11 H-E276X315D126P2-4
TH13 H-TC315BC236D102P2-4
TH9 H-TC315BC236D102p2-4
TH10 H-TC315BC236D102P2-4
TH14 H-TC315BC236D102P2-4
TH8 H-TC217BC256D126P2-4
TH7 H-TC217BC256D126P2-4

+PWR_SRC C703 0.1U/50V/0603 +5V_ALW
+DC_IN_SS C376 0.1U/50V/0603 +3.3V_RUN
+DC_IN_SS C414 0.1U/50V/0603 +1.8V_MEM_VDDQ
+DC_IN_SS C41 0.1U/50V/0603 +NB_CORE
+DC_IN_SS C457 0.1U/50V/0603
+PWR_SRC C78 0.1U/50V/0603 +NB_CORE
+PWR_SRC C91 0.1U/50V/0603 +DC_IN_SS
+PWR_SRC C470 0.1U/50V/0603 +VCC_CORE

+VCC_CORE C548 *0.1U/50V/0603_NC +PWR_SRC
+PWR_SRC C751 0.1U/50V/0603
+PWR_SRC C767 0.1U/50V/0603 +5V_ALW
+PWR_SRC C752 *0.1U/50V/0603_NC

TH23 H-R63X126DR24X87P2
TH24 H-Re36X107D16X87P2
TH25 H-Re36X107D16X87P2
LAN

TH26 H-Re36X107D16X87P2
TH27 H-Re36X107D16X87P2
CLOCK

+1.5V_RUN C753 *0.1U/10V_NC
+1.5V_RUN C275 *0.1U/10V_NC
+1.5V_RUN C222 *0.1U/10V_NC
+1.5V_RUN C147 *0.1U/10V_NC

+1.8V_RUN C666 *0.1U/10V_NC +1.2V_RUN
+3.3V_ALW C708 0.1U/10V
+1.2V_ALW_SUS C207 0.1U/10V +1.2V_RUN
+5V_ALW C774 0.1U/10V +5V_RUN
+VCC_CORE C654 0.1U/10V
+3.3V_RUN C701 0.1U/10V +5V_ALW

+3.3V_SUS C246 *0.1U/10V_NC +5V_ALW
+3.3V_SUS C17 *0.1U/10V_NC +5V_ALW
+1.2V_RUN C215 *0.1U/10V_NC +3.3V_RUN
+3.3V_RUN C507 *0.1U/10V_NC +3.3V_SB_R
+1.8V_MEM_VDDQ C48 *0.1U/10V_NC +3.3V_RUN
+3.3V_ALW_R C448 *0.1U/10V_NC +3.3V_RUN

+3.3V_SB_R C631 *0.1U/10V_NC +1.2V_VCC_SB_R
+1.2V_VCC_SB_R C646 *0.1U/10V_NC +3.3V_SB_R
+3.3V_SB_R C633 *0.1U/10V_NC +1.2V_RUN
+1.2V_RUN C643 *0.1U/10V_NC +3.3V_RUN

+DC_IN C378 *0.1U/50V/0603_NC

+PWR_SRC C754 0.1U/50V/0603
+PWR_SRC C723 0.1U/50V/0603
+PWR_SRC C764 0.1U/50V/0603
+PWR_SRC C604 0.1U/50V/0603
+PWR_SRC C471 0.1U/50V/0603
+PWR_SRC C427 0.1U/50V/0603
+3.3V_SUS C16 *0.1U/10V_NC

EMI requirement added on 0812

QUANTA COMPUTER

Title	EMI & Screw hole	
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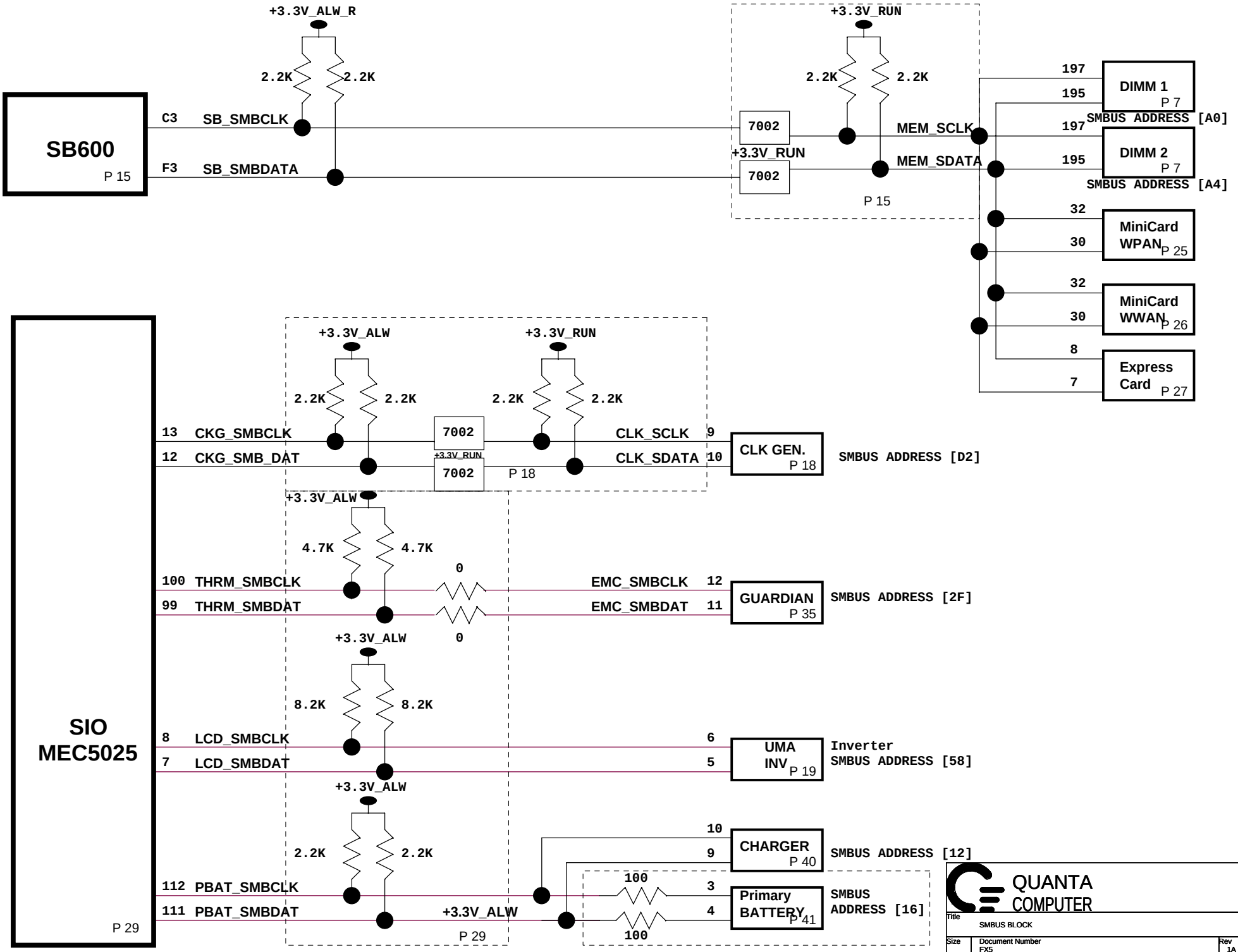

QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number FX5	Rev 1A
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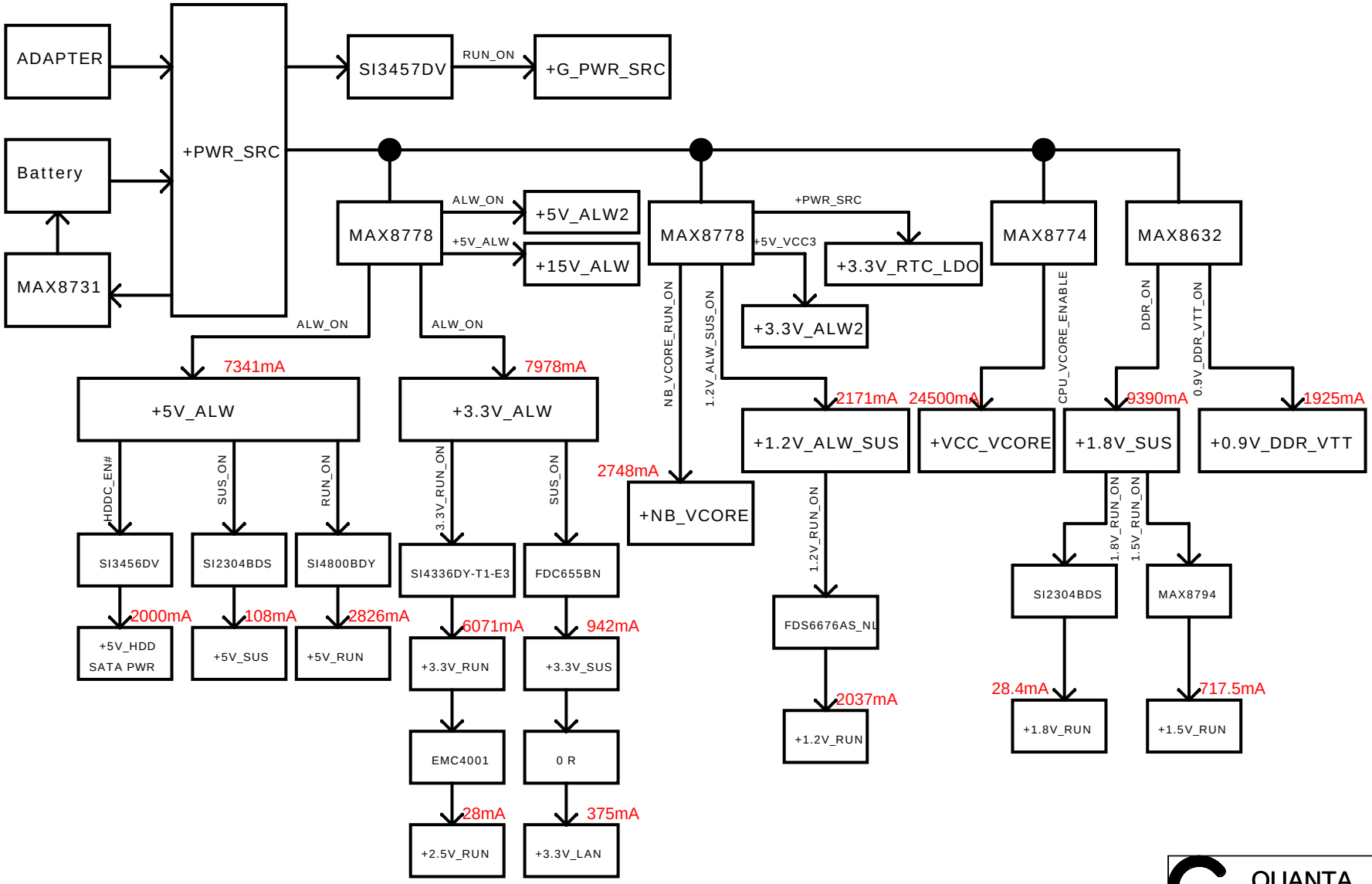
Power Design Block Diagram



QUANTA COMPUTER

Title	MB-50 Power BLOCK	
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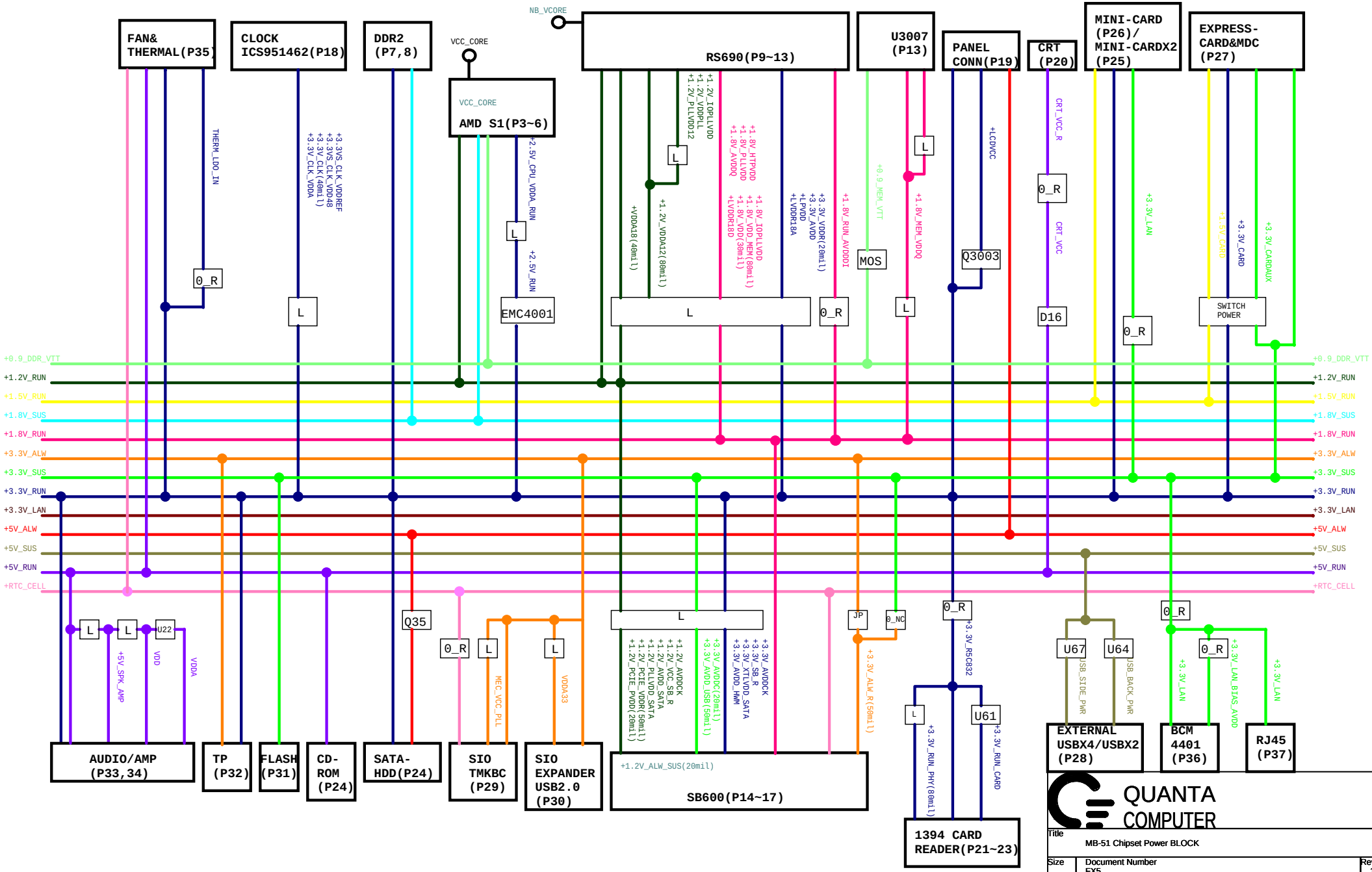
FAN& THERMAL(P35)
CLOCK ICS951462(P18)
DDR2 (P7,8)
VCC_CORE
AMD S1(P3~6)
NB_VCORE
RS690(P9~13)
U3007 (P13)
PANEL CONN(P19)
CRT (P20)
MINI-CARD (P26)/ MINI-CARDX2 (P25)
EXPRESS-CARD&MDC (P27)
THERM_LDO_IN
+3.3VS_CLK_VDDREF
+3.3VS_CLK_VDD48
+3.3V_CLK(40mil)
+3.3V_CLK_VDDA
+2.5V_CPU_VDDA_RUN
+2.5V_RUN
EMC4001
+1.2V_IOPLLVDD
+1.2V_VDDPLL
+1.2V_PLLVDD12
+VDDA18(40mil)
+1.2V_VDDA12(80mil)
+1.8V_HTPVDD
+1.8V_PLLVDD
+1.8V_AVDDQ
+1.8V_IOPLLVDD
+1.8V_VDD_MEM(80mil)
+1.8V_VDD(30mil)
+LVDDR18D
+3.3V_VDDR(20mil)
+3.3V_AVDD
+LPVDD
+LVDDR18A
+1.8V_RUN_AVDDDI
+0.9_MEM_VTT
MOS
+1.8V_MEM_VDDQ
+LCDVCC
Q3003
CRT_VCC_R
CRT_VCC
D16
+3.3V_LAN
+3.3V_CARD
+3.3V_CARDAUX
SWITCH POWER
+0.9_DDR_VTT
+1.2V_RUN
+1.5V_RUN
+1.8V_SUS
+1.8V_RUN
+3.3V_ALW
+3.3V_SUS
+3.3V_RUN
+3.3V_LAN
+5V_ALW
+5V_SUS
+5V_RUN
+RTC_CELL
U22
+5V_SPK_AMP
VDD
VDDA
Q35
MEC_VCC_PLL
VDDA33
+1.2V_AVDDCK
+1.2V_VCC_SB_R
+1.2V_AVDD_SATA
+1.2V_PLLVDD_SATA
+1.2V_PCIE_VDDR(50mil)
+1.2V_PCIE_PVDD(20mil)
+3.3V_AVDD_USB(50mil)
+3.3V_AVDDCK
+3.3V_SB_R
+3.3V_XTLVDD_SATA
+3.3V_AVDD_HWM
+3.3V_AVDDC(20mil)
+1.2V_ALW_SUS(20mil)
JP
0_NC
+3.3V_ALW_R(50mil)
+3.3V_R5C832
+3.3V_RUN_PHY(80mil)
+3.3V_RUN_CARD
U61
U67
U64
USB_SIDE_PWR
USB_BACK_PWR
+3.3V_LAN_BIAS_AVDD
AUDIO/AMP (P33,34)
TP (P32)
FLASH (P31)
CD-ROM (P24)
SATA-HDD(P24)
SIO TMKBC (P29)
SIO EXPANDER USB2.0 (P30)
SB600(P14~17)
1394 CARD READER(P21~23)
EXTERNAL USBX4/USBX2 (P28)
BCM 4401 (P36)
RJ45 (P37)
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Title
MB-51 Chipset Power BLOCK
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1A
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