Compal Confidential

ZSWAA/ZCWAA Schematics Document

Intel Haswell ULT/Broadwell U with DDR3L

AMD GPU Jet Pro/Topaz XT S3 (Single Rank)

LA-B301P REV 1.0 Schematic

Intel Processor (Haswell ULT/Broadwell U)
2014-02-10 Rev 1.0

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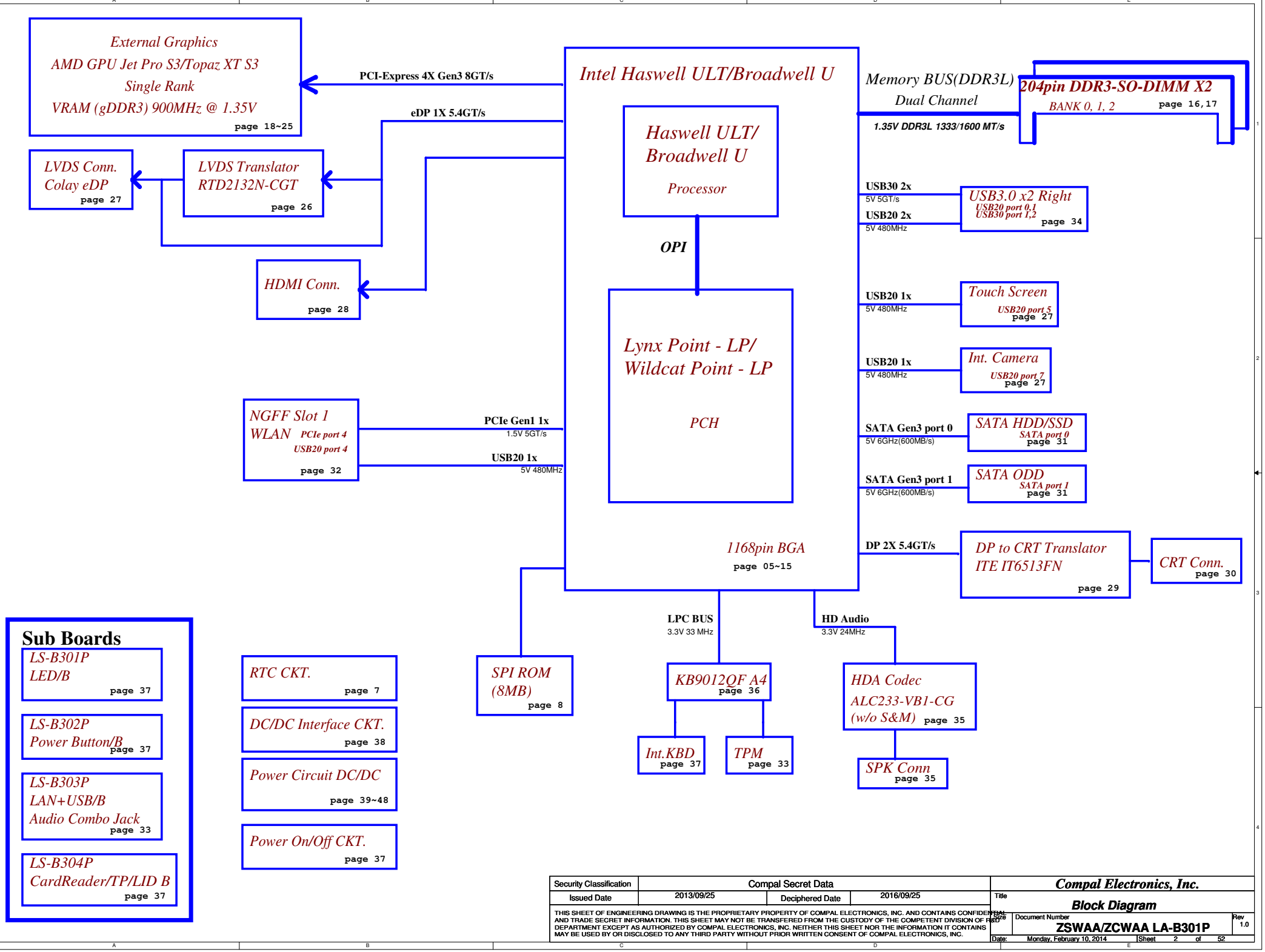

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Compal Electronics, Inc.	
Title	Block Diagram
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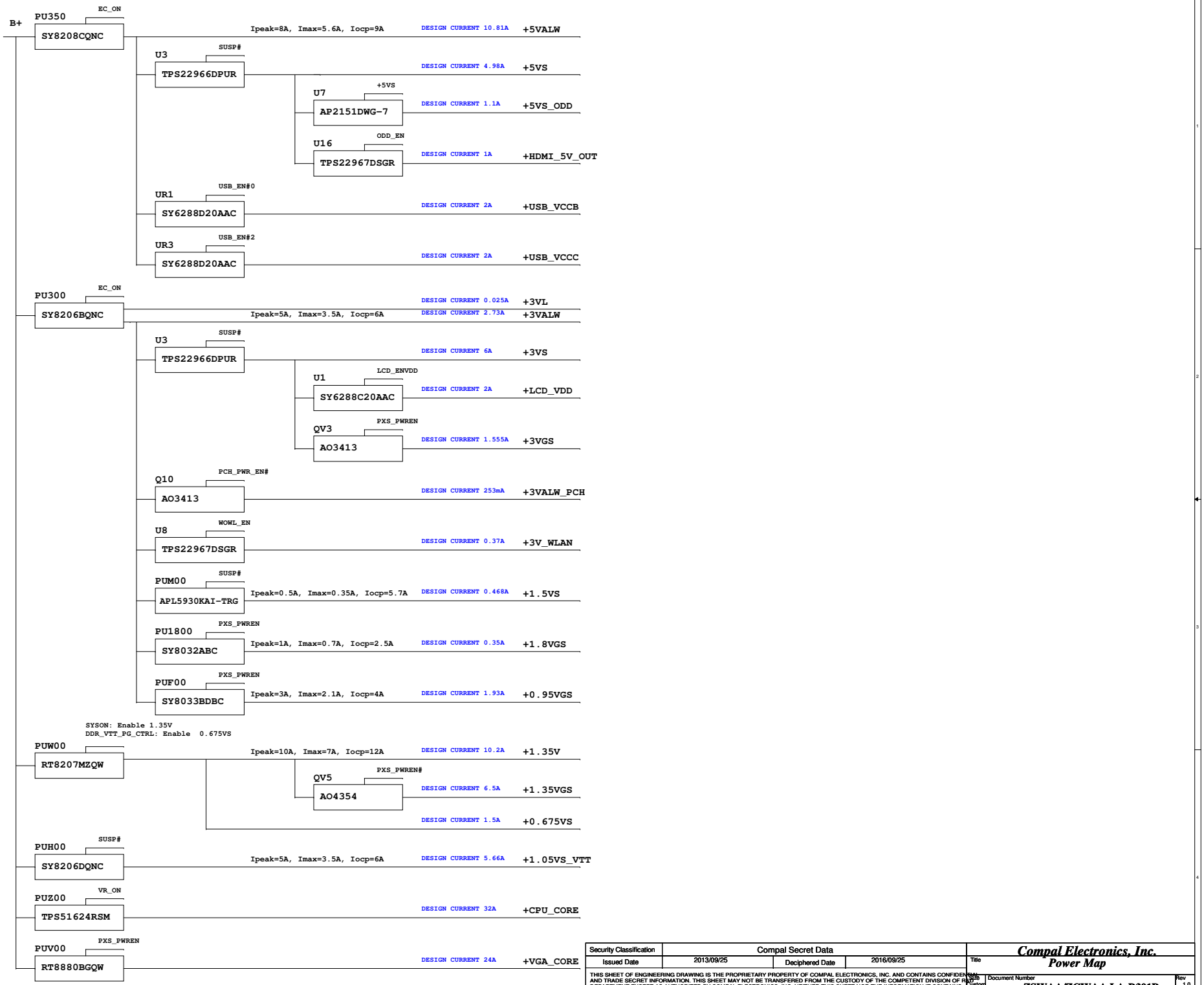

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.5VALW	+1.35V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS +1.05VS_VTT
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

Power	Device	HEX	Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VGS	AMD GPU	9E H	1001 1010 b

Platform	SKU	CPU	PCH	VGA
Intel SharkBay ULT	UMA DIS	Haswell-M ULT Processor	Lynx Point - LP	AMD GPU Jet Pro S3 Topaz XT S3

BTO Option Table

Function	SKU		Processor		GPU		VRAM	Internal Panel		HDMI	Wake On Wireless	
Description	UMA	DIS	HASWELL	BROADWELL	JET	TOPAZ	X76	LVDS	eDP	HDMI	WOWL	NON-WOWL
Explain	UMA	DIS	HASWELL	BROADWELL	JET	TOPAZ	X76	LVDS	eDP	HDMI	WOWL	NON-WOWL
BTO	UMA@	VGA@	HASWELL@	BROADWELL@	JET@	TOPAZ@	X76@	LVDS@	IEDP@	HDMI@	ISCT@	NOISCT@

Function	CPU (R1 PN)					
Description	I3-4005U	I5-4200U	I3-4010U	2990U	I5-4210U	I3-4015U
Explain	SA000072Q70	SA00006SM80	SA00006SXA0	SA00007LM00	SA00007LO00	SA00007LN00
BTO	4005UR1@	4200UR1@	4010UR1@	2990UR1@	4210UR1@	4015UR1@

Function	CPU (R3 PN)			
Description	I3-4005U	I5-4200U	I3-4010U	
Explain	SA000072Q60	SA00006SM90	SA00006SX90	
BTO	4005UR3@	4200UR3@	4010UR3@	

Function	ODD		XDP	FIX	Short pad	ESD	
Description	ZPODD	Non-ZPODD	XDP	FIX	Short pad	ESD	
Explain	Zero Power ODD	Non-Zero Power ODD	XDP	FIX	0 ohm short pad	ESD	
BTO	ZPODD@	NONZP@	XDP@	FIX@	Rshort@	ESD@	@ESD@

Function	EMI		CAM_EMI		CRT_EMI		TPM_EMI		TOUCH_EMI	
Description	EMI		CAM_EMI		CRT_EMI		TPM_EMI		TOUCH_EMI	
Explain	EMI		CAM_EMI		CRT_EMI		TPM_EMI		TOUCH_EMI	
BTO	EMI@	@EMI@	CAM_EMI@	@CAM_EMI@	CRT_EMI@	@CRT_EMI@	TPM_EMI@	@TPM_EMI@	TOUCH_EMI@	@TOUCH_EMI@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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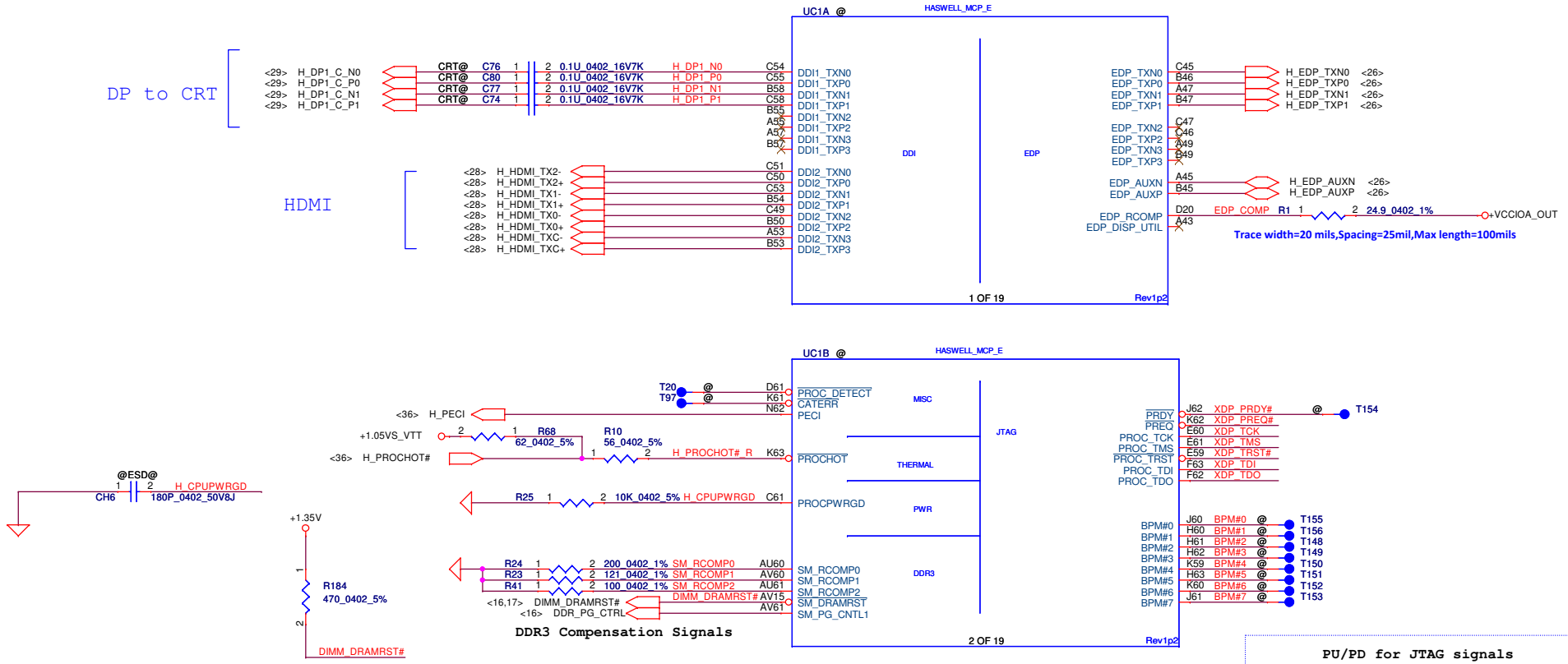

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Title	HSW MCP(1/11) DDI,MSIC,XDP		
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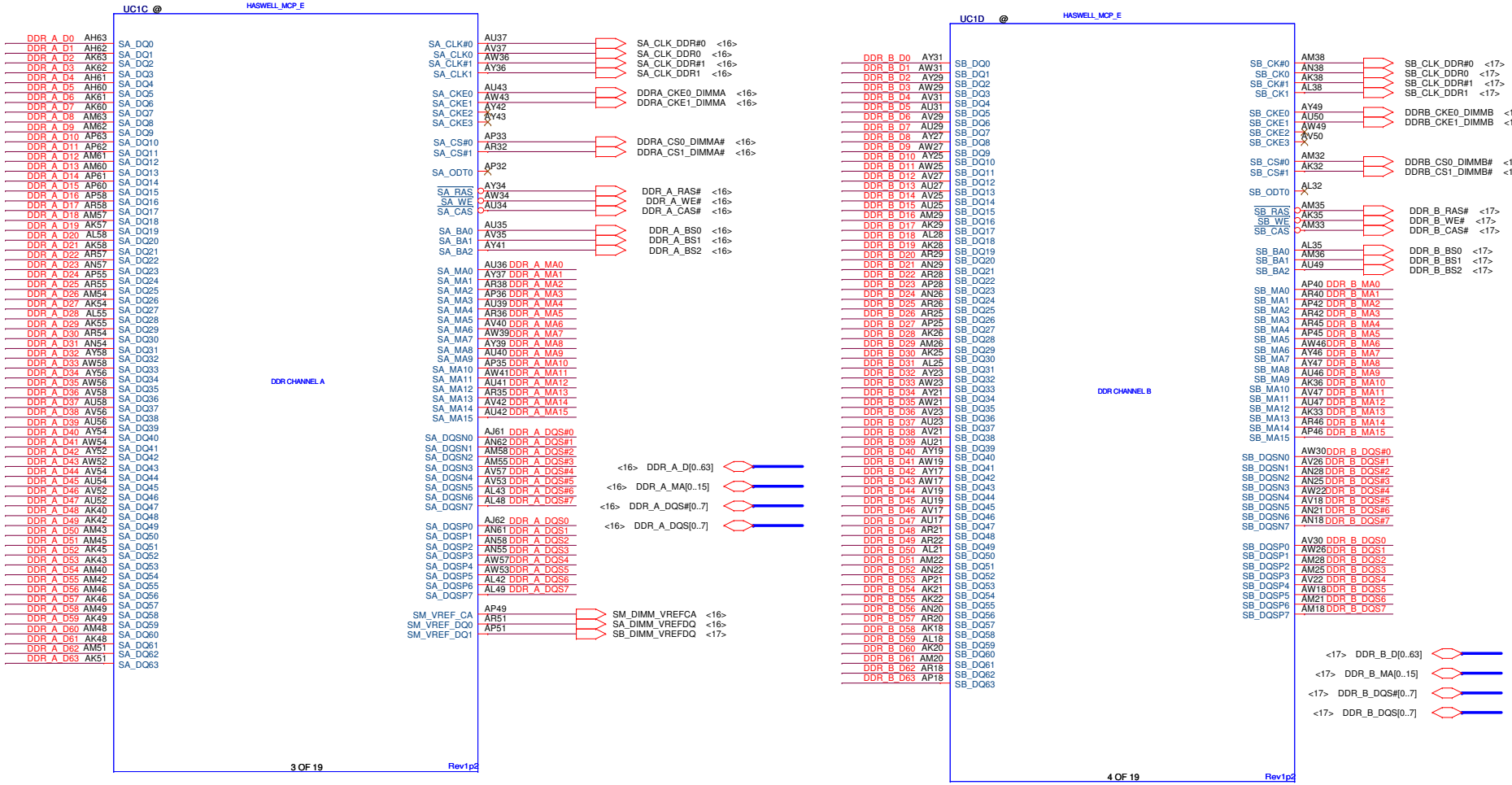

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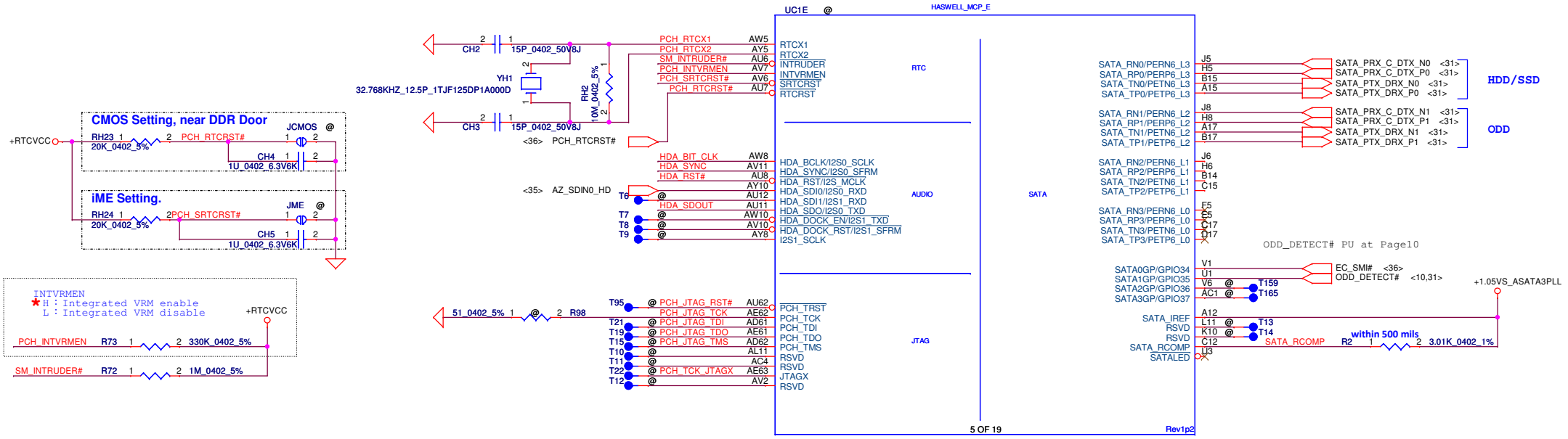
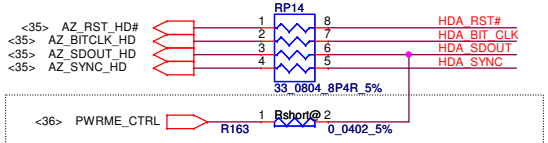
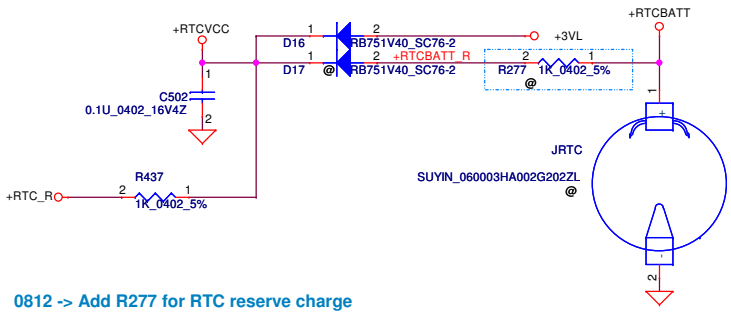


HDA for AUDIO



ME Debug

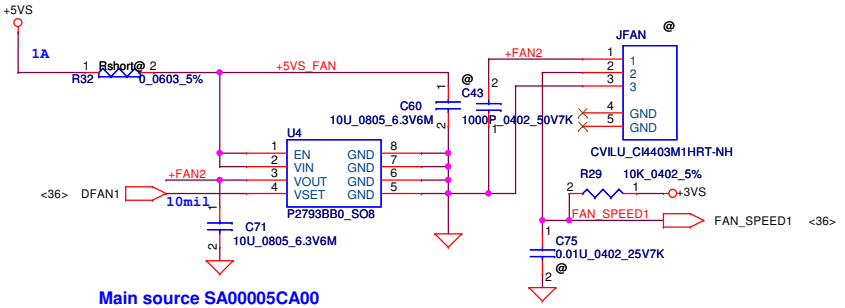
RTC schematic for non-chargeable



0812 -> Add R277 for RTC reserve charge

Change D16,D17 P/N from SCS0340L010 to SCS00003500 for X code.

FAN Control Circuit



Main source SA00005CA00
2nd source SA00005JO00

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Title	HSW MCP(3/11) RTC,SATA,XDP
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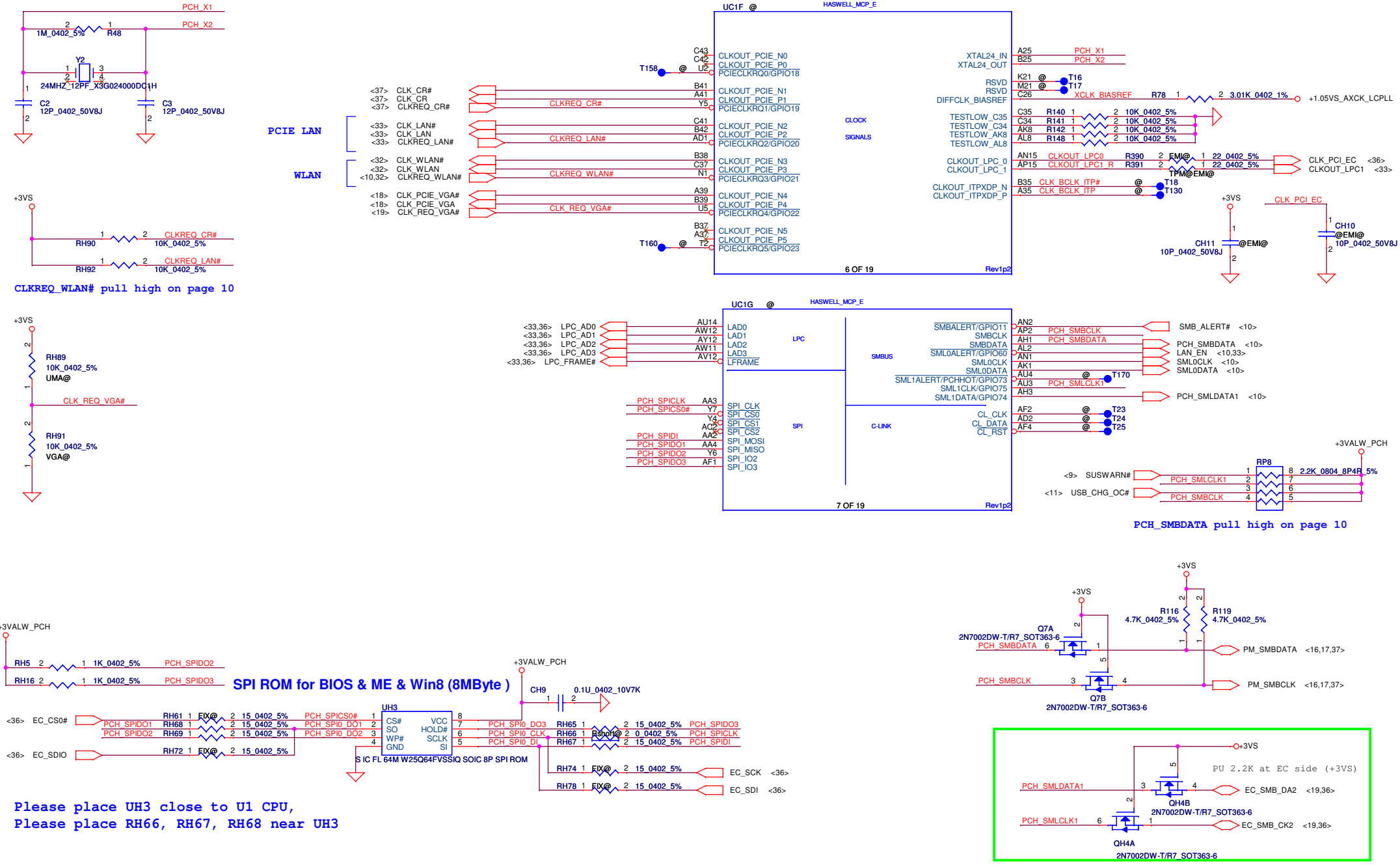

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Title	HSW MCP(4/11) CLK,SPI,SMBUS		
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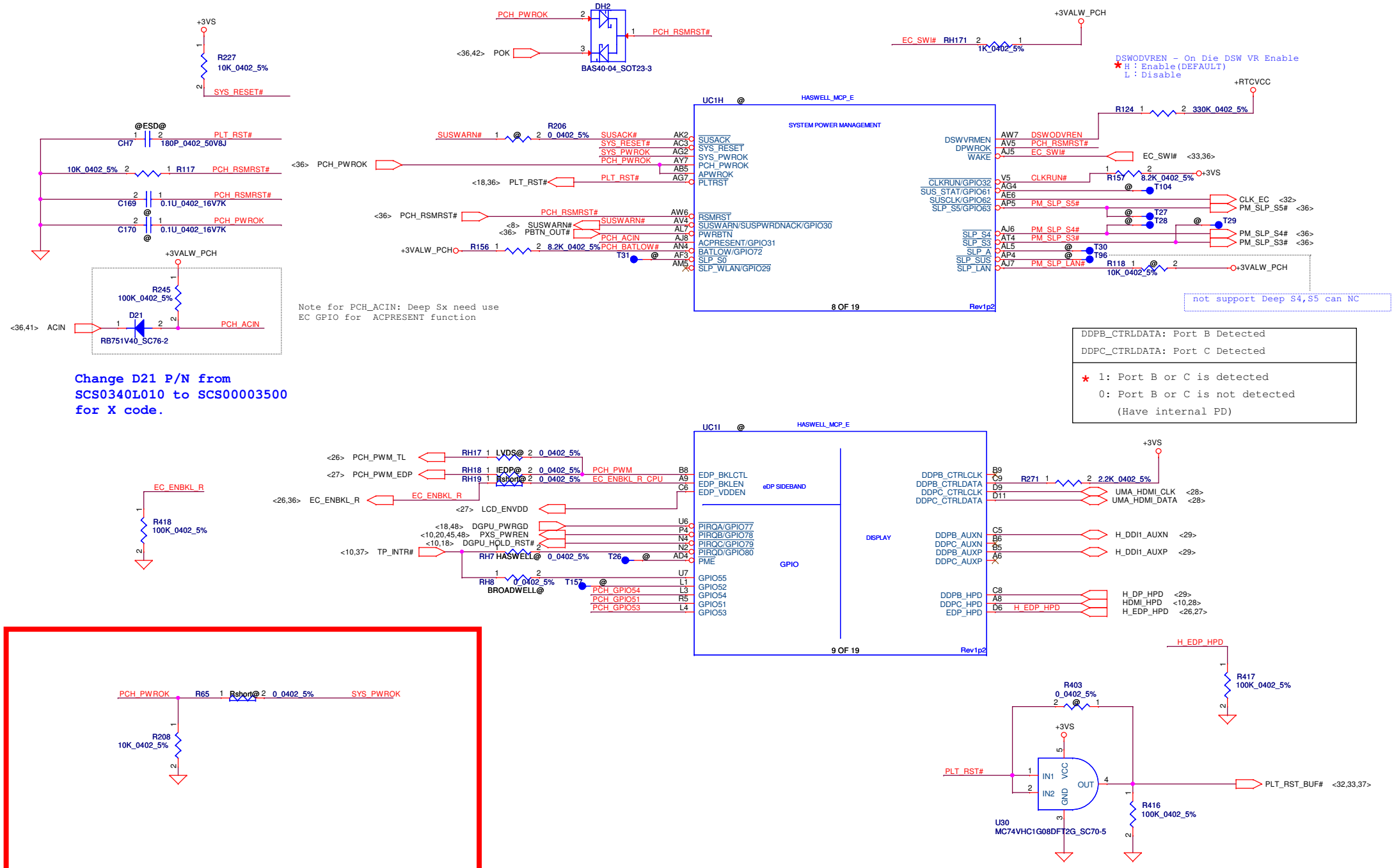

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Title	HSW MCP(5/11) PM,GPIO,DDI		
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Note: need check all GPIO PU need or not after BIOS post

+3VS

RP23 1 8 / 2 7 / 3 6 SERIRQ / 4 5 ODD_EN / 10K_0804_8P4R_5%
TP_INTR# <37,9>

RP27 1 8 / 2 7 / 3 6 ODD_DA# / 4 5 / 10K_0804_8P4R_5%
DGPU_HOLD_RST# <18,9>
CLKREQ_WLAN# <32,8>

ESD@ 1 2 ODD_DA# / CH8 180P_0402_50V8J

+3VALW_PCH

RP34 1 8 / 2 7 SML0DATA <8> / 3 6 LAN_EN <33,8> / 4 5 SMB_ALERT# <8> / SML0CLK <8> / 10K_0804_8P4R_5%

RP35 8 1 / 7 2 PCH_SMBDATA <8> / 6 3 PCH_SMLDATA1 <8> / 5 4 USB_OC#2 <11,33,36> / USB_OC#0 <11,34,36> / 2.2K_0804_8P4R_5%

+3VS

RP28 1 8 PCH_GPIO27 / 2 7 PASSWORD_CLEAR# / 3 6 / 4 5 / 10K_0804_8P4R_5%
ODD_DETECT# <31,7>
PXS_PWREN <20,45,48,9>

UC1J @ HASWELL_MCP_E

BMBUSY/GPIO76
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
GPIO16
GPIO17
GPIO24
GPIO27
GPIO28
GPIO26

GPIO56
GPIO57
GPIO58
GPIO59
GPIO44
GPIO47
GPIO48
GPIO49
GPIO50
HSIOPC/GPIO71
GPIO13
GPIO14
GPIO25
GPIO45
GPIO46

GPIO9
GPIO10
DEVSLP0/GPIO33
SDIO_POWER_EN/GPIO70
DEVSLP1/GPIO38
DEVSLP2/GPIO39
SPKR/GPIO81

GPIO

T162 @ P1 / T167 @ AU2 / AM7
<36> EC_LID_OUT# AD6
<38> ODD_EN Y1
<31> ODD_DA# T3
PCH_GPIO24 AD5
PCH_GPIO27 AN5
PCH_GPIO28 AD7
PCH_GPIO26 AN3

PASSWORD_CLEAR# AG6
T166 @ AP1
PCH_GPIO58 AL4
PCH_GPIO59 AT5
AK4
PCH_GPIO47 AB6
U4
DGPU_PRSNT# 1 RH10 2 0_0402_5% DGPU_PRSNT# GPIO49 Y3
T139 @ P3
PCH_GPIO71 Y2
T168 @ AT3
PCH_GPIO14 AH4
T169 @ AM4
PCH_GPIO45 AG5
PCH_GPIO46 AG3

PCH_GPIO9 AM3
<36> EC_SCI# HASWELL@ RH41 2 0_0402_5% AM2
P2
C4
T136 @ L2
BROADWELL@ RH61 2 0_0402_5% N5
<35> PCH_SPKR PCH_SPKR V2

JPW @ 1 2

CPU/MISC

THERMTRIP D60 H_THERMTRIP#
RCIN/GPIO82 V4 KB_RST#
SERIRQ T4 SERIRQ
PCH_OPI_RCOMP AW15 PCH_OPIRCOMP 1 2 R146 49.9_0402_1%
RSVD AF20 @ T106
RSVD AB21

KB_RST# <36>
SERIRQ <33,36>

LPIO

GSPI0_CS/GPIO83 R6 PCH_GPIO83
GSPI0_CLK/GPIO84 L6 PCH_GPIO84
GSPI0_MISO/GPIO85 N6 PCH_GPIO85
GSPI0_MOSI/GPIO86 L8 PCH_GPIO86
GSPI1_CS/GPIO87 R7 DGPU_PRSNT# GPIO87
GSPI1_CLK/GPIO88 L5 PCH_GPIO88
GSPI1_MISO/GPIO89 N7 PCH_GPIO89
GSPI_MOSI/GPIO90 K2 @ T135
UART0_RXD/GPIO91 J1 @ T134
UART0_TXD/GPIO92 K3 PCH_GPIO92
UART0_RTS/GPIO93 J2 PCH_GPIO93
UART0_CTS/GPIO94 G1 @ T114
UART1_RXD/GPIO0 K4
UART1_TXD/GPIO1 G2 @ T111
UART1_RST/GPIO2 J3 @ T133
UART1_CTS/GPIO3 J4 PCH_GPIO3
I2C0_SDA/GPIO4 F2 @ T132
I2C0_SCL/GPIO5 F3 PCH_GPIO5
I2C1_SDA/GPIO6 G4 PM_I2CSDA1
I2C1_SCL/GPIO7 F1 PM_I2CSCL1
SDIO_CLK/GPIO64 E3 PCH_GPIO64
SDIO_CMD/GPIO65 F4 PCH_GPIO65
SDIO_D0/GPIO66 D3 PCH_GPIO66
SDIO_D1/GPIO67 E4 PCH_GPIO67
SDIO_D2/GPIO68 C3 PCH_GPIO68
SDIO_D3/GPIO69 E2 ZP_DETECT

HDMI_HPD <28,9>
PM_I2CSDA1 <37>
PM_I2CSCL1 <37>

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Rev1p2

HASWELL@ RH9 0_0402_5% 1 2 DGPU_PRSNT#
+1.05VS_VTT
R144 1K_0402_5%
H_THERMTRIP#

+3VS
R306 10K_0402_5% UMA@
DGPU_PRSNT#
R219 10K_0402_5% VGA@

	GPIO87/GPIO49 DGPU_PRSNT#
PowerXpress	0
UMA	1

+3VS
R215 10K_0402_5% ZPODD@
ZP_DETECT
R216 10K_0402_5% NONZP@

	GPIO69
ZPODD SKU	1
None ZPODD SKU	0

+3VS
PM_I2CSDA1 R274 1 @ 2 1K_0402_5%
PM_I2CSCL1 R272 1 @ 2 1K_0402_5%

Need to check the resistors value

+3VS
R269 1 @ 2 1K_0402_1% PCH_SPKR

SPKR / GPIO81 : NO REBOOT
1: ENABLED
* 0: DISABLED (Have internal PD)

	GPIO88
TOUCH SKU	0
None TOUCH SKU	1

+3VALW_PCH
R247 1 2 10K_0402_5% EC_LID_OUT#

PCH_GPIO86 R273 1 @ 2 1K_0402_5%

PCH_GPIO66 R270 1 @ 2 1K_0402_1%

GPIO15 : TLS Confidentiality
1: Intel ME TLS with confidentiality
* 0: Intel ME TLS with no confidentiality (Have internal PD)

GSPI0_MOSI / GPIO86 : Boot BIOS Strap
1: ENABLED
* 0: SPI ROM (Have internal PD)

SDIO_D0 / GPIO66 : Top-Block Swap Override
* 1: ENABLED (Have internal PU)
0: DISABLED

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Title: HSW MCP(6/11) GPIO,LPIO

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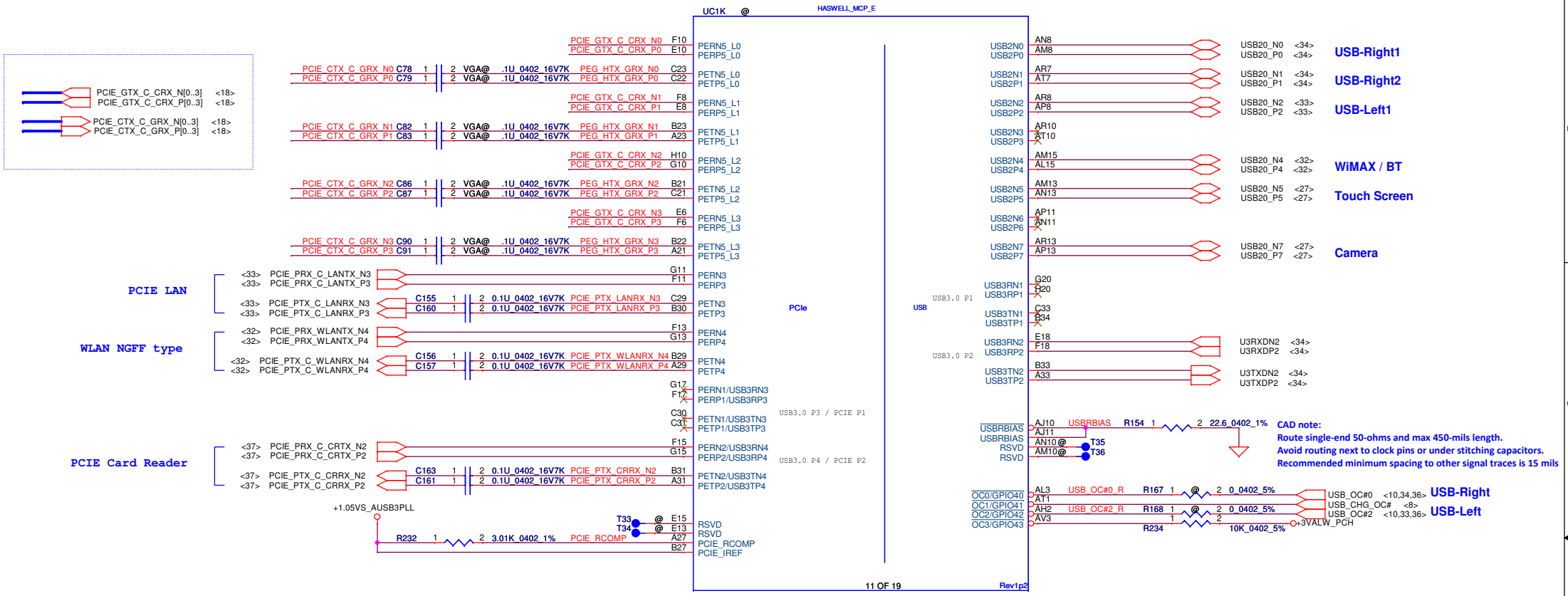

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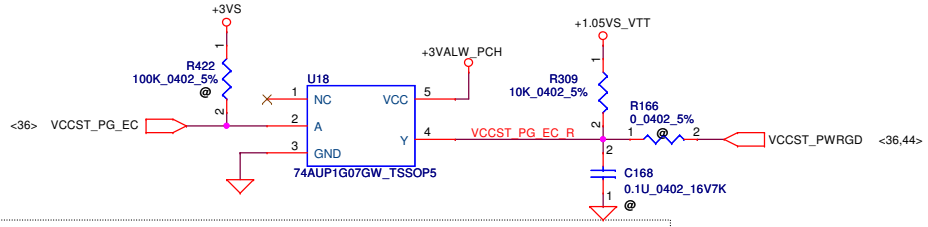
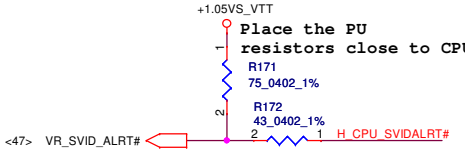


SVID ALERT



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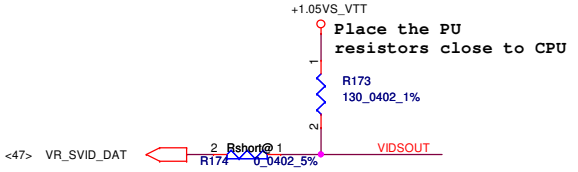

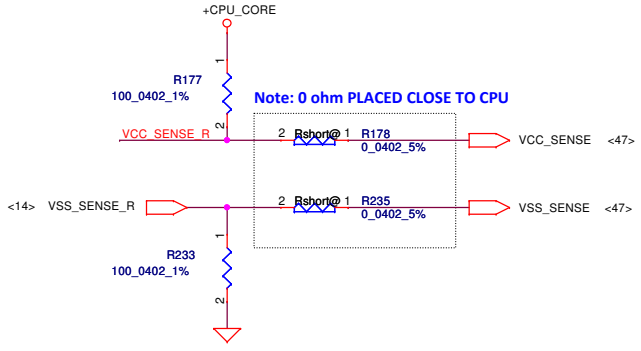

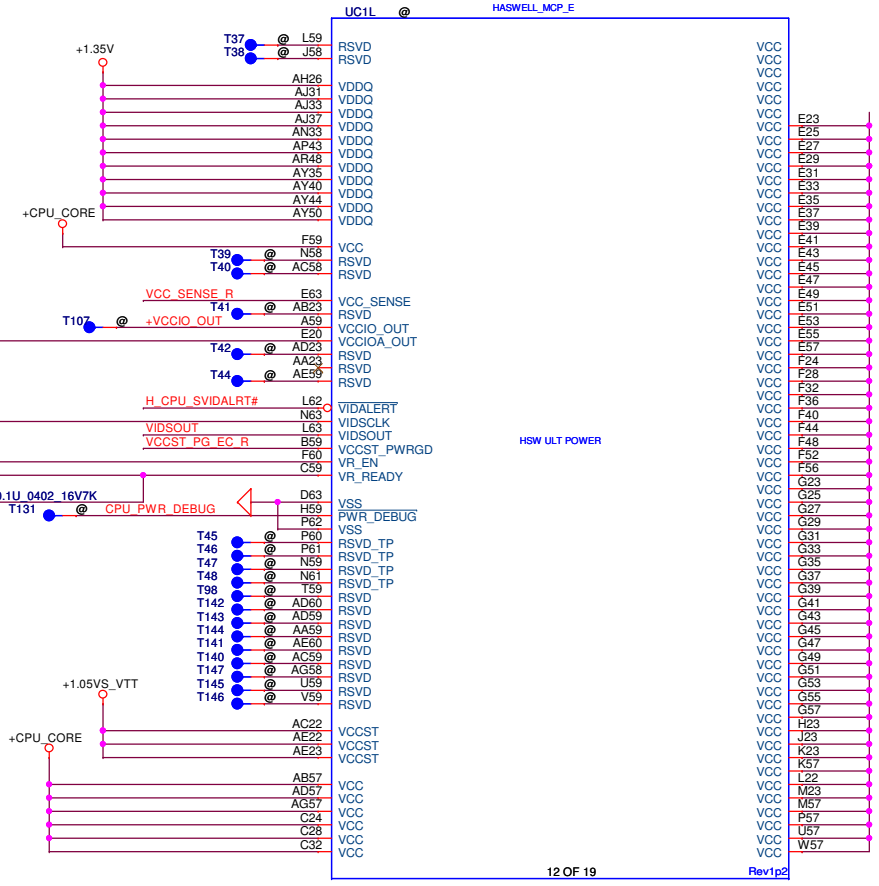

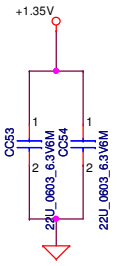

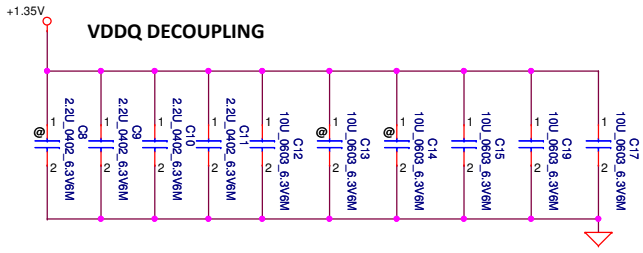

+1.35V : 470UF/2V/7343 *2
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

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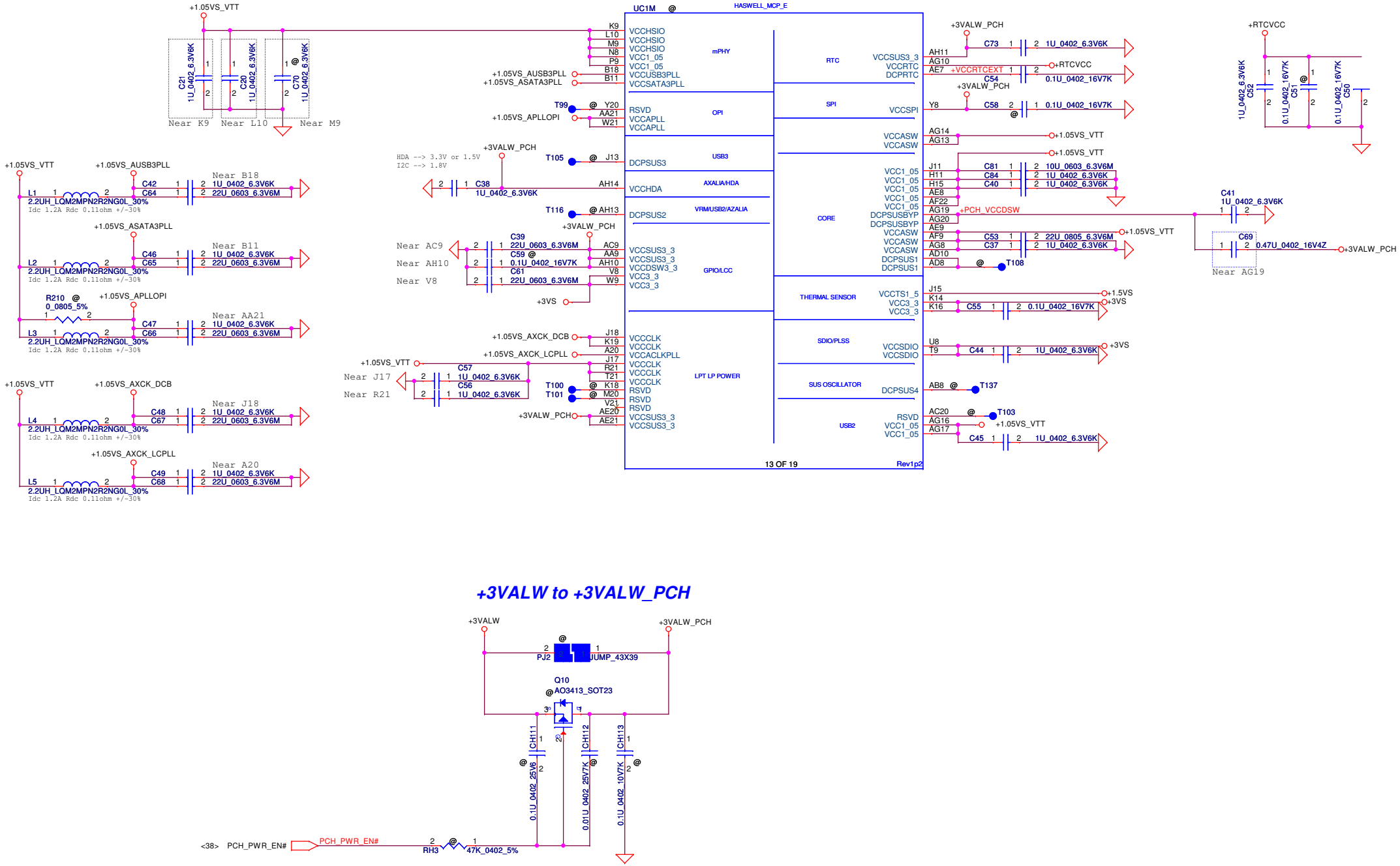

+3VALW to +3VALW_PCH

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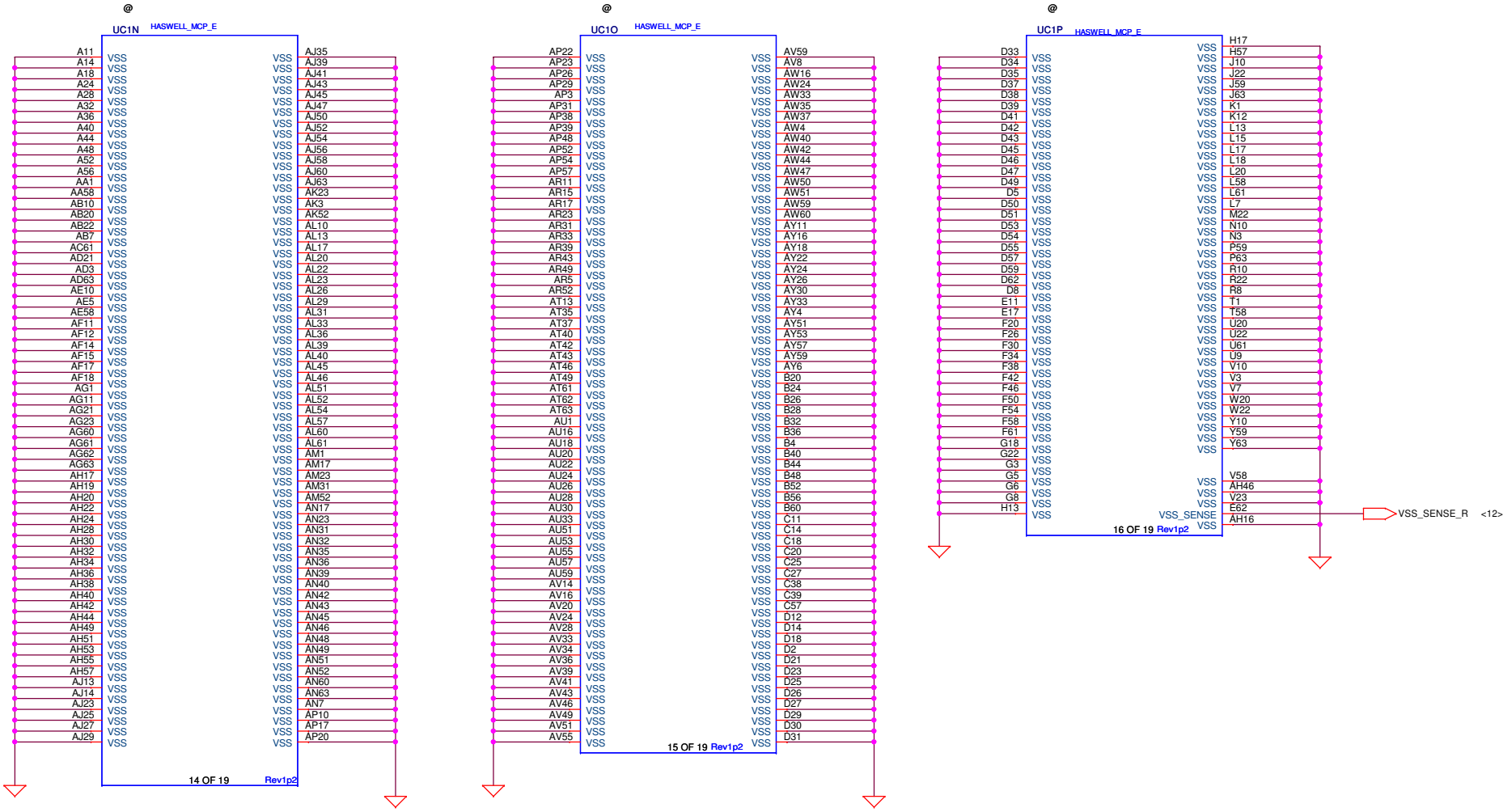

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Title: HSW MCP(10/11) GND

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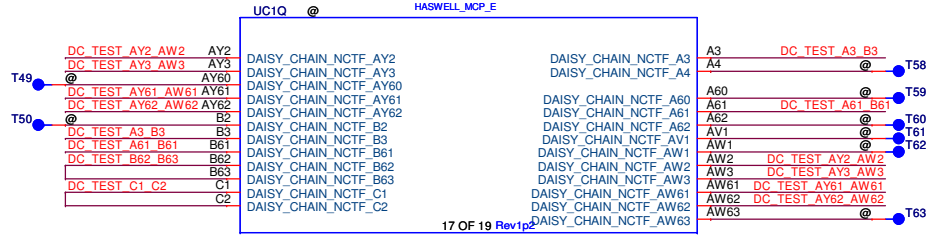
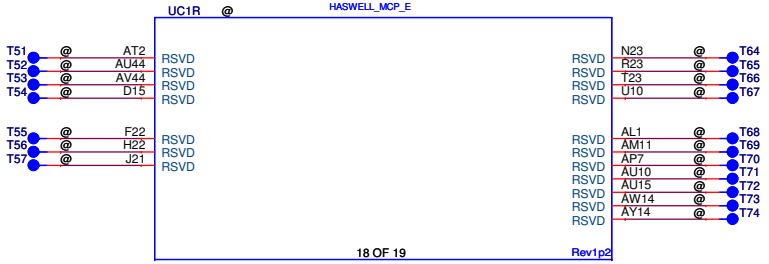
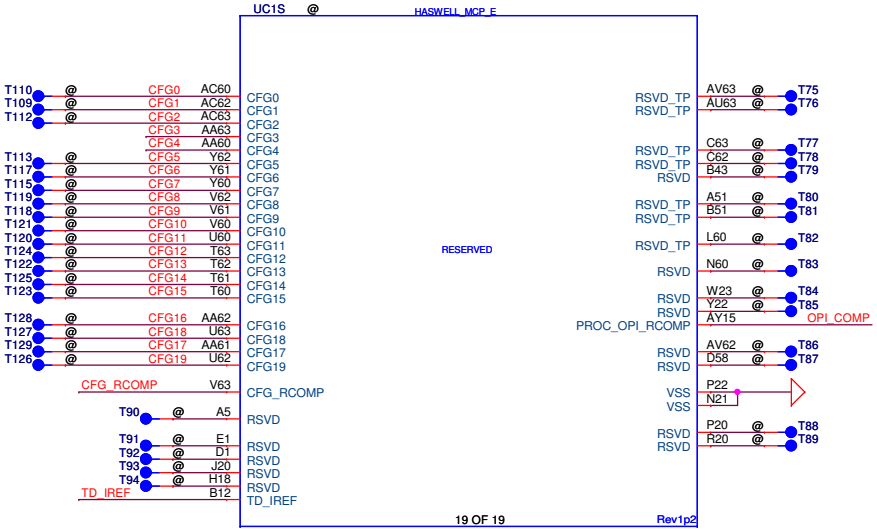
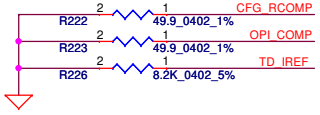
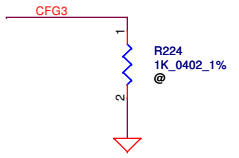




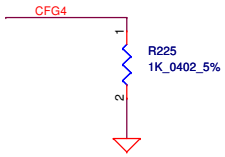




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: HSW MCP(11/11) RSVD

Size: Custom | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

Date: Monday, February 10, 2014 | Sheet 15 of 52

DDR3 SO-DIMM A
Reverse Type
H=4.0mm

Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width

Place near DDR connector for DQA easy access

Layout Note:
Place near JDIMM1.203,204

Channel A

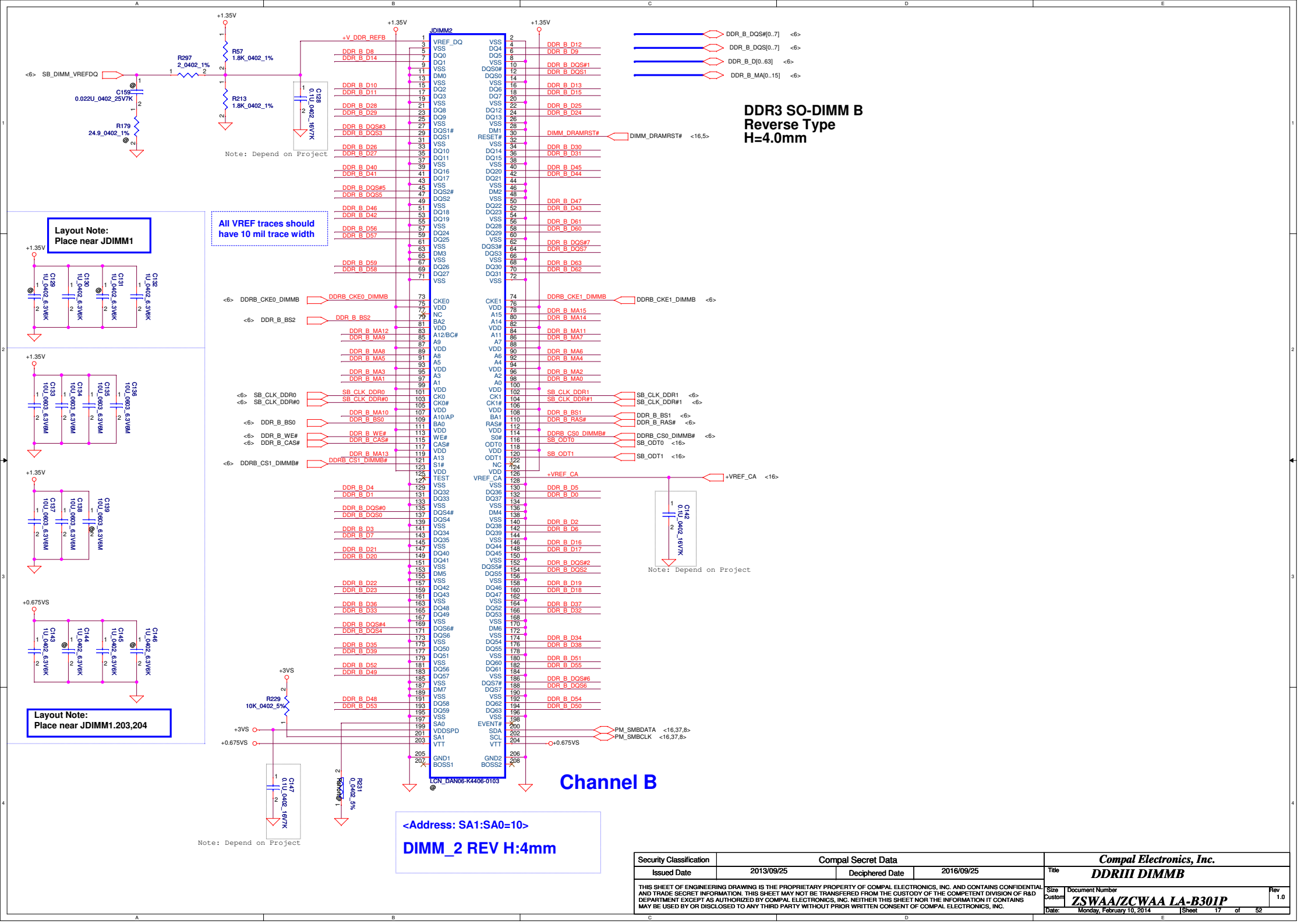
<Address: SA1:SA0=00>

DIMM_1 REV H:4mm

Note: Depend on Project

Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.			
Title: DDRIII DIMMA			
Size: Custom	Document Number: ZSWAA/ZCWAA LA-B301P		Rev: 1.0
Date: Monday, February 10, 2014	Sheet 16 of 52		



Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: DDRIII DIMMB

Size	Document Number	Rev
Custom	ZSWAA/ZCWAA LA-B301P	1.0

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AC Coupling Capacitor
PCIe Gen3: Recommended value is 220 nF
PCIe Gen1 and Gen2 only: Recommended value is 100 nF

LVDS Interface

UV1A

PCIE_CTX_C_GRX_P0 / PCIE_CTX_C_GRX_N0 → AF30 / AE31 PCIE_RX0P / PCIE_RX0N
PCIE_CTX_C_GRX_P1 / PCIE_CTX_C_GRX_N1 → AE29 / AD28 PCIE_RX1P / PCIE_RX1N
PCIE_CTX_C_GRX_P2 / PCIE_CTX_C_GRX_N2 → AD30 / AC31 PCIE_RX2P / PCIE_RX2N
PCIE_CTX_C_GRX_P3 / PCIE_CTX_C_GRX_N3 → AC29 / AB28 PCIE_RX3P / PCIE_RX3N
AB30 / AA31 PCIE_RX4P / PCIE_RX4N
AA29 / Y28 PCIE_RX5P / PCIE_RX5N
Y30 / W31 PCIE_RX6P / PCIE_RX6N
W29 / V28 PCIE_RX7P / PCIE_RX7N
V30 / U31 NC#V30 / NC#U31
U29 / T28 NC#U29 / NC#T28
T30 / R31 NC#T30 / NC#R31
R29 / P28 NC#R29 / NC#P28
P30 / N31 NC#P30 / NC#N31
N29 / M28 NC#N29 / NC#M28
M30 / L31 NC#M30 / NC#L31
L29 / K30 NC#L29 / NC#K30

PCI EXPRESS INTERFACE

PCIE_TX0P / PCIE_TX0N → AH30 / AG31 PCIE_GTX_CRX_P0 / PCIE_GTX_CRX_N0 .1U_0402_16V7K → VGA@ CV1 / CV2 PCIE_GTX_C_CRX_P0 / PCIE_GTX_C_CRX_N0 → PCIE_GTX_C_CRX_P0 / PCIE_GTX_C_CRX_N0
PCIE_TX1P / PCIE_TX1N → AG29 / AF28 PCIE_GTX_CRX_P1 / PCIE_GTX_CRX_N1 .1U_0402_16V7K → VGA@ CV3 / CV4 PCIE_GTX_C_CRX_P1 / PCIE_GTX_C_CRX_N1 → PCIE_GTX_C_CRX_P1 / PCIE_GTX_C_CRX_N1
PCIE_TX2P / PCIE_TX2N → AF27 / AF26 PCIE_GTX_CRX_P2 / PCIE_GTX_CRX_N2 .1U_0402_16V7K → VGA@ CV5 / CV6 PCIE_GTX_C_CRX_P2 / PCIE_GTX_C_CRX_N2 → PCIE_GTX_C_CRX_P2 / PCIE_GTX_C_CRX_N2
PCIE_TX3P / PCIE_TX3N → AD27 / AD26 PCIE_GTX_CRX_P3 / PCIE_GTX_CRX_N3 .1U_0402_16V7K → VGA@ CV7 / CV8 PCIE_GTX_C_CRX_P3 / PCIE_GTX_C_CRX_N3 → PCIE_GTX_C_CRX_P3 / PCIE_GTX_C_CRX_N3
PCIE_TX4P / PCIE_TX4N AC25 / AB25
PCIE_TX5P / PCIE_TX5N Y23 / Y24
PCIE_TX6P / PCIE_TX6N AB27 / AB26
PCIE_TX7P / PCIE_TX7N Y27 / Y26
NC#W24 / NC#W23 W24 / W23
NC#V27 / NC#U26 V27 / U26
NC#U24 / NC#U23 U24 / U23
NC#T26 / NC#T27 T26 / T27
NC#T24 / NC#T23 T24 / T23
NC#P27 / NC#P26 P27 / P26
NC#P24 / NC#P23 P24 / P23
NC#M27 / NC#N26 M27 / N26

CLOCK
<8> CLK_PCIE_VGA / <8> CLK_PCIE_VGA# → CLK_PCIE_VGA / CLK_PCIE_VGA# AK30 / AK32 PCIE_REFCLKP / PCIE_REFCLKN

RV2 1 VGA@ 2 1K_0402_5% → N10 TEST_PG
PLTRST_VGA# → AL27 PERSTB

CALIBRATION
PCIE_CALR_TX / PCIE_CALR_RX
Y22 VGA_PCIE_CALRP → RV1 1 VGA@ 2 1.69K_0402_1%
AA22 VGA_PCIE_CALRN → RV3 1 VGA@ 2 1K_0402_1%
+0.95VGS

@ 2160856030-A0_FCBGA631

UV1F

+VGA_CORE
VARY_BL / DIGON → AB11 / AB12 Topaz

TXCAP_DPA3P / TXCAM_DPA3N AL15 / AK14
TX0P_DPA2P / TX0M_DPA2N AH16 / AJ15
TX1P_DPA1P / TX1M_DPA1N AL17 / AK16
TX2P_DPA0P / TX2M_DPA0N AH18 / AJ17
NC_TXOUT_L3P / NC_TXOUT_L3N AL19 / AK18
TMDP
TXCBP_DPB3P / TXCBM_DPB3N AH20 / AJ19
TX3P_DPB2P / TX3M_DPB2N AL21 / AK20
TX4P_DPB1P / TX4M_DPB1N AH22 / AJ21
TX5P_DPB0P / TX5M_DPB0N AL23 / AK22
NC_TXOUT_U3P / NC_TXOUT_U3N AK24 / AJ23

@ 2160856030-A0_FCBGA631

For CRB reserved

+3VGS
PLT_RST# → UV11 MC74VHC1G08DFT2G_SC70-5 @ (IN1, IN2, VCC, GND, OUT)
<48,9> DGPU_PWRGD
DGPU_PWROK_R → @ RV167 0_0402_5% → DGPU_PWROK <48>
RV56 100K_0402_5% @

+3VGS
<36,9> PLT_RST#
<10,9> DGPU_HOLD_RST#
→ UV8 MC74VHC1G08DFT2G_SC70-5 VGA@ (IN1, IN2, VCC, GND, OUT)
PLTRST_VGA#
RV52 100K_0402_5% VGA@

Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: PCIE/LVDS

Size: Custom | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

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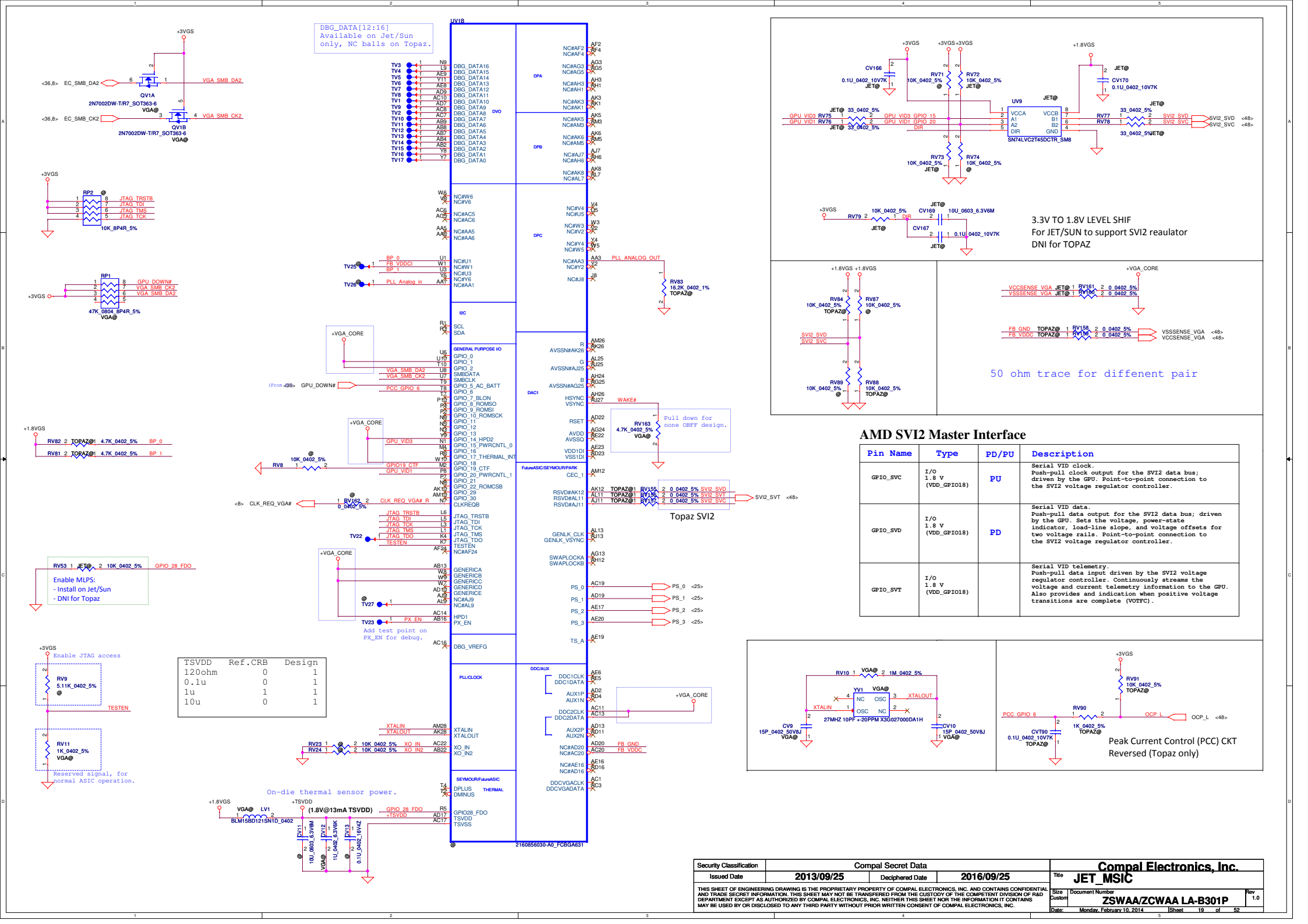

AMD SVI2 Master Interface

Pin Name	Type	PD/PU	Description
GPIO_SVC	I/O 1.8 V (VDD_GPIO18)	PU	Serial VID clock. Push-pull clock output for the SVI2 data bus; driven by the GPU. Point-to-point connection to the SVI2 voltage regulator controller.
GPIO_SVD	I/O 1.8 V (VDD_GPIO18)	PD	Serial VID data. Push-pull data output for the SVI2 data bus; driven by the GPU. Sets the voltage, power-state indicator, load-line slope, and voltage offsets for two voltage rails. Point-to-point connection to the SVI2 voltage regulator controller.
GPIO_SVT	I/O 1.8 V (VDD_GPIO18)		Serial VID telemetry. Push-pull data input driven by the SVI2 voltage regulator controller. Continuously streams the voltage and current telemetry information to the GPU. Also provides and indication when positive voltage transitions are complete (VOTFC).

TSVDD	Ref.CRB	Design
120ohm	0	1
0.1u	0	1
1u	1	1
10u	0	1

Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.			
Title: JET_MSIC			
Size: Custom	Document Number: ZSWAA/ZCWAA LA-B301P		Rev: 1.0
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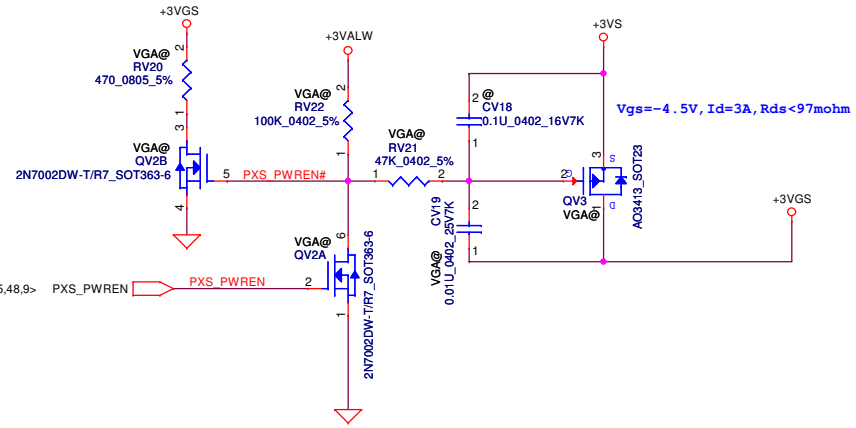
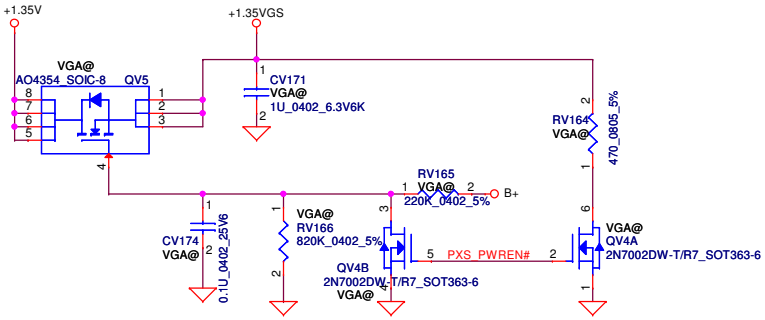
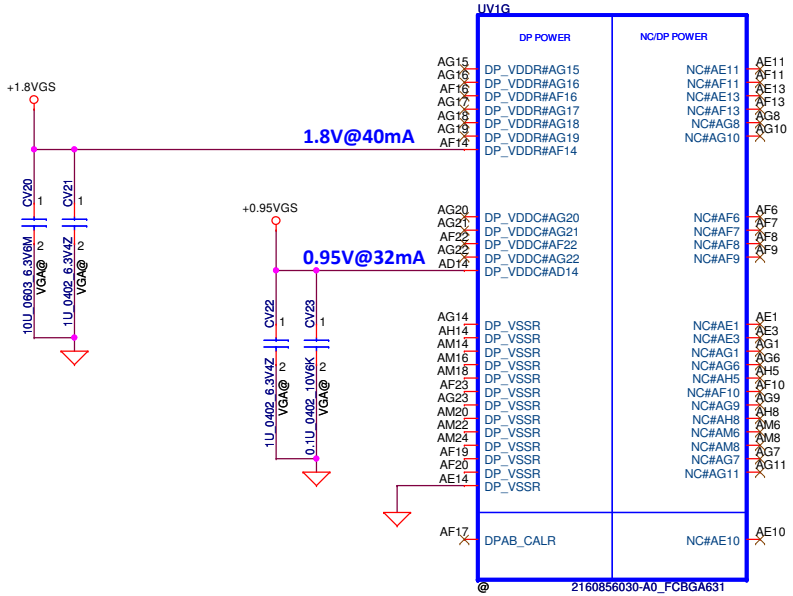
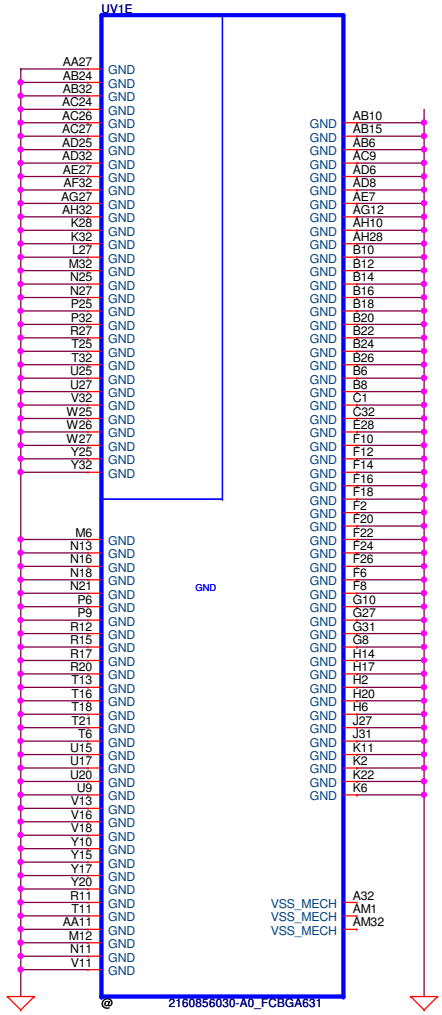
+3VS to +3VGS (25mA)



+1.35V to +1.35VGS (6.5A)







Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: **JET_Power/GND**

Size: Custom | Document Number: **ZSWAA/ZCWAA LA-B301P** | Rev: 1.0

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PCIE_PVDD	Jet CRB	Design
1u	1	1
10u	1	1

PCIE_VDDC/BIF_VDDC	Jet CRB	Design
1u	6	6
10u	1	1

VDDR1	Jet CRB	Design
0.01u	1	1
0.1u	1	1
2.2u	5	5
10u	1	1

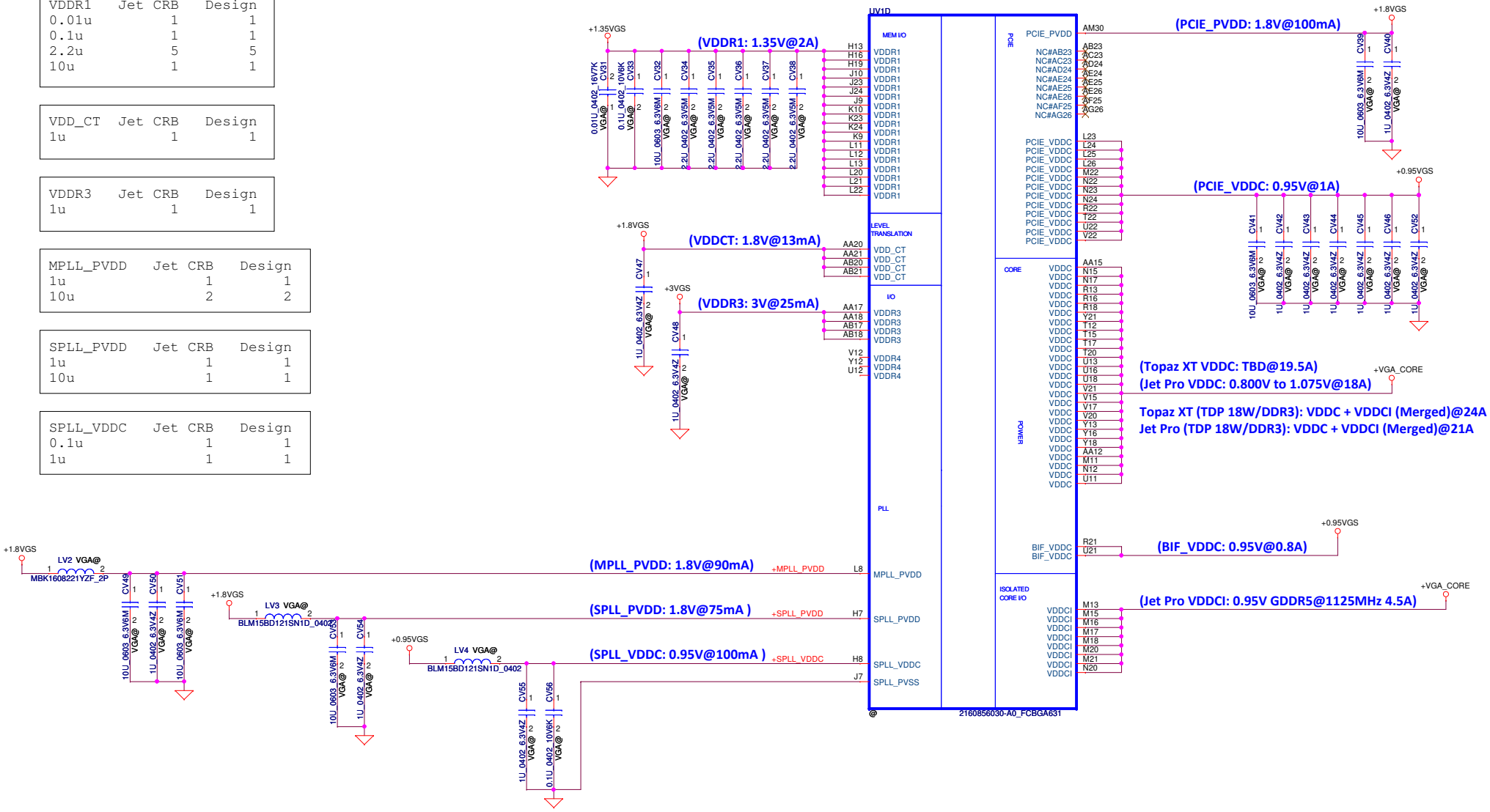
VDD_CT	Jet CRB	Design
1u	1	1

VDDR3	Jet CRB	Design
1u	1	1

MPLL_PVDD	Jet CRB	Design
1u	1	1
10u	2	2

SPLL_PVDD	Jet CRB	Design
1u	1	1
10u	1	1

SPLL_VDDC	Jet CRB	Design
0.1u	1	1
1u	1	1



Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: **JET_Power**

Size: Custom | Document Number: **ZSWAA/ZCWAA LA-B301P** | Rev: 1.0

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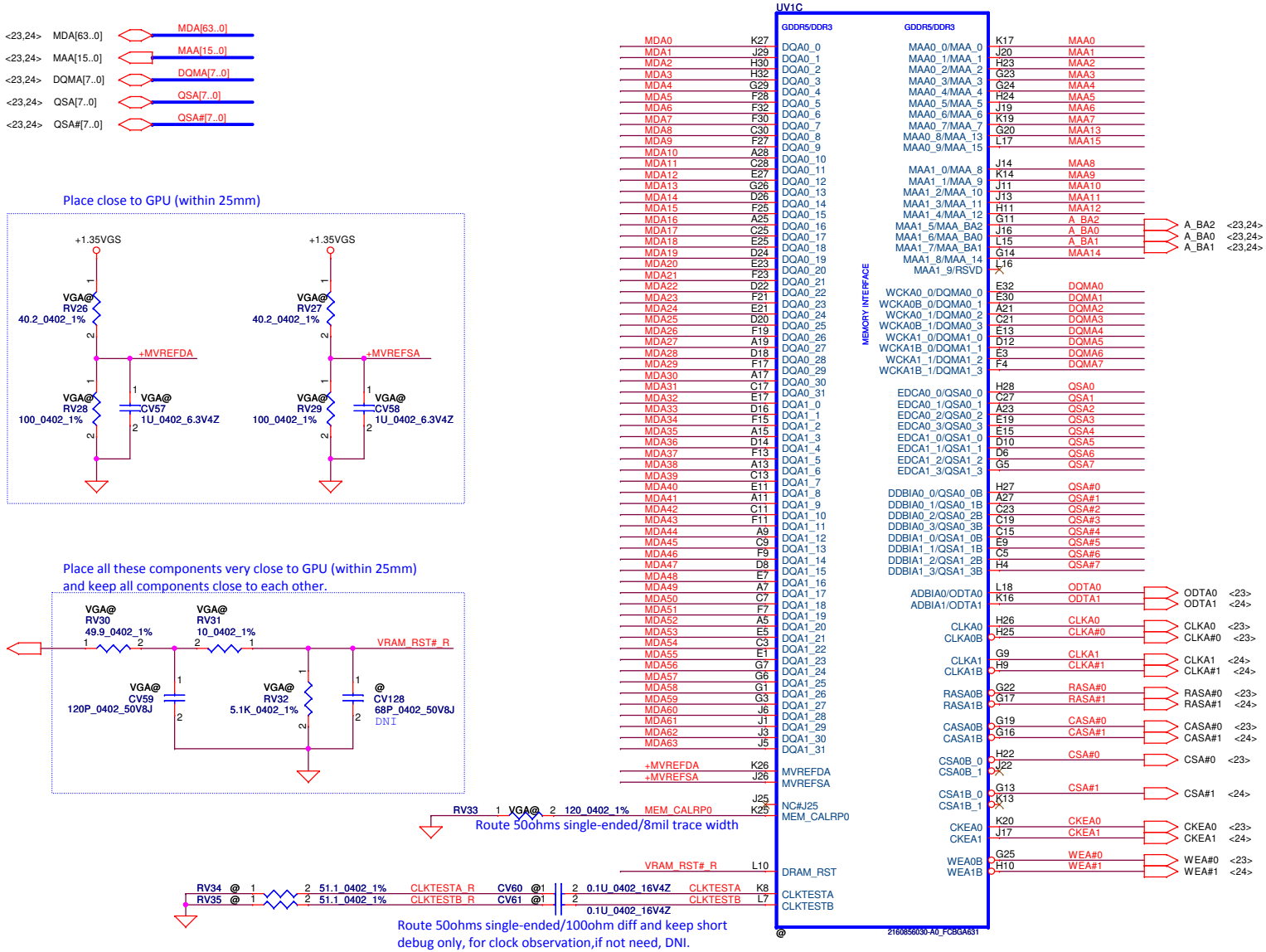

Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: **MEM IF**

Size	Document Number	Rev
Custom	ZSWAA/ZCWAA LA-B301P	1.0

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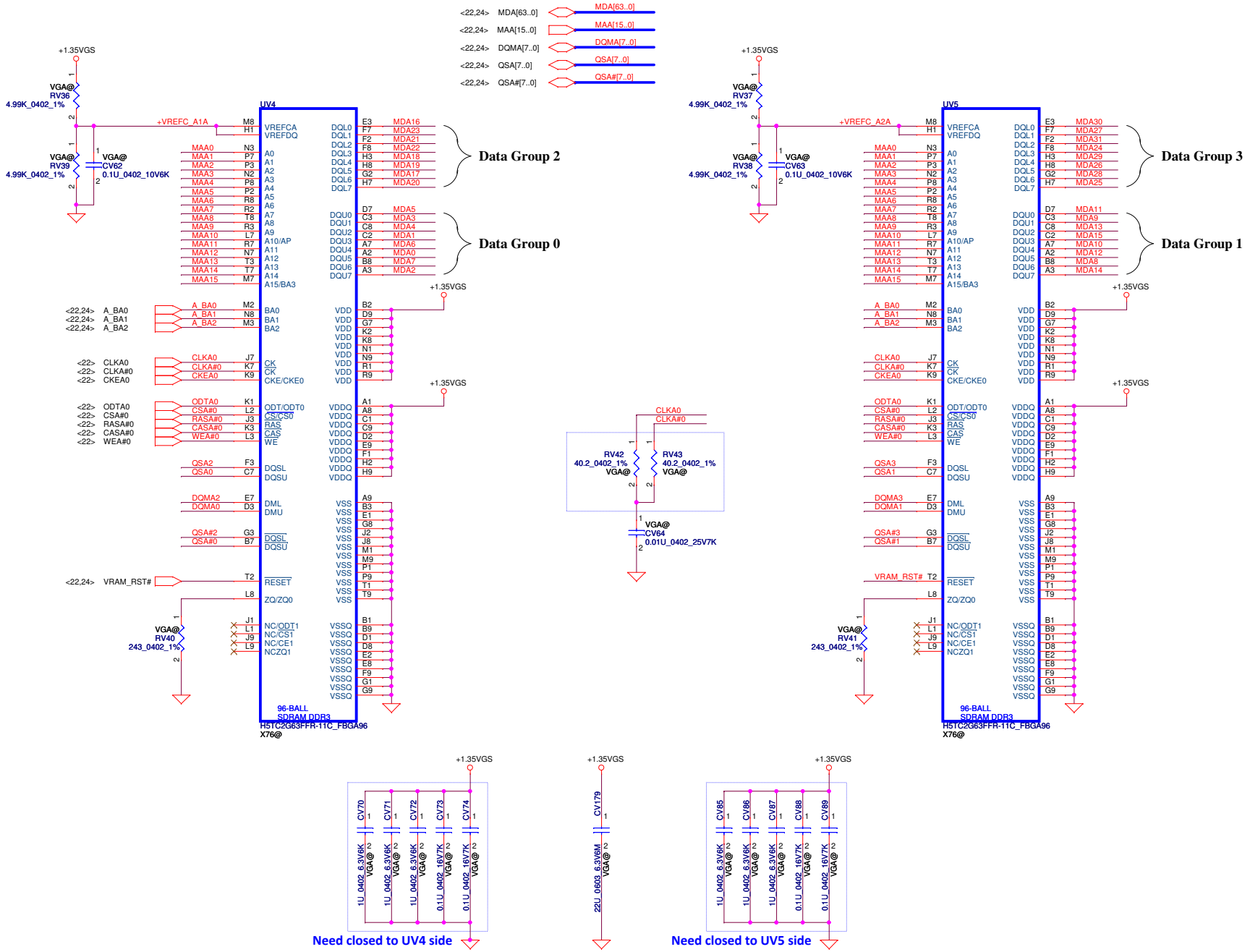
Memory Partition A - Lower 32 bits <Channel A0>



Channel A0, Data Group 0

MDA0
MDA1
MDA2
MDA3
MDA4
MDA5
MDA6
MDA7
DQMA0
QSA0
QSA#0

Channel A0, Data Group 1

MDA8
MDA9
MDA10
MDA11
MDA12
MDA13
MDA14
MDA15
DQMA1
QSA1
QSA#1

Channel A0, Data Group 2

MDA16
MDA17
MDA18
MDA19
MDA20
MDA21
MDA22
MDA23
DQMA2
QSA2
QSA#2

Channel A0, Data Group 3

MDA24
MDA25
MDA26
MDA27
MDA28
MDA29
MDA30
MDA31
DQMA3
QSA3
QSA#3

Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: VRAM A Lower

Size: Custom | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

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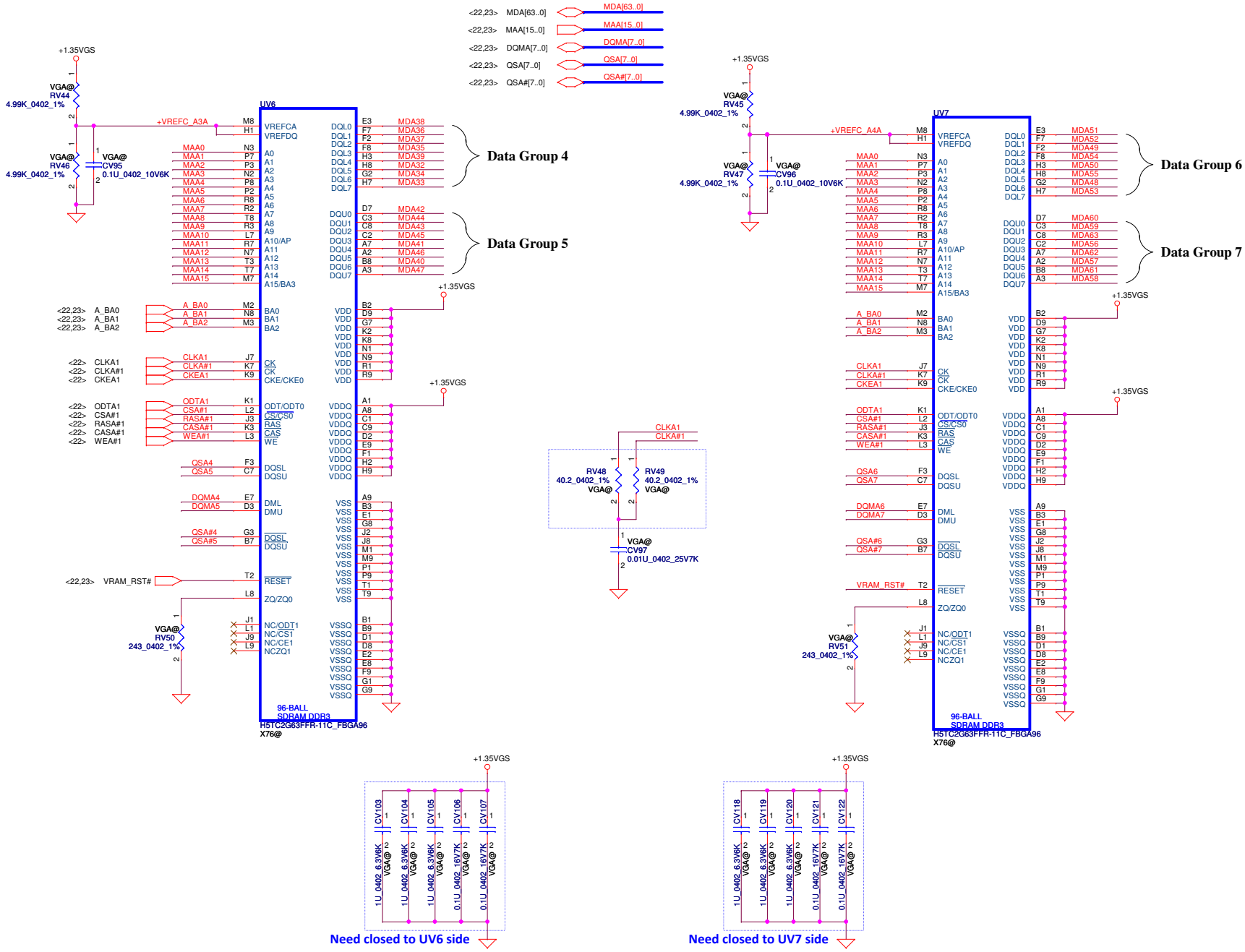
Memory Partition A - Upper 32 bits <Channel A1>



Channel A1, Data Group 4
MDA32
MDA33
MDA34
MDA35
MDA36
MDA37
MDA38
MDA39
DQMA4
QSA4
QSA#4

Channel A1, Data Group 5
MDA40
MDA41
MDA42
MDA43
MDA44
MDA45
MDA46
MDA47
DQMA5
QSA5
QSA#5

Channel A1, Data Group 6
MDA48
MDA49
MDA50
MDA51
MDA52
MDA53
MDA54
MDA55
DQMA6
QSA6
QSA#6

Channel A1, Data Group 7
MDA56
MDA57
MDA58
MDA59
MDA60
MDA61
MDA62
MDA63
DQMA7
QSA7
QSA#7

Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: VRAM A Upper

Size: Custom | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

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MLPS

Pin Name	Type	PD/PU	Description
GPIO_0	I/O 3.3 V (VDDR3)	PD-reset	Power-state indicator. Permits the voltage regulator to activate power-saving features. IF VR Suport PSI# and DPRSLPVR PU 10K to +3VGS. PSI# :Low load current flag DPRSLPVR : Deeper sleep enable flag
GPIO_5_AC_BATT	I/O 3.3 V (VDDR3)	PD-reset	(Optional) An input which allows the system to request a fastpower reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCNTL_0 GPIO_20_PWRCNTL_1 GPIO_29 GPIO_30	I/O 3.3 V (VDDR3)	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At reset, these signals will be inputs with weak internal pulldown resistors. The VBIOS can define all voltage-control signals to be either 3.3-V or open-drain outputs (all signals must be the same type). The output states (high/low) of these pins are programmable for each AMD PowerPlay state when they are used as voltage control signals. Note: GPIO_29 and GPIO_30 are only available on 28-nm ASICs, and are NC on earlier generation ASICs.
GPIO_8_ROMSO	I 3.3 V (VDDR3)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output. Design: No use external VGA ROM, so use the test point
GPIO_9_ROMSI	O 3.3 V (VDDR3)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK			Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB			BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations. Design: No use external VGA ROM, so use the test points.
GPIO_17_THERMAL_INT	I/O 3.3 V (VDDR3)	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTb).
GPIO_19_CTF	O 3.3 V (VDDR3)	PD-reset	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. The CTF setpoint is 109℃ by default, and is programmed during ASIC initialization. See the advisory for AMD PowerPlay states for more details.
GPIO_21	I/O 3.3 V (VDDR3)	PD-reset	(Optional) Voltage control signal for the memory-voltage regulator. Note: This signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_28_FDO	I/O 3.3 V (VDDR3)	PD-reset	Disable MLPS: PU 10K ohm to 3.3V. (Do not install for Mars) Enable MLPS: PD 10K ohm to GND. (Install for Mars)
CLKREQB	O		Supports the CLKREQB feature for saving power to turn on/off the REFCLK clock on the ASIC.
PX_EN	O	PD	On/off regulator switch in AMD PowerXpress? (switchable graphics) BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is deasserted.

MLPS Bit	Strap Name	Legacy	Description	Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	GPIO[13:11]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details.	001
PS_0[4]	N/A	GENLK_VSYNC	Reserved for internal use only. Must be 1 at reset.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO_2	Re-defined strap to indicate PCIe GEN3 capability. 1 = PCIe GEN3 supported. 0 = PCIe GEN3 not supported.	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO_8	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	GENLK_CLK	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	TX_PWRS_ENB	GPIO_0	Transmitter (Tx) power savings enable. 0 = 50% Tx output swing. 1 = Full Tx output swing.	1
PS_1[5]	TX_DEEMPH_EN	GPIO_1	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1
PS_2[1]	N/A	N/A	Reserved.	0
PS_2[2]	N/A	N/A	Reserved.	0
PS_2[3]	BIOS_ROM_EN	GPIO_22	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0
PS_2[4]	BIF_VGA_DIS	GPIO_9	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	N/A	Reserved.	0
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	N/A	Board configuration related strapping (such as memory ID).	Base on VRAM ID
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[0] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	N/A	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	111

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

00 for JET
10 for Topaz

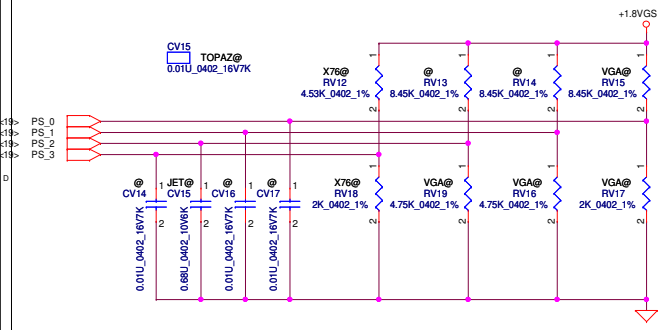
Mapping to VRAM type

Primary Memory Aperture Size Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG [2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not supported
1 GB	Not supported
2 GB	Not supported
4 GB	Not supported

MLPS configuration

Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC



PS_3[3:1]

Memory ID	P/N	Vendor	Configuration	Size
000	SA000068U40	Samsung	K4W2G1646Q-BC1A	1G
001	SA00006H400	Hynix	H5TC2G63FFR-11C	1G
010	SA00005XB00	Micon	MT41K128M16JT-107G:K	1G
011	SA000076P00	Samsung	K4W4G1646D-BC1A	2G
100	SA00006E800	Hynix	H5TC4G63AFR-11C	2G
101	SA000065D00	Micon	MT41K256M16HA-107G:E	2G

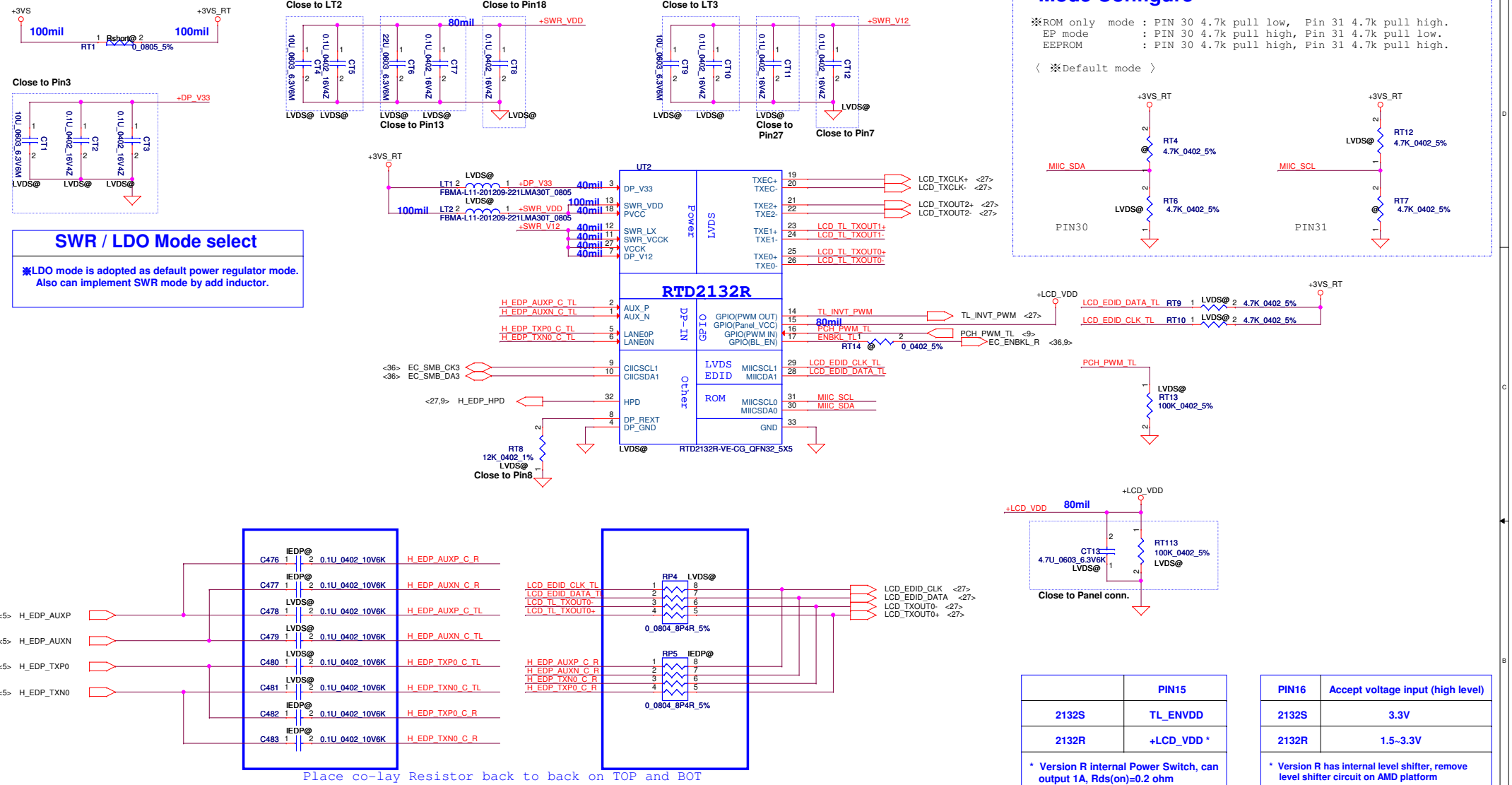
Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: JET_MSIC

Size: Custom | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

Date: Monday, February 10, 2014 | Sheet 25 of 52



	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

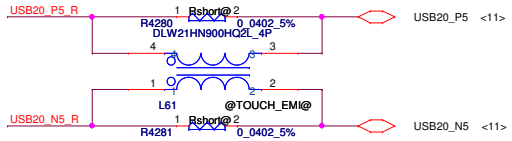
PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

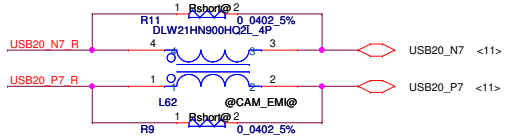
Different between 2132S and 2132R(N)	
2132S	2132R(N)
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/09/25	Deciphered Date 2016/09/25	Title: LVDS Translator - RTD2132R(N)-CG
			Size: Custom; Document Number: ZSWAA/ZCWAA LA-B301P; Rev: 1.0
			Date: Monday, February 10, 2014; Sheet 26 of 52

BTO : TOUCH_EMI@



EMI request - Close to JLVDS connector



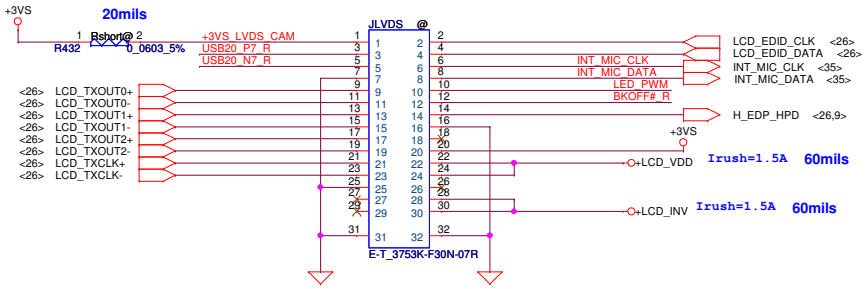
Change L62 P/N from SM070003Y00 to SM070003K00

LVDS colay eDP cable

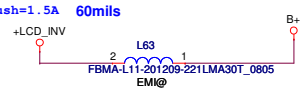
Pin define will be change after ME ready

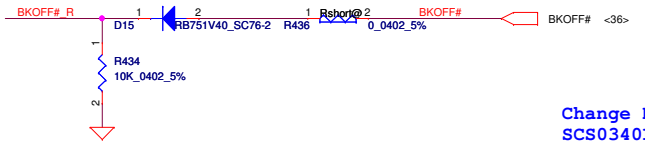
Camera

20mils



Irush=1.5A 60mils



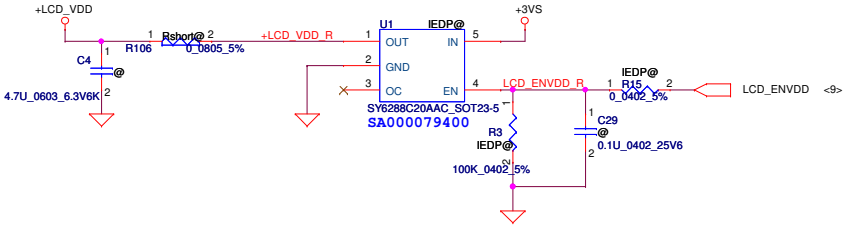


Change D15,D90,D91 P/N from SCS0340L010 to SCS00003500 for X code.

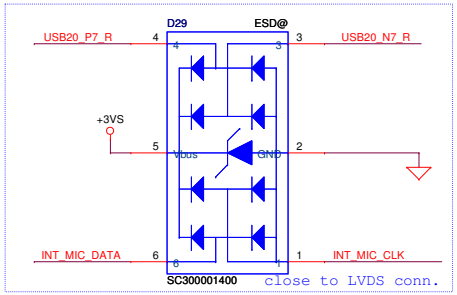
LCD POWER CIRCUIT (For EDP panel only)

I rush=2A

W=80mils

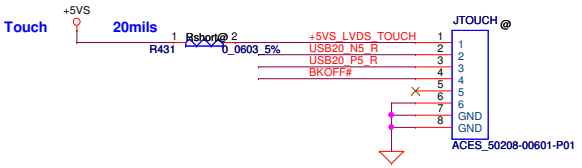


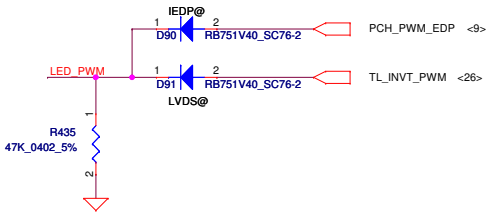
Camera & MIC

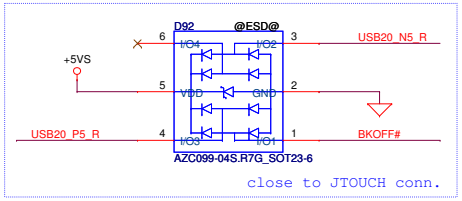


Touch

20mils







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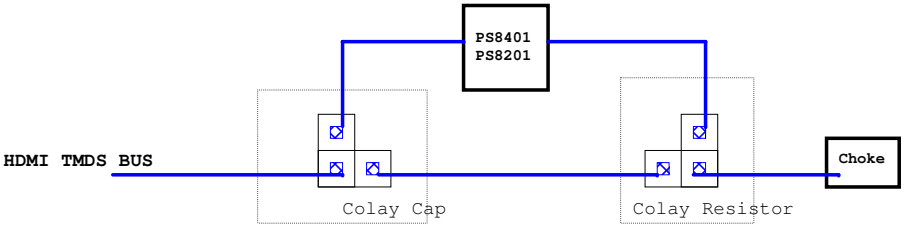
Issued Date	2013/09/25	Deciphered Date 2016/09/25	Title: LVDS

Size: Custom	Document Number: ZSWAA/ZCWAA LA-B301P		Rev: 1.0
Date: Monday, February 10, 2014	Sheet 27 of 52		



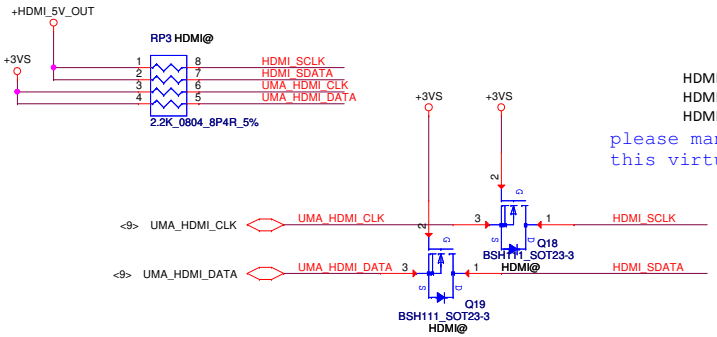
Componet close to Conn.
Impedance depend on platform design guide

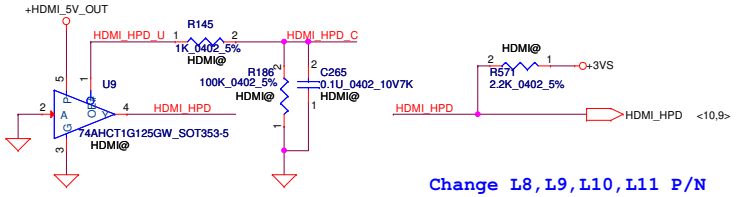
HDMI Royalty

ZZZ HDMI45@
RO0000003HM
HDMI W/Logo + HDCP

HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

please manually load
this virtual material to 45@ BOM

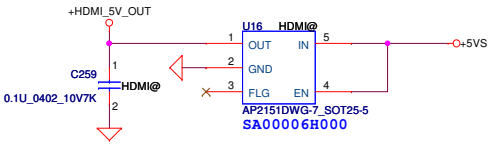


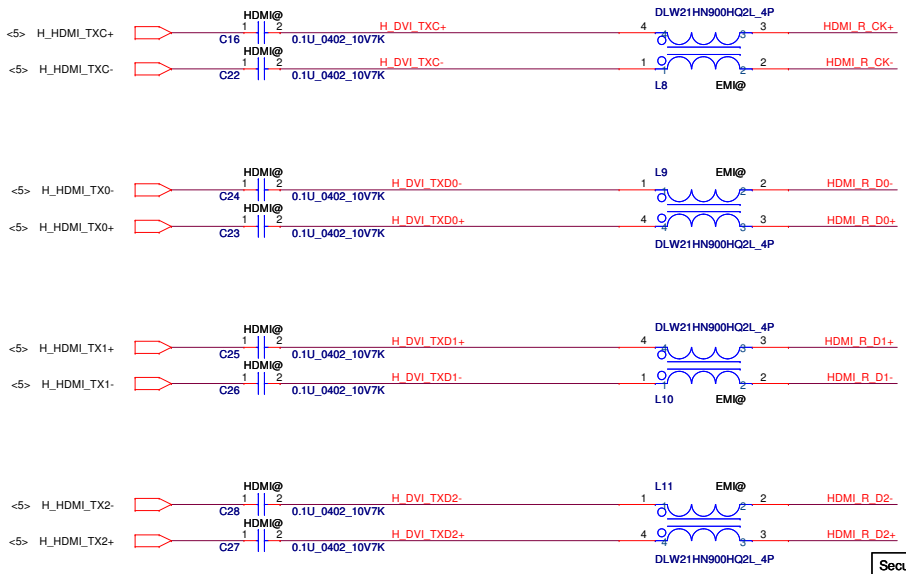


Change L8,L9,L10,L11 P/N
from SM070003Y00 to SM070003K00

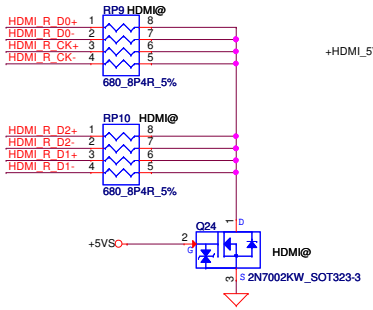
HDMI POWER CIRCUIT

VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A

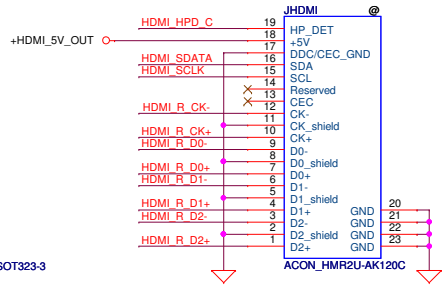




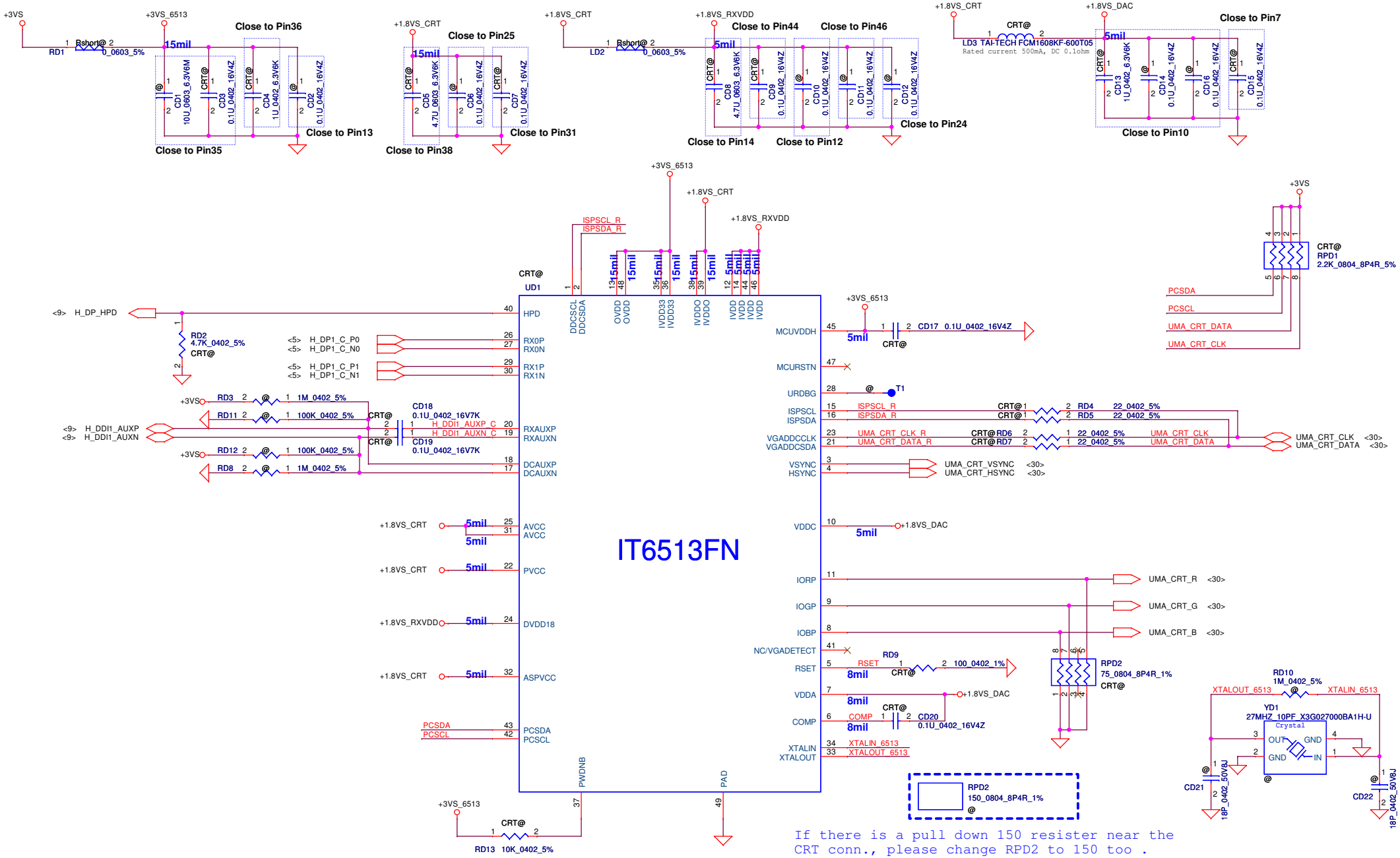
Common CHOKE use 90ohm



HDMI Connector



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: HDMI Conn.
Size: B	Document Number: ZSWAA/ZCWAA LA-B301P		Rev: 1.0
Date: Monday, February 10, 2014	Sheet 28 of 52		



If there is a pull down 150 resister near the CRT conn., please change RPD2 to 150 too .

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	

Title	DP-CRT_ITE IT6513FN	
Size	Document Number ZSWAA/ZCWAA LA-B301P	Rev 1.0
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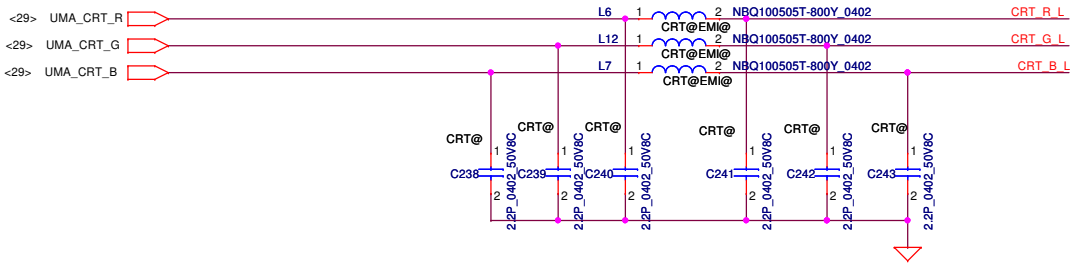
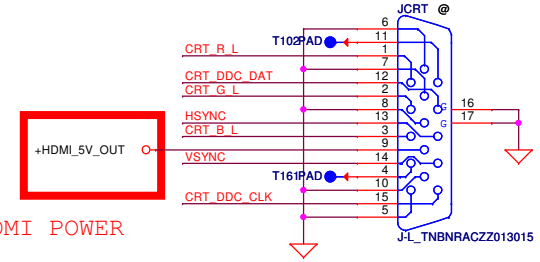
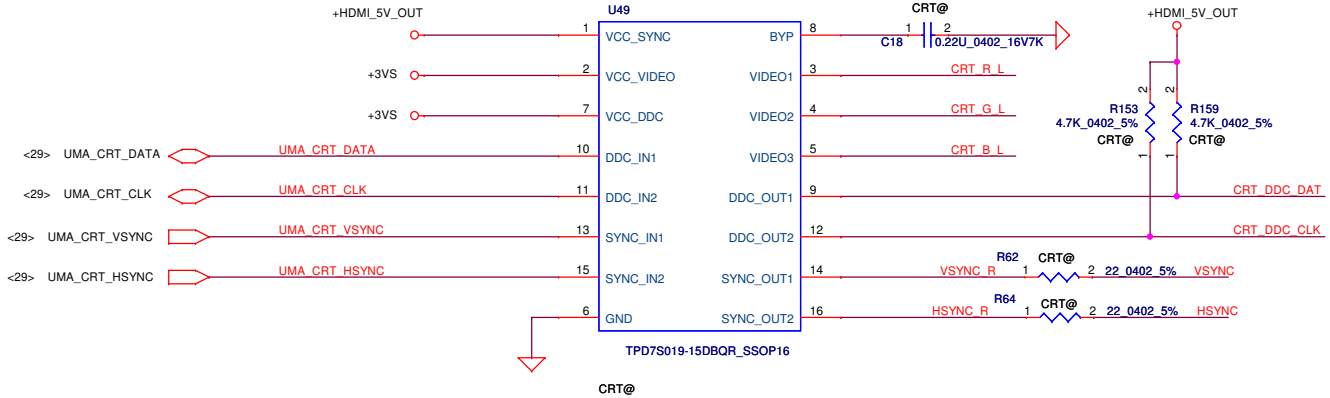
CRT CONNECTOR





USE HDMI POWER



Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: *CRT*

Size | Document Number: **ZSWAA/ZCWAA LA-B301P** | Rev: 1.0

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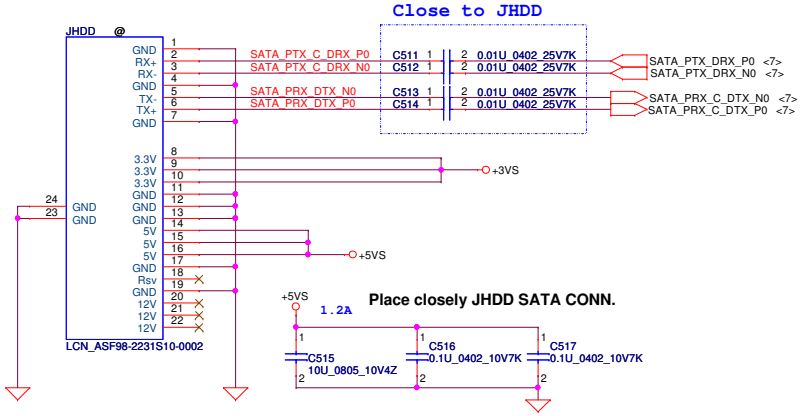
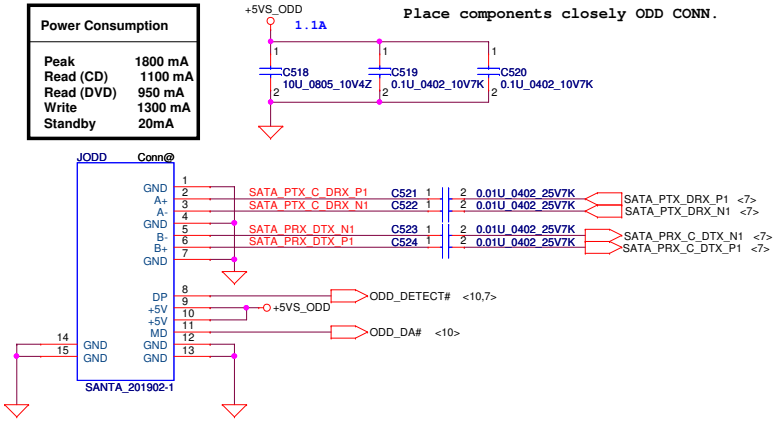
SATA HDD/SSD Conn.



SATA ODD Conn

Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA



Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: SATA HDD/SSD/ODD

Size | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

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NGFF-Slot1-E-Key-WLAN

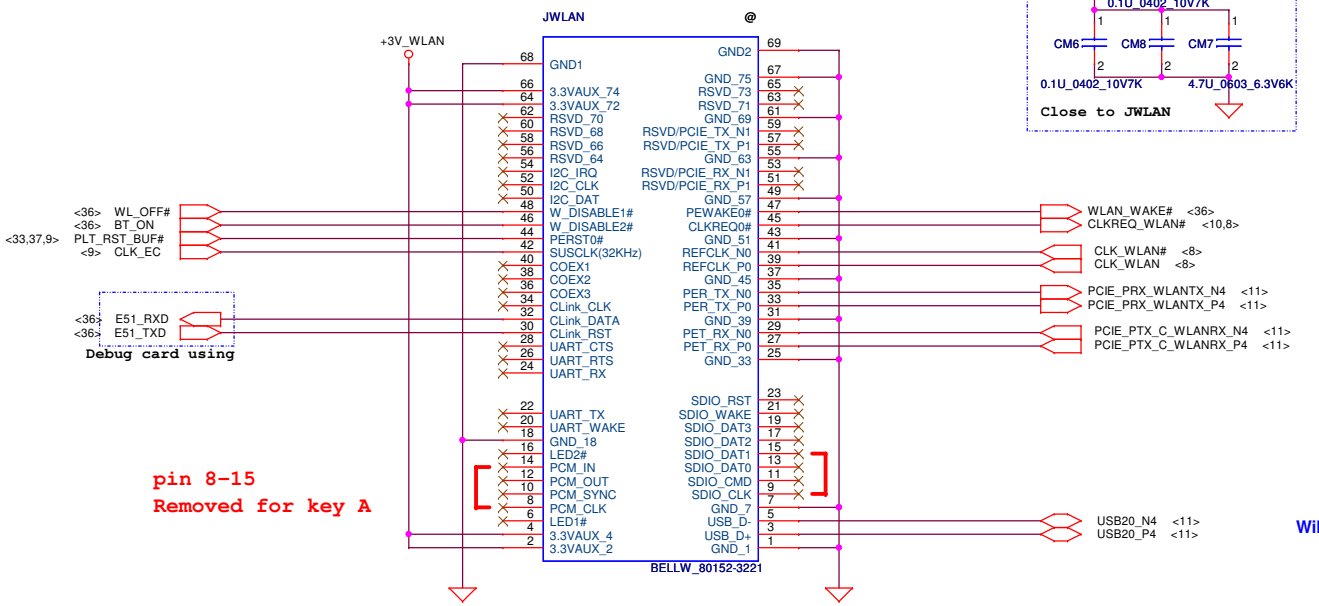

Table 23. SDIO Based Module Solution Pinout (Module Key E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UIM_Power_In/GPIO1/PEWake1#	RESERVED/REFCLKP1	71
68	UIM_Power_Out/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	Reserved/PETn1	67
64	RESERVED	Reserved/PETp1	65
62	ALERT# (O)(0/3.3)	GND	63
60	I2C CLK (I)(0/3.3)	Reserved/PERn1	61
58	I2C DATA (IO)(0/3.3)	Reserved/PERp1	59
56	W_DISABLE#1 (I)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (I)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
50	SUSCLK(32kHz) (I)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKN0	49
46	COEX2(I/O)(0/1.8V)	REFCLKP0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PETn0	43
40	VENDOR DEFINED	PETp0	41
38	VENDOR DEFINED	GND	39
36	UART CTS (I)(0/1.8V)	PERn0	37
34	UART RTS (O)(0/1.8V)	PERp0	35
32	UART Rx (I)(0/1.8V)	GND	33
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
22	UART Tx (O)(0/1.8V)	SDIO Reset(I)(0/1.8V)	23
20	UART Wake (O)(0/3.3V)	SDIO Wake(O)(0/1.8V)	21
18	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED#2 (O)(OD)	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC/I2S WS (IO)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK/I2S SCK (IO)(0/1.8V)	SDIO CLK(I)(0/1.8V)	9
6	LED#1 (O)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

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Issued Date	2013/09/25	Deciphered Date	2016/09/25

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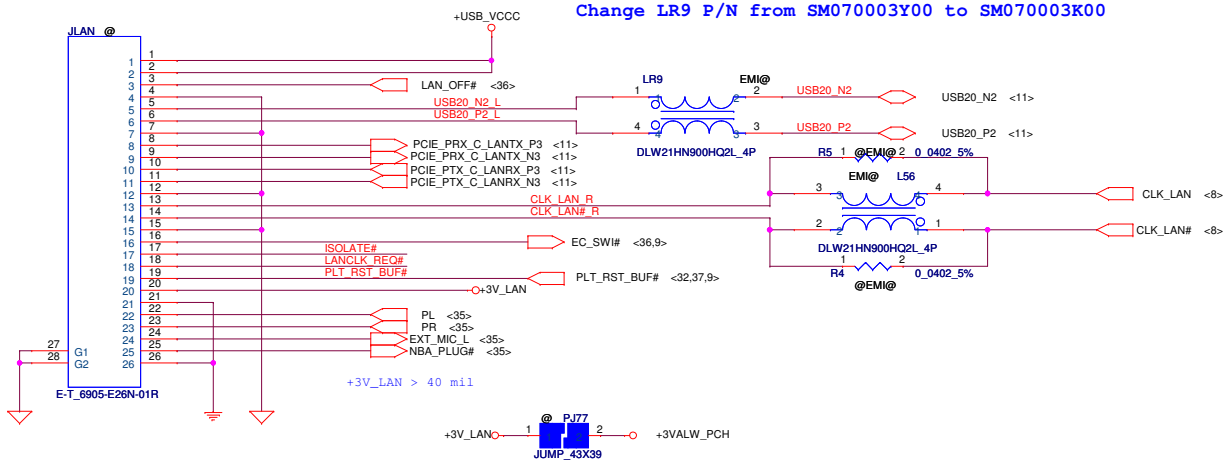
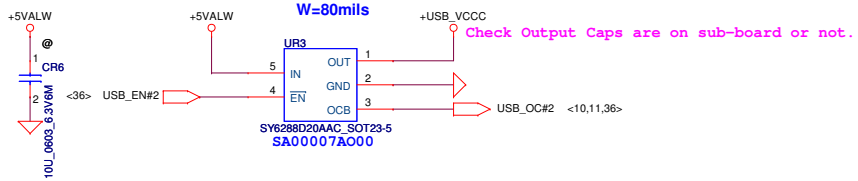
LAN/USB Small board Conn

Left USB 2.0 x 1

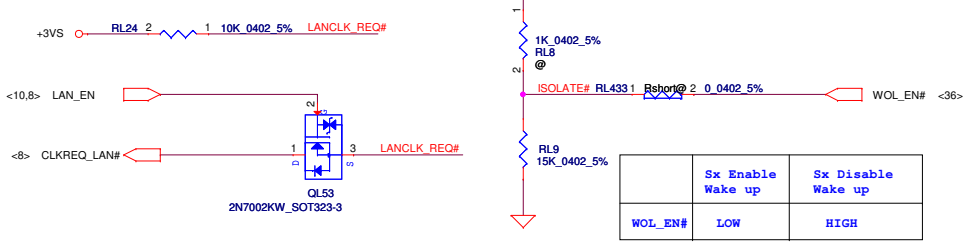
Current Limit 2A

Change LR9 P/N from SM070003Y00 to SM070003K00





For LAN function



	Sx Enable Wake up	Sx Disable Wake up
WOL_EN#	LOW	HIGH

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

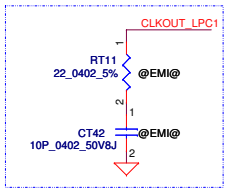
*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

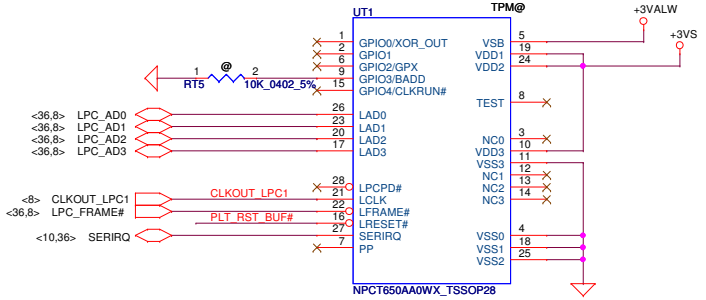
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

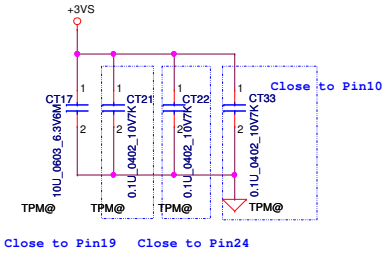
TPM

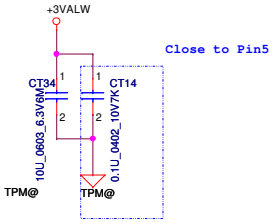
BADD	ADDRESS
0	EEh - EFh
* Floating	7Eh - 7Fh

For EMI









Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: TPM

Size: | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

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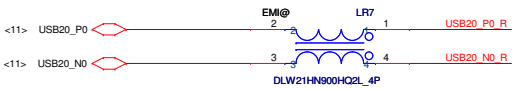
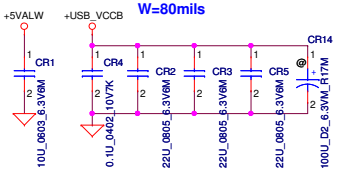
Right rear USB2.0 Conn.



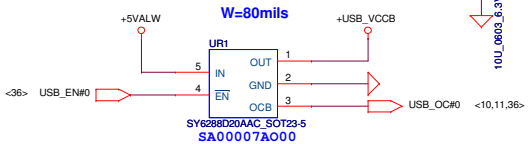
CLOSE UR1

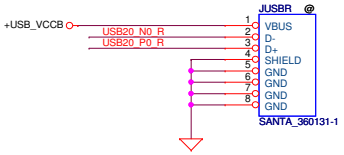
W=80mils



Current Limit 2A

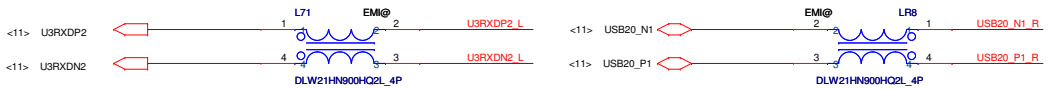
W=80mils

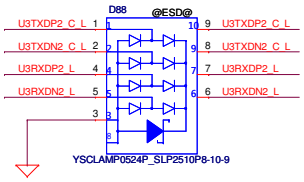




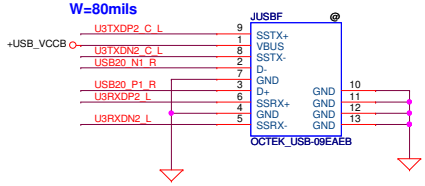
Right side USB 3.0 x 1 W/O Sleep&Charge

Change L71,L72,LR7,LR8 P/N
from SM070003Y00 to SM070003K00





W=80mils



Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: RUSB/S&C

Size: Custom | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

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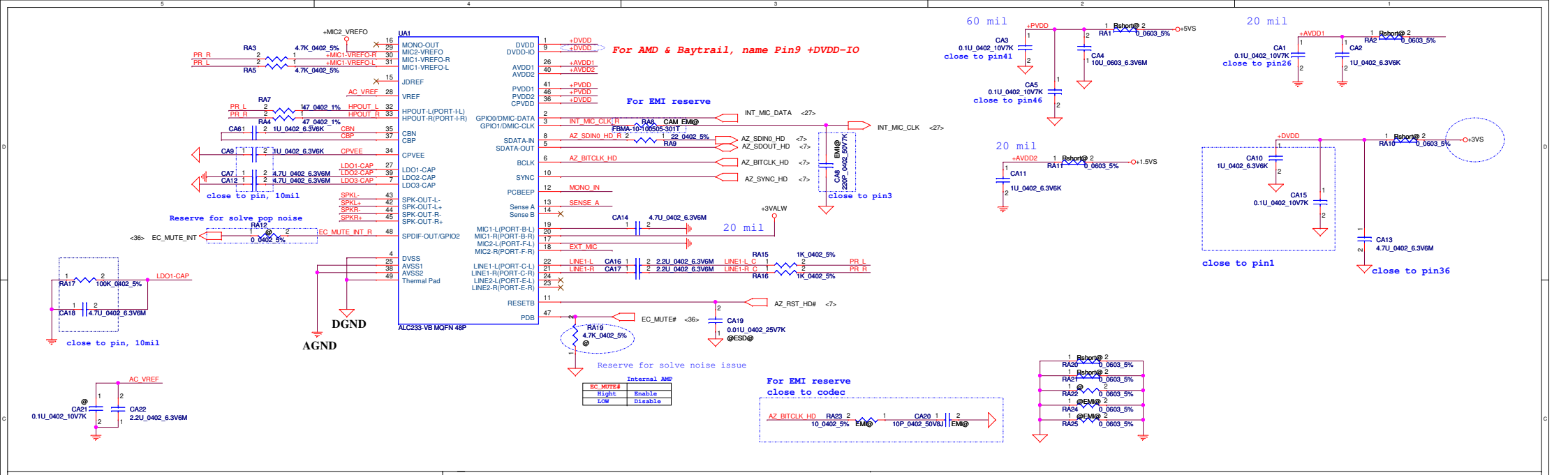
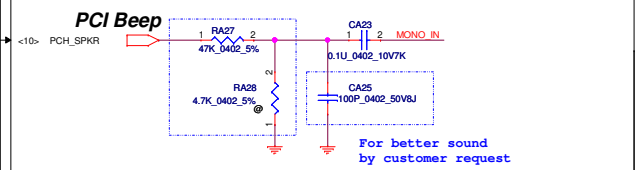
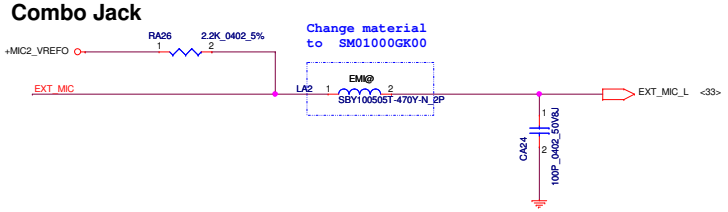


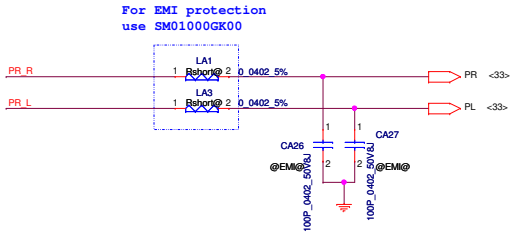
Beep sound

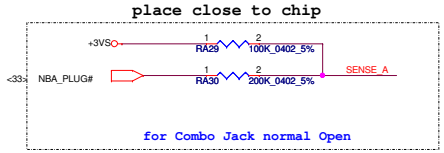


(ALC233 supported IPhone headset/ Headphone/ MIC in)

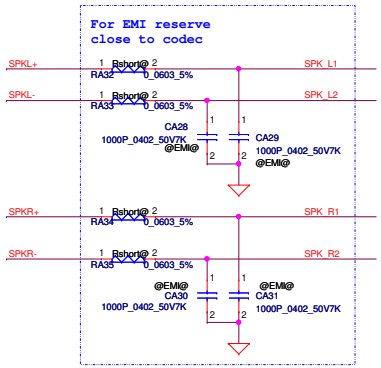
Combo Jack



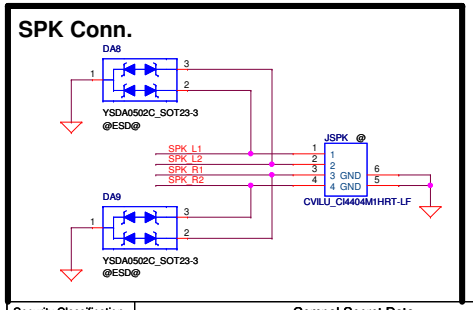




SPK



SPK Conn.

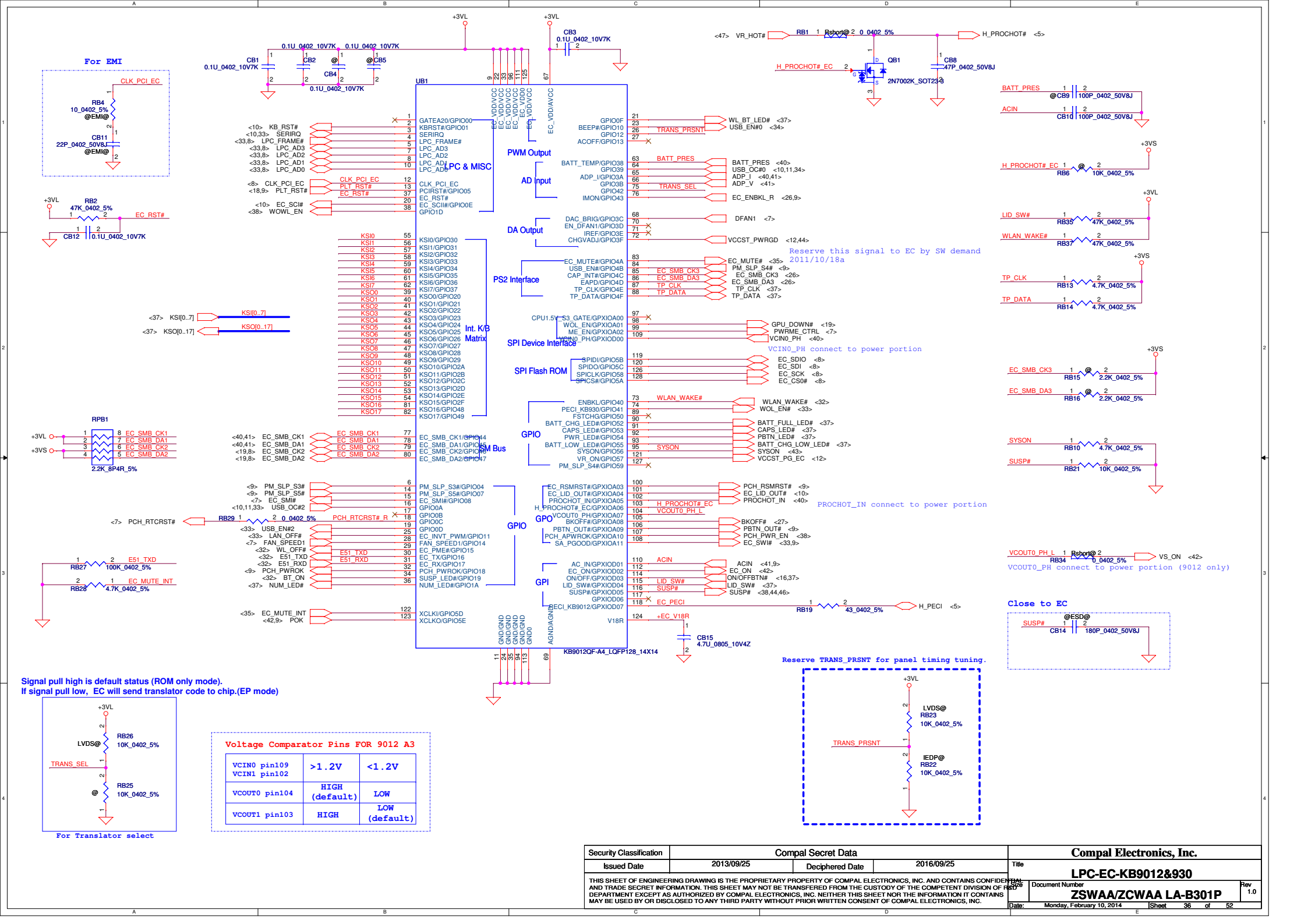


EXT_MIC、EXT_MIC_L、RING2、RING2_L
Speaker 4 ohm: 40mil
Speaker 8 ohm: 20mil

RA13、LA2、CA24
close to small board connector

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.	
Title	ALC233/233VB
Size	Document Number: ZSWAA/ZCWAA LA-B301P
Rev	1.0
Date: Monday, February 10, 2014	Sheet 35 of 52



Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: LPC-EC-KB9012&930

Size: C | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

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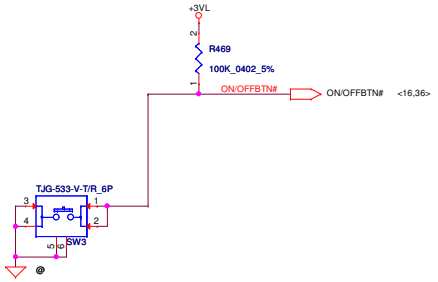
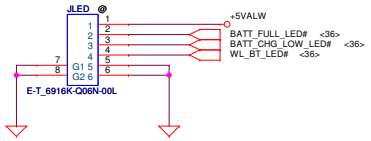
Power Button

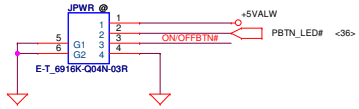


LED Small board to Conn

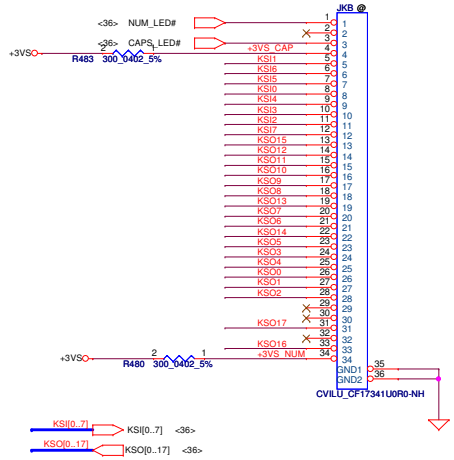


PBTN/B to M/B

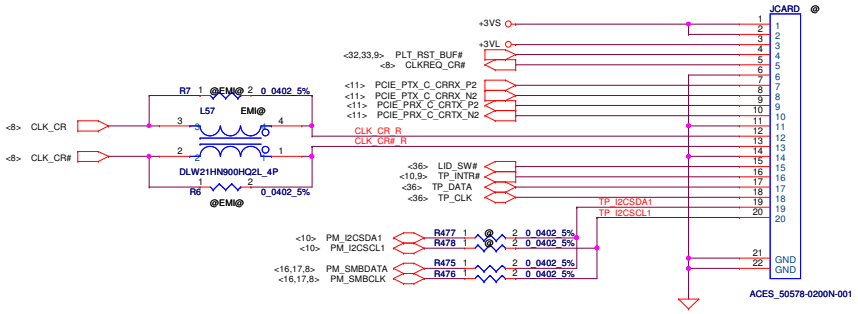
NOTICE: ON/OFFBTN# have pull-high resistance on motherboard



KEYBOARD CONN.



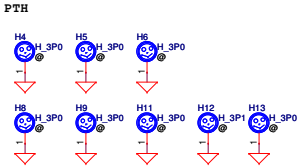
Card Reader + TP + Lid SW



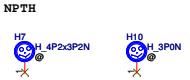
Screw Hole

CPU

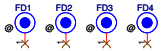
PTH



NPTH



PCB Fedical Mark PAD



ISPD

ZZZ
DAZ15H00100
PCB LA-B301PR10

CPU

R1 PN

UC1 4005UR1@ SA000072Q70 I3-4005U
UC1 4200UR1@ SA00006SM80 I5-4200U
UC1 4010UR1@ SA00006SXA0 I3-4010U
UC1 2990UR1@ SA00007LM00 2990U
UC1 4210UR1@ SA00007LO00 I5-4210U
UC1 4015UR1@ SA00007LN00 I3-4015U

R3 PN

UC1 4005UR3@ SA000072Q60 I3-4005U
UC1 4200UR3@ SA00006SM90 I5-4200U
UC1 4010UR3@ SA00006SX90 I3-4010U

GPU

UV1 TOPAZ@
TOPAZ XT S3 FCBGA 631P GPU 0FD

UV1 JET@
JET PRO S3 FCBGA 631P GPU 0FD

Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

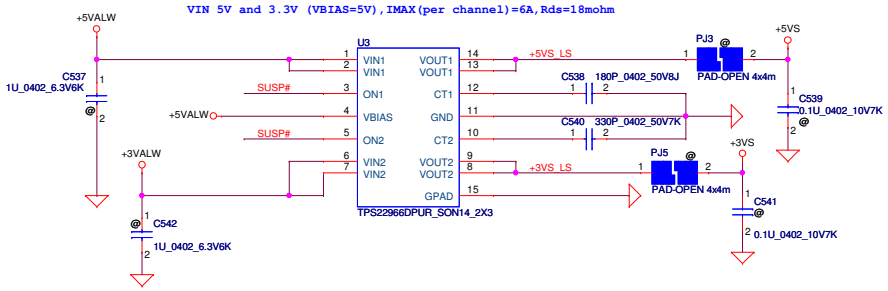
Compal Electronics, Inc.

Title: TP/ISPD/KB/Screw

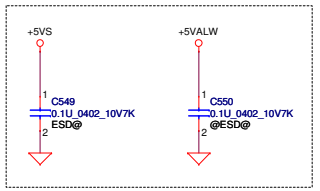
Size | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

Date: Monday, February 10, 2014 | Sheet 37 of 52

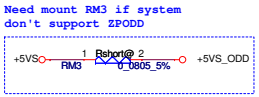
+3VALW TO +3VS
+5VALW TO +5VS
Load Switch

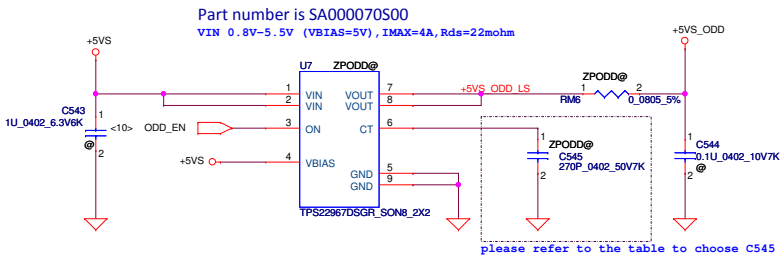


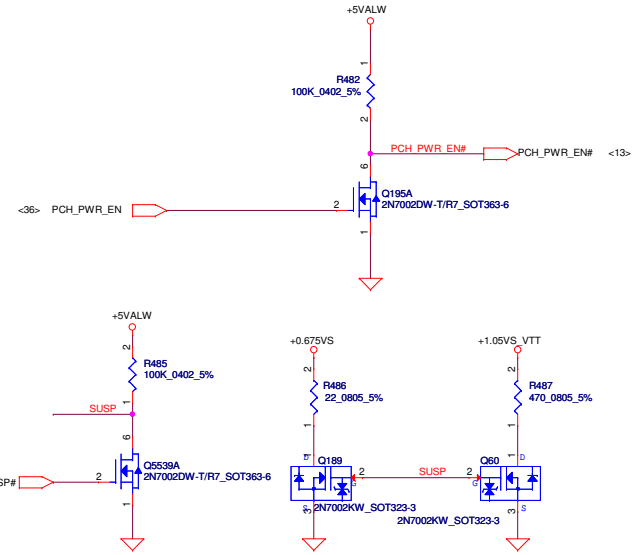
For ESD



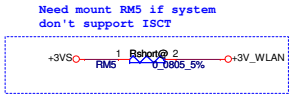
+5VS TO +5VS_ODD

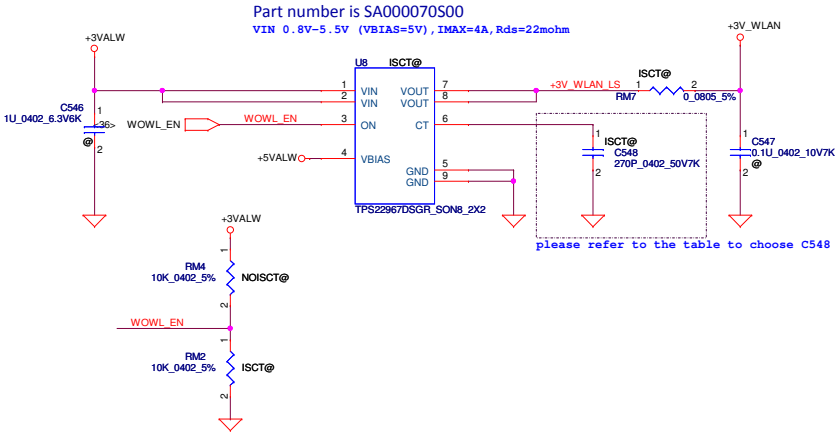






+3VALW TO +3V_WLAN
for WOWL





Security Classification	Compal Secret Data		
Issued Date	2013/09/25	Deciphered Date	2016/09/25

Compal Electronics, Inc.

Title: DC-DC INTERFACE

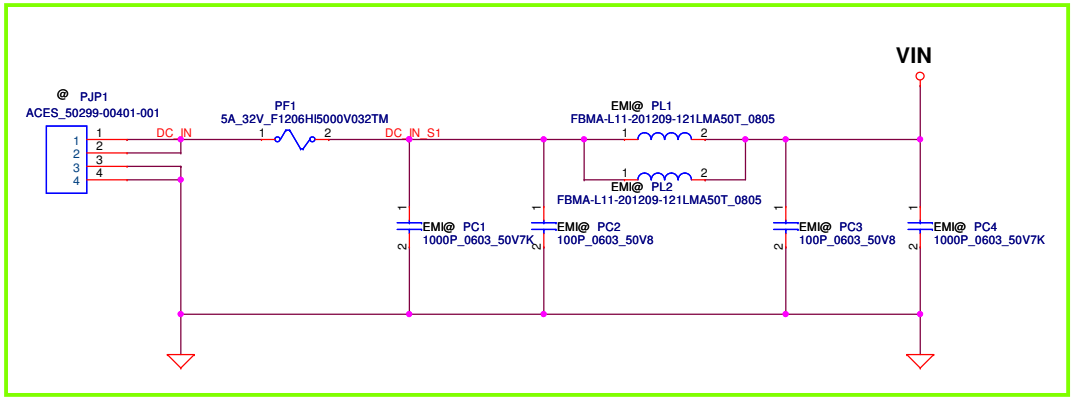
Size | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

Date: Monday, February 10, 2014 | Sheet 38 of 52

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Support 37.1
RTC 38.2
EMI Part 47.1



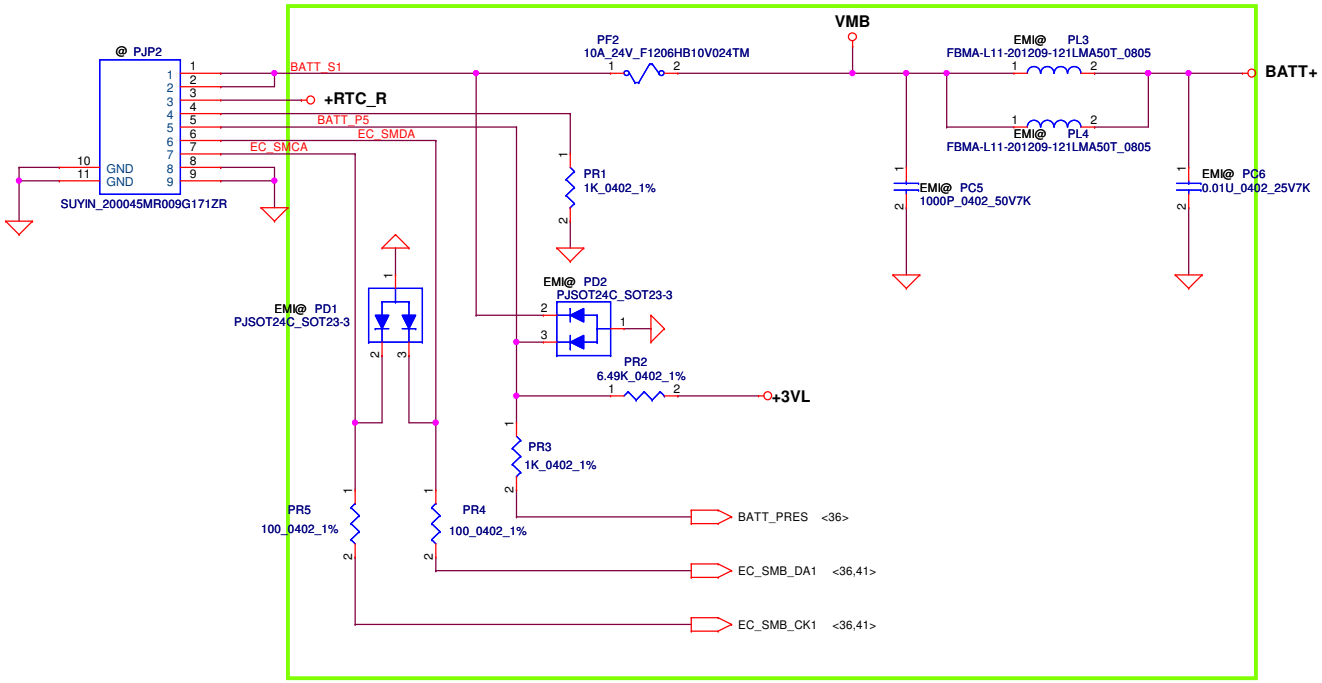
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: DCIN

Size: A3	Document Number: ZSWAA/ZCWAA LA-B301P		Rev: 1.0
Date: Monday, February 10, 2014	Sheet 39 of 52		

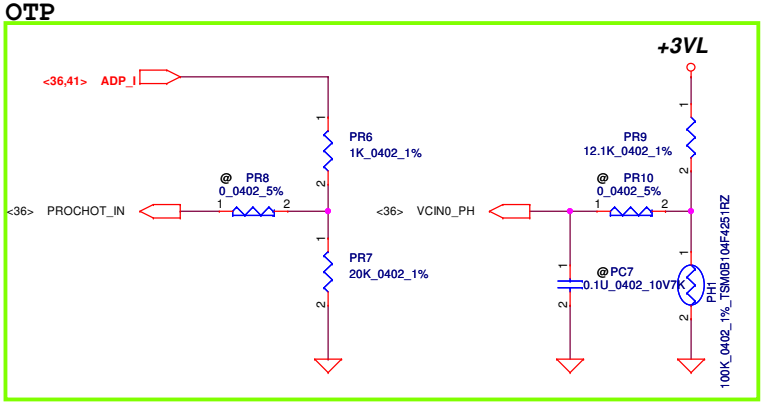
Mark Green frame that means this part is not belong to layout module part .

Function Field :

Support 37.1
OTP 39.7
EMI Part 47.1
ESD DIODE 47.2



OTP



	Initial	Recovery
45W UMA	0.55V	0.43V

	Initial	Recovery
CPU OTP	90 C	70 C

Compal Electronics, Inc.

Title: Battery Conn / OTP

Size: A3 | Document Number | Rev: 1.0

Date: Monday, February 10, 2014 | Sheet 40 of 52

Module model information

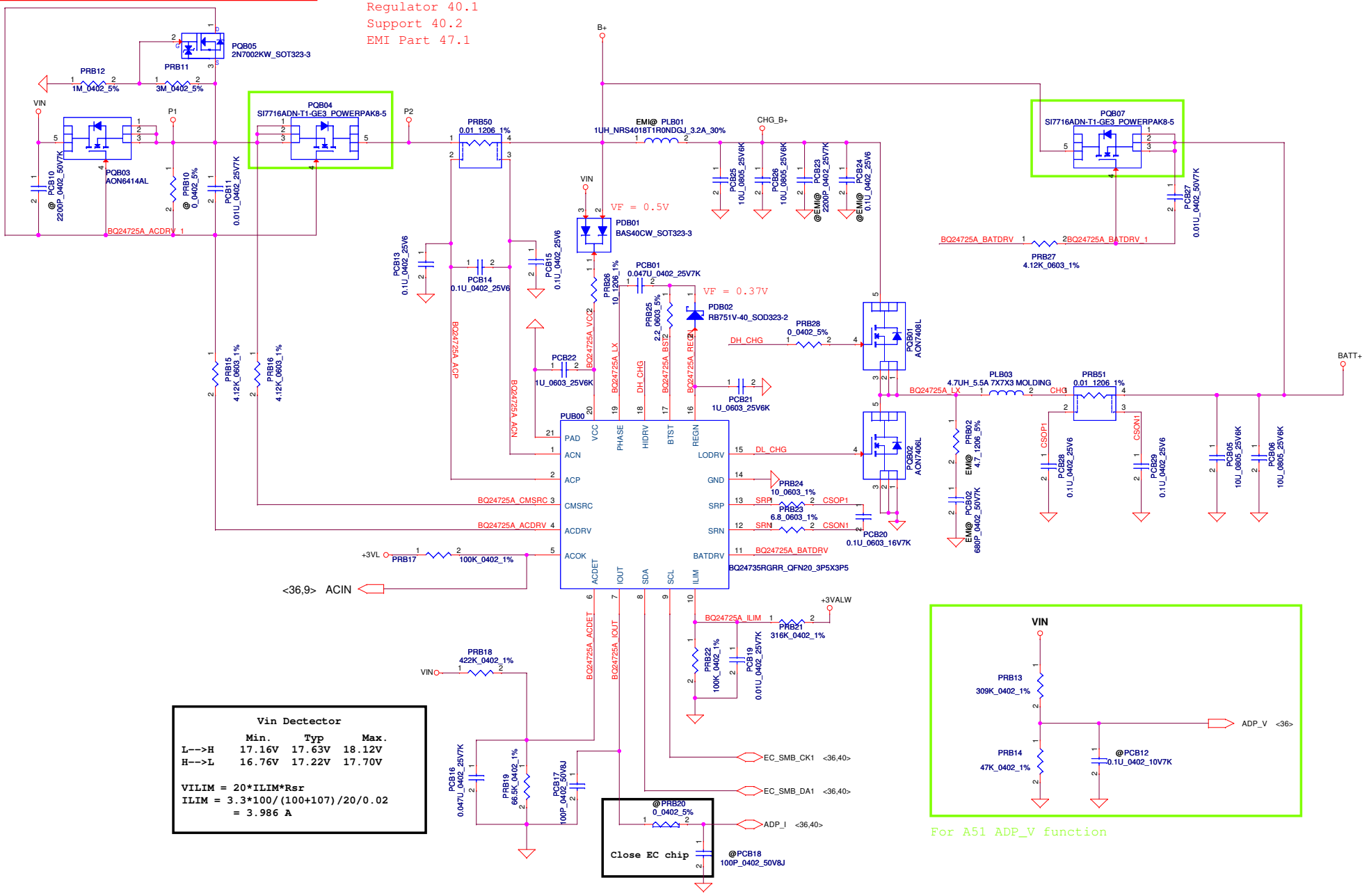
BQ24735A_V1.mdd

BQ24735A_V2.mdd

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 40.1
Support 40.2
EMI Part 47.1



Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+107)/20/0.02
= 3.986 A

For A51 ADP_V function

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

Date: Monday, February 10, 2014 | Sheet 41 of 52

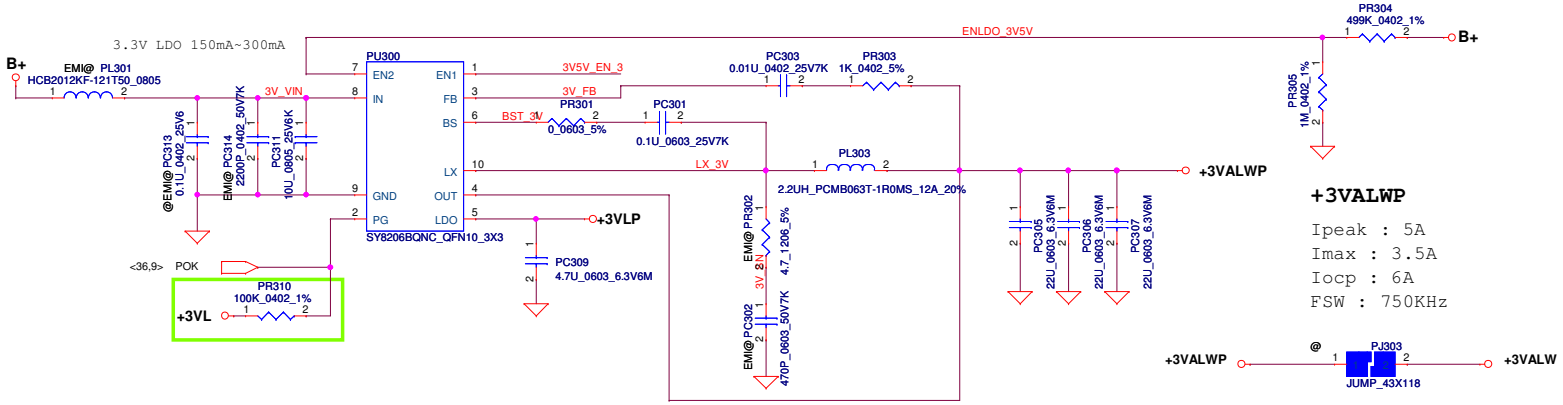
Module model information

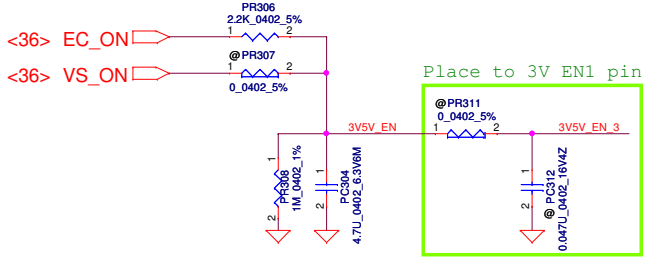
SY8206B_V2.mdd

Mark Green frame that means this part is not belong to layout module part .

Function Field :

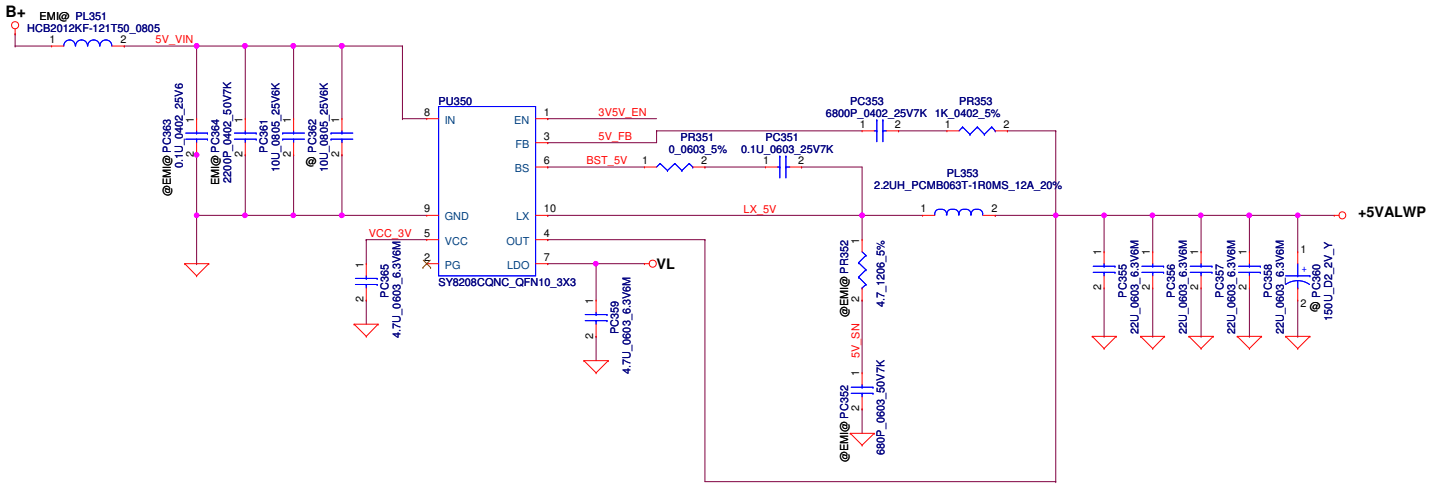
Regulator 35.1
Support 35.2
EMI Part 47.1





Module model information

SY8208C_V2.mdd



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: +3VALW / +5VALW

Size: Custom	Document Number: ZSWAA/ZCWAA LA-B301P		Rev: 1.0
Date: Monday, February 10, 2014	Sheet 42 of 52		

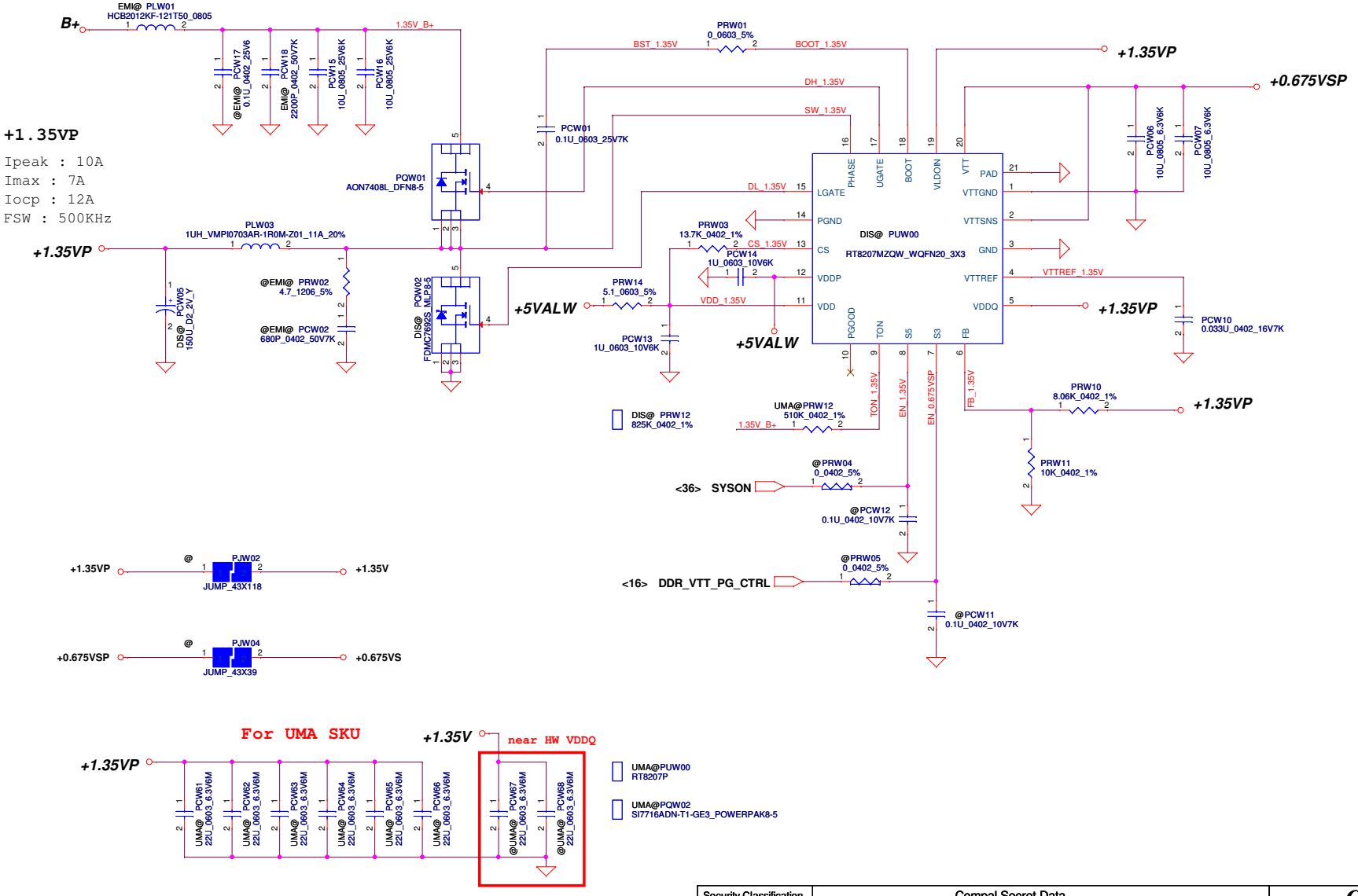
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 35.3
Support 35.4
EMI Part 47.1



Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: +1.35V / +0.675VS

Size: Custom | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

Date: Monday, February 10, 2014 | Sheet 43 of 52

Module model information

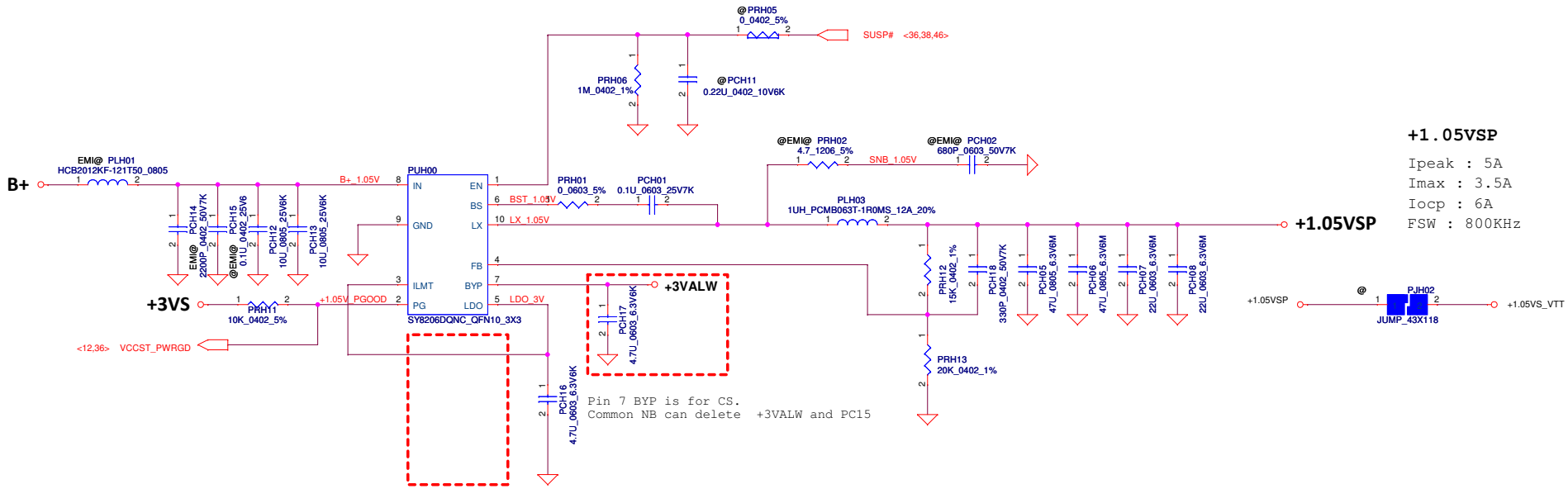
SY8206D_V1.mdd

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 35.5
Support 35.6
EMI Part 47.1

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



+1.05VSP

Ipeak : 5A
Imax : 3.5A
Iocp : 6A
FSW : 800KHz

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: +1.05VS

Size: Custom	Document Number: ZSWAA/ZCWAA LA-B301P		Rev: 1.0
Date: Monday, February 10, 2014	Sheet 44 of 52		

Module model information

SY8033_V1.mdd

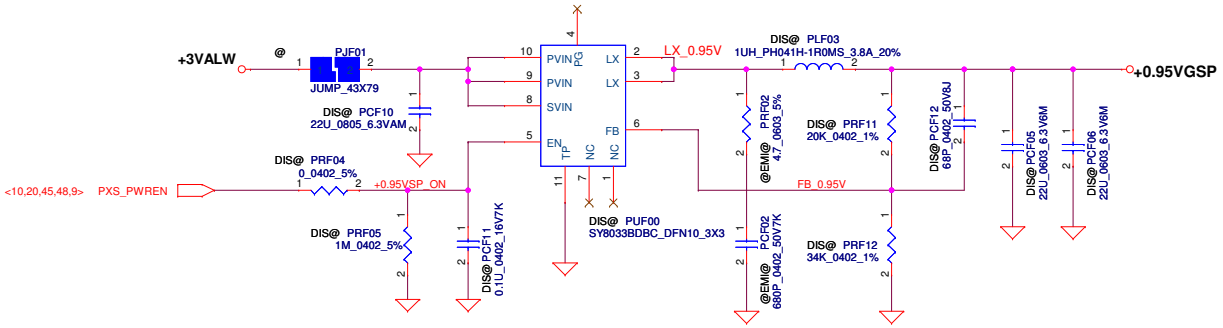
Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 35.15
Support 35.16
EMI Part 47.1

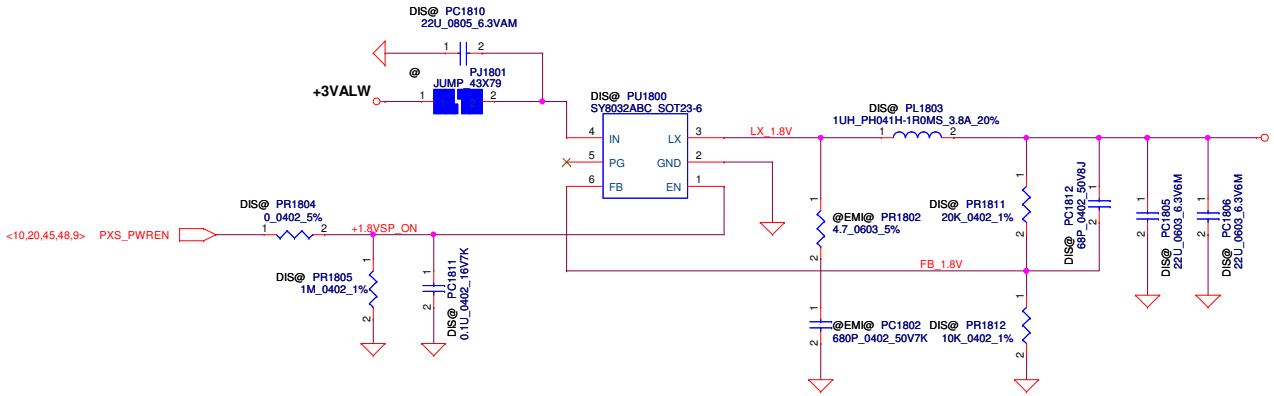
+0.95VGSP

Ipeak : 3A
Imax : 2.1A
Iocp : 4A
FSW : 1MHz



+1.8VGSP

Ipeak :1A
Imax : 0.7A
Iocp : 2.5A
FSW : 1MHz



Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: +0.95VGS / +1.8VS
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			Date: Monday, February 10, 2014; Sheet 45 of 52

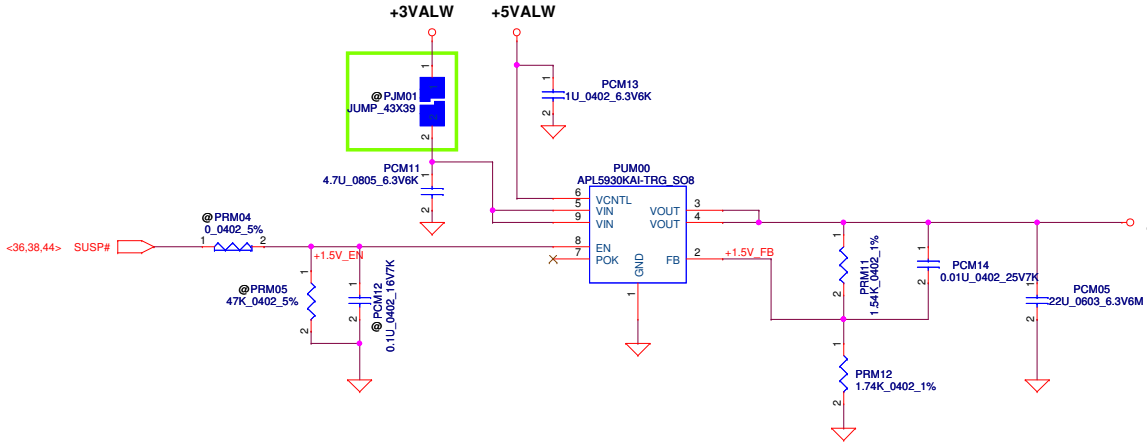
Module model information

APL5930_V1.mdd

Mark Green frame that means this part is not belong to layout module part .

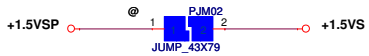
Function Field :

Regulator 35.31
Support 35.32
EMI Part 47.1



+1.5VSP

Ipeak : 0.5A
Imax : 0.35A
Iocp : 4.2A



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: +1.5VS
Size: Custom	Document Number: ZSWAA/ZCWAA LA-B301P		Rev: 1.0
Date: Monday, February 10, 2014	Sheet 46 of 52		

Module model information

TPS51622_V2A.mdd for IC portion
TPS51624_V2B.mdd for SW portion

Mark Green frame that means this part is not belong to layout module part .

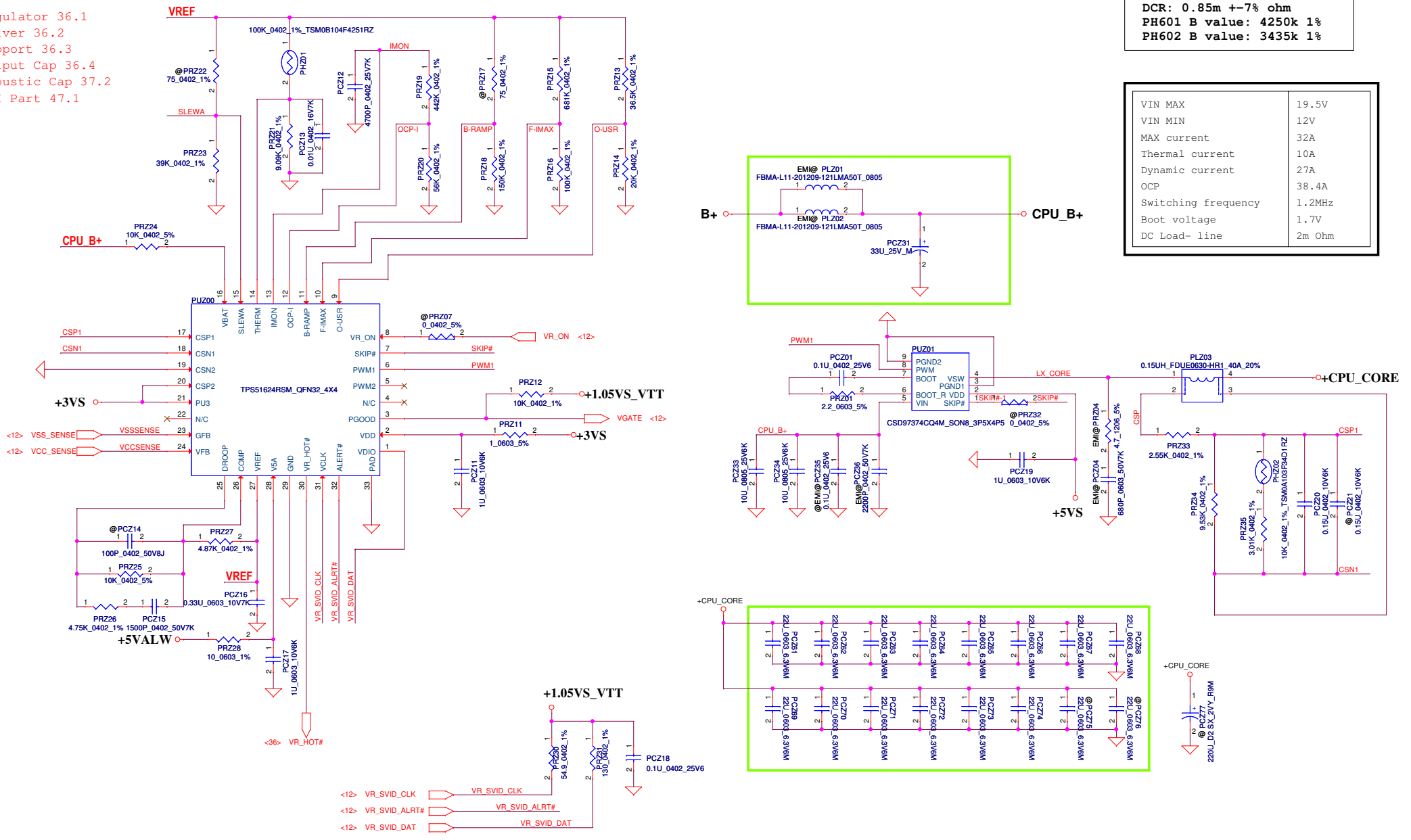
VR_HOT#
PR606 10K ohm for 100 degree
PR606 8K ohm for 110 degree

Function Field :

Regulator 36.1
Driver 36.2
Support 36.3
Output Cap 36.4
Acoustic Cap 37.2
EMI Part 47.1

CPU
Frequency = 1MHz
OCP Current 39 A
DCR: 0.85m +-7% ohm
PH601 B value: 4250k 1%
PH602 B value: 3435k 1%

VIN MAX	19.5V
VIN MIN	12V
MAX current	32A
Thermal current	10A
Dynamic current	27A
OCP	38.4A
Switching frequency	1.2MHz
Boot voltage	1.7V
DC Load- line	2m Ohm



Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: CPU_CORE

Size: Custom | Document Number: ZSWAA/ZCWAA LA-B301P | Rev: 1.0

Date: Monday, February 10, 2014 | Sheet 47 of 52

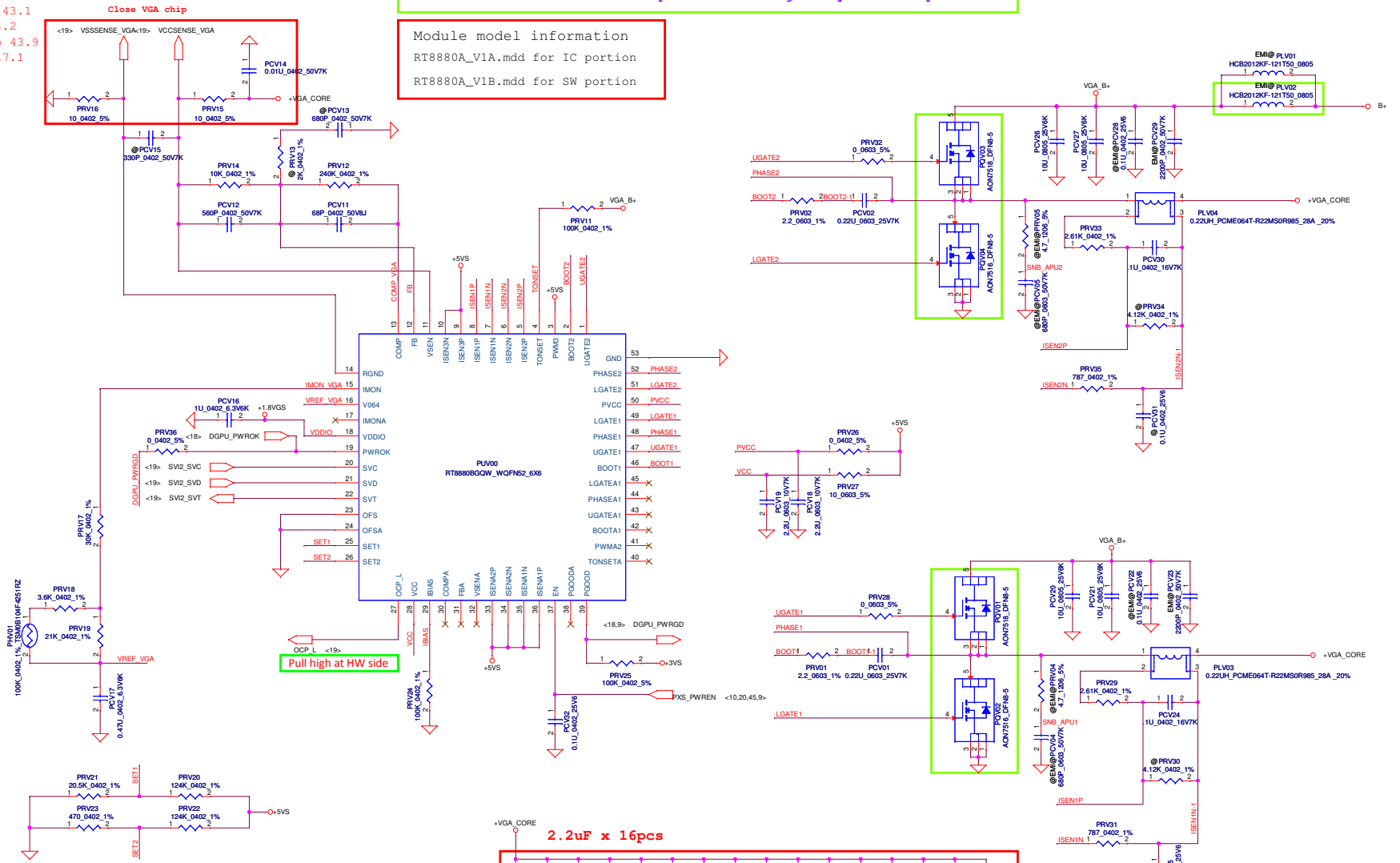
Function Field :

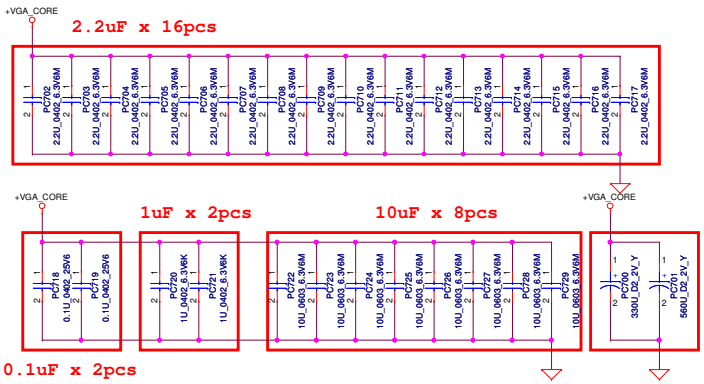
Regulator 43.1
Support 43.2
Output Cap 43.9
EMI Part 47.1

Mark Green frame that means this part is not belong to layout module part .

Module model information
RT8880A_V1A.mdd for IC portion
RT8880A_V1B.mdd for SW portion

Close VGA chip





VGA_CORE
TDC 24A
EDC 36A
OCP current > 43.2A
Load line -1mV/A
FSW=450kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	27mohm ,	34mohm
L/S Rds(on)	5.3mohm ,	6.5mohm

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: VGA_CORE

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PWR PIR (Product Improve Record)

ZSWAA LA-B301P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
PVT GERBER_OUT DATE: 2013/12/02

Item	Date	Page	Action	Component	Request
1)	11/21	48	Change	PRZ12 change to 10K and pull high +1.05VS_VTT	For design change
2)	11/21	48	Delete	PRZ29 removed	HW portion pull high
5)	11/25	41,48	Change	PH1,PHZ01 part number change to SL200002H00	change for common PN
6)	11/25	48	Change	PHZ02 part number change to SL200002F00	change for common PN
7)	11/25	42	Change	change PQB03 to SB00000NW00 AON6414AL	change for allocation
8)	12/03	48	Change	PRZ27 change to 4.87K	change for compensation
9)	12/03	41	Change	PF2 change to 1206 footprint component SP040005P00	for ME limitation
10)	12/03	44	Change	change PQW02 to SB00000GW00 SI7716 at UMA SKU	change for allocation
11)	12/03	48	Change	PRZ19 change to 316K	for CPU core conversation fine tune
12)	12/03	48	Change	PRZ20 change to 56K	for CPU core conversation fine tune

REVISION CHANGE: 0.3
PV REGRESSION GERBER_OUT DATE: 2014/01/06

Item	Date	Page	Action	Component	Request
13)	01/03	40	Change	change DC in jack footprint	for customer request
14)	01/03	43	Add	Add PR312 0ohm 0402	for HW 5V drop fine tune
15)	01/08	43	Change	change PR312 to 15ohm	for HW 5V drop fine tune
16)	01/08	47	Change	change PRZ19 to 442kohm	for CPU core conversation fine tune
17)	01/15	41	Delete	PCB10 2200p	for B2B fine tune
18)	01/15	41	Change	PCB11 0.1u change to 0.01u	for B2B fine tune
19)	01/16	43	Add	PR302,PC302 mount and PC302 change to 470p	for EMI request
20)	01/16	42	change	PCB16 2200p change to 0.047u	for decoupling cap fine tune
21)	01/22	47	Add	PRZ04,PCZ04 mount	for EMI request
22)	01/22	41	Add	PRB02,PCB02 mount	for EMI request
23)	01/22	47	change	PCZ31 100u change to 33u	for sourcer request

REVISION CHANGE: 1.0
Pre-MP GERBER_OUT DATE: 2014/02/10

Item	Date	Page	Action	Component	Request
24)	02/07	42	Delete	remove PR312 15ohm	for HW request
25)	02/07	48	Change	change net name from VREF to VREF_VGA change net name from VREF to IMON_VGA change net name from VREF to COMP_VGA	resolve duplicate net name
26)	02/10	42,44,46	Change	change PR311,PRH05,PRM04 footprint to 0ohm shortpad	common design rule

HW PIR (Product Improve Record)

ZSWAA LA-B301P Schematic Change List
REVISION: 0.1
Gerber-out date: 2013/10/29

Item	Date	Page	Action	Component	Request
1)	10/15	37	Add	CB14 on SUSP#	For ESD request
2)	10/15	16,17	Change	Swap DDR data of JDIMM1 & JDIMM2	For common module layout
3)	10/15	08	Add	RH91 on CLK_REQ_VGA#	For follow AMD GPU reference schematic
4)	10/15	34	Reserve	CR6 to +5VALW	For power switch common design
5)	10/15	35	Add	CR2,CR3,CR5 to +USB_VCCB	For power switch common design
6)	10/16	37	Add	RB11,RB12	For colay EC 9022
7)	10/16	37	Add	RB13,RB14	For colay Normal pad & Click pad
8)	10/17	38	Add	R8,R9	For colay Normal pad & Click pad
9)	10/17	27	Add	R15,C29 on LCD_ENVDD	For tune LCD_VDD sequence
10)	10/18	34	Swap	LR9	For smooth USB signal
11)	10/18	37	Change	DFAN1 to Pin 70	For EC request
12)	10/20	34	Remove	RT2, RT3	For no need
13)	10/22	39	Change	RM5,RM6,RM7 to 0_0805	For max current design
14)	10/22	10	Add	Test point on GPIO10	For SW debug
15)	10/22	07	Add	Test point on GPIO34	For SW debug
16)	10/23	16	Reserve	0_0805	For DQA's experiment
17)	10/23	05	Change	R23 to 121_0402_1%	For Intel check list
18)	10/23	38	Remove	SW2	For layout space concern
19)	10/23	30	Reserve	RD11, RD12	For Intel check list
20)	10/24	08	Change	Y2 to 4 pin	For common part
21)	10/24	10	Add	RH4, RH6, RH9, RH10	For SW request
22)	10/24	26	Change	RT1 from 0603 to 0805	For current concern
23)	10/24	09	Add	RH7, RH8	For SW request
24)	10/24	27	Change	JTOUCH from 4pin to 6pin	For module pin define
25)	10/27	20	Change	QV5 to AO4354	For sourcer request
26)	10/27	34	Change	UT1 P/N to SA00007IO00	For TPM2.0

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ZSWAA LA-B301P Schematic Change List
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Gerber-out date: 2013/12/2

Item	Date	Page	Action	Component	Request
01)	11/22	36	Delete	RA22	For audio codec
02)	11/22	36	Add	Add a reserve 0ohm resistor RA25	For EMI request
03)	11/22	27	Change	Change D15 P/N from SCS00002G00 to SCS00000Z00	For material shortage
04)	11/22	27,29,34,35	Change	Change L10,L11,L62,L71,L72,L8,L9,LR7,LR8,LR9 P/N from SM070003Y00 to SM070003K00	For material shortage
05)	11/22	05	Change	Change R184 from SD013470080 to SD028470080	The same as CRB board
06)	11/26	26	Change	Change RT14 config. from @ to LVDS@	For BKOFF circuit
07)	11/26	09	Change	Change RH19 config. to IEDP@	For BKOFF circuit
08)	11/26	09	Connect	Connect EC_ENBKL_R_CPU to AND GATE U50.1	For BKOFF circuit
09)	11/26	27	Change	Change U50.1 from EC_ENBKL_R to EC_ENBKL_R_CPU	For BKOFF circuit
10)	11/26	27	Change	Change U50 and R433 config. from IEDP@ to always mount	For BKOFF circuit
11)	11/26	27	Change	Change D15 and R436 config. from LVDS@ to @	For BKOFF circuit
12)	11/26	36	Change	Change UB1.26 (EC GPIO12) from NC to TRANS_PRSNT	For BKOFF circuit
13)	11/26	36	Add	Add a pull high 10Kohm (RB23) to +3VL and a pull down 10Kohm (RB22) to GND on TRANS_PRSNT	For BKOFF circuit
14)	11/27	27	Change	Change D15 P/N from SCS00000Z00 to SCS0340L010	For BOM reduce
15)	11/27	29	Change	Change UD1.25, UD1.31, UD1.22, UD1.32 from +1.8VS_RXVCC to +1.8VS_CRT	For DP to CRT translator
16)	11/27	29	Change	UD1.45 pull high from +3VS to +3VS_6513	For DP to CRT translator
17)	11/27	29	Add	Add test point on UD1.37	For DP to CRT translator
18)	11/27	29	Add	Add RPD2 symbol for 150ohm	For DP to CRT translator
19)	11/27	33	Change	Change LAN/USB Small board Connector pin (JLAN.3 to JLAN.6) define	For LAN/USB Small board
20)	11/27	35	Change	Change UA1 all analog outpout net name to PR_L/PR_R	Unify net name
21)	11/27	35	Change	Change CA15 0.1u cap from 16V4Z to 10V7K	Don't need to use 16V4Z
22)	11/27	35	Change	Add net name Line1-L_C & Line1-L_R on UA1 pin 21.22	For trace length table
23)	11/27	35	Detete	Delete ALC233 co-lay component RA6, RA30, UA1	Change to ALC233VB Only
24)	11/27	35	Change	Swap RA21 & RA22 BOM structure	Balance caps alignment
25)	11/28	29	Change	Change test point T2 to a pull high 10Kohm (RD13) to +3VS_6513	For DP to CRT translator
26)	11/28	27	Add	Add a reserved ESD diode (D92) for JTOUCH	For ESD requeset
27)	11/28	07	Change	Change Dual ESD diode (D13) to two single diodes (D16,D17)	For RTC circuit
28)	11/28	07	Change	Change R437.1 connecting from +RTCBATT to +RTCVCC	For RTC circuit
29)	11/29	07	Change	Change R437 from 0ohm to 1kohm	For RTC circuit
30)	11/29	33,37	Change	Change L56,L57 from SM070001U00 to SM070003K00	For EMI request
31)	11/29	33,37	Change	Change L56,L57 from @EMI@ to EMI@	For EMI request
32)	11/29	33,37	Change	Change R4,R5,R6,R7 from EMI@ to @EMI@	For EMI request
33)	11/29	34	Change	Change CR2,CR3,CR5 from 22U_0603 to 22U_0805	For droop issue
34)	11/29	35	Change	Change CA15 from SE076104K80 to SE102104K00	For BOM change
35)	11/29	07	Change	Change R277.2 net name from N113579902 to +RTCBATT_R	For RTC circuit
36)	12/01	33,37	Change	Swap L56,L57 pin define	For layout request
37)	12/01	27	Add	Add R9,R11 on EMI camera choke	For EMI request
38)	12/01	27	Change	Change L62 from CAM_EMI@ to @CAM_EMI@	For EMI request

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HW PIR (Product Improve Record)

ZSWAA LA-B301P Schematic Change List
REVISION: 0.3
Gerber-out date: 2014/01/06

Item	Date	Page	Action	Component	Request
01)	12/12	09	Change	Change RH19 BOM structure from IEDP@ to always mount	For LVDS & eDP cost down plan
02)	12/12	26	Change	Change RT14 BOM structure from LVDS@ to @	For LVDS & eDP cost down plan
03)	12/12	27	Delete	Delete U50,R433	For LVDS & eDP cost down plan
04)	12/12	27	Change	Change D15,R436 BOM structure from @ to always mount	For LVDS & eDP cost down plan
05)	12/12	36	Change	Change RB22 BOM structure from @ to IEDP@	For LVDS & eDP cost down plan
06)	12/12	36	Change	Change RB23 BOM structure from @ to LVDS@	For LVDS & eDP cost down plan
07)	12/12	07	Change	Change R277,D17 BOM structure from always mount to @	For RTC circuit
08)	12/12	07	Change	Change R437 BOM structure from @ to always mount	For RTC circuit
09)	12/30	11	Add	Add two reserved resistors R167,R168	For no use USB over current
10)	12/30	11	Change	Change UC1.AL3 connect to USB_OC#0_R	For no use USB over current
11)	12/30	11	Change	Change UC1.AH2 connect to USB_OC#2_R	For no use USB over current
12)	01/03	34	Add	Add a reserved capacitor CR7 on +USB_VCCB	For USB
13)	01/03	13	Add	Add a jumper PJ2 between +3VALW to +3VALW_PCH	For +3VALW to +3VALW_PCH
14)	01/06	38	Add	Add C549 and C550	For ESD's request
15)	01/06	37	Change	Change JLED footprint from E-T_6916K-Q06N-00L_6P to ACES_51524-0060N-001_6P	For DFX's request
16)	01/06	37	Change	Change JPWR footprint from E-T_6916K-Q04N-03R_4P to ACES_50504-0040N-001_4P	For DFX's request
17)	01/06	35	Change	Change UA1 Compal PN from SA00007BF00 to SA00007BF10	For audio codec
18)	01/07	13	Change	Change CH111,CH112,CH113,Q10,RH3 BOM structure from always mount to @	For +3VALW to +3VALW_PCH
19)	01/14	27	Change	Change D29 BOM structure from @ESD@ to ESD@	For ESD's request

ZSWAA LA-B301P Schematic Change List
REVISION: 1.0
Gerber-out date: 2014/02/10

Item	Date	Page	Action	Component	Request
01)	01/21	07,09,27	Change	Change D90,D91,D15,D16,D21,D17 from SCS0340L010 to SCS00003500.	For X code
02)	01/21	31	Change	Change JHDD footprint from SANTA_191503-1_22P-T to LCN_ASF98-2231S10-0002_22P.	For DFX's request
03)	01/21	37	Change/Add	Change CPU R1 BOM config and add R3 BOM config	For CPU BOM config
04)	01/29	33,36	Add	Add a GPIO pin LAN_OFF# for UB1.25 and connected to JLAN.3	For Disable/Enable LAN chip
05)	01/29	36	Add	Add a GPIO pin PCH_RTCRST#_R for UB1.18 and connected to a 0ohm resistor (RB29) and connected to PCH_RTCRST#.	For RTC reset
06)	01/29	34	Add	Add a reserved capacitor 100uF (CR14) for +USB_VCCB.	For USB droop
07)	02/05	07,09,27,35	Change	Change 0ohm resistor (RH19,R436,R32,R431,R432,RA11, RA1,RA2,RA10,R106) footprint to 0ohm short pad.	For 0ohm short pad
08)	02/05	35	Delete/Change	Delete RA13,RA18 and change UA1.18 to EXT_MIC and UA1.20 to +3VALW	For audio codec
09)	02/05	37	Change	Change SW3 BOM config from mount to un-mount.	For Pre-MP phase
10)	02/06	26,27,29,35	Change	Change 0ohm resistor (RT1,RD1,LD2,RA20,RA21,R4280, R4281,R11,R9) footprint to 0ohm short pad, and BOM config to Rshort@.	For 0ohm short pad
11)	02/07	07,09,12,27 ,35,16,17,36	Change	Change 0ohm resistor (RH19,R65,R178,R235,R174,R211, R212,R231,R436,LA1,LA3,RB34,RB1,R32,R431,R432,RA32, RA33,RA34,RA35,RA11,RA1,RA2,RA10,R106) BOM config to Rshort@.	For 0ohm short pad
12)	02/07	34	Delete	Delete CR7.	For USB droop
13)	02/07	38	Change	Change 0ohm resistor (RM3,RM5) footprint to 0ohm short pad, and BOM config to Rshort@.	For 0ohm short pad
14)	02/10	37	Change	Change screw hole size for H1,H2,H3.	For ME's request

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