Service Manual

Model : LG-A165

Internal Use Only

Service Manual

LG-A165

Date: September, 2010 / Issue 1.0

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1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.

The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc.Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicate 

by the sign. Following information is ESD handling:

- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current – Constant Voltage
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milli watt
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIB	General Purpose Interface Bus
GSM	Global System for Mobile Communications
IPUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop

PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
PSRAM	Pseudo SRAM
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. PERFORMANCE

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Li-ion Polymer, 3.7V 950mAh	
Stand by TIME	Up to 200 hrs : Paging Period 5, RSSI 85dBm	
Talk time	Up to 200min : GSM Tx Level 7	
Stand by time	Up to 200 hours (Paging Period: 5, RSSI: -85 dBm)	
Charging time	Approx. 3 hours	
RX Sensitivity	GSM, EGSM: -109dBm, DCS: -109dBm	
TX output power	GSM, EGSM: 32.3dBm(Level 5), DCS , PCS: 29.5dBm(Level 0)	
GPRS compatibility	Class 10	
SIM card type	3V Small	
Display	MAIN : TFT 176 × 220 pixel 262K Color	
Status Indicator	Hard icons. Key Pad 0 ~ 9, #, *, Up/Down Navigation Key Menu Key, Clear Key, Back Key, Confirm Key Send Key, Soft Key(Left/Right) Volume Key(Up/Down), PWR Key, Camera Key	
ANT	Internal	
EAR Phone Jack	Yes	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR	
Data and Fax	Yes	
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	
Microphone	Yes	

2. PERFORMANCE

Item	Feature	Comment
Speaker/Receiver	16Φ Speaker/ 12 x 7 Receiver	
Travel Adapter	Yes	
MIDI	SW MIDI (Mono SPK)	
Camera	0.3M	
Bluetooth / FM Radio	Bluetooth version 2.1 / 76~108MHz supported	

2.2 Technical Specification

<table>
<tr><th>Item</th><th>Description</th><th>Specification</th></tr>
<tr><td>1</td><td>Frequency Band</td><td>GSM850
TX: 824 ~ 849 MHz
RX: 869 ~ 894 MHz
EGSM
TX: 880 ~ 915MHz
RX: 925 ~ 960 MHz
DCS
TX: 1710 ~ 1785 MHz
RX: 1805 ~ 1880 MHz
PCS
TX: 1850 ~ 1910 MHz
RX: 1930 ~ 1990 MHz</td></tr>
<tr><td>2</td><td>Phase Error</td><td>RMS < 5 degrees
Peak < 20 degrees</td></tr>
<tr><td>3</td><td>Frequency Error</td><td>< 0.1 ppm</td></tr>
<tr><td>4</td><td>Power Level</td><td>
GSM850/EGSM
<table>
<tr><th>Level</th><th>Power</th><th>Toler.</th><th>Level</th><th>Power</th><th>Toler.</th></tr>
<tr><td>5</td><td>33dBm</td><td>±2dB</td><td>13</td><td>17dBm</td><td>± 3dB</td></tr>
<tr><td>6</td><td>31dBm</td><td>±3dB</td><td>14</td><td>15dBm</td><td>± 3dB</td></tr>
<tr><td>7</td><td>29dBm</td><td>±3dB</td><td>15</td><td>13dBm</td><td>± 3dB</td></tr>
<tr><td>8</td><td>27dBm</td><td>±3dB</td><td>16</td><td>11dBm</td><td>± 5dB</td></tr>
<tr><td>9</td><td>25dBm</td><td>±3dB</td><td>17</td><td>9dBm</td><td>± 5dB</td></tr>
<tr><td>10</td><td>23dBm</td><td>±3dB</td><td>18</td><td>7dBm</td><td>± 5dB</td></tr>
<tr><td>11</td><td>21dBm</td><td>±3dB</td><td>19</td><td>5dBm</td><td>± 5dB</td></tr>
<tr><td>12</td><td>19dBm</td><td>±3dB</td><td></td><td></td><td></td></tr>
</table>
DCS/PCS
<table>
<tr><th>Level</th><th>Power</th><th>Toler.</th><th>Level</th><th>Power</th><th>Toler.</th></tr>
<tr><td>0</td><td>30dBm</td><td>±2dB</td><td>8</td><td>14dBm</td><td>± 3dB</td></tr>
<tr><td>1</td><td>28dBm</td><td>±3dB</td><td>9</td><td>12dBm</td><td>± 4dB</td></tr>
<tr><td>2</td><td>26dBm</td><td>±3dB</td><td>10</td><td>10dBm</td><td>± 4dB</td></tr>
<tr><td>3</td><td>24dBm</td><td>±3dB</td><td>11</td><td>8dBm</td><td>± 4dB</td></tr>
<tr><td>4</td><td>22dBm</td><td>±3dB</td><td>12</td><td>6dBm</td><td>± 4dB</td></tr>
<tr><td>5</td><td>20dBm</td><td>±3dB</td><td>13</td><td>4dBm</td><td>± 4dB</td></tr>
<tr><td>6</td><td>18dBm</td><td>±3dB</td><td>14</td><td>2dBm</td><td>± 5dB</td></tr>
<tr><td>7</td><td>16dBm</td><td>±3dB</td><td>15</td><td>0dBm</td><td>± 5dB</td></tr>
</table>
</td></tr>
</table>

2. PERFORMANCE

Item	Description	Specification	
5	Output RF Spectrum (due to modulation)	**GSM850/ EGSM**	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-63
		3,000~ <6,000	-65
		6,000	-71
		DCS/PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-65
		3,000~ <6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	**GSM850/ EGSM**	
		Offset from Carrier (kHz).	Max. dBm
		400	-19
		600	-21
		1,200	-21
		1,800	-24

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td rowspan="6">6</td><td rowspan="6">Output RF Spectrum
(due to switching
transient)</td><td colspan="3">DCS/PCS</td></tr>
<tr><td colspan="2">Offset from Carrier (kHz).</td><td>Max. dBm</td></tr>
<tr><td colspan="2">400</td><td>-22</td></tr>
<tr><td colspan="2">600</td><td>-24</td></tr>
<tr><td colspan="2">1,200</td><td>-24</td></tr>
<tr><td colspan="2">1,800</td><td>-27</td></tr>
<tr><td>7</td><td>Spurious Emissions</td><td colspan="3">Conduction, Emission Status</td></tr>
<tr><td>8</td><td>Bit Error Ratio</td><td colspan="3">GSM850, EGSM
BER (Class II) < 2.439% @-102 dBm
DCS,PCS
BER (Class II) < 2.439% @-100 dBm</td></tr>
<tr><td>9</td><td>RX Level Report Accuracy</td><td colspan="3">±3 dB</td></tr>
<tr><td>10</td><td>SLR</td><td colspan="3">8±3 dB</td></tr>
<tr><td rowspan="10">11</td><td rowspan="10">Sending Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>-</td></tr>
<tr><td>200</td><td>0</td><td>-</td></tr>
<tr><td>300</td><td>0</td><td>-12</td></tr>
<tr><td>1,000</td><td>0</td><td>-6</td></tr>
<tr><td>2,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,400</td><td>4</td><td>-9</td></tr>
<tr><td>4,000</td><td>0</td><td>-</td></tr>
<tr><td>12</td><td>RLR</td><td colspan="3">2±3 dB</td></tr>
</table>

2. PERFORMANCE

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td rowspan="11">13</td><td rowspan="11">Receiving Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>-</td></tr>
<tr><td>200</td><td>0</td><td>-</td></tr>
<tr><td>300</td><td>2</td><td>-7</td></tr>
<tr><td>500</td><td>*</td><td>-5</td></tr>
<tr><td>1,000</td><td>0</td><td>-5</td></tr>
<tr><td>3,000</td><td>2</td><td>-5</td></tr>
<tr><td>3,400</td><td>2</td><td>-10</td></tr>
<tr><td>4,000</td><td>2</td><td></td></tr>
<tr><td colspan="3">* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.</td></tr>
<tr><td>14</td><td>STMR</td><td colspan="3">13±5 dB</td></tr>
<tr><td>15</td><td>Stability Margin</td><td colspan="3">> 6 dB</td></tr>
<tr><td rowspan="9">16</td><td rowspan="9">Distortion</td><td colspan="2">dB to ARL (dB)</td><td>Level Ratio (dB)</td></tr>
<tr><td colspan="2">-35</td><td>17.5</td></tr>
<tr><td colspan="2">-30</td><td>22.5</td></tr>
<tr><td colspan="2">-20</td><td>30.7</td></tr>
<tr><td colspan="2">-10</td><td>33.3</td></tr>
<tr><td colspan="2">0</td><td>33.7</td></tr>
<tr><td colspan="2">7</td><td>31.7</td></tr>
<tr><td colspan="2">10</td><td>25.5</td></tr>
<tr><td>17</td><td>Side Tone Distortion</td><td colspan="3">Three stage distortion < 10%</td></tr>
<tr><td>18</td><td>System frequency (13 MHz) tolerance</td><td colspan="3">≤ 2.5 ppm</td></tr>
<tr><td>19</td><td>32.768KHz tolerance</td><td colspan="3">≤ 30 ppm</td></tr>
<tr><td>20</td><td>Ringer Volume</td><td colspan="3">At least 65 dBspl under below conditions:
1. Ringer set as ringer.
2. Test distance set as 50 cm</td></tr>
</table>

<table>
<tr><th>Item</th><th>Description</th><th colspan="2">Specification</th></tr>
<tr><td>21</td><td>Charge Current</td><td colspan="2">Fast Charge : Typ. 430 mA
Slow Charge : Typ. 80mA
Total Charging Time : < 3 hours</td></tr>
<tr><td rowspan="8">22</td><td rowspan="8">Antenna Display</td><td>Bar Number</td><td>Power</td></tr>
<tr><td>7</td><td>Over -93</td></tr>
<tr><td>7 -> 5</td><td>-93 ± 2</td></tr>
<tr><td>5 -> 4</td><td>-98 ± 2</td></tr>
<tr><td>4 -> 2</td><td>-101 ± 2</td></tr>
<tr><td>2 -> 1</td><td>-104 ± 2</td></tr>
<tr><td>1 -> 0</td><td>-106 ± 2</td></tr>
<tr><td>0 -> OFF</td><td>Under -106</td></tr>
<tr><td rowspan="5">23</td><td rowspan="5">Battery Indicator</td><td>Battery Bar Number</td><td>Voltage</td></tr>
<tr><td>3</td><td>≥ 3.73± 0.05 V</td></tr>
<tr><td>3 -> 2</td><td>3.72 ± 0.05 V</td></tr>
<tr><td>2 -> 1</td><td>3.62 ± 0.05 V</td></tr>
<tr><td>1 -> 0</td><td>3.45 ± 0.05 V</td></tr>
<tr><td rowspan="2">24</td><td rowspan="2">Low Voltage Warning
(Blinking Bar)</td><td colspan="2">≤ 3.45 ± 0.05V (Call), Once per 1 minute.(Receiver)</td></tr>
<tr><td colspan="2">≤ 3.4 ± 0.05V (Standby), Once per 3 minute.(Speaker)</td></tr>
<tr><td>25</td><td>Forced shut down
Voltage</td><td colspan="2">3.35 ± 0.05V</td></tr>
<tr><td>26</td><td>Sustain RTC
without battery</td><td colspan="2">Over 50 hours</td></tr>
<tr><td>27</td><td>Battery Type</td><td colspan="2">Li-Ion Battery
Standard Voltage = 3.7 V
Battery full charge voltage = 4.2 V
Capacity: 800mAh</td></tr>
<tr><td>28</td><td>Travel Charger</td><td colspan="2">Switching-mode charger
Input: 100 ~ 350V, 50/60 Hz
Output: 5.1 V, 400 mA</td></tr>
</table>

3. TECHNICAL BRIEF

3.1 Digital Main Processor

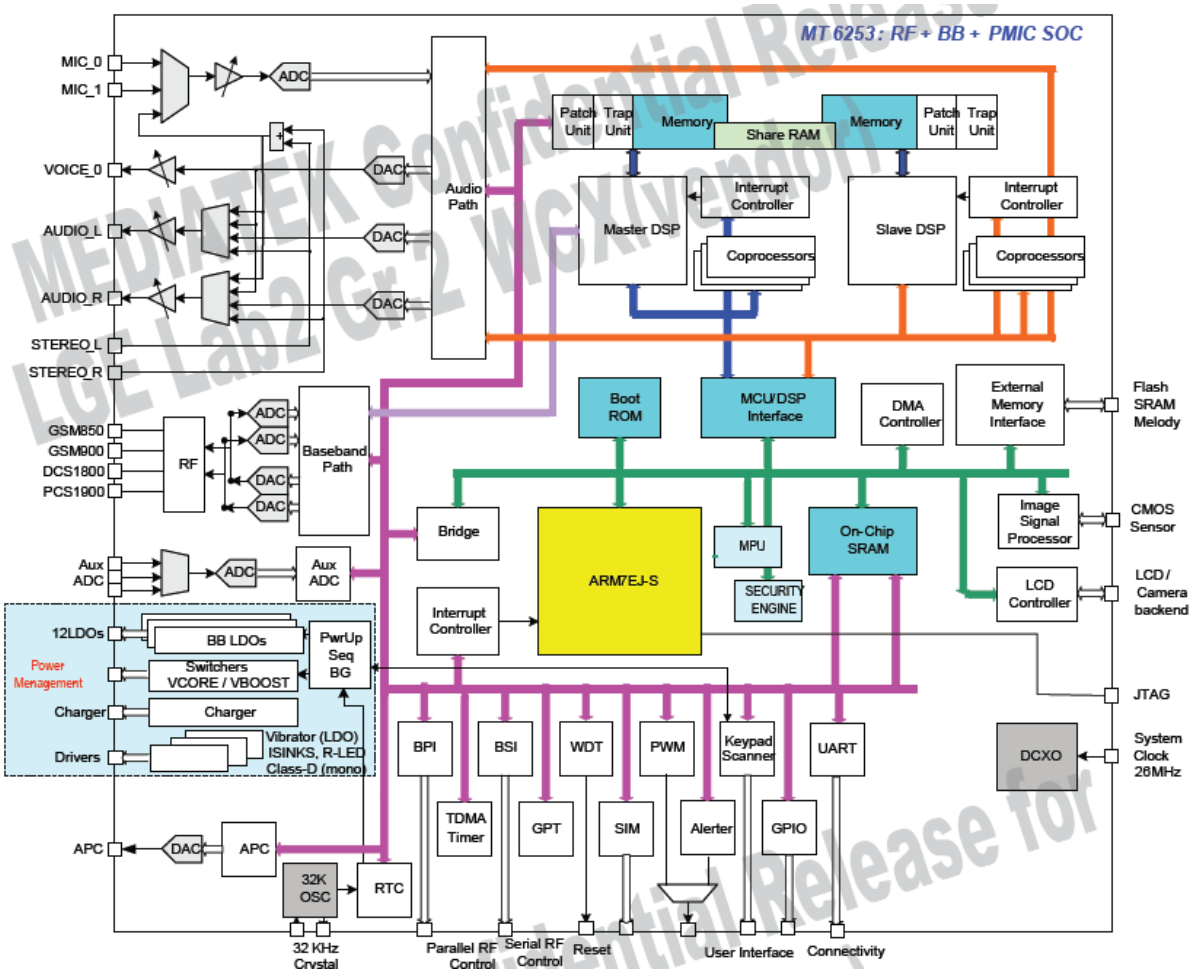


Figure. 3.1.1 MT6253 Hardware Block Diagram

3.1.1 General

• Integrated voice-band, audio-band and base-band analog front ends.
• Package:
– aQFN, 11.5x11.5x0.85 mm
– 0.47 mm pitch
– 260balls, 0.47mm pitch package

3.1.2 MCU Subsystem

• ARM7EJ-S 32-bit RISC processor
• High performance multi-layer AMBA bus
• Operating frequency 52/104MHz
• Dedicated DMA bus, 7DMA channels
• 144KB 0n-chip SRAM
• On-chip boot ROM for Factory Flash Programming
• Watchdog timer for system crash recovery
• 3 sets of General Purpose Timer
• Circuit Switch Data coprocessor
• Division coprocessor

3.1.3 External Memory Interface

• Supports up to 3 external devices
• Supports 16-bit memory components with maximum size of up to 64M Bytes for each bank
• Supports Flash and SRAM/PSRAM with Burst Mode
• Support legacy industry standard parallel LCD Interface
• Suppport multi-media companion chips with 8/16 bits data width
• Configurable driving strength for memory interface

3.1.4 User Interface

• 6-row x 7-column keypad control with hardware scanner
• Support multi key press for gaming
• SIM/USIM Controller with hardware T=0/T=1 protocol control
• Real Time Clock(RTC) operating with a separate power supply
• General Purpose I/Os (GPIOs)
• 1 set of Pulse Width Modulation(PWM) Output
• Alerter Output with Enhanced PWM or PDM
• Maximum 7 external interrupt lines

3.1.5 Security

• Support security key and 128bit chip unique ID

3.1.6 Connectivity

• 3 sets of UART with hardware flow control and speed up to 921600 bps
• IrDA modulator/demodulator with hardware framer supports SIR mode of operation
• HS/FS/LS USB 2.0 Device controller
• Multi Media Card/Secure Digital Memory Card/Memory Stick/Memory Stick Prto/SDIO host controller
• Supports SDIO interface for SDIO peripherals as well as WIFI connectivity
• DAI/PCM and !2S interface for Audio application

3.1.7 Low Power Schemes

• Power Down Mode for analog and digital circuits
• Processor Sleep Mode
• Pause Mode of 32KHs clocking at Standby State
• 3-channel Auxiliary 10-bit A/D Converter for application usage other than battery monitoring

3.1.8 Power and Supply Management

• 2.8V to 4.7V Input Range
• Charger Input up to 8V
• 11 sets of LDO Optimized Specific GSM Sub-systems
• One LDO for RF transceiver
• High Operation Efficiency and Low Stand-by Current
• Dual SIM Card Interface
• One boost regulator and Four Open-Drain Output Current Regulators to Supply/Control the LED
• LDO type Vibrator
• One NMOS switch to control R(GB) LED
• Thermal Overload Protection
• Under Voltage Lock-out Protection
• Over Voltage Protection

3.1.9 Integrated RF Receiver

• Direct conversion architecture
• Quad band differential input LNAs
• Quadrature RF mixers
• Fully integrated channel filter with f3dB=150kHs
• 95dB gain with 60dB gain control range
• No IIP2 calibration

3.1.10 Integrated RF Transmitter

- Offset phase lock loop
- IQ modulator DC offset calibration by BB ADC/DAC
- Precise quadrature by IF divide-by-4
- Integrated loop filter

3.1.11 Integrated RF Frequency Synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast setting time suitable for multi-slot SPRS applications

3.1.12 Integrated RF Digitally-Controlled Crystal Oscillator(DCXO)

- One-pin 26MHz crystal oscillator
- On-chip programmable capacitor array for cross tune

3.1.13 Radio Interface and Baseband Front End

- GMSK modulator with analog I and Q channel outputs
- 10-bit D/A Converter for uplink baseband I and Q signals
- 14-bit high resolution A/D Converter for downlink baseband I and Q signals
- Calibration mechanism of offset and gain mismatch for baseband A/D Converter and D/A Converter
- 10-bit D/A Converter for Automatic Power Control
- Programmable Radio RX filter with adaptive bandwidth control
- Dedicated Rx filter for FB acquisition
- 6-Pin Baseband Parallel Interface(BRI) with programmable driving strength
- Multi-band support

3.1.14 Voice and Modem CODEC

- Digital tone generation
- Voice Memo
- Noise Reduction
- Echo Suppression
- Advanced Sidetone Oscillation Reduction
- Digital sidetone generator with programmable gain
- Two programmable acoustic compensation filters
- GSM/GPRS quad vocoders for adaptive multirate(AMR), enhanced full rate(EFR), full rate(FR), and half rate(HR)
- GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
- GPRS GEA1, GEA2 and GEA3 ciphering

3.1.15 Voice Interface and Voice Front End

• Two microphone inputs sharing one low noise amplifier with programmable gain and automatic gain control(AGC) mechanism
• Voice power amplifier with programmable gain
• 2nd order Sigma-delta A/D Converter for voice uplink path
• D/A Converter for voice downlink path
• Supporter for voice downlink path
• Supports half-duplex hands-free operation
• Compliant with GSM 03.05

3.1.16 LCD Interface

• Dedicated Parallel Interface supports 2 external 8/9 bit Parallel Interface, and Serial interface for LCM

3.1.17 LCD Controller

• Supports LCM format: RGB332, RGB444, RGB565, RGB666, RGB888
• Supports LCD module with maximum resolution up to 240x320 at 16bpp
• Capable of combining display memories with up to 4 blending layers
• Accelerated Gamma correction with programmable gamma table.
• Supports hardware display rotation for each layer

3.1.18 Audio CODEC

• Wavetable synthesis with up to 64 tones
• Advanced wavetable synthesizer capable of generating and 47 sets of percussions
• PCM Playback and Record
• Digital Audio Playback

3.1.19 Audio Interface and Audio Front End

• Supports I2S interface
• High resolution D/A Converters for Stereo Audio playback
• Stereo analog input for stereo audio source
• Analog multiplexer for Stereo Audio
• FM Radio Recording
• Stereo to Mono Conversion
• HE-AAC decode support

3.2 Power Management

Power management unit, so called PMU, is integrated into analog part. To facilitate software control and interface design, PMU control share the CCI interface along with other analog parts, such as BBTX, BBRX, VBI and ABI during FT.

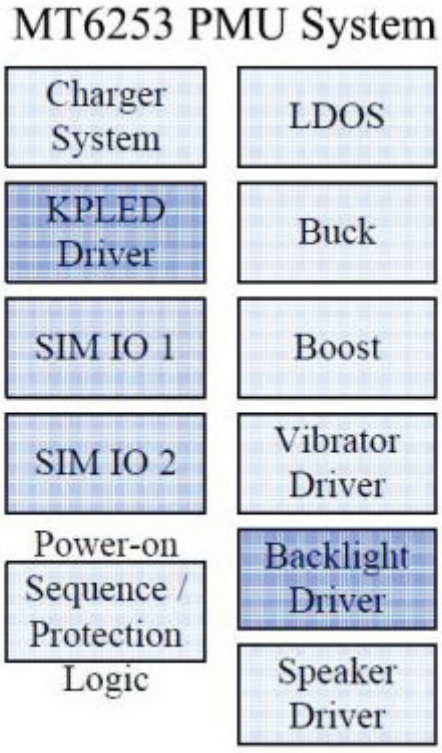


Figure. 3.2.1 PMU system block diagram

3.2.1 Low Dropout Regulators(LDOs), Buck converterand Reference

The PMU Integrates 12 LDOs that are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, and output noise.

▪ **RF LDO (Vrf)**

The RF LDO is a linear regulator that could source 180mA (max) with 2.8V output voltage. It supplies the RF circuitry of the handset. The LDO is optimized for high performance and adequate quiescent current.

▪ Digital Core Buck Converter (Vcore)

The digital core regulator is a DC-DC step-down (Buck converter) that could source 200mA(max) with 1.2V to 0.9V programmable output voltage based on software register setting. It supplies the power for baseband circuitry of the SoC. The buck converter is optimized for high efficiency and low quiescent current.

▪ Digital IO LDO (Vio)

The digital IO LDO is a linear regulator that could source 100mA (max) with 2.8V output voltage. It supplies the the power for baseband circuitry of the SoC. The LDO is optimized for very low quiescent current and turns on automatically together with Vm/Va LDOs.

▪ Analog LDO (Va)

The analog LDO is a linear regulator that could source 100mA (max) with 2.8V output voltage.
It supplies the analog sections of the SoC. The LDO is optimized for low frequency ripple rejection in order to reject the ripple coming from the burst at 217Hz of RF power amplifier.

▪ TCXO LDO (Vtcxo)

The TCXO LDO is a linear regulator that could source 20mA (max) with 2.8V output voltage.
It supplies the temperature compensated crystal oscillator, which needs ultra low noise supply with very good ripple rejection.

▪ Single-Step RTC LDO (Vrtc)

The single-step RTC LDO is a linear regulator that can charge up a capacitor-type backup coin cell to 2.8V, which also supplies the RTC module even at the absence of the main battery. The single-step LDO features the reverse current protection and is optimized for ultra low quiescent current while sustaining the RTC function as long as possible.

▪ Memory LDO (Vm)

The memory LDO is a linear regulator that could source 200mA (max) with 1.8V or 2.8V output voltage selection based on the supply specification of memory chips. It supplies the memory circuitry in the handset. The LDO is optimized for very low quiescent current with wide output loading range.

▪ SIM LDO (Vsim)

The SIM LDO is a linear regulator that could source 80mA (max) with 1.8V or 3.0V output voltage selection based on the supply specs of subscriber identity modules (SIM) card. It supplies the SIM card and SIM level shifter circuitry in the handset. The Vsim LDO is controlled independently by the register named VSIM_EN.

- **SIM2 LDO (Vsim2)**

The SIM2 LDO is a linear regulator that could source 20mA (max) with 1.8V or 3.0V output voltage selection based on the supply specs of the 2nd subscriber identity modules (SIM) card.
It supplies the 2nd SIM card and SIM level shifter circuitry in the handset. The Vsim2 LDO is controlled independently by the register named VSIM2_EN.

- **USB LDO (Vusb)**

The USB LDO is a linear regulator that could source 75mA (max) with 3.3V output dedicated for USB circuitry. It is controlled independently by the register named RG_VUSB_EN.

- **Memory Card / Bluetooth LDO (Vbt)**

The VBT LDO is a linear regulator that could source 150mA (max) with 1.5V, 1.8V, 2.5V or 2.8V output for memory card or Bluetooth module. It is controlled independently by the register named RG_VBT_EN.

- **Camera Analog LDO (Vcama)**

The Vcama LDO is a linear regulator that could source 150mA (max) with 1.5V, 1.8V, 2.5V or 2.8V output which is selected by the register named VCAMA_SEL[1:0]. It supplies the analog power of the camera module. Vcama is controlled independently by the register named RG_VCAMA_EN.

- **Camera Digital LDO (Vcamd)**

The Vcamd LDO is a linear regulator that could source 75mA (max) with 1.3V, 1.5V, 1.8V or 2.8V output which is selected by the register named VCAMD_SEL[1:0]. It supplies the digital power of the camera module. Vcamd is controlled independently by the register named RG_VCAMD_EN.

Item	LDO	Voltage	Current	Description
1	VCORE	1.2V / 0.9V	200 mA	Digital core
2	VIO	2.8V	100 mA	Digital IO
3	VRF	2.8V	180 mA	RF chip
4	VA	2.8V	100 mA	Analog baseband
5	VRTC	2.8V	1 mA	Real-time clock
6	VM	1.8V / 2.8V	200 mA	External memory, selectable
7	VSIM	1.8V / 3.0V	80 mA	SIM card, selectable
8	VTCXO	2.8V	20 mA	13/26 MHz reference clock
9	VSIM2	1.8V / 3.0V	20 mA	SIM2 card, selectable
10	VUSB	3.3V	75 mA	USB
11	VBT	1.3V / 1.8V / 2.5V / 3V	150 mA	Memory card or Bluetooth
12	VCAM_A	1.5V / 1.8V / 2.5V / 2.8V	150 mA	Analog camera power
13	VCAM_D	1.3V / 1.5V / 1.8V / 2.8V	75 mA	Digital camera power

Table3.2.1. Power Supply Domains (Without RF)

3.2.2 Power On

Together with Power Management IC (PMIC), MT6253 offers both fine and coarse resolutions of power control through software programming. With this efficient method, the developer can turn on selective resources accordingly in order to achieve optimized power consumption. The operating modes of MT6253 as well as main power states provided by the PMIC are shown in Figure.3.2.1.

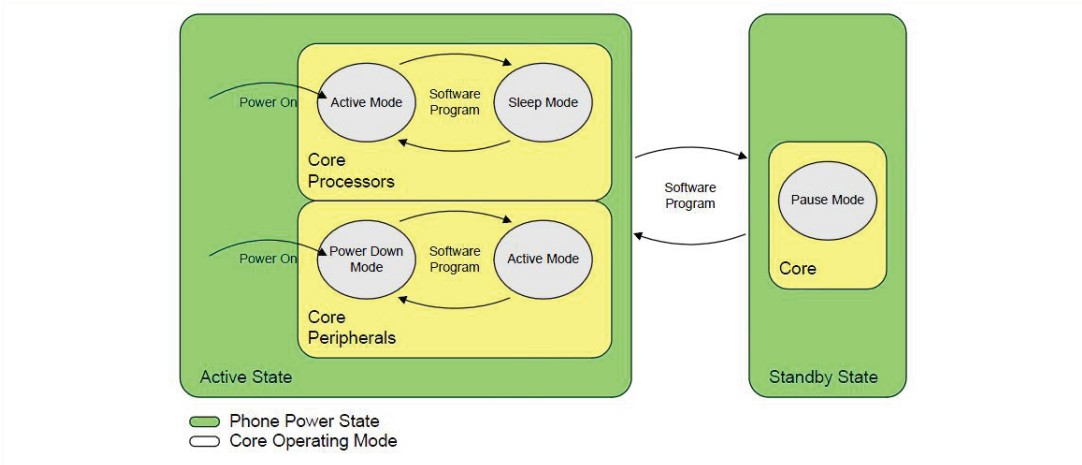


Figure 3.2.2. Major Phone Power States and Operating Modes for MT6253 based terminal

3.3 FEM with integrated Power Amplifier Module (SKY77547, U303)

3.3.1 Internal Block Diagram

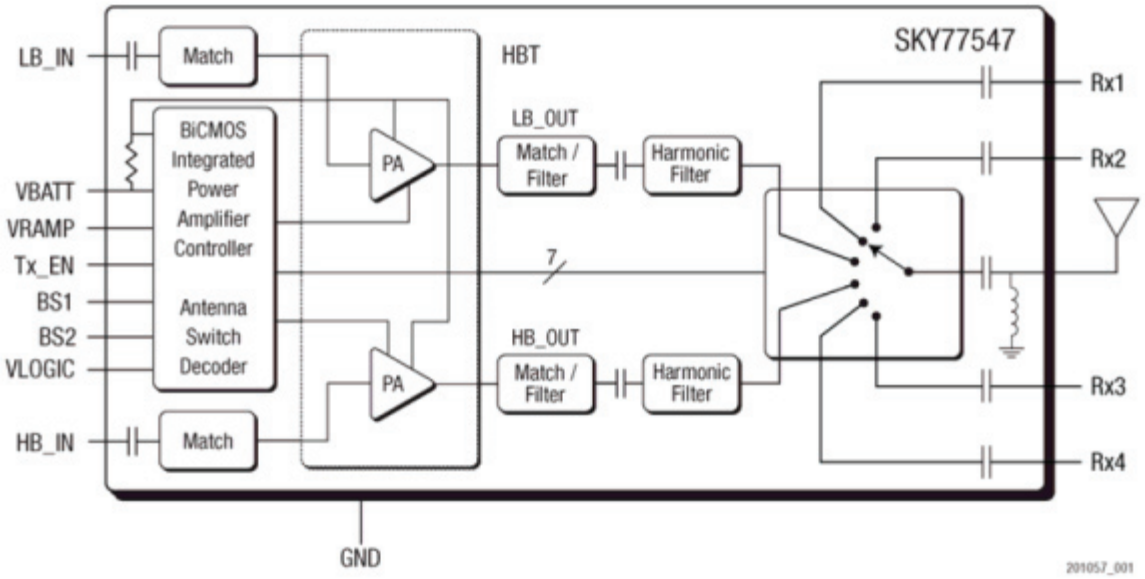


Figure. 3.3.1 SKY77547 FUNCTIONAL BLOCK DIAGRAM

3.3.2 General Description

The SKY77547 is a transmit and receive front-end module (FEM) with Integrated Power Amplifier Control (iPAC™) for quad-band cellular handsets comprising GSM850/900 and DCS1800/PCS1900 operation. Designed in a low profile, compact form factor, the SKY77547 offers a complete Transmit VCO-to-Antenna and Antenna-to-Receive SAW filter solution. The FEM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation.
The module consists of a GSM850/900 PA block and a DCS1800/PCS1900 PA block, impedance matching circuitry for 50 Ω input and output impedances, Tx harmonics filtering, high linearity and a low insertion loss PHEMT RF switch, and a Power Amplifier Control (PAC) block with internal current sense resistor. A custom BiCMOS integrated circuit provides the internal PAC function and decoder circuitry to control the RF switches. The two Hetero junction Bipolar Transistor (HBT) PA blocks are fabricated onto a single Gallium Arsenide (GaAs) die. One PA block supports the GSM850/900 bands and the other PA block supports the DCS1800/PCS1900 bands.

Both PA blocks share common power supply pads to distribute current. The output of each PA block and the outputs to the four receive pads are connected to the antenna pad through a PHEMT RF switch. The GaAs die, PHEMT die, Silicon (Si) die and passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

Mode	VRF	PA_EN	BAND_SW1	BAND_SW2
Standby	0	–	–	–
PCS Rx	1	0	0	0
DCS Rx	1	0	0	1
EGSM Rx	1	0	1	1
GSM850 Rx	1	0	1	0
GSM_OUT	1	1	0	–
DCS_PCS_OUT	1	1	1	–

1. – = DON'T CARE

Table 3.3.1 Band SW Logic Table

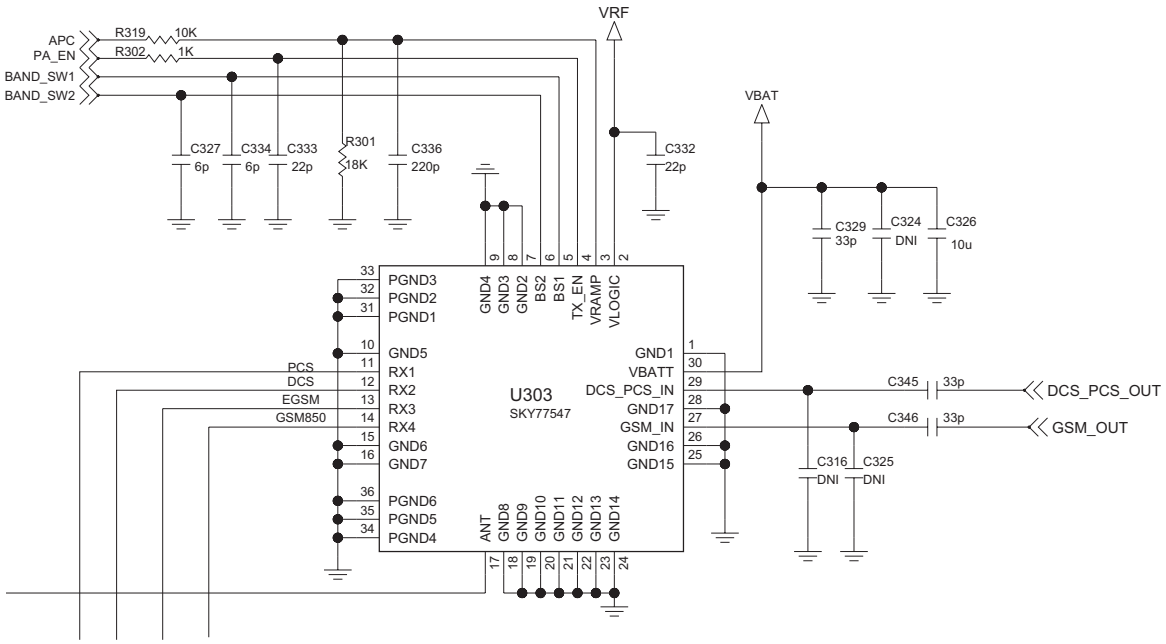


Figure 3.3.2 TX-module CIRCUIT DIAGRAM

3.4 Clocks

There are two major time bases in the MT6253. For the faster one is the 26 MHz clock originated from the digital control oscillator(DCXO) of RF block. This is then converted to the square-wave signal through CLKSQ.
The other time base is the 32768 Hz clock generated by an on-chip oscillator connected to an external crystal.

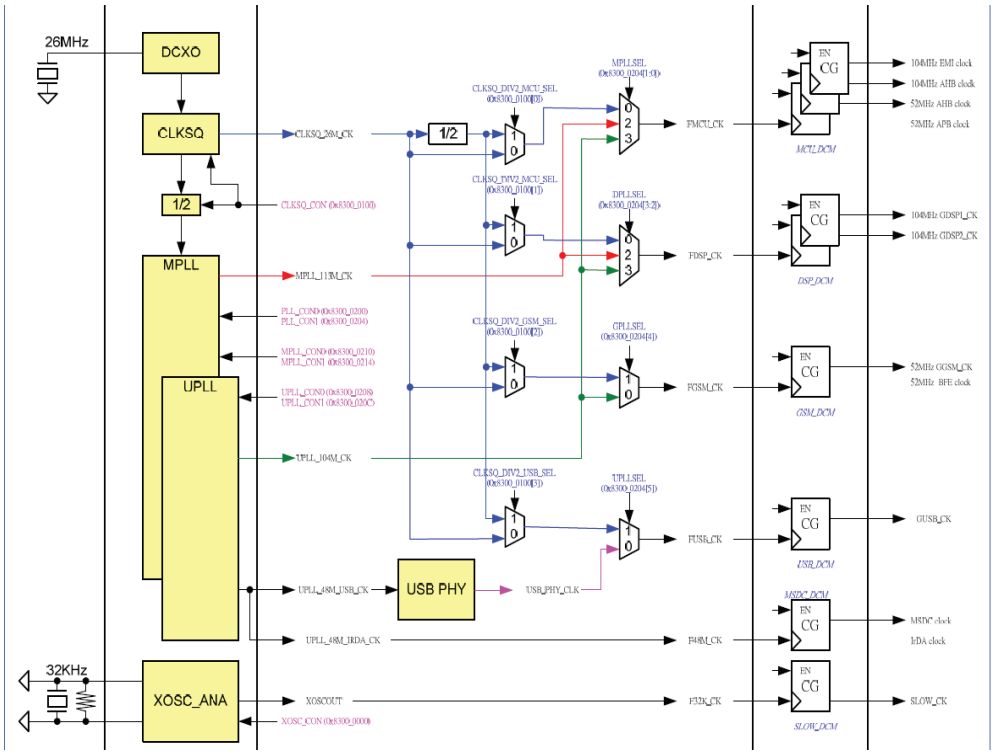


Figure. 3.4.1 Clock distributions inside the MT6253.

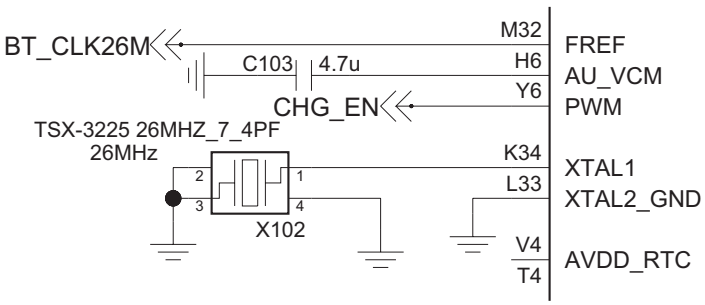


Figure. 3.4.2 Crystal Oscillator External Connection

3.4.1 32.768KHz Time Base

The 32768 Hz clock is always running. It's mainly used as the time base of the Real Time Clock(RTC) module, which maintains time and date with counters. Therefore, both the 32768Hz oscillator and the RTC module is powered by separate voltage supplies that shall not be powered down when the other supplies do.
In low power mode, the 13Mhz time base is turned off, so the 32768Hz clock shall be employed to update the critical TDMA timer and Watchdog Timer. This time base is also used to clocks the keypad scanner logic

3.4.2 26MHz Time Base

Since PLL are based on 13MHz reference clock. There is an ½-dividers for PLL existing to allow using 26MHz DCXO.
There are 2 phase-locked loops(PLL) in MT6253. The UPLL generates 624Mhz clock output, then a frequency divider further divide 6, and 13 to generate fixed 103Mhz, and 48Mhz for GSM_CLOCK and USB_CLOCK and DSP_CLOCK. These four primary clocks then feed into GSM, USB, MCU and DSP Clock Domain, respectively.
These 2 PLLs require no off-chip components for operations and can be turn off in order to save power. After power-on, the PLLs are off by default and the source clock signal is selected through multiplexers. The software shall take cares of the PLL lock time while changing the clock selections. The PLL and usages are listed below.

- PLL supply four clock source : MCU_CLOCK(104~113Mhz), DSP_CLOCK(104~113Mhz), GSM_CLOCK(104Mhz) and USB_CLOCK(48Mhz)

- For DSP/MCU system clock, MCU_CLOCK and DSP_CLOCK. The outputted 104~113Mhz clock is controlled by MCU for 500Khz per step and settled time is under 100uS. The clock is also connected to DSP/MCU DCM (dynamic clock manager) for dynamically adjusting clock rate by digital clock divider.

MCU_CLOCK paces the operations of the MCU cores, MCU memory system, and MCU peripherals as well

- Modem system clock, GSM_CLOCK, which paces the operations of the GSM/GPRS hardware, coprocessors as well. The outputted 104Mhz clock is connecter to GSM_DCM for dynamically adjusting clock rate by digital clock divider. Typically the GSM_DCM output clock no more than 52Mhz.

Note that PLL need some time to become stable after being powered up. The software shall take cares of the PLL lock time before switching them to the proper frequency. Usually, a software loop longer than the PLL lock time is employed to deal with the problem.
For power management, the MCU software program may stop MCU Clock by setting the Sleep Control Register. Any interrupt requests to MCU can pause the sleep mode, and thus MCU return to the running mode.
AHB also can be stop by setting the Sleep Control Register. However the behavior of AHB in sleep mode is a little different from that of MCU. After entering Sleep Mode, it can be temporarily waken up by any "hreq"(bus request), and then goes back to sloop automatically after all "hreqs" de-assert. Any transactions can take place as usual in sleep mode, and it can save power while there is no transaction on it. However the penalty is losing a little system efficiency for switching on and off bus clock, but the impact is small

3.5 RFSYS of MT6253 (U102)

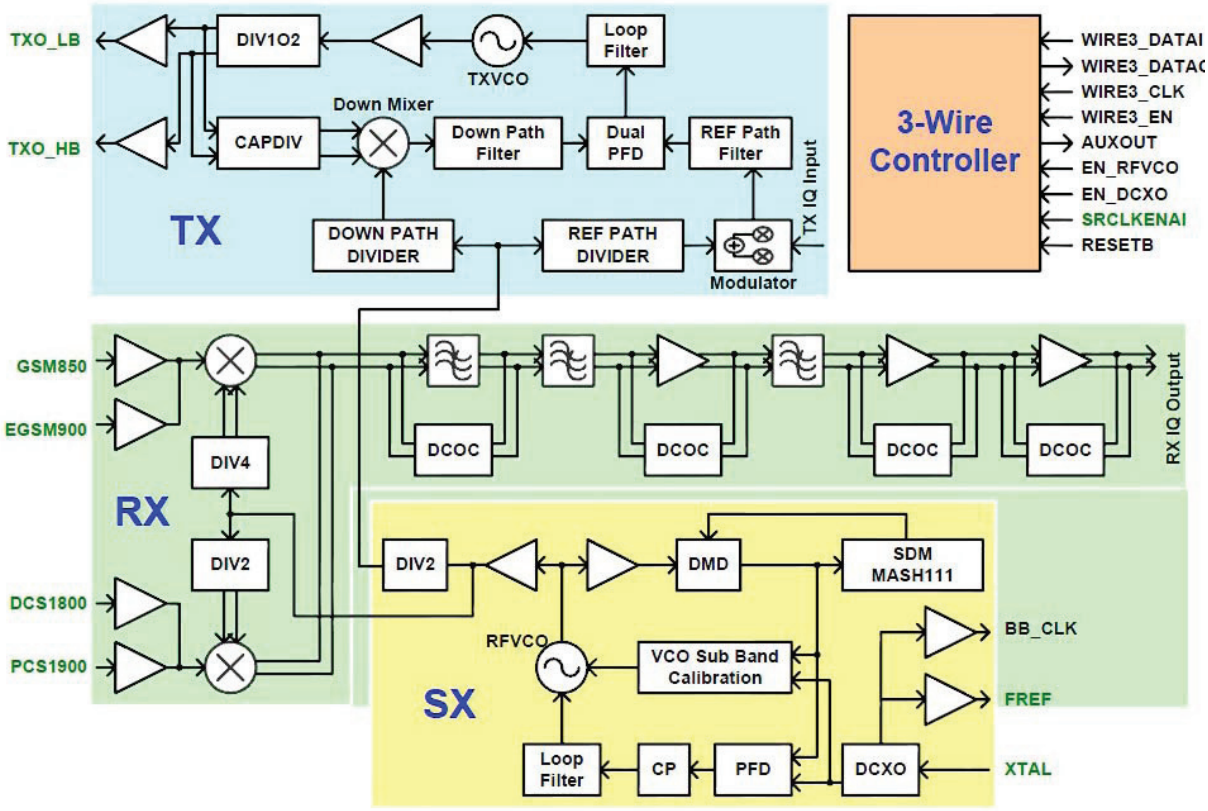


Figure. 3.5.1 Block DIAGRAM of RFSYS

3.5.1 GENERAL DESCRIPTION

RFSYS built in MT6253 SOC is a highly integrated RF transceiver for multi-band GMS and GPRS cellular systems. The features are listed as following.

- **Receiver**
  - Direct conversion architecture
  - Quad band differential input LNAs
  - Quadrature RF mixers
  - Fully integrated channel filter with f_{3dB}=150kHz
  - 95 dB gain with 60 dB gain control range

- **Transmitter**
  - Offset phase lock loop
  - IQ modulator
  - Integrated TX VCO
  - Integrated loop filter

- **Frequency Synthesizer**
  - Programmable fractional-N synthesizer
  - Integrated wide range RFVCO
  - Integrated loop filter
  - Fast settling time suitable for multi-slot GPRS/EDGE applications

- **Digitally-Controlled Crystal Oscillator (DCXO)**
  - One-pin 26 MHz crystal oscillator
  -On-chip programmable capacitor array for coarse tune
  - On-chip programmable capacitor array for fine tune

- **RFSYS in a-QFN package**

3.6 MEMORY(PF38F4050M0Y3DE, U101)

3.6.1 Functional Description

The Numonyx™ StrataFlash® Cellular Memory (M18) device provides high read and write performance at low voltage on a 16-bit data bus.
The flash memory device has a multi-partition architecture with read-while-program and read-while-erase capability.
The device supports synchronous burst reads up to 108 MHz using ADV# and CLK address-latching (legacy-latching) on some litho/density combinations and up to 133 MHz using CLK address-latching only on some litho/density combinations. It is listed below in the following table

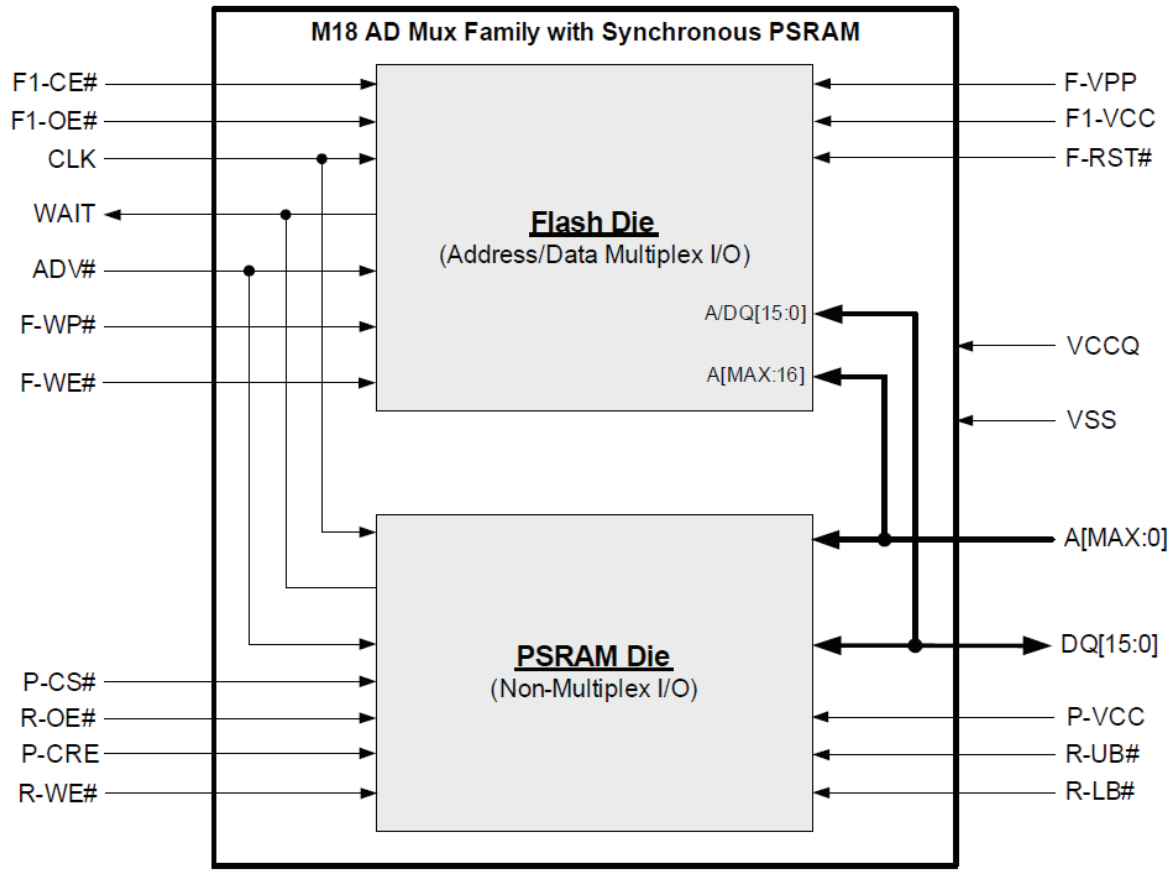


Figure. 3.6.1 MEMORY BLOCK DIAGRAM

Litho (nm)	Density (Mbit)	Supports frequency up to (MHz)	Sync read address-latching
90	256	133	CLK-latching
	512	108	ADV#- and CLK-latching
65	128	133	CLK-latching
	256	133	CLK-latching
	512	133	CLK-latching
	1024	108	ADV#- and CLK-latching
	1024	133	CLK-latching

Table 3_6_1 M18 Frequency combinations

In continuous-burst mode, a data Read can traverse partition boundaries.
Upon initial power-up or return from reset, the device defaults to asynchronous arrayread mode. Synchronous burst-mode reads are enabled by programming the Read Configuration Register. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.
Designed for low-voltage applications, the device supports read operations with VCC at1.8 V, and erase and program operations with VPP at 1.8 V or 9.0 V. VCC and VPP can be tied together for a simple, ultra-low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when VPP is less than VPPLK.
A Status Register provides status and error conditions of erase and program operations
One-Time-Programmable (OTP) registers allow unique flash device identification that can be used to increase flash content security. Also, the individual block-lock feature provides zero-latency block locking and unlocking to protect against unwanted program or erase of the array.
The flash memory device offers three power savings features:

• Automatic Power Savings (APS) mode: The device automatically enters APS following a read-cycle completion.

• Standby mode: Standby is initiated when the system deselects the device by deasserting CE#.

• Deep Power-Down (DPD) mode: DPD provides the lowest power consumption and is enabled by programming in the Enhanced Configuration Register. DPD is initiated by asserting the DPD pin.

3.6.2 Features

▪ **Device Architecture**
- Flash Die Density: 256MB
- PSRAM Die Density: 64MB
- x16 Non-Mux or AD-Mux I/O Interface Options

▪ **Device Voltage**
- Core: VCC = 1.8 V
-I/O: VCCQ = 1.8 V

▪ **Device Packaging**
- Ballout: x16C with 107 Active Balls, QUAD+ with 88 Active Balls, or 56-ball NOR/PSRAM AD-Mux
- Area: 8x8 mm to 11x13 mm
-Height: 1.0 mm to 1.4 mm

▪ **PSRAM Performance**
- 70 ns Initial Read Access; 20 ns Asynchronous Page-Mode Read
- Up to 104 MHz with 7 ns Clock-to-Output Synchronous Burst-Mode Reads
- Configurable 4-, 8-, 16- and Continuous-Word Burst-Length Reads and Writes
- Partial-Array and Temperature Compensated Self Refresh
-Programmable Output Impedance

▪ **Quality and Reliability**
- Extended Temperature –25 ˚C to +85 ˚C
- Minimum 100K Flash Block Erase Cycles
- ETOX™ IX (Flash) and ETOX™ X (Flash)
- Technology on 128 Mbit, 256 Mbit, and 512Mbit M18 die; ETOX™ X (Flash) on 1 Gbit M18 die

▪ **Flash Performance**
-96 ns Initial Read Access; 15 ns Asynchronous Page-Mode Read
-Up to 133 MHz with 5.5 ns Clock-to-Data Output Synchronous Burst-Mode Read
-Buffered Enhanced Factory and 1.8 V Low-Power Buffer Programming Modes:2 µs/Byte (Typ)
-Deep Power-Down Mode: 2 µA (Typ)
-Configurable Output Driver

▪**Flash Architecture**
-Multi-Level Cell Technology
-Hardware Read-While-Program/Erase
-Symmetrically Blocked Array
-Eight Partitions
-Configurable 8-, 16-, or Continuous-Words Burst Length Reads
-2-Kbit One-Time Programmable User Protection Register Bits
-Zero-Latency Block Locking
-Automated Blank Check Mode

▪**Flash Software**
-Numonyx™ FDI and Numonyx™ PSM
-Common Flash Interface
-Basic and Extended Flash Command Set

3.7 BT Module

The internal connection of the major physical blocks and their associated external interfaces are shown in Figure 3.7.1. The transceiver section of MT6612 incorporates the complete receive and transmit paths, including PLL, VCO, LNA, PA, modulator, demodulator.
The baseband signal processor incorporates hardware engines performing frequency hopping, error correcting, whitening, encrypting, data packet assembling and de-assembly to offload the embedded ARM7.

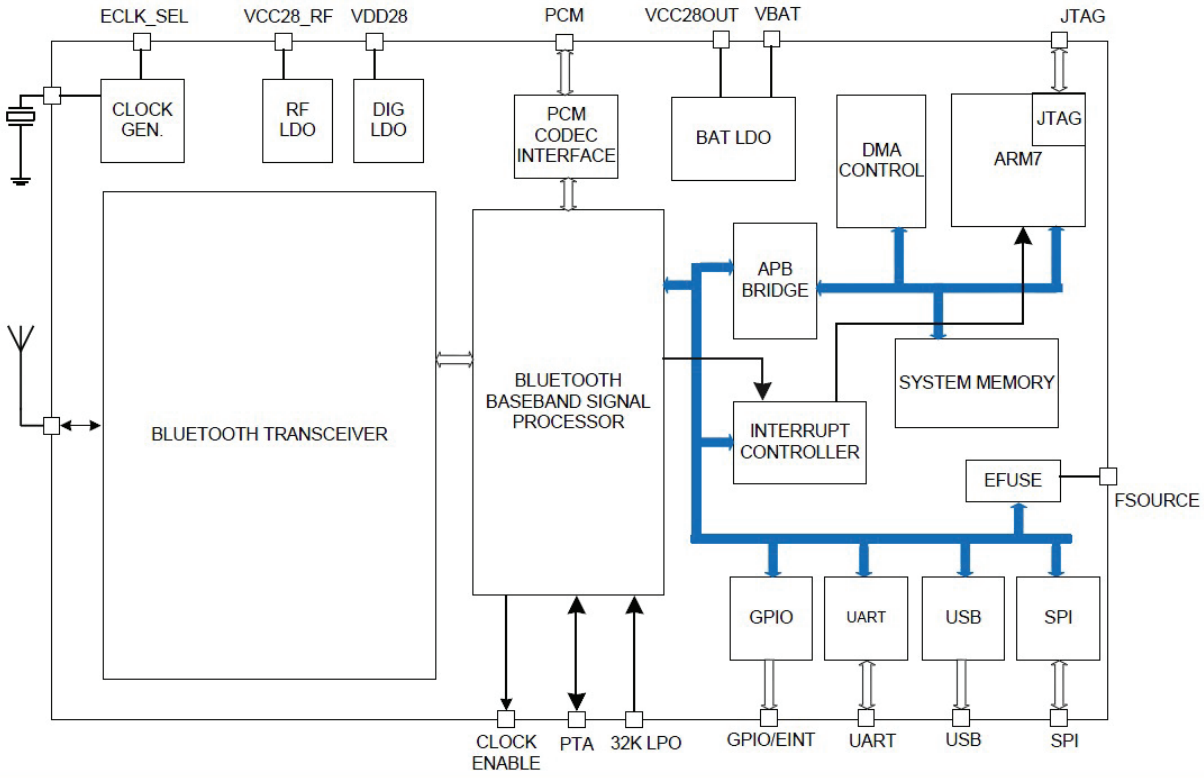


Figure 3.7.1. BT BLOCK DIAGRAM

3.7.1 General Description

Bluetooth is a low-cost wireless technology used to provide “ad hoc” networking between versatile portable devices such as cell phones, headsets, personal navigation device, and more.
MT6612 is a highly integrated Bluetooth platform IC. It includes powerful baseband processing capabilities with rich features and a high performance transceiver, all in a compact single package.

3.7.2 Feature

▪ **Radio features**

- Fully compliant with Bluetooth specification 2.1 + EDR.
- Low out-of-band spurious emissions supports simultaneous operation with GPS, GSM/GPRS worldwide radio systems.
- Low-IF architecture with high degree of linearity and high order channel filter.
- Integrated T/R switch.

▪ **Transmitter features**

- Meets class1, class 2 and class 3 transmitting requirement.
- Fully integrated PA provides 9dBm output power. (antenna out)

▪ **Receiver features**

- -91dBm sensitivity with excellent interference rejection performance.
- Hardware AGC dynamically adjusts receiver performance in changing environments.

▪ **Baseband features**

- Up to 7 simultaneous active ACL links.
- Up to 3 simultaneous SCO and eSCO links with CVSD coding.
- eSCO support.
- Scatternet support: Up to 4 piconets simultaneously with background inquiry/page scan.
- Sniff mode, hold mode, and park mode support.
- AFH and PTA collaborative support for WLAN/BT coexistence.
- Idle mode and sleep mode enables ultra low power consumption
- PCM interface and built-in transcoders for A-law, μ-law and linear voice with re-transmission support.

-Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening, and encryption.

- Channel quality driven data rate adaptation.
- Channel assessment for AFH.

▪ **Platform features**

- Integrated LDO enables direct connection to battery.
- Wide ranges of crystal and external reference clock support.
- High speed UART supports up to 3.2Mbps baud rate.
- Built-in RAM and ROM with patch system.
- External LPO clock support for sleep mode.
- Supports standard HCI interface.
- Capable to support Bluetooth 2.1 features.
- Provides USB full-speed device function.
- Supports a SPI interface to access external serial flash and EEPROM.
- Embedded 128-bit eFuse for Bluetooth Address use.

3.7.3 Functional Description

• Power Subsystem

MT6612 contains several LV (low voltage, 2.8V) linear regulators to provide power supply for every power domain, including RF circuitry and digital core circuitry. Besides, it has built in a BAT linear regulator which can be directly connected to battery. The BAT linear regulator is the power source for digital IO and those LV linear regulators. It supports the Li-ion battery. To keep it work properly, the battery voltage should be within the range from 3.2V to 4.3V.

The built-in LV linear regulators for RF circuitry are cap-less regulators. It provides high PSRR to keep excellent RF performance. MT6612 has internal enabling signals from the baseband to control different part of RF circuitry for optimized power control.

The DIG (digital) LV regulator requires an external capacitor. The main power control state machine is in the digital baseband circuitry. It requires no external enable signal for the DIG LV regulator. When the 1.2V power is supplied from the regulator on VDD12 pins, there will be an internal POR (Power-On Reset) to start the system. An external system reset to start the system is optional according to the application requirement.

The input pin LDO28EN is used by the host controller to turn on and off the BAT regulator. The host can control this pin to enable the whole MT6612 system. The enable voltage (V_{IH}) of pin LDO28EN is 1.4V. Be sure that the control signal meets the enable voltage requirement.

▪ Clock generation

There are two clock domains inside MT6612. The one is the System clock, which supports the RF and the major MODEM functions, while the other is the LPO clock, which keeps track the Bluetooth clock and could maintain the Bluetooth link in sleep mode.

MT6612 ha two options for the System clock source. The one is foe one-pin crystal input, and the other is for external clock source. The input pun ECLK_SEL is used to select between these two alternatives. If the crystal input is chosen, ECLK_SEL should be tied low, Otherwise, it should be tied high.

▪ Chip power management

There are 4 power modes that MT6612 operates in when it is powered on: Normal mode, Active mode, Idle mode, and Sleep mode. The following are brief introduction to each mode.

- Power off : Power supply is not enabled or LDO28EN is low.
- Normal mode : When MT6612 is powered on, it firstly enters Normal mode. In this mode, an internal digital PLL is turned on to supply the clock for baseband circuit.
- Active mode : It is defined as the state that RF circuit will be turned on at the same time.
- Idle mode : When the firmware finishes its task and starts to wait for next hardware trigger, it forces the hardware to enter this mode. In this mode, Part of the logic, like MCU, will enter a low power mode. RF circuit might still be operation in the mode.
- Sleep mode : The baseband controller can determine to enter sleep mode to turn off most of the circuit in MT6612. In sleep mode, the system could be awakened after sleep time expired or by an external wake up signal from the host controller.

▪ MCU Subsystem

The MCU (Micro-Controller Unit) subsystem contains ARM7 microprocessor, internal memory and the ROM patch function. It also contains the UART interface controller, USB full-speed device controller, serial flash interface controller and the power/clock management function.

▪ Bluetooth Baseband Subsystem

The Bluetooth baseband subsystem contains a baseband processor which supports the timing control, the bitstream processing, encryption, frequency hopping, and modulation/demodulation. It also contains the audio codec, Wi-Fi coexistence interface controller, and a sleep mode controller.

▪ RF Subsystem

MT6612 contains a fully integrated transceiver.
For TX path, the baseband transmit data is digitally modulated in the baseband processor, then up-converted to 2.4GHz RF channels through DA converter, filter, IQ up-converter, and the power amplifier. The power amplifier is capable of transmitting 9dBm power for class 1 operation.
For RX path, MT6612 is a low IF receiver architecture. An image-reject mixer down-converts the RF signal to the IF with the LO from the synthesizer, which could support different clock frequencies as the reference clock as described in section “Clock Generation”. The mixer output is then converted to digital signal, down-converted to baseband for demodulation. A fast AGC enables the effective discovery of device within the dynamic range of the receiver.
MT6612 features self calibration schemes to compensate the process and temperature variation to maintain high performance. Those calibrations are performed automatically right after system boot-up.

3.8 SIM Card Interface

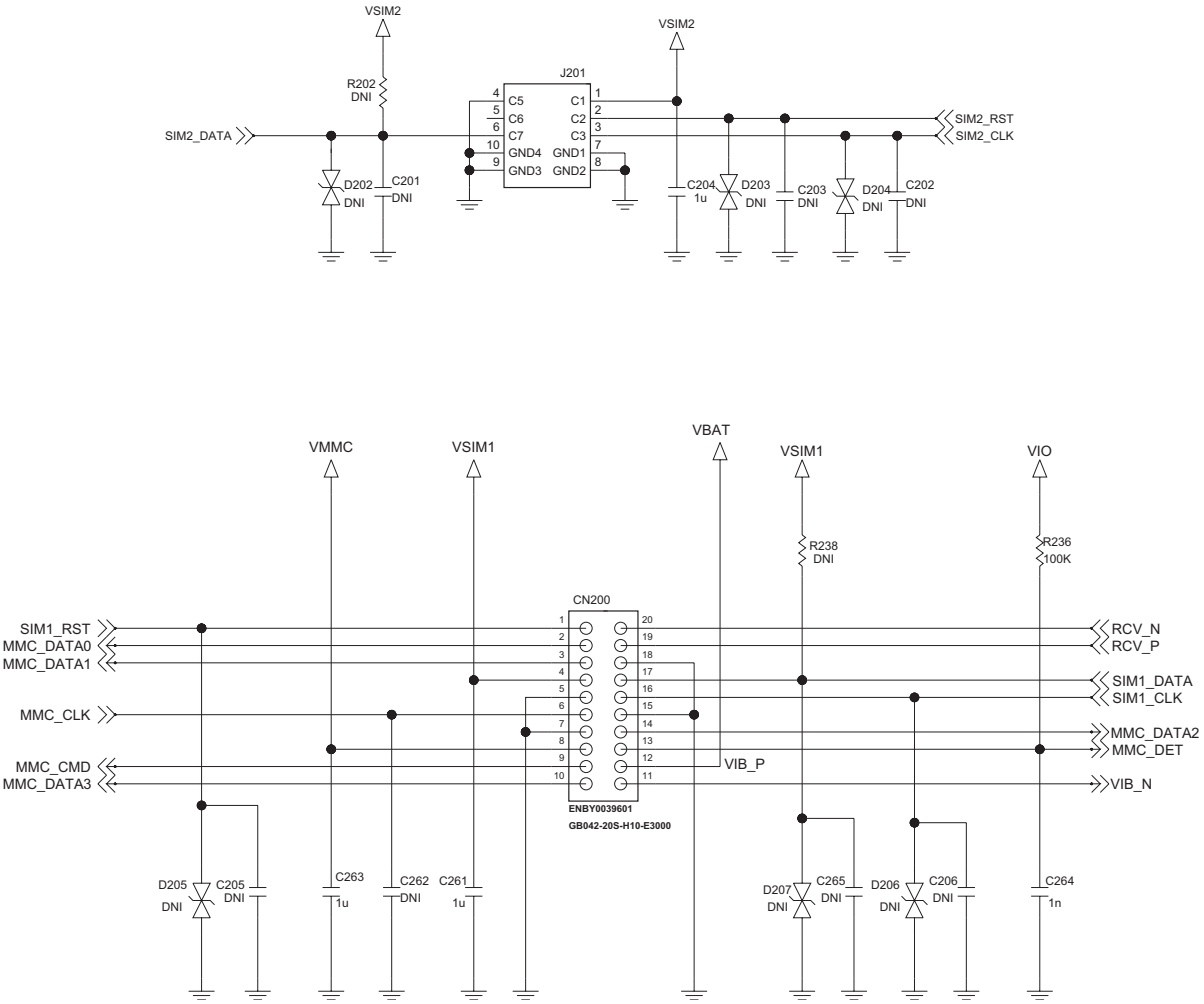


Figure 3.8.1 SIM Connector Circuit Diagram

The Main Base Band Processor(MT6253) contains two dedicated smart card interfaces to allow the MCU to access the two SIM cards. Each interface can operator via 5 terminals. As shown is the Figure 3.8.2, SIMVCC, SIMSEL, SIMRST, SIMCLK and SIMDATA are for one SIM interface, while SIM2VEE, SIM2SEL, SIM2RST, SIM2CLK and SIM2DATA are for the other one.
The functions of the two SIM interfaces are identical; therefore, only first SIM interface will be described in this document.
The VSIM is used to control the external voltage supply to the SIM card and SIM SEL determines the regulated smart card supply voltage. SIMRST is used as the SIM card reset signal. Besides, SIMDATA and SIMCLK are used for data exchange purpose

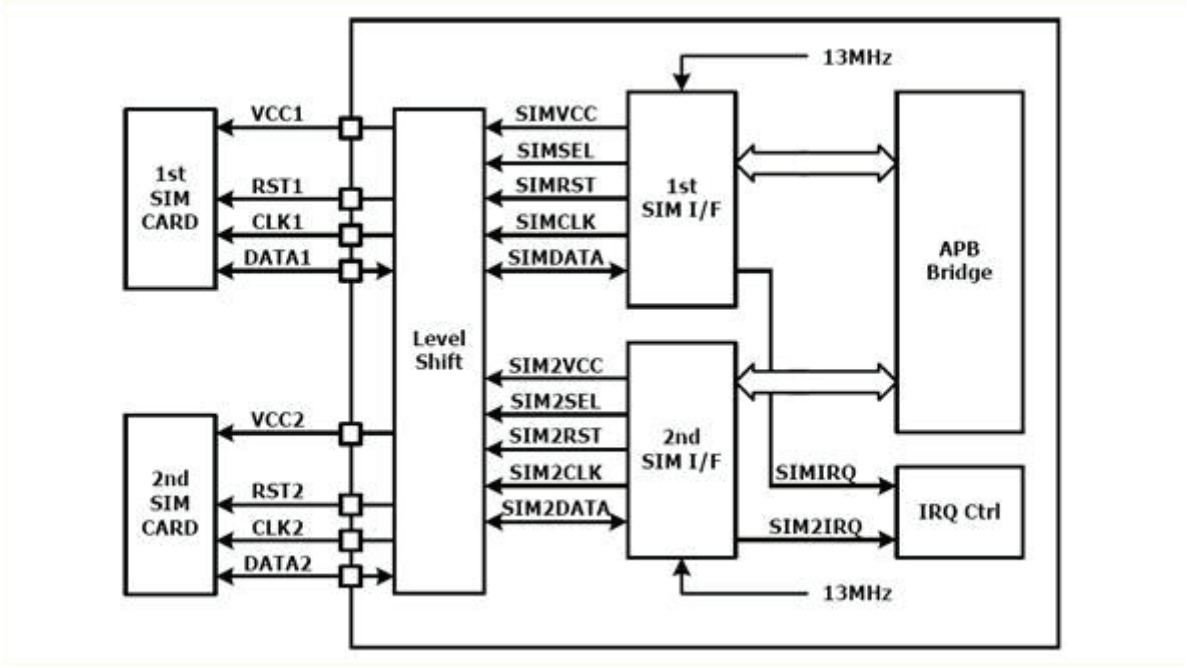


Figure 3.8.2 SIM Interface block diagram

3.9 Micro-SD Card Interface

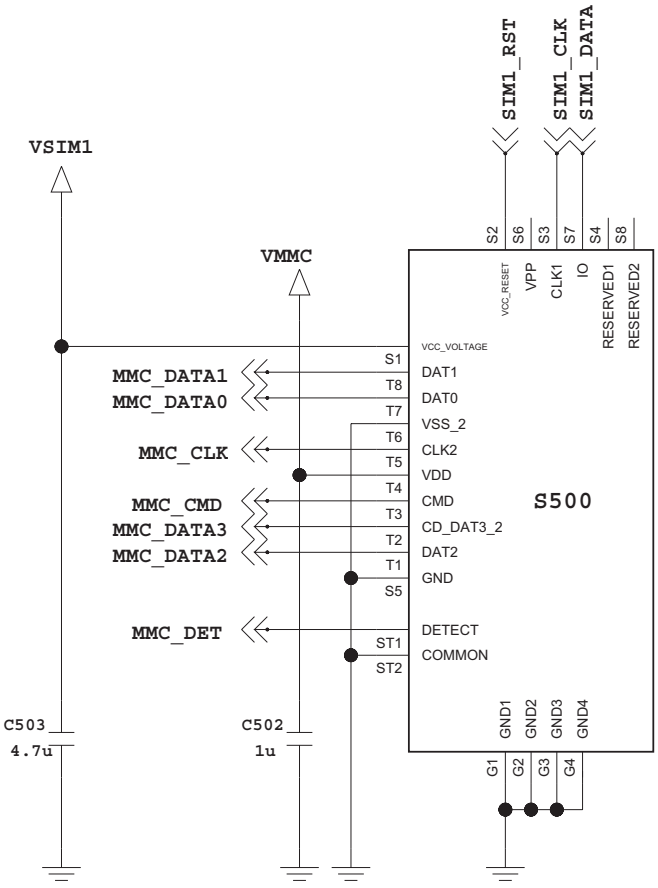


Figure 3.9.1 Micro-SD Card Interface

The controller fully supports the Memory Stick bus protocol as defined in Format Specification version 2.0 of Memory Stick Standard (Memory Stick PRO) and the SD Memory Card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0 as well as the Multi Media Card(MMC) bus protocol as defined in MMC system specification version 4.1. Since SD memory Card bus protocol is backward compatible to MMC bus protocol, the controller is capable of working well as the host on MMC bus under control of proper firmware. Furthermore, the controller also support SDIO card specification version 1.0 partially. However, the controller can only be configured as either the host controller.

3.9.1 Pin Assignment

Since the controller can only be configured as either the host of Memory Stick or the host of SD/MMC Memory Card at one time, pins for Memory Stick and SD/MMC Memory Card are shared in order to save pin counts. The following lists pins required for Memory Stick and SD/MMD Memory Card. Figure 3.9.2 shows how they are shared. In Table 3.9.1, all I/O pads have embedded both pull up and pull down resistor because they are shared by both the Memory Stick and SD/MMC Memory Card. Pins 2,4,5,8 are only useful for SD/MMC Memory Card. Pull down resistor for these pins can be used for power saving. All embedded pull-up and pull-down resistors can be disabled by programming the corresponding control registers if optimal pull-up or pull-down resistor are required on the system board. The pin VDDPD is used for power saving. Power for Memory Stick or SD/MMC Memory Card can be shut down by programming the corresponding control register. The pin WP(Write Protection) is only valid when the controller is configured for SD/MMC Memory Card. It is used to detect the status of Write Protection Switch on SD/MMC Memory Card.

No.	Name	Type	MMC	SD	MS	MSPRO	Description
1	SD_CLK	O	CLK	CLK	SCLK	SCLK	Clock
2	SD_DAT3	I/O/PP		CD/DAT3		DAT3	Data Line [Bit 3]
3	SD_DAT0	I/O/PP	DAT0	DAT0	SDIO	DAT0	Data Line [Bit 0]
4	SD_DAT1	I/O/PP		DAT1		DAT1	Data Line [Bit 1]
5	SD_DAT2	I/O/PP		DAT2		DAT2	Data Line [Bit 2]
6	SD_CMD	I/O/PP	CMD	CMD	BS	BS	Command Or Bus State
7	SD_PWRON	O					VDD ON/OFF
8	SD_WP	I					Write Protection Switch in SD
9	SD_INS	I	VSS2	VSS2	INS	INS	Card Detection

Table 3.9.1 Sharing of pins for Memory Stick and SD/MMC Memory Card controller

3.9.2 Card Detection

For SD/MMC Memory Card, detection of card insertion/removal by hardware is also supported. Because a pull down resistor with about 470 KΩ resistance which is impractical to embed in an I/O pad is needed on the signal CD/DAT3, and it has to be capable of being connected or disconnected dynamically onto the signal CD during initialization period, an additional I/O pad is needed to switch on/off the pull down resistor on the system board. The scenario of card detection for SD/MMC Memory Card is shown in Figure 3.9.2. Before SD/MMD Memory Card is inserted or powered on, SW1 and SW2 shall be opened for card detection of the host side. Meanwhile, pull down resistor R_{CD} on system board shall attach onto the signal CD/DAT3 by the output signal RCDEN. In addition, SW3 on the card is default to be closed. Upon insertion of SD/MMC Memory Card the signal CD/DAT3 will have a transition from low to high. If SD/MMC Memory Card is removed then the signal CD/DAT3 will return to logic low. After the card identification process, pull down resistor R_{CD} on system board shall disconnect with the signal CD/DAT3 and SW3 on the card shall be opened for normal operation.
Since the scheme above needs a mechanical switch such as a relay on system board, it is not ideal enough. Thus, a dedicated pin “INS” is used to perform card insertion and removal for SD/MMC. The pin “INS” will connect to the pin “VSS2” of a SD/MMC connector.

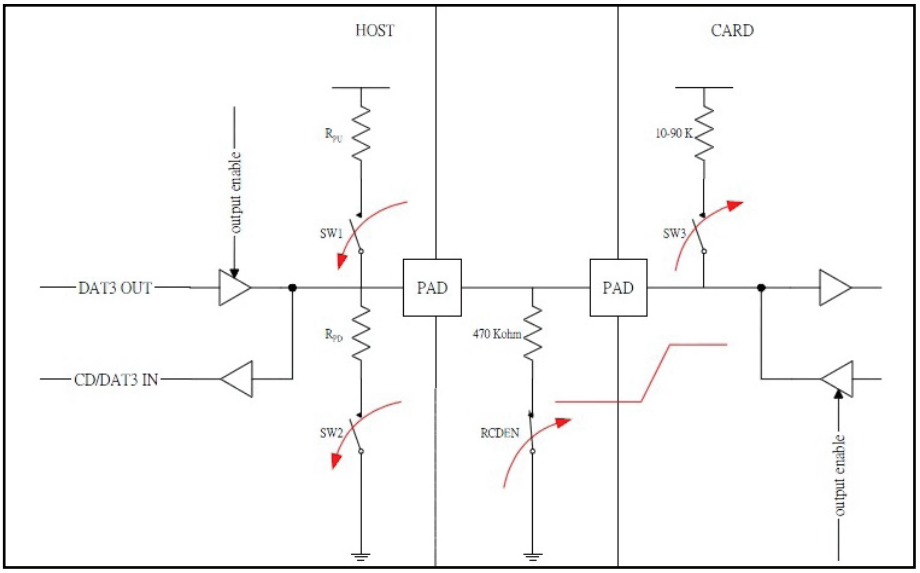


Figure 3.9.2 Card Detection for SD/MMC Memory Card

3.10 LCD Interface

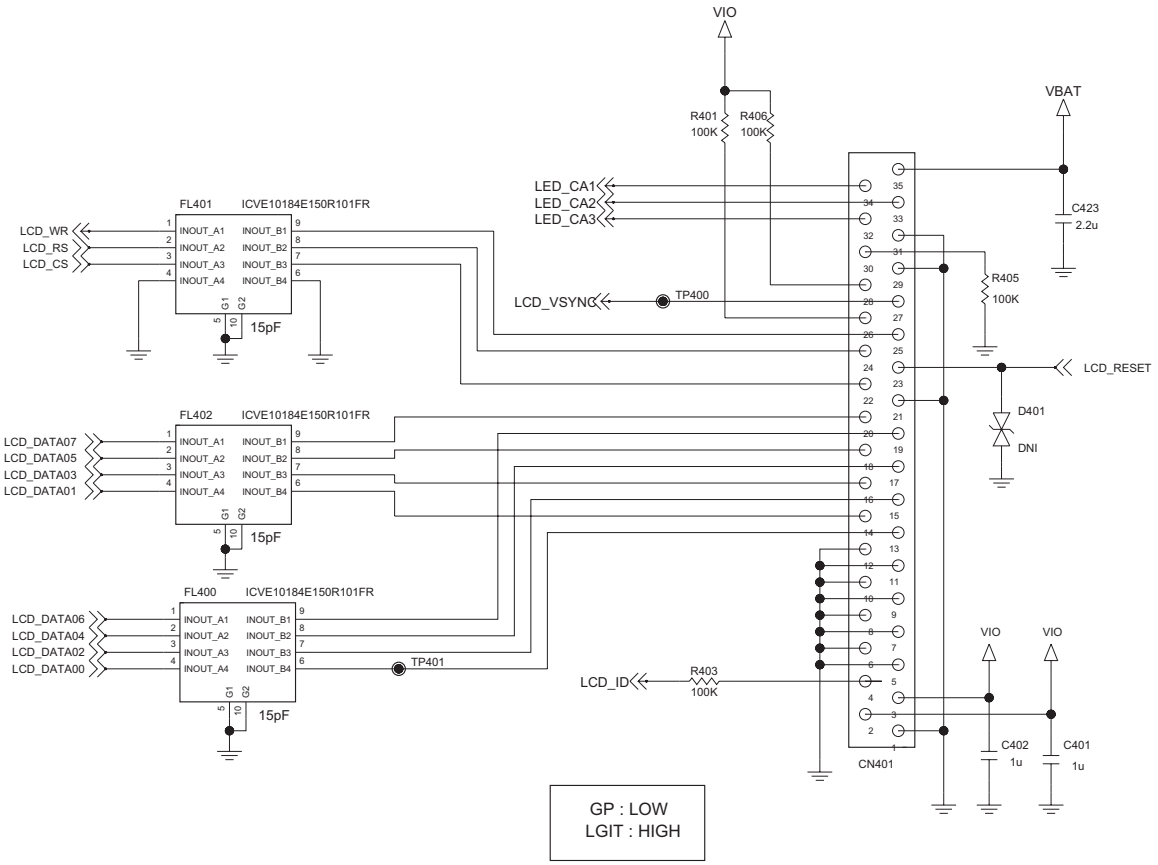


Figure 3.10.1 LCD Interface

ILI9225 is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 176RGBx220 dots, comprising a 528-channel source driver, a 220-channel gate driver, 87120 bytes RAM for graphic data of 176RGBx220 dots, and power supply circuit.
ILI9225 can operate with low I/O interface power supply up to 1.65V, with an incorporated voltage follower circuit to generate voltage levels for driving an LCD.
The ILI9225 also supports a function to display in 8 colors and a standby mode, allowing for precise power control by software. These features make the ILI9225 an ideal LCD driver for medium or small size portable products such as digital cellular phones or small PDA, where long battery life is a major concern.

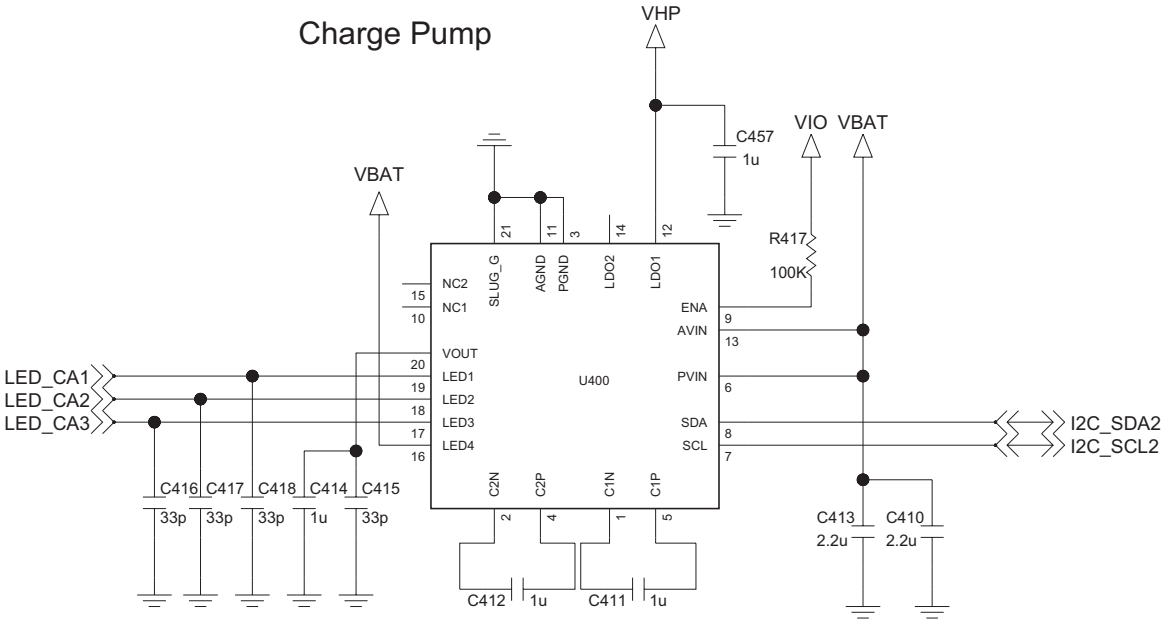


Figure 3.10.2 Charge Pump CIRCUIT DIAGRAM

The RT9367C is an integrated solution for backlighting and phone camera input supply. The part contains a charge pump white LED driver and dual low dropout linear regulators. This IC can be shut down by pulling EN low.

In the section of charge pump, The RT9367C can power up 4 white LEDs with regulated constant current for uniform intensity. Each channel (LED1-LED4) can support up to 25mA. The part maintains highest efficiency by utilizing a x1/x1.5/x2 fractional charge pump and low dropout current regulators. An internal 5-bit DAC is used for brightness control. Users can easily configure up to 32-step of LED current by I2C interface.

In the section of linear regulator, The RT9367C comprises a dual channel, low noise, and low dropout regulator sourcing up to 300mA at each channel. The range of output voltage can be configured from 1.1V to 3.3V by I2C interface. The outputs of LDO offer 3% accuracy and low dropout voltage of 250mV @ 300mA. The LDO also provides current limiting and output short circuit thermal folded back protection.

3.11 Battery Charger Interface

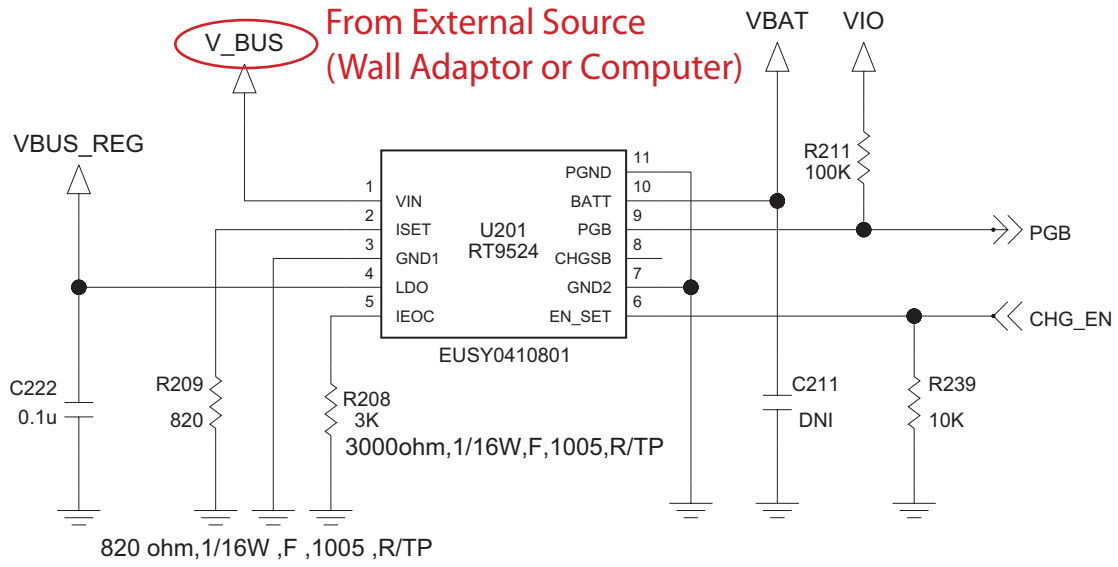


Figure 3.11.1 BATTERY CHARGER BLOCK

The RT9524 is a fully integrated single-cell Li-Ion battery charger IC ideal for portable applications. The RT9524 optimizes the charging task by using a control algorithm including pre-charge mode, fast charge mode and constant voltage mode. The input voltage range of the VIN pin can be as high as 30V. When the input voltage exceeds the OVP threshold, it will turn off the charging MOSFET to avoid overheating of the chip.
In RT9524, the maximum charging current can be programmed with an external resister. For the USB application, user can set the current to 100mA/500mA through EN/SET pin. For the factory mode, the RT9524 can allow 4.2V/2.3A power pass through to support system operation. It also provides a 50mA LDO to support the power of peripheral circuit. The internal thermal feedback circuit regulates the die temperature to optimize the charge rate for all ambient temperatures. The RT9524 provides protection functions such as under voltage protection, over voltage protection for VIN supply and thermal protection for battery temperature.
The RT9524 is available in a WDFN-10L 2x3 package to achieve optimized solution for PCB space and thermal considerations.

3.12 Keypad Interface

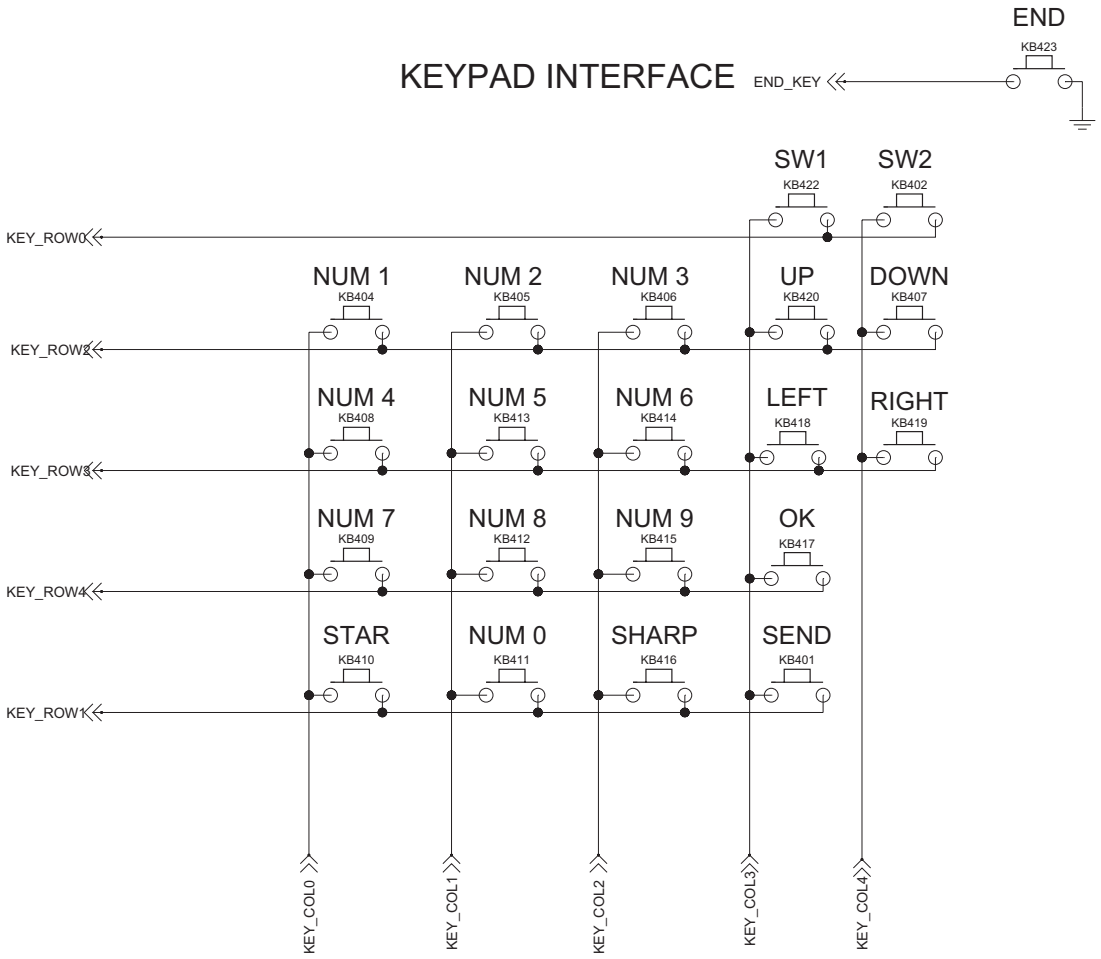


Figure 3.12.1 MAIN KEY STRUCTURE

The keypad can be divided into two parts: one is the keypad interface including 7 columns and 6 rows with one dedicated power-key, as shown in Figure 3.12.2; the other is the key detection block which provides key pressed, key released and de-bounce mechanisms. Each time the key is pressed or released, i.e. something different in the 6 x 7 matrix or power-key, the key detection block senses the change and recognizes if a key has been pressed or released. Whenever the key status changes and is stable, a KEYPAD IRQ is issued. The MCU can then read the key(s) pressed directly in KP_MEM1, KP_MEM2, KP_MEM3, and KP_MEM4 registers. To ensure that the key pressed information is not missed, the status register in keypad is not read-cleared by APB read command. The status register can only be changed by the key-pressed detection FSM.

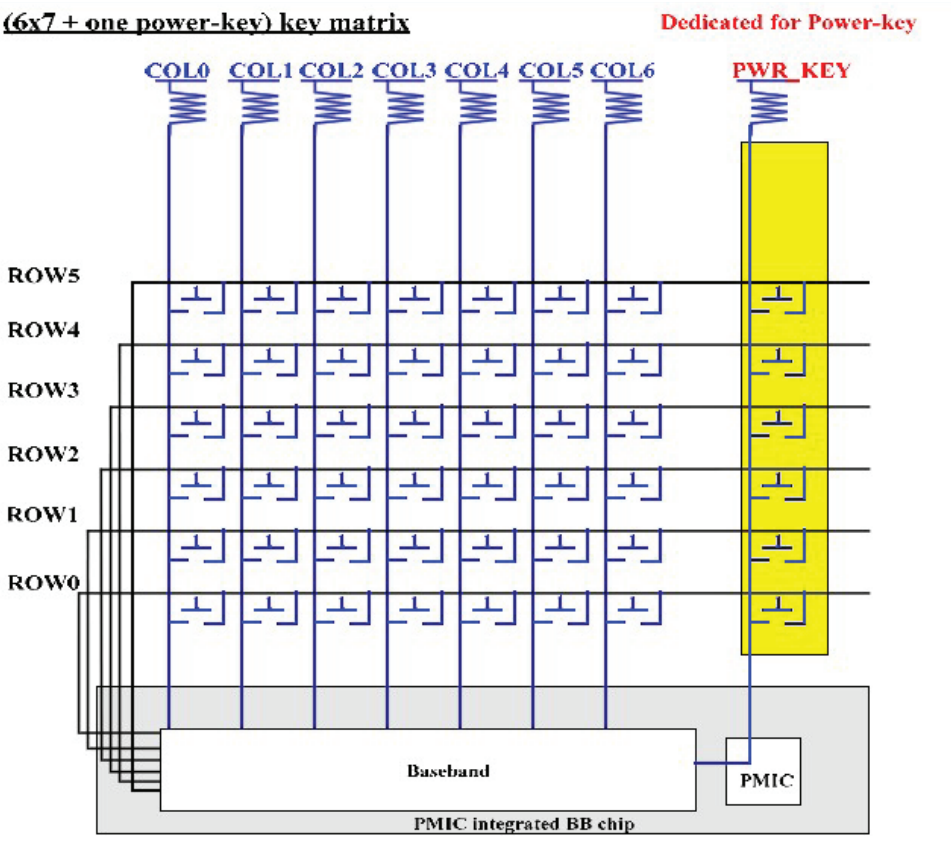


Figure 3.12.2 6x7 matrix with one power-key

This keypad can detect one or two key-pressed simultaneously with any combination. Figure 3.12.3 shows one key pressed condition. Figure 3.12.4(a) and Figure 3.12.4(b) illustrate two keys pressed cases. Since the key press detection depends on the HIGH or LOW level of the external keypad interface, if keys are pressed at the same time and there exists a key that is on the same column and the same row with the other keys, the pressed key cannot be correctly decoded. For example, if there are three key presses: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), then both key3 and key4 = (x2, y1) are detected, and therefore they cannot be distinguished correctly. Hence, the keypad can detect only one or two keys pressed simultaneously at any combination. More than two keys pressed simultaneously in a specific pattern retrieve the wrong information.

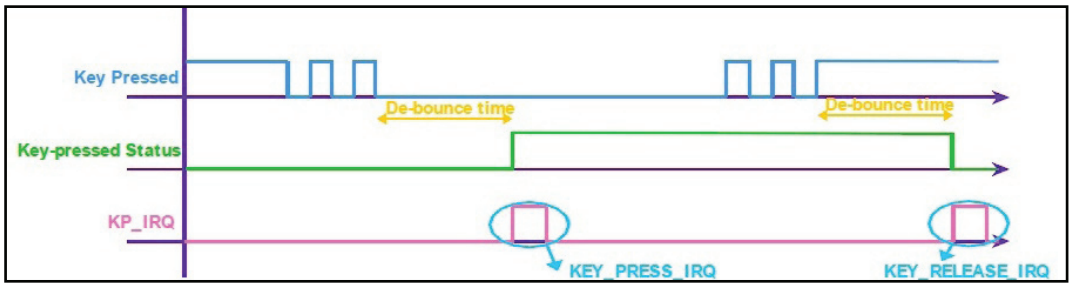


Figure 3.12.3 One key pressed with de-bounce mechanism denoted

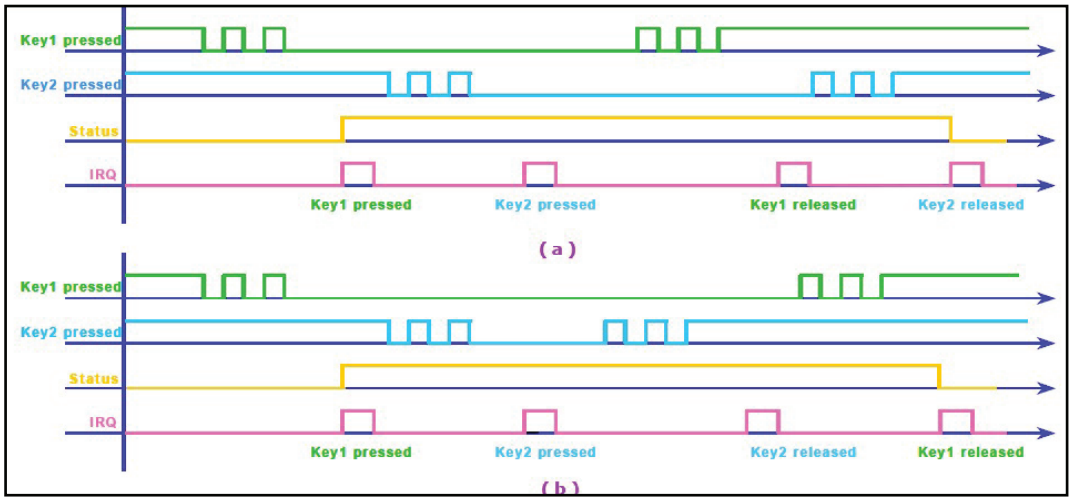


Figure 3.12.4 Two keys pressed, case 1 (b) Two keys pressed, case 2

3.13 Audio Front-End

3.13.1 General Description

The audio front-end essentially consists of voice and audio data paths. Figure 3.13.1 shows the block diagram of the audio front-end. All voice band data paths comply with the GSM 03.50 specification. Mono hands-free audio or external FM radio playback paths are also provided. The audio stereo path facilitates CD-quality playback, external FM radio, and voice playback through a headset.

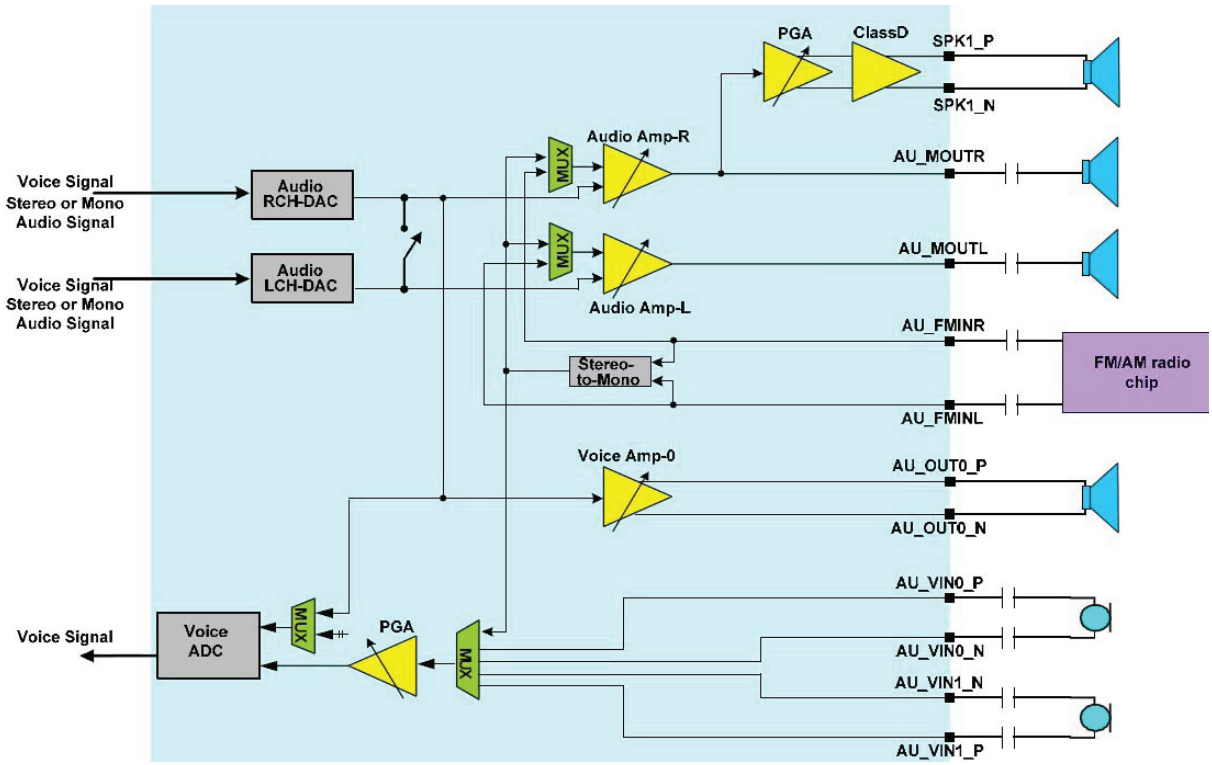


Figure 3.13.1 Block diagram of audio front end

Figure 3.13.2 shows the digital circuits block diagram of the audio front-end. The APB register block is an APB peripheral that stores settings from the MCU. The DSP audio port (DAP) block interfaces with the DSP for control and data communications. The digital filter block performs filter operations for voice band and audio band signal processing. The Digital Audio Interface (DAI) block communicates with the System Simulator for FTA or external Bluetooth modules.

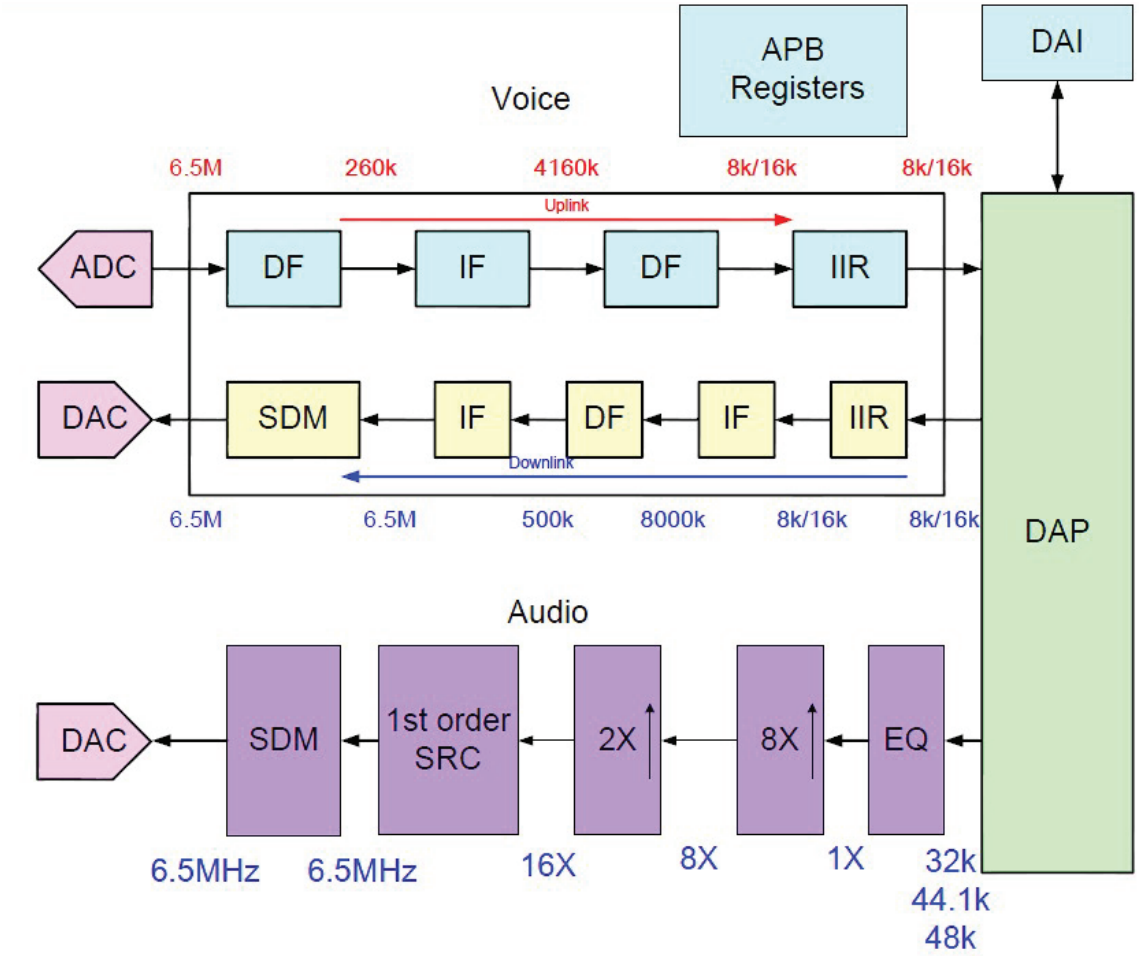


Figure 3.13.2 Block diagram of digital circuit of audio front end

To communicate with the external Bluetooth module, the master-mode PCM interface and master-mode I2S/EIAJ interface are supported. The clock of PCM interface is 256 kHz while the frame sync is 8 kHz. Both long sync and short sync interfaces are supported. The PCM interface can transmit 16-bit stereo or 32-bit mono 8 kHz sampling rate voice signal. Figure 3.13.3 shows the timing diagram of the PCM interface. Note that the serial data changes when the clock is rising and is latched when the clock is falling.

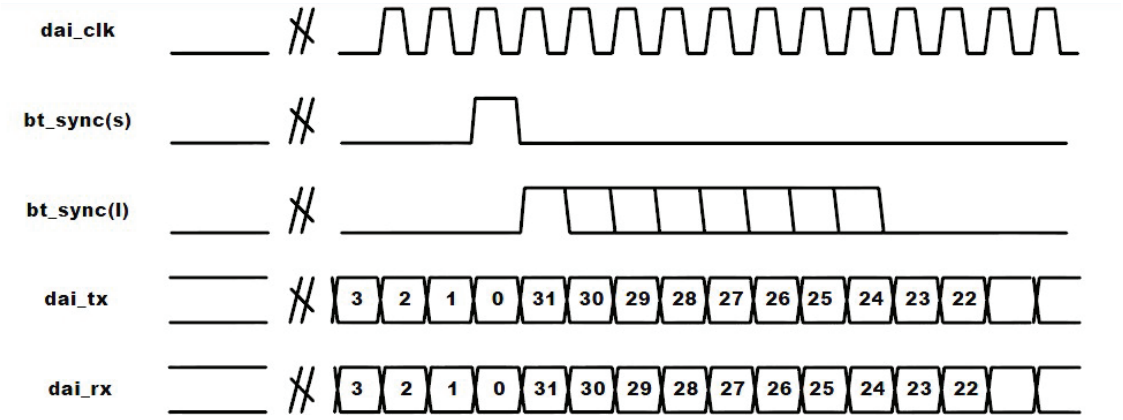


Figure 3.13.3 Timing diagram of Bluetooth application

I2S/EIAJ interface is designed to transmit high quality audio data. Figure 3.13.4 and Figure 3.13.5 illustrate the timing diagram of the two types of interfaces. I2S/EIAJ can support 32 kHz, 44.1 kHz, and 48 kHz sampling rate audio signals. The clock frequency of I2S/EIAJ can be 32×(sampling frequency), or 64×(sampling frequency). For example, to transmit a 44.1 kHz CD-quality music, the clock frequency should be 32 × 44.1 kHz = 1.4112 MHz or 64 × 44.1 kHz = 2.8224 MHz.

I2S/EIAJ interface is not only used for Bluetooth module, but also for external DAC components. Audio data can easily be sent to the external DAC through the I2S/EIAJ interface. In this document, the I2S/EIAJ interface is referred to as EDI (External DAC Interface).

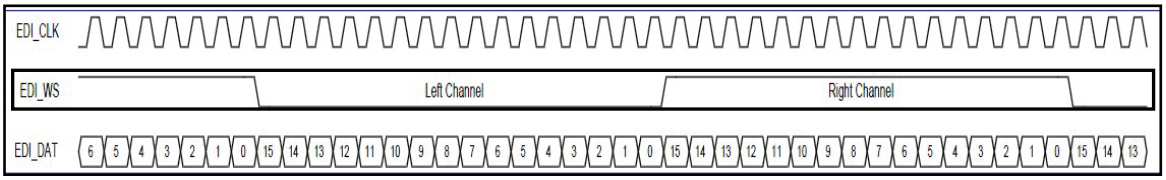


Figure 3.13.4 Block diagram of digital circuit of audio front end

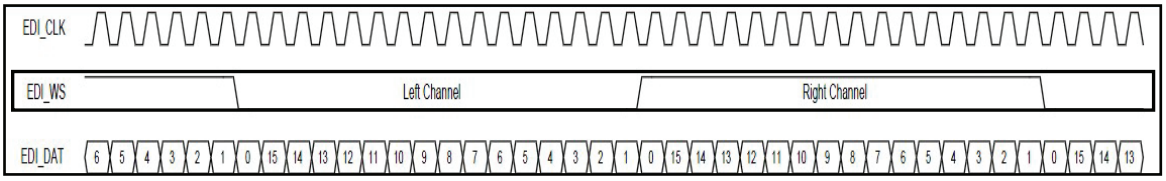


Figure 3.13.5 Block diagram of digital circuit of audio front end

3.14 Camera Interface

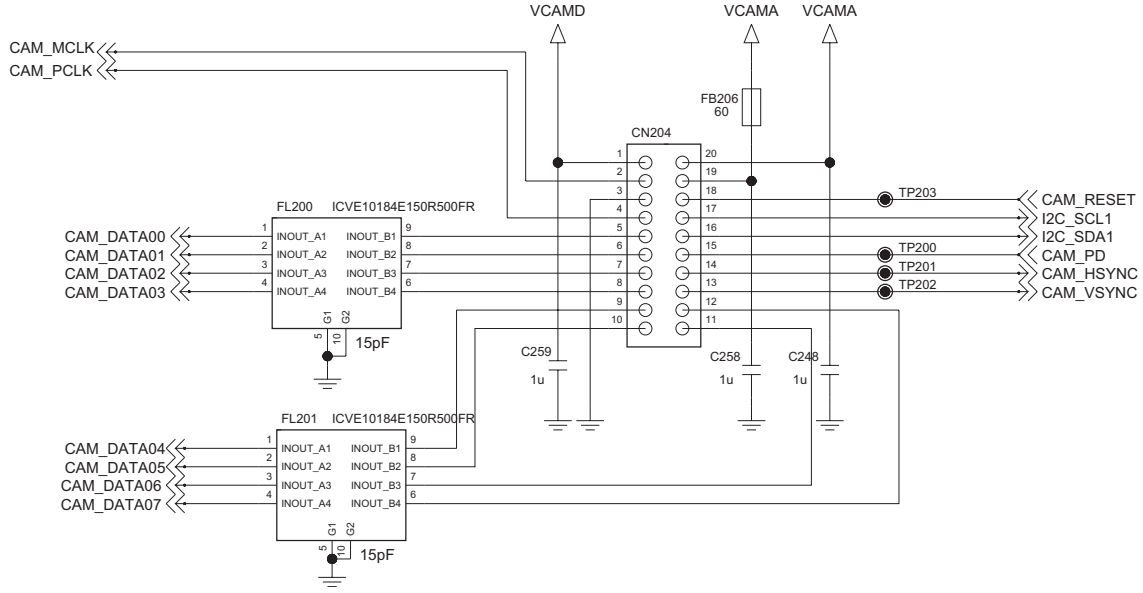


Figure 3.14.1 Camera Interface

The S5KA3DFX is a highly integrated VGA camera chip which includes CMOS image sensor (CIS) and Image Signal Processor (ISP). It is fabricated by SAMSUNG 0.13μm CMOS image sensor process developed for imaging application to realize high-efficiency and low-power photo sensor. The sensor consists of 640 x 480 effective pixels which meet with 1/10 inch optical format. The CIS has onchip 10-bit ADC arrays to digitize the pixel output and also on-chip Correlated Double Sampling (CDS) to reduce Fixed Pattern Noise (FPN) drastically. The ISP performs sophisticated image processing functions including color interpolation and correction, lens shading correction, edge enhancement, gamma correction, image scaling, noise reduction, auto exposure (AE), auto white balance (AWB), auto flicker correction, and auto defect correction. The AE and AWB functions are performed by an embedded 8-bit processor which uses to run built-in these sophisticated algorithms. The programmable functions are controlled by host processor via 2-wire I2C bus interface. The S5KA3DFX, which needs a single master clock, is suitable for low power camera module with 2.8V/1.8V or 2.8V/1.5Vpower supply.

3.14.1 FEATURES

- Optical size : 1/10 inch
- Unit pixel size : 2.25 um x 2.25 um
- Effective resolution : 656 (H) x 496 (V), VGA
- Color filter : RGB Bayer Pattern
- Shutter type : Electronic Rolling Shutter
- Scan mode : Line Progressive Readout
- Output format : Parallel 10/9/8-Bit (ITU-R.601/656 YUV422, RGB565, RGB444, and RAW10)
  Serial CCP-1 (YUV422, 565RGB, 444RGB, and RAW10)
- Frame rate : 15fps@VGA, 13MHz (30fps@VGA, 26MHz)
- ADC resolution : 10-Bit
- Lens shading correction
- Color interpolation and color correction
- Noise reduction
- Edge enhancement
- Gamma correction
- Image effect: sepia, negative, gray, red, green, blue
- Image scaling: CIF(352x288), QVGA(320x240), QCIF(176x144), QQVGA(160x120), and SubQCIF(128x96)
- Auto bad pixel replacement (defect correction, continuous 2x2 cluster removable)
- Auto flicker correction
- Auto exposure (AE)
- Auto white balance (AWB)
- Programmable functions:
  WOI (Window of Interest) panning, cropping, sizing and sub-sampling
  Vertical flip and horizontal mirror
  Exposure, gain, and frame rate control
- Host interface: I2C bus interface
- Internal PLL
- Internal regulator for 1.8V core supply voltage
- 8-bit parallel data interface
- Built-In test image generation
- Stand-by mode for power saving
- Operating temperature: -20˚C to +60˚C
- Supply voltage: 2.8V for analog, 1.8V or 1.5V for digital core and 1.8-2.8V for I/O
- Maximum pixel (data output) clock : 26MHz
- External master clock : up to 26MHz

3.15 KEY BACLKLIGHT LED Interface

Key Backlight LED is controlled by KEYPAD_LED signal of MT6253.
The built-in open drain output switch drives the Keypad LED in the handset. This switch is controlled by baseband with the enable register. The keypad LED can sink 150mA and will become high impedance as disabled.

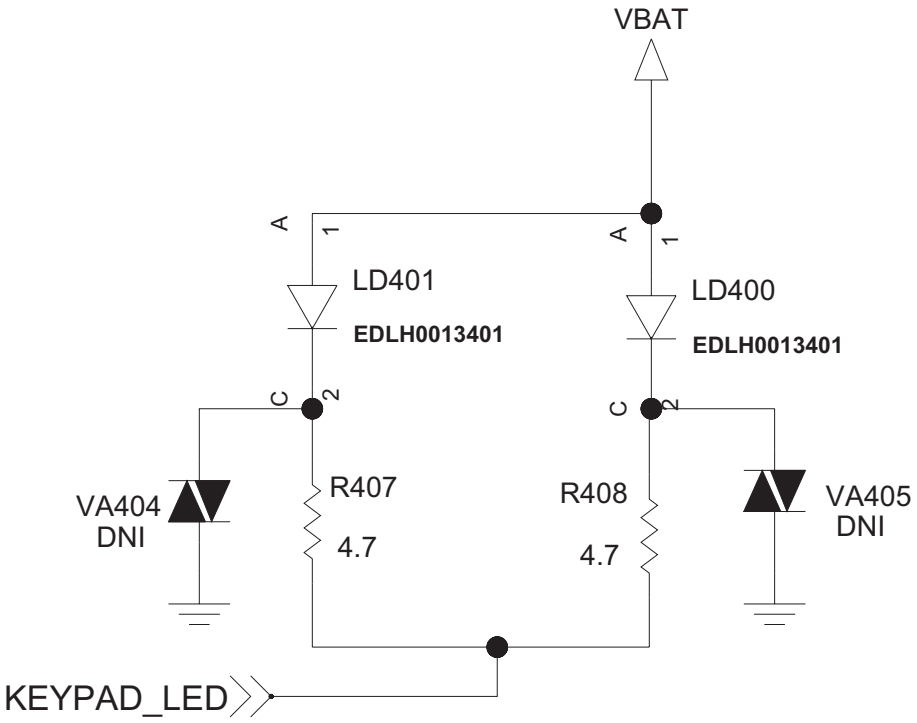


Figure 3.15.1 Key Backlight Block

3.16 Vibrator Interface

Vibrator is driven by BJT with bias resistor.
VBAT is connected with + terminal of vibrator and – terminal is connected with VIB_N. It is controlled by VIBRATOR signal of MT6253 with only ON/OFF function.

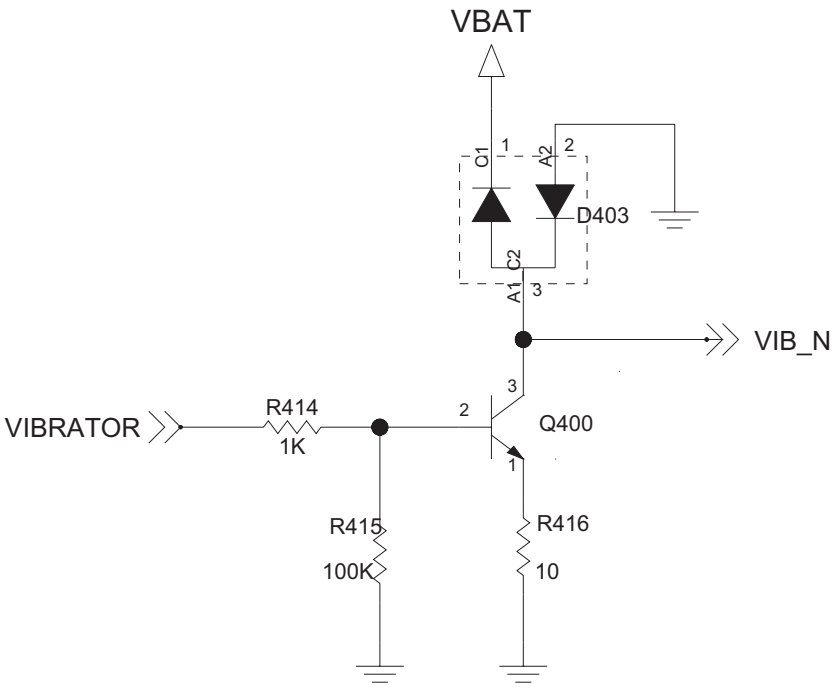


Figure 3.16.1 Vibrator Driver Block

4. TROUBLE SHOOTING

4.1 RF Component

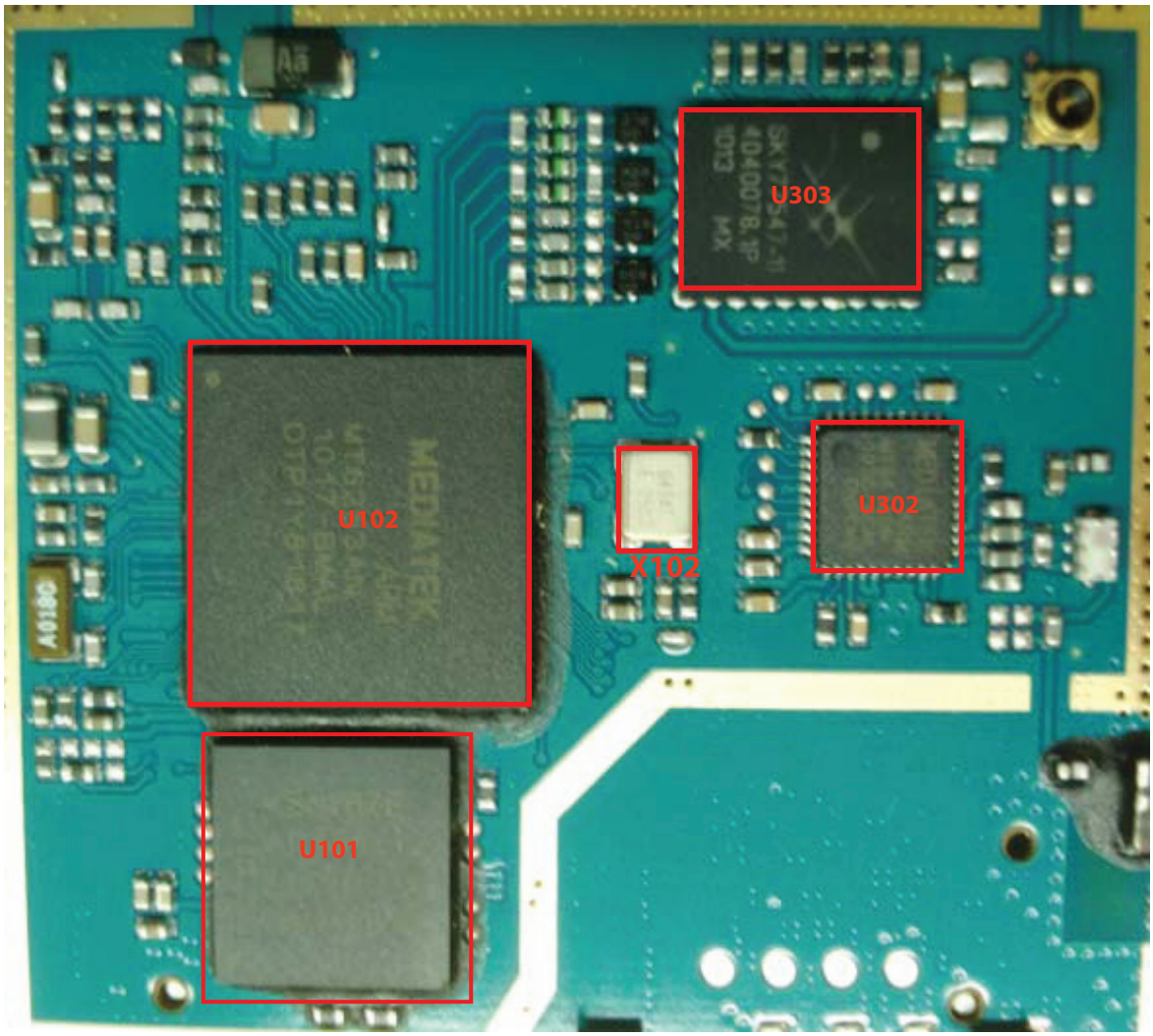
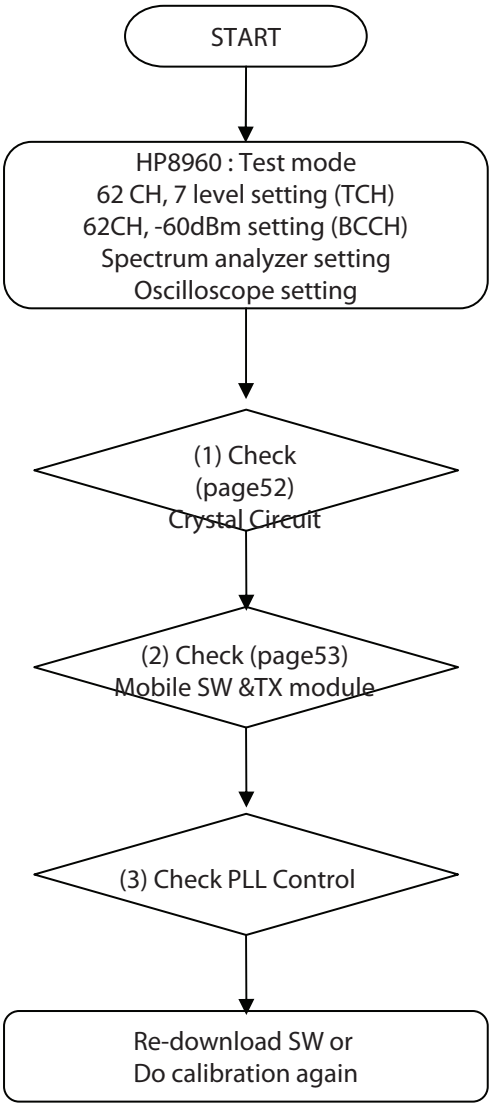


Figure 4.1

U101	Memory(256NOR/648pSDRAM) PF38F4050M0Y3DF
U102	Main Chip (MT6253)
U302	Bluetooth Chip (MT6612)
U303	TX Module (SKY77547)
X102	Crystal, 26MHz Clock

4.2 RX Trouble

CHECKING FLOW



(1) Checking Crystal Circuit

TEST POINT

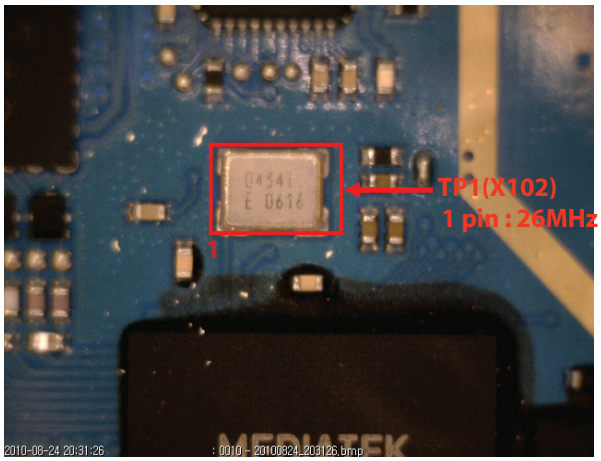
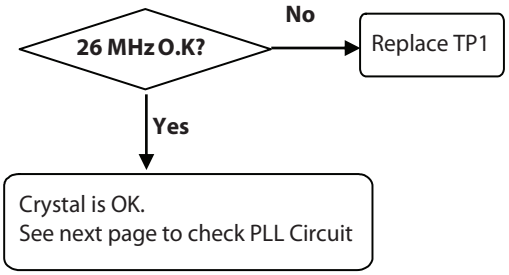
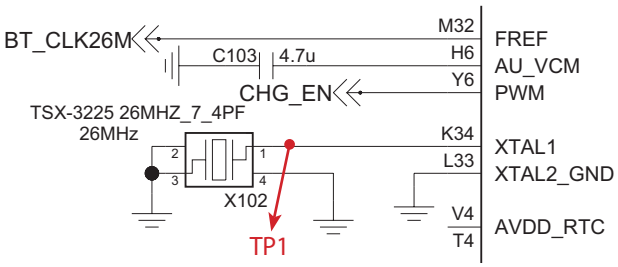


Figure 4.2.1

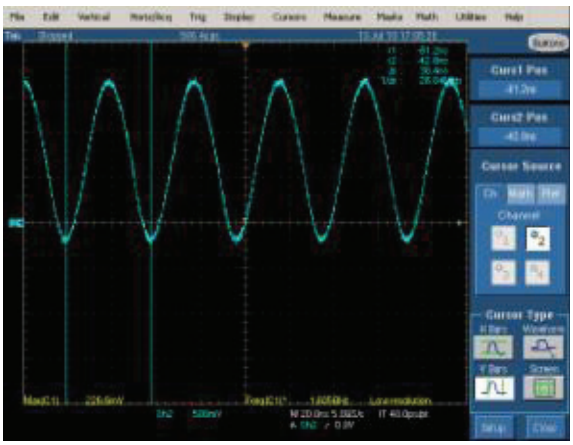
CHECKING FLOW



CIRCUIT



WAVEFORM



(2) Checking Mobile SW &Tx module

TEST POINT

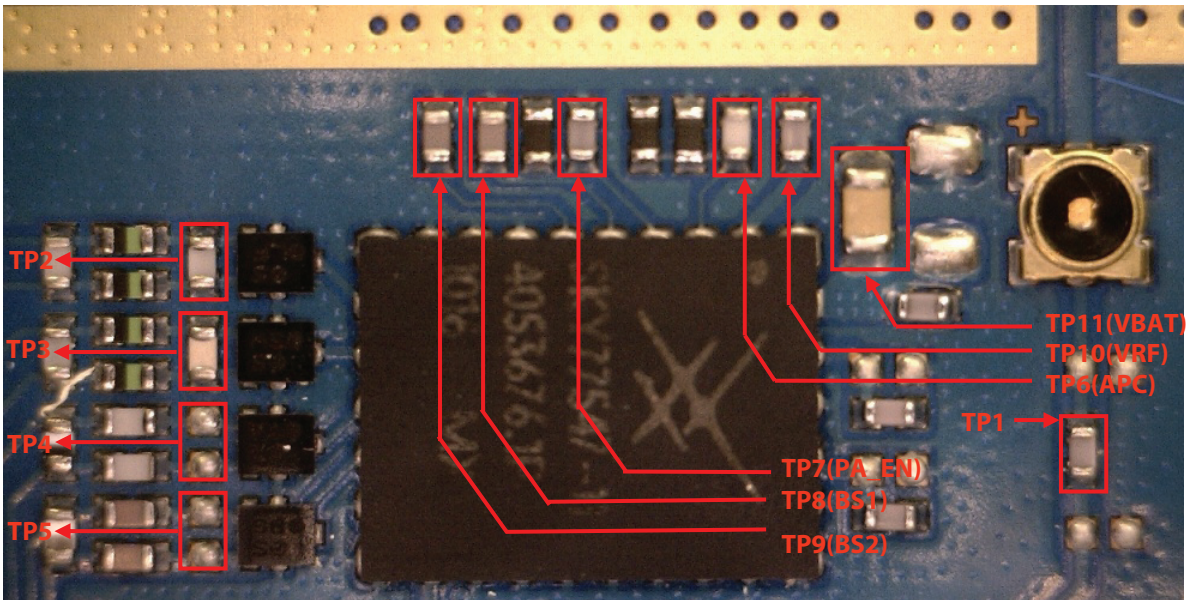
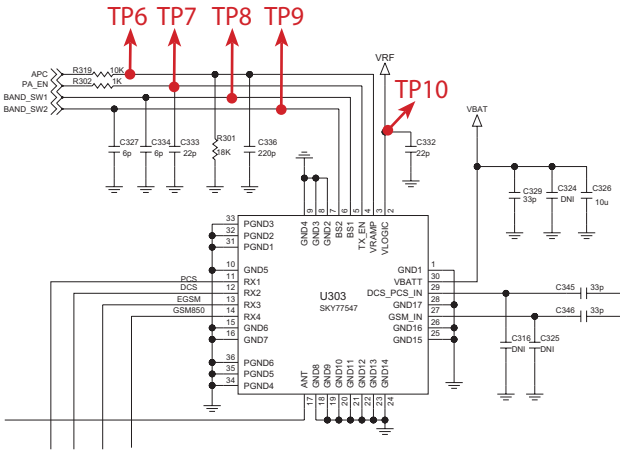


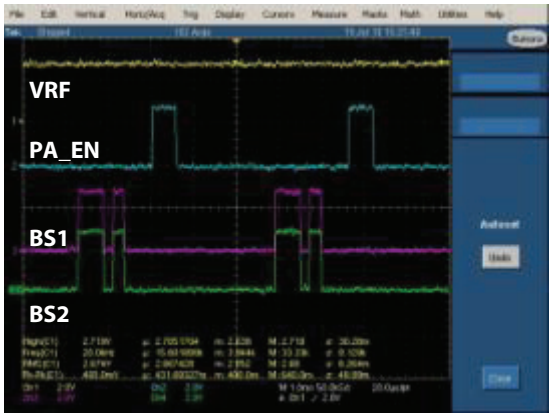
Figure 4.2.4

CIRCUIT

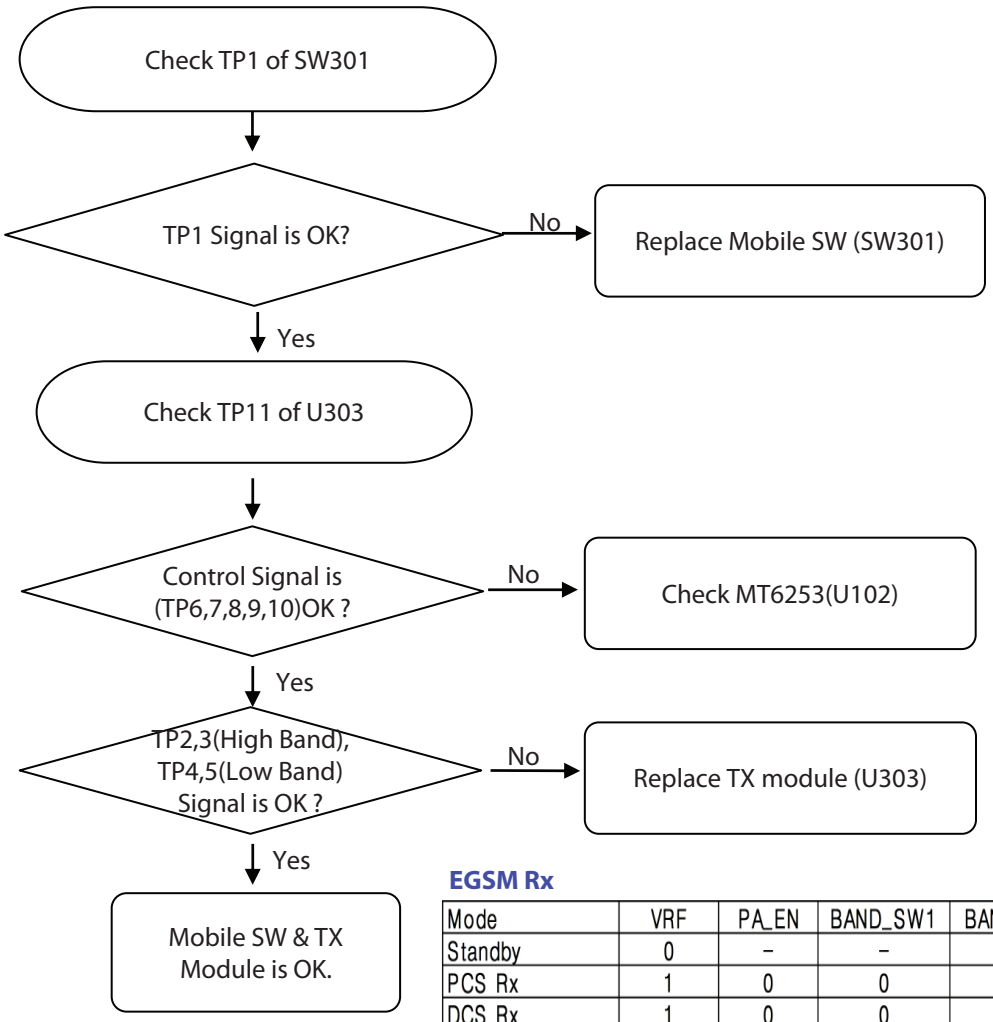


CONTROL LOGIC

EGSM Rx



CHECKING FLOW

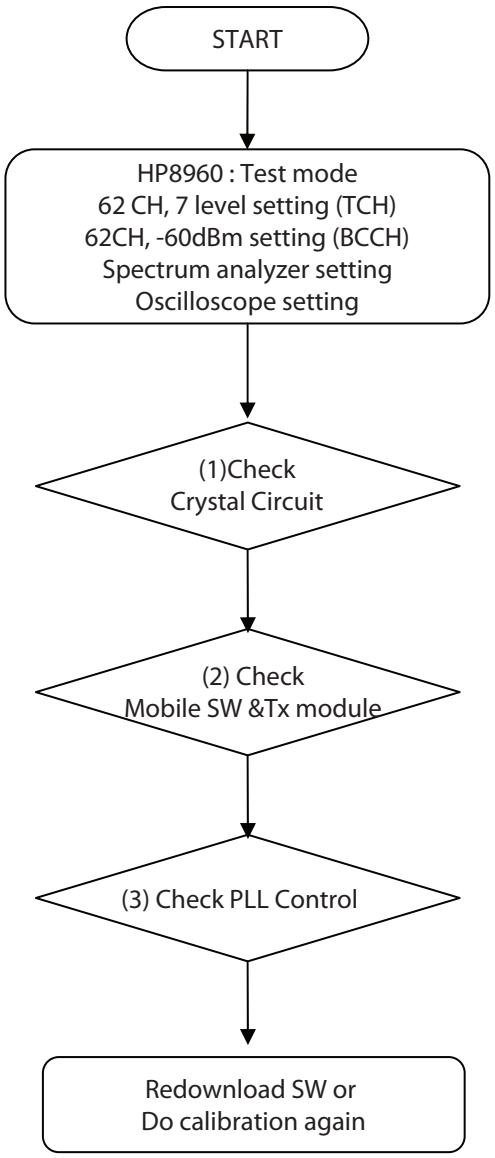


EGSM Rx

Mode	VRF	PA_EN	BAND_SW1	BAND_SW2
Standby	0	–	–	–
PCS Rx	1	0	0	0
DCS Rx	1	0	0	1
EGSM Rx	1	0	1	1
GSM850 Rx	1	0	1	0
GSM_OUT	1	1	0	–
DCS_PCS_OUT	1	1	1	–

4.3 TX Trouble

CHECKING FLOW



(1) Checking Crystal Circuit

TEST POINT

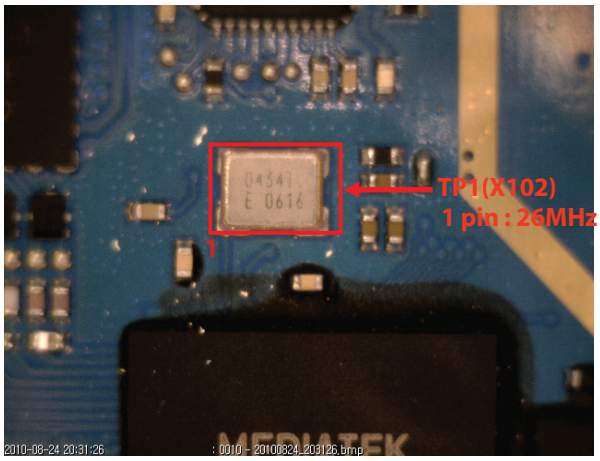
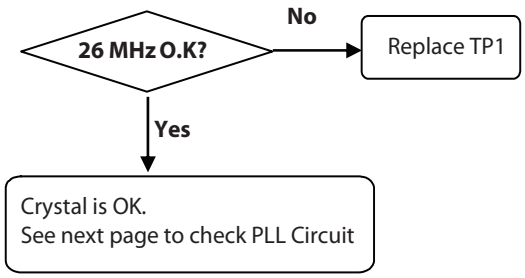
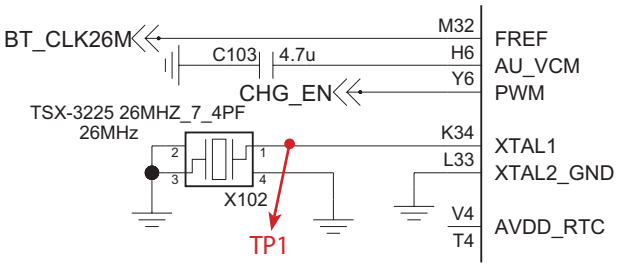


Figure 4.3.1

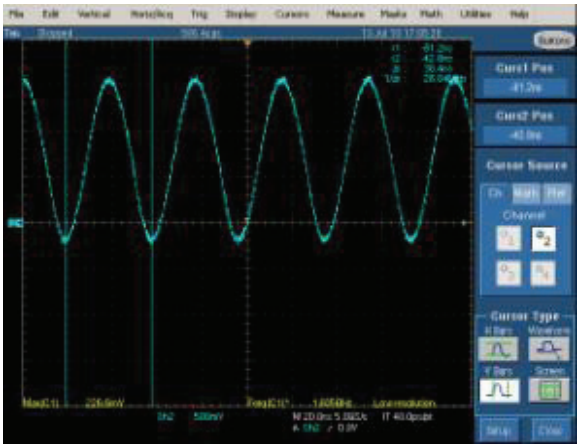
CHECKING FLOW



CIRCUIT



WAVEFORM



(2) Checking Mobile SW & TX Module

TEST POINT

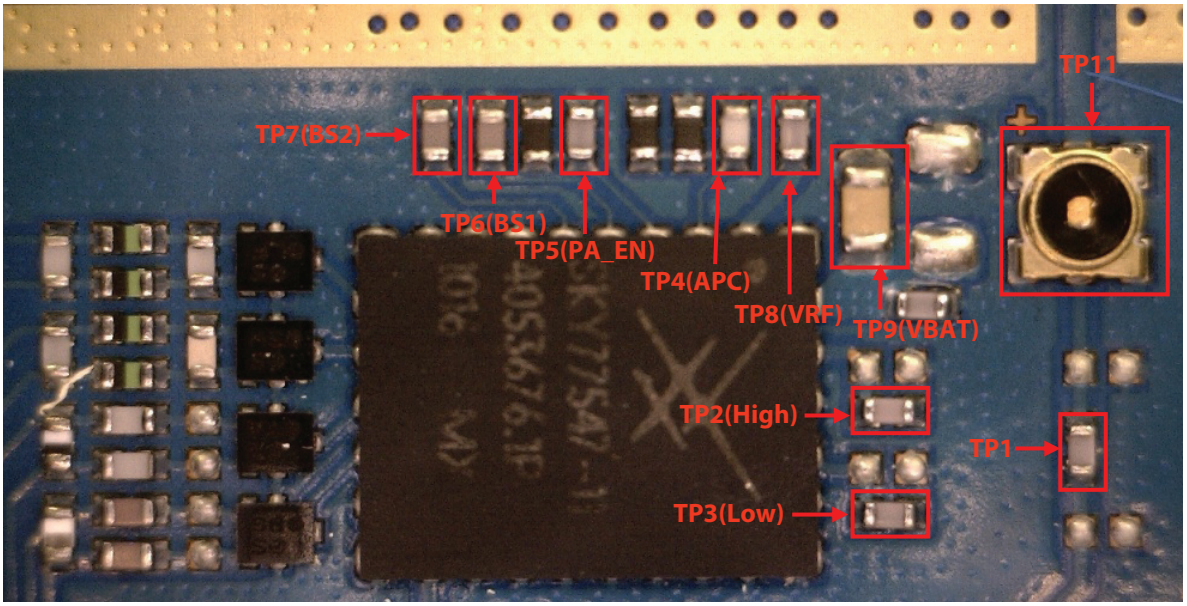
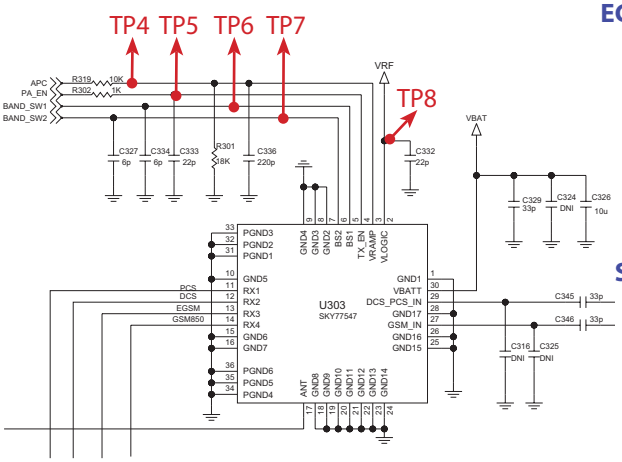
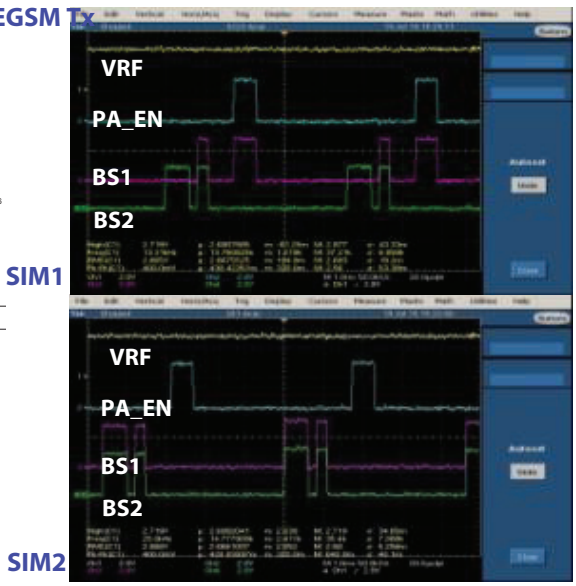


Figure 4.3.4

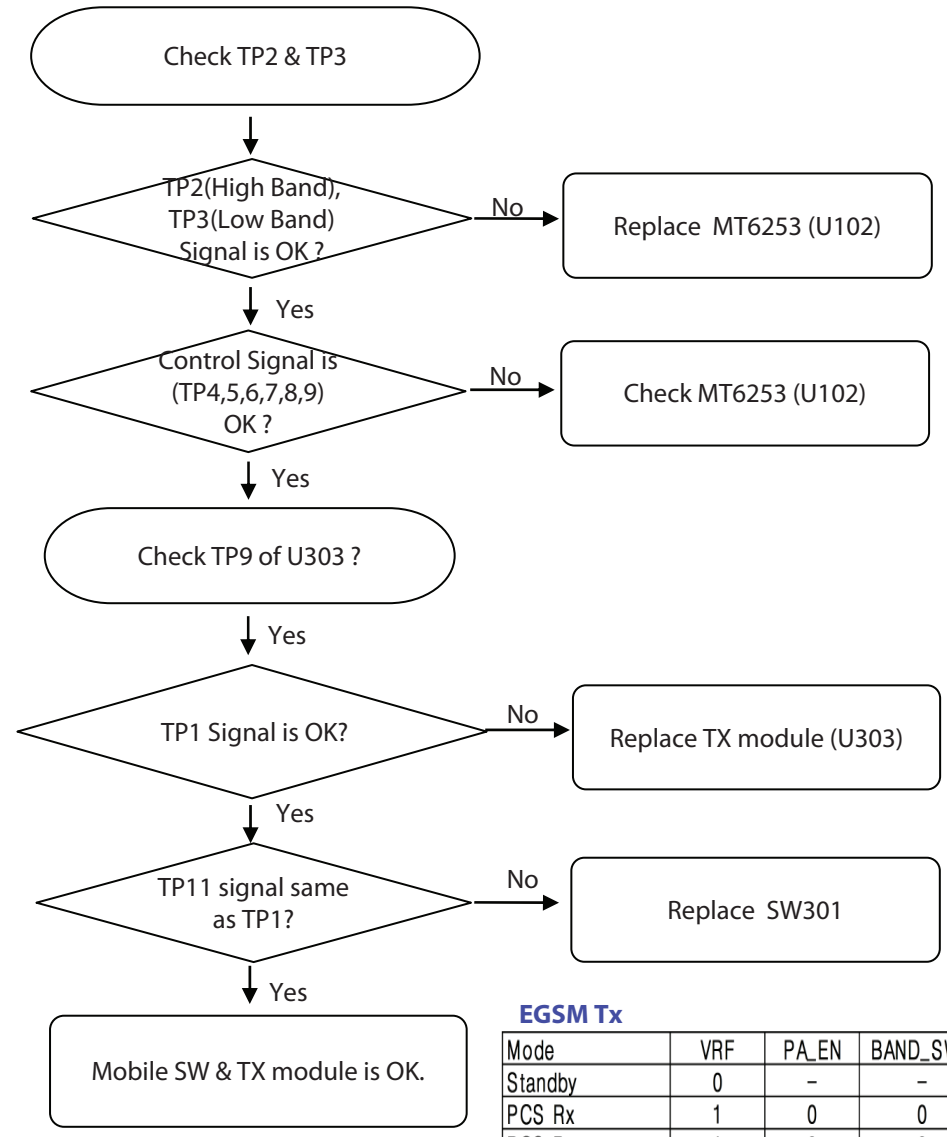
CIRCUIT



CONTROL LOGIC



CHECKING FLOW



EGSM Tx

Mode	VRF	PA_EN	BAND_SW1	BAND_SW2
Standby	0	–	–	–
PCS Rx	1	0	0	0
DCS Rx	1	0	0	1
EGSM Rx	1	0	1	1
GSM850 Rx	1	0	1	0
GSM_OUT	1	1	0	–
DCS_PCS_OUT	1	1	1	–

4.4 Power On Trouble

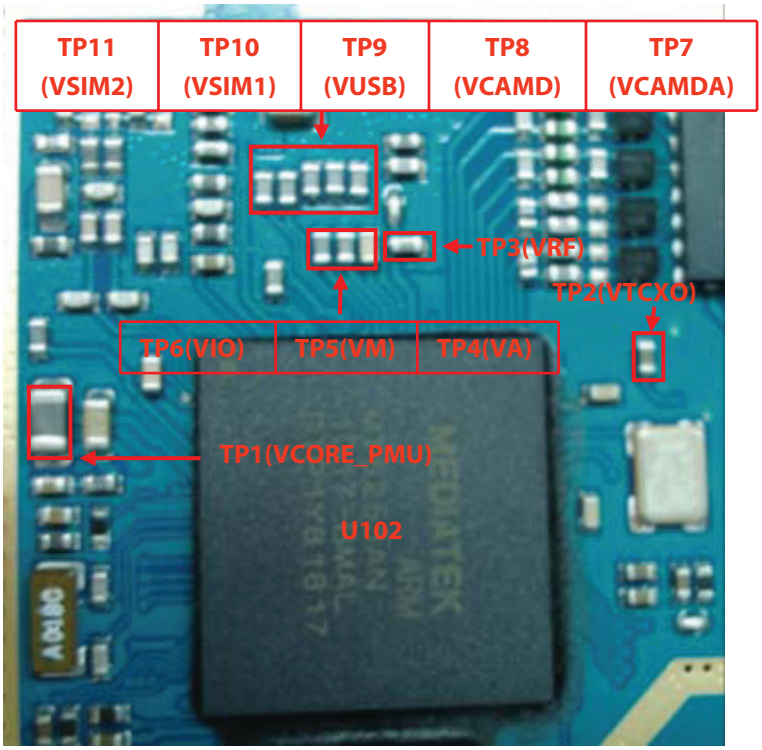


Figure 4.4.1

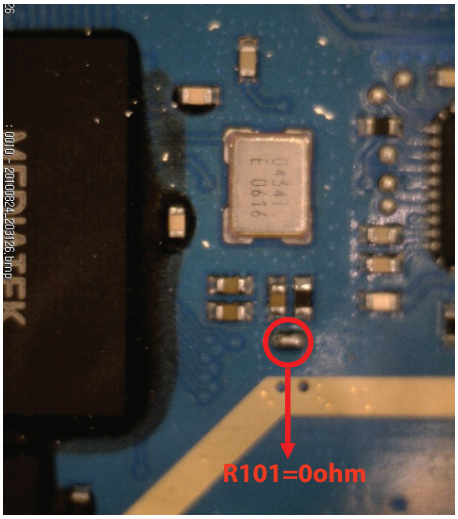


Figure 4.4.2

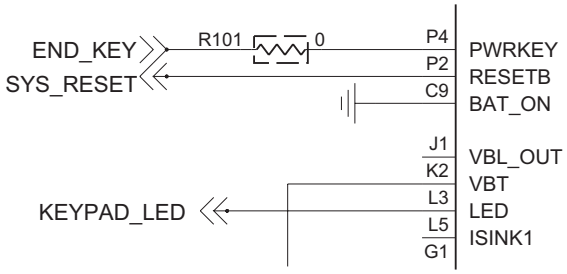


Figure 4.4.3 Remote power on

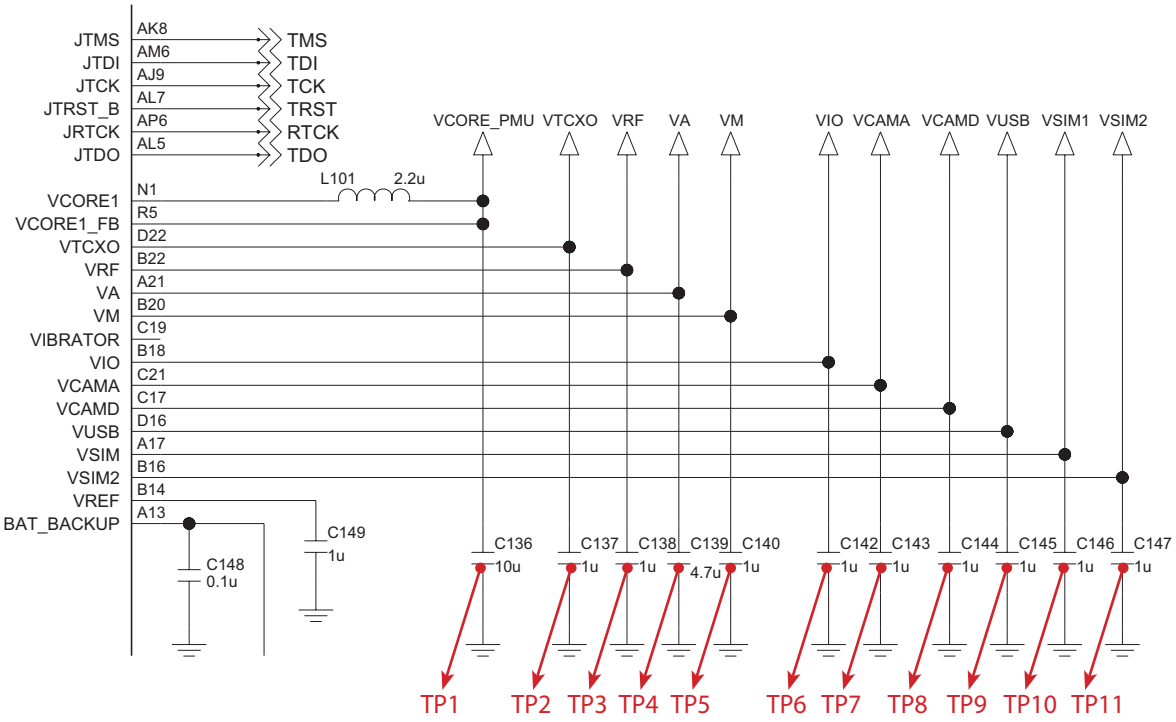
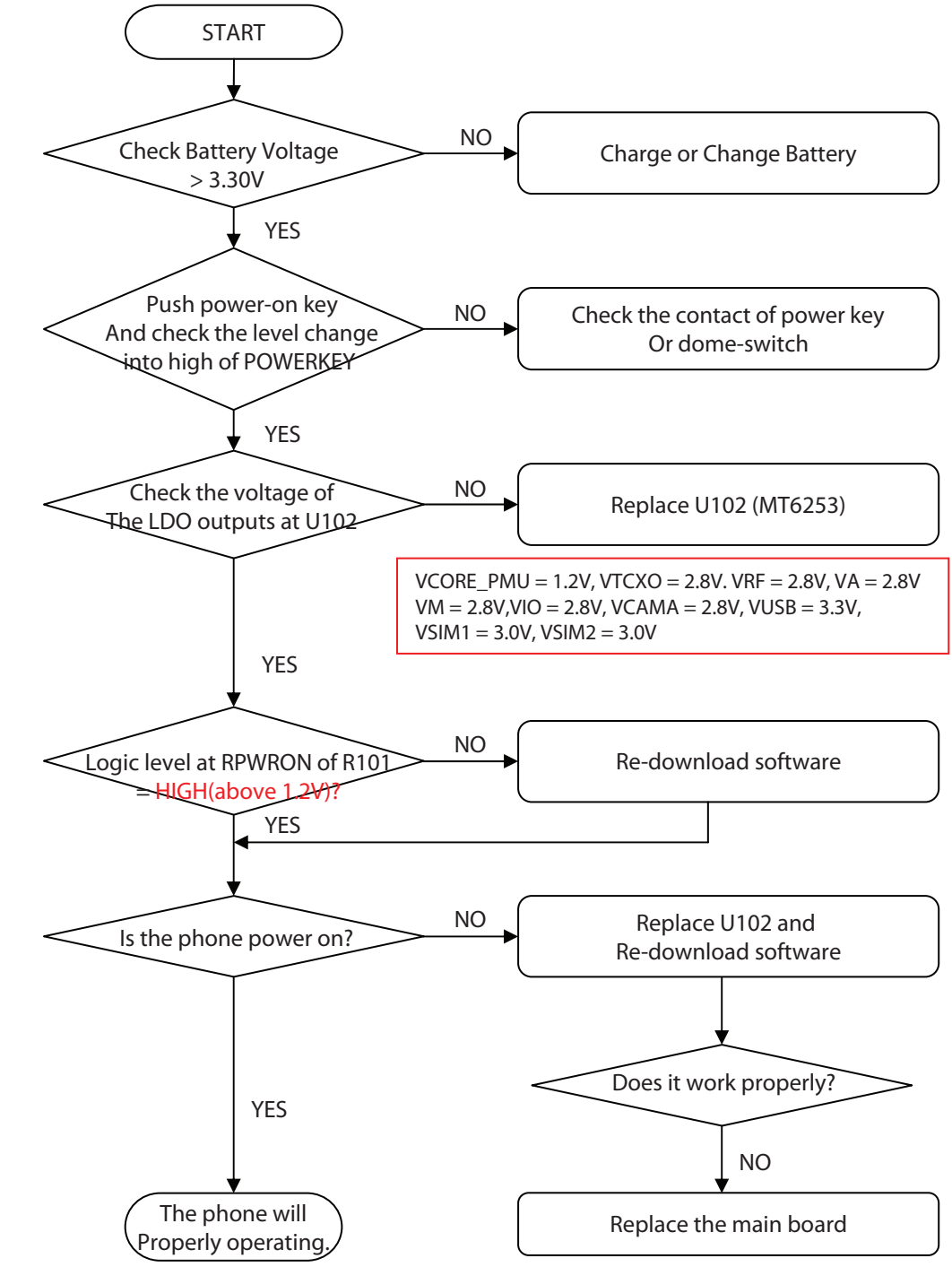


Figure 4.4.4 Power Block of LG-A165

CHECKING FLOW



4.5 Charging Trouble

TEST POINT

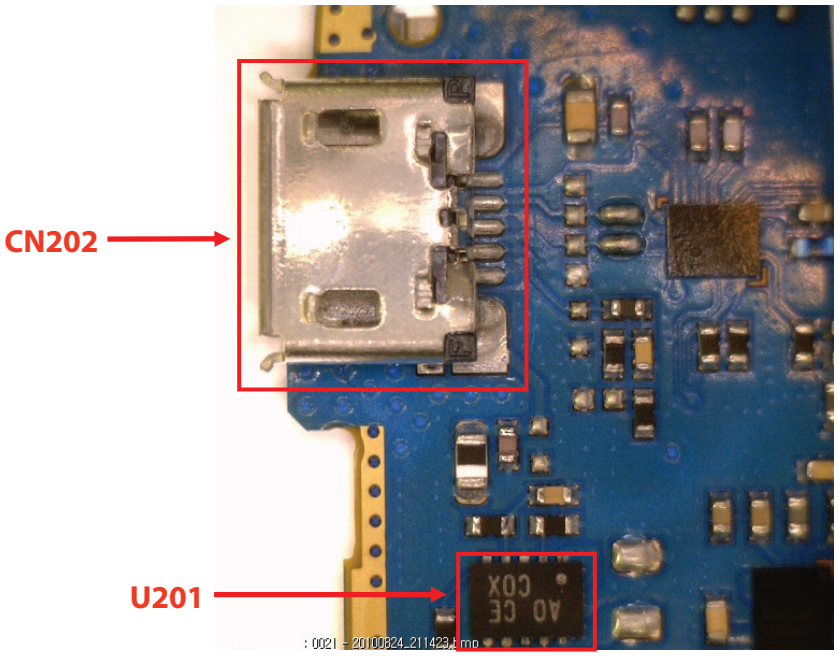
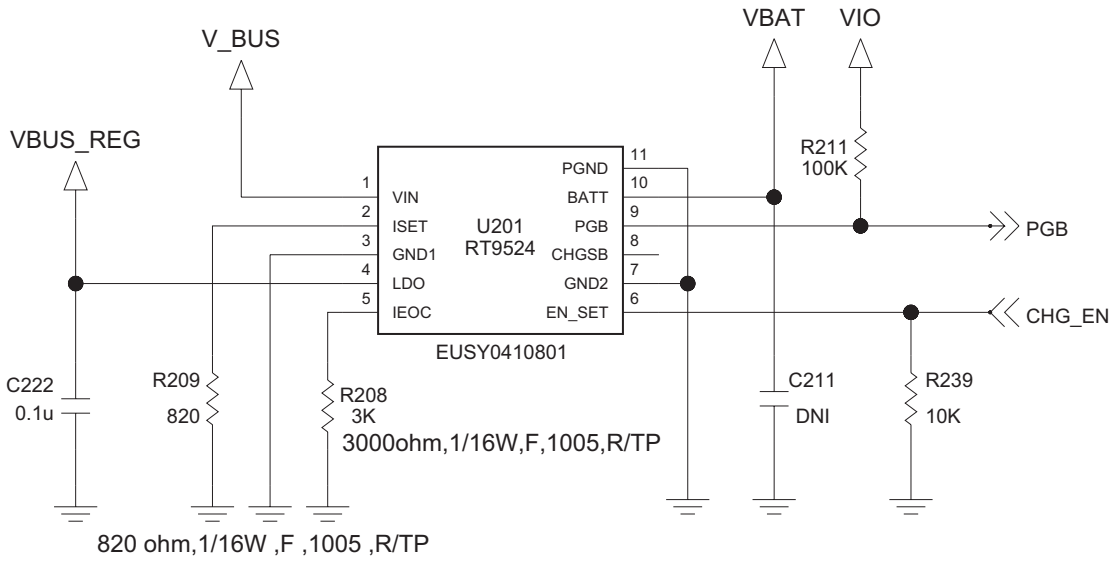
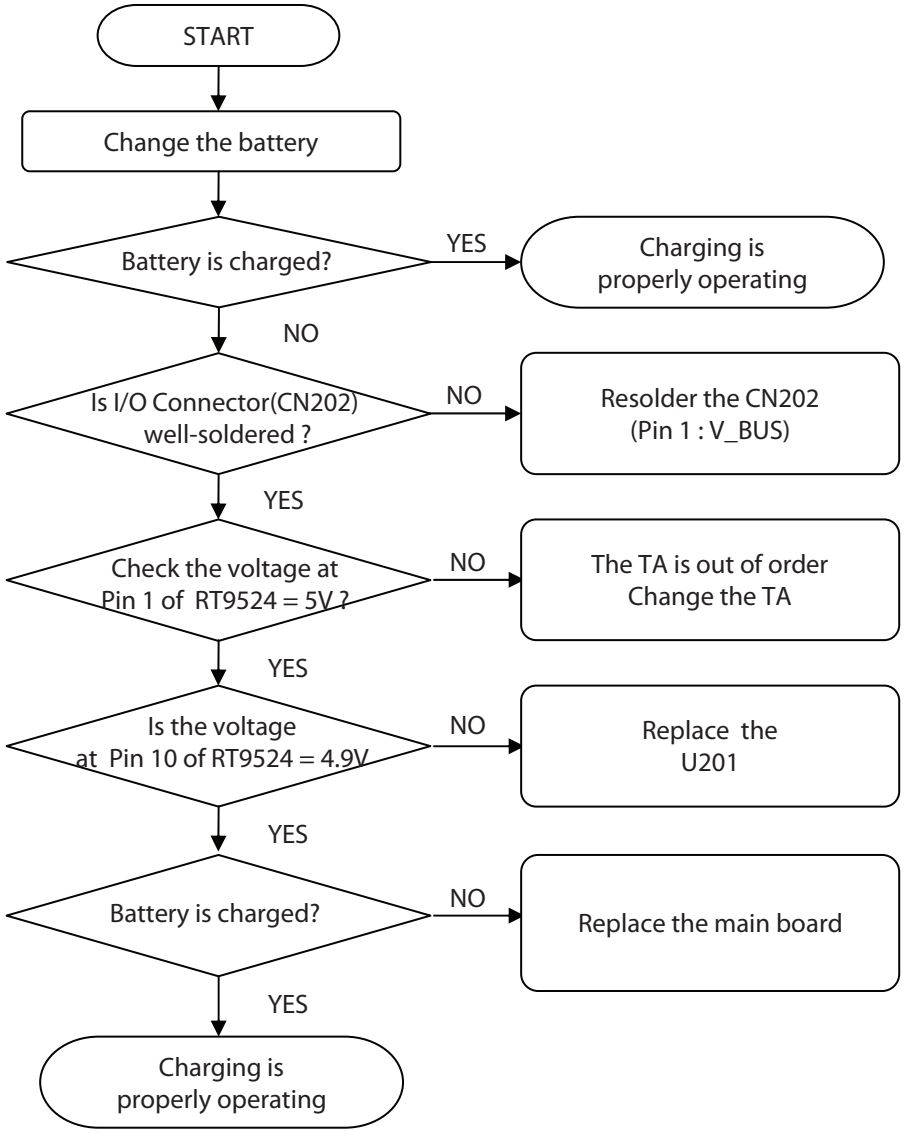


Figure 4.5.1

CIRCUIT



CHECKING FLOW



4.6 Vibrator Trouble

TEST POINT

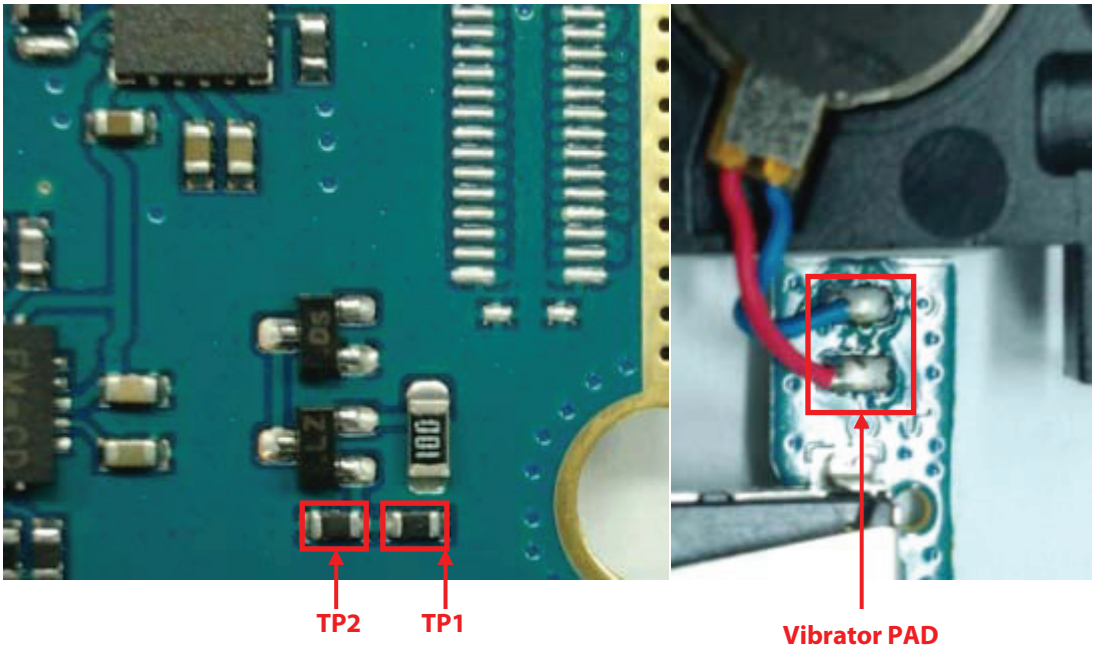
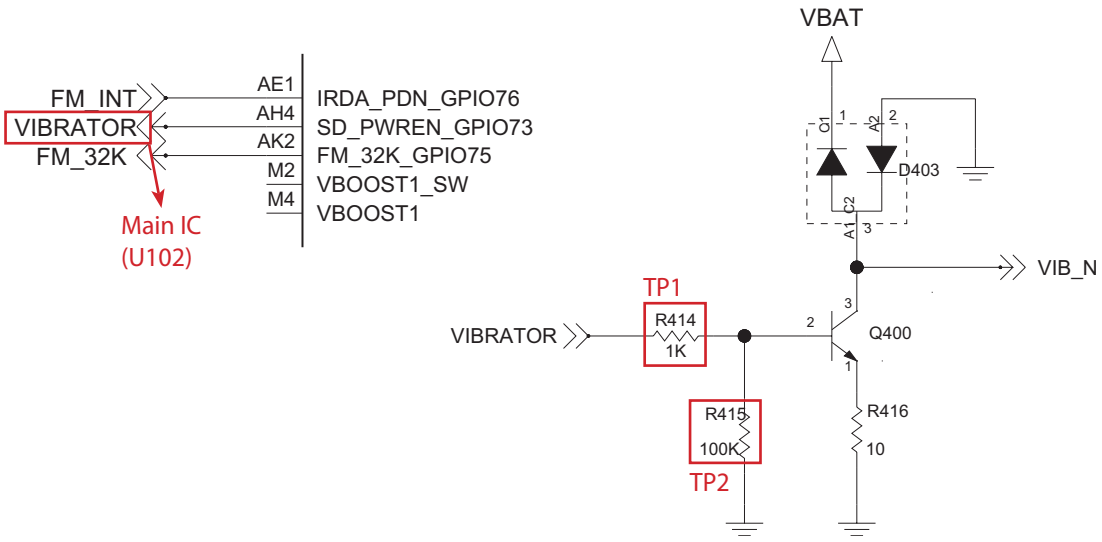


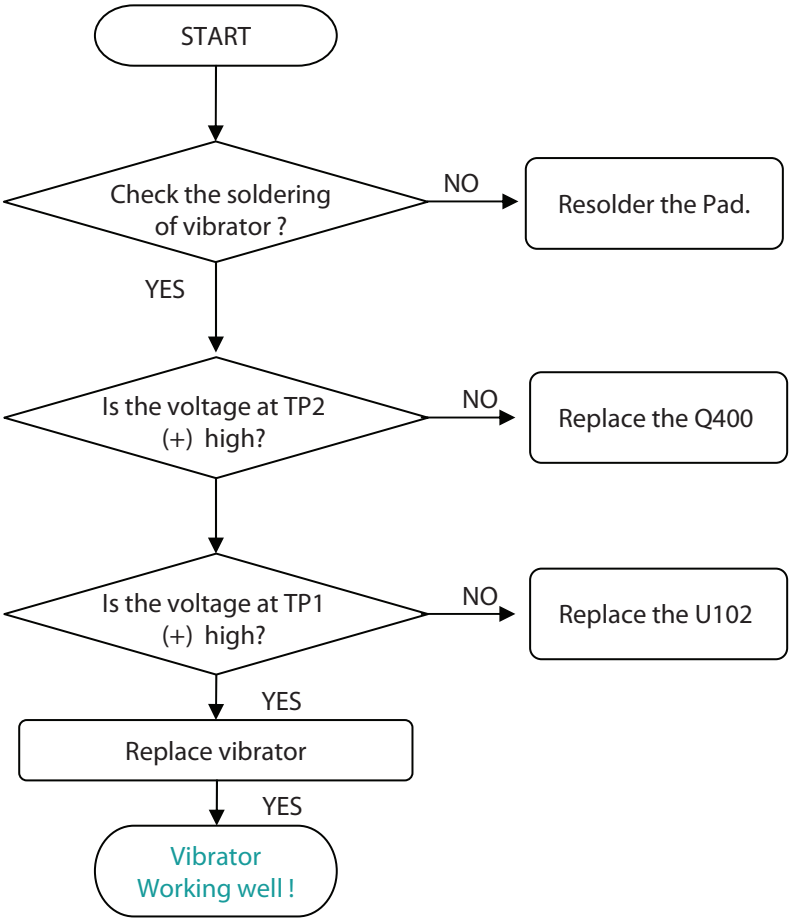
Figure 4.6

CIRCUIT



CHECKING FLOW

SETTING : Enter the engineering mode, and set vibrator on at vibration of BB test menu



4.7 LCD Trouble

TEST POINT

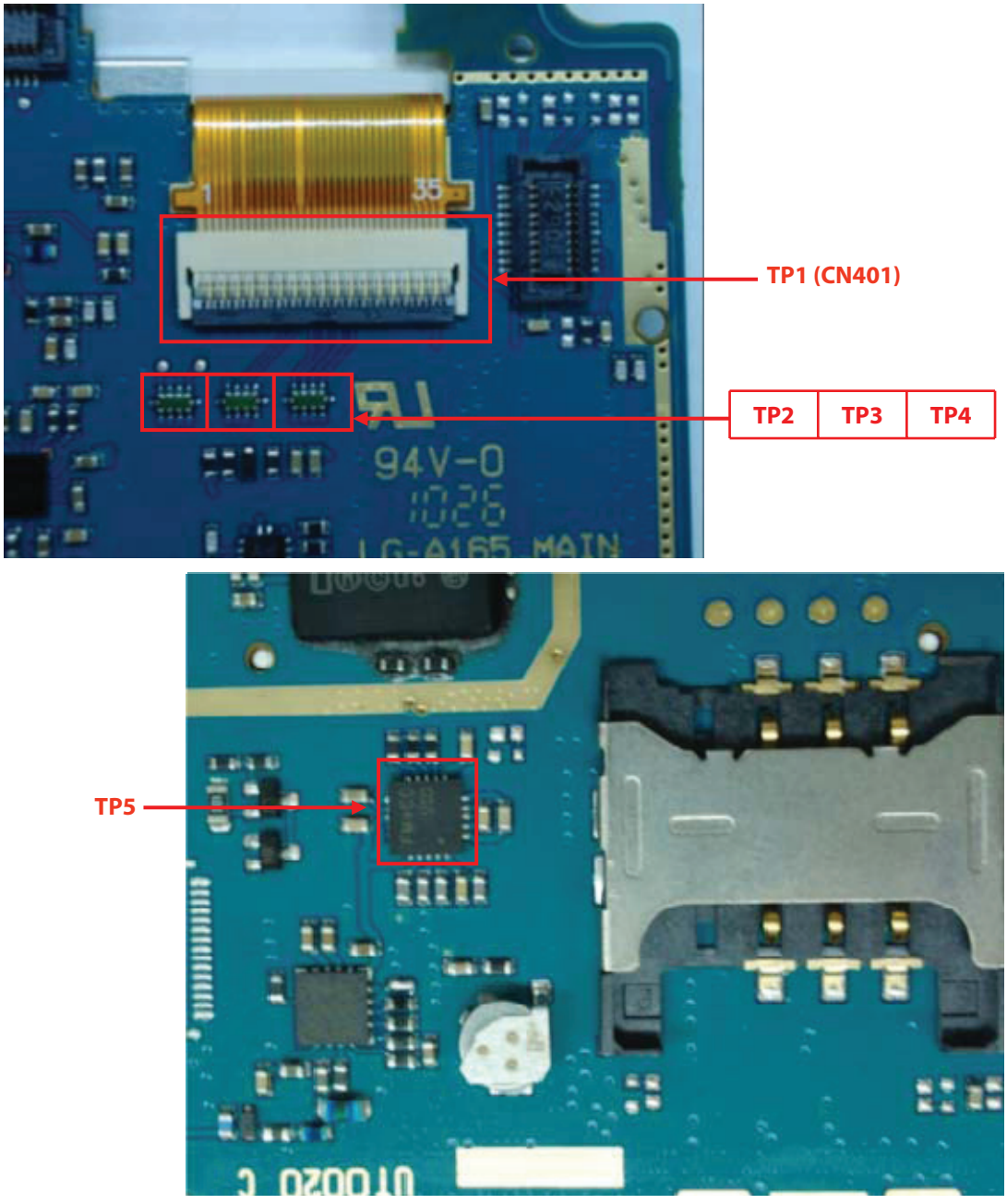
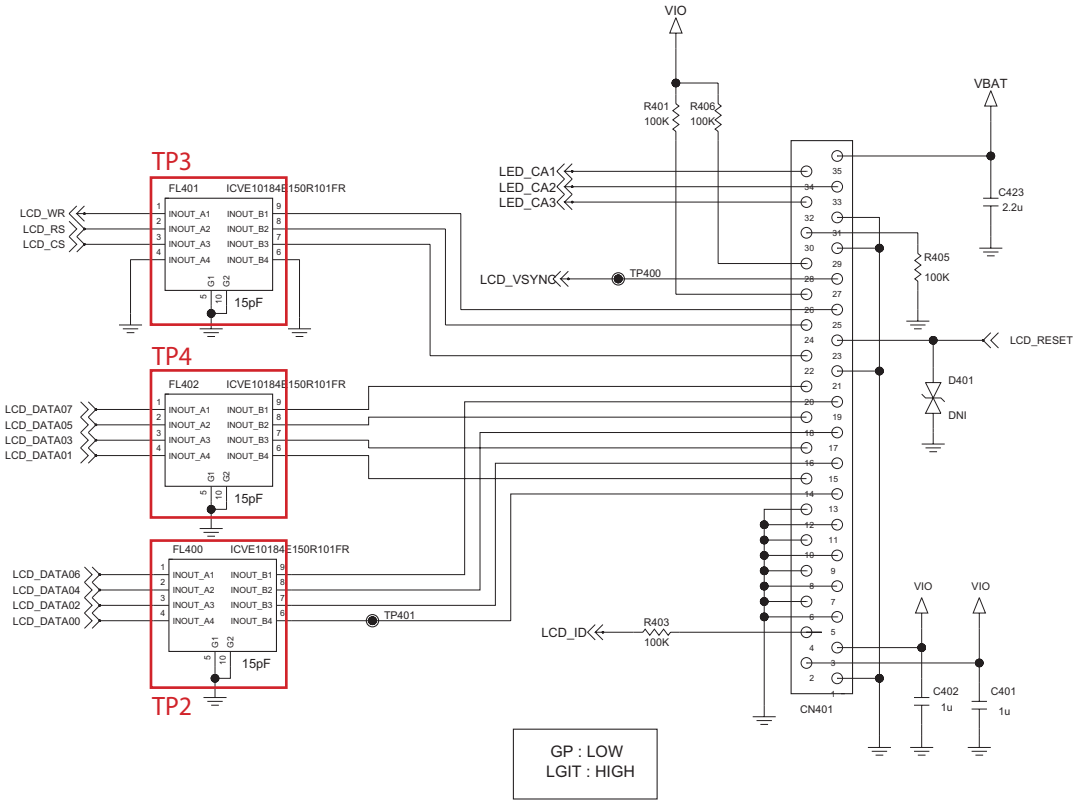
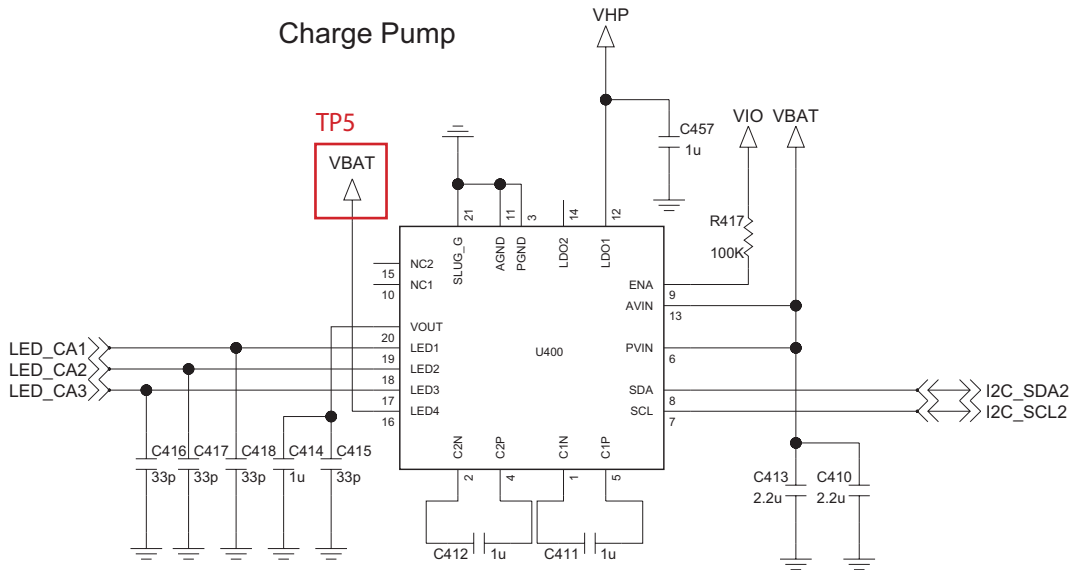


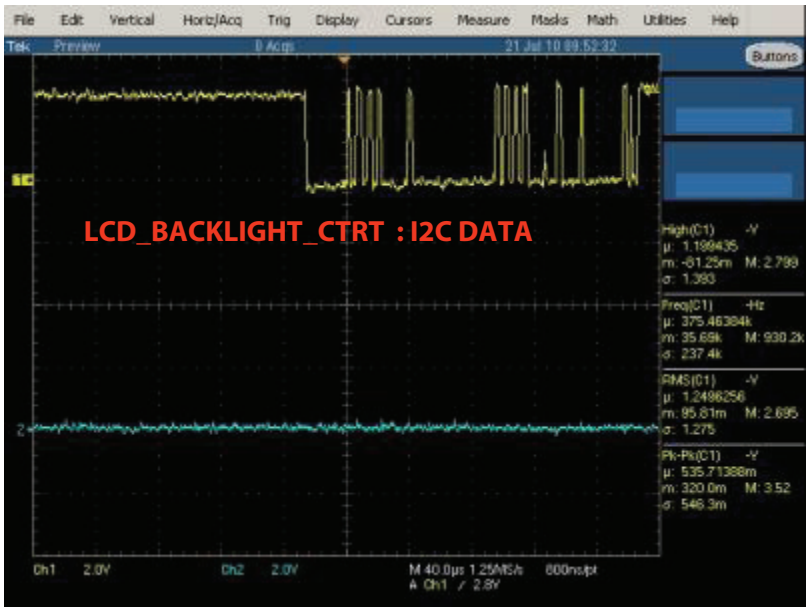
Figure 4.7.1

CIRCUIT





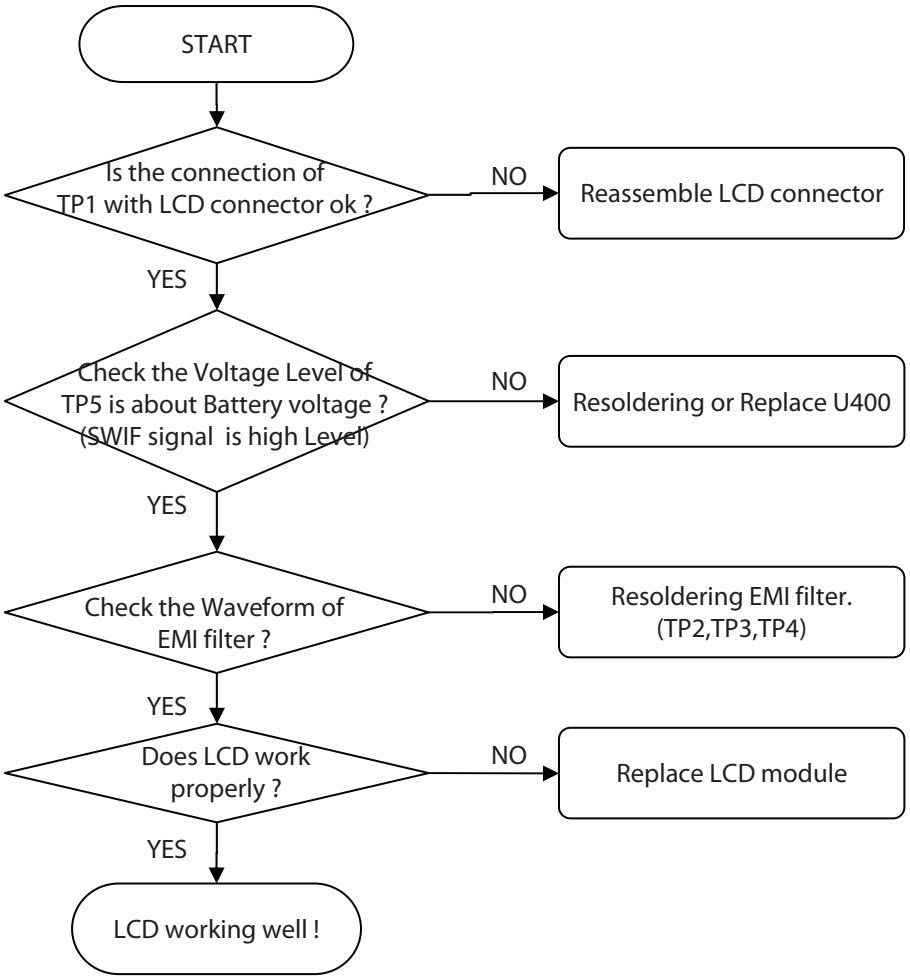
Waveform



Graph 4.7.1. LCD Backlight Control Signal Waveform

Graph 4.7.2. LCD Data Waveform

CHECKING FLOW



4.8 Camera Trouble

TEST POINT

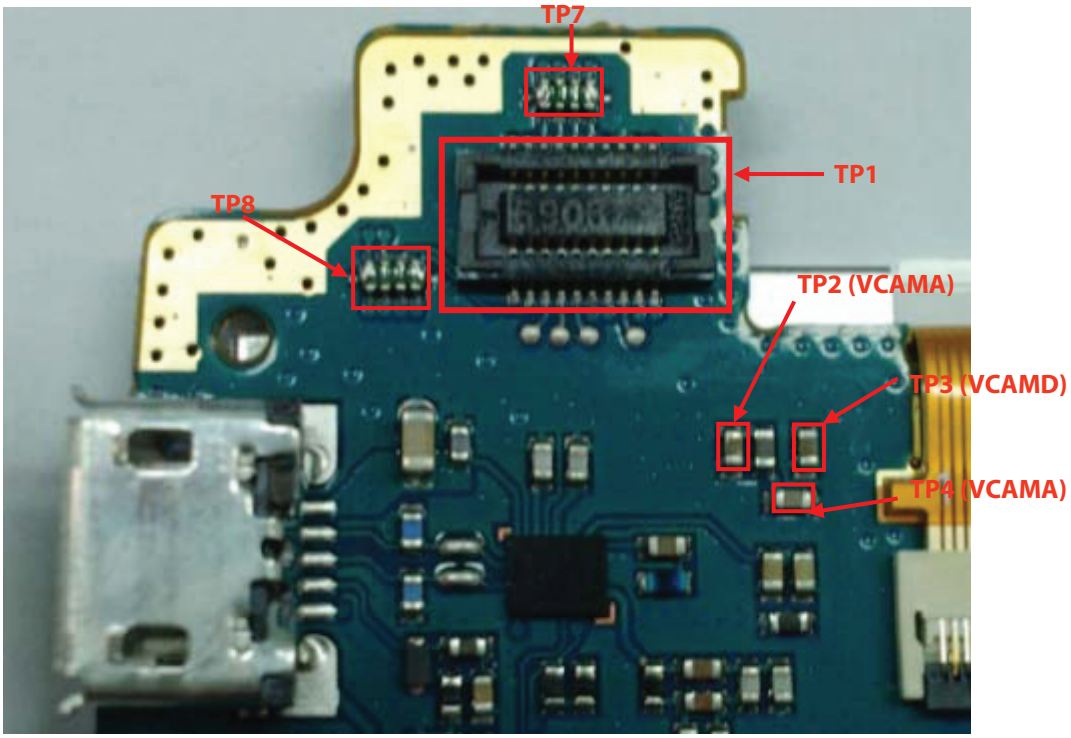


Figure 4.8.1

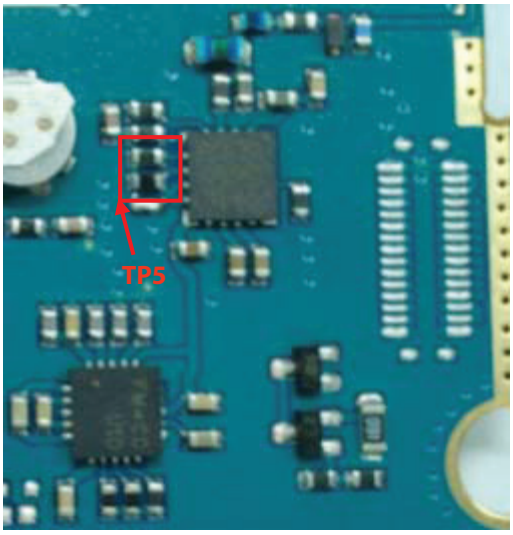
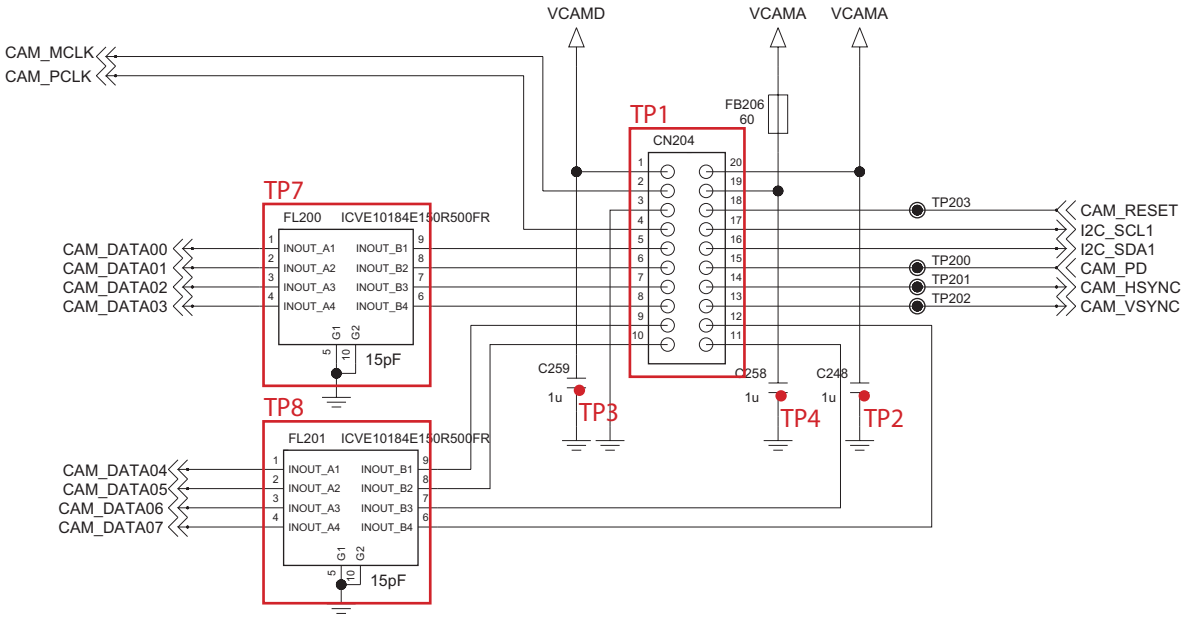
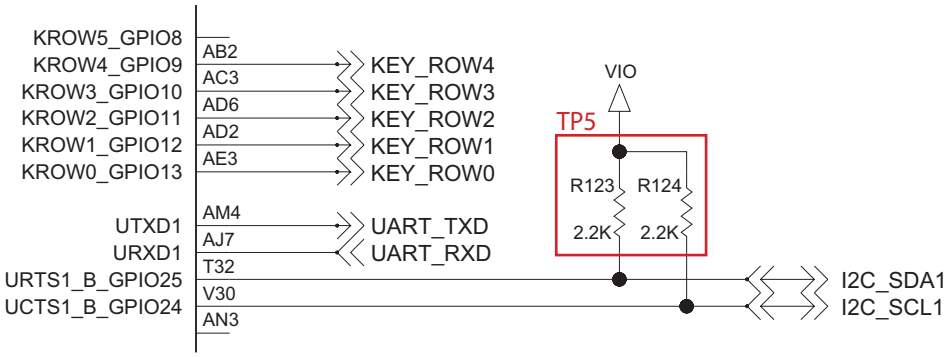


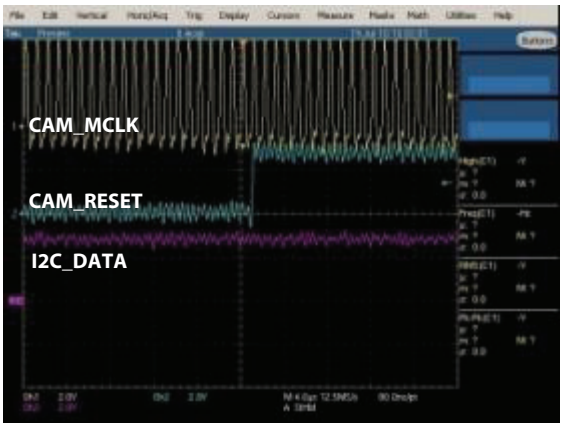
Figure 4.8.2

CIRCUIT



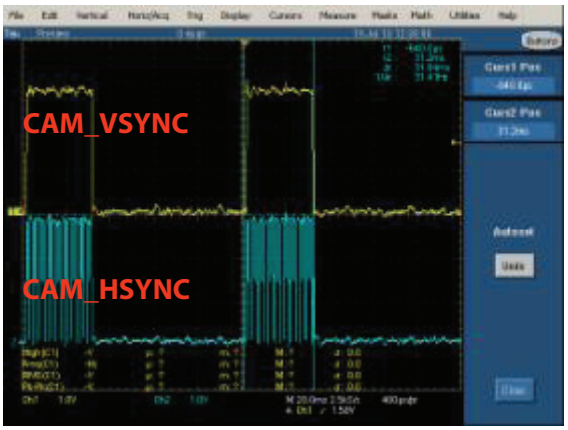


Waveform

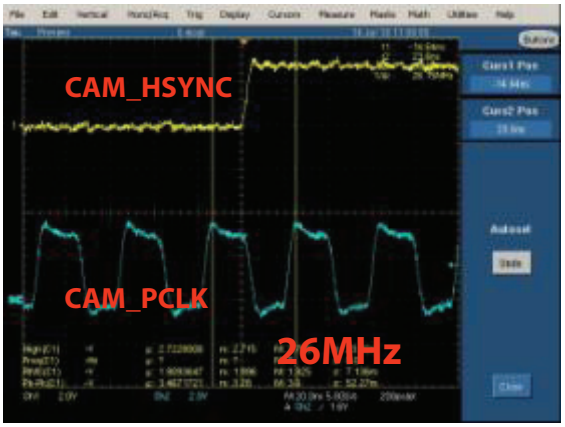


Graph 4.8.1. I2C Data Waveform

Graph 4.8.2. MCLK Waveform

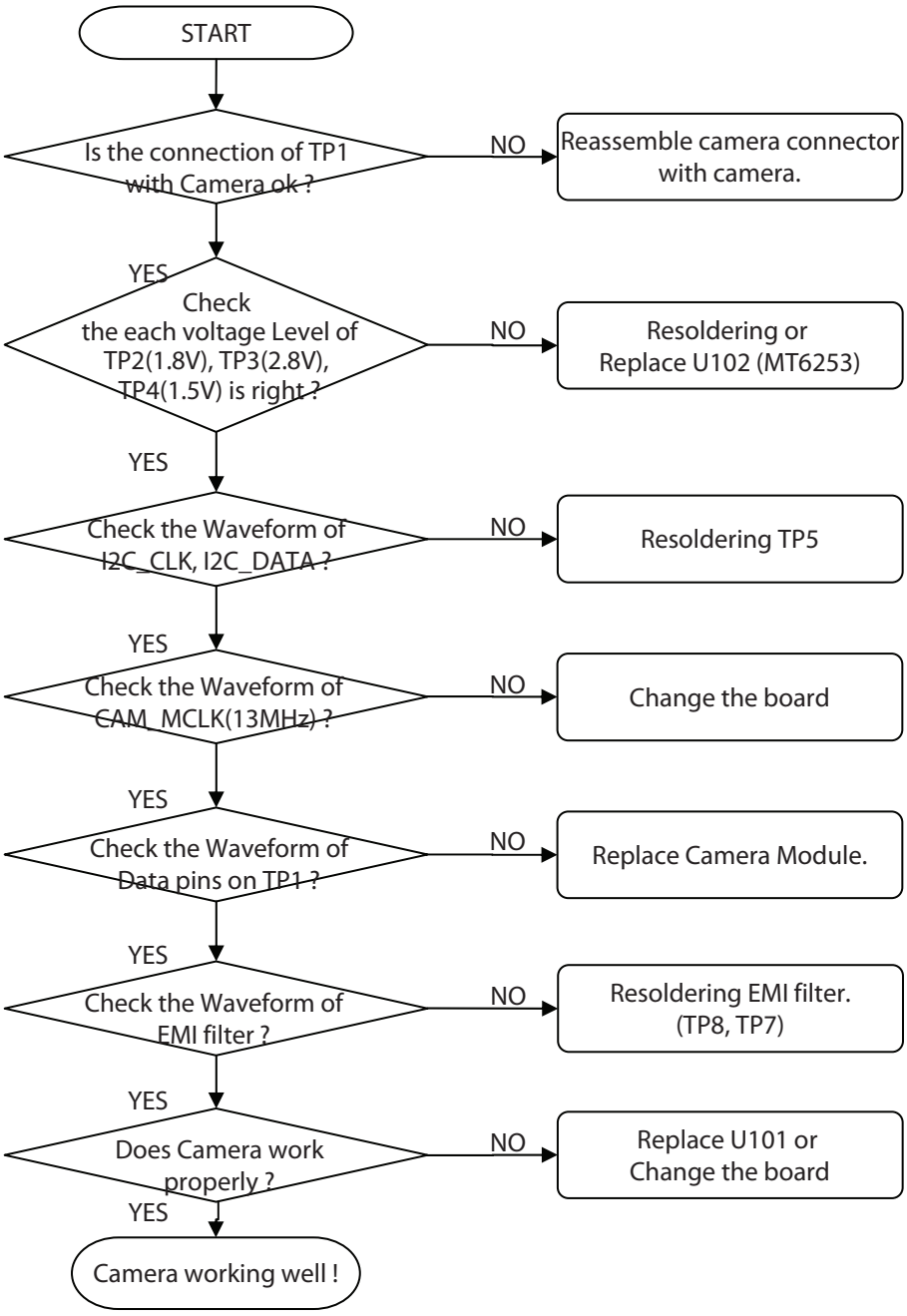


Graph 4.8.3.CAM_VSYNC vs. CAM_HSYNC Waveform



Graph 4.8.4.CAM_HSYNC vs. CAM_PCLK Waveform

CHECKING FLOW



4.9 Speaker Trouble

TEST POINT

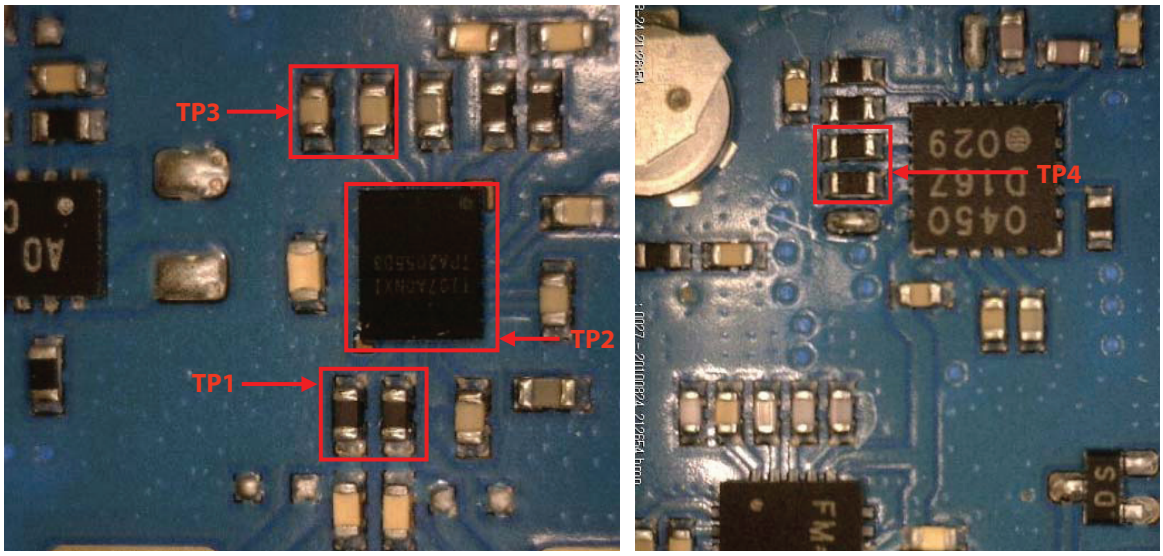
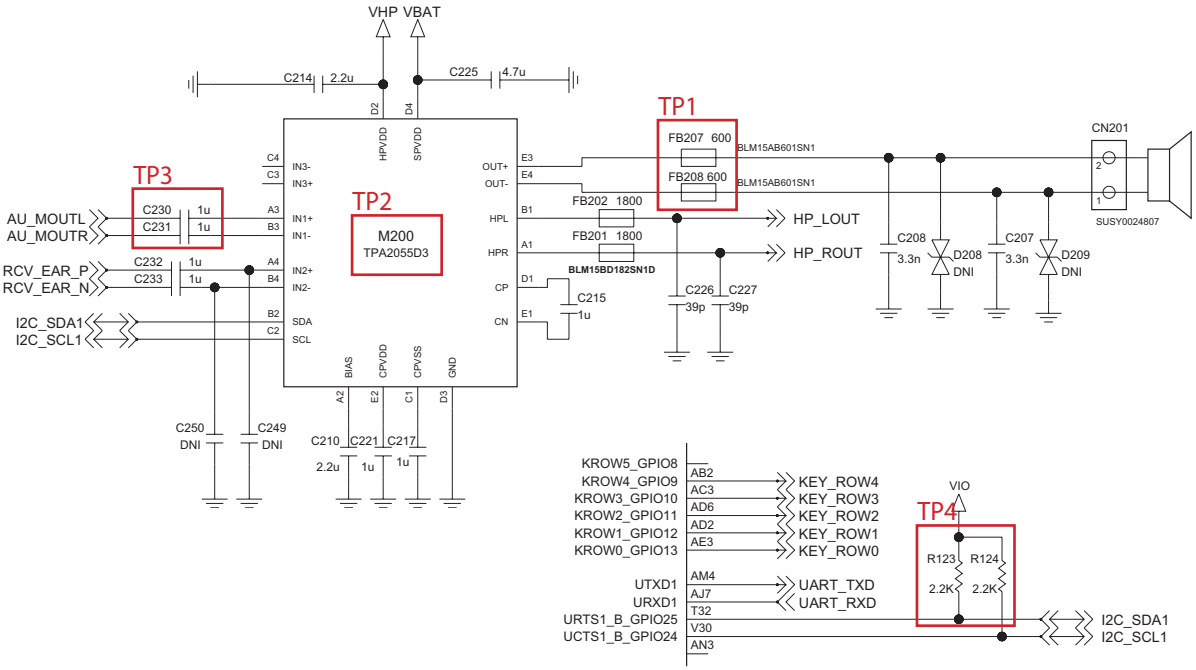
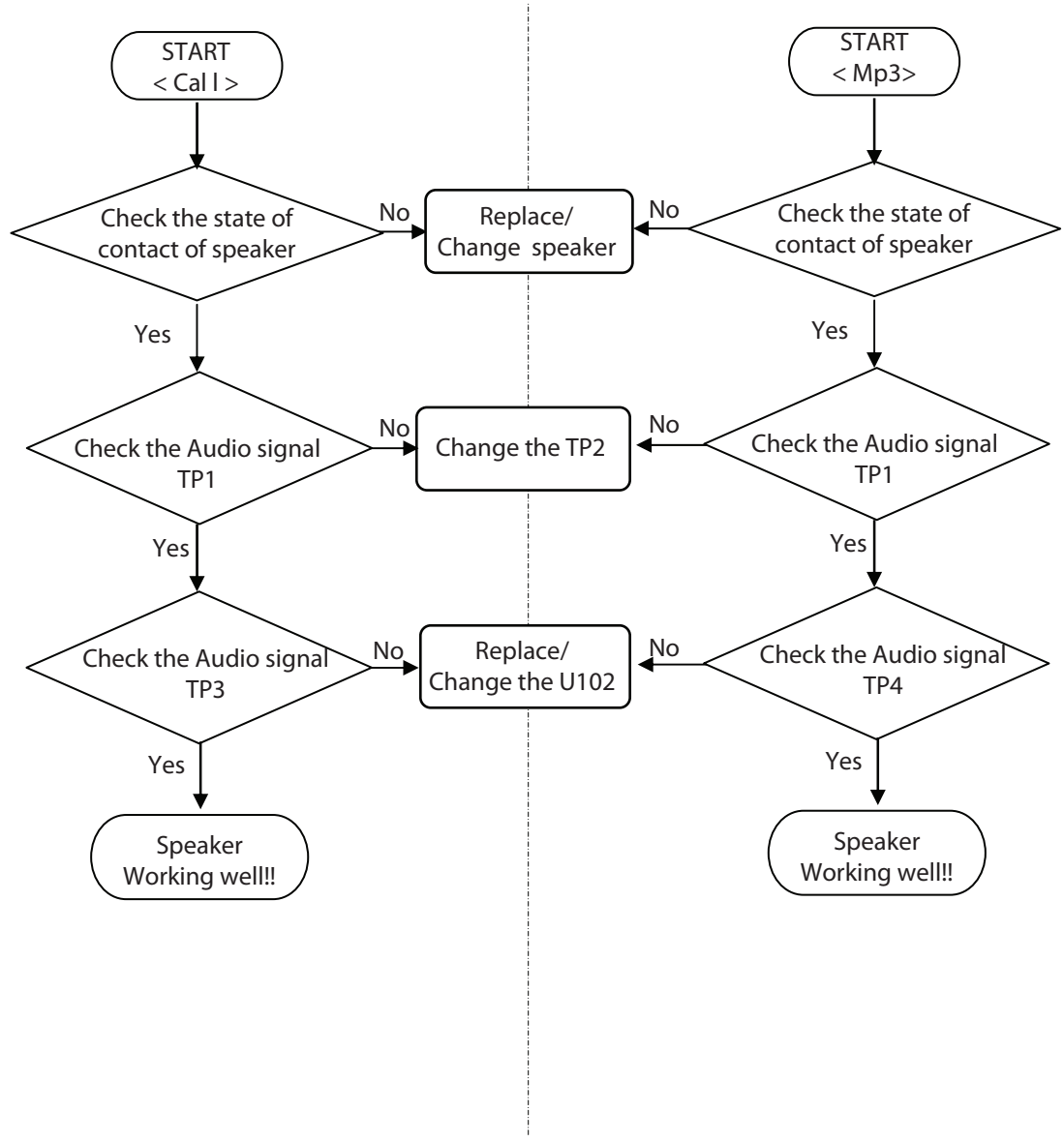


Figure 4.9.1

CIRCUIT



CHECKING FLOW



4.10 Earphone Trouble

TEST POINT

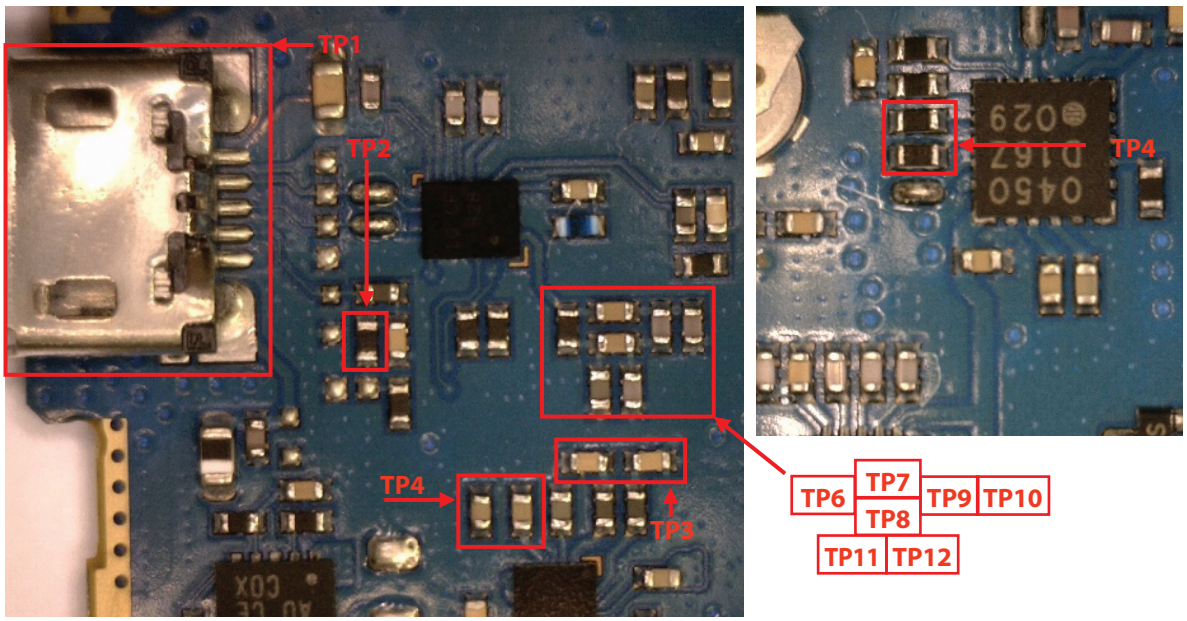
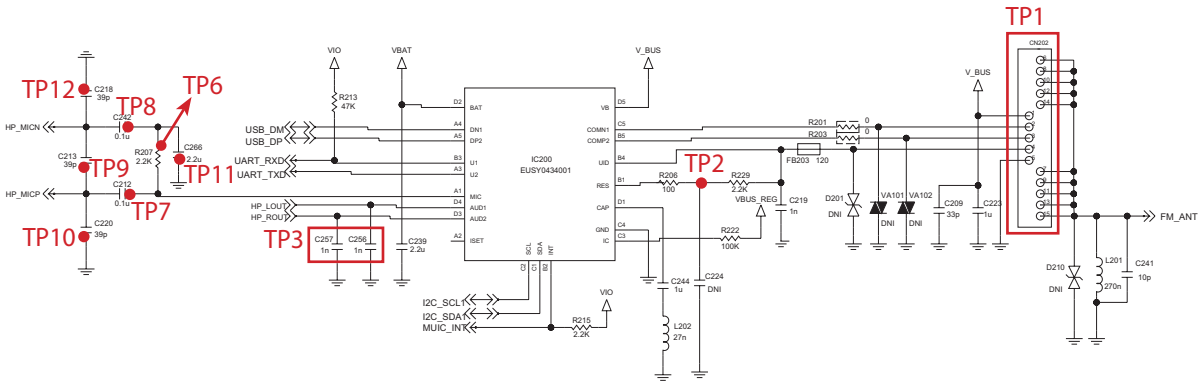
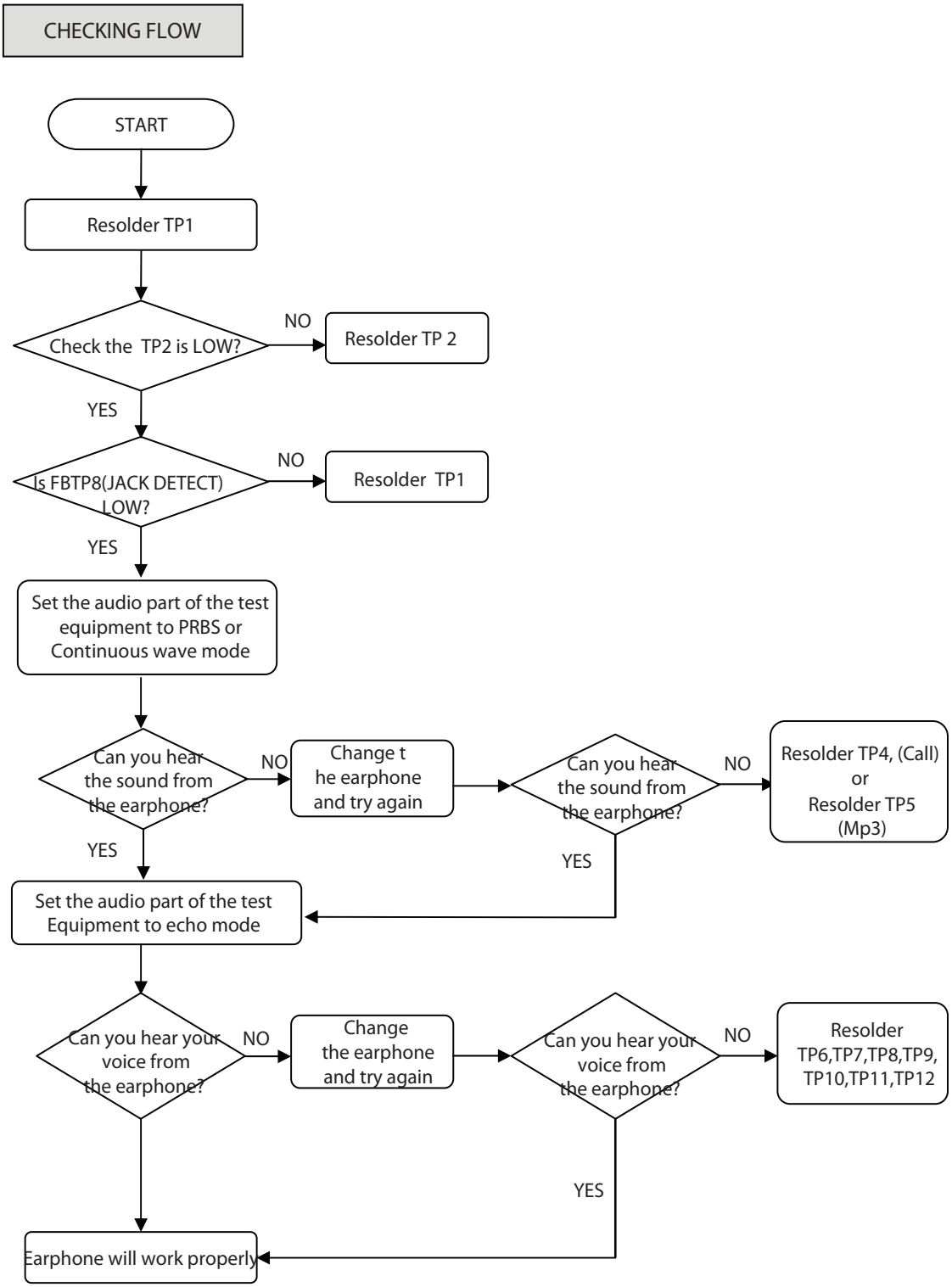


Figure 4.10.1

CIRCUIT





4.11 Receiver Trouble

TEST POINT

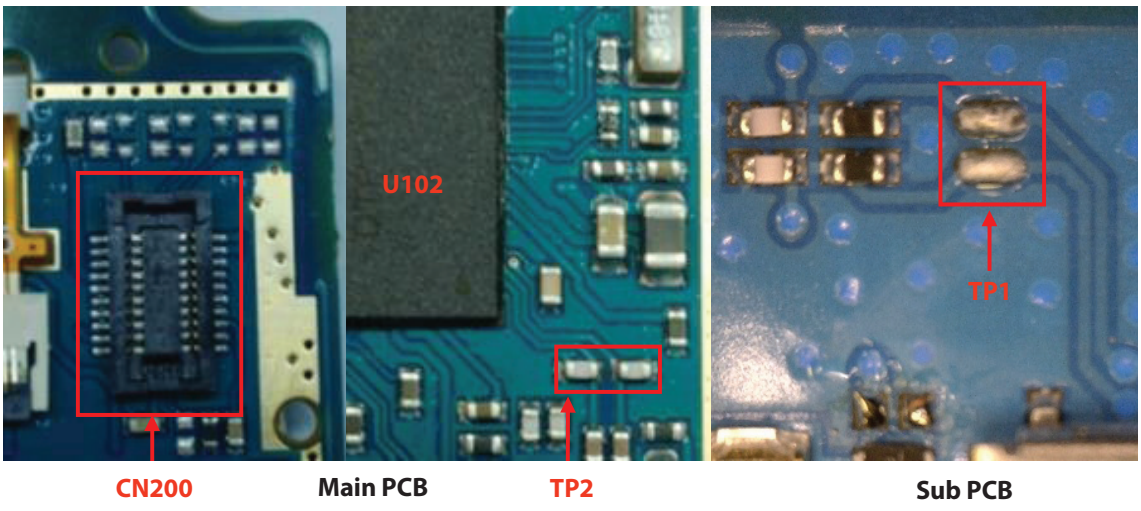
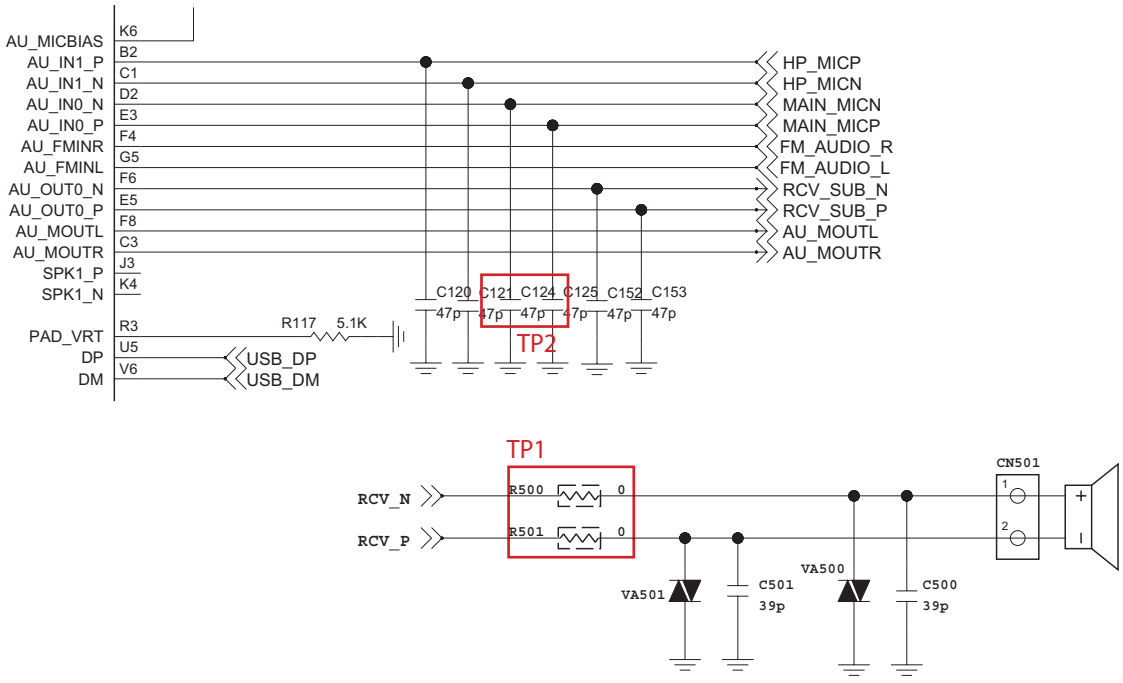


Figure 4.11.1

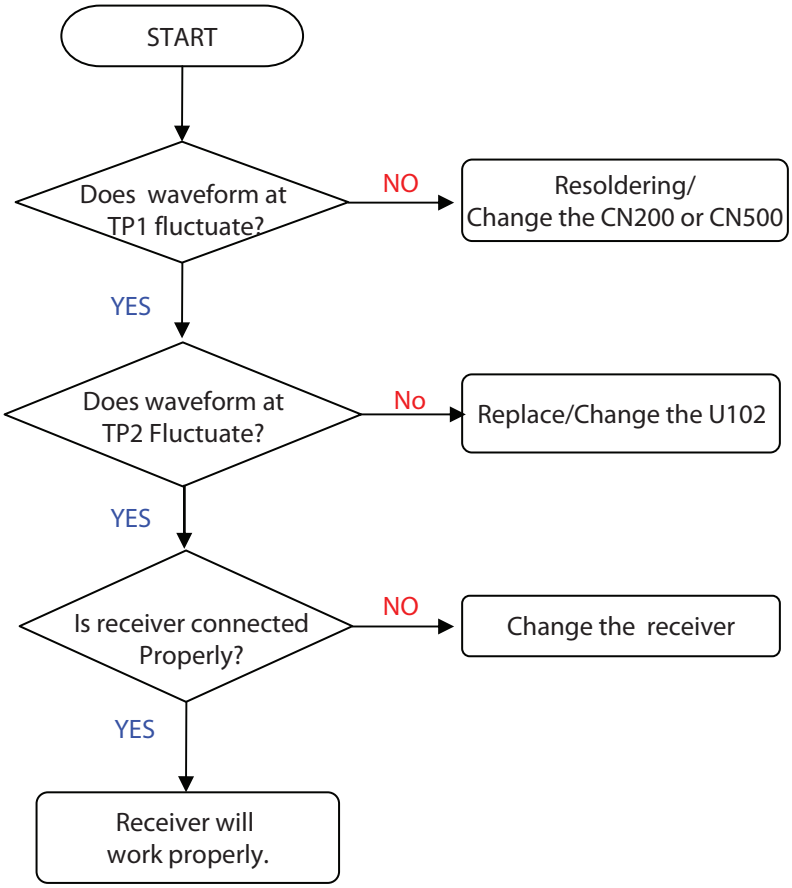
CIRCUIT



CHECKING FLOW

SETTING : After initialize Agilent 8960, Test EGSM900, DCS mode (or GSM850, PCS mode)

Set the property of audio as PRBS or continuous wave. Set the receiving volume of mobile as Max.



4.12 Microphone Trouble

TEST POINT

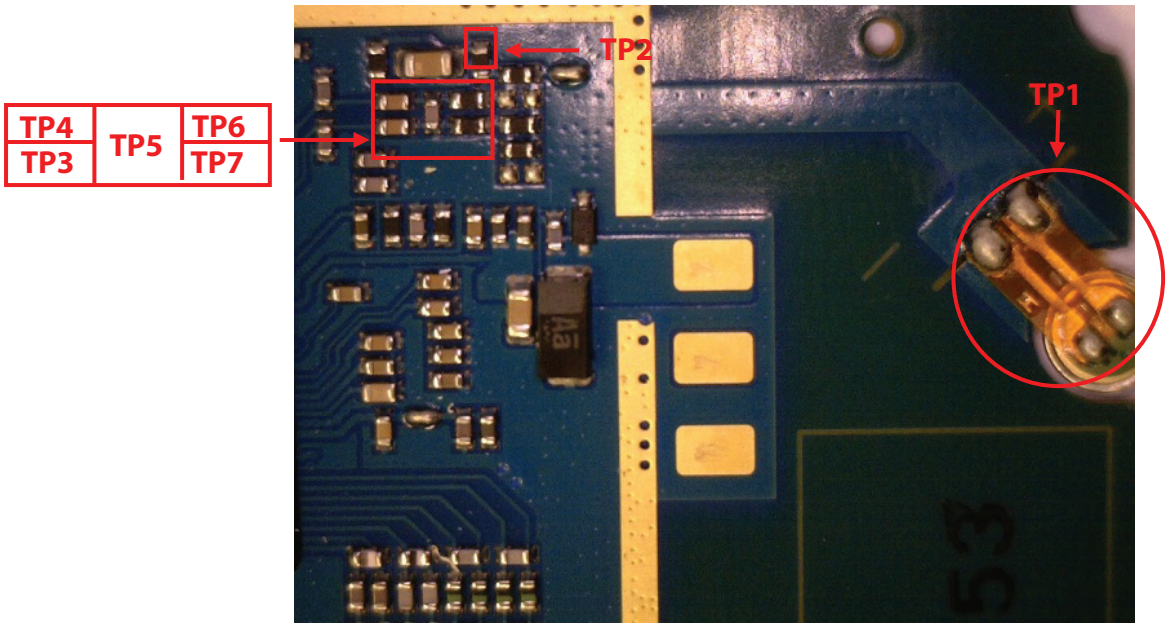
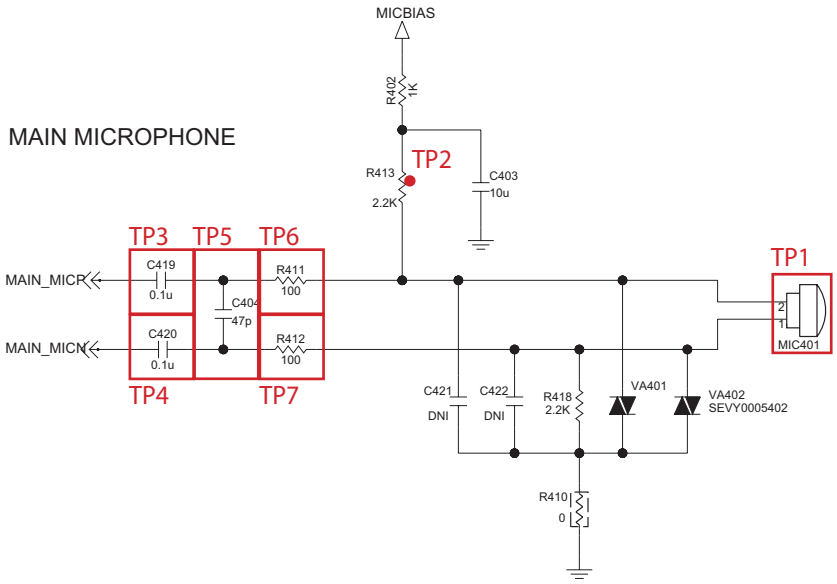


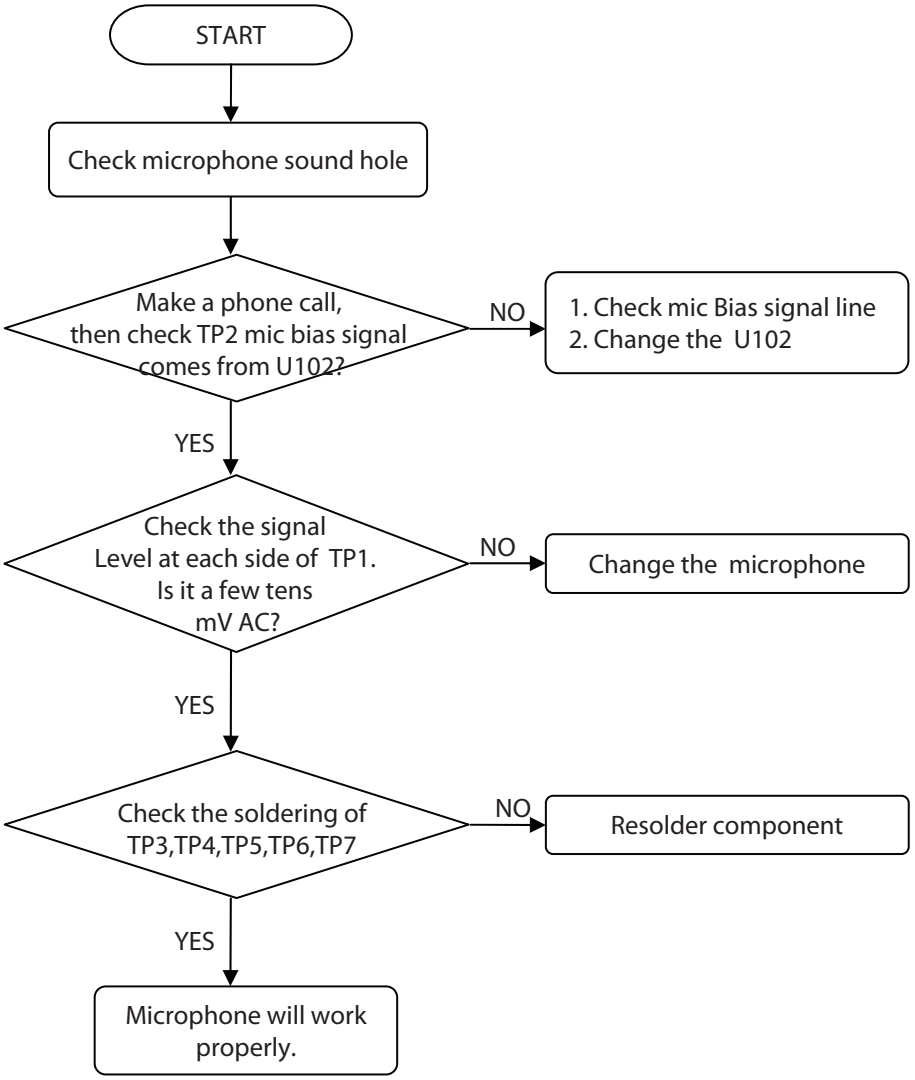
Figure 4.12.1

CIRCUIT



CHECKING FLOW

SETTING : After initialize Agilent 8960, Test EGSM900, DCS mode (or GSM850, PCS mode)



4.13 SIM1 Card Interface Trouble

TEST POINT

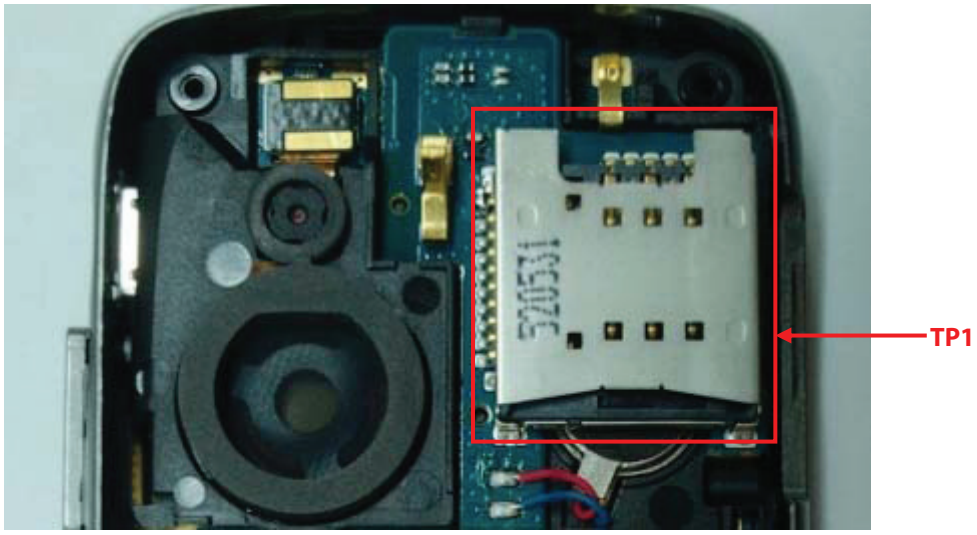
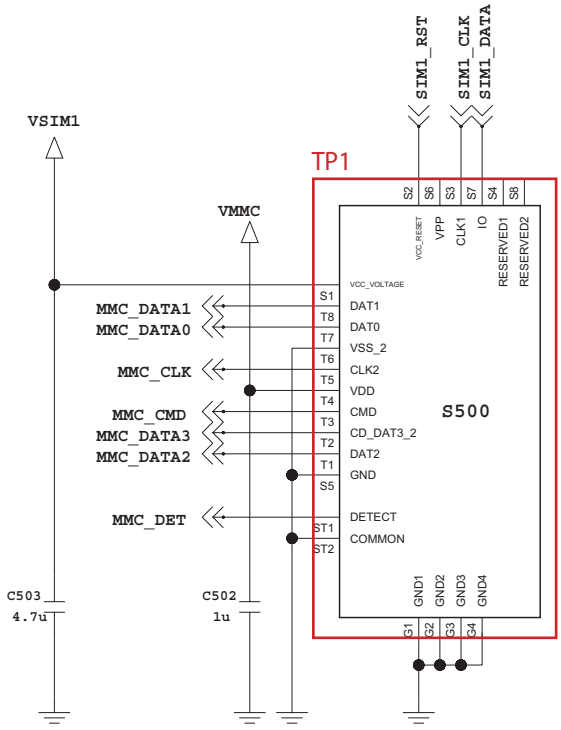
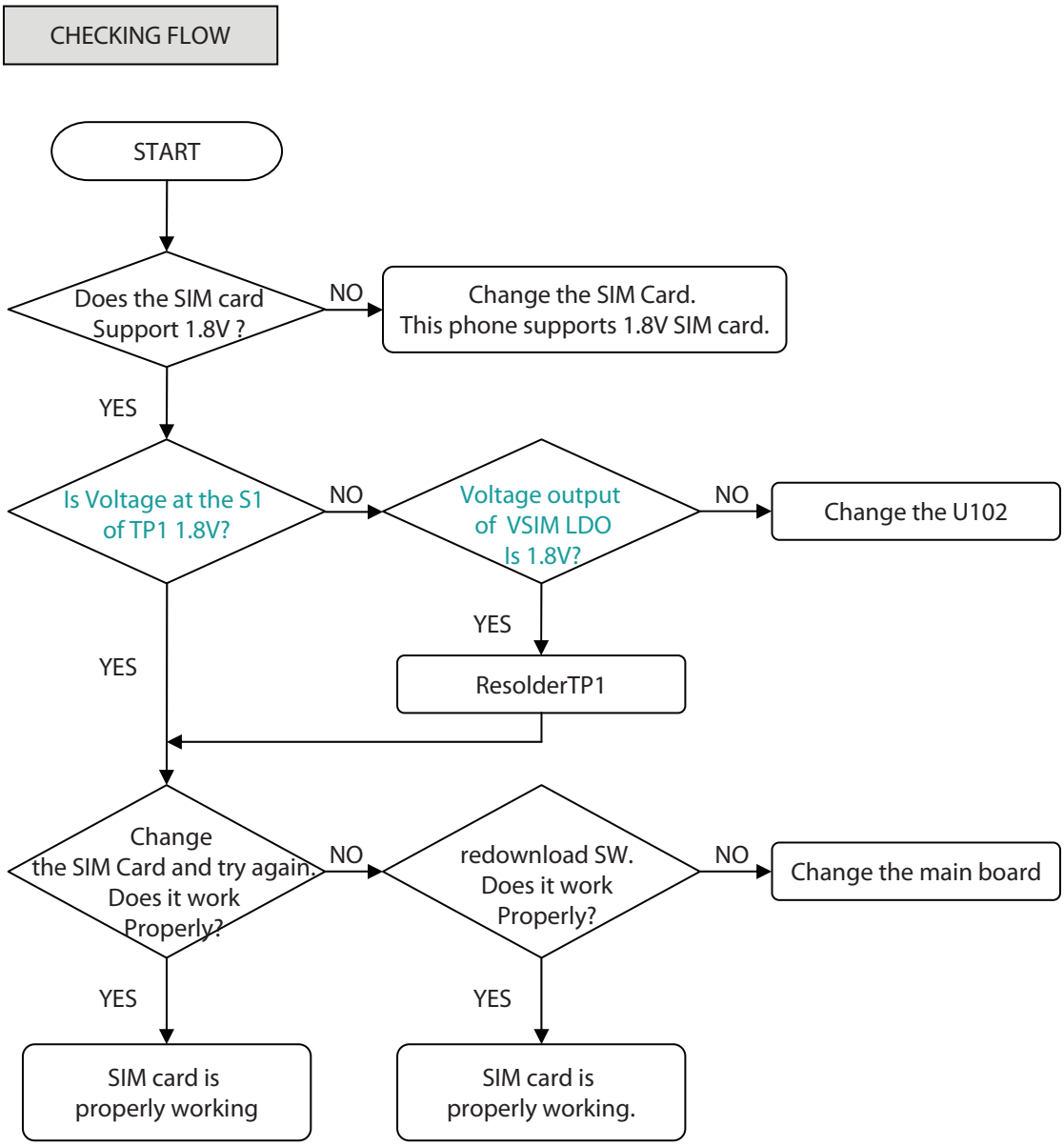


Figure 4.13.1

CIRCUIT





4.14 SIM2 Card Interface Trouble

TEST POINT

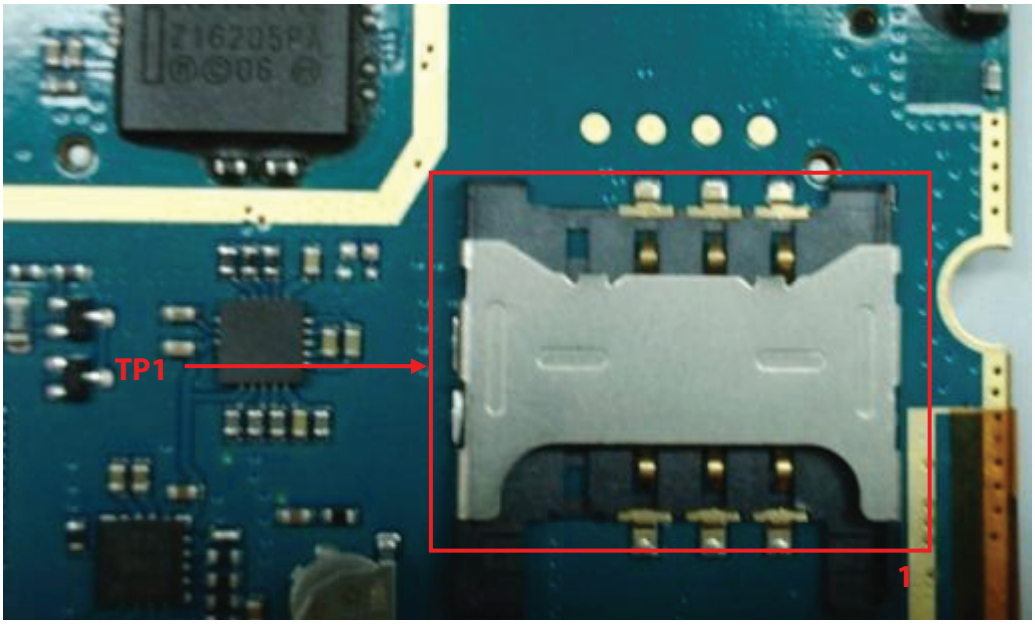
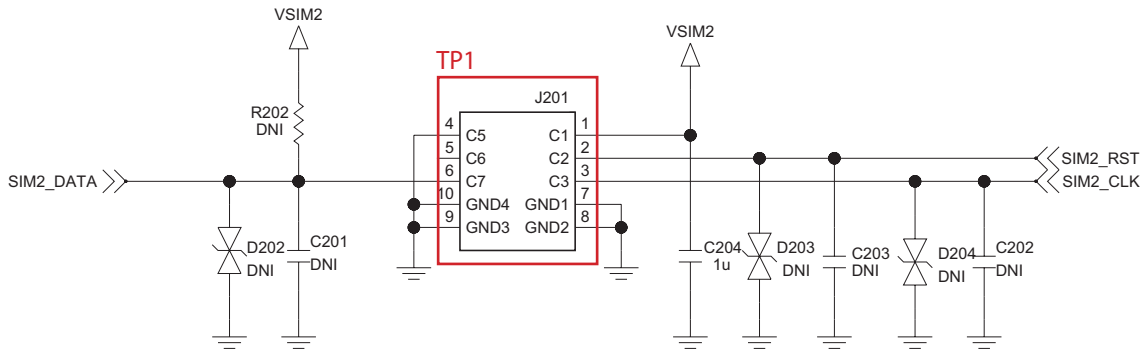
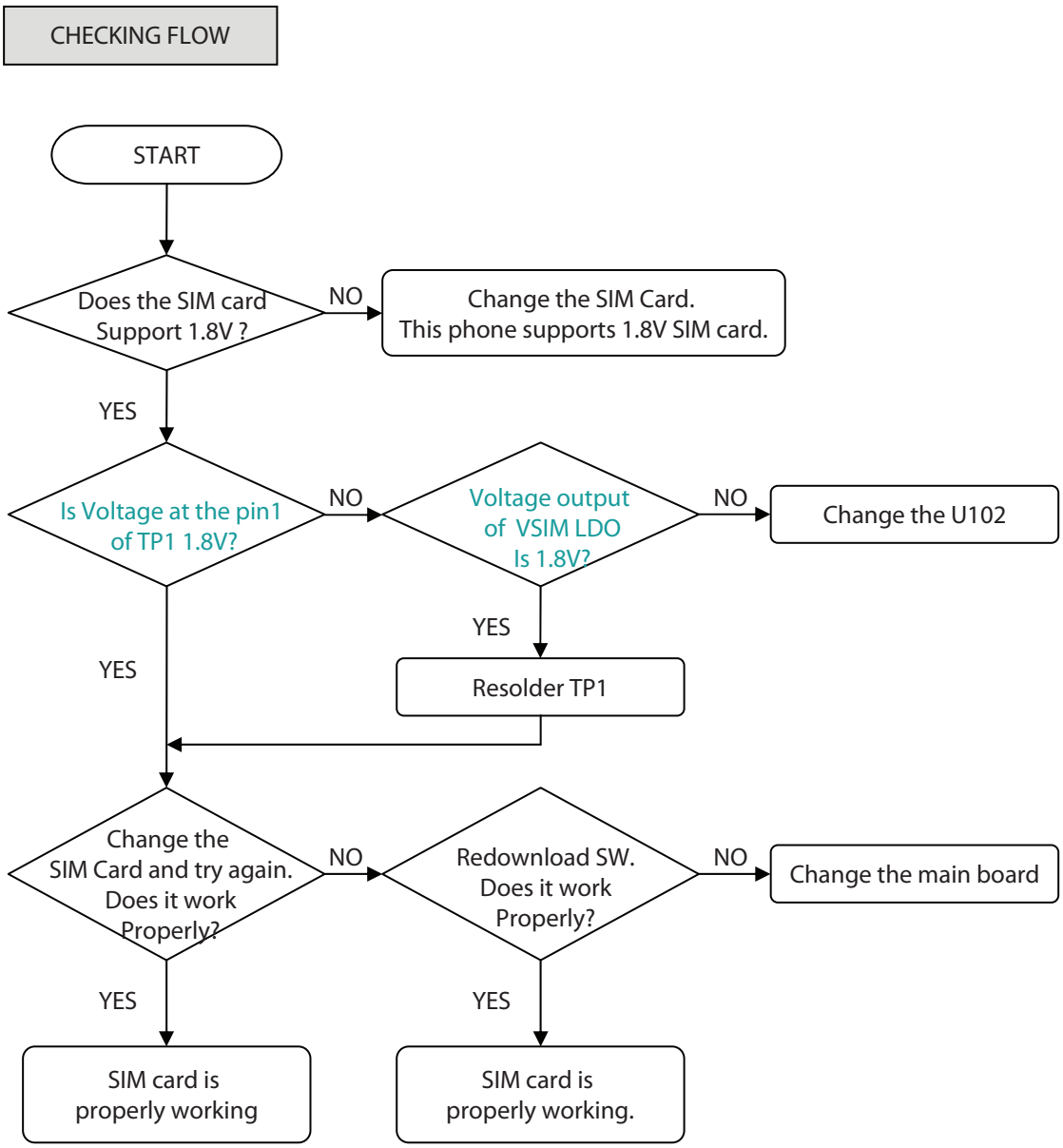


Figure 4.14.1

CIRCUIT





4.15 KEY backlight Trouble

TEST POINT

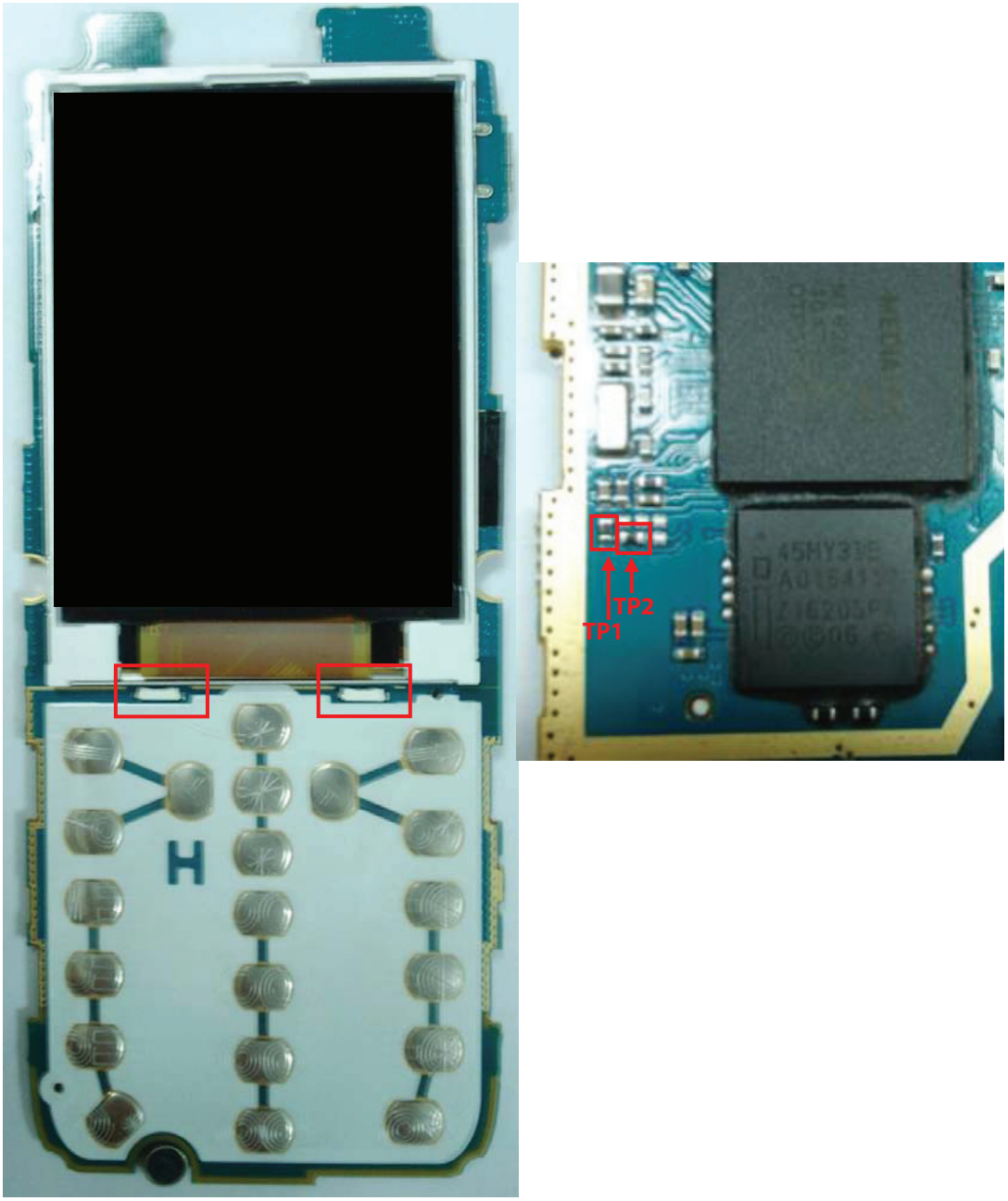
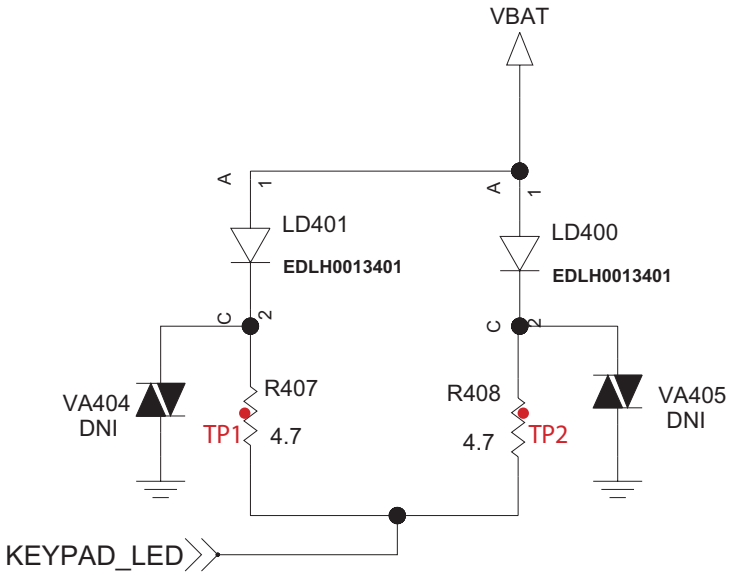
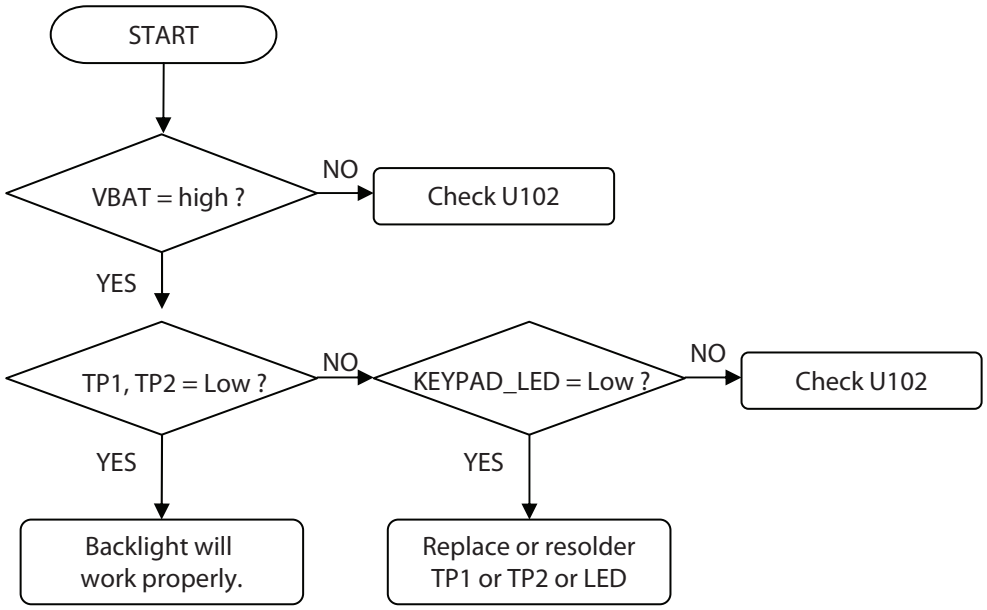


Figure 4.15.1

CIRCUIT



CHECKING FLOW



4.16 Micro SD Trouble

TEST POINT

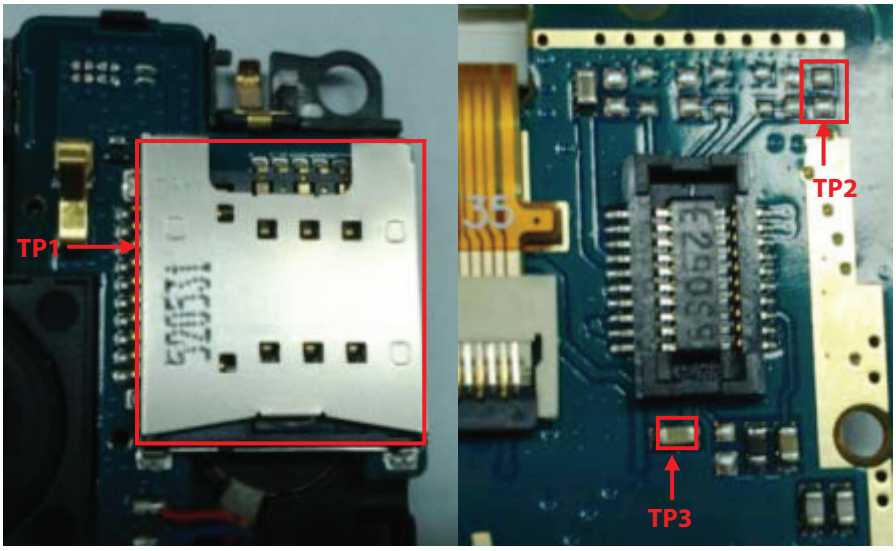
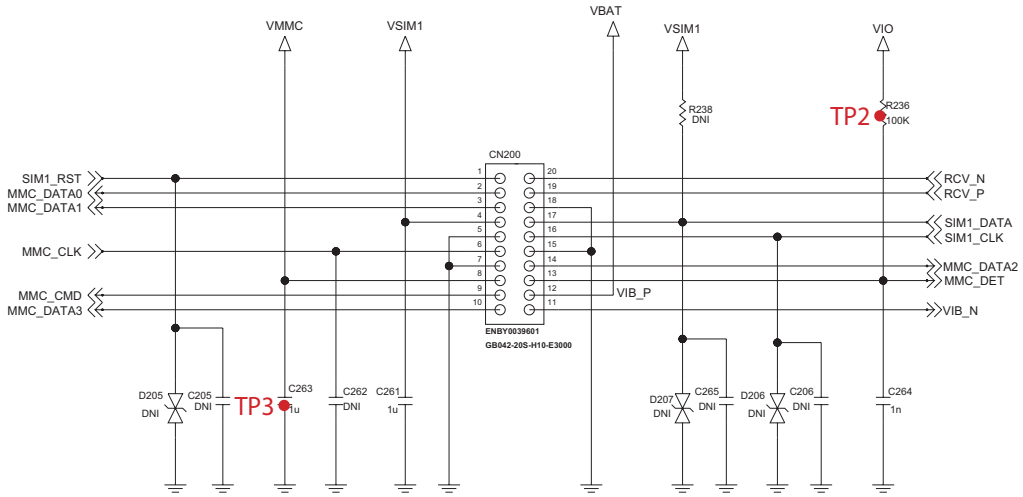
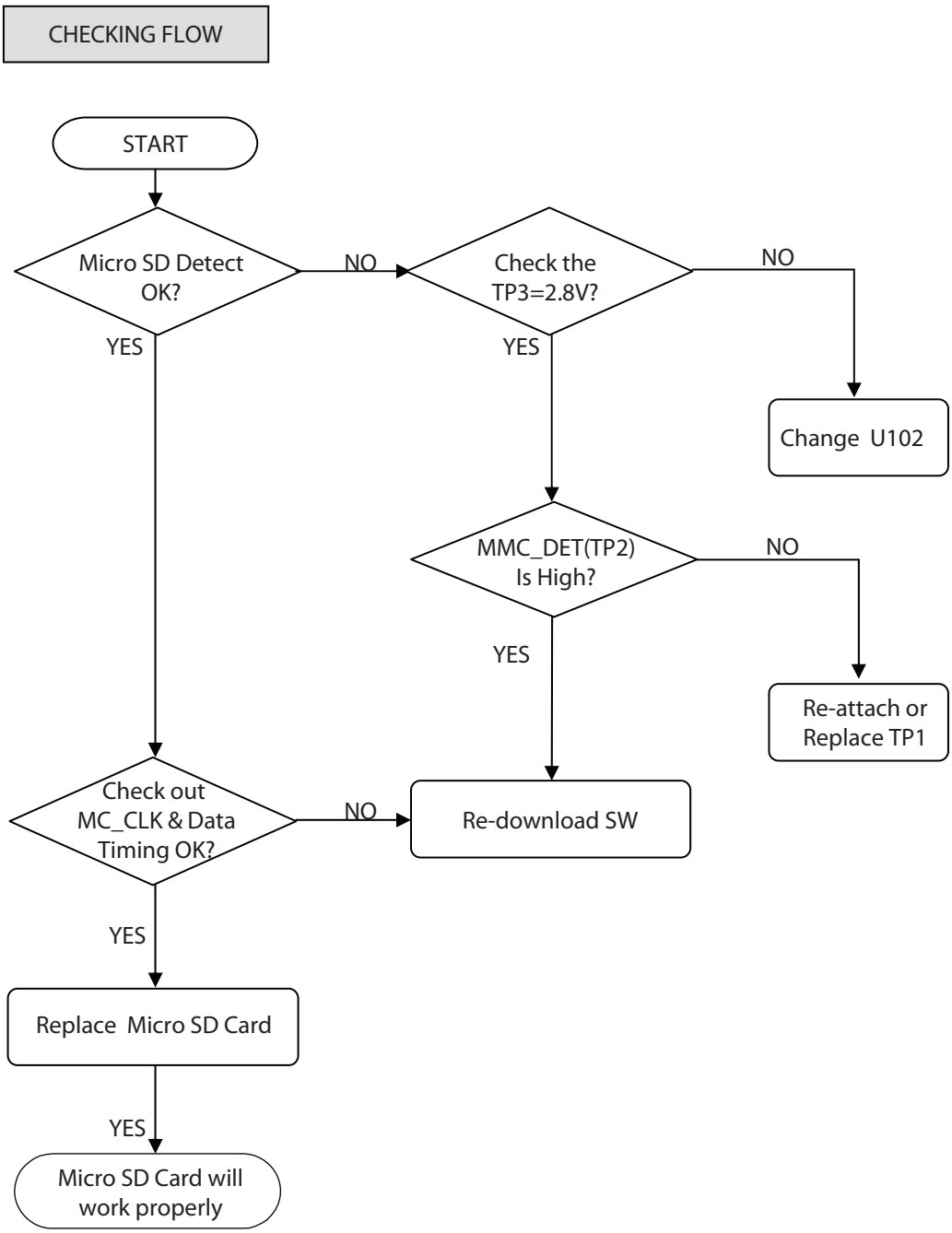


Figure 4.16.1

CIRCUIT





4.17 Bluetooth Trouble

TEST POINT

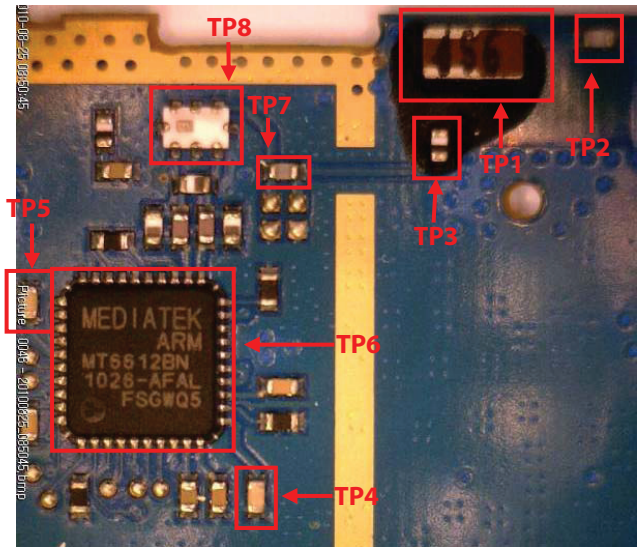
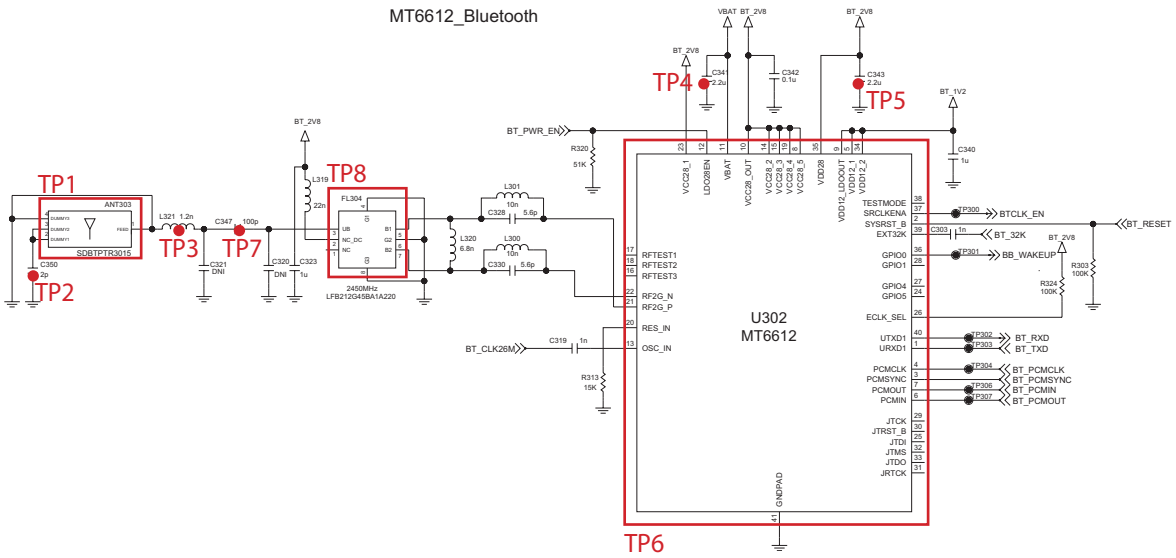
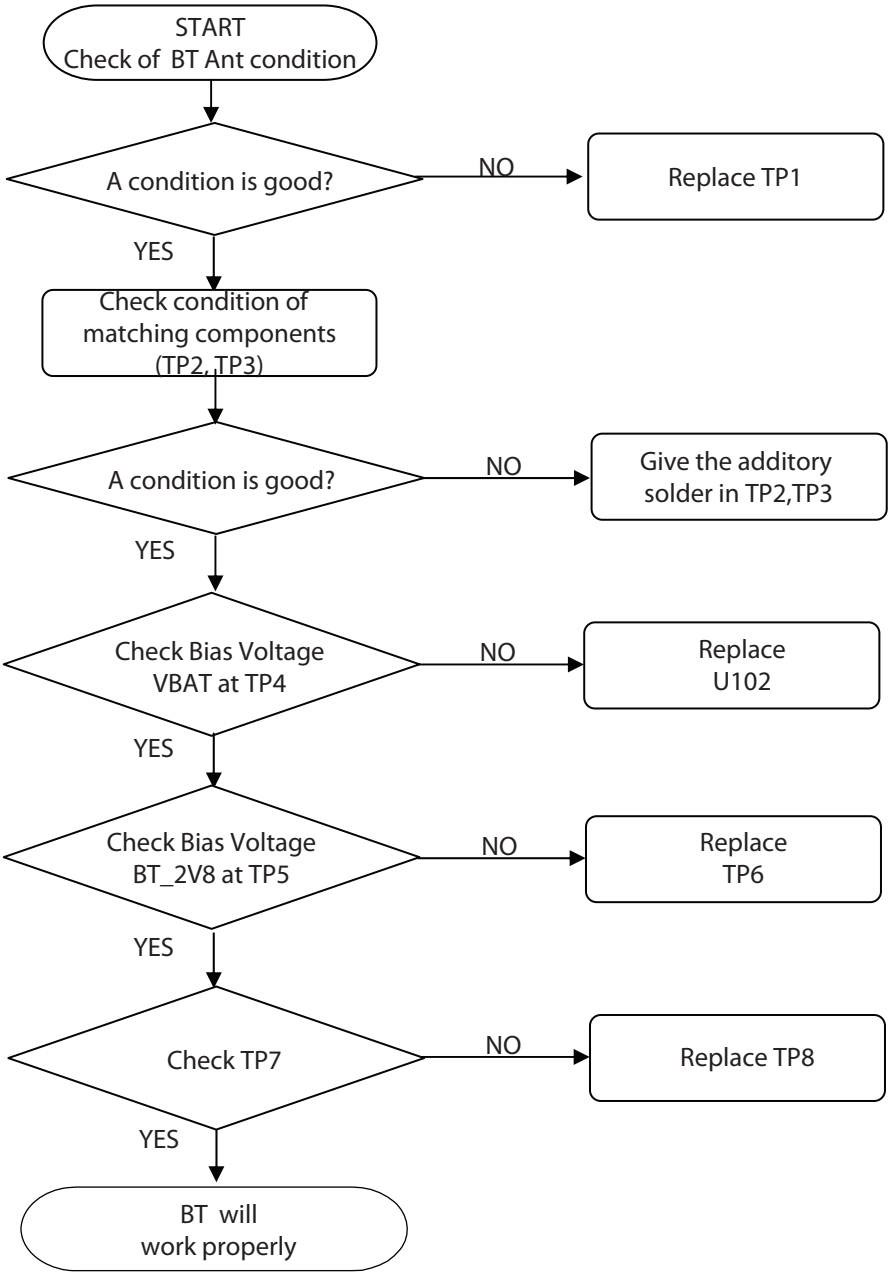


Figure 4.17.1

CIRCUIT



CHECKING FLOW



4.18 FM Radio Trouble

TEST POINT

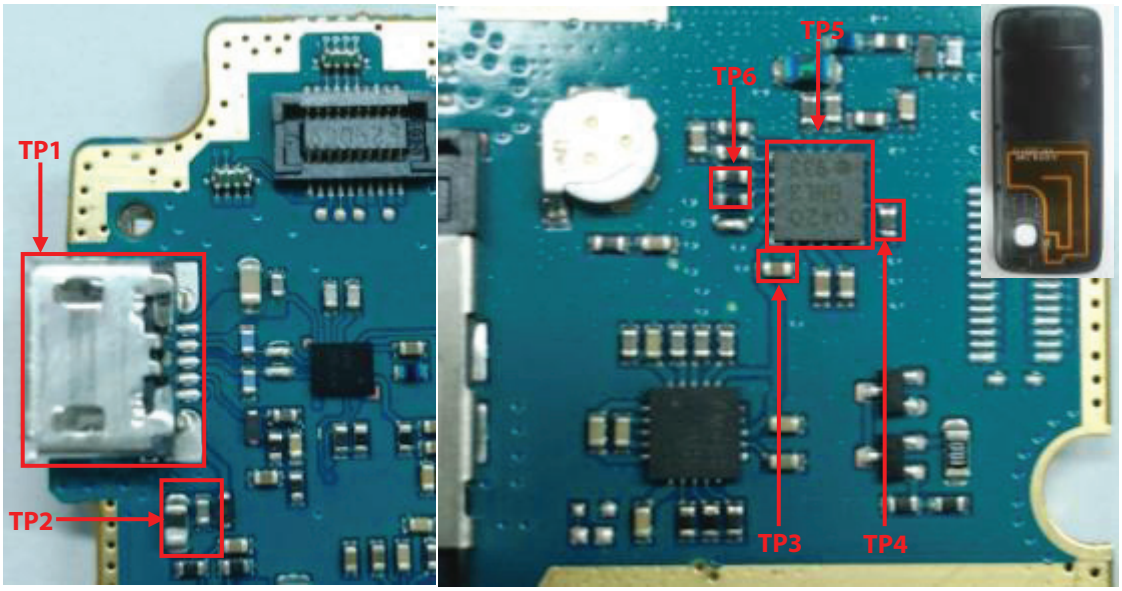
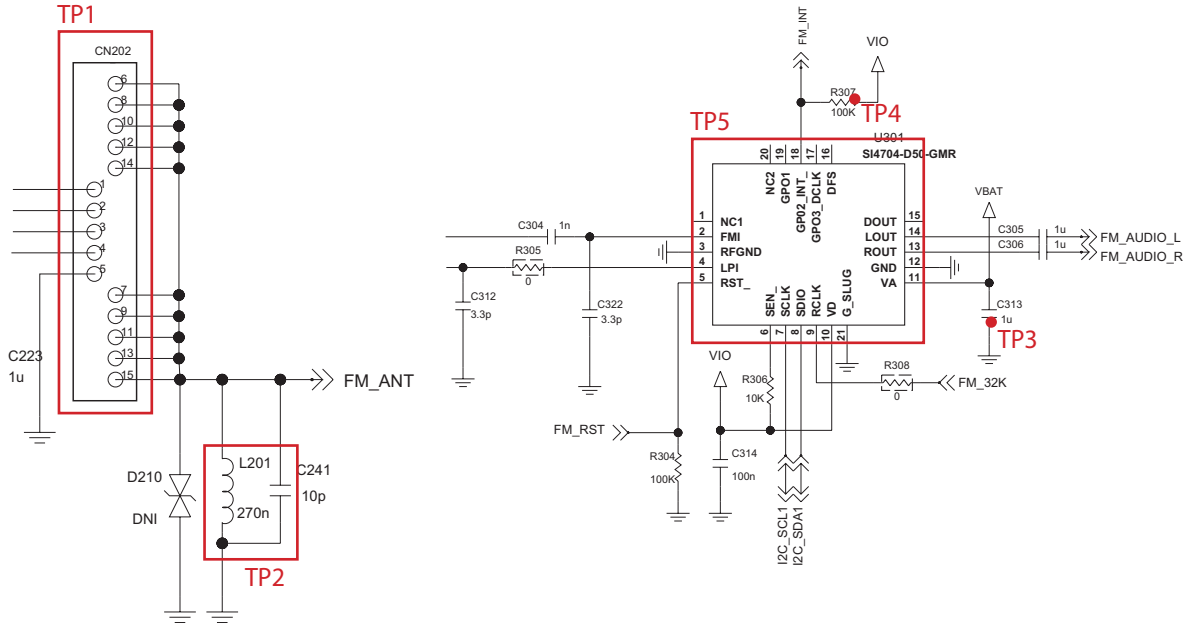
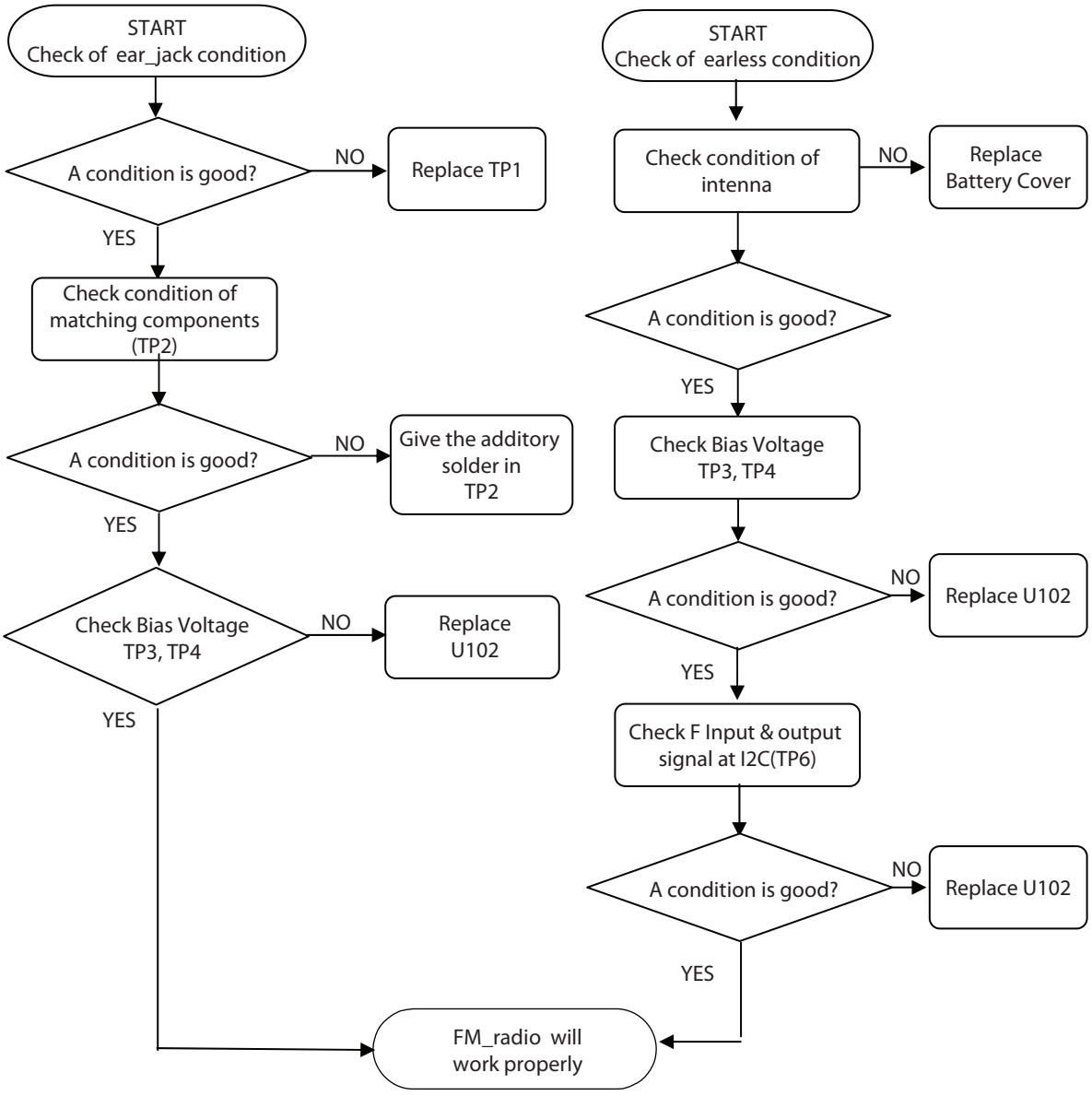


Figure 4.18.1

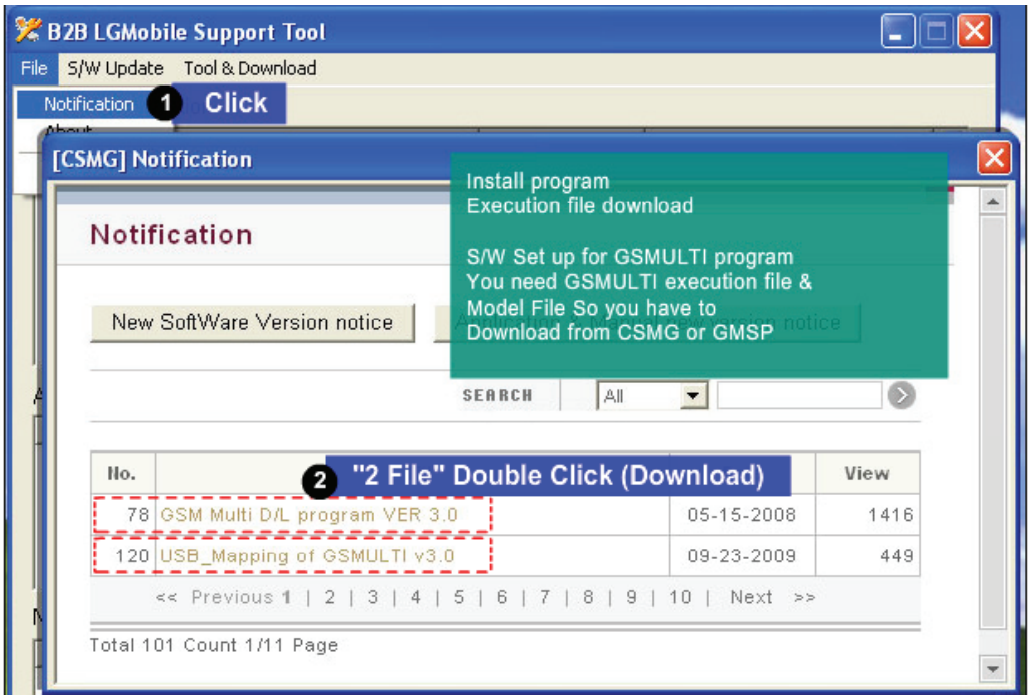
CIRCUIT

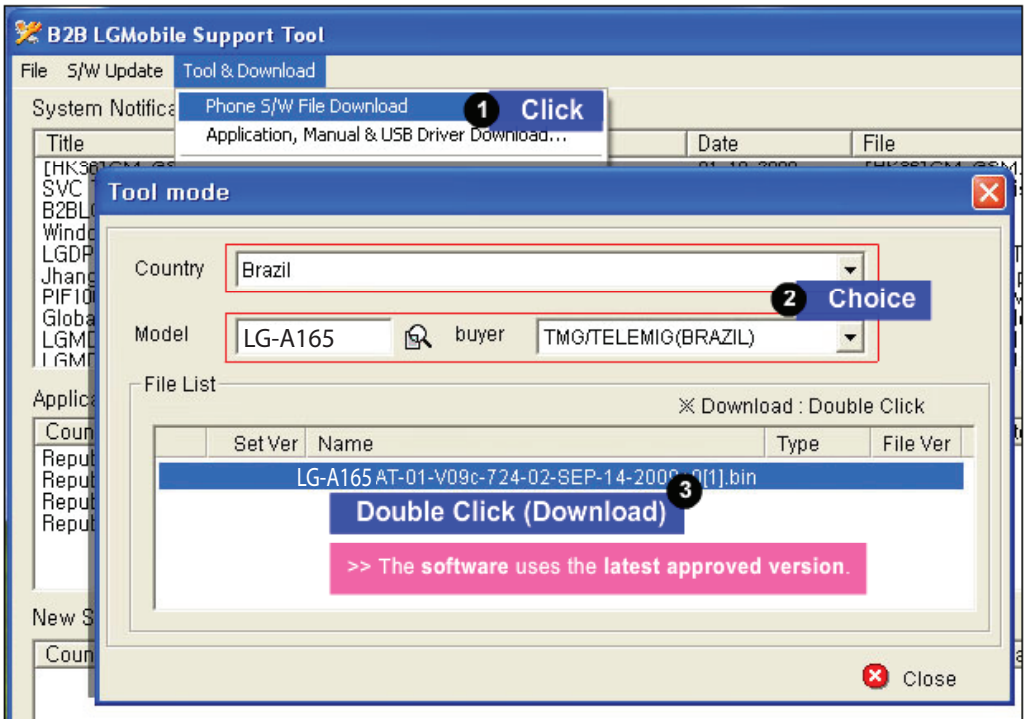


CHECKING FLOW



5. DOWNLOAD





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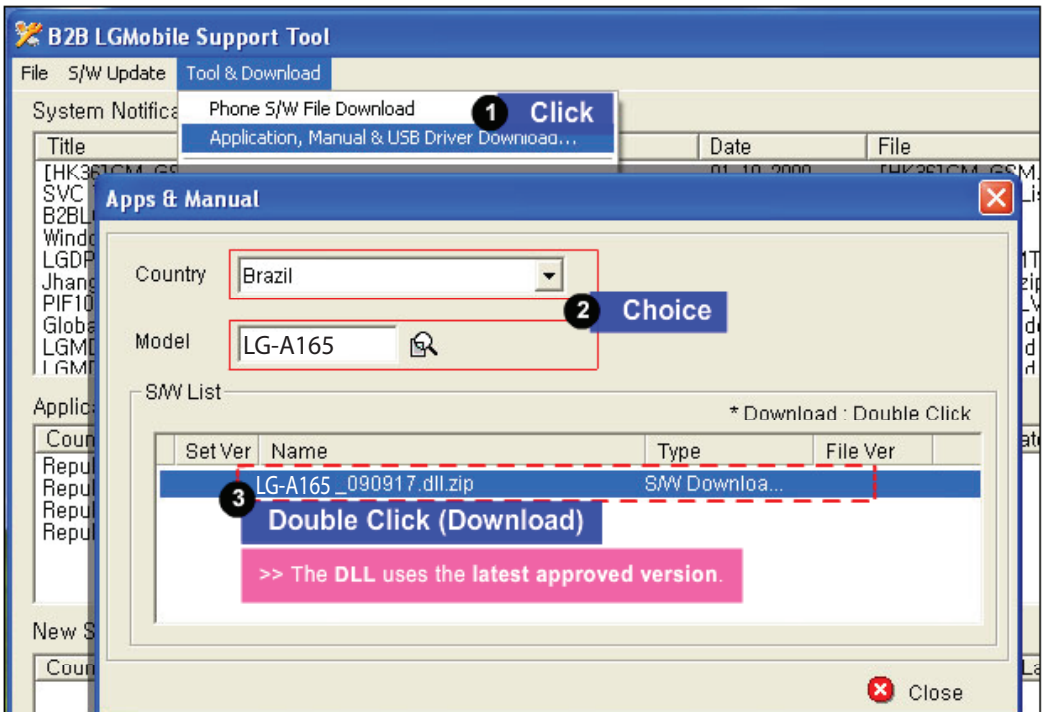

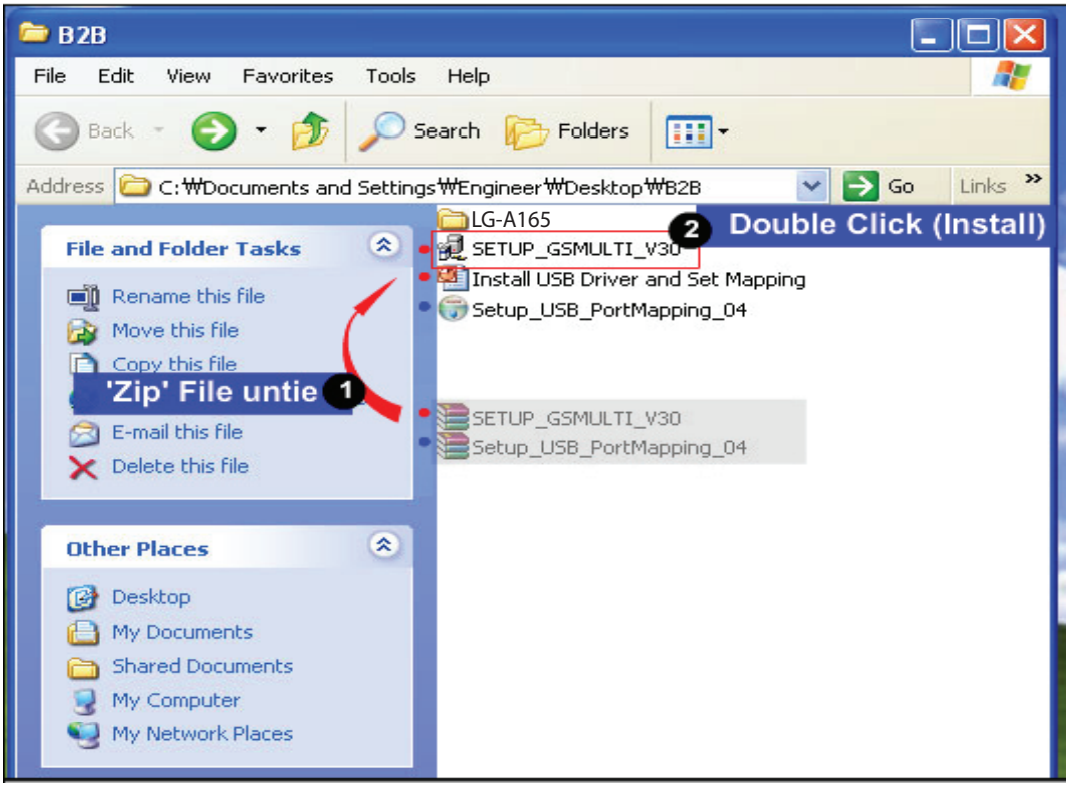

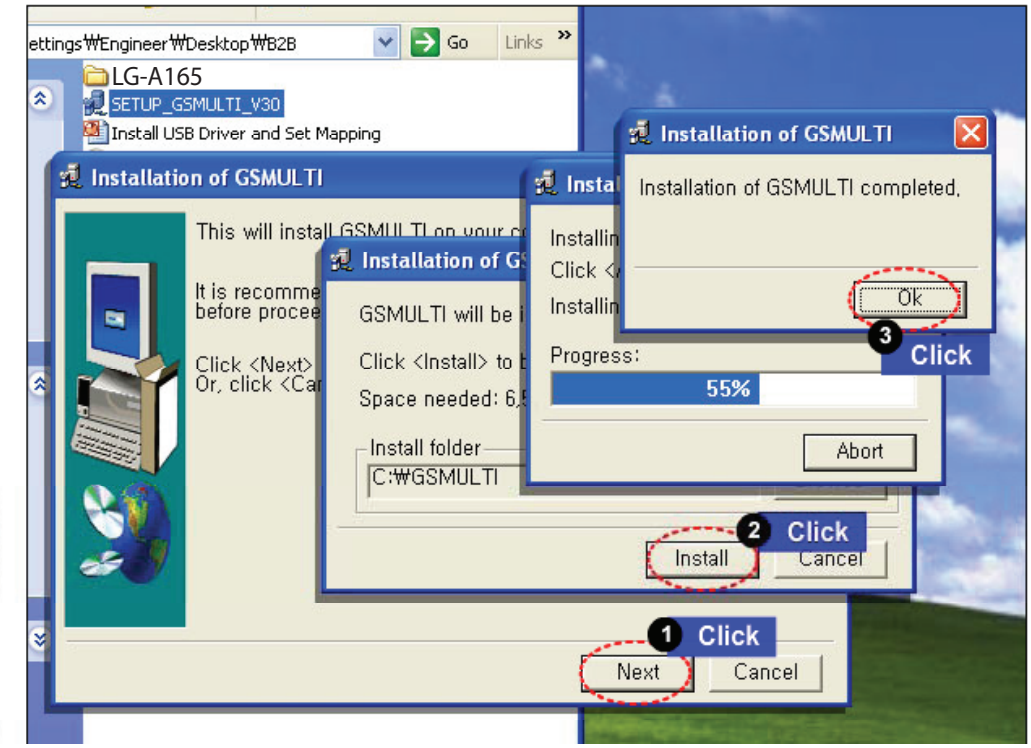

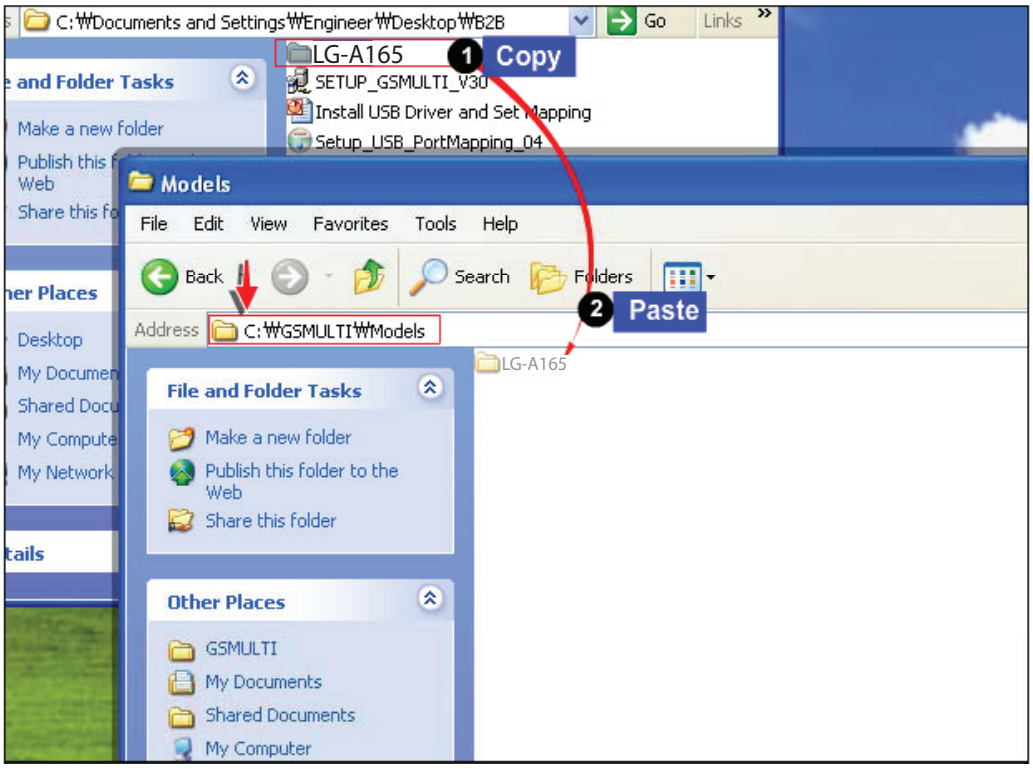

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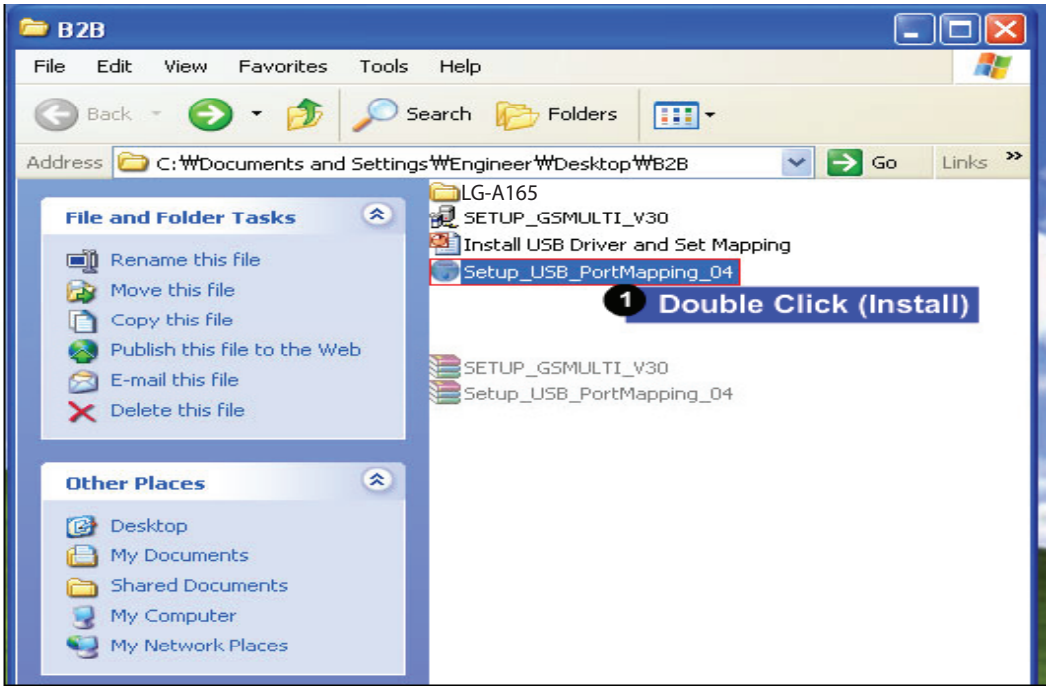

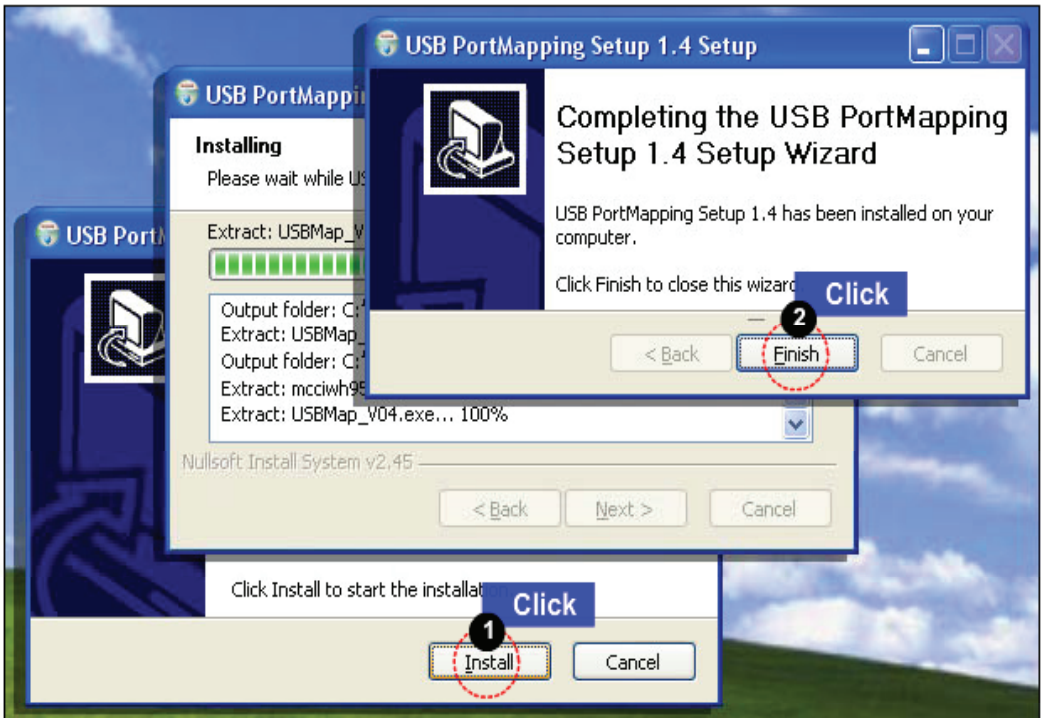

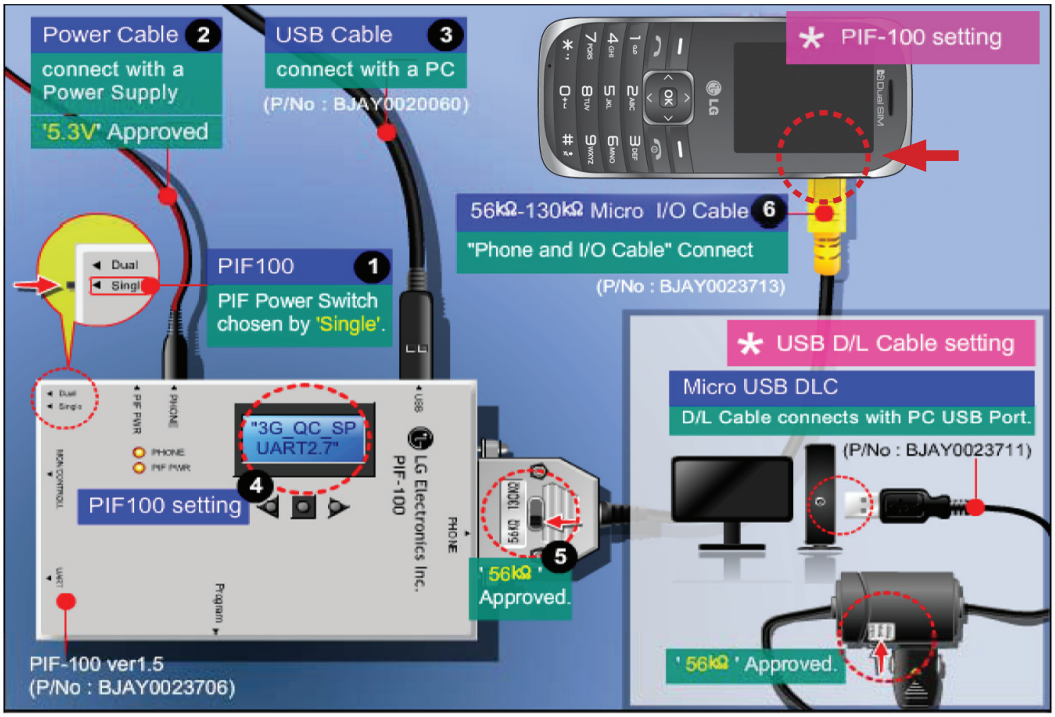

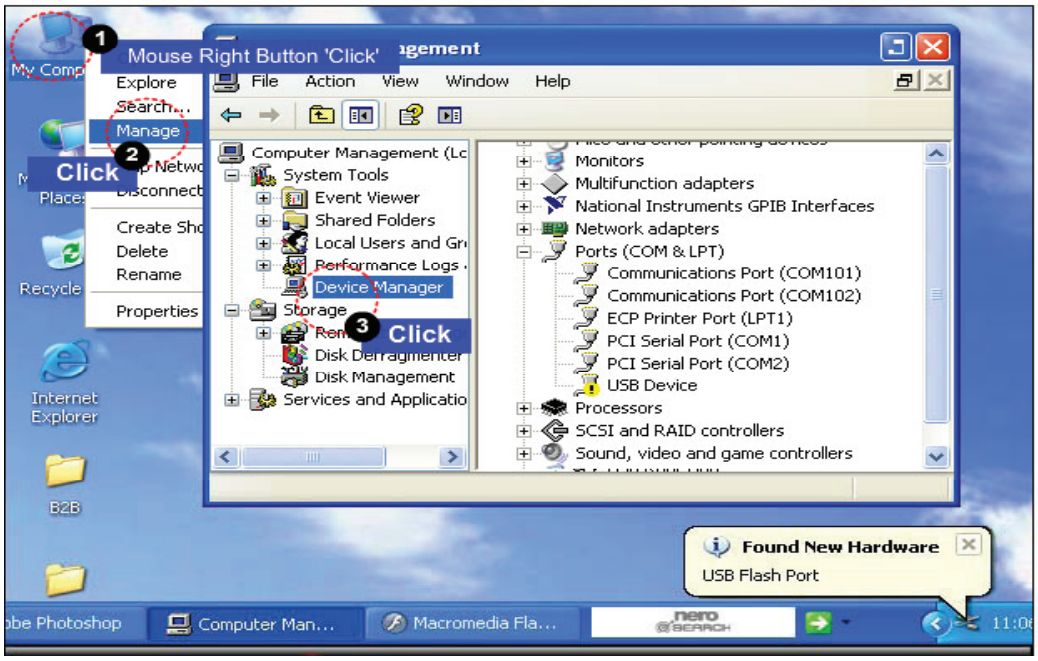

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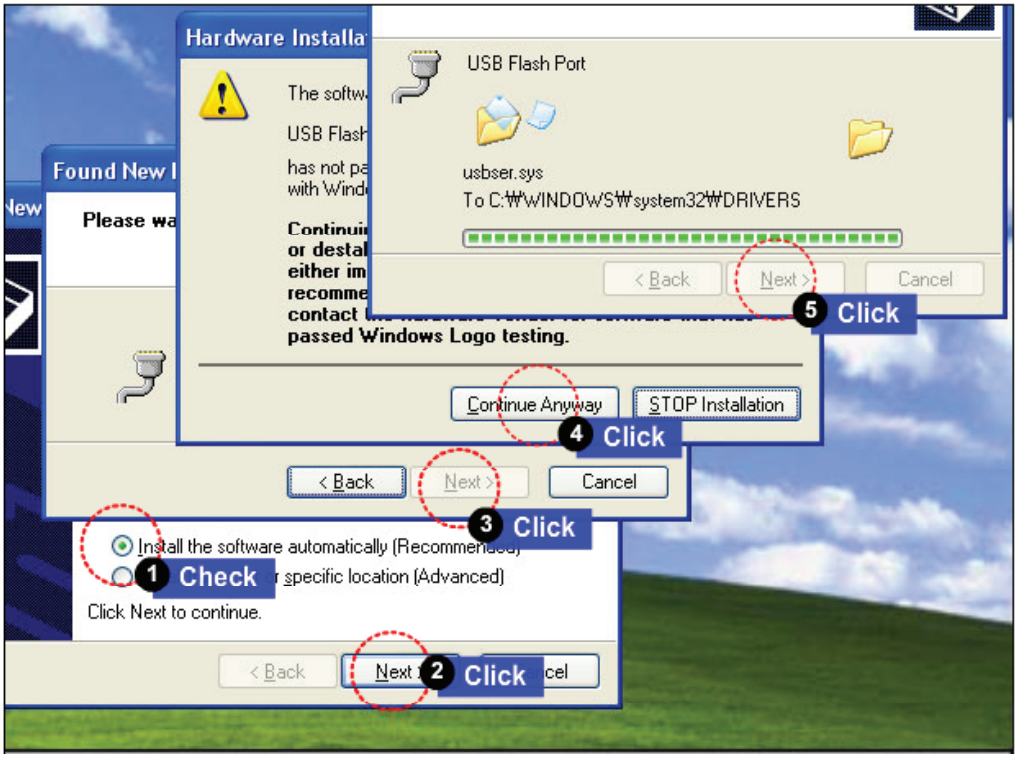

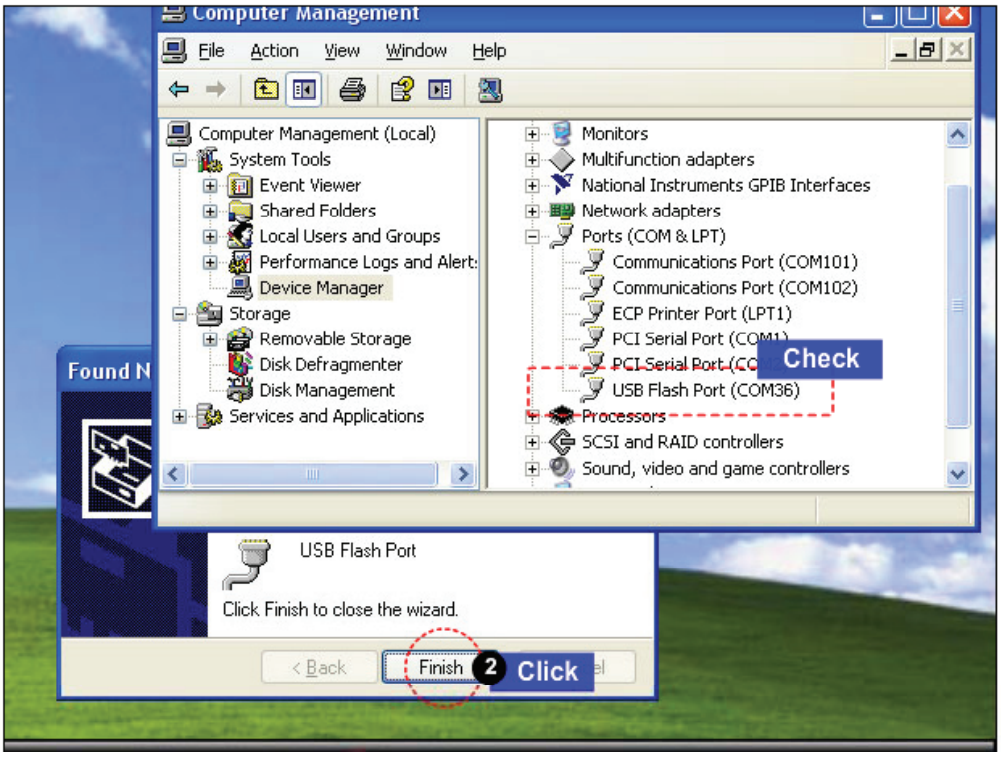

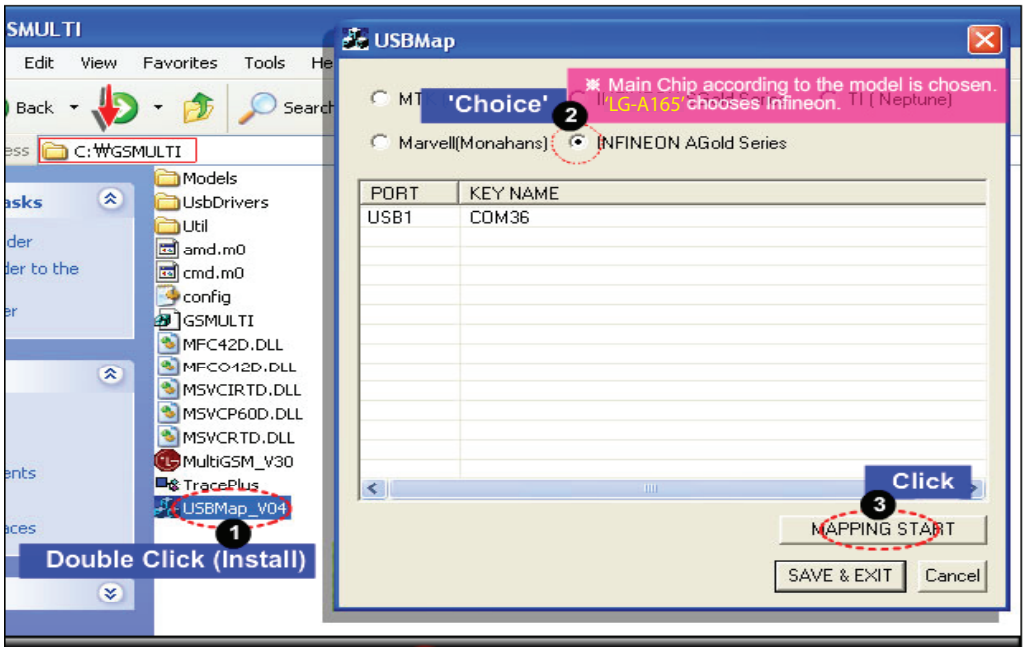

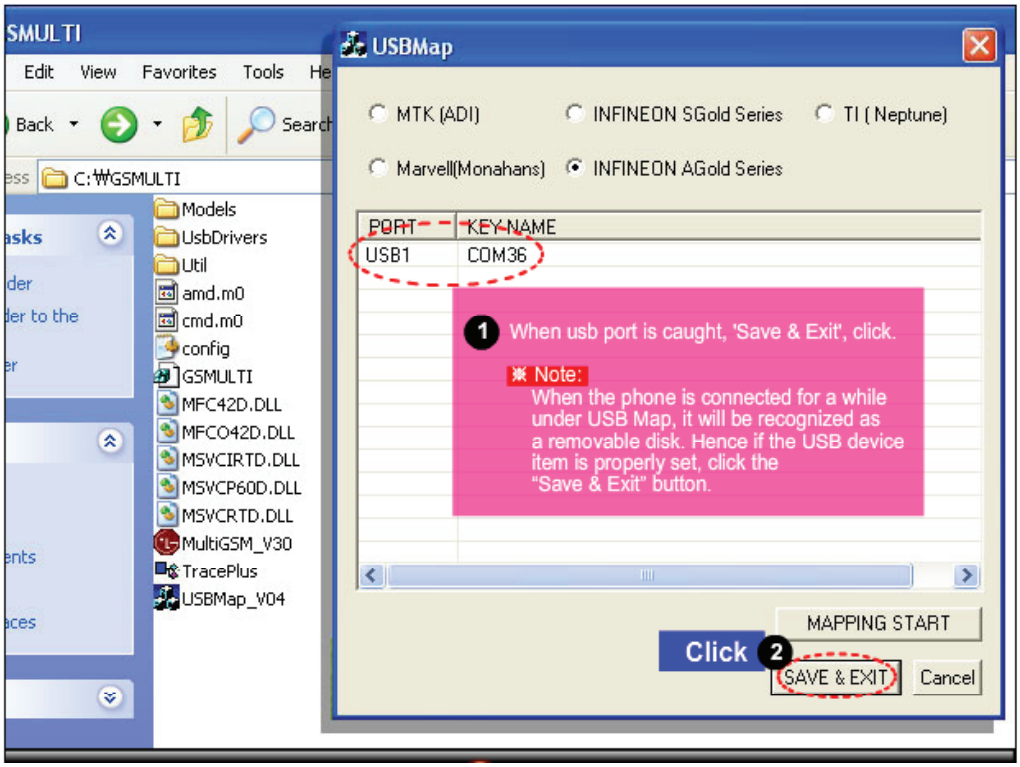

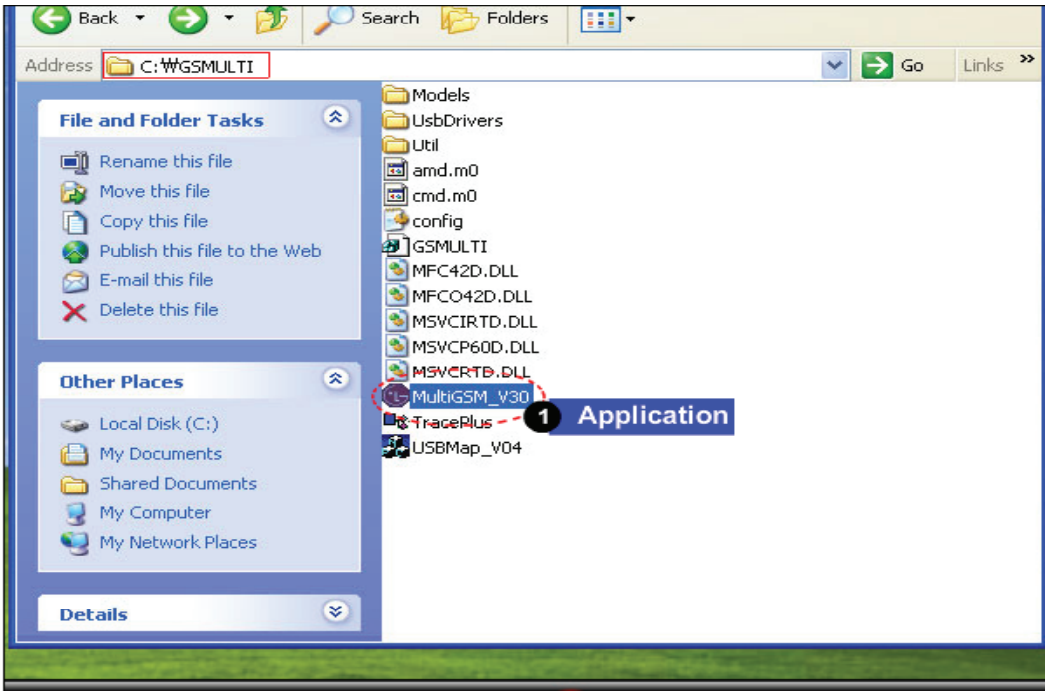

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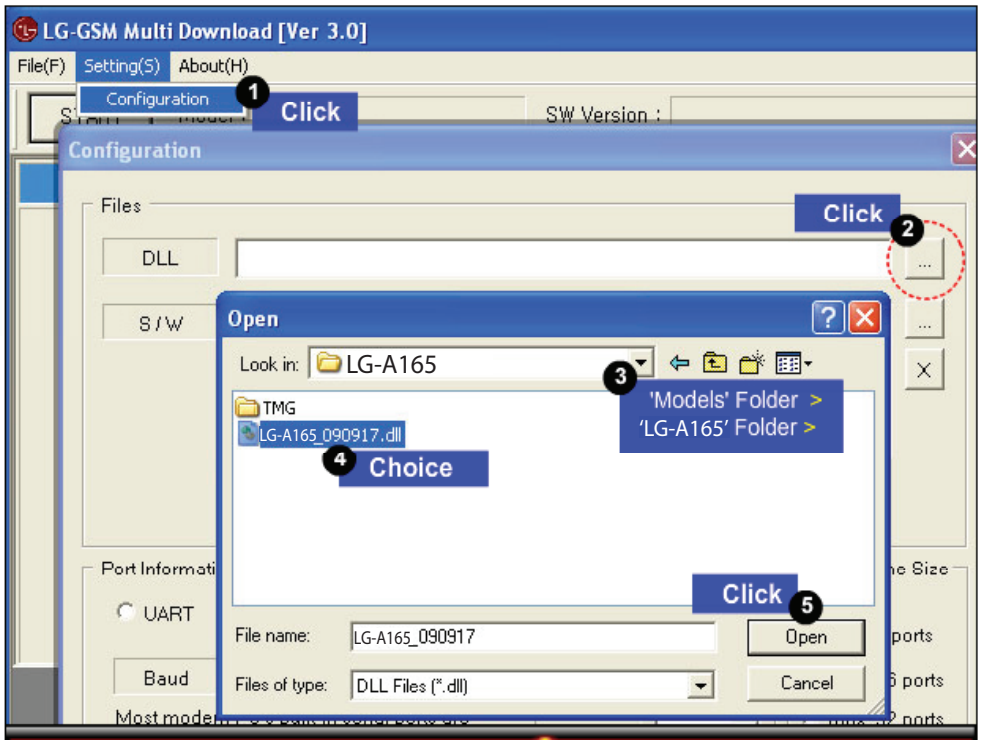

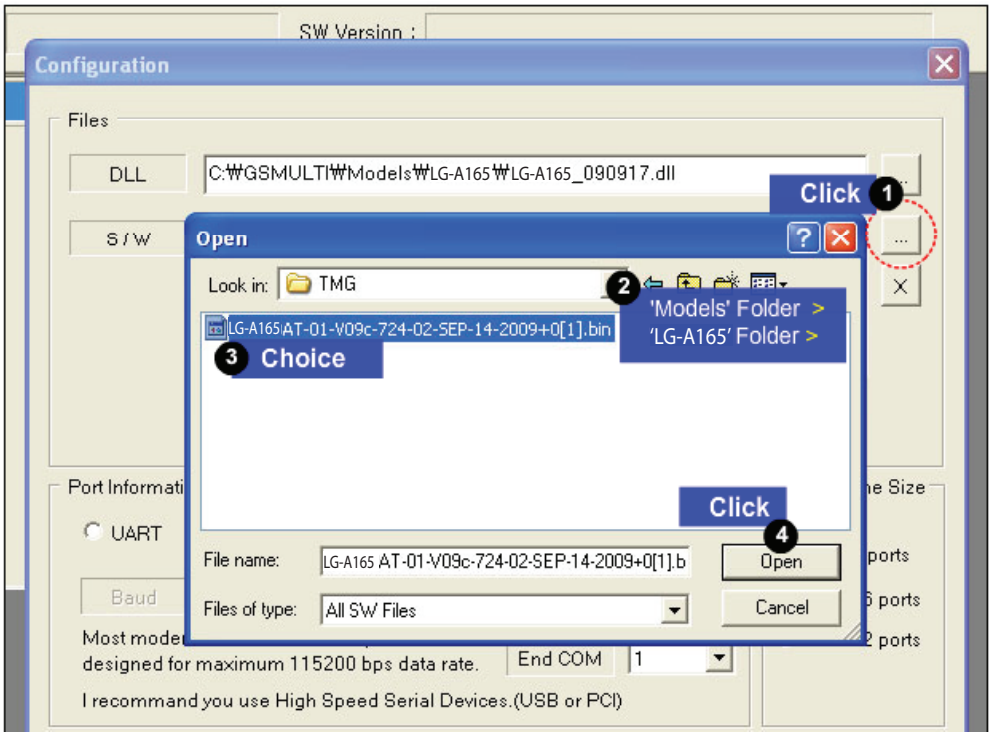

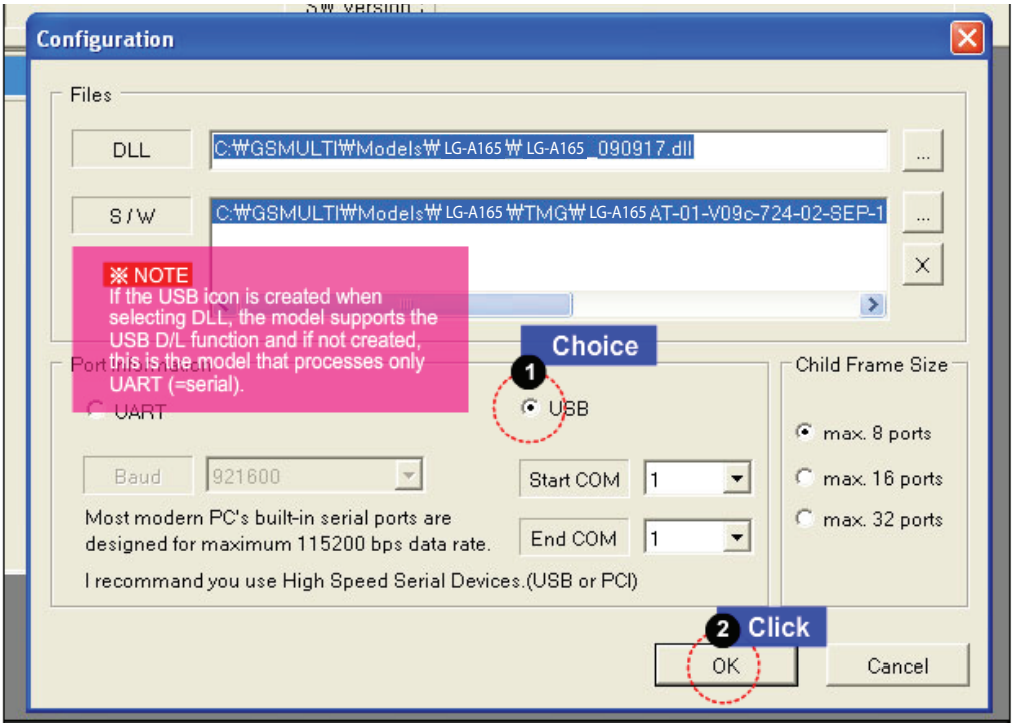

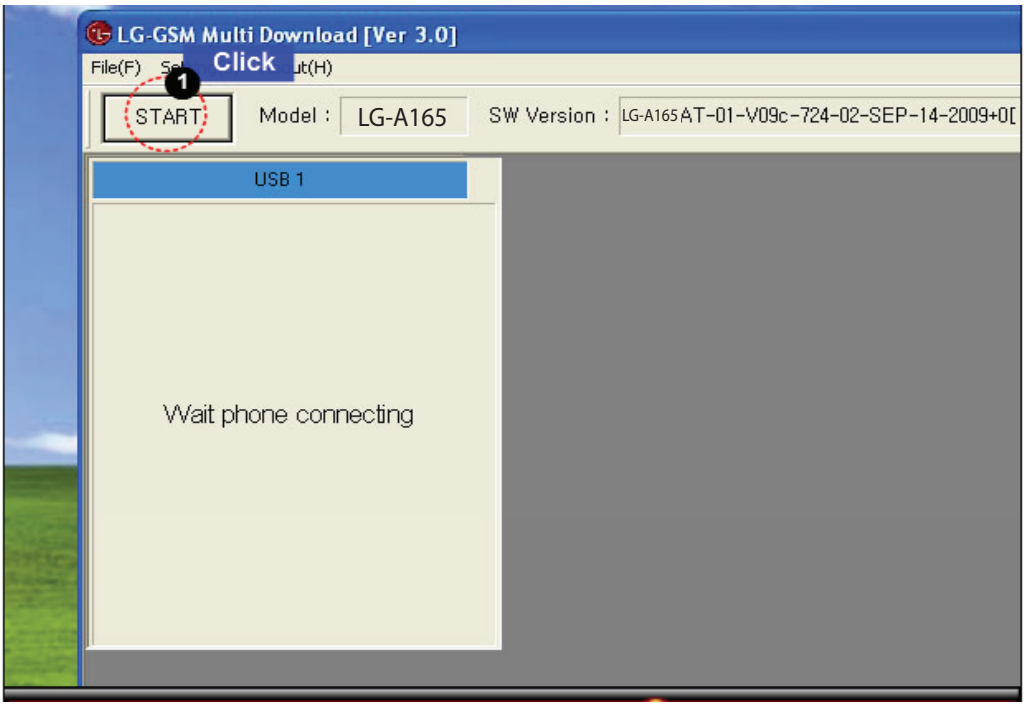

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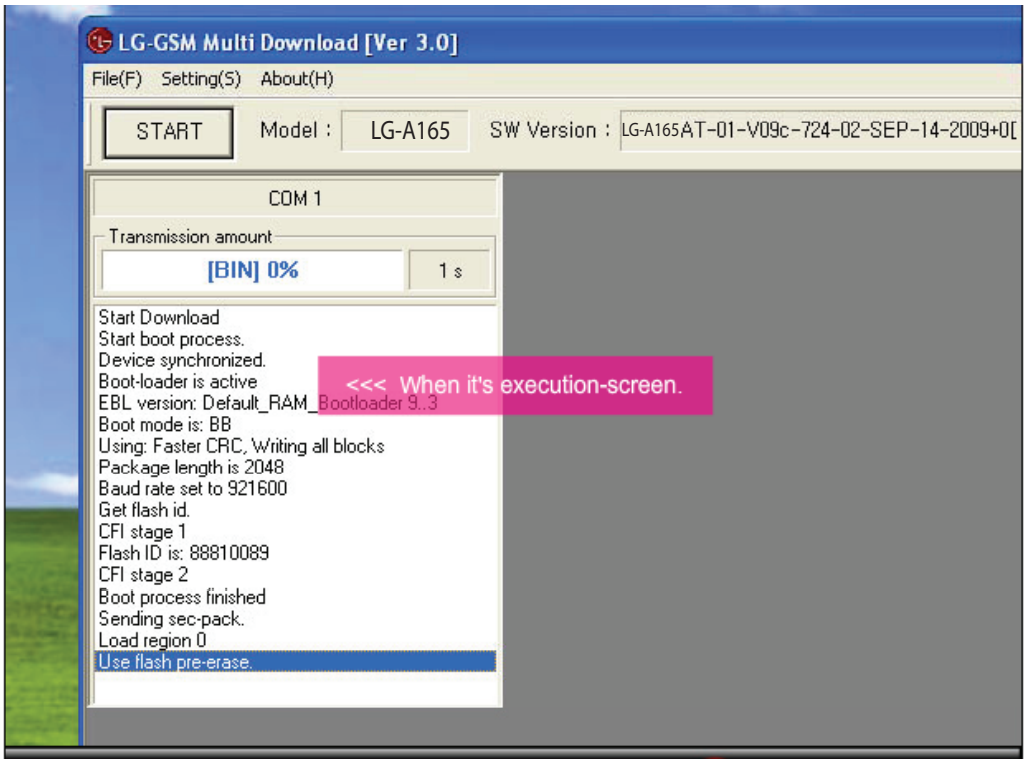
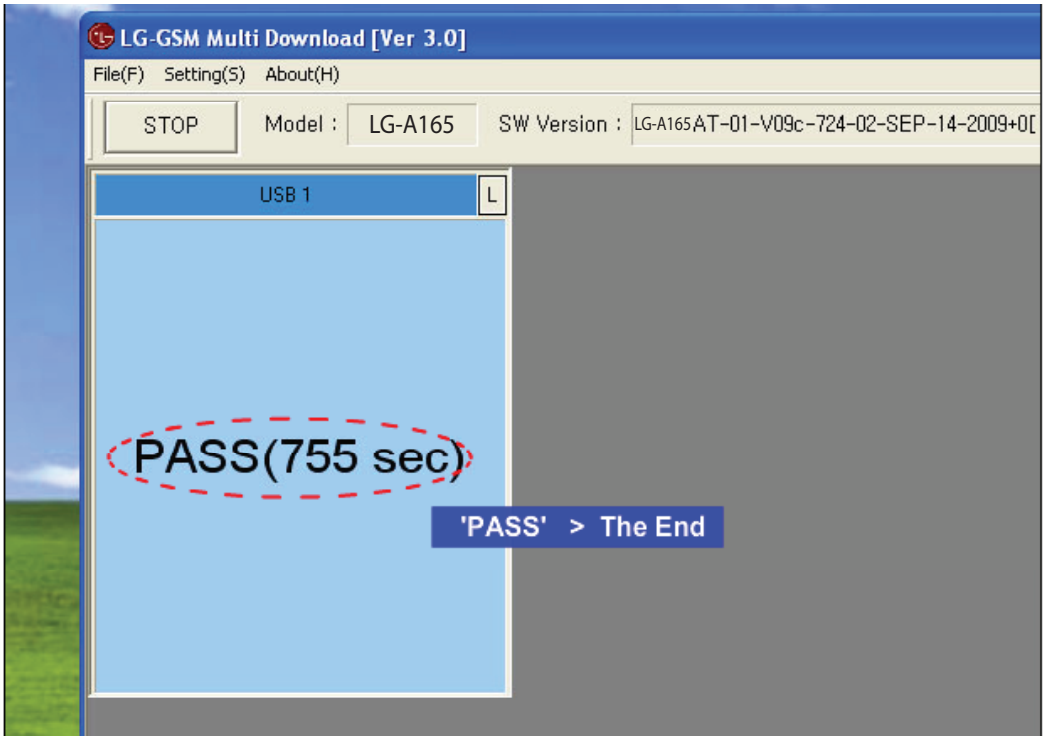
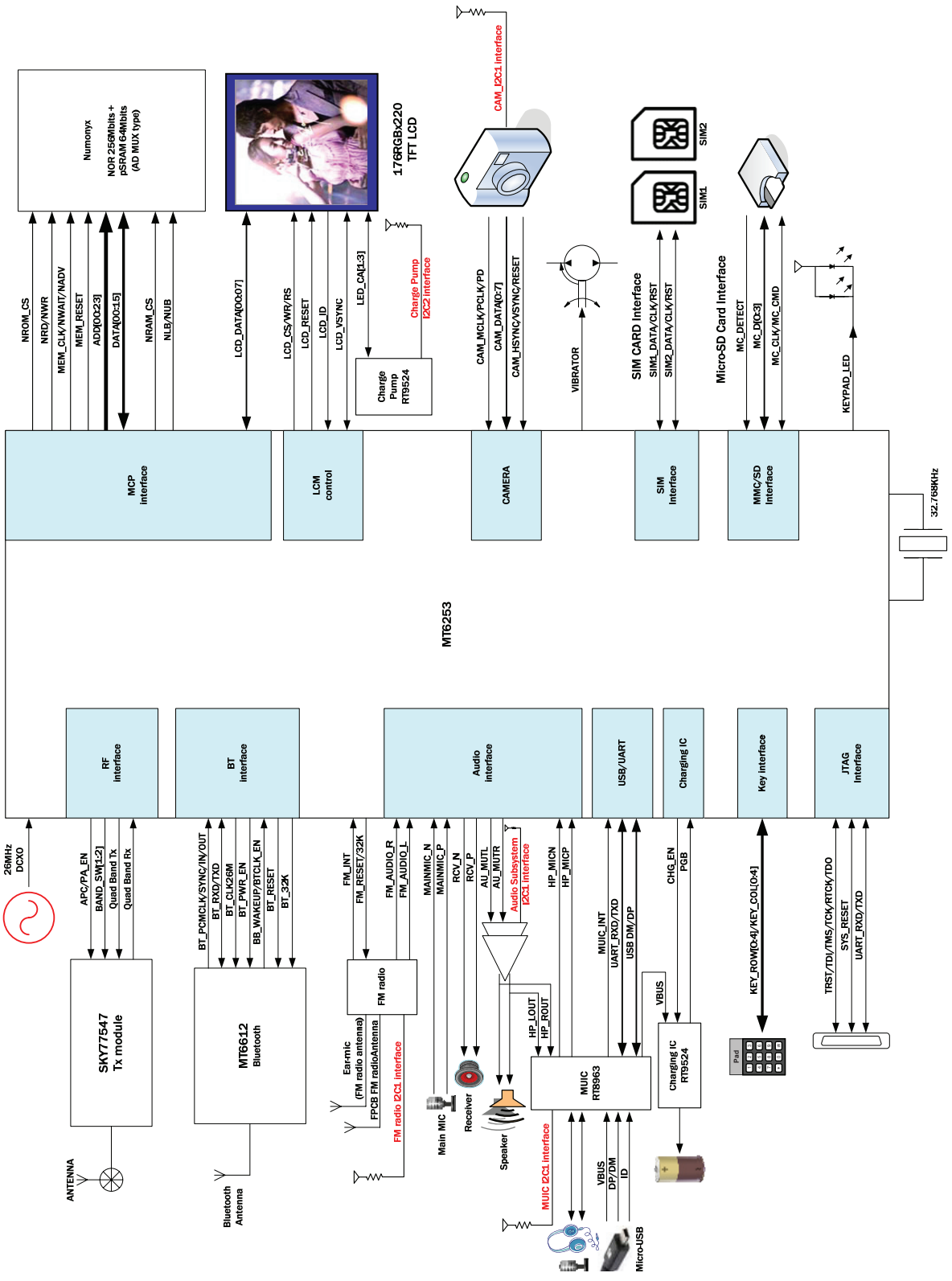
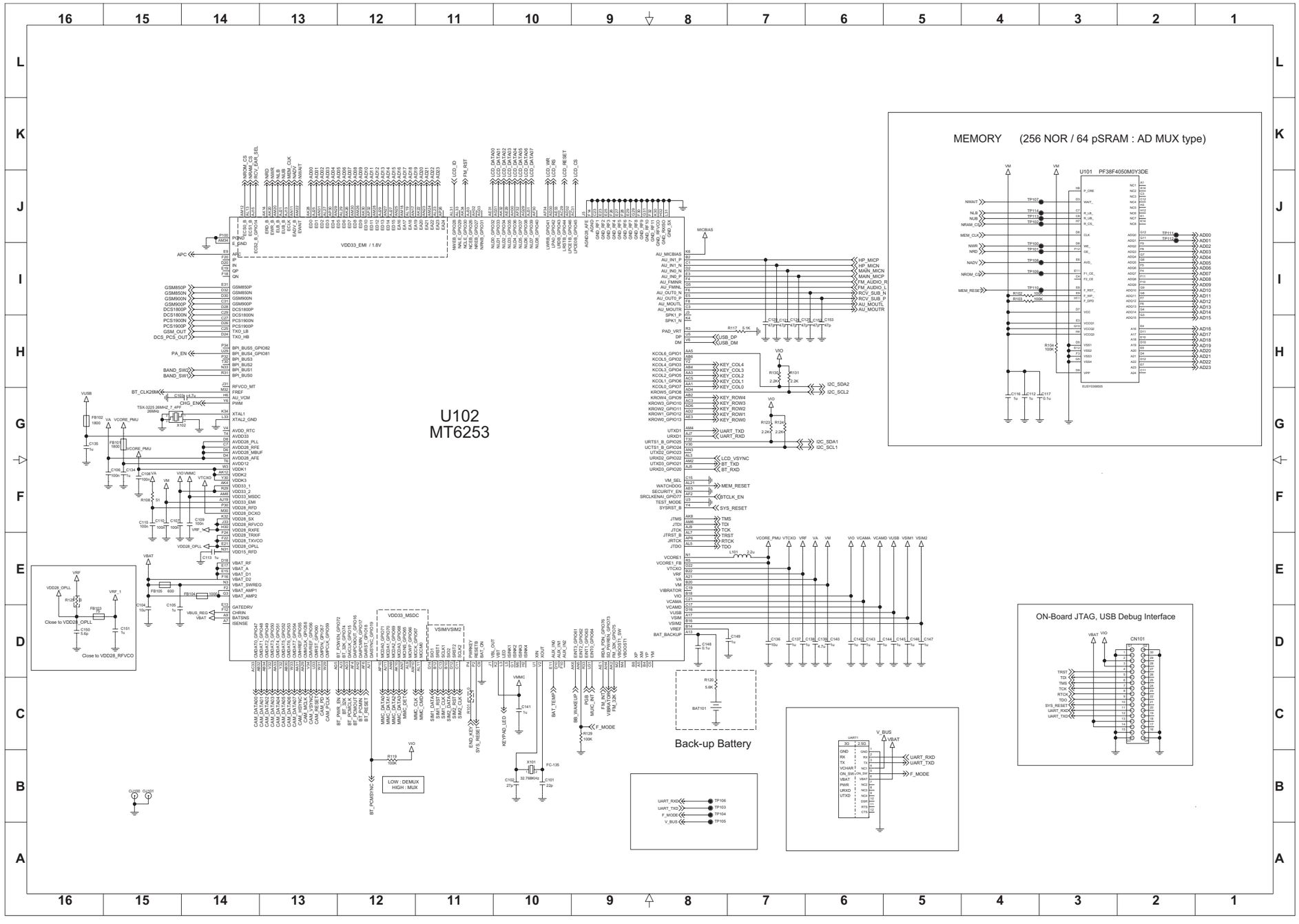




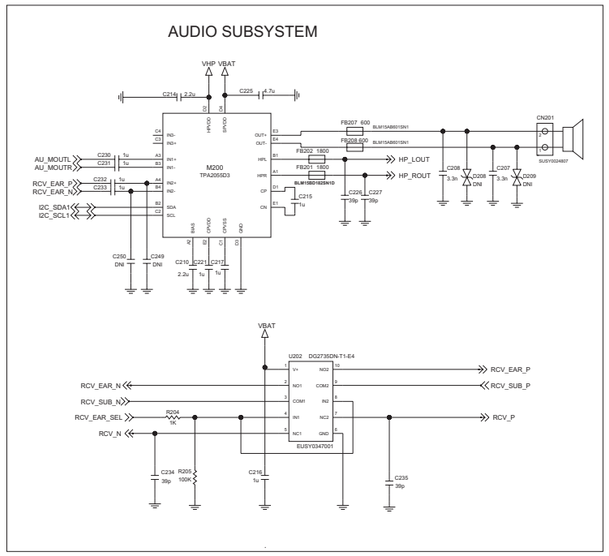
6. BLOCK DIAGRAM

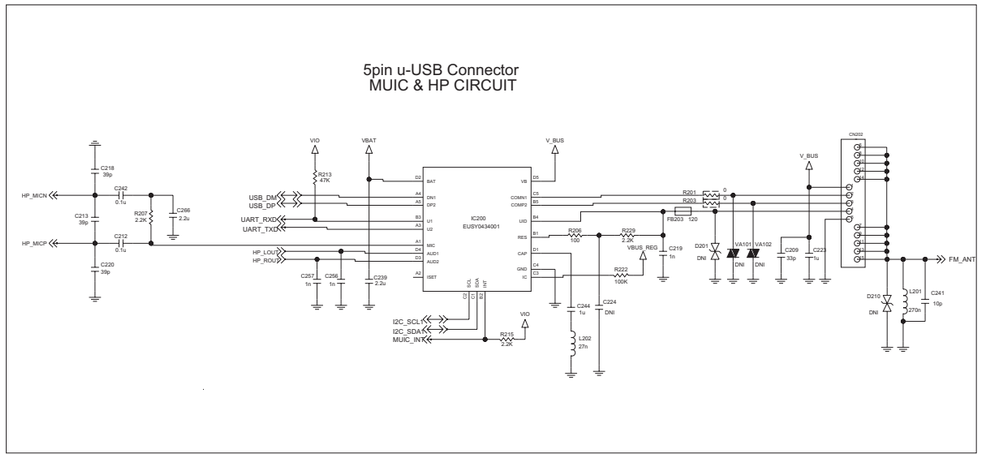


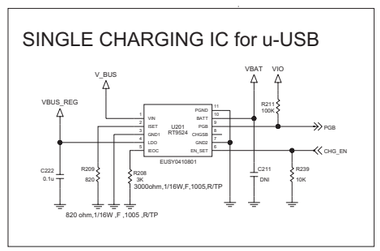
7. CIRCUIT DIAGRAM

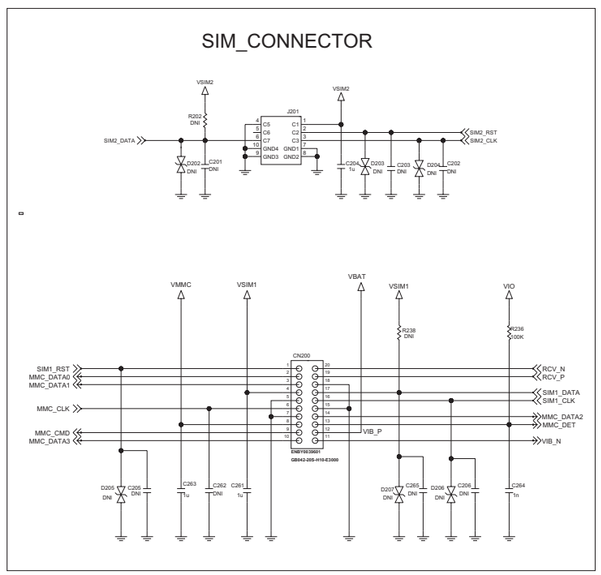


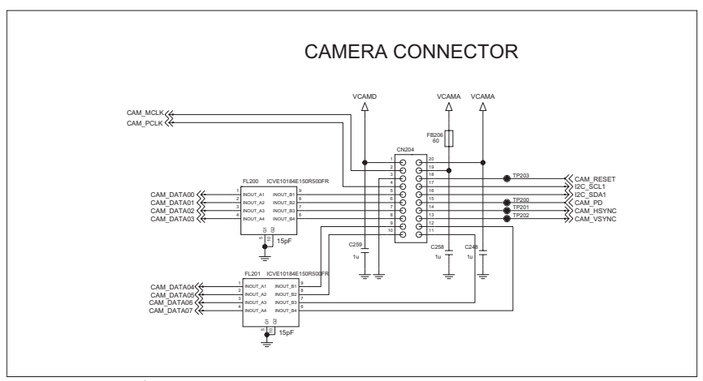
7. CIRCUIT DIAGRAM



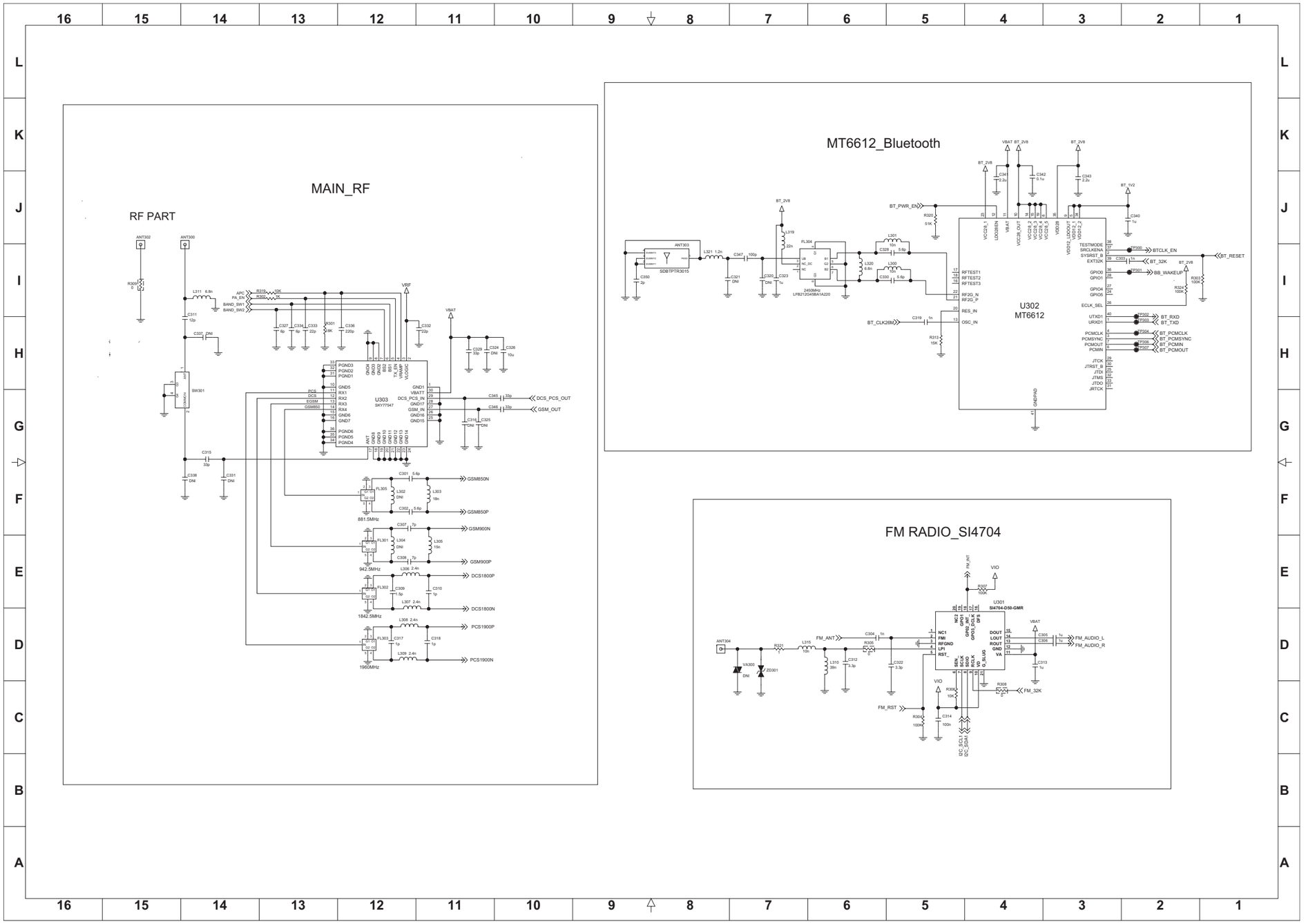






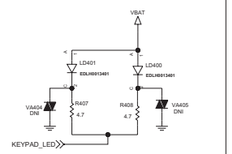


7. CIRCUIT DIAGRAM

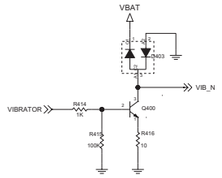


7. CIRCUIT DIAGRAM

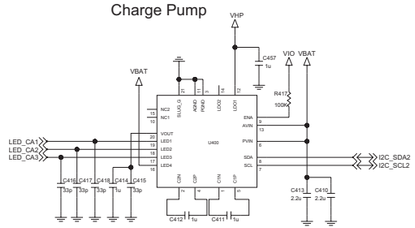
KEY BACKLIGHT



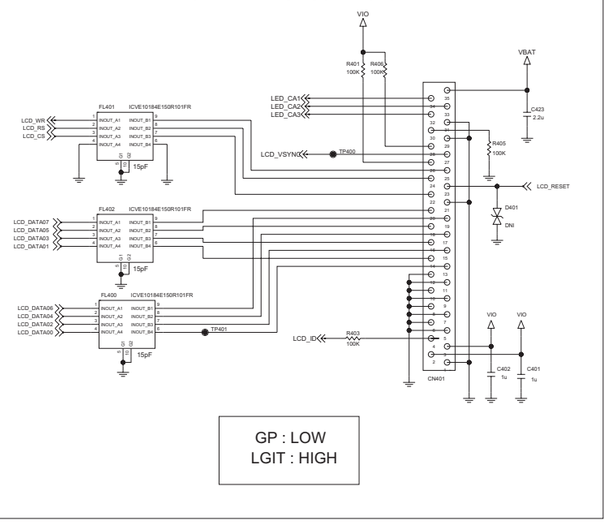
VIBRATOR CIRCUIT



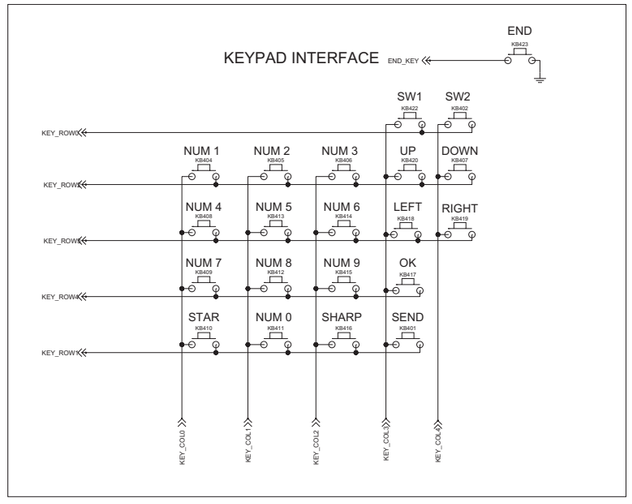
Charge Pump



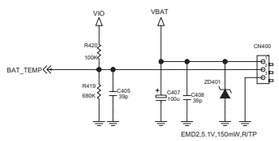
LCD INTERFACE CONNECTOR



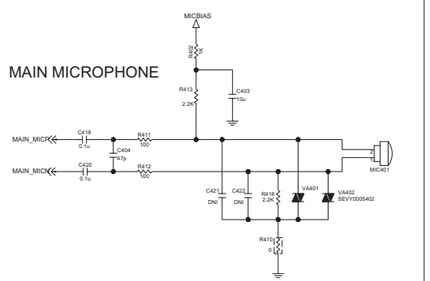
KEYPAD INTERFACE



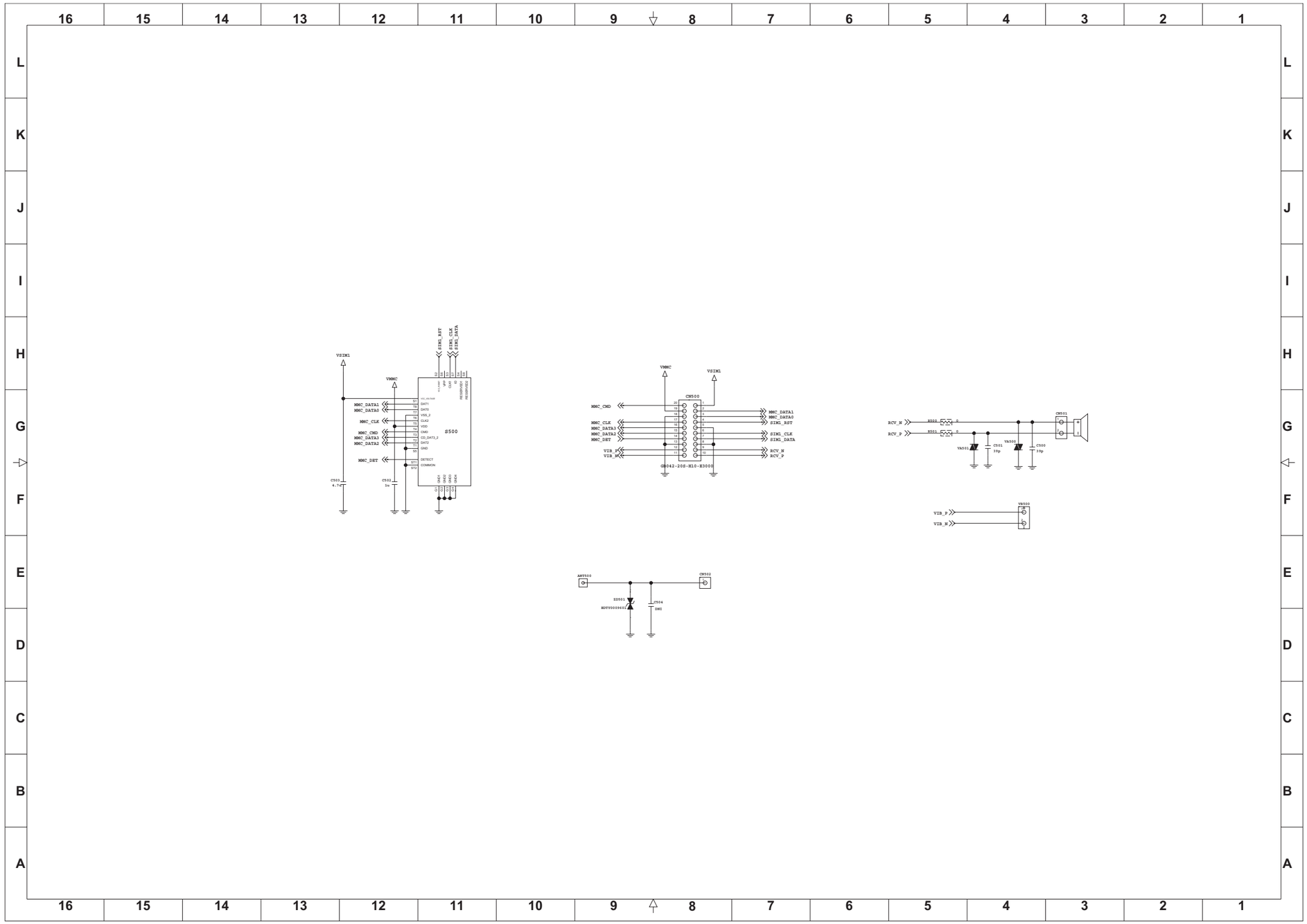
BATTERY CONNECTOR



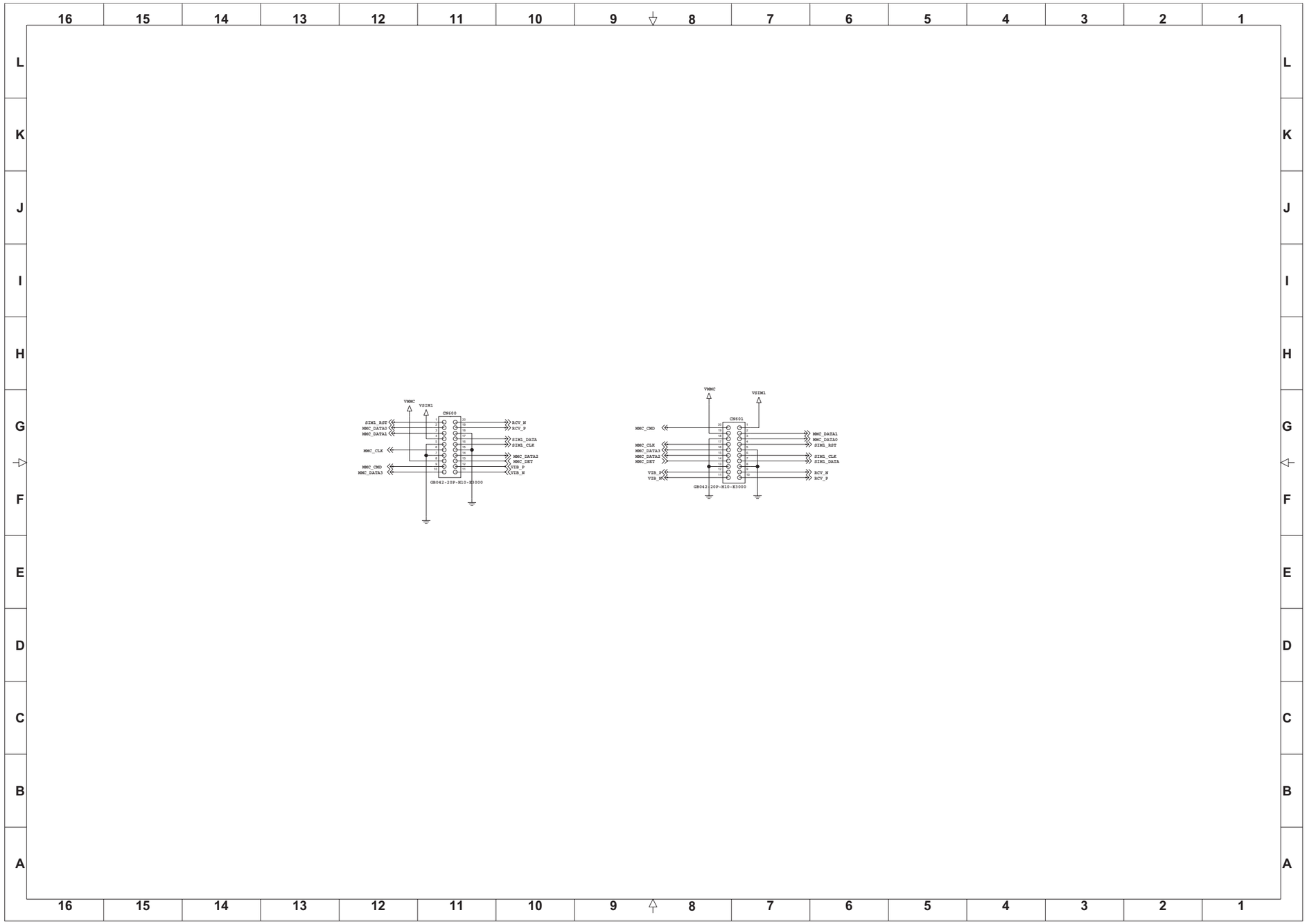
MAIN MICROPHONE



7. CIRCUIT DIAGRAM



7. CIRCUIT DIAGRAM



8. BGA PIN MAP

BGA IC pin check (U102)

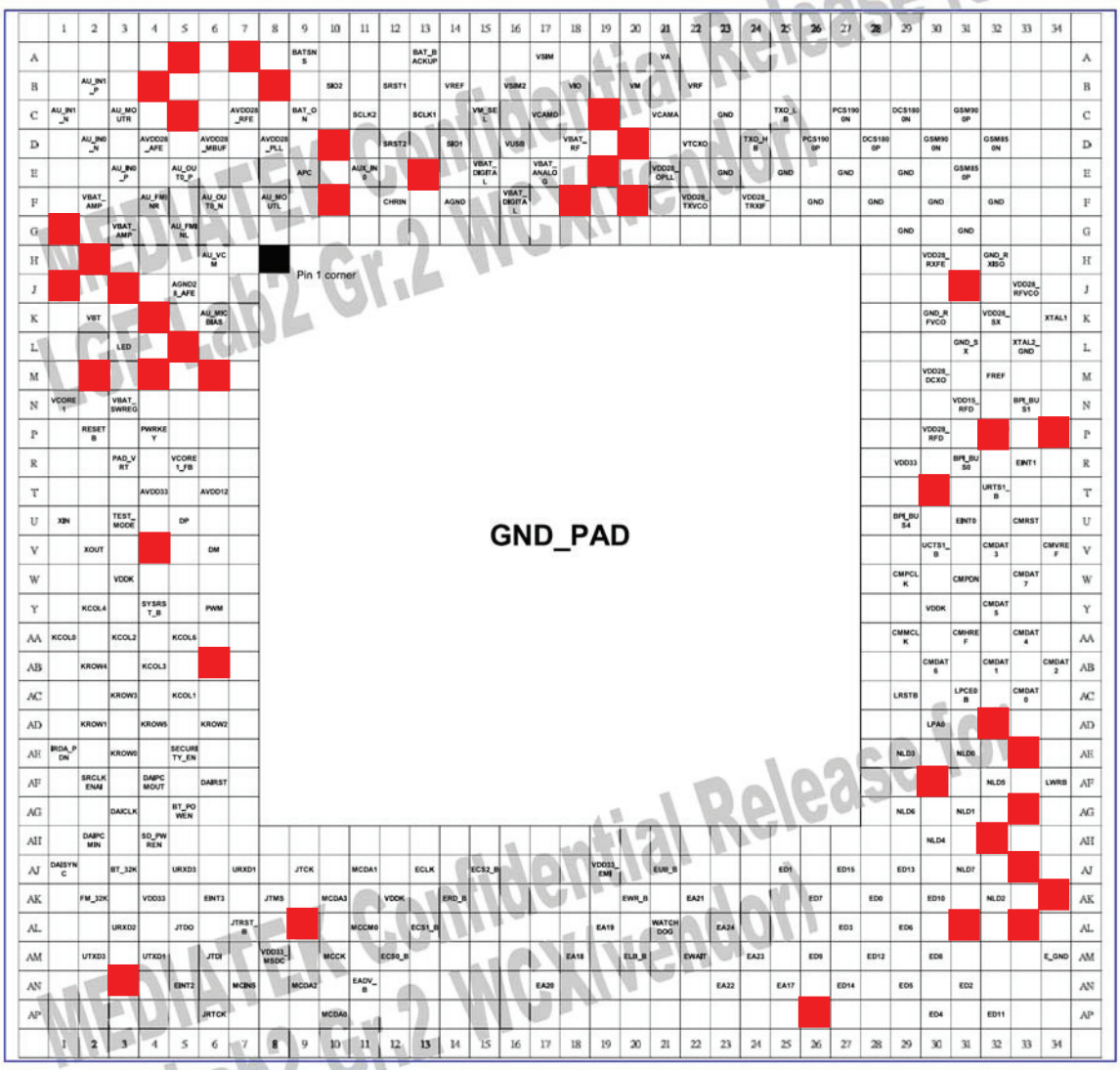


Figure 3 Top View of MT6253A aQFN 11.5mm * 11.5mm 0.47mm pitch package

: not in use

8. BGA PIN MAP

BGA IC pin check (U101)

▪ **Ball Diagram (Top View), PF38F4050M0Y3DF**

Pin 1

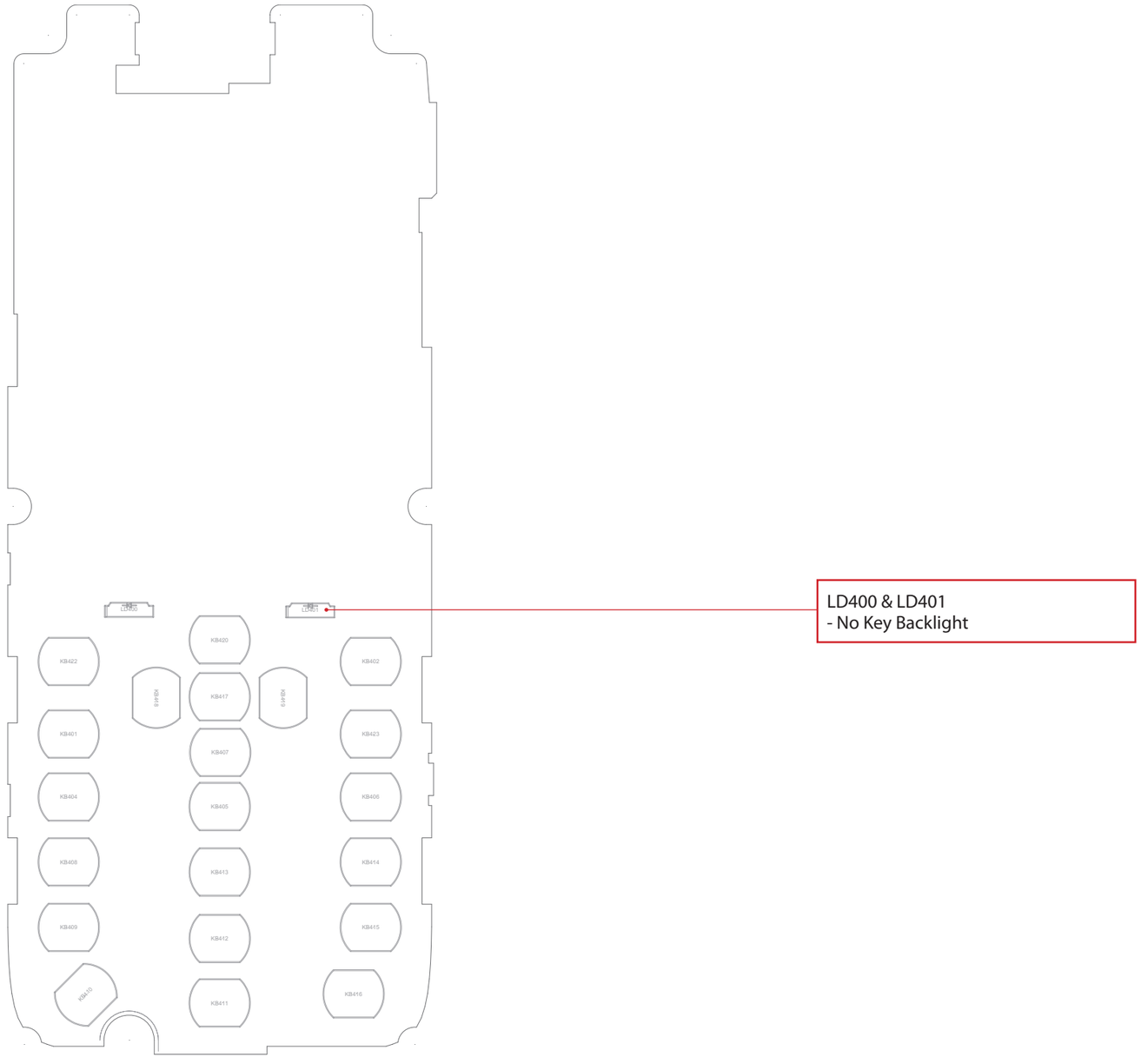
	1	2	3	4	5	6	7	8	9	
A		A4	A6	A7	A19	A23	A24	A25		A
B	A2	A3	A5	A17	A18	F-DPD	A22	A26	A16	B
C	A1	VSS	VSS	VSS	D-VCC	VSS	VSS	VSS	A15	C
D	A0	S-VCC	D-VCC	F1-VCC	ADV#	F2-VCC	D-VCC	N-ALE	A14	D
E	F-WP1#	WE#	D2-CS#	Depop (Index)	N-CLE	F4-CE# / A27	A21	A10	A13	E
F	F-WP2#	D1-CS#	D-CAS#	D-RAS#	Depop (RFUs)	N-RE# / S-CS1#	A20	A9	A12	F
G	RFU	F2-CE#	F1-CE#	D-BA0	Depop (RFUs)	D-CKE	F-RST#	A8	A11	G
H	N-RY/BY#	N-WE# / S-CS2	F3-CE#	D-BA1	D-CLK#	D-WE#	OE#	D-DM1 / R-UB#	D-DM0 / R-LB#	H
J	F-VPP	VCCQ	VCCQ	F1-VCC	D-CLK	F2-VCC	VCCQ	VCCQ	F-WAIT	J
K	AD2	VSS	VSS	VSS	F-CLK	VSS	VSS	VSS	AD13	K
L	AD1	AD3	AD5	AD6	AD7	AD9	AD11	AD12	AD14	L
M		AD0	D-LDQS	AD4	AD8	AD10	D-UDQS	AD15		M
	1	2	3	4	5	6	7	8	9	

Top View - Ball Side Down

Legend:		Active Balls
		De-Populated Balls
		Reserved for Future Use
		Do Not Use

: not in use

9. PCB LAYOUT



LG-A165_MAIN_SPFY0236101-1.0_TOP

9. PCB LAYOUT

CN204(Camera connector)
- No Camera

IC200
- No USB
- No Music

U201
- No Charging

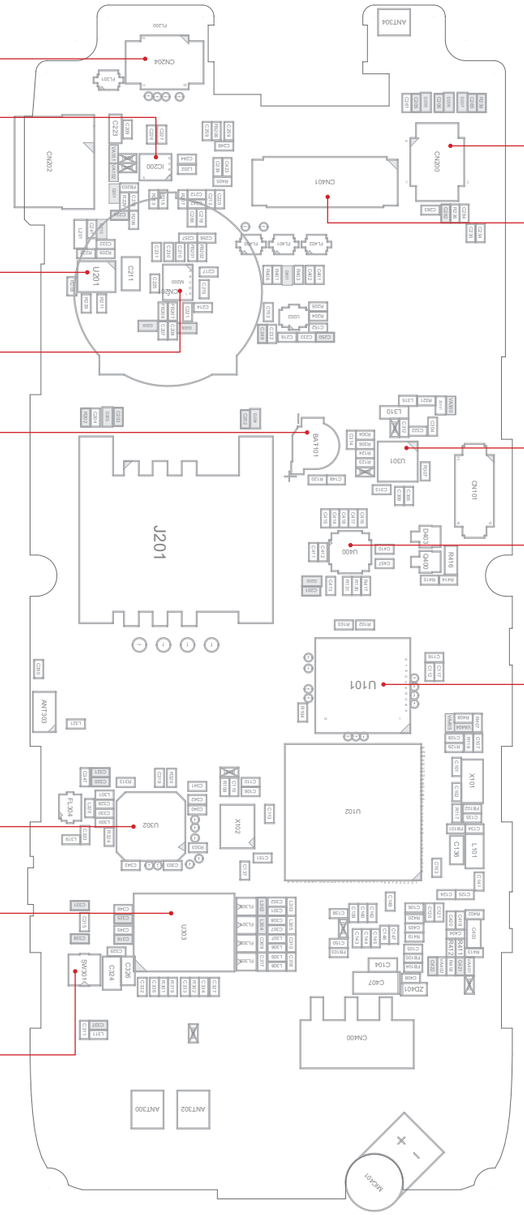
M200
- The Audio working bad

BAT101(Backup Battery)
- No service

U302
- The Bluetooth working bad

U303(TX Module)
- Can't make a call
- Tx Low power
- Not good BER
- No Service

SW301(mobile switch)
- Can't make a call
- Tx Low power
- Not good BER
- No Service



CN200
- No u-SD Memory
- No Receiver
- No Vibrator

CN401
- No LCD Display

U301
- The FM Radio working bad
  (in use intenna)

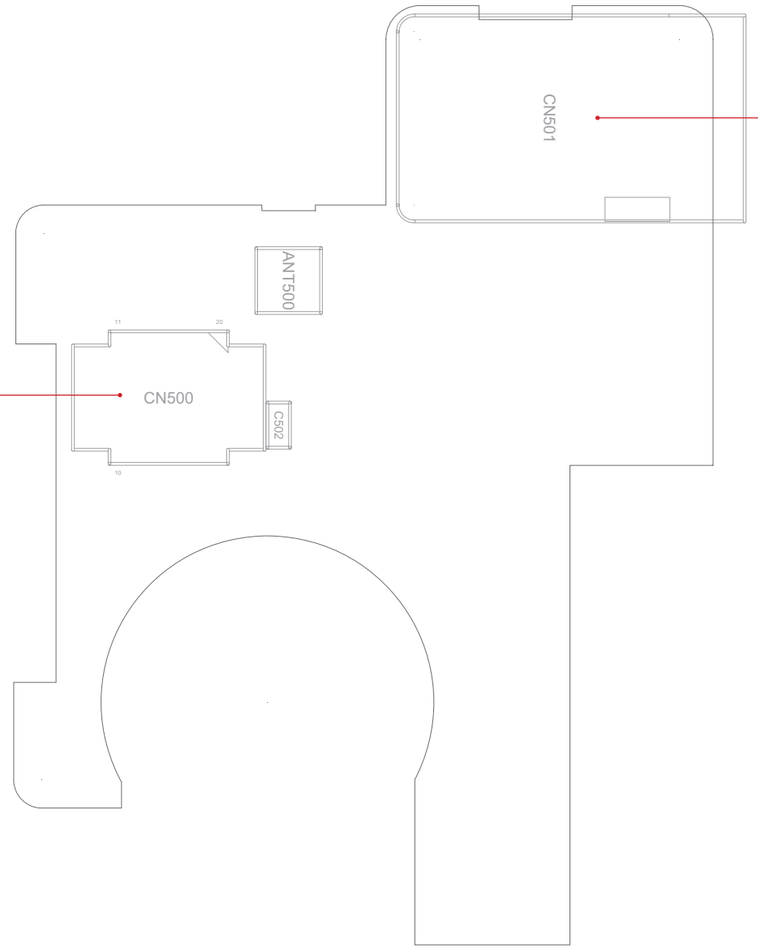
U400
- No LCD Back Light

U101(Memory)
- No booting

LG-A165_MAIN_SPFY0236101-1.0_BOT

9. PCB LAYOUT

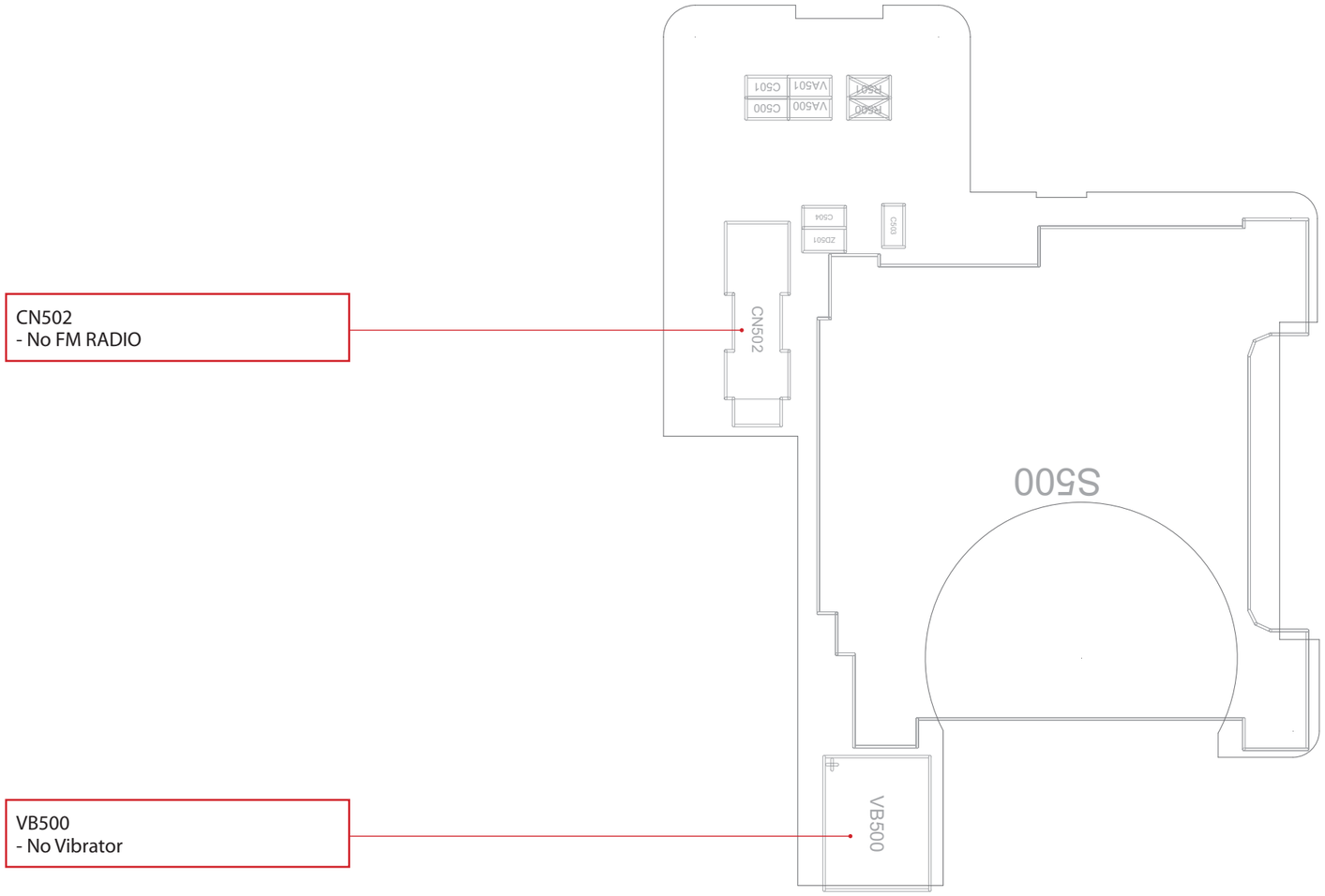
CN500
- No u-SD Memory
- No Receiver
- No Vibrator



CN501
- No Receiver

LG-A165_SUB_SPJY0086501-1.0_PLACE_TOP

9. PCB LAYOUT



LG-A165_SUB_SPJY0086501-1.0_PLACE_BOT

9. PCB LAYOUT

LG-A165_FPCB_SPCY0261001-1.0_PLACE_TOP

LG-A165_FPCB_SPCY0261001-1.0_PLACE_BOT

10.ENGINEERING MODE

Engineering mode is designed to allow a service man/engineer to view and test the basic functions provided by a handset. The key sequence for switching the engineering mode on is "1809#*165# "Select. Pressing END will switch back to non-engineering mode operation. Use Up and Down key to select a menu and press 'select' key to progress the test. Pressing 'back key will switch back to the original test menu.

- [1] Device test
  - [1-1] All auto
  - [1-2] Key press
  - [1-3] Sound
  - [1-4] Vibrator
  - [1-5] External memory
  - [1-6] SIM
  - [1-7] Camera
  - [1-8] Audio loopback
- [2] ELT mode
  - [2-1] Automatic
    - [2-1-1] 1Time
    - [2-1-2] 2Times
    - [2-1-3] 3Times
    - [2-1-4] 4Times
    - [2-1-5] 5Times
    - [2-1-6] 25Times
    - [2-1-7] 100Times
    - [2-1-8] Infinite Times
  - [2-2] Manual
    - [2-2-1] LCD backlight
    - [2-2-2] Ringtone
    - [2-2-3] Vibrator
    - [2-2-4] Camera
    - [2-2-5] Audio loopback
- [3] SW sanity test
  - [3-1] E serial NO
  - [3-2] UA string
  - [3-3] Unlock SIM
  - [3-4] DB check
- [4] Factory reset
- [5] Version
  - [5-1] Main SW
- [6] Usage info
  - [6-1] Call timer
- [7] ERS
  - [7-1] Client status
    - [7-1-1] Active
    - [7-1-2] Active + File save
    - [7-1-3] Inactive
    - [7-1-4] Inactive + File save
    - [7-1-5] Light mode
    - [7-1-6] Full mode
    - [7-1-7] Retry
  - [7-2] ERS test
    - [7-2-1] QM test
    - [7-2-2] Watch dog
    - [7-2-3] Divide by zero
    - [7-2-4] SWI
    - [7-2-5] Fatal
  - [7-3] Carrier setting

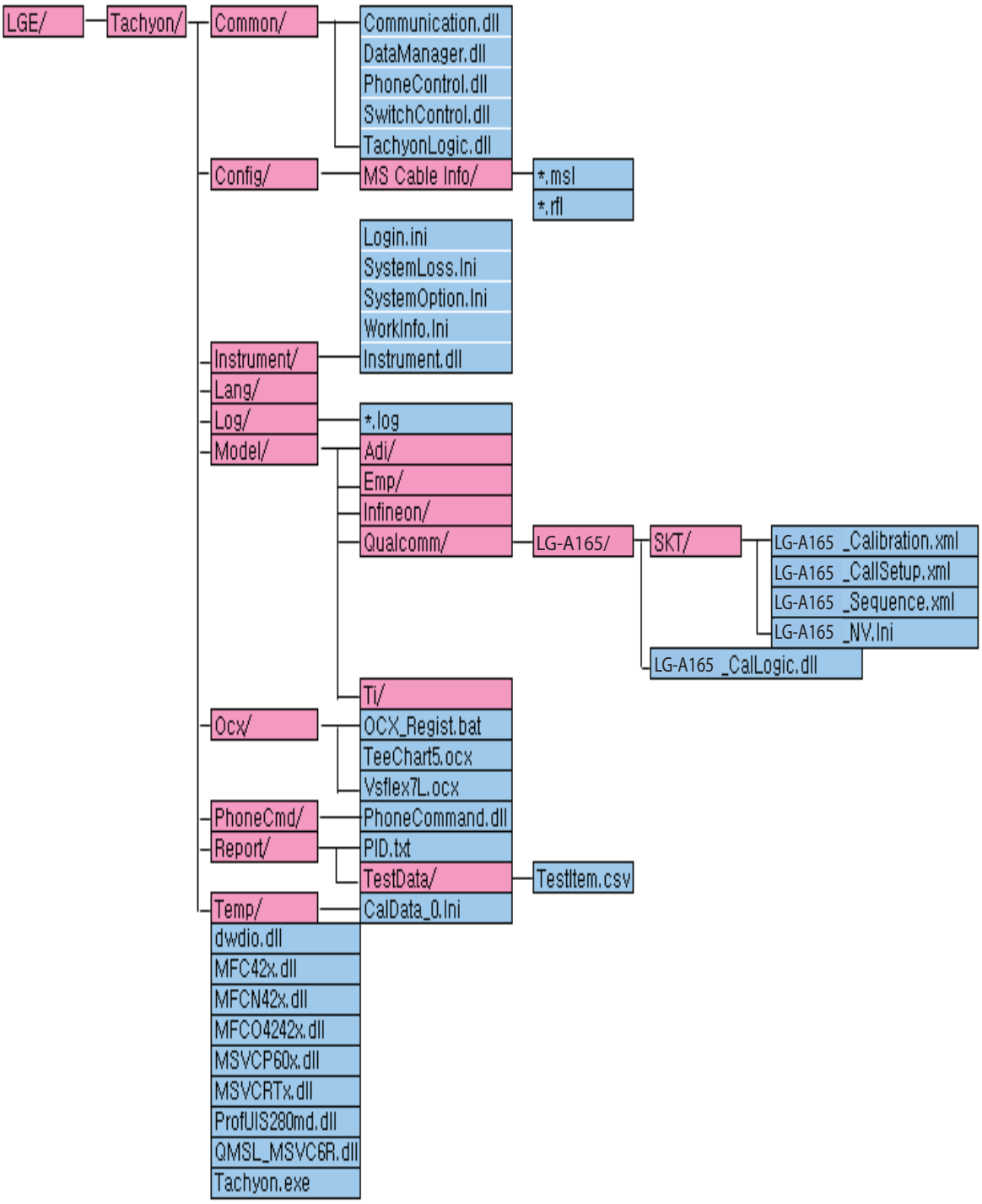
10.ENGINEERING MODE

- [8] Engineer mode
  - [8-1] FPRI test
  - [8-2] User pattern test
  - [8-3] PS
    - [8-3-1] Band selection
      - [8-3-1-1] SIM1
        - [8-3-1-1-1] Auto
        - [8-3-1-1-2] GSM850
        - [8-3-1-1-3] GSM900
        - [8-3-1-1-4] DCS1800
        - [8-3-1-1-5] PCS1900
      - [8-3-1-2] SIM2
        - [8-3-1-2-1] Auto
        - [8-3-1-2-2] GSM850
        - [8-3-1-2-3] GSM900
        - [8-3-1-2-4] DCS1800
        - [8-3-1-2-5] PCS1900
  - [8-4] MMS
  - [8-5] DRM
  - [8-6] RF(BER)
    - [8-6-1] Review
    - [8-6-2] LCD
    - [8-6-3] Vibrator
  - [8-7] Baseband
    - [8-7-1] Charging info
    - [8-7-2] Battery info
    - [8-7-3] LCD(Main)
  - [8-8] Audio tuning
  - [8-9] Bluetooth
    - [8-9-1] Set BT address
    - [8-9-2] BT Audio/RF test
      - [8-9-2-1] Audio test
      - [8-9-2-2] RF test
    - [8-9-3] Test menu
  - [8-10] Aging test
- [9] Wise debug
- [10] MTK debug
  - [10-1] Catcher
    - [10-1-1] Port
      - [10-1-1-1] NULL
      - [10-1-1-2] UART(microUSB)
      - [10-1-1-3] UART(Debug)
      - [10-1-1-4] UART(COM)
    - [10-1-2] Baudrate
      - [10-1-2-1] 921600
      - [10-1-2-2] 460800
      - [10-1-2-3] 115200
  - [10-2] Sleep mode
    - [10-2-1] Enable
    - [10-2-2] Disable
  - [10-3] DCM
    - [10-3-1] Enable
    - [10-3-2] Disable
  - [10-4] Memory dump
    - [10-4-1] Enable
    - [10-4-2] Disable
  - [10-5] Buffer monitor
    - [10-5-1] Disable
    - [10-5-2] All
    - [10-5-3] 8Bytes
    - [10-5-4] 16Bytes
    - [10-5-5] 32Bytes
    - [10-5-6] 64Bytes
    - [10-5-7] 128Bytes
    - [10-5-8] 256Bytes
    - [10-5-9] 512Bytes
    - [10-5-10] 1024Bytes
    - [10-5-11] 2048Bytes
  - [10-6] FS trace mode
    - [10-6-1] Disable
    - [10-6-2] Error
    - [10-6-3] API + Error
  - [10-7] Watch dog
    - [10-7-1] Enable
    - [10-7-2] Disable

11. RF CALIBRATION

11.1 Configuration of Tachyon

11.1.1 Configuration of directory



11.1.2 Description of basic folders

Folder	Description
Tachyon	Exe file and MFC dll, UI dll is present.
Common	Common dll files. (XML Data I/O , Auto Test Logic, Tachyon Logic Control, Communication)
Config	Envirement files. (Port configuration, Loss adjust)
Instrument	Tester control dll.
Model	Model files is present. (Model -> Solution (Qualcomm, EMP, ADI, INFINEON) -> MODEL NAME(LGGM630, LGSH470, ..) -> BUYER NAME(SKT, TEL, VIVO, …)
OCX	Conponent files.
PhoneCmd	Phone communication file
Report	Report Files is present. (Cal data, test data)

11.1.3 Description of configuration files

File	Description
'MODEL NAME'_Calibration.XML	There are imformations to calibrate. It consist of calibration items.
'MODEL NAME'_CallSetup.XML	There are imformations to call.
'MODEL NAME'_NV.INI	It consists of default values. It is written when 'cal&auto' is begun.
'MODEL NAME'_Sequence.XML	It is described a testing procedures.

11.2 How to use Tachyon

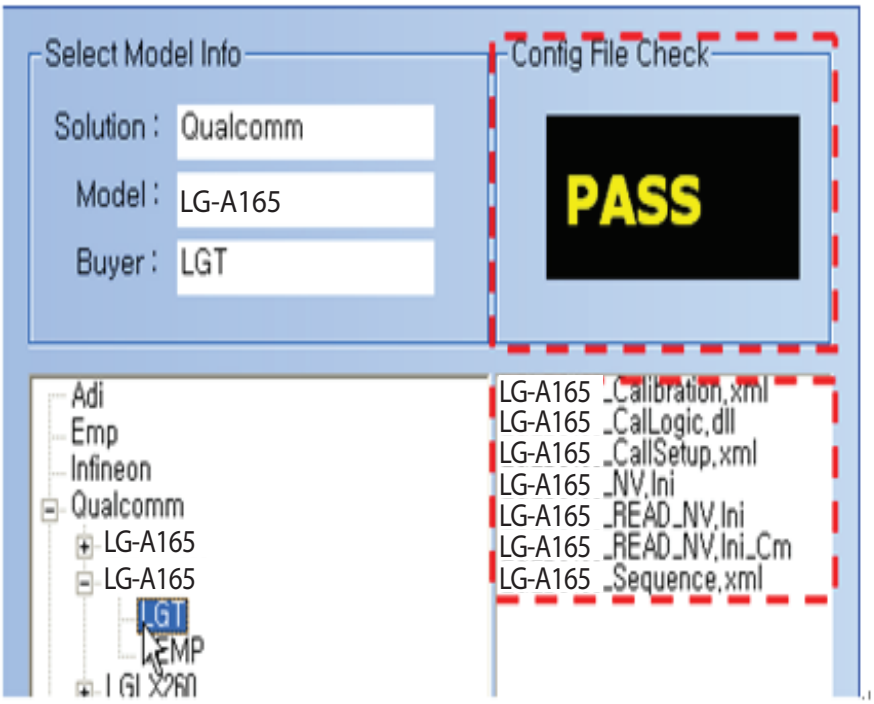
11.2.1 Model selection

Follow the procedure before start calibration & auto test

a. Click the icon,  in tool bar.

Then, You can make a choice of LG-A165 for loading cfg files before run.

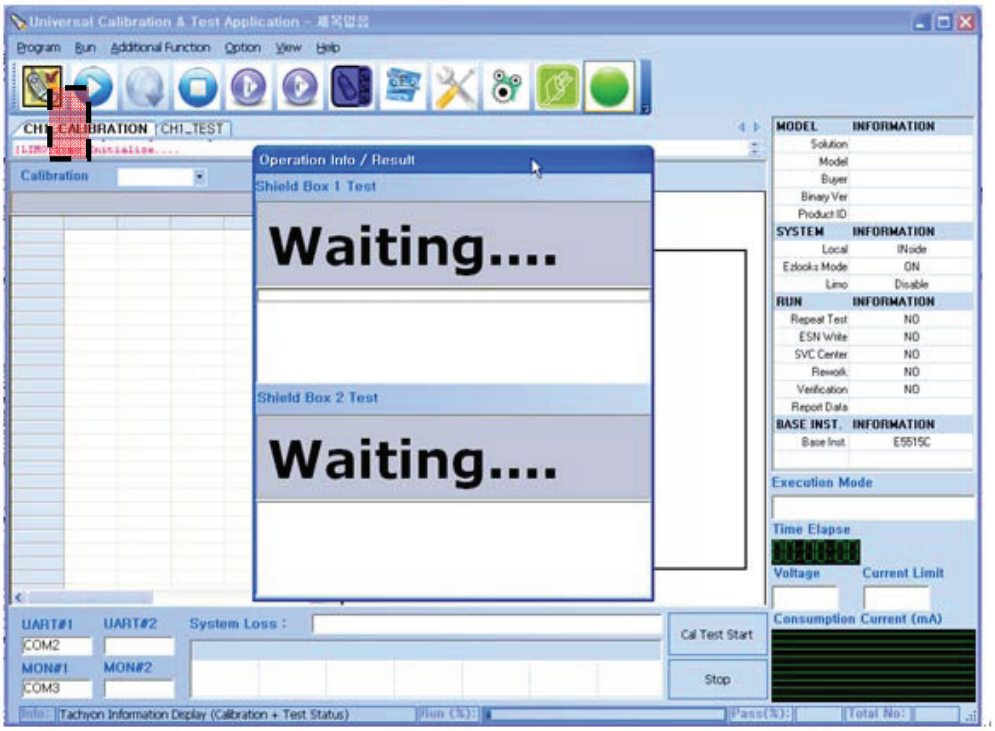
b. Select model name and then do double-click the buyer name.
You will see configuration files loaded in the right window with PASS information above



< Example of selection of model name>

11.2.2 Start cal & auto

a. Click calibration & autotest button,  in Tool bar

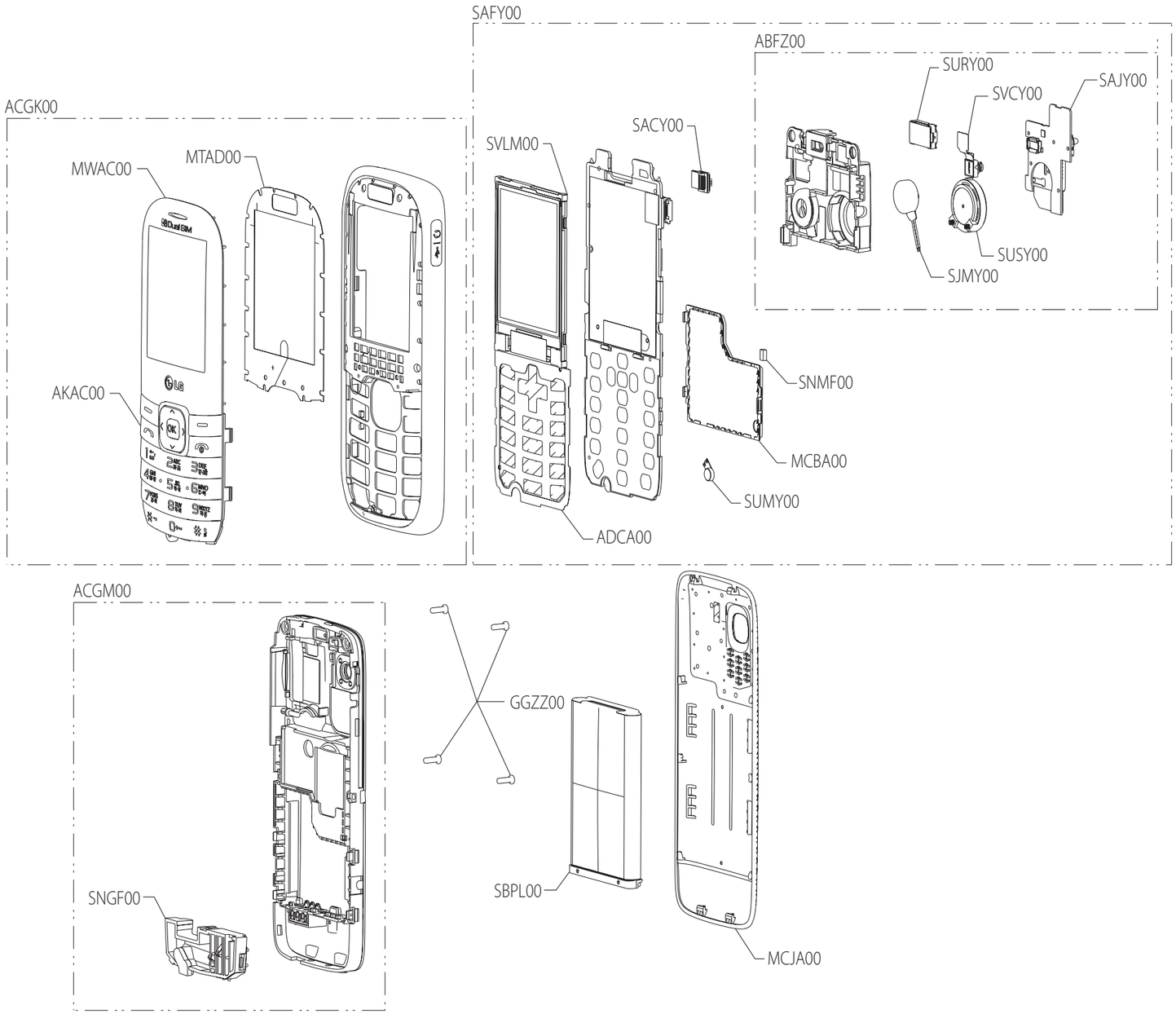


b. Calibration & autotest will be executed in order.

1) Precede Action.
   - NV write
   - Test command send.
2) RF Calibration
3) RF Auto test
4) After action
   - Phone reset
   - Change UE to AMSS

12. EXPLODED VIEW & REPLACEMENT PART LIST

12.1 EXPLODED VIEW



Location	Description
MCJA00	Cover,Battery
SBPL00	Mobile Phone Battery Li-Ion
ACGK00	COVER ASSY,FRONT
AKAC00	Keypad Assembly,Main
MTAD00	TAPE,WINDOW
MWAC00	Window,LCD
ACGM00	COVER ASSY,REAR
SNGF00	Antenna,Helical
GGZZ00	Screw,Tapping
SAFY00	PCB Assembly,Main
MCBA00	Can,Shield
SAJY00	PCB Assembly,Sub
SJMY00	Motor,DC
ABFZ00	BRACKET ASSY
SURY00	Receiver
SUSY00	Speaker Module
SVCY00	Camera Module
ADCA00	Dome Assembly,Metal
SUMY00	Microphone,Condenser
SVLM00	LCD Module
SACY00	PCB Assembly,Flexible
SNMF00	Antenna,Helical

12.2ReplacementParts <Mechanic component>

Note: ThisChapterisusedforreference,Partorderisordered bySBOMstandardonGCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
1	AAAY00	AdditionAssembly	AAAY0494301☞8	LG-A165INDKVZZ:WithoutColor-	
2	MCJA00	Cover,Battery	MCJA0119501	COMPLEXLG-A165INDKVZY:ColorUnfixedMOLD,PCLUPOYSC-1004A,	
2	MFL053800	Manual,Operation	MFL67000001	PRINTINGLGA165.JINDKVZZ:WithoutColor-	
1	APAY00	PackageAssembly	APAY0151402☞8	LG-A165INDKVZZ:WithoutColorLG-A165IND(TR1-1H/INDUB/6WD/Seal2/MRPLabel)	
2	APLY00	PalletAssembly	APLY0003209☞2	KS360ZAFBKZZ:WithoutColorTDRTR1-1PalletSleeve/6WDPallet	
3	MPBZ00	Damper	MPBZ0219601	COMPLEXKM500ROMBBZZ:WithoutColor-	
3	MPCY00	Pallet	MPCY0019330	COMPLEXKS360ZAFBKZZ:WithoutColor-	
2	MBAD00	Bag,Vinyl	MBAD0005204	COMPLEXLG-LX260SPRAGZZ:WithoutColor-	
2	MBEE00	Box,Master	MBEE0059801	COMPLEXKS360ACNRDZZ:WithoutColor-	
2	MBEF00	Box,Unit	MBEF0150202	COMPLEXLG-A165INDKVZZ:WithoutColorBOXTW,LG-A165IND(TR1-1H)	
2	MLAJ00	Label,MasterBox	MLAJ0004402	COMPLEXCG300CGRZZ:WithoutColorLABEL,MASTERBOX(forCGRTDR2VER.mbox_label)	
2	MLAP	Label,Unit	MLAP0001138	COMPLEXLG-RD6100RLCZZ:WithoutColor-	
2	MLAQ	Label,UnitBox	MLAQ0015213	COMPLEXKG270INDBKZZ:WithoutColorPRINTING,GSMMRPLABEL-MadebyLGE(100*48)	
2	MLAZ00	Label	MLAZ0050901	COMPLEXKU990GBRBKZZ:WithoutColor-	
1	APEY00	PhoneAssembly	APEY0949501☞2	LG-A165INDKVKV:BLACK_SILVERPOINT-	
2	ACGY00	CoverAssembly, EMS	ACGY0053101☞4	LG-A165INDKVZY:ColorUnfixed-	
3	ACGK00	CoverAssembly, Front	ACGK0170601☞11	LG-A165INDKVZY:ColorUnfixed-	
4	AKAC00	KeypadAssembly, Main	AKAC0018401	LG-A165INDKVZY:ColorUnfixed-	
4	MCCE00	Cap,Receptacle	MCCE0061401	COMPLEXLG-A165INDKVZY:ColorUnfixedMOLD,PCLUPOYSC-1004A,	
4	MCJK00	Cover,Front	MCJK0134601	COMPLEXLG-A165INDKVZY:ColorUnfixedMOLD,PCLUPOYSC-1004A,	
4	MDAY00	Decor	MDAY0084901	COMPLEXLG-A165INDKVZY:ColorUnfixedMOLD,PCLUPOYSC-1004A,	
4	MDJ000001	Filter	MDJ63024801	COMPLEXLGA165.AINDKVZY:ColorUnfixed-	
4	MFBZ00	Filter	MFBZ0025501	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
4	MPBG00	Damper,LCD	MPBG0113301	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAB00	Tape,Protect	MTAB0424301	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAD00	Tape,Window	MTAD0134101	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAZ0	Tape	MTAZ0363501	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MWAC00	Window,LCD	MWAC0151501	COMPLEXLG-A165INDKVZY:ColorUnfixedMOLD,PMMAHI835M,	
5	BFAA	Film,Inmold	BFAA0124501	LG-A165INDKV1.0,BLACK,	
3	ACGM00	CoverAssembly, Rear	ACGM0169501☞11	LG-A165INDKVZY:ColorUnfixed-	
4	MCCG00	Cap,MultimediaCard	MCCG0025801	COMPLEXLG-A165INDKVZY:ColorUnfixedMOLD,PCLUPOYSC-1004A,	
4	MCJN00	Cover,Rear	MCJN0126801	COMPLEXLG-A165INDKVZY:ColorUnfixedMOLD,PCLUPOYSC-1004A,	
4	MDAY00	Decor	MDAY0085001	COMPLEXLG-A165INDKVZY:ColorUnfixedMOLD,PCLUPOYSC-1004A,	
4	MFBZ00	Filter	MFBZ0025601	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MLAB	Label,AfterService	MLAB0004801	COMPLEXLG-LB3300LGTZZ:WithoutColor-	
4	MPBZ0	Damper	MPBZ0346901	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAZ00	Tape	MTAZ0345201	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAZ01	Tape	MTAZ0345301	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MWAE00	Window,Camera	MWAE0064801	COMPLEXLG-A165INDKVZY:ColorUnfixedCUTTING,PMMAMR200,	
3	GGZZ00	Screw,Tapping	GGZZ0005101	GGZZ0005101CH+-1.6mM4.5mMMSWRFZBSERVEONECO.,LTD.	
5	ABFZ00	BracketAssembly	ABFZ0025501☞13	LG-A165INDKVZY:ColorUnfixed-	
6	MBFZ00	Bracket	MBFZ0053701	COMPLEXLG-A165INDKVZY:ColorUnfixedMOLD,PCLUPOYSC-1004A,	
6	MCIZ00	Contact	MCIZ0006801	COMPLEXLG-A165INDKVZZ:WithoutColorPRESS,BeCu,	
6	MPBN00	Damper,Speaker	MPBN0091601	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
6	MPBT00	Damper,Camera	MPBT0099801	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
6	MPBZ00	Damper	MPBZ0323501	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	MPBZ02	Damper	MPBZ0325401	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
6	MTAK00	Tape,Camera	MTAK0042101	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
6	MTAZ00	Tape	MTAZ0345401	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
6	MTAZ01	Tape	MTAZ0345501	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
6	MTAZ02	Tape	MTAZ0345601	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
5	ADCA00	DomeAssembly, Metal	ADCA0117801	LG-A165INDKVZZ:WithoutColor-	
5	MBK070300	Can,Shield	MCBA0085801	COMPLEXLG-A165INDKVZZ:WithoutColorPRESS,STS,	
5	MEV000001	Insulator	MEV63651401	COMPLEXLGA165.AINDKVZY:ColorUnfixed-	
5	MIDZ00	Insulator	MIDZ0270401	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
5	MTAZ00	Tape	MTAZ0346601	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
5	MTAZ0	Tape	MTAZ0372901	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
7	MPBJ00	Damper,Motor	MPBJ0078401	COMPLEXLG-A165INDKVZZ:WithoutColorCOMPLEX,(empty),,,,,	
8	CN502	Contact	MCIZ0009501	COMPLEXLG-A165INDKVZZ:WithoutColorPRESS,BeCu,	
5	MEZ000000	Label	MLAZ0038301	COMPLEXLG-VX6000ZZ:WithoutColorPIDLabel4ArrayPRINTING,	
2	MEZ002100	Label,Approval	MLAA0062303	COMPLEXKB770DEUBKZZ:WithoutColor-	

12. EXPLODED VIEW & REPLACEMENT PART LIST

12.2ReplacementParts <Main component>

Note: ThisChapterisusedforreference,Partorderisordered bySBOMstandardonGCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
4	ENZY00	Connector, TerminalBlock	ENZY0015701	HSBC-3P-653P3.00MMSTRAIGHTSMDR/TP-HANSHINTERMINALCO.,LTD.	
4	SNGF00	Antenna,Helical	SNGF0063802	LS01-I-10V33-A03.0,-2dBd,LG-A165MainInternalGSM850+GSM900+DCS+PCS,QUAD,-2.0,50ohm,3.0LSMtronLtd.	
3	SAFY00	PCBAssembly,Main	SAFY0387501☞2	LG-A165INDKVMAING	
4	SAFB00	PCBAssembly,Main, Insert	SAFB0121801☞11	LG-A165MAING	
6	SURY00	Receiver	SURY0010118	EMR1207SPB2PASSY,dB,ohm,1207*2.5T,PIN,EM-TECH	
6	SUSY00	SpeakerModule	SUSY0024807	ISDR-1634-08C-01ASSY,8ohm,91dB,16mm,3.4Tspring,CONTACTGoerTekInc.	
6	SVCY00	CameraModule	SVCY0026401	HSIS-LM08SSFFHSIS-LM08SSFFVGA,Samsung(1/10"),5x5x2.5t,FPCB5mmHANSUNGELCOMTECCO.,LTD.	
5	SACY00	PCBAssembly, Flexible	SACY0124101	LG-A165INDKVFLEXIBLE1.0	
6	SACE00	PCBAssembly, Flexible,SMT	SACE0112001☞2	LG-A165INDKVFLEXIBLE1.0	
7	SACC00	PCBAssembly, Flexible,SMTBottom	SACC0084901	LG-A165INDKVFLEXIBLE1.0	
8	CN600, CN601	Connector,BtoB	ENBY0039501	GB042-20P-H10-E300020P0.40MMSTRAIGHTPLUGSMDR/TP1M-LSMtronLtd.	
7	SPCY00	PCB,Flexible	SPCY0261001	LG-A165INDKV,FLEXIBLE,C,POLYI,0.15mm,DOUBLE	
5	SAJY00	PCBAssembly,Sub	SAJY0052101☞2	LG-A165INDKVSUB,F	
6	SAJB00	PCBAssembly,Sub, Insert	SAJB0024201☞2	LG-A165INDKVSUB,B	
7	SJMY00	Motor,DC	SJMY0007104	3V80mA0A12KRPM0RPM0SEC0GF.CM0OHM	
6	SAJE00	PCBAssembly,Sub, SMT	SAJE0042601☞3	LG-A165INDKVSUB1.0	
7	SAJC00	PCBAssembly,Sub, SMTBottom	SAJC0041301☞7	LG-A165INDKVSUB1.1	
8	C500,C501	Capacitor,Ceramic, Chip	ECCH0000120	MCH155A390J39pF5%50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
8	C503	Capacitor,Ceramic, Chip	ECCH0017601	CL05A475MQ5NRNC4.7uF20%6.3VX5R-55TO+85C1005R/TP0.5MMSAMSUNGELECTRO-MECHANICSCO.,LTD.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
8	ZD501	Diode,TVS	EDTY0009601	Rclamp0521P.TCT5V65V4A100W-R/TP2P1SEMTECHCORPORATION	
8	S500	CardSocket	ENSY0022801	49619-161149619-1611,16,ANGLEmmHANKOOKMOLEX	
8	R500,R501	WirePad,Short	SAFP0000501	LG-VS760VRZ	
8	VA500, VA501	Varistor	SEVY0005201	EVLC5S020505.5V0%50F1.0*0.5*0.6-SMDR/TPAMOTECHCO.,LTD.	
7	SAJD00	PCBAssembly,Sub, SMTTop	SAJD0044201☞2	LG-A165INDKVSUB1.0	
8	C502	Capacitor,Ceramic, Chip	ECCH0004904	GRM155R60J105K1uF10%6.3VX5R-55TO+85C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
8	CN500	Connector,BtoB	ENBY0039601	GB042-20S-H10-E300020P0.4MMSTRAIGHTSOCKETSMDR/TP1M-LSMtronLtd.	
7	SPJY00	PCB,Sub	SPJY0086501	SPJY0086501FR-4MultiMULTI-2-LG-A165INDKV,SUB,D,FR-4mm,MULTI-2UNITECHPRINTEDCIRCUITBOARDCORP.	
5	SUMY00	Microphone, Condenser	SUMY0003815	B4010AL443-49-44DB2.2KOHMOMNI1.1TO10V4x1.0tFPCBGoerTekInc.	
5	SVLM00	LCDModule	SVLM0031401	GPM945A0GPM945A0,Main,2.0,176*220,37.5*53.4*1.9,262K,TFT,TM,ILI9225GIANTPLUSTECHNOLOGYCO.,LTD.	
4	SAFF00	PCBAssembly,Main, SMT	SAFF0287701☞4	LG-A165INDKVMAIN1.0	
5	SAFC00	PCBAssembly,Main, SMTBottom	SAFC0154301☞102	LG-A165INDKVMAIN1.0	
6	C327,C334	Capacitor,Ceramic, Chip	ECCH0000107	MCH155A060DK6pF0.25PF50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C307,C308	Capacitor,Ceramic, Chip	ECCH0000108	MCH155A070DK7pF0.25PF50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C241	Capacitor,Ceramic, Chip	ECCH0000110	MCH155A100D10pF0.25PF50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C101,C332, C333	Capacitor,Ceramic, Chip	ECCH0000115	MCH155A220JK22pF5%50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C102	Capacitor,Ceramic, Chip	ECCH0000117	CL05C270JB5NNNC27pF5%50VNP0-55TO+125C1005R/TP0.5SAMSUNGELECTRO-MECHANICSCO.,LTD.	
6	C213,C218, C220,C226, C227,C234, C235,C405, C408	Capacitor,Ceramic, Chip	ECCH0000120	MCH155A390J39pF5%50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C120,C121, C124,C125, C152,C153, C404	Capacitor,Ceramic, Chip	ECCH0000122	MCH155A470JK47pF5%50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C219,C256, C257,C264, C303,C304, C319	Capacitor,Ceramic, Chip	ECCH0000143	MCH155CN102KK1nF10%50VX7R-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C207,C208	Capacitor,Ceramic, Chip	ECCH0000149	MCH155CN332KK3.3nF10%50VX7R-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C312,C322	Capacitor,Ceramic, Chip	ECCH0000180	GRM1555C1H3R3C3.3pF0.25PF50VNP0-55TO+125C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C314,C342	Capacitor,Ceramic, Chip	ECCH0000182	GRM155R61A104K0.1uF10%10VX5R-55TO+85C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C150,C301, C302,C328, C330	Capacitor,Ceramic, Chip	ECCH0000185	GRM1555C1H5R6C5.6pF0.25PF50VNP0-55TO+125C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C210,C214, C239,C266	Capacitor,Ceramic, Chip	ECCH0000198	CL05A225MQ5NSNC2.2uF20%6.3VX5R-55TO+85C1005R/TP.SAMSUNGELECTRO-MECHANICSCO.,LTD.	
6	C222	Capacitor,Ceramic, Chip	ECCH0002001	C1005JB0J104KT000F0.1uF10%6.3VY5P-30TO+85C1005R/TP-TDKCORPORATION	
6	C112,C116, C134,C135, C215,C216, C217,C221, C230,C231, C232,C233, C244,C248, C258,C259, C305,C306, C313,C323, C340	Capacitor,Ceramic, Chip	ECCH0004904	GRM155R60J105K1uF10%6.3VX5R-55TO+85C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C104,C136, C326,C403	Capacitor,Ceramic, Chip	ECCH0005604	GRM188R60J106M10000000pF,6.3V,M,X5R,TC,1608,R/TP, 0.8mmMURATAMANUFACTURINGCO.,LTD.	
6	C341,C343, C410,C413, C423	Capacitor,Ceramic, Chip	ECCH0007804	CL05A225MP5NSNC2.2uF20%10VX5R-55TO+85C1005R/TP0.5MMSAMSUNGELECTRO-MECHANICSCO.,LTD.	
6	C103,C139, C225	Capacitor,Ceramic, Chip	ECCH0017601	CL05A475MQ5NRNC4.7uF20%6.3VX5R-55TO+85C1005R/TP0.5MMSAMSUNGELECTRO-MECHANICSCO.,LTD.	
6	C407	Capacitor,TA, Conformal	ECTH0002703	TCTAL1A107M8R0.0001F20%10V50UA-55TO+125C0OHM3.2x1.6x1.1NONESMDR/TPROHMCO.,LTD.	
6	C336	Capacitor,Ceramic, Chip	ECZH0000801	C1005C0G1H221JT000F220pF5%16VNP0-55TO+125C1005R/TP-TDKKOREACOOPERATION	
6	C310,C317, C318	Capacitor,Ceramic, Chip	ECZH0000802	C1005C0G1H010CT1pF0.25PF50VNP0-55TO+125C1005R/TP-TDKKOREACOOPERATION	
6	C350	Capacitor,Ceramic, Chip	ECZH0000803	C1005C0G1H020CT000F2pF0.25PF50VNP0-55TO+125C1005R/TP-TDKKOREACOOPERATION	
6	C347	Capacitor,Ceramic, Chip	ECZH0000813	C1005C0G1H101JT100pF5%50VNP0-55TO+125C1005R/TP-TDKKOREACOOPERATION	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C311	Capacitor,Ceramic, Chip	ECZH0000816	C1005C0G1H120JT000F12pF5%50VNP0-55TO+125C1005R/TP-TDKKOREACOOPERATION	
6	C309	Capacitor,Ceramic, Chip	ECZH0000822	C1005C0G1H1R5CT000F1.5pF0.25PF50VNP0-55TO+125C1005R/TP-TDKKOREACOOPERATION	
6	C209,C315, C329,C345, C346,C415, C416,C417, C418	Capacitor,Ceramic, Chip	ECZH0000830	C1005C0G1H330JT000F33pF5%50VNP0-55TO+125C1005R/TP-TDKKOREACOOPERATION	
6	C105,C113, C137,C138, C140,C141, C142,C143, C144,C145, C146,C147, C149,C151, C204,C261, C263,C401, C402,C411, C412,C414, C457	Capacitor,Ceramic, Chip	ECZH0001215	C1005X5R1A105KT000F1uF10%10VX5R-55TO+85C1005R/TP-TDKKOREACOOPERATION	
6	C117,C148, C212,C242, C419,C420	Capacitor,Ceramic, Chip	ECZH0003103	GRM36X7R104K10PT100nF10%10VX7R-55TO+125C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C223	Capacitor,Ceramic, Chip	ECZH0003503	GRM188R61E105K1uF10%25VX5R-55TO+85C1608R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C106,C107, C108,C109, C110,C115	Capacitor,Ceramic, Chip	ECZH0004402	MCH153C104ZK0.1uF10%16VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	ZD401	Diode,Zener	EDNY0013602	EDZTE615.1BEDZTE615.1B,EMD2,5.1V,150mW,R/TP,ROHMSemiconductorKOREACORPORATION	
6	D403	Diode,Switching	EDSY0014001	KDS221E-RTK1.1V20V200mA300mA0SEC100mWESMR/TP3P2KECCORPORAITION	
6	ZD301	Diode,TVS	EDTY0009601	Rclamp0521P.TCT5V65V4A100W-R/TP2P1SEMTECHCORPORATION	
6	L300,L301	Inductor,Multilayer, Chip	ELCH0001048	1005GC2T10NJLF10NH5%0V250mA0.42OHM2.5GHZ8NONSHIELD11.0X0.5X0.5MMR/TPPILKORELECTRONICSLTD.	
6	L311,L320	Inductor,Multilayer, Chip	ELCH0001049	1005GC2T6N8JLF6.8NH5%0V250mA0.32OHM3GHZ8NONSHIELD11.0X0.5X0.5MMR/TPPILKORELECTRONICSLTD.	
6	L303	Inductor,Multilayer, Chip	ELCH0001052	1005GC2T18NJLF18NH5%0V200mA0.65OHM1.6GHZ8NONSHIELD11.0X0.5X0.5MMR/TPPILKORELECTRONICSLTD.	
6	L305	Inductor,Multilayer, Chip	ELCH0001401	LL1005-FHL15NJ_15NH5%0V300mA0.5OHM2.5GHZ9NONSHIELD11.0X0.5X0.5MMR/TPTOKO,INC.	
6	L321	Inductor,Multilayer, Chip	ELCH0001411	LL1005-FHL1N2S1.2NH0.3NH0V500mA0.1OHM16GHZ8NONSHIELD11.0X0.5X0.5MMR/TPTOKO,INC.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	L319	Inductor,Multilayer, Chip	ELCH0001413	LL1005-FHL22NJ22NH5%0V300mA0.7OHM2.1GHZ10NONSHIELD 11.0X0.5X0.5MMR/TPTOKO,INC.	
6	L201	Inductor,Multilayer, Chip	ELCH0001556	LL1608-FSLR27JLL1608-FSR27J,270nH,J,1608,R/TP,TOKO,INC.	
6	L306,L307, L308,L309	Inductor,Multilayer, Chip	ELCH0003828	LQG15HS2N4S02D2.4NH0.3NH0V300mA0.15OHM6GHZ8NONSHIELD11X0.5X0.5MMR/TPMURATAMANUFACTURINGCO.,LTD.	
6	L202	Inductor,Multilayer, Chip	ELCH0012501	LQW15AN27NG00D27NH2%0V280mA0.52OHM3.5GHZ25NONSHIELD11.0X0.5X0.5MMR/TPMURATAMANUFACTURINGCO.,LTD.	
6	L315	Inductor,Multilayer, Chip	ELCH0012502	LQW15AN10NG00D10NH2%-500mA0.17OHM5.5KHZ-NONSHIELD11.0X0.5X0.55MMR/TPMURATAMANUFACTURINGCO.,LTD.	
6	L310	Inductor,Multilayer, Chip	ELCH0025601	LQW18AN39NG039NH2%-400mA0.26OHM2.8GHZ-NONSHIELD01.6X0.8X0.8MMR/TPMURATAMANUFACTURINGCO.,LTD.	
6	L101	Inductor,WireWound,Chip	ELCP0008017	CIG21L2R2MNE2.2UH30%-1.3A0.08OHM--SHIELD2X1.25X1MMNONE-SAMSUNGELECTRO-MECHANICSCO.,LTD.	
6	CN101	Connector,BtoB	ENBY0029001	AXT43016430P0.40MMSTRAIGHTHEADERSMDR/TP1.5M-PanasonicCorporation	
6	CN200, CN204	Connector,BtoB	ENBY0039601	GB042-20S-H10-E300020P0.4MMSTRAIGHTSOCKETSMDR/TP1M-LSMtronLtd.	
6	CN401	Connector,FFC/FPC/PIC	ENQY0014901	GF032-35S-E200035P0.30MMFPCSTRAIGHTBOTHSMDR/TPLOCKING-LSMtronLtd.	
6	CN202	connector,I/O	ENRY0008801	GU073-5P-SD-E1500GU073-5P-SD-E1500,5,mm,ANGLELSMtronLtd.	
6	J201	CardSocket	ENSY0025101	GCA26D-6S-H18-E1500SIM6PANGLESMDR/TP-LSMtronLtd.	
6	SW301	Connector,RF	ENWY0008701	MS-156CNONESTRAIGHTSOCKETSMDT/REELAU50OHM400mDBHIROSEKOREACO.,LTD	
6	Q400	TR,Bipolar	EQBN0007101	2SC5585NPN6V15V12V500mA100mA680150mWEMT3R/TP3PROHM.	
6	R108	Resistor,Chip	ERHY0000105	MCR01MZP5F51R051OHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R313	Resistor,Chip	ERHY0000128	MCR01MZP5F150215KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R301	Resistor,Chip	ERHY0000129	MCR01MZP5F180218KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R209	Resistor,Chip	ERHY0000185	MCR01MZP5F8200820OHM1%1/16W1005R/TP-ROHM.	
6	R302,R402, R414	Resistor,Chip	ERHY0000241	MCR01MZP5J1021KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R206,R411, R412	Resistor,Chip	ERHY0003301	MCR01MZP5J101100OHM5%1/16W1005R/TP-ROHM.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	R415,R417, R420	Resistor,Chip	ERHZ0000204	MCR01MZP5F1003100KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R229	Resistor,Chip	ERHZ0000243	MCR01MZP5F22012.2KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R208	Resistor,Chip	ERHZ0000264	MCR01MZP5F30013000ohm,1/16W,F,1005,R/TPROHMSemiconductorKOREACORPORATION	
6	R117	Resistor,Chip	ERHZ0000294	MCR01MZP5F51015.1KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R320	Resistor,Chip	ERHZ0000295	MCR01MZP5F510251KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R204	Resistor,Chip	ERHZ0000404	MCR01MZP5J1021KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R239,R306, R319	Resistor,Chip	ERHZ0000405	MCR01MZP5J10310KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R102,R103, R104,R119, R129,R205, R211,R222, R236,R303, R304,R307, R324,R401, R403,R405, R406	Resistor,Chip	ERHZ0000406	MCR01MZP5J104100KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R321	Resistor,Chip	ERHZ0000434	MCR01MZP5J1R01OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R123,R124, R130,R131, R207,R215, R413,R418	Resistor,Chip	ERHZ0000443	MCR01MZP5J2222.2KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R213	Resistor,Chip	ERHZ0000486	MCR01MZP5J47347KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R407,R408	Resistor,Chip	ERHZ0000488	MCR01MZP5J4R74.7OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R120	Resistor,Chip	ERHZ0000499	MCR01MZP5J5625.6KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R419	Resistor,Chip	ERHZ0000537	MCR01MZP5F6803680KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R416	Resistor,Chip	ERHZ0000702	MCR03EZP5J10010OHM5%1/10W1608R/TP-ROHMSemiconductorKOREACORPORATION	
6	U400	IC,ChargePump	EUSY0344402	RT9367CQFN,20,R/TP,4CH,2LDO,3X3,IC,SubPMICIC,SubPMICRICHTEKTECHNOLOGYCORP.	
6	U202	IC,AnalogSwitch	EUSY0347001	DG2735DN-T1-E4MiniQFN-10L,10PIN,R/TP,1.8X1.4X0.55,0.6DualSPDTAnalogSwitch,;,IC,AnalogSwitchVISHAYINTERTECHNOLOGYASIAPTELTD	
6	U101	IC,MCP,NOR	EUSY0368505	PF38F4050M0Y3DENOR/256MBIT+PSRAM/64MBIT1.7VTO1.9V8 8 1.0TR56P---NumonyxAsiaPacificPteLtd.	
6	U302	IC,Bluetooth	EUSY0395001	MT66123VTO4.8V108.9mWQFNR/TP40P-MEDIATEKINC.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	U102	IC,DigitalSignalProcessors	EUSY0409701	MT6253000NONENONEBGAR/TP263P-MEDIATEKSINGAPOREPTE.LTD.	
6	U201	IC,VoltageReference	EUSY0410801	RT9524DFN,10,R/TP,DFNCalTestModeSingleChargerICforMicroUSB,IC,ChargerIC,ChargerRICHTEKTECHNOLOGYCORP.	
6	M200	IC,AudioSubSystem	EUSY0420001	TPA2055D31.6~5.5V0WWLCSPR/TP20P-TEXASINSTRUMENTSINCO.	
6	U301	IC,Tuner	EUSY0430601	SI4704-D50-GMRQFN,20,R/TP,FMTuner(NoRDS),InternalFMAnt,3*3*0.6,110nm,0.5p,;,IC,TunerSILICONLABORATORIES	
6	IC200	IC,AnalogSwitch	EUSY0434001	RT8968WSCWLCSP,20,R/TP,WLCSP,20,R/TP,MUIC-Basic,;,IC,AnalogSwitchRICHTEKTECHNOLOGYCORP.	
6	X101	Crystal	EXXY0018701	FC-135(12.5PF,+-20PPM)32.768KHZ20PPM12.5PF32*15SMDR/TPSEIKOEPSONCORP	
6	X102	Crystal	EXXY0027401	X1E00002104340026MHZ10PPM0FNONESMDR/TPEPSONTOYOCOMCORP	
6	R101,R125,R201,R203,R305,R308,R309,R410	WirePad,Short	SAFP0000501	LG-VS760VRZ	
6	VA401,VA402	Varistor	SEVY0005402	ICVS0505500FR5.6V0%50F1.0*0.5*0.55-SMDR/TPINNOCHIPSTECHNOLOGY	
6	FB206	Filter,Bead	SFBH0000909	HB-1M1005-600JT60ohm1.0*0.5*0.5SMDR/TP2PCERATECHCORPORATION	
6	FB203	Filter,Bead	SFBH0007101	BLM15AG121PN1120ohm1.0x0.5x0.55SMDR/TP2PMURATAMANUFACTURINGCO.,LTD.	
6	FB103	Filter,Bead	SFBH0007103	BLM15BB750SN1J75ohm1.0x0.5x0.55SMDR/TP2PMURATAMANUFACTURINGCO.,LTD.	
6	FB105,FB207,FB208	Filter,Bead	SFBH0008101	BLM15AG601SN1600ohm1.0x0.5x0.55SMDR/TP2PMURATAMANUFACTURINGCO.,LTD.	
6	FB104	Filter,Bead	SFBH0008103	BLM15BD102SN110001.0x0.5x0.5MMSMDR/TP2PMURATAMANUFACTURINGCO.,LTD.	
6	FB101,FB102,FB201,FB202	Filter,Bead	SFBH0008105	BLM15BD182SN1D1800ohm;1.0x0.5x0.55SMDR/TP2PMURATAMANUFACTURINGCO.,LTD.	
6	FL304	Filter,Dielectric	SFDY0002601	LFB212G45BA1A220BPF2.45KHZ100SMDR/TP-MURATAMANUFACTURINGCO.,LTD.	
6	FL400,FL401,FL402	Filter,EMI/Power	SFEY0010501	ICVE10184E150R101FRESD/EMI0HZ15pF0HSMDR/TPINNOCHIPSTECHNOLOGY	
6	FL200,FL201	Filter,EMI/Power	SFEY0011601	ICVE10184E150R500FRESD/EMI0HZ15pF0HSMDR/TPINNOCHIPSTECHNOLOGY	
6	FL301	Filter,Saw	SFSY0024301	SAFEB942MFL0F00942.51.4*1.1*0.6SMDR/TP5PMURATAMANUFACTURINGCO.,LTD.	

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	FL302	Filter,Saw	SFSY0024302	SAFEB1G84FA0F001842.51.4*1.1*0.6SMDR/TP5PMURATA MANUFACTURINGCO.,LTD.	
6	FL303	Filter,Saw	SFSY0024303	SAFEB1G96FA0F0019601.4*1.1*0.6SMDR/TP5PMURATAM ANUFACTURINGCO.,LTD.	
6	FL305	Filter,Saw	SFSY0030003	SAFEB881MFL0F55881.5MHz1.4*1.1*0.6SMDR/TP5PMUR ATAMANUFACTURINGCO.,LTD.	
6	U303	RFModule	SMRH0005601	SKY77547MHz,MHz,GSMQuadTxModule6x8,SKYWORKSSO LUTIONSINC.	
6	BAT101	Module,Assembly	SMZY0026701	EECEP0F333YDGM750SFRTNBackupCapacitor,0.03F,3.8pi, ModuleAssemblyPANASONICINDUSTRIALKOREACO.,LTD	
6	ANT303	Antenna,Helical	SNMF0051501	SDBTPTR3015SINGLE-5DB50OHM5PARTRONCOMPANYLIMITED	
5	SAFD00	PCBAssembly,Main, SMTTop	SAFD0152001☞2	LG-A165INDKVMAIN1.0	
6	LD400, LD401	LED,Chip	EDLH0013401	SWAA07WHITE3.0~3.220mA1200~1400mcd0.285~0.31120 mW1005R/TP2P-SEOULSEMICONDUCTORCO.,LTD	
6	SPFY	PCB,Main	SPFY0236101	SPFY0236101FR-4MultiMULTI-60.8LG-A165INDKV,MAIN,D,FR-4,0.8mm,MULTI-6UNITECHPRINTEDCIRCUITBOARDCORP.	

12. EXPLODED VIEW & REPLACEMENT PART LIST

12.3 Accessory

Note: ThisChapterisusedforreference,Partorderisordered bySBOMstandardonGCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
2	SBPL00	MobilePhone BatteryLi-Ion	SBPL0090501	KU250-553450-LGC-EUKU250-553450-LGC-EU,3.7V,950mAh,1CELL,PRISMATIC,KU250EuropeBATT,IP,Pb-FreeLGCHEMICAL	
2	SGEY00	Earphone,Stereo	SGEY0003218	EMB-LGE011STKC3mW16OHM115DB85HZTO126HZ1MBLACK5PIN5CRESYNCO.,LTD	
2	SSAD00	Adapters	SSAD0032601	STA-U34IDSTA-U34ID,100-240V,5060Hz,5.1V,0.7A,CE,AC-DCADAPTORDONGDOELECTRONICSCO.,LTD	
2	SSAD00	Adapters	*S*SSAD0032604	STA-U34IV150Vac~350Vac5.1V700mA5060CENONENONE-PowerSystemsTechnologiesFarEastLtd	
2	SSAD00	Adapters	*S*SSAD0032602	STA-U34IR100-240V,5060Hz,5.1V,0.7A,CE,AC-DCADAPTOR,150Vac~350Vac,4.75Vdc~5.25Vdc,700mA,5060,WALL2P,USB,150Vac~350Vac,4.75Vdc~5.25Vdc,700mA,5060,WALL2P,USB,SUNLINELECTRONICSCO.,LTD	
2	SSAD00	Adapters	*S*SSAD0032603	STA-U34IS100-240V,5060Hz,5.1V,0.7A,CE,AC-DCADAPTOR,150Vac~350Vac,4.75Vdc~5.25Vdc,700mA,5060,WALL2P,USB,150Vac~350Vac,4.75Vdc~5.25Vdc,700mA,5060,WALL2P,USB,SALCOMPOY	