Internal Use Only

Service Manual

LG-A230

Date: May, 2011 / Issue 1.0

Table Of Contents

1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.
The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc.Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated  **by the sign. Following information is ESD handling:**

- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current – Constant Voltage
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milli watt
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIB	General Purpose Interface Bus
GSM	Global System for Mobile Communications
IPUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop

PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
PSRAM	Pseudo SRAM
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. PERFORMANCE

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Lithium-Ion, 3.7V 950mAh	
Stand by TIME	Up to 605 hrs : Paging Period 5, RSSI 85dBm	
Talk time	Up to 200min : GSM Tx Level 7	
Stand by time	Up to 389 hours (Paging Period: 5, RSSI: -85 dBm)	
Charging time	Approx. 3 hours	
RX Sensitivity	GSM, EGSM: -109dBm, DCS: -109dBm	
TX output power	GSM, EGSM: 32.3dBm(Level 5), DCS , PCS: 29.5dBm(Level 0)	
GPRS compatibility	Class 10	
SIM card type	3V / 1.8V	
Display	MAIN : 1.77" QVGA 160 × 128 pixel	
Status Indicator	Send Key, End Key, Navi Key (Up,Down,Left,Right)	
ANT	Internal	
EAR Phone Jack	Yes	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR	
Data and Fax	Yes	
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	
Microphone	Yes	
Speaker/Receiver	18x12Φ Speaker/ Receiver	
Travel Adapter	Yes	
MIDI	SW MIDI (Mono SPK)	
Camera	1.3M FF	
Bluetooth / FM Radio	Bluetooth version 2.1 / 76~108MHz supported	

2.2 Technical Specification

<table>
<tr><th>Item</th><th>Description</th><th>Specification</th></tr>
<tr><td>1</td><td>Frequency Band</td><td>GSM850
TX: 824 ~ 849 MHz
RX: 869 ~ 894 MHz
EGSM
TX: 880 ~ 915MHz
RX: 925 ~ 960 MHz
DCS
TX: 1710 ~ 1785 MHz
RX: 1805 ~ 1880 MHz
PCS
TX: 1850 ~ 1910 MHz
RX: 1930 ~ 1990 MHz</td></tr>
<tr><td>2</td><td>Phase Error</td><td>RMS < 5 degrees
Peak < 20 degrees</td></tr>
<tr><td>3</td><td>Frequency Error</td><td>< 0.1 ppm</td></tr>
<tr><td>4</td><td>Power Level</td><td>
GSM850/EGSM
<table>
<tr><th>Level</th><th>Power</th><th>Toler.</th><th>Level</th><th>Power</th><th>Toler.</th></tr>
<tr><td>5</td><td>33dBm</td><td>±2dB</td><td>13</td><td>17dBm</td><td>± 3dB</td></tr>
<tr><td>6</td><td>31dBm</td><td>±3dB</td><td>14</td><td>15dBm</td><td>± 3dB</td></tr>
<tr><td>7</td><td>29dBm</td><td>±3dB</td><td>15</td><td>13dBm</td><td>± 3dB</td></tr>
<tr><td>8</td><td>27dBm</td><td>±3dB</td><td>16</td><td>11dBm</td><td>± 5dB</td></tr>
<tr><td>9</td><td>25dBm</td><td>±3dB</td><td>17</td><td>9dBm</td><td>± 5dB</td></tr>
<tr><td>10</td><td>23dBm</td><td>±3dB</td><td>18</td><td>7dBm</td><td>± 5dB</td></tr>
<tr><td>11</td><td>21dBm</td><td>±3dB</td><td>19</td><td>5dBm</td><td>± 5dB</td></tr>
<tr><td>12</td><td>19dBm</td><td>±3dB</td><td></td><td></td><td></td></tr>
</table>
DCS/PCS
<table>
<tr><th>Level</th><th>Power</th><th>Toler.</th><th>Level</th><th>Power</th><th>Toler.</th></tr>
<tr><td>0</td><td>30dBm</td><td>±2dB</td><td>8</td><td>14dBm</td><td>± 3dB</td></tr>
<tr><td>1</td><td>28dBm</td><td>±3dB</td><td>9</td><td>12dBm</td><td>± 4dB</td></tr>
<tr><td>2</td><td>26dBm</td><td>±3dB</td><td>10</td><td>10dBm</td><td>± 4dB</td></tr>
<tr><td>3</td><td>24dBm</td><td>±3dB</td><td>11</td><td>8dBm</td><td>± 4dB</td></tr>
<tr><td>4</td><td>22dBm</td><td>±3dB</td><td>12</td><td>6dBm</td><td>± 4dB</td></tr>
<tr><td>5</td><td>20dBm</td><td>±3dB</td><td>13</td><td>4dBm</td><td>± 4dB</td></tr>
<tr><td>6</td><td>18dBm</td><td>±3dB</td><td>14</td><td>2dBm</td><td>± 5dB</td></tr>
<tr><td>7</td><td>16dBm</td><td>±3dB</td><td>15</td><td>0dBm</td><td>± 5dB</td></tr>
</table>
</td></tr>
</table>

Item	Description	Specification	
5	Output RF Spectrum (due to modulation)	**GSM850/ EGSM**	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-63
		3,000~ <6,000	-65
		6,000	-71
		DCS/PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-65
		3,000~ <6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	**GSM850/ EGSM**	
		Offset from Carrier (kHz).	Max. dBm
		400	-19
		600	-21
		1,200	-21
		1,800	-24

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td rowspan="6">6</td><td rowspan="6">Output RF Spectrum
(due to switching
transient)</td><td colspan="3">DCS/PCS</td></tr>
<tr><td colspan="2">Offset from Carrier (kHz).</td><td>Max. dBm</td></tr>
<tr><td colspan="2">400</td><td>-22</td></tr>
<tr><td colspan="2">600</td><td>-24</td></tr>
<tr><td colspan="2">1,200</td><td>-24</td></tr>
<tr><td colspan="2">1,800</td><td>-27</td></tr>
<tr><td>7</td><td>Spurious Emissions</td><td colspan="3">Conduction, Emission Status</td></tr>
<tr><td>8</td><td>Bit Error Ratio</td><td colspan="3">GSM850, EGSM
BER (Class II) < 2.439% @-102 dBm
DCS,PCS
BER (Class II) < 2.439% @-100 dBm</td></tr>
<tr><td>9</td><td>RX Level Report Accuracy</td><td colspan="3">±3 dB</td></tr>
<tr><td>10</td><td>SLR</td><td colspan="3">12±3 dB</td></tr>
<tr><td rowspan="10">11</td><td rowspan="10">Sending Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>-</td></tr>
<tr><td>200</td><td>0</td><td>-</td></tr>
<tr><td>300</td><td>0</td><td>-12</td></tr>
<tr><td>1,000</td><td>0</td><td>-6</td></tr>
<tr><td>2,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,000</td><td>4</td><td>-6</td></tr>
<tr><td>3,400</td><td>4</td><td>-9</td></tr>
<tr><td>4,000</td><td>0</td><td>-</td></tr>
<tr><td>12</td><td>RLR</td><td colspan="3">4±3 dB</td></tr>
</table>

<table>
<tr><th>Item</th><th>Description</th><th colspan="3">Specification</th></tr>
<tr><td rowspan="11">13</td><td rowspan="11">Receiving Response</td><td>Frequency (Hz)</td><td>Max.(dB)</td><td>Min.(dB)</td></tr>
<tr><td>100</td><td>-12</td><td>-</td></tr>
<tr><td>200</td><td>0</td><td>-</td></tr>
<tr><td>300</td><td>2</td><td>-7</td></tr>
<tr><td>500</td><td>*</td><td>-5</td></tr>
<tr><td>1,000</td><td>0</td><td>-5</td></tr>
<tr><td>3,000</td><td>2</td><td>-5</td></tr>
<tr><td>3,400</td><td>2</td><td>-10</td></tr>
<tr><td>4,000</td><td>2</td><td></td></tr>
<tr><td colspan="3">* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.</td></tr>
<tr><td>14</td><td>STMR</td><td colspan="3">> 17 dB</td></tr>
<tr><td>15</td><td>Stability Margin</td><td colspan="3">> 6 dB</td></tr>
<tr><td rowspan="9">16</td><td rowspan="9">Distortion</td><td colspan="2">dB to ARL (dB)</td><td>Level Ratio (dB)</td></tr>
<tr><td colspan="2">-35</td><td>17.5</td></tr>
<tr><td colspan="2">-30</td><td>22.5</td></tr>
<tr><td colspan="2">-20</td><td>30.7</td></tr>
<tr><td colspan="2">-10</td><td>33.3</td></tr>
<tr><td colspan="2">0</td><td>33.7</td></tr>
<tr><td colspan="2">7</td><td>31.7</td></tr>
<tr><td colspan="2">10</td><td>25.5</td></tr>
<tr><td>17</td><td>Side Tone Distortion</td><td colspan="3">Three stage distortion < 10%</td></tr>
<tr><td>18</td><td>System frequency (13 MHz) tolerance</td><td colspan="3">≤ 2.5 ppm</td></tr>
<tr><td>19</td><td>32.768KHz tolerance</td><td colspan="3">≤ 30 ppm</td></tr>
<tr><td>20</td><td>Ringer Volume</td><td colspan="3">At least 55 dBspl under below conditions:
1. Ringer set as ringer.
2. Test distance set as 1 m</td></tr>
</table>

<table>
<tr><th>Item</th><th>Description</th><th colspan="2">Specification</th></tr>
<tr><td>21</td><td>Charge Current</td><td colspan="2">Fast Charge : Typ. 400 mA
Slow Charge : Typ. 95mA
Total Charging Time : < 3 hours</td></tr>
<tr><td rowspan="6">22</td><td rowspan="6">Antenna Display</td><td>Bar Number</td><td>Power</td></tr>
<tr><td>5</td><td>Over -93</td></tr>
<tr><td>5 -> 4</td><td>-93 ± 2</td></tr>
<tr><td>4 -> 2</td><td>-101 ± 2</td></tr>
<tr><td>2 -> 1</td><td>-104 ± 2</td></tr>
<tr><td>1 -> 0</td><td>-106 ± 2</td></tr>
<tr><td>0 -> OFF</td><td>Under -106</td></tr>
<tr><td rowspan="3">23</td><td rowspan="3">Battery Indicator
(SPG:Software Power Gauge)</td><td>Battery Bar display</td><td>Percentage</td></tr>
<tr><td>Full Battery</td><td>100%</td></tr>
<tr><td>Half Battery</td><td>50%</td></tr>
<tr><td rowspan="2">24</td><td rowspan="2">Low Voltage Warning
(Blinking Bar)</td><td colspan="2">5% in 950mA, 1 time (standby)
10% in 950mA, 1 time (standby)</td></tr>
<tr><td colspan="2">5% in 950mA, 1 time (Call)
10% in 950mA, 1 time (Call)</td></tr>
<tr><td>25</td><td>Forced shut down
Voltage</td><td colspan="2">3.35 ± 0.05V</td></tr>
<tr><td>26</td><td>Sustain RTC
without battery</td><td colspan="2">Over 15 Mins</td></tr>
<tr><td>27</td><td>Battery Type</td><td colspan="2">Lithium-Ion Battery
Standard Voltage = 3.7 V
Battery full charge voltage = 4.2 V
Capacity: 950mAh</td></tr>
<tr><td>28</td><td>Travel Charger</td><td colspan="2">Switching-mode charger
Input: 100 ~ 240V, 50/60 Hz
Output: 4.8V, 400mA</td></tr>
</table>

3. TECHNICAL BRIEF

3.1 Digital Main Processor

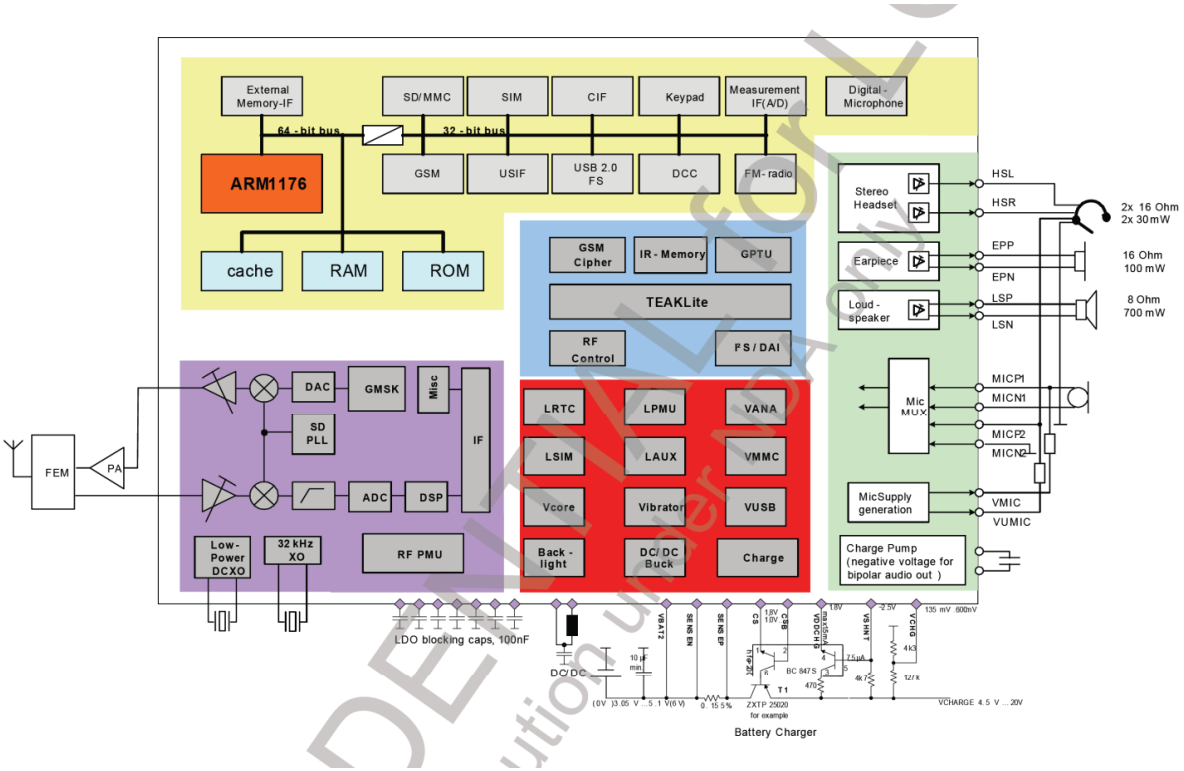


Figure. 3.1.1 X-Gold 215 Hardware Block Diagram

3.1.1 General

• Technology:
– SoC, Monolithic, 65 nm CMOS
• Package:
– eWLB, 8x8x0.8 mm
– 0.5 mm pitch
– 217 balls / 8-layer PCB

3.1.2 RF Transceiver

• Dual-band direct conversion receiver
• Tri/Quad-band possible with external circuitry
• Fully integrated digital controlled X0
• Additional buffer for 2 external system clocks
• Fully digital RF-Synthesizer incl. ΣΔ-Transmitter

3.1.3 Baseband

• DSP:
– 156 MHz TeakLite™
• MCU:
– ARM1176® @ 208 MHz
• MCU RAM:
– 3.00Mbit
• Memory I/F:
– 512 Mbit
• Modem:
– GPRS class 12, (RX/TX CS1-CS4)
– EGPRS class 12, (RX MCS1-MCS9, TX MCS1-MCS4)
• Cipher Units:
– A51/2/3
– GEA-1/2/3
• Security:
– OMTP TR0
– Secure Boot
– RSA(ROM)/SHA-1(HW accel.)
– OCDS disabling
– Certificate Management

• Speech Codec:
– FR / HR / EFR / NB-AMR
• Audio Codec (running on ARM1176):
– SP-MIDI
– SB-ADPCM
– MP3
– WB-AMR
– AAC/AAC+/eAAC+
• Others:
– DARP (SAIC)
– TTY
• Customization:
– E-Fuses

3.1.4 External Memory

• External Bus Unit
– 25-bit address bus (512 Mbit)
– 16-bit data bus
– 1.8V & 2.8V support
• Flash / RAM
– NAND Type
– Serial Flash SPI and SPI-4
– Parallel Flash (Page & Burst Mode)
- 16-bit Demultiplexed
- 16-bit AD-multiplexed
- 16-bit AAD-multiplexed
– iNAND Type e.g. oneNAND
• Memory card
– SD/MMC card interface with 1 or 4 data lines

3.1.5 Connectivity

• 3xUSIF (configurable either as SPI or UART), I2C, I2S; Interfaces @ 1.8V
• Direct (U)SIM 1.8/3V
• USB2.0 up to 480 Mbit/s (High Speed) w/ external USB Phy over ULPI interface
• Stereo Headset (Amplifier integrated)
• 3 external analog measurement PIN's
• Bluetooth

3.1.6 Mixed Signal

• Improved audio performance
• Loudspeaker Audio Class D Amplifier, 700 mW@8 Ω mono for hands-free and ringing
• Stereo Headset 2x30 mW@16 Ω w/o coupling C
• Mono Earpiece 100 mW@16 Ω
• Digital microphone supported
• Differential microphone inputs

3.1.7 FM Radio

• Integrated FM radio
– FM Stereo RDS Receiver
– Sensitivity 2 μV EMF
– Support for US & EU bands
– Stereo recording

3.1.8 Power Management

• Direct-to-Battery Connection
– LDOs (incl. capless)
– DC/DC step-down converter
– DC/DC step-up for white LED supply
• Battery Type
– Li-Polymer
• Charging control
– Battery temperature
– Watchdog protection
– Start-up on flat battery
• External Charger
– Switch mode
• USB battery charging
– USB charging spec 1.0 compliant
• Backlight
– Up to 4 serial white LEDs (integrated LDO)

3.1.9 Main LCD Display

• Type
– 128x160, 65k color (serial)
– QQVGA, 262k color (parallel)
• Interface
– Parallel 8/9bit MIPI-DBI Type B
– Serial MIPI-DBI Type C
– Interf. voltage at 1.8V or 2.8V
• gRacr - Display Controller (Hardware)
– 30 fps Display update without DMA (up to 60 fps) (full or partial)
– Video post processing Scaling, Rotation (90° steps), Mirroring
– Overlay with alpha blending
– Color conversion YUV -> RGB
– 2D vector graphics (Lines, filled rectangles, Bit block transfer (e.g. sprites, scrolling, antialiased bitmapfonts)

3.1.10 Camera

• 2 Mpx YUV parallel interface
• HW JPEG encoder (39 Mpx/sec)
• 39 MHz Pixel Rate
• 15 fps@ 2 Mpx full resolution

3.1.11 Video Capabilities

• Video Decoding MPEG-4/H.263
– QCIF@30 fps
– QVGA@15 fps
• Video Encoding MPEG-4/H.263
– QCIF@15 fps

3.1.12 Audio Capabilities

• Polyphonic ring tones
– 64 voices MIDI, SP-MIDI
– FM synthesizer
• AMR-WB
• True ring tones (MP3)
• MP3, eAAC+
• G.722 SB-ADPCM encoding/decoding

3.2 Power Management

A mobile platform requires different power supplies for different functions. These power supplies are generated in the integrated Power Management Unit (PMU). The PMU is designed to deliver the power for a typical standard phone. For advanced features additional off chip power supplies might be necessary.

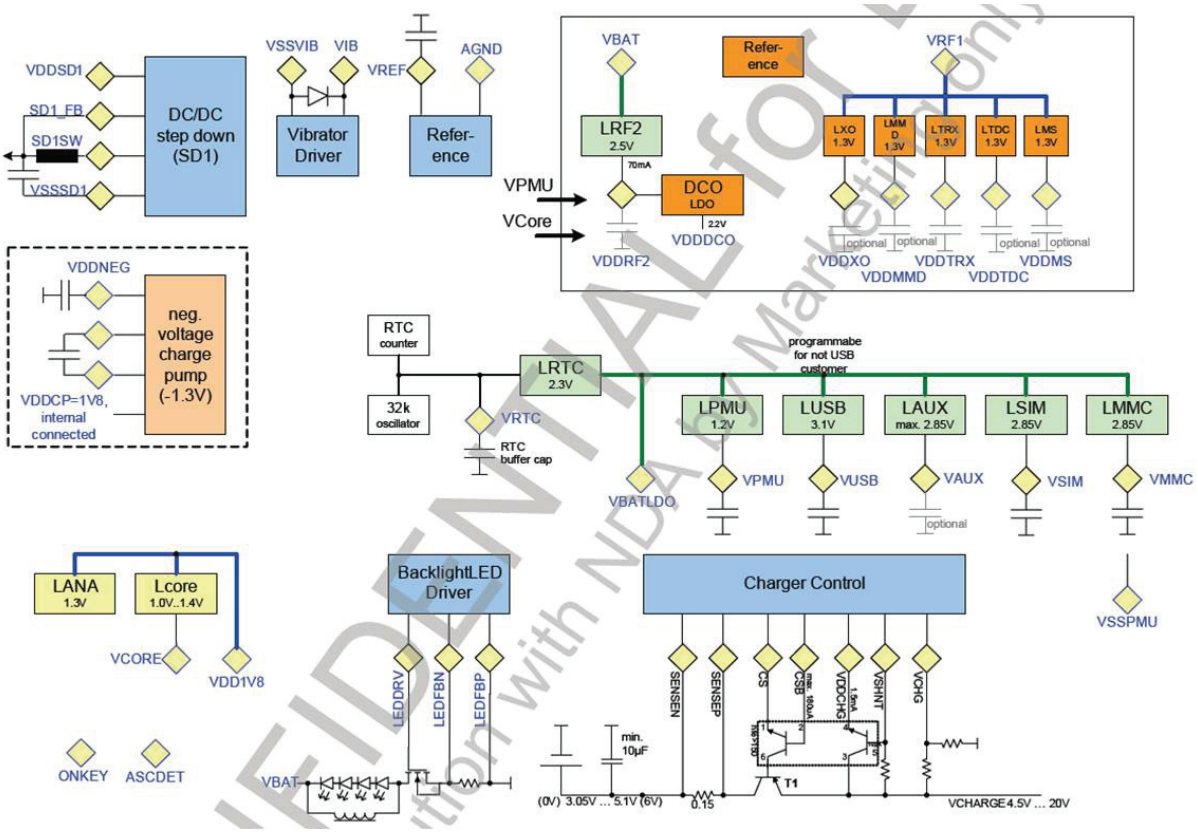


Figure. 3-2-1 Block Figure of the PMU Modules X-GOLD™ 215

▪ **DC/DC Step Down Converter for 1.8V (SD1)**

The DC/DC converter generates a 1.8 V supply rail. This voltage rail is used to supply main parts of the system, like the digital core of the chip (via LDO LCORE), some parts of the mixed signal macro, parts of the RF macro and the external memory if a 1.8 V memory is used. The efficiency of the DC/DC converter is optimized for an average load current of 100 mA. That is the load current estimated for the GSM talk mode.

▪ Linear voltage Regulators (low dropout) LDOs

The LDOs are used to generate the supply for the different supply domains not directly supplied out of the DC/DC converter.

▪ LCORE

The LCORE LDO provides the VCORE supply used for most of the digital parts of the chip. ip

▪ LPMU

The LPMU provides VPMU used for the PMU supply, e.g. for the startup statemachine and analog parts like ADC, sense amplifier etc.

▪ LUSB

The LUSB LDO generates the supply for the USB transceiver (output driver and input). If no USB interface is required, LUSB can be used as general purpose LDO.

▪ LAUX

The LAUX generates VAUX. It is a general purpose LDO and can be used for different functions depending on the phone application, e.g. for the display or camera.

▪ LMMC

The LMMC generates VMMC. It is a general purpose LDO and can be used e.g. for memory cards.

▪ LSIM

The LSIM LDO generates the VSIM supply for the SIM card and interface. It is designed to supply Standard SIM cards according ETSI TS 102 221.

▪ Other LDOs

• The RF module has implemented several LDO's for different RF power domains.
• The mixed signal module has some LDO's for the audio driver and microphone supply
• The FM receiver has an internal LDO for sensitive RF circuits.

Supply Domain LDO Name	Voltage	Max. Current	Output Cap	Input Domain	Comment
VBAT	0 ... 6.0 V				Operating range is 3.05 V ... 5.5 V, system emergency switch off voltage is about 2.8 V
VDD1V8	1.8 V	450 mA	22 µF	VBAT	This voltage is generated by the DC/DC converter with 3.3 µH inductor, The voltage is used for: Memory supply, and via LDO's for digital core supply, mixed signal supply and RF supply.
LCORE	1.2 V	300 mA	2x100 nF	VDD1V8	
LANA	1.3 V	10 mA	No	VDD1V8	No ball
LRTC	2.3 V	2 mA	>=100 nF	VBAT	This supply is only used for the HPBG, the 32.768 kHz oscillator and the real-time clock counter required during the sleep- and low-power mode.
LPMU	1.2 V	15 mA	100 nF	VBAT	Supply for the digital part of the PMU including digital control of DC/DC converter. This voltage is also used for the N-DEMOS driver of DC/DC converter and the class-D amplifier and the core PLL.
LUSB	3.1 V	40 mA	100 nF	VBAT	Used for the USB driver supply or as general purpose LDO with programmable output voltages (2.5 V, 2.85 V, 3.1 V)
LAUX	1.5 V ... 2.85 V	150 mA	470 nF	VBAT	General purpose LDO for e.g. Display, Bluetooth, Camera etc. Programmable output voltages are (1.5 V, 1.8 V, 2.5 V, 2.85 V)
LSIM	1.8 V / 2.85 V	30 mA	>=100 nF	VBAT	LDO dedicated to the SIM-Card supply. It is chip internal connected to the SIM interface driver.
LMMC	1.5 V ... 2.85 V	150 mA	>=470 nF	VBAT	General purpose LDO, targeted for MMC/SD card supply.
VDDNEG	-1.3 V	100 mA	100 nF	VDD1V8	Negative voltage for the bipolar headset audio driver. Generated by a charge pump.

Table. 3-2-1 Power supply Domains (without RF)

3.2.1 Power on and startup

▪ **Analog startup Circuit**

Because the POR circuit and the LPBG are directly connected to the battery, it is not possible to switch them off. If the battery voltage exceed the power on reset threshold (2.5V), the power on reset is released, the LPMU regulator and the LRTC voltage regulator are switched on. The LPMU regulator starts in its ultra-low power mode

The LPMU regulator generates a control signal (lpmu_OK) that enables the 50KHZ PMU oscillator. The output clock of the oscillator is checked with a fully coded counter. A counter overflow releases the reset (vpmu_rst_n) signal for the small PMU state-machine.

▪ **Small first digital State-Machine**

The small PMU state-machine is always connected to VPMU After starting from reset the small startup state machine enters the SYSTEM OFF state and only continuous the startup procedure if a switch on event like first connect, on-key, wake up or charge detect occurs.

▪ **PMU-main State-Machine**

The main PMU state-machine is always connected to VPMU also. The power up sequence driven by the PMU state-machine can be seen in Figure18. After enabling the reference (HPGB) and waiting for the settling time, the battery voltage is measured and compared with the power on threshold. If the battery voltage is high enough, the SD1 DC/DC converter and the LCORE LDO are started. A timer ensures that the supply voltage will be stable before the DCXO is enabled. The DCXO settling time is ensured using a fixed timer. After an overflow of this timer, the reset is released for the rest of the system. The PMU state machine remains in this System-ON state until the system is switched into the OFF state. For example the system sleep mode is completely configured by software(for example switching off the LDO's, switching of the DCXO etc.) and controlled by the VCXO_enable signal. The reason for the startup is stored in the ResetSourceRead register.

▪ **Battery Measurement**

The ADC and the oscillator for the ADC needs the VDD_ADC supply voltage from the LADC LDO. LADC uses either the charger voltage VDD_CHARGE or VDDRTC as input voltage. The input voltage is selected automatically by a bulk switch circuit. LADC, the ADC and the oscillator are enabled on request for every battery measurement if the charger unit is not running. This is handled by an ADC control block in one of the state-machines. If the charger unit is running the ADC is controlled by the charger state-machine

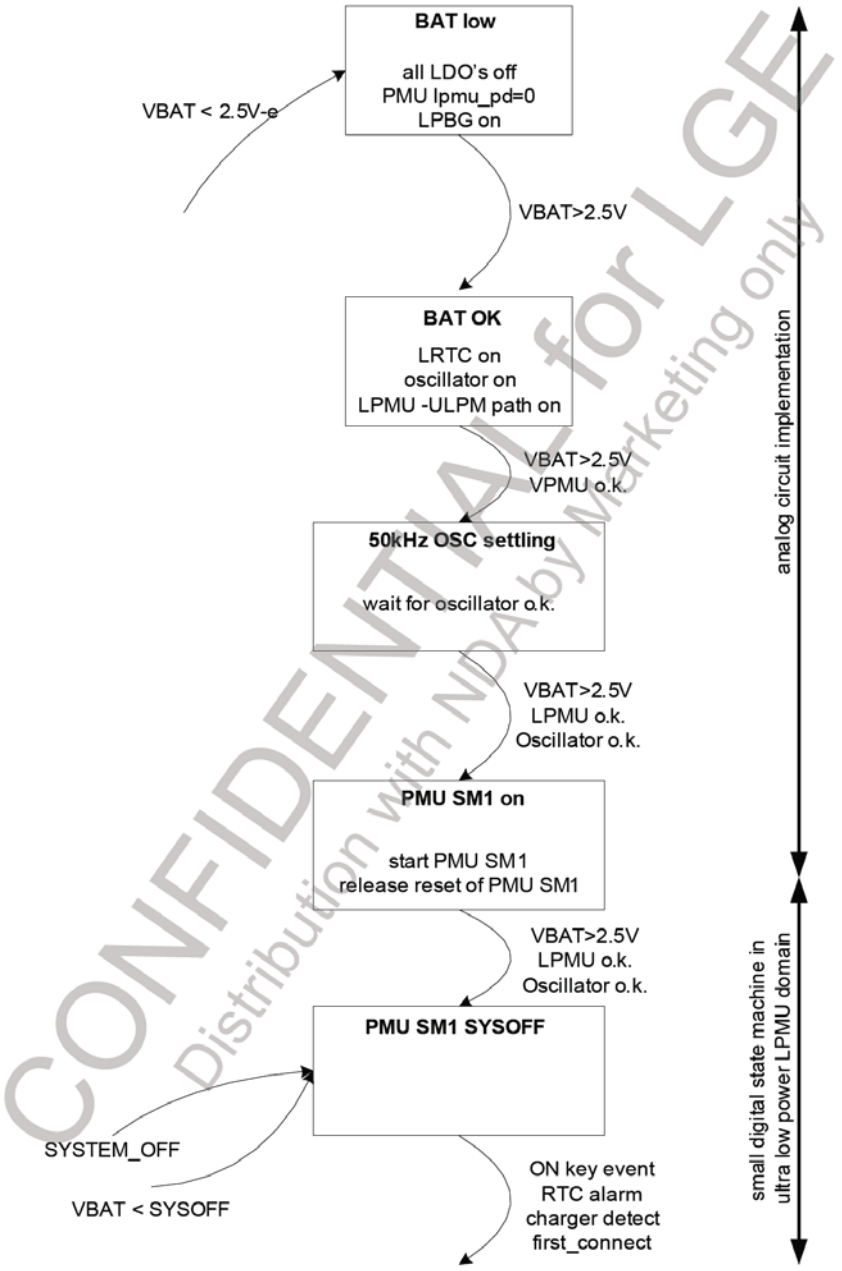


Figure.3.2.1 First Part of the State Machine, Running in Different Power Domains than the Second Part

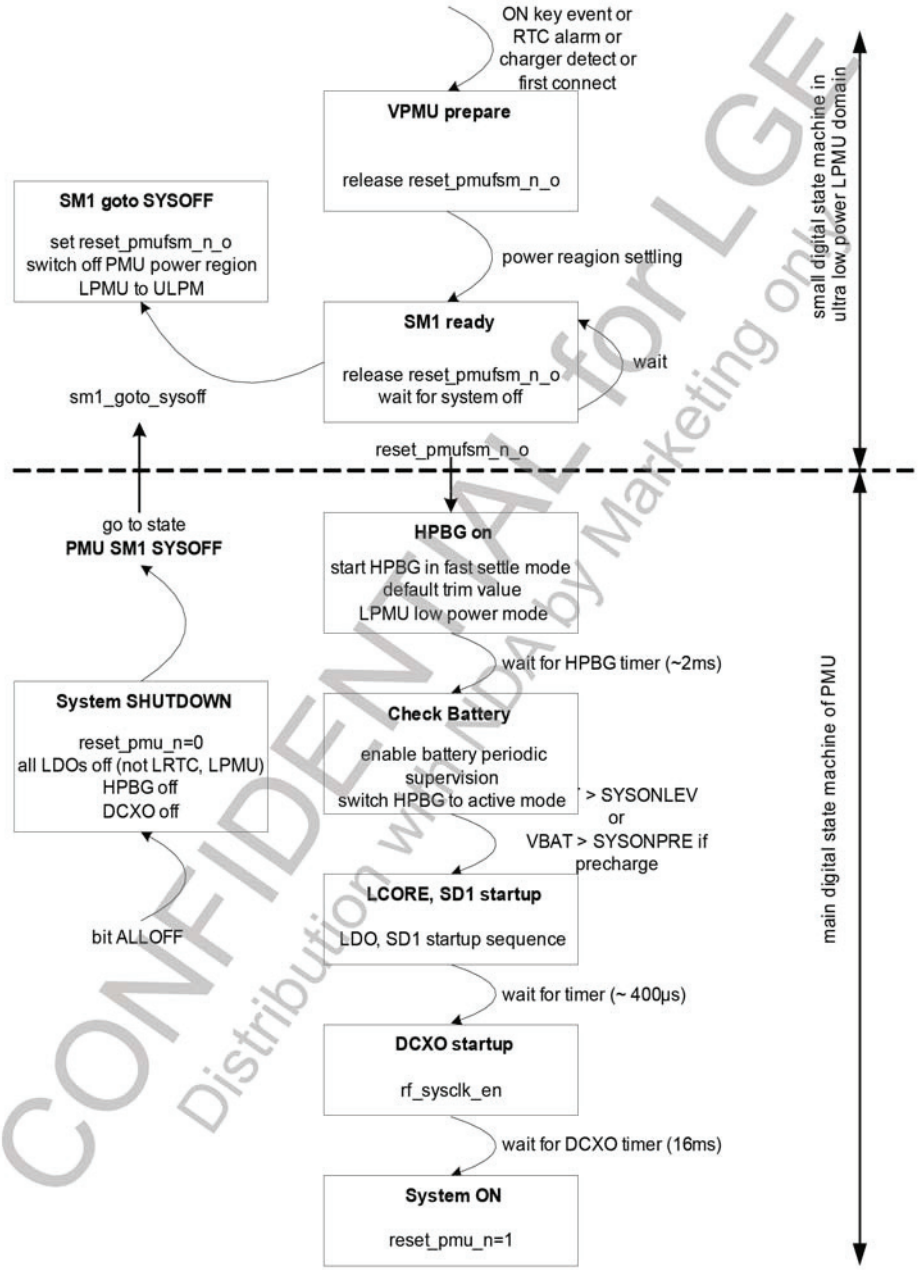


Figure 3.2.2 Second (Main) Part of the Startup State Machine in the VPMU Domain

3.2.2 Switching on due to first connect

If the battery voltage is connected the first time, that means the system enters the first time the SYSOFF state, this is stored in a first connect flag. If the first connect flag is set, the system will start immediately and not wait for any other system on event in the SYSOFF state.

3.2.3 Switching on due to on-Key event

The on key is connected to the ONKEY pad. The ESD protection and the input structure of this pad are connected to VRTC. If the ONKEY pad is forced to VRTC by an external key or similar circuit, the system starts. The ONKEY is sampled with the PMU clock. It has to be sampled four times high before a valid on event is generated. The status of the ON key can be read in the PMU registers, so it can be used as a functional key during phone operation also

3.2.4 Switching on due to RTC alarm

The real time clock can generate a wakeup signal called RTC alarm. This signal is sampled from the state-machine and after successfully detecting a high, the system is switched on.

3.2.5 Switching on due to charging

When a battery with a voltage below the SSONLEV level is inserted, the state machine will not start the system. As long as the battery voltage stays lover than SYSONLEV the system will stay off. The only possibility to start up the system is due to an external charger.
If an external charger is connected and detected and the battery is charged above the SYSONPRE voltage level the system will start up.
The PMU main state machine waits in the Check battery state until the battery voltage condition is fulfilled. The charger state machine provides the necessary pre-charge indication signal. This pre-charge signal is denounced in a small counter to have a stable signal. This is important, especially in half/full-wave charging where the charger detection is switching between charger detected/not detected according the AC supply frequency. reasons

machine. The pre-charge signal is used to trigger the pre-charge signal is used to trigger the pre-charge functionality. The charger state machine fully control the pre-charge, the PMU-state machine now changes to state HPBG on state and the system starts. This state change is indicated to the charger state-machine to enable the charger watchdog for safety

3.2.6 Power Supply Start-up sequence

In order to avoid an excessive drop on the battery voltage caused by in-rush current during system power-on, possibly leading to system instability and “hick-ups” a staggered turn-on approach for the regulators is implemented. The regulators are turned on in a well defined sequence, thus spreading the in-rush current transients over time.

The IO’s of X-GOLD TM 215 are isolated in OFF mode (core supply is off). The isolation signal is controlled by the PMU state machine. This ensures that the PADs are in a well defined state during core supply settling. This allows to power up the LCORE core regulator and wait for the core to reach reset state before powering up the I/O supply regulators.

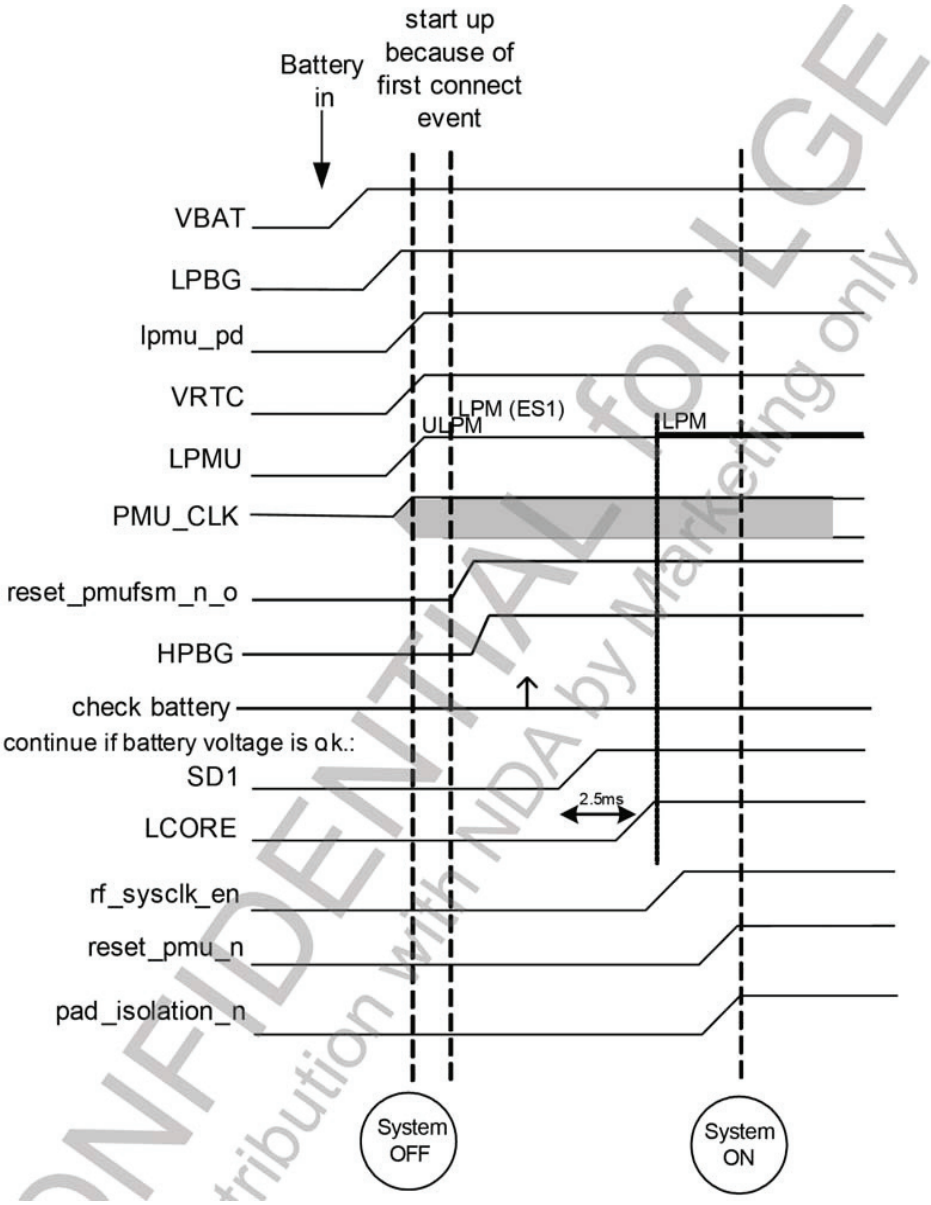


Figure 3.2.3 Start Up Sequence (triggered by First Connect Event)

3.2.7 External Reset Handling

The chip reset can be controlled by an external RESET_N ball. If this ball is pulled low, the chip will be reset. All PMU registers are reset during the external reset including LSIM control bits. The PMU statemachines are also not reset from the external reset.
An SW or watchdog reset will not reset the PMU registers. A SW and Watchdog reset is seen on the reset_n pad to allow the reset of external devices. Basically there are three reset sources, first the reset signal controlled by the PMU (reset_pmu_n_o), second the reset signal controlled by the SCU (resetout_o) and third the external reset (RESET_N). The SCU reset is triggered by SW (for example due to a SW reset or watchdog reset). The PMU reset is controlled by the PMU state machine.
The output of the reset handling block is the reset_postscu_n_o signal. This signal controls for example the µC subsystem and releases reset for the controller. During normal start up, the PMU releases the reset_pmu_n_o signal after entering the SYSTEM ON state. At this time the resetout_o signal is high, the RESET_N pad is not pulled low and therefore the reset_postscu_n_o signal follows the reset_pmu_n_o signal.
That means the µC reset will be released and the µC starts operation. If the SW triggers an external reset via the SCU, signal resetout_o will be forced to low for a certain time and RESET_N will be forced to low by the open drain driver. At the same time the feedback to the SCU will be masked to not reset the baseband. The RESET_N pad is in the VDDRTC domain but the internal pull up is connected to the VDD_VDIG1 (1.8V) domain. That allows the pad to be used as reset for external devices running in the VDD1V8 domain. The RESET_N pad can also be used to monitor the chip internal reset condition during startup.

The open drain driver is a weak driver, that means it can be forced to high during debug from external pushing some current into the pad. In testmode signal reset_pmu_n_o is high, that means the chip reset is fully controlled from external

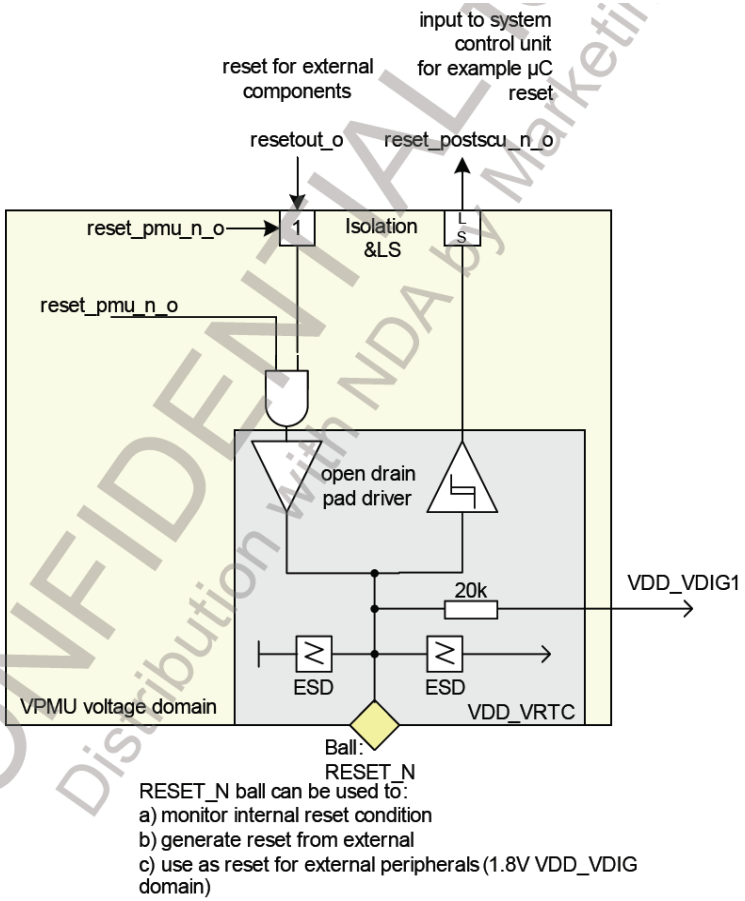


Figure 3.2.4 PMU, CGU and External Reset

3.2.8 Sysclock Switching

The PMU controls the rf_sysclk_en signal of the DCXO in the RF macro. During startup the PMU enables the DCXO. After the system is running the DCXO is controlled by the SCU of the baseband by using the vcxo_enable signal. This is handled by a dedicated logic in the PMU, see **Figure 21**. As long as rf_sysclk_en_pmu, the output of the PMU state-machine is high, vcxo_enable controls the rf_sysclk_en signal to the RF. If rf_sysclk_en_pmu is low, the DXCO is switched off, independent from vcxo_enable.

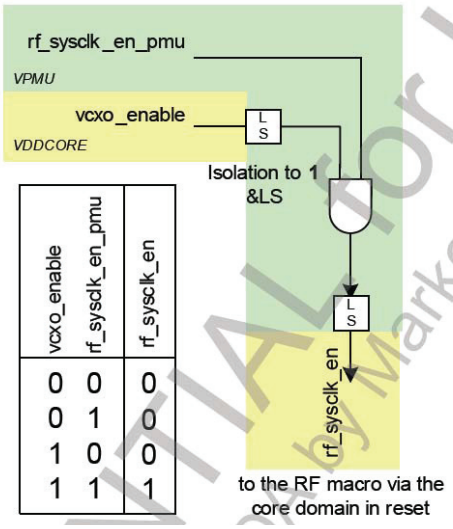


Figure 3.4.2 How sysclock Enable is Routed in the PMU

3.2.9 Undervoltage Shutdown

In active mode the PMU periodically measures the battery voltage using the ADC from the charger unit. If the battery is measured to be below the programmable shut-down level (called SYSOFF), the system changes to OFF mode. This is done via the SHUTDOWN state of the PMU state machine. (see chapter switch OFF)

3.2.10 Software Reset

A software reset does not affect any PMU register. The PMU register are reset with the reset_pmufsm_n_o signal. That means all PMU register are reset in OFF state. For details about the SW reset see chapter **External Reset Handling**

3.2.11 PMU Clock

During the first startup (for example plugging in a battery) a PMU internal oscillator is used for generation of the PMU clock (pmu_clock). The frequency is slightly above 32 kHz (typ. 50 kHz) to be out of the audio band also for worst case devices. After first startup the software shall enable the 32 kHz crystal oscillator. It is not possible to use the 32 kHz oscillator during first startup, because the settling time of the oscillator can be quite long. After the 32 kHz oscillator is running and settled the software shall switch the PMU clock to the 32 kHz clock and disable the internal PMU oscillator for power saving reasons. The 32 kHz oscillator shall never be disabled after the PMU clock has been switched. The ADC in the charger unit has it's own oscillator generating a frequency of about 10 MHz. This oscillator is running during charging and during battery measurements triggered by the PMU. It is off otherwise.

3.2.12 System Sleep Mode

The sleep mode is controlled by using the VCXO_enable signal. This signal is used to switch the LDO's and the DC/DC converter SD1 in a programmable way into its low power mode (PFM). In addition DC/DC converter SD1 can be configured to change the output voltage to a lower value for additional power saving. VCXO_enable is also used to deactivate the HPBG and setting LDO LPMU in the ultra-low-power mode. In addition the DCXO is switched off by the VCXO_enable signal. The VCXO_enable signal is also used to switch some LDO's (software configured) to sleep and/or off mode or to change the output voltages of said LDO's. The state of the main PMU state machine is not changed due to VCXO_enable.

3.2.13 DC/DC Pre-Load Register Handling

The DC/DC converter works in different modes. If the mode is switched from PFM to PWM the pulse-width of the DC/DC converter depends on the current battery voltage (and on the output voltage). The PMU state-machine knows the battery voltage because of the battery supervision function. Depending on this value it selects a startup pulse-width for the DC/DC converter out of a register table. (4-values)

3.2.14 Power Down Sequence

Setting bit OFF in the GeneralControl register switches the system into OFF mode. After the turn off event, the state-machine switches to the SHUTDOWN state. The reset_pmu_n_o signal changes to low, the I/O pads are isolated using the padisolation_n signal, the LCORE LDO and the SD1 DC/DC converter are switched off, the LPMU LDO is switched to ultra-low power mode, the DCXO is turned off and the bandgap buffer is disabled. Before switching OFF the software shall have enabled the 32 kHz oscillator and has switched the PMU clock to the 32 kHz clock to archive the target OFF current

3.3 FEM with integrated Power Amplifier Module (SKY77550, U500)

3.3.1 Internal Block Diagram

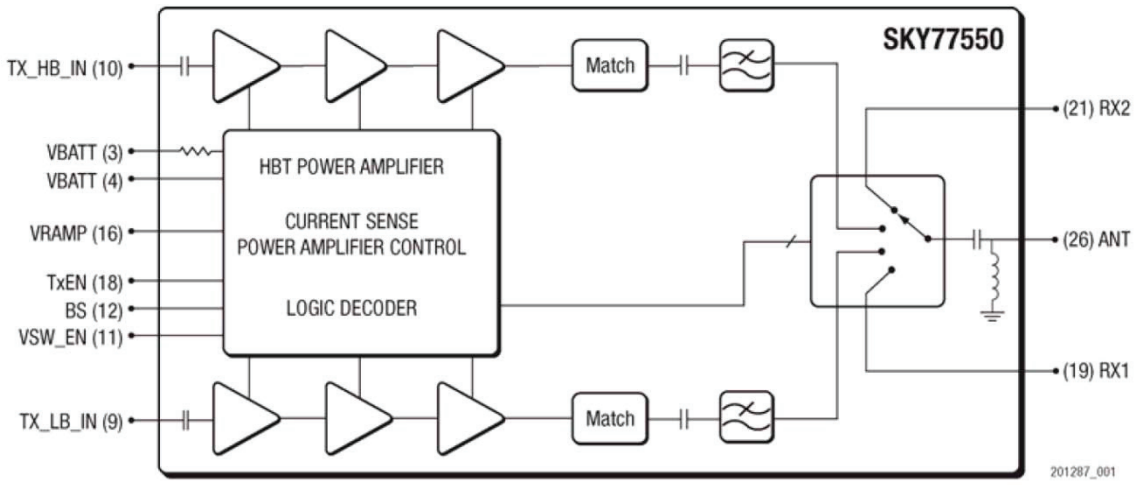


Figure. 3-3-1 SKY77550 FUNCTIONAL BLOCK DIAGRAM

3.3.2 General Description

Skyworks latest front-end modules (FEM) for GSM applications with integrated power amplifier control (iPAC™) provide a high level of integration, high efficiency, ease of application, and smaller packaging.
The new BiFET control circuit improves the output RF spectrum and simplifies the calibration process.
This Application Note aids phone anufacturers with implementing the latest Skyworks SKY77550 iPAC™ Front-End Module.
A Skyworks iPAC™ FEM consists of a PA lineup block, a PAcontrol block, impedance matching circuits, harmonic filtering,and a switch. Embedded in a single Gallium Arsenide (GaAs) die,one Heterojunction Bipolar Transistor (HBT) PA lineup supports theGSM850/900 bands and another supports the DCS1800 and PSC1900 bands.
A BiFET block provides the internal PAC function and interface circuitry. The front-end, with switches and diplexer, provides a single antenna port and low insertion loss receive paths for two Rx ports.

Mode	Input Control Bits		
	V_{SW_EN}	TxEN	BS
STANDBY	0	0	0
Rx1[1]	1	0	0
Rx2[1]	1	0	1
Tx_LB	1	1	0
Tx_HB	1	1	1

1 Rx1 and Rx2 are broadband receive ports and each supports the GSM850, GSM900, DCS, and PCS bands.

Figure 3.3.2 Band SW Logic Table

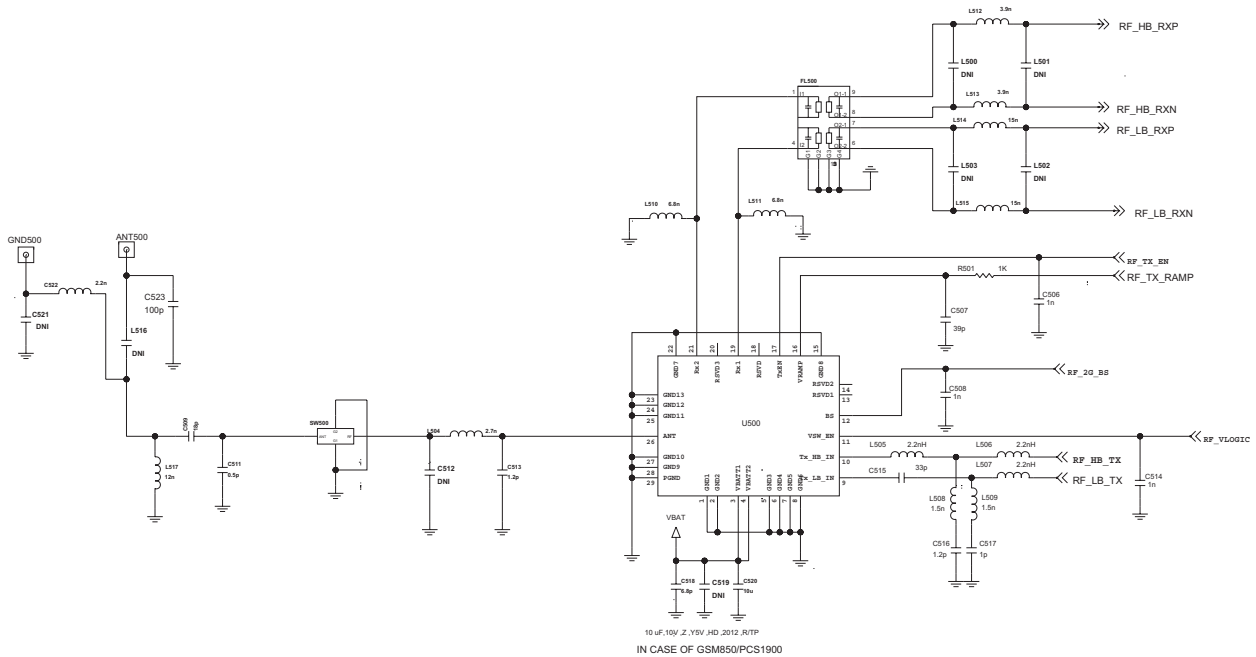


Figure 3.3.3 FEM CIRCUIT DIAGRAM

3.4 Crystal(26 MHz, X100)

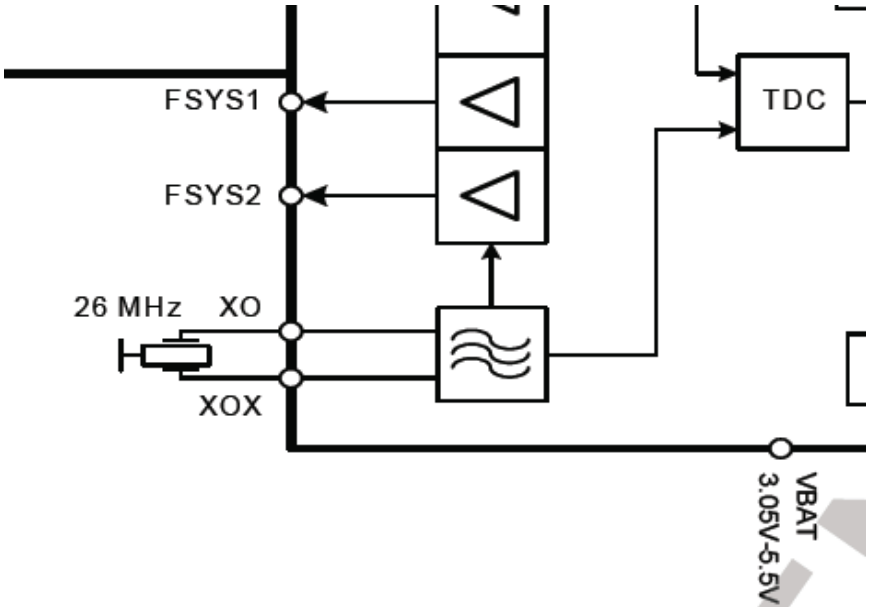


Figure. 3.4.1 Crystal Oscillator External Connection

The X-GOLDTM215 RF-Subsystem contains a fully integrated 26 MHz digitally controlled crystal oscillator, designed for 8 pF crystals. The only external part of the oscillator is the crystal itself. Overall pulling range of the DCXO is approximately ±55 ppm, controllable by a 13-bit tuning word.

This frequency serves as comparison frequency within the RF-PLL and as clock frequency for the digital circuitry.
The 26 MHz reference clock can also be applied to external components like Bluetooth or GPS, via the two buffered output signals FSYS1 and FSYS2.

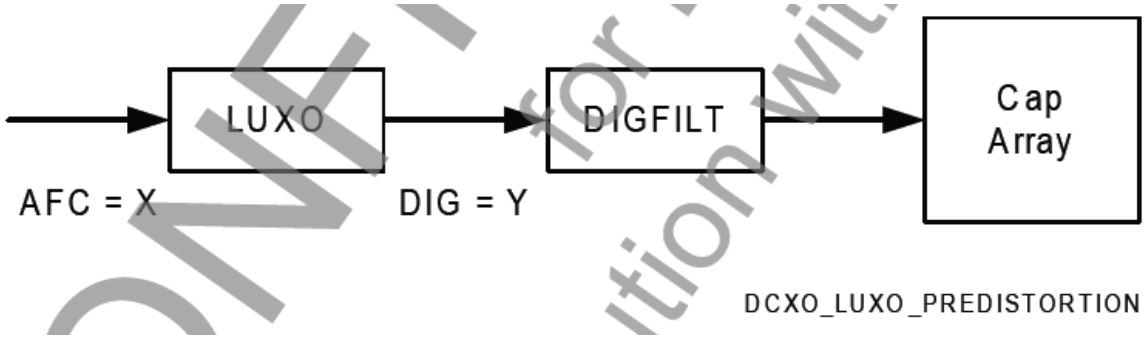


Figure. 3.4.2 Digital PREDISTORTION with LUXO

The DCXO tuning characteristic should be a first order linear function of the programming word AFC. The variable capacitance array is a first order linear function of the digital word DIG, which leads to a nonlinear curve ppm vs. DIG (and also a nonlinear ppm vs. AFC for DIG=AFC). In order to linearize the ppm vs. AFC curve the implementation of a predistortion is necessary.
To get the wanted linear ppm vs. AFC tuning curve some digital predistortion of the AFC word is required. This predistortion is performed by the linearization unit for crystal oscillator (LUXO). The LUXO calculates the corresponding DIG value according to the given AFC value.

3.5 RF Subsystem (U101)

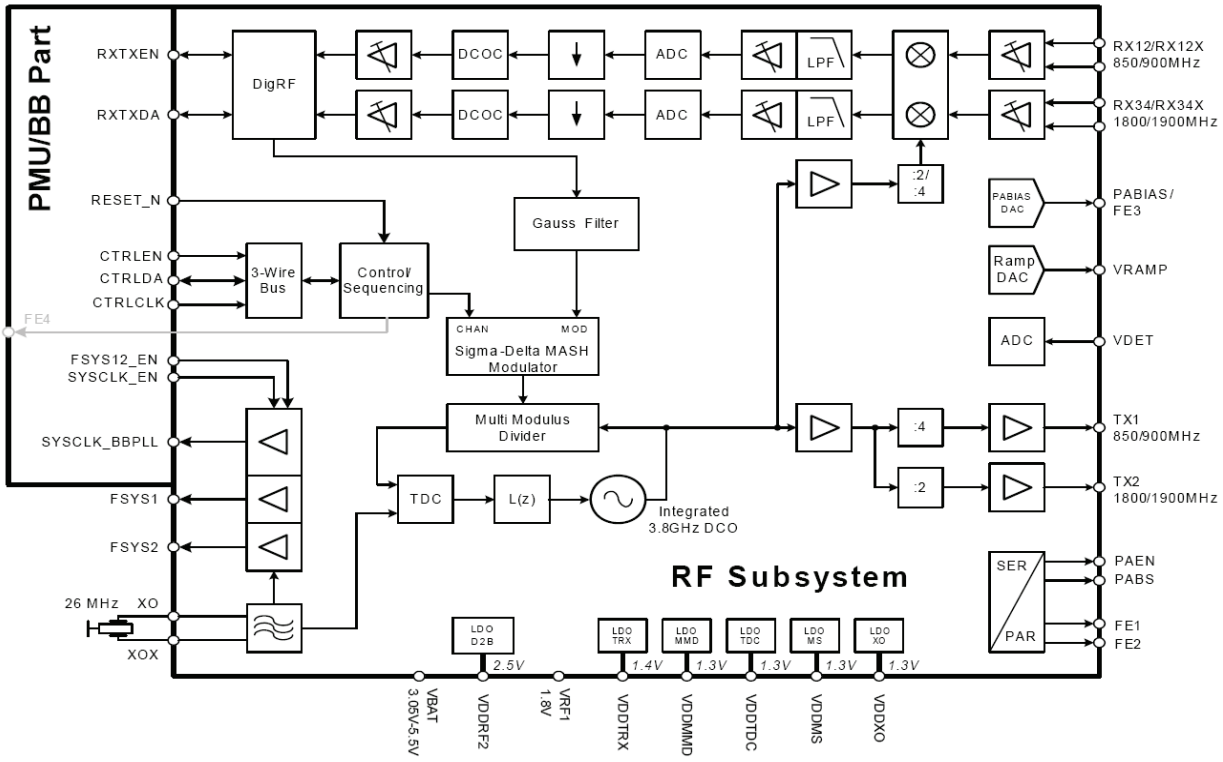


Figure. 3-5-1 Block DIAGRAM of RF Subsystem

3.5.1 GENERAL DESCRIPTION

The X-GOLD™ 215 RF subsystem is designed for dual-band GSM voice and data applications (GPRS class 12). The system can be configured to support one low band, GSM850 or EGSM900, and one high band, DCS1800 or PCS1900. A block diagram of the RF subsystem is given in **Figure 3-5-1**.

3.5.2 FUNCTIONAL DESCRIPTION

Receiver

The X-GOLD™215 dual-band receiver is based on a Direct Conversion Receiver (DCR) architecture. Input impedance of the LNAs is optimized to achieve a matching without (external) high quality inductors. By use of frequency dividers (by 2/4) the LO frequency is derived from the RF frequency synthesizer.

The receive path is fully differential to suppress the on-chip interferences and reduce DC-offsets. The analog chain of the receiver contains two LNAs (low/high band), a quadrature mixer followed by an analog baseband filter and 14-bit continuous-time delta-sigma analog-to-digital converter. The filtered and digitized signal is fed into the digital signal processing chain, which provides decimation, DC offset removal and programmable gain control.

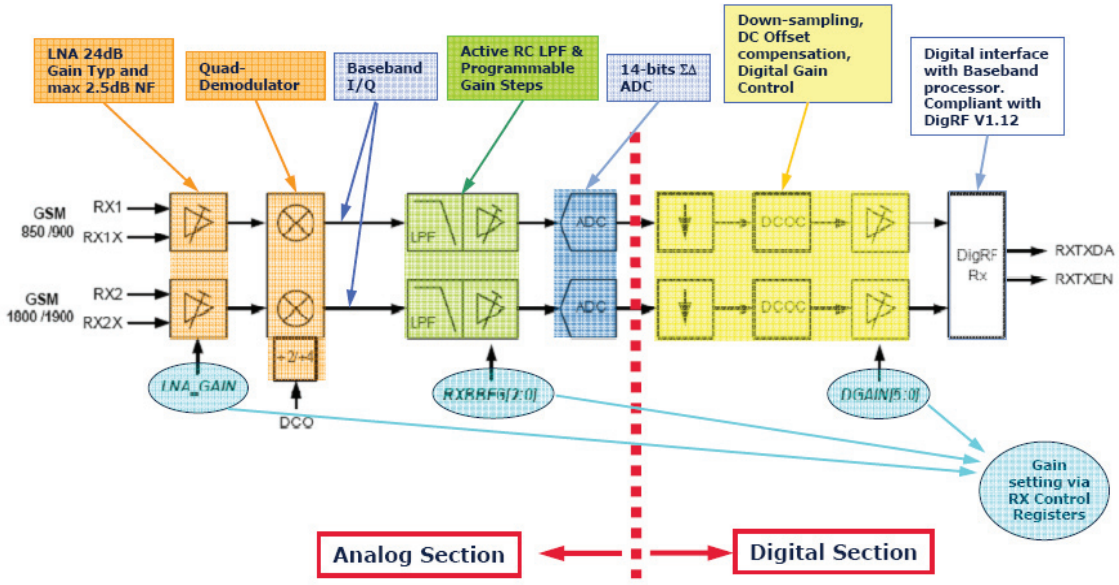


Figure. 3.5.2 RECEIVER CHAIN BLOCK DIAGRAM

Transmitter

The GMSK transmitter supports power class 4 for GSM850 or GSM900 as well as power class 1 for DCS1800 or PCS1900. The digital transmitter architecture is based on a fractional-N sigma-delta synthesizer for constant envelope GMSK modulation. This configuration allows a very low power design without any external components.

Up- and down-ramping is performed via the ramping DAC connected to VRAMP.

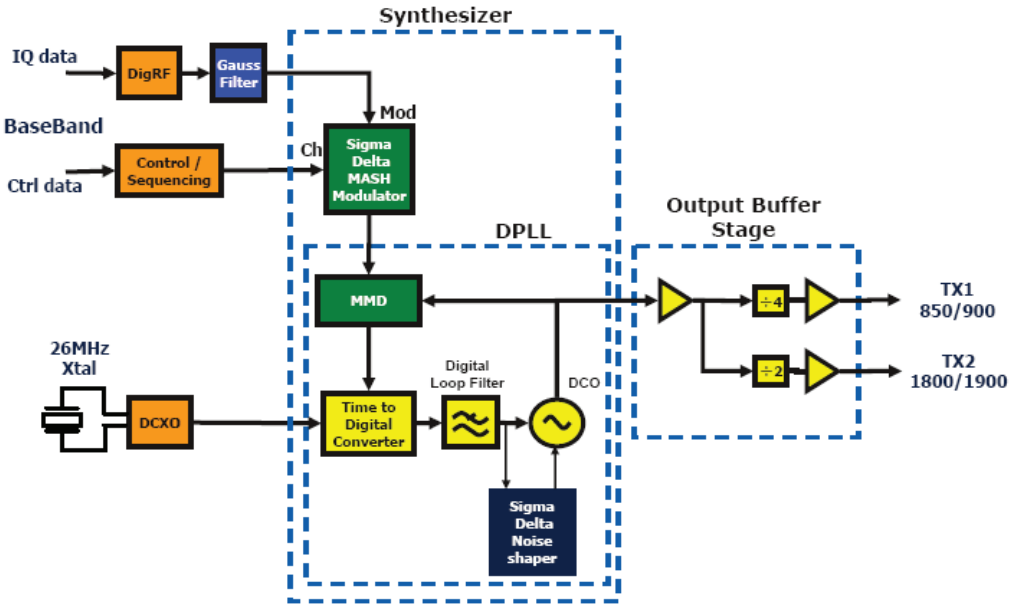


Figure. 3.5.3 TRANSMITTER CHAIN BLOCK DIAGRAM

RF synthesizer

The RF subsystem contains a fractional-N sigma-delta synthesizer for the frequency synthesis. Respective to the chosen band of operation the phase locked loop (PLL) operates at twice or forth of the target signal frequency. In receive operation mode the divided output signal of the digital controlled oscillator output (DCO) serves as local oscillator signal for the balanced mixer. For transmit operation the fractional-N sigma-delta synthesizer is used as modulation loop to process the phase/frequency signal. The 26 MHz reference signal of the phase detector incorporated in the PLL is provided by the reference oscillator.

Front-end/PA Control Interface

Two outputs (FE1, FE2) for direct control of antenna switch modules enable to select RX- and TX-mode as well as low- and high-band operation.

An extra band select signal PABS for the power amplifier is used, to support discrete PA and switching modules. Time accurate power dissipation of the PA is achieved by the control signal PAEN.

A minor set of power amplifiers require a bias voltage to enhance power efficiency. Support of this power amplifiers is achieved by the implemented bias DAC.

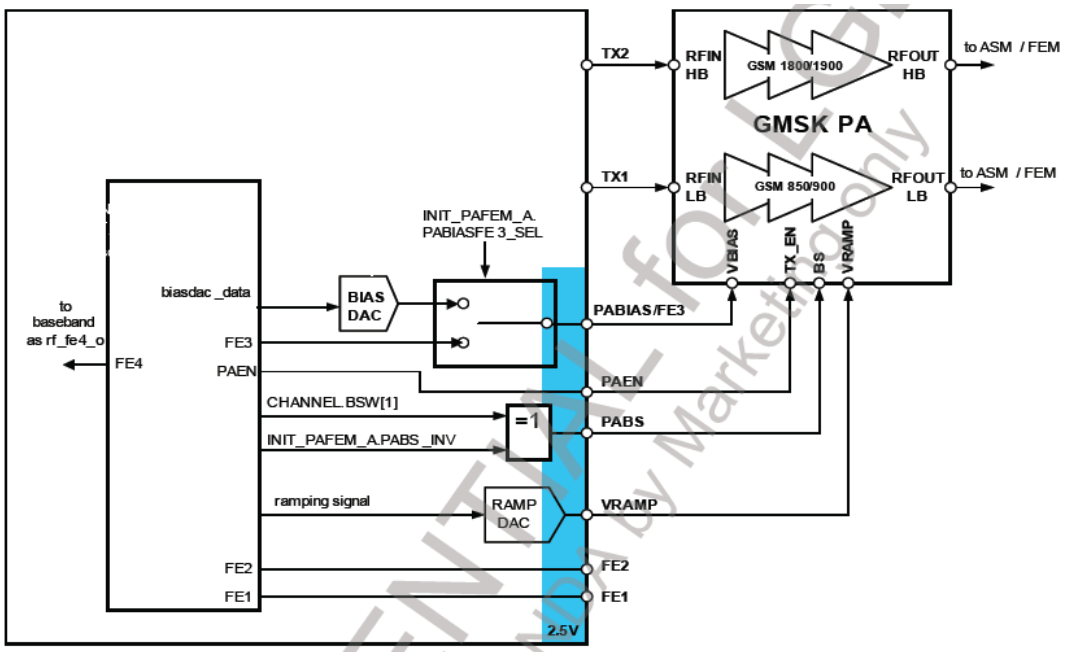


Figure. 3.5.4 PA AND FEM CONTROL BLOCK DIAGRAM

Power Supply

To increase power efficiency most parts of the RF subsystem are supplied by the DCDC converter situated in the PMU subsystem. Conversion of the 1.8 V output voltage of the DCDC to the 1.3 V/1,4 V circuit supply voltages is achieved by several Low-DropOut regulators (LDO).

One embedded direct-to-battery LDO provides the 2.5 V supply voltage for the remaining circuits.

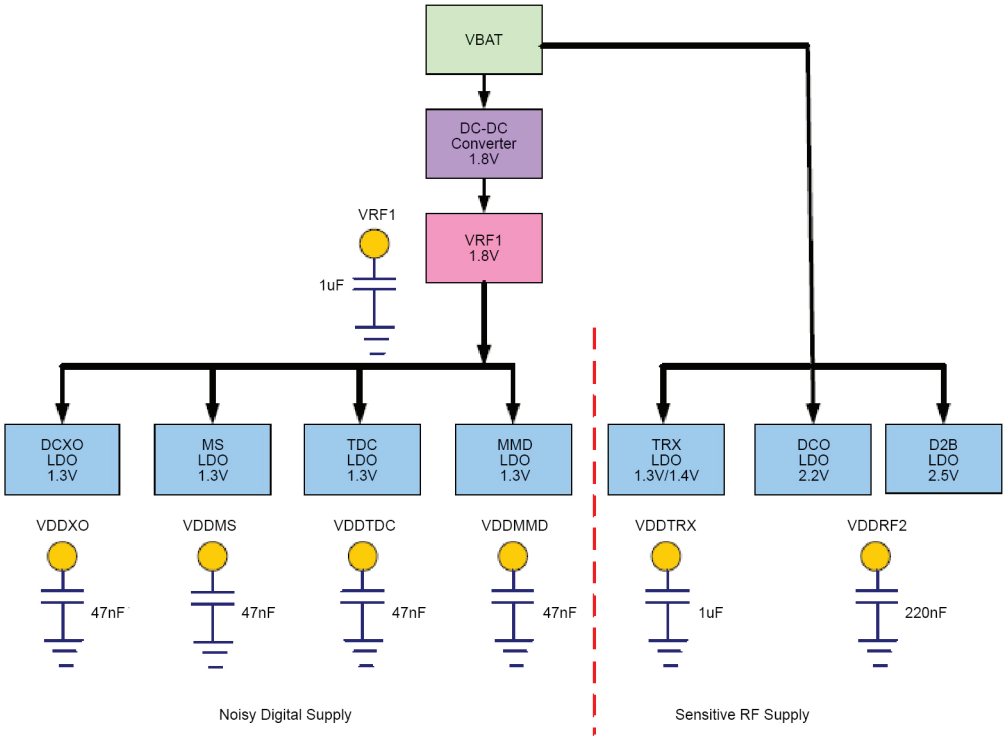
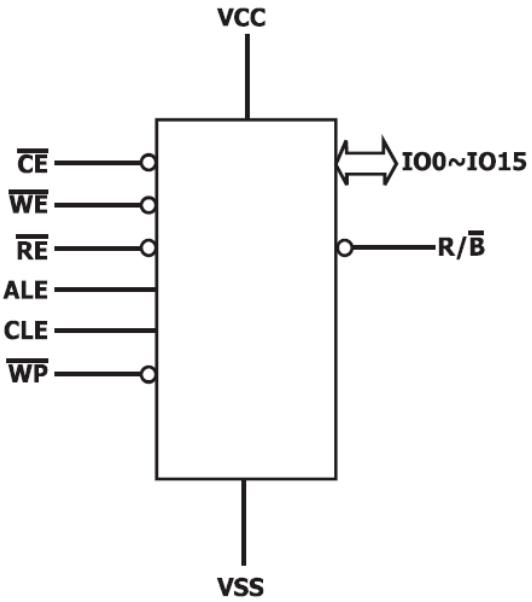


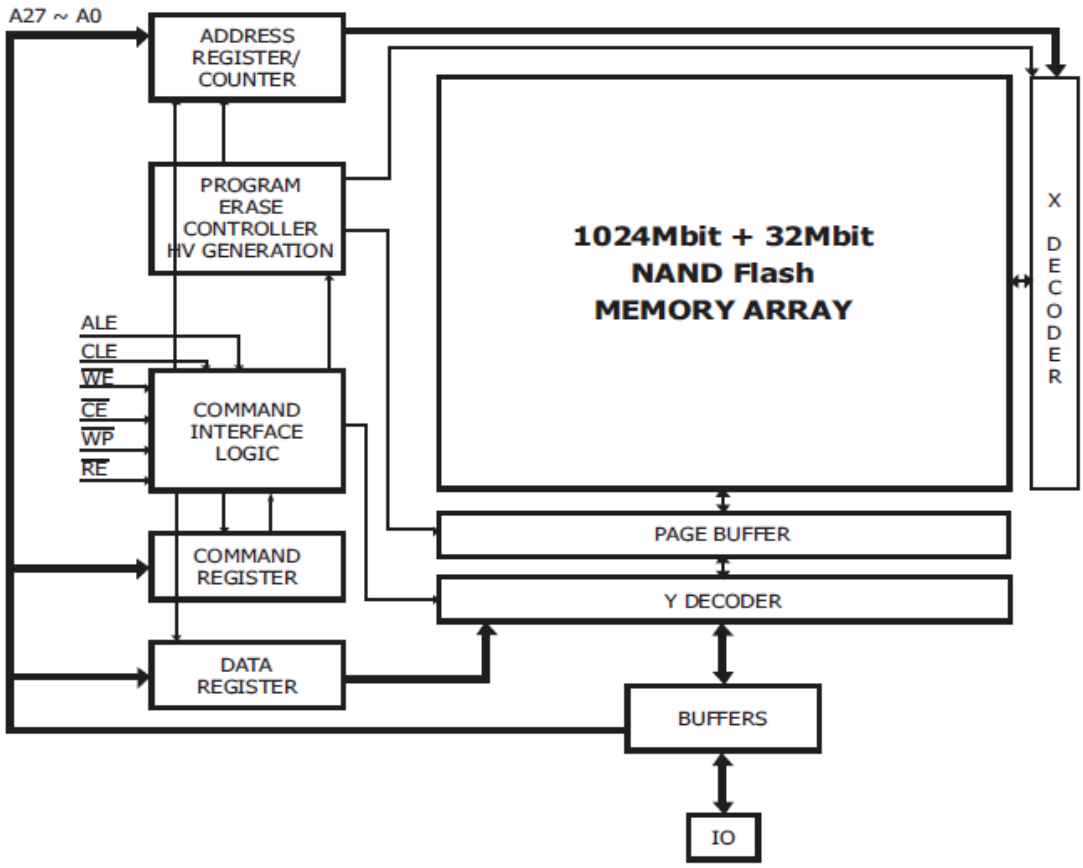
Figure. 3.5.5 POWER SUPPLY BLOCK DIAGRAM

3.6 MEMORY(H8BCS0QG0MMR, U100)



IO15 - IO0	Data Inputs / Outputs
CLE	Command latch enable
ALE	Address latch enable
CE	Chip Enable
RE	Read Enable
WE	Write Enable
WP	Write Protect
R/B	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

The device is offered in 1.8 V Vcc Power Supply, and with x16 I/O interface. Its NAND cell provides the most costeffective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains 1024 blocks, composed by 64 pages. A program operation allows to write the 1056 words page in typical 200 us and an erase operation can be performed in typical 2.0 ms on a 128 K byte block.
Data in the page can be read out at 45 ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.
Commands, Data and Addresses are synchronously introduced using CE, WE, RE ALE and CLE input pin. The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the WP input.



The chip supports CE don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE transitions do not stop the read operation.
The output pin R/B (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/B pins can be connected all together to provide a global status signal.
Even the write-intensive systems can take advantage of the H27S1G6F2B Series extended reliability of 100 K program/ erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.
The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Data read out after copy back read is allowed
This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

3.7 BT module

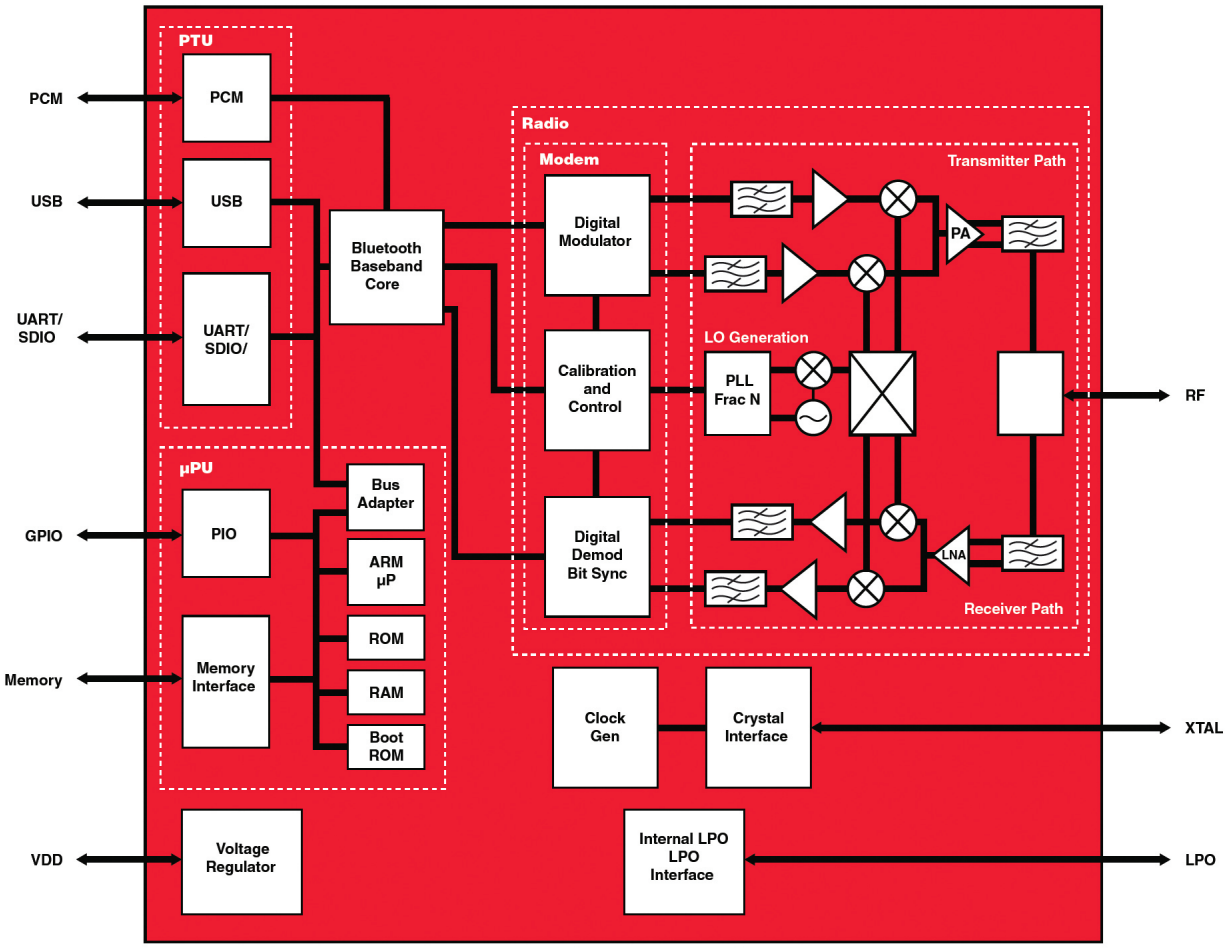


Figure 3_7_1. BT BLOCK DIAGRAM

This module has an integrated radio transceiver that has been optimized for use in 2.4GHz Bluetooth Wireless systems. It has been designed to provide low-power, robust communications for applications Operating in the globally available 2.4GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and enhanced data rate specification and meets or exceed the requirement to provide the highest communication link quality of service.

3.7.1 Transmitter path

This module features a fully integrated zero IF transmitter. The baseband transmitted data Is digitally modulated in the modem block and up-converted the 2.4GHz ISM band in the Transmitter path. The transmitter path consists of signal filtering, I/Q up-conversion, high -output power amplifier(PA), and RF filtering. It also incorporates modulation schemes P/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support enhanced data rate.

• Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift Or anomalies in the modulation characteristics of the transmitted signal and is much more Stable than direct VCO modulation schemes.

• Power Amplifier

The integrated PA for the BCM2070 is configurable for Class 2 operation, transmitting up to +4 dBm as well as Class 1 operation and transmit power up to +12 dBm at the chip, gFSK, >2.5V supply. Due to the linear nature of the PA, combined with some integrated filtering, no External filters are requires for meeting Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications, where Bluetooth is integrated next to the celluar radio, minimal external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions.
Using a highly linearized, temperature compensated design the PA can transmit +12 dBm for Basic rate and +10 dBm for enhanced data rates(2 to 3 Mbps). A flexible supply voltage range Allows the PA to operate from 1.2V to 3.0V. The minimum supply voltage at VDDTF is 1.8V to achieve +10dBm of transmit power.

3.7.2 Receiver path

The receiver path uses a low IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of Linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4GHz ISM bnad. The front-end topology, with built-in out -of-bnad attenuation, enables the device to be used in most applications with no off-chip Filtering. For integrated handset operation where the Bluetooth function is integrated close to the celluar transmitter, minimal external filtering is required to eliminate the desensitization of The receiver by the cellular transmit signal.

3.8 SIM Card Interface

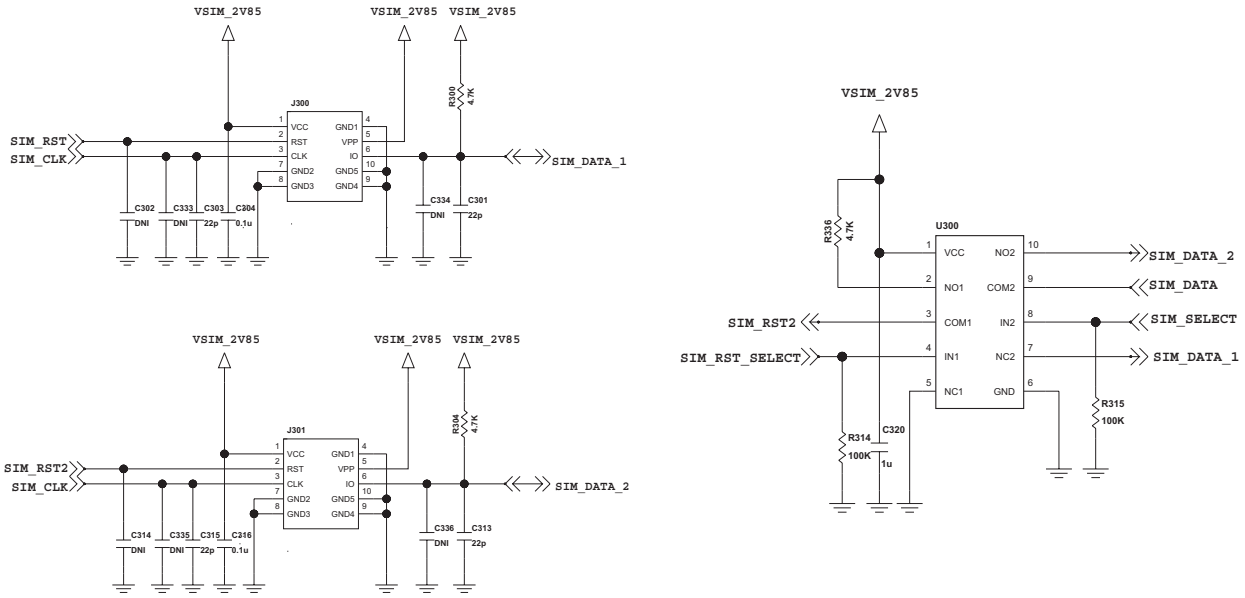


Figure 3-8-1. SIM CARD Interface

The Main Base Band Processor(XMM2150) provides SIM Interface Module.
The XMM2150 checks status Periodically During established call mode whether SIM card is inserted or not, but it doesn't check during deep sleep mode. In order to communicate with SIM card, 3 signals SIM_DATA, SIM_CLK, SIM_RST.
And This model supports 1.8/3V SIM Card.

Signal	Description
SIM_RST SIM_RST2	This signal makes SIM card to HW default status.
SIM_CLK	This signal is transferred to SIM card.
SIM_DATA1 SIM_DATA2	This signal is interface datum.

3.9 LCD Interface

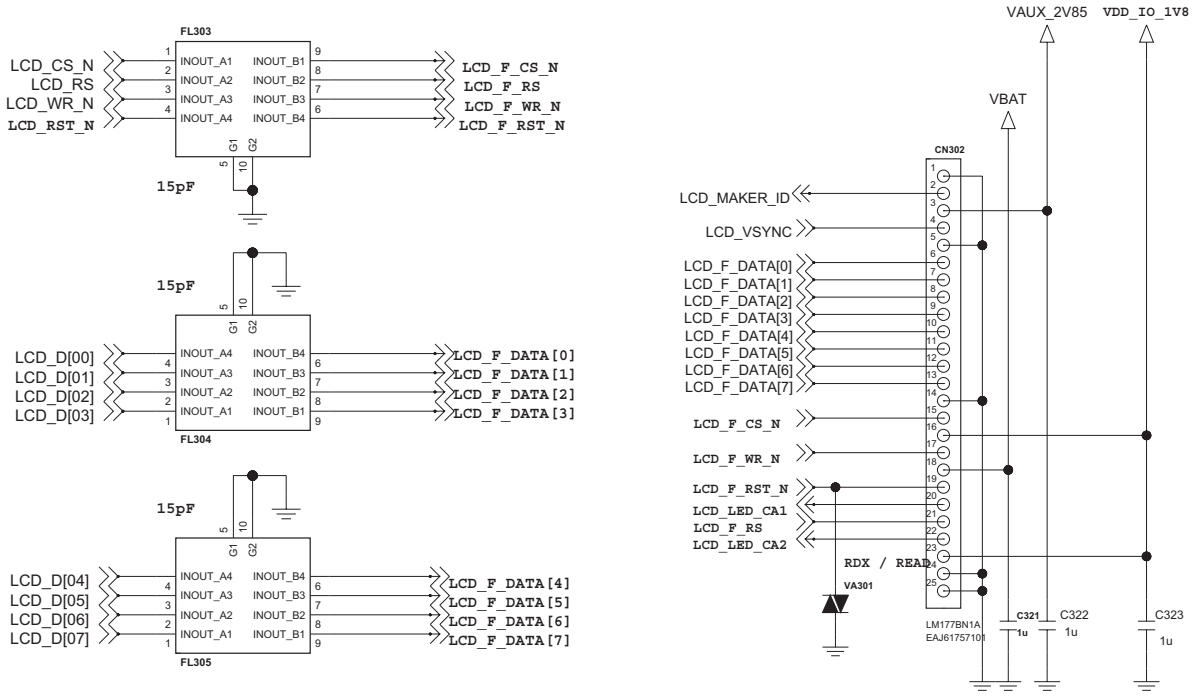


Figure 3-9-1. LCD Interface of LCD FPCB

ILI9163C is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 132RGBx162 dots, comprising a 396-channel source driver, a 162-channel gate driver, 8,114bytes G RAM for graphic data of 132RGBx162 dots, and power supply circuit.

The ILI9163C supports 18-/16-/9-/8-bit data bus interface and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

ILI9163C can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9163C also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9163C an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

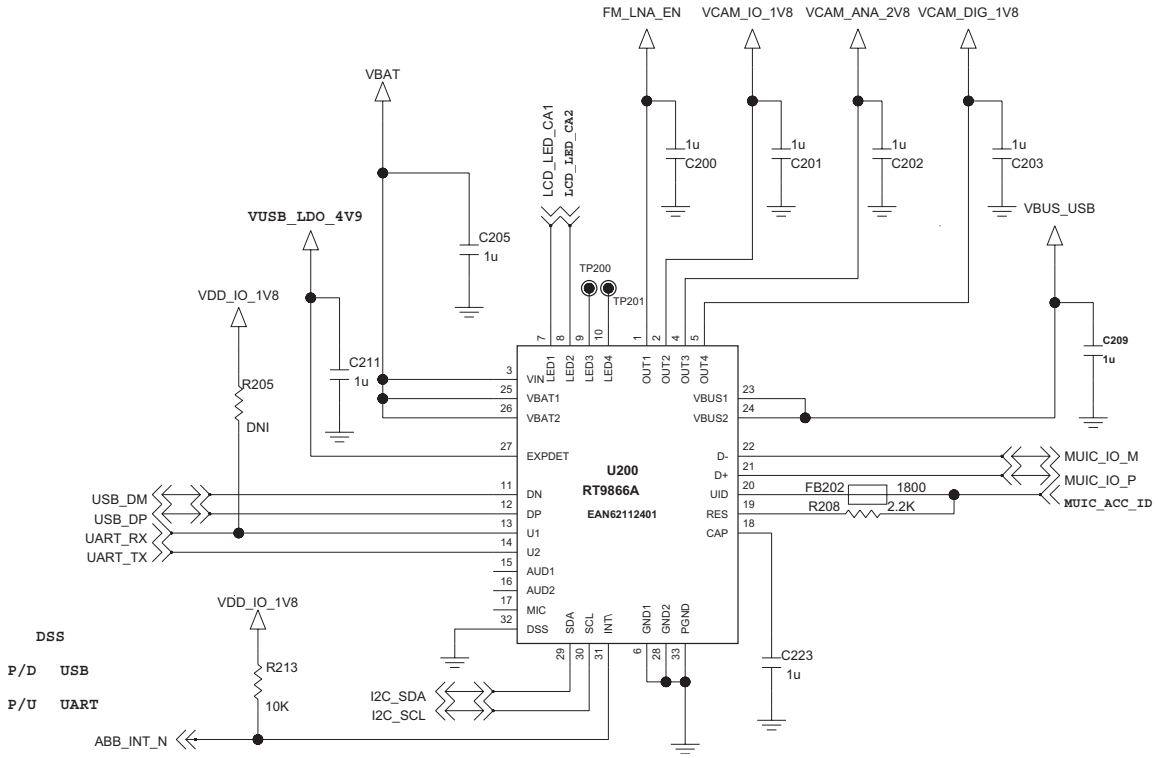


Figure 3-9-2. RT8966AGQW CIRCUIT DIAGRAM

The RT8966AGQW is a power management IC (PMIC) for backlighting and phone camera applications.
The PMIC contains a 6-Channel charge pump white LED driver and four low dropout linear regulators.
The charge pump drives up to 6 white LEDs with regulated constant current for uniform intensity.
Each channel (LED1 to LED6) supports up to 25mA of current. These 6-Channels can be also programmed as 4 plus 2-Channels or 5 plus 1-Channels with different current setting for auxiliary LED application.
The RT8966AGQW maintains highest efficiency by utilizing a x1/ x1.5/ x2 fractional charge pump and low dropout current regulators. An internal 6-bit DAC is used for backlight brightness control. Users can easily configure up to 64-steps of LED current via the I2C interface control. The RT8966AGQW also comprises low noise, low dropout regulators, which provide up to 200mA of current for each of the four channels.
The four LDOs deliver 3% output accuracy and low dropout voltage of 200mV @ 200mA.
Users can easily configure LDO output voltage via the I2C interface control. The LDOs also provide current limiting and over-temperature functions. The RT8966AGQW is available in a WQFN-24L 3x3 package.

LED Backlight Current

RT8966AGQW communicates with a host (master) Using the standard I2C 2-wire interface.
The two bus lines of SCL and SDA must be pulled high when the bus is not in use. Internal pull-up resistors are installed. After the START condition, the I2C master sends a chip address. This address is eight bits long, consisting of seven address bits and a following data direction bit (R/W). The RT8966AGQW address is 10101000 (A8h) and is a receive-only (slave) device. The second word selects the register to which the data will be written. The third word contains data to write to the selected register. Figure 2 shows the writing information for the four LDOs as well as for each LED current.
In the second word, the sub-address of the four LDOs is "001" and the sub-address of the LED Driver for different dimming modes are respectively "010", "011" and "100". For the LDO output voltage setting, bits B1 to B4 represent each LDO channel respectively where a "1" indicates selected and a "0" means not selected. The B0 bit controls on/off (1/0) mode for the selected LDO channel(s).
Then, in the third word, bite C0 to C3 control a 16-step setting of LDO1 to LDO4.The voltage values are listed in Table 1. For LED dimming, there are three operating modes (Backlight I, Backlight II and Backlight III) to select from by writing respectively "010", "011" and "100" into the First three bits of the second word, It should be noticed that no matter which mode is selected, LED1 to LED3 must be turned on, else LED4 to LED6 can not be Turned on.
When Backlight I is selected, all six LEDs have the same behavior. Their 64-step dimming currents are set by bits C0 to C5, which are listed in Table 2. The bits C6 and C7 determine the fade in/out time of each step as shown in Figure 2. For Backlight II and Backlight III, two sets of LEDs, called Main and Sub, can work separately.

Backlight Quiescent Current

The quiescent current required to operate all four backlights is reduced by 1.5mA when backlight current is set to 4.0mA or less. This feature results in higher efficiency under light-load conditions. Further reduction in quiescent current will result from using fewer than four LEDs.

3.10 Battery Charger Interface

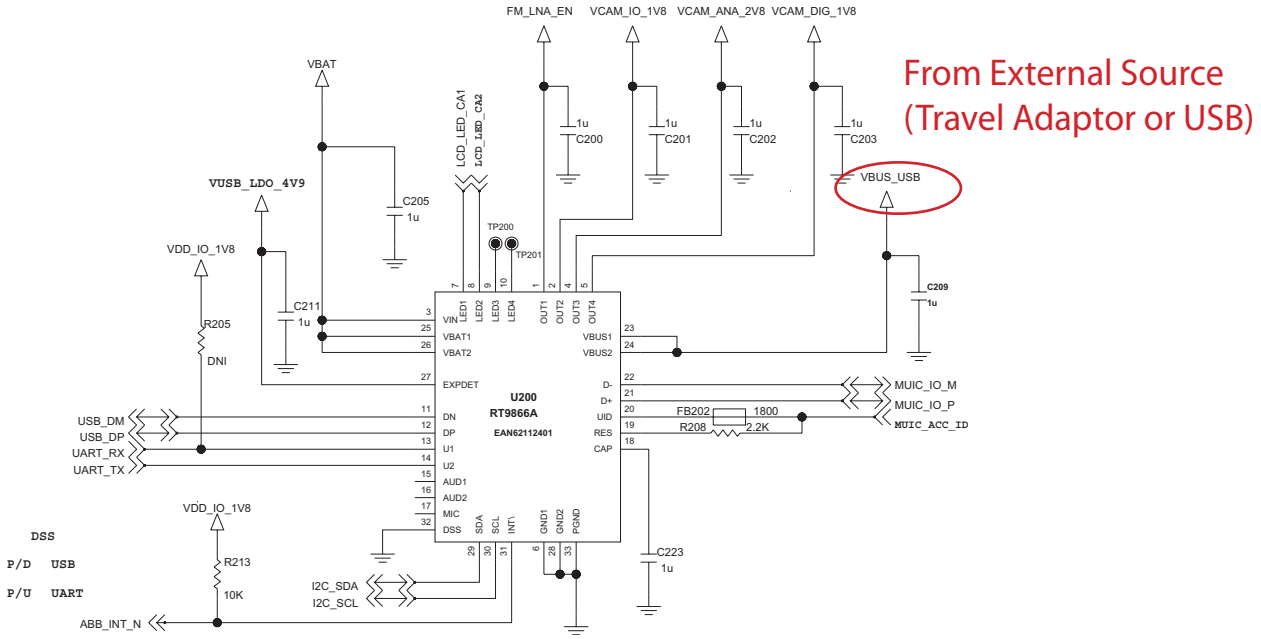


Figure 3-10-1 BATTERY CHARGER BLOCK

The RT8966 integrates a single-cell Li-ion battery charger IC with pre-charge mode, a fast charge mode (constant current mode) or constant voltage mode. The charge current is programmable via the I2C interface as shown in the control register address tables, CHG_Ctrl1 and CHG_Ctrl2. The CV mode voltage is fixed at 4.2V. The pre-charge threshold is fixed at 2.6V. If the battery voltage is below the pre-charge threshold, the RT8966 charges the battery with a trickle current until the battery voltage rises above the pre-charge threshold. The RT8966 is capable of being powered up from AC adapter and USB (Universal Serial Bus) port inputs. Moreover, the RT8966 includes a linear regulator (LDO 4.9V, 50mA) for supplying low power external circuitry.

3.11 Audio Interface

3.11.1 Functional Overview

The audio front-end of X-GOLD™215 offers the digital and analog circuit blocks for both receive and transmit audio operation, from a mobile phone perspective (called audio-in and audio-out subsequently). It features a high-quality, stereo digital-to-analog path with amplifier stages for connecting acoustic transducers to X-GOLD™215. In audio-in path the supply voltage generation for electret microphones, a low-noise amplifier and analog to digital conversion are integrated in X-GOLD™215. A more detailed functional description will be given in the following sections.

The audio front-end itself can be considered to be organized in three sub-blocks:
• Interface to processor cores (TEAKLite® and - indirectly - ARM)
• Digital filters
• Analog part

The following figure shows an architecture overview of the Audio section.

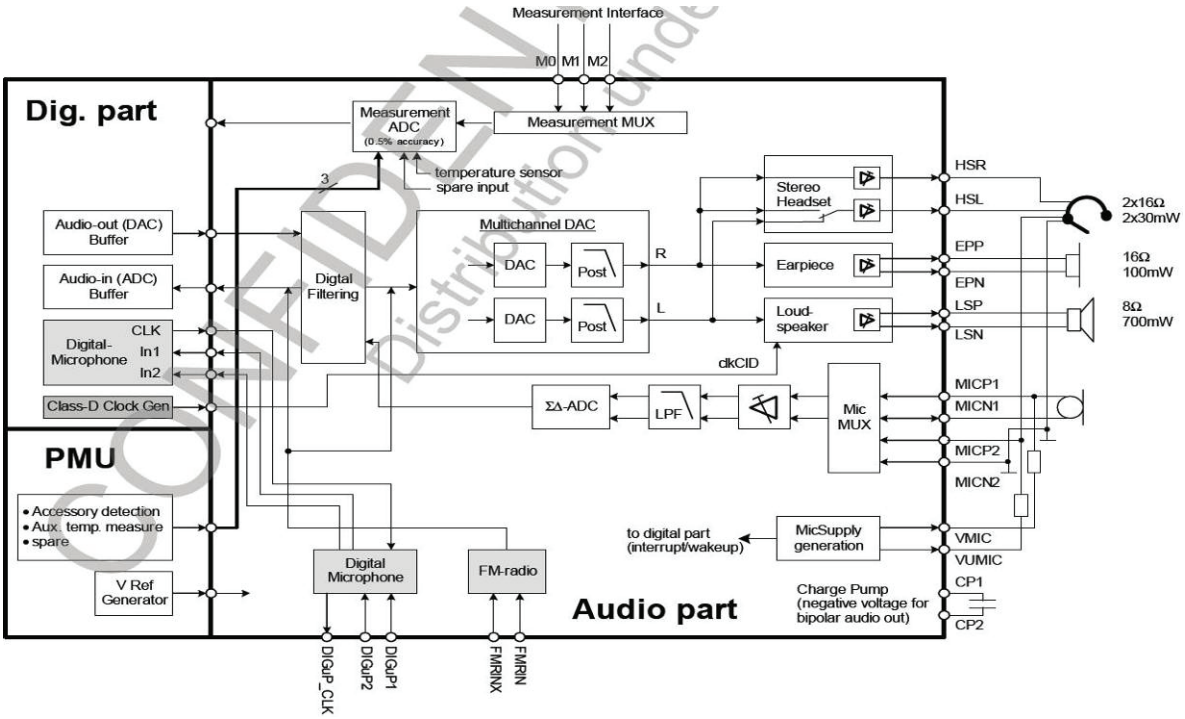


Figure 3.12.1 Audio Section Overview

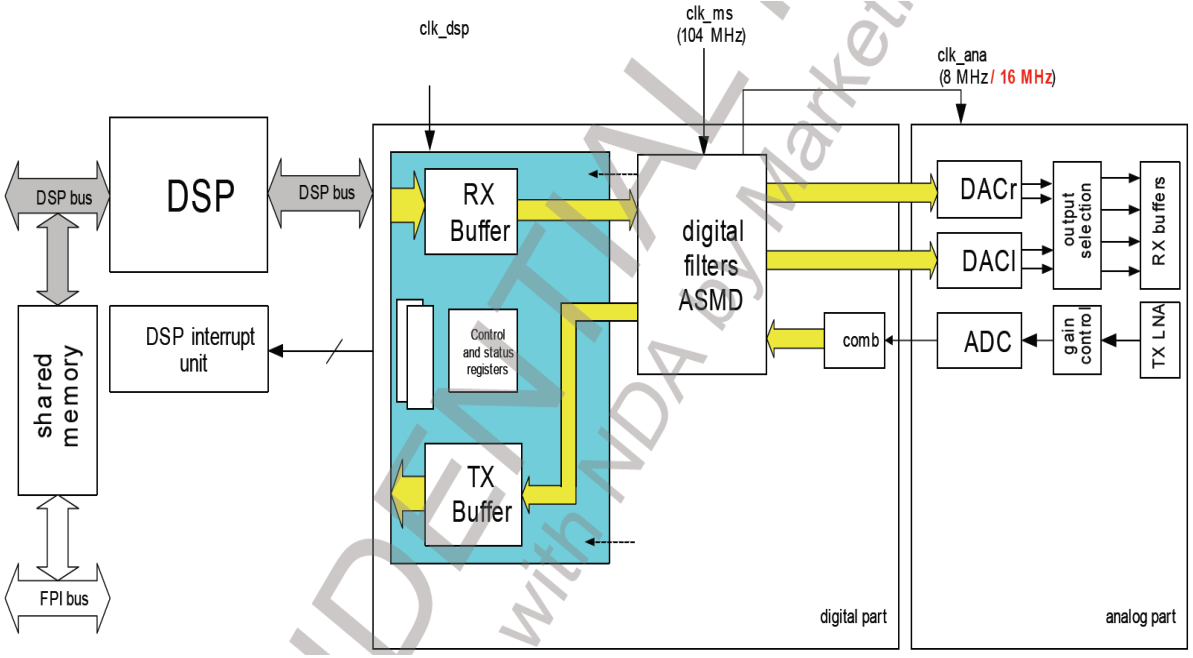


Figure 3.12.2 Overview of Clocking and Interfaces of Audio Front End

The audio front-end of X-GOLD™215 has the following major operation modes:

- Power-down: All analog parts are in power down and all clocks of the digital part are switched off.
- Audio mode: Digital decimation/interpolation filters are connected to the interface buffers and the analog part is enabled.

These major modes can be modified by certain control register settings.

- Due to the new gain settings in the TX path, the maximum input voltage is limited to 0.8 Vpp.
- In both voiceband paths, the value range for voice samples is confined to 97.5%, i.e. to [-31948, 31947] or [8334H, 7CCBH] in X-GOLD™215.
- On the TX path, 83% "1"s on the VTPDM line correspond to a 16-bit value of 7CCBH and 17% "1"s correspond to a 16-bit value of 8334H at the digital filter output. Thus the usable range is 66%. This range can be scaled to 100% by Firmware.
- The high-pass functions of the voiceband filters have to be implemented in firmware on TEAKLite®.

3.11.2 Digital Part

The digital part of the X-GOLD™215 audio front-end comprises an interface to the TEAKLite® bus, interfaces to the interrupt units of TEAKLite®, digital interpolation filters for oversampling digital-to-analog conversion, digital decimation filters for analog-to-digital conversion and an interface to the analog part of the audio front-end. For the digital microphone all the filtering is done in a dedicated hardware. The output sample stream is then fed in a duplicated ring buffer structure like the data from the analog microphone path (after A/D conversion and subsequent digital filtering).

▪ Interpolation Filter

The interpolation path of the X-GOLD™215 audio front-end increases the sampling rate of the audio samples to the rate of the digital-to-analog converter. Because the input sampling rates can vary between 8 kHz and 47.619 kHz the filter characteristic and oversampling ratio can be adjusted to the respective sampling rate. The requirements for the interpolation filters depend on the sampling rate, because a sufficient out-of-band discrimination in the audio frequency band (20 Hz,...,20 kHz) has to be ensured.

▪ Decimation Filter

The digital decimation filter on X-GOLD™215 has two operating modes: 8 kHz output sampling rate and 16 kHz output sampling rate (or 16 kHz output sample rate and 16kHz bandwidth in case of doubled ASMD clock).

3.11.3 Analog Part

The analog part of the X-GOLD™215 audio front-end in audio-out direction consists of a stereo digital to analog converter (multi-bit oversampling converter) which transforms the output of the digital interpolation filter into analog signals. It is followed by the gain control/amplifier section. The DAC outputs can be switched to several output buffers. In audio-in section there is an input multiplexer which selects either one of two differential microphone inputs to be connected to the low-noise amplifier and analog pre-filter. The signals from the analog pre-filter are input to a second-order sigma-delta analog-to-digital converter. In addition there is a connection for FM-radio playing.

▪ Audio-out Part

The analog audio-out part consists of two multi-bit digital-to-analogue converters (DAC) and an output stage. The signal sources are switched to the output drivers in the output stage. The output drivers consist of: a) one mono, differential class-D Loudspeaker driver, b) one mono, differential Earpiece driver and c) one stereo, single-ended (with uni- or bipolar signals), Headset driver.

▪ **Digital-to-analog converters**

The multi-bit oversampling DACs of the X-GOLD™215 audio front-end convert the 16-bit data words coming from the digital interpolation filters to analogue signals.

▪ **Output Amplifier**

The different output buffers in X-GOLD™215 are driven by the outputs of the selection block. The differential earpiece driver can be used to drive a 16 Ω earpiece and works in differential. The two single ended headset drivers can be used to drive a 16 Ω headset. They can work unipolar mode, where an AC coupling of the headset might be needed, or can work also in bipolor mode. The differential loudspeaker driver can be used to drive a 8 Ω loudspeaker. As it is a class-D amplifier the needed suppression of the higher harmonics of the switching signals has to be achieved by the external circuitry. The buffers are designed to be short circuit protected.

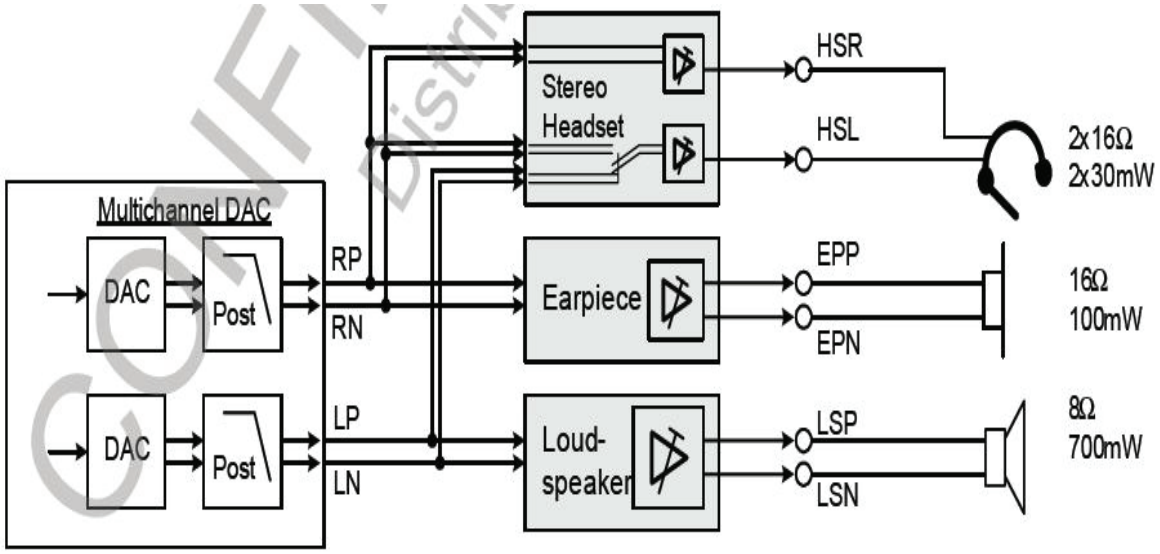


Figure 3.12.3 Switching for R/L DACs onto Buffers

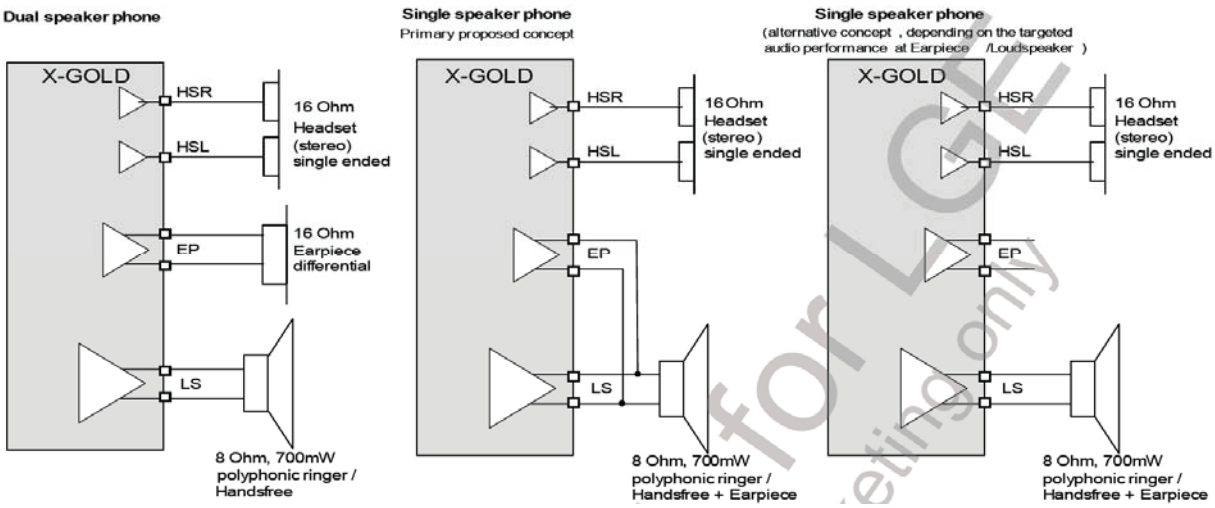


Figure 3.12.4 Different Application Scenarios

In order to achieve the single-speaker concept by parallel connection of Earpiece and Headset amplifier the Earpiece amplifier have to sustain the up to 5 V voltage of the class-D amplifier.

▪ Audio-in Path

The audio-in path of X-GOLD™215 provides two differential microphone input sources, MIC1and MIC2.

• The inputs for microphone MIC1 are MICP1 and MICN1.
• The inputs for microphone MIC2 are MICP2 and MICN2.

The audio-in path consists of an input selector, a low noise amplifier and following pre-filter with gain control, a second order ΣΔ-converter and a digital decimation filter. It supports both standard GSM (bandwidth 3.5 kHz) and wideband (bandwidth 7 kHz) speech bands.
The differential input signal from the microphone first passes a low noise amplifier and following pre-filter and an anti-aliasing pre-filtering stage achieving and overall variable gain ranging from 0 dB to +39 dB . The signal is then modulated by a second order ΣΔ-converter which is clocked with the same clock rate as the digital to analog converters. The ΣΔ-converter delivers a 1-bit pulse density modulated data stream at a rate of 2 MHz to the digital decimation filter which reduces the rate to 8 kHz or 16 kHz, depending on the current mode.
To improve SNR the sample frequency can be doubled in dedicated modes and the modulated data stream is 4MHz instead of 2 MHz.

▪ Microphone Supply

X-GOLD™215 has a single ended power-supply concept for electret microphones:
For both modes a minimal load capacitance of t.b.d. nF is necessary to guarantee stable operation of the buffer.
The maximal load capacitance must not exceed t.b.d. nF.
2 microphone supplies VMIC and VUMIC are available. The supply VUMIC has a ultra-low-power mode, where the current consumption is minimum, whilst at the same time the noise performance is reduced.
For this purpose the VUMIC is directly supplied out of the VMIC regulator, the Mic-Buffer can be switched off and only the quiescent current of the VMIC regulator is present. This mode can be used to supply a headset and allow accessory detection with highly reduced current consumption For normal operation the supply can be switched to normal operation mode with improved noise performance. In case of an digital microphone VMIC can be used for supplying this microphone.

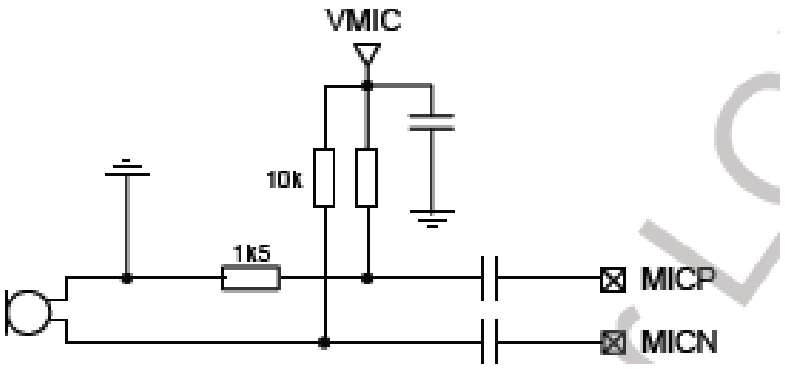


Figure 3.12.5 Typical Microphone Supply Generation (alternative)

3.12 Camera Interface(1.3M Fixed Focus Camera)

3.12.1 PMB8815 Camera Interface

The Camera Interface (CIF) represents a complete video and still picture input interface (see Figure 26).

The CIF contains image processing, scaling, and compression functions. The integrated image processing unit supports image sensors with integrated YC_bC_r processing.
Scaling is used for downsizing the sensor data for either displaying them on the LCD, or for generating data streams for MPEG-4 compression. In general, YC_bC_r 4:2:2 JPEG compressed images should use the full sensor resolution, but they can also be downscaled to a lower resolution for smaller JPEG files. Scaling also can be used for digital zoom effects, because the scalers are capable of up-scaling as well.
CIF
All data is transmitted via the memory interface to an AHB bus system using a bus master interface.
Programming is done by register read/write transactions using an AHB slave interface.

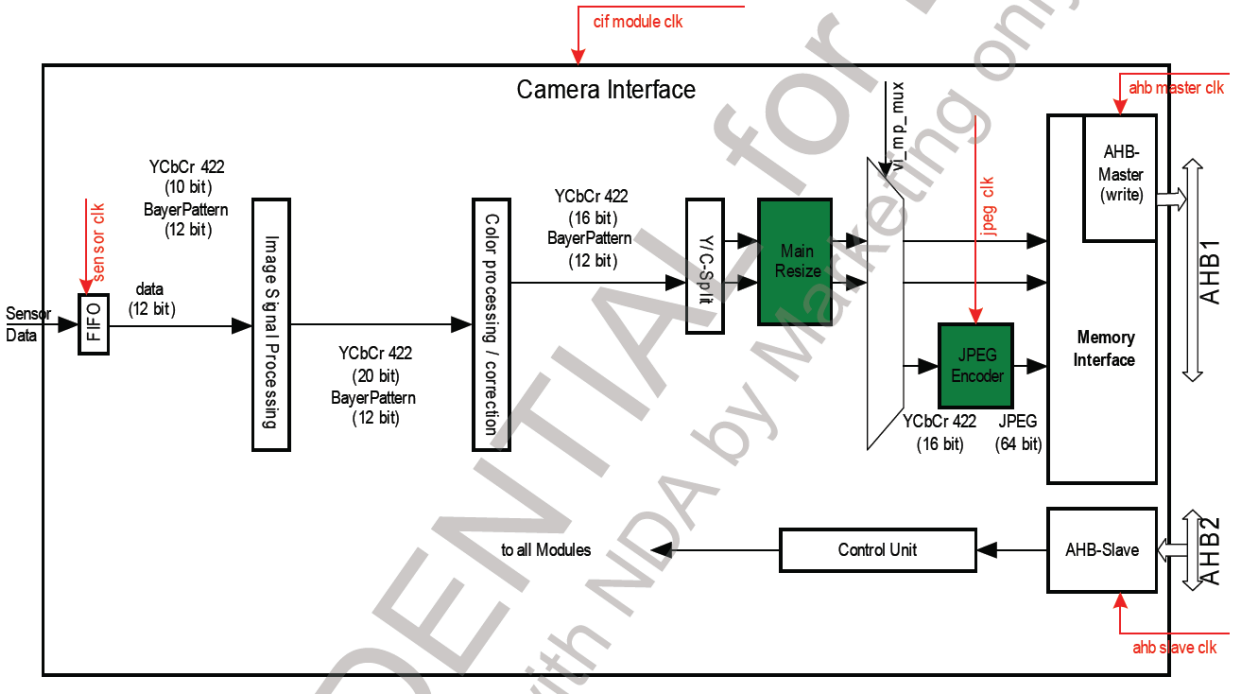


Figure 3.12.1 Block Diagram of Camera Interface

Functional Overview of CIF

The following list gives an overview over the CIF's functionality:

- 78 MHz system clock
- 78 MHz sensor clock
- 78 MHz JPEG encoder clock
- 32-bit AHB slave programming interface
- ITU-R BT 601 compliant video interface supporting YC_bC_r
- ITU-R BT 656 compliant video interface supporting YC_bC_r data
- 8-bit camera interface
- 12-bit resolution per color component internally
- YC_bC_r 4:2:2 processing
- Hardware JPEG encoder incl. JFIF1.02 stream generator and programmable quantization and Huffman tables
- Windowing and frame synchronization
- Continuous resize support
- Frame skip support for video (e.g. MPEG-4) encoding
- Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
- Programmable polarity for synchronization signals
- Luminance/chrominance and chrominance blue/red swapping for YUV input signals
- Maximum input resolution of 3 Mpixels (2048x1536 pixels)
- Main scaler with pixel-accurate up- and down-scaling to any resolution between 3 MP (2048x1536) and 32x16
- pixel in processing mode
- Buffer in system memory organized as ring-buffer
- Buffer overflow protection for raw data and JPEG files
- Asynchronous reset input, software reset for the entire IP and separate software resets for all sub-modules
- Interconnect test support
- Semi planar storage format
- Color processing (contrast, saturation, brightness, hue)
- Power management by software controlled clock disabling of currently not needed sub-modules

4. TROUBLE SHOOTING

4.1 RF Component

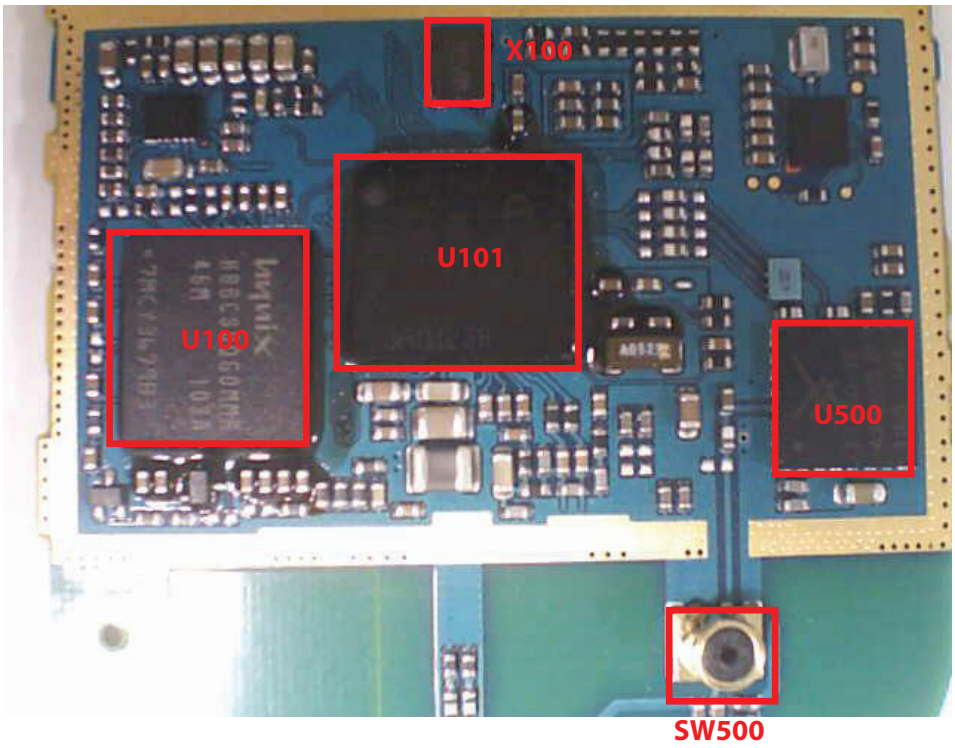
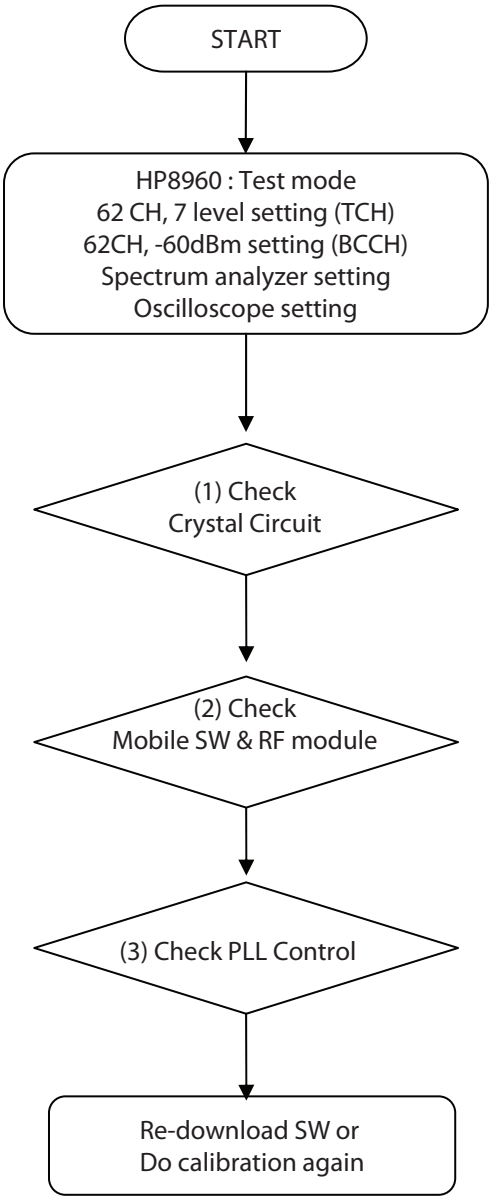


Figure 4.1

U100	Memory (1G/512DDR)
U101	Main Chip (IFX_XMM215x_NAND)
U500	RF Module (SKY77550)
X100	Crystal, 26MHz Clock
SW500	RF Switch

4.2 RX Trouble

CHECKING FLOW



(1) Checking Crystal Circuit

TEST POINT

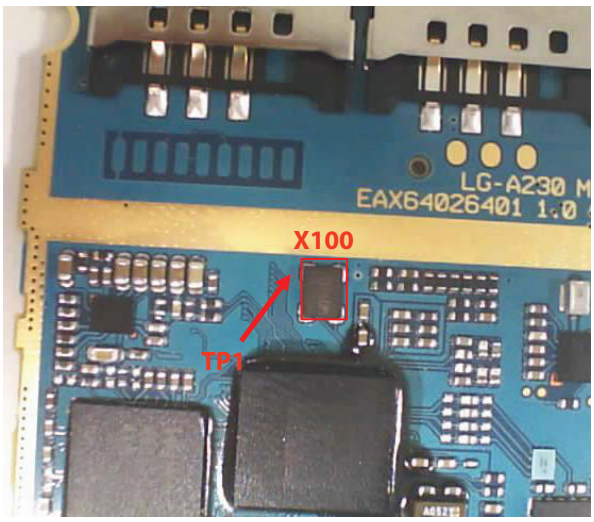
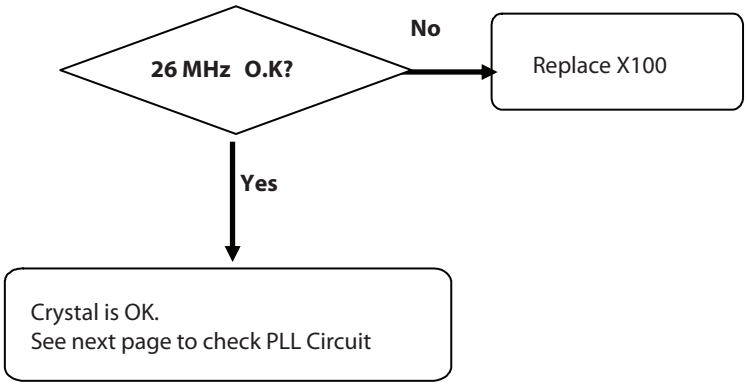


Figure 4.2.1

CHECKING FLOW



CIRCUIT

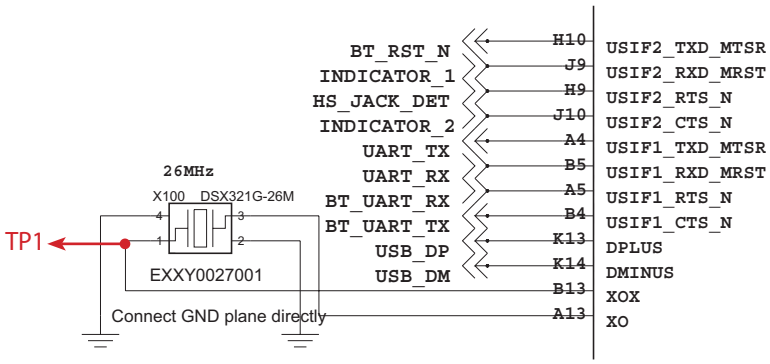


Figure 4.2.2

WAVEFORM

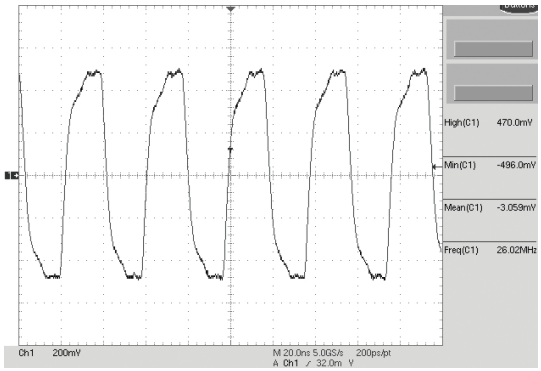


Figure 4.2.3

(2) Checking Mobile SW &FEM

TEST POINT

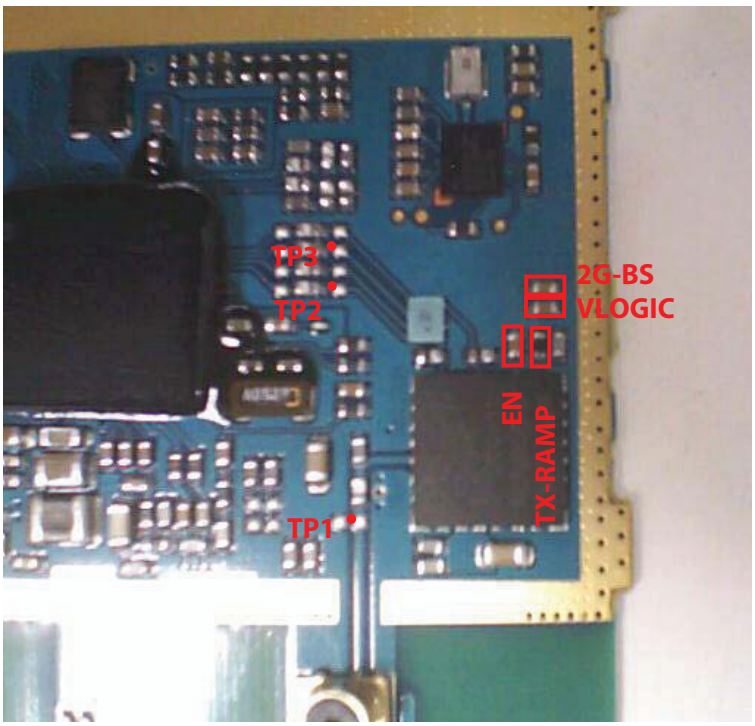
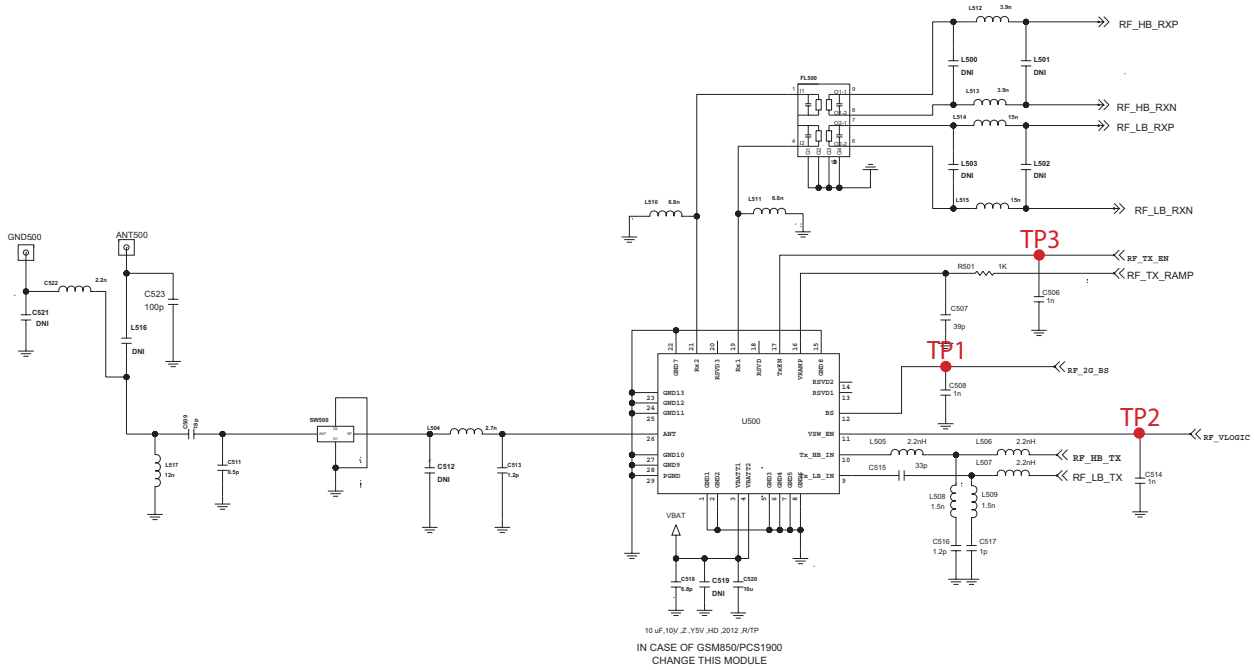


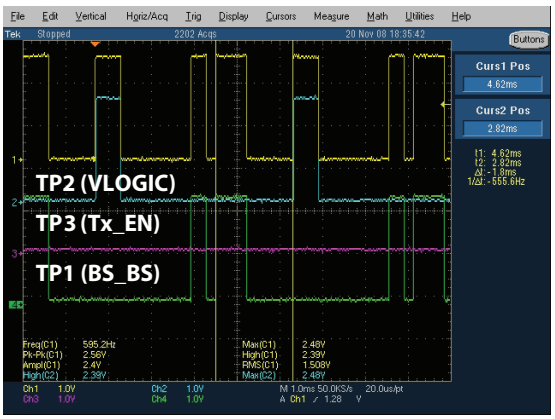
Figure 4.2.4

CIRCUIT

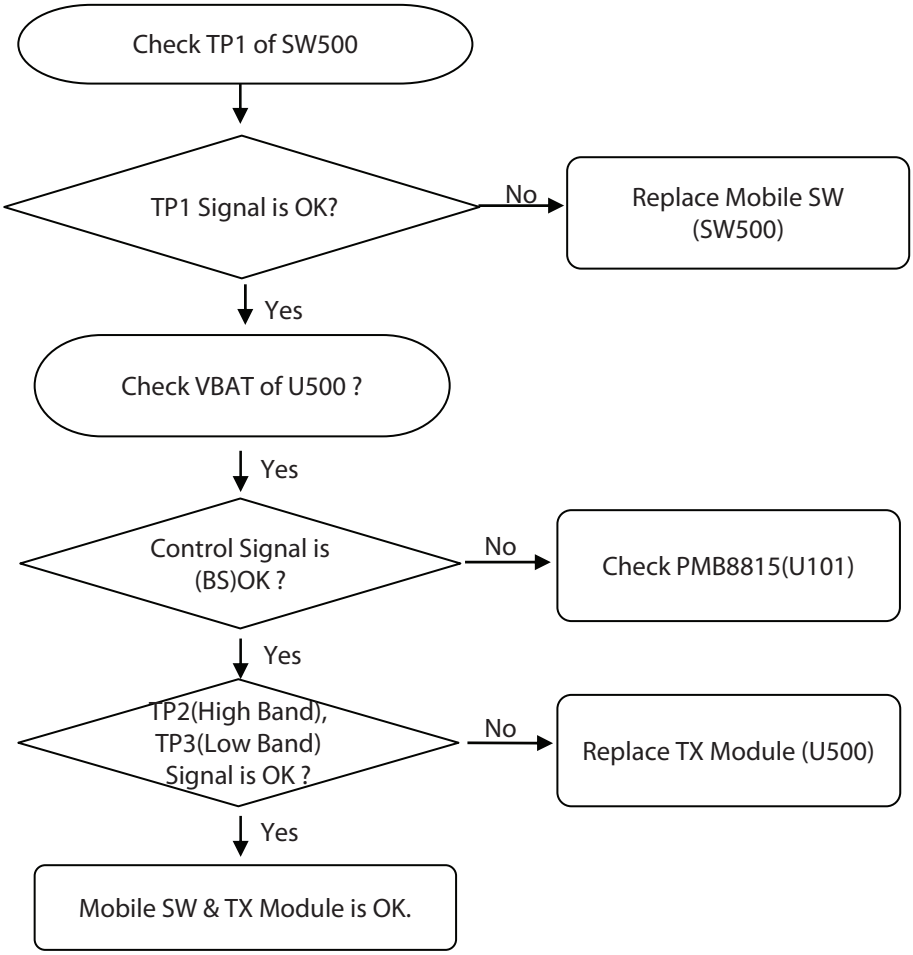


CONTROL LOGIC

EGSM Rx



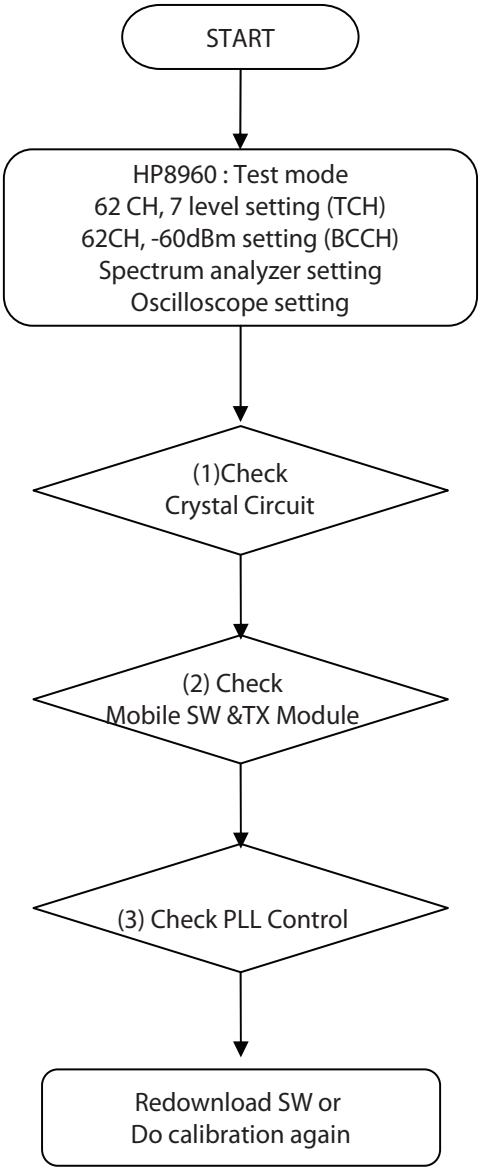
CHECKING FLOW



Mode	Input Control Bits		
	V_{SW_EN}	TxEN	BS
STANDBY	0	0	0
Rx1[1]	1	0	0
Rx2[1]	1	0	1
Tx_LB	1	1	0
Tx_HB	1	1	1

4.3 TX Trouble

CHECKING FLOW



(1) Checking Crystal Circuit

TEST POINT

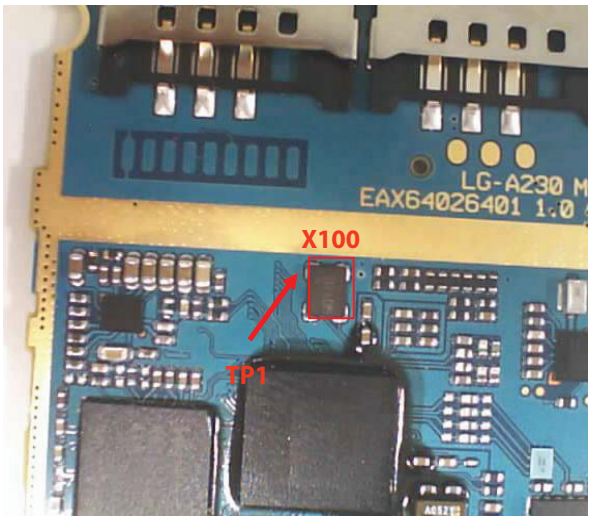
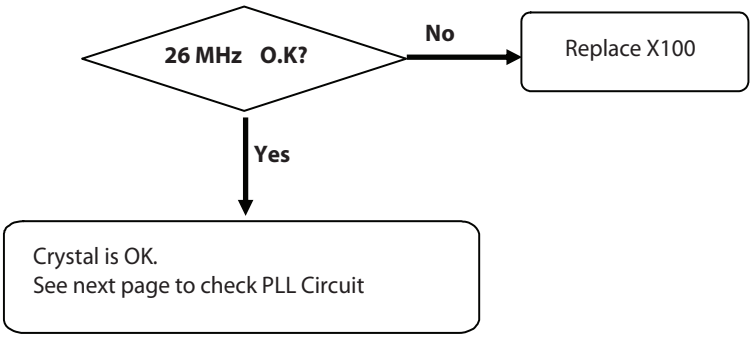


Figure 4.3.1

CHECKING FLOW



CIRCUIT

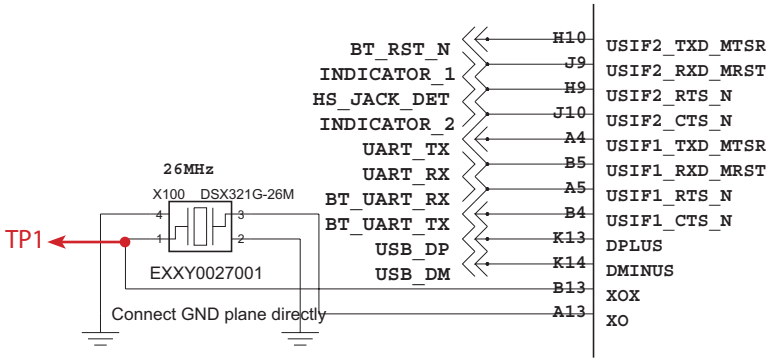


Figure 4.3.2

WAVEFORM

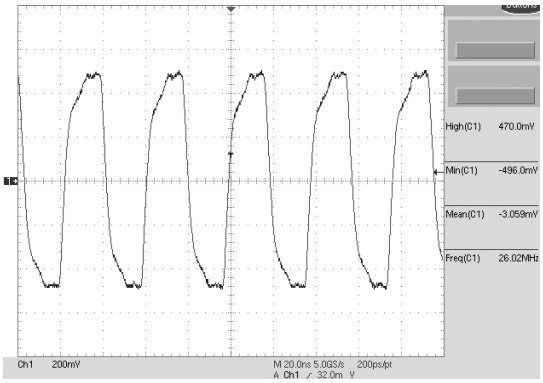


Figure 4.3.3

(2) Checking Mobile SW & TX Module

TEST POINT

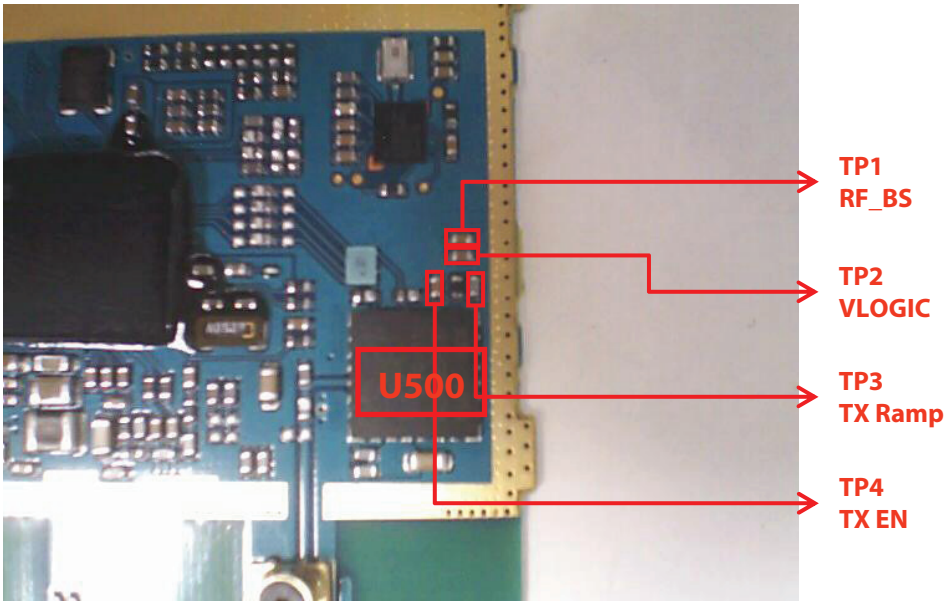
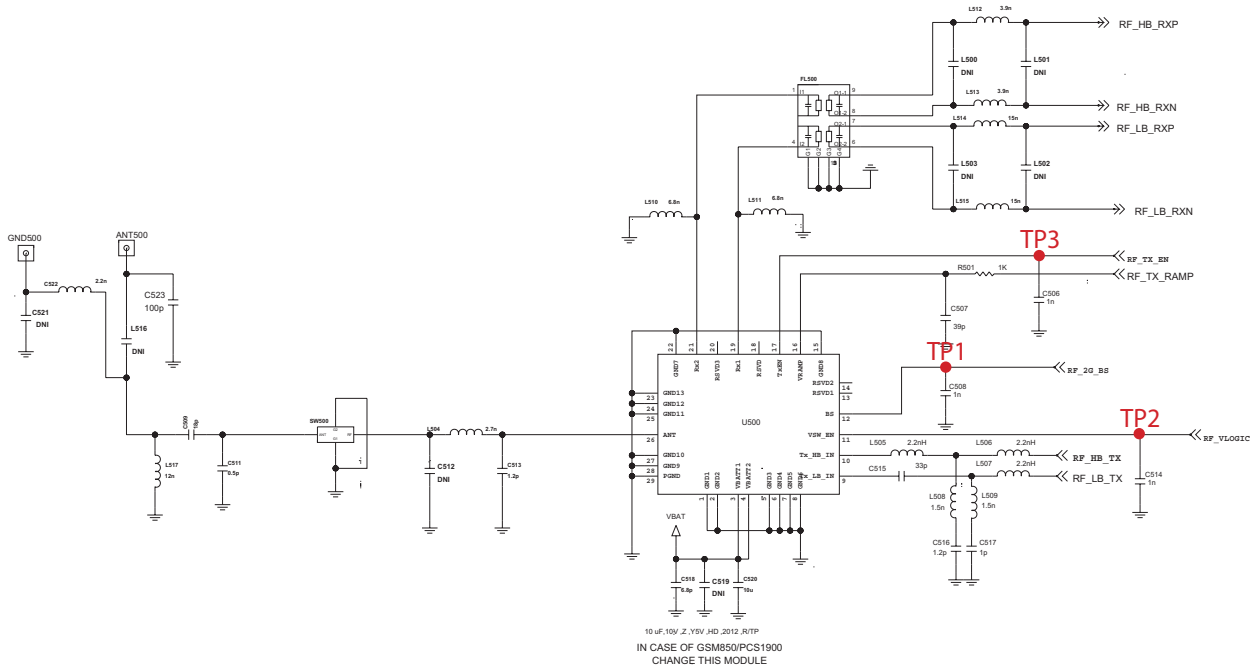


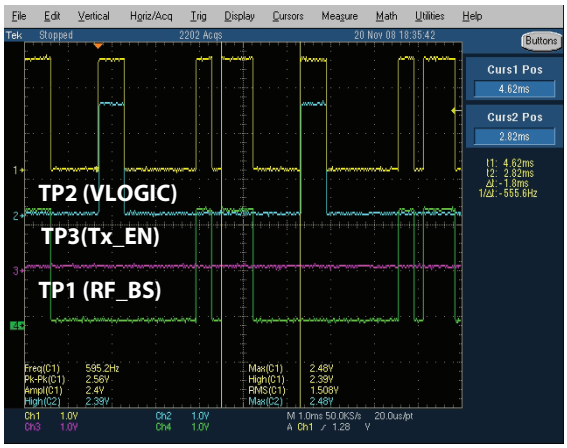
Figure 4.3.4

CIRCUIT

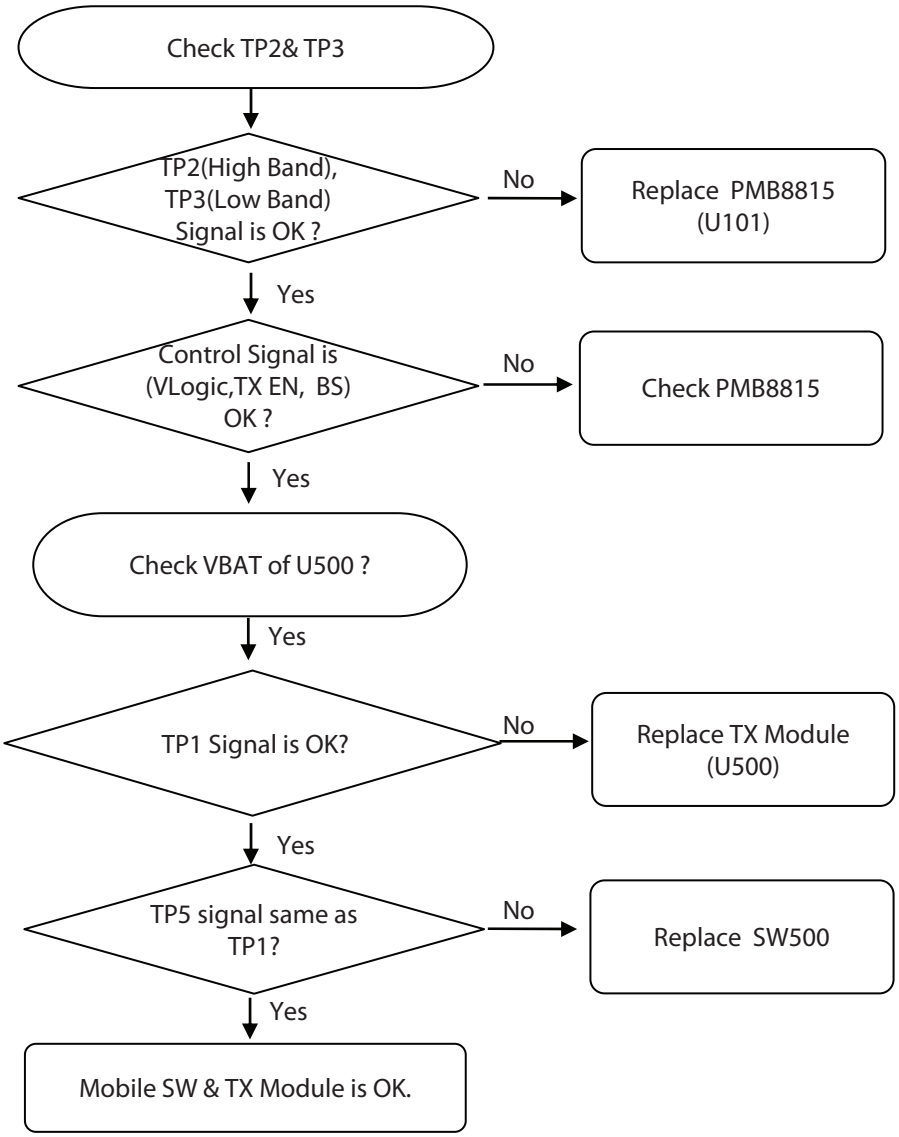


CONTROL LOGIC

Low Band(850/900)Tx



CHECKING FLOW



Low Band(850/900) Tx

Mode	Input Control Bits		
	V_{SW_EN}	TxEN	BS
STANDBY	0	0	0
Rx1[1]	1	0	0
Rx2[1]	1	0	1
Tx_LB	1	1	0
Tx_HB	1	1	1

4.4 Power On Trouble

TEST POINT

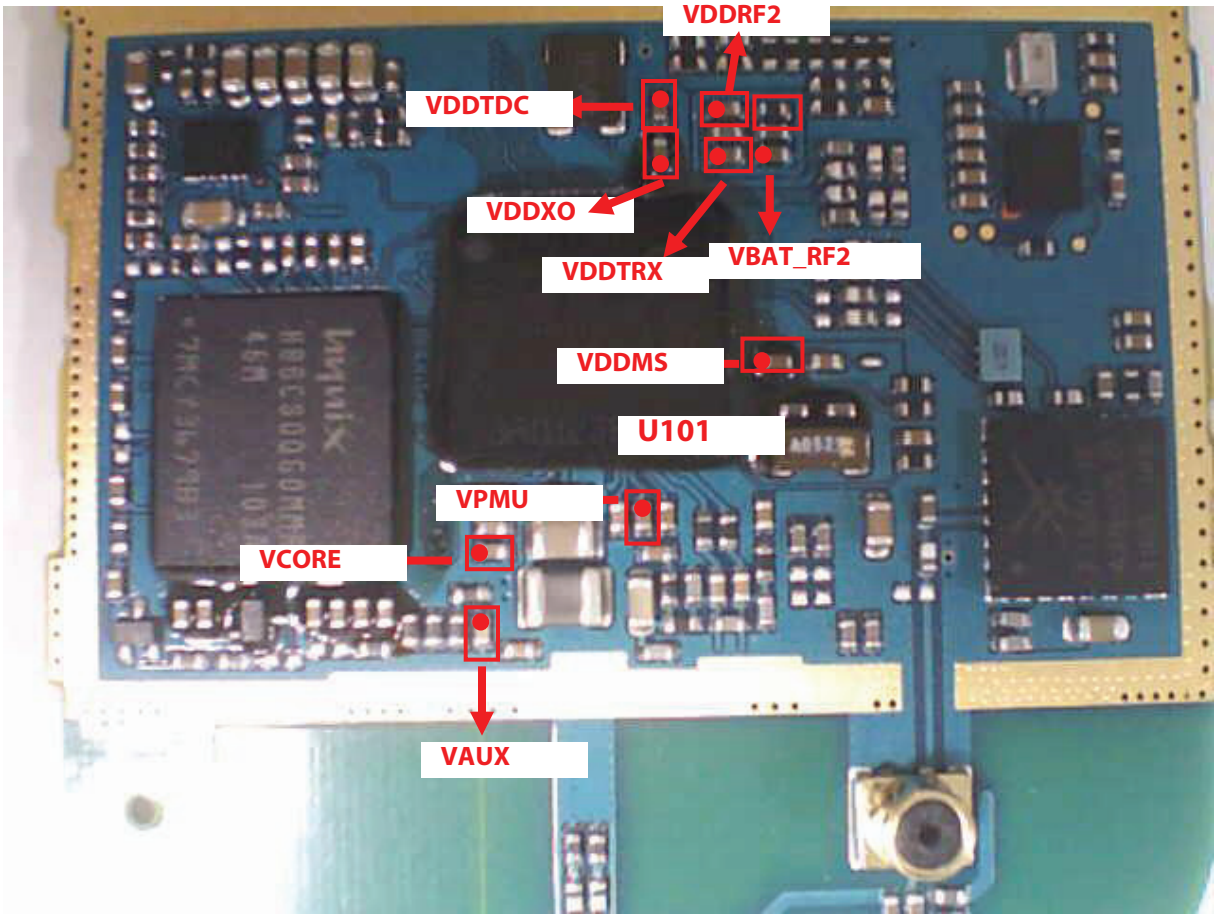


Figure 4.1

CIRCUIT

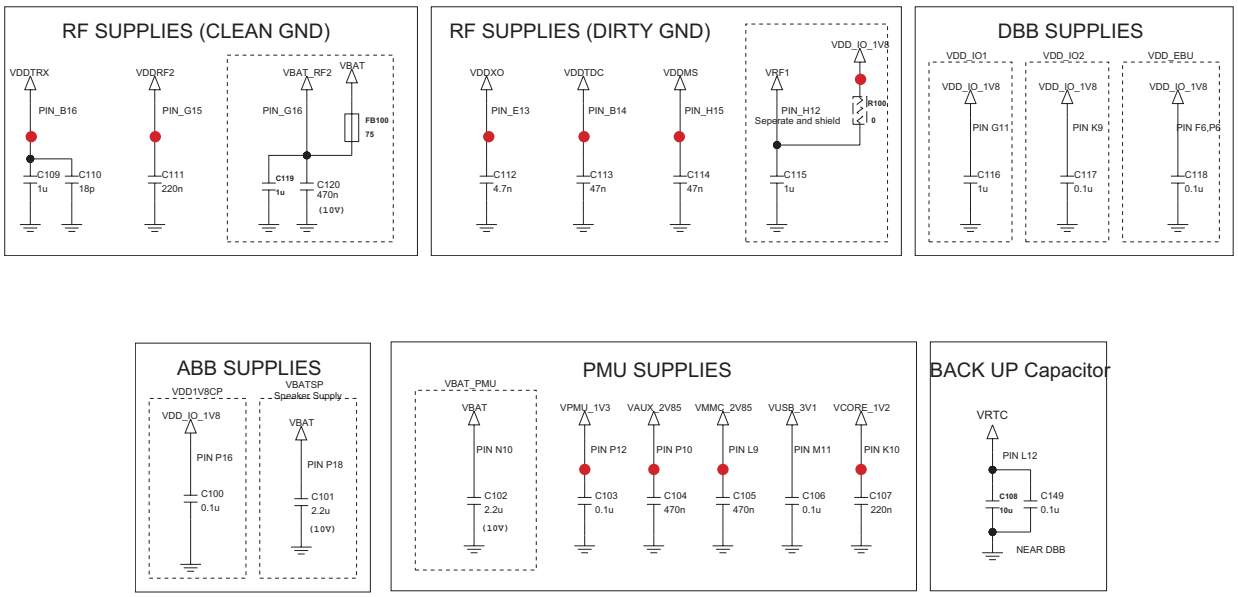
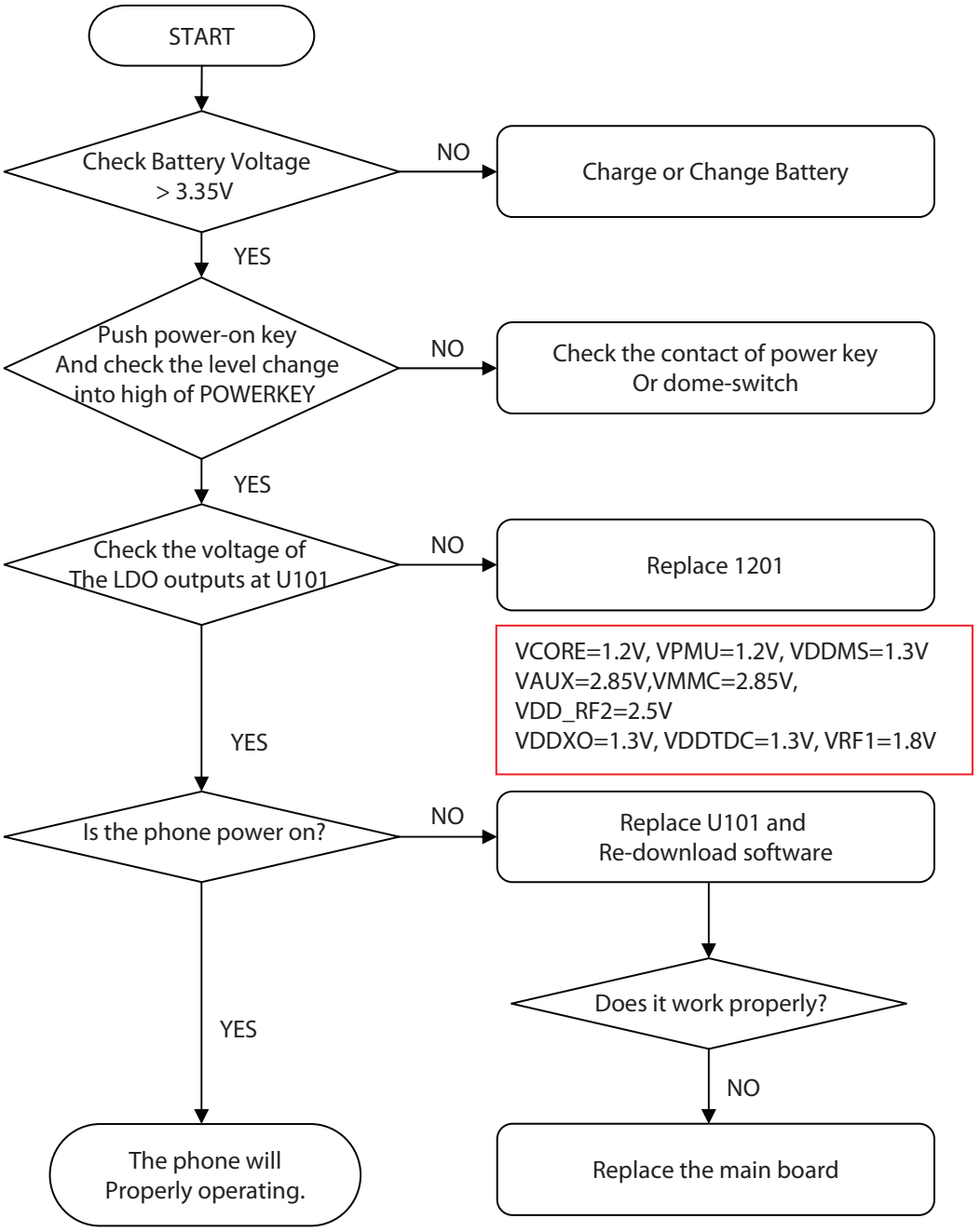


Figure 4.5.4 power block of LG-A230

CHECKING FLOW



4.5 Charging Trouble

TEST POINT

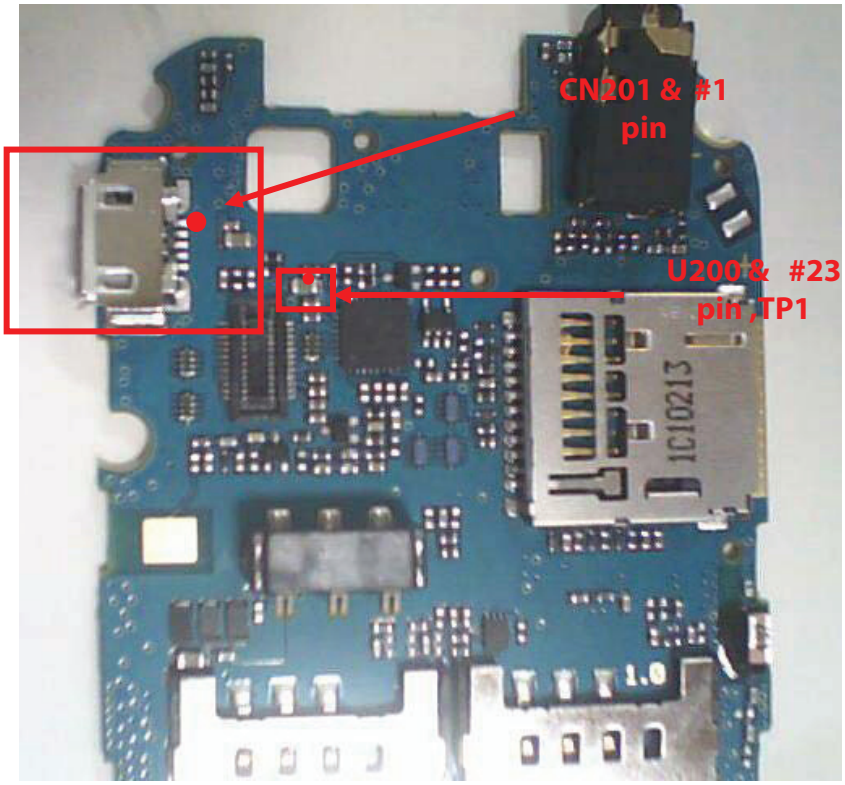
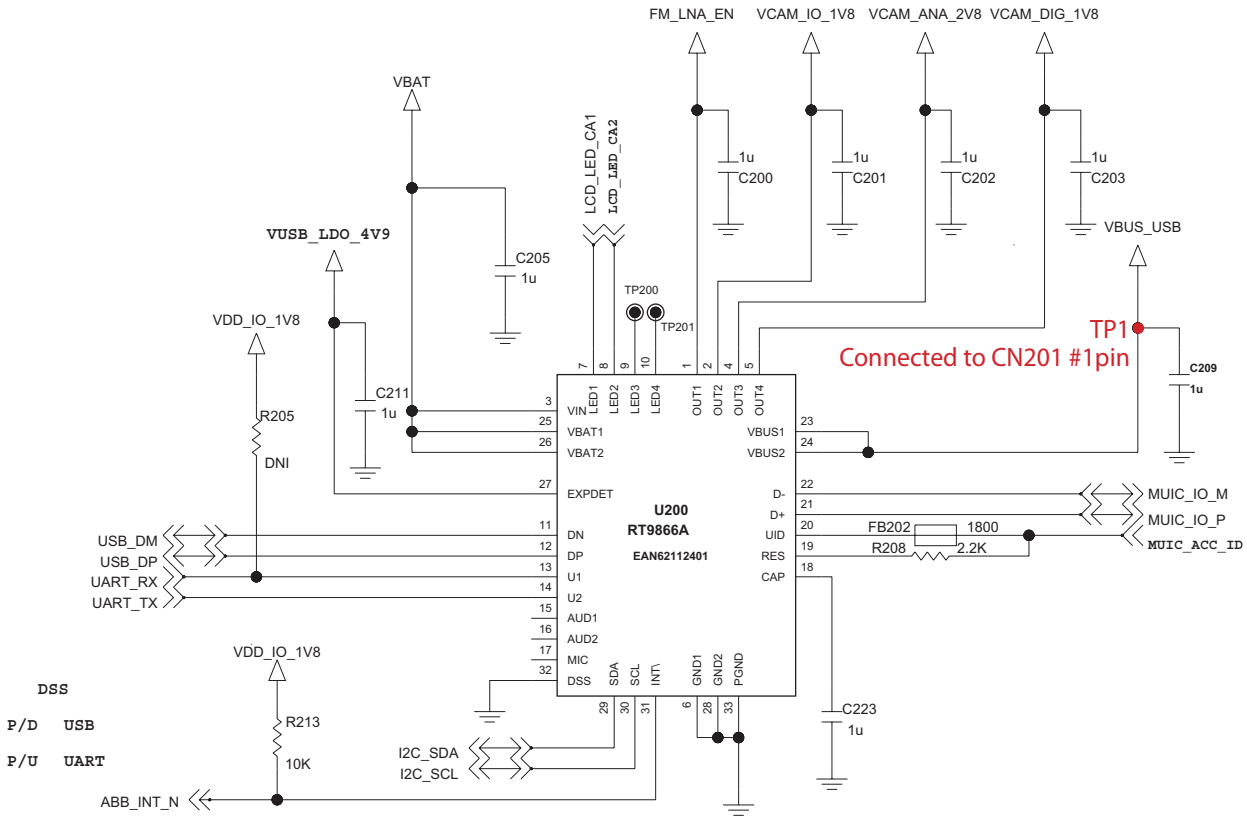
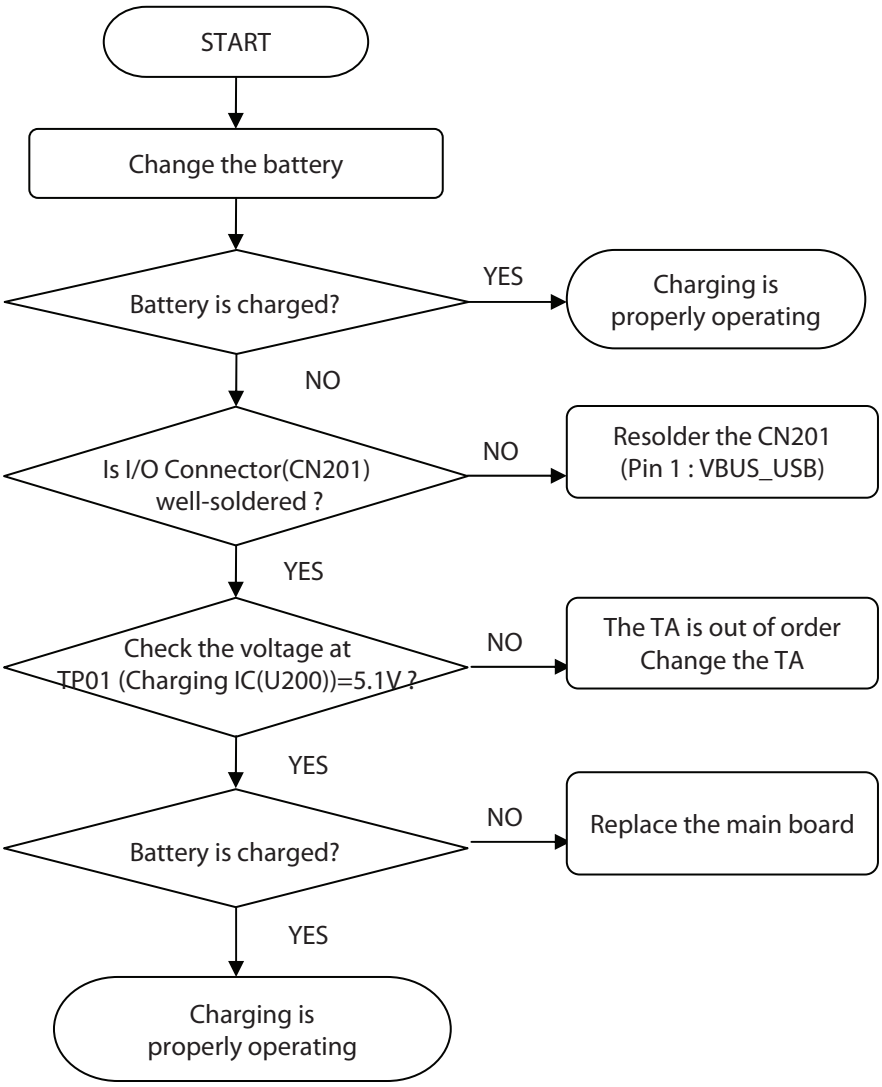


Figure 4.5

CIRCUIT



CHECKING FLOW



4.6 Vibrator Trouble

TEST POINT

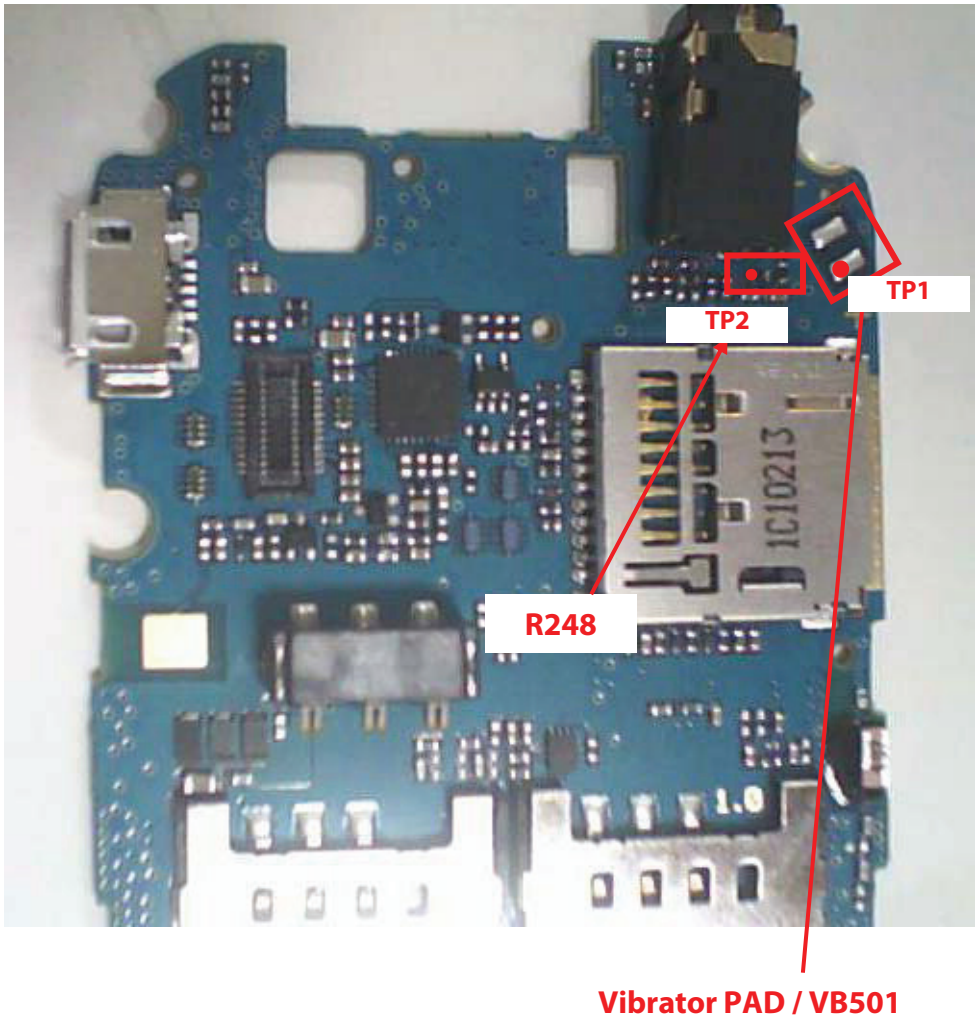
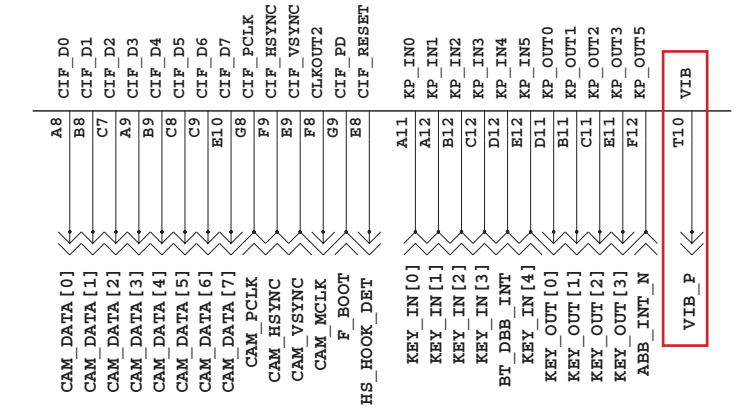
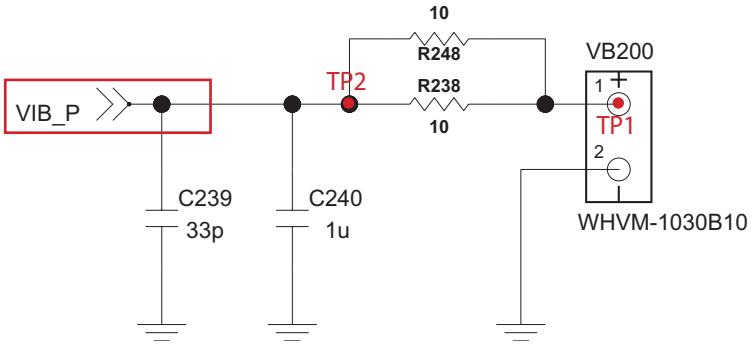


Figure 4.6

CIRCUIT

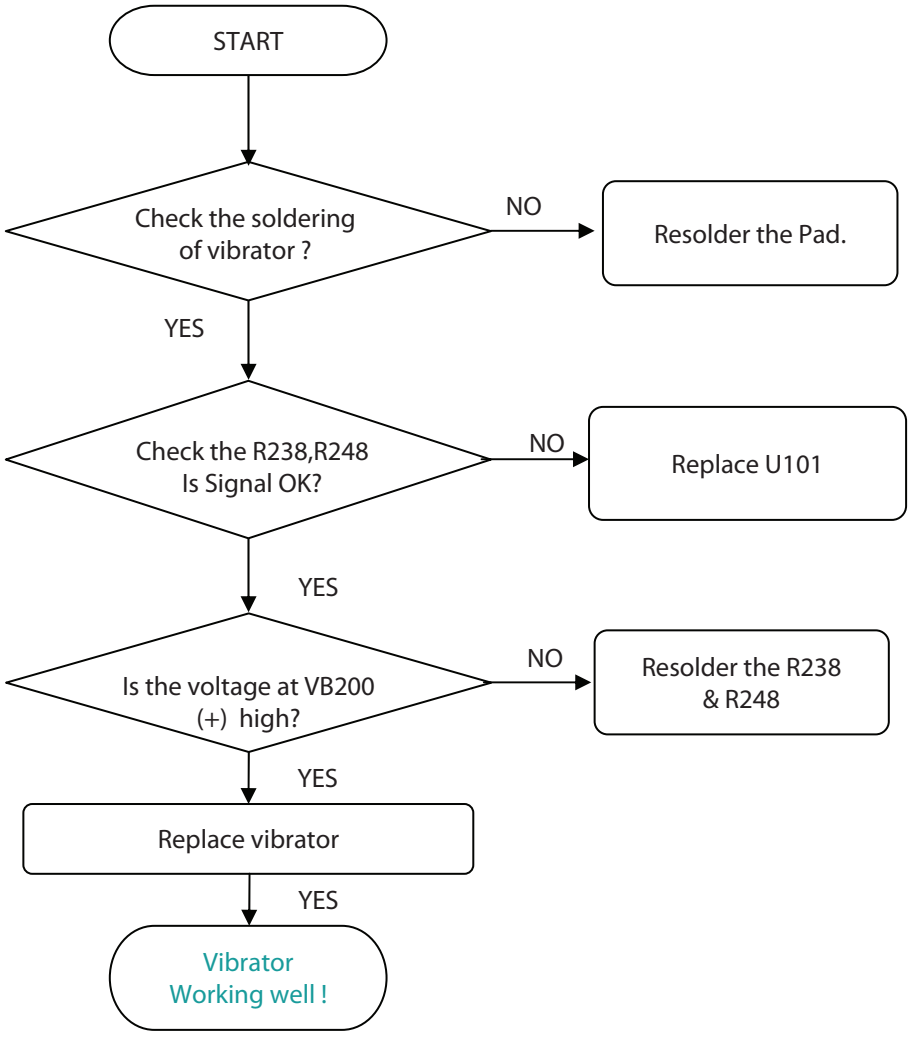
MAIC IC





CHECKING FLOW

SETTING : Enter the engineering mode, and set vibrator on at vibration of BB test menu



4.7 LCD Trouble

TEST POINT

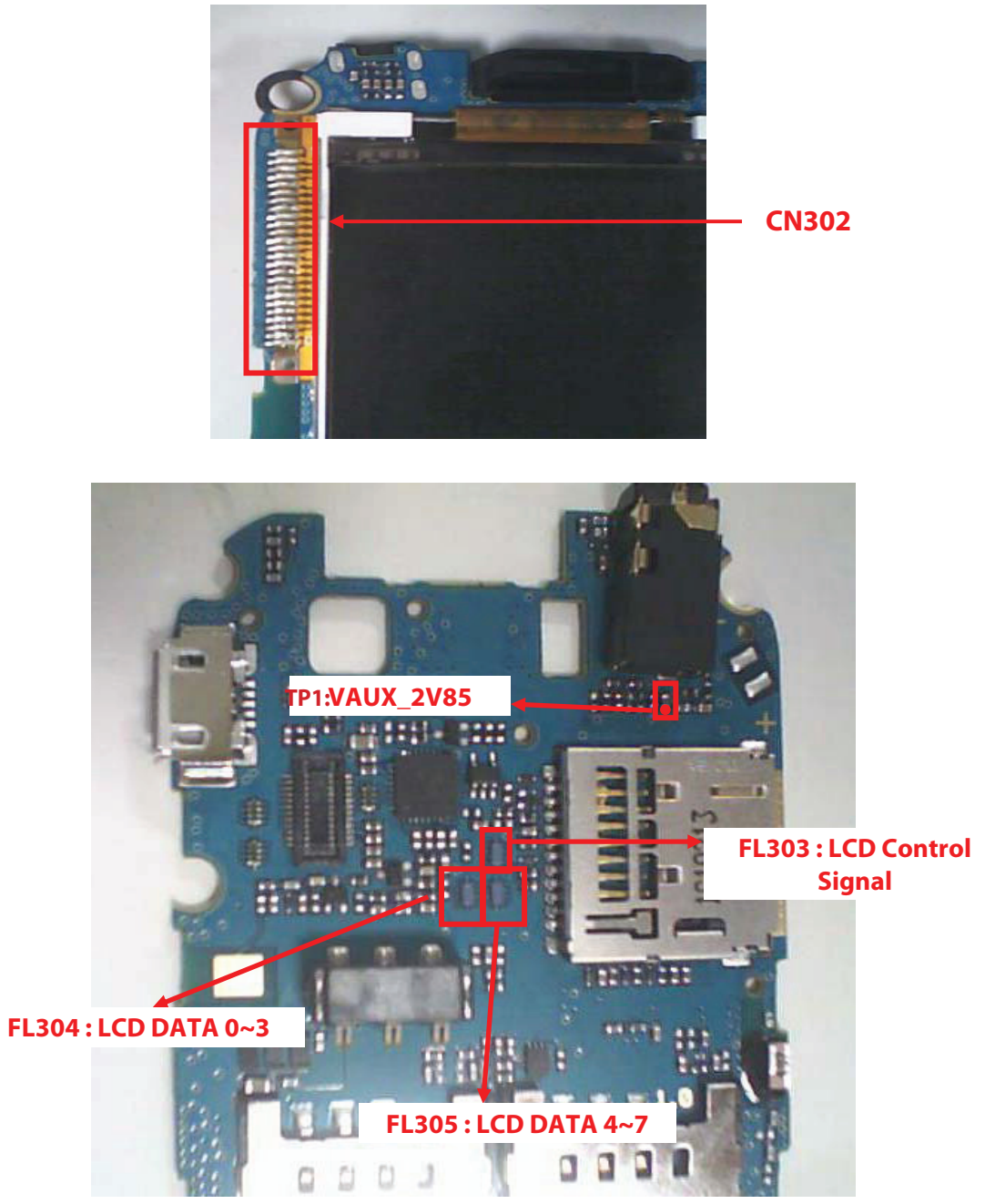
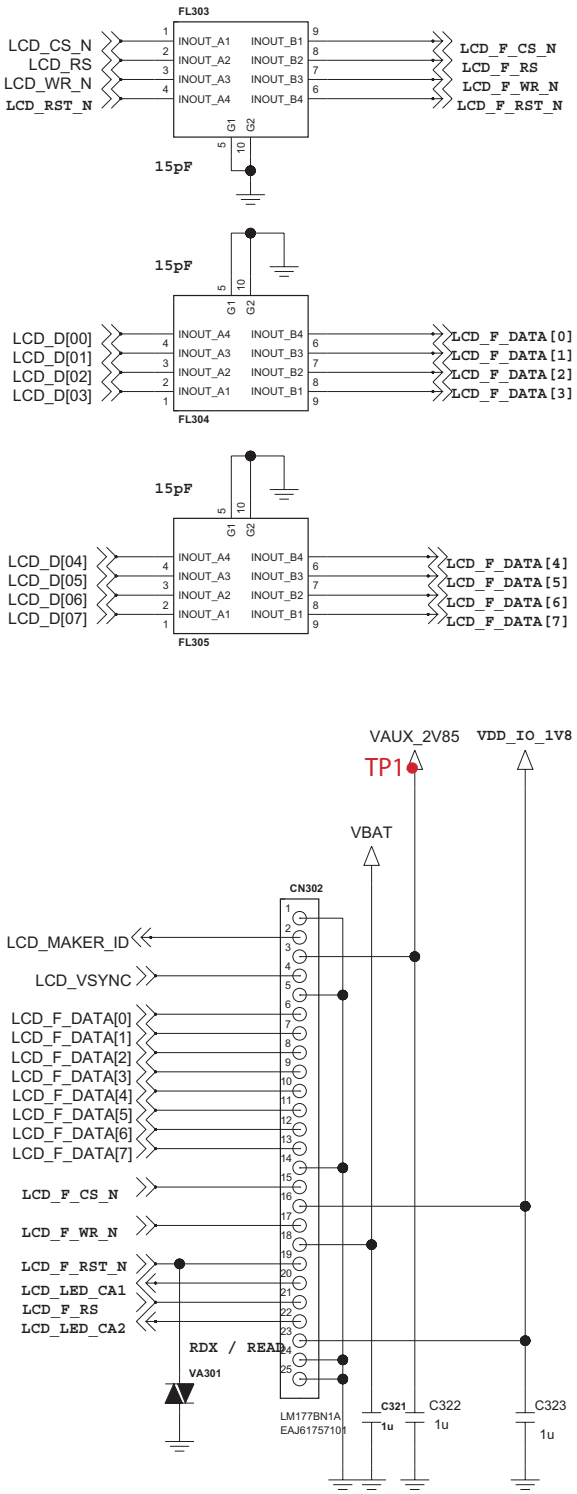
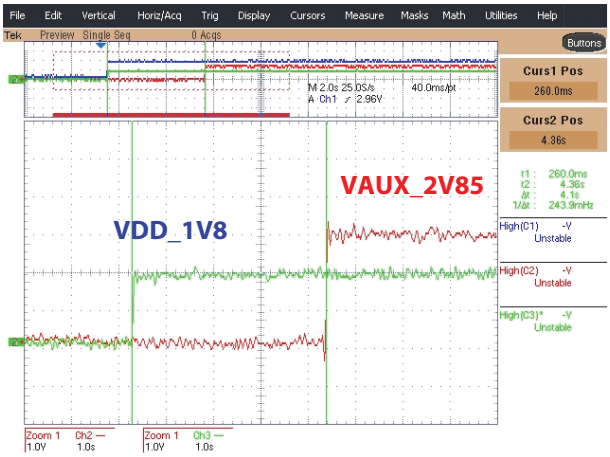


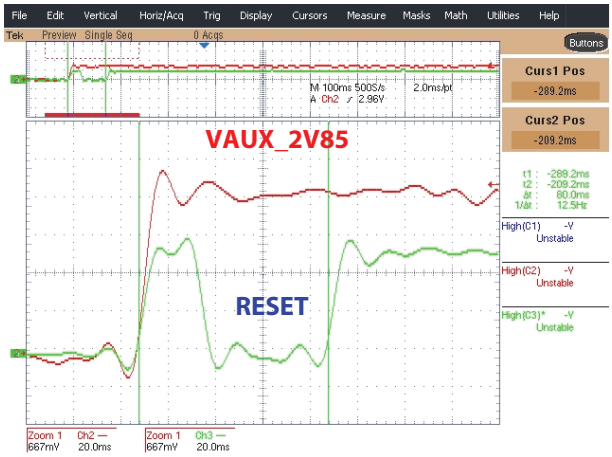
Figure 4.7

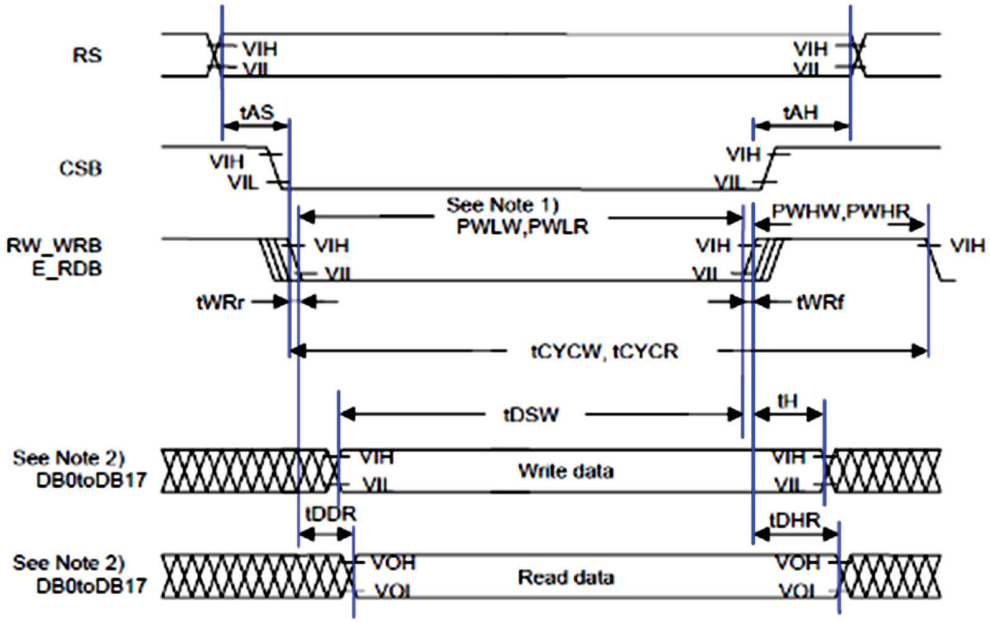
CIRCUIT



Waveform



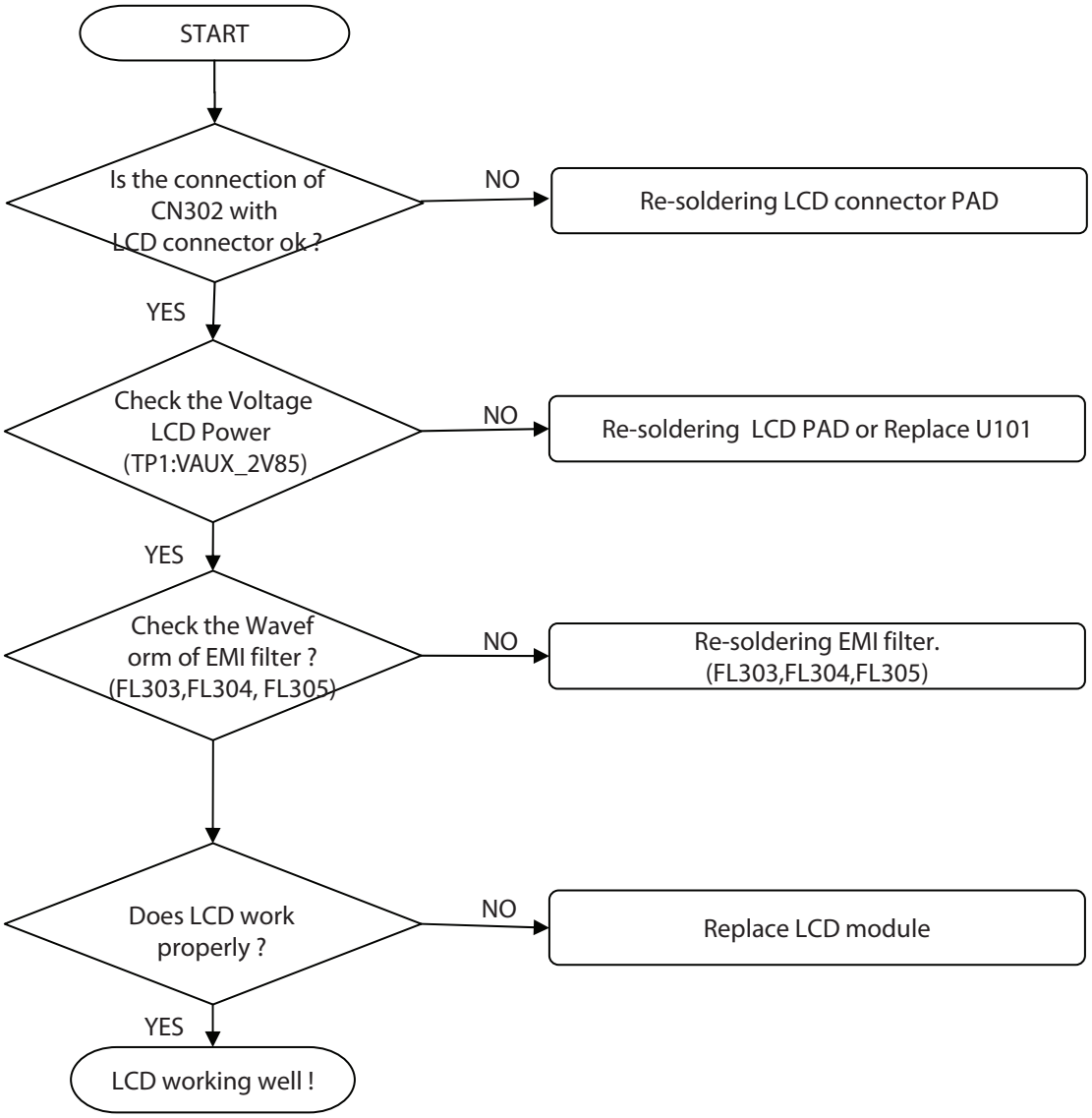




Note 1) PWLW and PWLR are defined by the overlap period when CSB is "Low" and RW_WRB or E_RDB is "Low".
Note 2) Unused DB pins must be fixed at "VDD3" or "GND".

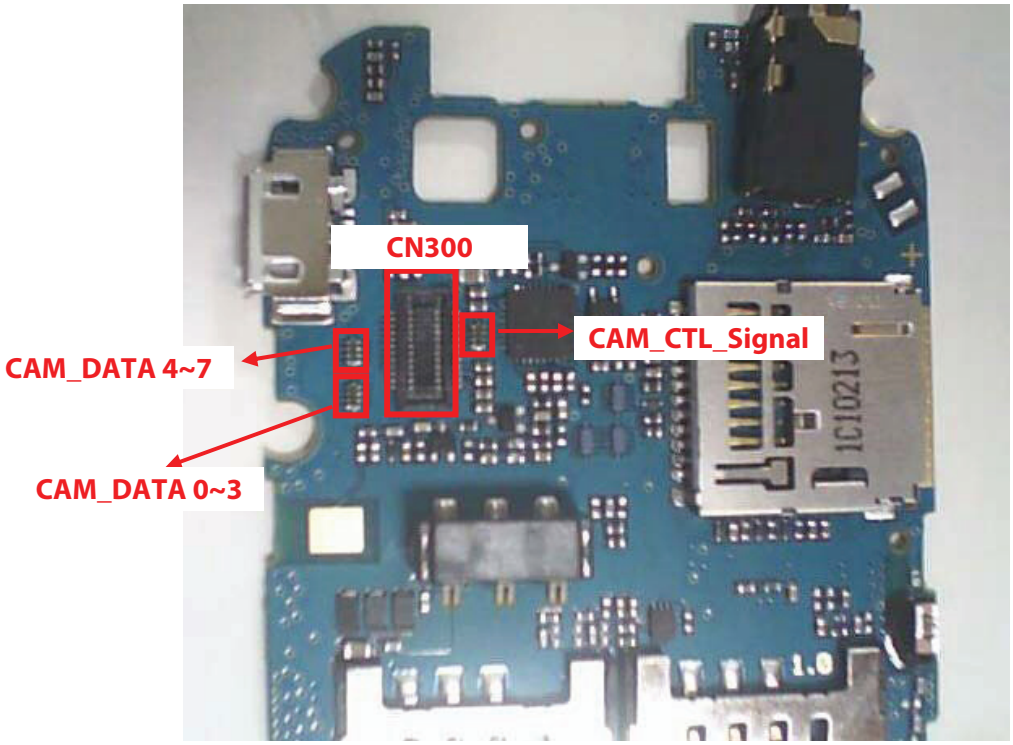
Graph 4.7.2. LCD Data Waveform

CHECKING FLOW



4.8 Camera Trouble

TEST POINT



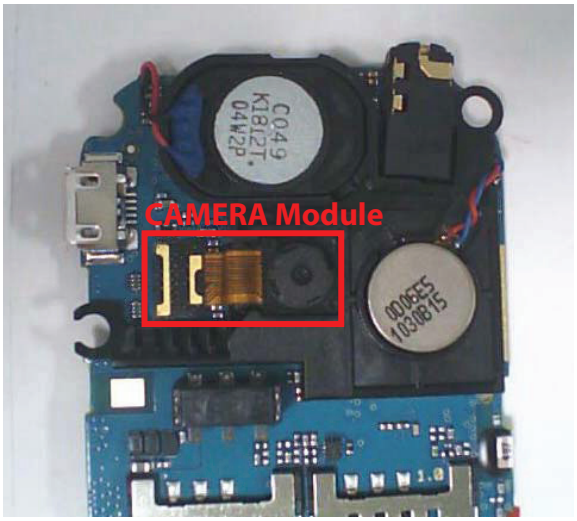
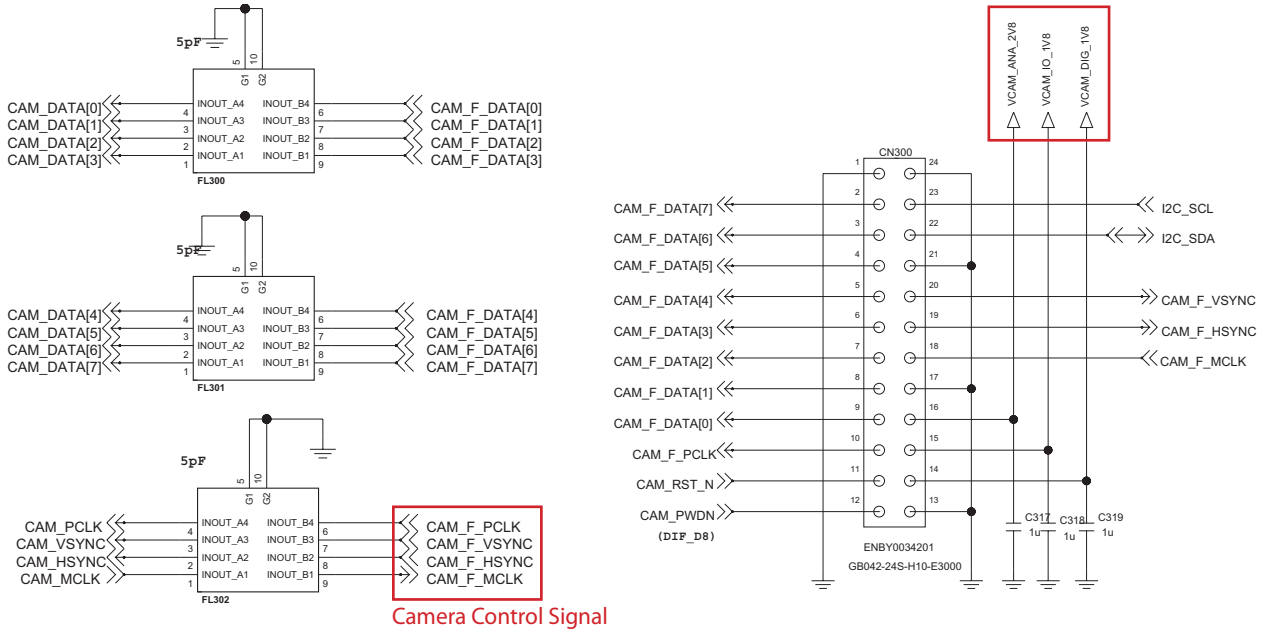
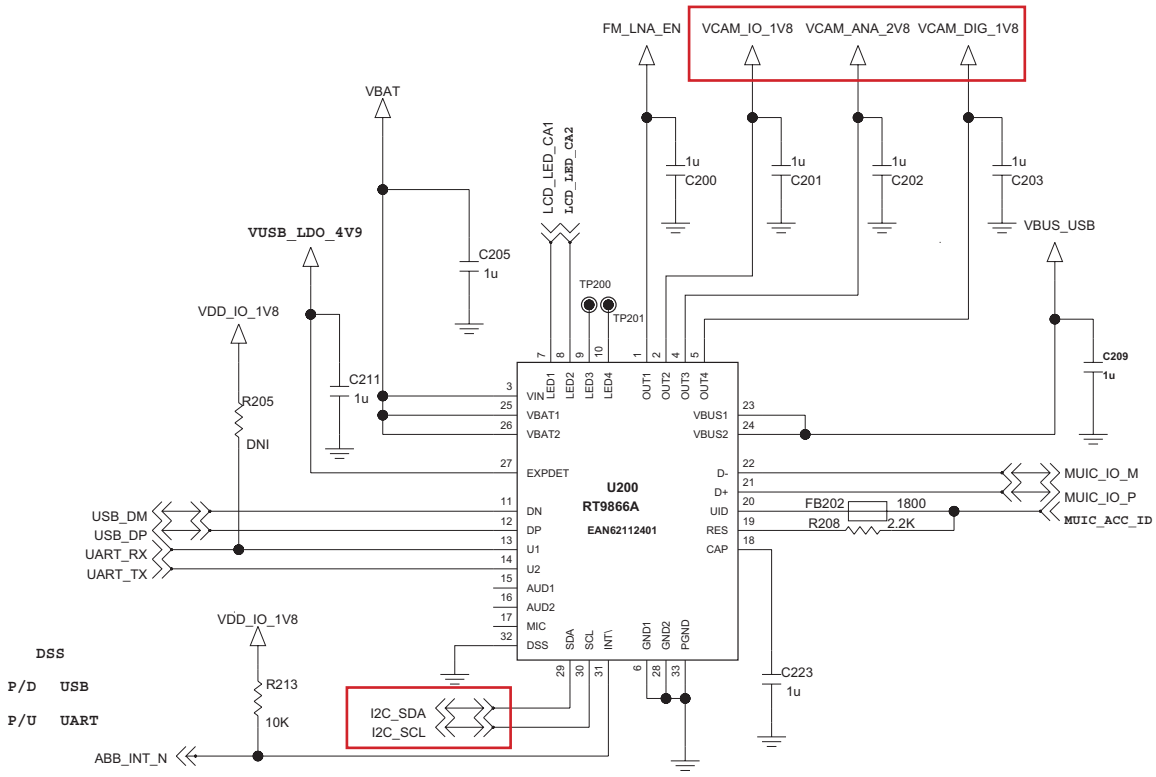


Figure 4.8

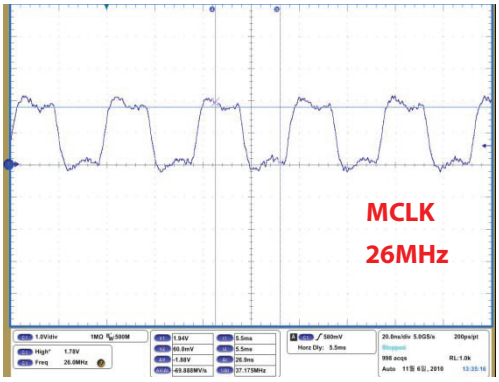
CIRCUIT

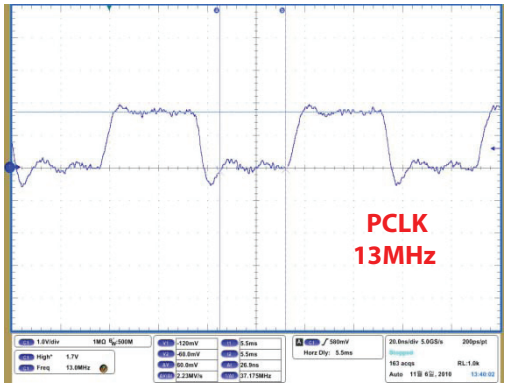


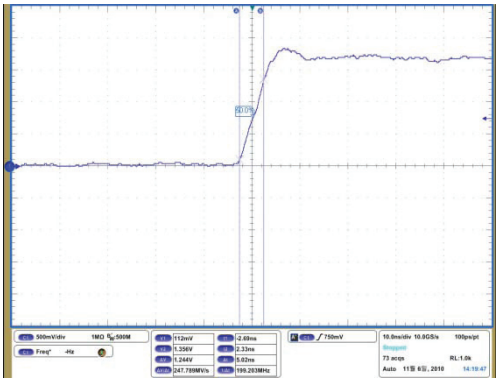
Camera Control Signal



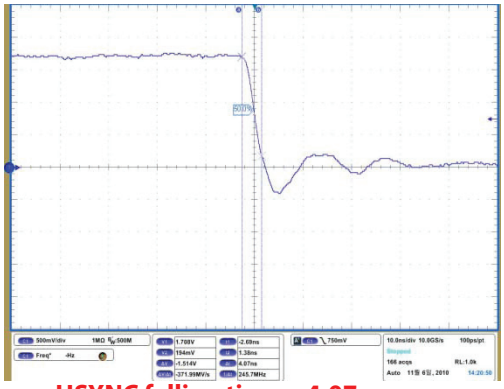
Waveform



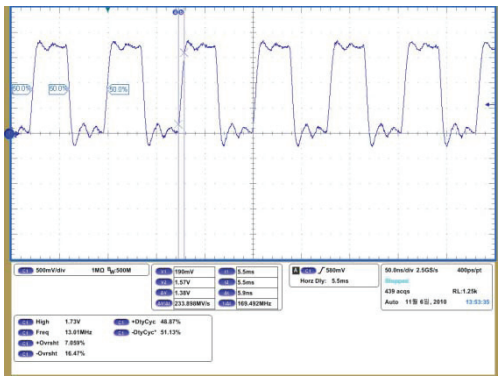




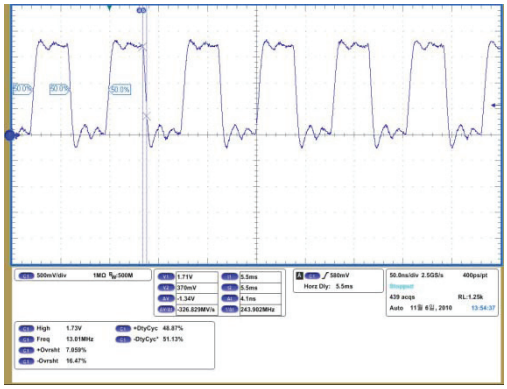
HSYNC rising time = 5.02ns



HSYNC falling time = 4.07ns

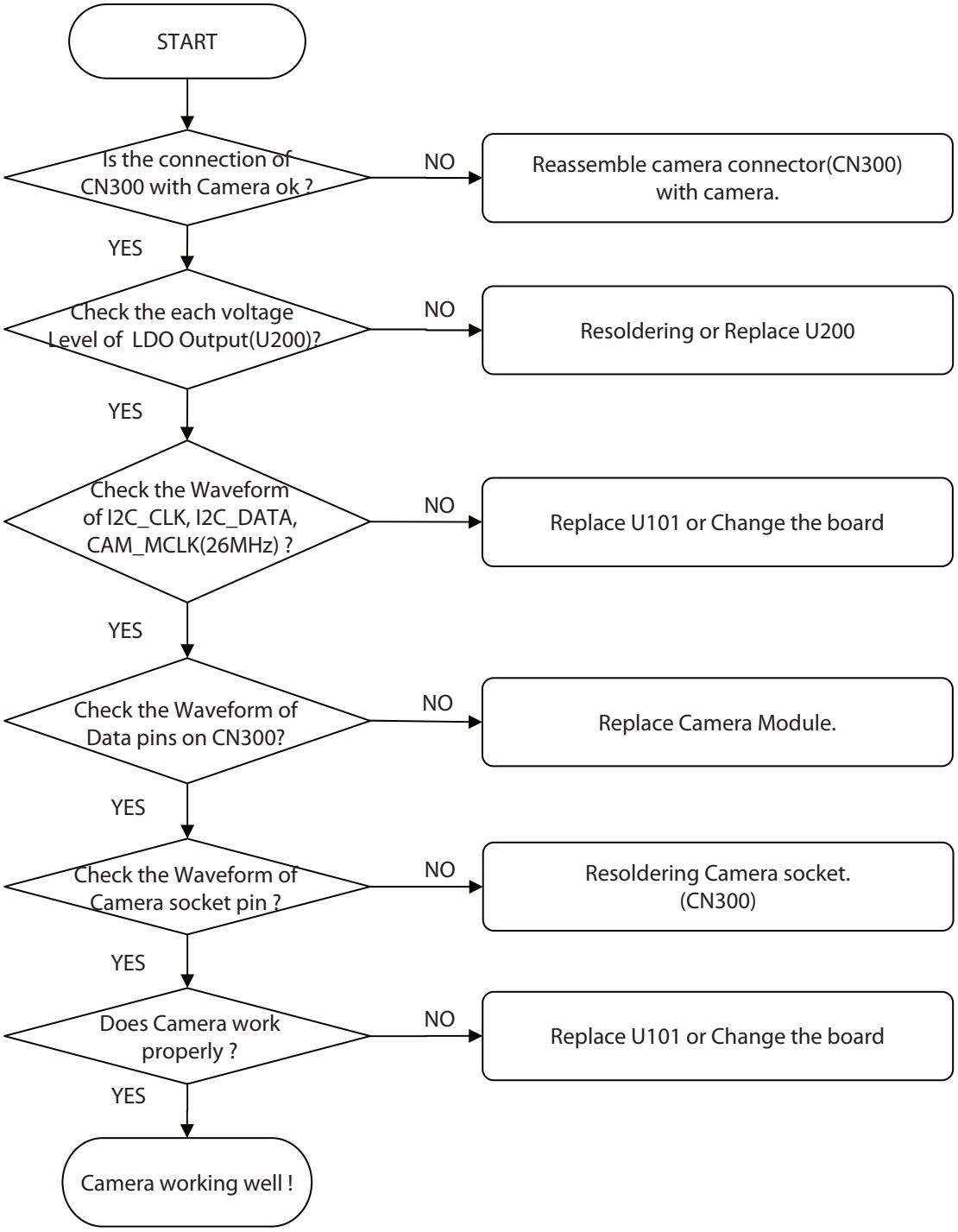


PCLK rising time = 5.9ns



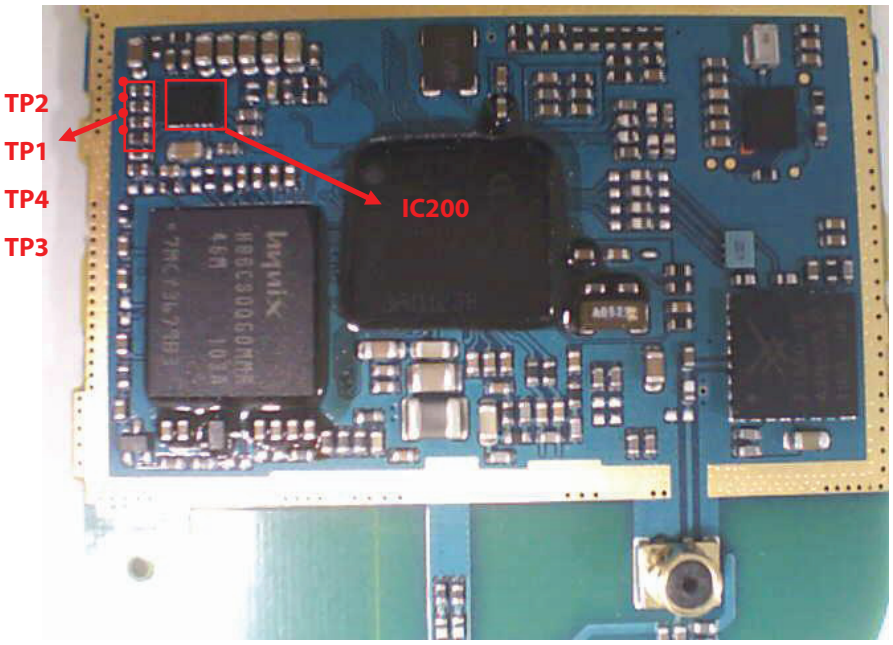
PCLK falling time = 4.1ns

CHECKING FLOW

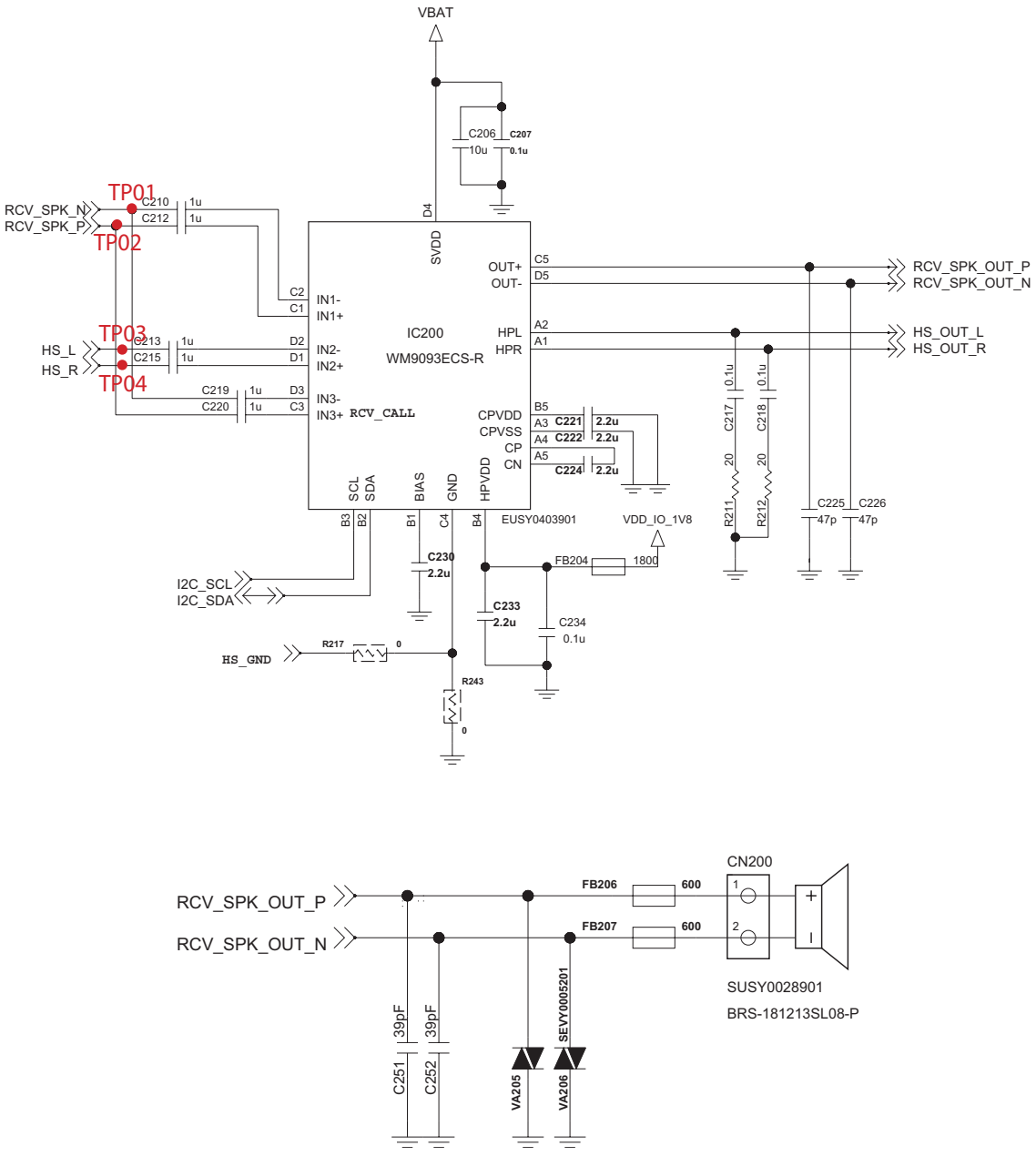


4.9 Speaker / Receiver Trouble

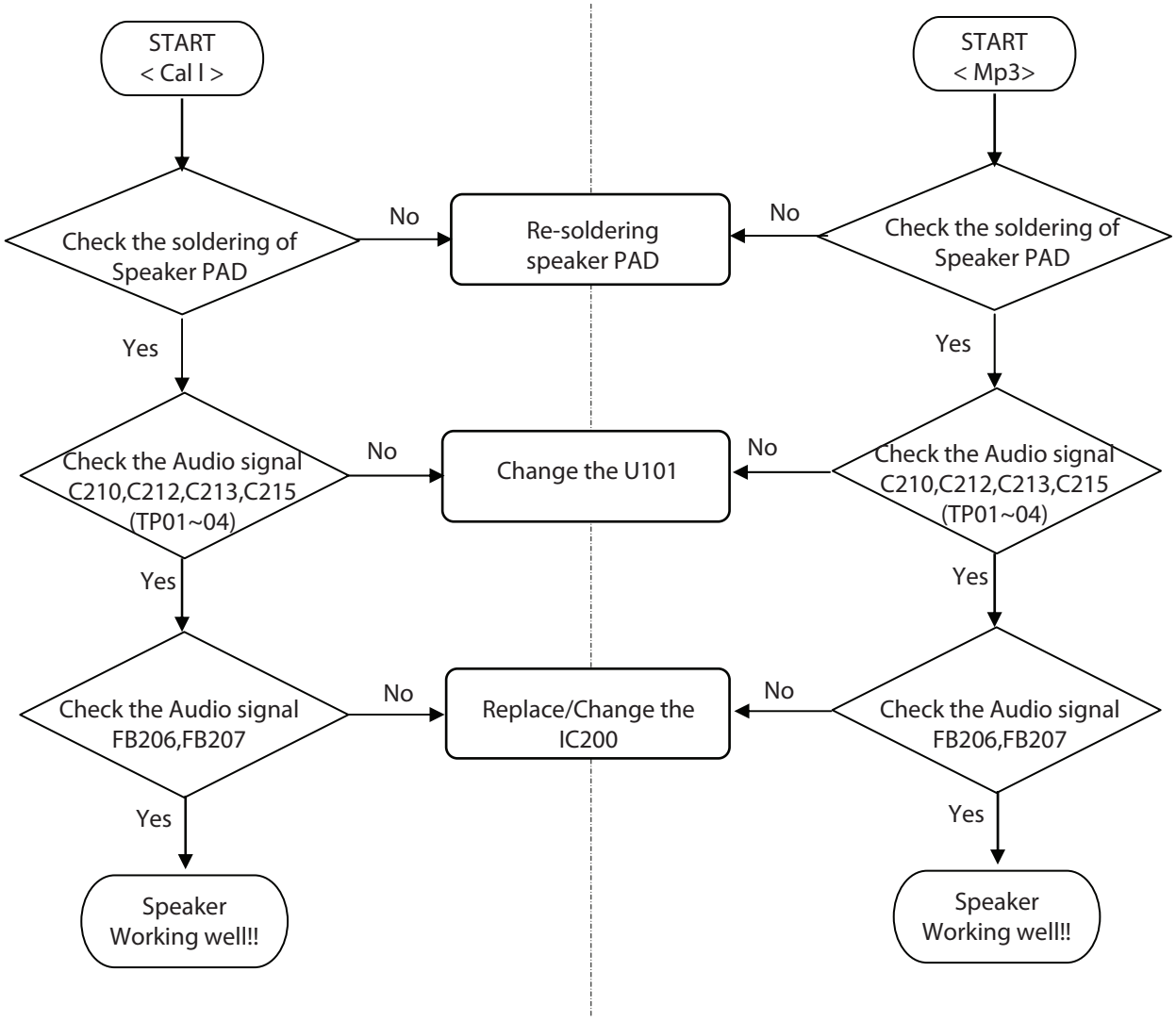
TEST POINT



CIRCUIT

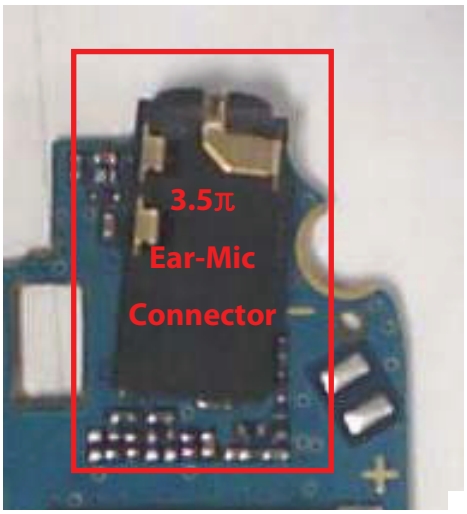


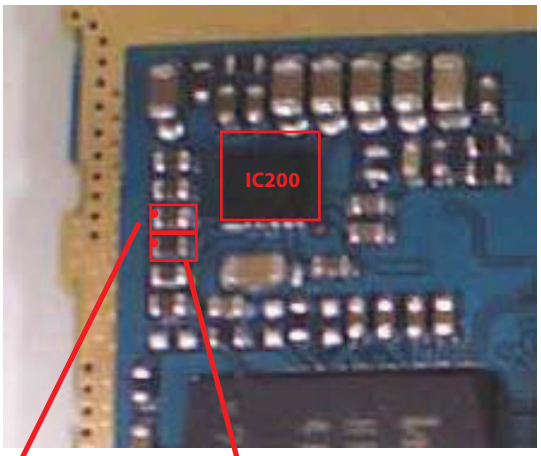
CHECKING FLOW

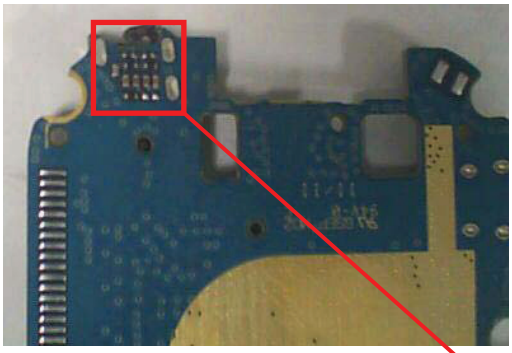


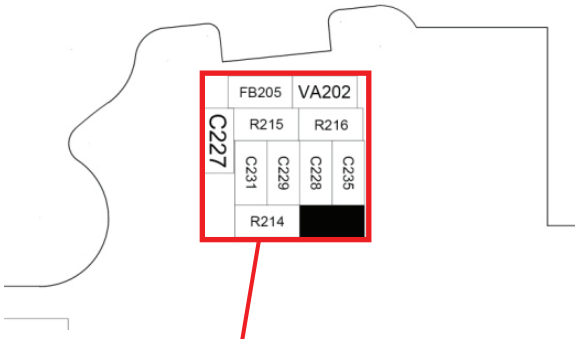
4.10 Earphone Trouble

TEST POINT



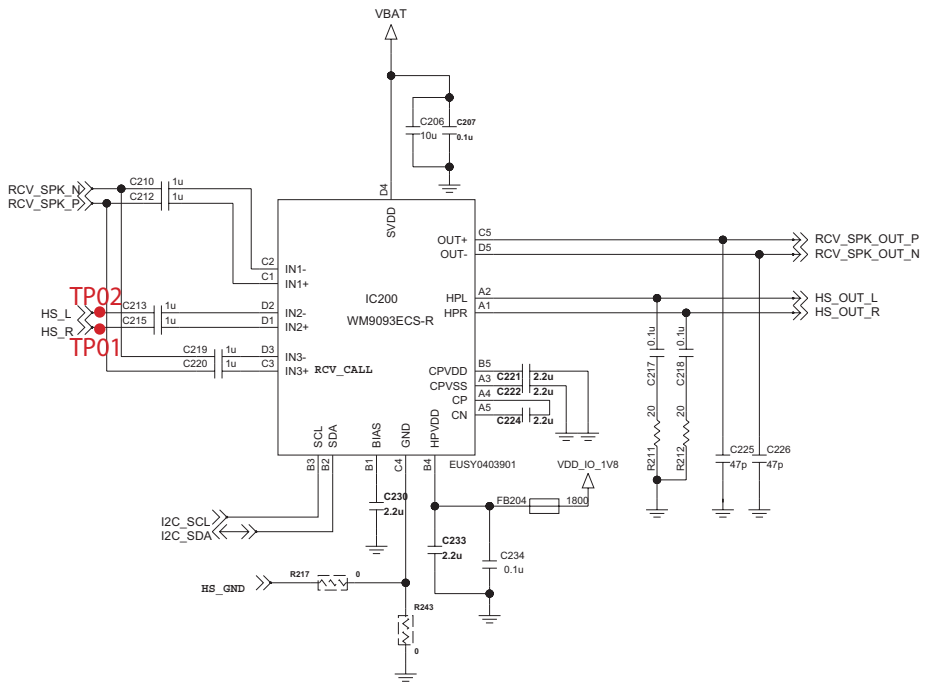


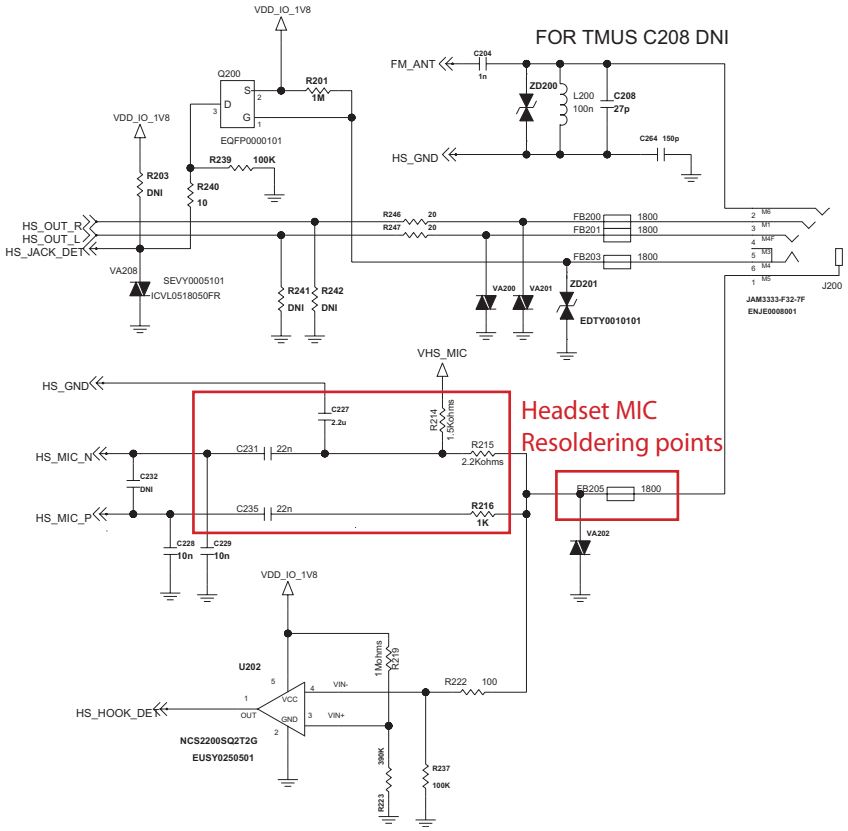




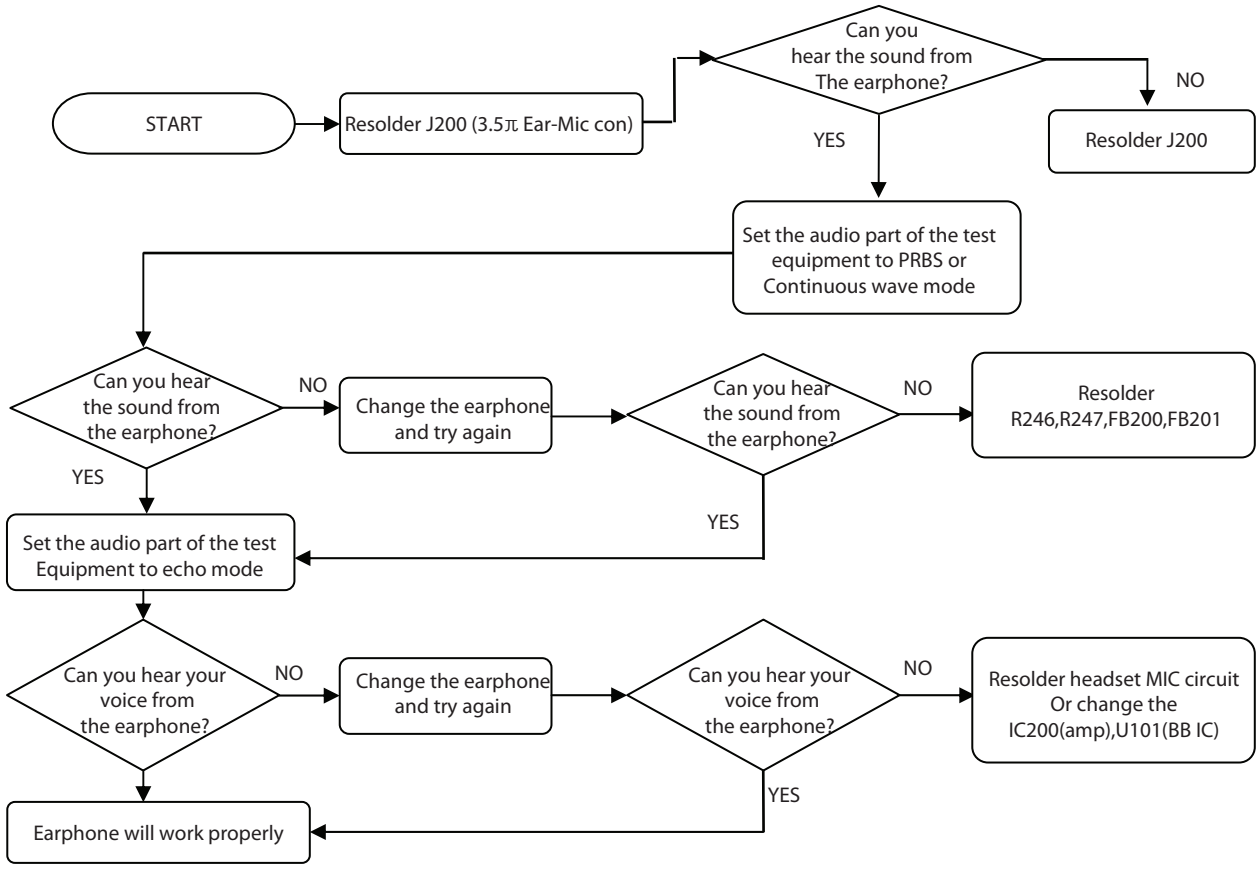
Headset MIC
Resoldering points

CIRCUIT





CHECKING FLOW



4.11 Microphone Trouble

TEST POINT

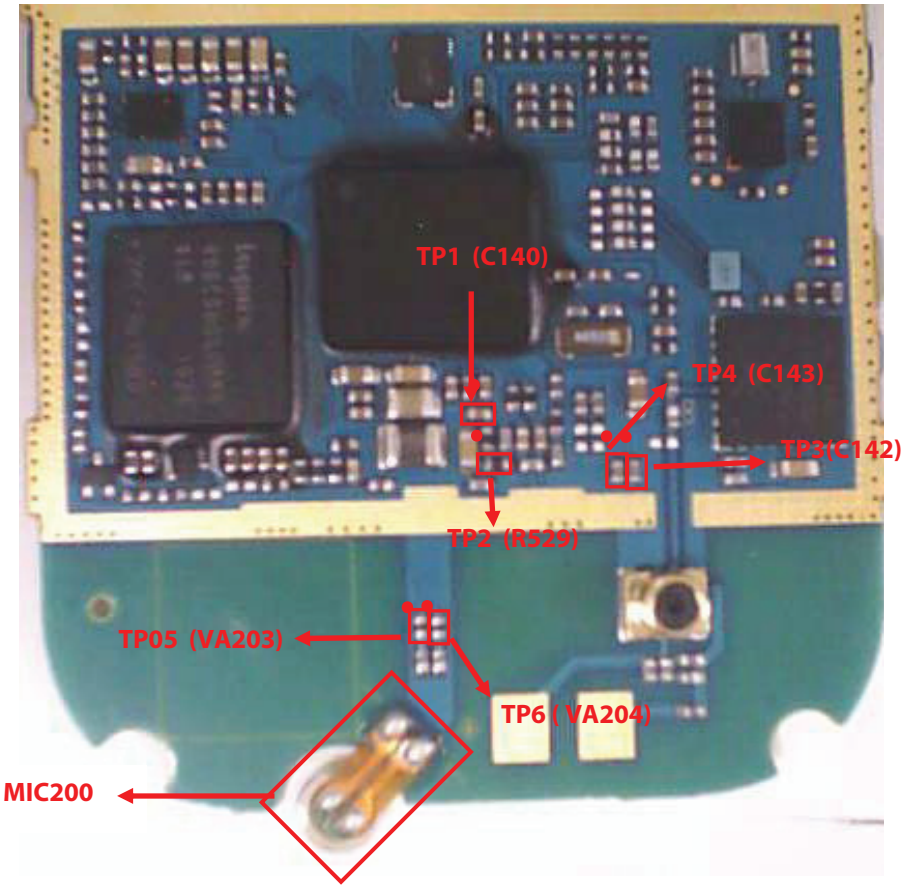
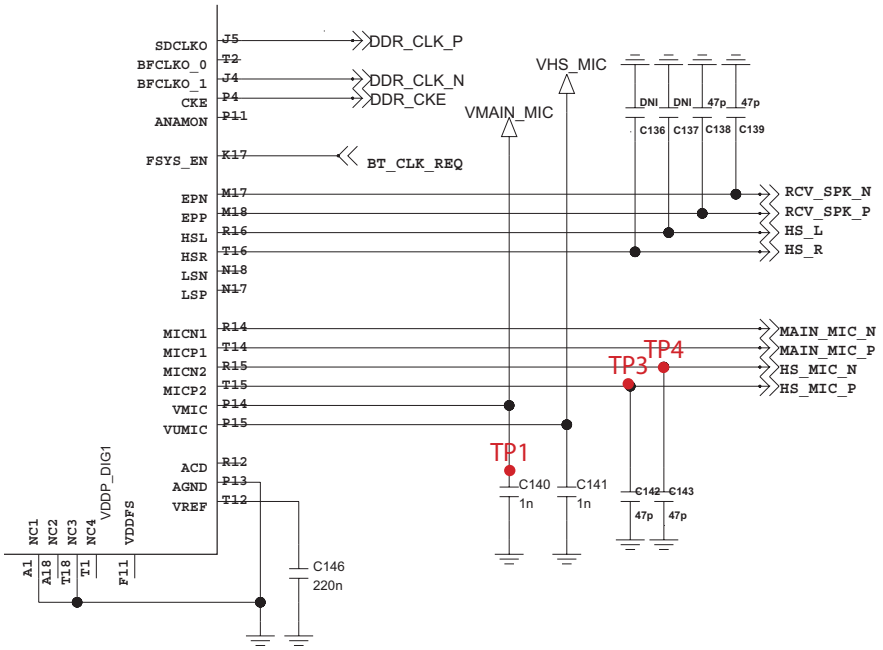
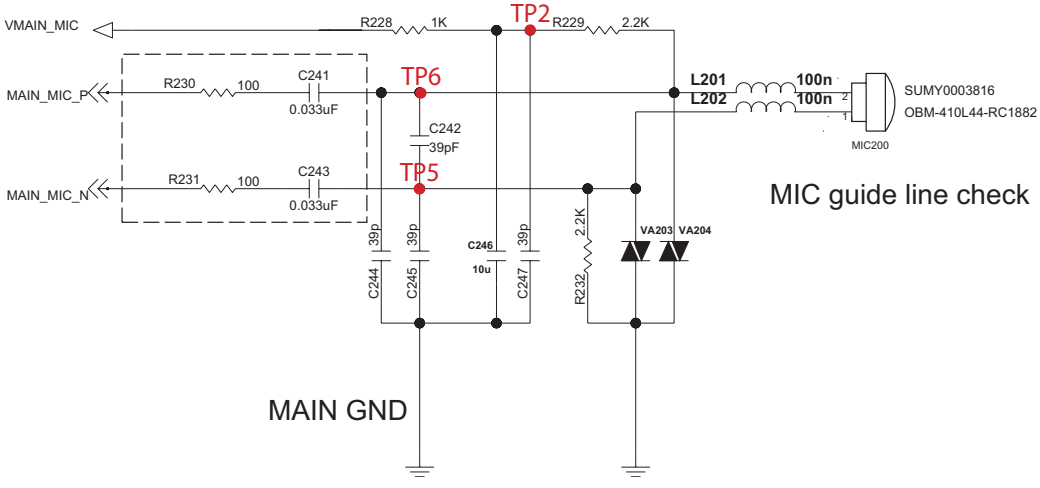


Figure 4.12

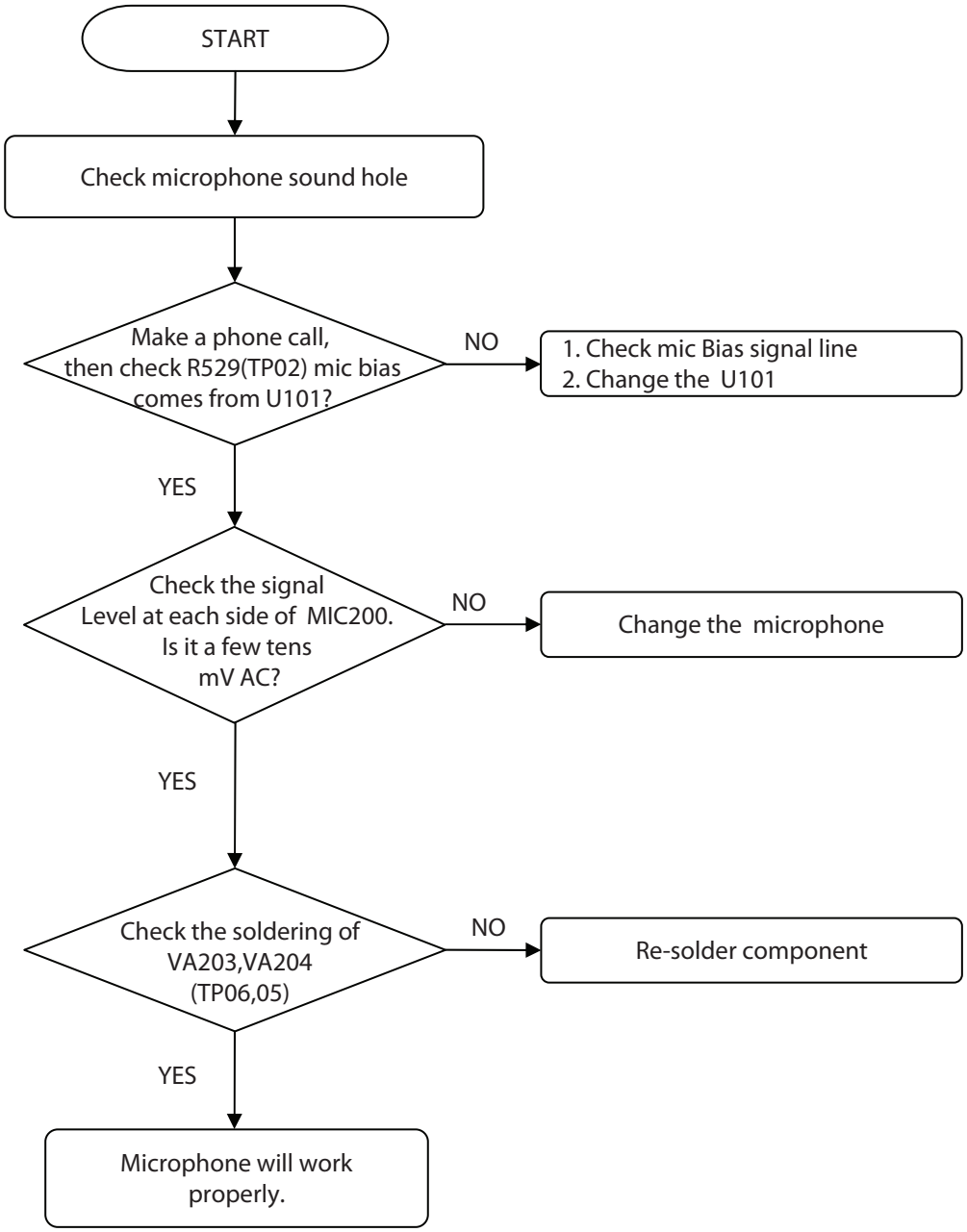
CIRCUIT





CHECKING FLOW

SETTING : After initialize Agilent 8960, Test EGSM900, DCS mode (or GSM850, PCS mode)



4.12 SIM Card Interface Trouble

TEST POINT

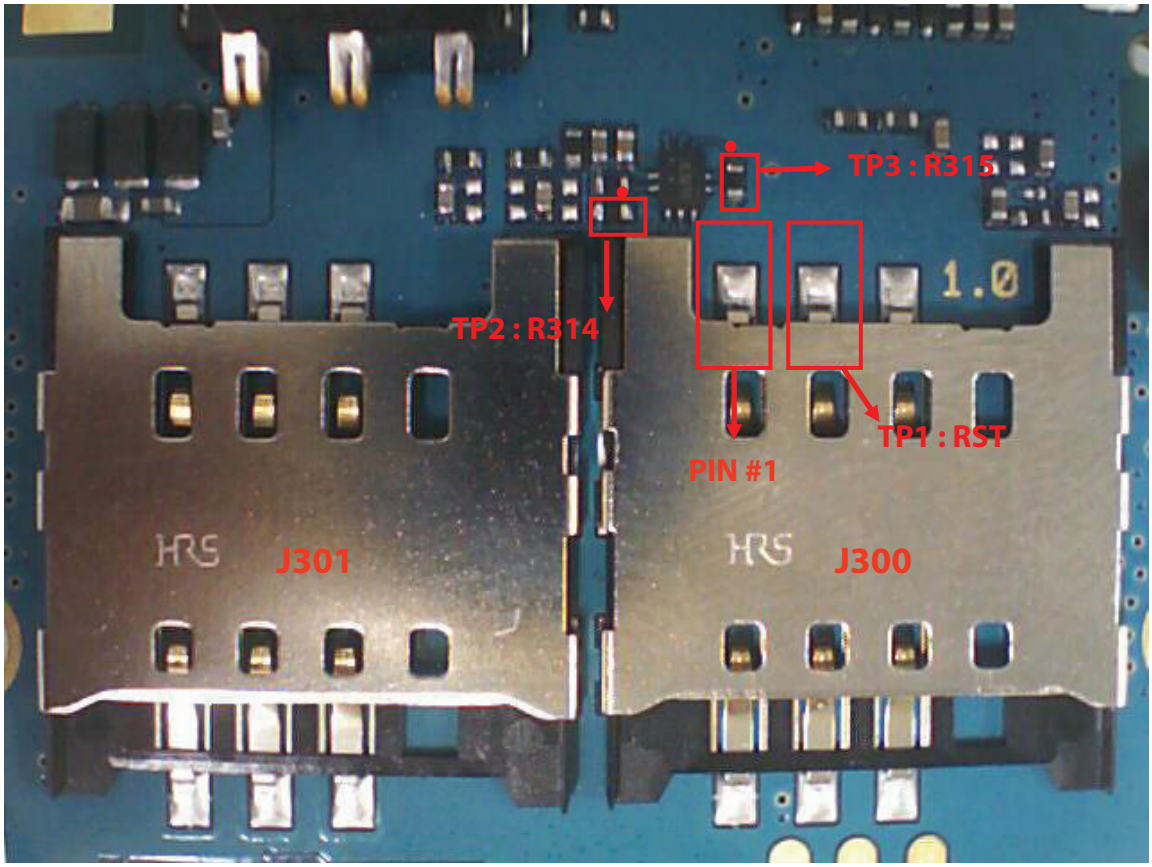
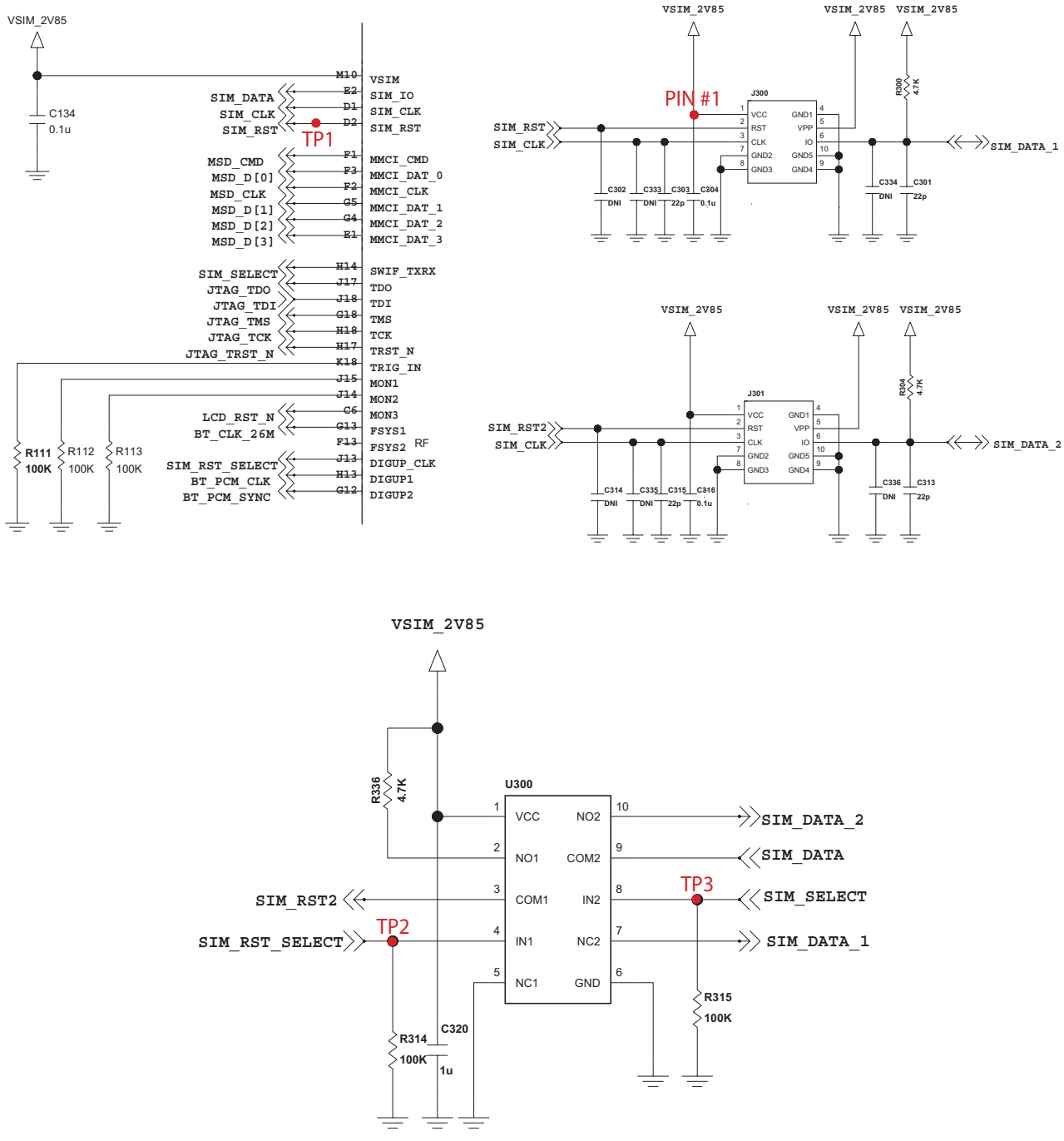
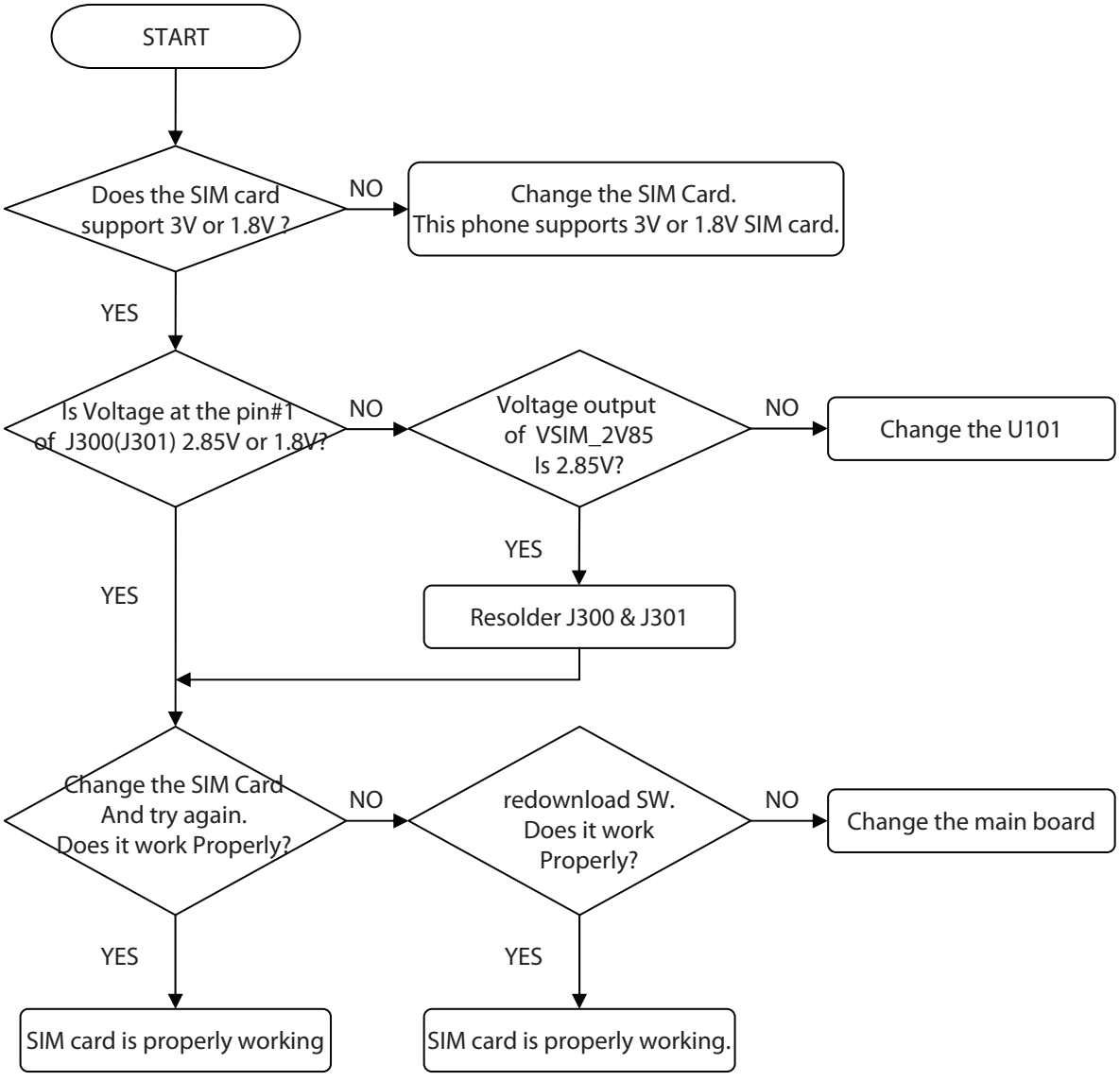


Figure 4.13

CIRCUIT



CHECKING FLOW



4.13 Micro SD (uSD) Trouble

TEST POINT

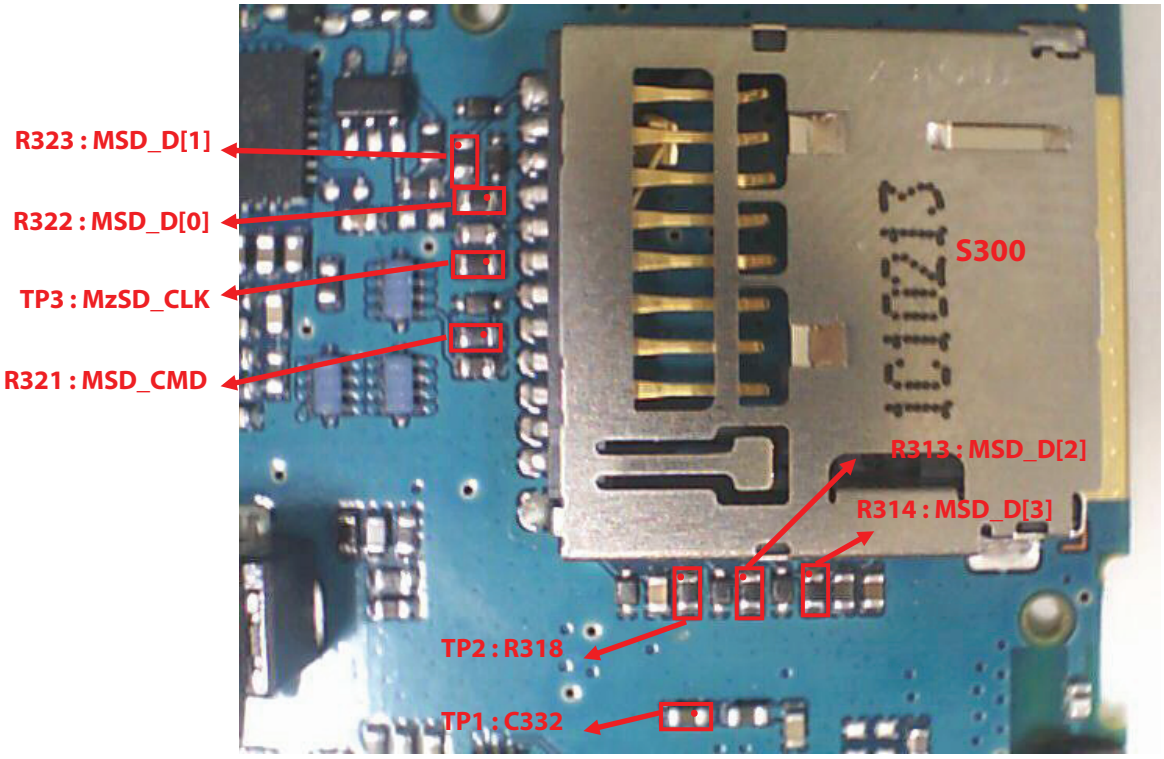
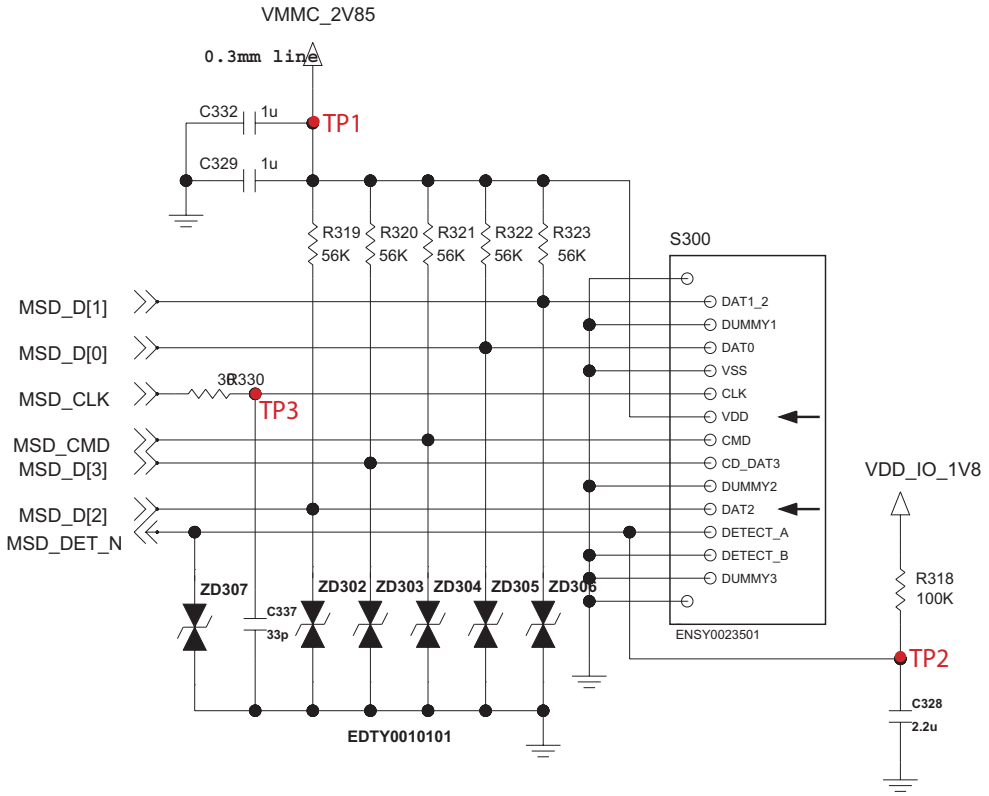
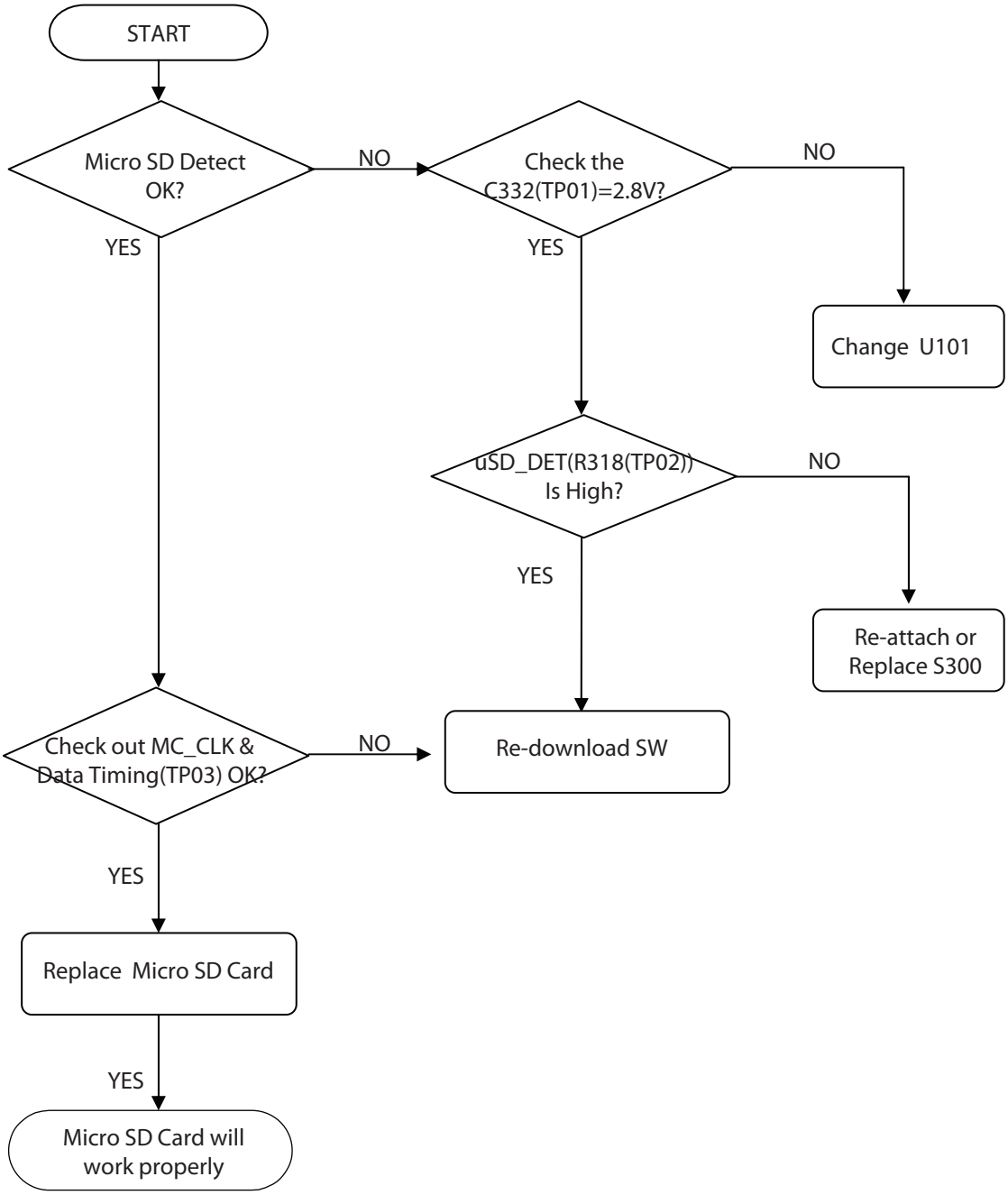


Figure 4.14

CIRCUIT

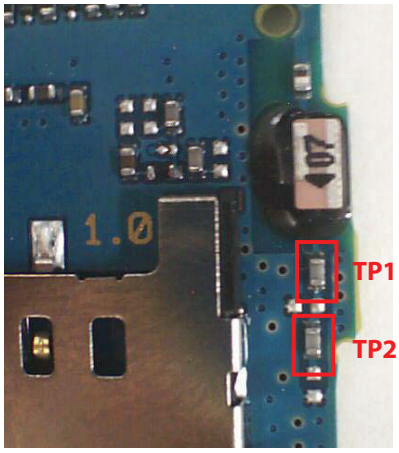


CHECKING FLOW



4.14 Bluetooth Trouble

TEST POINT



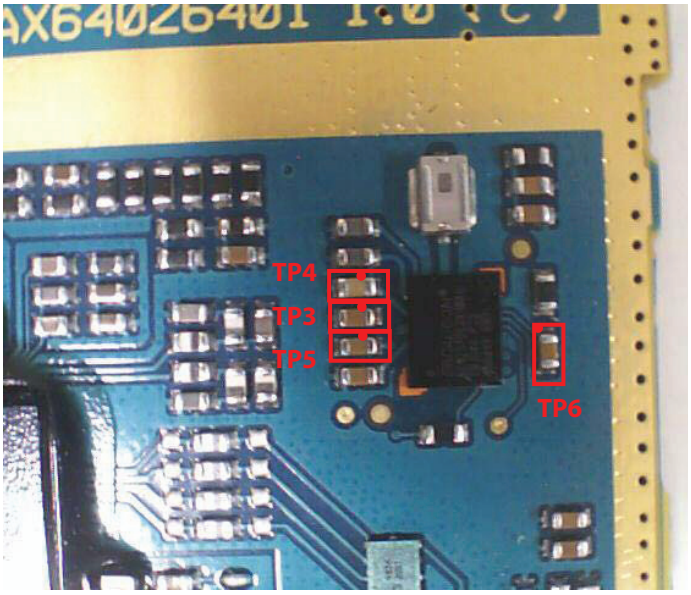
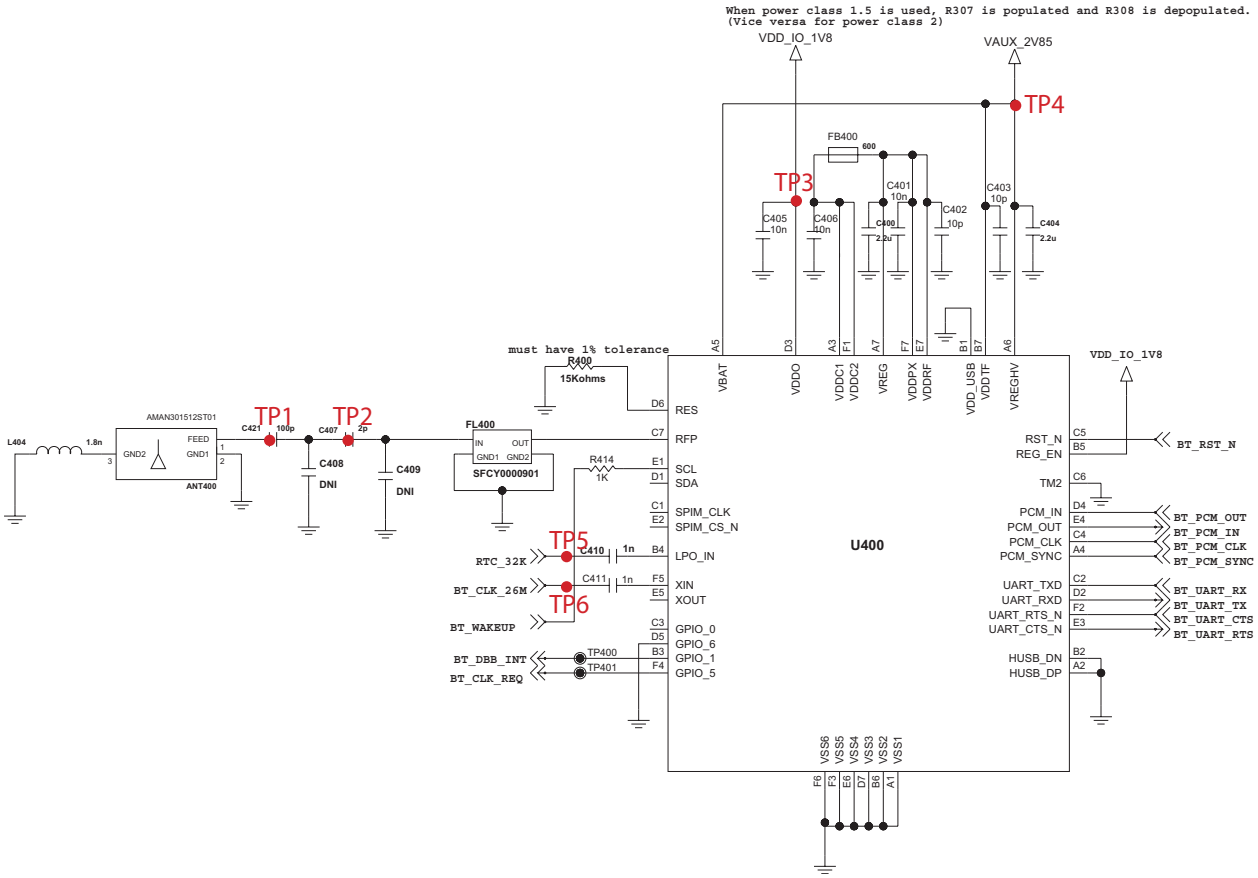
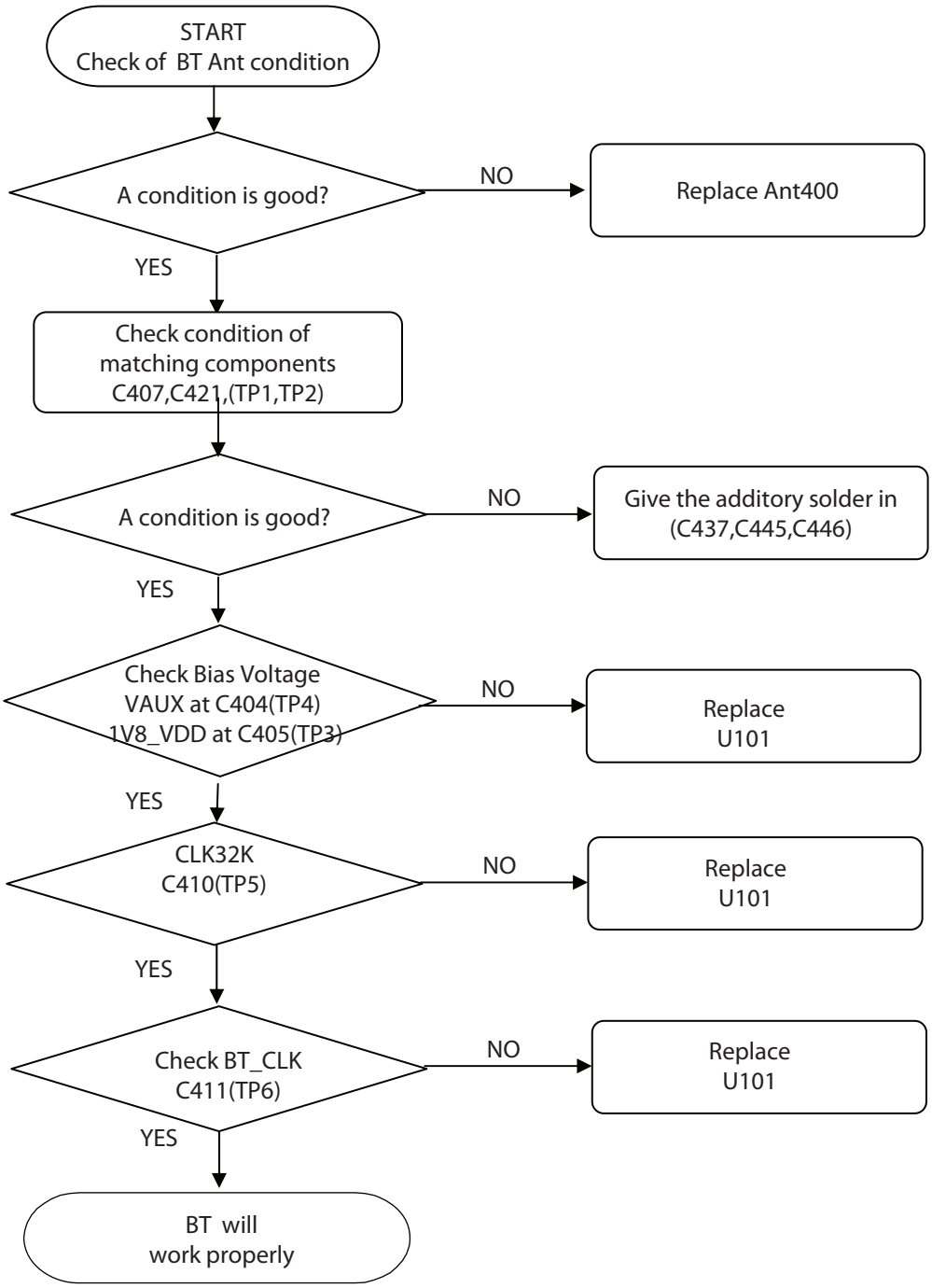


Figure 4.16.1

CIRCUIT



CHECKING FLOW



4.15 FM Radio Trouble

TEST POINT

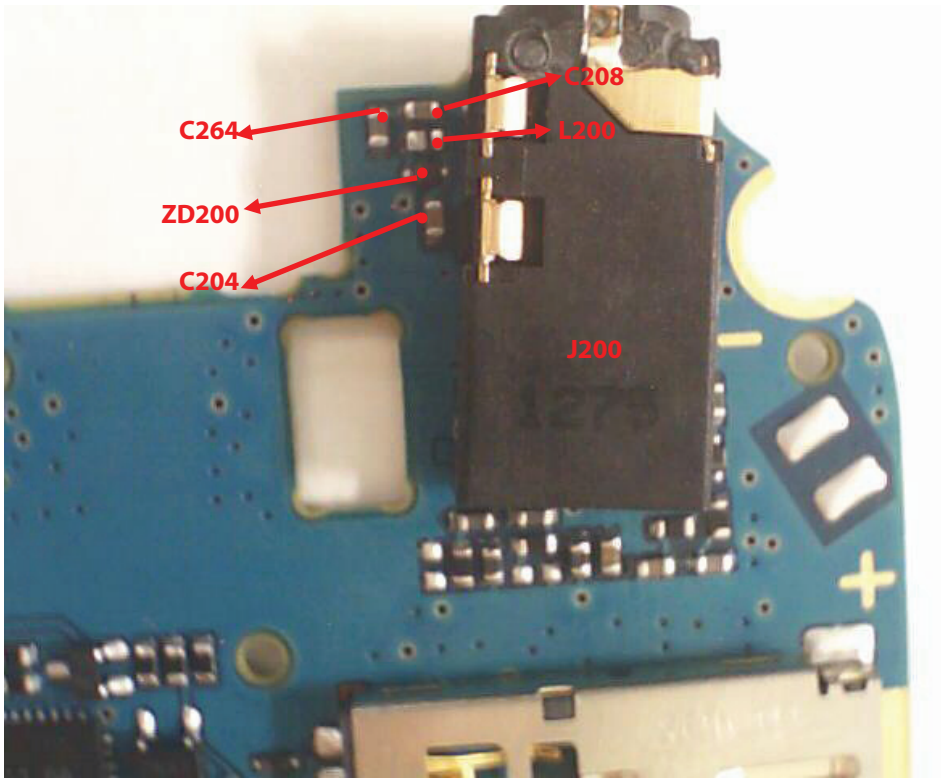
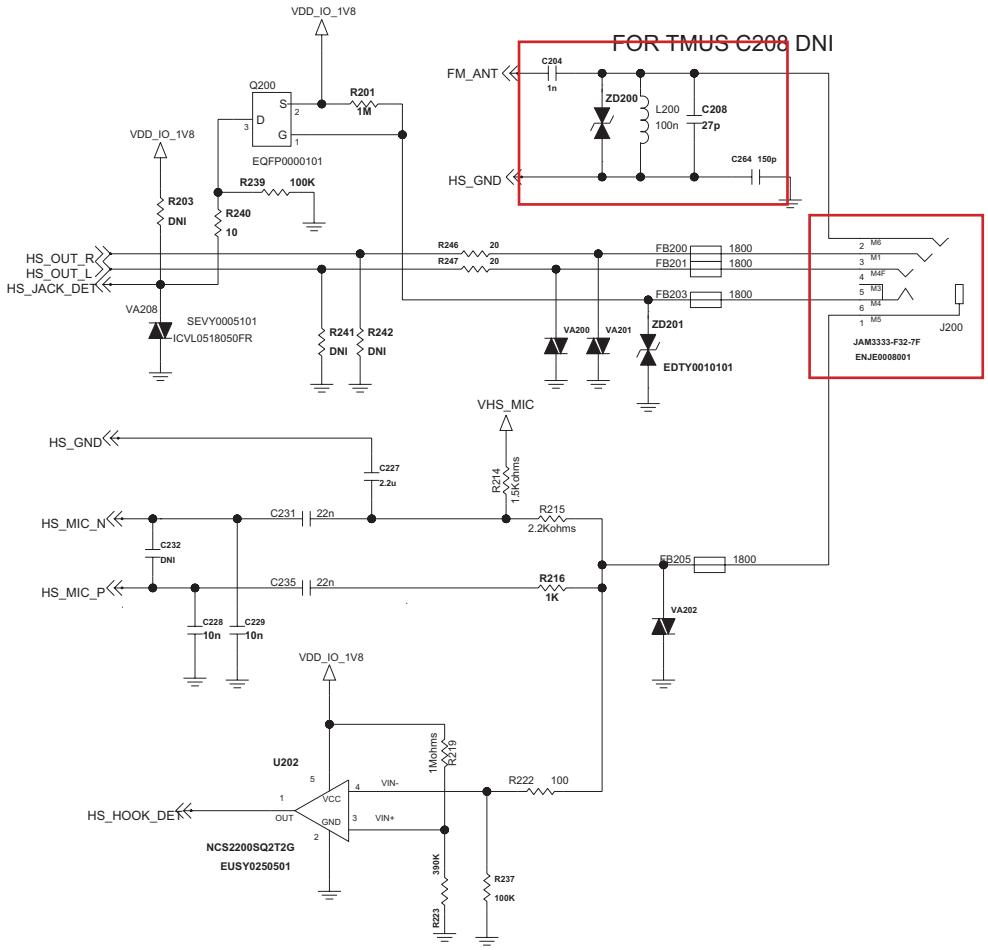
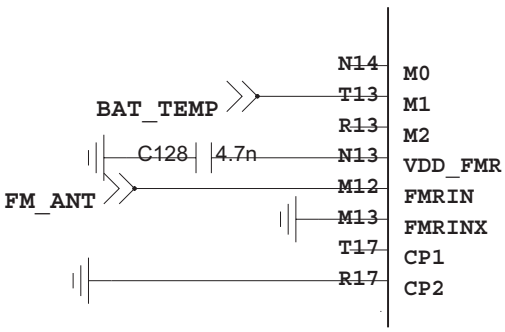


Figure 4.17

CIRCUIT





4.16 Wireless FM Radio Trouble

TEST POINT

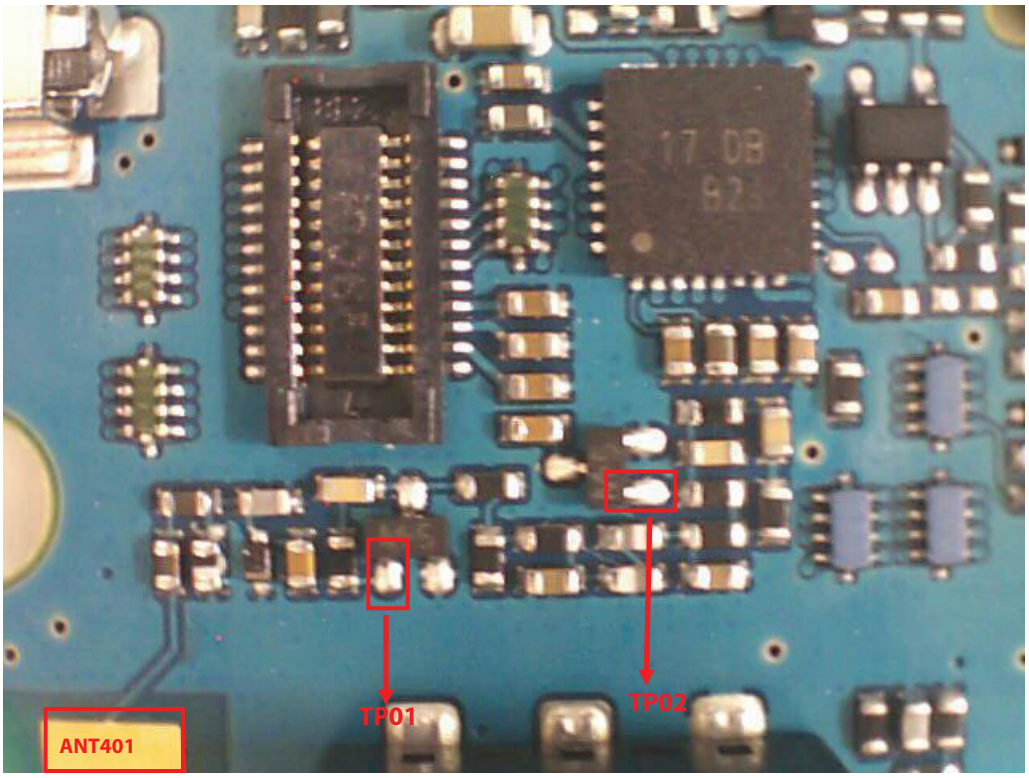
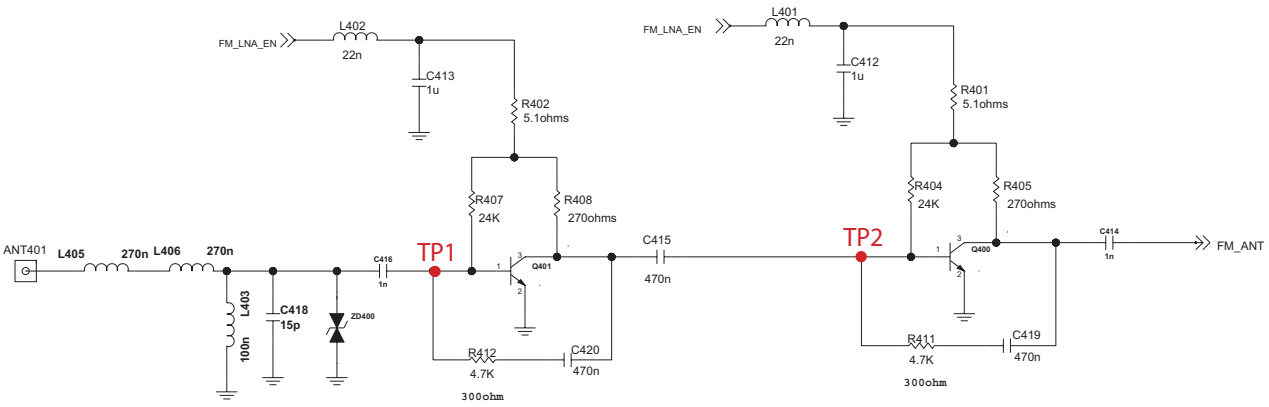
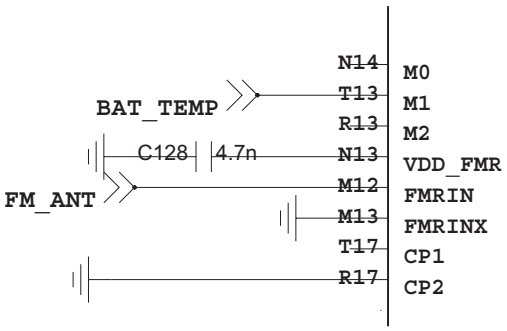


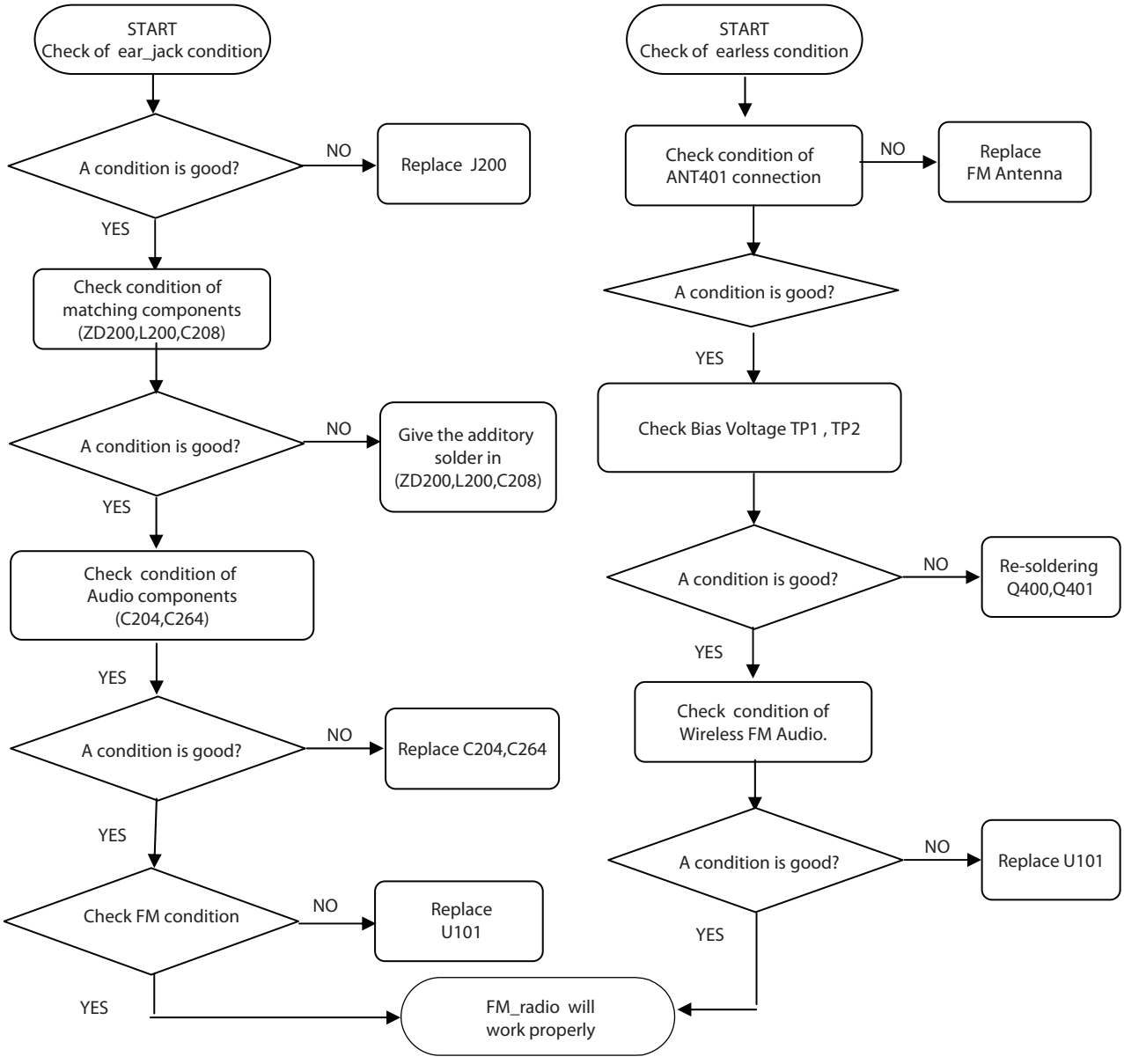
Figure 4.17

CIRCUIT

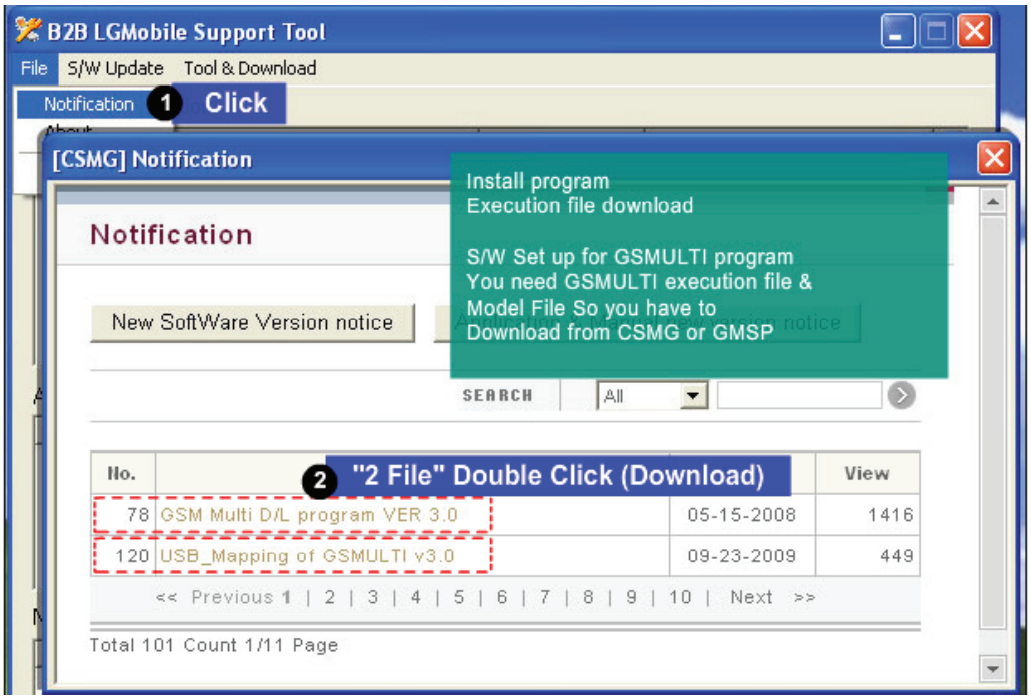


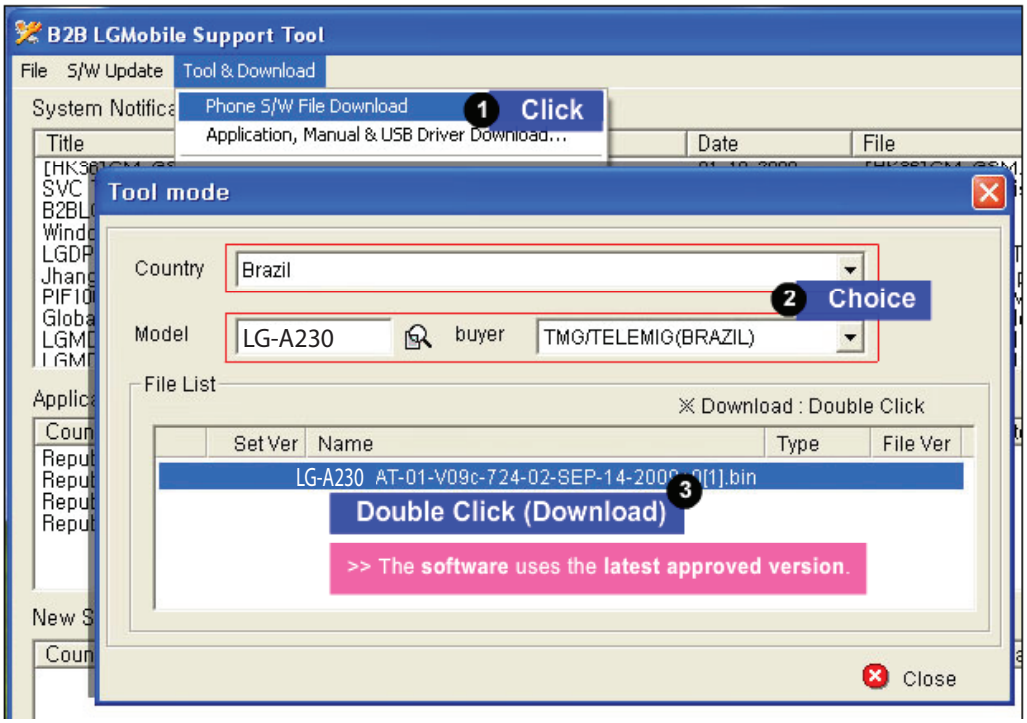


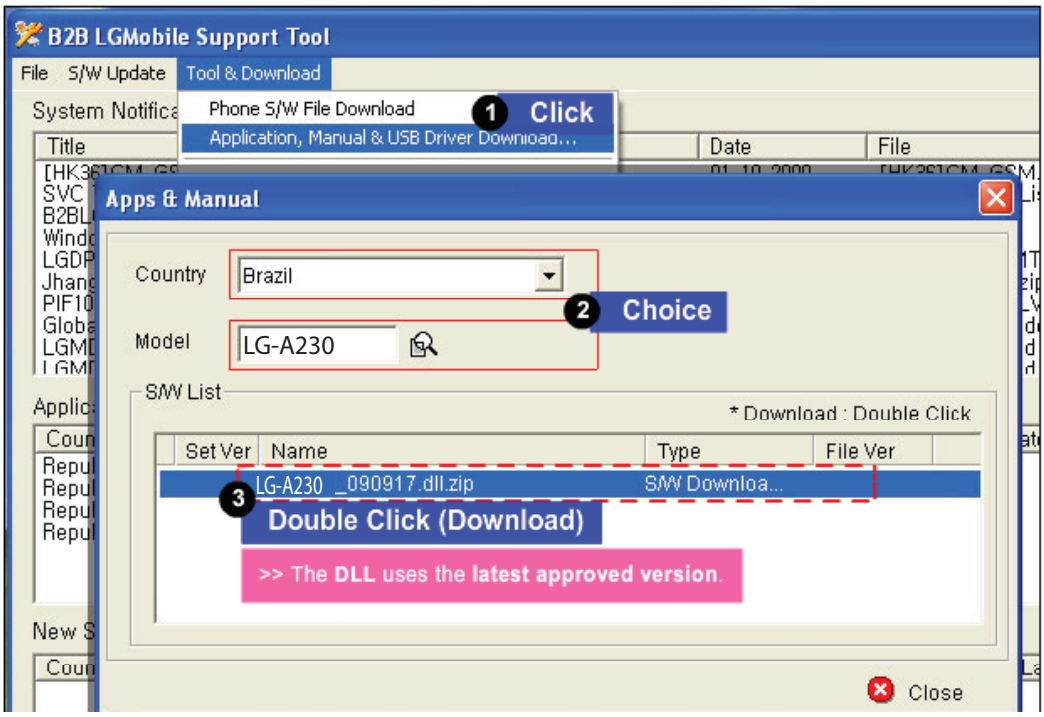
CHECKING FLOW

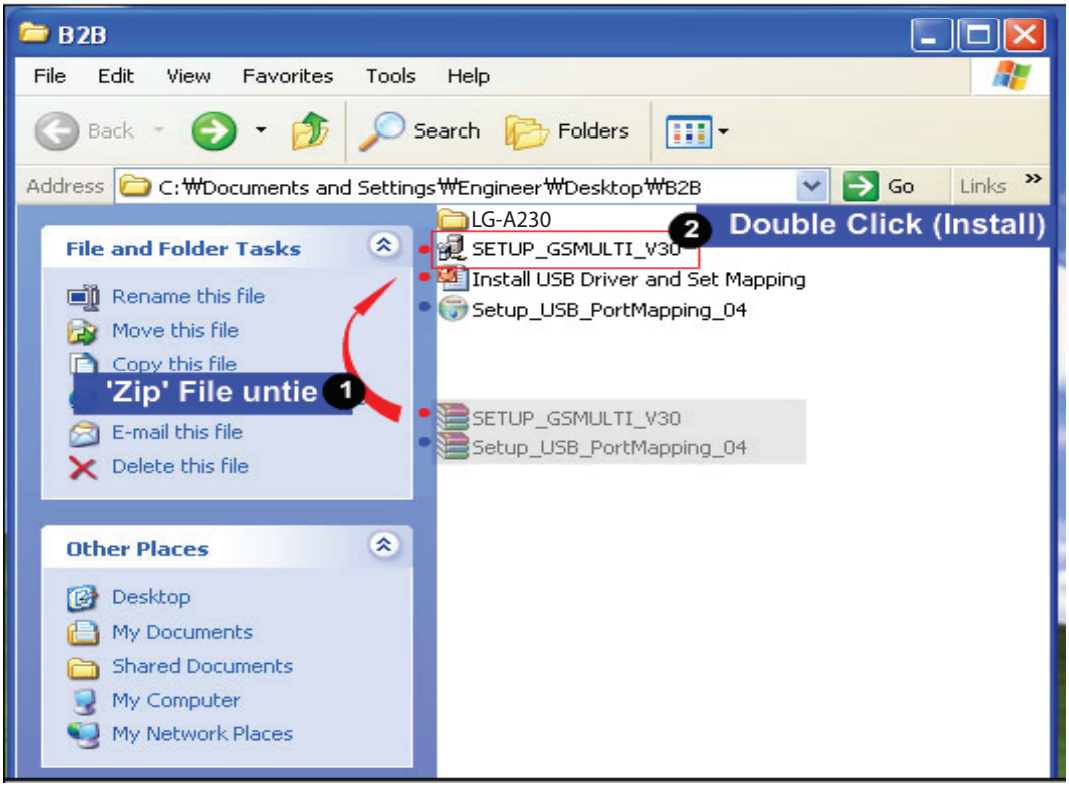


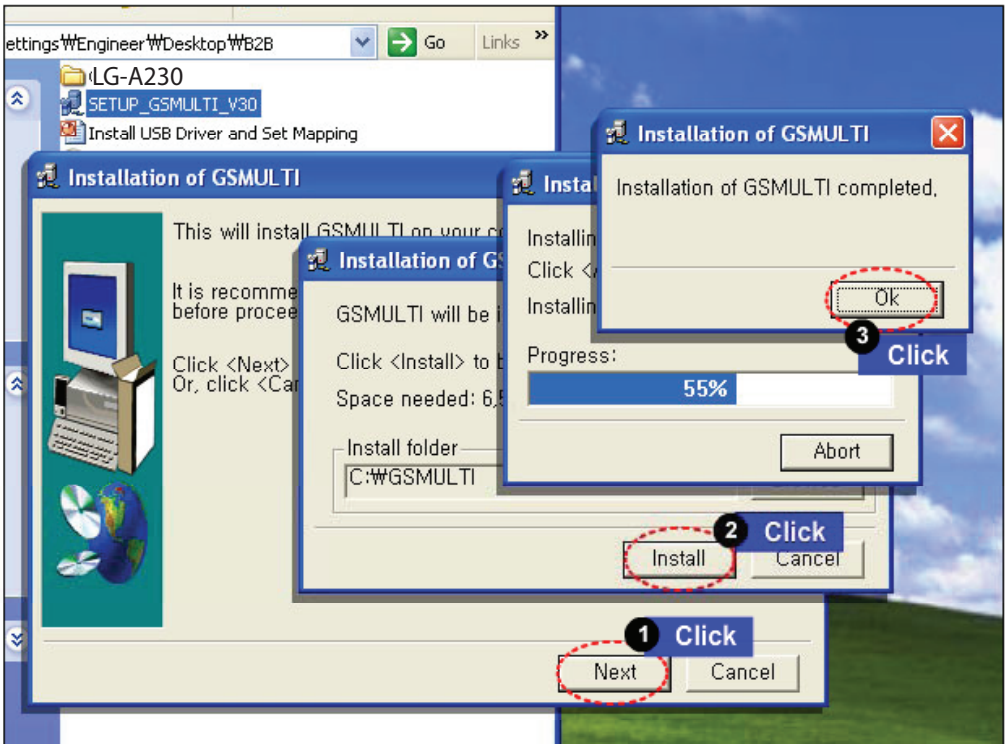
5. DOWNLOAD

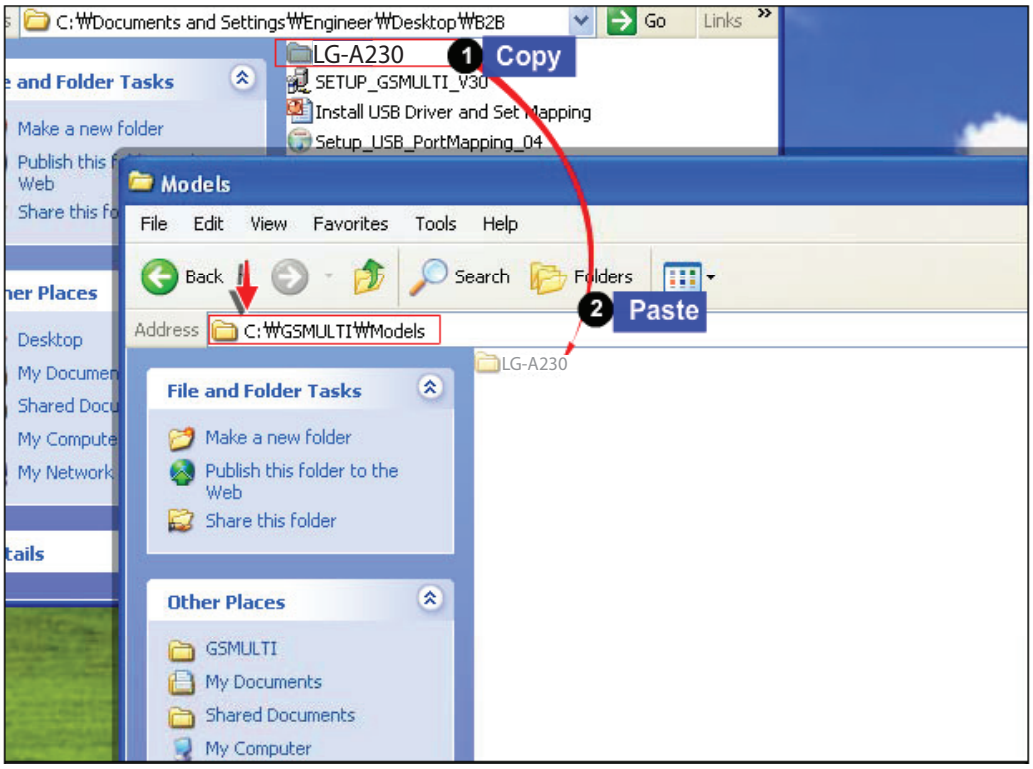


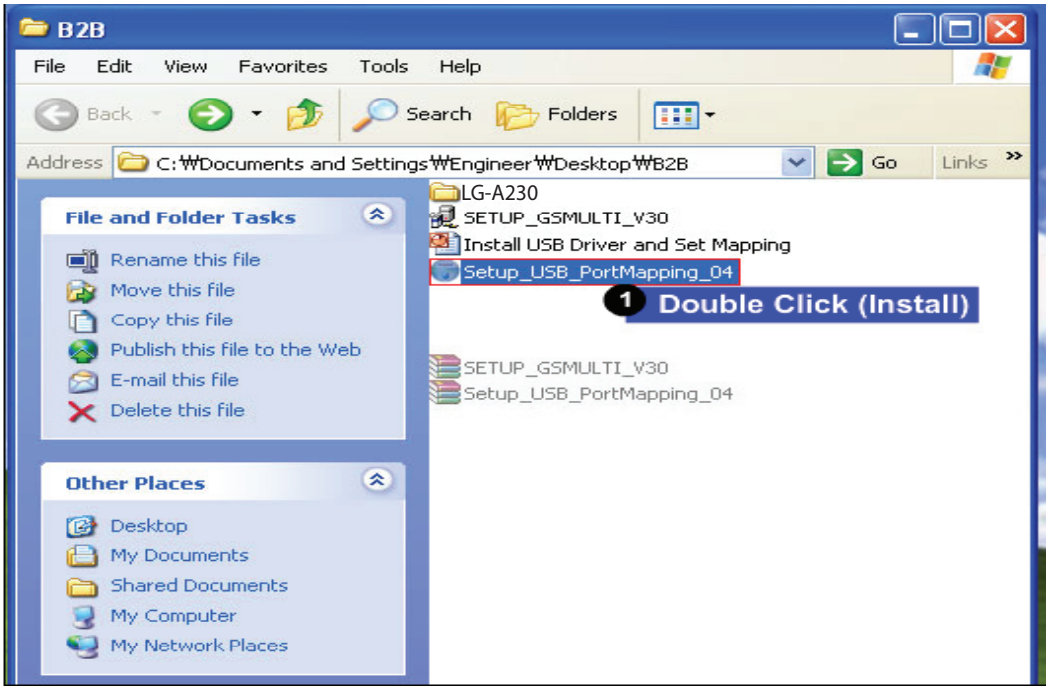


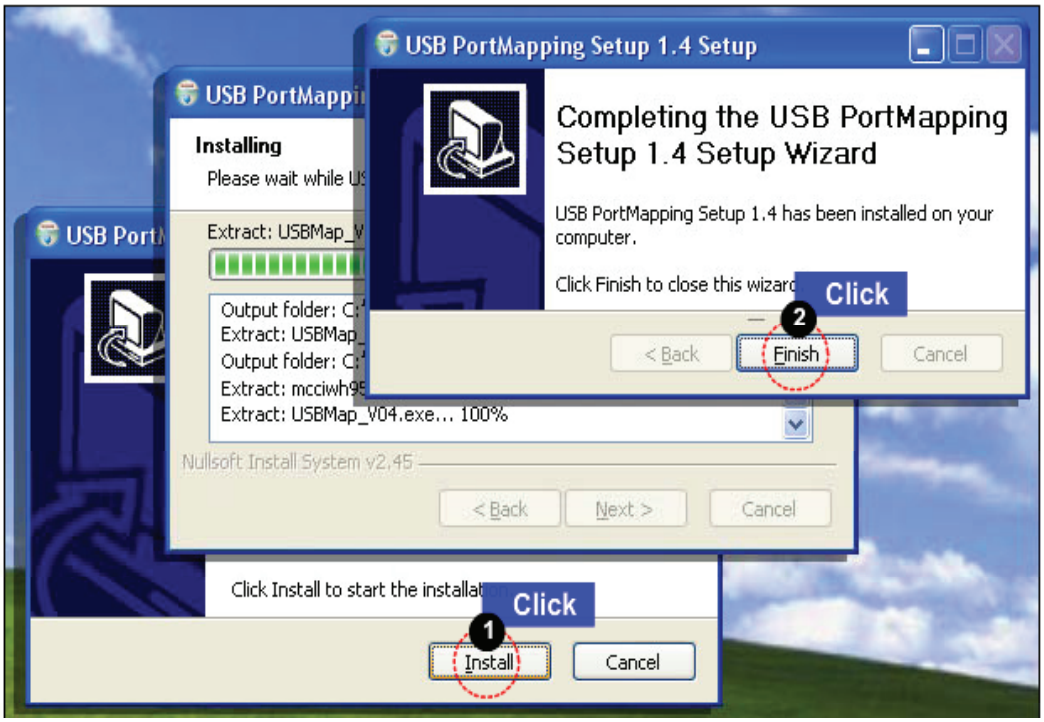


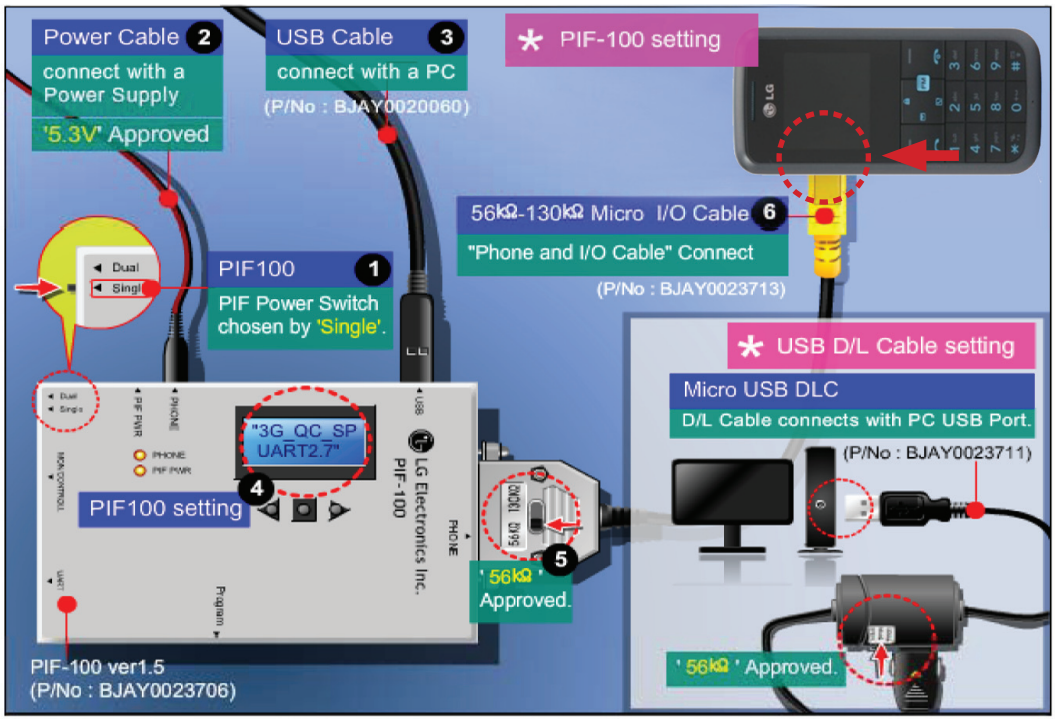


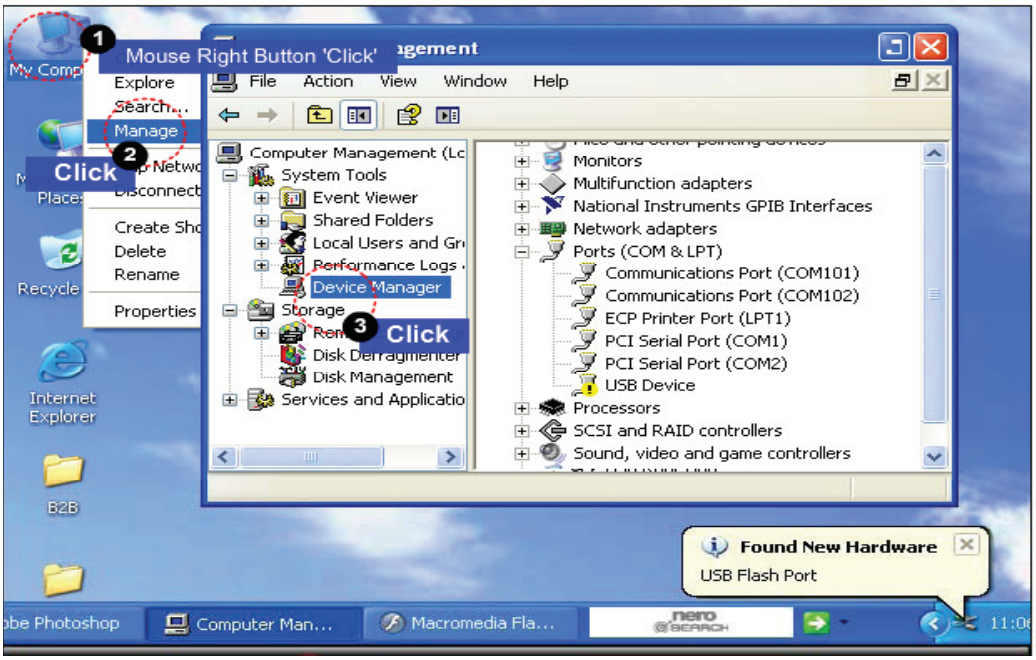


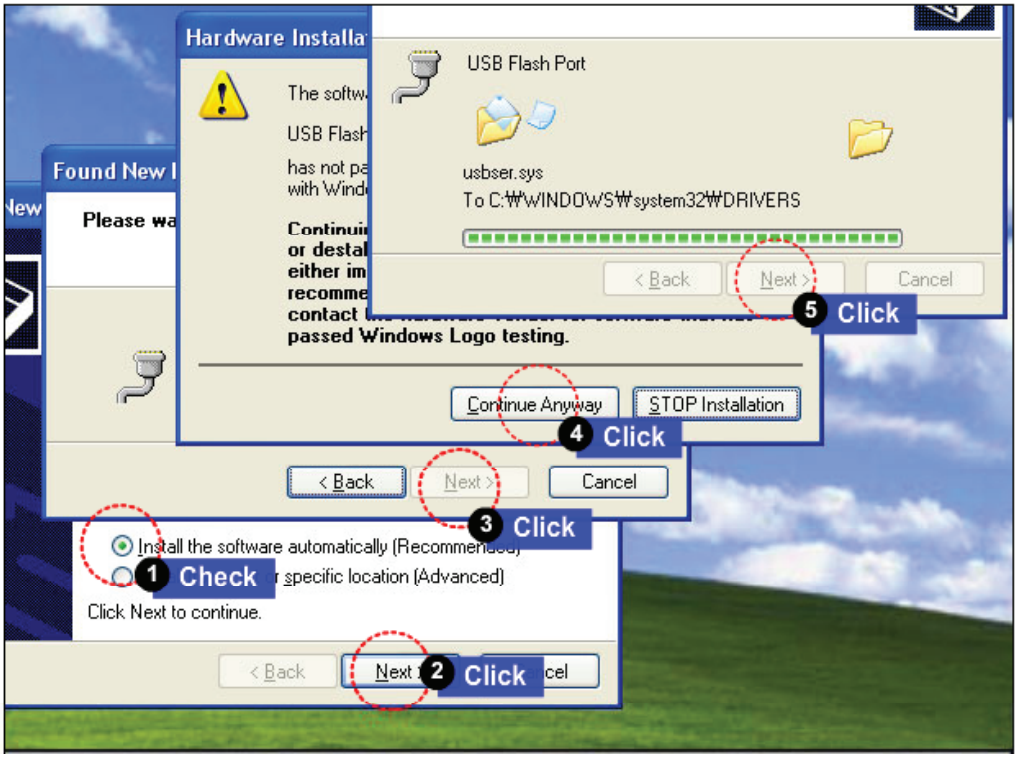


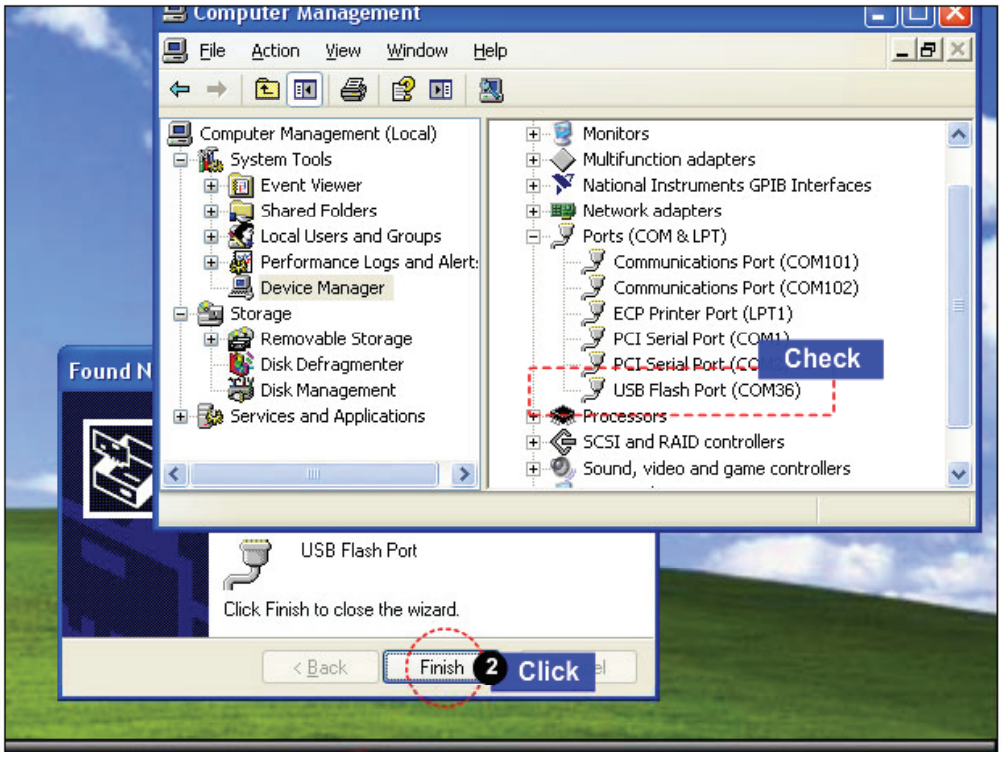


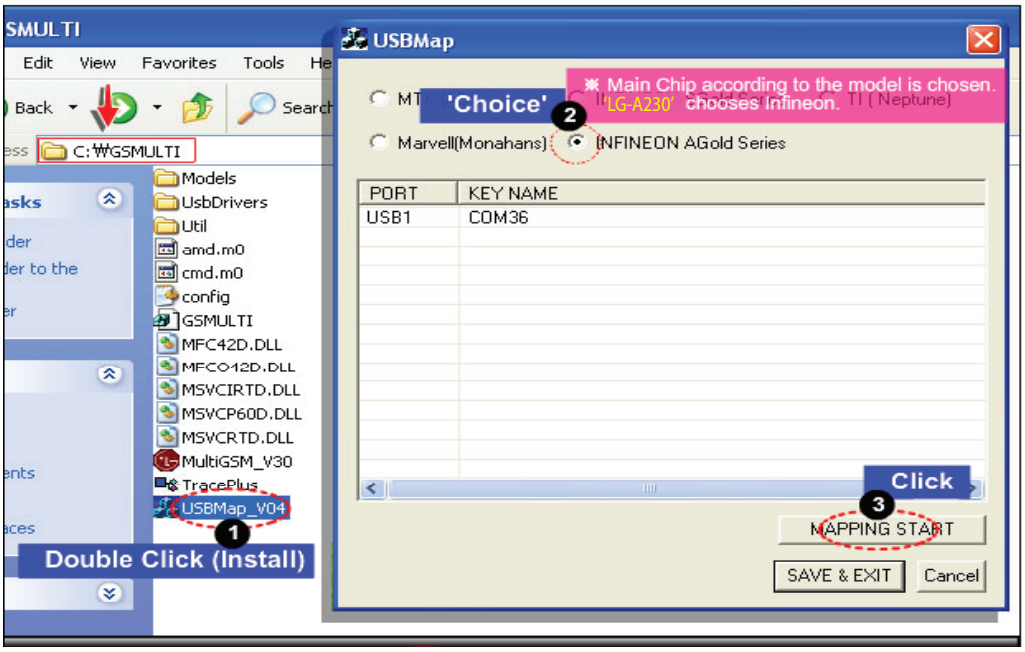


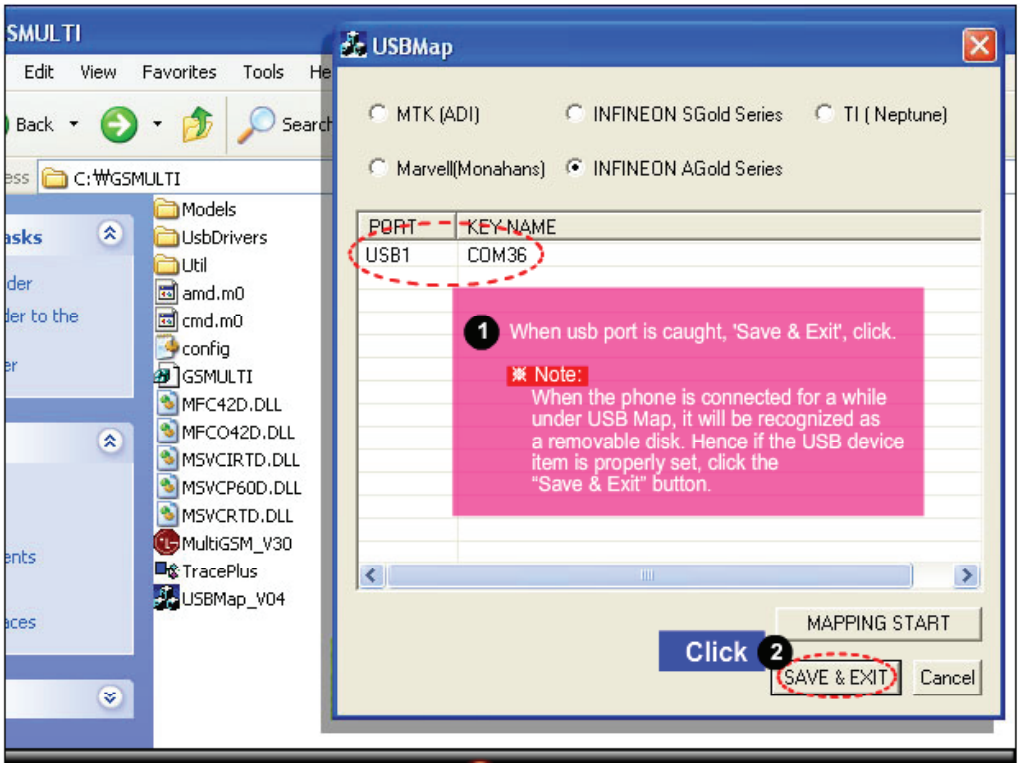


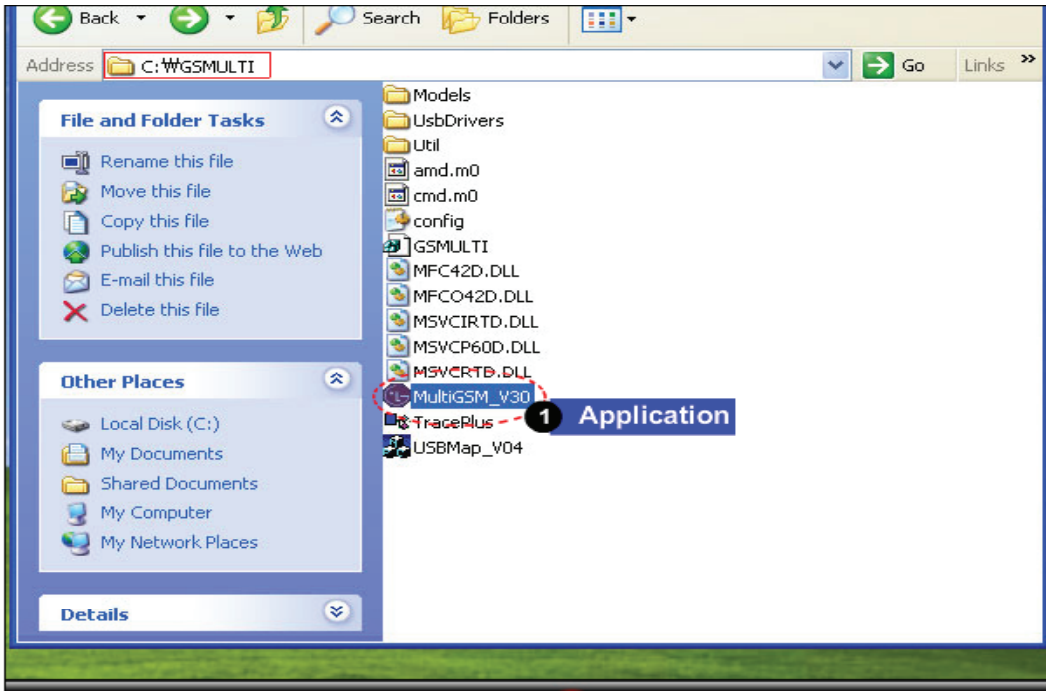


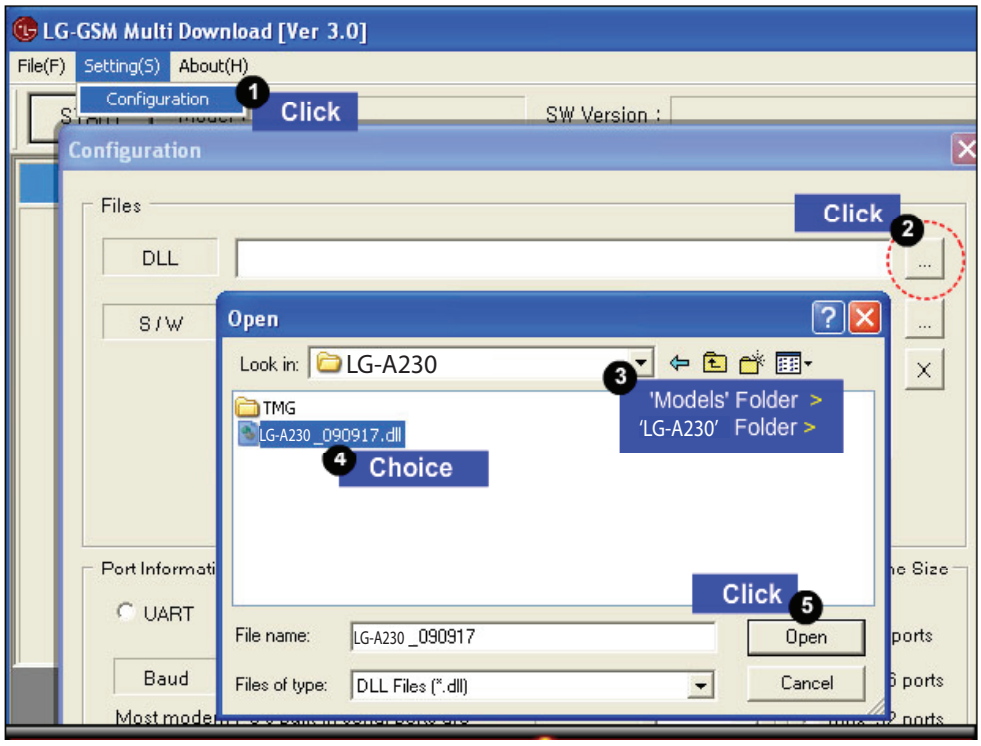


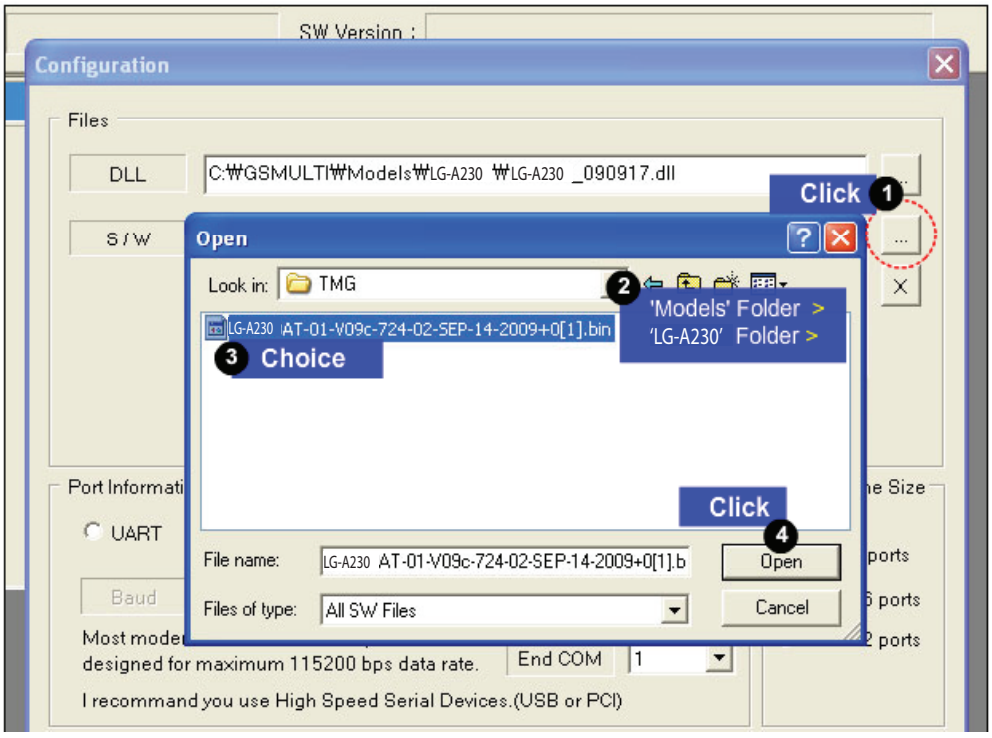


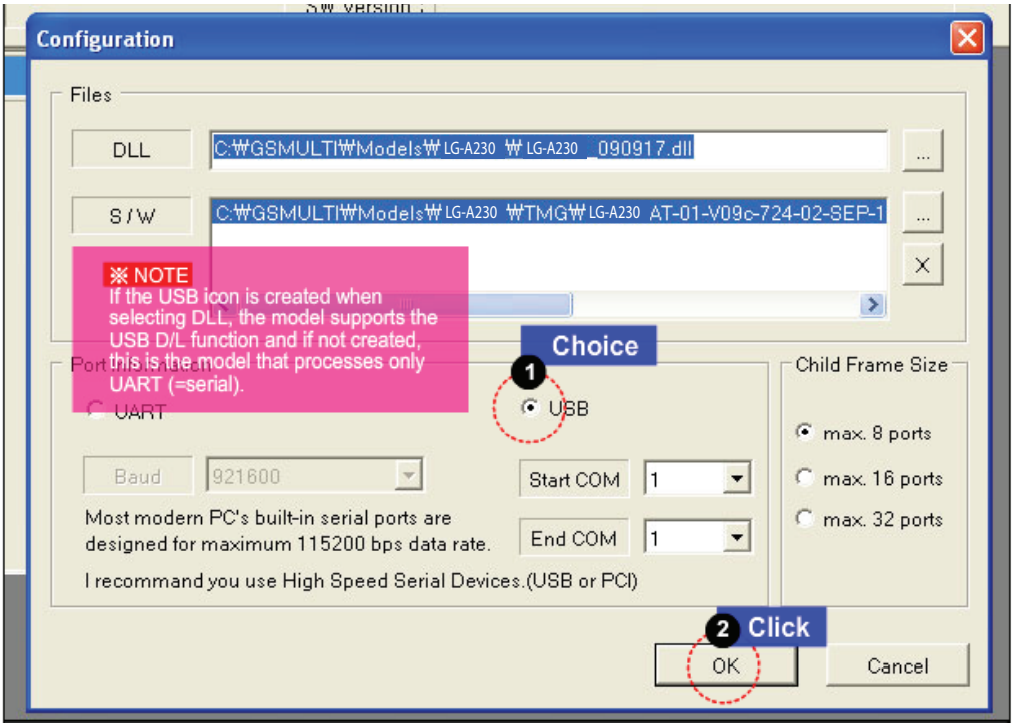


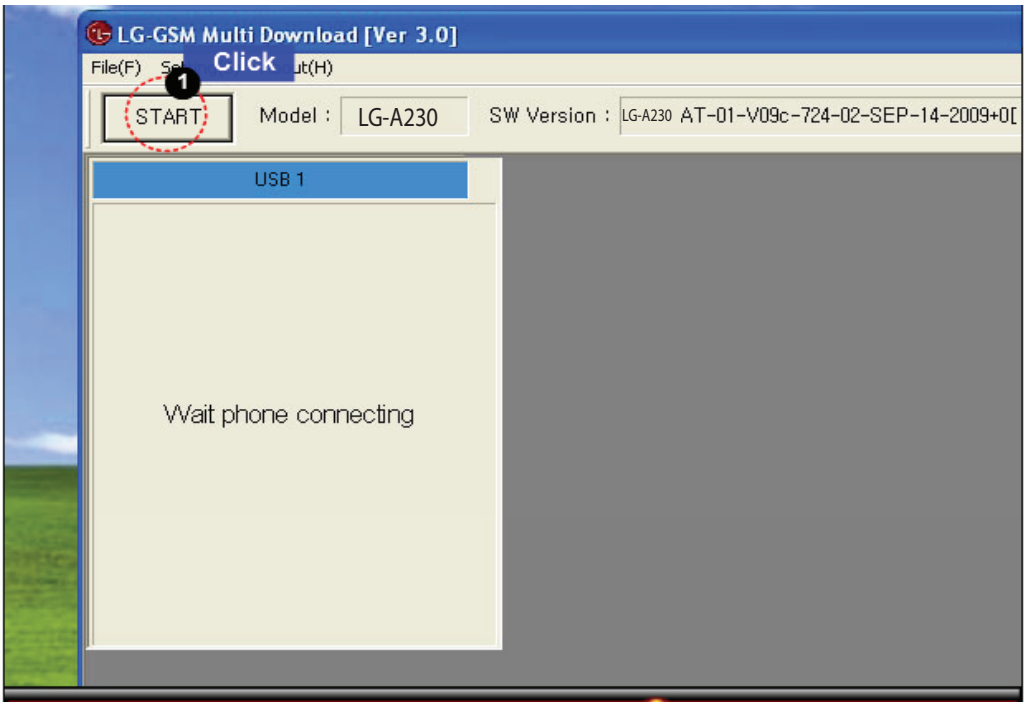


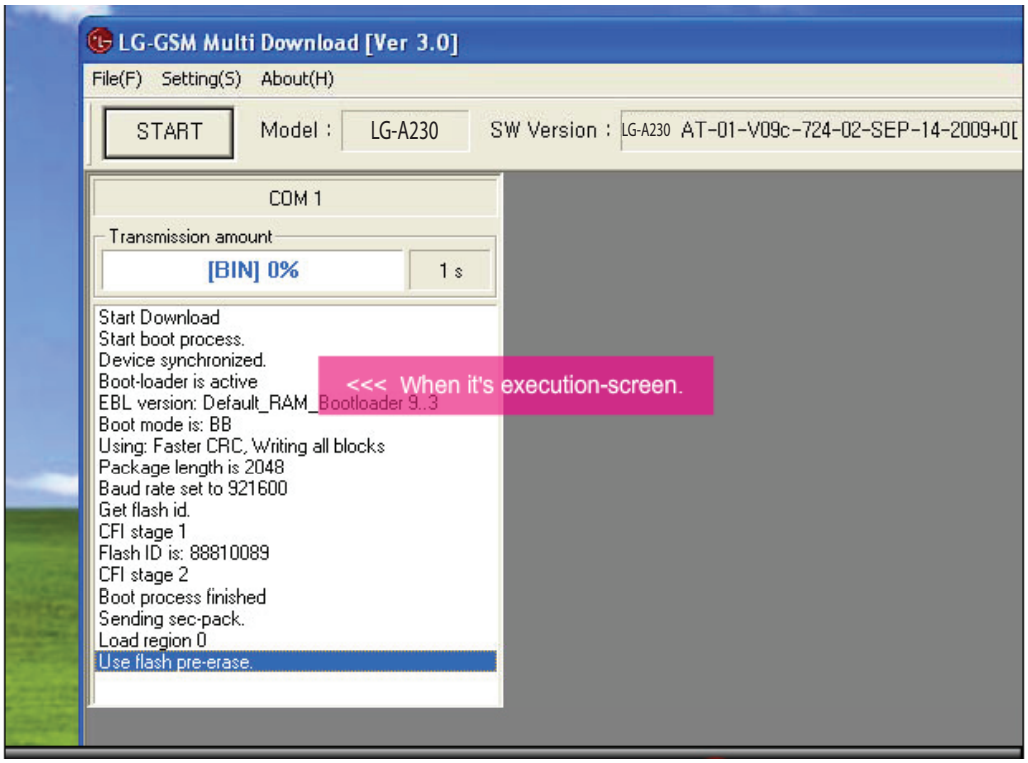


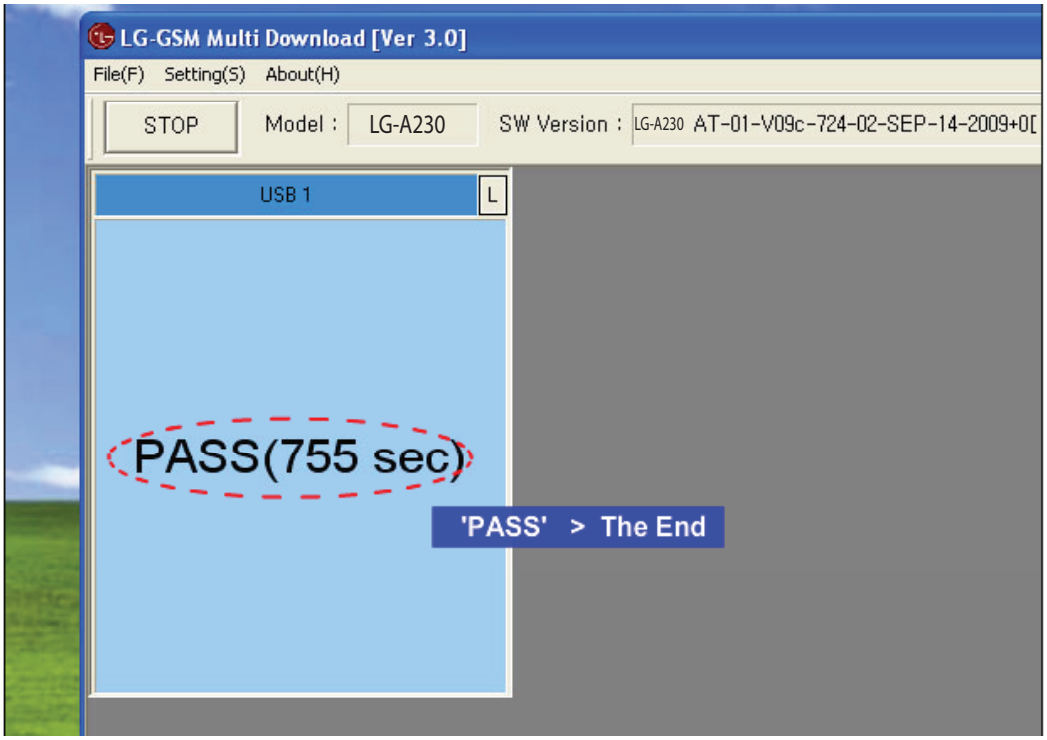




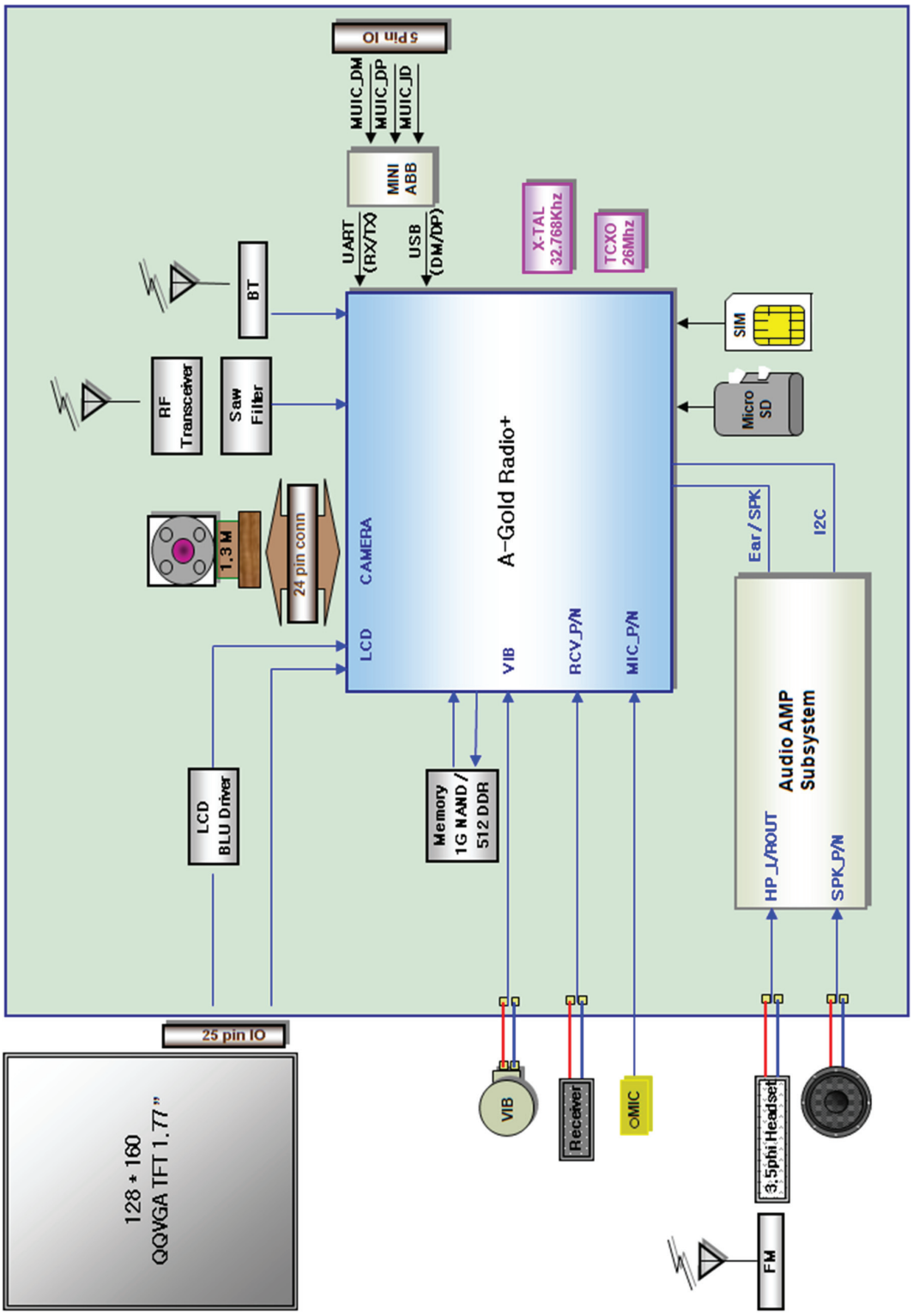






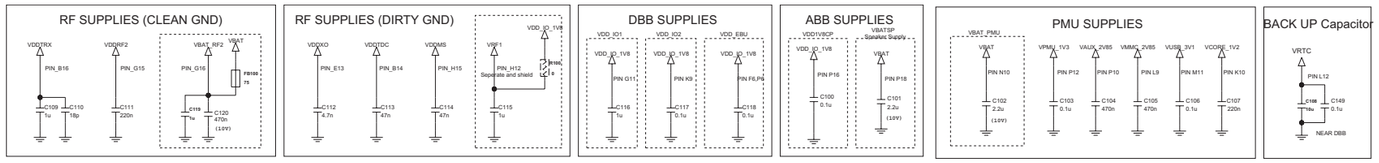


6. BLOCK DIAGRAM

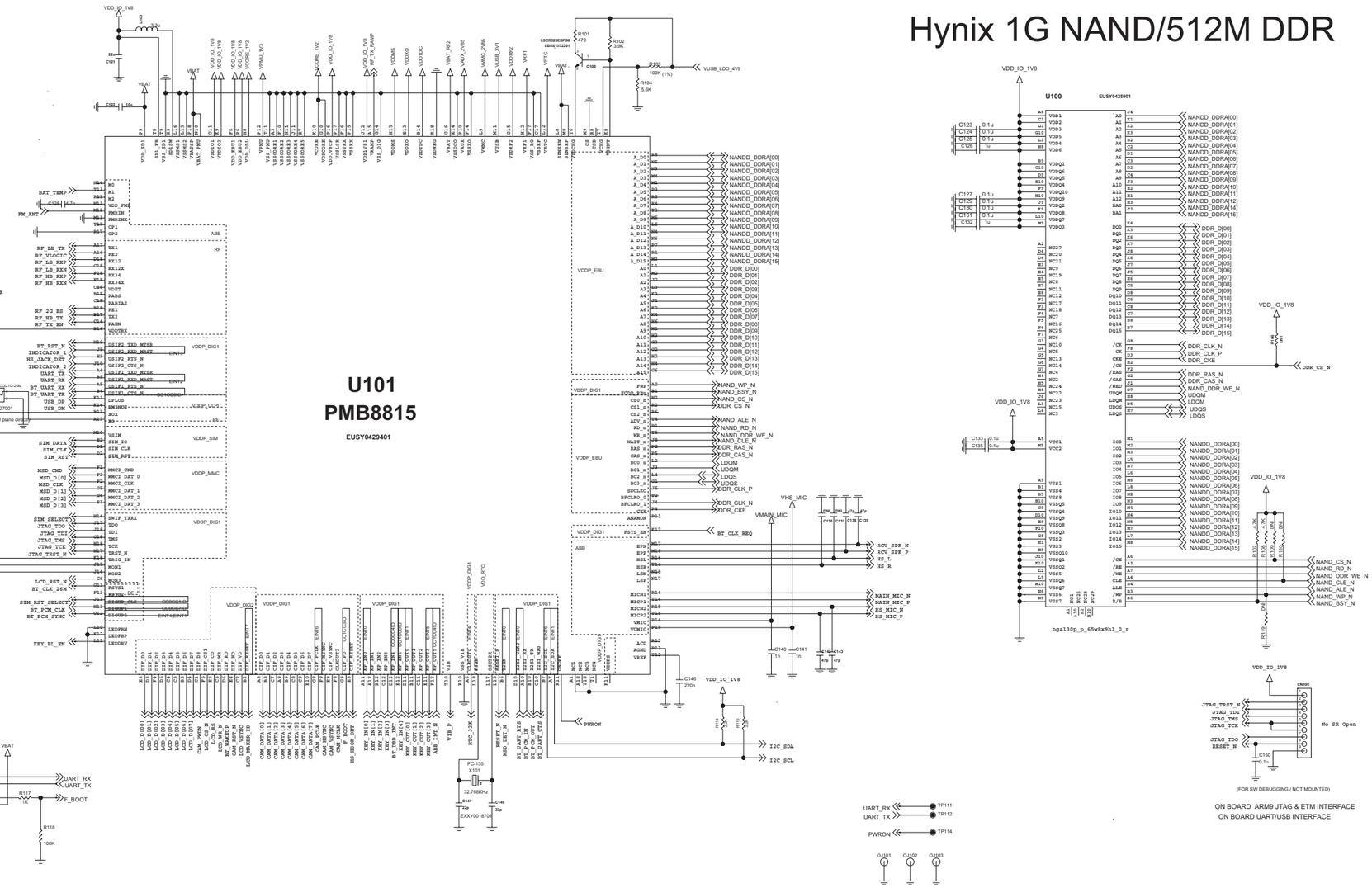


7. CIRCUIT DIAGRAM

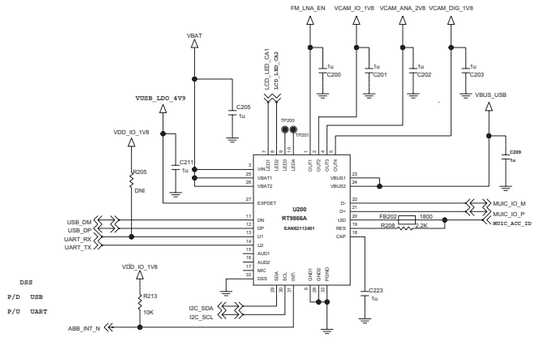
IFX_XMM215x_NAND



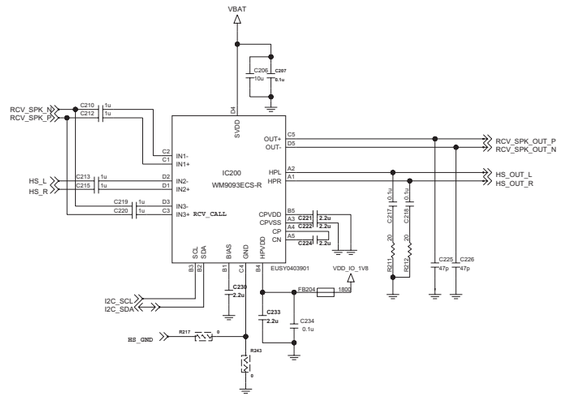
Hynix 1G NAND/512M DDR



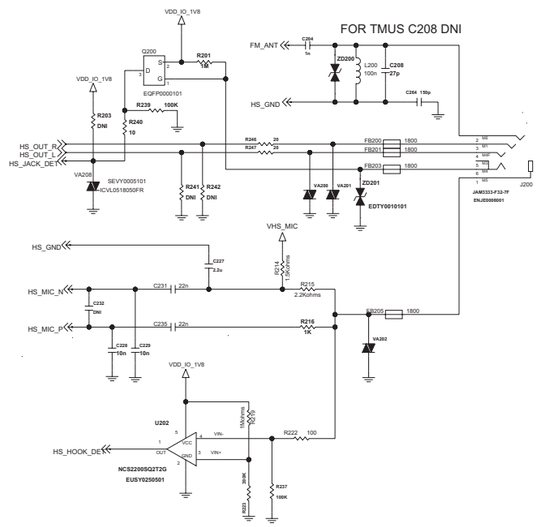
Mini ABB



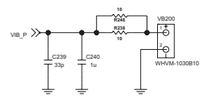
AUDIO SUBSYSTEM



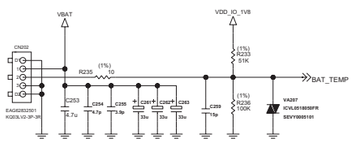
3.5phi JACK



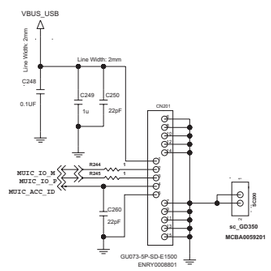
VIBRATOR



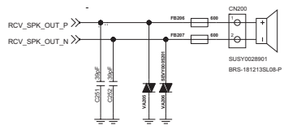
BATTERY CONNECTOR



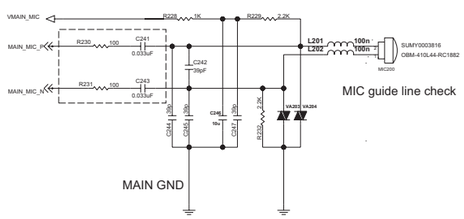
5PIN CONNECTOR



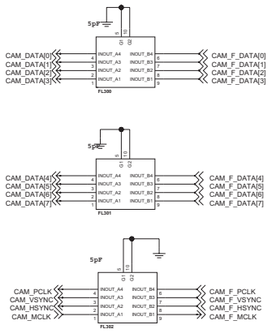
SPK/RCV Dualmode Circuit



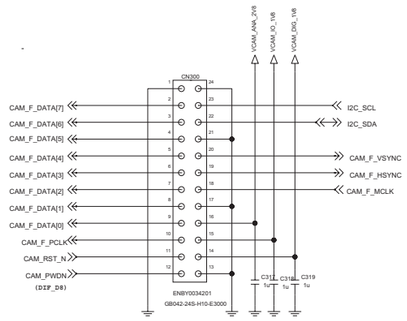
MICROPHONE



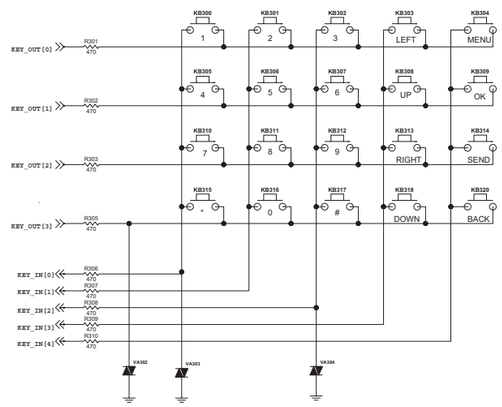
EMI FILTER



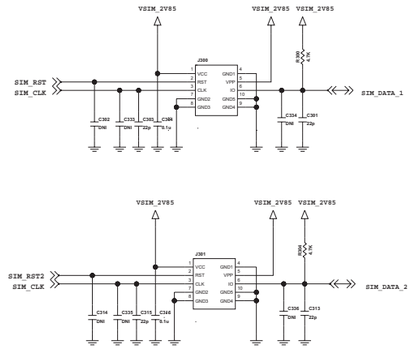
CAM CONN



KEY MATRIX



SIM_CONNECTOR

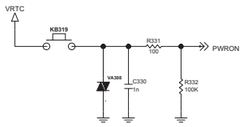


SIM SELECTION (Dual SIM)

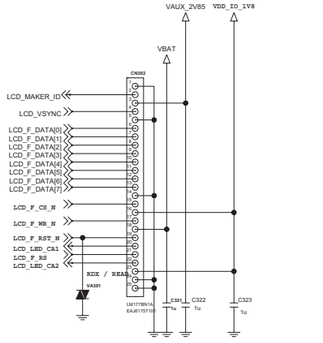
FOR SINGLE SIM - DNI

FOR SINGLE SIM (SHORT) SAFP0000401
FOR DUAL SIM (OPEN) SAFO0000401

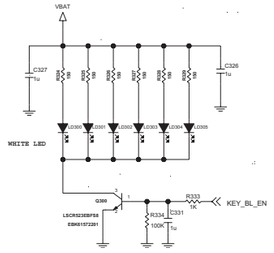
POWER ON KEY



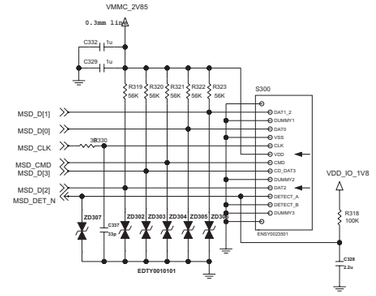
1.77" QQVGA_24pin FPC



KEY BACKLIGHT

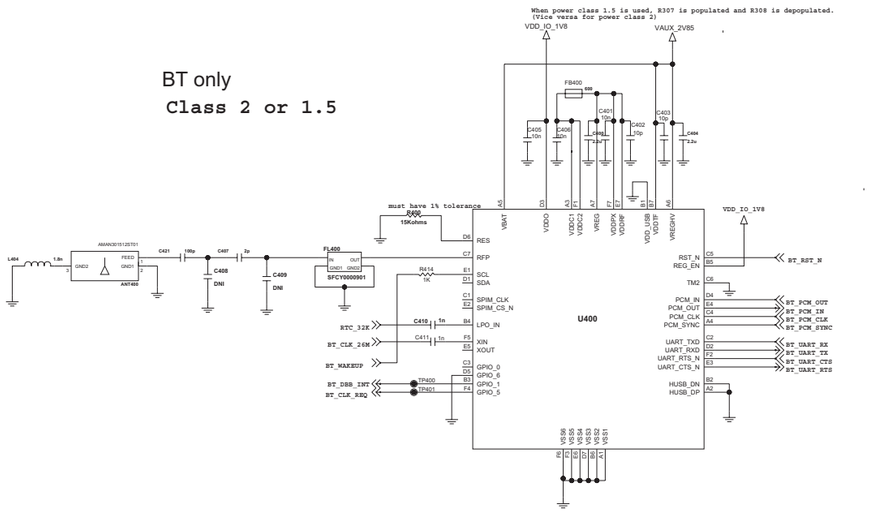


u-SD CARD_Reverse Type

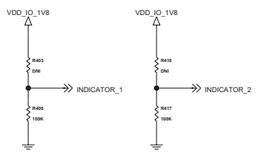


BT only

Class 2 or 1.5

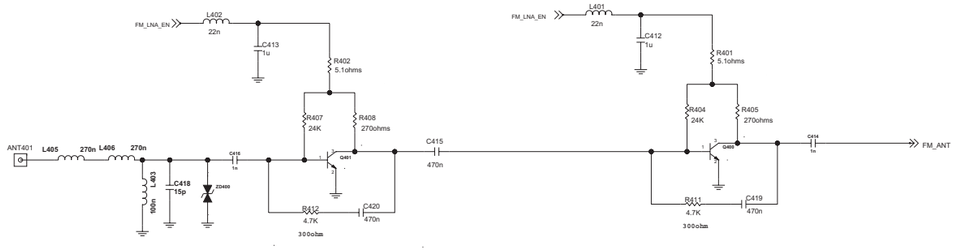


INDICATOR



		R403	R416	R406	R417	INDICATOR_1	INDICATOR_2
A230	Dual / 1.3M / Wireless FM	DNI	DNI	100k	100k	0	0
A235	single / 1.3M / Wireless FM	100k	DNI	DNI	100k	1	0
A225	single / VGA / Wireled FM	100k	100k	DNI	DNI	1	1
VARI_3	??	DNI	100k	100k	DNI	0	1

FM Radio(LNA)



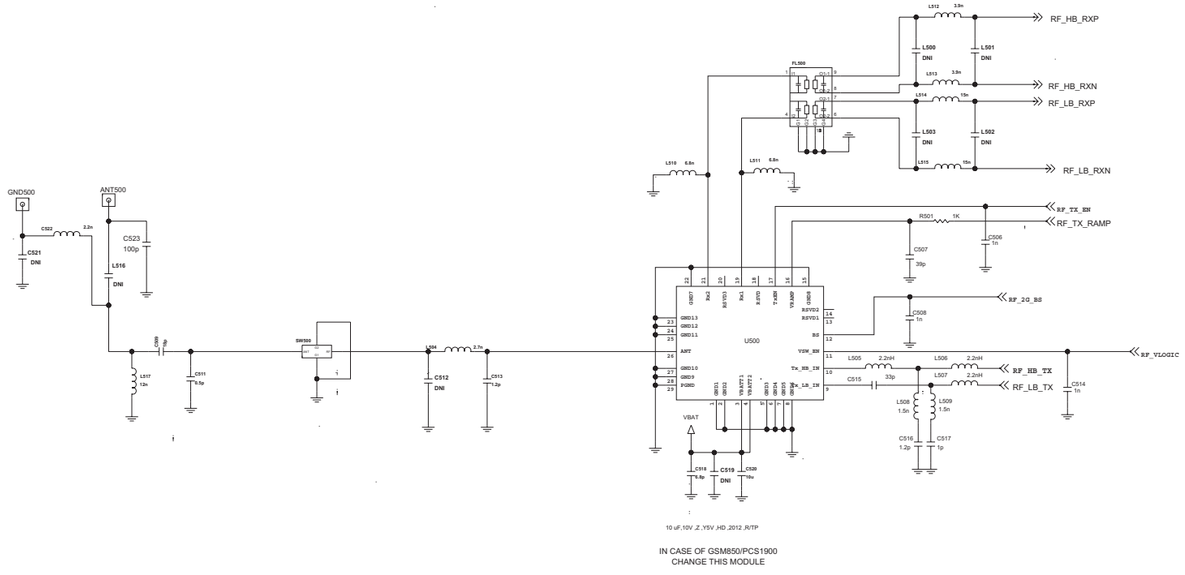
RF PART

MODE CONTROL LOGIC

MODE	VSW_EN	TxEN	BS
STANDBY	0	0	0
RX1	1	0	0
RX2	1	0	1
Tx_LB	1	1	0
Tx_HB	1	1	1

TX module

IN CASE OF GSM850/PCS1900
CHANGE THIS DUAL SAW FILTER
TO PART_NO SFSB0001301(B9310)

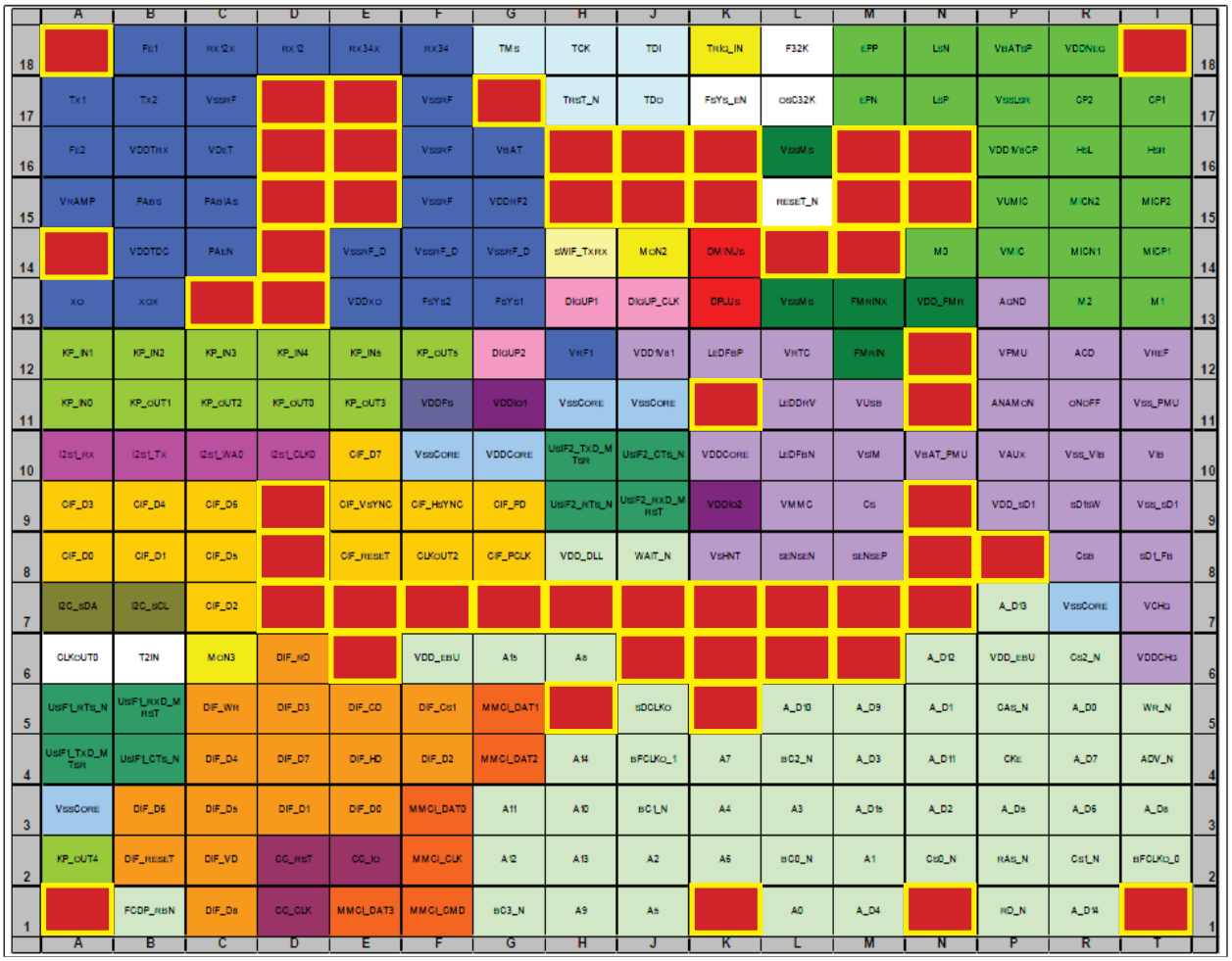


IN CASE OF GSM850/PCS1900
CHANGE THIS MODULE

8. BGA PIN MAP

BGA IC pin check (U101)

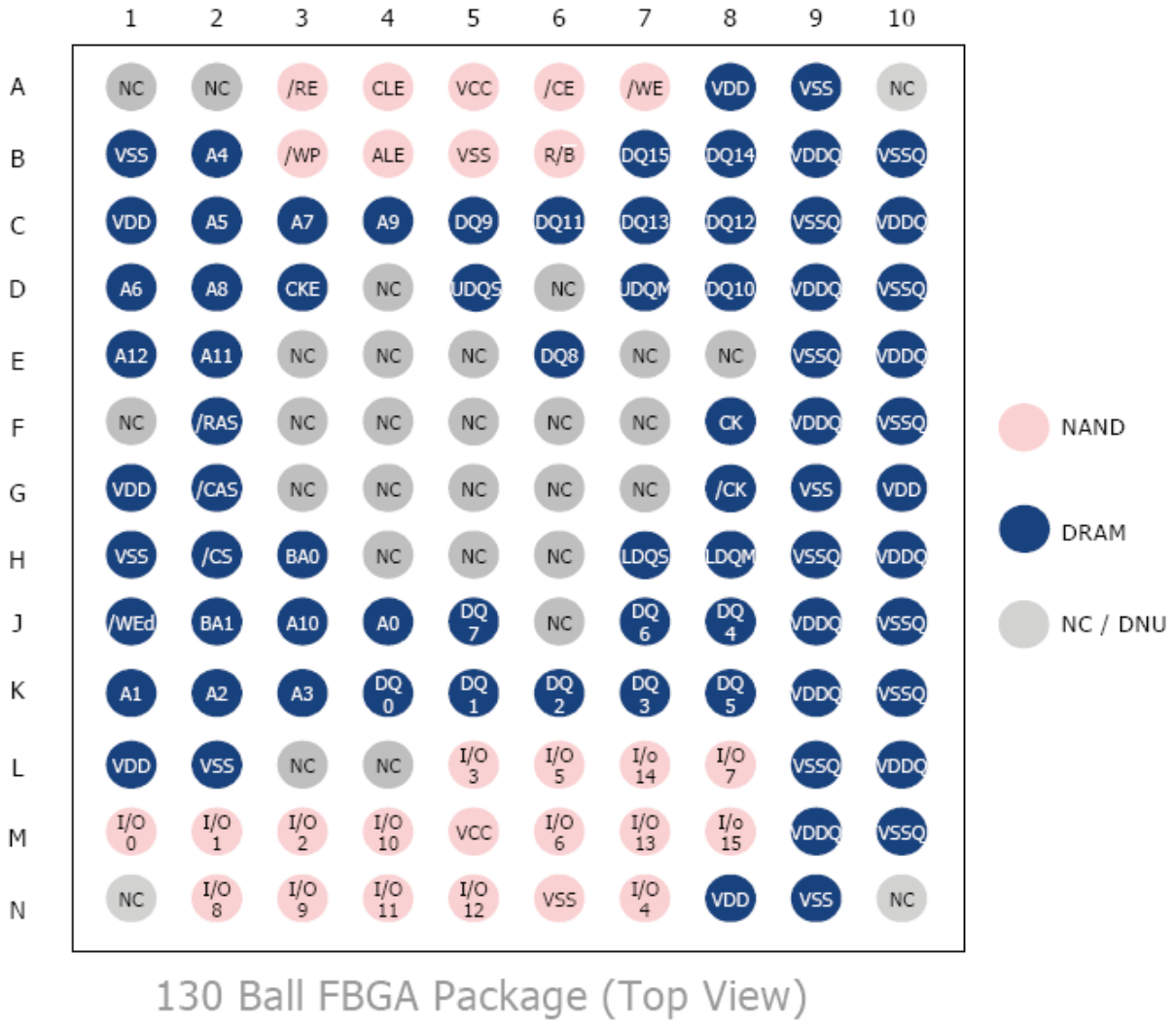
▪ **Ball Diagram (Top View), PMB8815**



: not in use

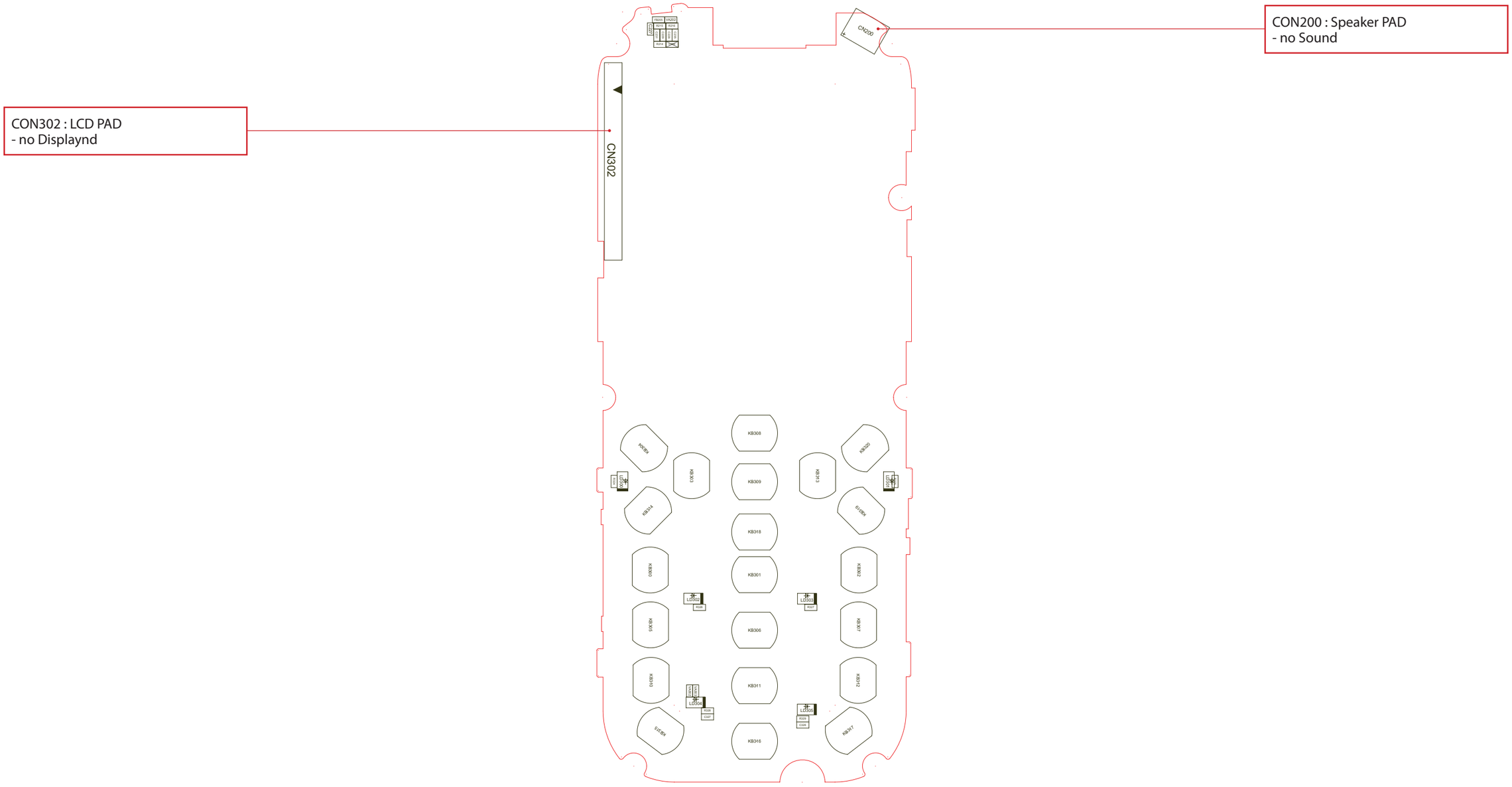
BGA IC pin check (U301)

▪ **Ball Diagram (Top View), H8BCS0QG0MMR**



130 Ball FBGA Package (Top View)

9. PCB LAYOUT



LG-A230_MAIN_EAX64026401_1.1_TOP

CN201 : I/O conn.
- no USB Connection.
- no Serial Connection.

CN300 : Camera Conn.
- no Camera

CN202 : Battery Conn.
- no power On

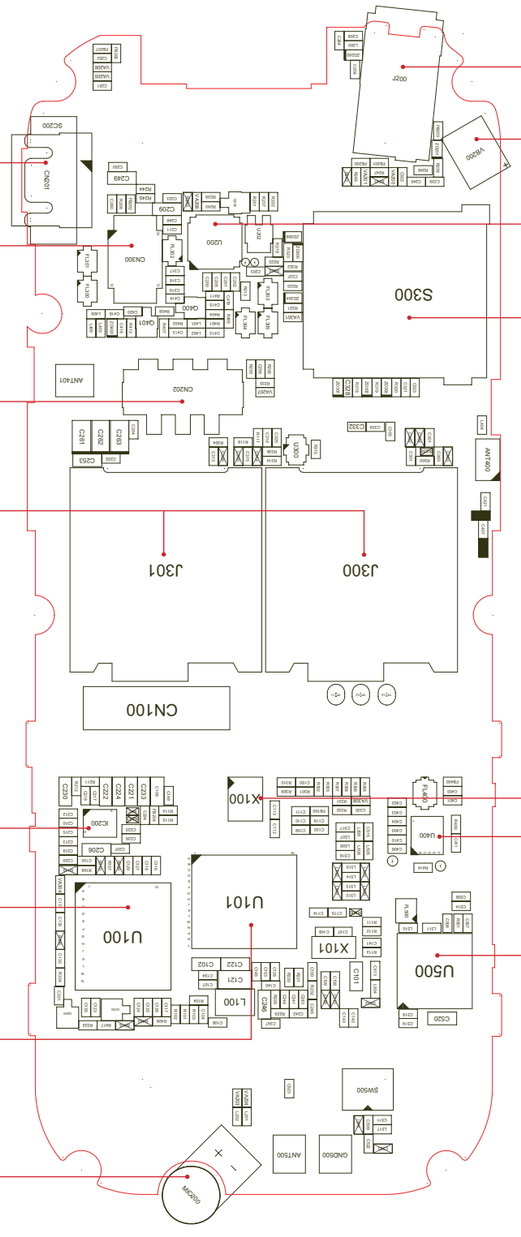
J301,J300 : SIM Conn.
- No SIM

IC200 : Audio Sub System.
- no Sound

U100 : Memory
- no Booting

U101 : BB IC
- no Power On
- no Servive
- no FM radio

MIC200 : MAIN MIC
- no voice sending
- no voice recording



J200 : 3.5 pai ear jack
- no Earphone, headset MIC

VB200 : Motor PAD
- no Vibrator

U200 : ChargePump,PMIC : MUIC
- no Booting
- no USB/Serial Connection
- no Battery Charge
- no LCD backlight
- no Camera

S300 : external Memory socket
- no External memory

X100 : 26Mhz X-tal
- no Power On
- no Service

U400 : BT Module
- no BT Connection

U500 : TX Module
- no Service
- RF Sensitivity & TX Power

LG-A230_MAIN_EAX64026401_1.1_BOT

10.ENGINEERING MODE

Engineering mode is designed to allow a service man/engineer to view and test the basic functions provided by a handset. The key sequence for switching the engineering mode on is "1809#*230# "Select. Pressing END will switch back to non-engineering mode operation. Use Up and Down key to select a menu and press 'select' key to progress the test. Pressing 'back key will switch back to the original test menu.

[1] Factory Mode

[1-1] Device Test

[1-1-1] Auto All Test
[1-1-2] Auto All Test Result
[1-1-3] Main LCD
[1-1-5] LCD Backlight
[1-1-6] Key Backlight
[1-1-7] Speaker
[1-1-8] Vibrator
[1-1-8] Vibrator
[1-1-9] Vibrator Duration
Camera
MicRcv
Key Press Test
SpeakerVibTest

[1-2] ELT Mode

[1-2-1] Automatic
[1-2-2] Manual

[1-3] SW Sanity Test

[1-3-1] FPRI Test
[1-3-2] DB Check
[1-3-3] E Serial NO
[1-3-4] UA.String
[1-3-5] Unlock SIM

[1-4] Factory Reset

[1-5] Version

[2] Eng Mode

[2-1] Call Timer

[2-2] Eng Mode

[2-2-1] Band Selection
[2-2-1-1] Mattery Info
[2-2-1-2] LCD Info
[2-2-1-3] SD Card Info

[2-2-2] Remote Band
[2-2-2-1] Auto
[2-2-2-2] GSM 850
[2-2-2-3] GSM 900
[2-2-2-4] DCS 1800
[2-2-2-5] PCS 1900

[2-2-3] Battery Info
[2-2-4] Audio Tunning
[2-2-5] UART Setting
[2-2-6] BT Testing
[2-2-7] ERS & CoreDump
[2-2-8] SD Card Info

[2-3] Network Info
[2-4] Others

[2-5-1] Bluetooth Test Menu
[2-5-2] PS Attach Mode
[2-5-3] Packet Data Connection
[2-5-4] Module Test
[2-5-6] DRM Test Set
[2-5-7] MMS Test
[2-5-8] Auto Call Test
[2-5-9] Aging Test
[2-5-10] SIM Info
RPC Status
ICCID STatus

[2-5] Debug Setting

11. STAND ALONE TEST

11.1 Introduction

This manual explains how to examine the status of RX and TX of the model.

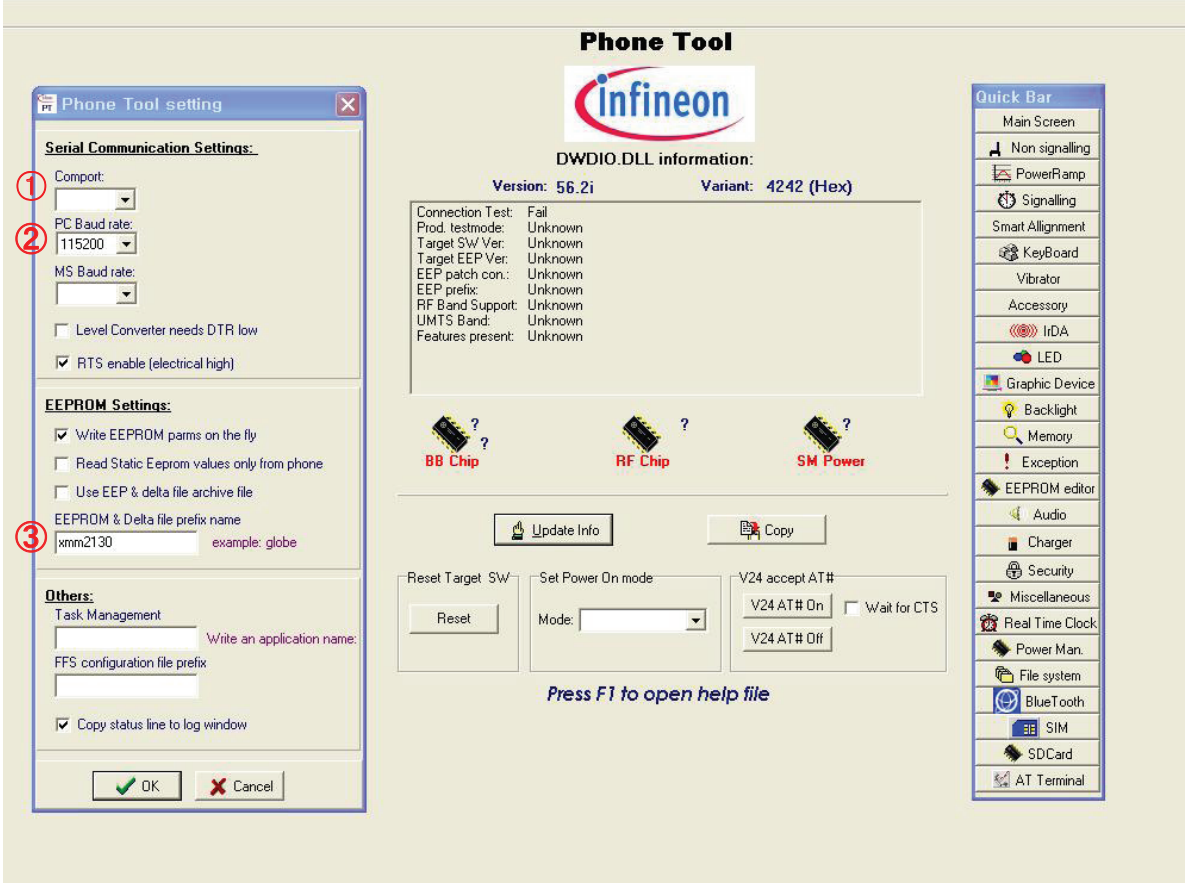
A. Tx Test

TX test - this is to see if the transmitter of the phones is activating normally.

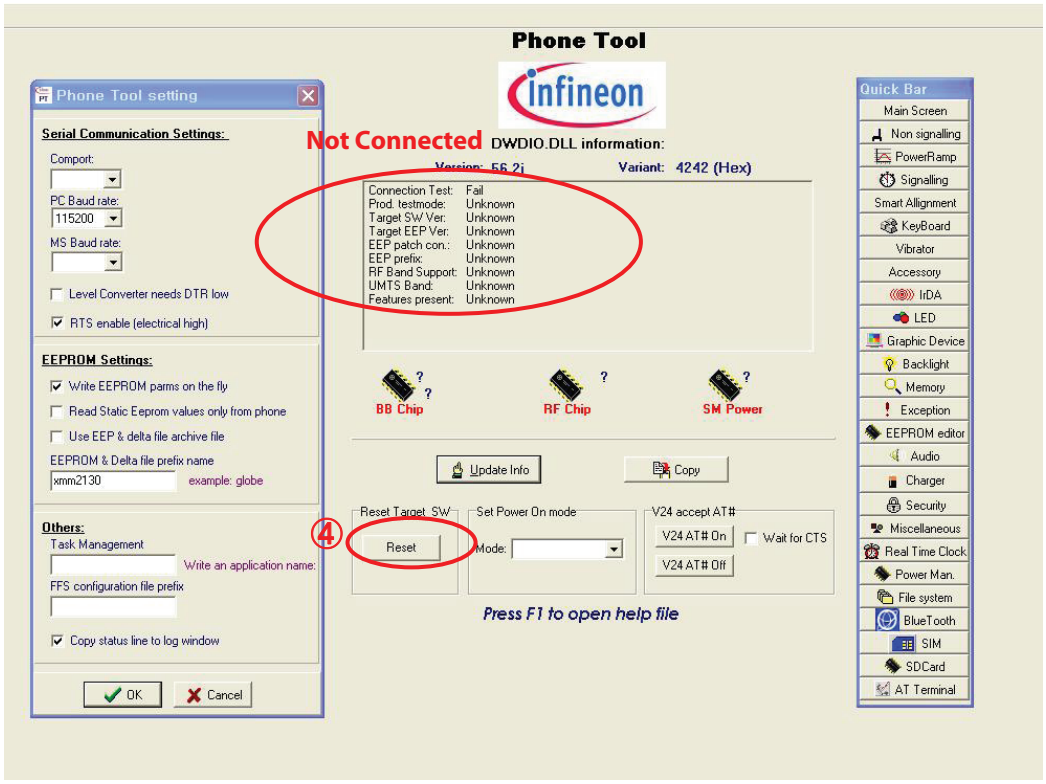
B. Rx Test

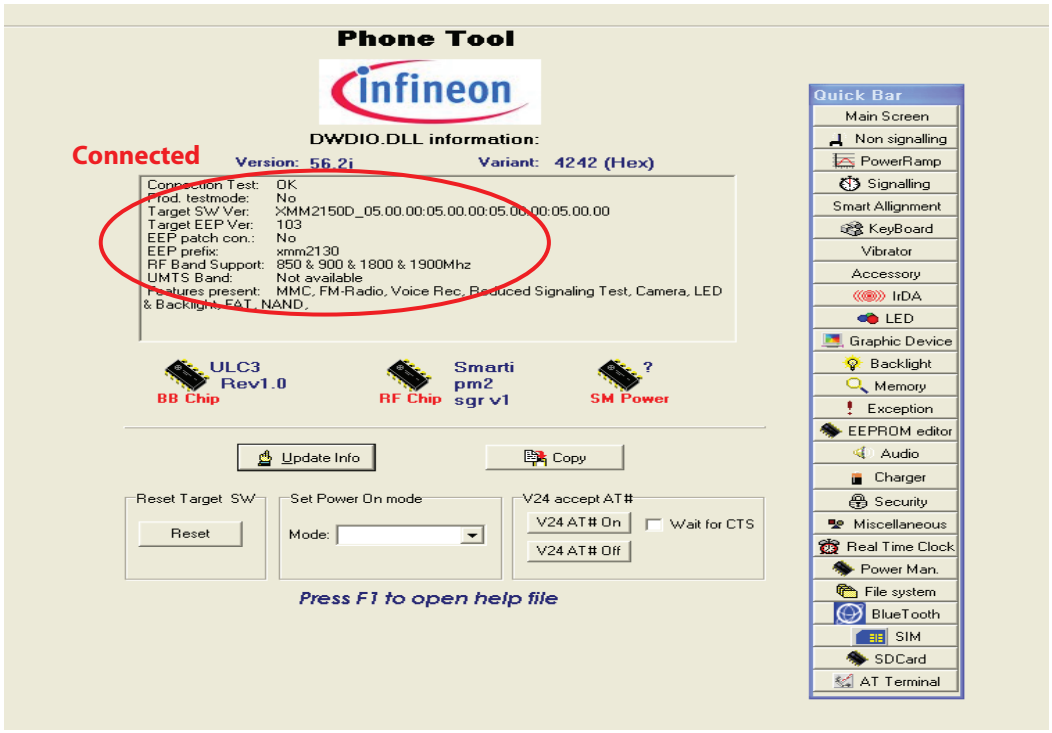
RX test - this is to see if the receiver of the phones is activating normally.

11.2 Setting Method

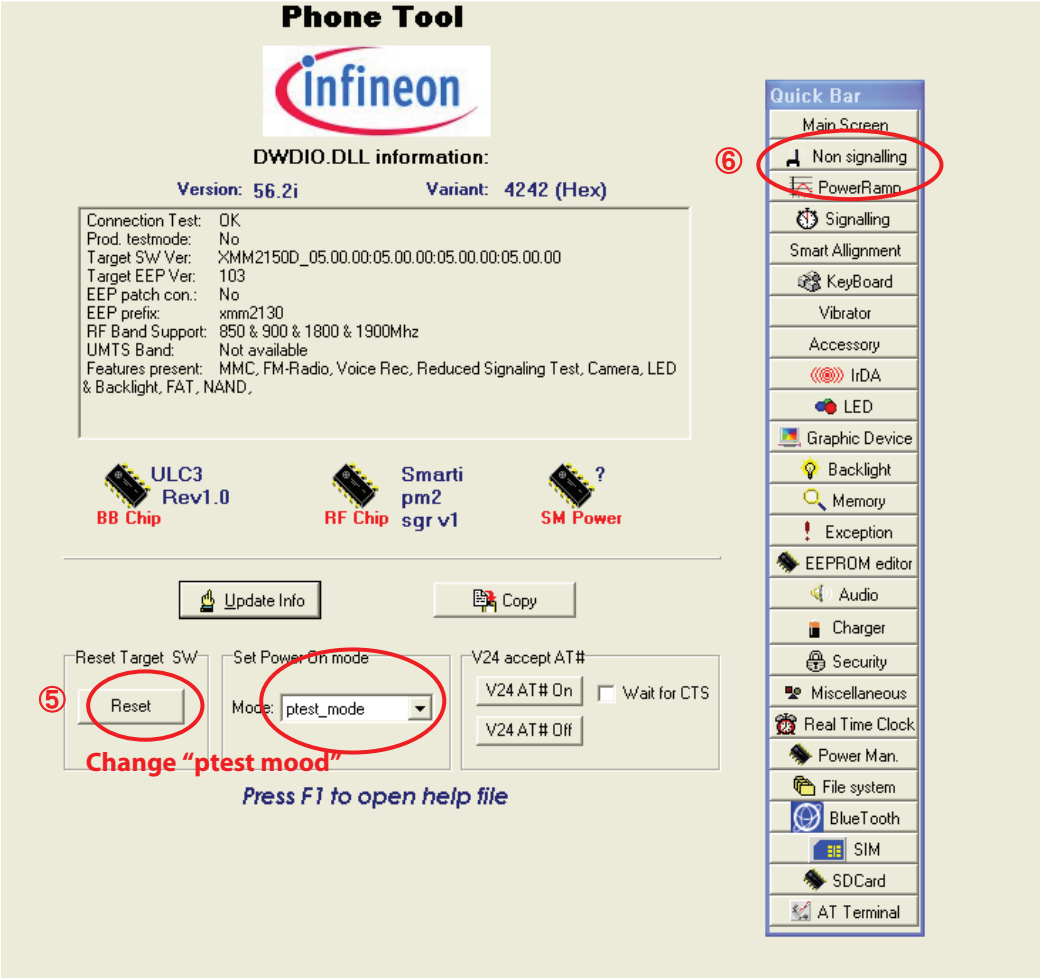


1. Set COM Port
2. Check PC Baud Rate
3. Confirm EEPROM & Delta file prefix name



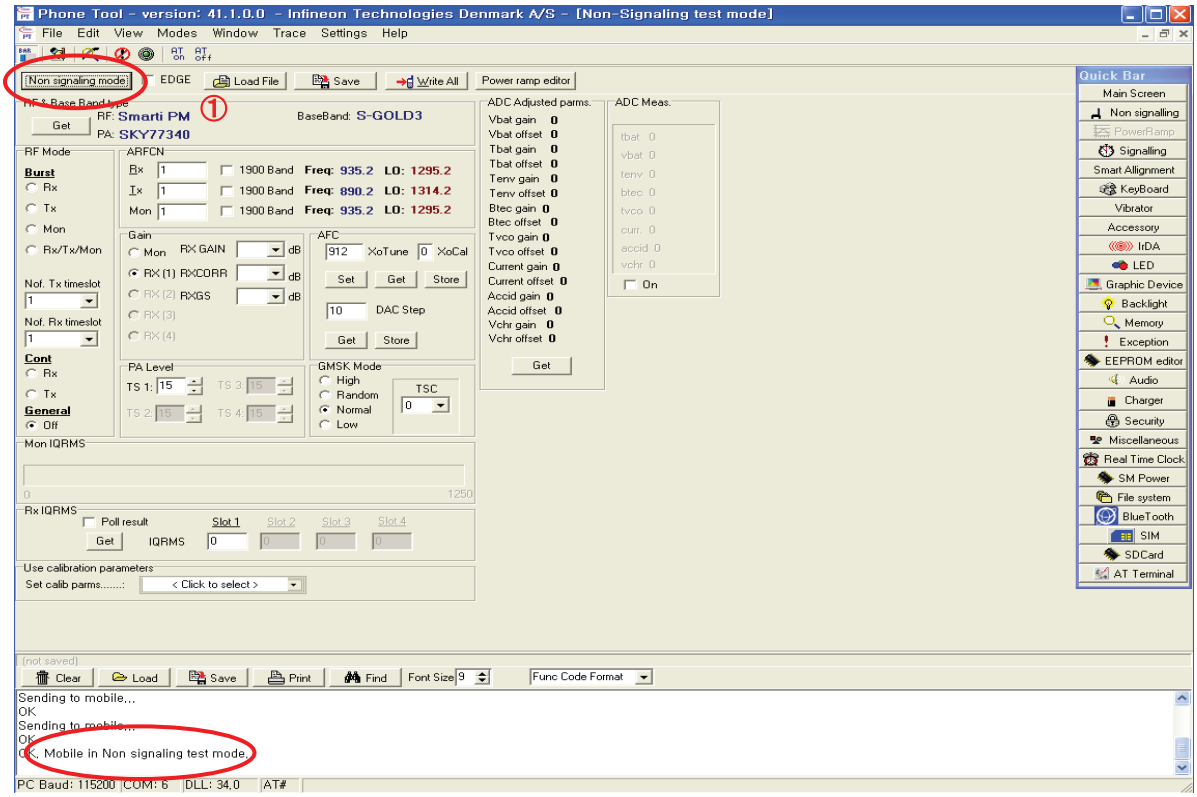


4. Click “Update Info” for communicating Phone and Test-Program

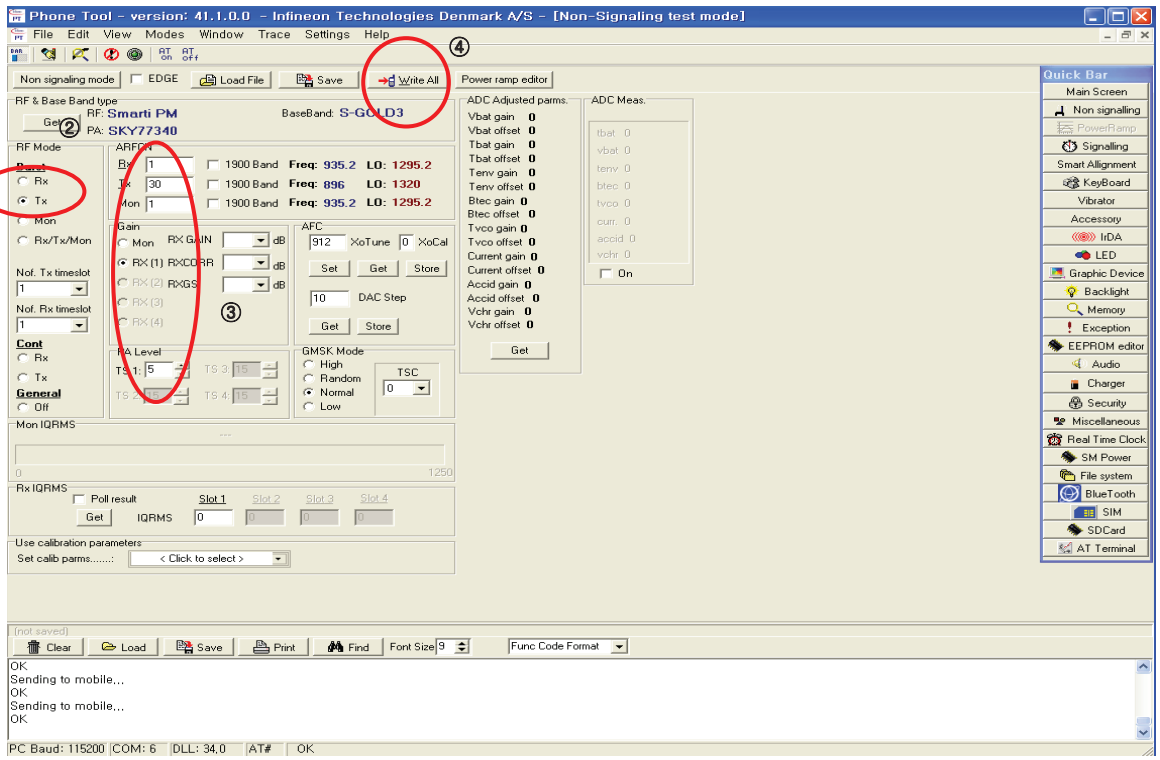


5. For the purpose of the Standalone Test, Change the Phone to "ptest mode" and then Click the "Reset" bar.
6. Select "Non signaling" in the Quick Bar menu. Then Standalone Test setup is finished.

11.3 Tx Test

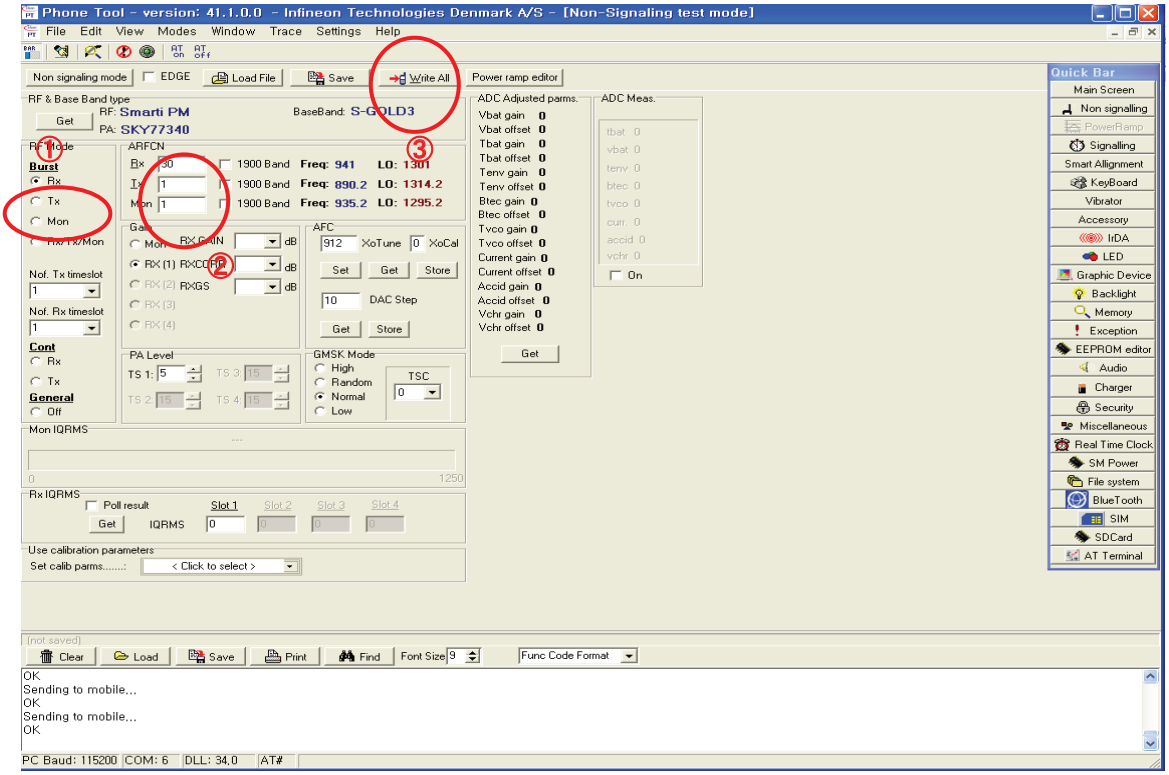


1. “Non signaling mode” bar and then confirm “OK” text in the command line.

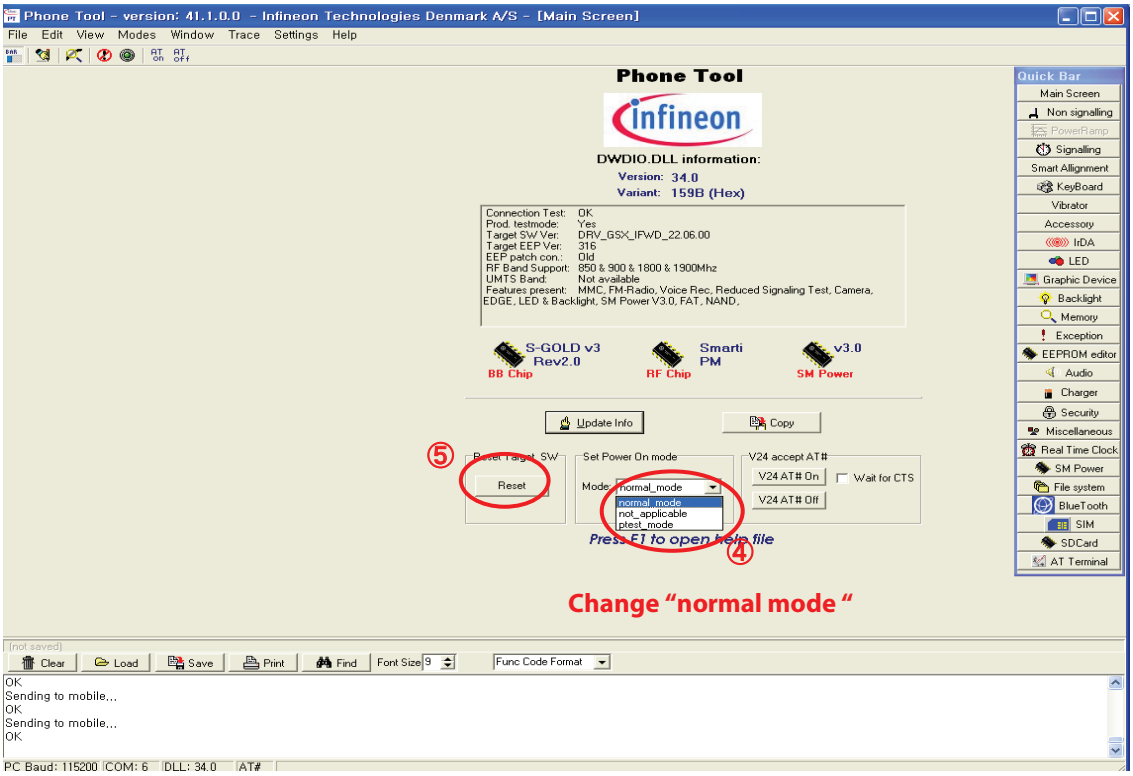


2. Put the number of TX Channel in the ARFCN
3. Select “Tx” in the RF mode menu and “PCL” in the PA Level menu.
4. Finally, Click “Write All” bar and try the efficiency test of Phone.

11.4 Rx Test



1. Put the number of RX Channel in the ARFCN.
2. Select “Rx” in the RF mode menu.
3. Finally, Click “Write All” bar and try the efficiency test of Phone.



4. The Phone must be changed “normal mode” after finishing Test.
5. Change the Phone to “normal mode” and then Click the “Reset” bar.

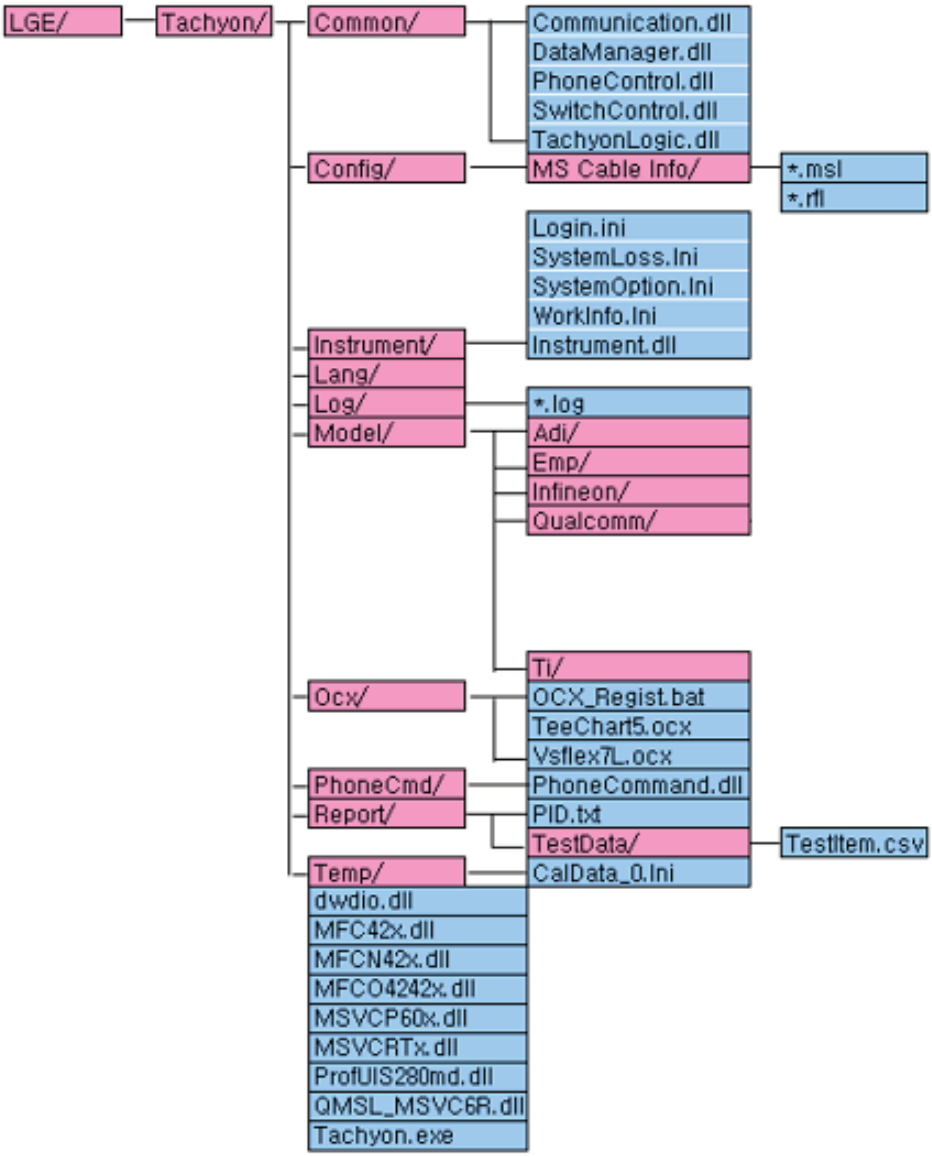
12. AUTO CALIBRATION

12.1 Overview

Auto-cal (Auto Calibration) is the PC side Calibration tool that perform Tx, Rx and Battery Calibration with Agilent 8960(GSM call setting instrument) and Tektronix PS2521G (Programmable Power supply).
Auto-cal generates calibration data by communicating with phone and measuring equipment then write it into calibration data block of flash memory in GSM phone.

12.2 Directory structure of Tachyon

"C₩LGE₩Tachyon"



12.3 Description of Folder & File.

12.3.1 Folder Explain

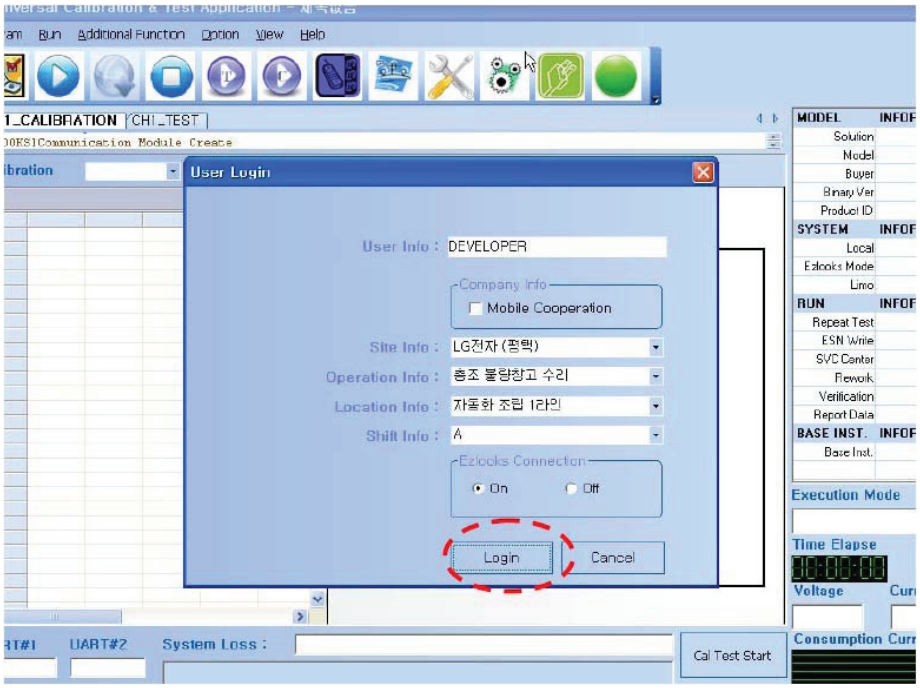
-. Tachyon : exist tachyon execute file, dll for MFC, dll for UI
-. Common : common files(XML Data I/O , Auto Test Logic, Tachyon Logic Control), dll for communication with system.
-. Config : *.ini configuration files for port setting and cable loss.
-. Model : configuration files for each model.
-. OCX : component files for Tachyon.
-. PhoneCmd : files for communication with phone.
-. Report : test result files.
-. Temp : store calibration value.

12.3.2 File Explain

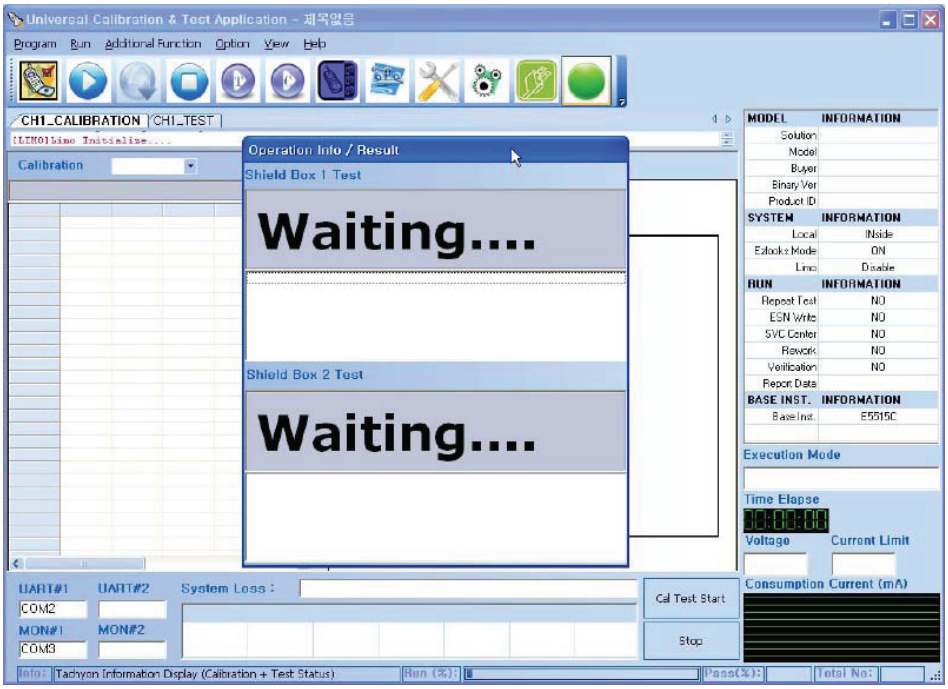
-. Model_Calibration.xml : stored data for calibration.
-. Model_CallSetuo.xml : stored equipment setting data for auto test.
-. Model_NV.ini : default NV data.
-. Model_Sequence.xml : stored calibration and auto test procedure.

12.4 Procedure

1. Execute "/LGE/Tachyon/Tachyon.Exe" and Click Login button.



2. Tachyon execute ready display



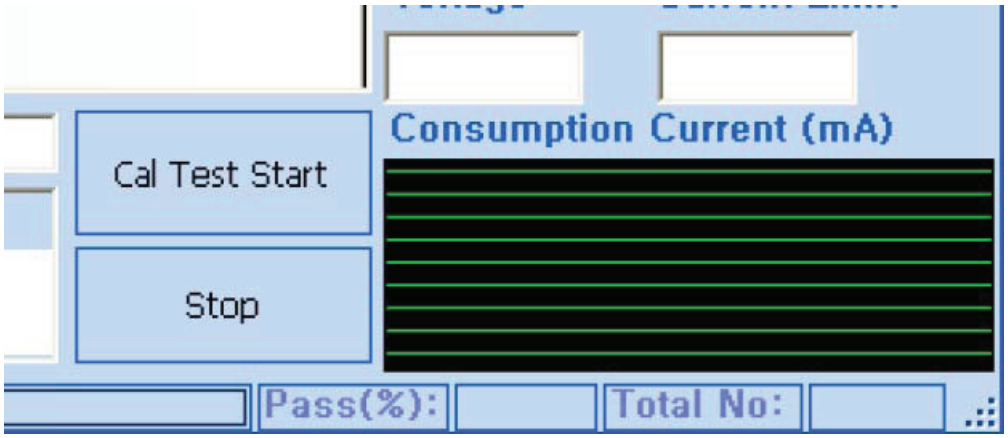
12.5 Tachyon Main UI

12.5. 1 Tool bar

1. Model Selection
2. Calibration + Test
3. Not Support
4. Stop
5. Test Only
6. Calibration Only
7. Phone Control
8. Loss Adjustment
9. System Option
10. Run Option
11. Voltage / Current Setting
12. Show Result

12.5.2 Command button

Only support Calibration Test and Stop button.



12.6 AGC

This procedure is for Rx calibration.
In this procedure, We can get RSSI correction value. Set band EGSM and press Start button the result window will show correction values per every power level and gain code and the same measure is performed per every frequency.

12.7 APC

This procedure is for Tx calibration.
In this procedure you can get proper scale factor value and measured power level.

12.8 ADC

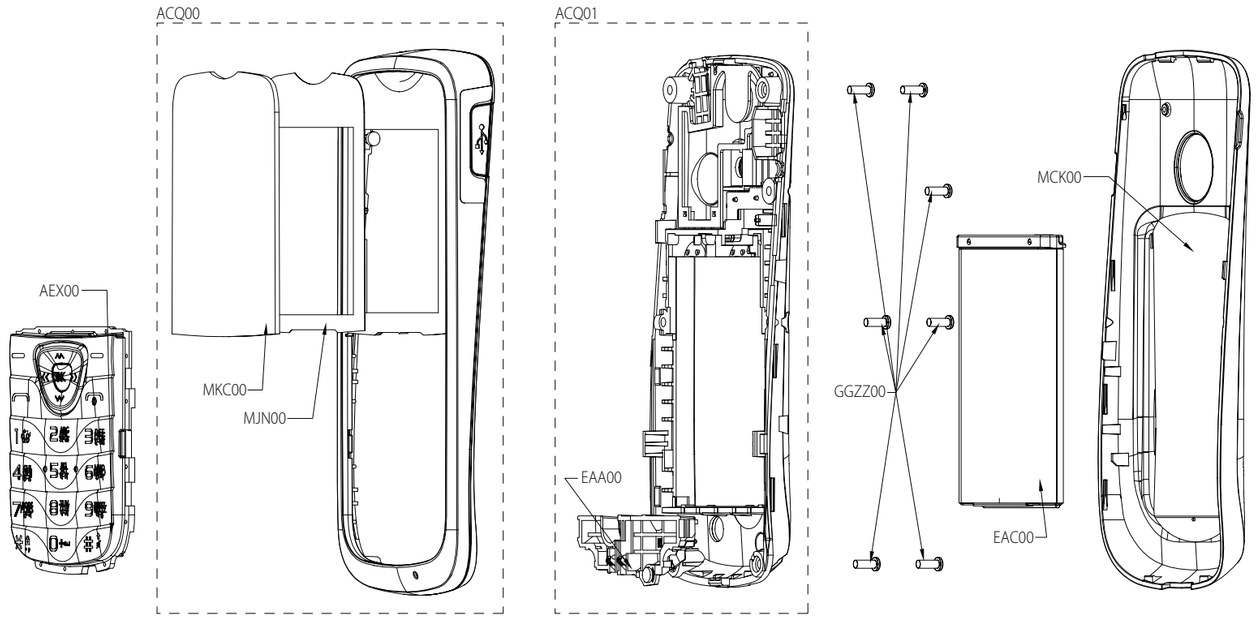
This procedure is for battery calibration.
You can get main Battery Config Table and temperature Config Table will be reset.

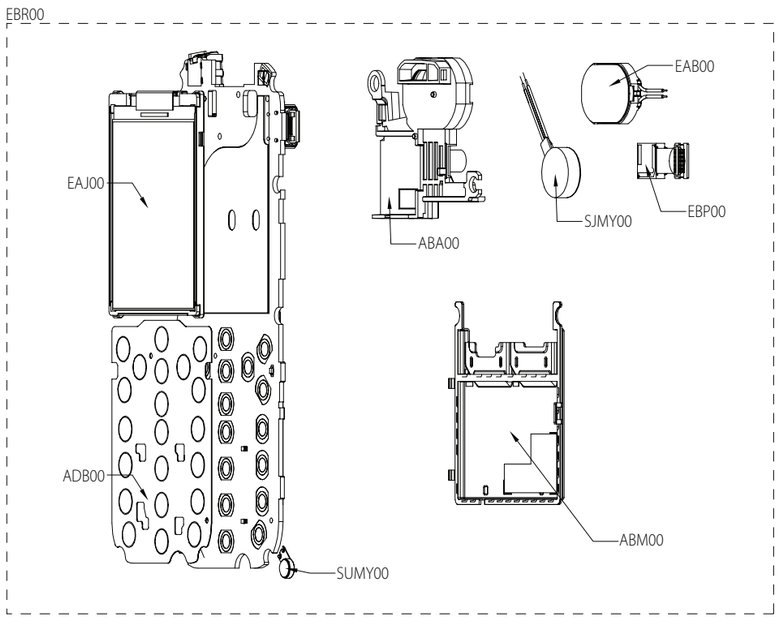
12.9 Target Power

BAND	Description	Low	Middle	High
GSM 850	Channel	128	191	251
	Frequency	824.2 MHz	836.8 MHz	848.8 MHz
	Max power	32.5 dBm	32.5 dBm	32.5 dBm
EGSM 900	Channel	975	37	124
	Frequency	880.2 MHz	897.4 MHz	914.8 MHz
	Max power	32.5 dBm	32.5 dBm	32.5 dBm
DCS1800	Channel	512	699	885
	Frequency	1710.2 MHz	1747.6 MHz	1784.8 MHz
	Max power	29.5 dBm	29.5 dBm	29.5 dBm
PCS 1900	Channel	512	661	810
	Frequency	1850.2 MHz	1880 MHz	1909.8 MHz
	Max power	29.5 dBm	29.5 dBm	29.5 dBm

12. EXPLODED VIEW & REPLACEMENT PART LIST

12.1 EXPLODED VIEW





Location	Description
GGZZ00	Screw,Tapping
ACQ00	Cover Assembly,Front
MJN00	Tape,Window
MKC00	Window,LCD
ACQ01	Cover Assembly,Rear
EAA00	PIFA Antenna,Multiple
EBR00	PCB Assembly,Main
ABA00	Bracket Assembly
ABM00	Can Assembly,Shield
SUMY00	Microphone,Condenser
SJMY00	Motor,DC
ADB00	Dome Assembly,Metal
EAB00	Speaker,Dual Mode
EAJ00	LCD,Module-TFT
EBP00	Camera Module
AEX00	Keypad Assembly,Main
MCK00	Cover,Battery
EAC00	Rechargeable Battery,Lithium Ion

12.2 Replacement Parts <Mechanic component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	PartNumber	Spec	Remark
1	AGQ000000	Phone Assembly	AGQ86511301	LGA230.AINDKG KG:BLACK GRAY -	
2	MEZ002100	Label, Approval	MLAA0062303	COMPLEX KB770 DEUBK ZZ:Without Color -	
2	ACQ100400	Cover Assembly, EMS	ACQ85370001	LGA230.AINDZY ZY:Color Unfixed -	
3	GGZZ00	Screw, Tapping	GGZZ0004901	GGZZ0004901 BH + - 1.6mM 4mM SWCH FZB SERVEONE CO., LTD.	
3	ACQ00	Cover Assembly, Front	ACQ85458601	LGA230.AINDZY BK:Black -	
4	MBL00	Cap, Multimedia Card	MBL64899101	MOLD TPU LGA230.AINDZY BK:Black -	
4	MBL01	Cap, Receptacle	MBL64899201	MOLD TPU LGA230.AINDZY BK:Black -	
4	MCK032701	Cover, Front	MCK66669201	MOLD PC LEXAN141R LGA230.AINDZY BK:Black -	
4	MCQ043301	Damper, LCD	MCQ66589201	COMPLEX LGA230.AINDZY ZZ:Without Color -	
4	MDJ000001	Filter	MDJ63105801	COMPLEX LGA230.AINDZY ZZ:Without Color -	
4	MDJ000002	Filter	MDJ63105901	COMPLEX LGA230.AINDZY ZZ:Without Color -	
4	MJN00	Tape, Window	MJN67751601	COMPLEX LGA230.AINDZY ZZ:Without Color -	
4	MKC00	Window, LCD	MKC63980201	CUTTING PMMA LGA230.AINDZY BK:Black -	
3	ACQ01	Cover Assembly, Rear	ACQ85459601	LGA230.AINDZY BK:Black -	
4	EAA00	PIFA Antenna, RF	EAA62524501	KI-B01630 SINGLE -2DB 5 Metal Stamping Type - KOMATECH CO., LTD	
4	EAA00	PIFA Antenna, Multiple	EAA62524601	LS01-I-10030-A0 QUAD -2DB 5 Metal Stamping Type - LS Mtron Ltd.	
4	MEZ000900	Label, After Service	MLAB0001102	COMPLEX C2000 CGRSV WA:White C2000 USASV DIA 4.0 PRINTING,	
4	MCK063301	Cover, Rear	MCK66669301	MOLD PC LEXAN141R LGA230.AINDZY BK:Black -	

Level	Location No.	Description	PartNumber	Spec	Remark
4	MCQ009401	Damper, Camera	MCQ66589001	COMPLEX LGA230.AINDZY ZZ:Without Color -	
4	MCQ015701	Damper, Connector	MCQ66589101	COMPLEX LGA230.AINDZY ZZ:Without Color -	
4	MCQ049801	Damper, Motor	MCQ66589601	COMPLEX LGA230.AINDZY ZZ:Without Color pad motor	
4	MCQ000001	Damper	MCQ66589701	COMPLEX LGA230.AINDZY ZZ:Without Color pad rear bracket	
4	MJN089301	Tape, Window	MJN67752001	COMPLEX LGA230.AINDZY ZZ:Without Color tape cam window	
4	MKC009401	Window, Camera	MKC63980101	COMPLEX LGA230.AINDZY ZZ:Without Color cam window	
3	EBR00	PCB Assembly, Main	EBR72889501	LGA230.AINDZY 1.0 MAIN	
4	EBR071500	PCB Assembly, Main, Insert	EBR73886701	LGA230.AINDKG 1.0 Main	
5	ABA00	Bracket Assembly	ABA73929201	LGA230.AINDZY ZZ:Without Color -	
6	MAZ000000	Bracket	MAZ63106501	MOLD PC LEXAN141R LGA230.AINDZY ZZ:Without Color SPK BRACKET	
6	MCQ074200	Damper, Speaker	MCQ66589501	COMPLEX LGA230.AINDZY ZZ:Without Color pad speaker	
6	MJN009400	Tape, Camera	MJN67751501	COMPLEX LGA230.AINDZY ZZ:Without Color -	
6	MJN000000	Tape	MJN67751901	COMPLEX LGA230.AINDZY ZZ:Without Color tape motor	
5	ABM00	Can Assembly, Shield	ABM73616501	LGA230.AINDZY ZY:Color Unfixed -	
6	MBK070300	Can, Shield	MBK62913801	PRESS SUS 304 0.3 LGA230.AINDZY ZZ:Without Color -	
6	MKU101700	Absorber, Electromagnetic Wave	MKU30343601	COMPLEX LGA230.AINDKG ZZ:Without Color Absorber	
5	RAA050100	Resin, PC	BRAH0001301	UF-1060	
5	SUMY00	Microphone, Condenser	SUMY0003815	B4010AL443-49 -44DB 2.2KOHM OMNI 1.1TO10V 4x1.0t FPCB GoerTek Inc.	
5	SJMY00	Motor, DC	SJMY0007109	WHVM-1030B15 WHVM-1030B15, 3 V, 80 mA, 10*3.0, 17mm WOOSUNG G&T CO., LTD	

Level	Location No.	Description	PartNumber	Spec	Remark
5	ADB00	Dome Assembly, Metal	ADB73618601	LGA230.AINDZY ZZ:Without Color -	
5	EAB00	Speaker, Dual Mode	EAB62308201	Nd-Fe-B 700mW 8OHM 91DB 720HZ 1812*3.0T wire 15mm DCCA coil WIRE	
5	EAJ00	LCD, Module-TFT	EAJ61757101	LM177BN1A QQVGA 1.77INCH 160X128 250CD COLOR 60% None 400 60Hz Inverter N - TOVIS	
5	EBP00	Camera Module	EBP61322001	CW1334-ABDBS CW1334-ABDBS 1.3M hynix 1/6 COWELL ELECTRONICS CO., LTD	
5	MDS000000	Gasket	MDS63632801	COMPLEX LGA230.AINDZY ZZ:Without Color -	
5	MEV000000	Insulator	MEV63773601	COMPLEX LGA230.AINDZY ZZ:Without Color INSULATOR LCD FPCB	
4	EBR071800	PCB Assembly, Main, SMT	EBR72889701	LGA230.AINDZY 1.0 MAIN	
5	EBR071600	PCB Assembly, Main, SMT Bottom	EBR72889801	LGA230.AINDZY 1.1 MAIN	
5	MEZ000000	Label	MLAZ0038301	COMPLEX LG-VX6000 ZZ:Without Color PID Label 4 Array PRINTING,	
5	EBR071700	PCB Assembly, Main, SMT Top	EBR72889901	LGA230.AINDZY 1.0 MAIN	
6	EAX010000	PCB, Main	EAX64026401	EAX64026401 LGA230.AINDZY 1.0 FR-4 SBL 6 10 Main LG Innotek.com	
3	AEX00	Keypad Assembly, Main	AEX73698101	LGA230.AINDZY BK:Black -	
1	AGF000000	Package Assembly	AGF76209001	LGA230.AINDKG ZZ:Without Color LG-A230 IND(TR1-1H/IND UB/Seal2/MRP Label/6WD/500ea)	
2	MAY084000	Box, Unit	MAY65172802	BOX Paper 160 59 120 5 COLOR LGA230.AINDKG ZZ:Without Color LG-A230 IND(EU1/English)	
2	APLY00	PALLET ASSY	APLY0003209	KS360 ZAFBK BK, ZZ, TDR TR1-1 Pallet Sleeve/6WD Pallet	
3	MPBZ00	Damper	MPBZ0219601	COMPLEX KM500 ROMBB ZZ:Without Color -	
3	MPCY00	Pallet	MPCY0019330	COMPLEX KS360 ZAFBK ZZ:Without Color -	
2	MBAD00	Bag, Vinyl	MBAD0005204	COMPLEX LG-LX260 SPRAG ZZ:Without Color -	
2	MBEE00	Box, Master	MBEE0059801	COMPLEX KS360 ACNRD ZZ:Without Color -	

Level	Location No.	Description	PartNumber	Spec	Remark
2	MLAJ00	Label, Master Box	MLAJ0004402	PRINTING CG300 CGR DG ZZ:Without Color LABEL MASTER BOX(for CGR TDR 2VER. mbox_label) GSM standard_master box label	
2	MLAP	Label, Unit	MLAP0001138	PRINTING LG-RD6100 RLC ZZ:Without Color GSM standard_Seal label	
2	MLAQ	Label, Unit Box	MLAQ0015213	PRINTING KG270 INDBK ZZ:Without Color GSM MRP LABEL-Made by LGE(100*48) IND MRP_unit box label	
2	MLAZ00	Label	MLAZ0050901	COMPLEX KU990 GBRBK ZZ:Without Color -	
1	AAD000000	Addition Assembly	AAD85818901	LGA230.AINDKG KG:BLACK GRAY -	
2	MCK00	Cover, Battery	MCK66669401	MOLD PC LEXAN141R LGA230.AINDZY BK:Black -	

12.2 Replacement Parts <Main component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	PartNumber	Spec	Remark
6	C255	Capacitor, Ceramic, Chip	ECCH0000195	GRM1555C1H3R9C 3.9pF 0.25PF 50V NP0 - 55TO+125C 1005 R/TP - MURATA MANUFACTURING CO., LTD.	
6	L510, L511	Inductor, Multilayer, Chip	ELCH0001408	LL1005-FHL6N8J 6.8NH 5% - 300mA 0.23OHM 5.6GHZ 9 SHIELD NONE 1.0X0.5X0.5MM R/TP TOKO, INC.	
6	R201, R219	Resistor, Chip	ERHZ0000407	MCR01MZP5J105 1MOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C109, C115, C116, C126, C132, C200, C201, C202, C203, C240, C317, C318, C319, C320, C322, C323, C331, C412, C413	Capacitor, Ceramic, Chip	ECCH0004904	GRM155R60J105K 1uF 10% 6.3V X5R -55TO+85C 1005 R/TP - MURATA MANUFACTURING CO., LTD.	

Level	Location No.	Description	PartNumber	Spec	Remark
6	C100, C103, C106, C117, C118, C123, C124, C125, C127, C129, C130, C131, C133, C134, C135, C149, C150, C207, C217, C218, C248, C304, C316	Capacitor, Ceramic, Chip	ECZH0003103	GRM36X7R104K10PT 100nF 10% 10V X7R - 55TO+125C 1005 R/TP - MURATA MANUFACTURING CO., LTD.	
6	C259, C418	Capacitor, Ceramic, Chip	ECCH0000112	MCH155C150J 15pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	R111, R112, R113, R118, R237, R239, R314, R315, R318, R332, R334, R406, R417	Resistor, Chip	ERHZ0000406	MCR01MZP5J104 100KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C407	Capacitor, Ceramic, Chip	ECZH0000803	C1005C0G1H020CT000F 2pF 0.25PF 50V NP0 - 55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	R222, R230, R231, R331	Resistor, Chip	ERHY0003301	MCR01MZP5J101 100OHM 5% 1/16W 1005 R/TP - ROHM.	
6	C518	Capacitor, Ceramic, Chip	ECCH0001001	C1005C0G1H6R8CT000F 6.8pF 0.5PF 50V NP0 - 55TO+125C 1005 R/TP - TDK KOREA COOPERATION	

Level	Location No.	Description	PartNumber	Spec	Remark
6	C112, C128	Capacitor, Ceramic, Chip	ECCH0000151	CL05B472KB5NNNC 4.7nF 10% 25V X7R -55TO+125C 1005 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	C147, C148, C250, C260, C301, C303, C313, C315	Capacitor, Ceramic, Chip	ECCH0000115	MCH155A220JK 22pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C140, C141, C204, C330, C410, C411, C414, C416, C506, C508, C514	Capacitor, Ceramic, Chip	ECCH0000143	MCH155CN102KK 1nF 10% 50V X7R -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C242, C244, C245, C247, C251, C252, C507	Capacitor, Ceramic, Chip	ECCH0000120	MCH155A390J 39pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C209, C249	Capacitor, Ceramic, Chip	ECZH0003503	GRM188R61E105K 1uF 10% 25V X5R -55TO+85C 1608 R/TP - MURATA MANUFACTURING CO., LTD.	
6	R117, R333, R414	Resistor, Chip	ERHY0000241	MCR01MZP5J102 1KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	L200, L201, L202, L403	Inductor, Multilayer, Chip	ELCH0001430	LL1005-FHLR10J 100NH 5% - 150mA 2.2OHM 1.03GHZ 10 SHIELD NONE 1.0X0.5X0.5MM R/TP TOKO, INC.	
6	C104, C105, C415, C419, C420	Capacitor, Ceramic, Chip	ECZH0001217	GRM155R60J474K 470nF 10% 6.3V X5R -25TO+70C 1005 BK-DUP - MURATA MANUFACTURING CO., LTD.	
6	U100	IC, MCP, NAND	EUSY0425901	H8BCS0QG0MMR-46M NAND/1G SDRAM/512M 0VTO0V 8.0x9.0x1.0 TR 130P NAND+DRAM BGA - HYNIX SEMICONDUCTOR INC.	

Level	Location No.	Description	PartNumber	Spec	Remark
6	C101, C102, C221, C222, C224, C230, C233	Capacitor, Ceramic, Chip	ECCH0005603	GRM188R61A225K 2.2uF 10% 10V X5R -55TO+85C 1608 R/TP - MURATA MANUFACTURING CO., LTD.	
6	SW500	Connector, RF	ENWY0007601	NMS-306 NMS-306, SMD, dB NAMAE ELECTRONICS INC	
6	C138, C139, C142, C143, C225, C226	Capacitor, Ceramic, Chip	ECCH0000122	MCH155A470JK 47pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	R244, R245	Resistor, Chip	ERHZ0000434	MCR01MZP5J1R0 1OHM 5% 1/16W 1005 R/TP - ROHM.	
6	FL303, FL304, FL305	Filter, EMI/Power	SFEY0013201	EVRC14S03Q030100R ESD/EMI 0HZ 15pF 0H SMD R/TP AMOTECH CO., LTD.	
6	C119, C205, C210, C211, C212, C213, C215, C219, C220, C223, C321, C329, C332	Capacitor, Ceramic, Chip	ECZH0001215	C1005X5R1A105KT000F 1uF 10% 10V X5R -55TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	R114, R115, R208, R229, R232	Resistor, Chip	ERHZ0000443	MCR01MZP5J222 2.2KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	ZD200, ZD201, ZD302, ZD303, ZD304, ZD305, ZD306, ZD307, ZD400	Diode, TVS	EDTY0010101	ESD9B5.0ST5G ESD9B5.0ST5G, SOD-923, 5 V, 300 mW, R/TP, 15pF SCG HONG KONG SAR LTD.	

Level	Location No.	Description	PartNumber	Spec	Remark
6	C122, C206, C246, C520	Capacitor, Ceramic, Chip	ECCH0007803	CL10A106MP8NNNC 10uF 20% 10V X5R -55TO+85C 1608 R/TP 0.8MM SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	R211, R212, R246, R247	Resistor, Chip	ERHZ0000435	MCR01MZP5J200 20OHM 5% 1/16W 1005 R/TP - ROHM.	
6	U101	IC, Digital Baseband Processor, GSM	EUSY0429401	PMB8815 , 281, EDGE Rx, ARM11 208MHz, NAND booting, 2.0Mp, FMR, IC, Digital Baseband Processor BGA R/TP 281P INFINEON TECHNOLOGIES (ASIA PACIFIC) PTE LTD.	
6	R223	Resistor, Chip	ERHY0000166	RC1005F394CS 390KOHM 1% 1/16W 1005 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	FB200, FB201, FB202, FB203, FB204	Filter, Bead	SFBH0008105	BLM15BD182SN1D 1800 ohm 1.0X0.5X0.5 25% 1.4 ohm 0.1A SMD R/TP 2P 0 MURATA MANUFACTURING CO., LTD.	
6	C107, C111, C146	Capacitor, Ceramic, Chip	ECZH0001216	C1005X5R1A224KT000E 220nF 10% 10V X5R - 55TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	R233	Resistor, Chip	ERHZ0000295	MCR01MZP5F5102 51KOHM 1% 1/16W 1005 R/TP - ROHM.	
6	U200	IC, Mini ABB	EAN62112401	RT8966AGQW RT8966A 1.65~5.5V 60uA SWITCH/MULTIPLEXER QFN R/TP 32P Mini ABB MUIC, Charger IC, Current Sink 4Ch, LDO 4Ch RICHTEK TECHNOLOGY CORP. QFN R/TP 32P RICHTEK TECHNOLOGY CORP.	
6	R103, R236	Resistor, Chip	ERHZ0000204	MCR01MZP5F1003 100KOHM 1% 1/16W 1005 R/TP - ROHM.	
6	R100, R217, R243	PCB ASSY, MAIN, PAD SHORT	SAFP0000401	LG-LU3000 LGTBK, MAIN, A,	
6	R319, R320, R321, R322, R323	Resistor, Chip	ERHY0000275	MCR01MZP5J563 56KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	L517	Inductor, Multilayer, Chip	ELCH0005003	HK1005 12NJ 12NH 5% - 300mA 0.4OHM 2.7GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO., LTD	
6	Q200	FET	EQFP0000101	2SJ347 P-CHANNEL MOSFET -20V -7 -0.05A 40OHM 100mW SSM R/TP 3P TOSHIBA	

Level	Location No.	Description	PartNumber	Spec	Remark
6	C108	Capacitor, Ceramic, Chip	ECCH0005604	GRM188R60J106M 10000000 pF, 6.3V, M, X5R, TC, 1608, R/TP, 0.8 mm MURATA MANUFACTURING CO., LTD.	
6	C261, C262, C263	Capacitor, TA, Conformal	ECTH0002002	F981A336MSA 33F 20% 10V 3.3A -55TO+85C 6OHM 2.2X1.1X1.1MM - SMD R/TP NICHICON CORPORATION, EAST JAPAN SALES OFFICE	
6	L514, L515	Inductor, Multilayer, Chip	ELCH0001031	HK1005 15NJ-T 15NH 5% - 300mA 0.46OHM 2.3GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO., LTD	
6	U500	Module, Tx Module	SMRH0007101	SKY77550 33DBM, 33DBM, 31DBM, 31DBM 30DB, 30DB, 28DB, 28DB 39%, 39%, 37%, 37% 50UA 1.46A, 970mA -33DB, -33DB -45DBM -1.3DBM 28P 6.0x6.0x1.0MM - SKYWORKS SOLUTIONS INC.	
6	L505, L506, L507	Inductor, Multilayer, Chip	ELCH0004721	1005GC2T2N2SLF 2.2NH 0.3NH - 300mA 0.16OHM 6GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	
6	R101, R301, R302, R303, R305, R306, R307, R308, R309, R310	Resistor, Chip	ERHZ0000484	MCR01MZP5J471 470OHM 5% 1/16W 1005 R/TP - ROHM.	
6	R235, R238, R248	Resistor, Chip	ERHZ0000206	MCR01MZP5F10R0 10OHM 1% 1/16W 1005 R/TP - ROHM.	
6	R102	Resistor, Chip	ERHZ0000475	MCR01MZP5J392 3.9KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	FL300, FL301, FL302	Filter, EMI/Power	SFEY0015501	ICVE10184E050R101FR ESD/EMI 550HZ 10F 0H SMD R/TP INNOCHIPS TECHNOLOGY	
6	VA200, VA201, VA203, VA204, VA301, VA304, VA308	Varistor	SEVY0003601	ICVL0505101V150FR 5.6V 0% 60F 1.0*0.5*0.55 NONE SMD R/TP INNOCHIPS TECHNOLOGY	
6	C113, C114	Capacitor, Ceramic, Chip	ECCH0002002	C1005X7R1A473KT000F 47000pF 10% 10V Y5P - 30TO+85C 1005 R/TP - TDK CORPORATION	

Level	Location No.	Description	PartNumber	Spec	Remark
6	C239, C337, C515	Capacitor, Ceramic, Chip	ECZH0000830	C1005C0G1H330JT000F 33pF 5% 50V NP0 -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	S300	Socket, Card	ENSY0023501	104042-001 Micro-SD 8P ANGLE SMD R/TP - HANKOOK MOLEX	
6	C264	Capacitor, Ceramic, Chip	ECCH0000187	GRM1555C1H151J 150pF 5% 50V NP0 -55TO+125C 1005 R/TP - MURATA MANUFACTURING CO., LTD.	
6	R107, R108, R300, R304, R336, R411, R412	Resistor, Chip	ERHZ0000485	MCR01MZP5J472 4.7KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C121	Capacitor, Ceramic, Chip	ECZH0025502	GRM219R60J226M 0.000022F 20% 6.3V X5R -55TO+85C 2012 R/TP 0.85MM MURATA MANUFACTURING CO., LTD.	
6	Q100, Q300	TR, Bipolar	EBK61572201	LSCR523EBFS8 NPN 5V 50V 50V 100mA 100NA 120~560 150mW EMT3 R/TP 3P ROHM Semiconductor KOREA CORPORATION	
6	L504	Inductor, Multilayer, Chip	ELCH0001039	HK1005 2N7S-T 2.7NH 0.3NH - 300mA 0.13OHM 6GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO., LTD	
6	R228, R501	Resistor, Chip	ERHZ0000404	MCR01MZP5J102 1KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C234	Capacitor, Ceramic, Chip	ECCH0000182	GRM155R61A104K 0.1uF 10% 10V X5R -55TO+85C 1005 R/TP - MURATA MANUFACTURING CO., LTD.	
6	L401, L402	Inductor, Multilayer, Chip	ELCH0005004	HK1005 22NJ 22NH 5% - 300mA 0.6OHM 1.9GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO., LTD	
6	U202	IC, Comparator	EUSY0250501	NCS2200SQ2T2G NCS2200SQ2T2G, SC70, 5 PIN, R/TP, Comparator, pin compatible to EUSY0077701 - - SC70 R/TP 5P - ON SEMICONDUCTOR	
6	C402, C403	Capacitor, Ceramic, Chip	ECCH0000110	MCH155A100D 10pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	L508	Inductor, Multilayer, Chip	ELCH0004707	1005GC2T1N5SLF 1.5NH 0.3NH - 300mA 0.13OHM 7GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP PILKOR ELECTRONICS LTD.	

Level	Location No.	Description	PartNumber	Spec	Remark
6	J300, J301	Card Socket	ENSY0024302	KP09NC-6S-2.54SF SIM 6P ANGLE SMD R/TP Stroke : 11.25mm HIROSE KOREA CO., LTD	
6	FL500	Filter, Saw, Dual	EAM62071301	B9836 GSM QUAD 1.8*1.4*0.4 SMD R/TP 10P EPCOS PTE LTD.	
6	FL400	Filter, Ceramic	SFCY0000901	LFB212G45SG8A166 BPF 2.45KHZ 100Hz SMD R/TP 4P MURATA MANUFACTURING CO., LTD.	
6	C513, C516	Capacitor, Ceramic, Chip	ECCH0000701	C1005C0G1H1R2CT000F 1.2pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP - TDK CORPORATION	
6	C254	Capacitor, Ceramic, Chip	ECZH0000839	C1005C0G1H4R7CT000F 4.7pF 0.25PF 50V NP0 -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	R240	Resistor, Chip	ERHZ0000402	MCR01MZP5J100 10OHM 5% 1/16W 1005 R/TP - ROHM.	
6	IC200	IC, Audio Sub System	EUSY0403901	WM9093ECS/R 1.71~5.5V 0W WLCSP R/TP 20P - WOLFSON MICROELECTRONICS PLC	
6	L509	Inductor, Multilayer, Chip	ELCH0001033	HK1005 1N5S-T 1.5NH 0.3NH - 300mA 0.1OHM 6GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO., LTD	
6	C511	Capacitor, Ceramic, Chip	ECZH0001002	C1005CH1H0R5BT000F 0.5pF 0.1PF 50V NP0 -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	C253	Capacitor, Ceramic, Chip	ECCH0007802	CL10A475KP8NNNC 4.7uF 10% 10V X5R -55TO+85C 1608 R/TP - SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	FB400	Filter, Bead	SFBH0000903	HB-1M1005-601JT 600 ohm 1.0*0.5*0.5 25% 0.6 ohm 0.3A SMD R/TP 2P 0 CERATECH CORPORATION	
6	C421, C523	Capacitor, Ceramic, Chip	ECZH0000813	C1005C0G1H101JT 100pF 5% 50V NP0 -55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	CN201	Connector, I/O	ENRY0008801	GU073-5P-SD-E1500 GU073-5P-SD-E1500, 5, mm, ANGLE LS Mtron Ltd.	
6	R335	PCB ASSY, MAIN, PAD OPEN	SAFO0000401	AX3100 ATL SV_SHIPBACK, MAIN, A, 0OHM DNI	
6	C241, C243	Capacitor, Ceramic, Chip	ECCH0000161	MCH153CN333KK 33nF 10% 16V X7R -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	X100	Crystal	EXXY0027001	DSX321G-26M(8PF) 26MHZ 10PPM 0F NONE SMD R/TP DAISHINKU CORPORATION.	

Level	Location No.	Description	PartNumber	Spec	Remark
6	R213	Resistor, Chip	ERHZ0000405	MCR01MZP5J103 10KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C110, C509	Capacitor, Ceramic, Chip	ECCH0000113	MCH155A180J 18pF 5% 50V NP0 -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C328, C400, C404	Capacitor, Ceramic, Chip	ECCH0000198	CL05A225MQ5NSNC 2.2uF 20% 6.3V X5R - 55TO+85C 1005 R/TP . SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	X101	Crystal	EXXY0018701	FC-135(12.5PF, +-20PPM) 32.768KHZ 20PPM 12.5PF 32*15 SMD R/TP SEIKO EPSON CORP	
6	U300	IC, Analog Switch	EUSY0317101	SLAS4717EPMTR2G - - - - WQFN R/TP 10P 1.8*1.4*0.75 ON SEMICONDUCTOR	
6	C522	Inductor, Multilayer, Chip	ELCH0003832	LQG15HS2N2S02D 2.2NH 0.3NH - 300mA - - 0.12OHM 6GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP MURATA MANUFACTURING CO., LTD.	
6	R405, R408	Resistor, Chip	ERHZ0000531	MCR01MZP5J271 270OHM 5% 1/16W 1005 R/TP - ROHM.	
6	R104	Resistor, Chip	ERHZ0000499	MCR01MZP5J562 5.6KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	Q400, Q401	TR, Bipolar	EBK61573301	2SC5086 NPN 3V 20V 12V 80mA 1UA 80~160 100mW 2-2H1B R/TP 3P TOSHIBA ELECTRONICS KOREA CORPORATION	
6	R404, R407	Resistor, Chip	ERHZ0000449	MCR01MZP5J243 24KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	C208	Capacitor, Ceramic, Chip	ECCH0000117	CL05C270JB5NNNC 27pF 5% 50V NP0 -55TO+125C 1005 R/TP 0.5 SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	L405, L406	Inductor, Multilayer, Chip	ELCH0010402	LK1005 R27K-T 270NH 10% - 25mA 0.91OHM 120MHZ 10 SHIELD NONE 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO., LTD	
6	U400	IC, Bluetooth	EUSY0418701	BCM2070B2KUBXG 2.3VTO5.5V 158.4mW 42P - WLBGA R/TP 42P BROADCOM ASIA DISTRIBUTION PTE LTD	
6	ANT400	Antenna, Helical	SNMF0059501	AMAN301512ST01 SINGLE -2DB 50OHM 3 AMOTECH CO., LTD.	
6	C517	Capacitor, Ceramic, Chip	ECZH0000802	C1005C0G1H010CT 1pF 0.25PF 50V NP0 - 55TO+125C 1005 R/TP - TDK KOREA COOPERATION	
6	R401, R402	Resistor, Chip	ERHZ0003801	MCR01MZP5J5R1 5.1OHM 5% 1/16W 1005 R/TP - ROHM.	

Level	Location No.	Description	PartNumber	Spec	Remark
6	R330	Resistor, Chip	ERHZ0000457	MCR01MZP5J300 30OHM 5% 1/16W 1005 R/TP - ROHM.	
6	C401, C405, C406	Capacitor, Ceramic, Chip	ECCH0000155	MCH153CN103KK 10nF 10% 16V X7R -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	VA205, VA206	Varistor	SEVY0005201	EVLC5S02050 5.5V 0% 50F 1.0*0.5*0.6 - SMD R/TP AMOTECH CO., LTD.	
6	CN300	Connector, BtoB	ENBY0034201	GB042-24S-H10-E3000 24P 0.40MM STRAIGHT SOCKET SMD R/TP 1M - LS Mtron Ltd.	
6	L512, L513	Inductor, Multilayer, Chip	ELCH0001040	HK1005 3N9S-T 3.9NH 0.3NH - 300mA 0.21OHM 4GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TAIYO YUDEN CO., LTD	
6	L100	Inductor, Wire Wound, chip	ELCP0009410	LQM2HPN3R3MG0 LQM2HPN3R3MG0, 3.3 uH, N, 2x2.5x1.0, R/TP, chip power MURATA MANUFACTURING CO., LTD.	
6	SC200	Can, Shield	MCBA0059201	COMPLEX GD350 CLP ZZ:Without Color -	
6	J200	Jack, Phone	ENJE0008001	JAM3333-F32-7F 1P 4P ANGLE R/TP 4mM BLACK 6P - HON HAI PRECISION INDUSTRY CO., LTD.	
6	VA207, VA208	Varistor	SEVY0005101	ICVL0518050FR 18V 0% 5F 1.0*0.5*0.55 NONE SMD R/TP INNOCHIPS TECHNOLOGY	
6	CN202	Connector, Terminal Block	EAG62832501	KQ03LV2-3R 3P 3.00MM ANGLE SMD T/REEL - HIROSE KOREA CO., LTD	
6	FB206, FB207	Filter, Bead	SFBH0008101	BLM15AG601SN1D 600 ohm 1.0X0.5X0.5 25% 0.6 ohm 0.3A SMD R/TP 2P 0 MURATA MANUFACTURING CO., LTD.	
6	C120	Capacitor, Ceramic, Chip	ECZH0001210	C1005Y5V1A474ZT000F 470nF -20TO+80% 10V Y5V -30TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	FB100	Filter, Bead	SFBH0007103	BLM15BB750SN1D 75 ohm 1.0X0.5X0.5 25% 0.4 ohm 0.3A SMD R/TP 2P 0 MURATA MANUFACTURING CO., LTD.	
6	L404	Inductor, Multilayer, Chip	ELCH0001412	LL1005-FHL1N8S 1.8NH 0.3NH - 400mA 0.14OHM 15GHZ 8 SHIELD NONE 1.0X0.5X0.5MM R/TP TOKO, INC.	
6	R400	Resistor, Chip	ERHY0000128	MCR01MZP5F1502 15KOHM 1% 1/16W 1005 R/TP - ROHM.	

Level	Location No.	Description	PartNumber	Spec	Remark
6	LD300, LD301, LD302, LD303, LD304, LD305	LED, Chip	EDLH0015101	19-217/BHC-ZM1N2QY/3T BLUE 2.7~3.2 25mA 18~45mcd 465~475nm 95mW 1608 R/TP 2P - EVERLIGHT ELECTRONICS CO., LTD.	
6	C401, C405, C406	Capacitor, Ceramic, Chip	ECCH0000155	MCH153CN103KK 10nF 10% 16V X7R -55TO+125C 1005 R/TP - ROHM Semiconductor KOREA CORPORATION	
6	C119, C205, C210, C211, C212, C213, C215, C219, C220, C223, C321, C329, C332	Capacitor, Ceramic, Chip	ECZH0001215	C1005X5R1A105KT000F 1uF 10% 10V X5R - 55TO+85C 1005 R/TP - TDK KOREA COOPERATION	
6	C328, C400, C404	Capacitor, Ceramic, Chip	ECCH0000198	CL05A225MQ5NSNC 2.2uF 20% 6.3V X5R - 55TO+85C 1005 R/TP . SAMSUNG ELECTRO-MECHANICS CO., LTD.	
6	R117, R333, R414	Resistor, Chip	ERHY0000241	MCR01MZP5J102 1KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	R324, R325, R326, R327, R328, R329	Resistor, Chip	ERHZ0000420	MCR01MZP5J151 150OHM 5% 1/16W 1005 R/TP - ROHM.	
6	VA200, VA201, VA203, VA204, VA301, VA304, VA308	Varistor	SEVY0003601	ICVL0505101V150FR 5.6V 0% 60F 1.0*0.5*0.55 NONE SMD R/TP INNOCHIPS TECHNOLOGY	
6	C231, C235	Capacitor, Ceramic, Chip	ECCH0000179	GRM155R71C223K 22nF 10% 16V X7R -55TO+85C 1005 R/TP - MURATA MANUFACTURING CO., LTD.	

Level	Location No.	Description	PartNumber	Spec	Remark
6	FB200, FB201, FB202, FB203, FB204	Filter, Bead	SFBH0008105	BLM15BD182SN1D 1800 ohm 1.0X0.5X0.5 25% 1.4 ohm 0.1A SMD R/TP 2P 0 MURATA MANUFACTURING CO., LTD.	
6	R214	Resistor, Chip	ERHZ0000529	MCR01MZP5J152 1.5KOHM 5% 1/16W 1005 R/TP - ROHM.	
6	R114, R115, R208, R229, R232	Resistor, Chip	ERHZ0000443	MCR01MZP5J222 2.2KOHM 5% 1/16W 1005 R/TP - ROHM.	

12.3 Accessory

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	PartNumber	Spec	Remark
2	AFN053800	Manual Assembly, Operation	AFN75475701	LGA230.AINDKG ZZ:Without Color LGA230 manual assy for IND	
3	MBM087200	Card, Warranty	MCDF0001111	COMPLEX KG270 INDBK ZZ:Without Color -	
3	MFL053800	Manual, Operation	MFL67213401	COMPLEX LGA230.AINDKG ZZ:Without Color LGA230 manual for IND	
2	EAB010200	Earphone, Stereo	SGEY0003744	EMB-LGE004MSKB 3mW 16OHM 115DB 85HZTO126HZ 1M BLACK 3.5 L TYPE STEREO 4POLE PLUG - CRESYN CO., LTD	
2	EAY060000	Adapters	SSAD0032601	STA-U34ID STA-U34ID, 100-240V, 5060 Hz, 5.1 V, 0.7 A, CE, AC-DC ADAPTOR DONG DO ELECTRONICS CO., LTD	
2	EAC00	Rechargeable Battery, Lithium Ion	EAC61578801	LGIP-531A-LI-EU PRISMATIC 3.7V 950AH 950mAH 5.5X34X50 5.7*34.15*53.55 BLACK INNERPACK - Tianjin Lishen Battery Joint-Stock Co., Ltd	