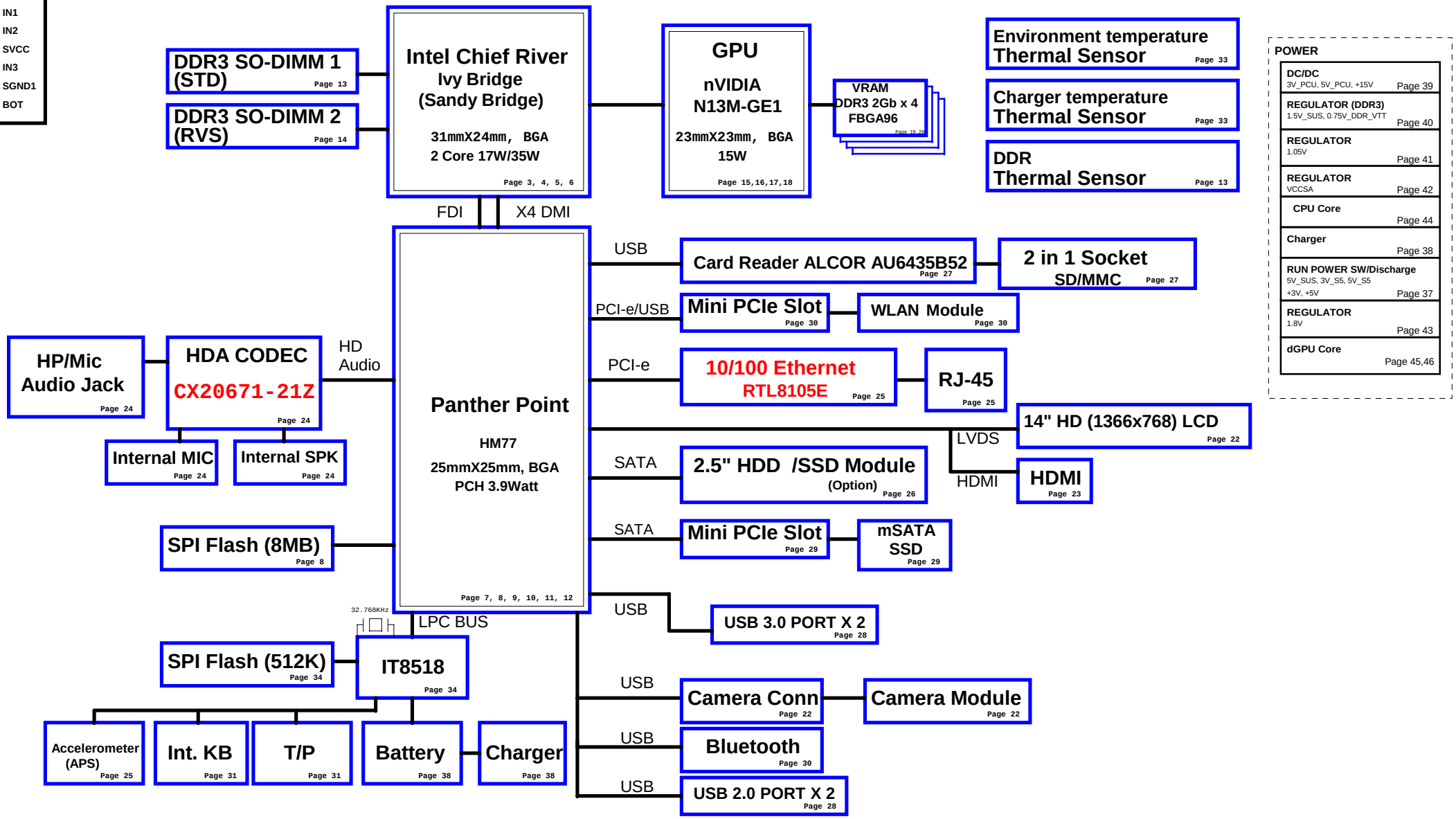
LZ8 14" Block Diagram -- Intel Chief River ULV

PCB STACK UP 8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT



POWER

DC/DC 3V_PCU, 5V_PCU, +15V	Page 39
REGULATOR (DDR3) 1.5V_SUS, 0.75V_DDR_VTT	Page 40
REGULATOR 1.05V	Page 41
REGULATOR VCCSA	Page 42
CPU Core	Page 44
Charger	Page 38
RUN POWER SW/Discharge 5V_SUS, 3V_S5, 5V_S5 +3V, +5V	Page 37
REGULATOR 1.8V	Page 43
dGPU Core	Page 45,46

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.
System Block Diagram
Size: Document Number: Rev 1A
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Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	22,36,38,39,40,41,42,44,45	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,34	RTC		S0~S5
3VPCU	+3.3V	7,8,22,23,25,30,31,34,35,36,37,38,39,43,45	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	22,36,37,39,40,41,42,43,44,45,46	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
15V	+15V	22,37,39,40,46	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	25,37	LAN POWER	LAN_ON	
5V_S5	+5V	11,24,28,32,37	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,30,35,37,45	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
1.5V_SUS	+1.5V	3,11,13,14,36,37,40,46	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	13,14,37,40	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,22,23,24,26,31,33,36,37,38	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,21,22,23,24,25,26,27 29,30,31,33,34,35,36,37,38,39 40,41,42,43,44,45,46	SLP_S3# CTRLD POWER	MAINON	S0
VCC_GFX		5,36,44	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	5,37,42	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,37,43	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,21,36,37,41,46	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
VCC_CORE		5,6,36,44	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	22	LCD Power	ENVDD	S0
+3V_HDD	+3V	26	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	26	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	38	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3,5,36	DDR3 1.5V Rails	PS_S3CNTRL	S0

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

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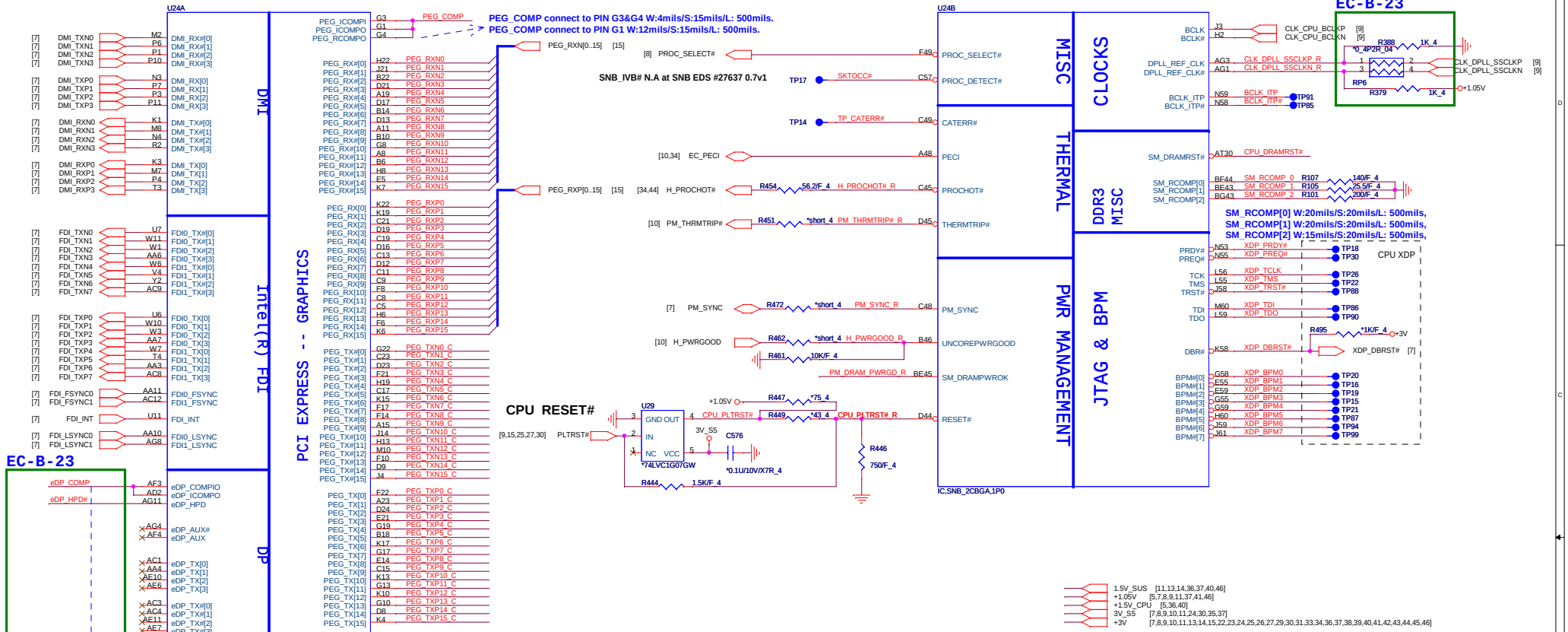
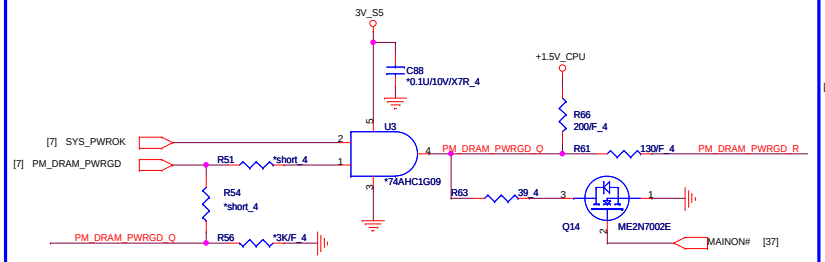
Ivy/Sandy Bridge Processor (DMI,PEG,FDI)

Ivy/Sandy Bridge Processor (CLK,MISC,JTAG)

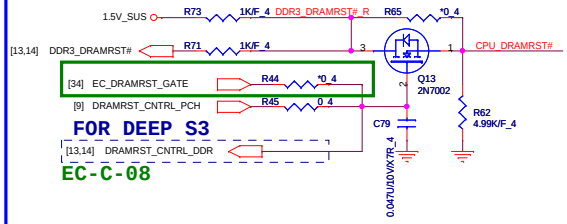
03



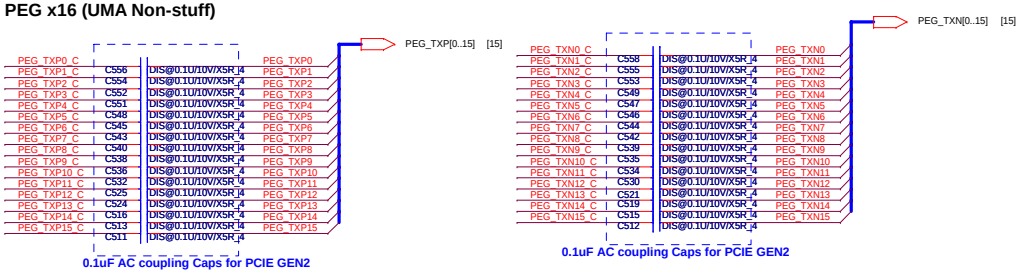
SM_DRAMPWROK Processor Input.



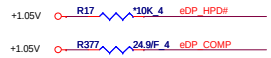
DDR3 DRAM RESET



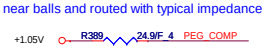
PEG x16 (UMA Non-stuff)



DP & PEG Compensation

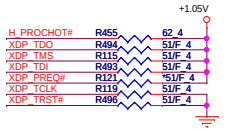


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

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	IVY 1/4 (PCIE&DMI&FDI)	3A
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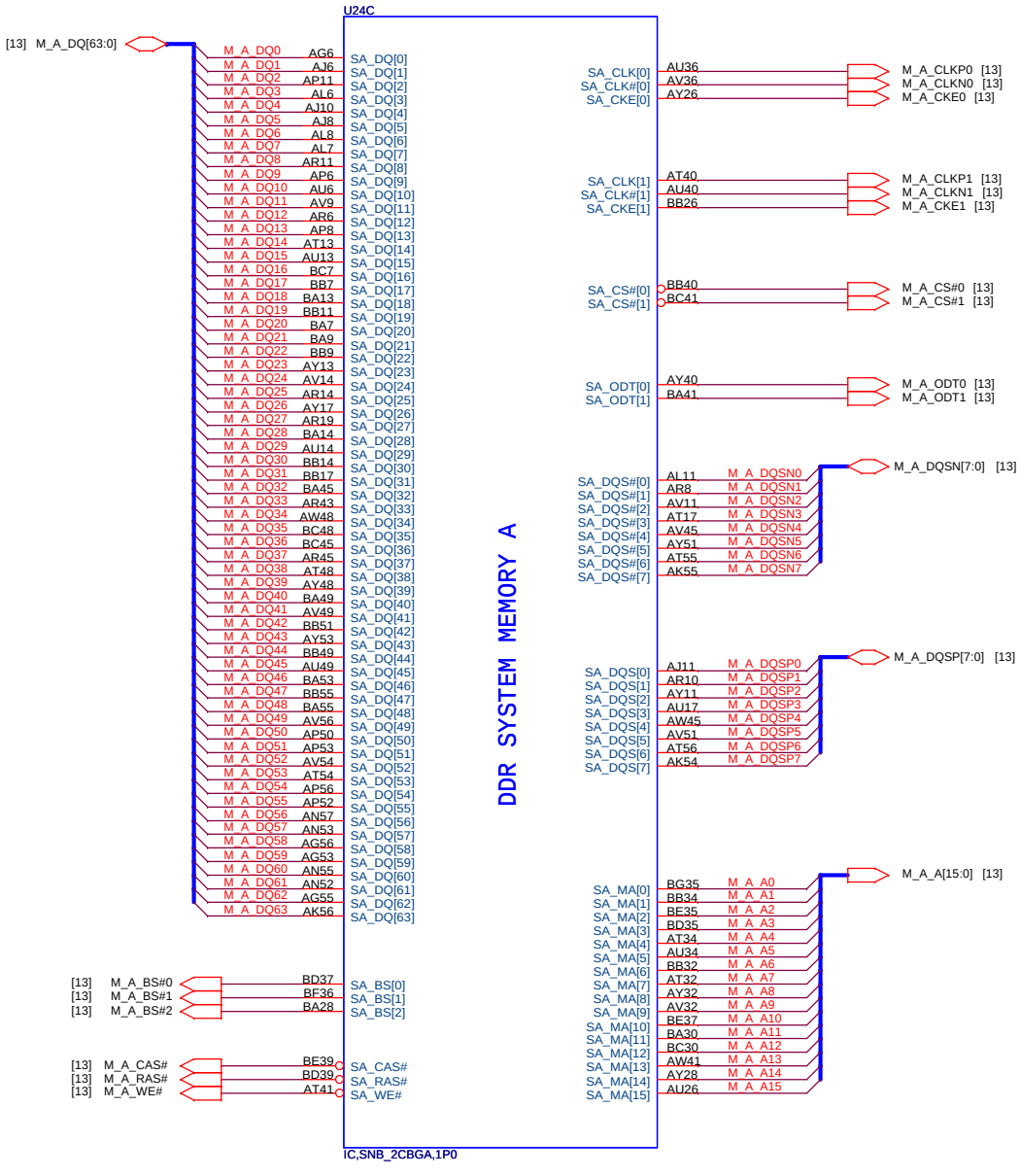
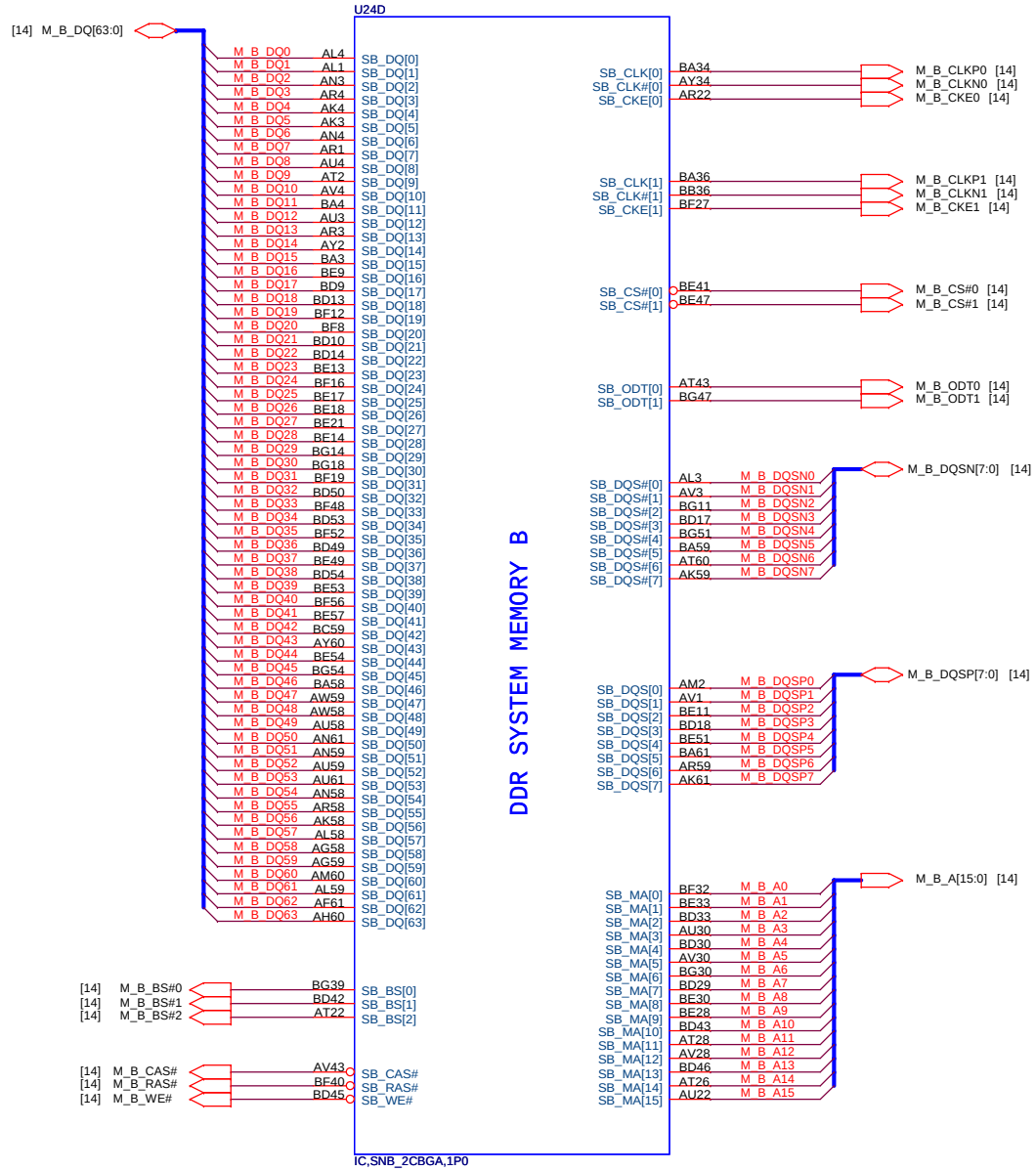
Ivy/Sandy Bridge Processor (DDR3)





PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	Custom IVY 2/4 (DDR3 I/F)	1A
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Ivy/Sandy Bridge Processor (POWER)

Ivy/Sandy Bridge Processor (GRAPHIC POWER)

05

330uF locate power side

CPU Core Power

IVY:33A

8.5A

33A

5A

U24F

U24G

IC,SNB_2CBGA,1P0

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

CORE SUPPLY

PEG AND DDR

POWER

GRAPHICS

DDR3 - 1.5V RAILS

QUIET RAILS

SVID

SENSE LINES

1.8V RAIL

SA RAIL

3.3V_SUS?(PDDG p127)

SNB->NC
IVB->GND

1.2A

SNB:6A

EC-B-19

SNB_IVB# N.A at SNB EDS #27637 0.7v1

If +1.5V_CPU will be implemented, have to change the two divided resistor as 100-ohm 1%

SVID CLK

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to VR

SVID DATA

Place PU resistor close to CPU

Place PU resistor close to VR

SVID ALERT

Place PU resistor close to CPU

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

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	SNB 3/4 (POWER)	1A
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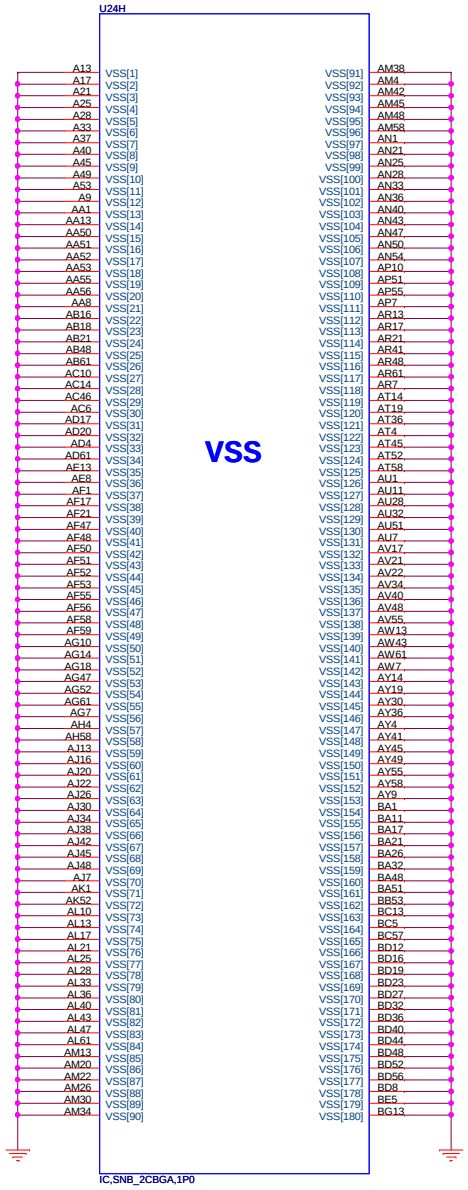
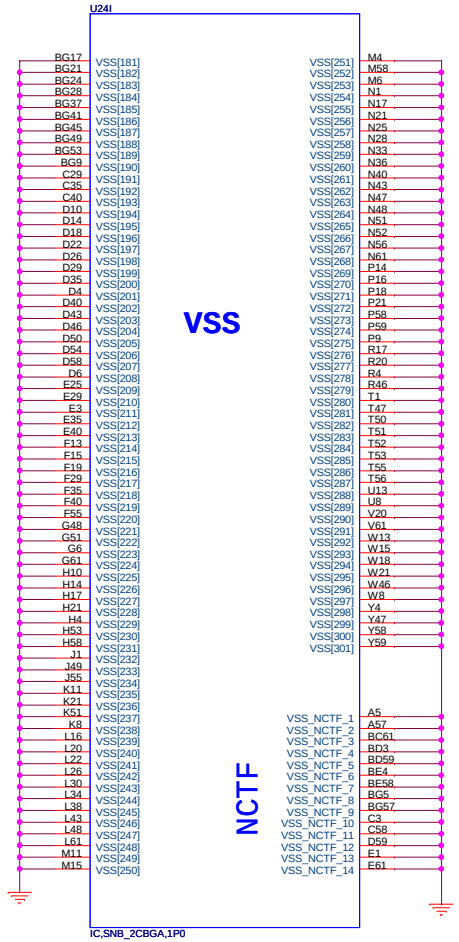
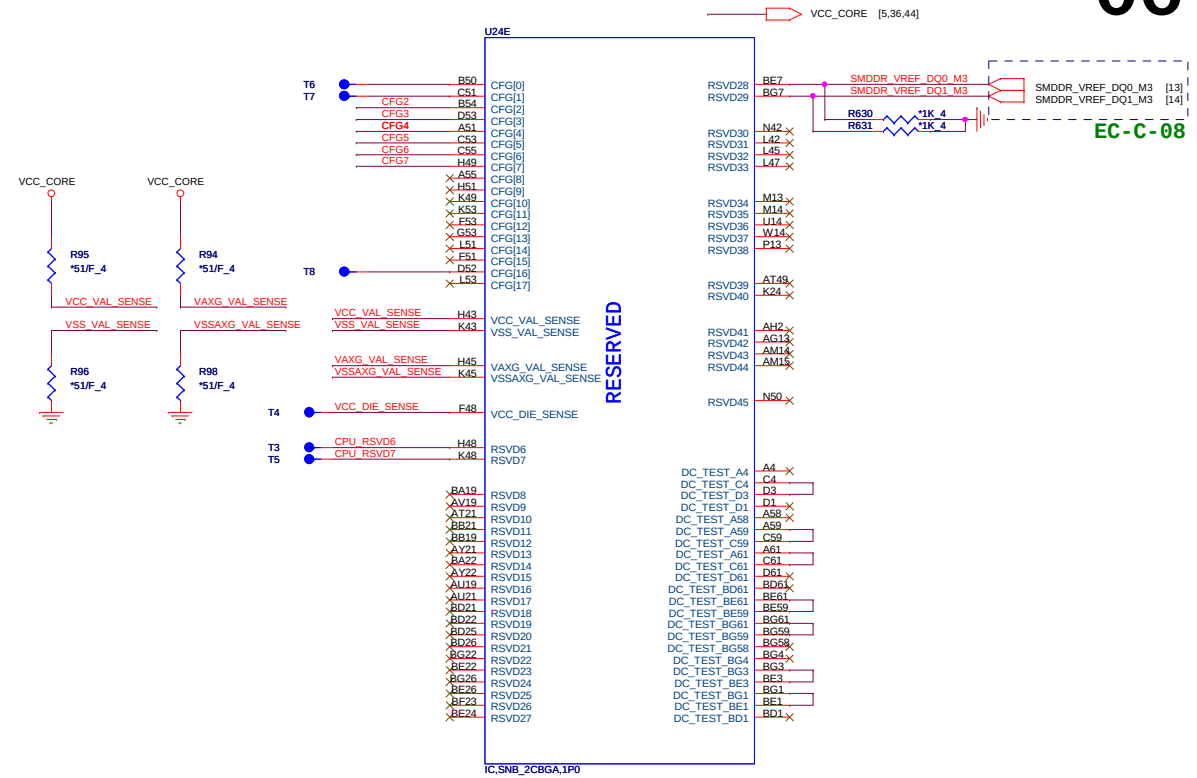
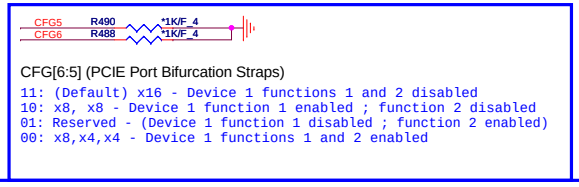
Sandy Bridge Processor (GND)





Sandy Bridge Processor (RESERVED, CFG)





Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

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	Custom SNB 4/4 (GND)	3A

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06

Panther/Cougar Point (DMI,FDI,PM)

Panther/Cougar Point (LVDS,DDI)

07

U32C

U32D

EC-B-23

EC-B-01

EC-B-02

EC-B-24

FOR DEEP S3

Layout note:
AC coupling capacitors of DP are placed on near connector

DMI

FDI

System Power Management

LVDS

CRT

Digital Display Interface

INT. HDMI

CougarPoint_R1P0

CougarPoint_R1P0

PCH Pull-high/low(CLG)

System PWR_OK(CLG)

INT HDMI DETECT

LVDS for HM76

DPWROK FOR DSW (DEEP S3)

On Die DSW VR Enable

High = Enable (Default)
Low = Disable

PROJECT LZ8 Chief River DIS		
Quanta Computer Inc.		
Size	Document Number: PCH 1/6 (DMI/FDI/VIDEO)	Rev: 2A
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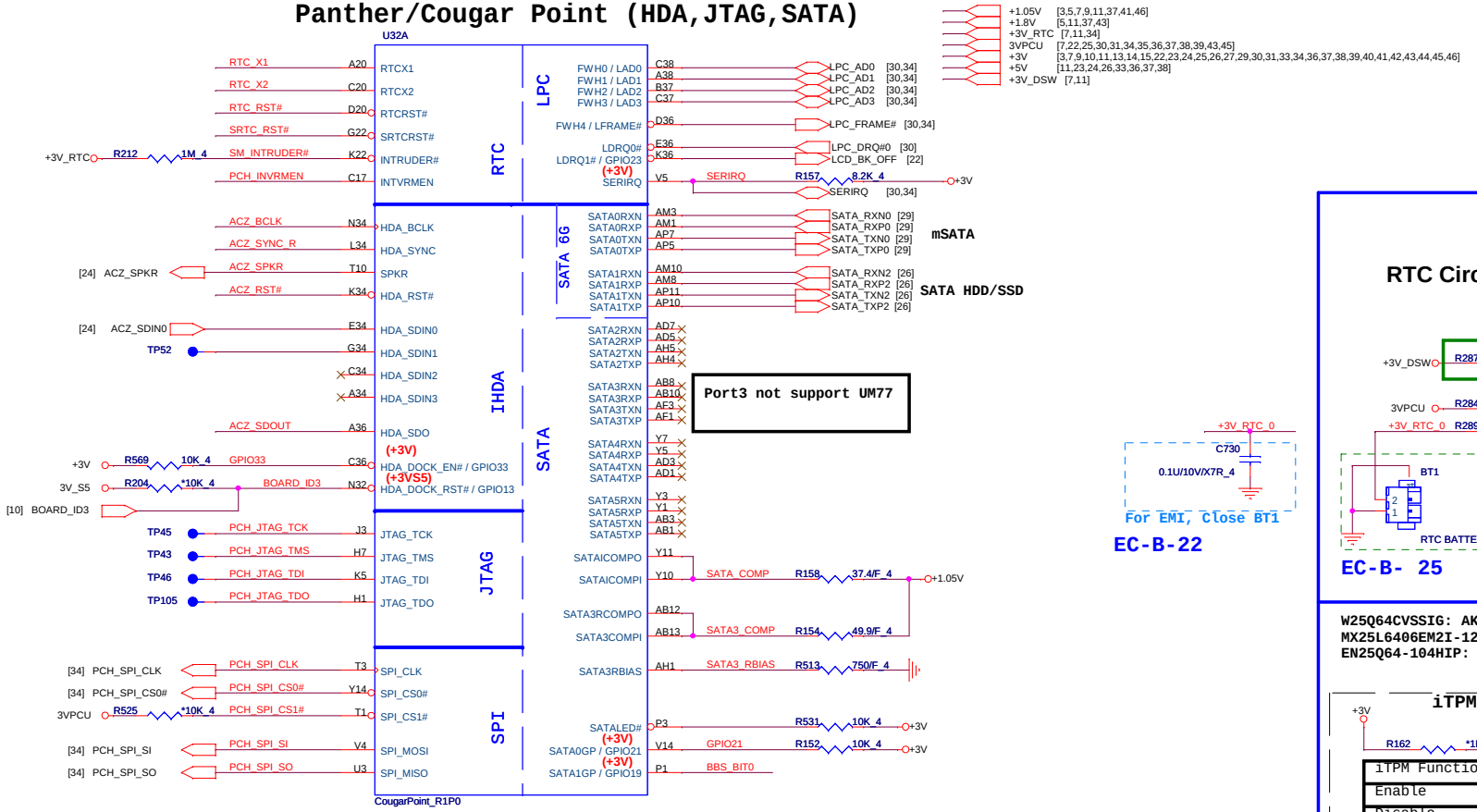
Panther/Cougar Point (HDA,JTAG,SATA)



+1.05V [3,5,7,9,11,37,41,46]
+1.8V [5,11,37,43]
+3V_RTC [7,11,34]
3VPCU [7,22,25,30,31,34,35,36,37,38,39,43,45]
+3V [3,7,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
+5V [11,23,24,26,33,36,37,38]
+3V_DSW [7,11]

+3V_RTC_0
C730
0.1U/10V/X7R_4

For EMI, Close BT1

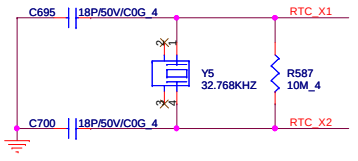
EC-B-22

if default boot destination is SPI,
no external pull-up/-down resistors on the board are necessary

PCH Strap Table

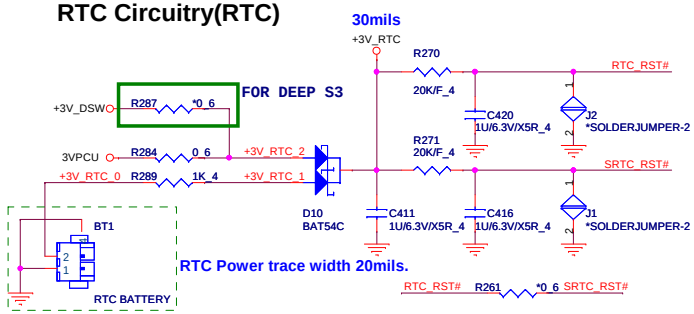
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R180 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R578 *1K_4 R561 *10K_4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R564 330K_4 +3V_RTC
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDOUT R567 *1K_4 3V_S5
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 1 SPI; 1 0 LPC	[Need external pull-down for LPC BIOS] R530 *1K_4 BBS_BIT0 R592 *1K_4 BBS_BIT1 [9]
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
DF_TVS	DMI Termination voltage	PWROK	weak pull-down 20kohm	R500 2.2K_4 +1.8V N.A at CPT EDS 0.7 [3] PROC_SELECT# R501 1K_4 DF_TVS [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R203 1K_4 ACZ_SYNC_R
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite		Low = Disable (Default) High = Enable	[10] HOST_ALERT#1_R HOST_ALERT#1_R R554 1K_4 3V_S5
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R195 *1K_4 PLL_ODVR_EN [10]
DSWVREN	0: disable 1: enable			

RTC Clock 32.768KHz



08

RTC Circuitry(RTC)



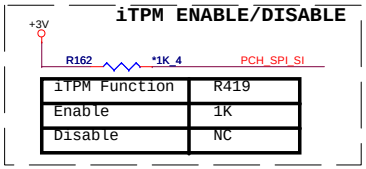
EC-B- 25

W25Q64CVSSIG: AKE3EFP0N04
MX25L6406EM2I-12G: AKE3NFP0Z00
EN25Q64-104HIP: AKE3EFN0Q00

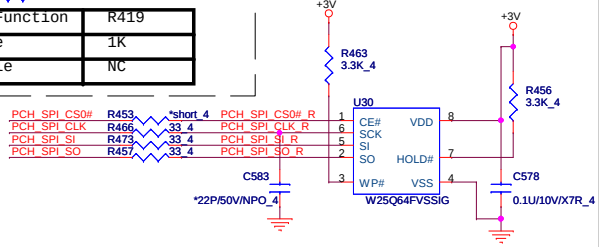
PCH Dual SPL

64Mbit (8M Byte), SPI

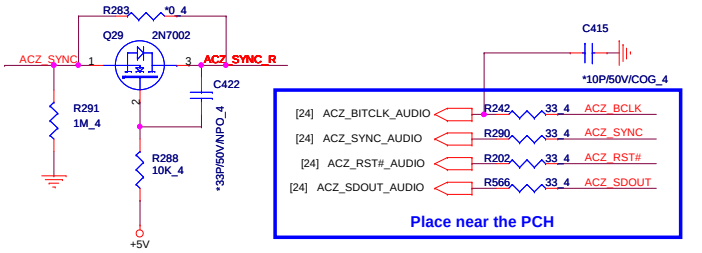
iTPM ENABLE/DISABLE



iTPM Function	R419
Enable	1K
Disable	NC



HDA Bus(CLG)



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Quanta Computer Inc.

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Panther/Cougar Point-M (PCI,USB,NVRAM)

Panther/Cougar Point-M (PCI-E,SMBUS,CLK)

09

PCI/USBOC# Pull-up(CLG)

+3V
PCI_PIRQA# R223 8.2K_4
PCI_PIRQB# R236 8.2K_4
PCI_PIRQC# R218 8.2K_4
PCI_PIRQD# R213 8.2K_4

+3V
RP1
PIRQH#
PWM_SELECT#
PIRQG#
MPC_PWR_CTRL#
PIRQF#
REQ2#
10K_10P8R_6

3V_S5
RP12
USB_OC4#
USB_OC1#
USB_OC2#
USB_OC3#
USB_OC6#
USB_OC0#
USB_OC7#
USB_OC5#
10K_10P8R_6

Port4-Port7 not support UM77

USB3.0

[28] USB30_RX1-
[28] USB30_RX2-
[28] USB30_RX1+
[28] USB30_RX2+
[28] USB30_TX1-
[28] USB30_TX2-
[28] USB30_TX1+
[28] USB30_TX2+

USB ports 6 and 7 are disabled on 12 port SKUs(UM77).

USB ports 12 and 13 are disabled on 10 port SKUs(UM77).

USB 3.0
USB 3.0 (BIOS debug)
CCD
WLAN/BT
USB2.0/USB3.0 COMBO
USB2.0/USB3.0 COMBO
EHCI1
WLAN

USB 2.0(common design for 14")
USB 2.0 (DB&BIOS debug)
Card Reader
EHCI2
WLAN
LAN

OC0# For USB3.0
OC4# For USB2.0

PLTRST#(CLG)

3V_S5
C692 *0.1U/10V/X7R_4
U35 *TC7SH08FU
R586 100K_4
R585 *short_4
PCI_PLTRST#
PLTRST#
PLTRST# [3,15,25,27,30]

DGPU Power ON

R610 DIS@_4
R611 *DIS@_4
R237 *DIS@10K_4
3V_GPU_EN_EC [34]
DGPU_PWR_EN
GFXON [45,46]
EC-B-03

SMBus/Pull-up(CLG)

2N7002KDW Q52A
Q52B 2N7002KDW
Q53A 2N7002KDW
Q53B 2N7002KDW
SMB_ME1_CLK
SMB_ME1_DAT
SMB_PCH_DAT
SMB_PCH_CLK
R272 2.2K_4
R273 2.2K_4
R280 4.7K_4
R281 4.7K_4
PDAT_SMB [13,14]
PCLK_SMB [13,14]
EC-B-17

CLK_REQ/Strap Pin(CLG)

CLK_PCIE_REQ1# R534 10K_4
PCIECLKRQ2# R164 10K_4
PCIECLKRQ0# R552 10K_4
PCIECLKRQ3# R577 10K_4
PCIE_CLKREQ_WLAN# R251 10K_4
CLK_PEGB_REQ# R250 10K_4
PCIECLKRQ6# R229 10K_4
PCIECLKRQ7# R253 10K_4
CLK_PEGA_REQ# R259 DIS@10K_4
PCIE_CLKREQ_LAN# R183 10K_4
CLK_PEGA_REQ# R240 *UMA@10K_4
CLK_BUF_BCLK_N R469 10K_4
CLK_BUF_BCLK_P R468 10K_4
CLK_BUF_PCIE_3GPLL# R124 10K_4
CLK_BUF_PCIE_3GPLL R125 10K_4
CLK_BUF_DREFCLK# R188 10K_4
CLK_BUF_DREFCLK R205 10K_4
CLK_BUF_DREFSSCLK# R134 10K_4
CLK_BUF_DREFSSCLK R139 10K_4
CLK_PCH_14M R211 10K_4
CLOCK TERMINATION for FCIM

PCIE Clock

Layout note:
PCIE_CLKREQ_LAN# layout adjacent to CLK_PEGA_REQ#

DGPU_HOLD_RST# R593 DIS@100K_4
GFXON R243 DIS@100K_4

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R198 *1K_4

SMBus/Pull-up(CLG)

R574 1K_4 DRAMRST_CNTRL_PCH
R252 10K_4 SMBALERT#
R583 2.2K_4 SMB_PCH_CLK
R584 2.2K_4 SMB_PCH_DAT
R562 2.2K_4 SMB_ME0_CLK
R255 2.2K_4 SMB_ME0_DAT
R254 10K_4 SMLIALERT#_R

R214 *10K_4 CL_CLK_R
R191 *10K_4 CL_DAT_R
R185 *10K_4 CL_RST#_R

3V_S5 [3,7,8,10,11,24,30,35,37]
+3V [3,7,8,10,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

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Quanta Computer Inc.

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	PCH 3/6 (PCIE/USB/CLK)	3A

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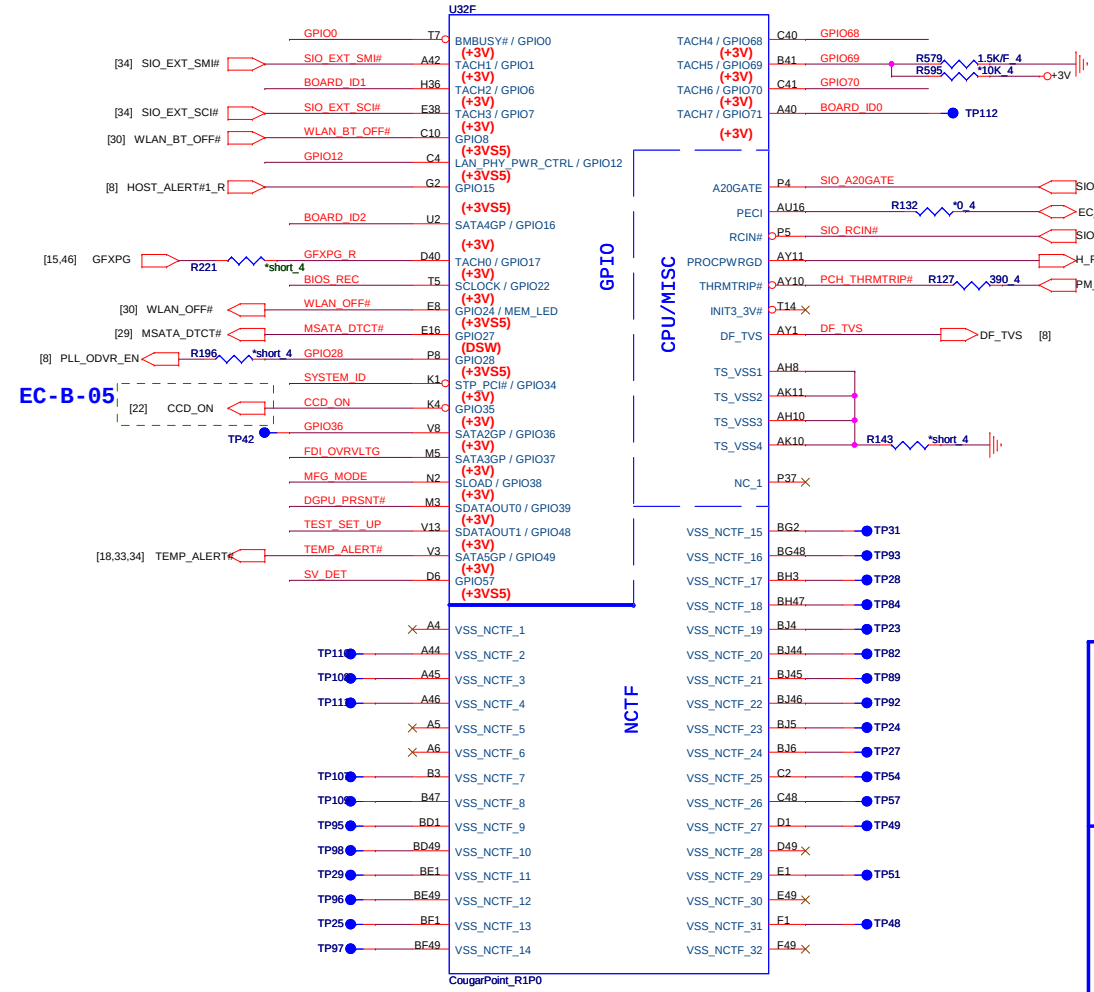
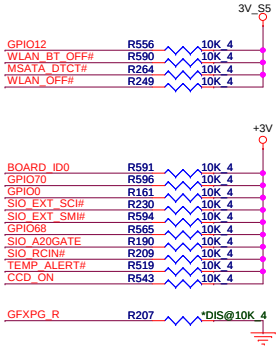
Panther/Cougar Point (GPIO,VSS_NCTF,RSVD)



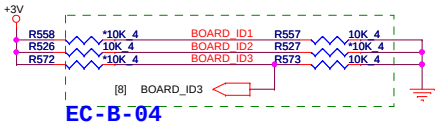
3V_S5 [3,7,8,9,11,24,30,35,37]
+3V [3,7,8,9,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

GPIO Pull-up/Pull-down(CLG)



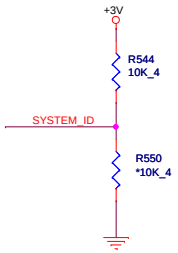
BOARD ID SETTING

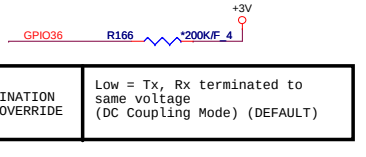
Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			



EC-B-04
EC-C-02

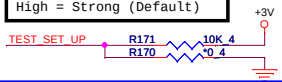
	SYSTEM_ID
LZ7	0
LZ8	1





DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

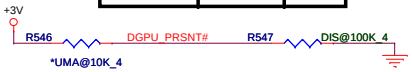
SV_SET_UP
High = Strong (Default)

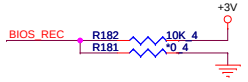


FDI TERMINATION VOLTAGE OVERRIDE	LOW = Tx, Rx terminated to same voltage

MFG-TEST

	Optimus	UMA
Stuff	R547	R546
No Stuff	R546	R547





BIOS RECOVERY	High = Disable (Default) Low = Enable

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	3A

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Panther/Cougar Point-M (POWER)

Panther/COUGAR POINT (POWER)

11

POWER

U32J

CougarPoint_R1P0

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

FOR DEEP S3

1.01A (60mils)

3mA (10mils)

119mA (20mils)

119mA (15mils)

266mA (20mils)

160mA (20mils)

80mA 40mils)

80mA (40mils)

55mA (10mils)

95mA (10mils)

1.01A (60mils)

10mA (10mils)

V_PROC_IO=1mA (10mils)

VCCRTC<1mA (10mils)

U32G

CougarPoint_R1P0

VCC CORE

VCCIO

CRT

LVDS

HVCMOS

DMI

DFT / SPI

FDI

1.3 A (60mils)

2.925 A (140mils)

(Mobile 1.5V)

160mA (15mils)

1mA (10mils)

60mA (10mils)

EC-B-23

42mA (10mils)

190 mA (15mils)

20mA (10mils)

FOR DEEP S3

EC-C-07

EC-B-15

VCC5REFSUS=1mA

V5REF= 1mA

80mA (40mils)

80mA (40mils)

20mA (10mils)

20mA (10mils)

5VPCU [22,36,37,39,40,41,42,43,44,45,46]
+3V_RTC [7,8,34]
3V_S5 [3,7,8,9,10,24,30,35,37]
+3V [3,7,8,9,10,13,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
5V_S5 [28,32,37]
+5V [8,23,24,26,33,36,37,38]
+1.05V [3,5,7,8,9,37,41,46]
1.5V_SUS [3,13,14,36,37,40,46]
+1.8V [5,8,37,43]
+3V_DSW [7,8]

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	PCH 5/6 (POWER)	3A

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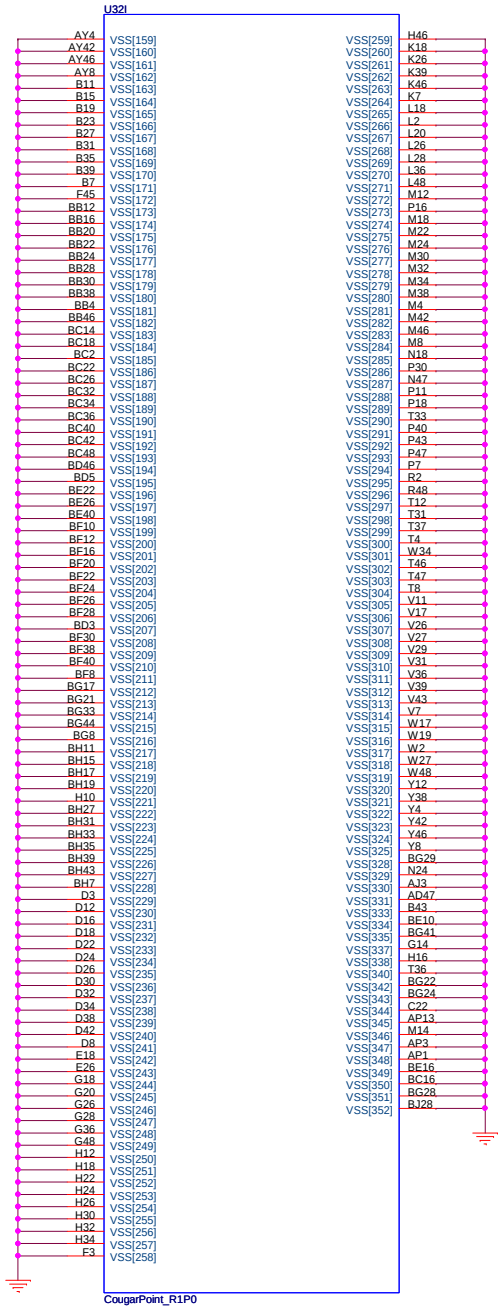
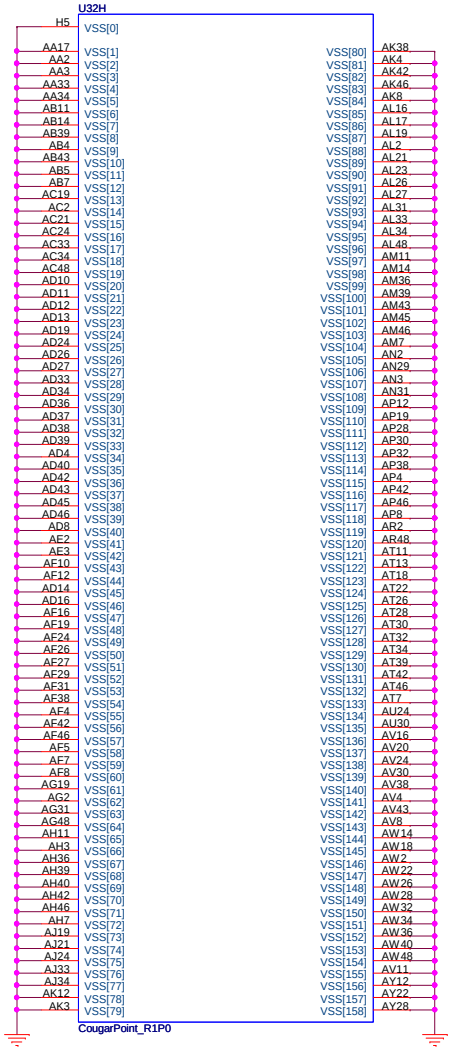
Panther/Cougar Point-M (GND)



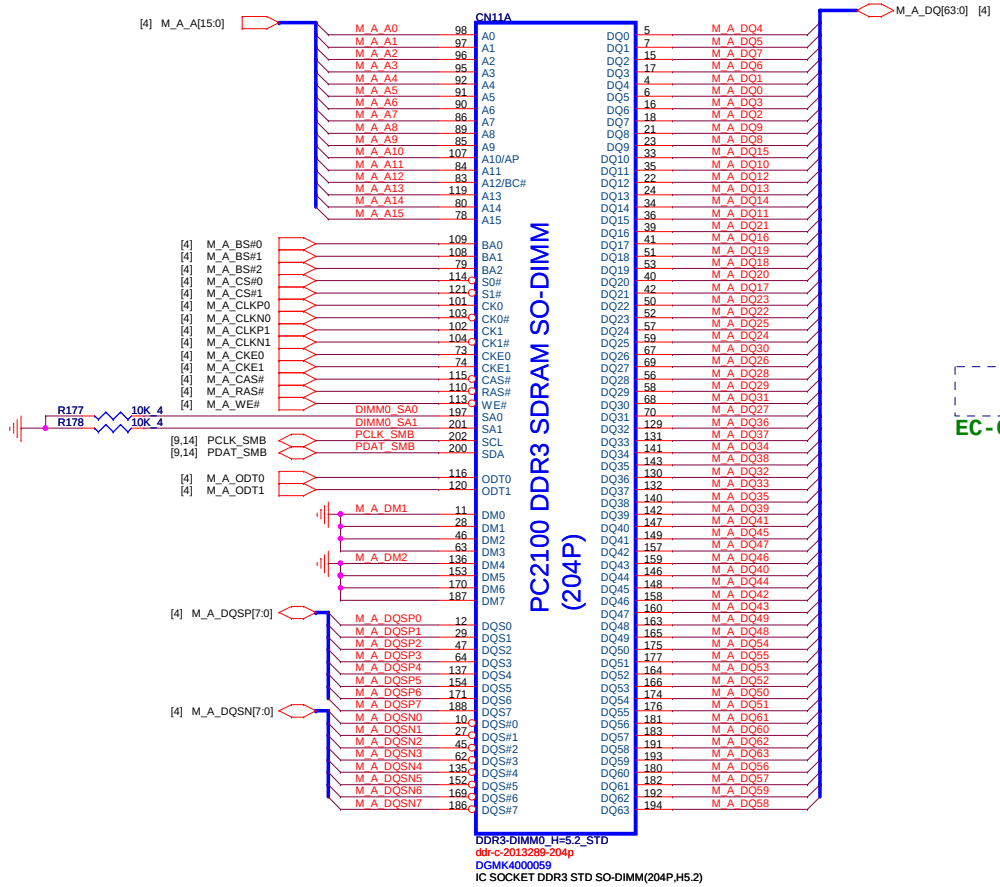
Panther/Cougar Point-M (GND)

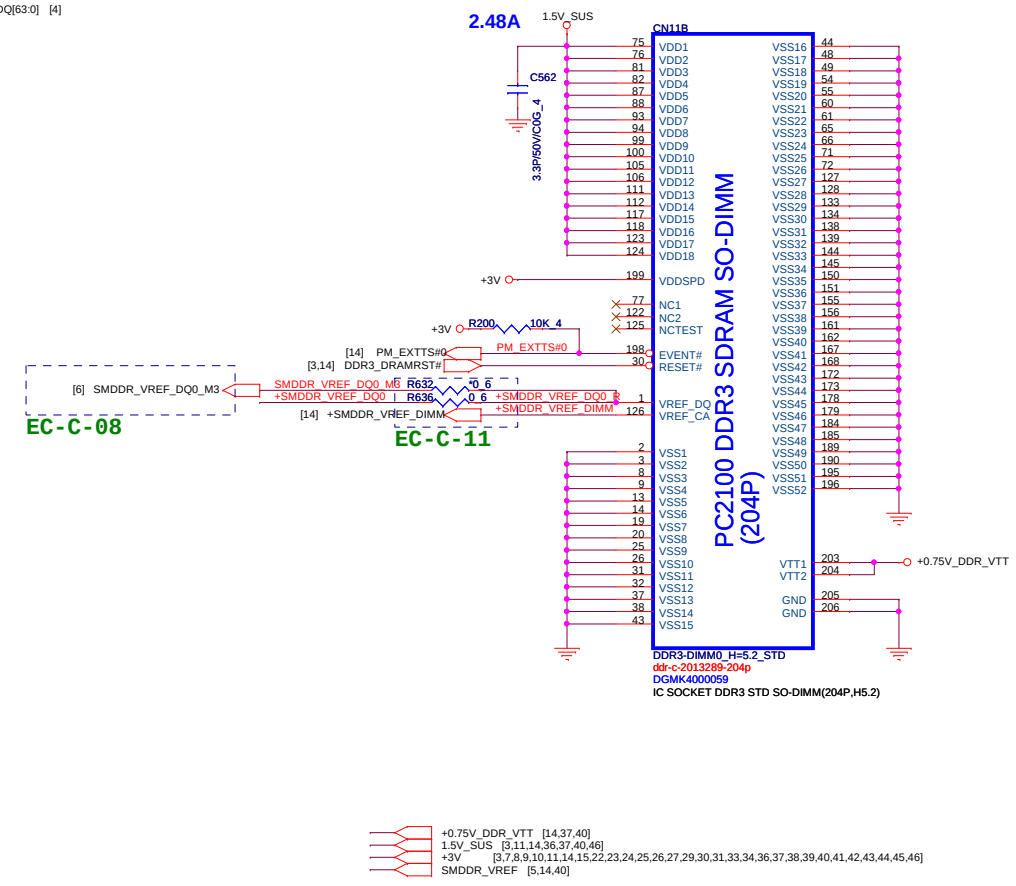


PROJECT LZ8 Chief River DIS

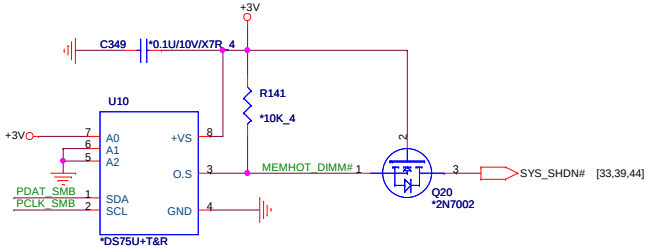
Quanta Computer Inc.

Size	Document Number	Rev
	PCH 6/6 (GND)	1A
Date: Friday, November 11, 2011	Sheet 12 of 49	



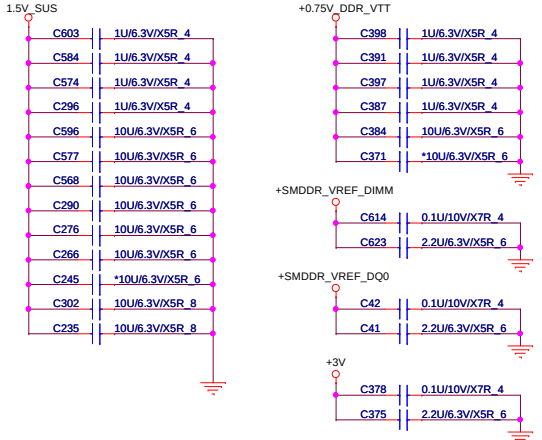


+0.75V_DDR_VTT [14,37,40]
1.5V_SUS [3,11,14,36,37,40,46]
+3V [3,7,8,9,10,11,14,15,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
SMDDR_VREF [5,14,40]

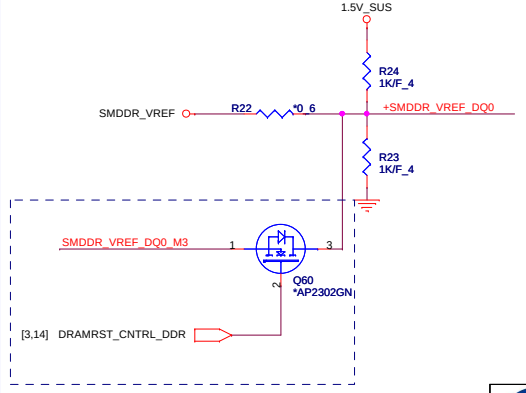


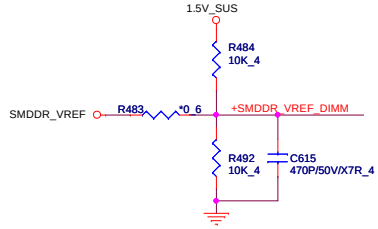
ADDRESS: 92H Close DDR3 socket CN22,CN23

Place these Caps near So-Dimm0.



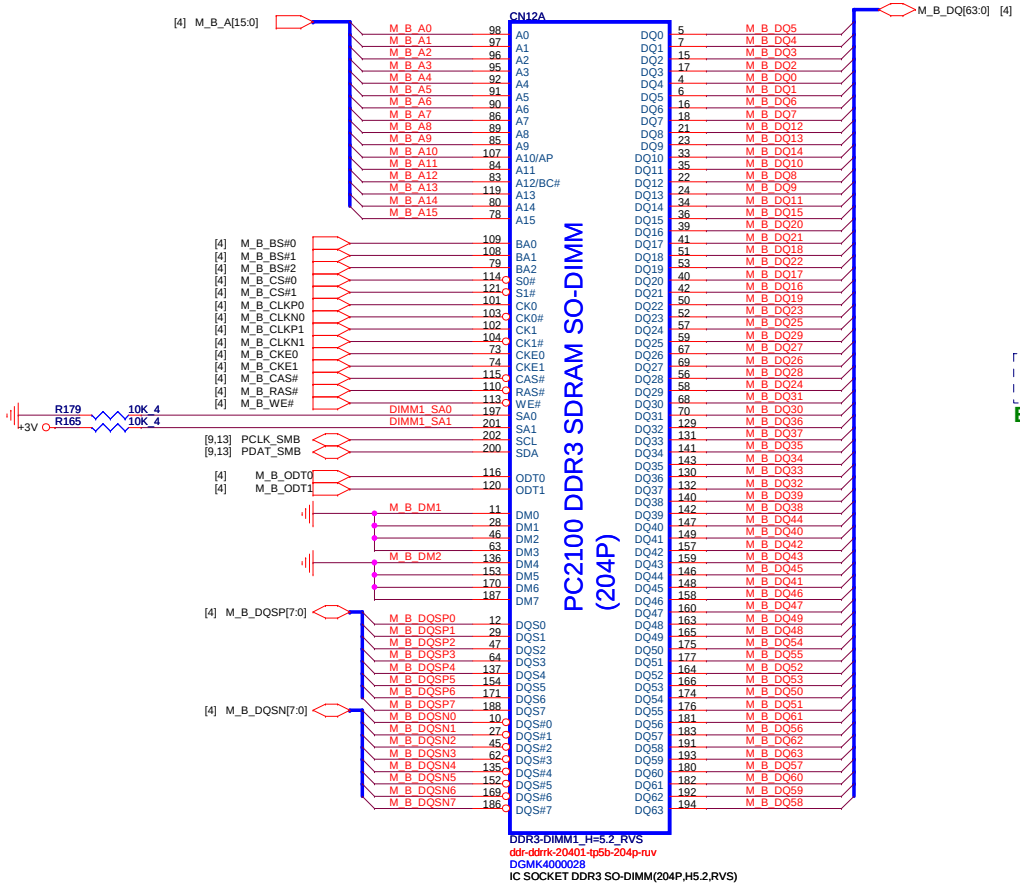
VREF DQ0 M1/M3 Solution

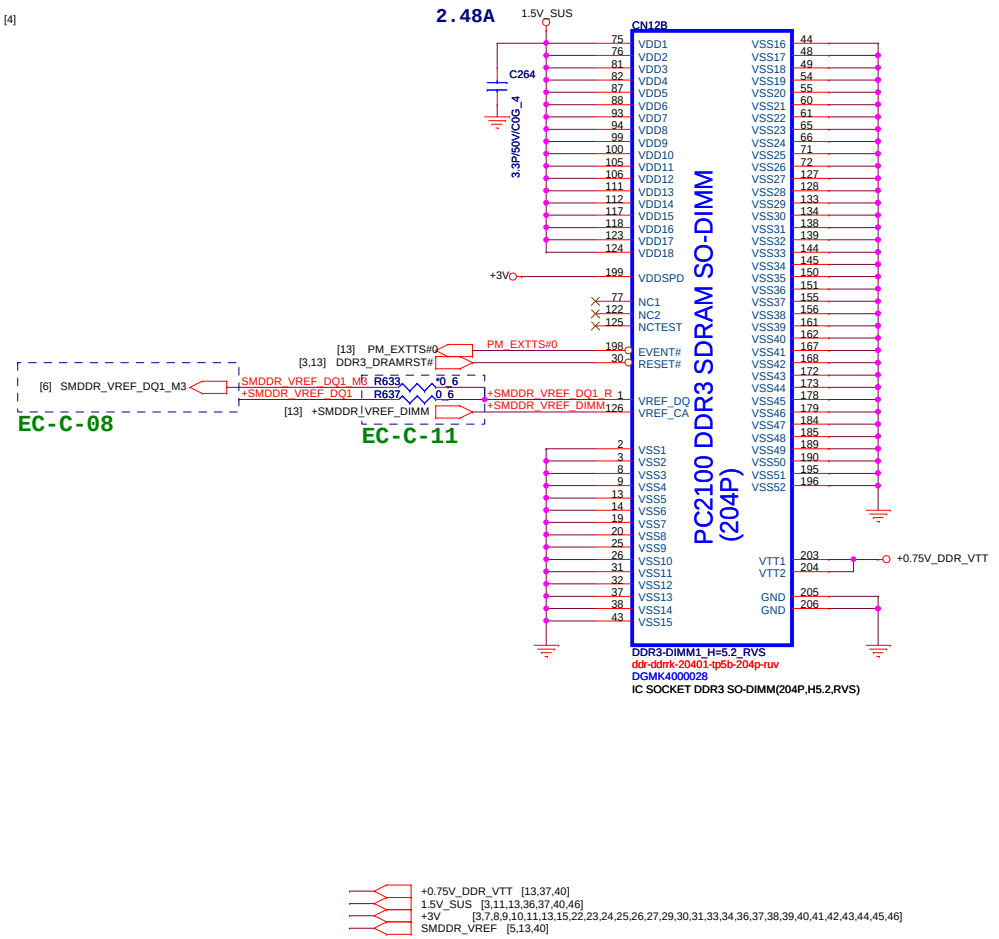




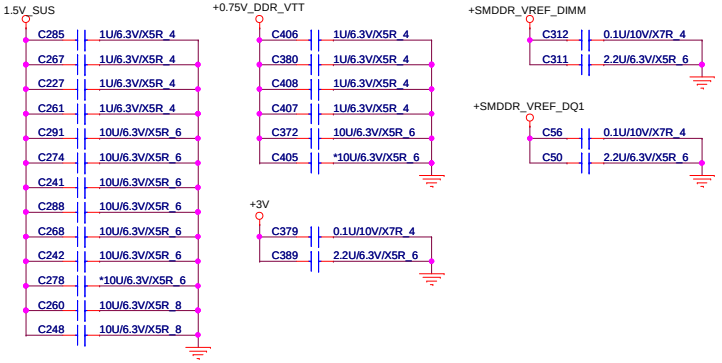
PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	Custom DDR3 DIMM0-STD (5.2H)	3A
Date: Tuesday, December 20, 2011	Sheet 13 of 49	

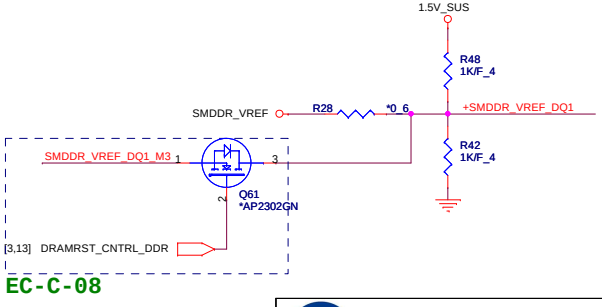




Place these Caps near So-Dimm1.



VREF DQ1 M1/M3 Solution



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	Custom DDR3 DIMM1-RVS (4.0H)	3A
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U23A

N13M

1/13 PCI_EXPRESS

3.55A

1.05V_GFX_PCIE

C53 DIS@1U/6.3V/X5R_4
C105 DIS@1U/6.3V/X5R_4
C66 DIS@22U/6.3V_8
C96 DIS@22U/6.3V_8
C37 DIS@4.7U/6.3V/X5R_6
C40 DIS@10U/6.3V/X5R_8
C48 DIS@10U/6.3V/X5R_8

PLACE NEAR BALLS

1.05V_GFX_PCIE

C45 DIS@22U/6.3V_8
C59 DIS@22U/6.3V_8
C87 DIS@1U/6.3V/X5R_4
C120 DIS@1U/6.3V/X5R_4
C43 DIS@4.7U/6.3V/X5R_6
C39 DIS@10U/6.3V/X5R_8
C36 DIS@10U/6.3V/X5R_8

PLACE UNDER BALLS

AC9 AD7 AD8 AE7 AF7 AG7 → PEX_IOVDD_01 … PEX_IOVDD_06

AB13 AB16 AB17 AB7 AB8 AB9 AC13 AC7 AD6 AE6 AF6 AG6 → PEX_IOVDDQ_01 … PEX_IOVDDQ_12

PLACE UNDER BALLS

VGPU_CORE

16.82A

C135 C136 C99 C107 C73 DIS@4.7U/6.3V/X5R_6

C97 DIS@4.7U/6.3V/X5R_6
C103 C134 C115 C76 DIS@0.1U/10V/X7R_4

C75 C86 C137 DIS@4.7U/6.3V/X5R_6

C89 DIS@22U/6.3V/X5R_8
C68 DIS@47U/6.3V/X5R_8
C20 DIS@4.7U/6.3V/X5R_6

C12 *220U/2.5V_3216

PLACE NEAR BALLS

J10 J12 J13 J9 L9 M11 M17 M9 N11 N12 N13 N14 N15 N16 N17 N19 N9 P11 P12 P13 P14 P15 P16 P17 R11 R12 R13 R14 R15 R16 R17 R9 T11 T17 T9 U19 U9 W10 W12 W13 W18 W19 W9 → VDD_01 … VDD_43

[45] GPU_VDD_SENSE → W15 VDD_SENSE
[45] GPU_VSS_SENSE → W16 GND_SENSE
E15 VDD_SENSE (NC)
E14 GND_SENSE (GND)

80mA

3V_GPU

1.05V_GFX_PCIE

L3 DIS@0_6

C82 DIS@4.7U/6.3V/X5R_6
C94 DIS@1U/6.3V/X5R_4
C92 DIS@0.1U/10V/X7R_4
C70 DIS@0.1U/10V/X7R_4
C101 DIS@0.1U/10V/X7R_4

A12 B12 C12 D12 E12 F12 → VDD33_01 … VDD33_06

PLACE UNDER BALLS

110mA
12~16 mils

C72 DIS@0.1U/10V/X7R_4
C33 *DIS@1U/16V/X7R_6
C32 DIS@22U/6.3V_8

PLACE NEAR BALLS

+PEX_PLLVDD → AF9 PEX_PLLVDD

R391 *DIS@200_4 → AE10 PEX_TSTCLK_OUT*
AF10 PEX_TSTCLK_OUT

3V_GPU

AG9 PEG_SVDD (NC)

PEX_TERMP → AG10 PEX_TERMP

C69 DIS@0.1U/10V/X7R_4
C65 DIS@4.7U/6.3V/X5R_6
C60 DIS@1U/6.3V/X5R_4

R390 DIS@2.49K/F_4

DIS@U_GPU_GB1_64

(NC) PEX_CLKREQ ← AE9 PEX_CLKREQ#
PEX_RST* ← AD9 GPU_RST#

PEX_REFCLK ← AB10 CLK_PCIE_VGAP [9]
PEX_REFCLK* ← AC10 CLK_PCIE_VGAN [9]

PEX_TX0	AD10	C_PEG_RX0	C57	DIS@0.1U/10V/X5R_4	PEG_RXP15
PEX_TX0*	AD11	C_PEG_RX#0	C61	DIS@0.1U/10V/X5R_4	PEG_RXN15
PEX_TX1	AD12	C_PEG_RX1	C62	DIS@0.1U/10V/X5R_4	PEG_RXP14
PEX_TX1*	AC12	C_PEG_RX#1	C71	DIS@0.1U/10V/X5R_4	PEG_RXN14
PEX_TX2	AB11	C_PEG_RX2	C52	DIS@0.1U/10V/X5R_4	PEG_RXP13
PEX_TX2*	AB12	C_PEG_RX#2	C54	DIS@0.1U/10V/X5R_4	PEG_RXN13
PEX_TX3	AD13	C_PEG_RX3	C85	DIS@0.1U/10V/X5R_4	PEG_RXP12
PEX_TX3*	AD14	C_PEG_RX#3	C93	DIS@0.1U/10V/X5R_4	PEG_RXN12
PEX_TX4	AD15	C_PEG_RX4	C100	DIS@0.1U/10V/X5R_4	PEG_RXP11
PEX_TX4*	AC15	C_PEG_RX#4	C95	DIS@0.1U/10V/X5R_4	PEG_RXN11
PEX_TX5	AB14	C_PEG_RX5	C74	DIS@0.1U/10V/X5R_4	PEG_RXP10
PEX_TX5*	AB15	C_PEG_RX#5	C81	DIS@0.1U/10V/X5R_4	PEG_RXN10
PEX_TX6	AC16	C_PEG_RX6	C104	DIS@0.1U/10V/X5R_4	PEG_RXP9
PEX_TX6*	AD16	C_PEG_RX#6	C112	DIS@0.1U/10V/X5R_4	PEG_RXN9
PEX_TX7	AD17	C_PEG_RX7	C145	DIS@0.1U/10V/X5R_4	PEG_RXP8
PEX_TX7*	AD18	C_PEG_RX#7	C154	DIS@0.1U/10V/X5R_4	PEG_RXN8
PEX_TX8	AC18	C_PEG_RX8	C132	DIS@0.1U/10V/X5R_4	PEG_RXP7
PEX_TX8*	AB18	C_PEG_RX#8	C141	DIS@0.1U/10V/X5R_4	PEG_RXN7
PEX_TX9	AB19	C_PEG_RX9	C116	DIS@0.1U/10V/X5R_4	PEG_RXP6
PEX_TX9*	AB20	C_PEG_RX#9	C125	DIS@0.1U/10V/X5R_4	PEG_RXN6
PEX_TX10	AD19	C_PEG_RX10	C160	DIS@0.1U/10V/X5R_4	PEG_RXP5
PEX_TX10*	AD20	C_PEG_RX#10	C168	DIS@0.1U/10V/X5R_4	PEG_RXN5
PEX_TX11	AD21	C_PEG_RX11	C189	DIS@0.1U/10V/X5R_4	PEG_RXP4
PEX_TX11*	AC21	C_PEG_RX#11	C181	DIS@0.1U/10V/X5R_4	PEG_RXN4
PEX_TX12	AB21	C_PEG_RX12	C174	DIS@0.1U/10V/X5R_4	PEG_RXP3
PEX_TX12*	AB22	C_PEG_RX#12	C180	DIS@0.1U/10V/X5R_4	PEG_RXN3
PEX_TX13	AC22	C_PEG_RX13	C191	DIS@0.1U/10V/X5R_4	PEG_RXP2
PEX_TX13*	AD22	C_PEG_RX#13	C196	DIS@0.1U/10V/X5R_4	PEG_RXN2
PEX_TX14	AD23	C_PEG_RX14	C197	DIS@0.1U/10V/X5R_4	PEG_RXP1
PEX_TX14*	AD24	C_PEG_RX#14	C208	DIS@0.1U/10V/X5R_4	PEG_RXN1
PEX_TX15	AE25	C_PEG_RX15	C209	DIS@0.1U/10V/X5R_4	PEG_RXP0
PEX_TX15*	AE26	C_PEG_RX#15	C212	DIS@0.1U/10V/X5R_4	PEG_RXN0

PEX_RX0	AE12	PEG_TXP15	PEG_TXP15 [3]
PEX_RX0*	AF12	PEG_TXN15	PEG_TXN15 [3]
PEX_RX1	AG12	PEG_TXP14	PEG_TXP14 [3]
PEX_RX1*	AG13	PEG_TXN14	PEG_TXN14 [3]
PEX_RX2	AF13	PEG_TXP13	PEG_TXP13 [3]
PEX_RX2*	AE13	PEG_TXN13	PEG_TXN13 [3]
PEX_RX3	AE15	PEG_TXP12	PEG_TXP12 [3]
PEX_RX3*	AF15	PEG_TXN12	PEG_TXN12 [3]
PEX_RX4	AG15	PEG_TXP11	PEG_TXP11 [3]
PEX_RX4*	AG16	PEG_TXN11	PEG_TXN11 [3]
PEX_RX5	AF16	PEG_TXP10	PEG_TXP10 [3]
PEX_RX5*	AE16	PEG_TXN10	PEG_TXN10 [3]
PEX_RX6	AE18	PEG_TXP9	PEG_TXP9 [3]
PEX_RX6*	AF18	PEG_TXN9	PEG_TXN9 [3]
PEX_RX7	AG18	PEG_TXP8	PEG_TXP8 [3]
PEX_RX7*	AG19	PEG_TXN8	PEG_TXN8 [3]
PEX_RX8	AF19	PEG_TXP7	PEG_TXP7 [3]
PEX_RX8*	AE19	PEG_TXN7	PEG_TXN7 [3]
PEX_RX9	AE21	PEG_TXP6	PEG_TXP6 [3]
PEX_RX9*	AF21	PEG_TXN6	PEG_TXN6 [3]
PEX_RX10	AG21	PEG_TXP5	PEG_TXP5 [3]
PEX_RX10*	AG22	PEG_TXN5	PEG_TXN5 [3]
PEX_RX11	AF22	PEG_TXP4	PEG_TXP4 [3]
PEX_RX11*	AE22	PEG_TXN4	PEG_TXN4 [3]
PEX_RX12	AE24	PEG_TXP3	PEG_TXP3 [3]
PEX_RX12*	AF24	PEG_TXN3	PEG_TXN3 [3]
PEX_RX13	AG24	PEG_TXP2	PEG_TXP2 [3]
PEX_RX13*	AF25	PEG_TXN2	PEG_TXN2 [3]
PEX_RX14	AG25	PEG_TXP1	PEG_TXP1 [3]
PEX_RX14*	AG26	PEG_TXN1	PEG_TXN1 [3]
PEX_RX15	AF27	PEG_TXP0	PEG_TXP0 [3]
PEX_RX15*	AE27	PEG_TXN0	PEG_TXN0 [3]

[16,17,46] 1.05V_GFX_PCIE
[17,18,46] 3V_GPU
[16,19,20,46] 1.5V_GPU
[3,7,8,9,10,11,13,14,22,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46] +3V
[45] VGPU_CORE

R386 DIS@10K/F_4 3V_GPU

R387 *DIS@10K/F_4

For PCIE clock request signal 07/05

PEG_TXP[0..15] → PEG_TXP[0..15] [3]
PEG_TXN[0..15] → PEG_TXN[0..15] [3]
PEG_RXN[0..15] → PEG_RXN[0..15] [3]
PEG_RXP[0..15] → PEG_RXP[0..15] [3]

For power-down sequency

3V_GPU → D3 DIS@RB500V-40 → 1.5V_GPU
3V_GPU → D4 DIS@RB500V-40 → VGPU_CORE

PEG CLK detect

GFXPG [10,46]
[9] CLK_PEGA_REQ# → Q36 DIS@ME2N7002E → PEX_CLKREQ#

GPU RST#(CLG)

+3V
C487 DIS@0.1U/10V/X7R_4
[3,9,25,27,30] PLTRST#
[9] DGPU_HOLD_RST#
U19 DIS@TC7SH08FU(F)
GPU_RST#

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N13M(PCIE I/F) 1/5	1A

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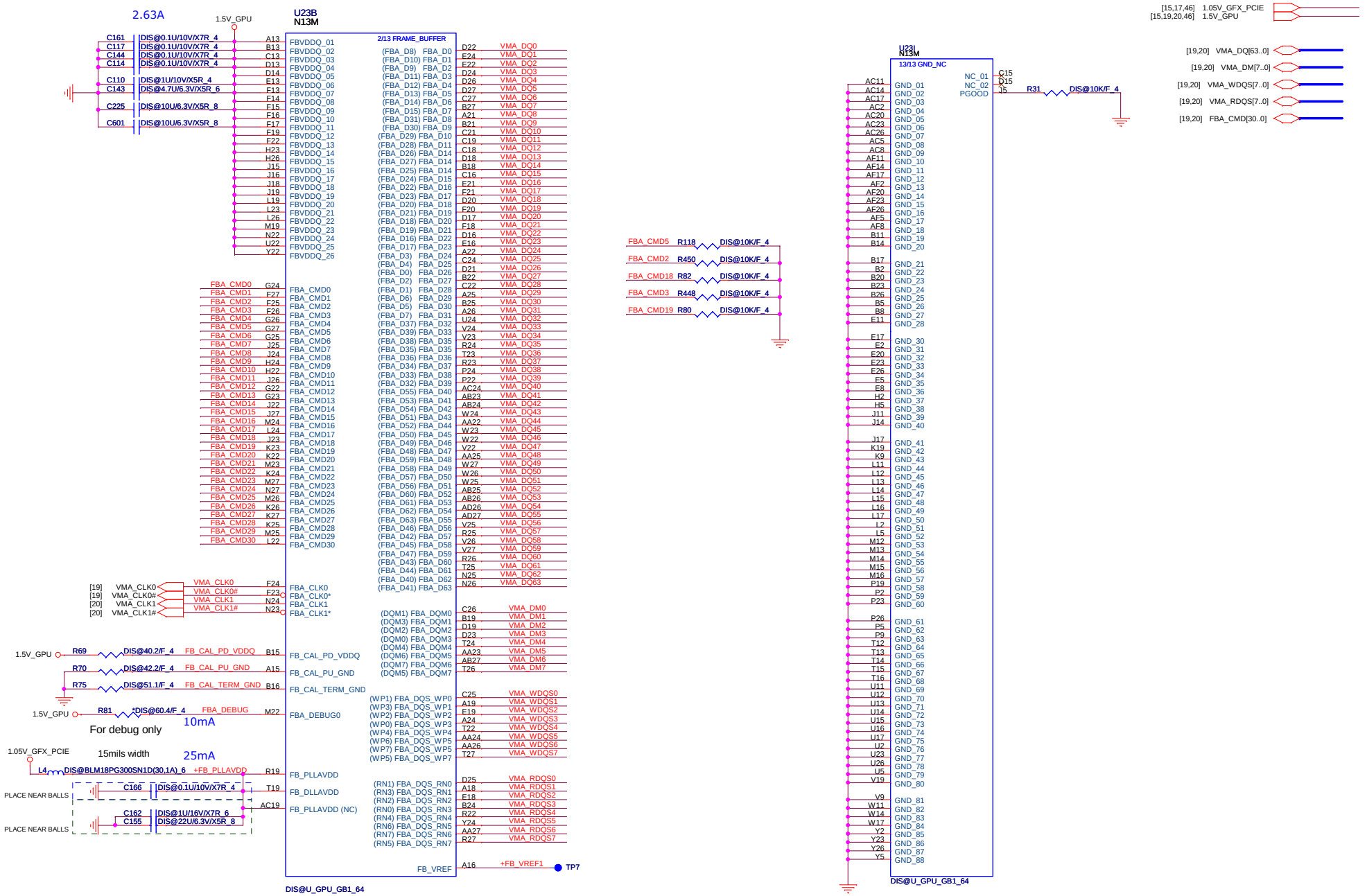

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	N13M(MEMORY I/F & GND) 2/5	1A

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[15,16,46] 1.05V_GFX_PCIE
[15,18,46] 3V_GPU

220 mA (1.05V +/- 3%)

220 mA (1.8V)

U23F
N13M
6/13 IFPAB

+IFPAB_PLLVDD AD5 IFPAB_PLLVDD
TP72 AB6 IFPAB_RSET
R33 DIS@10K_4

+IFPAB_IOVDD V3 IFPA_IOVDD
V2 IFPB_IOVDD
R29 DIS@10K_4

A
DATA
B
CLOCK
A
B

IFPA_TXD0* V4
IFPA_TXD0 V5
IFPA_TXD1* AA4
IFPA_TXD1 AA5
IFPA_TXD2* Y4
IFPA_TXD2 W4
IFPA_TXD3* AB5
IFPA_TXD3 AB4
IFPB_TXD4* V1
IFPB_TXD4 W1
IFPB_TXD5* W2
IFPB_TXD5 W3
IFPB_TXD6* AA3
IFPB_TXD6 AA2
IFPB_TXD7* AA1
IFPB_TXD7 AB1
IFPA_TXC* AD4
IFPA_TXC AC4
IFPB_TXC* AB2
IFPB_TXC AB3

DIS@U_GPU_GB1_64

U23G
N13M
8/13 IFPE

+IFPD_PLLVDD N6 IFPD_PLLVDD
TP64 M6 IFPD_RSET
R38 DIS@10K_4

+IFPDE_IOVDD H6 IFPDE_IOVDD
R47 DIS@10K_4

DVI DP
D
TXC TXC
TXD0 TXD0
TXD1 TXD1
TXD2 TXD2

IFPD_AUX* D4
IFPD_AUX C3
IFPD_L3* B4
IFPD_L3 B3
IFPD_L2* C4
IFPD_L2 C3
IFPD_L1* D5
IFPD_L1 C4
IFPD_L0* E4
IFPD_L0 E5

DIS@U_GPU_GB1_64

120 mA

U23C
N13M
3/13 DACA

3V_GPU
R357 *DIS@0_8 +DACA_VDD AG2
R373 DIS@10K_4
DACA_VDD
DACA_VREF AE1
DACA_RSET AE1
DACA_VREF
DACA_RSET
C495 *DIS@0.1U/10V/X5R_4
R382 *DIS@124/F_4

DACA_HSYNC AD2 1 TP66
DACA_VSYNC AD1 TP63
DACA_RED AE2 1 TP65
DACA_GREEN AE3 TP67
DACA_BLUE AD3 1 TP69

DIS@U_GPU_GB1_64

220 mA

285 mA (1.05V +/- 3%)

U23H
N13M
7/13 IFPC

+IFPC_PLLVDD P6 IFPC_PLLVDD
TP2 1 R5 IFPC_RSET
R40 DIS@10K_4

+IFPC_IOVDD J6 IFPC_IOVDD
R34 DIS@10K_4

DVI DP
C
TXC TXC
TXD0 TXD0
TXD1 TXD1
TXD2 TXD2

IFPC_AUX* G5
IFPC_AUX G4
IFPC_L3* J4
IFPC_L3 H4
IFPC_L2* K4
IFPC_L2 L4
IFPC_L1* M4
IFPC_L1 M5
IFPC_L0* N4
IFPC_L0 P4

DIS@U_GPU_GB1_64

U23D
N13M
5/13 DACC

+DACB_VDD W5 DACB_VDD
TP3 1 R6 DACB_VREF
TP6 1 V6 DACB_RSET
R32 DIS@10K_4

DACB_HSYNC U6
DACB_VSYNC U4
DACB_RED T5
DACB_GREEN T4
DACB_BLUE R4

DIS@U_GPU_GB1_64

U23E
N13M
8/13 IFPE

IFPE_PLLVDD D7
TP4 F8 IFPE_PLLVDD(DACB_VDD)
IFPD_RSET(DACB_RSET)
R36 DIS@10K/F_4

DVI DP
E
TXC TXC
TXD0 TXD0
TXD1 TXD1
TXD2 TXD2

IFPE_AUX* G6
IFPE_AUX F7
IFPE_L3* E7
IFPE_L3 E6
IFPE_L2* B7
IFPE_L2 B6
IFPE_L1* A7
IFPE_L1 A6
IFPE_L0* C6
IFPE_L0 D6

DIS@U_GPU_GB1_64

60mA
45mA
45mA

1.05V_GFX_PCIE L1 DIS@BLM18PG300SN1D(30,1A) PLLVDD
C49 DIS@0.1U/10V/X7R_4
C44 DIS@22U/6.3V/X5R_8

1.05V_GFX_PCIE L2 DIS@EMI FILTER HCB1608KF-181T15(180,1.5A)
PLACE UNDER BALLS
C55 DIS@0.1U/10V/X7R_4
C51 DIS@0.1U/10V/X7R_4
C46 DIS@4.7U/6.3V/X5R_6
+NV_PLLVDD
C38 DIS@22U/6.3V/X5R_8
PLACE NEAR BALLS

U23J
N13M
DIS@U_GPU_GB1_64
12/13 XTAL_PLL

PLLVDD K5
VID_PLLVDD K6
SP_PLLVDD L6
XTAL_SSIN D11
XTAL_IN D10
XTAL_OUTBUFF F9 BXTALOUT
XTAL_OUT E10 XTALOUT

R43 DIS@10K/F_4 XTAL_SSIN
XTALIN D10
R37 DIS@10K/F_4
Y1 DIS@27MHZ 30ppm
C77 DIS@27P/50V/NPO_4
C78 DIS@27P/50V/NPO_4

STUFF PDs on XTALSSIN and
XTALOUTBUFF WHEN EXT_SS
Install it when not connected to Spread spectrum device

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	N13M(DISPLAY) 3/5	1A

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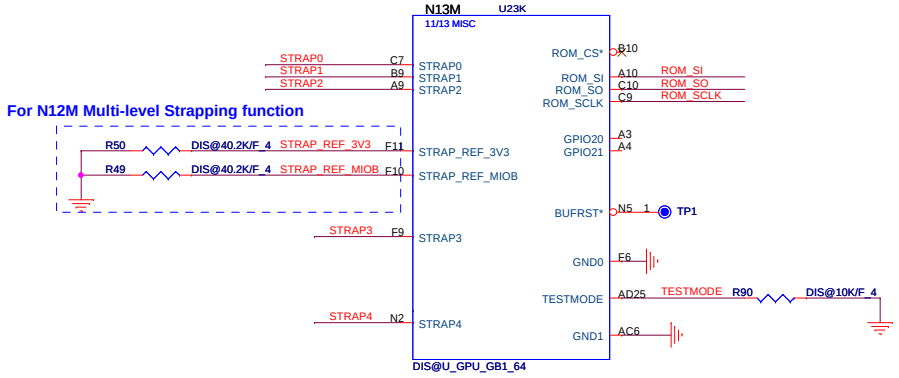
nV FAE suggest that the device ID
for N13M-GE1 is 0x1058

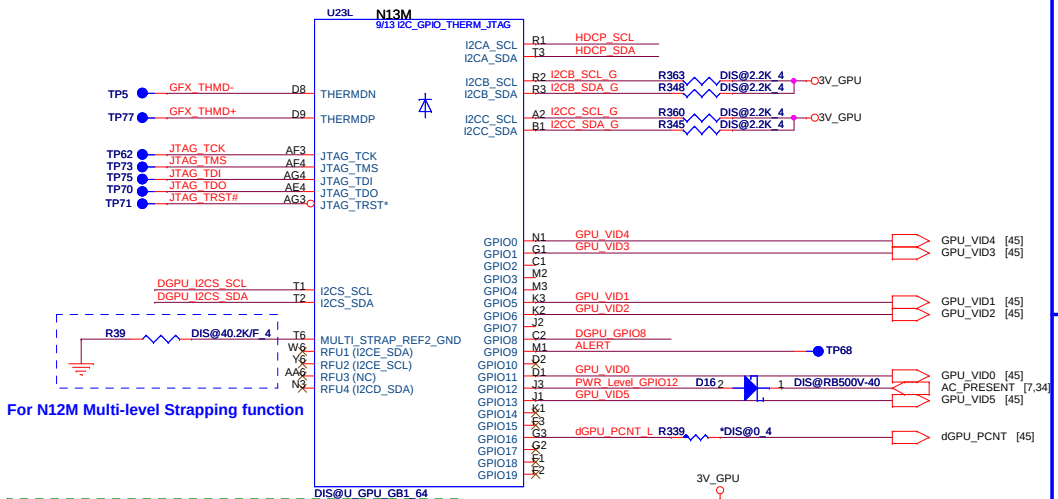
[15,17,46] 3V_GPU



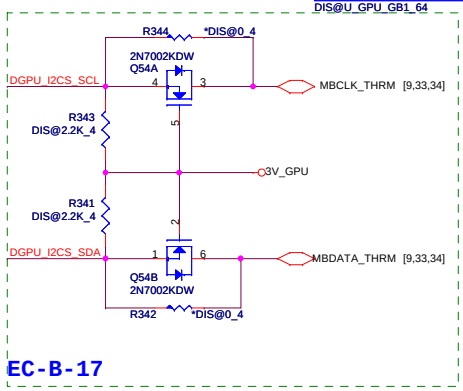
For N12M Multi-level Strapping function

9.5 Unused I2C Pins

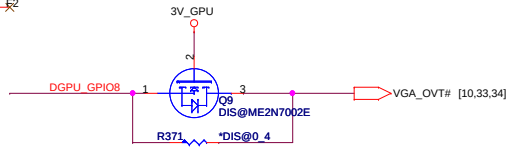
For unused dedicated (non-AUX) I2C pins, pull-up both the I2Cx_SCL, I2Cx_SDA, to 3.3 V using 2.2 kΩ resistors.routing.



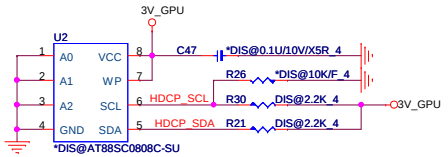
For N12M Multi-level Strapping function



EC-B-17



HDCP ROM



DHCP ROM	
HDCP_SCL	Low: Crypto ROM **Hi: I2C ROM**

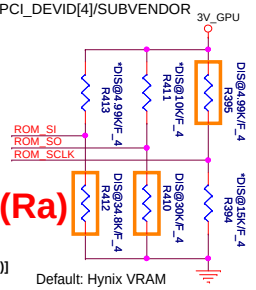
Logical Strap Bit Mapping

Rv	PU-VDD	PD-GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

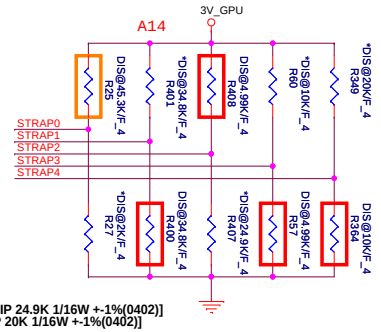
N13M-GE1

PCI_DEVID[4]/SUBVENDOR

(Ra)



Default: Hynix VRAM



4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30K/F_4: CS33002FB13 [RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4: CS33482FB22 [RES CHIP 34.8K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

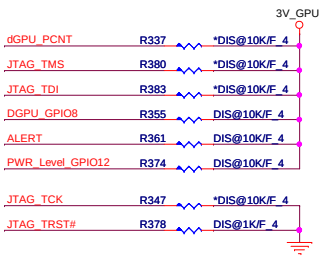
24.9K/F_4: CS32492FB16 [RES CHIP 24.9K 1/16W +-1%(0402)]
20K/F_4: CS32002FB29 [RES CHIP 20K 1/16W +-1%(0402)]

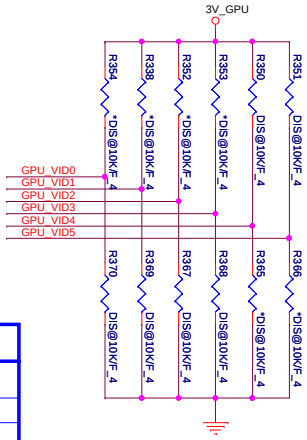
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO N13M-GE1	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0101
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V	0001

VRAM Configuration Table

(Ra)

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001		Reserved		
0010		Reserved		
0011		Reserved		
0101		Reserved		
0110		Reserved		
AKD5MGWTW00 0110	DDR3 128Mx16x4, 64bit, 1GB,900MHz	Hynix	H5TQ2G63BFR-11C	PD 34.8K/F
AKD5MGWT500 0111	DDR3 128Mx16x4, 64bit, 1GB,900MHz	Samsung	K4W2G1646C-HC11	PD 45.3K/F





GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	O	Panel Power Enable
GPIO4	LCD_BLEN	O	Panel Backlight Enable
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC Power Detect Input. High = AC, Low= Battery
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	MEM_VDD_CTL	O	Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

NVVDD Table

N13M-GE1 (GF119)	NVVDD (0.875V)
GPU_VID0	0 (R370)
GPU_VID1	0 (R369)
GPU_VID2	0 (R367)
GPU_VID3	0 (R368)
GPU_VID4	1 (R350)
GPU_VID5	1 (R351)

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Quanta Computer Inc.

Size	Document Number	Rev
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CHANNEL A: 1024MB DDR3

[15,16,20,46] 1.5V_GPU

[16,20] VMA_DQ[63..0]
[16,20] VMA_DM[7..0]
[16,20] VMA_WDQS[7..0]
[16,20] VMA_RDQS[7..0]
[16,20] FBA_CMD[30..0]

U8

VREFC_VMA1 M8 VREFCA
VREFD_VMA1 H1 VREFDQ

FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

DQL0 E3 VMA_DQ20
DQL1 F7 VMA_DQ18
DQL2 F2 VMA_DQ23
DQL3 F8 VMA_DQ19
DQL4 H3 VMA_DQ21
DQL5 H8 VMA_DQ17
DQL6 G2 VMA_DQ22
DQL7 H7 VMA_DQ16

DQU0 D7 VMA_DQ6
DQU1 C3 VMA_DQ7
DQU2 C8 VMA_DQ2
DQU3 C2 VMA_DQ4
DQU4 A7 VMA_DQ1
DQU5 A2 VMA_DQ3
DQU6 B8 VMA_DQ0
DQU7 A3 VMA_DQ5

FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
BA0 BA1 BA2

1.5V_GPU
VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9

VMA_CLK0 J7
VMA_CLK0# K7
FBA_CMD3 K9
CK CK CKE

1.5V_GPU
FBA_CMD2 K1
FBA_CMD0 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3
ODT CS RAS CAS WE

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VMA_WDQS2 F3
VMA_RDQS2 G3
DQSL DQSL

VMA_DM2 E7
VMA_DM0 D3
DML DMU

VMA_WDQS0 C7
VMA_RDQS0 B7
DQSU DQSU

FBA_CMD5 T2
RESET

VMA_ZQ1 L8
ZQ

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

96-BALL SDRAM DDR3
DIS@VRAM _DDR3

VMA_CLK0
R437
DIS@162/F_4
VMA_CLK0#

[16] VMA_CLK0
[16] VMA_CLK0#

Should be 240 Ohms +-1%
R111
DIS@240/F_4

U27

VREFC_VMA1 M8 VREFCA
VREFD_VMA1 H1 VREFDQ

FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

DQL0 E3 VMA_DQ8
DQL1 F7 VMA_DQ12
DQL2 F2 VMA_DQ9
DQL3 F8 VMA_DQ15
DQL4 H3 VMA_DQ11
DQL5 H8 VMA_DQ13
DQL6 G2 VMA_DQ10
DQL7 H7 VMA_DQ14

DQU0 D7 VMA_DQ28
DQU1 C3 VMA_DQ29
DQU2 C8 VMA_DQ26
DQU3 C2 VMA_DQ25
DQU4 A7 VMA_DQ27
DQU5 A2 VMA_DQ31
DQU6 B8 VMA_DQ24
DQU7 A3 VMA_DQ30

FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
BA0 BA1 BA2

1.5V_GPU
VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9

VMA_CLK0 J7
VMA_CLK0# K7
FBA_CMD3 K9
CK CK CKE

1.5V_GPU
FBA_CMD2 K1
FBA_CMD0 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3
ODT CS RAS CAS WE

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VMA_WDQS1 F3
VMA_RDQS1 G3
DQSL DQSL

VMA_DM1 E7
VMA_DM3 D3
DML DMU

VMA_WDQS3 C7
VMA_RDQS3 B7
DQSU DQSU

FBA_CMD5 T2
RESET

VMA_ZQ2 L8
ZQ

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

96-BALL SDRAM DDR3
DIS@VRAM _DDR3

Should be 240 Ohms +-1%
R443
DIS@240/F_4

1.5V_GPU
C561 DIS@1U/6.3V/X5R_4
C305 DIS@1U/6.3V/X5R_4
C621 DIS@1U/6.3V/X5R_4
C306 DIS@1U/6.3V/X5R_4

C307 DIS@0.1U/10V/X5R_4
C269 DIS@0.1U/10V/X5R_4
C620 DIS@0.1U/10V/X5R_4
C618 DIS@0.1U/10V/X5R_4
C271 DIS@0.1U/10V/X5R_4

1.5V_GPU
C604 DIS@1U/6.3V/X5R_4
C295 DIS@1U/6.3V/X5R_4
C609 DIS@1U/6.3V/X5R_4
C308 DIS@1U/6.3V/X5R_4

C303 DIS@0.1U/10V/X5R_4
C567 DIS@0.1U/10V/X5R_4
C617 DIS@0.1U/10V/X5R_4
C122 DIS@0.1U/10V/X5R_4
C252 DIS@0.1U/10V/X5R_4

1.5V_GPU
R465
DIS@1.33K/F_4
VREFC_VMA1
R458
DIS@1.33K/F_4
C582
DIS@0.1U/10V/X5R_4

1.5V_GPU
R487
DIS@1.33K/F_4
VREFD_VMA1
R491
DIS@1.33K/F_4
C612
DIS@0.1U/10V/X5R_4

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N13M (DDR3) 5/5	1A
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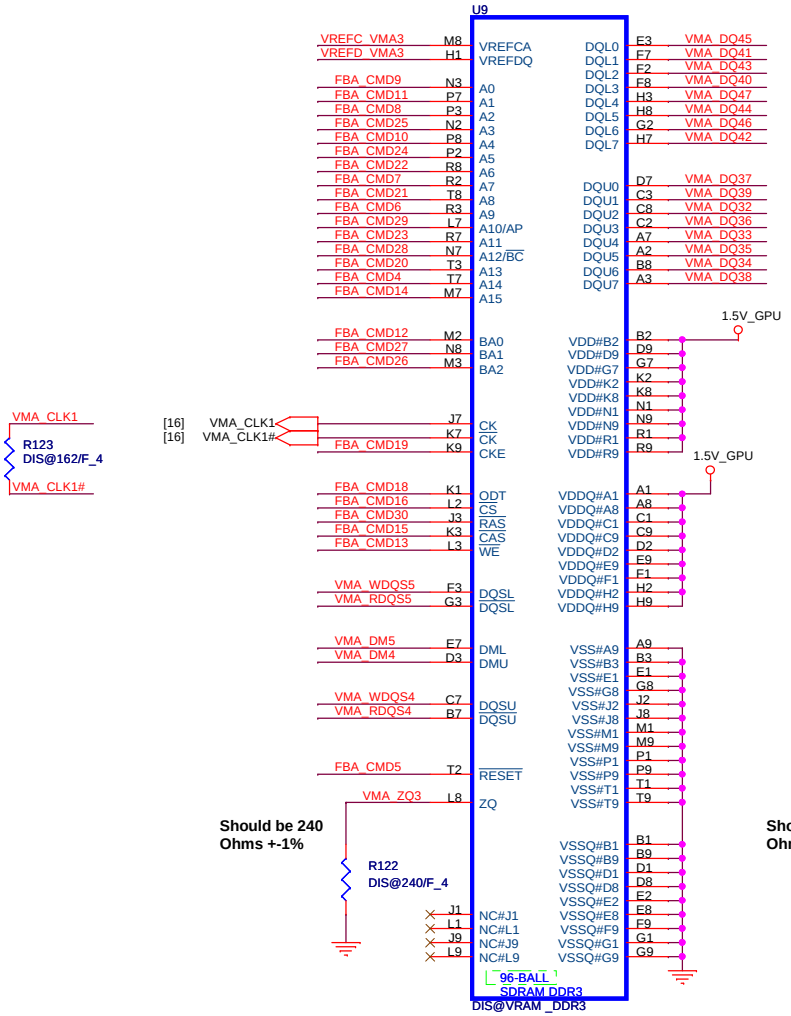
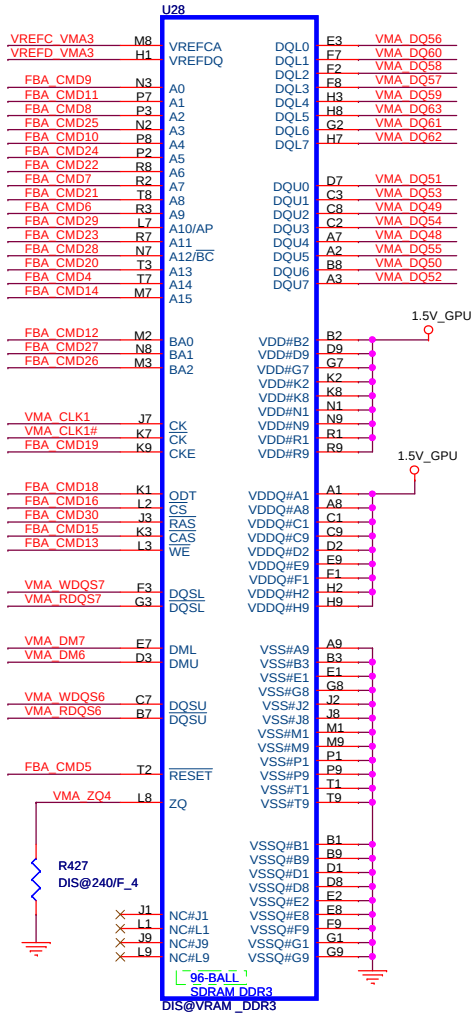
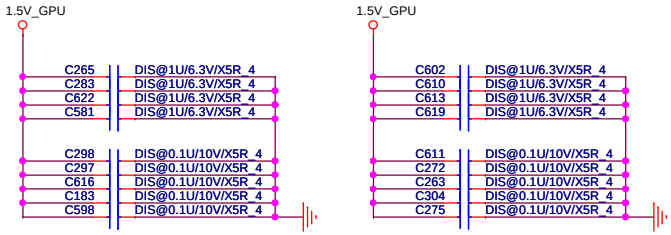
CHANNEL A: 1024MB DDR3

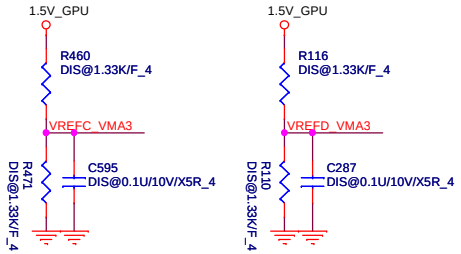
[15,16,19,46] 1.5V_GPU

[16,19] VMA_DQ[63..0]
[16,19] VMA_DM[7..0]
[16,19] VMA_WDQS[7..0]
[16,19] FBA_CMD[30..0]
[16,19] VMA_RDQS[7..0]









PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N13M (DDR3) 6/6	1A
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PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Blank	1A

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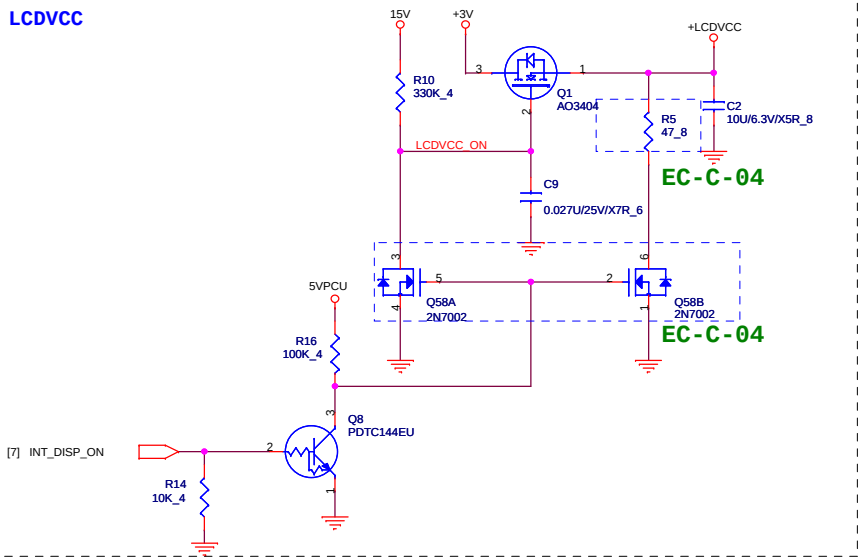
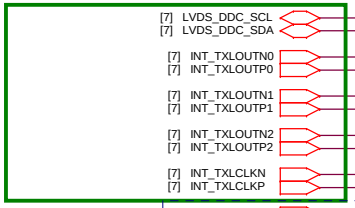
+3V [3,7,8,9,10,11,13,14,15,23,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
3VPCU [7,8,25,30,31,34,35,36,37,38,39,43,45]
15V [37,39,40,46]
VIN [36,38,39,40,41,42,44,45]
5VPCU [11,36,37,39,40,41,42,43,44,45,46]

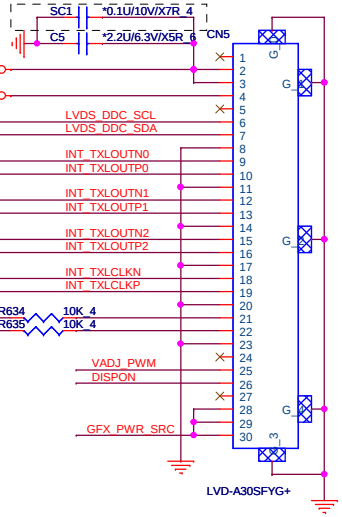
LCDVCC

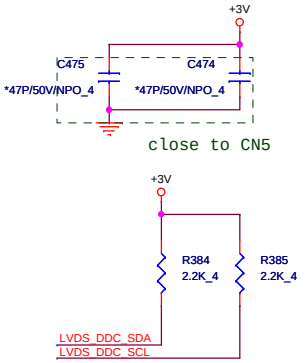


EC-B-22



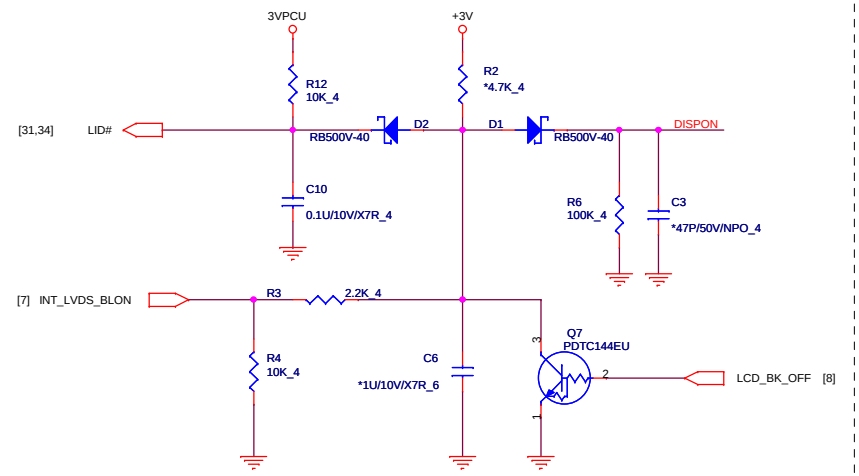
For ESD

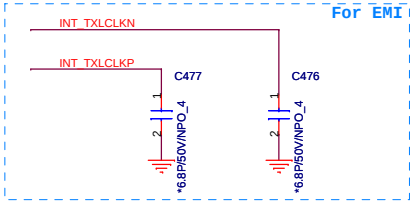




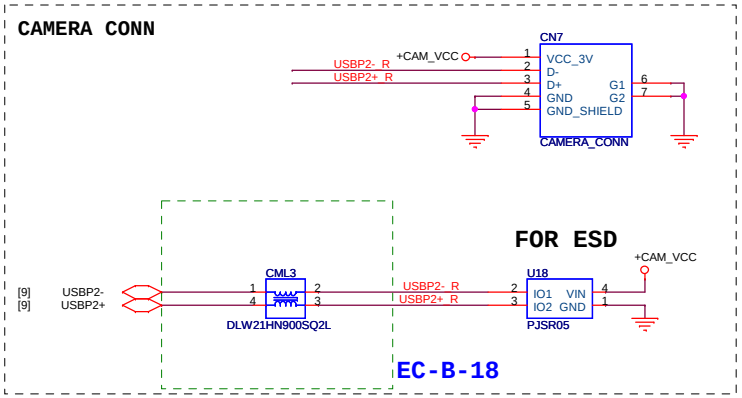
LVDS (14") (1024x600, 1366x768)

Back light

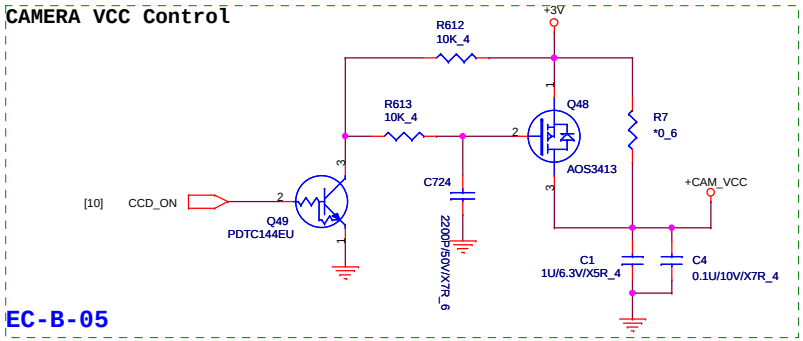




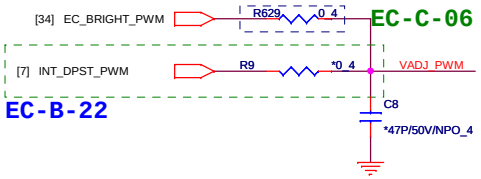
CAMERA CONN

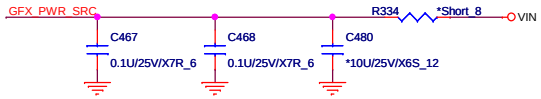


CAMERA VCC Control



EC-B-22





PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	LCD/CAMERA	3A
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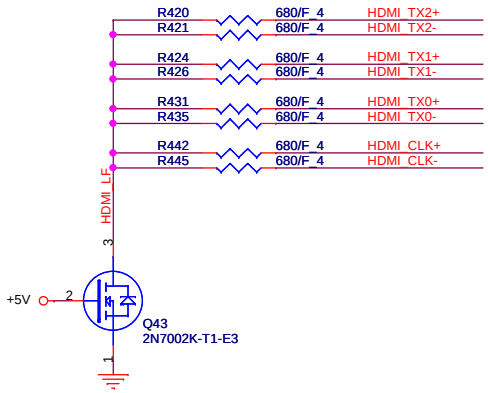
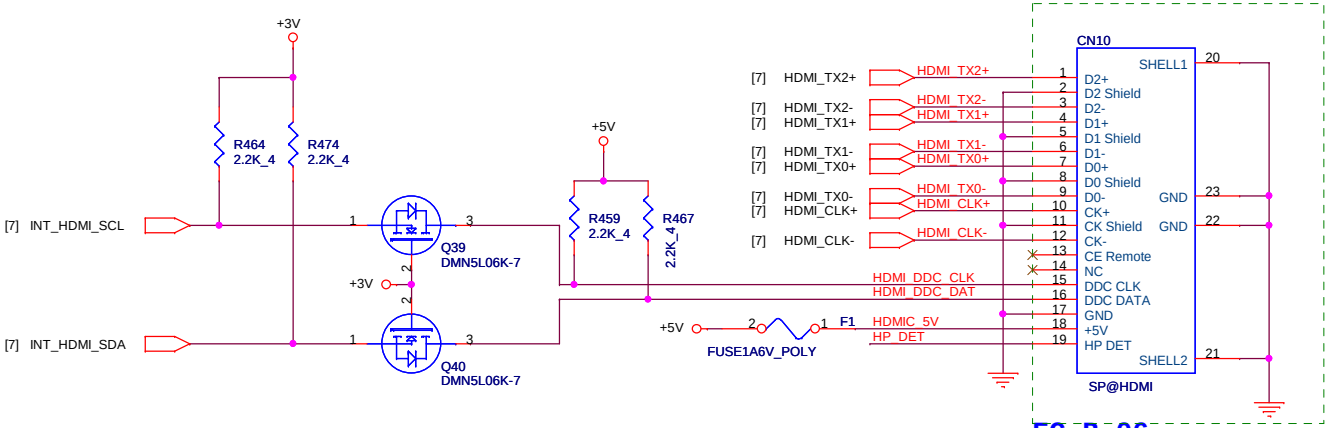
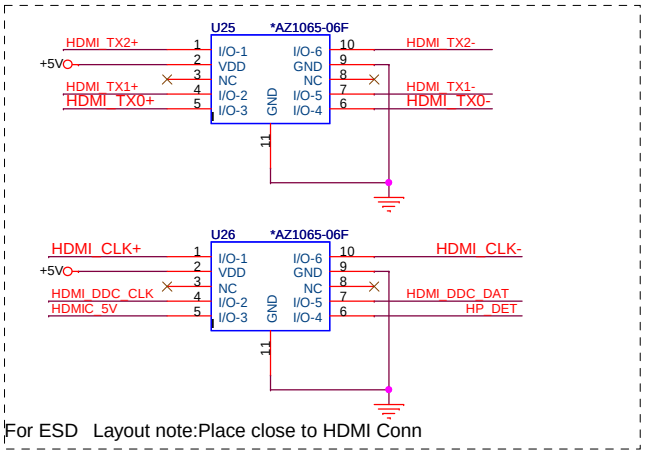
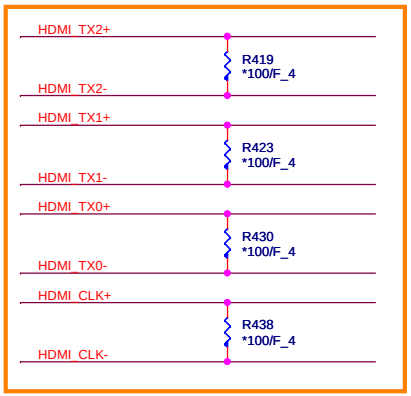
[3,7,8,9,10,11,13,14,15,22,24,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46] +3V
[8,11,24,26,33,36,37,38] +5V

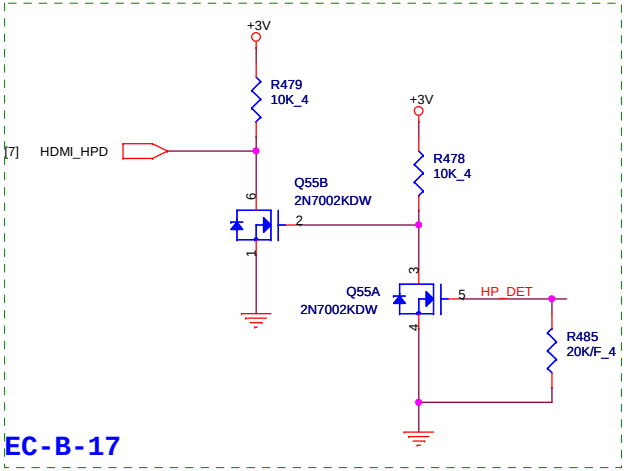


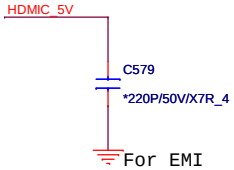




EMI reserve for HDMI







PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

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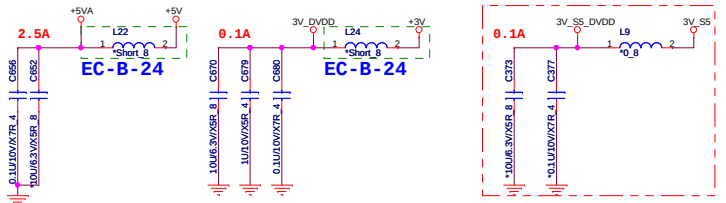
+3V [3,7,8,9,10,11,13,14,15,22,23,25,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
+5V [8,11,23,26,33,36,37,38]
3V_S5 [3,7,8,9,10,11,30,35,37]

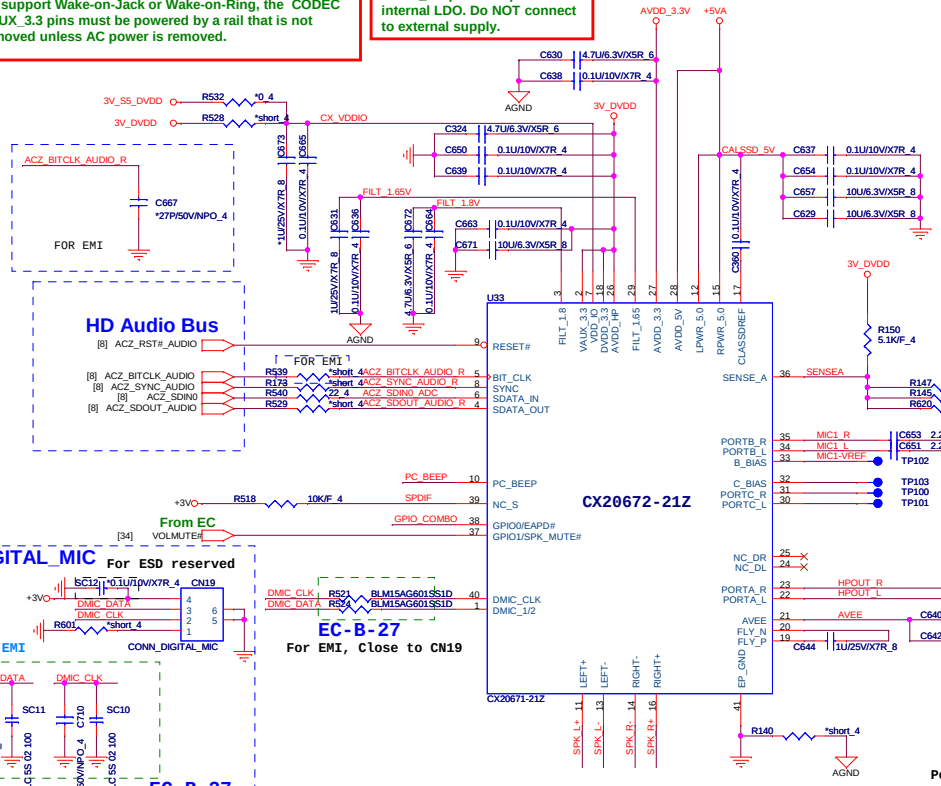
Note:
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

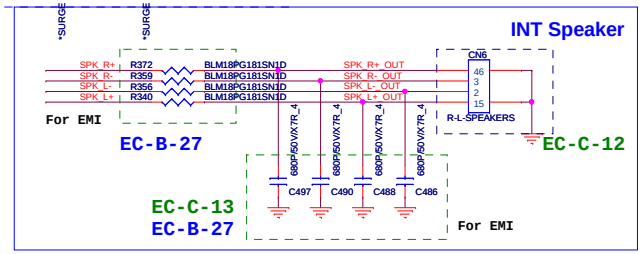
AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

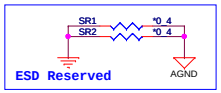
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.



Conexant FAE Suggest when use intel HDA interface

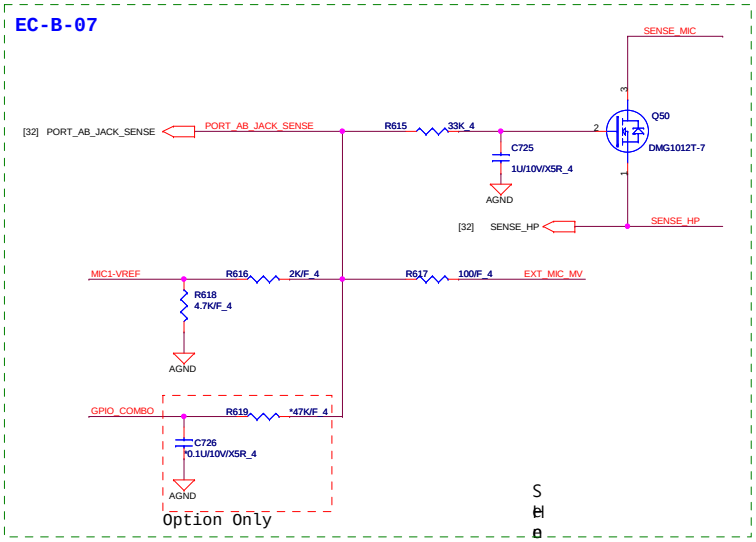


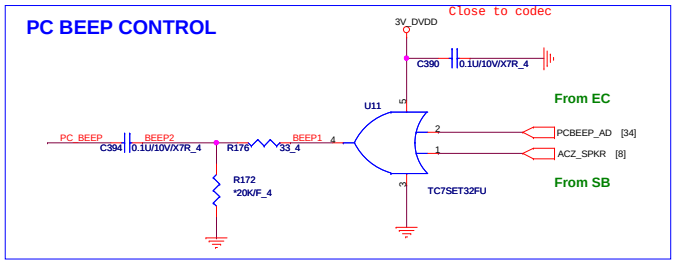


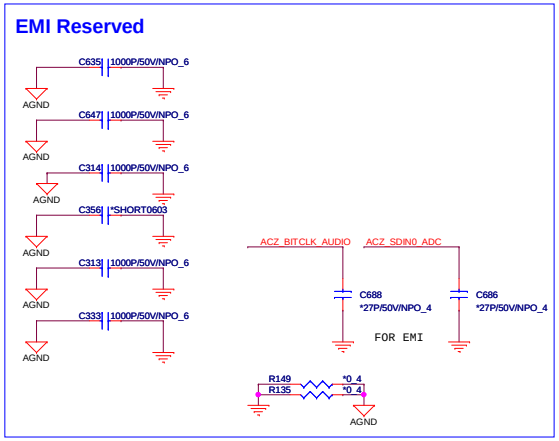


Port Configuration

Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono or stereo MIC.
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Optional Internal stereo digital mic
Port H: S/PDIF (jack shared with headphone)







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Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO CODEC CX20672	2A
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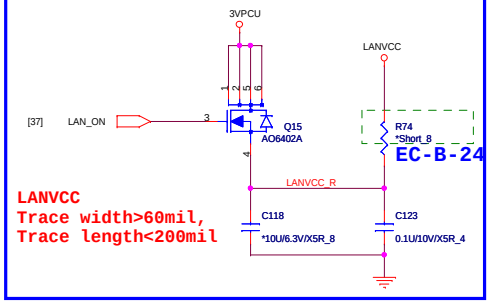
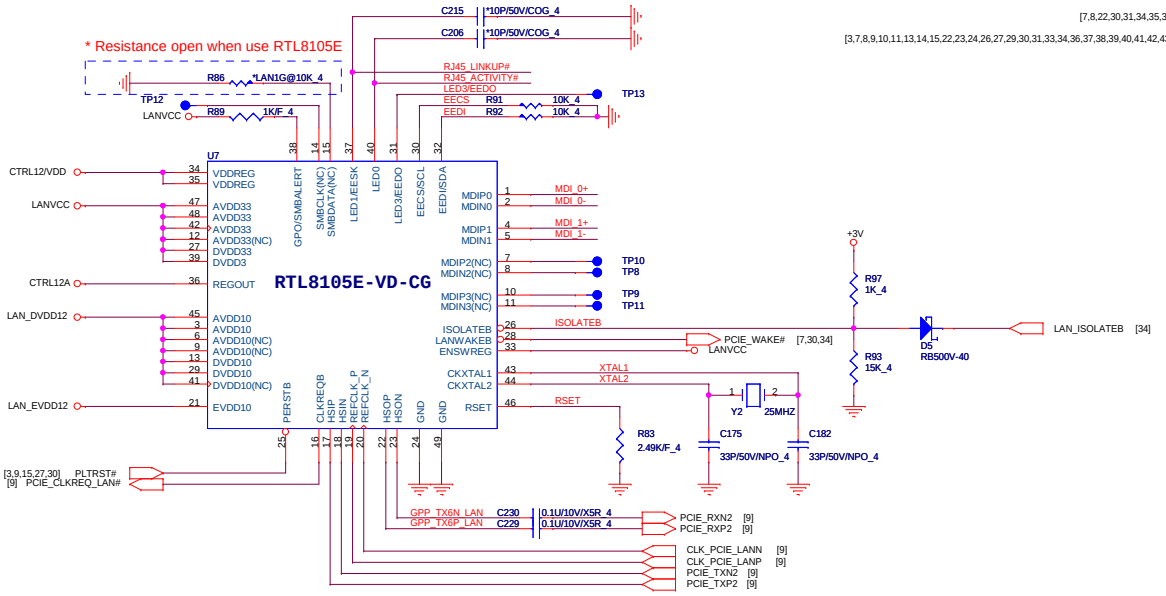
LANVCC

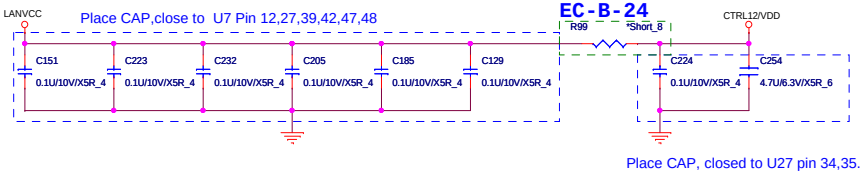


LANVCC
Trace width>60mil,
Trace length<200mil

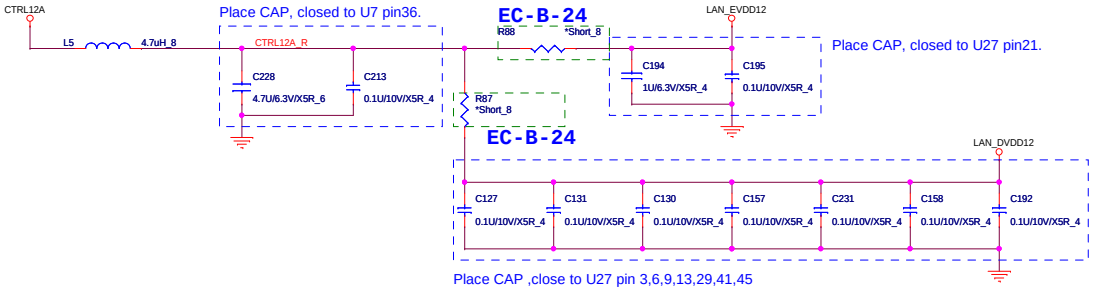
* Resistance open when use RTL8105E



[7,8,22,30,31,34,35,36,37,38,39,43,45] [37] 3VPCU LANVCC +3V
[3,7,8,9,10,11,13,14,15,22,23,24,26,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

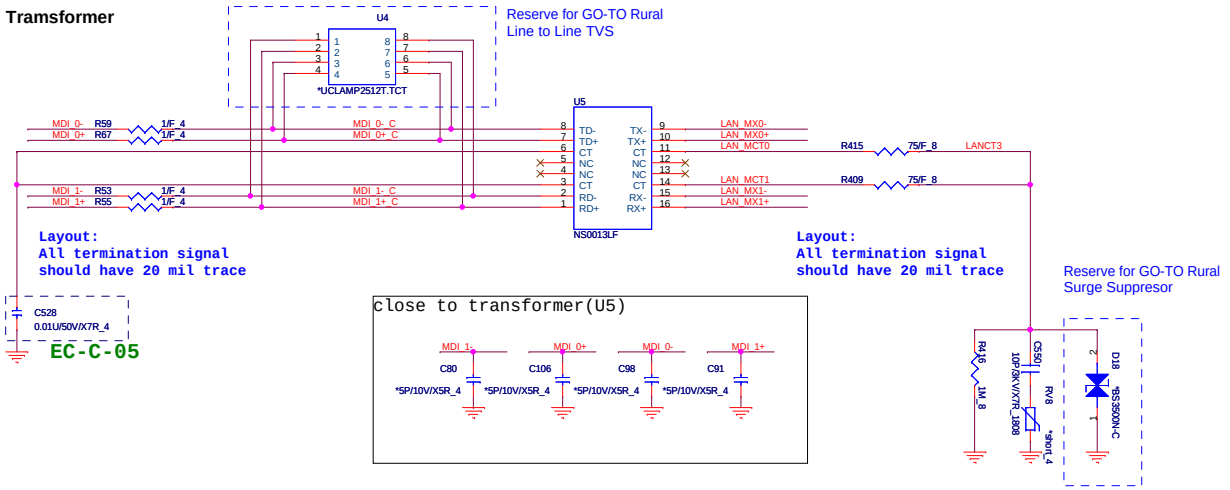


Place CAP, closed to U27 pin 34,35.

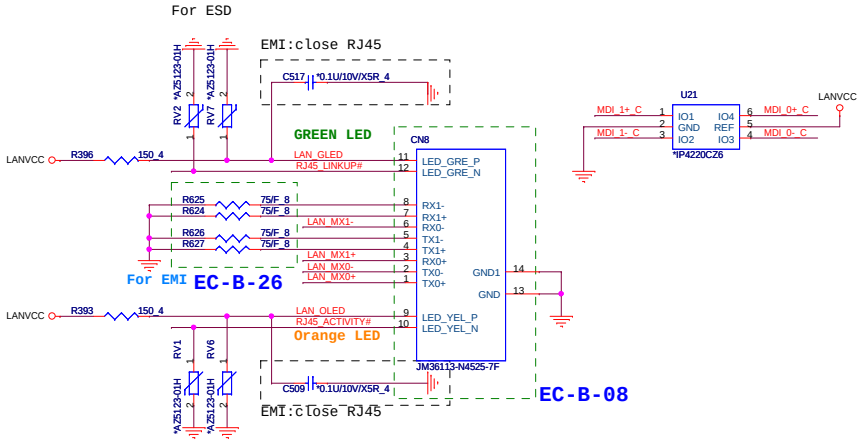


Place CAP ,close to U27 pin 3,6,9,13,29,41,45

Tramsformer



RJ45 Connector



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Quanta Computer Inc.		
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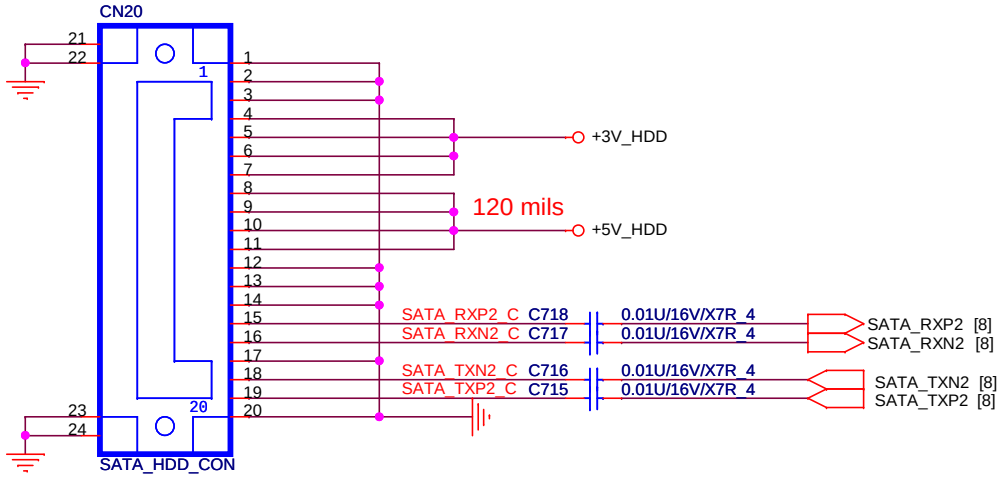
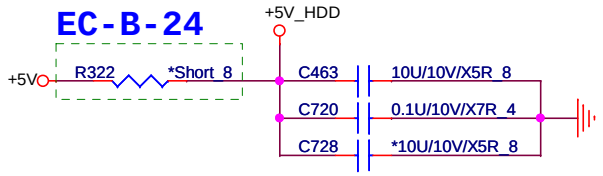
HDD

PLACE SATA AC COUPLING
CAPS CLOSE TO Connector

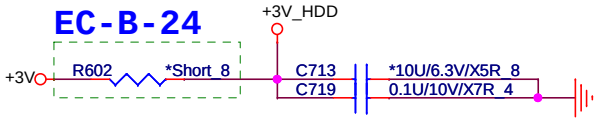
+3V [3,7,8,9,10,11,13,14,15,22,23,24,25,27,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]
+5V [8,11,23,24,33,36,37,38]



DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

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	SATA	1A
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AU6435-GDL CARD READER Controller

[3,7,8,9,10,11,13,14,15,22,23,24,25,26,29,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46]

+3V

R277	0	Normal mode
	1	Saving mode

option for power reset or system reset

EC-C-01

EC-B-24

EC-B-24

EC-B-21

2 IN 1 CARD READER (SD/MMC)

QCI P/N : DFHD14MS009

TTN P/N : PSDBT4-09GLAG1004N1

Main	DFHD14MS009
Second	

CTRL0, CRTL 1 trace length shorter , and surround with GND.

Close to CNxx Pin 6

crystal trace width needs at least 10 mils.

close PIN11, 12 pin13 output 20mils

SD write protect
1:decided by SDWP[Default]
0:letting SD always write-able

Clock input selection
'1' for 48MHz input [Default]
'0' for 12MHz input

for EMI

PSDBT4-09GLAG1004N1

AU6435-GDL

PROJECT	LZ8 Chief River DIS
Quanta Computer Inc.	
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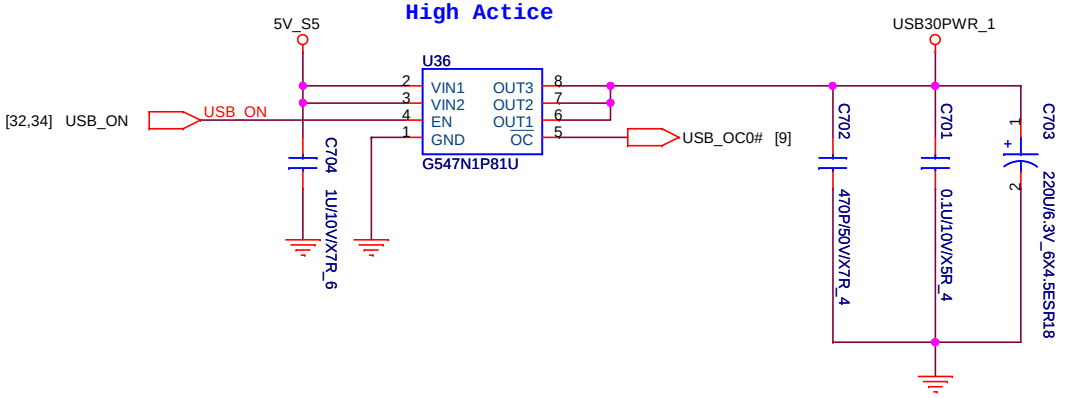
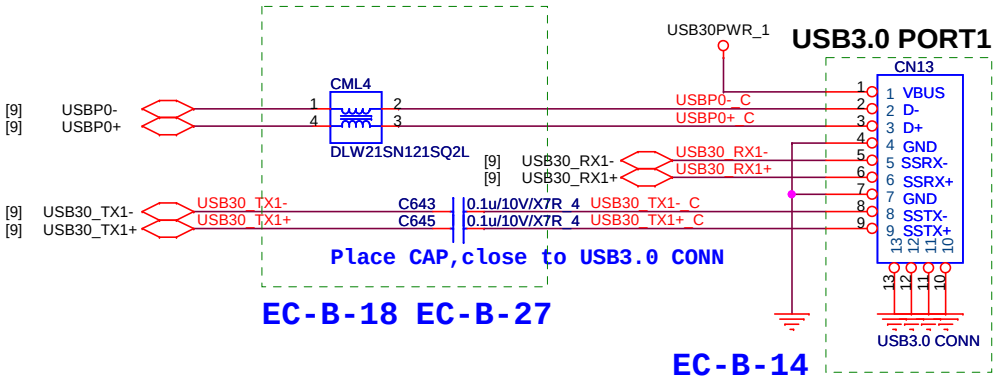
5V_S5 [11,32,37]

150 mils (Iout=3.5A)

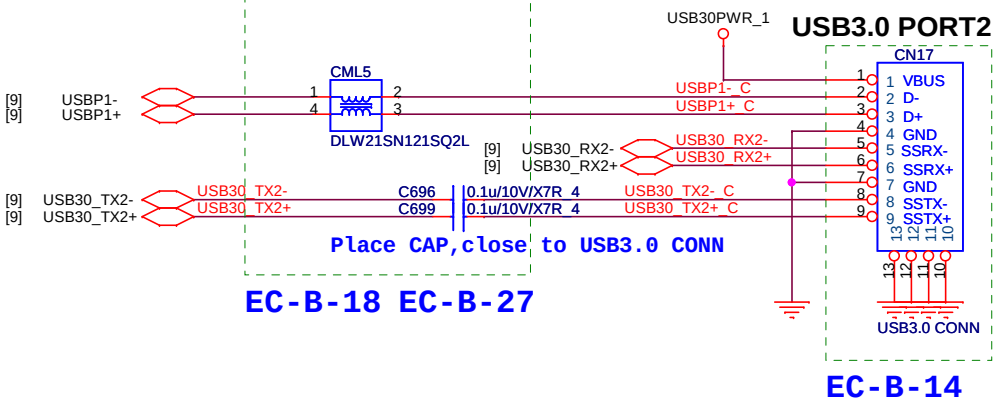
High Actice

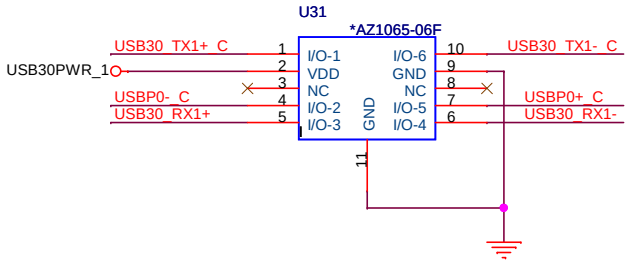


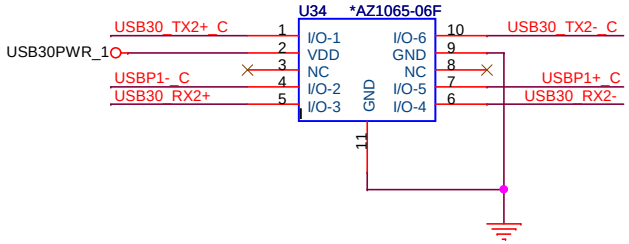
USB3.0 PORT1



USB3.0 PORT2







PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	USB3.0 x2	2A
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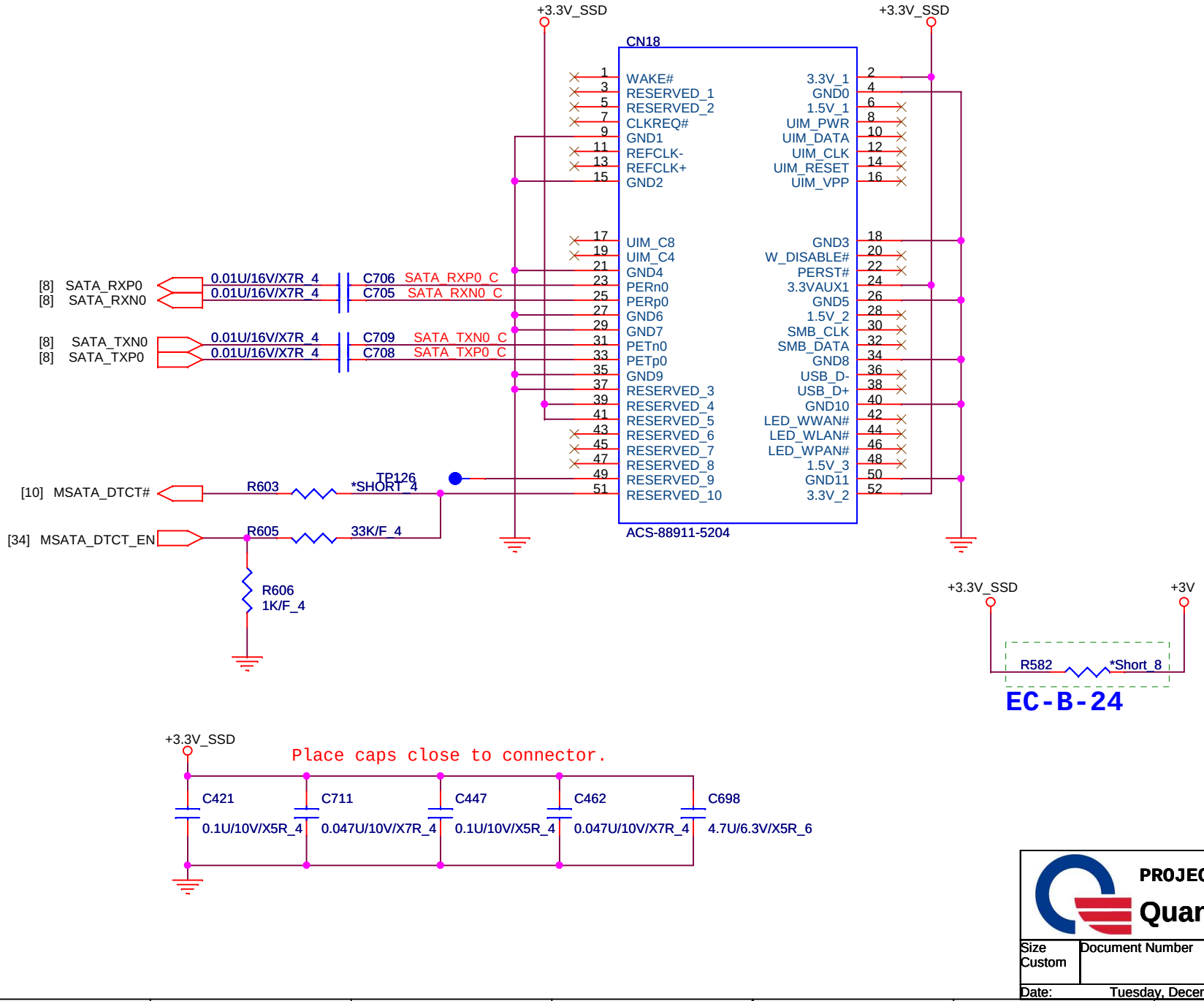
SSD

[3,7,8,9,10,11,13,14,15,22,23,24,25,26,27,30,31,33,34,36,37,38,39,40,41,42,43,44,45,46] +3V



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

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Custom	MINI Card (SSD)	1A
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MiniCard WLAN connector

PCI-Express TX and RX direct to connector

CN9

ACS-88911-5204

EC-B-22

EC-B-01

EC-B-13

EC-B-13

AOAC

Place caps close to connector.

close to CN22

close to CN22

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	WLAN	2A

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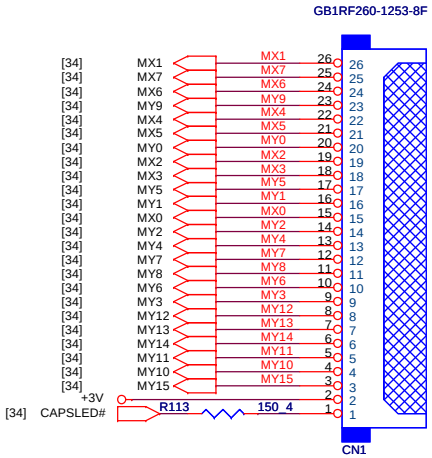
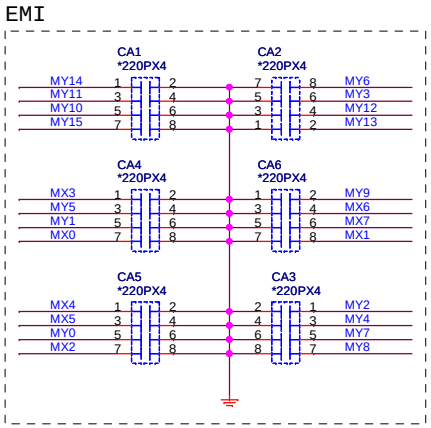
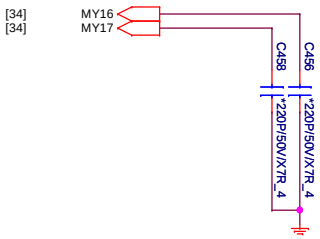
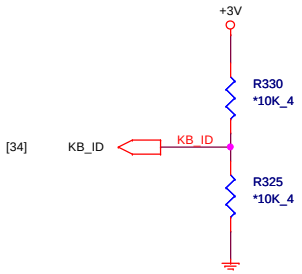
KEYBOARD

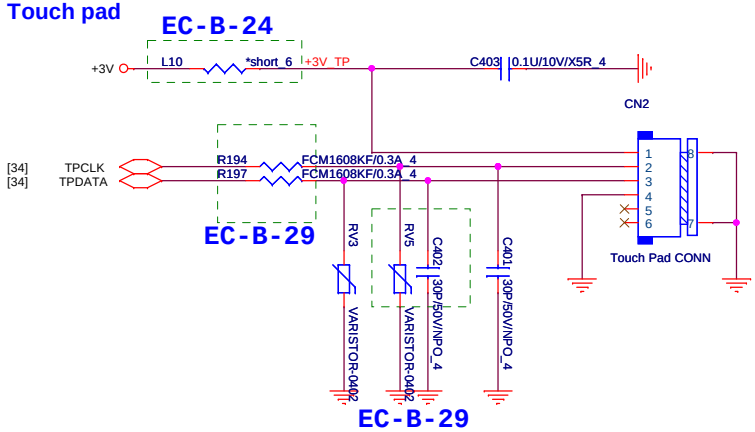




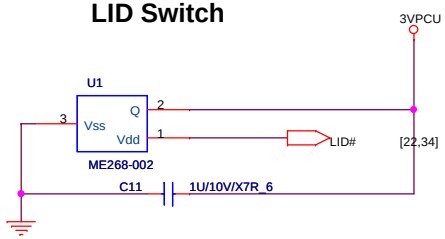




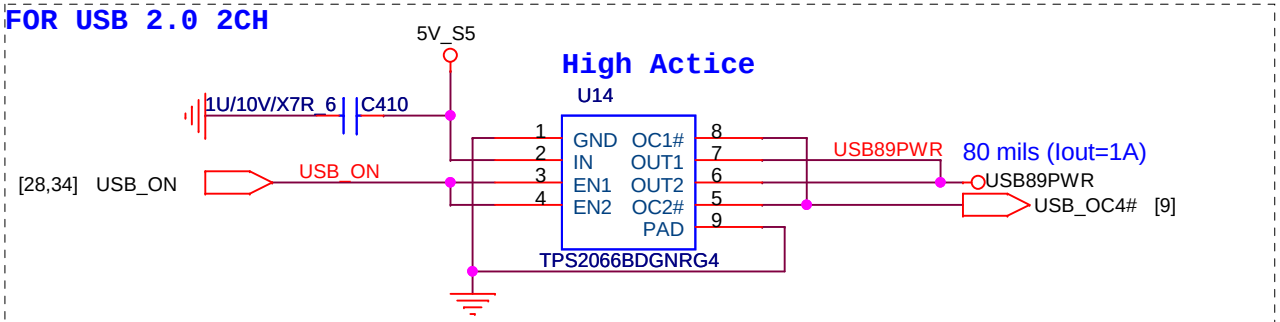
Touch pad

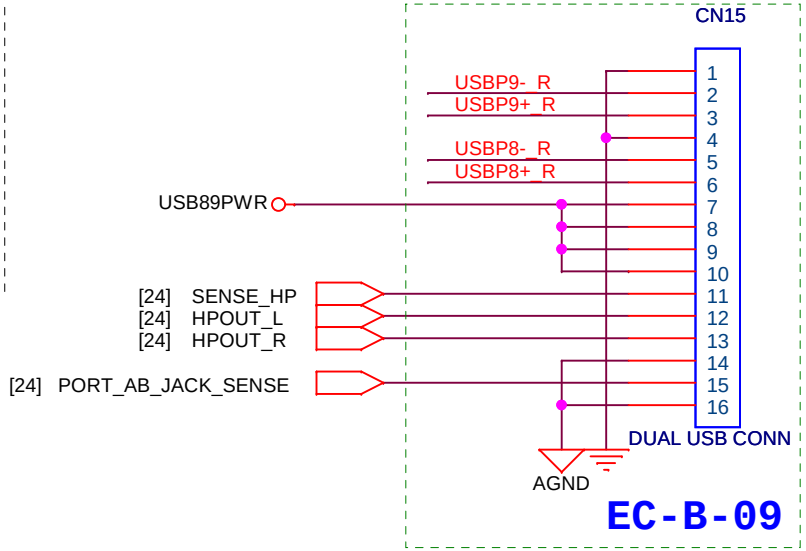


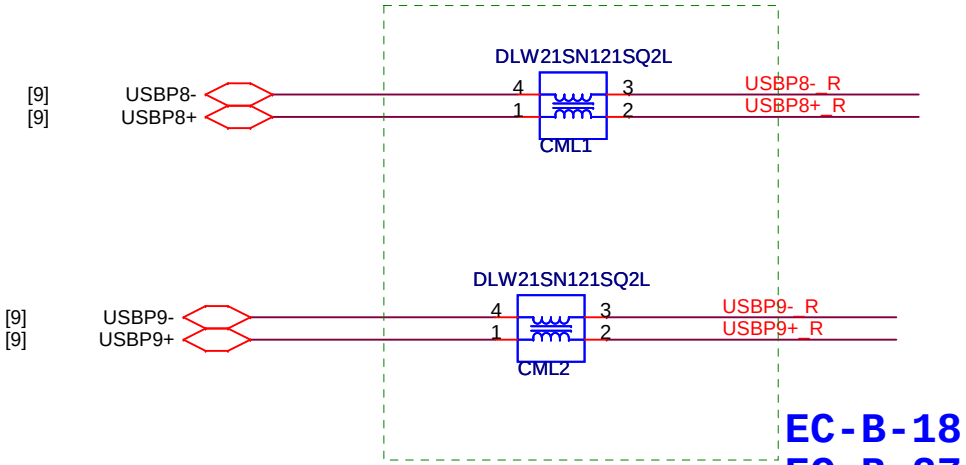
LID Switch



PROJECT LZ8 Chief River DIS		
Quanta Computer Inc.		
Size	Document Number: KB/TP/LID	Rev: 1A
Date: Tuesday, December 20, 2011	Sheet 31 of 49	







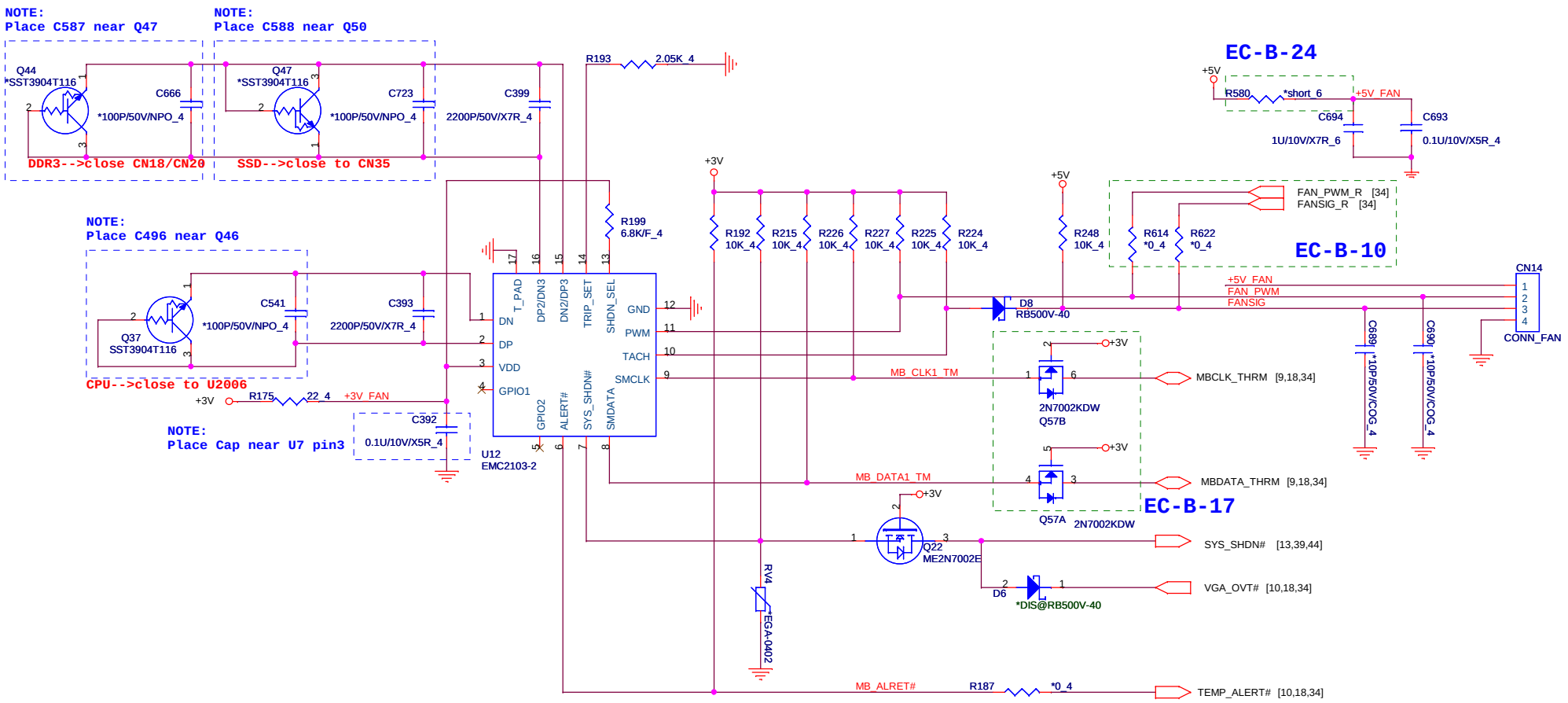
PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

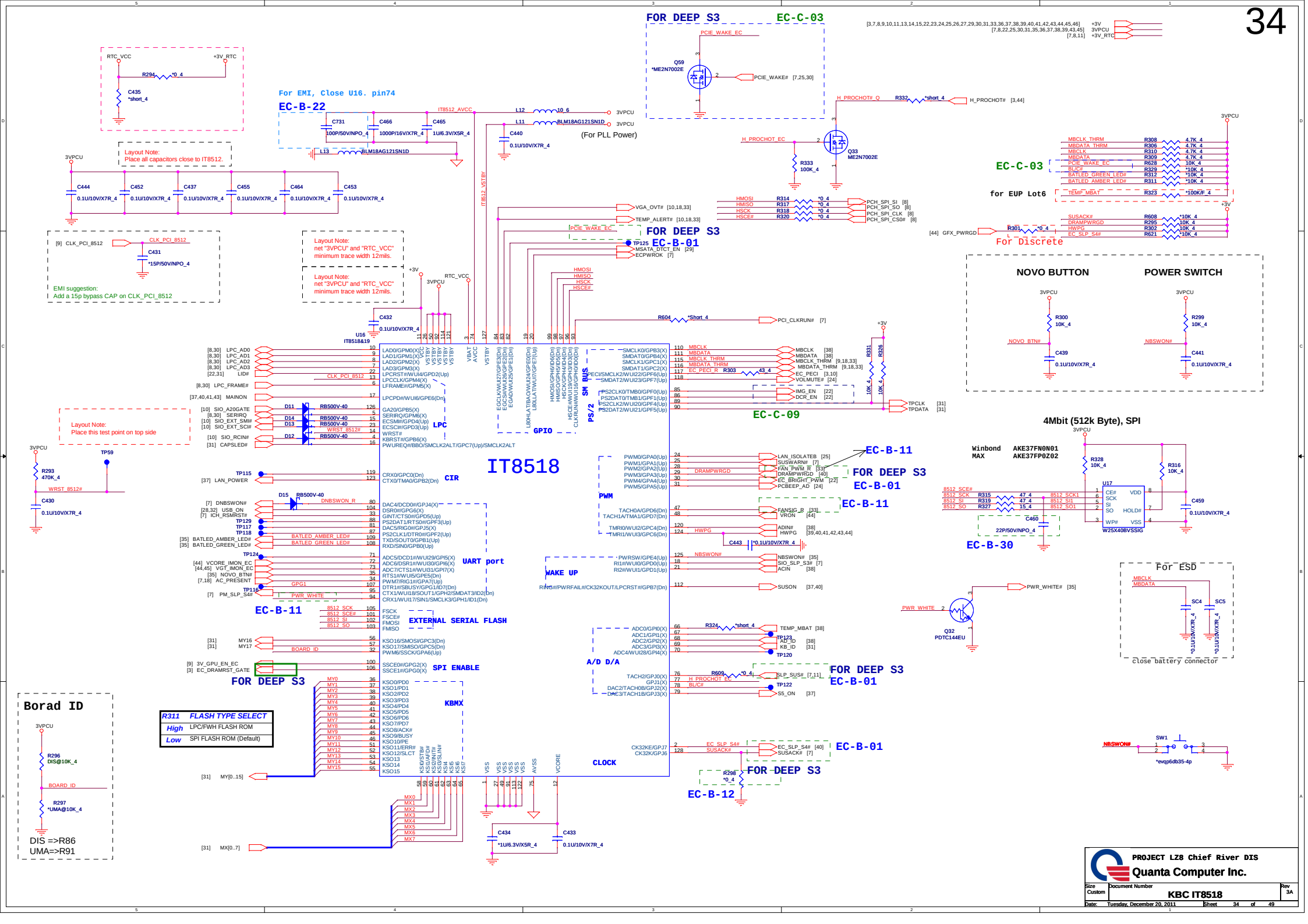
Size	Document Number	Rev
	USB2.0--Audio Jack Conn	3A
Date: Tuesday, December 20, 2011	Sheet 32 of 49	

FAN CONTROL

[3,7,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,34,36,37,38,39,40,41,42,43,44,45,46] +3V
[8,11,23,24,26,36,37,38] +5V

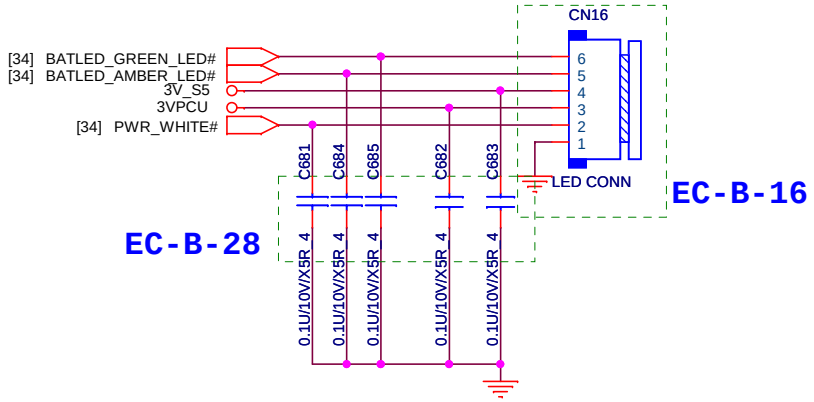


PROJECT LZ8 Chief River DIS		
Quanta Computer Inc.		
Size	Document Number: FAN/Thermal	Rev: 2A
Date: Tuesday, December 20, 2011	Sheet 33 of 49	

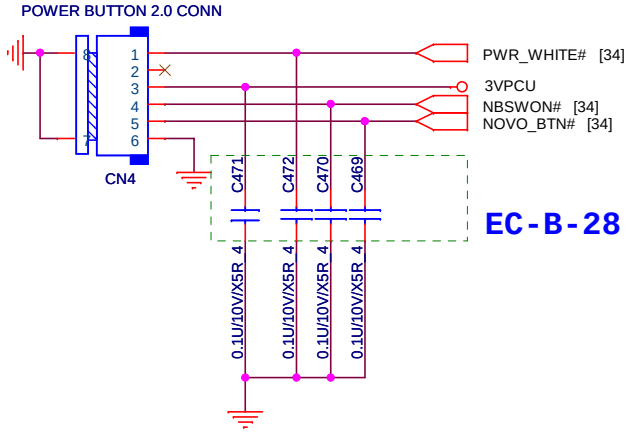

IT8518
FOR DEEP S3
EC-C-03
EC-B-22
EC-B-01
EC-C-09
EC-B-11
EC-B-30
EC-B-12
For EMI, Close U16. pin74
(For PLL Power)
for EUP Lot6
For Discrete
NOVO BUTTON
POWER SWITCH
4Mbit (512k Byte), SPI
Winbond AKE37FN0N01
MAX AKE37FP0Z02
LPC
GPIO
SM BUS
PS/2
CIR
UART port
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
PWM
WAKE UP
A/D D/A
CLOCK
Borad ID
DIS =>R86
UMA=>R91
R311 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
Layout Note: Place all capacitors close to IT8512.
Layout Note: Place this test point on top side
Layout Note: net "3VPCU" and "RTC_VCC" minimum trace width 12mils.
Layout Note: net "3VPCU" and "RTC_VCC" minimum trace width 12mils.
EMI suggestion: Add a 15p bypass CAP on CLK_PCI_8512
For ESD
close battery connector
PROJECT LZ8 Chief River DIS
Quanta Computer Inc.
KBC IT8518
Tuesday, December 20, 2011

3VPCU [7,8,22,25,30,31,34,36,37,38,39,43,45]
3V_S5 [3,7,8,9,10,11,24,30,37]

LED Conn



POWER BUTTON/NOVO Button



PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	SW/LED/RFID_EEPROM	2A
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Hole for CPU support

HOLE13 *H-C181D181N
HOLE12 *H-TC217BIC142D142N
HOLE10 *H-TC236BIC142D142N
HOLE9 *H-C142D142N

MiniCard WWAN

HOLE14 H-TC217BIC142D102P2

MiniCard WLAN

HOLE11 H-TC217BIC142D102P2

SPAD3 *SPAD-LZ8-2
SPAD4 *SPAD-LZ8-3
HOLE15 *H-TBR315X350I178D98P2

Hole for GPU support

HOLE4 *H-C142D142N
HOLE5 *H-TC236BIC142D142N

Boundary Hole

HOLE8 *H-C276I146D106P2
HOLE2 *H-C276I146D106P2
HOLE1 *HG-C276I146D106P2-5
HOLE6 *HG-C276I146D106P2-5
HOLE7 *H-C86D86N

EMI

1.5V_SUS: C273 C256 C282 C270 C294 C210 C299 — 2200P/50V/X7R_4
VIN: C493 C707 C669 — 0.1U/50V/X7R_6
+3V: C67 C484 C317 C721 C482 C473 C668 C712 — 2200P/50V/X7R_4
VIN: C662 C722 C451 — 0.1U/50V/X7R_6
+5V: C34 — 1U/6.3V/X5R_4
C600 C35 C697 C646 C461 — 2200P/50V/X7R_4

3VPCU [7,8,22,25,30,31,34,35,37,38,39,43,45]

Fro ESD

+1.5V_CPU: SC2 SC3 — *0.1U/10V/X7R_4
VCC_GFX: SC7 SC6 SC9 SC8 — *0.1U/10V/X7R_4

VIN — C330 — *0.1U/10V/X7R_4 — VCC_CORE

Fro EMI

5VPCU: C319 — 1000P/50V/X7R_4; C13 — 1U/6.3V/X5R_4; C58 — 1U/6.3V/X5R_4

3VPCU: C729 — 100P/50V/NPO_4

For EMI, Close U16.PIN92

EC-B-22

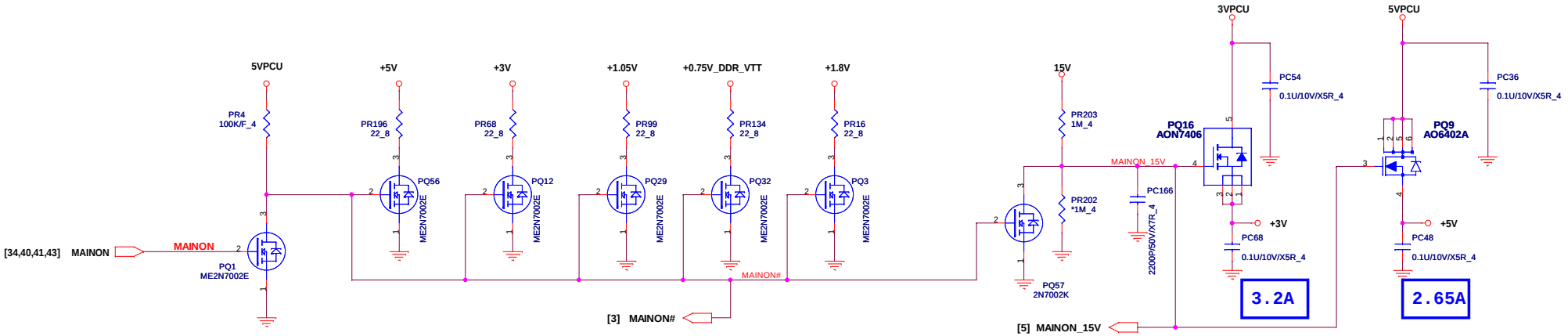
+1.5V_CPU [3,5,40]
3VPCU [7,8,22,25,30,31,34,35,37,38,39,43,45]
VCC_GFX [5,44]
+3V [3,7,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,33,34,37,38,39,40,41,42,43,44,45,46]
+5V [8,11,23,24,26,33,37,38]
1.5V_SUS [3,11,13,14,37,40,46]
5VPCU [11,22,37,39,40,41,42,43,44,45,46]
VIN [22,38,39,40,41,42,44,45]
VCC_CORE [5,6,44]
+1.05V [3,5,7,8,9,11,37,41,46]

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

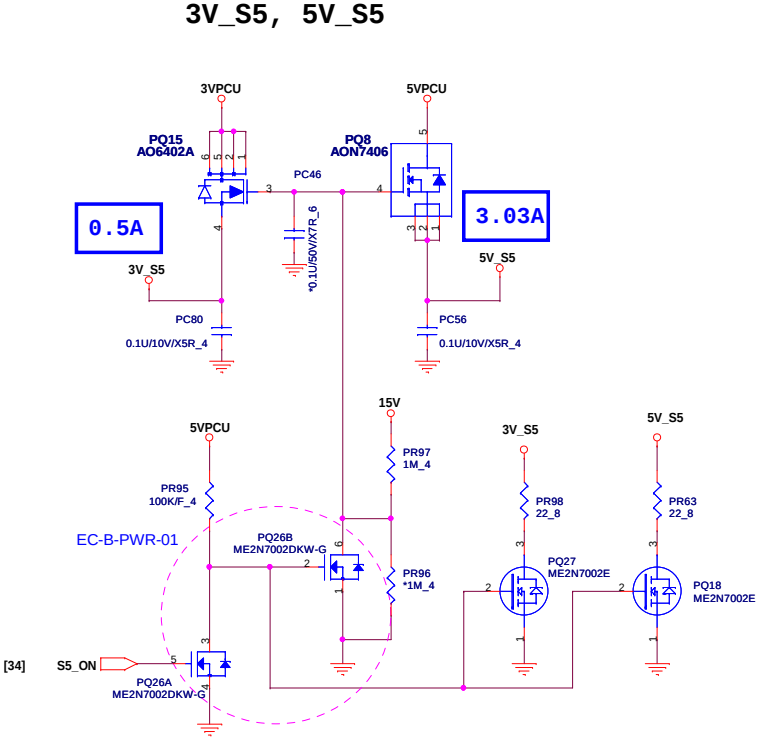
Size	Document Number	Rev
	Screw Hole/EMI	1A
Date: Tuesday, December 20, 2011	Sheet 36 of 49	

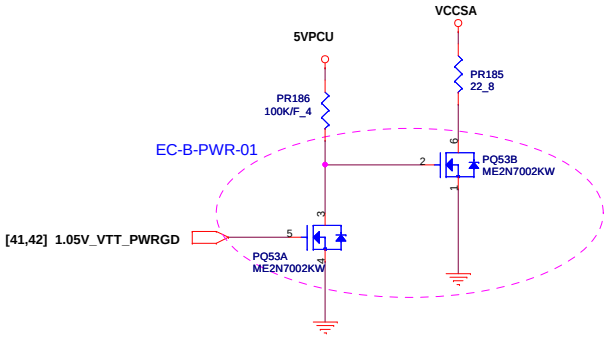
DISCHARGE

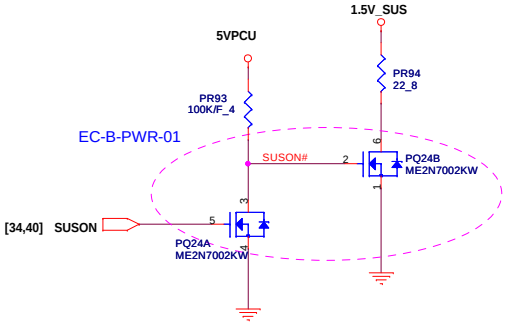
+3V, +5V,+1.5V



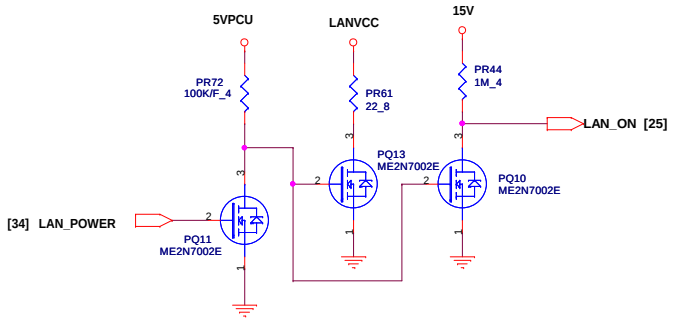
3V_S5, 5V_S5







LANVCC



PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	

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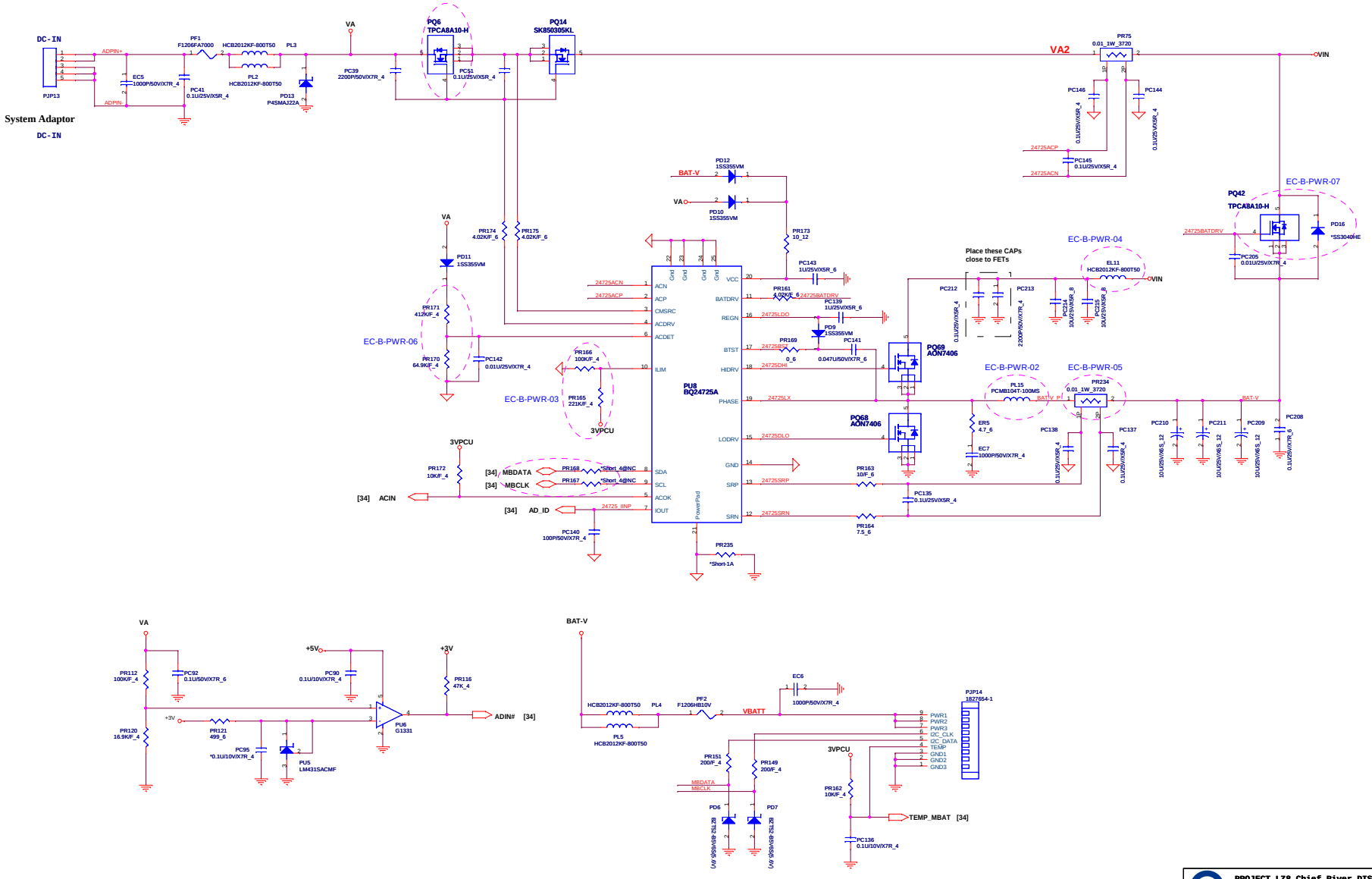
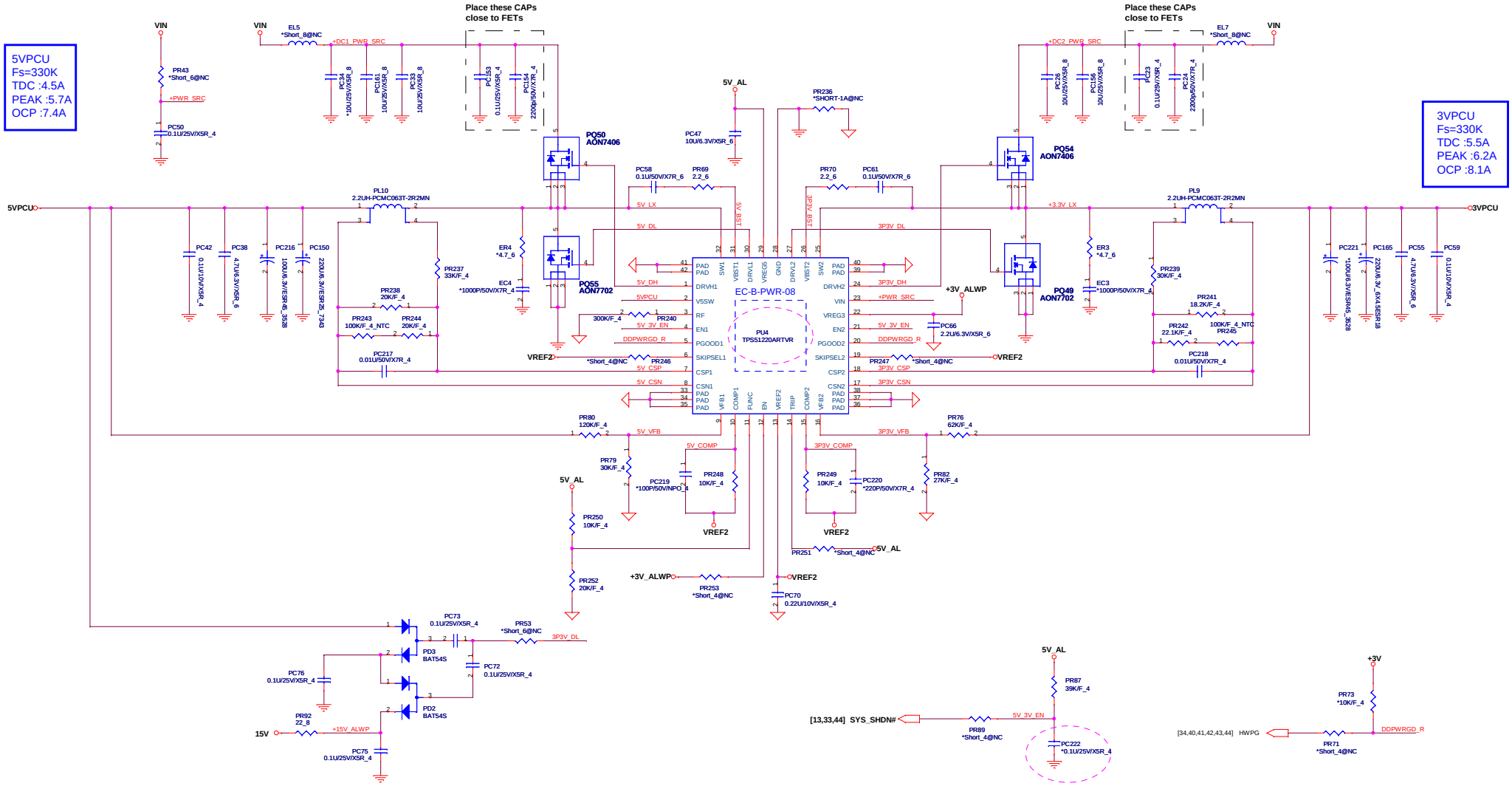


PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	CHARGER (BQ24725)	1A
Date: Tuesday, December 20, 2011	Sheet 38 of 49	


5VPCU
Fs=330K
TDC :4.5A
PEAK :5.7A
OCP :7.4A
3VPCU
Fs=330K
TDC :5.5A
PEAK :6.2A
OCP :8.1A
Place these CAPs close to FETs
Place these CAPs close to FETs
PU4 TPS51220ARTVR
EC-B-PWR-08
PQ50 AON7406
PQ55 AON7702
PQ54 AON7406
PQ49 AON7702
PL10 2.2UH-PCMC063T-2R2MN
PL9 2.2UH-PCMC063T-2R2MN
VIN
5V_AL
+3V_ALWP
VREF2
15V
+3V
[13,33,44] SYS_SHDN#
[34,40,41,42,43,44] HWPG
PROJECT Z Plus Chief River DIS
Quanta Computer Inc.
Document Number
3V/5V (TPS51220ARTVR)
Rev 1A
Date: Tuesday, December 20, 2011
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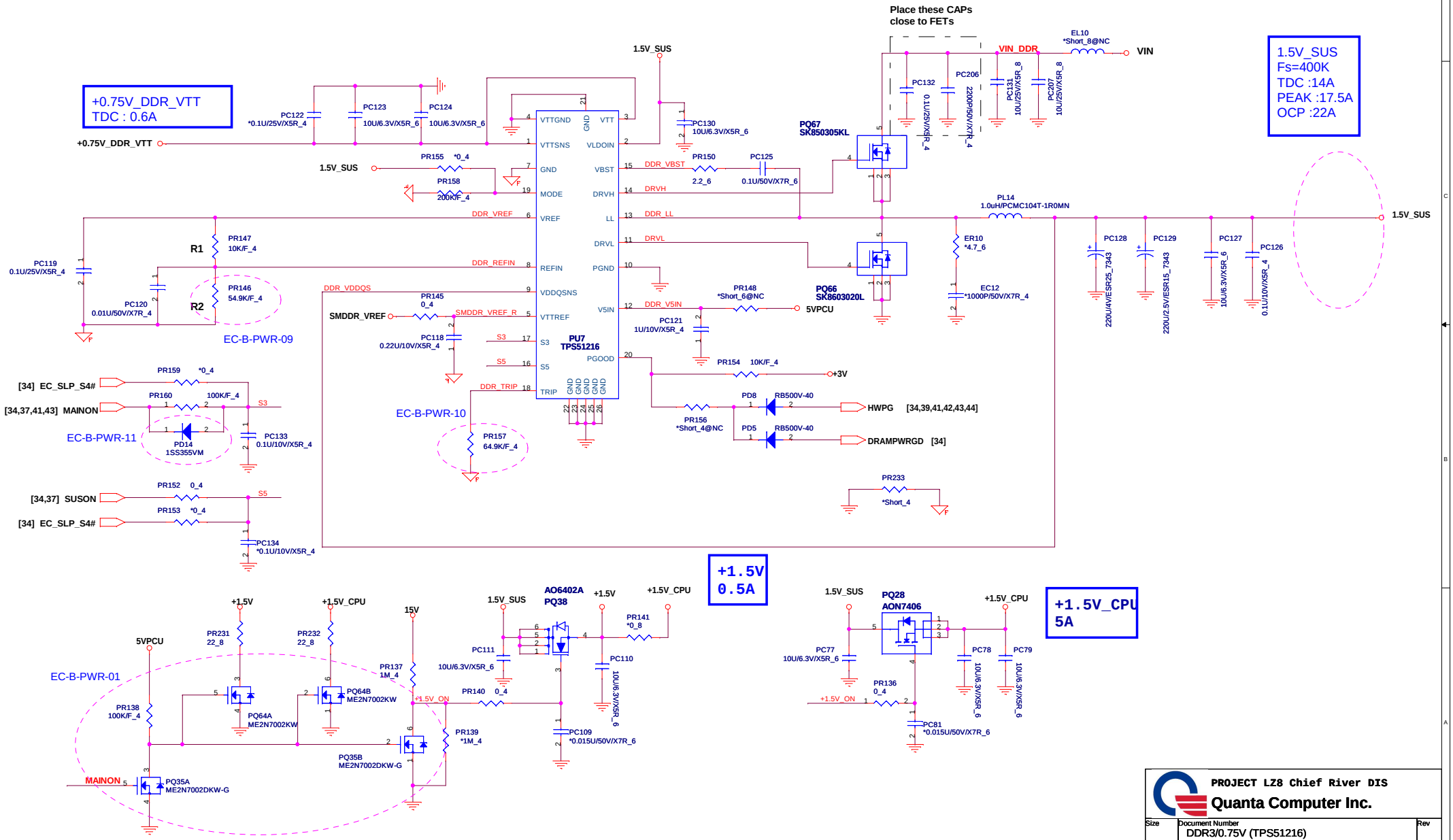

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	DDR3/0.75V (TPS51216)	

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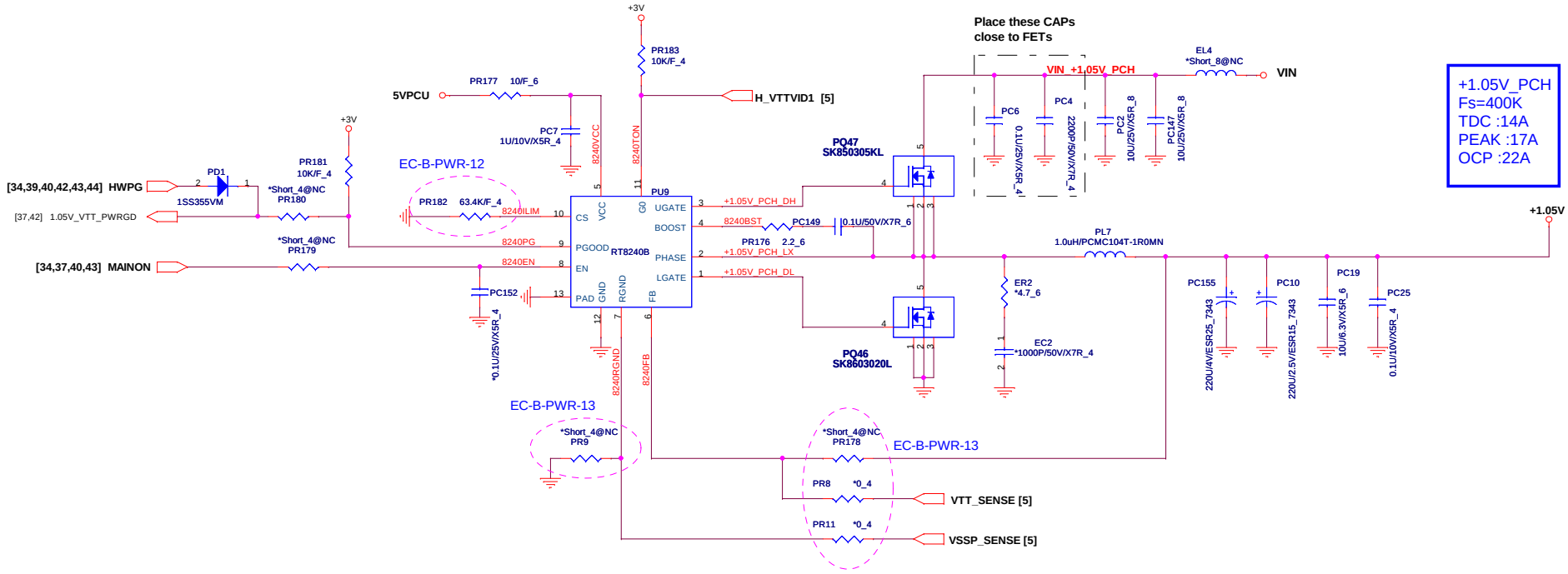

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	+1.05V_VTT&+1.05V_PCH	

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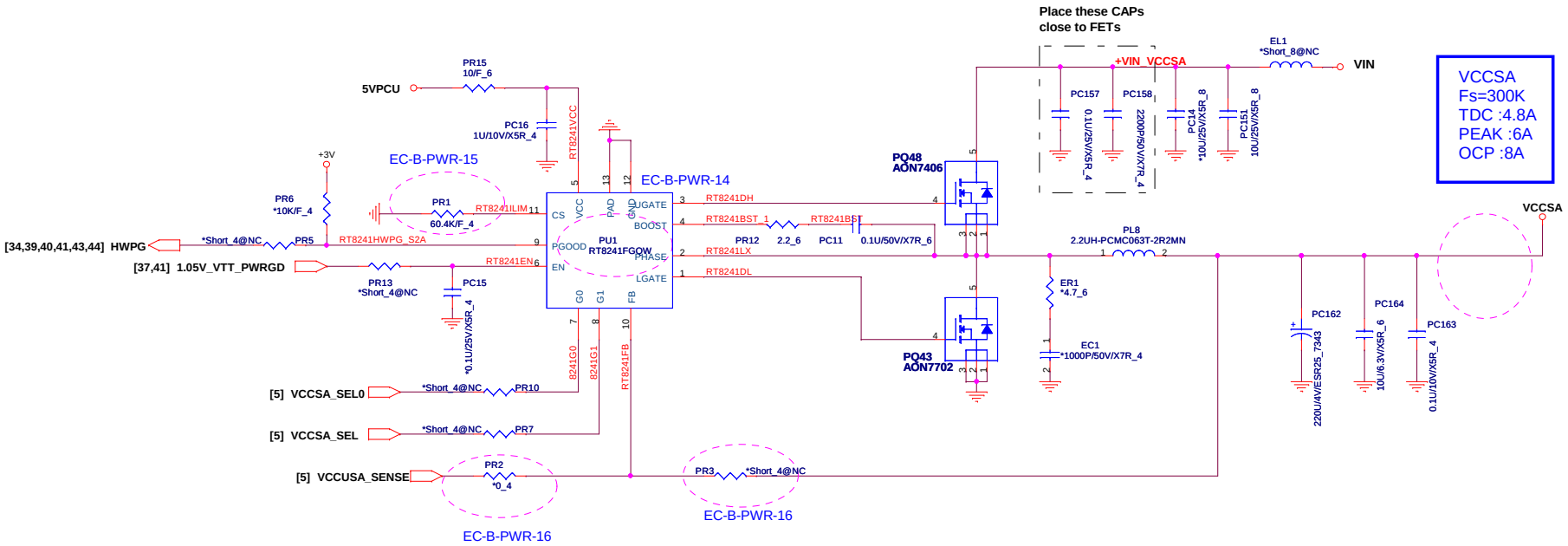

G0	G1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	VCCSA (RT8241E)	

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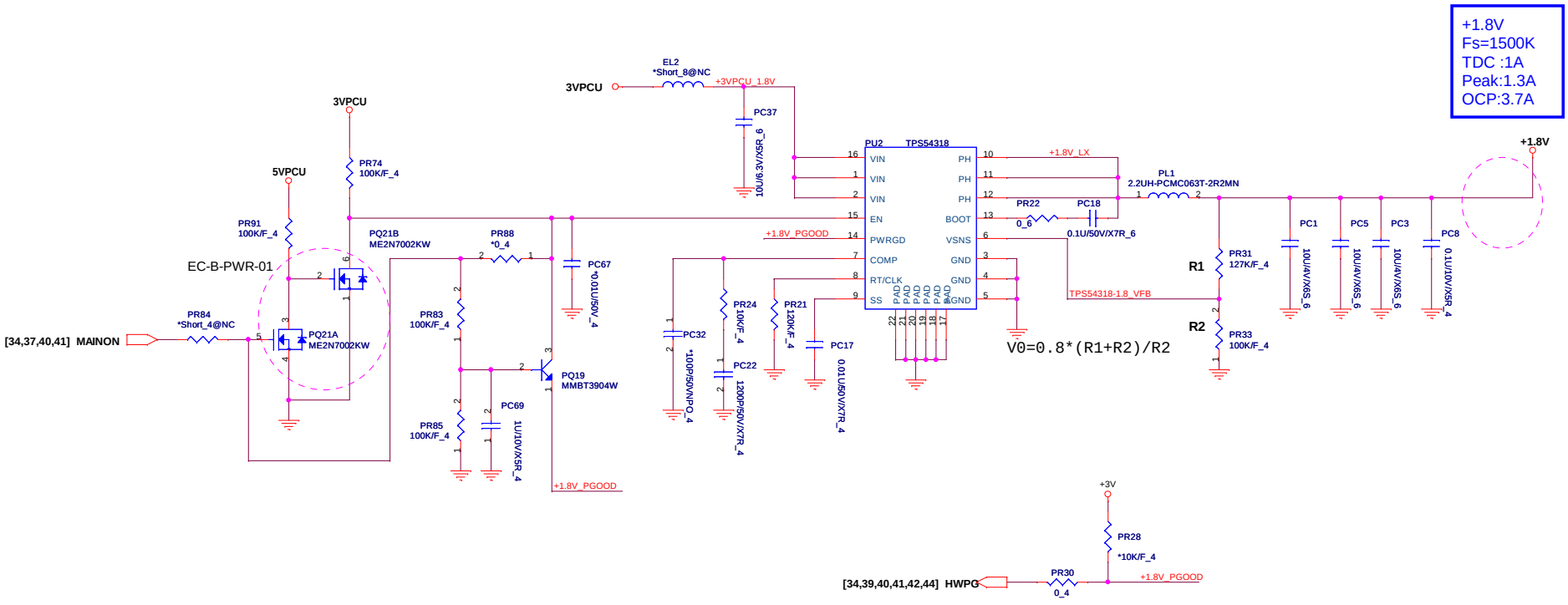
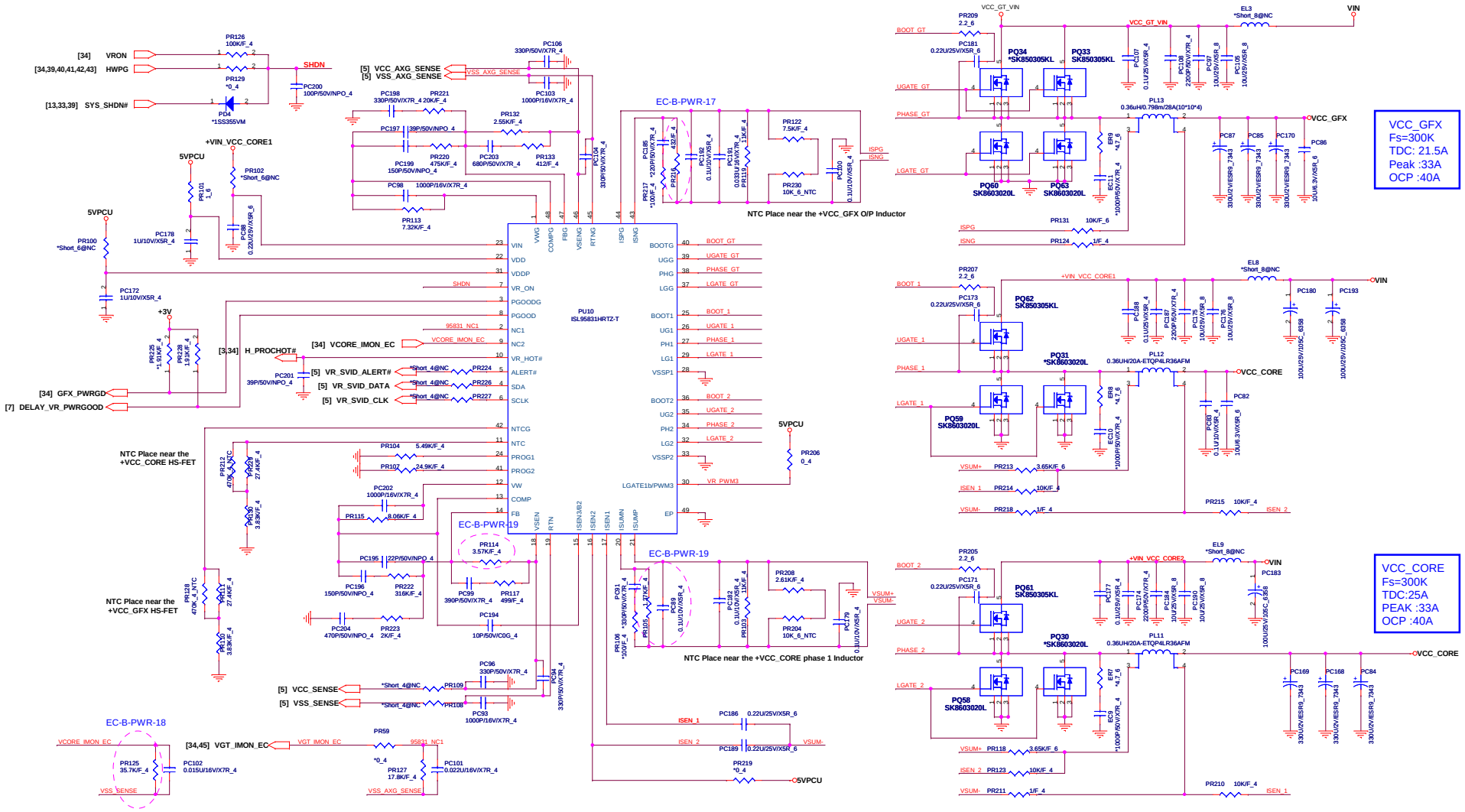


PROJECT LZ8 Chief River DIS		
Quanta Computer Inc.		
Size	Document Number: 1.8V (TPS54318)	Rev
Date: Tuesday, December 20, 2011	Sheet 43 of 49	



PROJECT	LZ8 Chief River DIS
Quanta Computer Inc.	
Size	Document Number: CPU(ISL95831)IMVP2+1
Rev	
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VID 1.2875V

3VPCU
PR36 *0_4 H_VID0
PR191 *0_4 H_VID1
PR192 *0_4 H_VID2
PR194 *0_4 H_VID3
3VPCU
PR195 *0_4 H_VID4
PR45 *0_4 H_VID5

[18] dGPU_PCNT
5VPCU
PR25 *Short_6@NC
PC28 2.2u/6.3V/X5R_4
+3V
51728_V5FILT
PR49 *Short_4@NC
PR52 *0_4
PR34 *10K/F_4

[46] NVVDD_PG
PR188 *0_4
PR193 *100K/F_4
+3V
GPU_EN
PR51 *Short_4@NC
[9,46] GFXON
PR190 100K/F_4
PC40 100P/50V_4

[18] GPU_VID0 PR35 *Short_4@NC H_VID0
[18] GPU_VID1 PR38 *Short_4@NC H_VID1
[18] GPU_VID2 PR37 *Short_4@NC H_VID2
[18] GPU_VID3 PR40 *Short_4@NC H_VID3
[18] GPU_VID4 PR39 *Short_4@NC H_VID4
[18] GPU_VID5 PR42 *Short_4@NC H_VID5
PR48 1K/F_4 H_VID6

PU3
TPS51728
PGD PG PCNT SLP EN THAL VID0 VID1 VID2 VID3 VID4 VID5 VID6 DROOP VREF SLEW THRM VFB GFB IMON PwPd GND V5IN DRVH2 VBST2 LL2 DRVL2 CSP2 CSN2 DRVH1 VBST1 LL1 DRVL1 CSP1 CSN1 PGND TONSEL TRIPSEL OSRSEL PU V5FILT

EC-B-PWR-22
PC52 68P/50V/COG_4
51728_DROOP
PC53 1200p/50V/X7R_4
PR41 8.2K/F_4
51728_VREF
PC57 0.22u/10V/X7R_6
PR50 *0_4
51728_V5FILT
PR198 *0_4
PR56 *0_4
PR57 0_4
51728_TONSEL
PR197 124K/F_4
PR200 20K/F_4
51728_SLEW

+3V
PR26 0_4
EC-B-PWR-21
51728_TONSEL
51728_TRIPSEL
51728_OSRSEL
PR187 0_4
PR27 *0_4
EC-B-PWR-21
PC43 2.2u/6.3V/X5R_4
PR32 *0_4
PR29 *0_4
51728_V5FILT

VGPU_CORE
PR67 10_4
PR66 *Short_4@NC
[15] GPU_VDD_SENSE
[15] GPU_VSS_SENSE
PR65 *Short_4@NC
Parallel
51728_VFB
51728_GFB
PR60 56K/F_4
PC60 3300p/50V/X7R_4
PR64 10_4
EC-B-PWR-20
PR201
[34,44] VGT_IMON_EC
PR55 *Short_4@NC
51728_IMON

VGPU_CORE
Fs=300k Hz
TDC:20A
Peak:25A
OCP:33A
Loadline=0mV/A

+VIN_GPU_CORE
EL6 *Short_8@NC
VIN
PC29 0.1U/25V/X5R_4
PC160 2200p/50V/X7R_4
PC27 10U/25V/X5R_8
PC159 10U/25V/X5R_8

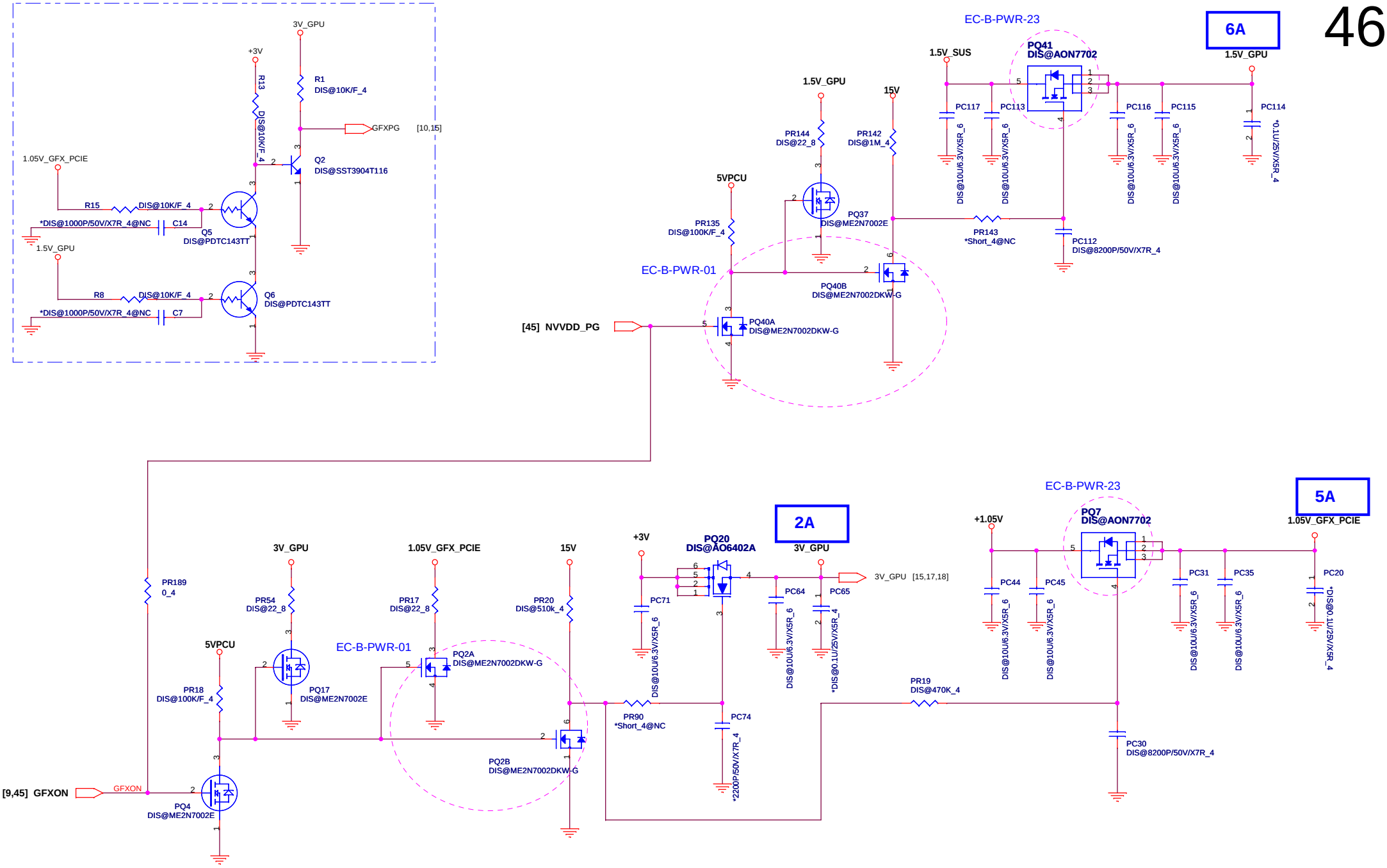
51728_VBST1
PR23 2.2/F_6
PC21 0.22u/25V_6
51728_DRVH1
PQ51 SK850305KL
51728_LL1
51728_DRVL1
PQ44 SK8603020L
PQ45 SK8603020L
PL6 0.36uH/0.798m/28A(10*10*4)
VGPU_CORE
ER6 *4.7_6
EC8 *1000P/50V_4
PR14 30K/F_4
PR62 0_4
PC9 10U/6.3V/X5R_6
PC12 330u/2V/ESR9_7343
PC13 330u/2V/ESR9_7343
PC148 330u/2V/ESR9_7343
EC-B-PWR-21

51728_CSP1
PC62 33p/50V/NPO_4
PC167 0.022u/25V_4
PC63 33p/50V/NPO_4
PR199 29.4K/F_4
PR58 100K/F_4
51728_CSN1
PR184 100K/F_4_NTC
Close to the VR side.

*SHORT-1A

PROJECT LZ8 Chief River DIS
Quanta Computer Inc.

Size	Document Number	Rev
	DGPU Core (TPS51728)	1A
Date: Tuesday, December 20, 2011	Sheet 45 of 49	



PROJECT LZ8 Chief River DIS		
Quanta Computer Inc.		
Size	Document Number: GPU Sequence	Rev: 1A
Date: Tuesday, December 20, 2011	Sheet 46 of 49	

ECN	PG	DATE yy/mm/dd	PART	DESCRIPTION
EC-B-01	7,11,34	11/10/13	Add R607,R608,R621 and no ASM	Add DEEP S3 function
EC-B-02	7	11/10/13	R210	R210 chnage to short pad
EC-B-03	9	11/10/13	R610 no ASM,R611 ASM,	For DGPU power enable sequence
EC-B-04	10	11/10/13	R573 no ASM,R572 ASM	Change Board ID for SIV stage
EC-B-05	10,22	11/10/13	C49,R613,C724,R612,Q48 add and ASM	Change CCD control by PCH GPIO35
EC-B-06	23	11/10/13	CN10	Change CN10 to correct footprint
EC-B-07	24	11/10/13		Change Audio detect schematic
EC-B-08	25	11/10/13	CN8	Change CN8 to correct footprint
EC-B-09	32	11/10/13	CN15	Change CN25 Pin define
EC-B-10	33	11/10/13	Add R614,R622 no ASM	Add EC detect Fan speed schematic
EC-B-11	34	11/10/13	DELR321	Change EC pin define,PIN94 connect to PWR_WHITE,PIN28 connect to FAN_PWM_R,PIN47 connect to FANSIG_R
EC-B-12	34	11/10/13	R298 no ASM	EC can output CLOCK by itself
EC-B-13	30	11/10/13	R35 no ASM,Q11ASM	input AOAC function
EC-B-14	28	11/10/13	CN13,CN17	Change CN13,CN17 to correct footprint
EC-B-15	28	11/10/13	add Q51,R623 no ASM	Add DEEP S3 function
EC-B-16	35	11/10/13	CN16	Change CN16 footprint for ME request
EC-B-17	9,18,22 23,33	11/10/14	Q30,Q31,Q26,Q27,Q34,Q35,Q3,Q4, Q41,Q42,Q23,Q24 DEL Add Q52,Q53,Q54,Q55,Q56,Q57 and ASM	Change MOS to Dual MOS
EC-B-18	21	11/10/19	Add Q58	For PS8622 flash ROM by EC ROM
EC-B-19	05	11/10/19	Add C727	Add a 10UF CAP for INTEL suggestion
EC-B-20	21	11/10/19	L14,L15,L16	Change footprint to 0603
EC-B-21	27	11/10/20	CN3	Change footprint for ME request
EC-B-22	36	11/10/24	Add C729,C730,C731	For EMI request
EC-B-23	3,7,11	11/10/24		Change LVDS singal by PCH provide
EC-B-24	7,24,25 26,27,29 30,31,33	11/10/24	R602,R322,R274,R305,R582,R580, L10,R129,R88,R87,R99,R79,R78, L22,L24	Change to short PAd
EC-B-25	8	11/10/24	BT1	Change BT1 footprint
EC-B-26	25	11/10/24	CN8	CN8 PIN4,5,7,8 connect to GND
EC-B-27	11,15	11/10/24	CML1,CML2,CML4,CML5 ASM R505,R502,R560,R563,R232,R233 R234,R235,C486,C488,C490,C497	for EMI request
EC-B-28	35	11/10/25	C472, C471, C470,C469,C681, C682 C683, C684,C685 ASM 0.1U	for EMI request
EC-B-29	35	11/10/25	RV5,C402 ASM 30P R194,R197 change to Bead	for EMI request
EC-B-30	35	11/10/26	C460 ASM 22P	for EMI request

PROJECT LZ8 Chief River DIS

Quanta Computer Inc.

Size	Document Number	Rev
	Change List for B	2A

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ECN NO	PG	DATE yy/mm/dd	PART	DESCRIPTION
EC-C-01	27	11/12/05	R277 ASM	Change Card reader to normal mode for pre load image
EC-C-02	10	11/12/05	R526 ASM,R527 no ASM,R573 ASM, R572 no ASM	Chaneg Board ID
EC-C-03	34	11/12/05	Add Q59 no ASM, and R628 ASM	For Deep S3
EC-C-04	22	11/12/05	Add Q58 and ASM	Chaneg to Dual MOS
EC-C-05	28	11/12/05	C528 change to raiting to 50V	for China 家電下鄉
EC-C-06	22	11/12/05	Add R629	For PWM control by EC
EC-C-07	11	11/12/05	Change R623 connect to 5VPCU	For Deep S3
EC-C-08	3,6,13,14	11/12/05	Add DDR M3 solution	DDR M3 solution for Deep S3
EC-C-09	22,34	11/12/05	Add R634,R635	Add color engine/dynamtic control function
EC-C-10	9	11/12/10	DEL RP7	Connect VGA CLK to PCH directly
EC-C-11	13,14	11/12/10	ADD R636,R637	to differentiate between M1 and M3 solution
EC-C-12	24	11/12/14	CN6	Change CN6 footprint for follow PDC suggestion
EC-C-13	24	11/12/14	C486,C488,C490,C497	Change to 680P for Vendor suggestion

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ECN NO	PG	DATE yy/mm/dd	PART	DESCRIPTION
EC-B-PWR-01	37, 40, 43, 46	11/10/31	PQ26, PQ24, PQ53, PQ35, PQ64, PQ21, PQ2, PQ40	Change to dual 2N7002
EC-B-PWR-02	38	11/10/31	PL15	Change PL15 to 10u H, size 10*10
EC-B-PWR-03	38	11/10/31	PR165, PR166	Change charger ILIM resistors
EC-B-PWR-04	38	11/10/31	PR11	Add EL11
EC-B-PWR-05	38	11/10/31	PR234	Change Charger resistor
EC-B-PWR-06	38	11/10/31	PR170, PR171	Change charger ACDET res
EC-B-PWR-07	38	11/10/31	PQ42	Change MOSFET with Schottky
EC-B-PWR-08	39	11/10/31	PU4 and so on	Change 3V/5V IC and schematic
EC-B-PWR-09	40	11/10/31	PR146	Change voltage setting resistor
EC-B-PWR-10	40	11/10/31	PR157	Change 1.5V_SUS OCP resistor
EC-B-PWR-11	40	11/10/31	PD14	Add PD14 to improve sequence
EC-B-PWR-12	41	11/10/31	PR182	Change 1.05V OCP resistor
EC-B-PWR-13	41	11/10/31	PR8, PR9, PR11, PR178	Improve 1.05V feedback
EC-B-PWR-14	42	11/10/31	PU1	Change VCCSA IC to AL008241003
EC-B-PWR-15	42	11/10/31	PR1	Change VCCSA OCP resistor
EC-B-PWR-16	42	11/10/31	PR2, PR3	Improve VCCSA feedback
EC-B-PWR-17	44	11/10/31	PR216	Change GFXcore OCP resistor
EC-B-PWR-18	44	11/10/31	PR125	Change VCC_core IMON resistor
EC-B-PWR-19	44	11/10/31	PC89, PR114, PR105	Change VCC_core OCP and Loadline
EC-B-PWR-20	45	11/10/31	PR60	Change DGPU IMON resistor
EC-B-PWR-21	45	11/10/31	PR26, PR27, PR14, PR58	Change DGPU OCP resistors
EC-B-PWR-22	45	11/10/31	PC52, PC53, PR41	Improve function
EC-B-PWR-23	46	11/10/31	PQ7, PQ41	Improve function

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