

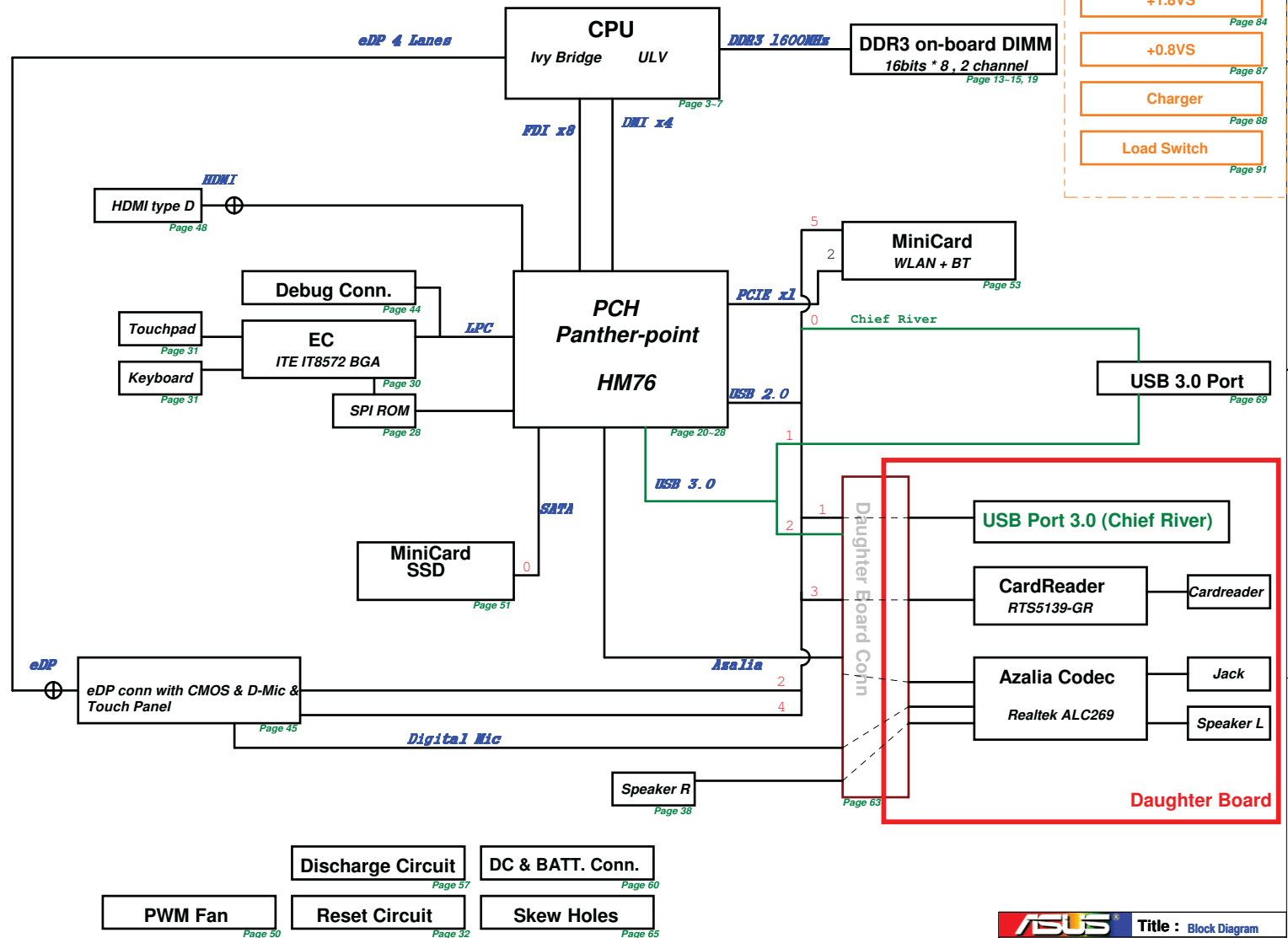
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80. PW_VCORE(RT8168B)
81. PW_SYSTEM(RT8239B)
82. PW_I/O_VCCP(TPS51317)
83. PW_I/O_DDR(RT8207M)
84. PW_+1.8VS(RT8015B)
87. PW_+0.8VS(RT8015B)
88. PW_CHARGER(BQ24725)
91. PWR_LOAD SWITCH

UX31A2 SCHEMATIC Revision R2.0

BLOCK DIAGRAM



PCH_CPT
GPIO

PCH_IBEX GPIO	Use As	Signal Name	Int.& Ext Pull up / down	Power
GPIO 00	Native	NC_TP	EXT PU 1K	+3VS
GPIO 01	GPI	EXT_SMI#	INT PU 20K, EXT PU 10K	+3VS
GPIO 02	Native	NC_TP	EXT PU 10K	+3VS
GPIO 03	GPI	SATA_ODD_DA#	EXT PU 10K	+5VS
GPIO 04	GPI	PCB_ID0	EXT PD 10K	
GPIO 05	GPI	PCB_ID1	EXT PD 10K	
GPIO 06	Native	TMDS_HDMI_HPD	INT PU 20K, EXT PU 10K	+3VS
GPIO 07	GPI	USB3_SMI#	INT PU 20K, EXT PU 10K	+3VS
GPIO 08	Strapping	ICC_EN#		
GPIO 09	Native	EXT_SCI#	EXT PU 10K	+3VSUS
GPIO 10	Native	OC#6	EXT PU 10K	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU 10K	+3VSUS
GPIO 12	GPO			
GPIO 13	Native	HDA_DOCK_RST#		
GPIO 14	Native	OC#7	EXT PU 10K	+3VSUS
GPIO 15	GPO	BT_LED	INT PD 20K, EXT PU 1K	+3VSUS
GPIO 16	Native	SATA_DET#4	EXT PU 10K	+3VS
GPIO 17	GPI		INT PU 20K, EXT PD 10K	
GPIO 18	Native	CLK_REQ1#	EXT PU 10K	+3VS
GPIO 19	Native	SATA1GP	INT PU 20K, EXT PU 10K	+3VS
GPIO 20	Native	CLK_REQ2#	EXT PU 10K	+3VS
GPIO 21	Native	SATA0GP	EXT PU 10K	+3VS
GPIO 22	GPO	WLAN_LED	EXT PU 10K	+3VS
GPIO 23	Native	LPC_DRQ#1	INT PU 20K	
GPIO 24	GPO		EXT PU 10K	+3VSUS
GPIO 25	Native	CLKREQ_USB3#	EXT PU 10K	+3VSUS
GPIO 26	Native	CLK_REQ4#	EXT PU 10K	+3VSUS
GPIO 27	Native	DSW_WAKE#	INT PU 20K	
GPIO 28	Strapping	WLAN_ON#	INT PU 20K	+3VSUS
GPIO 29	Native	SLP_LAN#	EXT PU 10K	+3VSUS
GPIO 30	Native	ME_SusPwrDnAck	EXT PU 10K	+3VSUS
GPIO 31	Native	ME_AC_PRESENT_PCH	INT PD 20K, EXT PU 10K	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU 10K	+3VS
GPIO 33	Native	HDA_DOCK_EN#		
GPIO 34	Native	STP_PCI#	EXT PU 10K	+3VS
GPIO 35	GPO	GPIO35_PCH		
GPIO 36	Native	DMI_OVRVLTG	INT PD 20K, EXT PU 20K	+3VS
GPIO 37	Native	FDI_OVRVLTG	INT PD 20K, EXT PU 10K	
GPIO 38	Native	MFG_MODE	EXT PU 10K	+3VS
GPIO 39	Native	GF_X_CRB_DET	EXT PU 10K	+3VS
GPIO 40	Native	OC#1	EXT PU 10K	+3VSUS
GPIO 41	Native	DIMM_SEL0	EXT PU 10K	+3VSUS
GPIO 42	Native	DIMM_SEL1	EXT PU 10K	+3VSUS
GPIO 43	Native	DIMM_SEL2	EXT PU 10K	+3VSUS
GPIO 44	Native	CLKREQ_GLAN#	INT PU 20K, EXT PU 10K	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU 10K	+3VSUS
GPIO 46	Native	CLK_REQ7#	INT PD 20K, EXT PU 10K	+3VSUS
GPIO 47	Native	CLK_PEGA_REQ#	EXT PU 1K	+3VSUS
GPIO 48	GPIO	TEST_SET_UP	EXT PU 10K	+3VS
GPIO 49	GPI	SATA_DET#5	EXT PU 10K	+3VS
GPIO 50	GPO	GPU_RST#	EXT PD 10K	
GPIO 51	Strapping	PCI_GNT1#	INT PU 20K, EXT PU 10K	+3VS
GPIO 52	Native	PCI_REQ#2	EXT PU 10K	+3VS
GPIO 53	Native	DGPU_PWM_SELECT#	INT PU 20K	
GPIO 54	GPO	DGPU_PWR_EN#	EXT PD 1K	
GPIO 55	Strapping	STP_A16OVR	INT PU 20K, EXT PD 1K	
GPIO 56	Native	CLK_PEGB_REQ#	EXT PU 10K	+3VSUS
GPIO 57	GPO	BT_ON	EXT PD 100K	
GPIO 58	Native	SML1_CLK	EXT PU 2.2K	+3VSUS
GPIO 59	Native	OC#0	EXT PU 10K	+3VSUS
GPIO 60	GPO	DRAMRST_PCH	EXT PU 2.2K	+3VSUS
GPIO 61	Native	PM_SUS_STAT#		
GPIO 62	Native	SUS_CLK#		
GPIO 63	Native	SLP_S5#		
GPIO[66:64]	Native	CLK_OUT[2:0]	INT PD 20K	
GPIO 67	Native		INT PD 20K	
GPIO 68	GPO	NC_TP	INT PU 20K	
GPIO 69	GPI	NC_TP	INT PU 20K, EXT PD 1K	
GPIO[71:70]	Native	NC_TP	INT PU 20K, EXT PU 1K	+3VS
GPIO 72	Native	PM_BATLOW#	INT PU 20K, EXT PU 10K	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU 10K	+3VSUS
GPIO 74	Native	PCHHOT#	EXT PU 10K	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU 2.2K	+3VSUS

EC IT8572
GPIO

EC GPIO	Use As	Signal Name
GPA0	0	PWR_LED#
GPA1	0	
GPA2	0	CHG_FULL_LED#
GPA3	0	
GPA4	0	
GPA5	0	FAN_PWM
GPA6		-
GPA7	0	KB_LED_PWM
GPB0	0	ME_AC_PRESENT
GPB1	0	
GPB2	0	+3VA_ON
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	0	A20GATE
GPB6	0	RCIN#
GPB7	0	PM_RSMRST#
GPC0		
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	0	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5		
GPC6	I	BAT1_IN_OC#
GPC7		
GPD0	I	PWRLIMIT#_EC
GPD1	0	CAP_LED#
GPD2	I	BUF_PLT_RST#
GPD3	0	EXT_SCI#
GPD4	0	EXT_SMI#
GPD5	0	OP_SD#
GPD6	I	FANO_TACH
GPD7		-
GPE0	0	SUSC_EC#
GPE1		
GPE2	0	1.5V_ON
GPE3	0	BIOS_WP#
GPE4	I	PWR_SW#
GPE5	I	PM_SUSC#
GPE6	I	LID_SW_EC#
GPE7		
GPFO	0	PM_SYSPWROK
GPF1	0	3VSUS_ON
GPF2		-
GPF3	0	USB_CHARGE_ON#
GPF4	IO	TP_CLK
GPF5	IO	TP_DAT
GPF6	I	PECI_EC
GPF7	0	PCH_SPI_OV
GPGo	I	ME_SusPwrDnAck
GPg1	I	PM_SUSB#
GPg2		
GPg6		-
GPHo	IO	PM_CLKRUN#
GPH1	0	THRO_CPU#
GPH2	0	LCD_BACKOFF#
GPH3	0	SUSB_EC#
GPH4	0	USB_CHARGE_VBUS_EC
GPH5		
GPH6	I	5VSUS_PWRGD
GP10	I	Light_Sensor_AD
GP11	I	SUS_PWRGD
GP12	I	ALL_SYSTEM_PWRGD
GP13	I	CORE_PWRGD
GP14		-
GP15		-
GP16		-
GP17	I	Adaptor_Sense
GPJ0	0	
GPJ1	0	PM_PWROK
GPJ2	0	
GPJ3	0	
GPJ4	0	5VSUS_PWRON
GPJ5	0	DRAMRST_EC

Design IP Source: N53S

SM_BUS ADDRESS :		
PCH Master		
SM-Bus Device	SM-Bus Address	
EC Master (SMB1)		
SM-Bus Device	SM-Bus Address	
DIMM TEMP.	9Ah	
CPU Thermal Sensor	90h	

PCI Express

PCIE 1	
PCIE 2	Minicard WLAN
PCIE 3	
PCIE 4	USB 3.0
PCIE 5	
PCIE 6	
PCIE 7	
PCIE 8	

USB Port

USB 0	USB 3.0 Port
USB 1	USB Port 1
USB 2	Touch Panel
USB 3	Card Reader
USB 4	CMOS Camera
USB 5	Bluetooth
USB 6	
USB 7	
USB 8	
USB 9	
USB 10	
USB 11	
USB 12	
USB 13	

SATA Port

SATA 0	SATA SSD
SATA1	
SATA2	
SATA4	

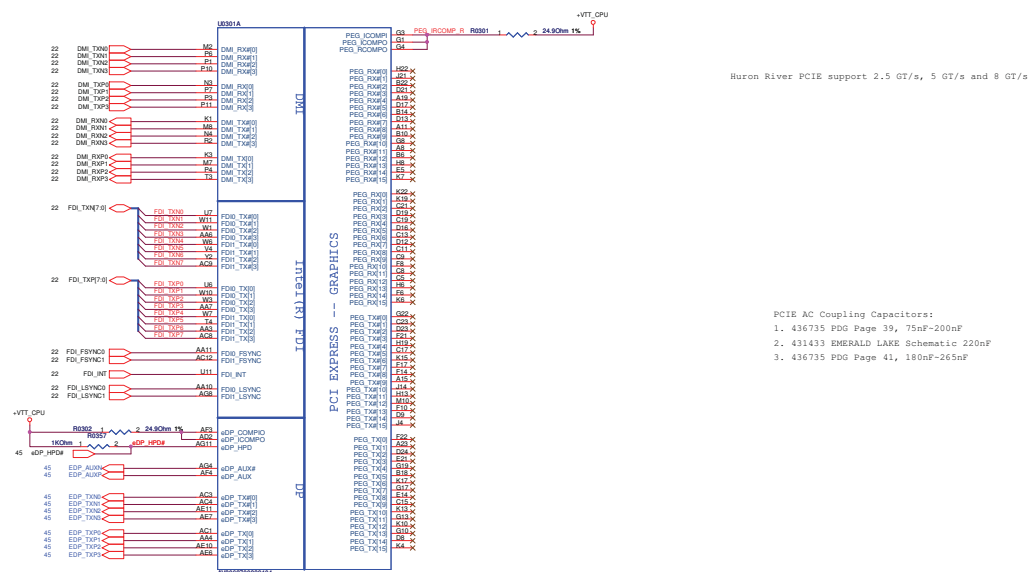
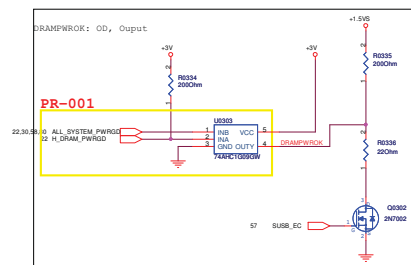
Device Identification

CPU Thermal Sensor		
1st	06G023123010	NCT7717U
2nd		

Memory Thermal Sensor		
1st	06G023048020	G781-1
2nd		

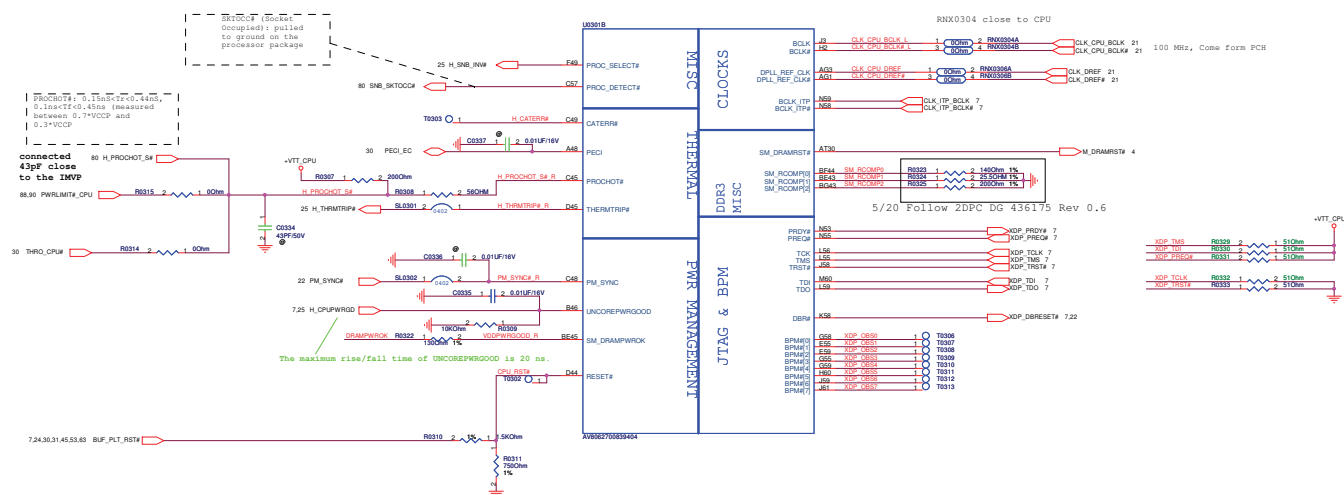
FDI disable: (For discrete graphic)
1. NC: FDI_TX[0:7], FDI_TX[0:7], VCC_AOXSENSE, VSS_AOXSENSE
2. Pull-down to GND via 1KΩ ± 5% resistor: FDI_FSYNC[0:1], FDI_LSYNC[0:1], FDI_INT, GFX_IMON ~15mW power saving
3. Connected to GND: VCCAXG
4. Can be connected to GND directly: DPLL_REF_CLK, DPLL_REF_CLK#
5. Connect to +V1.05S rail: VCCFDIPLL

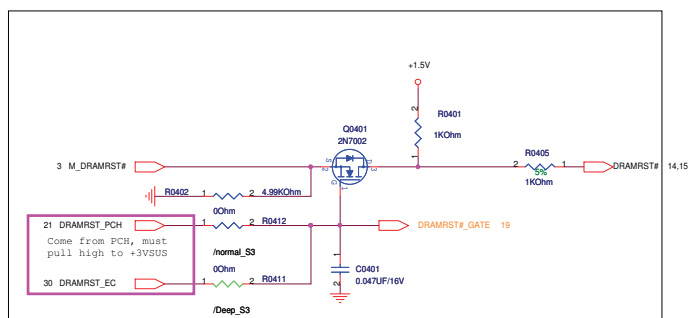
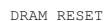
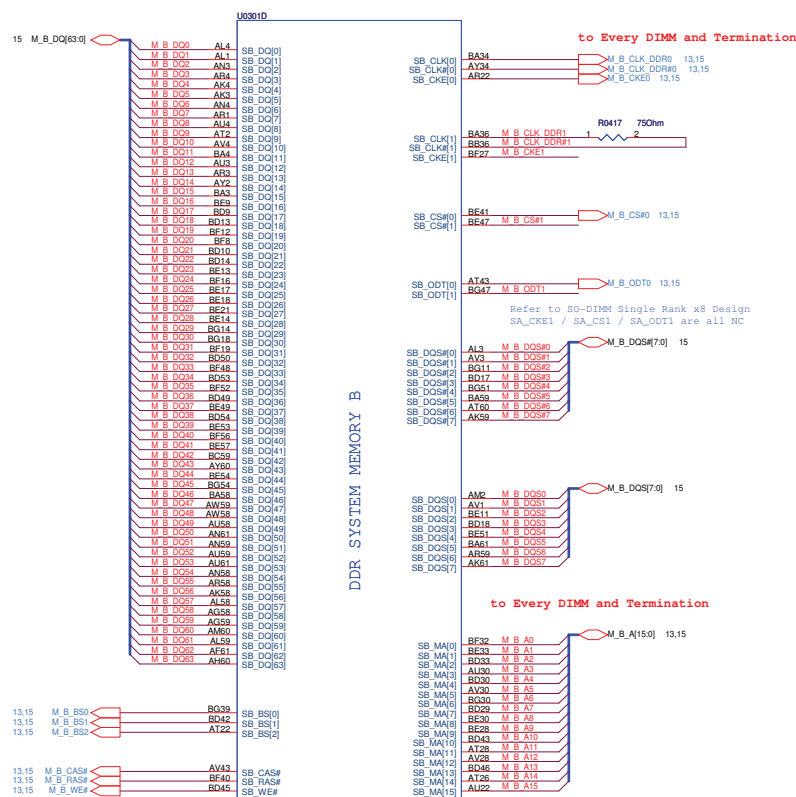
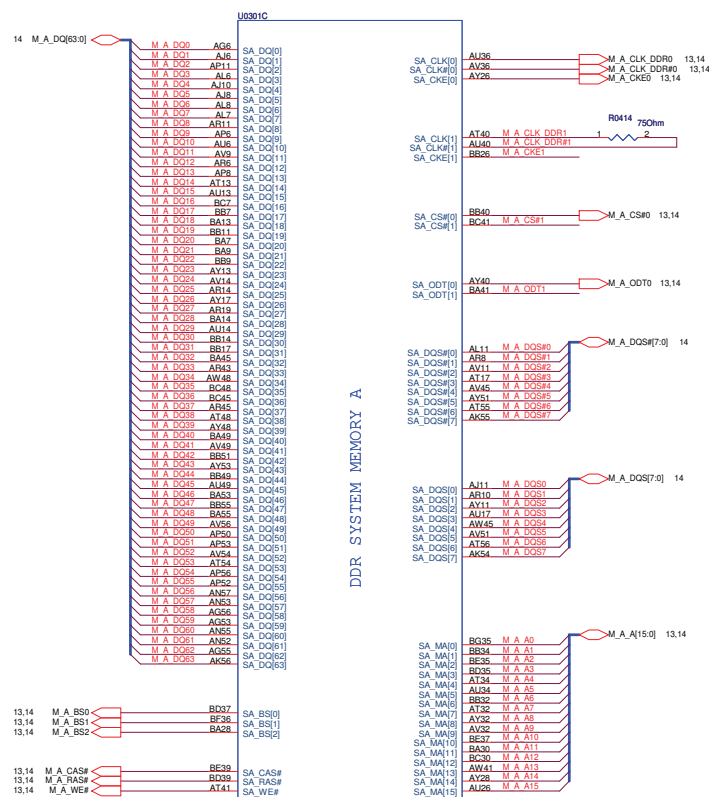
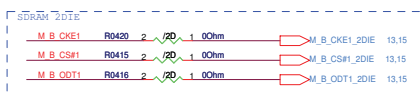
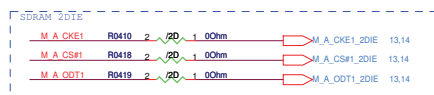
eDP disable/Enable
CFG[4]:
Enable: Mount R0503, R0303=1K
Disable: un-mount R0503, R0303=10Kohm

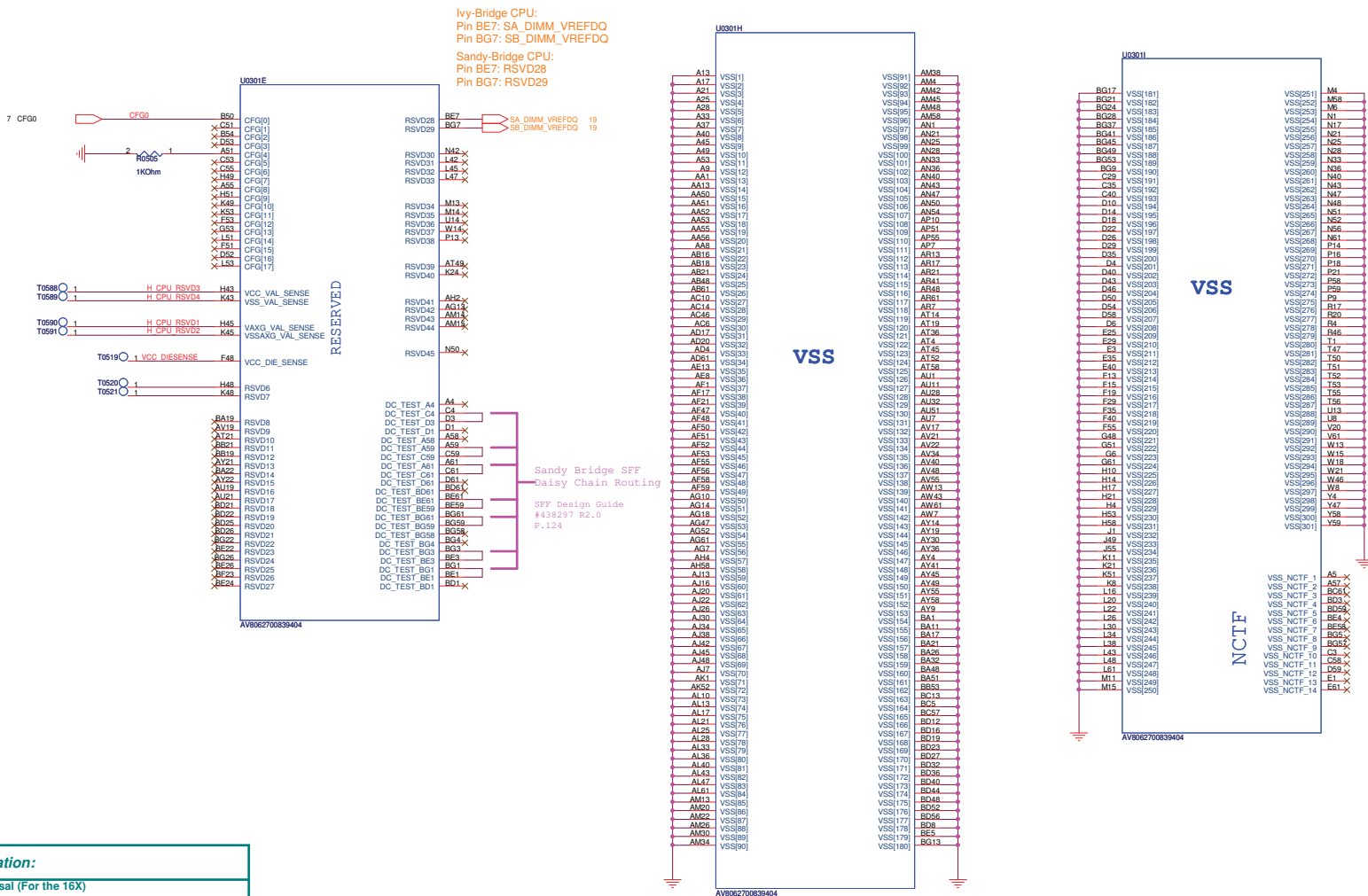


PCIE AC Coupling Capacitors:

1. 436735 PDG Page 39, 75nF-200nF
2. 431433 EMERALD LAKE Schematic 220nF
3. 436735 PDG Page 41, 180nF-265nF







CFG strapping information:

CFG[2]: PEG Static Lane Reversal (For the 16X)

- 1: (Default) Normal Operation; Lane # definition matches socket pin map definition
- 0: Lane Reversed

CFG[4]: Display Port Presence Strap

- 1 : (Default) Disable; No Physical Display Port attached to Embedded Display Port
- 0 : Enable; An external Display Port device is connected to the Embedded Display port

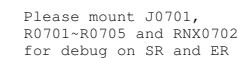
CFG[6:5]: PCIe Port Bifurcation Straps

- 11 : (Default) X16 - Device 1 functions 1 and 2 disable
- 10 : X8, X8 - Device 1 function 1 enabled; Function 2 disable
- 01 : Reserved - (Device 1 Function 1 disable ; Function 2 enable
- 00 : X8, X4 X4 - Device 1 function 1 and 2 enabled

CFG[7]: Defer Training

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS for training





Main Board



Title : NB ****

ASUSTeK COMPUTER INC. NB1

Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0
Date: Tuesday, March 27, 2012		Sheet 9 of 99

Main Board



Title : NB_****

ASUSTeK COMPUTER INC. NB1

Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0

Date: Tuesday, March 27, 2012Sheet 10 of 99

Main Board



Title : NB_****

ASUSTeK COMPUTER INC. NB1

Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0
Date: Tuesday, March 27, 2012		Sheet 11 of 99

Main Board



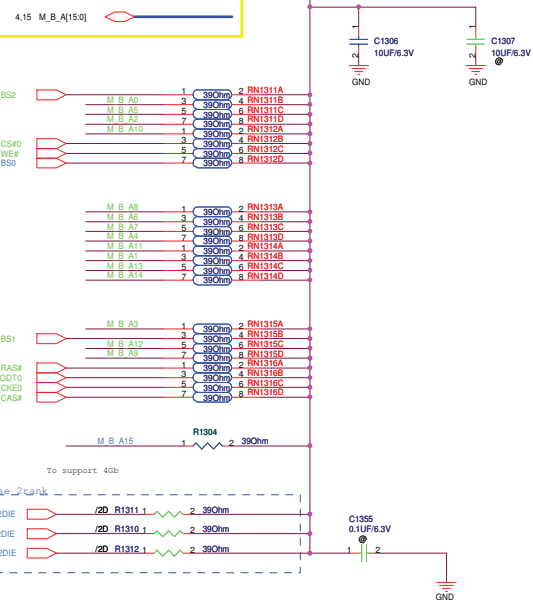
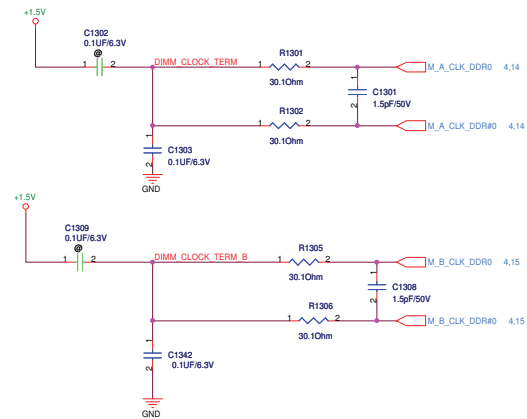
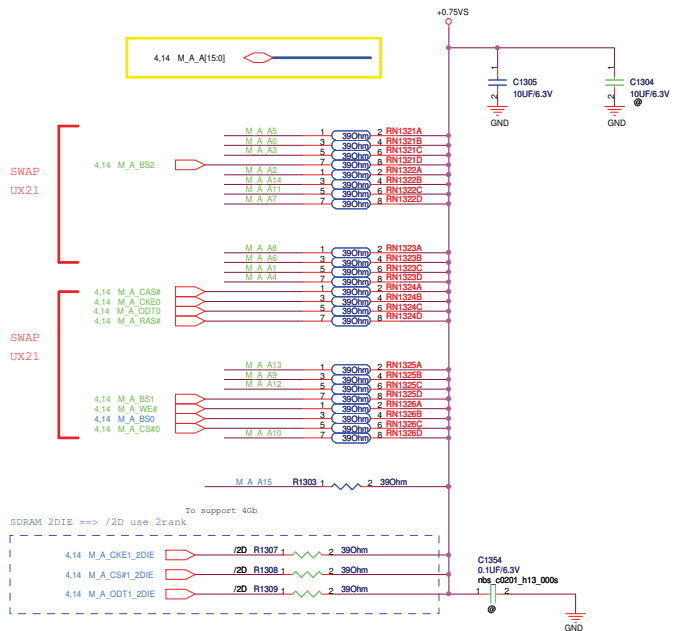
Title : NB_****

ASUSTeK COMPUTER INC. NB1

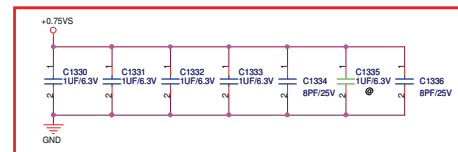
Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0

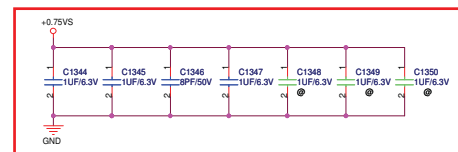
Date: Tuesday, March 27, 2012Sheet 12 of 99



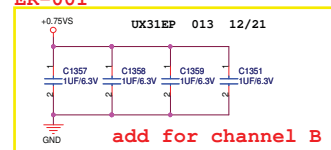
Refer to Intel CSB



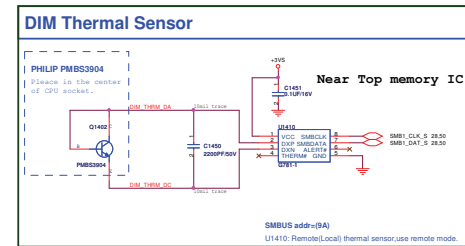
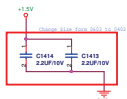
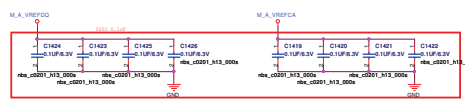
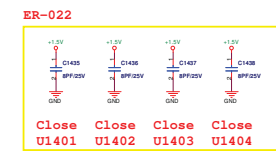
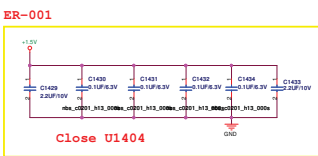
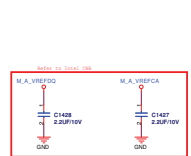
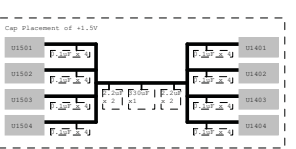
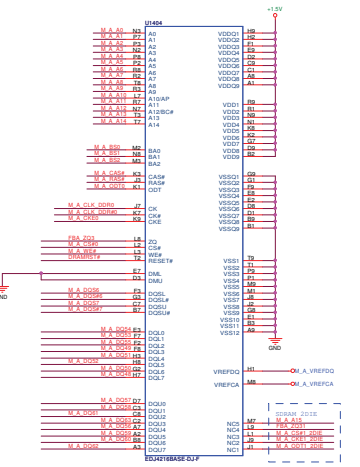
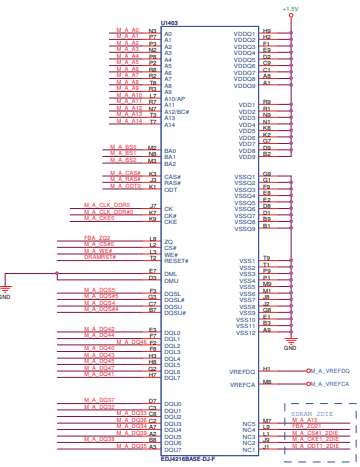
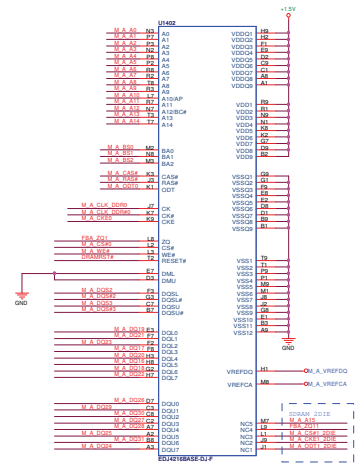
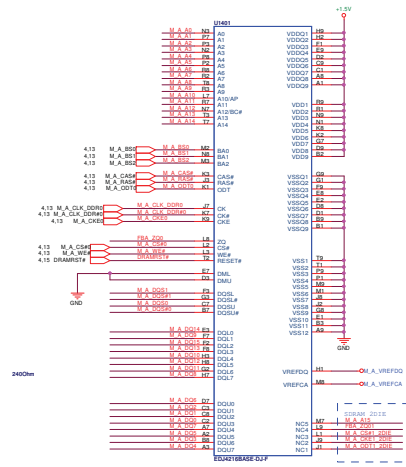
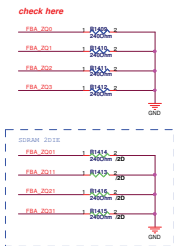
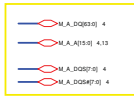
Refer to Intel CSB

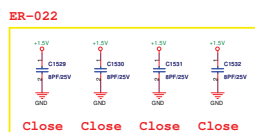
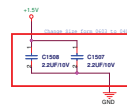
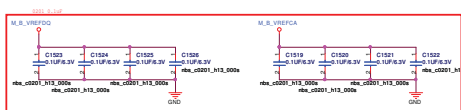
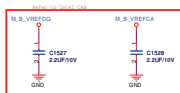
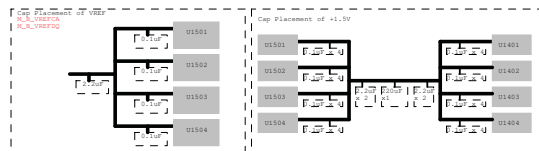
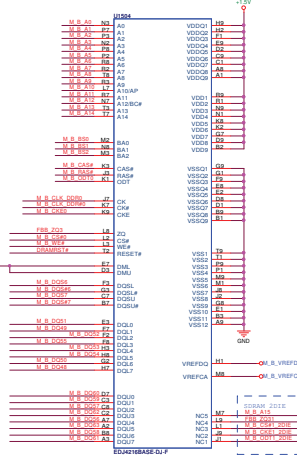
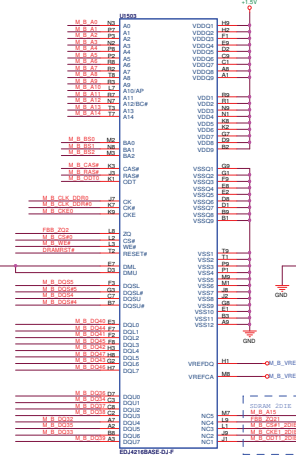
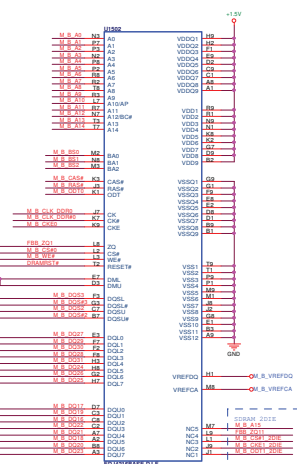
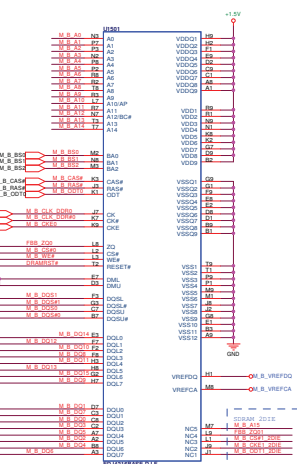
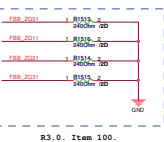
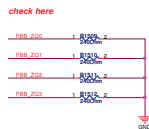


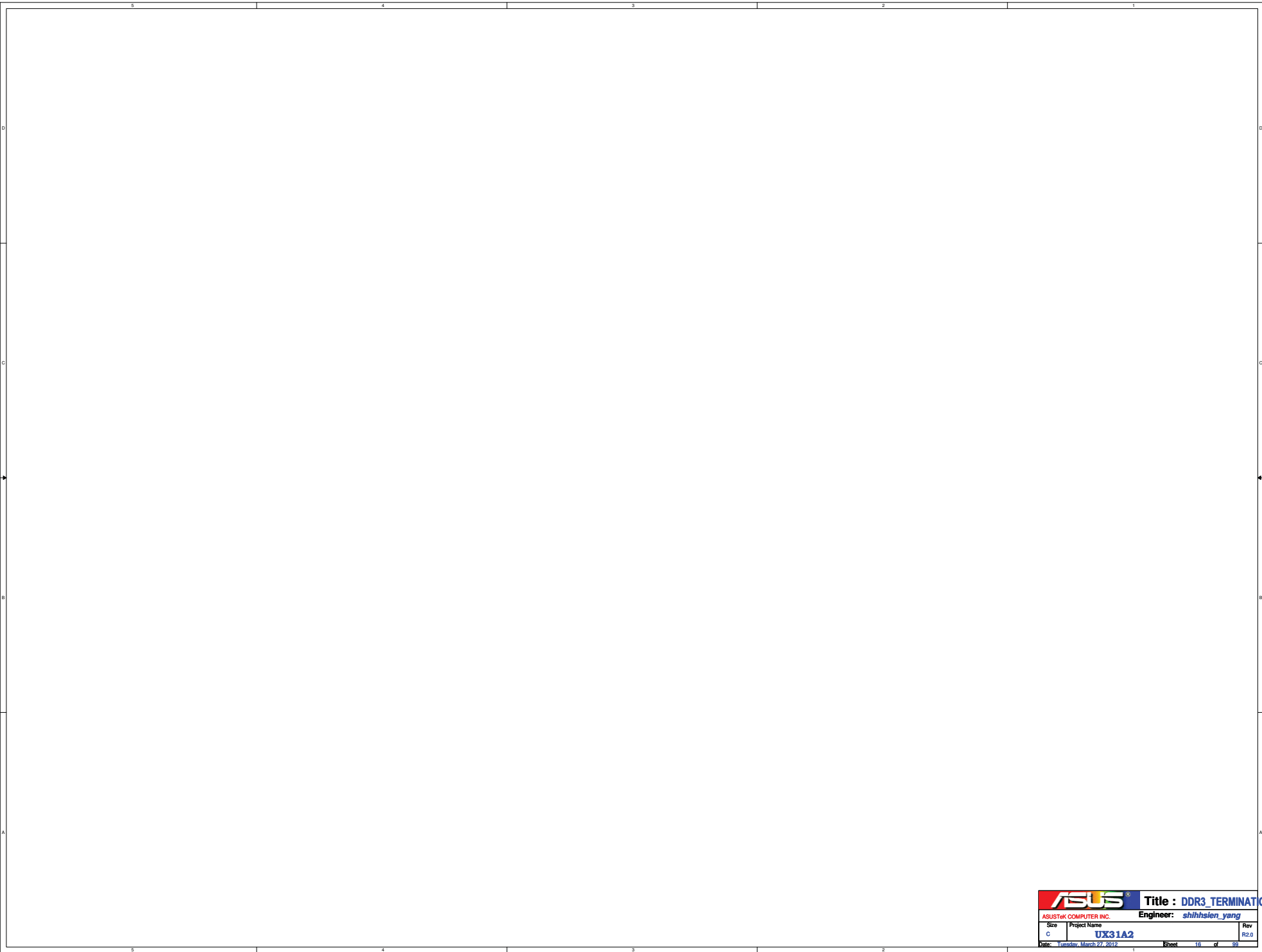
ER-001

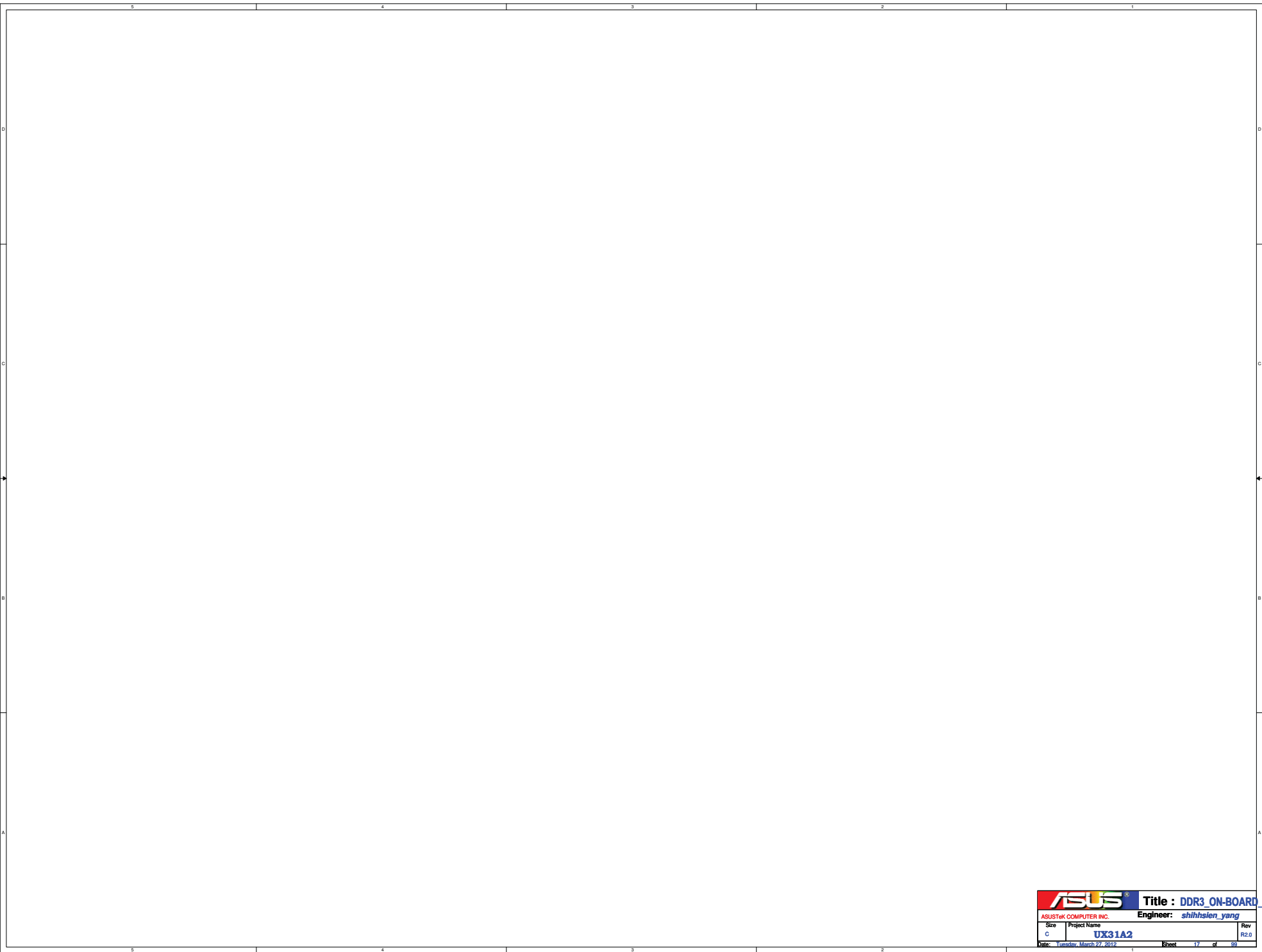


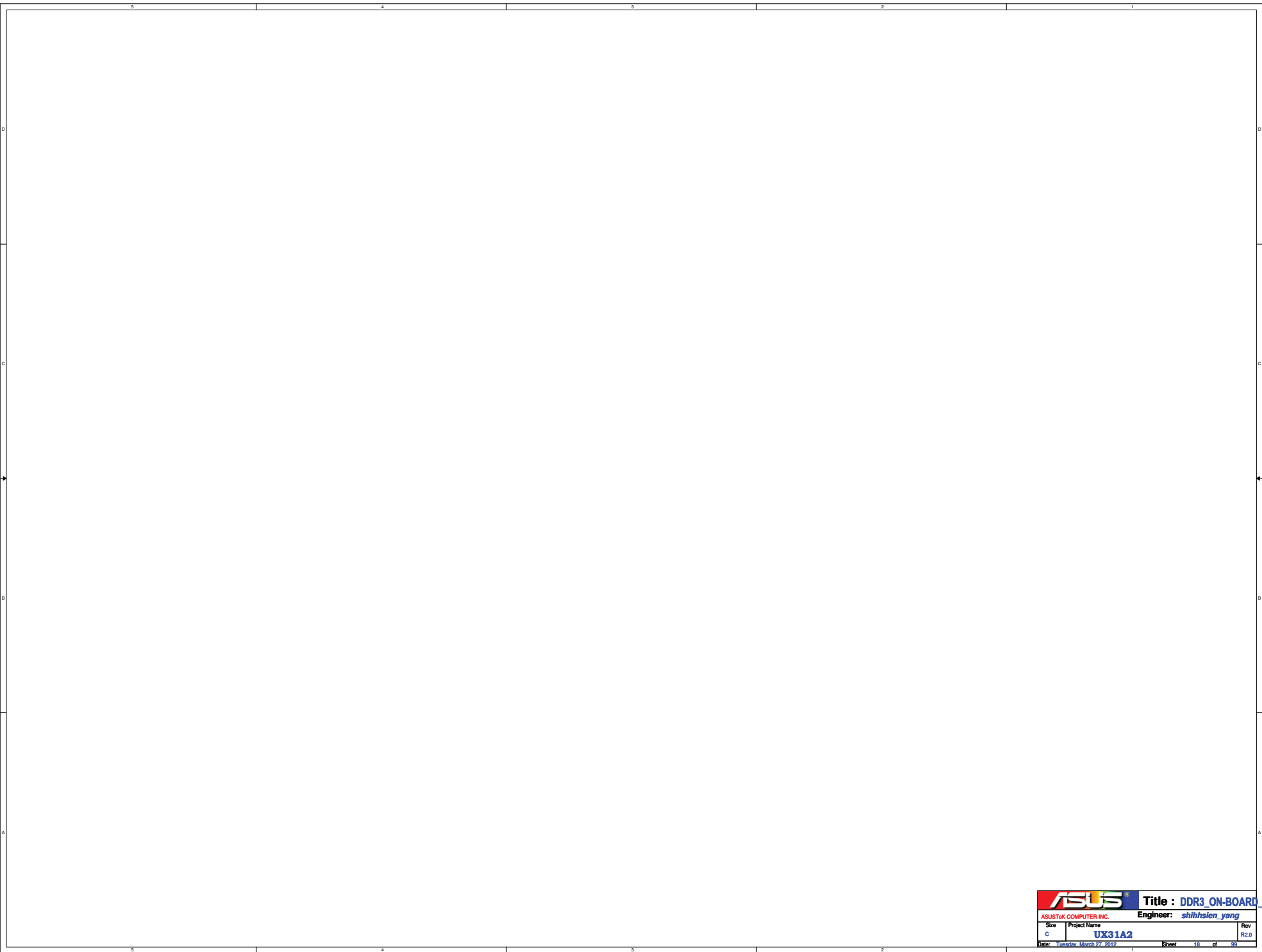
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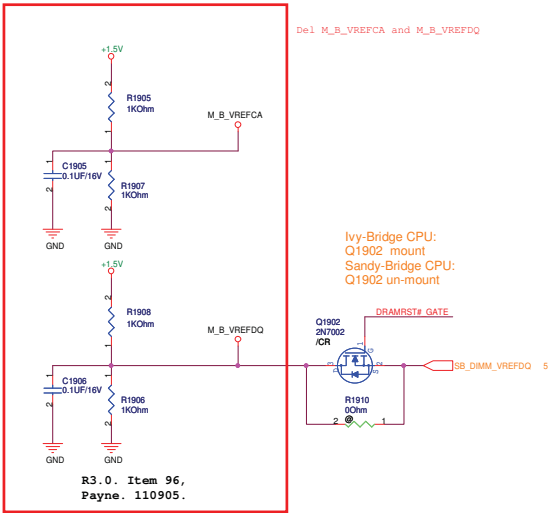
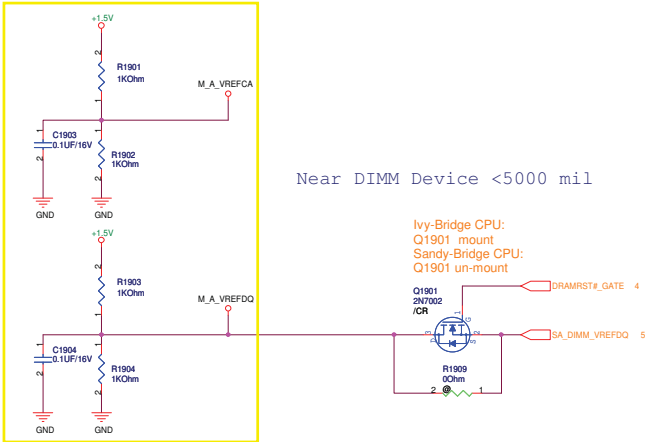






DDR3 Vref

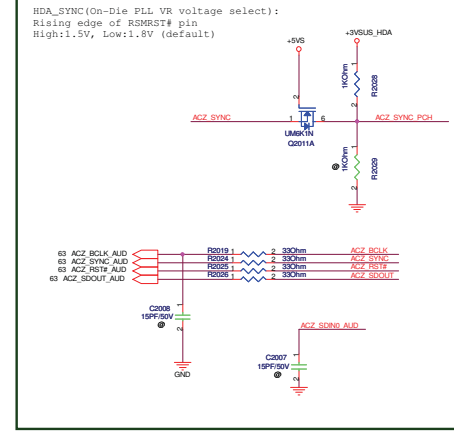
Intel Document Number: 400755



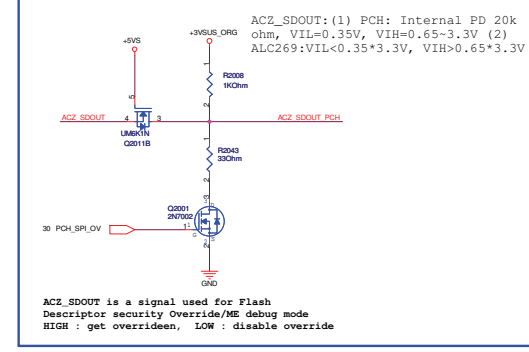
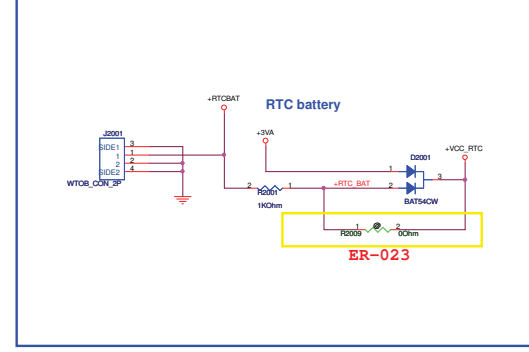
R3.0. Item 96,
Payne. 110905.

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)
TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

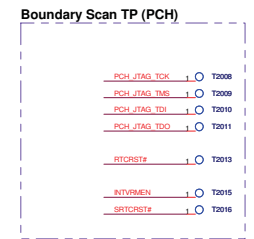
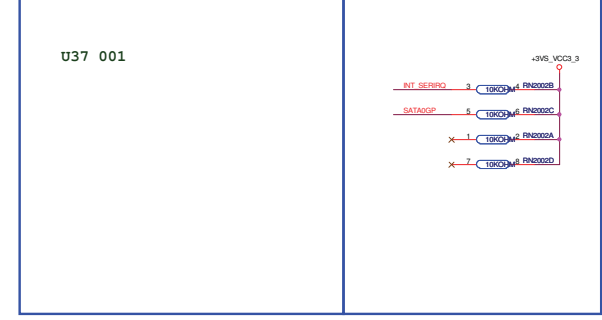
HD Audio



RTC Battery

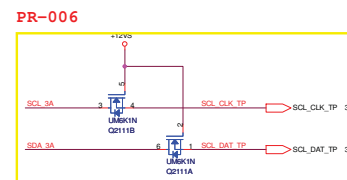
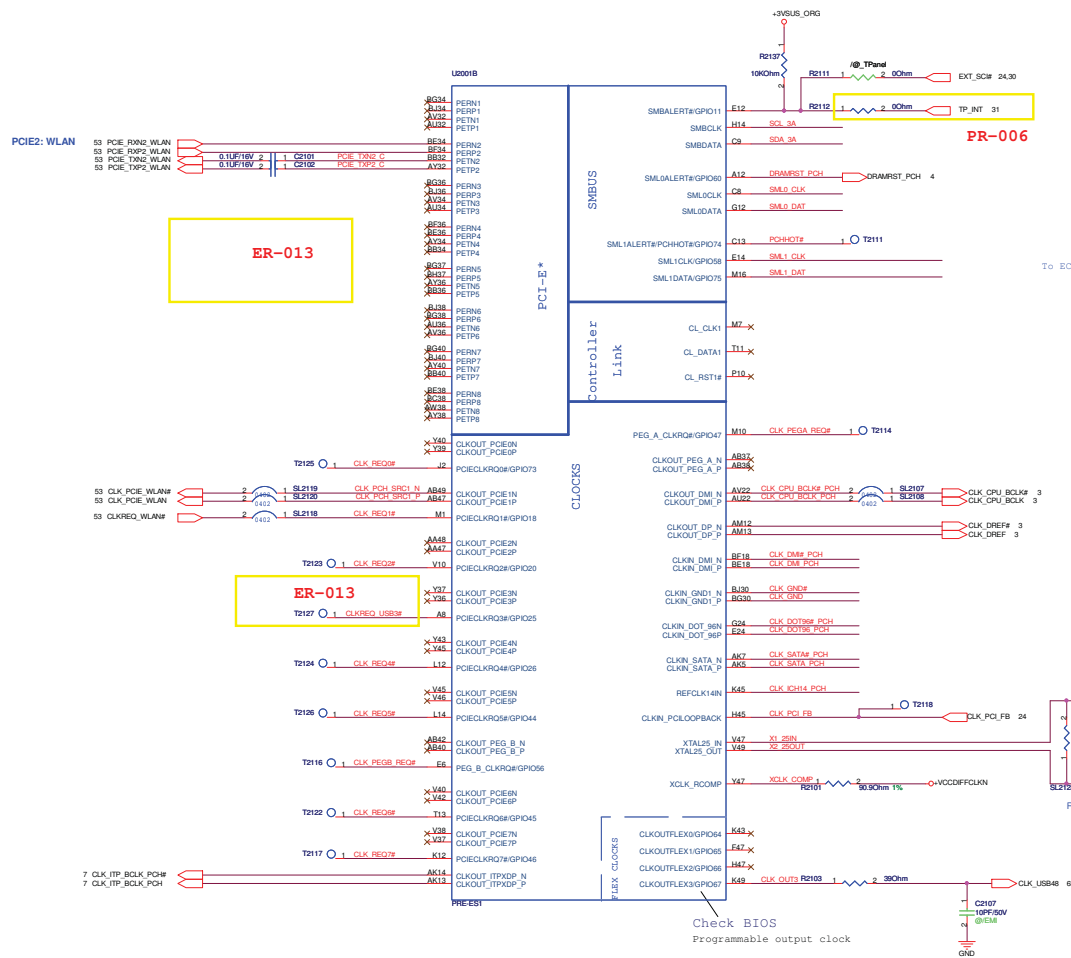


JTAG

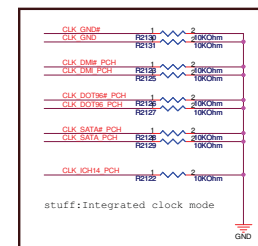
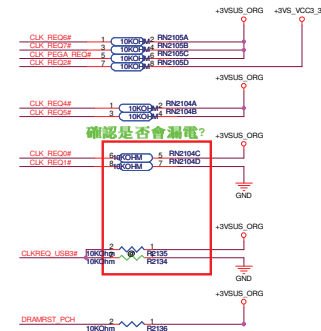
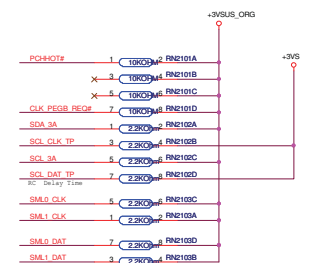


01/04 Modify by Spark
Follow Capella
ER-026

Boot BIOS Strap:GNT1#(BBS0), SATA1GP(BBS1)

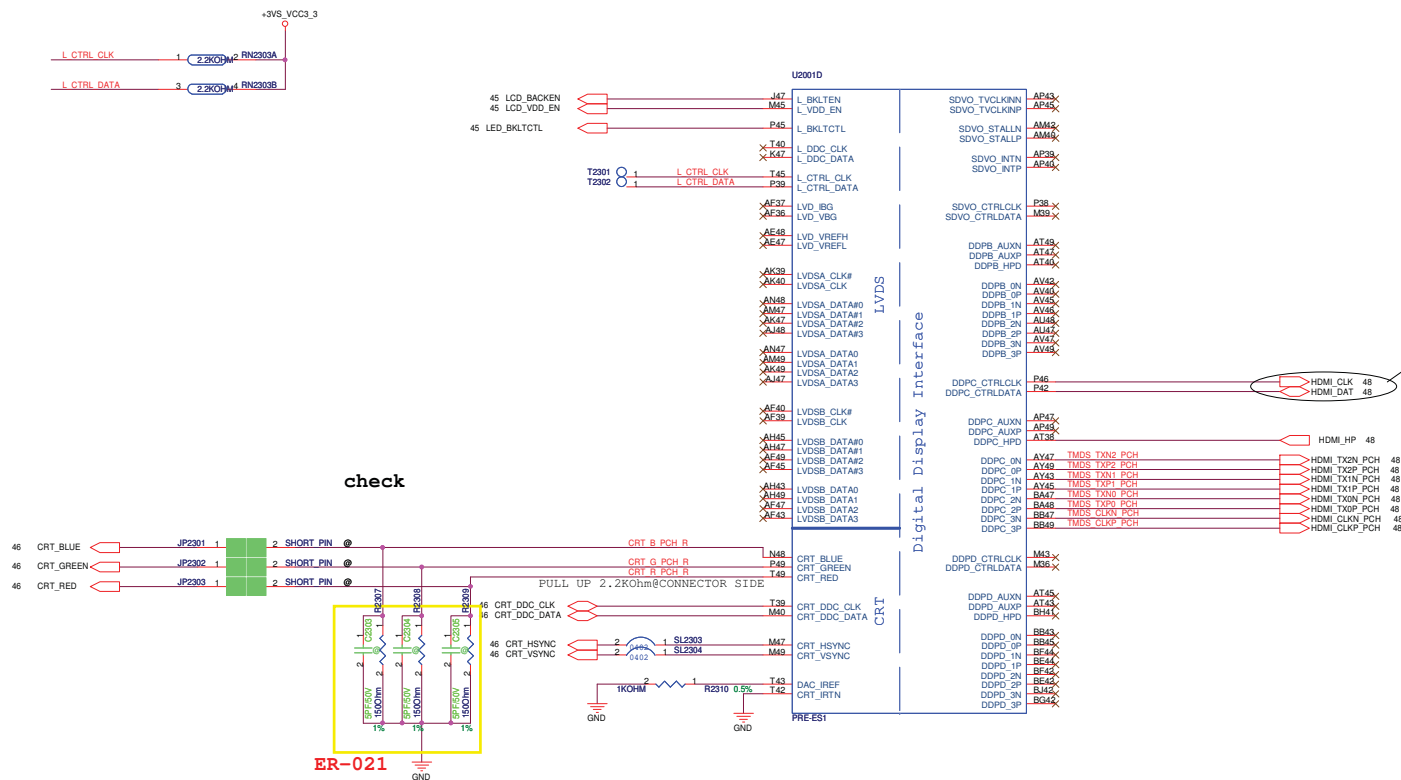


PCH CLKREQ Setting:



PORT	STRAP	ENABLE PORT	DISABLE PORT
LVDS	L_DDC_DATA		
PORT B	SDVO_CTRLDATA	Pull up to 3.3(V) with 2.2k Ohm	NC
PORT C	DDPC_CTRLDATA		
PORT D	DDPD_CTRLDATA		

DG P.105,168



Tacoma Pass (NVRAM) Disabling and termination guidelines (DG R0.7 p.322)
 If the Tacoma Pass interface is not used,
 the interface signals, including NV_ROMP,
 can be left as No connects with few exceptions.
 VccpMND, NV_ALE, NV_CLE

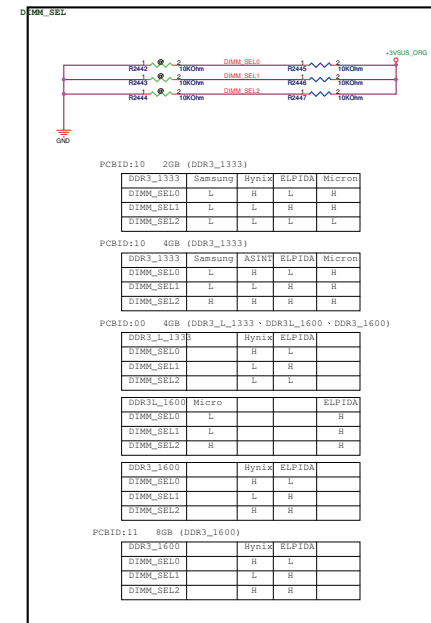
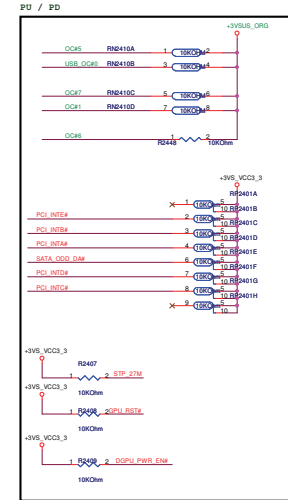
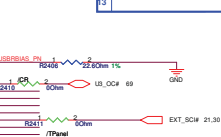
DMI & FDI Termination Voltage	
NV_CLE	LOW : Set to Vss
	HIGH : Set to Vcc

ER-018



USB2.0		USB 3.0	
0	USB 3.0 Port	1	USB 3.0 Port
1	USB 2.0 Port (Debug)	2	USB 3.0 Port
2		3	
3		4	
4	Camera		
5	WiFi/ WiMax/ Blue Tooth		
6			
7			
8	Touch Panel		
9	Card Reader		
10			
11			
12			
13			

ER-031



PCBID:10 2GB (DDR3_1333)	
DDR3_1333	Samsung Hynix ELPIDA Micron
DIMM_SEL0	L H L H
DIMM_SEL1	L L H H
DIMM_SEL2	L L L L

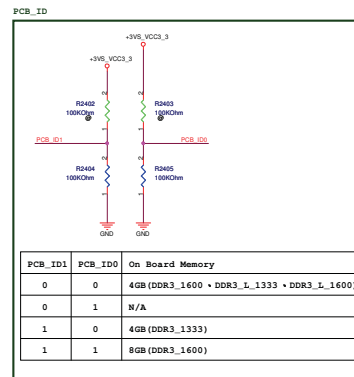
PCBID:10 4GB (DDR3_1333)	
DDR3_1333	Samsung ASINIX ELPIDA Micron
DIMM_SEL0	L H L H
DIMM_SEL1	L L H H
DIMM_SEL2	H H H H

PCBID:00 4GB (DDR3_L_1333 + DDR3L_1600 + DDR3_1600)	
DDR3_L_1333	Hynix ELPIDA
DIMM_SEL0	H L
DIMM_SEL1	L H
DIMM_SEL2	L L

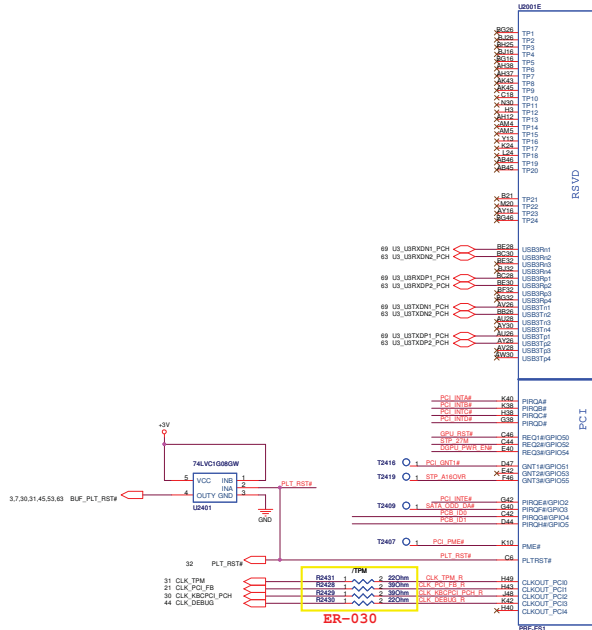
DDR3L_1600 Micron	
DIMM_SEL0	L
DIMM_SEL1	L
DIMM_SEL2	H

DDR3_1600 Hynix ELPIDA	
DIMM_SEL0	H L
DIMM_SEL1	L H
DIMM_SEL2	H H

PCBID:11 8GB (DDR3_1600)	
DDR3_1600	Hynix ELPIDA
DIMM_SEL0	H L
DIMM_SEL1	L H
DIMM_SEL2	H H



PCB_ID1	PCB_ID0	On Board Memory
0	0	4GB (DDR3_1600 + DDR3_L_1333 + DDR3_L_1600)
0	1	N/A
1	0	4GB (DDR3_1333)
1	1	8GB (DDR3_1600)



ER-030

Boot BIOS Strap : GNT1#, SATA1GP

Boot BIOS Strap		
GNT1#(BBS1)	SATA1GP(BBS2)	Boot BIOS Location
0	1	Reserved
1	0	PCI
1	1	SPT (PCR)
0	0	LPC

Sampled on rising edge of PWRCK.

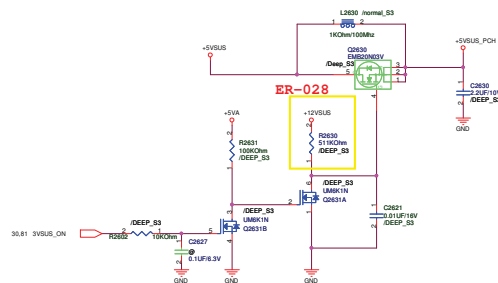
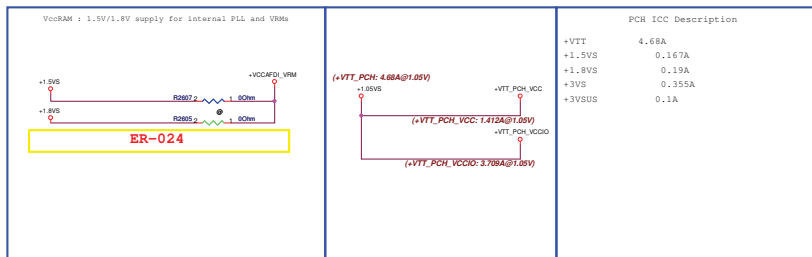
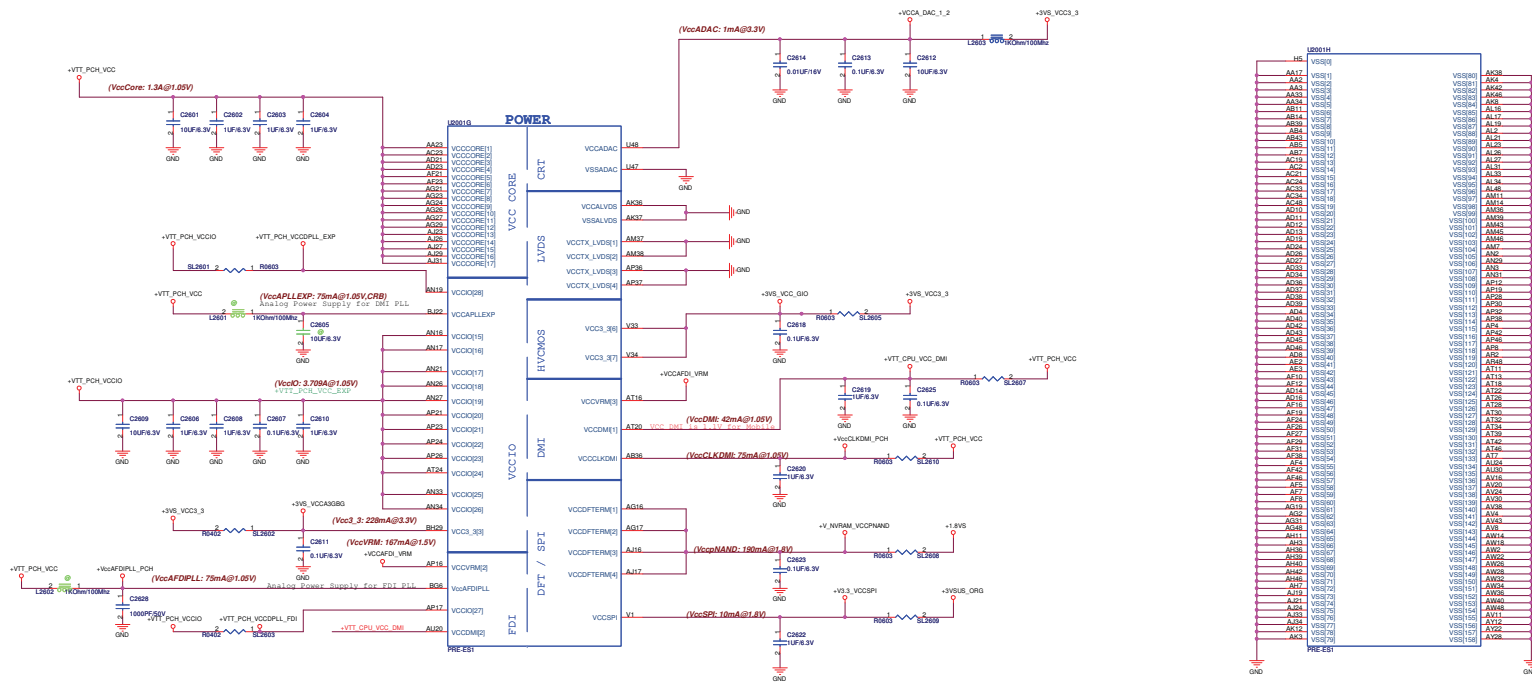
Default
PU 20K
OHM

GNT3#: A16 swap override Strap/
Top-Block swap override jumper

Low=Enabled A16 swap override/
Top-Block swap override

High=Default

All Beads : 0603 !!



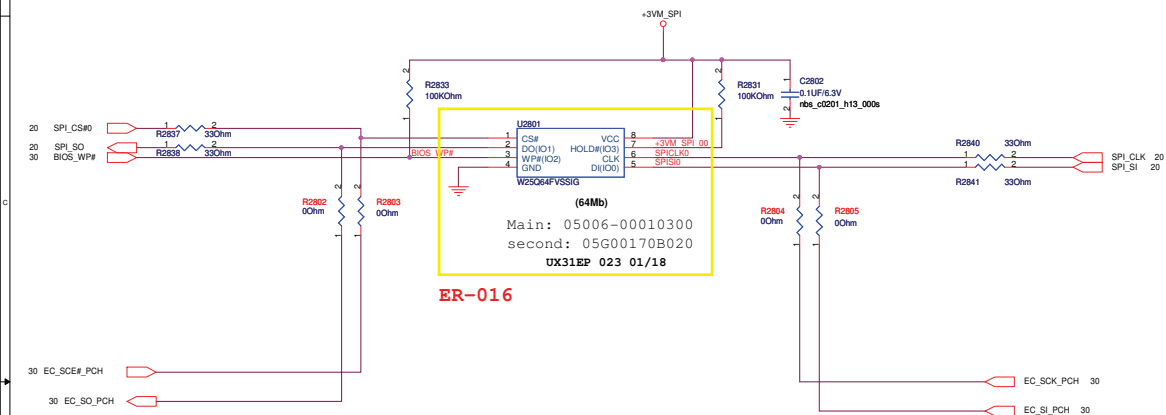
PCH SPI ROM

05/12 delete +3VA

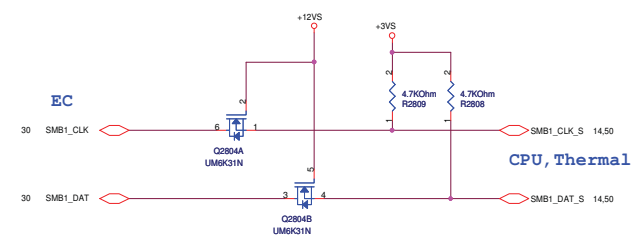
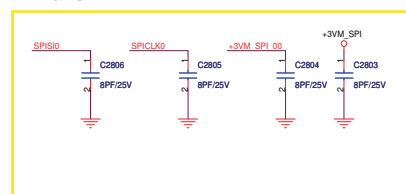
+3VSUS_ORG

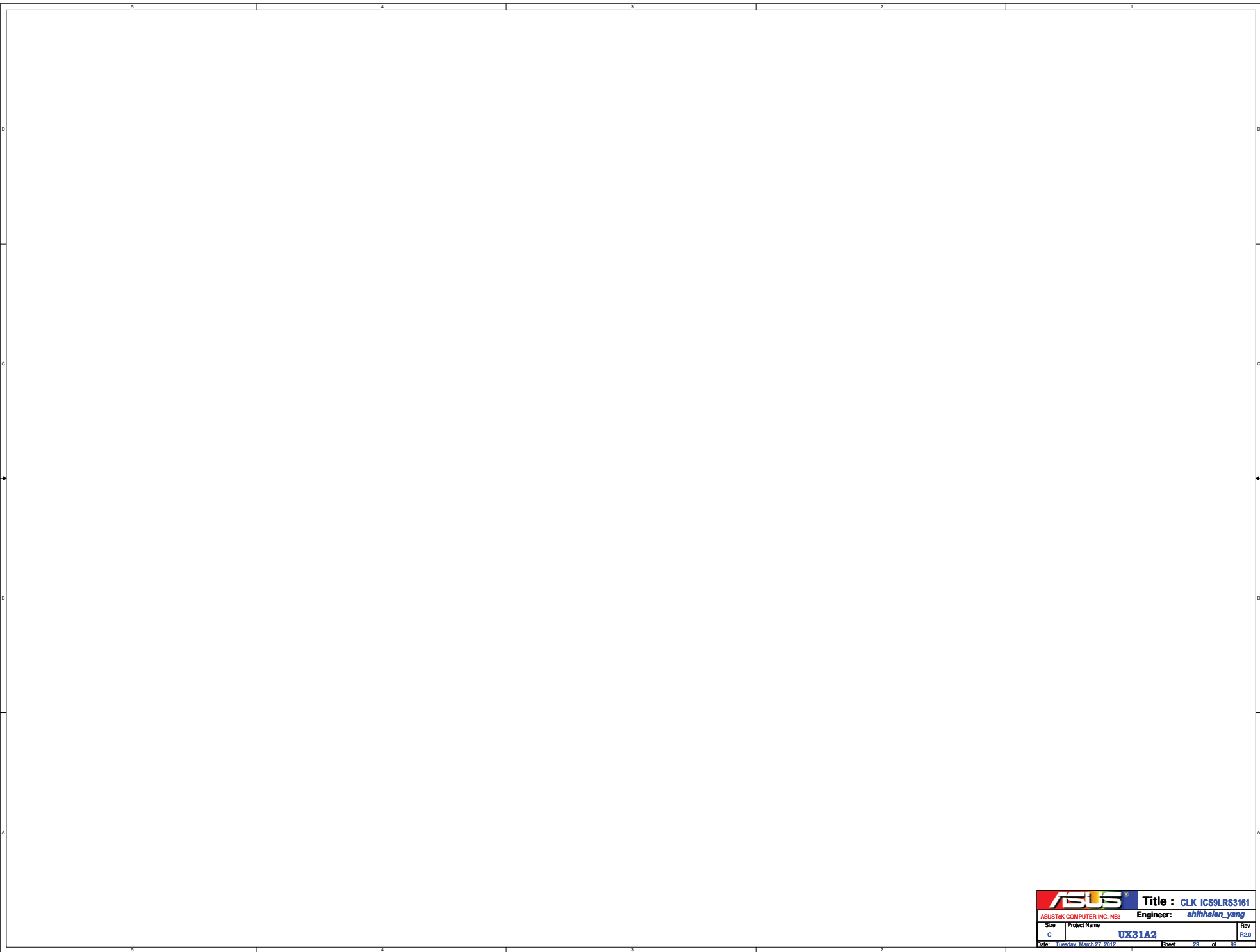
+3VM_SPI

Remove SPI FLASH TOOL CON



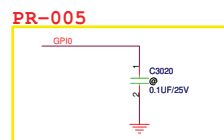
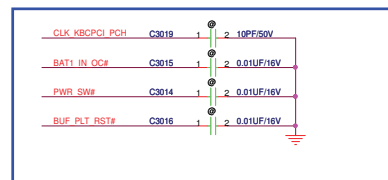
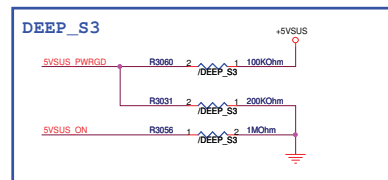
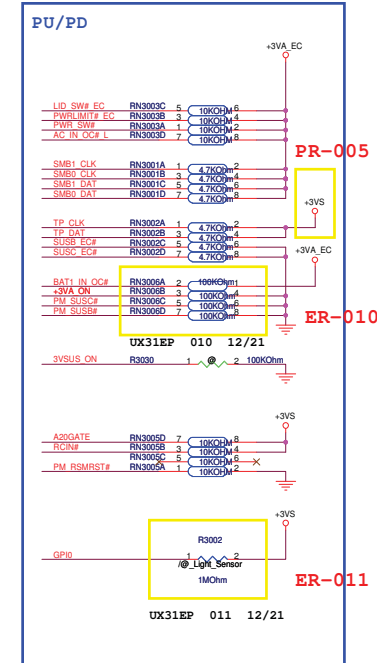
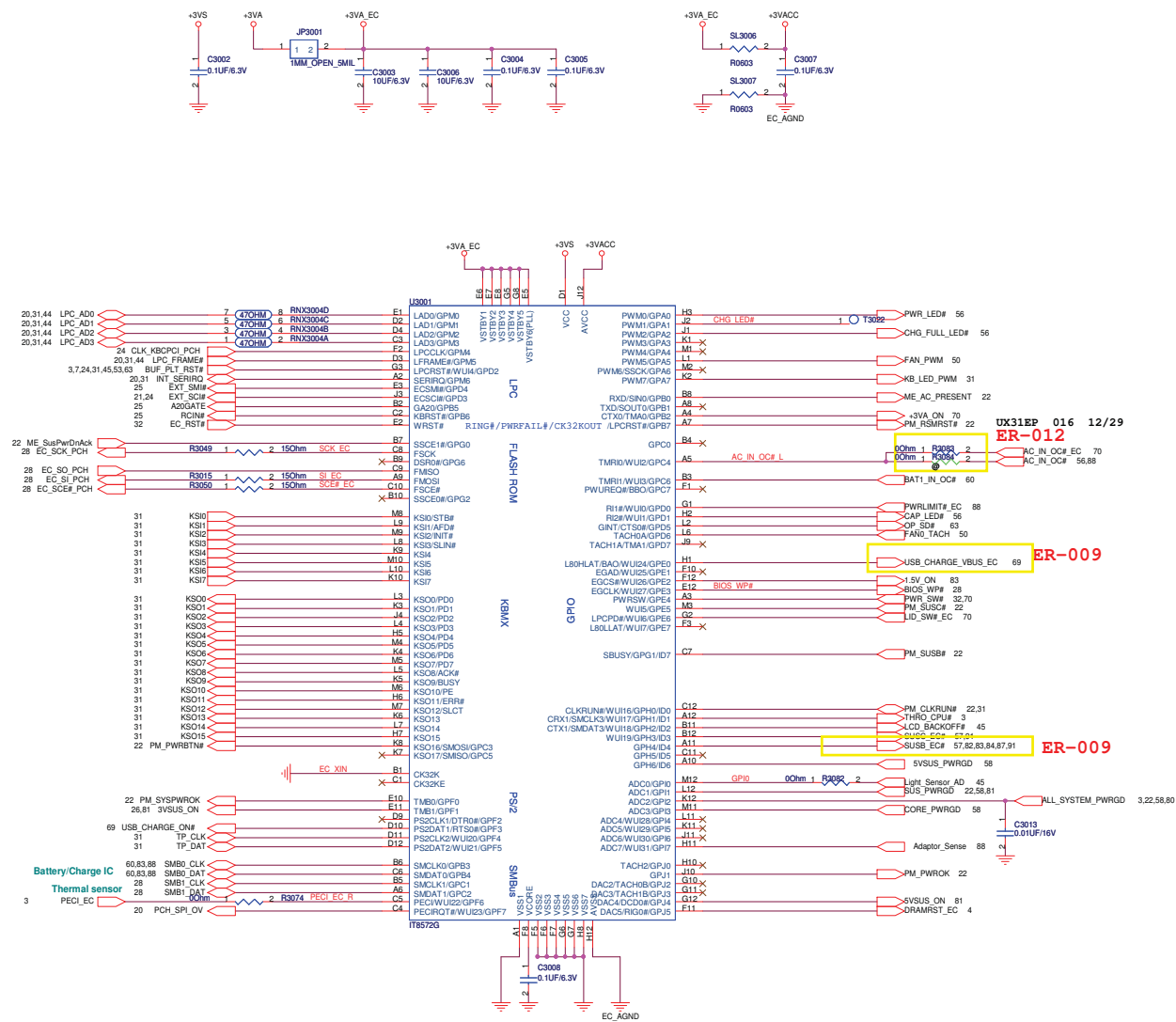
ER-025





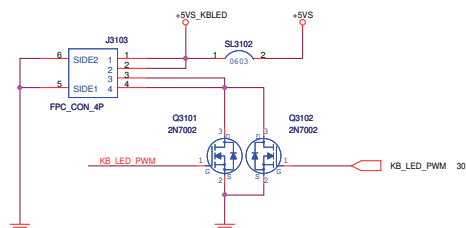
		Title : CLK_ICS9LR3161	
ASUSTek COMPUTER INC. NBS		Engineer: shihhsien_yang	
Size	Project Name	Rev	
C	UX31A2	R2.0	
Date: Tuesday, March 27, 2012		Sheet 26 of 99	

Main Board

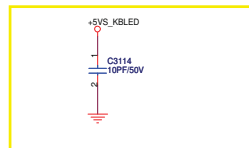


Keyboard

BL_CON

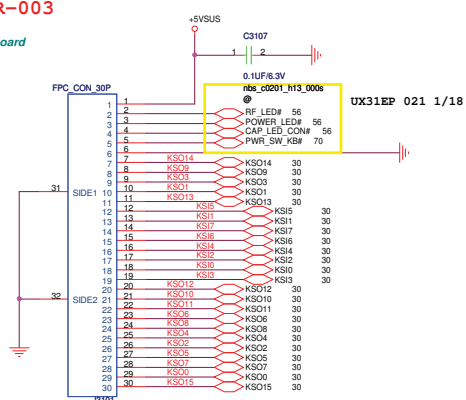


PR-009

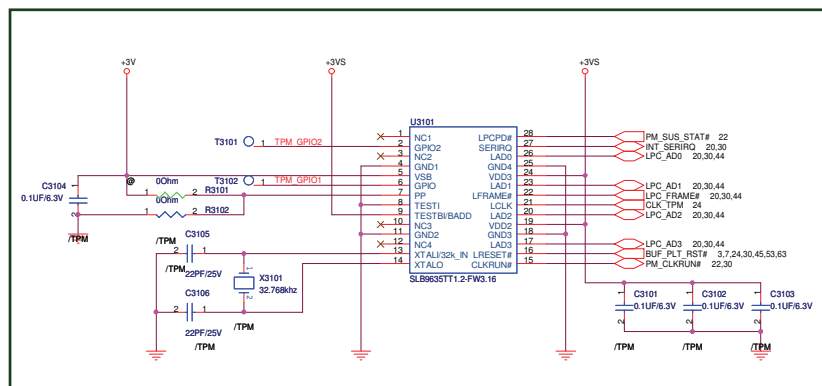


ER-003

Keyboard



TPM



ClickPad Schematic

BOM Note

Normal TP option -> /PS2TP

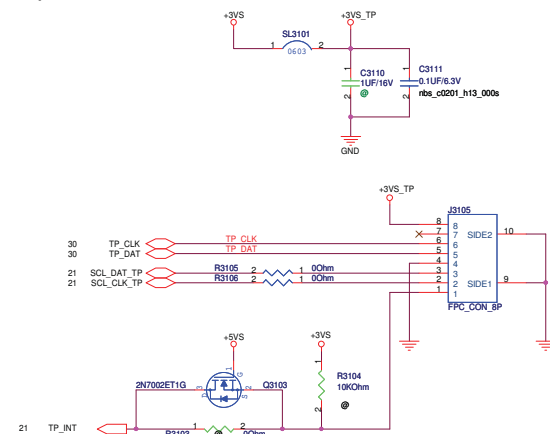
ELAN SMBUS TP option

Synaptics SMBUS TP option

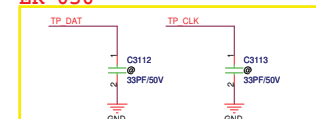
click pad option is for win8 requirement Function

PR-005

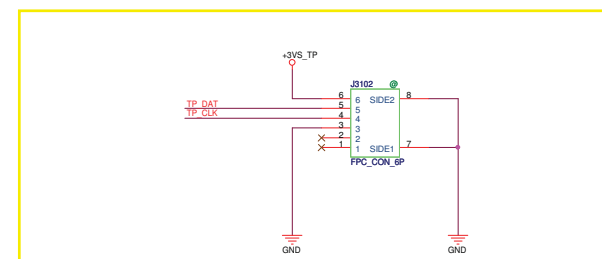
T/P



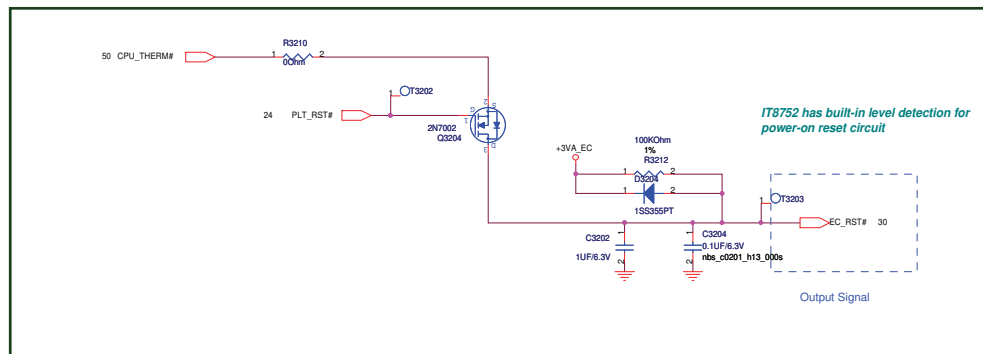
ER-036



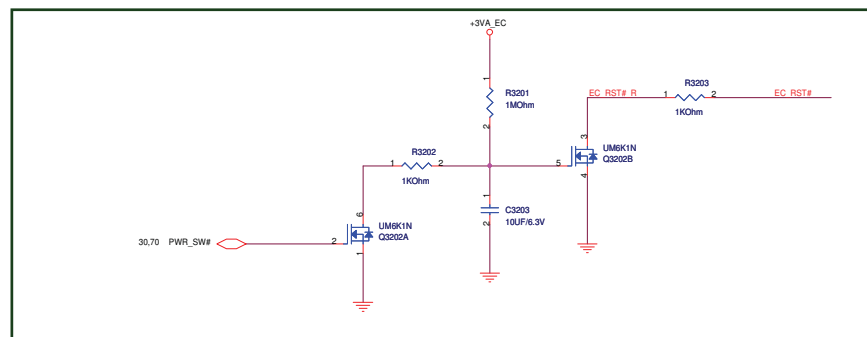
PR-010

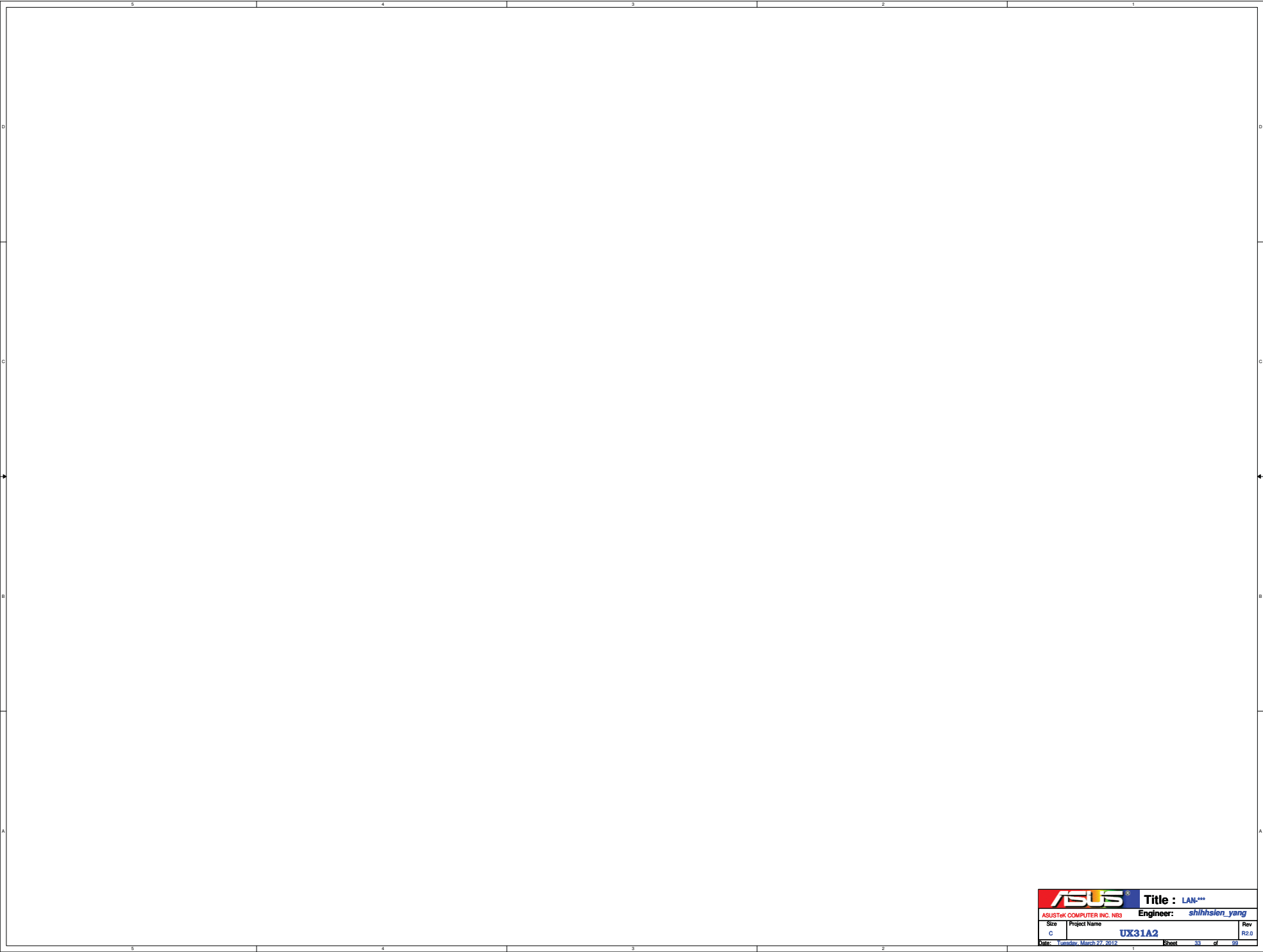


Thermal Policy



battery embedded (press pwr_sw 10sec, then reset ec)





**ASUS**[®]

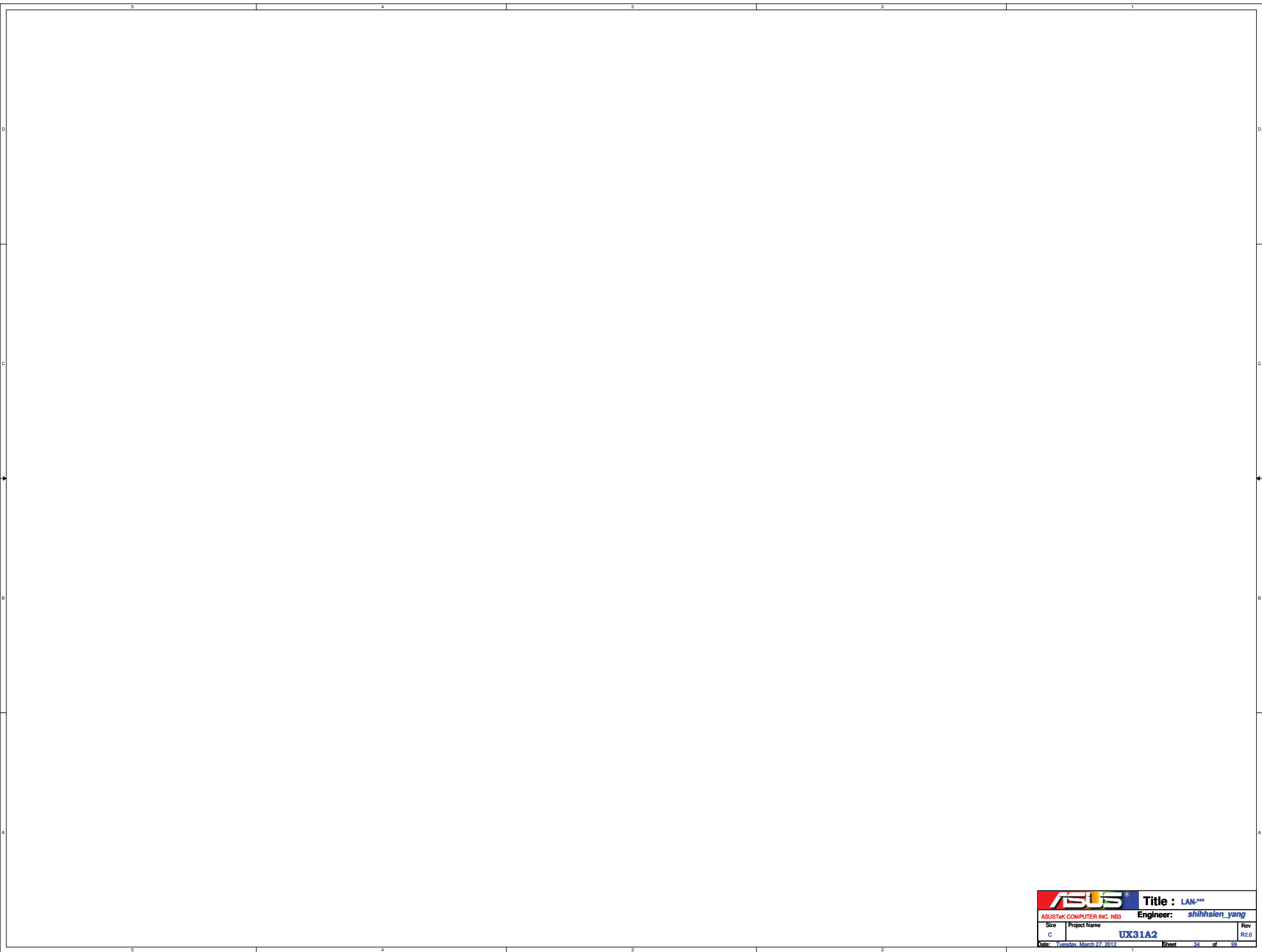
ASUSTeK COMPUTER INC. NBS

Title : LAN***

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

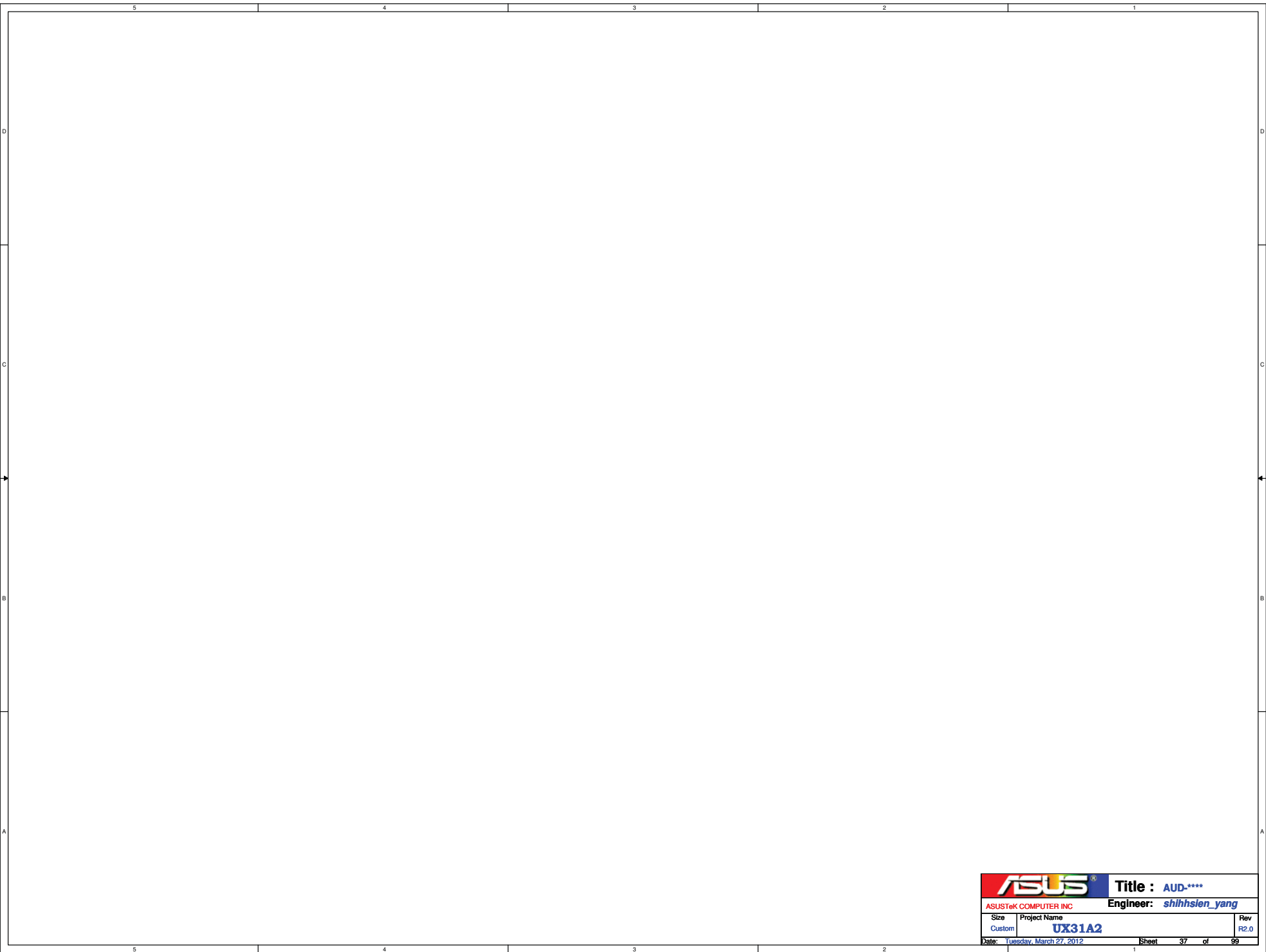
Date: Tuesday, March 27, 2012Sheet 33 of 99



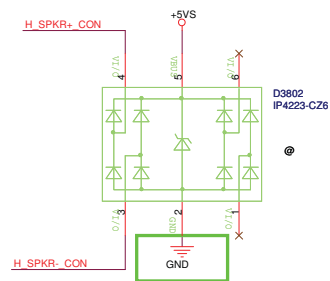
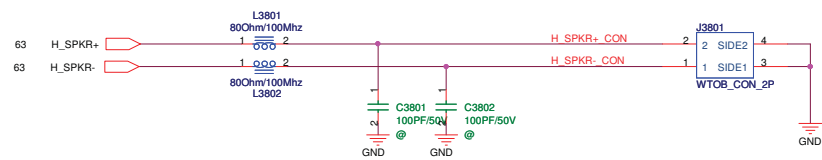
		Title : LAN***	
ASUSTek COMPUTER INC. NBS		Engineer: shihhsien_yang	
Size	Project Name	Rev	
C	UX31A2	R2.0	
Date: Tuesday, March 27, 2012		Sheet 34 of 99	

The image shows a standard architectural or engineering drawing sheet. It features a large rectangular area defined by a grid. The horizontal axis at the top and bottom is labeled with letters A, B, C, D, and E from left to right. The vertical axis on the left side is labeled with letters A, B, C, and D from bottom to top. This creates a grid of columns and rows. In the bottom right corner, there is a designated area for project information, which includes fields for the company name (ASUSTek COMPUTER INC), project name (UX31A2), date (Tuesday, March 27, 2012), sheet number (36 of 99), and engineer's name (shihhsien_yang). The title field contains the text "Title :AUD.***".

ASUSTek COMPUTER INC		Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012	Sheet 36	of 99		

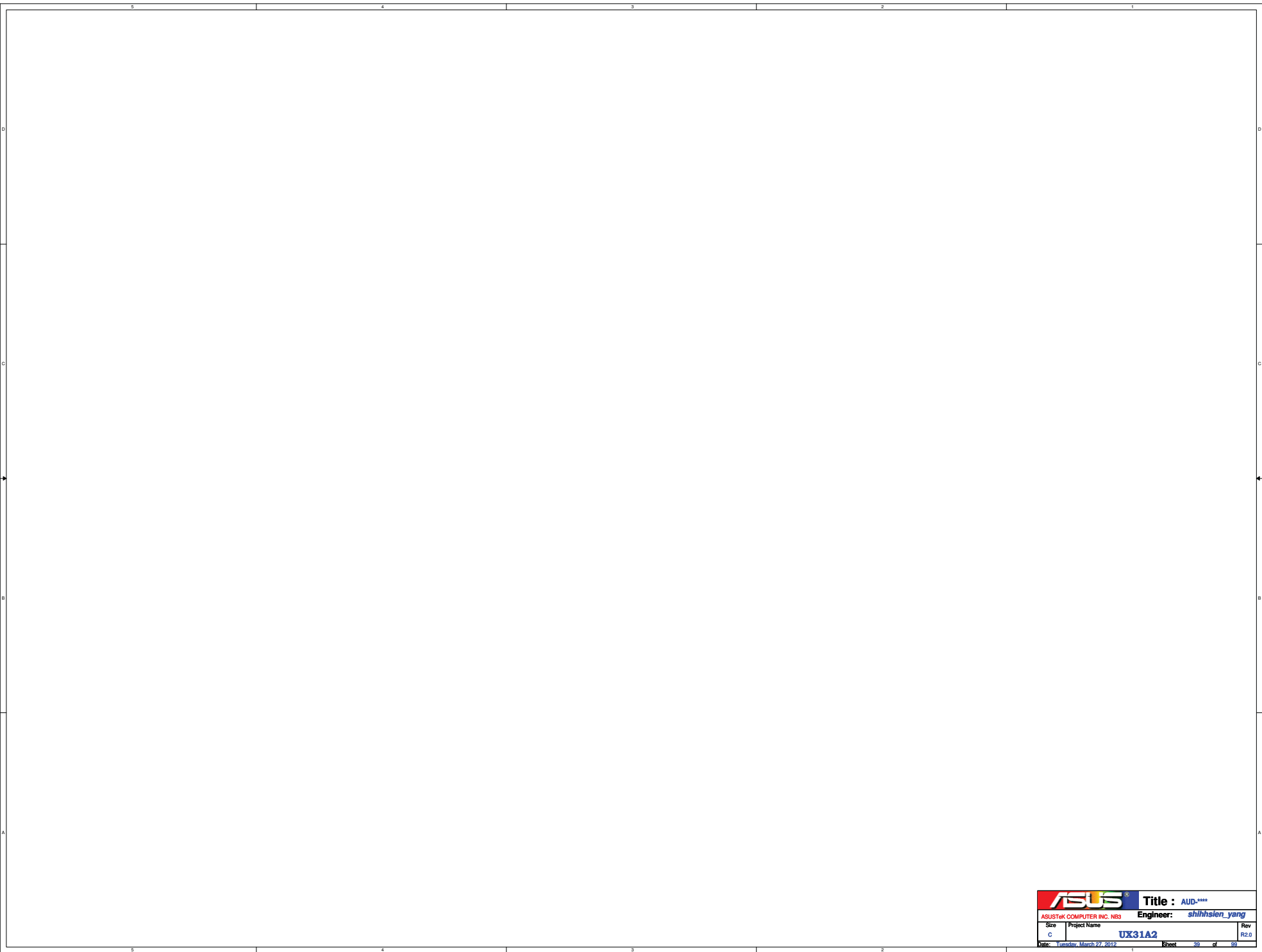


		Title : AUD-****	
ASUSTeK COMPUTER INC		Engineer: shihhsien_yang	
Size Custom	Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012		Sheet 37 of 99	



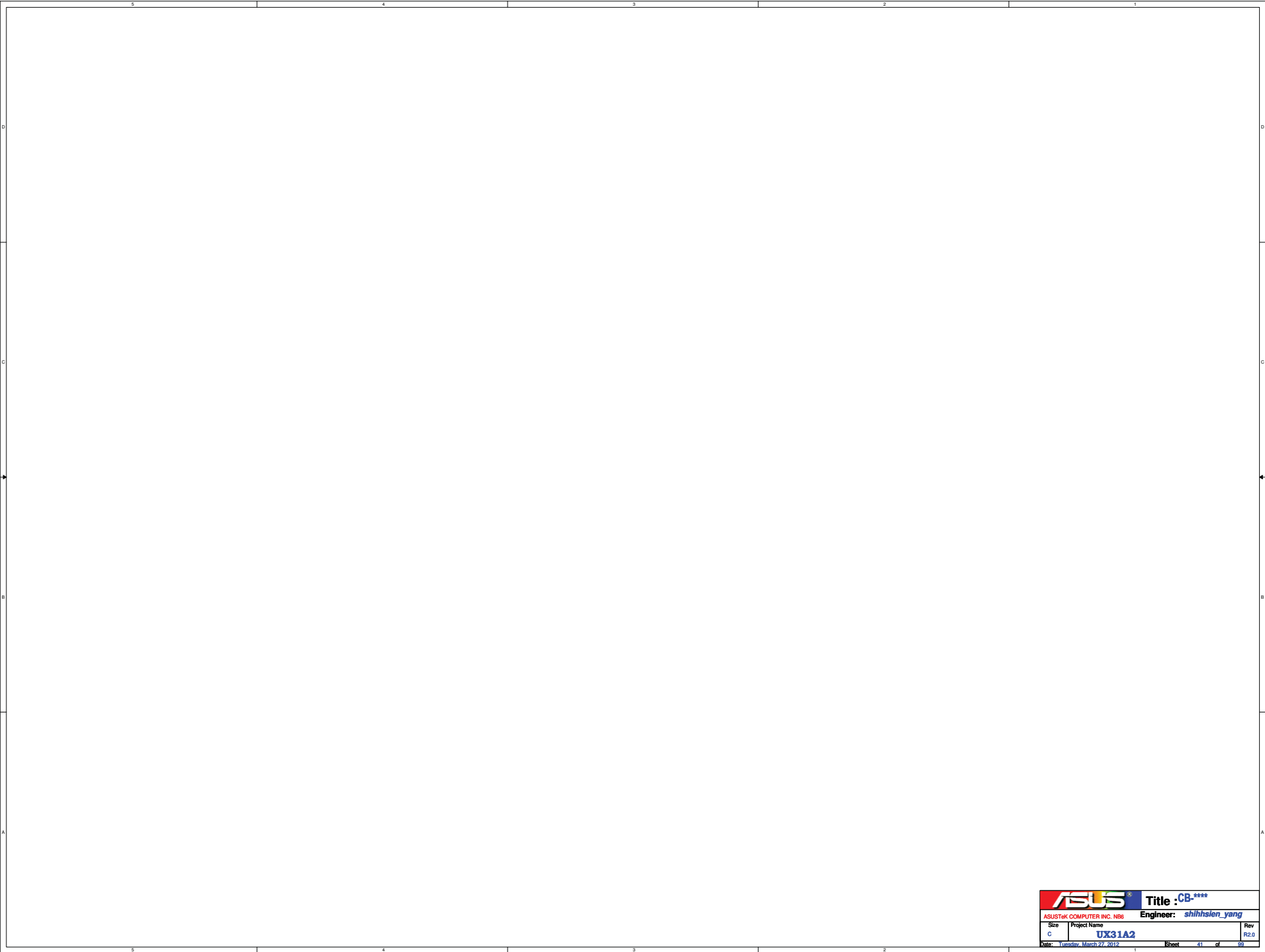
<Variant Name>

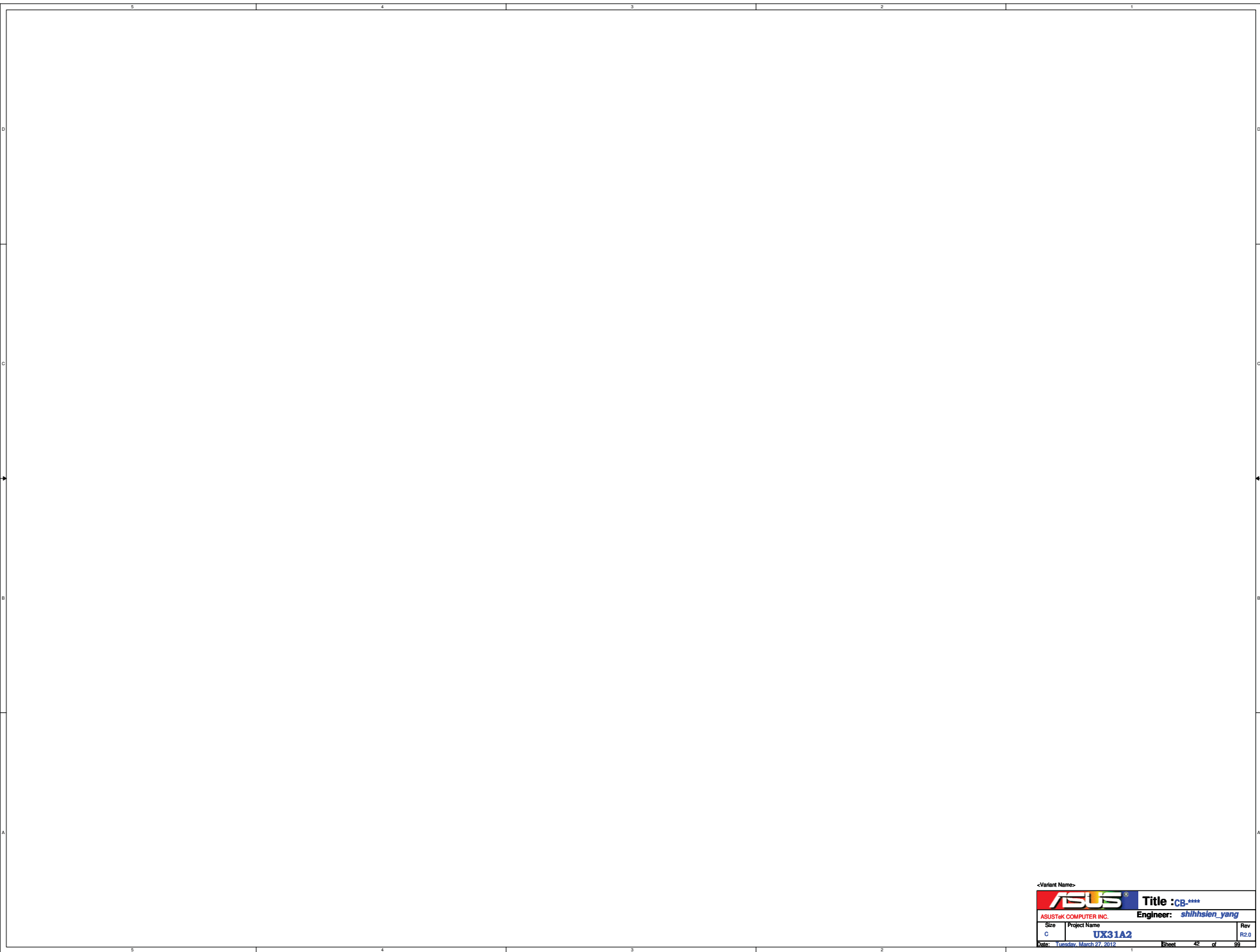
ASUS		Title :AUD SPK-R CONN	
ASUSTek COMPUTER INC		Engineer: shihhsien_yang	
Size	Project Name		Rev
Custom	UX31A2		R2.0
Date: Tuesday, March 27, 2012		Sheet 38 of 99	



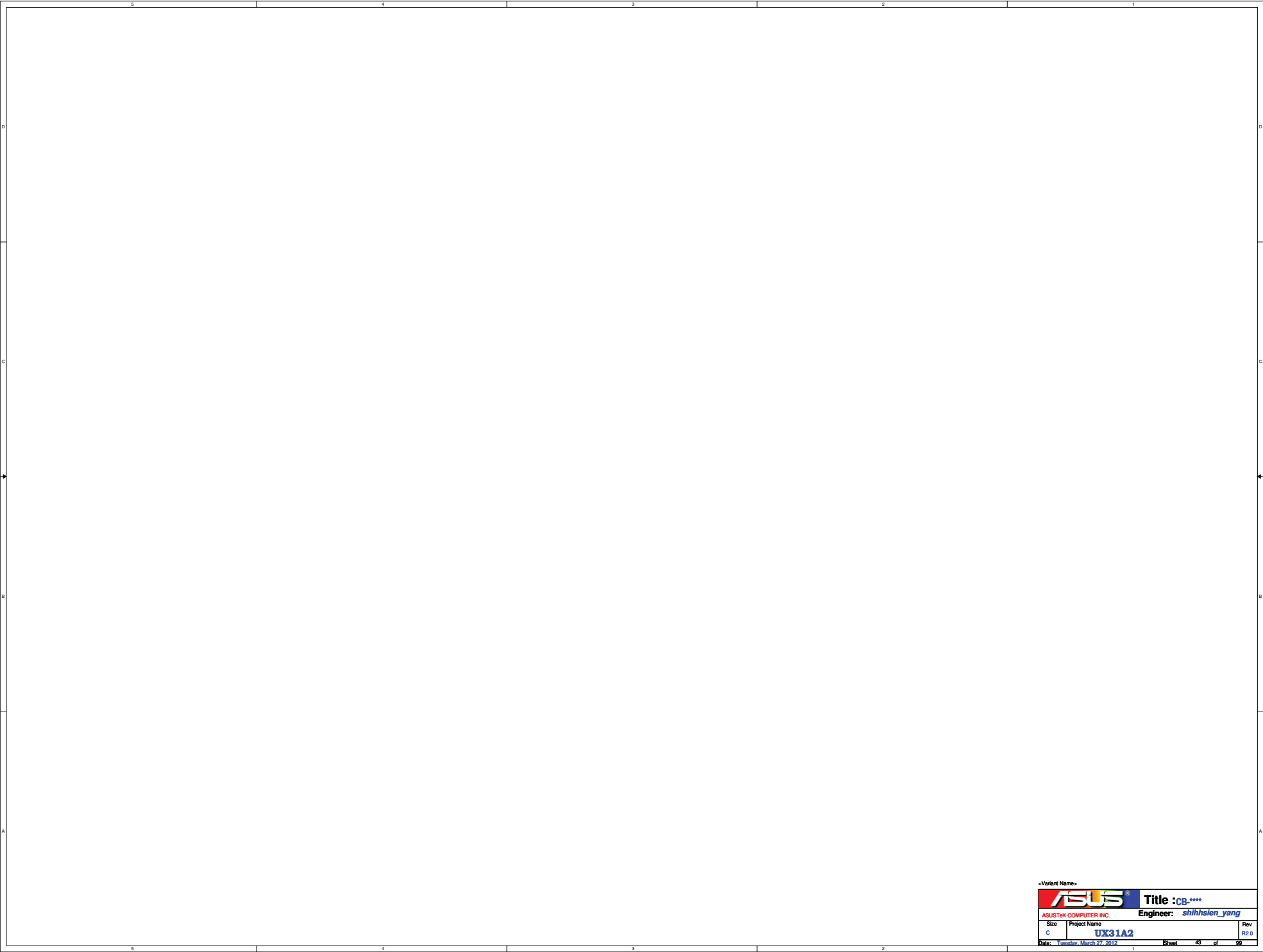
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : CB-****	
ASUSTeK COMPUTER INC. NB6		Engineer: <i>shihhsien_yang</i>	
Size A	Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012		Sheet	40 of 99



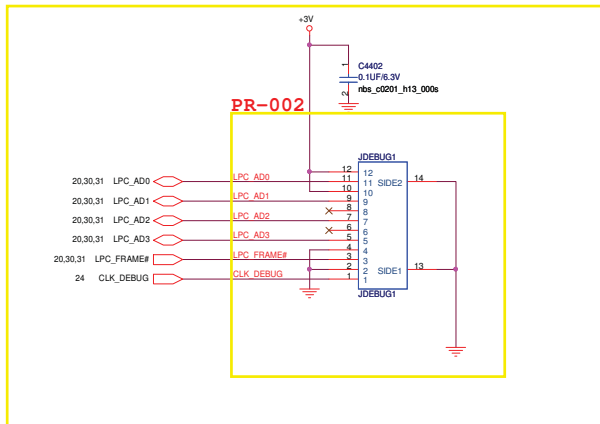


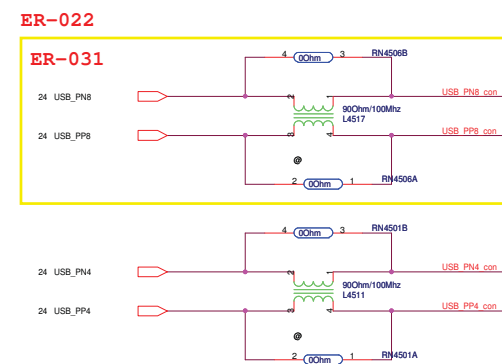
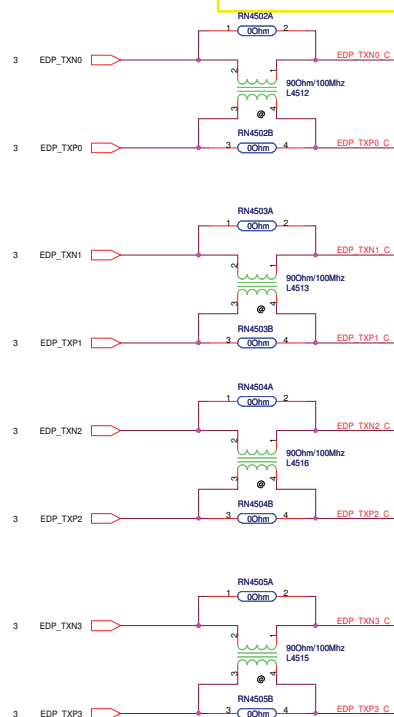
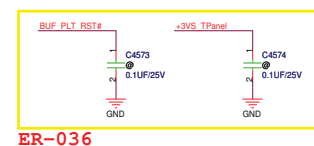
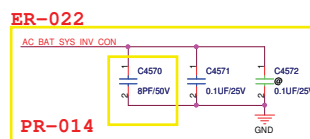
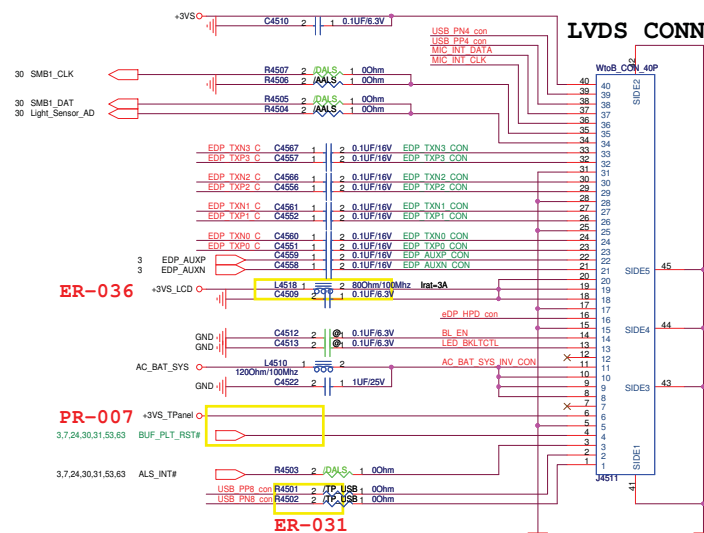
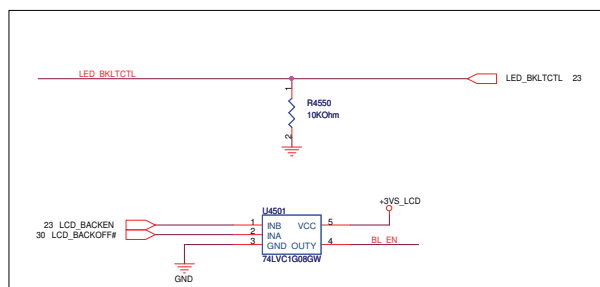
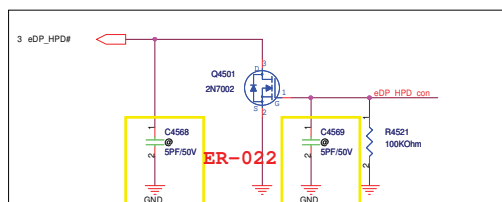
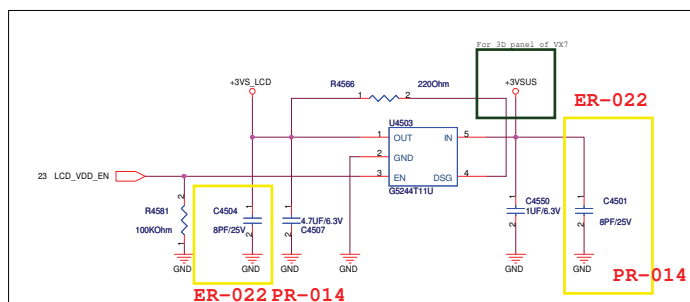
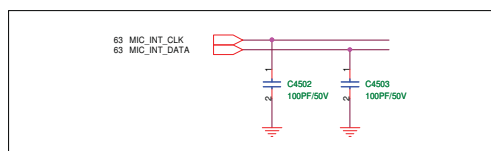
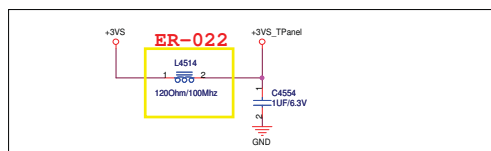
<Variant Name>			
		Title :CB-****	
ASUSTek COMPUTER INC.		Engineer : shihhsien_yang	
Size	Project Name	Rev	
C	UX31A2	R2.0	
Date : Tuesday, March 27, 2012		Sheet 42 of 99	



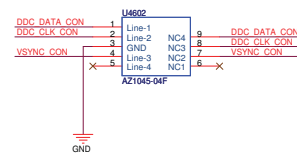
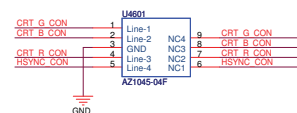
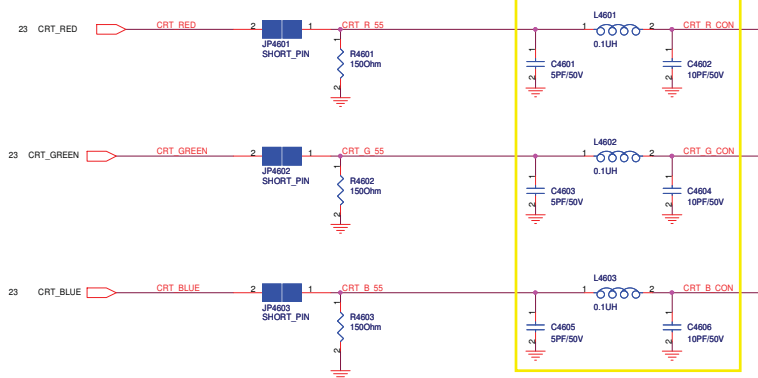
LPC Debug Port

PR-013



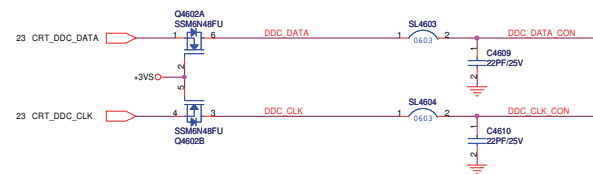
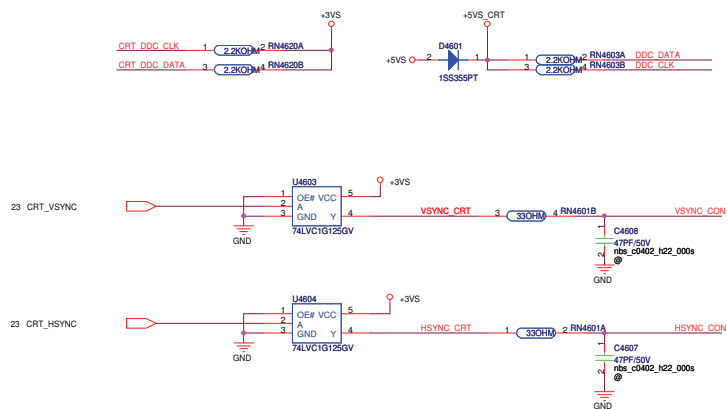
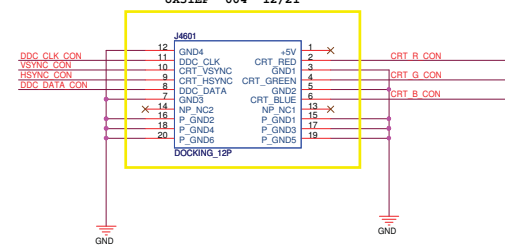


ER-030

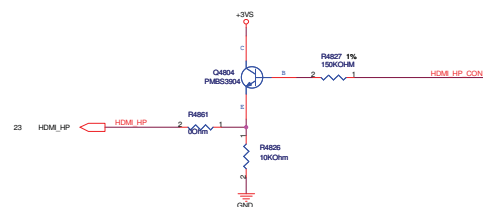
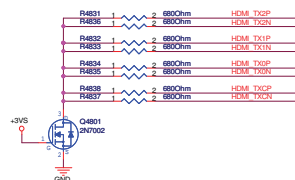
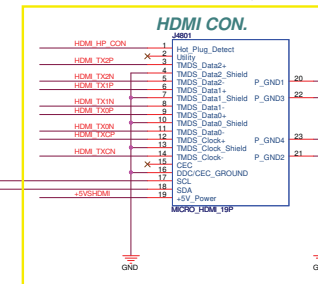
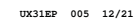
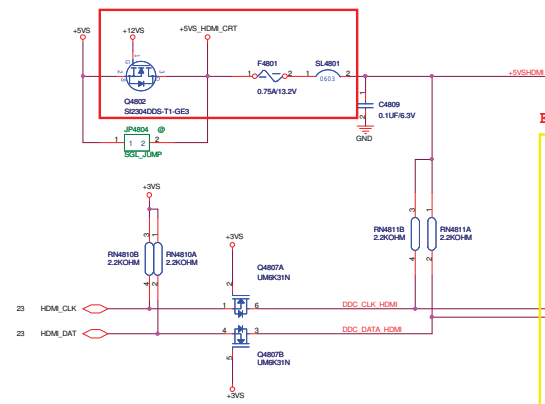
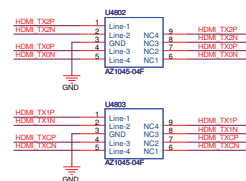


ER-004

UX31EP 004 12/21

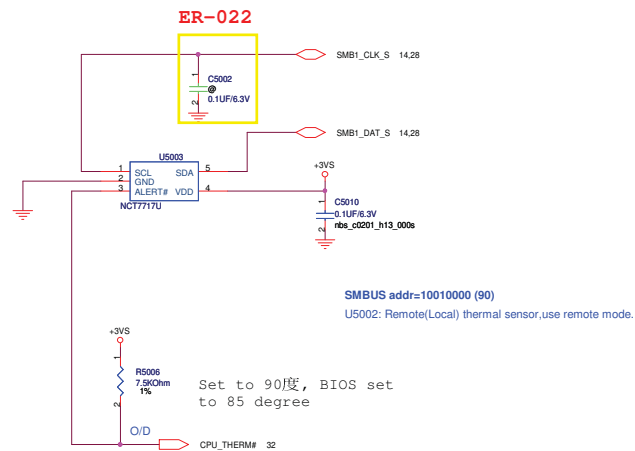


Near CON J4801



Main Board

CPU Thermal Sensor

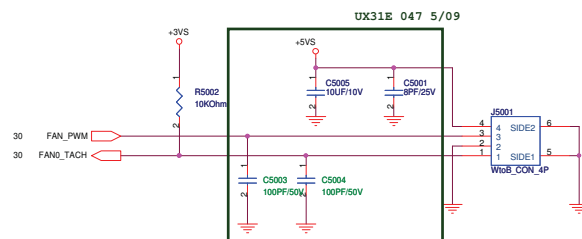


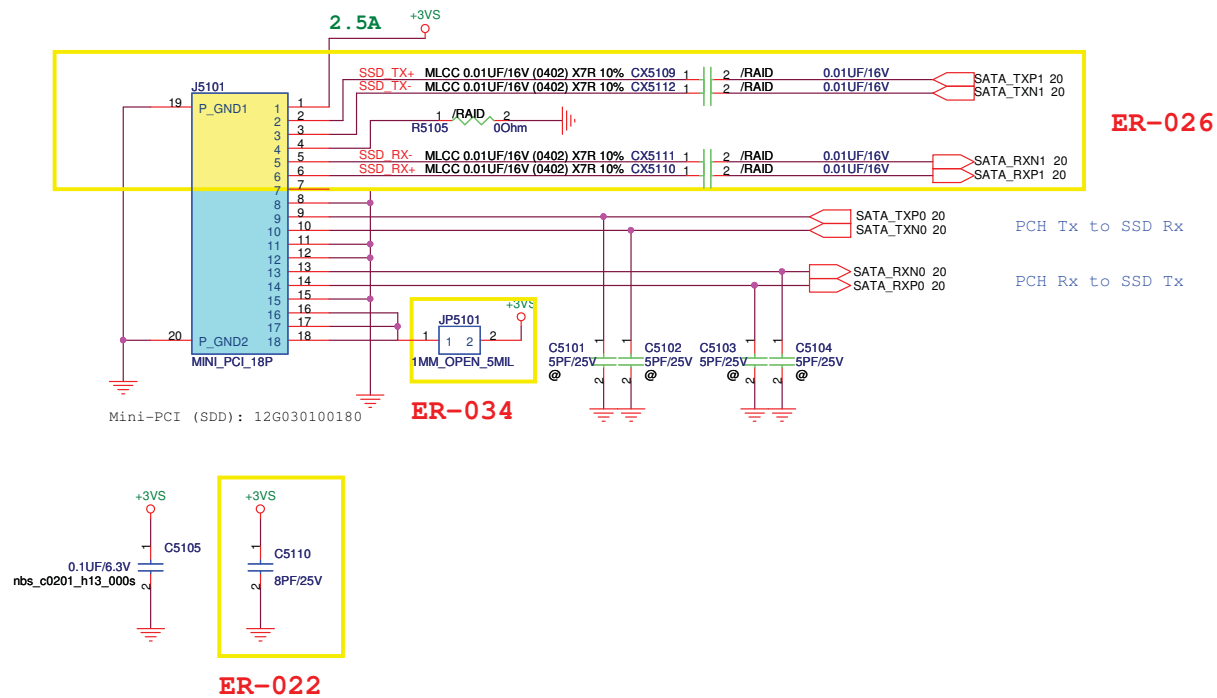
Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS

Avoid FSB,Power

DC FAN Control





ASUS		Title : MiniCard_SSD	
ASUSTeK COMPUTER INC. NB4		Engineer: shihhsien_yang	
Size B	Project Name UX31A2	Rev R2.0	
Date: Friday, May 18, 2012		Sheet	51 of 99

Main Board



Title : USB_USB Port*3

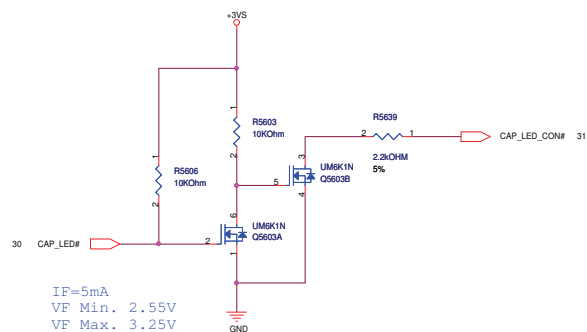
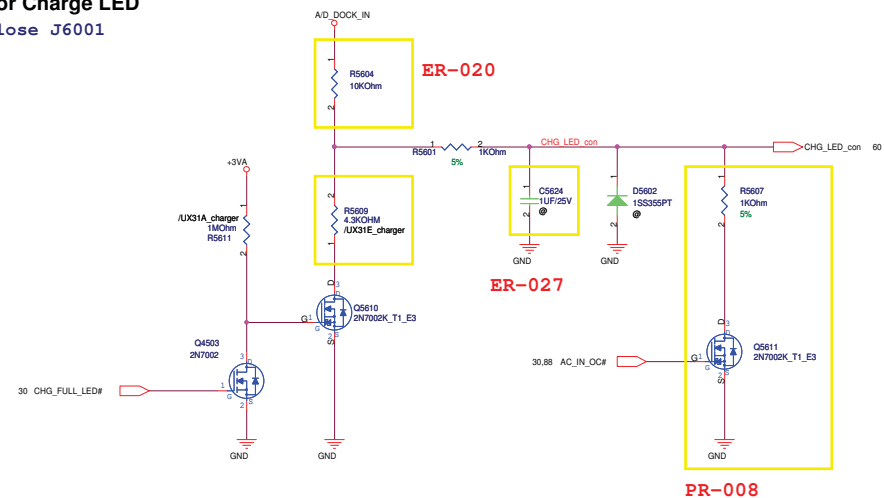
Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0
Date: Tuesday, March 27, 2012		Sheet 52 of 99

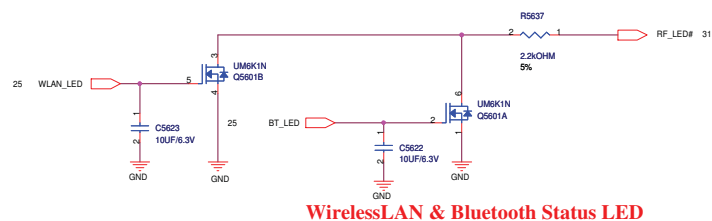
Main Board

Main Board

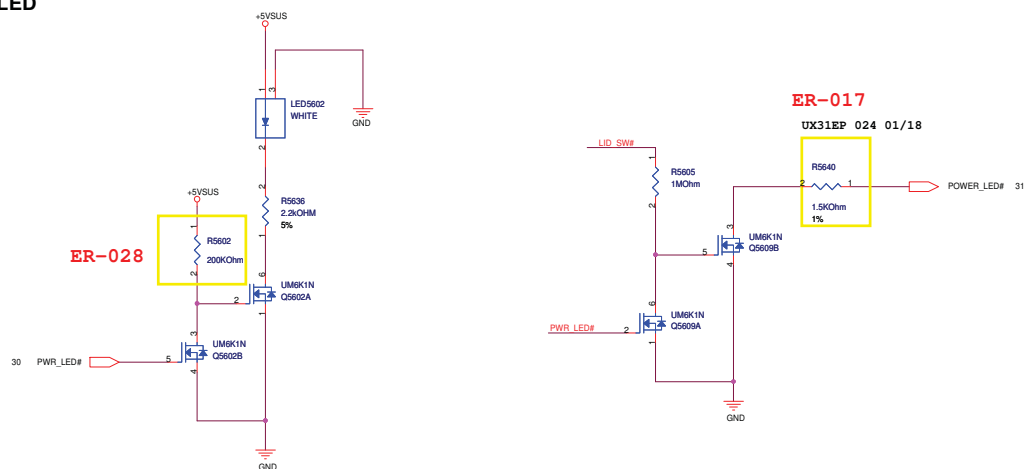
CAPS_LOCK LED

For Charge LED
Close J6001

WireLess/BT LED

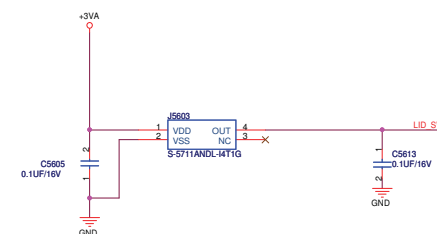


PWR LED

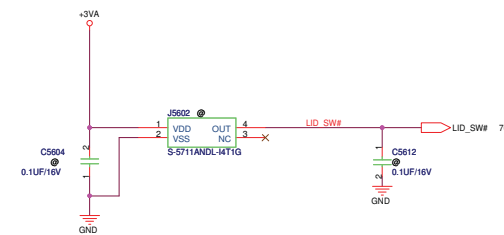


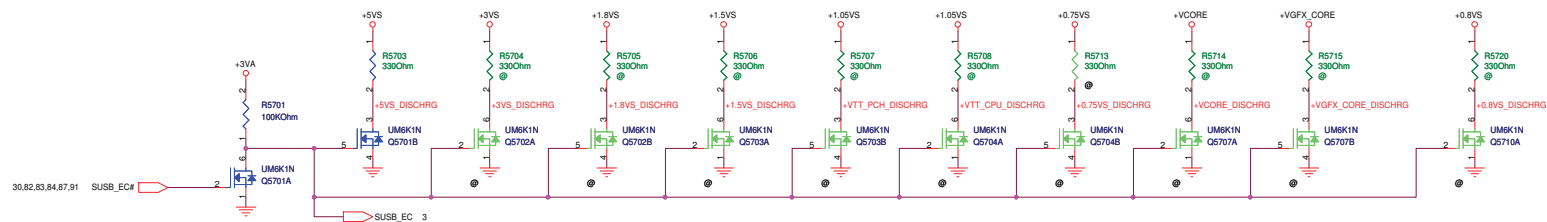
PR-003

LID SW (no TouchPanel)

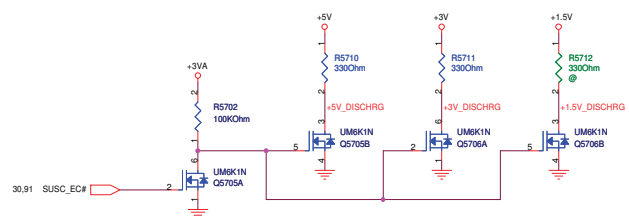


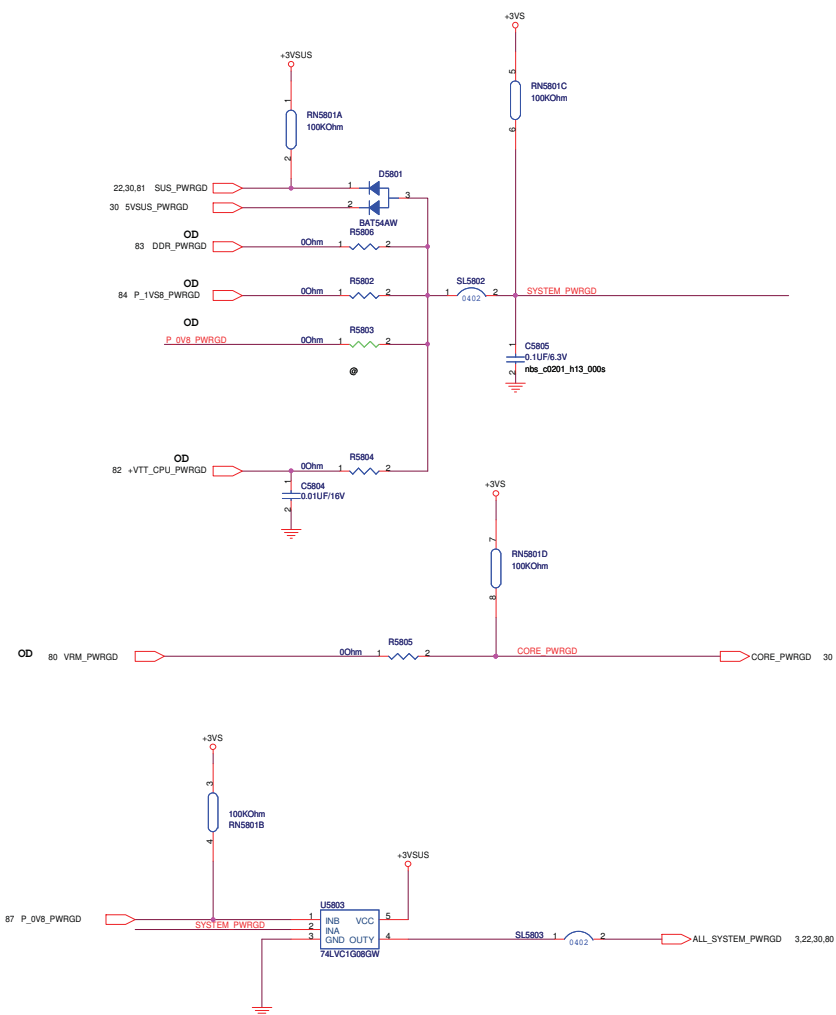
LID SW (for TouchPanel)





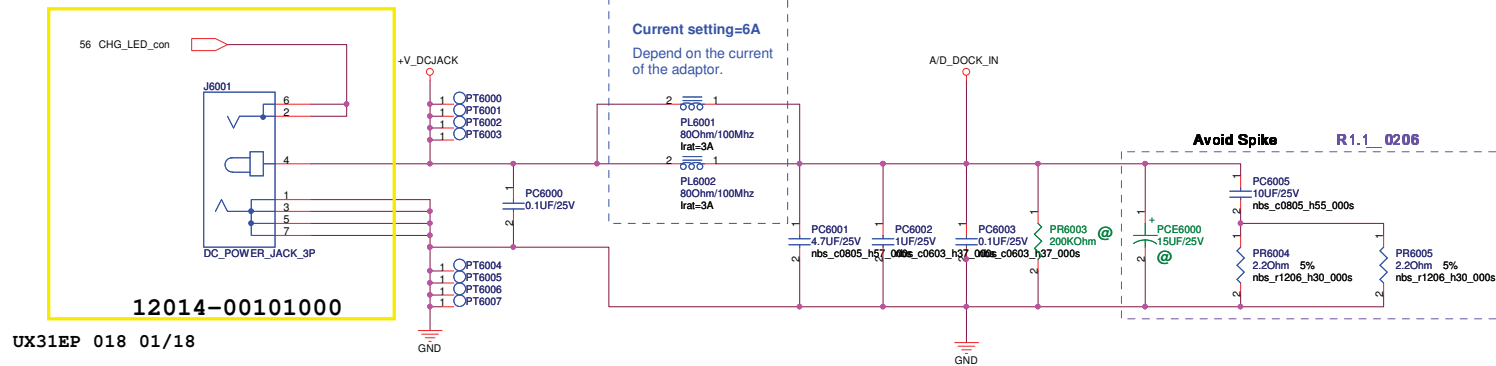
4/20 Stuff R5710 and R5711



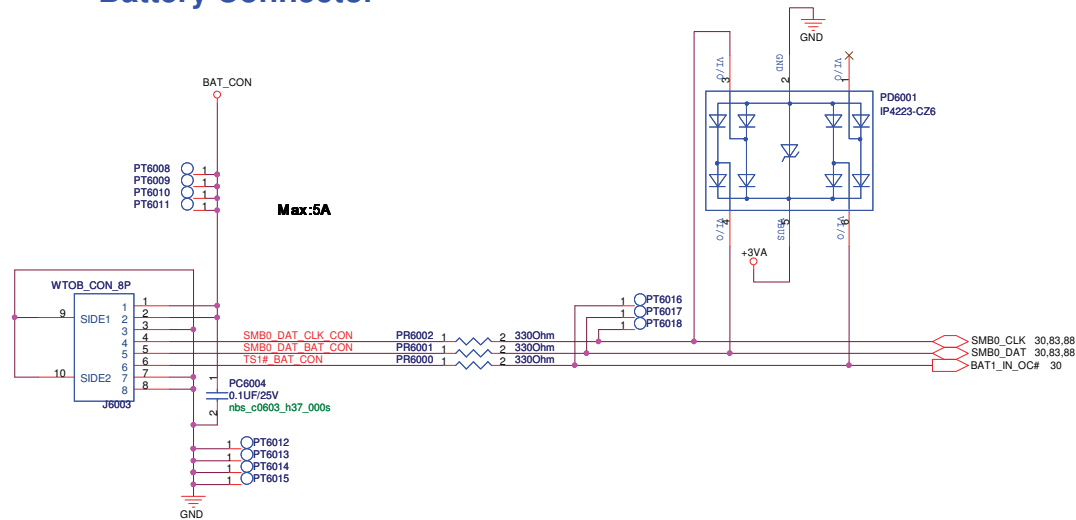


Main Board

ER-015



Battery Connector





		Title : BT	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>shihhsien_yang</i>	
Size	Project Name		Rev
Custom	UX31A2		R2.0
Date: Tuesday, March 27, 2012	Sheet 61 of 99		

Main Board



ASUSTeK COMPUTER INC. NBM

Size: C

Title: **UX31A2**

Project Name: **UX31A2**

Engineer: **shihhsien yang**

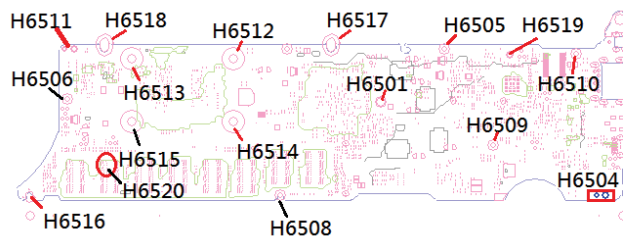
Date: **Tuesday, March 27, 2012**

Rev: **R2.0**

Sheet: **62** of **99**

Main Board

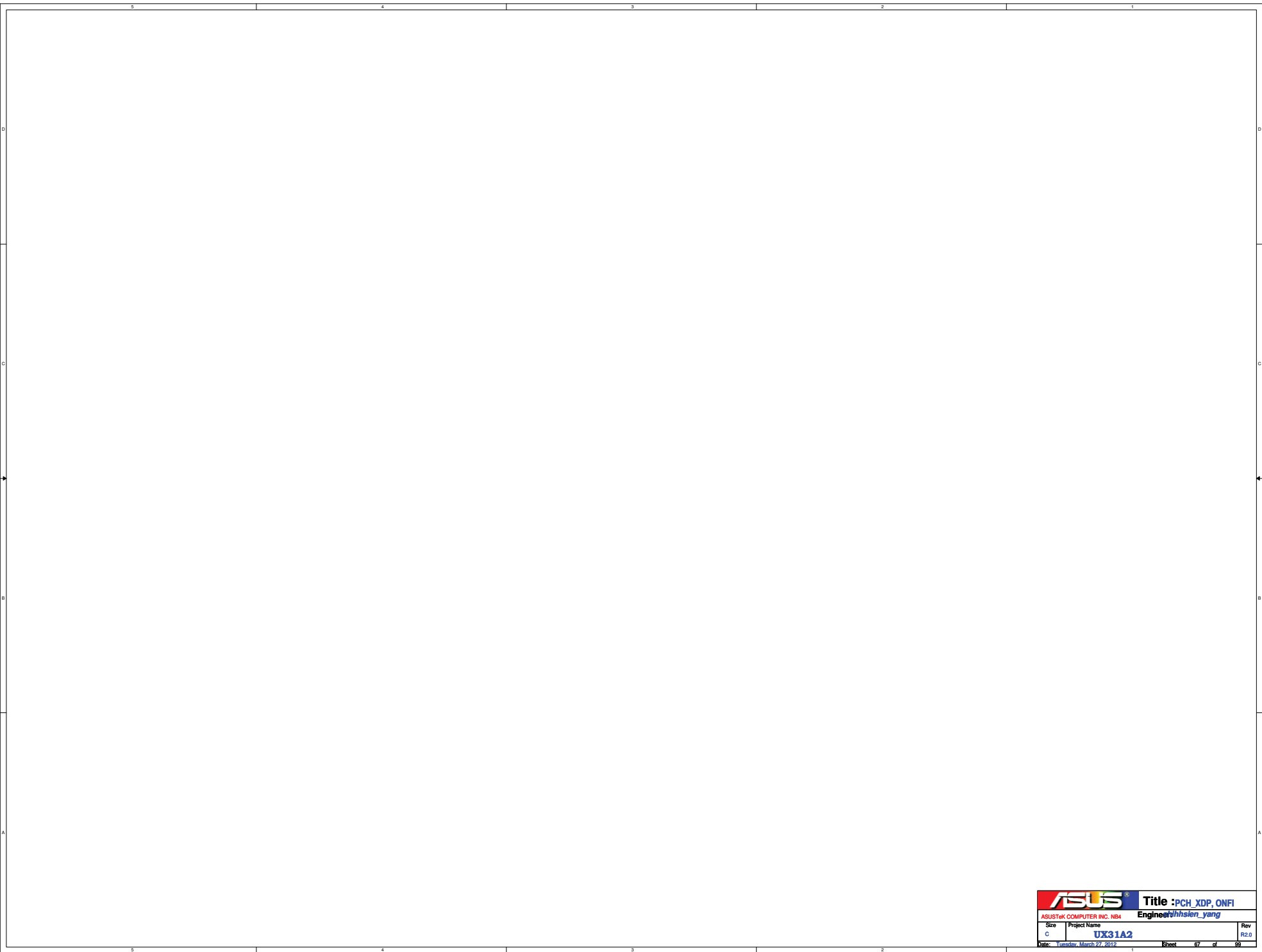
A schematic diagram showing a component represented by a blue circle with a smaller blue circle inside. The component is labeled "H6520" above it and "CT217CS140D110" to its right. A red line connects the bottom of the component to a ground symbol, which is labeled "GND".



UX31EP 002 12/21

ER-002

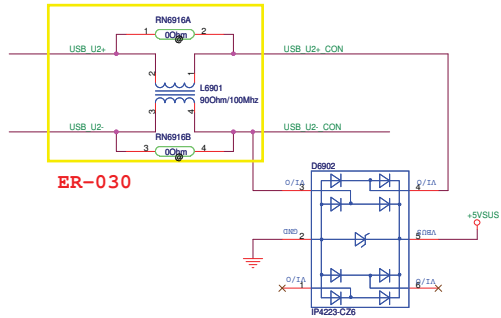
Main Board



ER-013

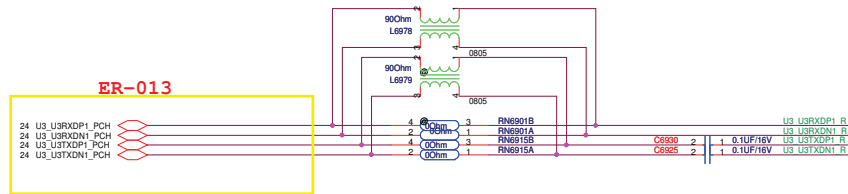
		Title : ****	
ASUSTek COMPUTER INC. NBS		Engineer: <i>Susi_Hong</i>	
Size	Project Name	Rev	
C	UX31A2	R2.0	
Date: Tuesday, March 27, 2012		Sheet 08 of 09	

USB2.0 EMI-Protection & ESD-Protection



ER-030

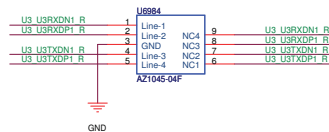
USB3.0 EMI-Protection



ER-013

USB3.0 ESD-Protection

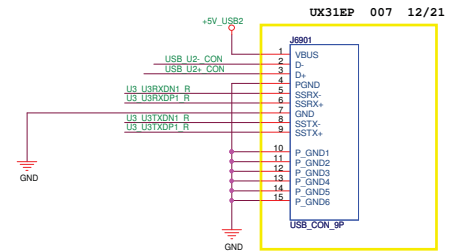
1st : 07G028076030
ESD PROTECTION AZ1045-04F
2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB



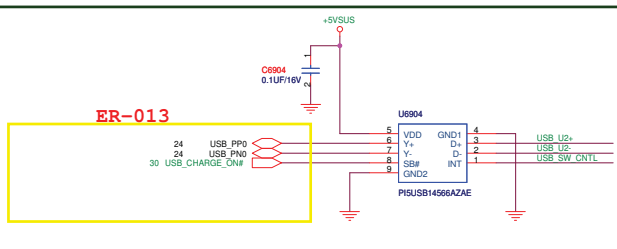
USB30 CONN

USB30 CONN

UX21 CON 12013-00011600



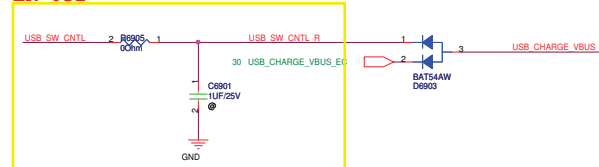
USB Charger



ER-013

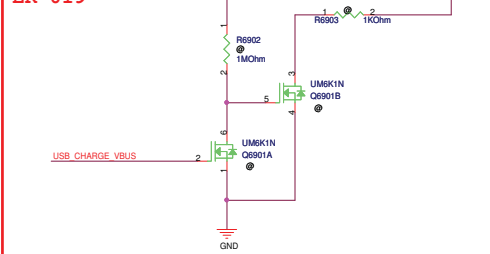
Charger_pwr_control & DC mode low voltage control

ER-032

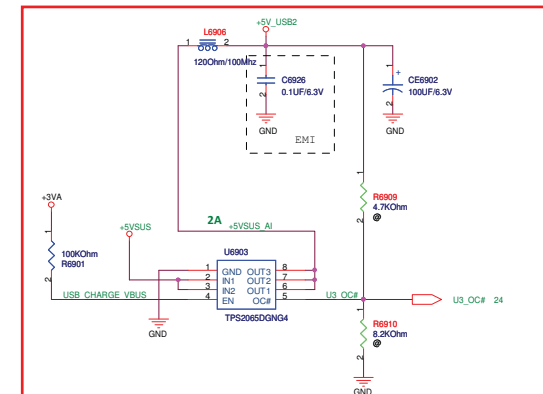


VBUS_discharger

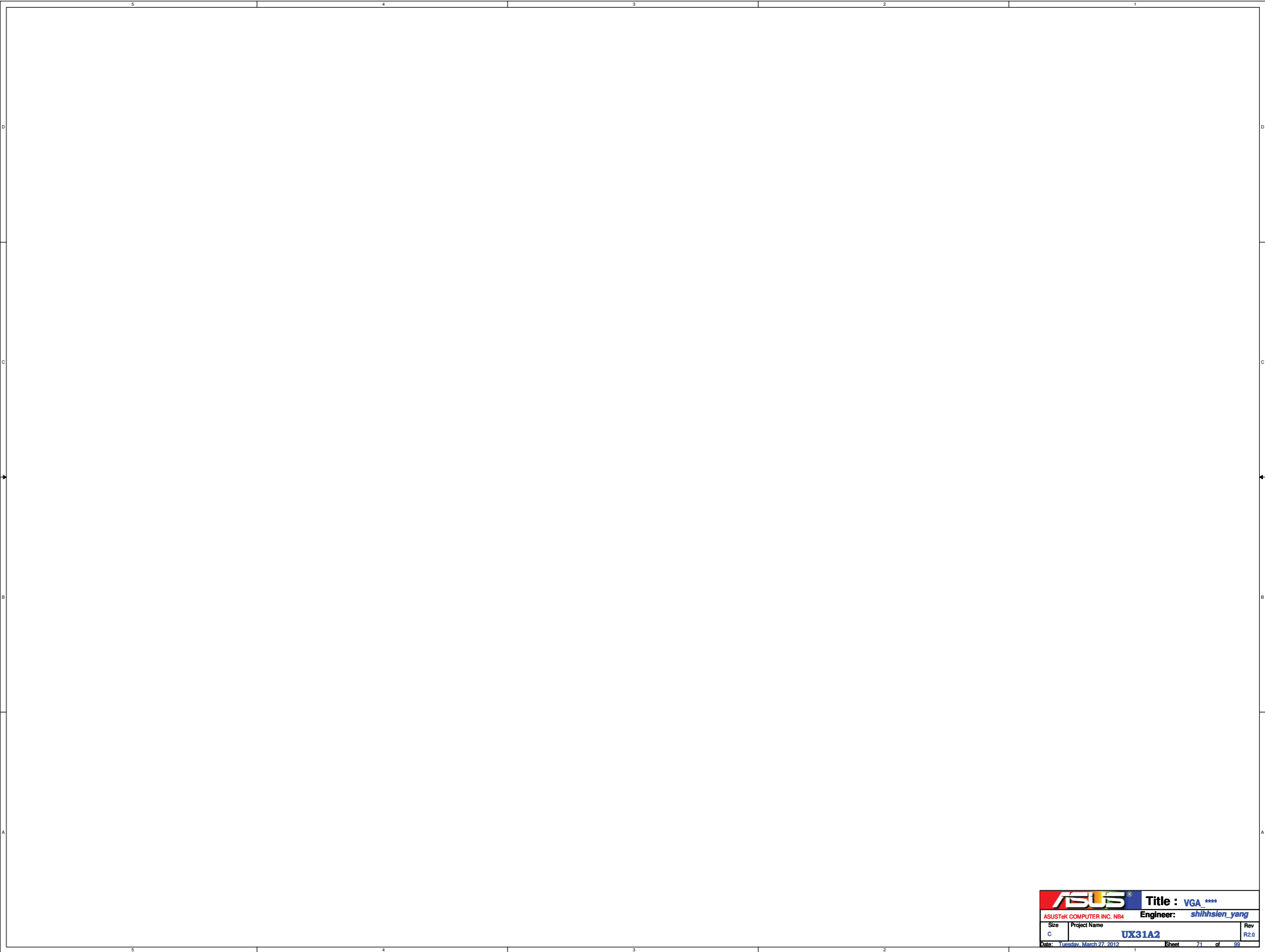
ER-019

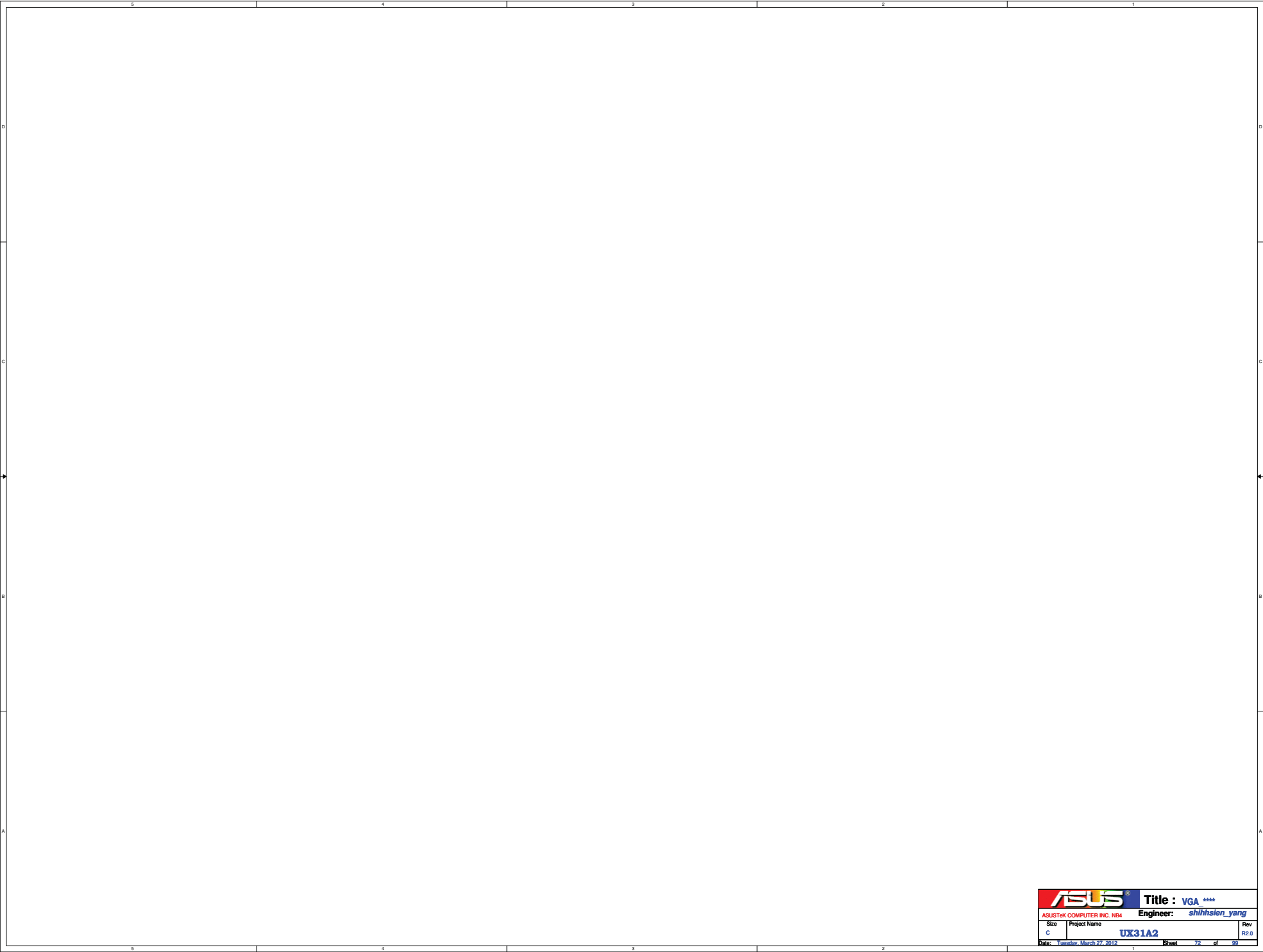


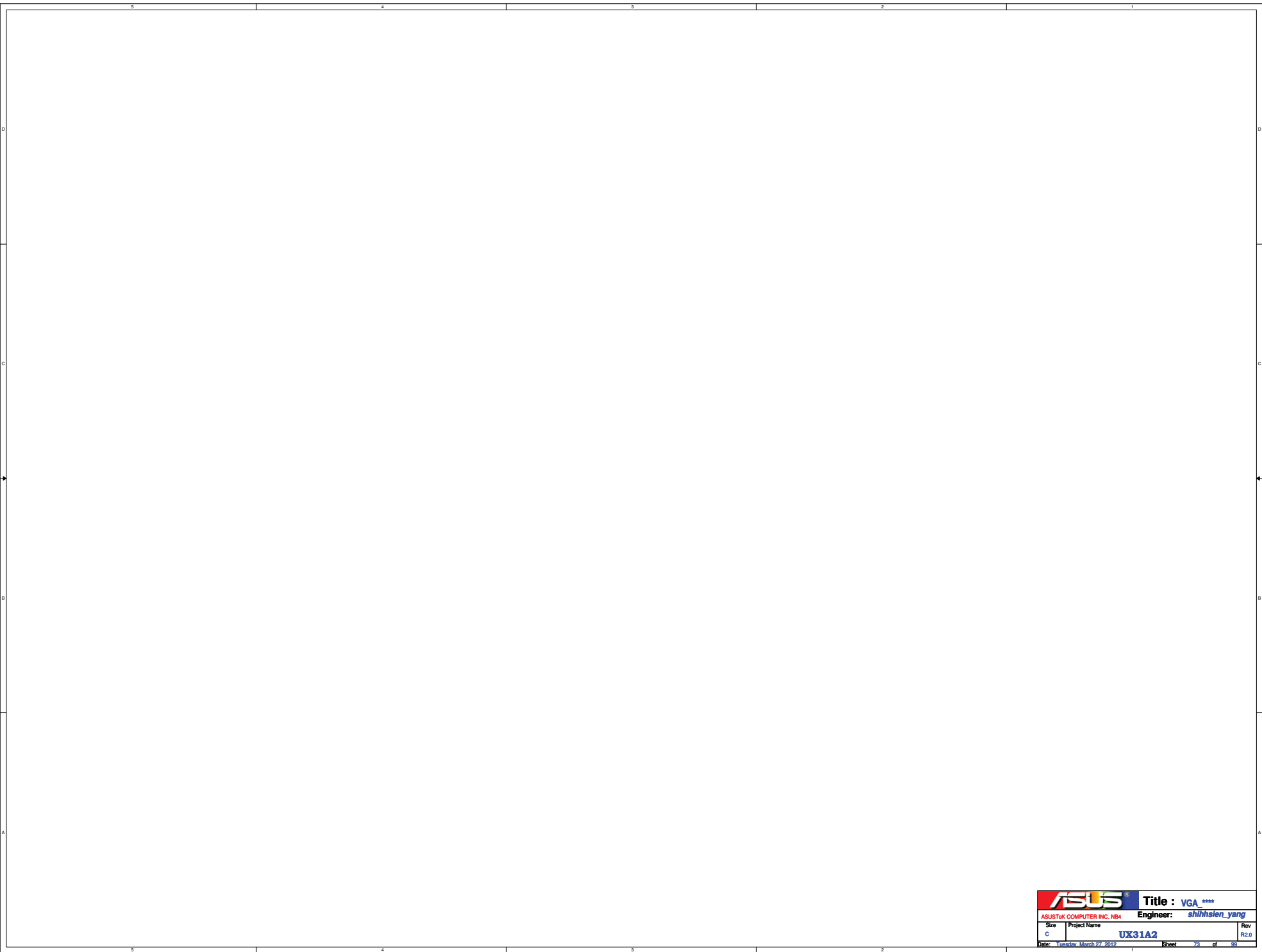
USB_SW VBUS Contorl Circuit



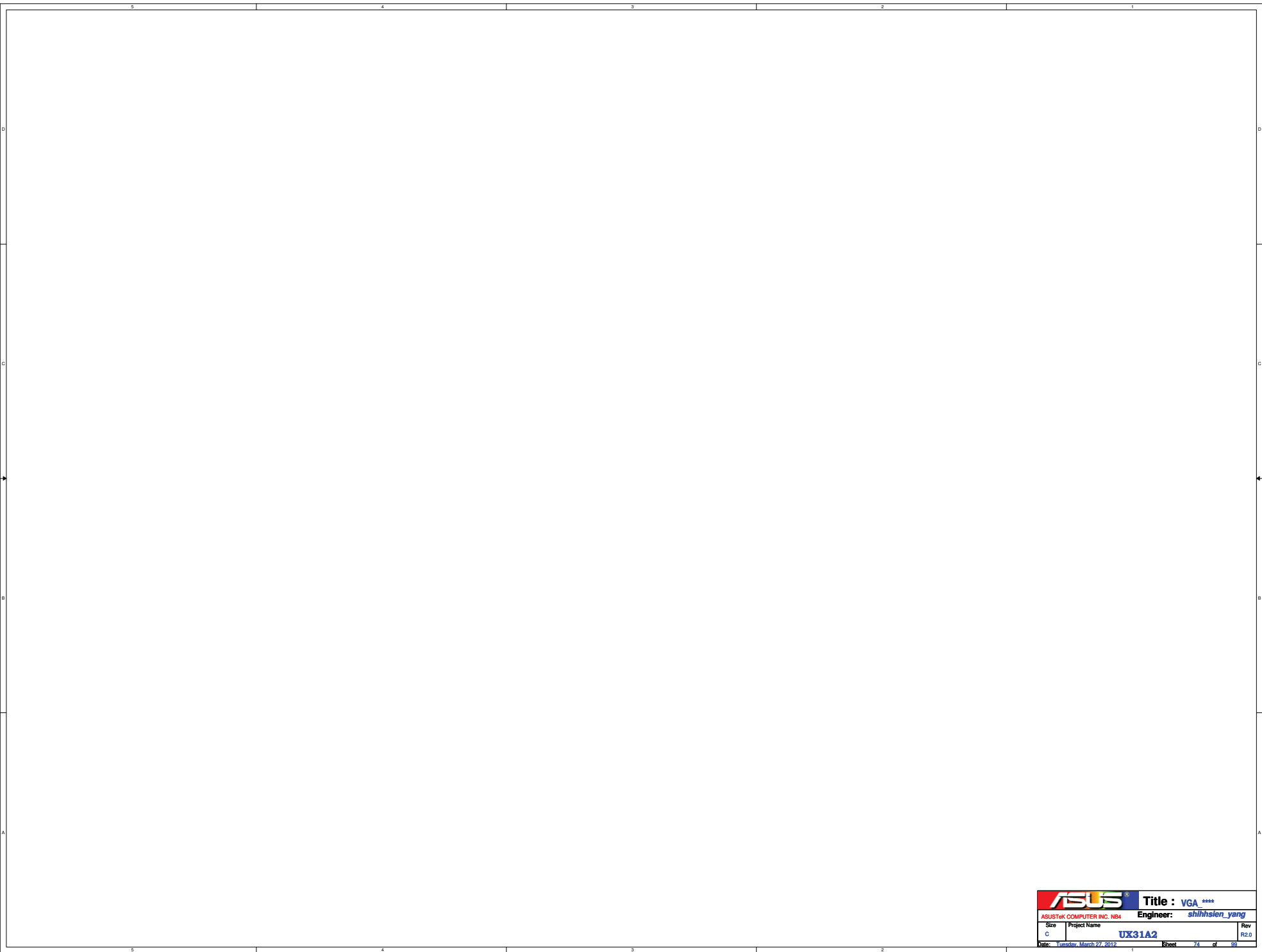
Using TI IC, then the
iphone4S can't charger
in S4&S3 mode.



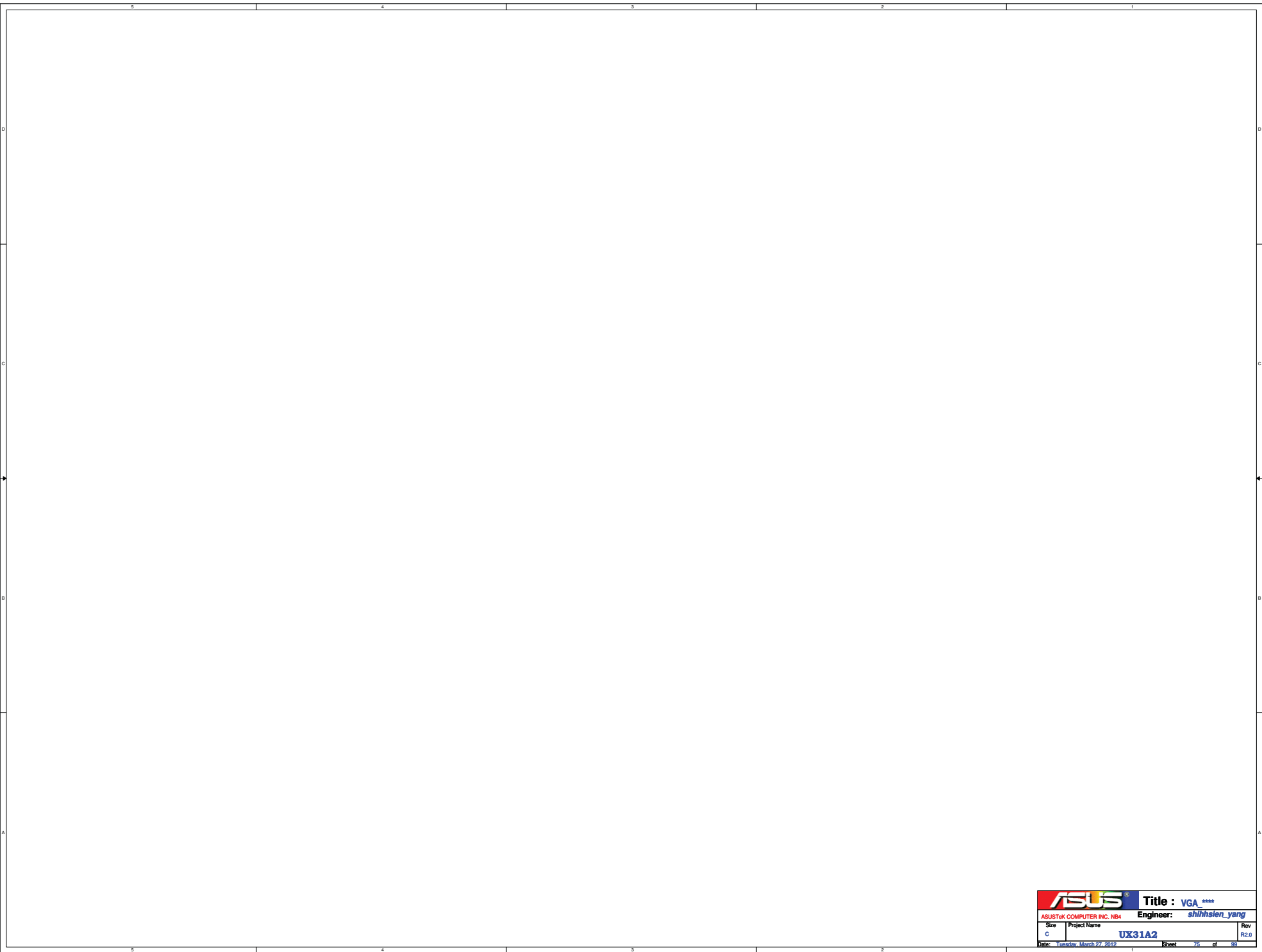




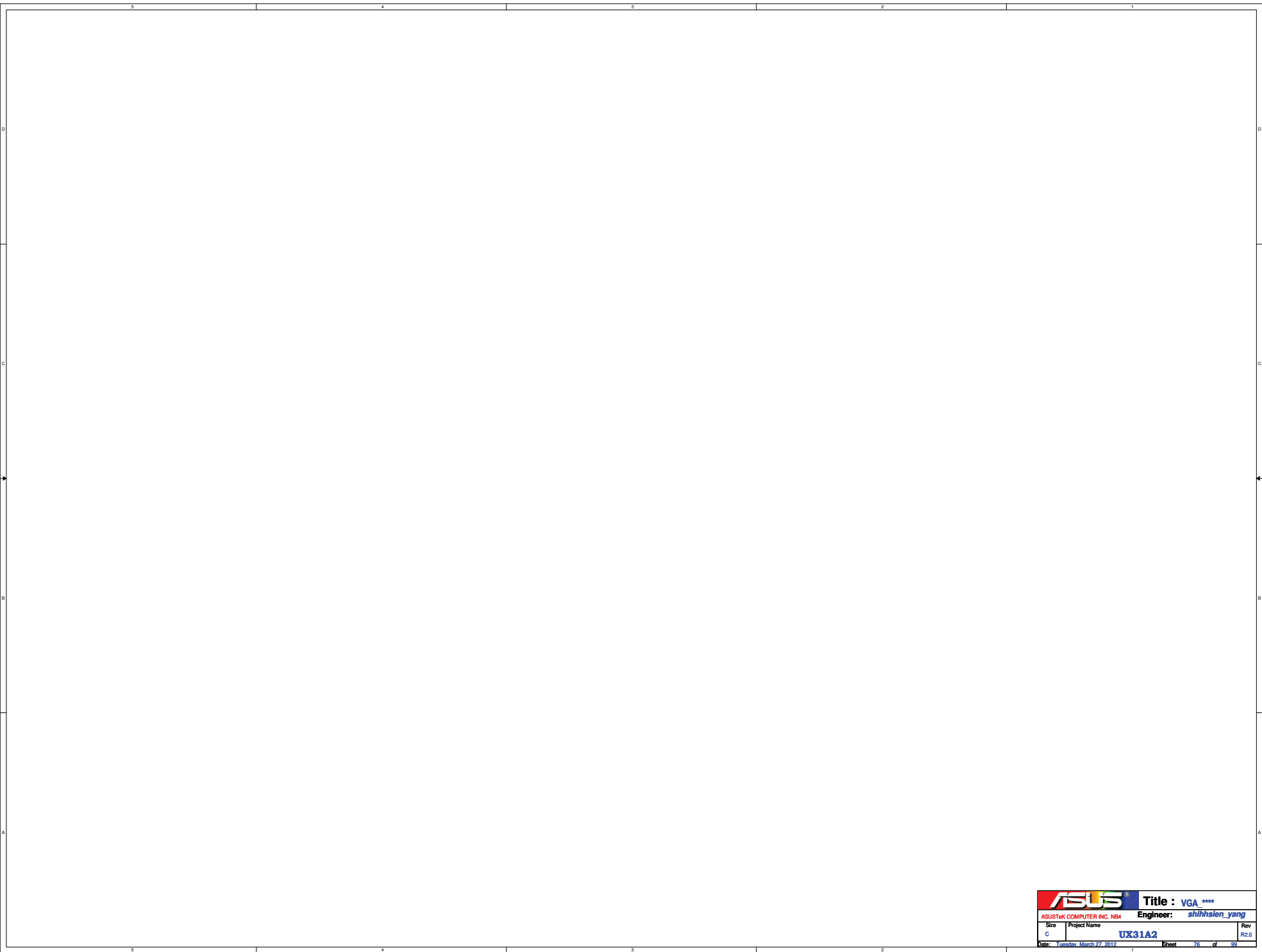
		Title : VGA ****	
ASUSTek COMPUTER INC. NEM		Engineer: shihhsien yang	
Size	Project Name	Rev	
C	UX31A2	R2.0	
Date: Tuesday, March 27, 2012		Sheet	75 of 90



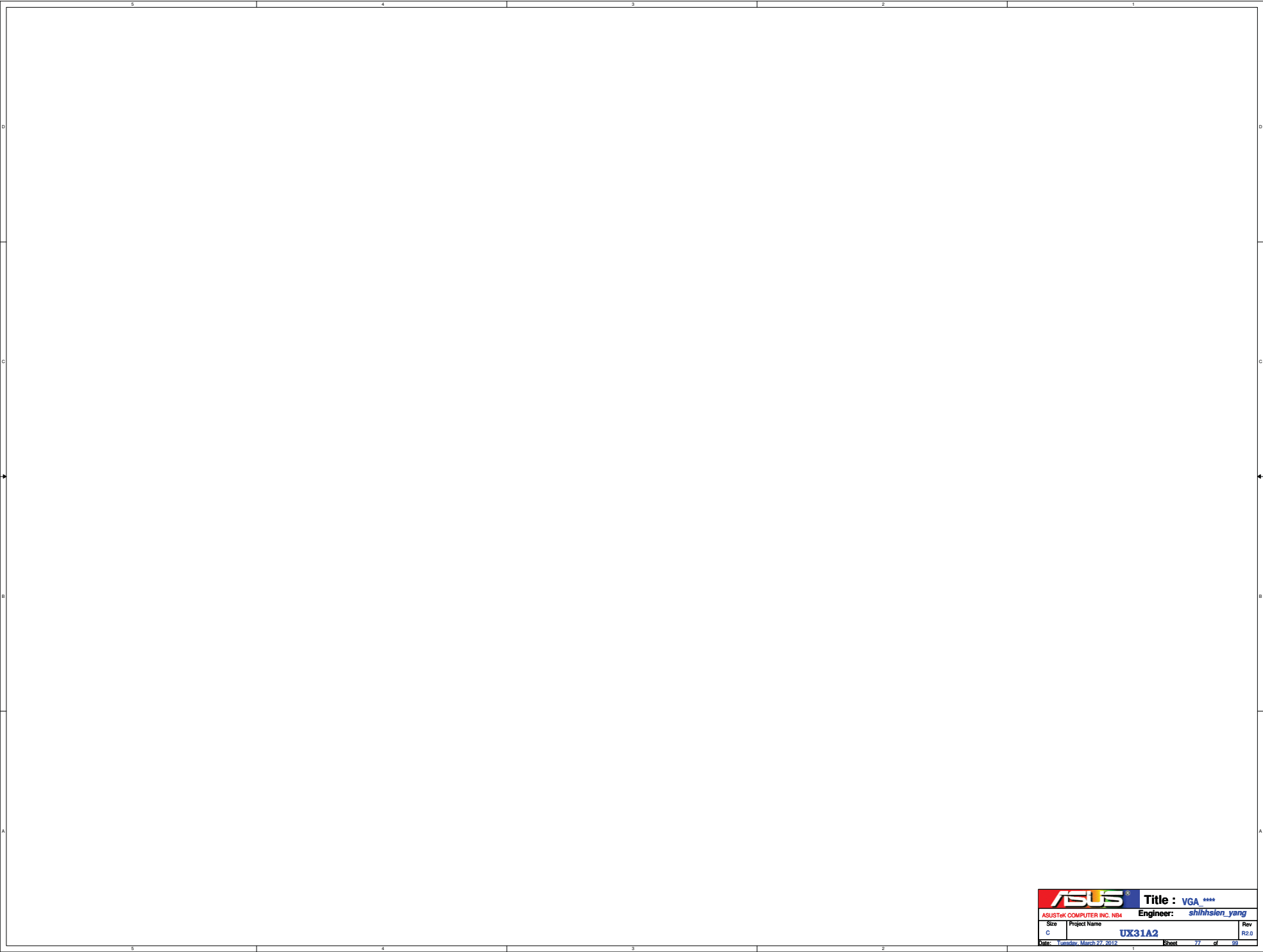
		Title : VGA ****	
ASUSTek COMPUTER INC. NEM		Engineer: shihhsien_yang	
Size C	Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012		Sheet 74 of 99	



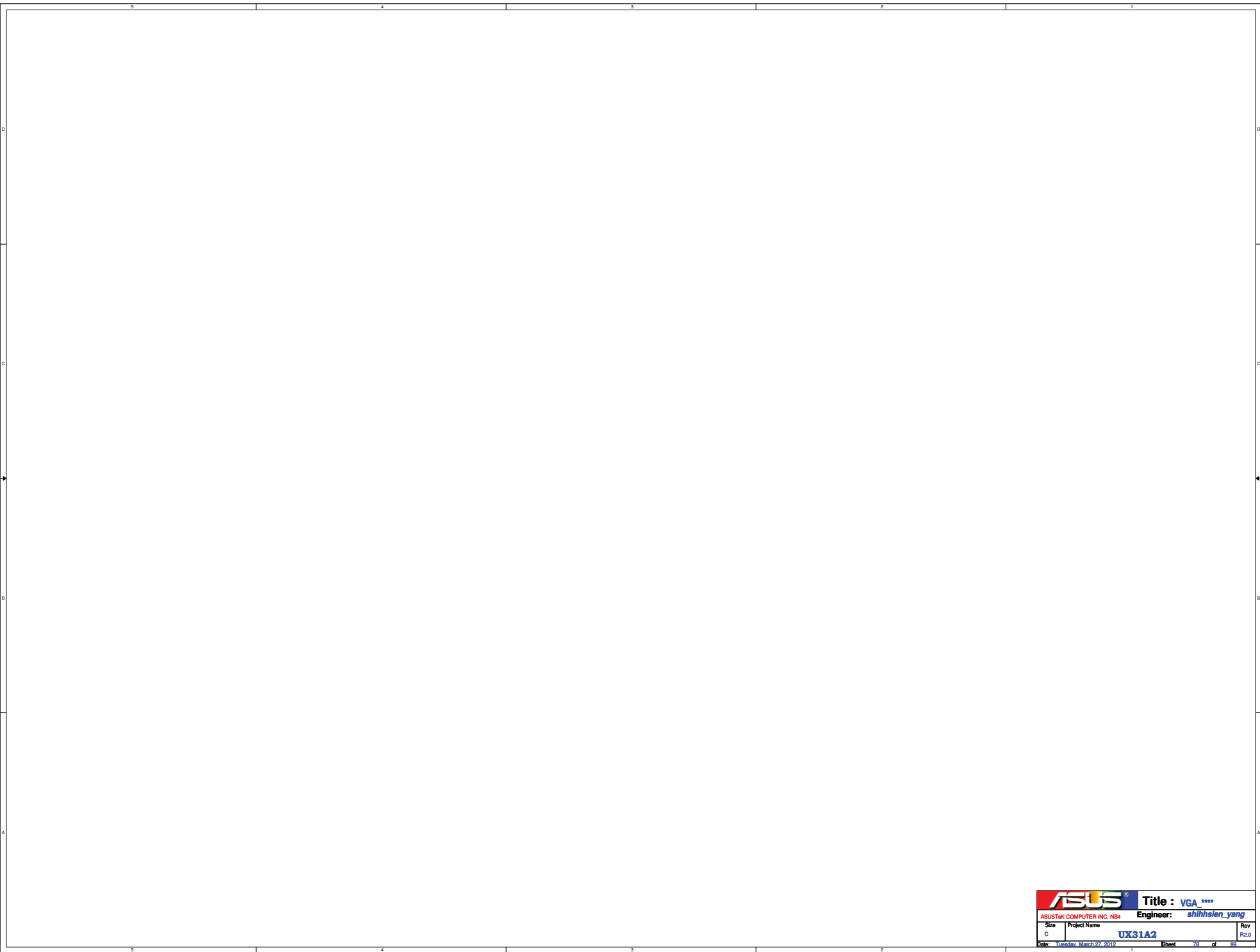
		Title : VGA ****	
ASUSTek COMPUTER INC. NEM		Engineer: shihhsien_yang	
Size C	Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012		Sheet 75 of 90	



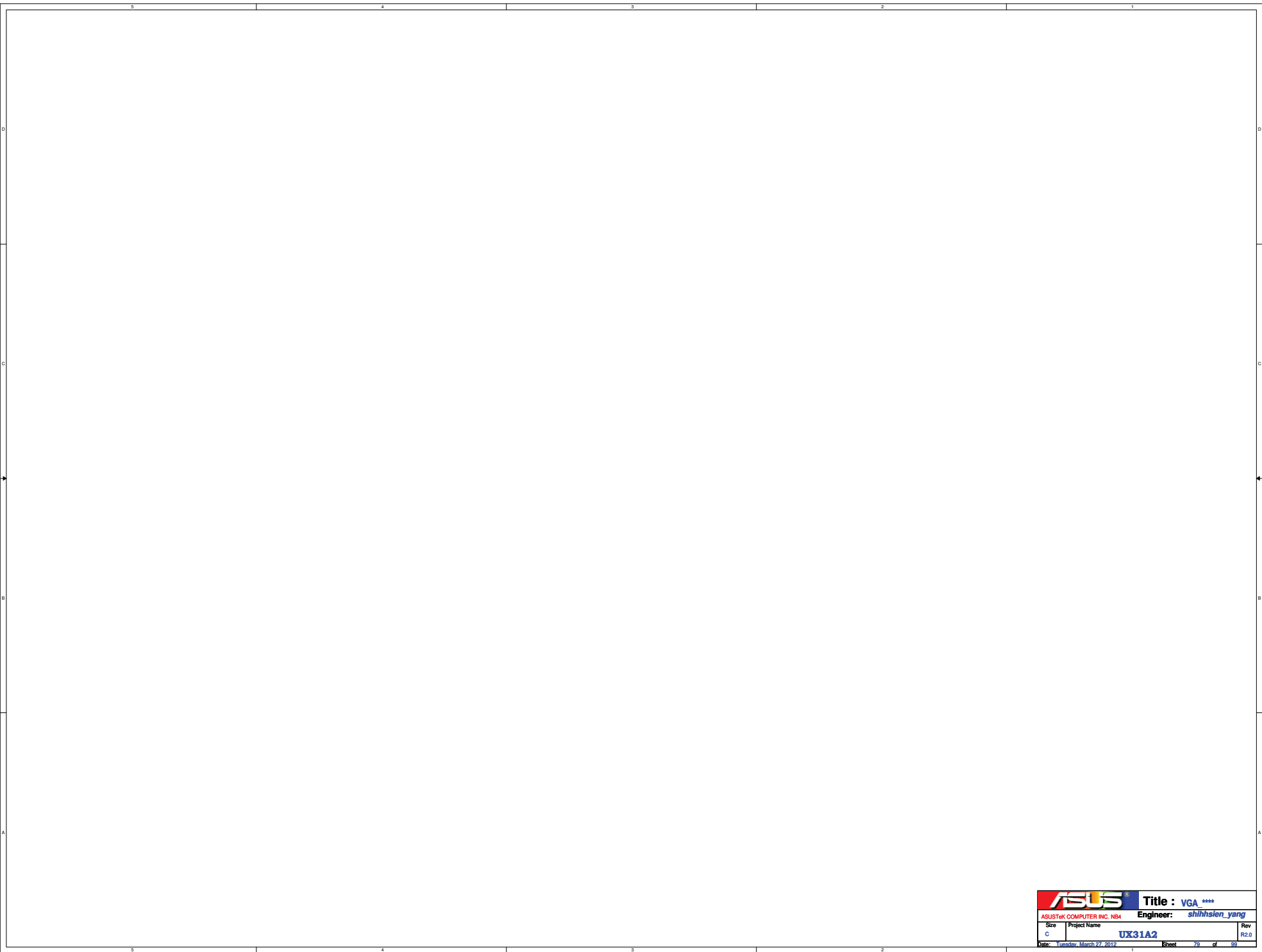
		Title : VGA ****	
ASUSTek COMPUTER INC. NEM		Engineer: shihhsien_yang	
Size C	Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012		Sheet 76 of 90	



		Title : VGA ****	
ASUSTek COMPUTER INC. NEM		Engineer: shihhsien yang	
Size C	Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012		Sheet 77 of 80	

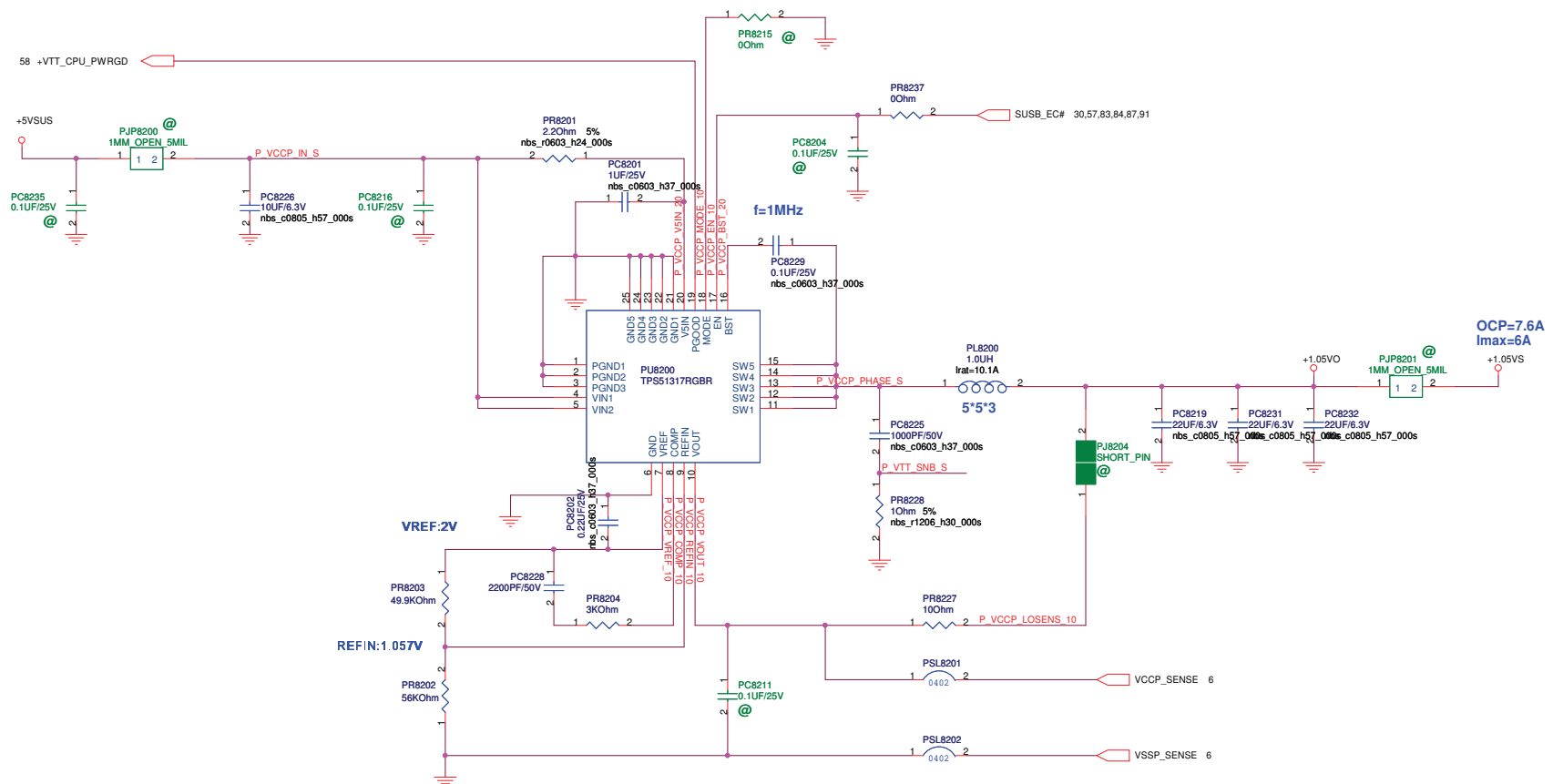


		Title : VGA ****	
ASUSTek COMPUTER INC. NEM		Engineer: shihhsien_yang	
Size C	Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012		Sheet 78 of 90	



		Title : VGA ****	
ASUSTek COMPUTER INC. NEM		Engineer: shihhsien_yang	
Size C	Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012		Sheet 79 of 99	

+VTT CPU & +VTT PCH & +1.05VS POWER SUPPLY



<Variant Name>



Title : *+1.05VS*

ASUSTeK COMPUTER INC. NB

Engineer: *shihhsien_yang*

Size

Project Name	
--------------	--

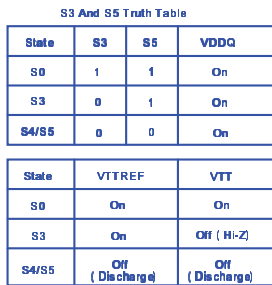
UX31A2

Rev

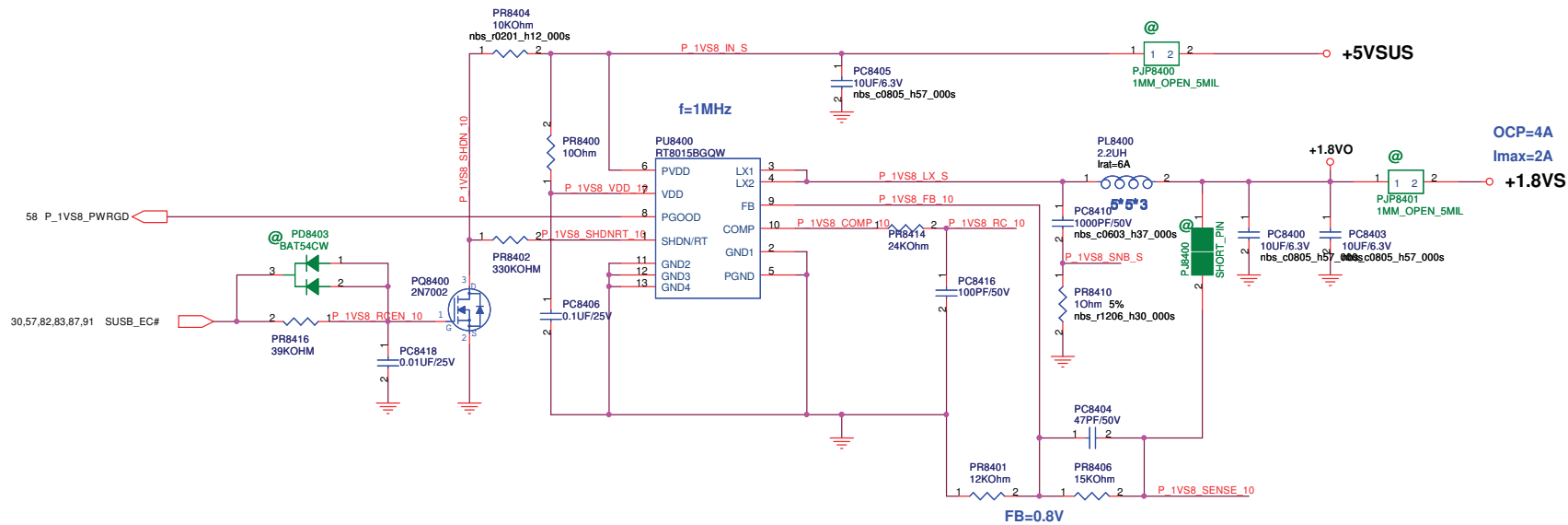
R2.0

Date: Tuesday, March 27, 2012

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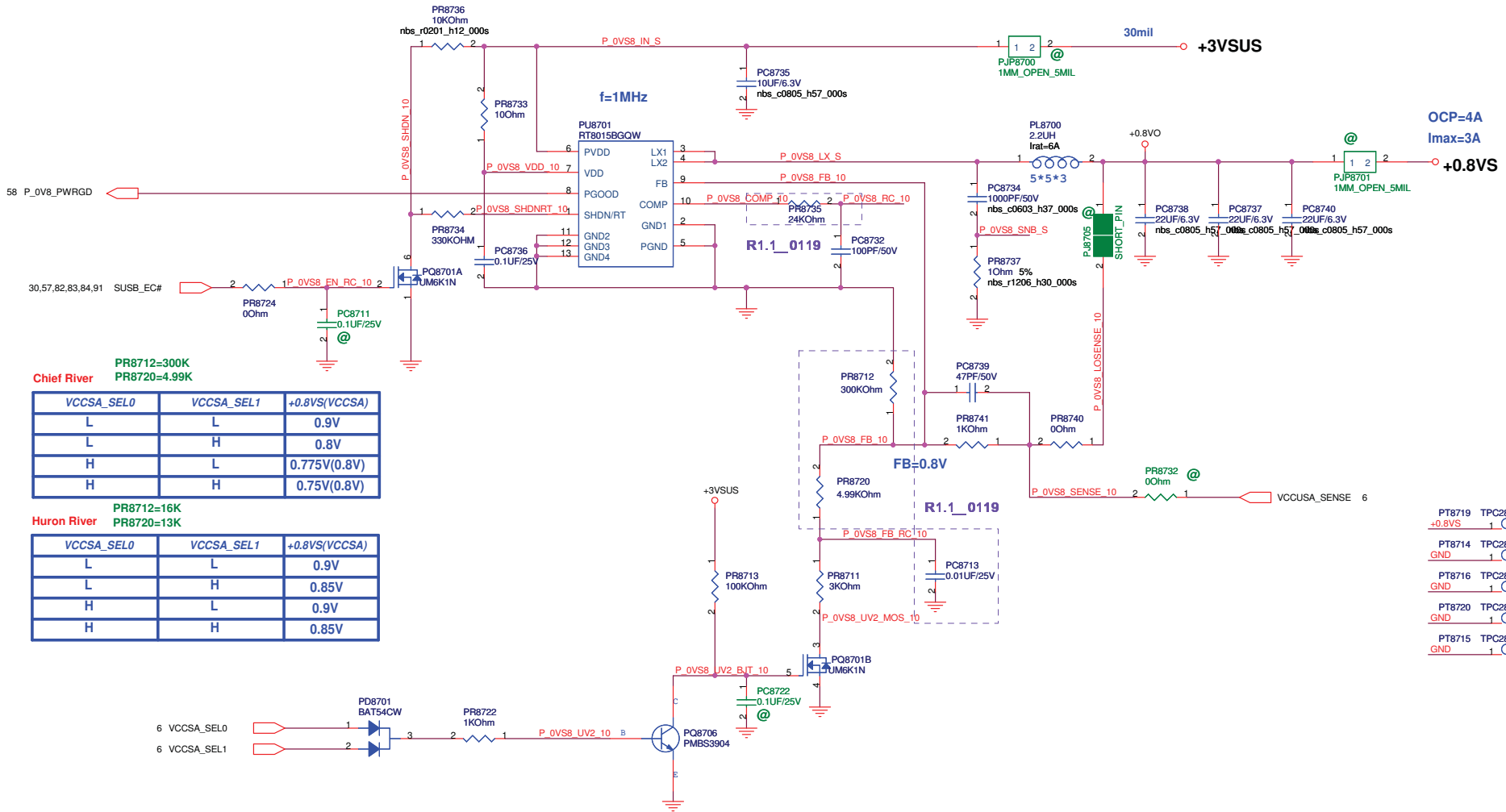
+1.8VS POWER SUPPLY

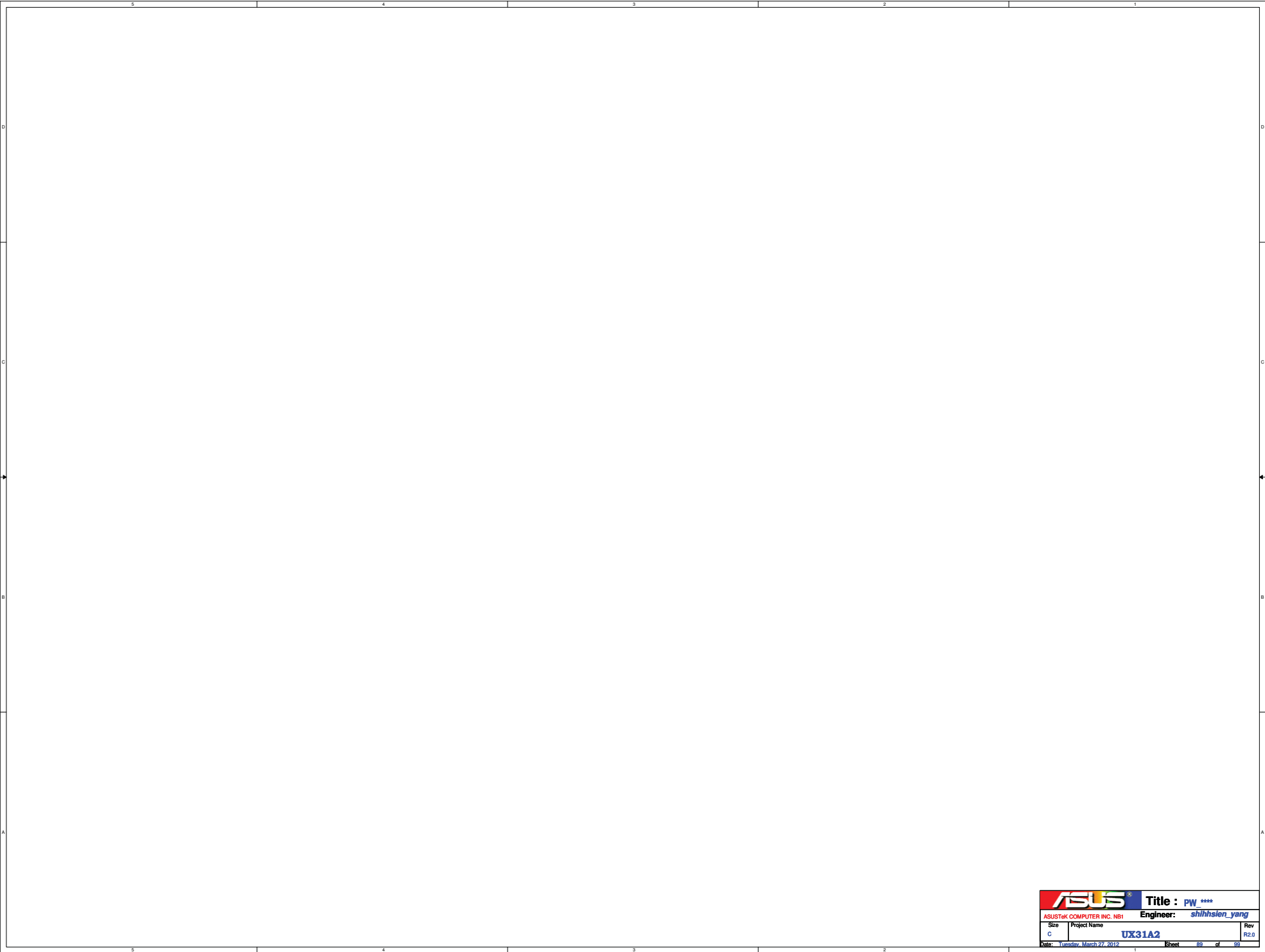


PT8401 TPC28T
+1.8VS 1
PT8402 TPC28T
GND 1
PT8403 TPC28T
GND 1

ASUS		Title : +1.8VS	
ASUSTeK COMPUTER INC.		Engineer: shihhsien yang	
Size Custom	Project Name UX31A2	Rev R2.0	
Date: Tuesday, March 27, 2012		Sheet 84 of 99	

+0.8VS POWER SUPPLY



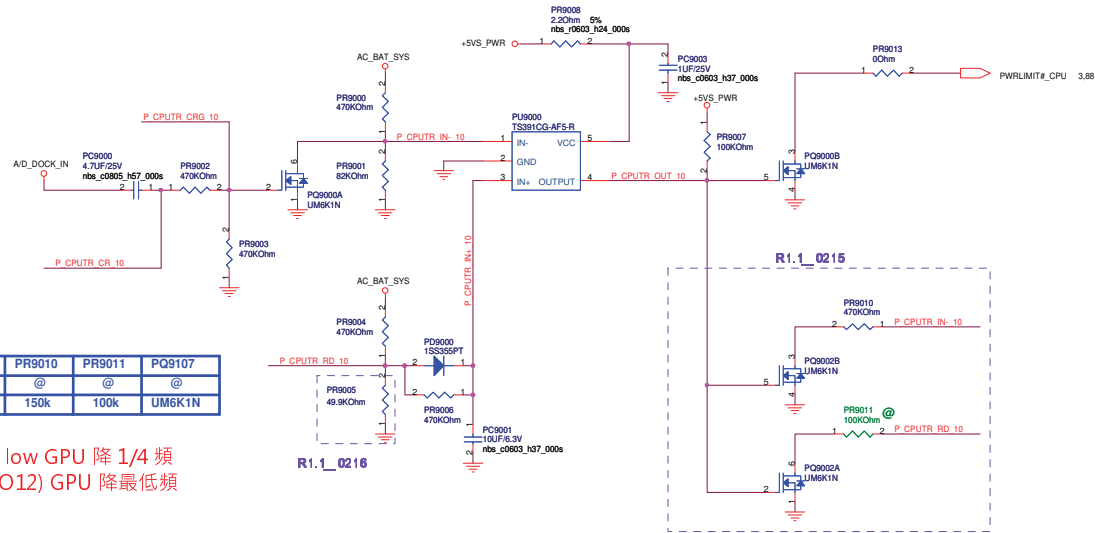


		Title : PW_****	
ASUSTek COMPUTER INC. NBI		Engineer: shihhsien_yang	
Size C	Project Name UX31A2		Rev R2.0
Date: Tuesday, March 27, 2012		Sheet 01 of 01	

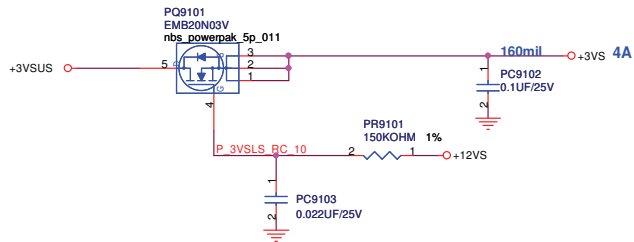
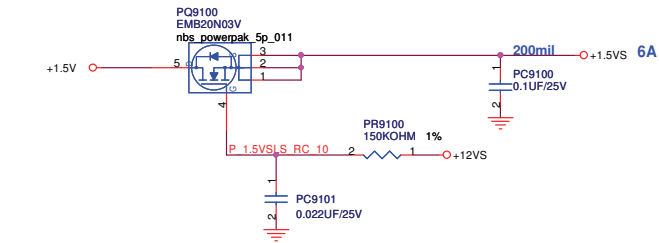
請遠離熱源！

	PR9005	PR9010	PR9011	PQ9107
UX series 2S BAT	62k	@	@	@
Other series 3S/4S BAT	75k	150k	100k	UM6K1N

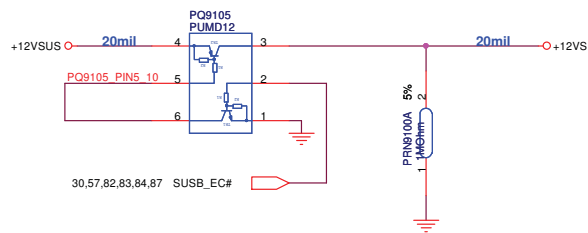
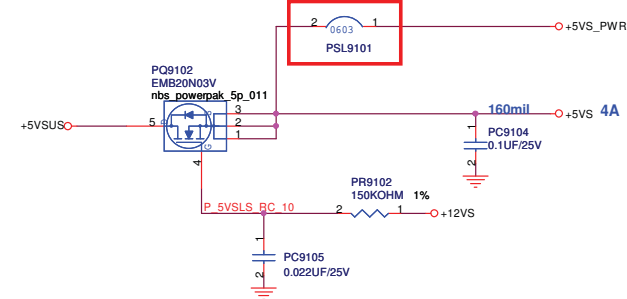
VGA_Alert (GPIO9) pull low GPU 降 1/4 頻
dGPU_PD pull low (GPIO12) GPU 降最低頻



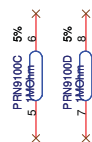
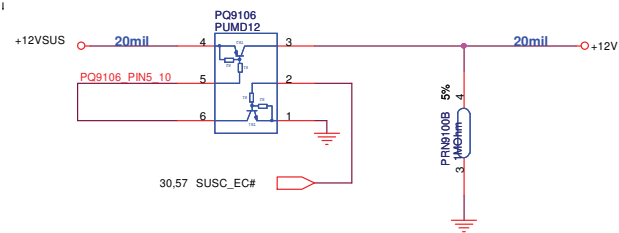
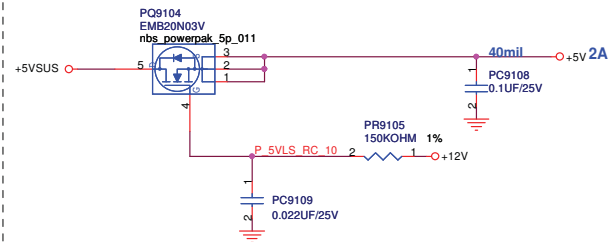
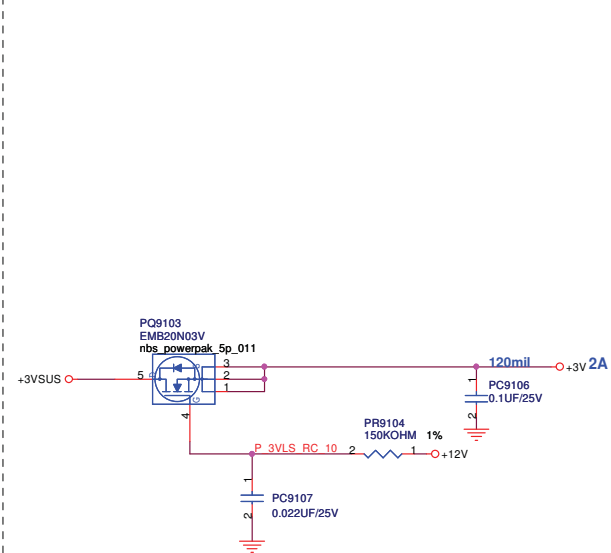
SUSB#_PWR POWER



PSL9101 請擺在 PQ9102 旁邊

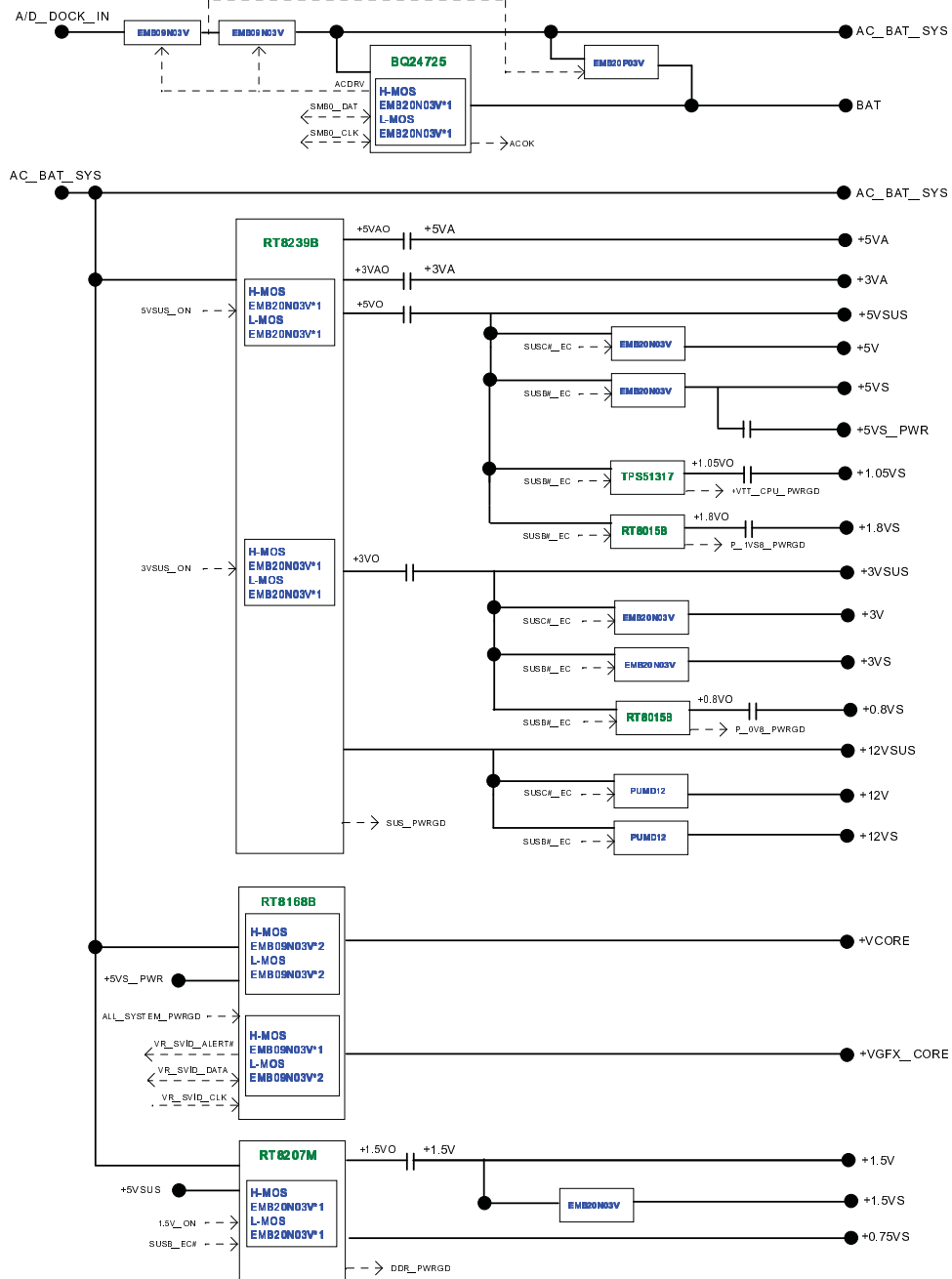


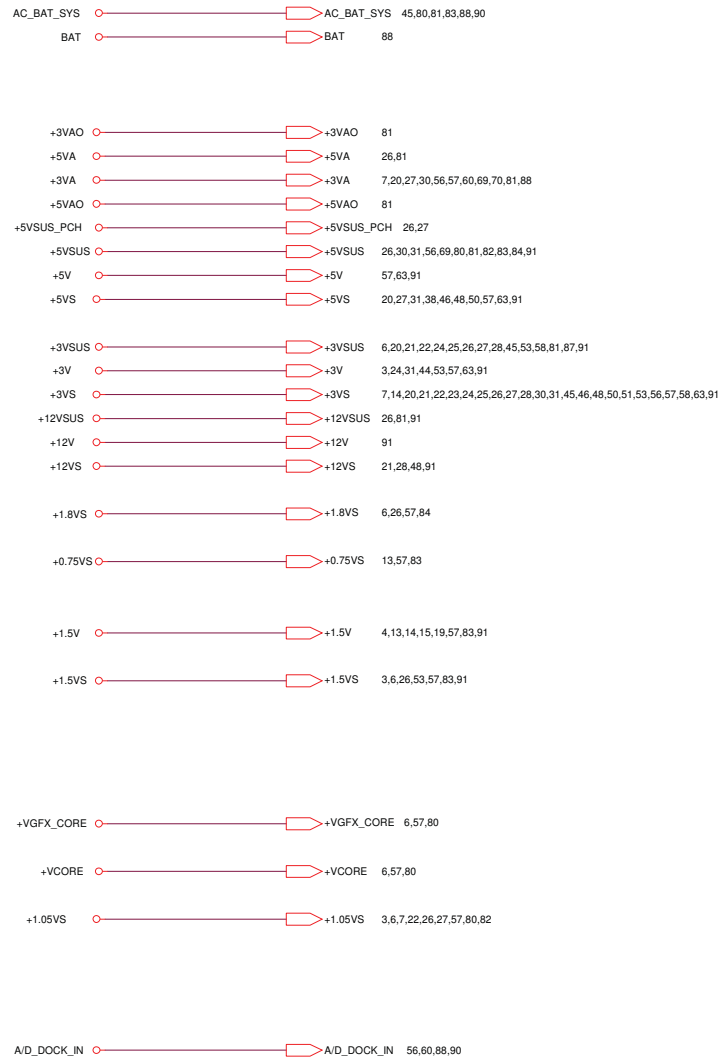
SUSC#_PWR POWER



<Variant Name>

ASUS		Title : Load Switch	
ASUSTeK COMPUTER INC. NB		Engineer: shihhsien yang	
Size	Project Name	Rev	
Custom	UX31A2	R2.0	
Date: Tuesday, March 27, 2012		Sheet 91 of 98	





[U36SD] R1.1

- 1. Change source of PQ9102 and PQ9104 from +5VSUS to +5VSYSP91
- 2. transform pin1,4,7,10 trace to +1.7v_lanp34
- 3. WLAN clk_req1 follow u36jc pull lowp21
- 4. ALC269 pin9 trace to +3vsus for leakage currentp36
- 5. EC PIN3 is NCp30
- 6. Add ESD protect part for HDMI p48
- 7. Add capacitance for EMI request on H_CPUPWRGDP25
- 8. Change C3404 trace from GND_LAN to GNDp34
- 9. Follow U36JC CRT solutionp46

[M61JA] R1.0 => R1.1

1. Follow E.E RC delay
+5v R9107 100K change to 68K
+3v R9106 200K change to 121K
+1.5v R8306 49.9K change to 68K
+5VS R9104 200K change to 68K
+3VS R9103 200K change to 121K
+1.8VS R8401 33.2K change to 121K
+1.5VS R9102 470K change to 390K
+1.05VS R8252 39K change to 200K
+0.75VS R8312 0 change to 2.49K C8310 0.1U change to 2.2U
- 2.VR_VID0~2 pull high 1K VR_VID6 pull low 1K.
- 3.U8401 RT8015A change to RT8015B
- 4.Reserve GVR_VID0~VID6 pull high and low resistor R8627~R8633
- 5.Reserve R8517~R5720 pull high & pull low resistor for MCP_CORE_VID
- 6.page86 component option change to ARD (CFD no stuff)
- 7.R8004 option change to CFD & R8049 change to ARD(For IMON)
- 8.Change RN8801A RN8801B(layout request)
- 9.R8517 R8519 change to stuff
- 10.R8406 13K change to 12K
- 11.CE8005 no stuff , CE8007 stuff
- 12.C8403 C8406 size 0603 change to 0805
- 13.R8213 R8305 ohm change to 2.2 ohm
- 14.R8621~R8633 stuff 1K ohm
- 15.R8512 change form 200K to 33K ohm
- 16.VTT_PCH component option change to CFD
- 17.Delete U8502 & GPU_PWRON signal change to GPU_PWRON_1.8VSG_&_3.3VSG
- 18.L8601 1uH => 0.56uH , C8608 0.01uF/50 => 0.01uF/16V , R8621 43K => 36K , C8617 =>0.1uF/16V 1uF/10V ,
C8607 68pF/50V => 33pF/50V , R8625 10K => 18.7K , R8613 3.6K => 4.02K
- 19.R8057 change form 10K to 2.05K
- 20.Add Q8007 & Q8008 form thermal issue

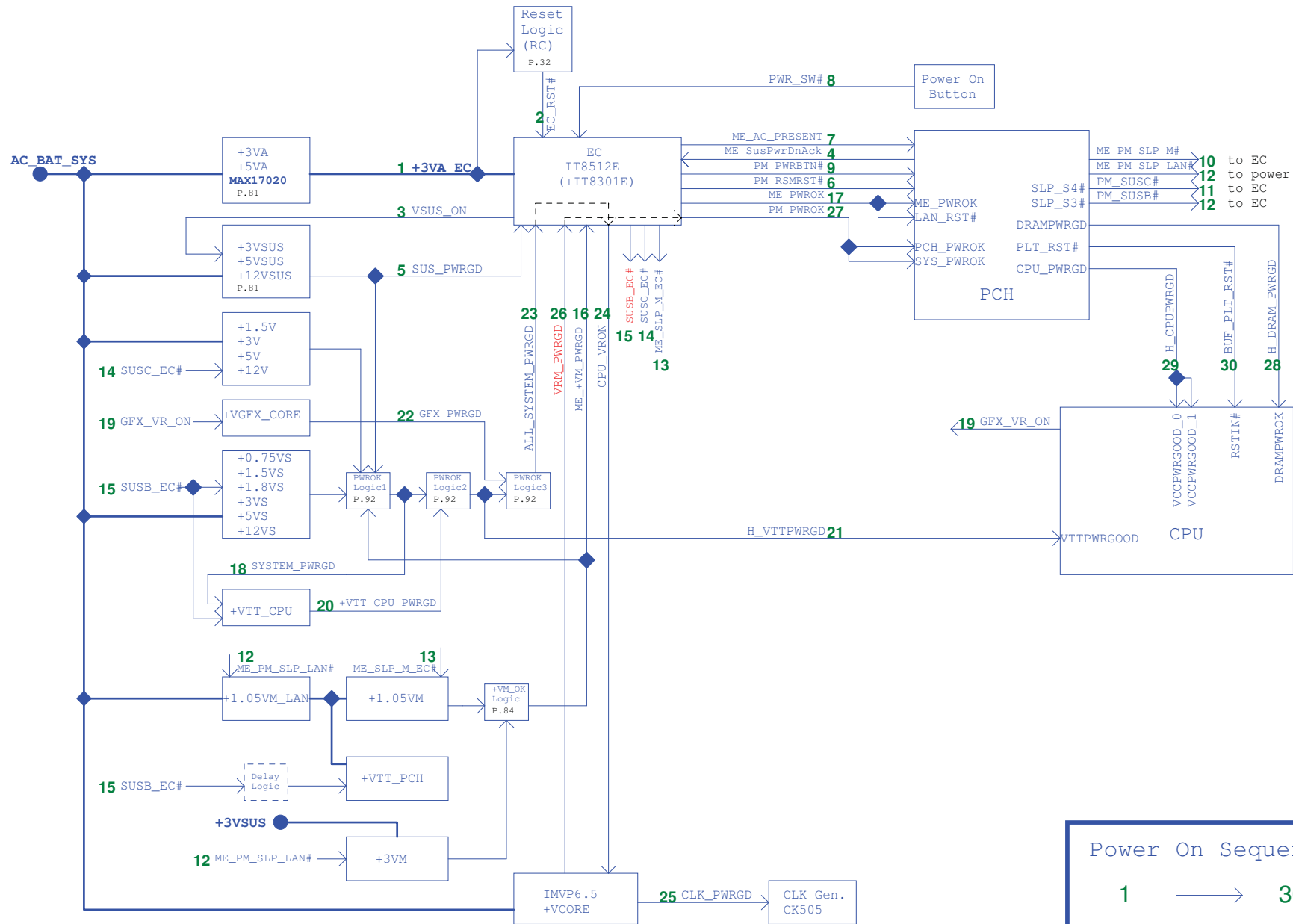
		Title : System History	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size Custom	Project Name UX31A2		Rev
Date: Tuesday, March 27, 2012		Sheet	96 of 99

ER
001 Page 13 & 14 : add +0.75VS de-coupling capacitors for channel B by samsung simulation recommend , and add +1.5V de-coupling capacitors around U1404 by samsung simulation recommend
002 Page 65 : remove U6511~14, U6516
003 Page 31: change J3101 to 12G183000403 and add PWR_SW ~ PWR_LED function on Keyboard
004 Page 46 : change J4601 to 12019-00020000
005 Page 48 : change J4801 to 12022-00013700
006 Page 70 : remove SW7001
007 Page 69 : change J6901 to 12013-00011600
008 Page 53 : change J5303 to 12003-00020700
009 Page 30 : swap EC GP20 and GPH4 for EC request
010 Page 30 : +3VA ON pull low
011 Page 30 : add R3002 for without Light sensor system
012 Page 30 : unmount R3084, mount R3083 for S4/S5 EC power down
013 Page 21,68,69 : remove about FL1009 circuit
014 Page 06 : modify R0617, R0618 to 1K follow intel DG
015 Page 60 : change J6001 to 12014-00101000 for MP
016 Page 28 : change U2801 to 05006-00010300 (64M)
017 Page 56 : add R5640 for PWR_LED current limit
018 Page 24,25 : change (H_SMB_INV#) AV10 to AV1 for following VC circuit.
019 Page 69 : add +5V USB2 discharge for AI-charger function fail on iPhone 4S
020 Page 56 : Change R5604 size from 0201 to 0402.
021 Page 23 : Reserve 8pF cap. of RGB signals for EMI suggestion.
022 Page 45 : Reserved 8pF cap. to +3VS_LCD & +3VSUS for RF suggestion.
Page 45 : Reserved 5pF cap. to G & D sides of Q4501 for RF suggestion.
Page 45 : Reserved 5pF cap. to G & D sides of Q4501 for RF suggestion.
Page 45 : Reserved 0.1pF cap. to AC_BAT_SYS_INV_CON for RF suggestion.
Page 45 : Changed R4503 to L4514 for RF suggestion.
Page 45 : Colay USB_PP2 0 ohm & choke for RF suggestion.
Page 13 : Add cap. to +1.5V for RF suggestion.
Page 14 : Add cap. to +1.5V for RF suggestion.
Page 15 : Add cap. to +1.5V for RF suggestion.
Page 48 : Colay HDMI ohm & choke for RF suggestion.
Page 50 : Reserved cap. to SMB1_CLK_3 for RF suggestion.
Page 51 : Reserved cap. to +3VS for RF suggestion.
Page 53 : Reserved cap. to +3VAUX_WLAN for RF suggestion.
Page 70 : Reserved cap. to pin 4 of Q7003 for RF suggestion.
Page 70 : Reserved cap. to pin 4 of Q7003 for RF suggestion.
Page 63 : Reserved cap. to +3V for RF suggestion.
Page 63 : Reserved cap. to net of for RF suggestion.
023 Page 20 : Reserved R2009 for RTC battery change type.
024 Page 26 : Deleting R2606 for DDR3L power change path.
Page 53 : Deleting R5302 for DDR3L power change path.
025 Page 28 : Add cap. to pin 5-8 of SPT ROM for RF suggestion.
026 Page 24 & 51 : Add SATA_TX1 net to SSD for SSD support RAID
027 Page 56 : Change R5609 and reserve C5624 for DC jack change size.
028 Page 26 : Change resistor value of R2630 to 511K ohm and change size from 0201 to 0402 for reducing power consumption.
Page 70 : Change resistor value of R7004 ~ R7005 to 200K ohm for reducing power consumption.
Page 56 : Change resistor value of R5602 to 200K ohm for reducing power consumption.
029 Page 25 : Change R2529 ~ R2530 ~ R2531 for following sedding schematic design.
030 Page 46 : Change C4602 ~ C4604 ~ C4606 cap. value to 10PF and L4601 ~ L4602 ~ L4603 for EMI suggestion & EA measure pass.
Page 24 : Change R2428 resistor value to 39 ohm for EA measure pass.
Page 69 : Delete RN6916 and add L6901 for EMI suggestion.
031 Page 24 & 45 & 63 : Change USB port2 & port3 to port 8 & port 9 for BIOS suggestion.
032 Page 69 : Add R6905 & C6901 for USB problem.
033 Page 27 : Change power plane of VCCDSW3_3 for supporting hybrid sleep mode.
034 Page 51 : Add JP5101 for measurement.
035 Page 63 : Add 0.1uF cap. to +3VS & +5V for RF suggestion.
036 Page 45 : Reserve 0.1uF cap. to BUF_PL1_RST# & TPANEL_INT#_C for EMI suggestion.
Page 31 : Reserve 0.1uF cap. to TP_DAT & TP_CLK for EMI suggestion.
Page 45 : Add L4518 to +3VS_LCD for EMI suggestion.
037 Page 14 & 15 : Change C1416 & C1501 cap. value from 8PF to 0.1uF for RF suggestion.

PWR modify
Page 88 : Updating CHG IC to BQ24725A
Page 88 : Add shut down sche.
Page 90 : Add HW_throttle sche.
Page 90 : Add PR8107 for WLAN noise.
Page 83 : Delete PCE8301 for WLAN noise.
Page 83 : Change PL8300 to 2.2uH for WLAN noise.
Page 83 : Add PC8326 ~ PC8327 for RF suggestion.
Page 83 : Add PR8321 to 330k
Page 83 : Change PR8314 to 9.53k
Page 60 & 90 : Change BOM
Page 81 & 90 : Change BOM & sche. for power design ip sche change.
Page 81 & 90 : Change BOM PCE8101 to 220uF, and FR9005 to 49.9k ohm

PR
001 Page 03 : Change U0303 to 06G004753010 for CR sche.
002 Page 44 : Change JDBUG1 to 12G18340120R
003 Page 56 : Add a new lid sw for touchpanel using. (Panel PCB length change)
004 Page 30 : Reserved 0.1uF to light_sensor.
005 Page 31 : Change 6 pin to 8 pin for TP changing.
006 Page 21 : Change SMBus and INT for TP using.
007 Page 45 : Change Touch Panel pin define.
008 Page 56 : Change control method of charger led.
009 Page 31 : Add C3114 for RF suggestion.
010 Page 31 : Add and reserve the old 6 pins con and delete +5VS_TP.
011 Page 63 : Add 8PF cap. to +5VS for RF suggestion.
012 Page 53 : Add R5306 and Pull high to +3VSUS for intel smart card function using.
013 Page 44 : Change pin define for footprint vs datasheet aren't the same.
014 Page 45 : Add C4570 ~ C4501 ~ C4504 Cap. for RF suggestion.

PWR modify
Page 81 : Add PC8131, PC8132
Page 83 : Add PC8317 / P8316 / PR8305 / PC8305
Page 83 : Change PR8314=>12k
Page 88 : Update Adaptor voltage table
Page 84 : Change PL8400 BOM
Page 87 : Change PL8700 BOM
Page 83 : PR8304 & PR8305 pull high to +3VA_EC
Page 88 : PR8810 & PR8817 change 10ohm/0603 to 0ohm/0603.
Page 88 : PR8838 change 95.3kohm/0402 to 100kohm/0402.

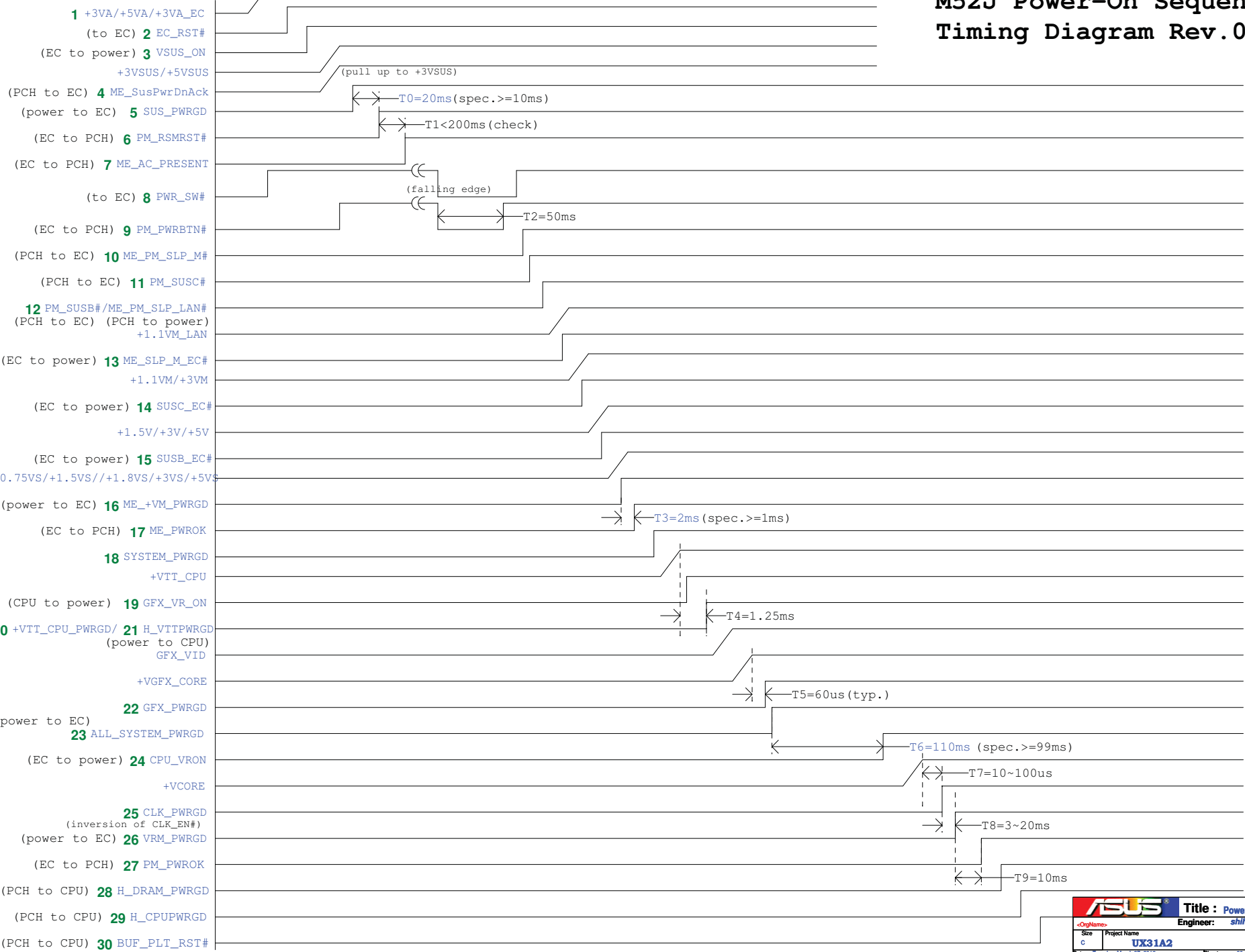


Power On Sequence

1 → 30

AC-IN Mode

M52J Power-On Sequence
Timing Diagram Rev.0.31



UX31A R2.0 SKU table

BCM	CPU	Memory	TPM	SSD	PANEL
Option	/CPU	/MEM	/TPM		
60-NIOMBI60*-B0*	I7-3517U	Elpida 4G DDR3LRS-1600	/TPM	A-DATA/XM11-256GB-V2	CMO/N133HSE-EA1
60-NIOMBI60*-A0*	I7-3517U	Elpida 4G DDR3LRS-1600	N/A		
60-NIOMBI60*-B0*	I5-3317U	Elpida 4G DDR3LRS-1600	/TPM		
60-NIOMBI60*-B0*	I5-3317U	Elpida 4G DDR3LRS-1600	N/A	A-DATA/XM11-128GB-V2	CMO/N133HSE-EA1
60-NIOMBI60*-A0*	I7-3667U	Micron 4G DDR3LRS-1600	/TPM		
60-NIOMBI60*-A0*	I7-3517U	Elpida 4G DDR3-1600	N/A	SANDISK/SDSA5JK-128G	CPT/CLAA133UA03 CW

1. CPU:
- INT I7-3667U 2G/4M : 01001-00173400 (MP)
- INT I7-3517U 1.9G/4M : 01001-00172300 (MP)
- INT I5-3317U 1.7G/3M : 01001-00172400 (MP)
2. PCH:
- INT PANTHERPOINT HM76 : 02001-00051100 (MP)
3. MEM: Differential memory DIMM & Vendor have the differential DIMM_SEL[2:0] defined on board memory.
- Elpida 4G DDR3LRS 1600 256M*16 : 03006-00051300
- Elpida 4G DDR3 1600 256M*16 : 03006-00050800
- Micron 4G DDR3LRS 1600 256M*16 : 03006-00051100

DDR3L_1600	Micron			ELPIDA
DIMM_SEL0	L			R
DIMM_SEL1	L			R
DIMM_SEL2	R			R
DDR3_1600	Hyundai	ELPIDA		
DIMM_SEL0	R	S		
DIMM_SEL1	L	R		
DIMM_SEL2	R	R		