

Compal Confidential

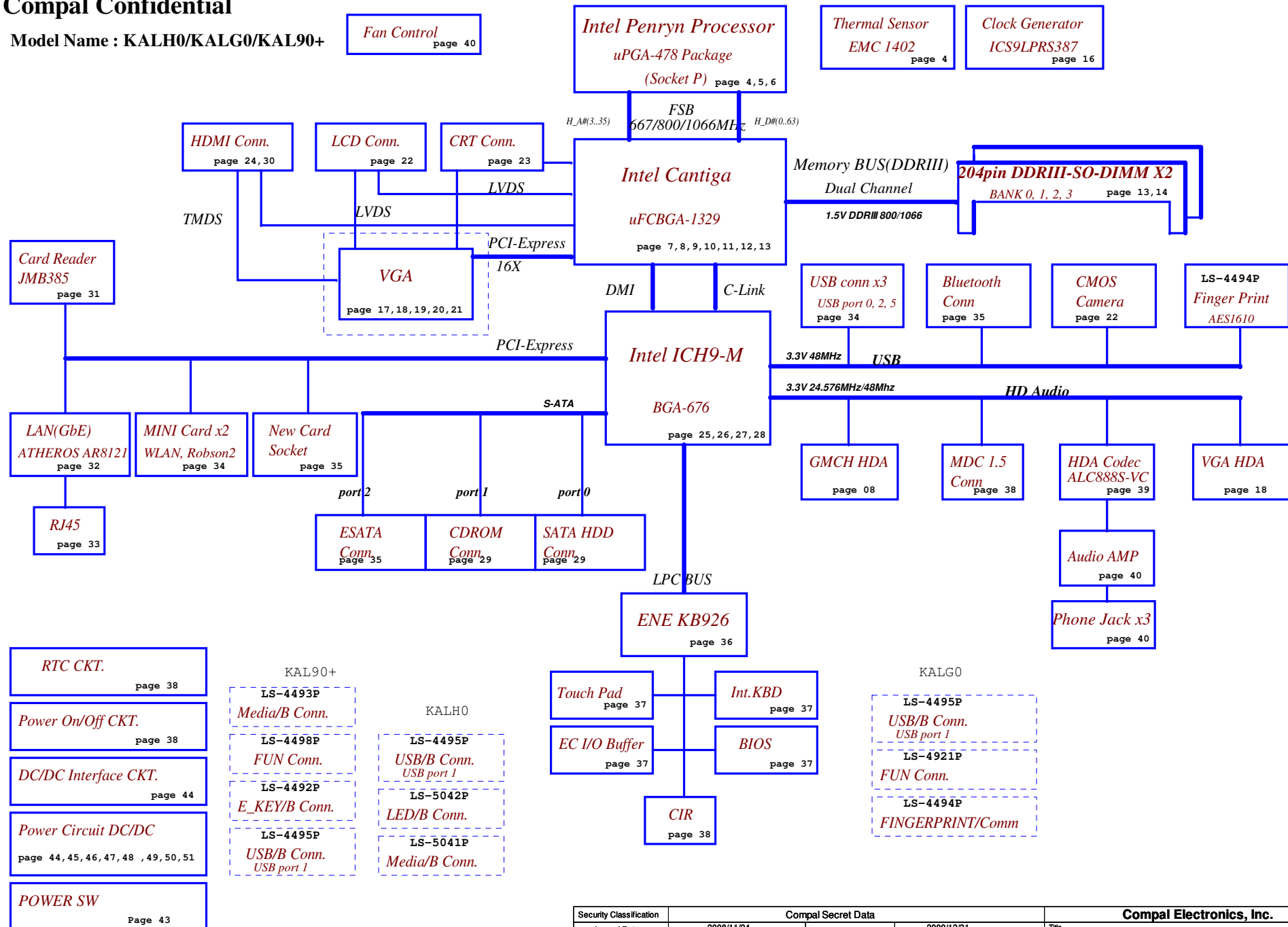
KALH0 /KAL90+ /KALG0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-3-4

REV:1.0

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA/DDR3	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V GM LVDS MODULE	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG6SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Configuration Table

Project	BOM Configuration
KAL90-UMA	XXXXXXXXXX: KAL90@/GM@/888VC@/8121@/GM45@
KAL90-Dis	XXXXXXXXXX: KAL90@/PM@/888VC@/8121@
KALH0-GM45	XXXXXXXXXX: KALH0@/GM@/888VC@/8121@/GM45@
KALH0-GL40	XXXXXXXXXX: KALH0@/GM@/888VC@/8121@/GL40@
KALH0-PM45	XXXXXXXXXX: KALH0@/PM@/888VC@/8121@
KAL90+ -UMA	GM@/888VC@/8121@/GM45@/KAL90+_G0@/KAL90_90+@/KAL90_G0_90+@/KAL90_H0_90+@/KAL90+_PCB@
KAL90+ -Dis	PM@/888VC@/8121@/KAL90+_G0@/KAL90_90+@/KAL90_G0_90+@/KAL90_H0_90+@/KAL90+_PCB@/PM45@
KALG0 -UMA (GL40)	KALG0@/GM@/888VC@/8121@/GL40@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -Dis	KALG0@/PM@/888VC@/8121@/PM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -UMA (GM45)	KALG0@/GM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -DIS (GM45)	KALG0@/PM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@

KALG0 LAN to AR-8131----- 8121@ Change to 8131@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

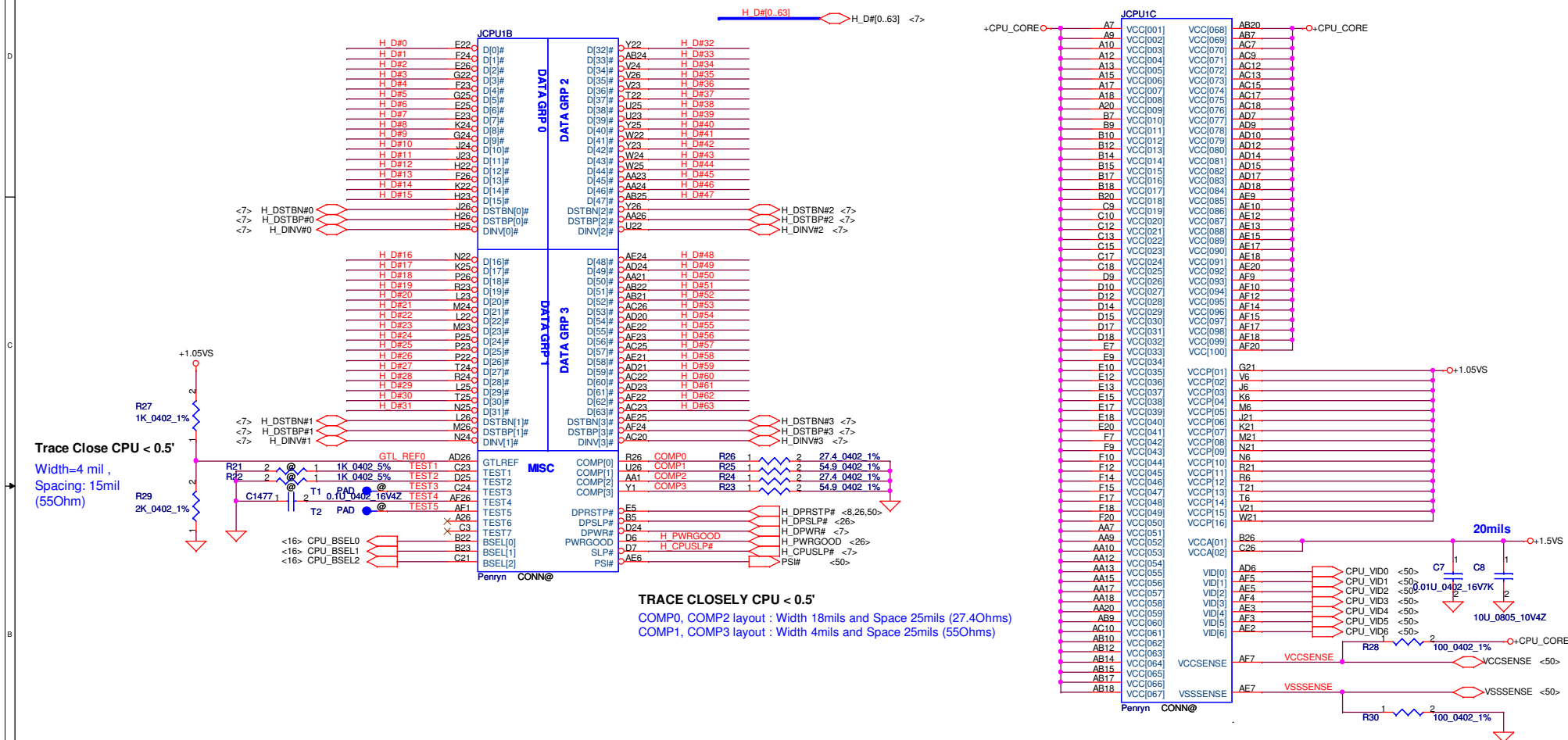
Board ID	PCB Revision
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1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

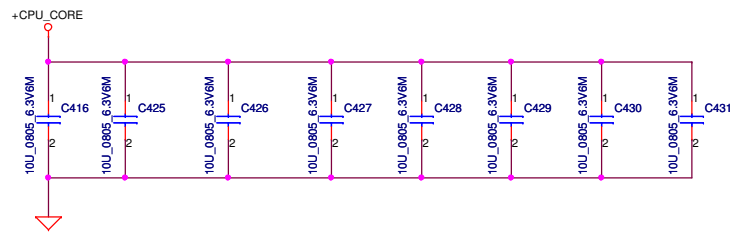
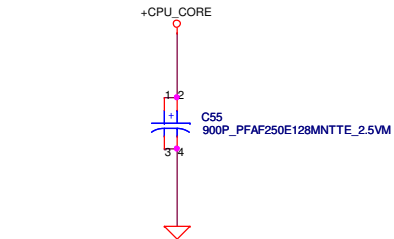
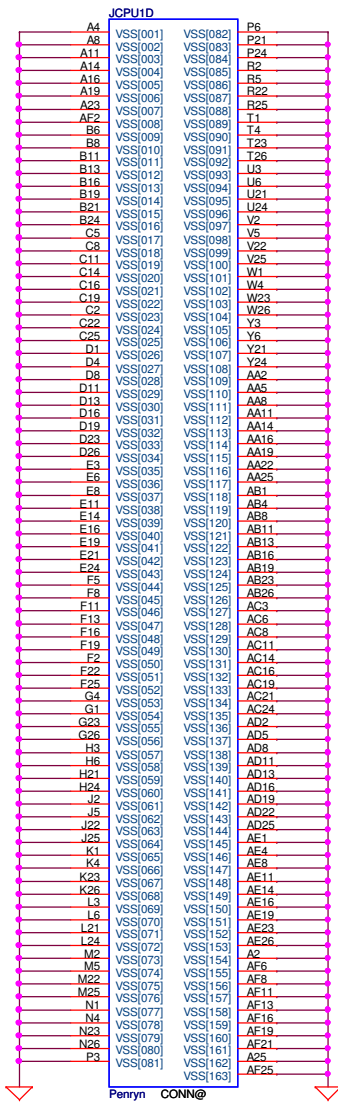
BTO Option Table

BTO Item	BOM Structure
KAL90	KAL90@
UMA	GM@
PM@	PM@
ALC888VC	888VC@
ALC888VB	888VB@
AR8121	8121@
AR8112	8112@
ALC268	268@
GL40	GL40@
GM45	GM45@
KAL90-G0	KAL90_G0@
KAL90-H0	KAL90_H0@
KALG0	KALG0@
KALH0	KALH0@
ALC268	268@
	KAL90_90+@
	KAL90_H0_G0@
	KAL90+_G0
	KALH0_G0
	KAL90_G0_90+@
	KAL90_H0_90+@
	KAL90+_PCB@
	KALG0_PCB@

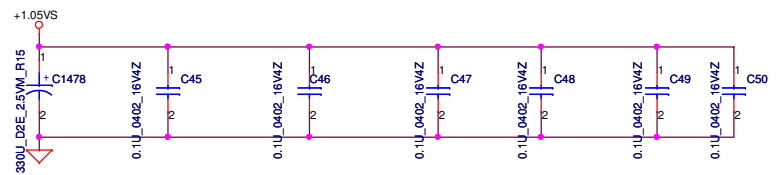
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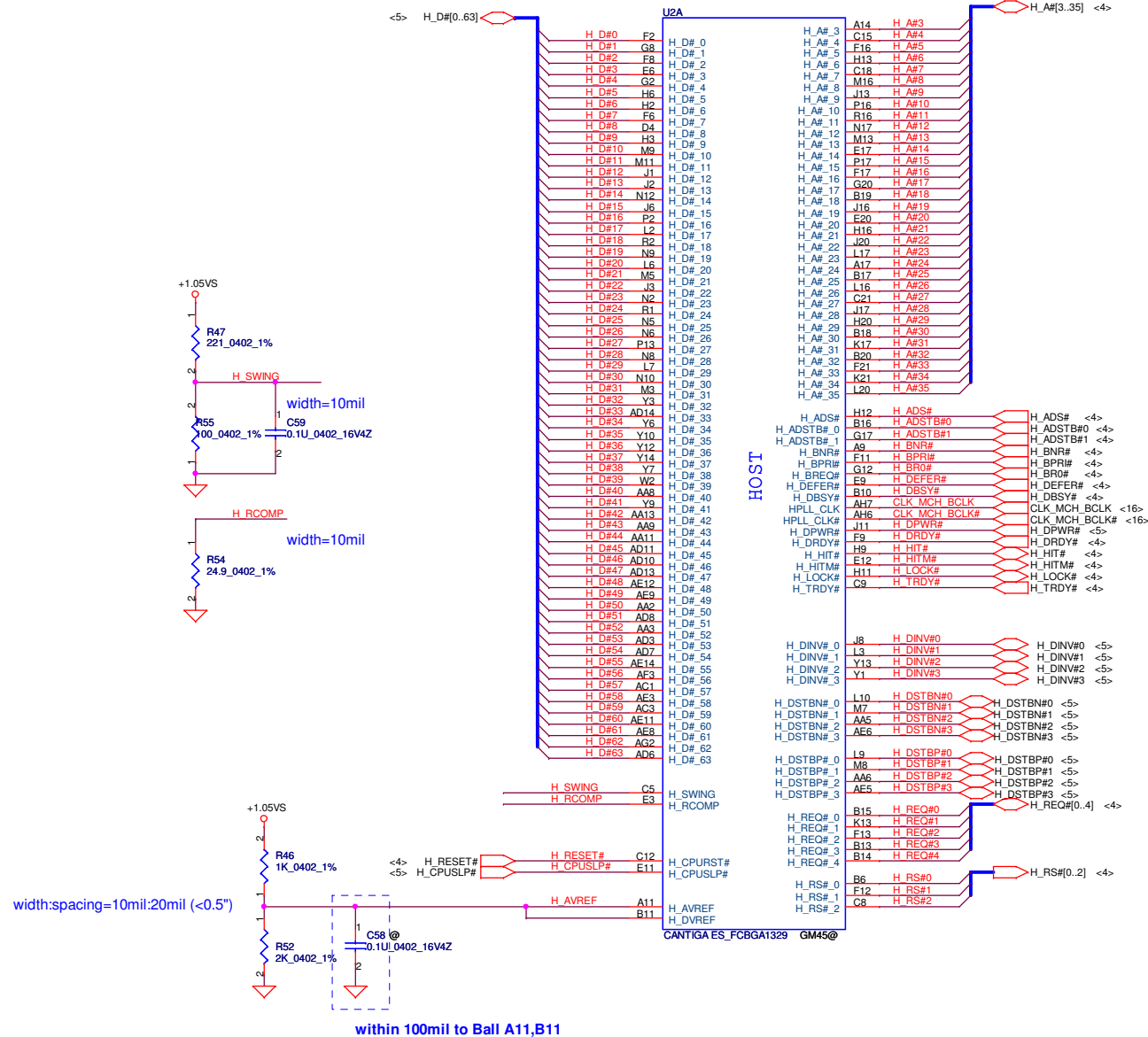
Notes List





+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32





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26-

MCH_CFG_5

MCH_CFG_6

MCH_CFG_7

MCH_CFG_9

MCH_CFG_10

MCH_CFG_12

MCH_CFG_13

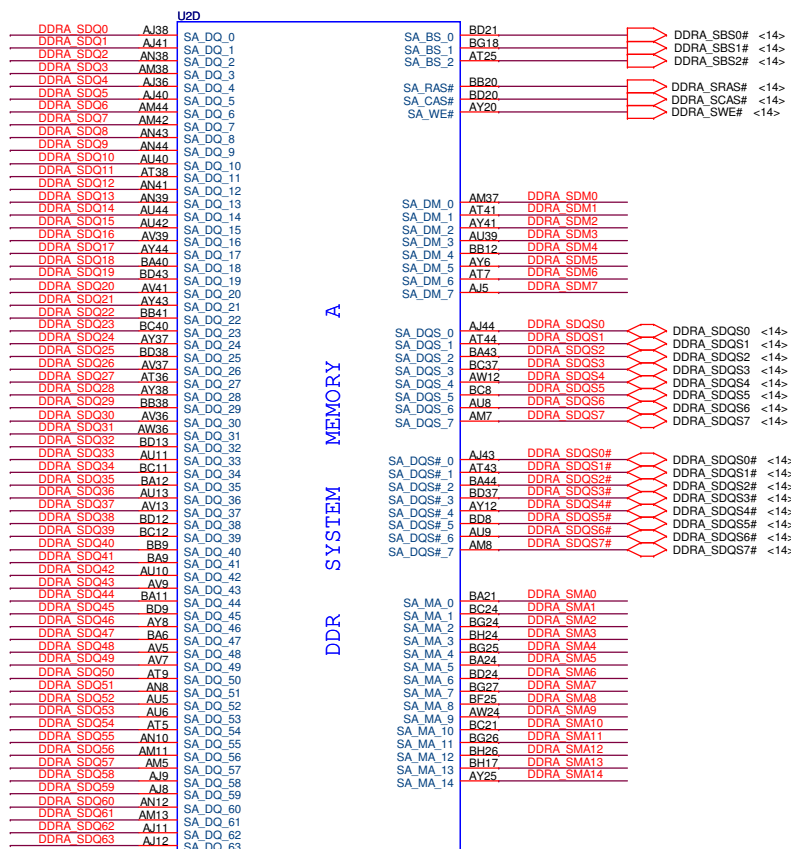
MCH_CFG_16

MCH_CFG_19

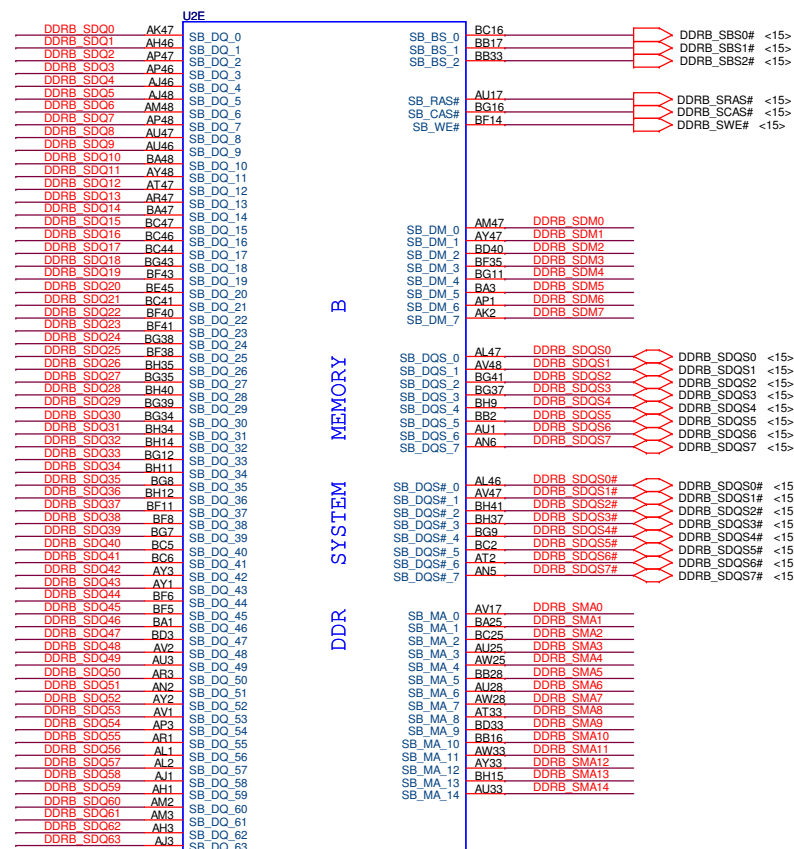
MCH_CFG_20

3V3

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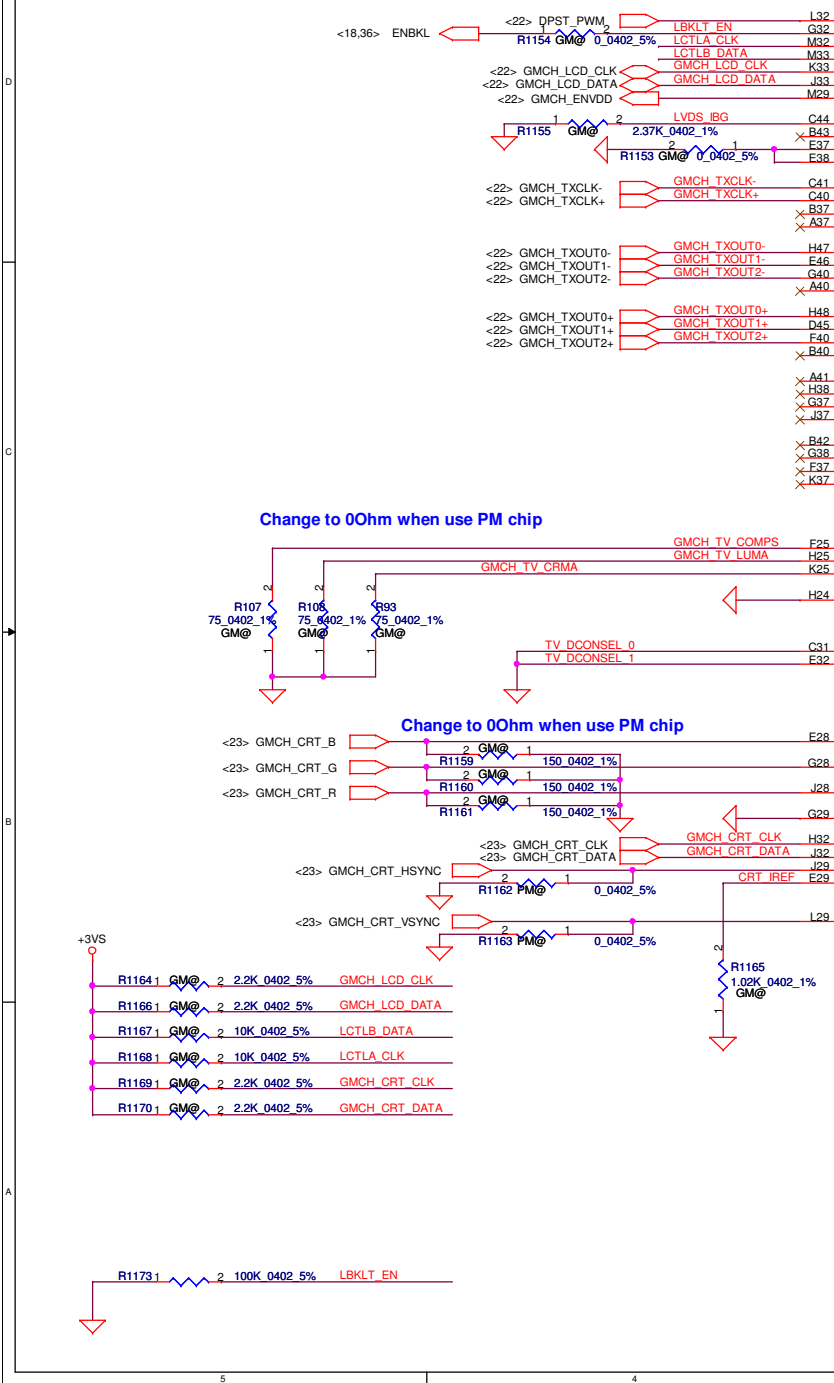


CANTIGA ES_FCBGA1329
GM45@

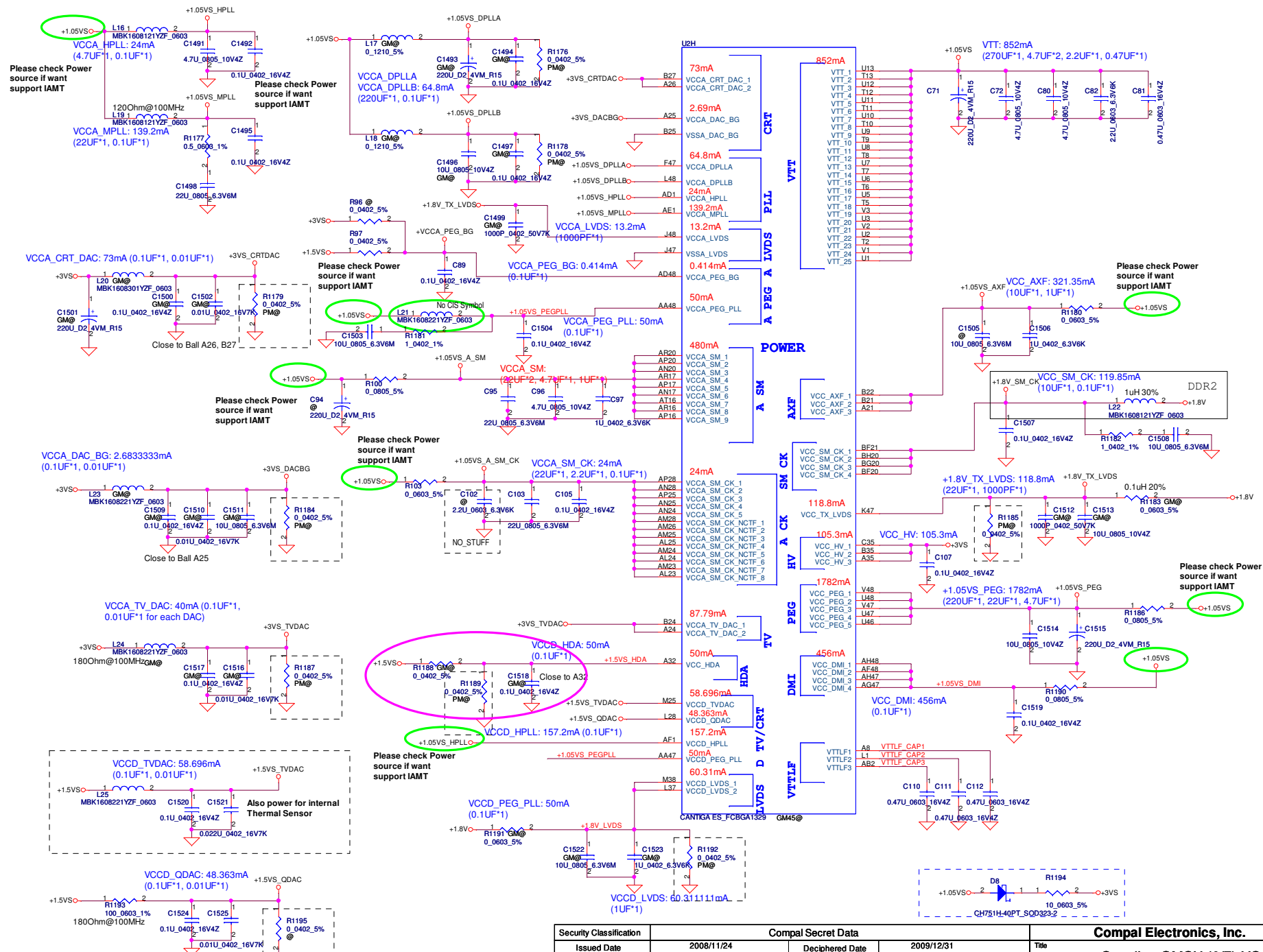


CANTIGA ES_FCBGA1329
GM45@

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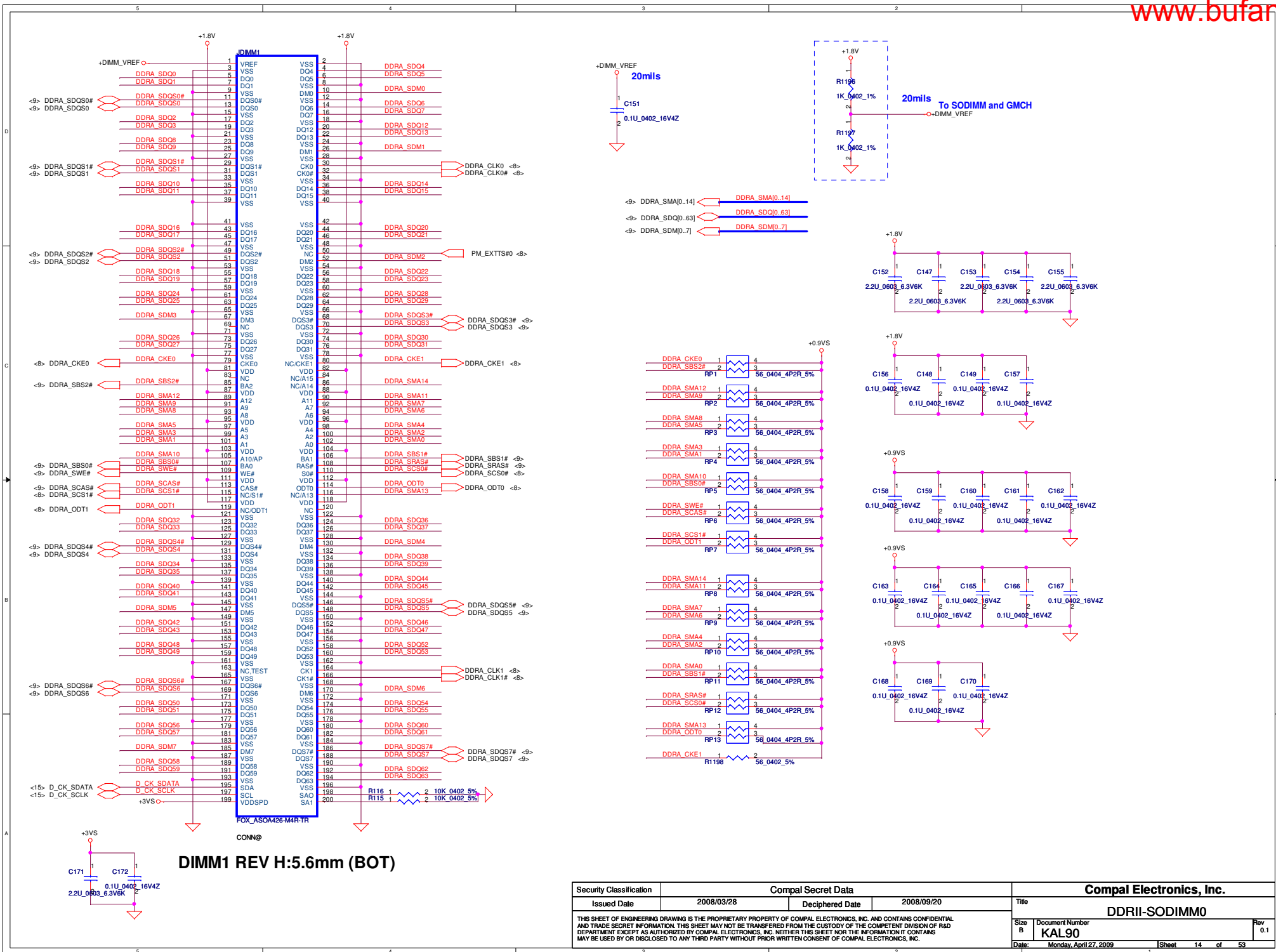
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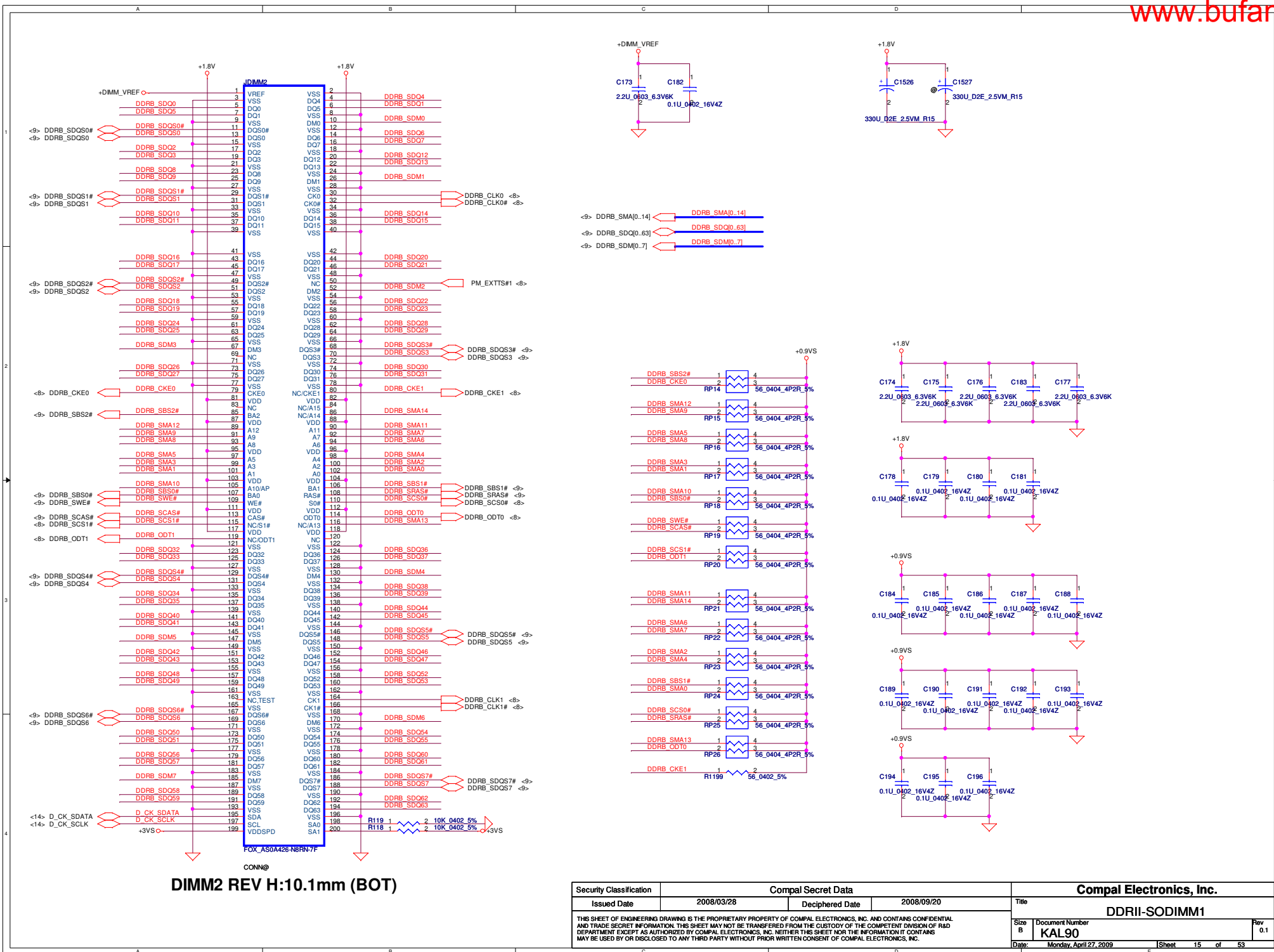


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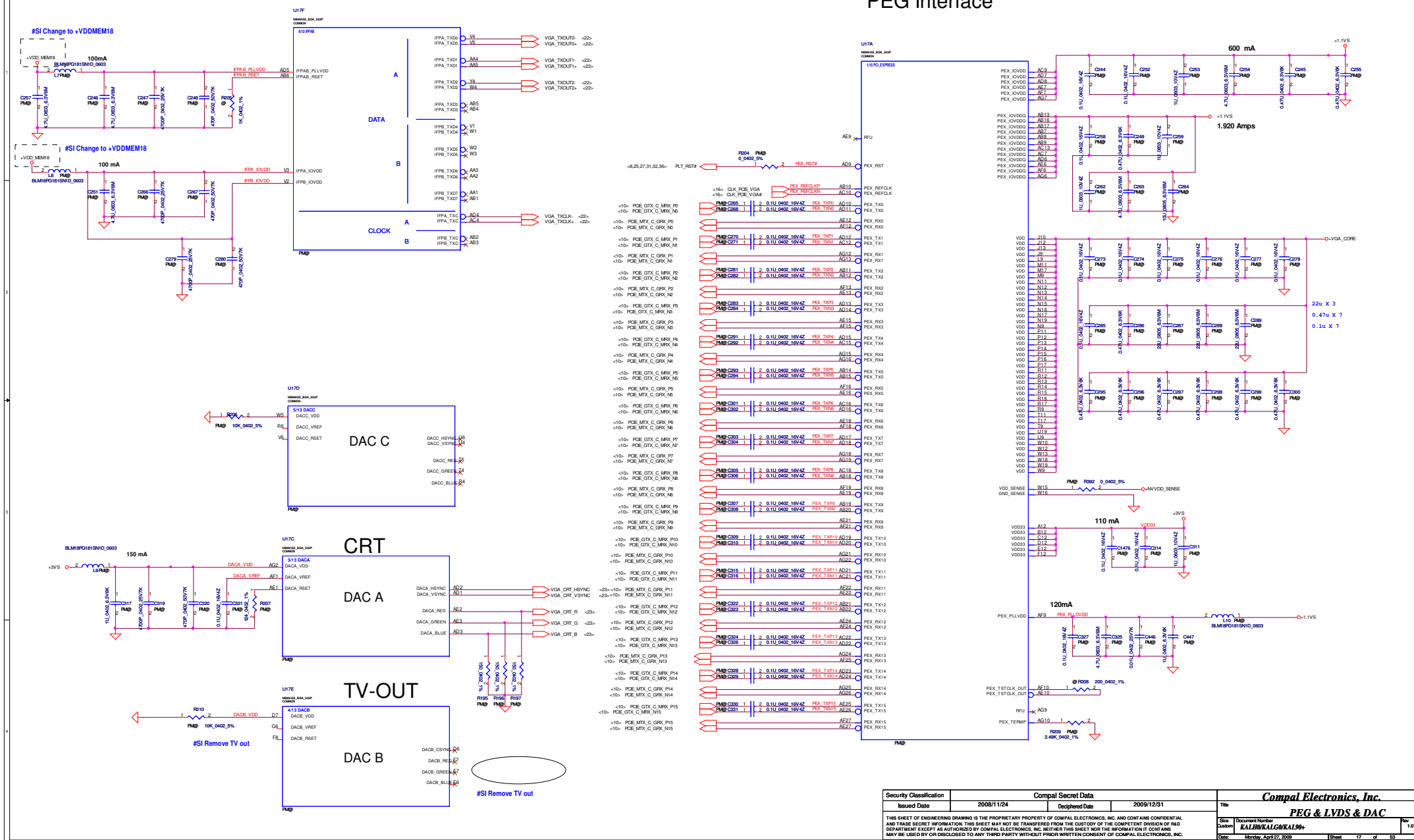
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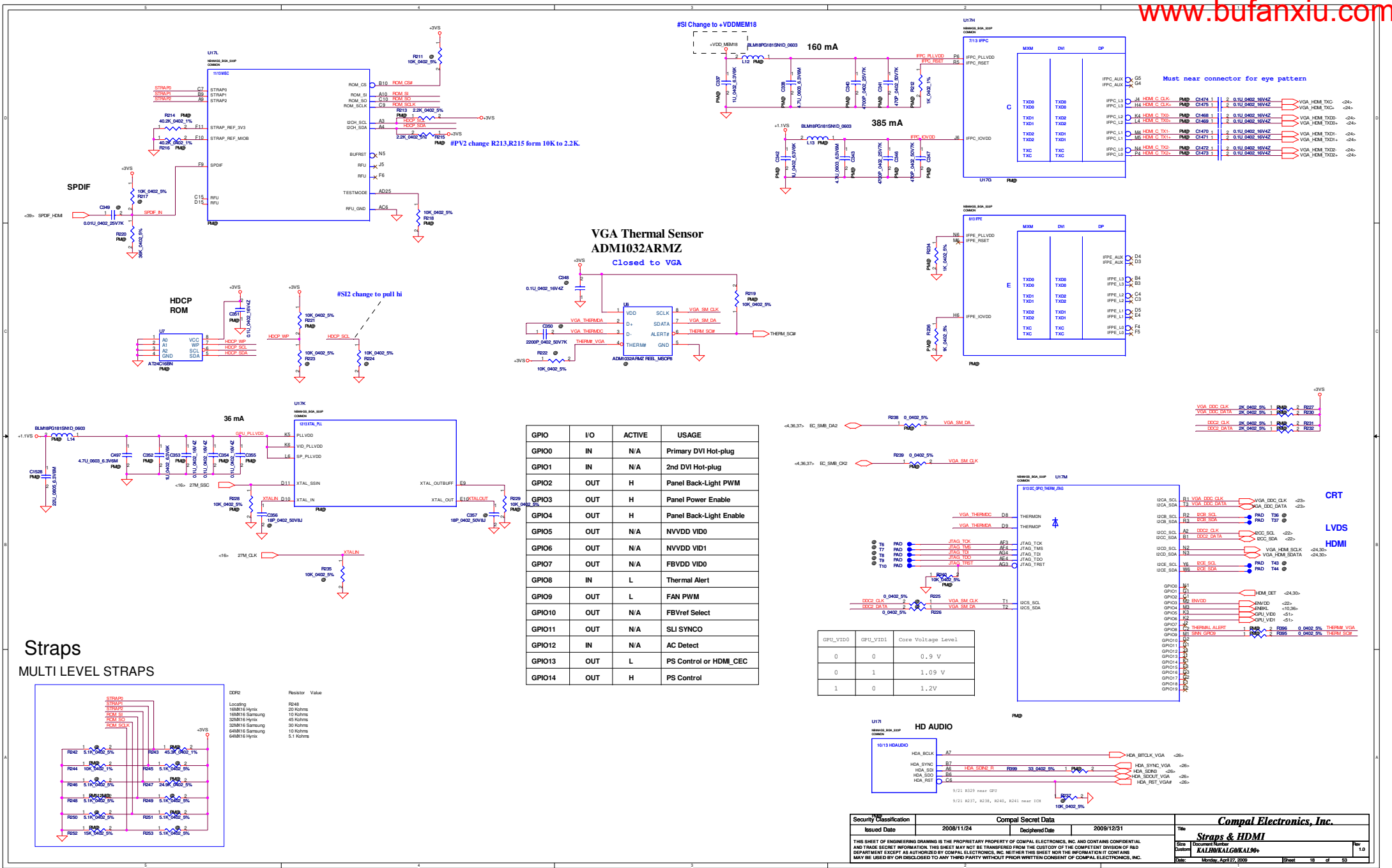


LVDS & DAC Interface

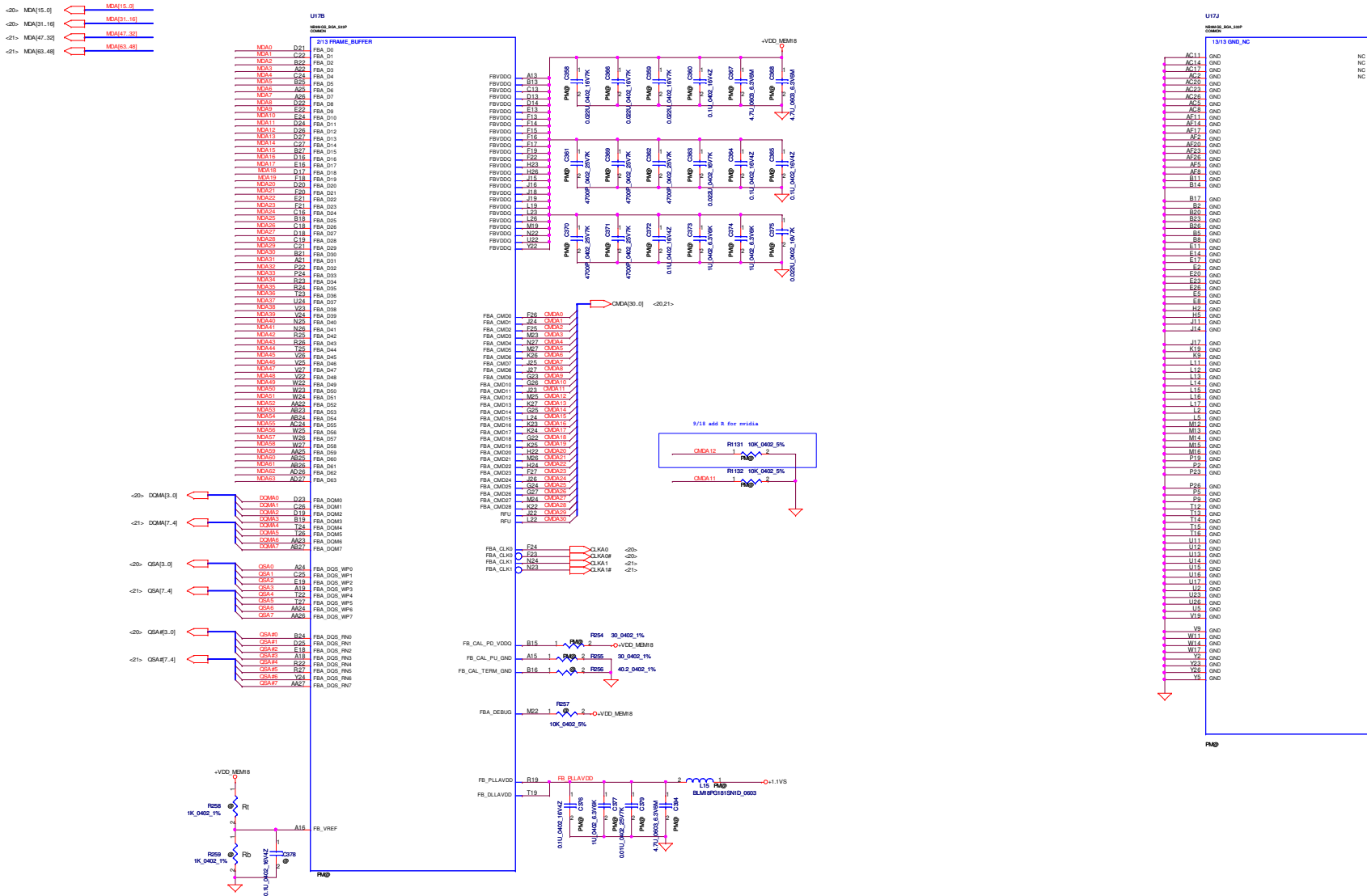
PEG Interface



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VRAM Interface

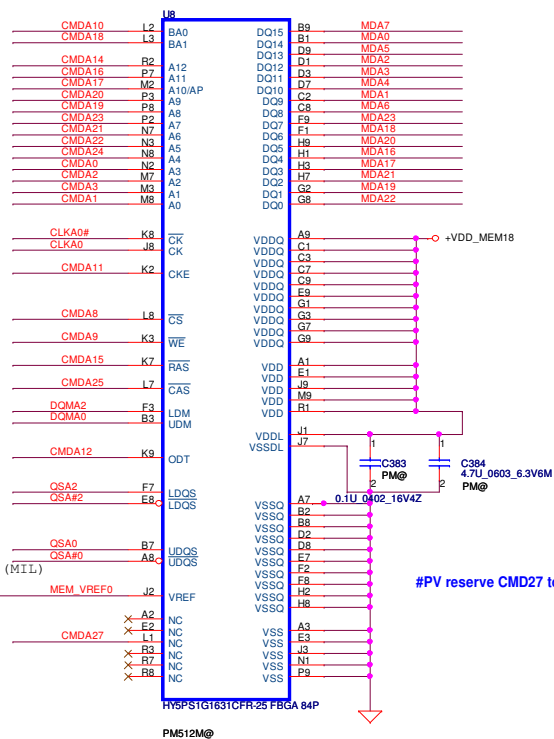
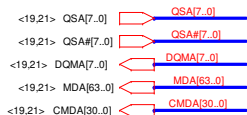


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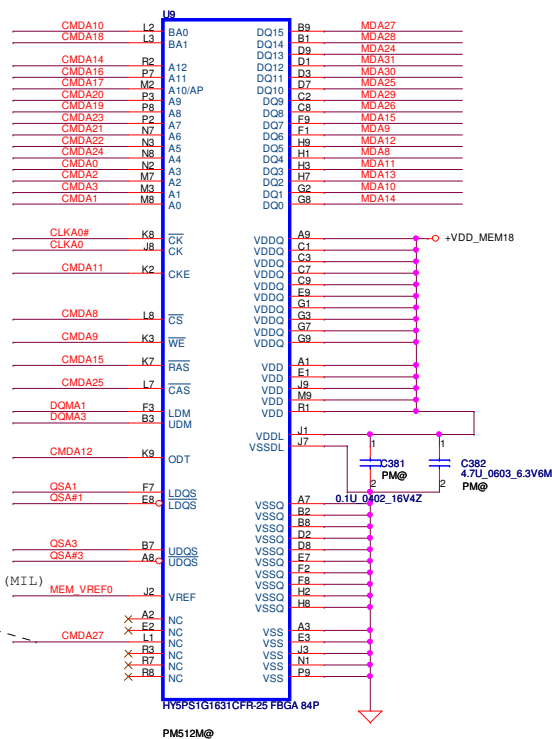
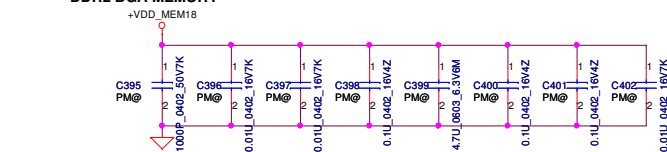
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

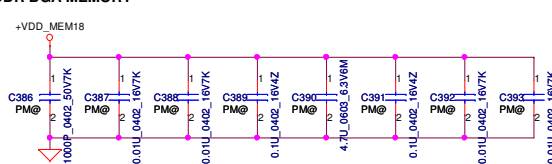
64Mx16 DDR2 400MHz*4==>512MB



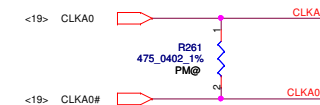
DDR2 BGA MEMORY



DDR BGA MEMORY



Address	DATA Bus
CMD0	A3
CMD1	A0
CMD2	A2
CMD3	A1
CMD4	A3
CMD5	A4
CMD6	A5
CMD7	
CMD8	CS#
CMD9	WE#
CMD10	BA0
CMD11	CKE
CMD12	ODT
CMD13	
CMD14	A12
CMD15	RAS#
CMD16	A11
CMD17	A10
CMD18	BA1
CMD19	A8
CMD20	A9
CMD21	A6
CMD22	A5
CMD23	A7
CMD24	A4
CMD25	CAS#
CMD26	A13
CMD27	BA2
CMD28	
CMD29	
CMD30	

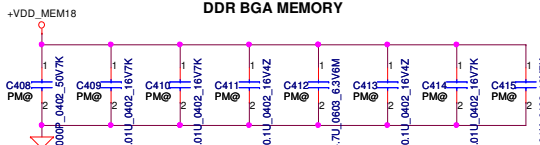
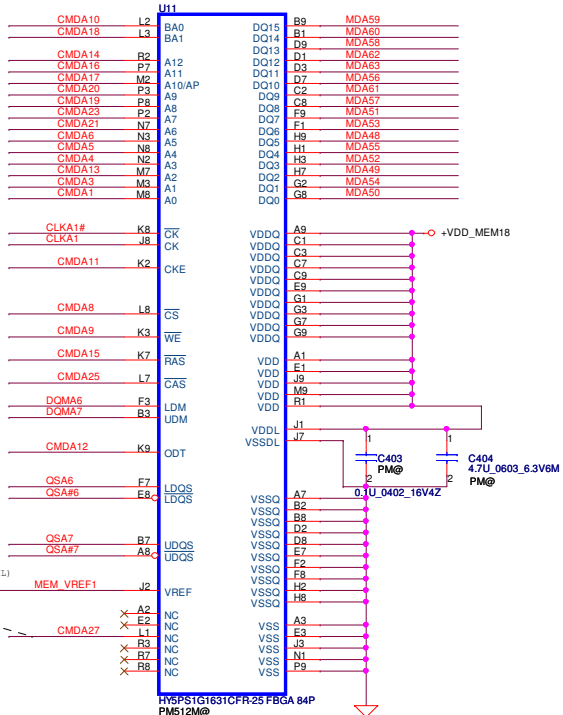
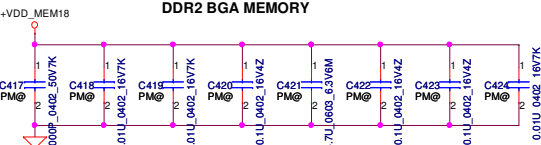
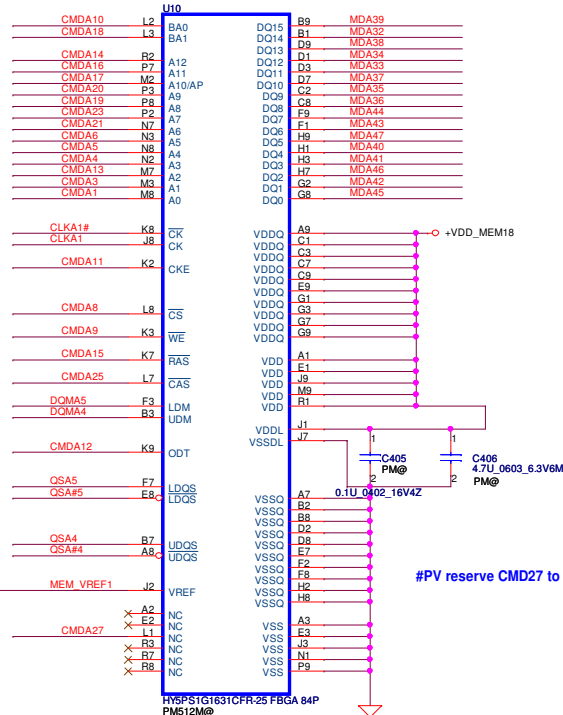
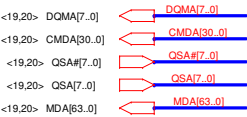


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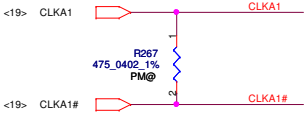
VRAM DDR2 chips (256MB & 512MB)

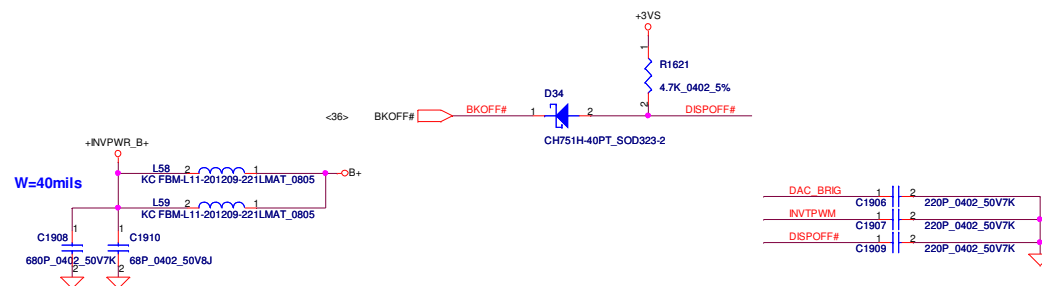
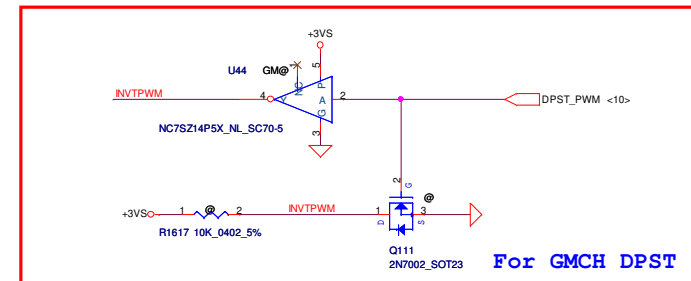
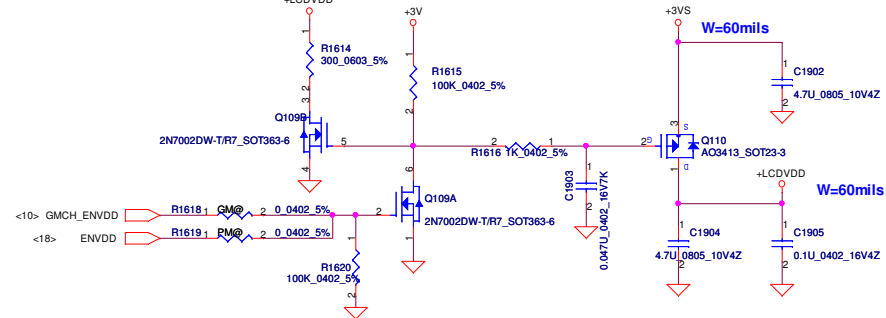
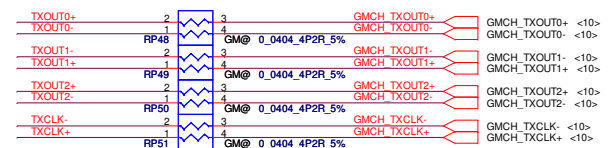
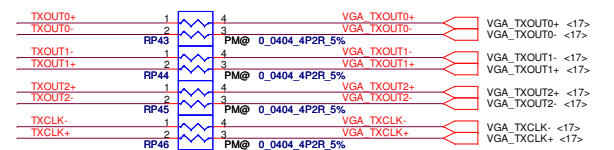
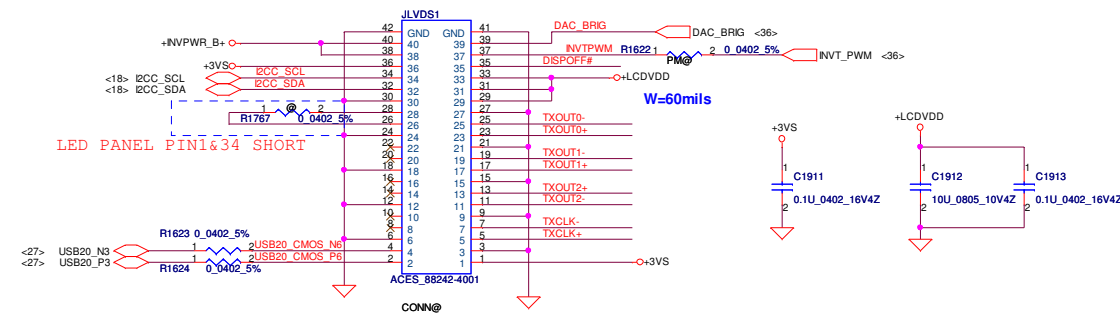
32Mx16 DDR2 400MHz *4==>256MB

64Mx16 DDR2 400MHz*4==>512MB



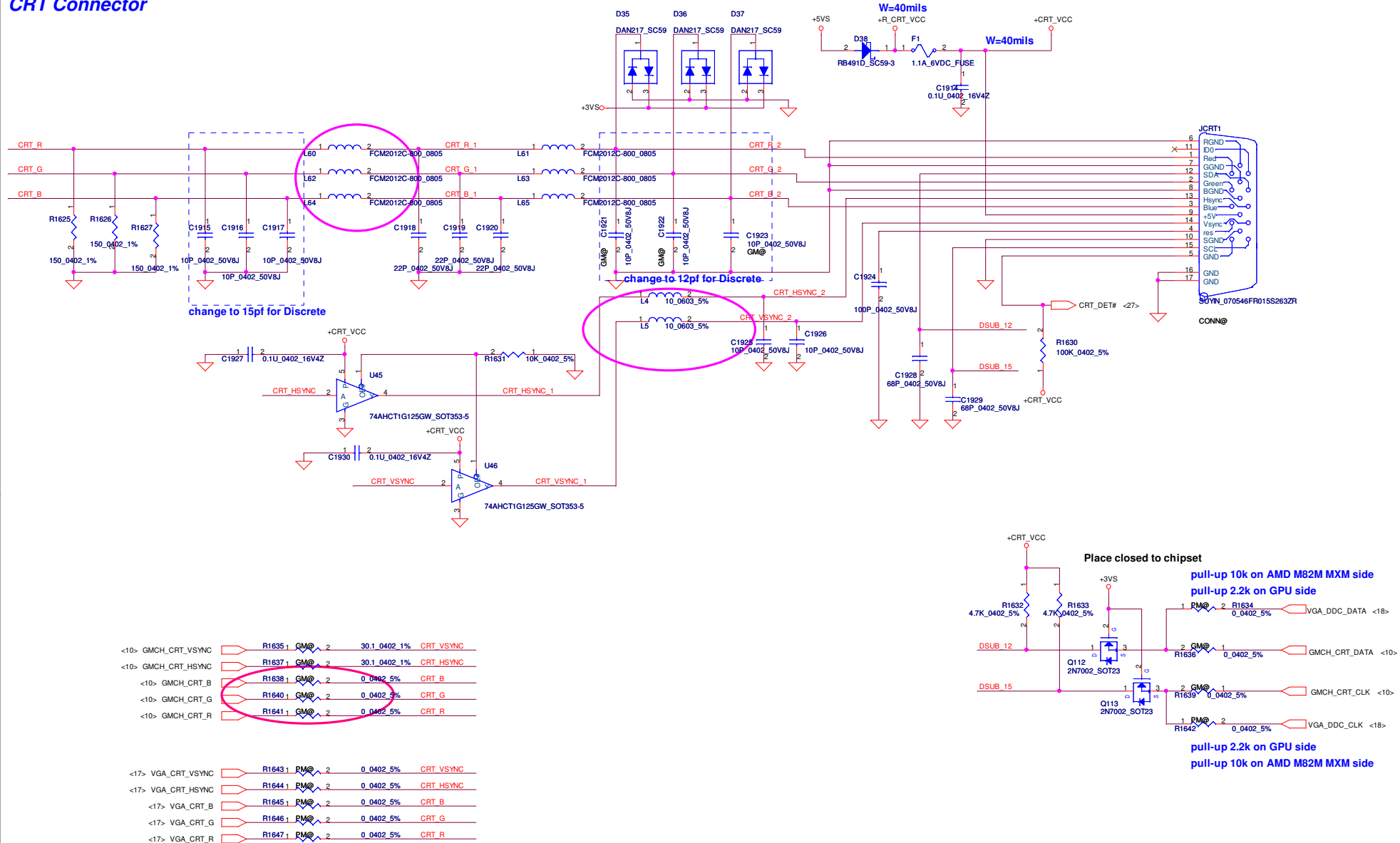
DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



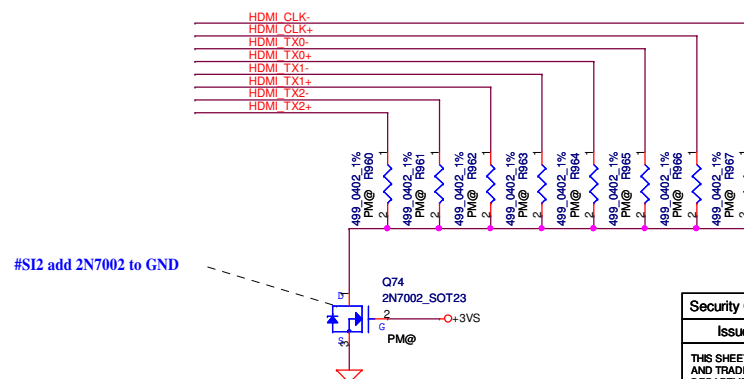
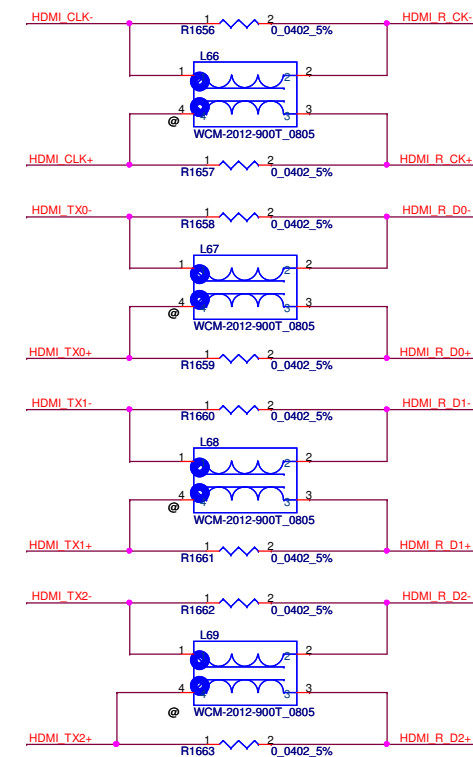
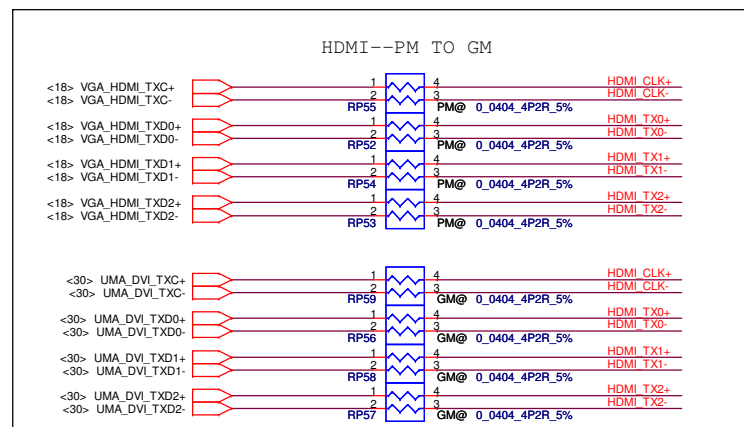
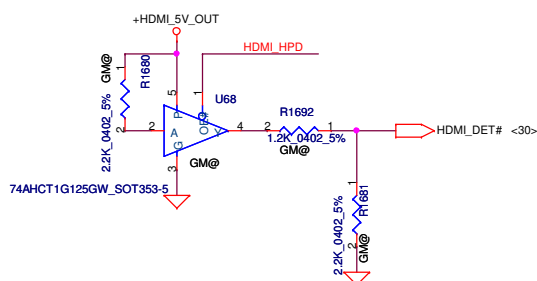
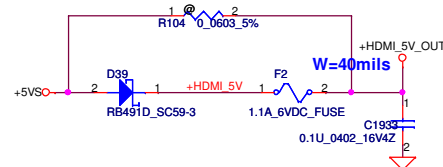
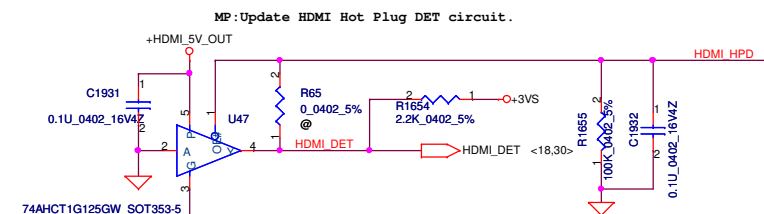
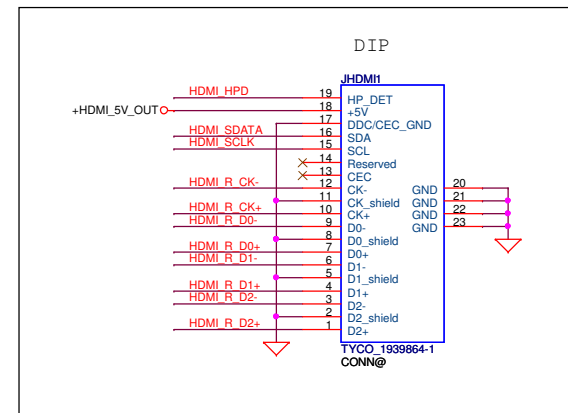
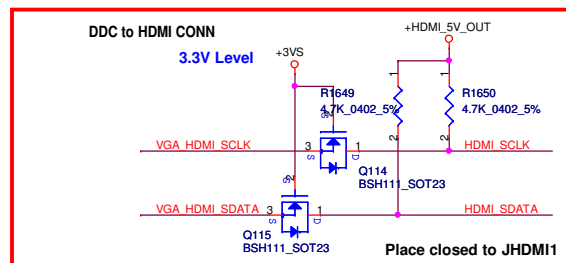
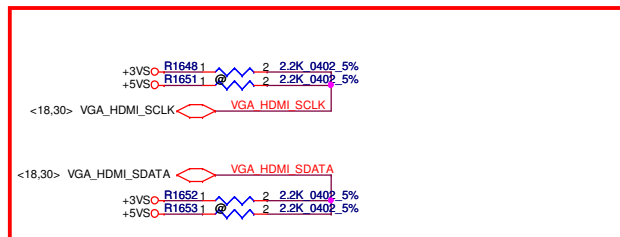
LCD POWER CIRCUIT**LCD/PANEL BD. Conn.**

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Size	Document Number	Customer	KALHO/KALGO/KAL90+	Rev	1.0
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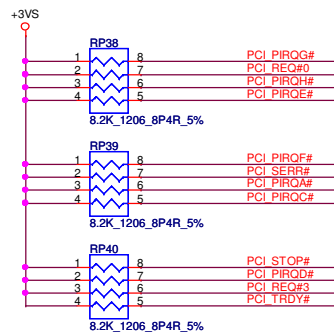
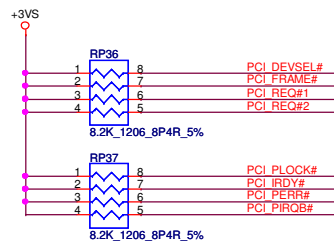
CRT Connector



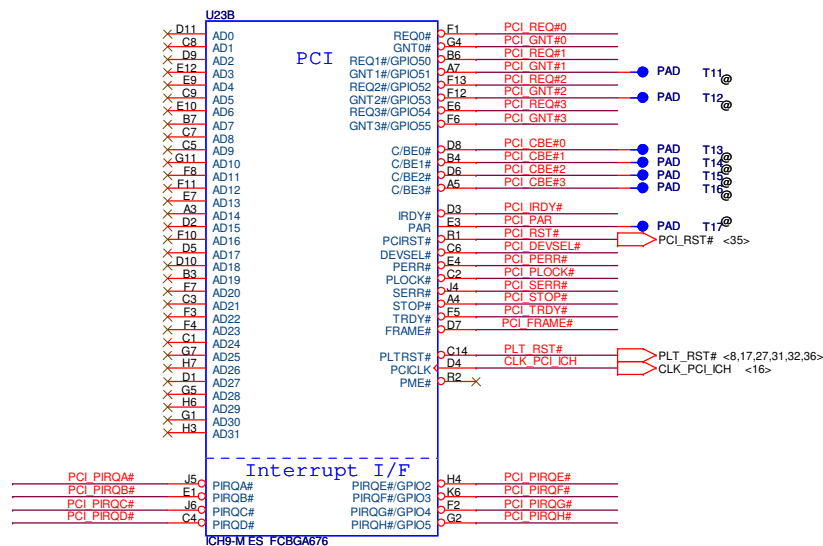
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	
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Size	B	Document Number	KALH0/KALG0/KAL90+	Rev	1.0
Date	Monday, April 27, 2009	Sheet	23	of	53



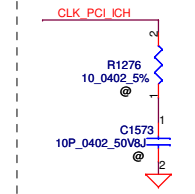
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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	
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Size	Document Number	Date		Sheet	Rev
Custom	KALH0/KALG0/KAL90+	Monday, April 27, 2009		24	1.0
				of	53



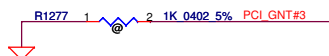
DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)



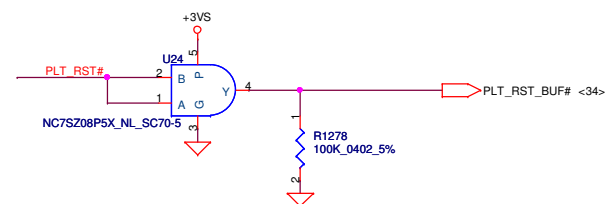
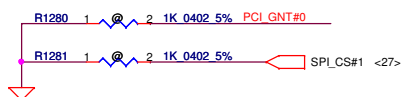
Place closely pin B10



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

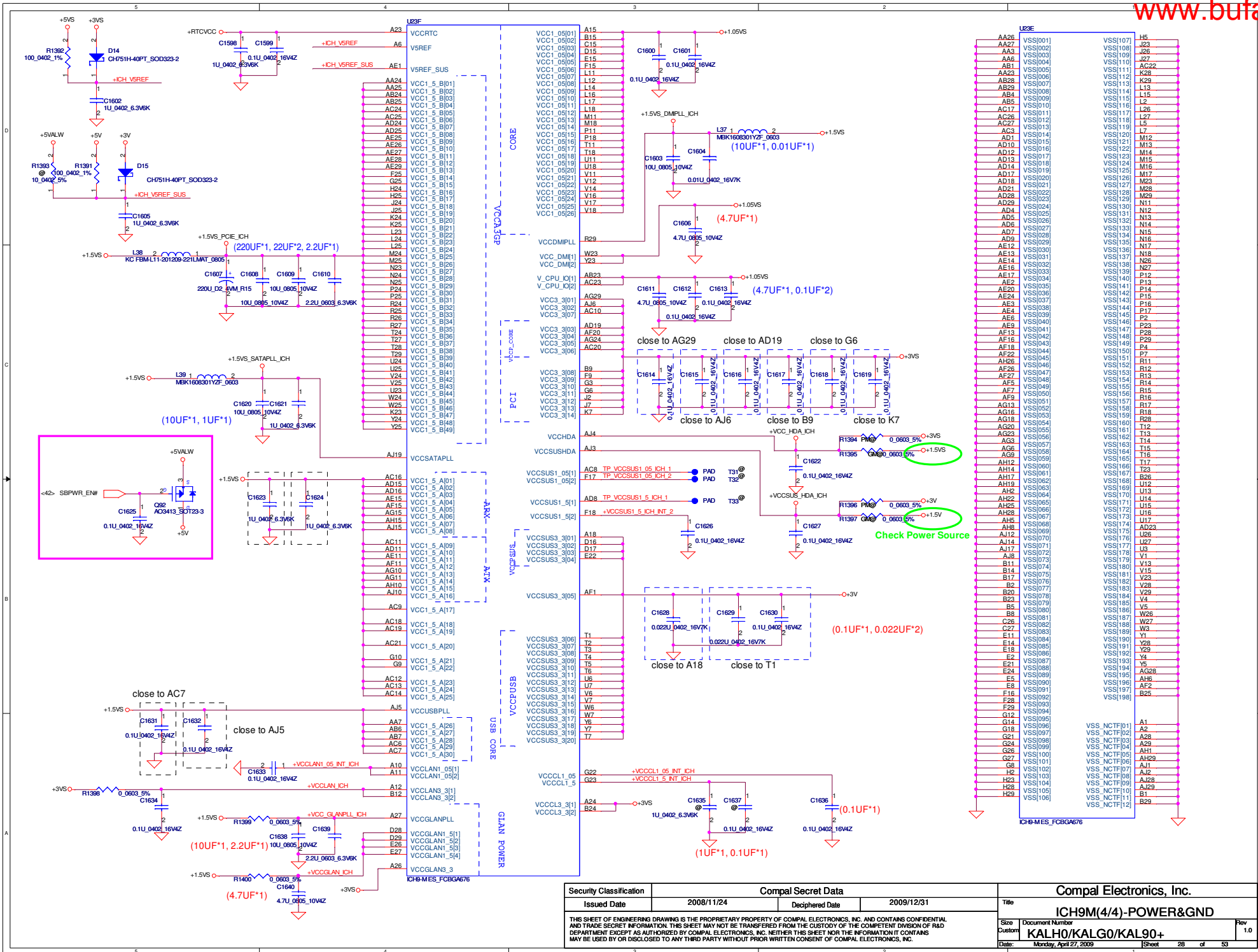


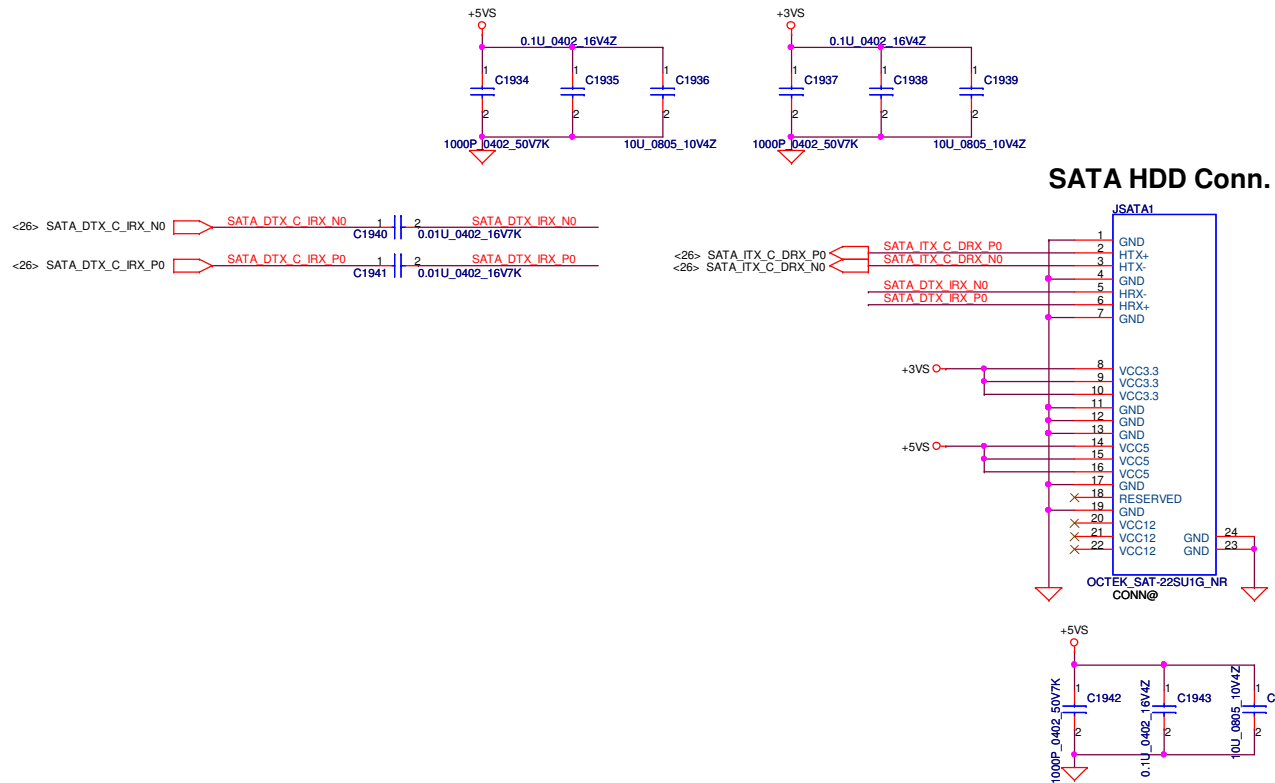
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



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SATA ODD Conn.



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Size		Document Number		Rev	
Custom		KALH0/KALG0/KAL90+		1.0	
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20071029:
C1 (10U_0805) close to JP1.Pin 226, 228, 230

20071029:
C2, C3, C4, C5, C6, C7, C8 (0.1U_0402) close to U1 VCC (+3VS) pins (one Pin one Capacitor)

PCIE_MTX_C_GRPX_N0.1S] <10.17>
PCIE_MTX_C_GRPX_P0.1S] <10.17>

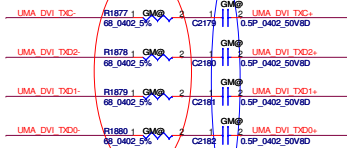
20071210:
R6 change to 1K_0402_1%
(Old - 1.2K)

20071210:
R3 change to 0_0402_1%
(Old-10K)

20071026:
Del R4 (0_0402_5%) for D_DVI_DET remove.

20071210:
R9-R12 change to 68_0402_5%
(Old - 6.8)

Trace AS Short PASSS



20071026:
C9,C10,C11,C12-
Change P/N to SA00000AU00 (0.5P_0402_50V8D)
20080130_PVT
C9,C10,C11,C12-
Change P/N to SE00000HA00 (0.5P 50V C NPO 0402)

20080118 (JAL90_PVT):
Add R17 for Inverting Current

20080128_PVT (change to B version):
SA00001U900 (CH7318A-BF-TR)
SA00001U910 (CH7318B-BF-TR)

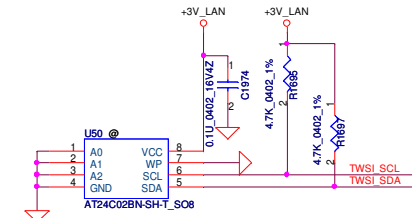
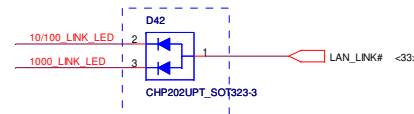
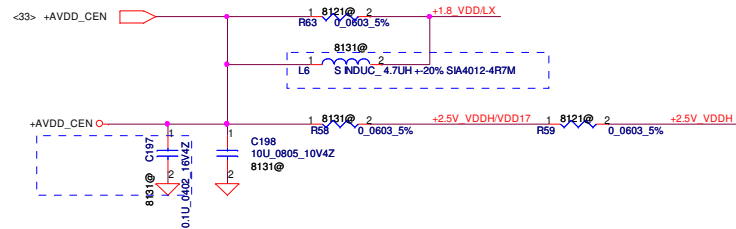
20071031:
Add U1.49 (THERMAL_GND) to GND Plane

Intel Cantiga TMDS Pin Definition

TMDS_B_CLK	PEG_TXP_3
TMDS_B_CLK#	PEG_TXN_3
TMDS_B_DATA0	PEG_TXP_2
TMDS_B_DATA0#	PEG_TXN_2
TMDS_B_DATA1	PEG_TXP_1
TMDS_B_DATA1#	PEG_TXN_1
TMDS_B_DATA2	PEG_TXP_0
TMDS_B_DATA2#	PEG_TXN_0
TMDS_B_HPD#	PEG_RXP_3

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title
				HDM/DVI CH7318
				Size C Document Number
				KALH0/KALG0/KAL90+
				Date: Monday, April 27, 2009 Sheet 30 of 53

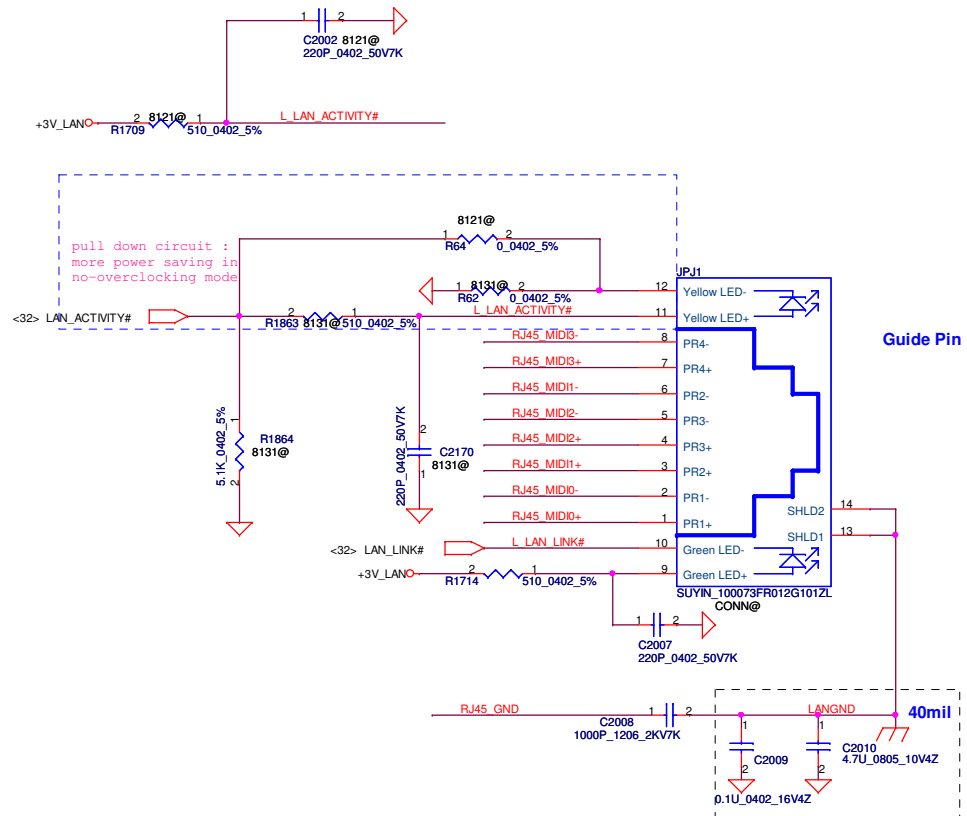
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[illegible]

Pin	Signal	Direction
30	TWSI SDA	Input
29	TWSI SCL	Input
48	10/100 LINK LED	Output
47	LAN_ACT/ITYW	Output
27	LAN_ACTn	Output
26	1000 LINK LED	Output
40	CLK_PCIE_LAN#	Output
41	CLK_PCIE_LAN	Output
14	LAN MID0-	Output
13	LAN MID0+	Output
18	LAN MID1-	Output
17	LAN MID1+	Output
21	LAN MID2-	Output
20	LAN MID2+	Output
24	LAN MID3-	Output
23	LAN MID3+	Output

$+1.2\text{ AVDD}$
 C205 8131@
 1U 0.002 3.34Z
 C206 8121@
 0.1U 0.002 16V4Z
 C207
 0.1U 0.002 16V4Z
 C208
 0.1U 0.002 16V4Z
 C214
 0.1U 0.002 16V4Z
 C215
 0.1U 0.002 16V4Z
 C216
 0.1U 0.002 16V4Z
 C217
 0.1U 0.002 16V4Z

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				Rev 1.0	
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L LAN ACTIVITY#

1 2

C2011 @ 68P_0402_50V8J

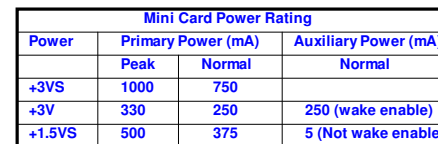
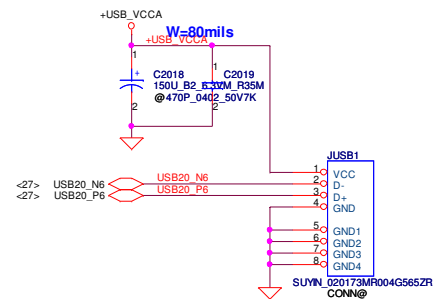
L LAN LINK#

1 2

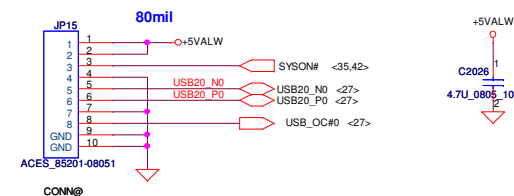
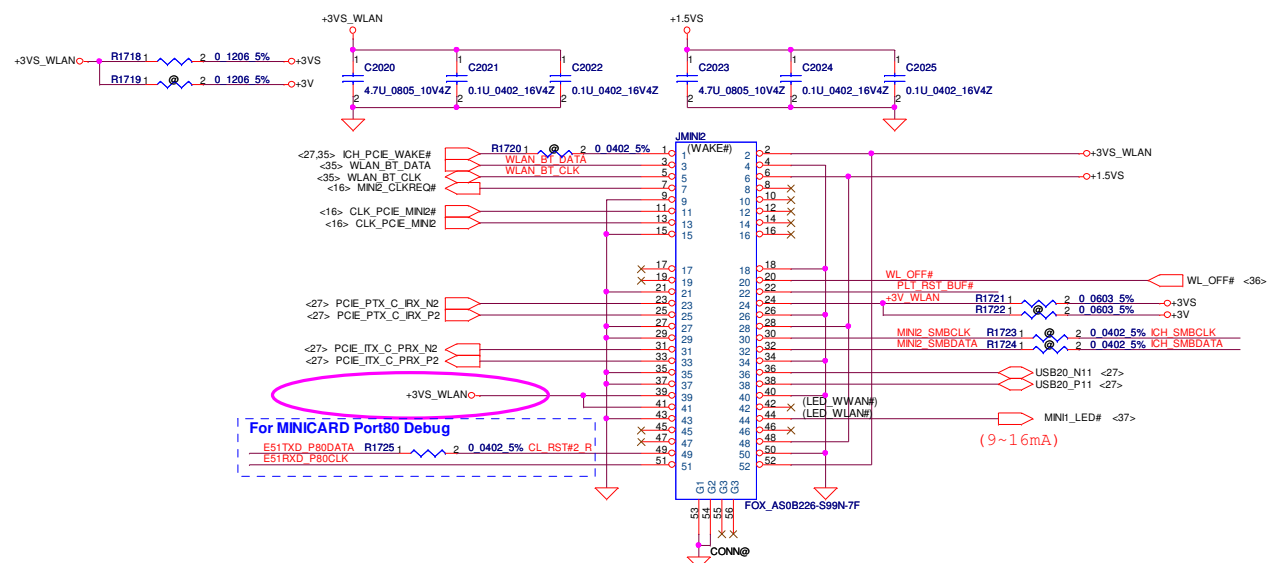
C2012 @ 68P_0402_50V8J

For EMI

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				B	KALH0/KALG0/KAL90+		1.0
				Date:	Monday, April 27, 2009		Sheet 33 of 53

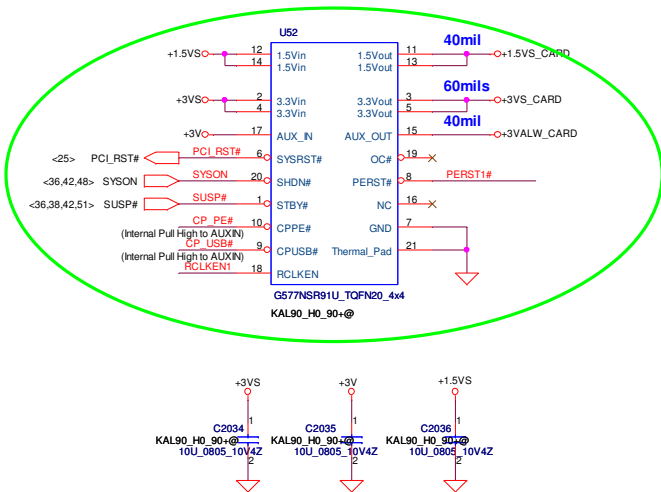
**USB CONN.**

For Wireless LAN

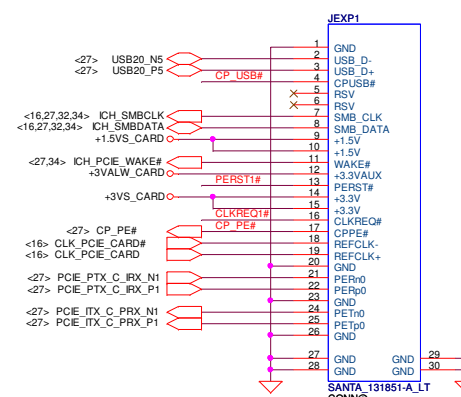


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				Date:	Monday, April 27, 2009	Sheet 34 of 53

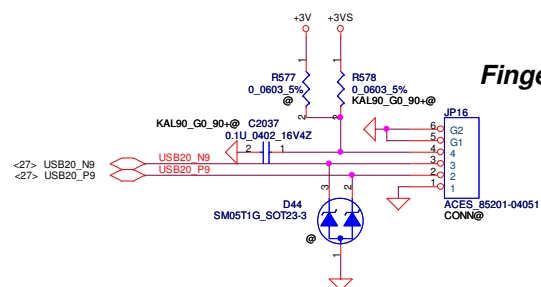
New Card Power Switch



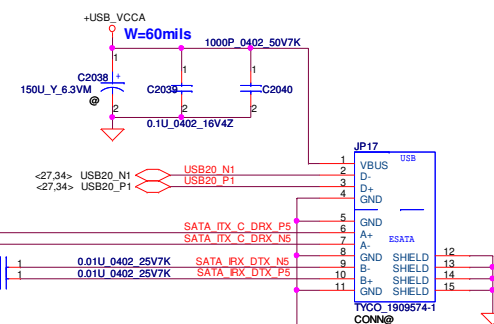
New Card Socket (Left/TOP)



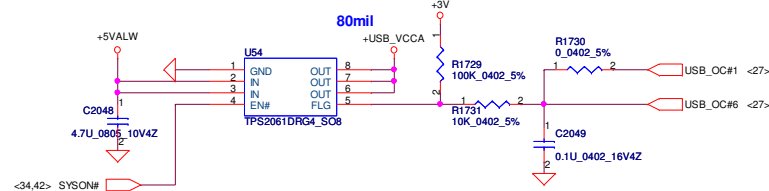
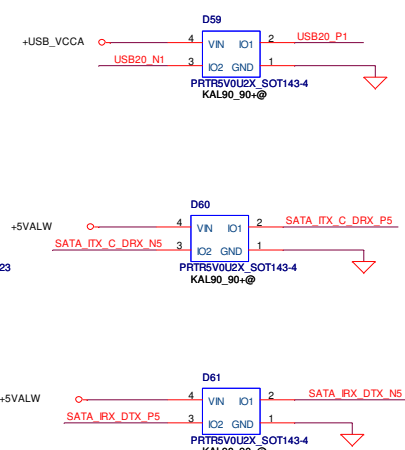
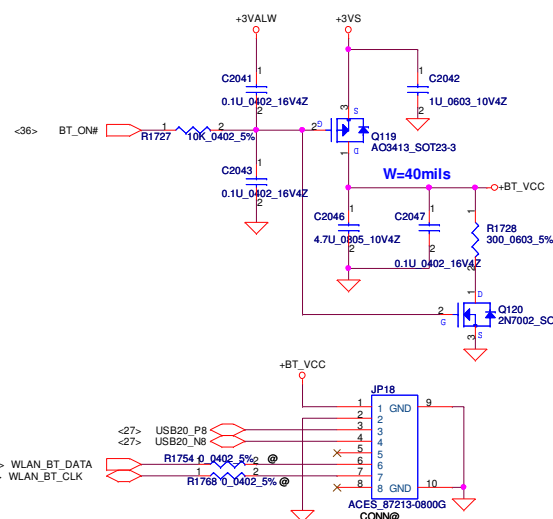
Finger Print Conn.



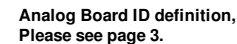
ESATA CONN



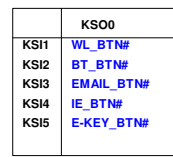
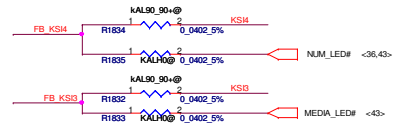
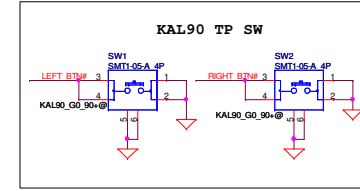
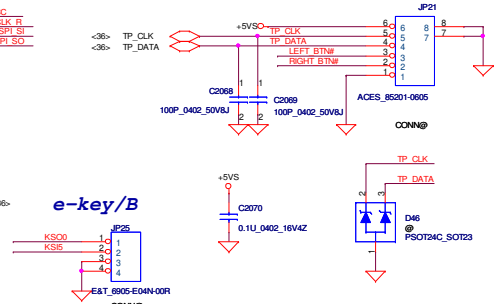
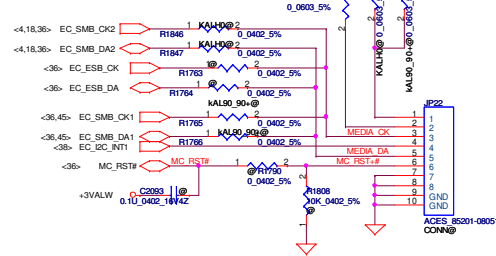
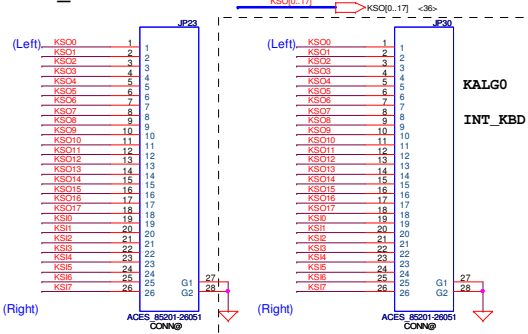
Bluetooth Conn.



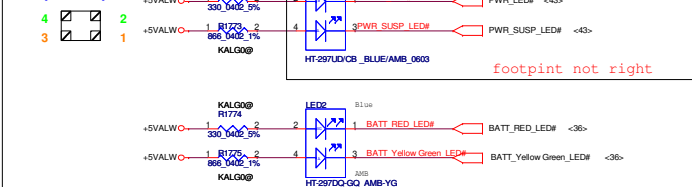
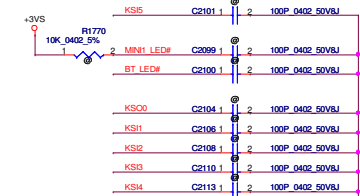
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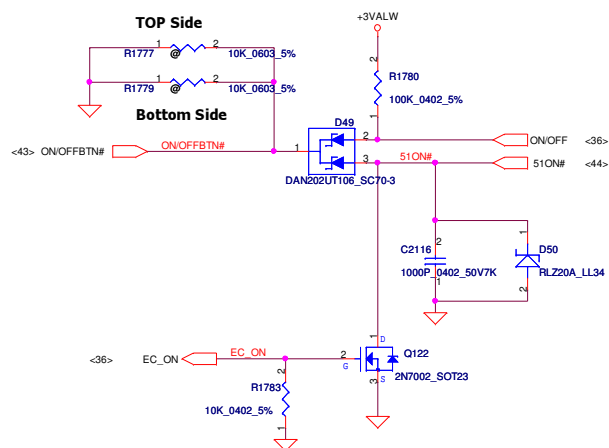
(Hall Effect Switch)



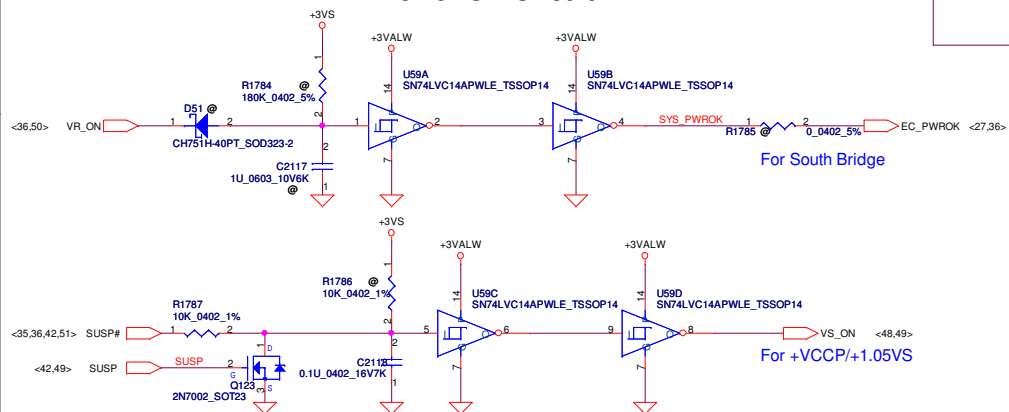
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Power Button

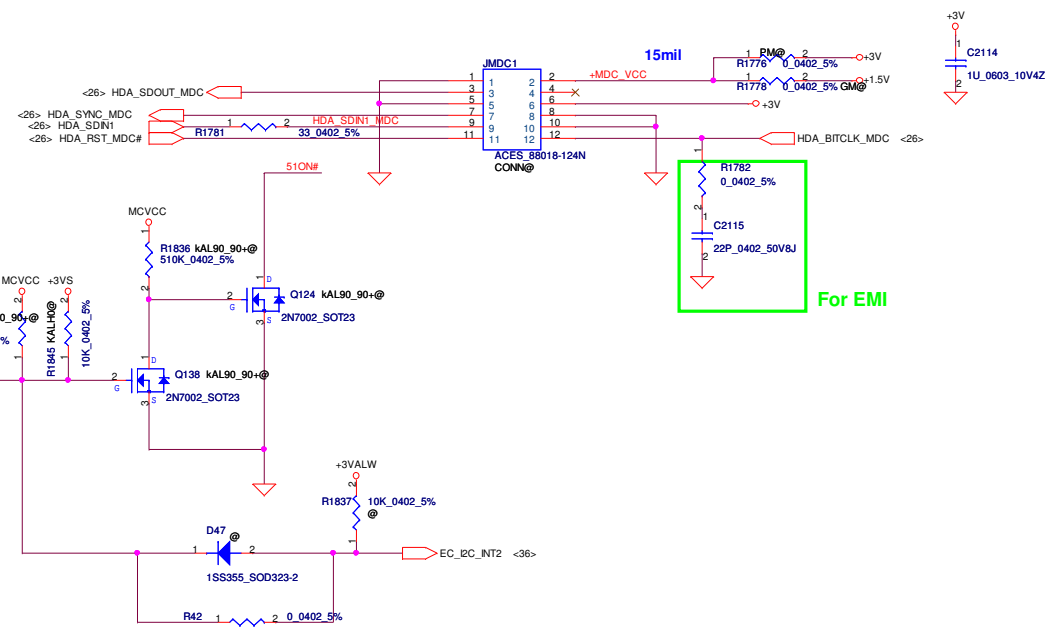
ON/OFF switch



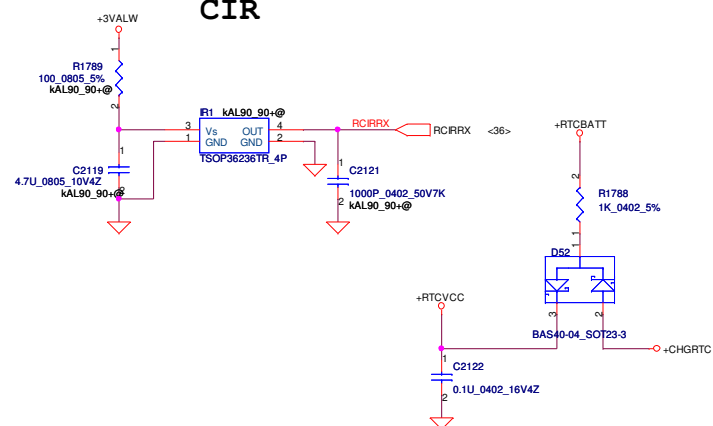
Power ON Circuit



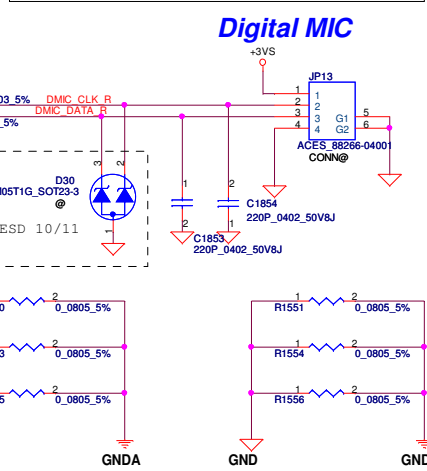
HDA MDC Conn.



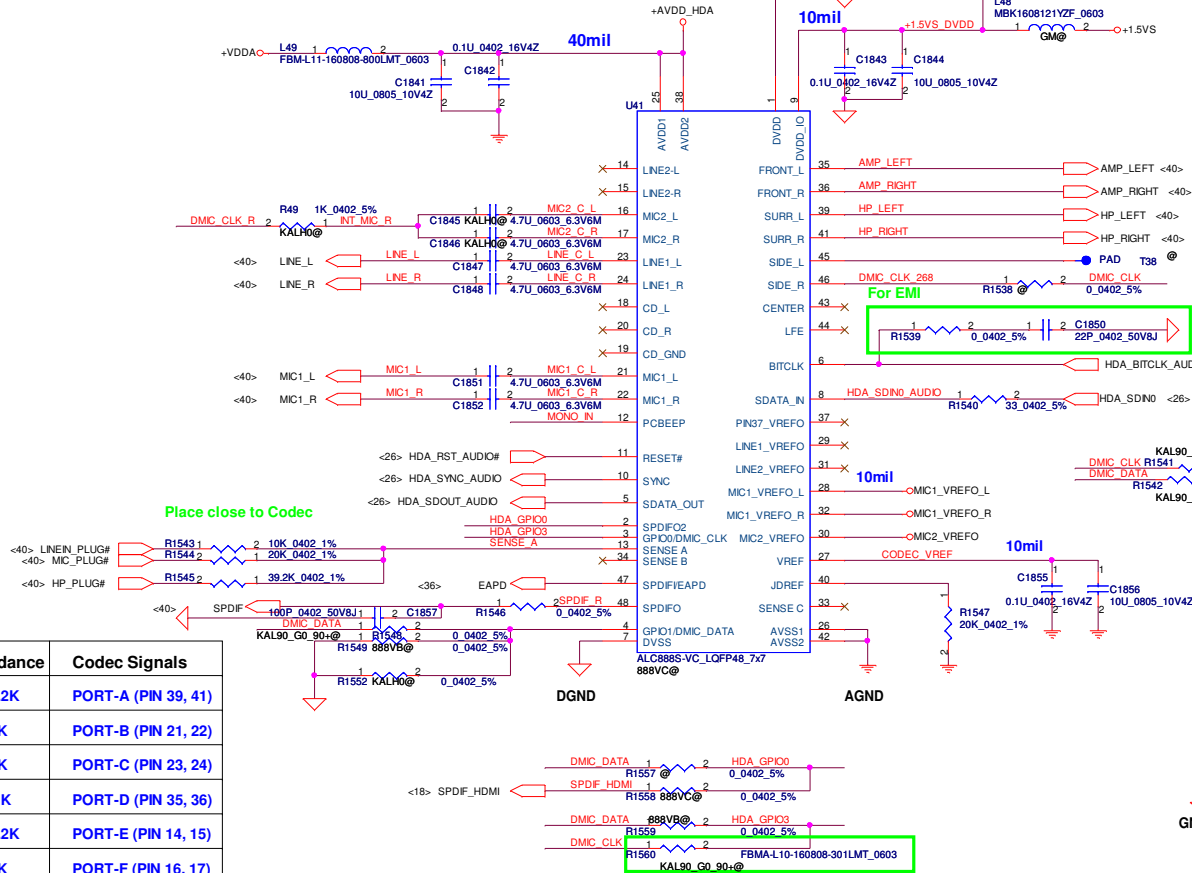
CIR



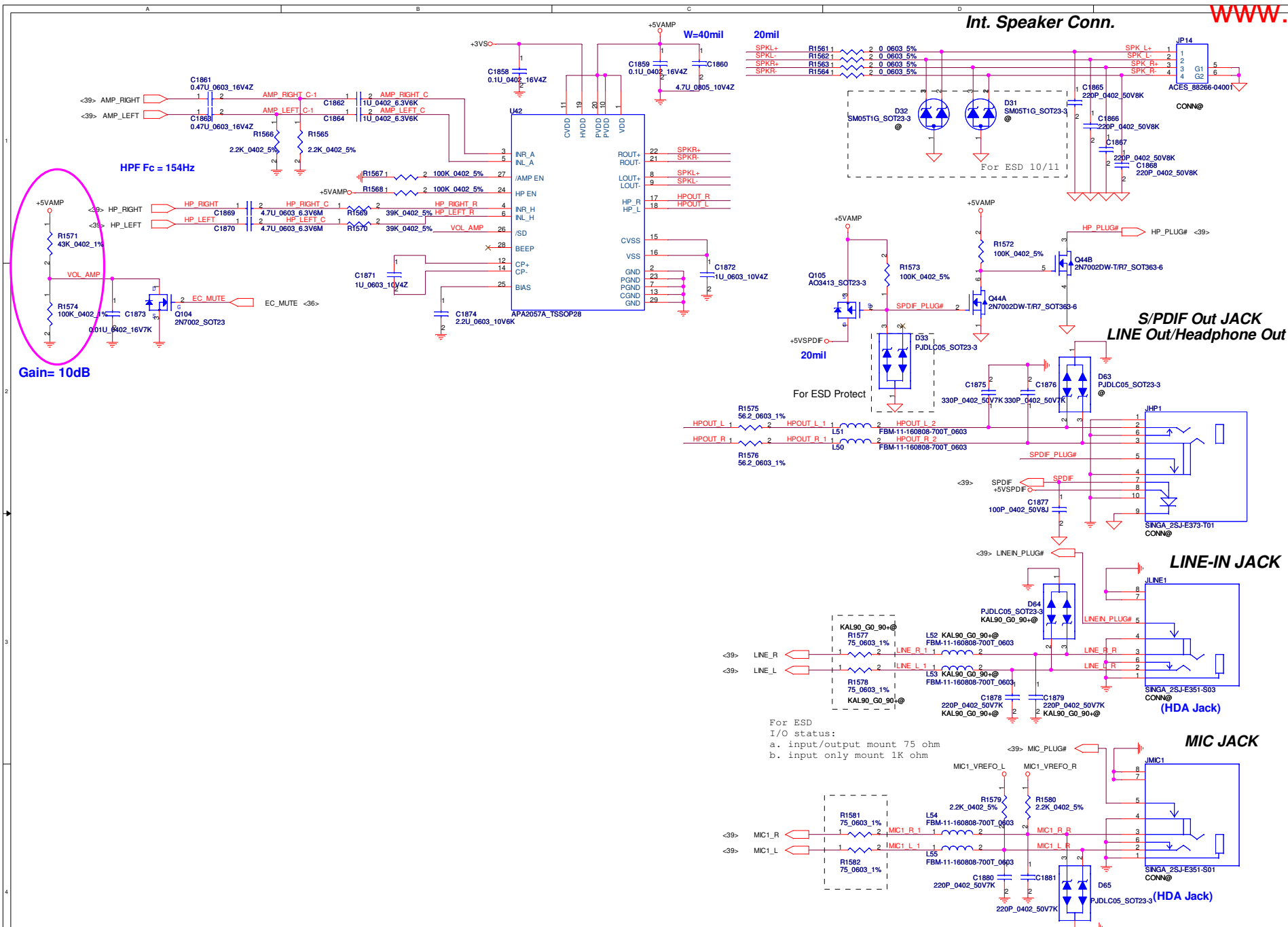
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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	
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				KALH0/KALG0/KAL90+	
				Date: Monday, April 27, 2009	Sheet 38 of 53



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

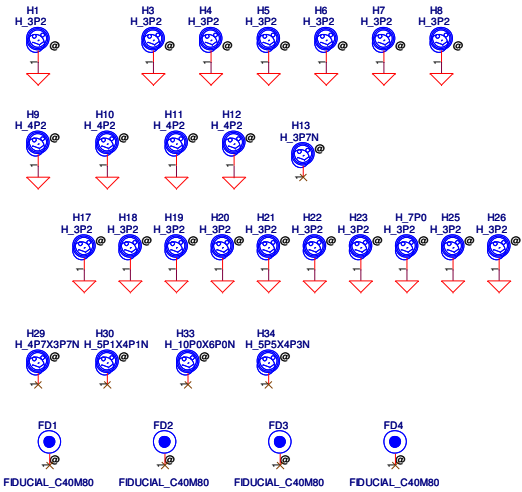
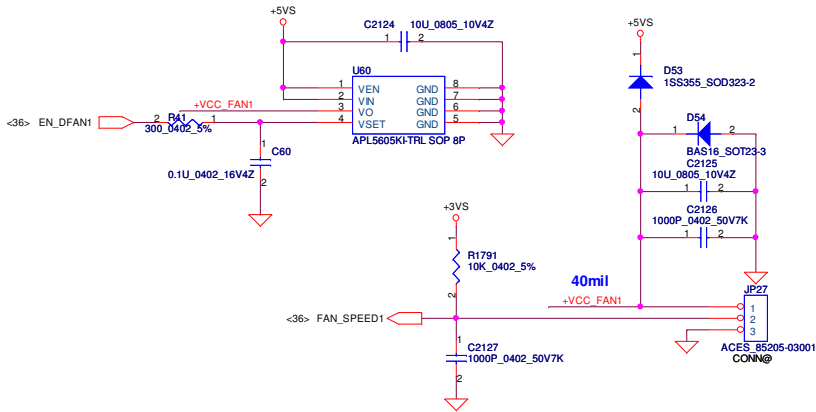


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								Size	Document Number	Rev
								KALH0/KALG0/KAL90+	1.0	1.0
								Date:	Monday, April 27, 2009	Sheet

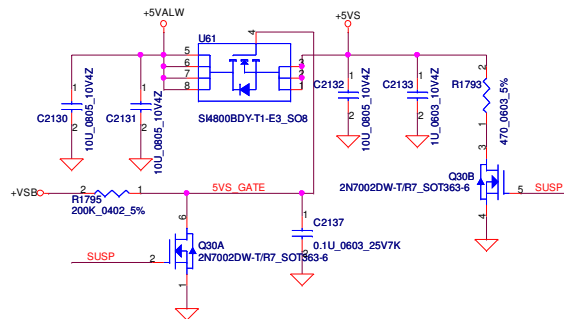
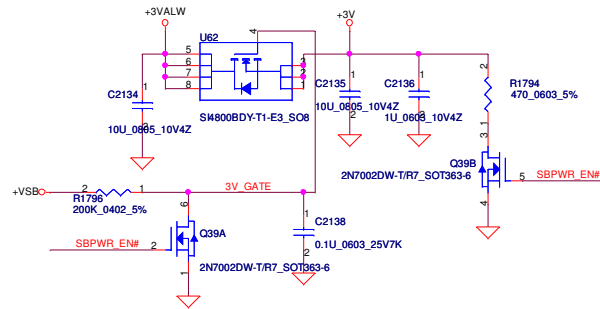
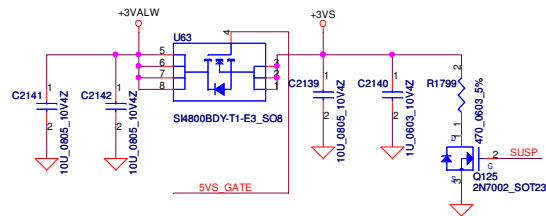
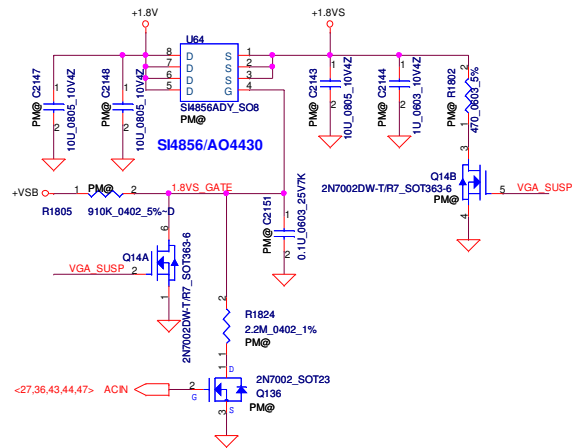
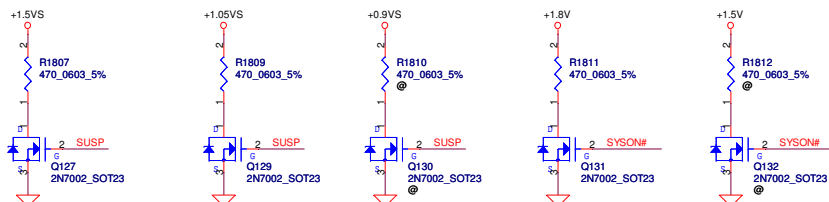
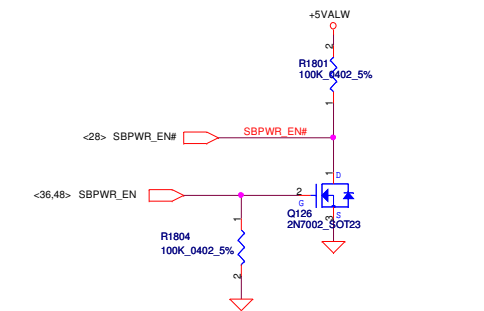
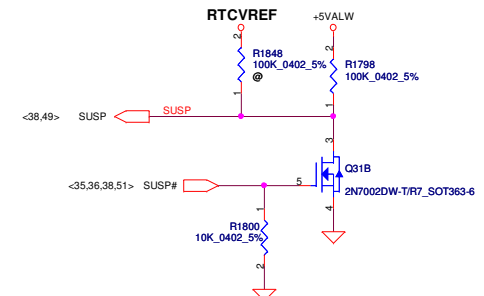
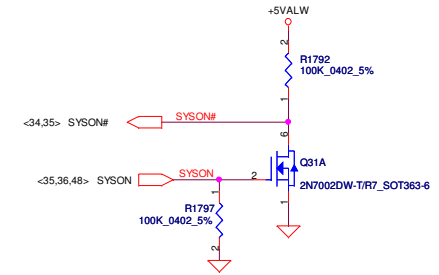
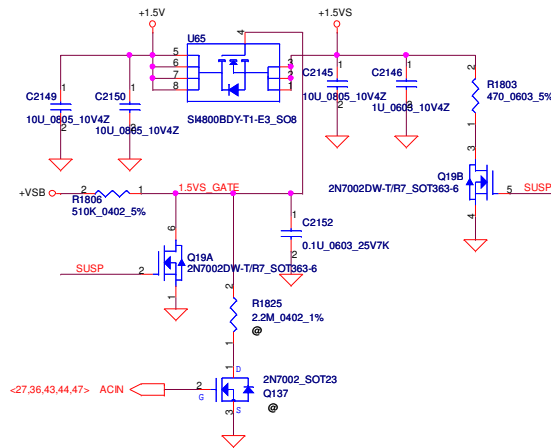


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				B	KALH0/KALG0/KAL90+	1.0
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FAN1 Conn

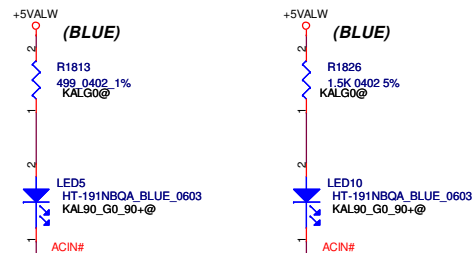


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Size		Document Number			Rev
B		KALH0/KALG0/KAL90+			1.0
Date:		Monday, April 27, 2009		Sheet 41 of 53	

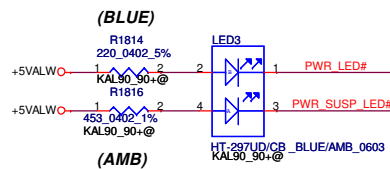
+5VALW TO +5VS**+3VALW TO +3V_SB(ICH8M AUX Power)****+3VALW TO +3VS****+1.8V to +1.8VS****+1.5V to +1.5VS**

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Size B	Document Number	KALHO/KALGO/KAL90+		Date	Monday, April 27, 2009
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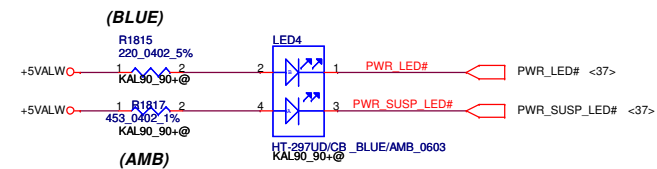
Enlightener LED



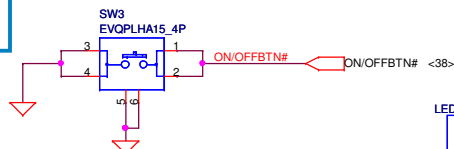
ON/OFF LED LEFT



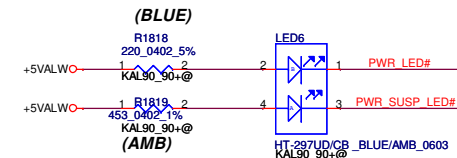
ON/OFF LED RIGHT



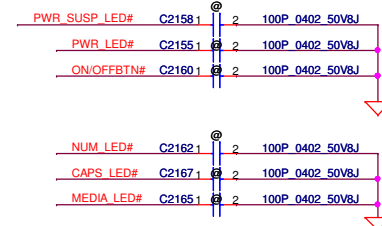
ON/OFF Button



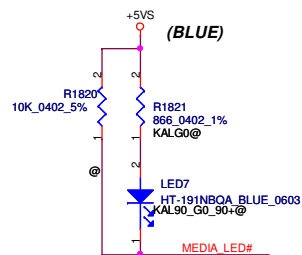
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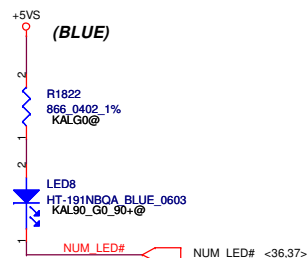
FOR EMI



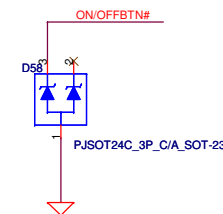
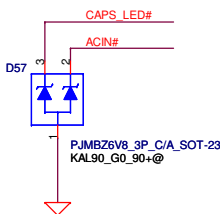
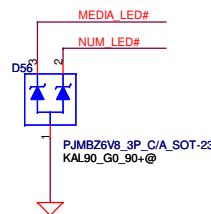
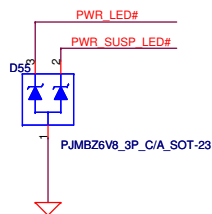
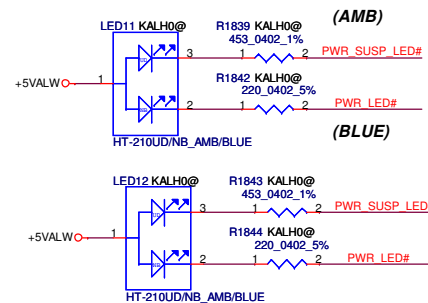
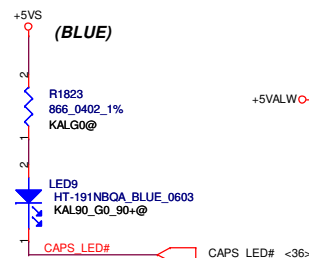
MEDIA_LED



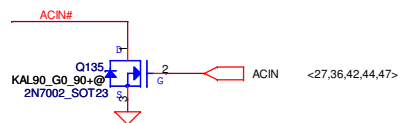
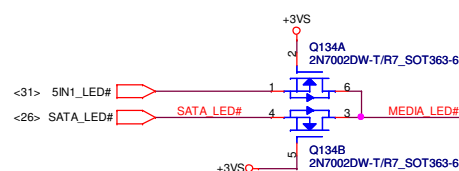
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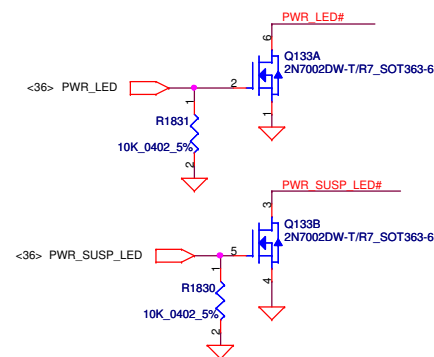
CAPS_LED



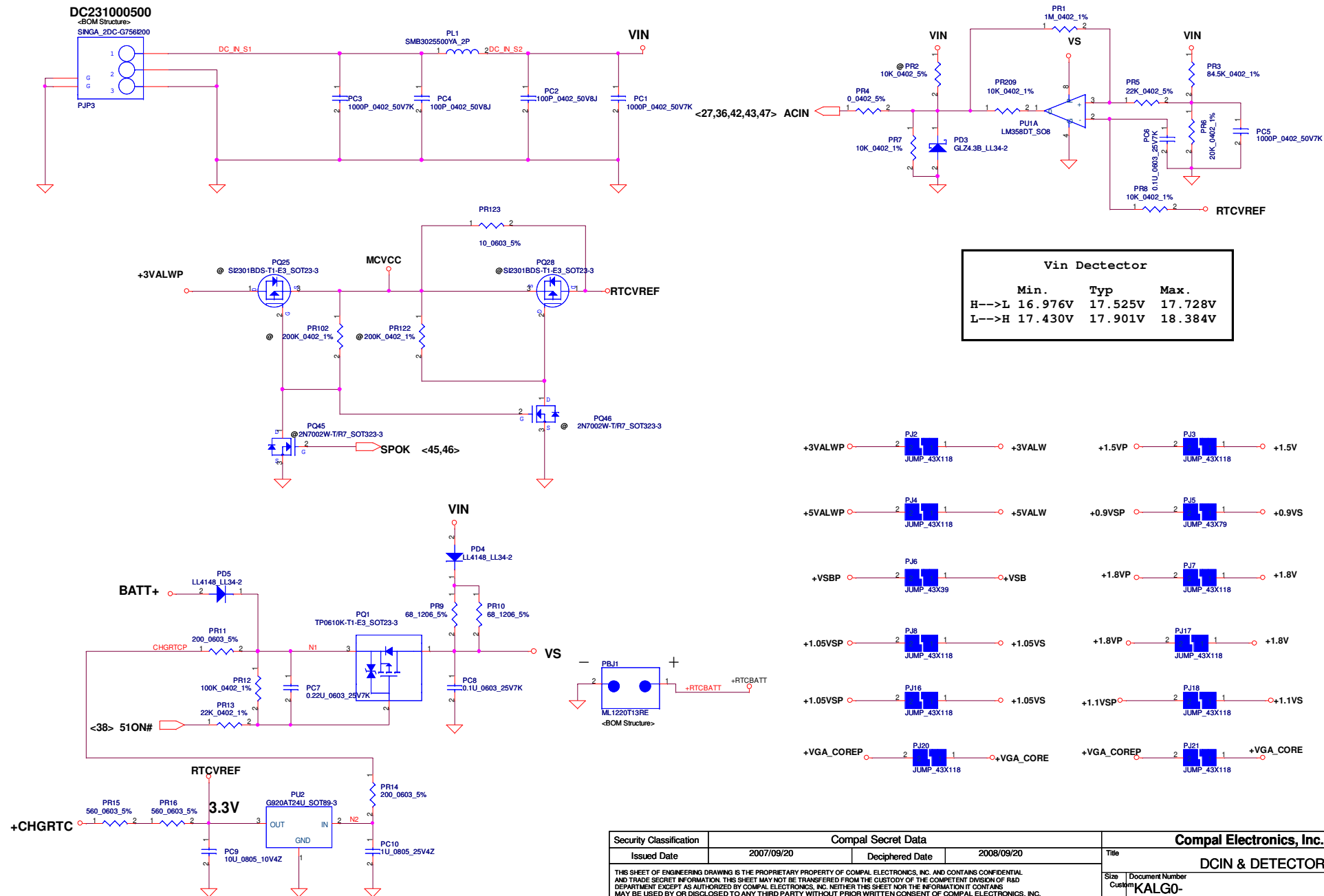
D1 D2 D3 USE PANJIT PJMBZ6V8
SCA00000100
6.8V



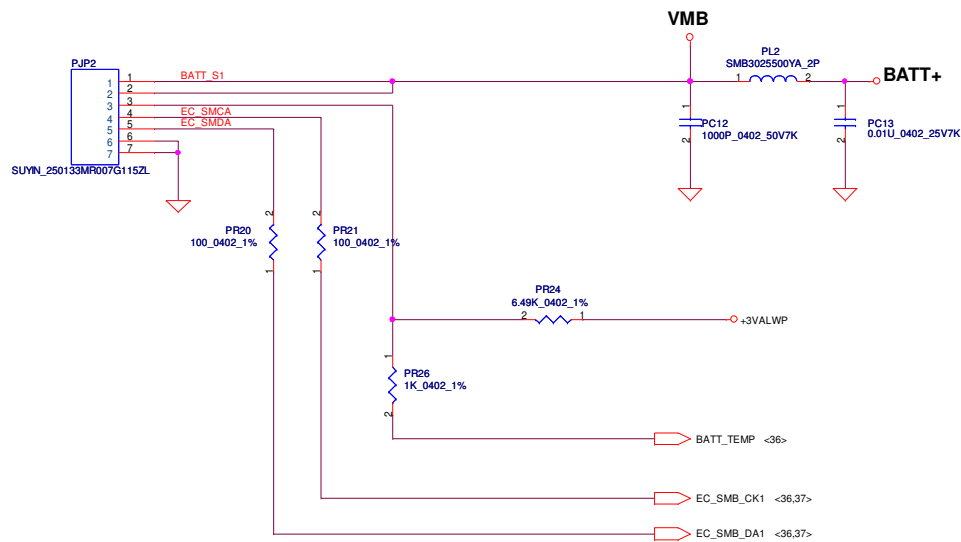
D4 USE
PJSOT24C 3P C/A SOT-23
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24V



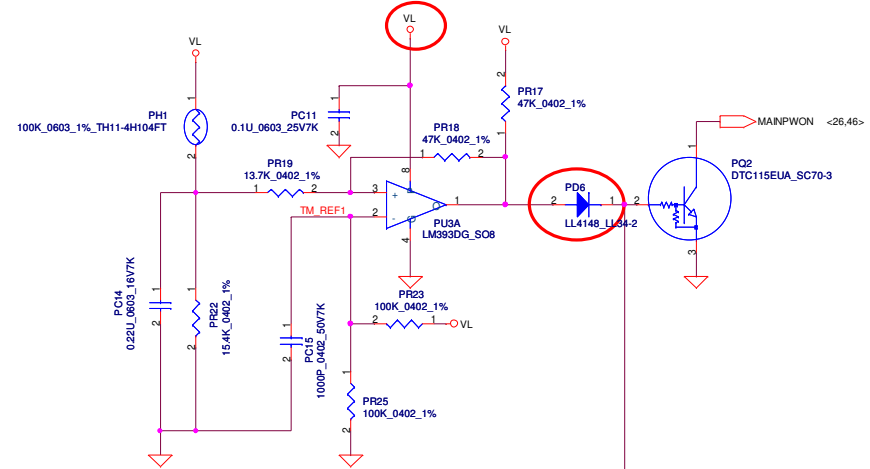
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				Document Number	KALH0/KALG0/KAL90+
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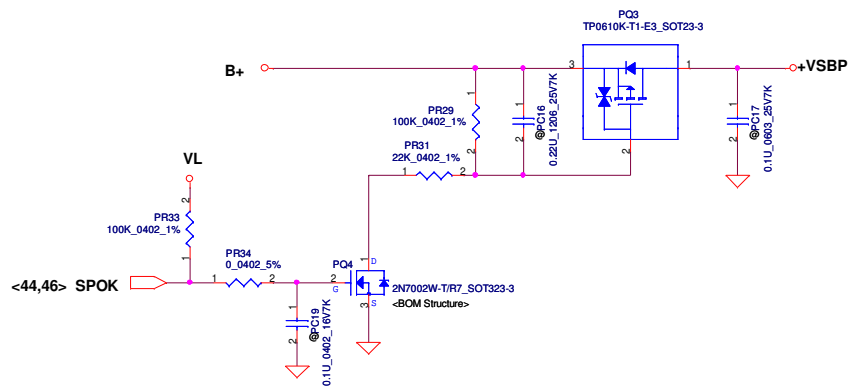
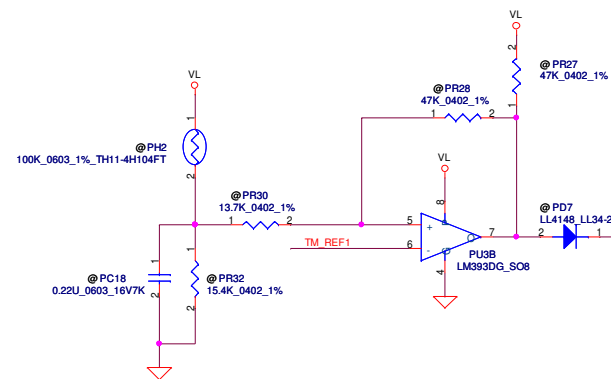
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title
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PH1 under CPU botten side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C

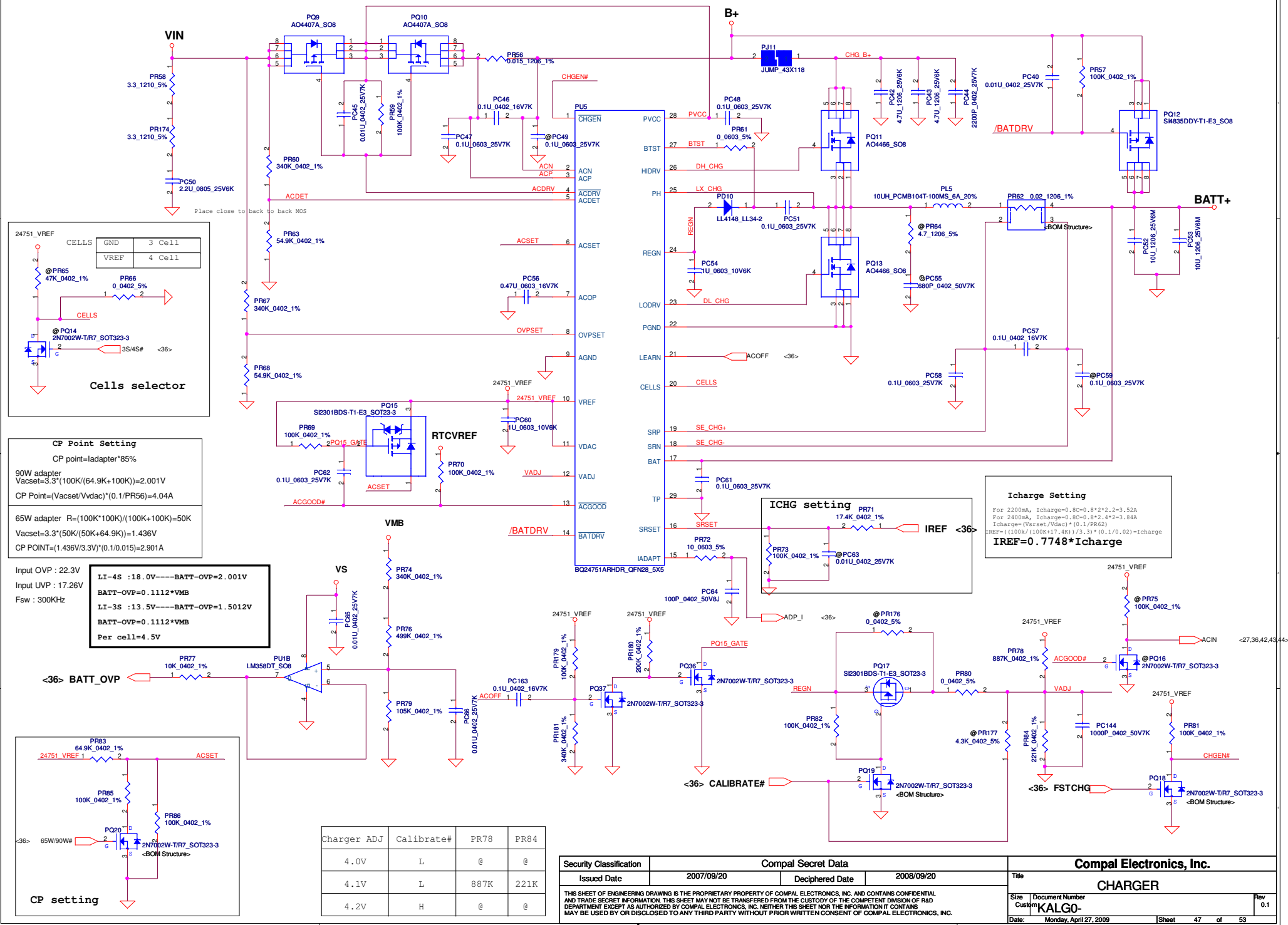


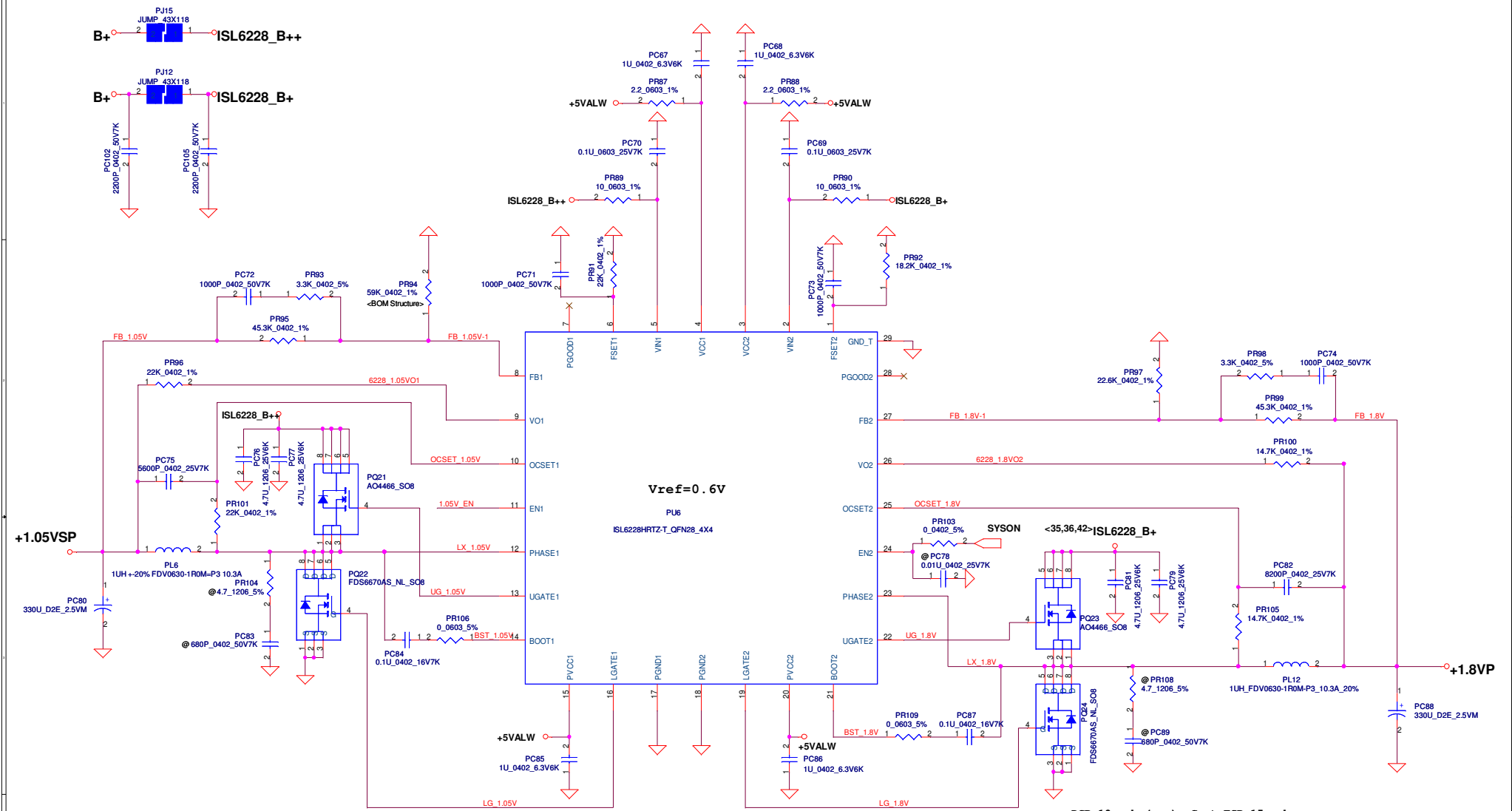
PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



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Size		Document Number		Rev	
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Date		Monday, April 27, 2009		Sheet 45 of 53	

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Issued Date		2007/09/20		Deciphered Date		2008/09/20		Title					
								+5VALWP/+3VALWP					
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						Customer		KALGO-		0.1			
						Date:		Monday, April 27, 2009		Sheet		46 of 53	





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DCR 10m ohm(max)      Cout ESR=15m ohm
1.05VSP ( Ibudget=17.47A)      OCP Setting
Fsw=1/1.5E-10*22k =303K
Vo=Vref*( (PR95+PR94)/PR94)
Ipeak=13.29A, Imax=9.31A
Iocp=13.29*1.2=15.95A
Delta I=4.09A
Iocp*DCR=(Rocset*9.5uA)=(15.95*1.3*10m; Roset=21.8K
now chose Roset=22K
Csen=L/(DCR*Roset)=1uH/(10m*22k); Csen=0.00523uF
now chose Csen=5600pF
Iocp_min=(22K*9.5uA)/(10m ohm*1.3) =16.07A
Iocp_max=(22K*10.5uA)/(10m ohm) =23.1A

```

<36,42> SBPWR_EN

<38,49> VS ON

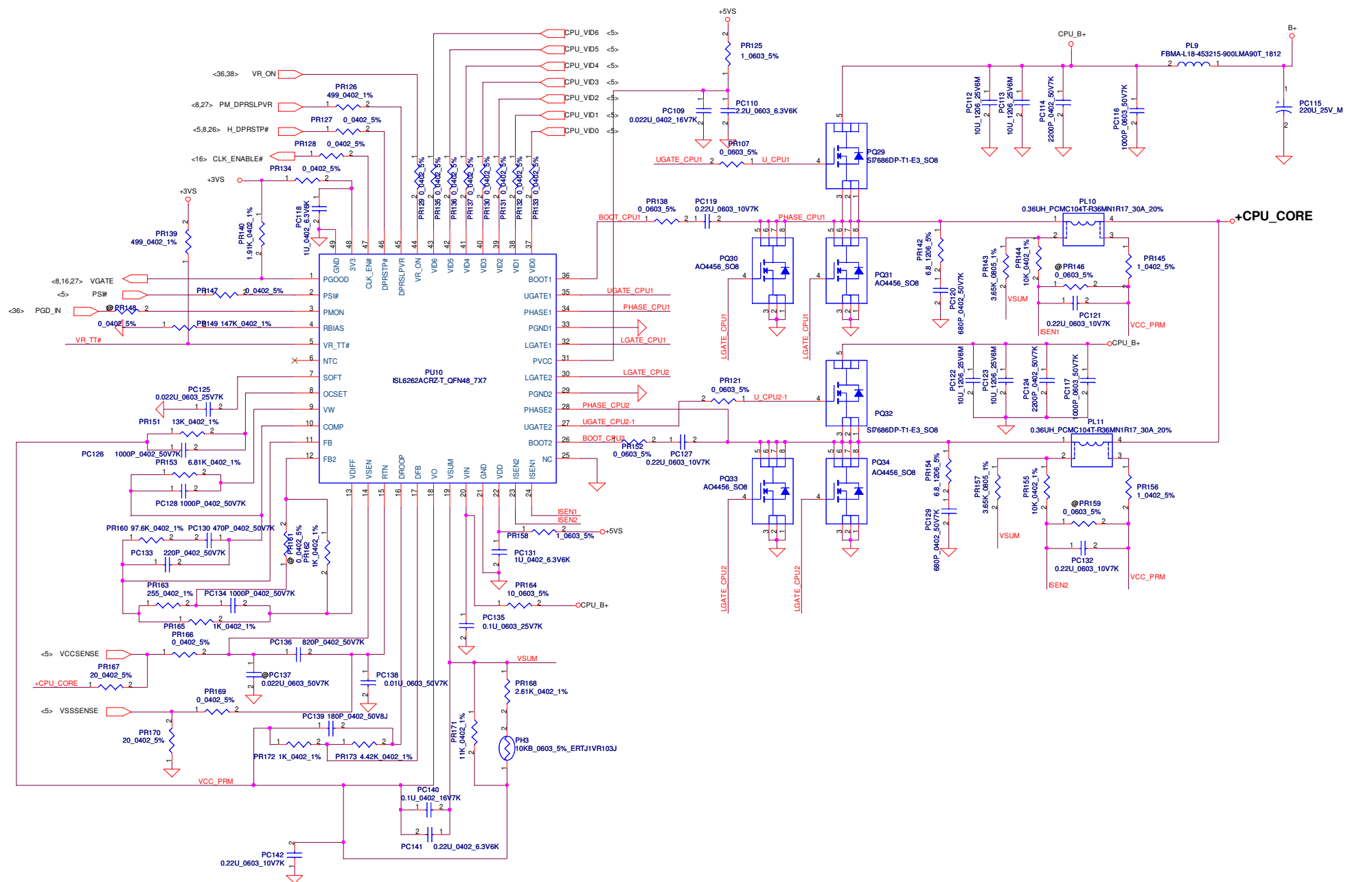
```

DCR 10m ohm(max) Cout ESR=15m ohm
1.8Vp( Ibudget=9.91A ) Ipeak=9A, Imax=6.3 A
Fsw=1/1.5E-10*18.2k =366K
Vo=Vref*( (PR97+PR99)/PR97)
Iocp=9*1.2=10.8A
Iocp*DCR=(Rocset*9.5uA)=10.67*1.3*10m; Rocset=14.78K
now choose Rocset=14.7K
Csen=L/(DCR*Fsw)=1uH/(10m*14.7k); Csen=8.16nF
now choose Csen=8200pF
Iocp_min=(14.7K*9.5uA)/(10m ohm*1.3) =10.74A
Iocp_max=(14.7*10.5uA)/(10m ohm)=15.43A

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				Customer	KALGO-
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				Date: Mondav, April 27, 2009	Sheet 49 of 53 Rev 0.1



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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title
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		M86-M
GPU_VID0	GPU_VID1	Core Voltage Level
0	0	0.9 V
0	1	1.09 V
1	0	1.2V
1	1	1.35 V

Security Classification		Compal Secret Data		Compal Electronics, Inc. VGA CORE/1.IVSP	
Issued Date	2007/12/18	Deciphered Date	2008/12/18		
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				Size Custom	Document Number KALGO-MXM
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PR196 value	VGA OCP	0.3	50	change the resistance value of pr196 from 57.6K to 40.2K	2009/02/06	PVT
2	Change PL14 value	prevent OVP occur	0.3	50	change the inductance value of PL14 from 1uH to 0.56 uH	2009/02/06	PVT
3	Change PU4 IC part number	vender suggestion	0.3	45	change part number to SA00002V400	2009/02/06	PVT
4							
5							
6							

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
				PIR (PWR)	
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B --> C Change List

0220-----
Page 6, Change C98 BOM structure to @

0218-----
Page 20, Add R569 with BOM structure @
Page 23, R34, R38, R40, R53, R54, R55 change BOM structure to @
Page 31, Change R215 to 18K
Update Power Schematics

0213-----
Page 11, Delete R113
Add J1 JUMP_43X79 with BOM structure @
Page 31, R558, R559 0 ohm with BOM structure @
R560, R561 4.7K with BOM structure @
Page 32, R562, R563 0 ohm with BOM Structure @
R564, R565 0 ohm
Page 38, Delete C619
Add R566, R567, R568 0_0603 with BOM Structure JAL90@

0204-----
Page 12, Change L31 to MBK1608301YZF_0603 with BOM structure GM@
Change R163 to 0_0805_5%
Page 23, Change BOM Structure of U5 to @
Page 27, Change BOM Structure of R555 and R550 to @
Page 33, Change R217 to 31.6K_0402_1%
Change C313 to 1U_0603_10V6K
Page 34, Change R503 to FBMA-L10-160808-301LMT_0603

01/31-----
Page 23, Delete U10

01/29-----
Page 23, Change R152 BOM Structure to @

01/24-----
Page 4, Change U8 to SA00001Z700 (EMC1402)
Page 33, Change C338 to SE076104K80
Page 35, Mount C584

01/23-----
Page 38 Delete F3, R558~560, C609~614

01/22-----
Page 11, Delete R79
Change J1 Symbol to JUMP_43X79
Page 33, Add R557 10K (Check)
Change R245 BOM Structure with @
Page 38, Add C609~614, R558~560 (Check)
C607,608, 615~619 (Check)

01/17-----
Page 11, Add R79 0_0805
Update Power Schematics

01/16-----
Page 11, Delete R79 0_0805
Add J1 JUMP_43X79
Page 16, Change C296, R301 to 27P_0402
Page 19, Change L17, L19, L21 BOM structure to GM@
Page 23, Mount U29, R339
Add U10 with BOM structure @ (Co-lay with U5)
Change R340 Bom structure to @
Change U5 to MX25L4005AMC-12G_SO8 (SA00002A900)

Page 27, Change U26, C420 BOM structure to @
Change R550 to 0_0402
Add R555 0_0402
Page 32, Change R269 to 240_0402_5%, R267 to 453_0402_1%
Change R268 pin1 connect to +5VALW
Page 33, Change R217 to 18K_0402_1% with BOM structure PM@
Page 35, Add R551,R552, R553, R554 75_0603_1% with BOM structure JAL90@
Add D32 PJDLC05_SOT23-3
Page 38, Add F3 3A_15VDC_SMD2920P300TF/15
Page 49, Add R551,R552, R553, R554 1K_0603_1% with BOM structure 268@
Add L17, L19, L21 0_0805 with BOM structure PM@
Update U38 (ALC268-VB1-GR) PN:SA00001GD10 for JAW50

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