COMPAL CONFIDENTIAL

MODEL NAME : ZAR00

PCB NO : LA-B541P

BOM P/N : i5 - 4319TQ31L01 (HSW)
i7 - 4319TQ31L02 (HSW)

GPIO MAP: GPIO map rev 3.6C

Delray 17

Broadwell H-type (2 chip)

REV : 0.1 (X00)

2014.01.13

@ : Nopop Component

EMC@ : EMI/ESD/RF part

CONN@ : Connector Component

PXDP@,CXDP@ : Total debug Component (pop them until ST)

TB@ : Thunderbolt function

BDW@ : HSW_BDW compatibility circuit

Layout Dell logo

REV: X00
PWB: XXXXX
DATE: 1403-06

PCB_178_LA-B541P_REV0_MB

Part Number	Description
DAA0008R000	PCB 178 LA-B541P REV0 MB

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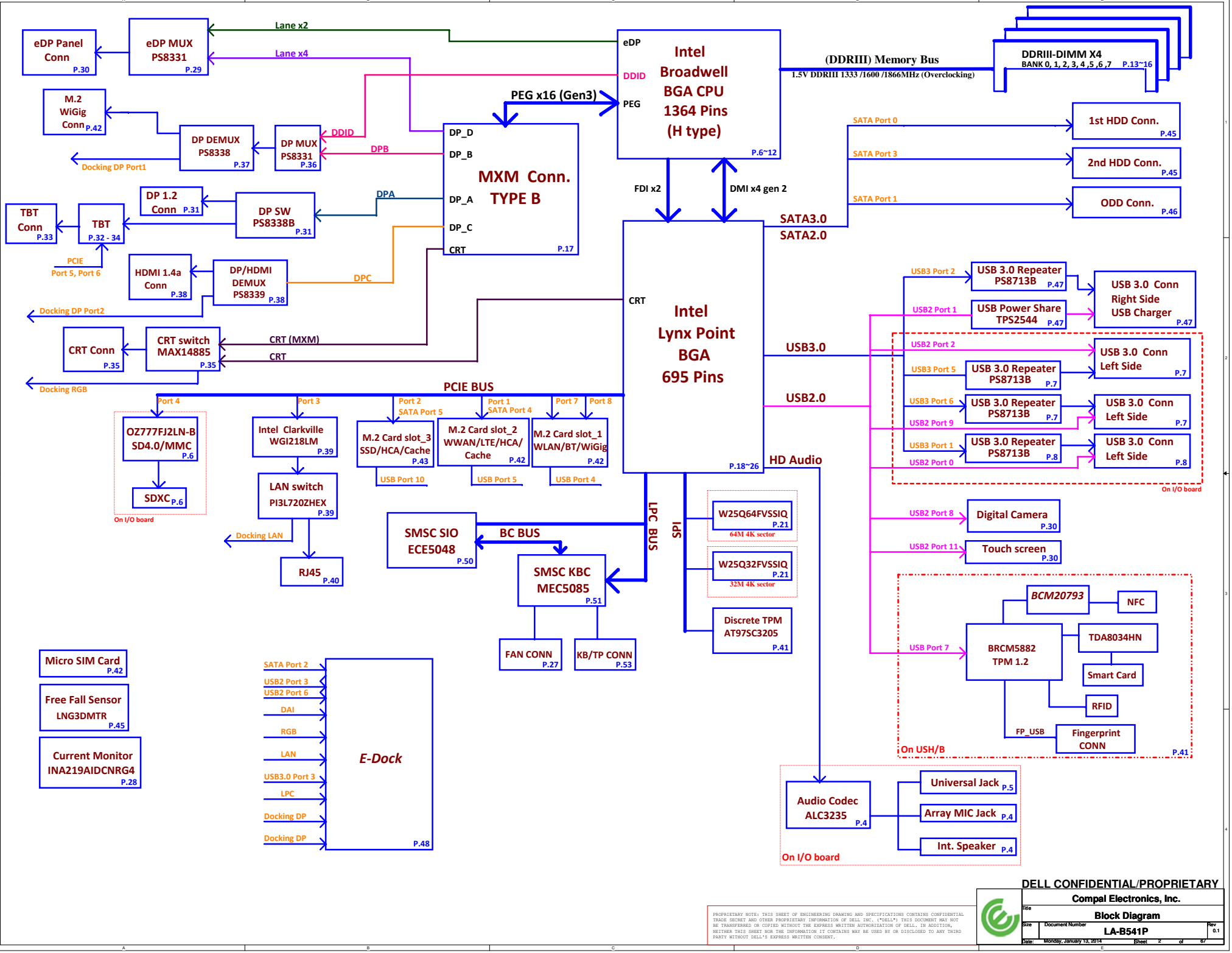
Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-B541P | Rev: 0.1

Date: Monday, January 13, 2014 Sheet 1 of 67

Power CKT: 0108



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Title: Block Diagram

Size: | Document Number: LA-B541P | Rev: 0.1

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POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +VCC_CORE +1.05V_RUN +3.3V_MXM +5V_MXM +MXM_PWR_SRC	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top		Copper foil	0.5oz
		3.7	Prepreg	1080
2	GND1		Copper foil	1oz
		3.7	Core	4mil
3	Sig 1		Copper foil	1oz
		3.9	Prepreg	1080H+2116H
4	GND/PWR		Copper foil	2oz
		3.7	Core	4mil
5	Sig 2		Copper foil	1oz
		3.8	Prepreg	1080Hx2
6	Sig 3		Copper foil	1oz
		3.7	Core	4mil
7	GND/PWR		Copper foil	2oz
		3.9	Prepreg	1080H+2116H
8	Sig 4		Copper foil	1oz
		3.7	Core	4mil
9	GND 3		Copper foil	1oz
		3.7	Prepreg	1080
10	Bottom		Copper foil	0.5oz
			Add Plating	
			SolderMask	
Overall Thickness (1.45mm ± 10%)			57.09	

SATA	DESTINATION
SATA 0	HDD 1
SATA 1	ODD
SATA 2	Dock
SATA 3	HDD 2
SATA 4	M.2 Slot-2
SATA 5	M.2 Slot-3

USB3.0	DESTINATION
Port 1	IO Board- JUSB3
Port 2	JUSB1 (Ext Right Side)
Port 3	Docking
Port 4	NA
Port 5	IO Board- JUSB1
Port 6	IO Board- JUSB2

	USB PORT#	DESTINATION
PCH	0	IO Board- JUSB3 (Ext Left Side)
	1	JUSB1 (Ext Right Side)
	2	IO Board- JUSB1 (Ext Left Side)
	3	Docking USB3.0
	4	M.2 Slot-1 (WLAN/BT/WiGig)
	5	M.2 Slot-2 (WWAN/LTE/HCA)
	6	Docking USB 2.0
	7	USH
	8	Camera
	9	IO Board- JUSB2 (Ext Left Side)
	10	M.2 Slot-3 (SSD/HCA/Cache)
	11	Touch Screen
	12	NA
	13	NA

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	M.2 Slot-2 (WWAN/LTE/HCA)
Lane 2	M.2 Slot-3 (SSD/HCA/Cache)
Lane 3	10/100/1G LOM
Lane 4	MMI(Card reader)
Lane 5	TBT-1
Lane 6	TBT-2
Lane 7	M.2 Slot-1 (WLAN/BT/WiGig)
Lane 8	M.2 Slot-1 (WLAN/BT/WiGig)

Compal Electronics, Inc.
Title: Index and Config.
Size: Document Number: LA-B541P
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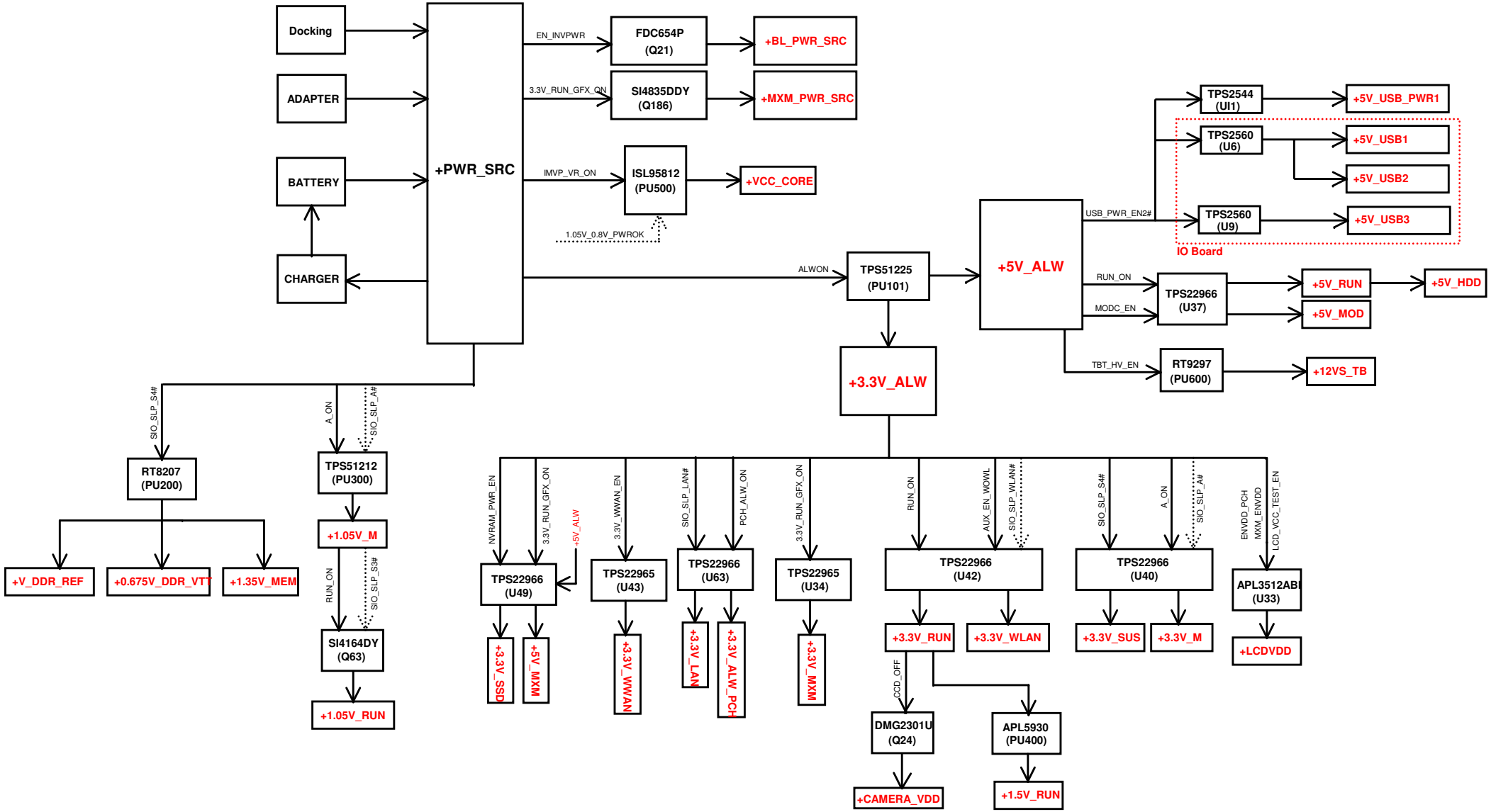

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Title: Power Rail

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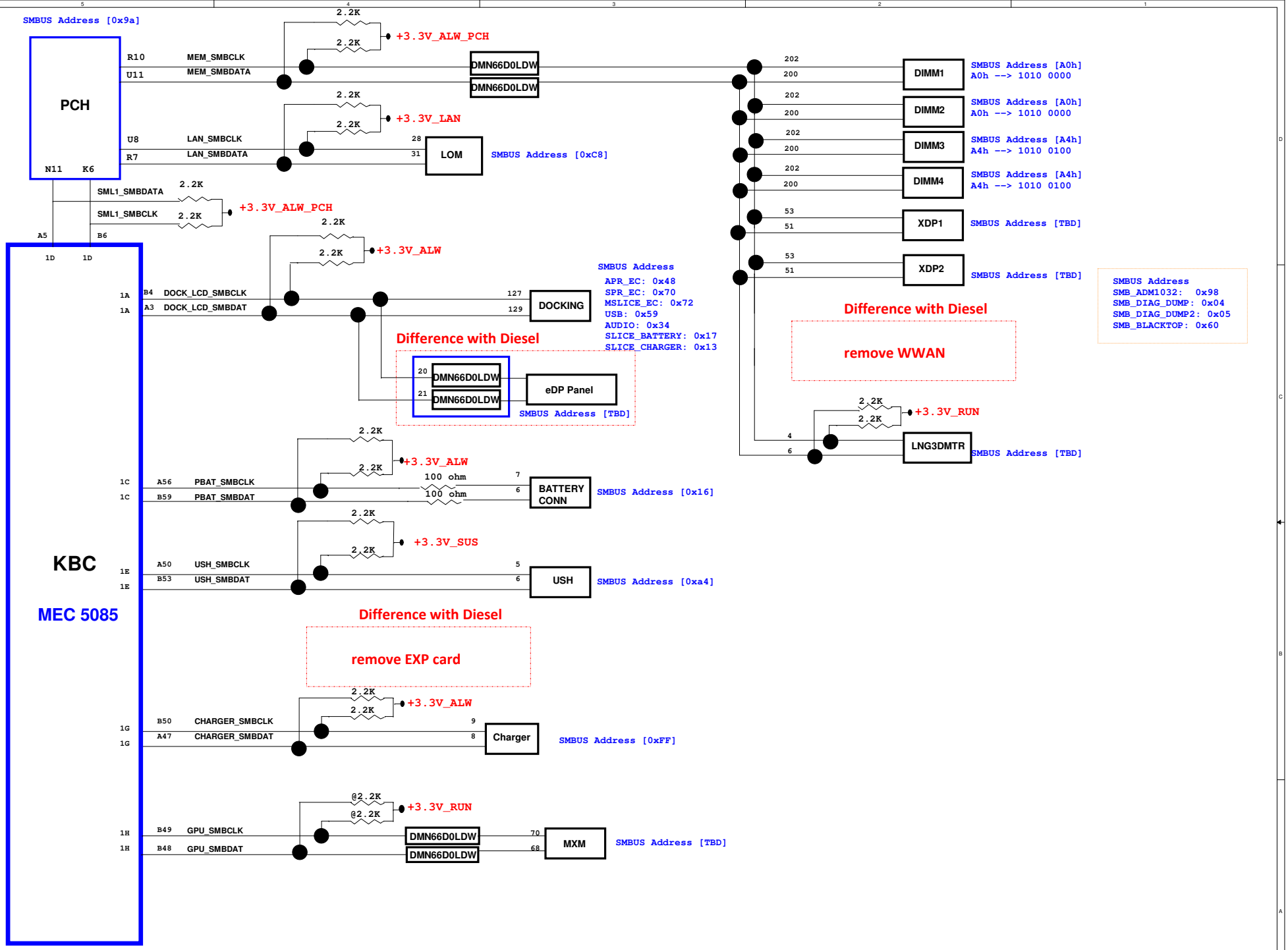

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Title: SMBUS Bolck Diagram

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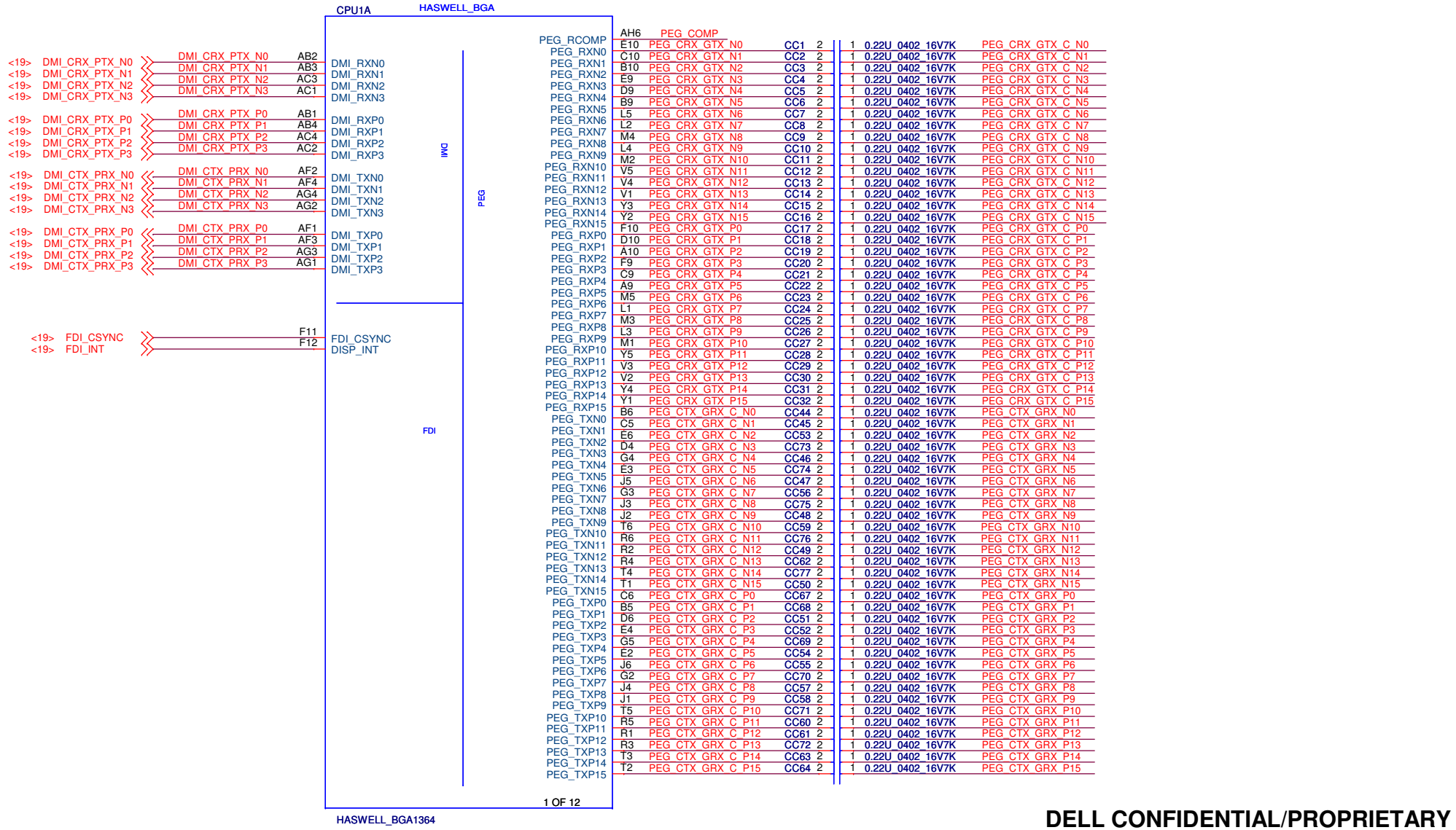

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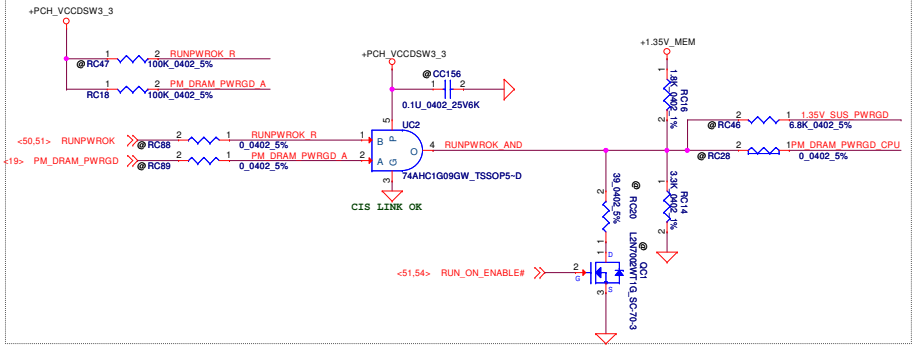
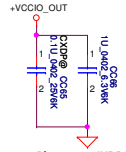
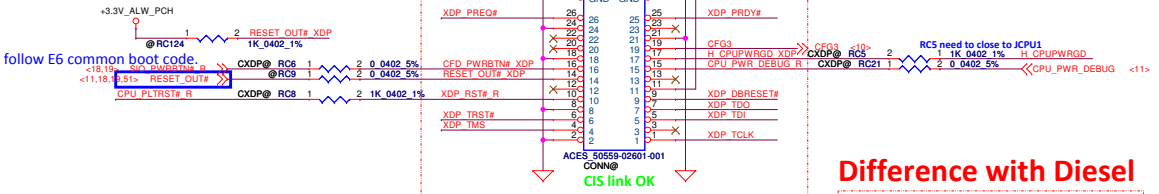
SM_DRAMPWROK with DDR Power Gating Topology

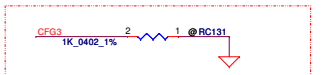


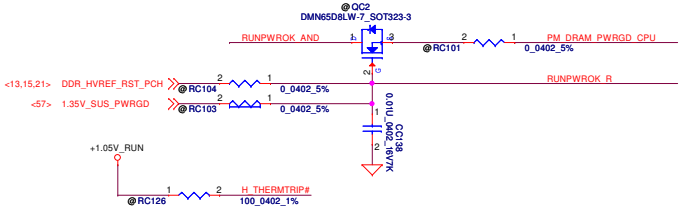
Difference with Diesel



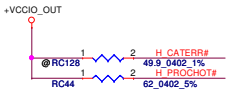


Difference with Diesel



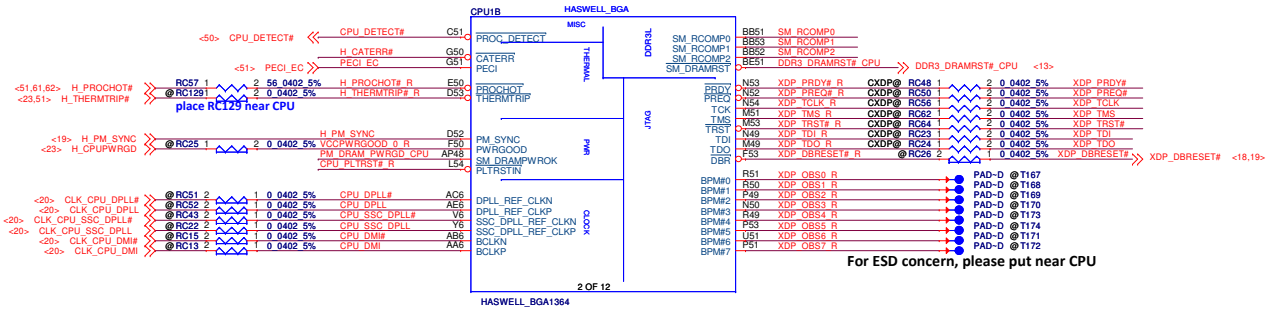


2 chip XDP debug component list - CPU side(CXDP@)			
item	Qty	Part reference	Part description
1	1	CC65	SE00000G880 (S CER CAP 0.1U 25V K X5R 0402)
2	9	RC6,RC21,RC48,RC50,RC56,RC62,RC64,RC23,RC24	SD028000080 (S RES 1/16W 0 +-5% 0402)
3	2	RC8,RC5	SD028100180 (S RES 1/16W 1K +-5% 0402)
4	1	JXDP1	LTCX004MX00(ACES_50559-02601-001_26P-T)



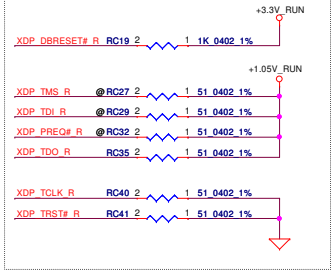
Difference with Diesel

Remove +1.05V_RUN to +VCCST circuit for rPGA usage.

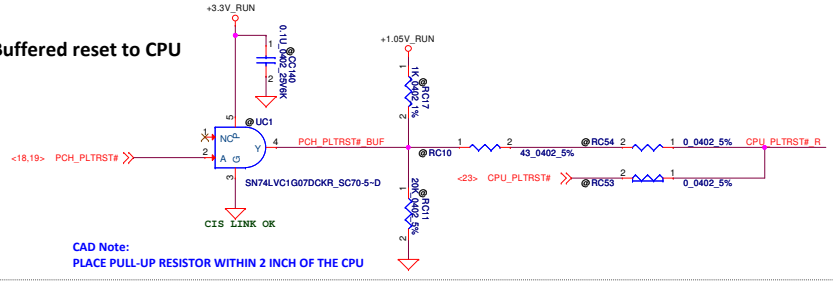


For ESD concern, please put near CPU

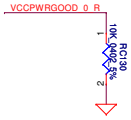
PU/PD for JTAG signals



Buffered reset to CPU

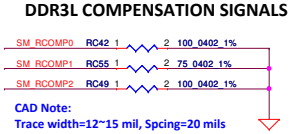


CAD Note:
PLACE PULL-UP RESISTOR WITHIN 2 INCH OF THE CPU



CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC25 & RC130

DDR3L COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

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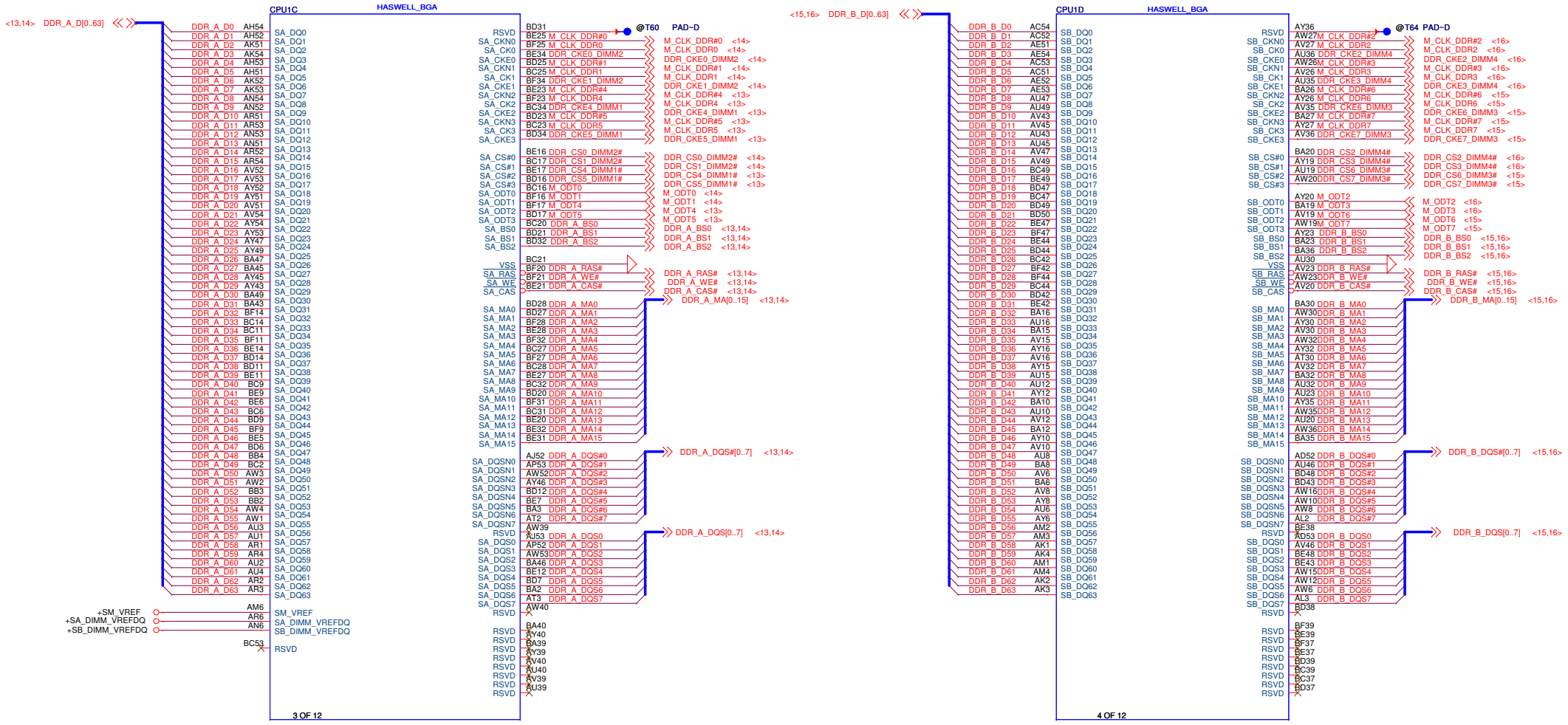

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Title: Broadwell (3/7)

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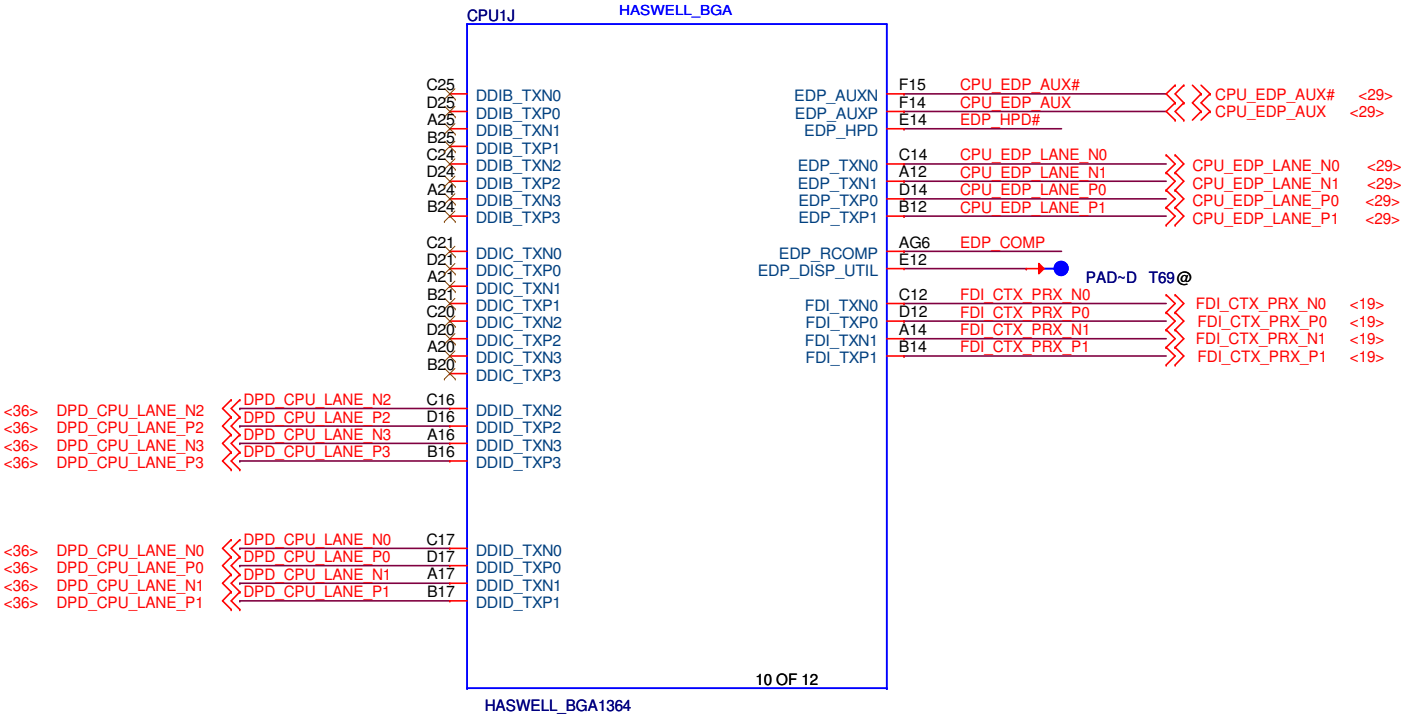
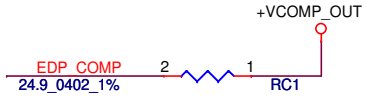
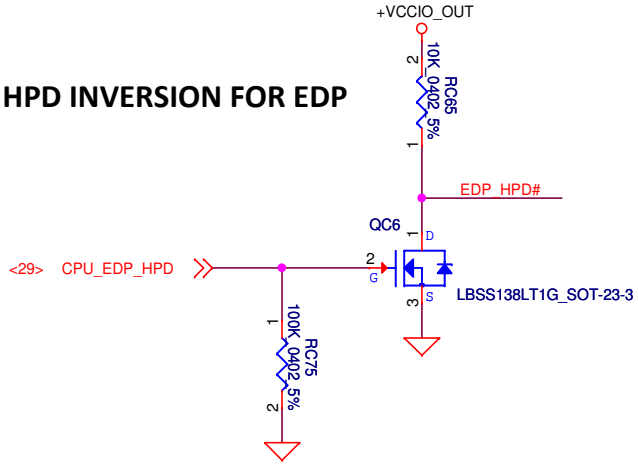


COMPENSATION PU FOR eDP



CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

HPD INVERSION FOR EDP



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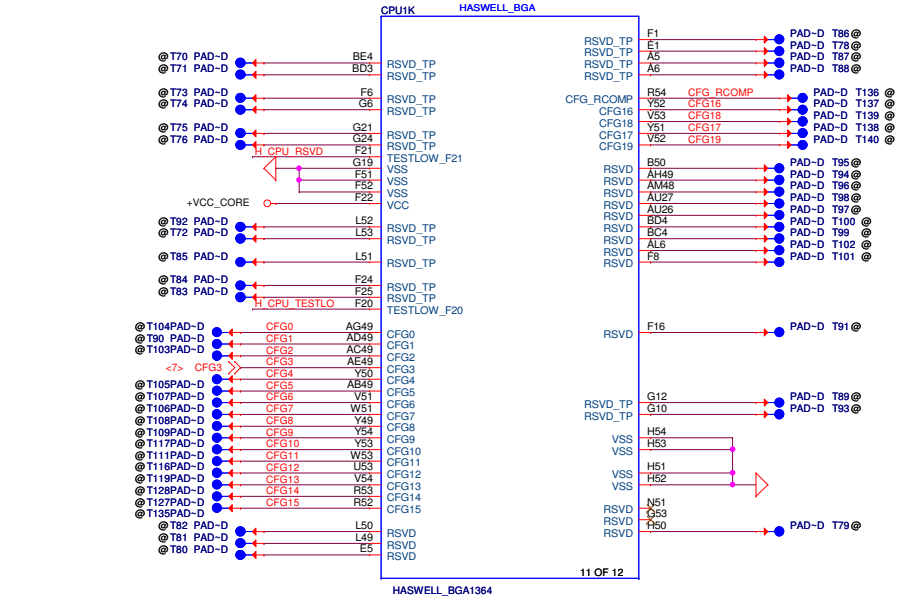
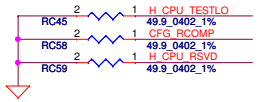
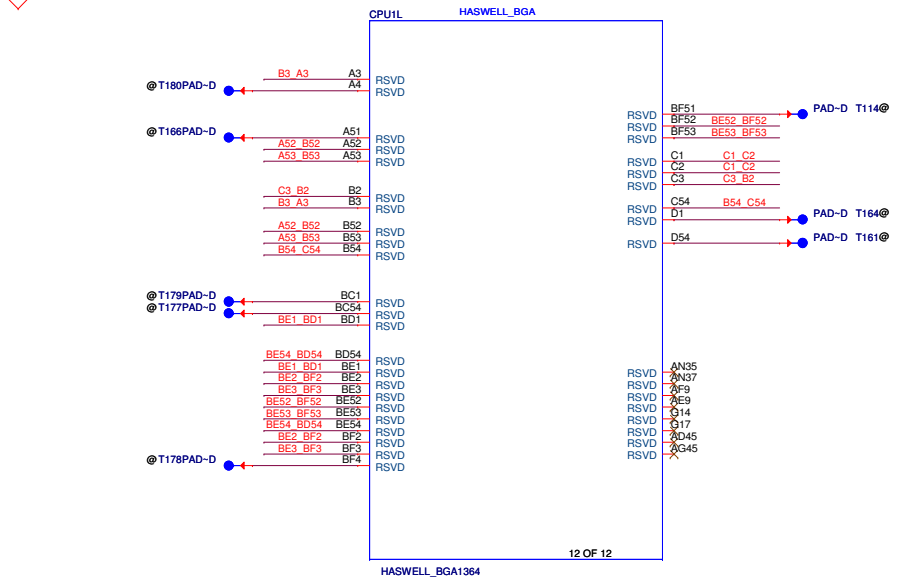
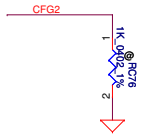


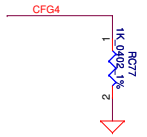




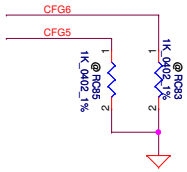
CFG STRAPS for CPU



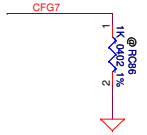
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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SVID ALERT

+VCCIO_OUT

RC60 75_0402_1%

CAD Note: Place the PU resistors close to CPU
RC60 close to CPU 300 - 1500mils

<61> VIDALERT_N — 43_0402_5% — H_CPU_SVIDALRT# RC61

SVID DATA

+VCCIO_OUT

RC63 130_0402_1%

CAD Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils

<61> VIDSOUT — VIDSOUT

VCC_SENSE

+VCC_CORE

RC66 100_0402_1%

CAD Note: RC67 SHOULD BE PLACED CLOSE TO CPU

<61> VCCSENSE — VCCSENSE — @RC67 — VCCSENSE_R 0_0402_5%

CAD Note: RC68 SHOULD BE PLACED CLOSE TO CPU

<61> VSSSENSE — VSSSENSE — @RC68 — VSSSENSE_R 0_0402_5% — VSSSENSE_R <12>

RC70 100_0402_1%

HSW_BDW compatibility CKT

Difference with Diesel (follow HSW-BGA CRB Rev 0.7)

VDDQ DECOUPLING

+1.35V_MEM

10U_0603_6.3V6M-D: @CC161, CC170, CC164, CC168, CC163, CC166, CC171, CC165

330U_D2_2VM_R6M: CC172

10U_0402_6.3V6K-D: @CC85, CC84, @CC88, CC87, @CC43, @CC80, @CC81, @CC82, @CC83, @CC86

+1.05V_RUN

RC69 150_0402_1%

CPU_PWR_DEBUG

RC71 10K_0402_5%

CPU1E — HASWELL_BGA

@T110 PAD-D	J17	RSVD	
@T77 PAD-D	J21	RSVD	
@T112 PAD-D	J26	RSVD	
@T113 PAD-D	J31	RSVD	
+1.35V_MEM	AR29	VDDQ	
	AR31	VDDQ	
	AR33	VDDQ	
	AT13	VDDQ	
	AT19	VDDQ	
	AT23	VDDQ	
	AT27	VDDQ	
	AT32	VDDQ	
	AT36	VDDQ	
	AV37	VDDQ	
	AW22	VDDQ	
	AW25	VDDQ	
	AW29	VDDQ	
	AW33	VDDQ	
	AY18	VDDQ	
	BB21	VDDQ	
	BB22	VDDQ	
	BB26	VDDQ	
	BB27	VDDQ	
	BB30	VDDQ	
	BB31	VDDQ	
	BB34	VDDQ	
	BB36	VDDQ	
	BD22	VDDQ	
	BD26	VDDQ	
	BD30	VDDQ	
	BD33	VDDQ	
	BE18	VDDQ	
	BE22	VDDQ	
	BE26	VDDQ	
	BE30	VDDQ	
	BE33	VDDQ	
@T115 PAD-D	AN31	RSVD	
+VCC_CORE	L6	VCC	
	M6	VCC	
	AN22	RSVD	
@T151 PAD-D	AN18	RSVD	
@T152 PAD-D			
	VCCSENSE_R C50	VCC_SENSE	
@T153 PAD-D	AH9	RSVD	
+VCCIO_OUT	D51	VCCIO_OUT	
+VCCIO2PCH	F17	RSVD	
+VCOMP_OUT	AK8	VCOMP_OUT	
	AN33	RSVD	
@T160 PAD-D	W9	RSVD	
@T159 PAD-D	J12	RSVD	
	AR49	RSVD	
@T154 PAD-D			
	H_CPU_SVIDALRT# J53	VIDALERT	
<61> VIDSCLK	VIDSCLK J52	VIDSCLK	
	VIDSOUT J50	VIDSOUT	
	B51	VSS	
<7> CPU_PWR_DEBUG	CPU_PWR_DEBUG F19	PWR_DEBUG	
	E52	VSS	
	V49	RSVD_TP	
@T157 PAD-D	U49	RSVD_TP	
@T158 PAD-D	IVR_ERROR AM49	RSVD_TP	
@T162 PAD-D	IST_TRIGGER W49	RSVD_TP	
@T163 PAD-D	V50	RSVD_TP	
	AN49	VSS	
	AJ49	VSS	
	AG50	VSS	
	AK49	VSS	
	AJ50	VSS	
	AP49	VSS	
	AB50	VSS	
	AP50	VSS	
	AD50	VSS	
	AM50	VSS	
	VSS		
+VCC_CORE	A36	VCC	
	A38	VCC	
	A39	VCC	
	A42	VCC	
	A43	VCC	
	A45	VCC	
	A46	VCC	
	A48	VCC	
	AA46	VCC	
	AA47	VCC	
	AA8	VCC	
	AA9	VCC	

5 OF 12

HASWELL_BGA1364

Difference with Diesel

+VCC_CORE

	B43	VCC
	B45	VCC
	B46	VCC
	B48	VCC
	C27	VCC
	C28	VCC
	C31	VCC
	C32	VCC
	C34	VCC
	C36	VCC
	C38	VCC
	C39	VCC
	C42	VCC
	C43	VCC
	C45	VCC
	C46	VCC
	C48	VCC
	D27	VCC
	D28	VCC
	D31	VCC
	D32	VCC
	D34	VCC
	D36	VCC
	D38	VCC
	D39	VCC
	D42	VCC
	D43	VCC
	D45	VCC
	D46	VCC
	D48	VCC
	E27	VCC
	E28	VCC
	E31	VCC
	E32	VCC
	E34	VCC
	E36	VCC
	E38	VCC
	E39	VCC
	E42	VCC
	E43	VCC
	E45	VCC
	E46	VCC
	E48	VCC
	F27	VCC
	F28	VCC
	F31	VCC
	F32	VCC
	F34	VCC
	F36	VCC
	F38	VCC
	F39	VCC
	F42	VCC
	F43	VCC
	F45	VCC
	F46	VCC
	F48	VCC
	G27	VCC
	G29	VCC
	G31	VCC
	G32	VCC
	G34	VCC
	G36	VCC
	G38	VCC
	G39	VCC
	G42	VCC
	G43	VCC
	G45	VCC
	G46	VCC
	G48	VCC
	H11	VCC
	H12	VCC
	H13	VCC
	H14	VCC
	H16	VCC
	H17	VCC
	H18	VCC
	H19	VCC
	H20	VCC
	H21	VCC
	H23	VCC
	H24	VCC
	H25	VCC
	H26	VCC
	H27	VCC
	H29	VCC
	D5	FC_D5
FC_D3	D3	FC_D3

HSW_BDW compatibility CKT
+VCCIO2PCH

55A

+VCC_CORE — CPU1F — HASWELL_BGA — +VCC_CORE

	AB45	VCC	H33
	AB46	VCC	H34
	AB8	VCC	H36
	AC46	VCC	H37
	AC47	VCC	H38
	AC8	VCC	H39
	AC9	VCC	H40
	AD46	VCC	H42
	AD8	VCC	H43
	AE46	VCC	H45
	AE47	VCC	H46
	AE8	VCC	H48
	AF8	VCC	H8
	AG46	VCC	H9
	AG8	VCC	J10
	AH46	VCC	J14
	AH47	VCC	J19
	AH8	VCC	J24
	AJ45	VCC	J29
	AJ46	VCC	J33
	AK46	VCC	J36
	AK47	VCC	J37
	AK8	VCC	J38
	AL45	VCC	J39
	AL46	VCC	J40
	AL8	VCC	J42
	AL9	VCC	J43
	AM46	VCC	J45
	AM47	VCC	J46
	AM8	VCC	J48
	AM9	VCC	J8
	AN10	VCC	J9
	AN12	VCC	K38
	AN13	VCC	K40
	AN14	VCC	K43
	AN15	VCC	K44
	AN16	VCC	K45
	AN17	VCC	K46
	AN19	VCC	K48
	AN20	VCC	K8
	AN21	VCC	K9
	AN23	VCC	L37
	AN24	VCC	L38
	AN25	VCC	L39
	AN26	VCC	L40
	AN27	VCC	L42
	AN29	VCC	L43
	AN30	VCC	L44
	AN32	VCC	L46
	AN34	VCC	L47
	AN36	VCC	L8
	AN38	VCC	M37
	AN39	VCC	M38
	AN40	VCC	M39
	AN41	VCC	M40
	AN42	VCC	M42
	AN43	VCC	M43
	AN44	VCC	M44
	AN45	VCC	M45
	AN46	VCC	M46
	AN8	VCC	M8
	AN9	VCC	M9
	AP10	VCC	N37
	AP12	VCC	N38
	AP13	VCC	N39
	AP14	VCC	N40
	AP15	VCC	N42
	AP16	VCC	N43
	AP17	VCC	N44
	AP18	VCC	N46
	AP19	VCC	N47
	AP20	VCC	N8
	AP21	VCC	N9
	AP22	VCC	P45
	AP23	VCC	P46
	AP24	VCC	P8
	AP25	VCC	R46
	AP26	VCC	R47
	AP27	VCC	R8
	AP29	VCC	R9
	AP30	VCC	T45
	AP31	VCC	T46
	AP32	VCC	U46
	AP33	VCC	U47
	AP34	VCC	U8
	AP35	VCC	U9
	AP36	VCC	V45
	AP37	VCC	V46
	AP38	VCC	V8
	AP39	VCC	W46
	AP40	VCC	W47
	AP41	VCC	W8
	AP42	VCC	Y45
	AP43	VCC	Y46
	AP44	VCC	Y8
	AP46	VCC	A27
	AP47	VCC	A28
	AP8	VCC	A31
	AP9	VCC	A32
	AR35	VCC	A34
	AR37	VCC	B27
	AR39	VCC	B28
	AR41	VCC	B31
	AR43	VCC	B32
	AR45	VCC	B34
	AR46	VCC	B36
	H30	VCC	B38
	H31	VCC	B39
	H32	VCC	B42

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HASWELL_BGA1364

	HSW	BDW
RC105	X	V
CC137	X	V
CC173	X	V
RC72	X	V
RC73	X	V

HSW_BDW compatibility CKT

RESET_OUT# — RESET_OUT# <18,19,51,7>

BDW@ RC73 6.04K_0402_1%

FC_D3

BDW@ RC72 2.67K_0402_1%

+1.05V_RUN — +VCCIO_OUT

@RC4 0_0603_5%

RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES

HSW_BDW compatibility CKT

+1.05V_RUN — +VCCIO2PCH

BDW@RC105 0_0603_5%

BDW@CC173 0.1U_0402_10V7K

BDW@CC137 22U_0805_6.3V6M

place CC173 close to CPU

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Broadwell (6/7)

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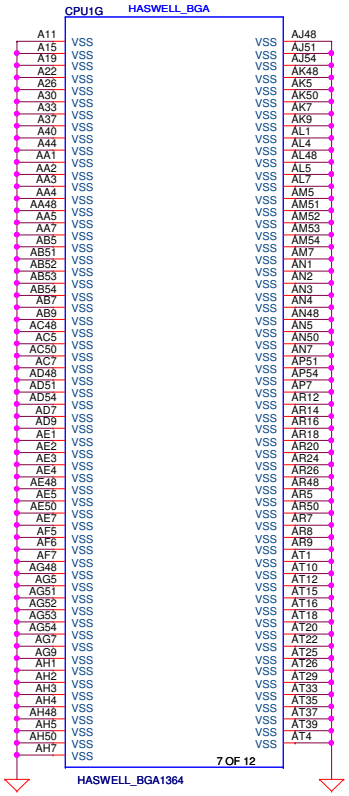

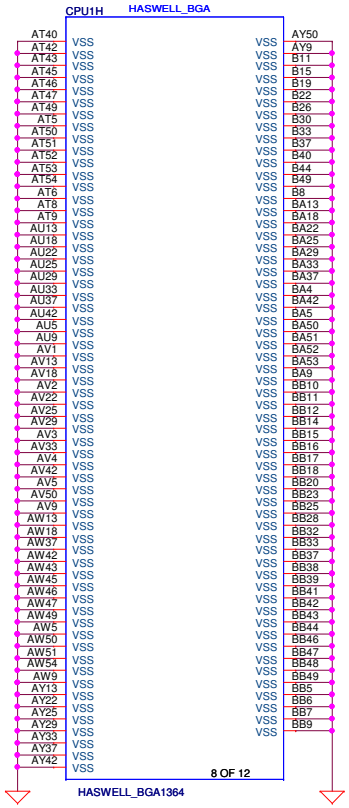

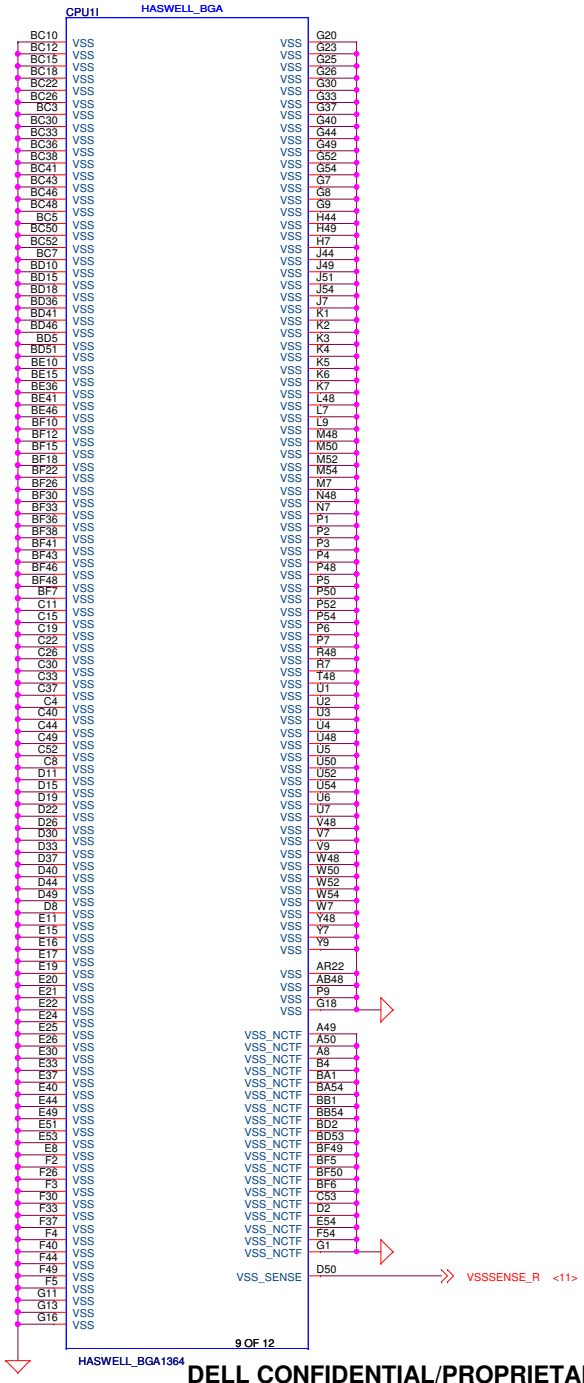

Compal Electronics, Inc.	
Title	Broadwell (7/7)
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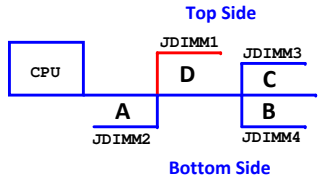
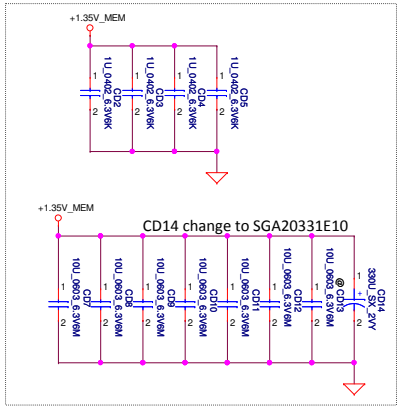
All VREF traces should have 10 mil trace width

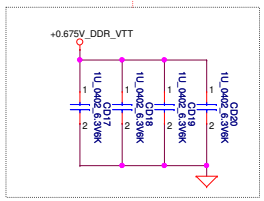
Populate RD1, De-Populate RD2 for Intel DDR3 VREFDQ multiple methods M1
Populate RD2, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

JDIMM1 STD Type H=9.2





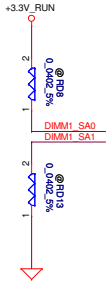
Layout Note:
Place near JDIMM1.203,204

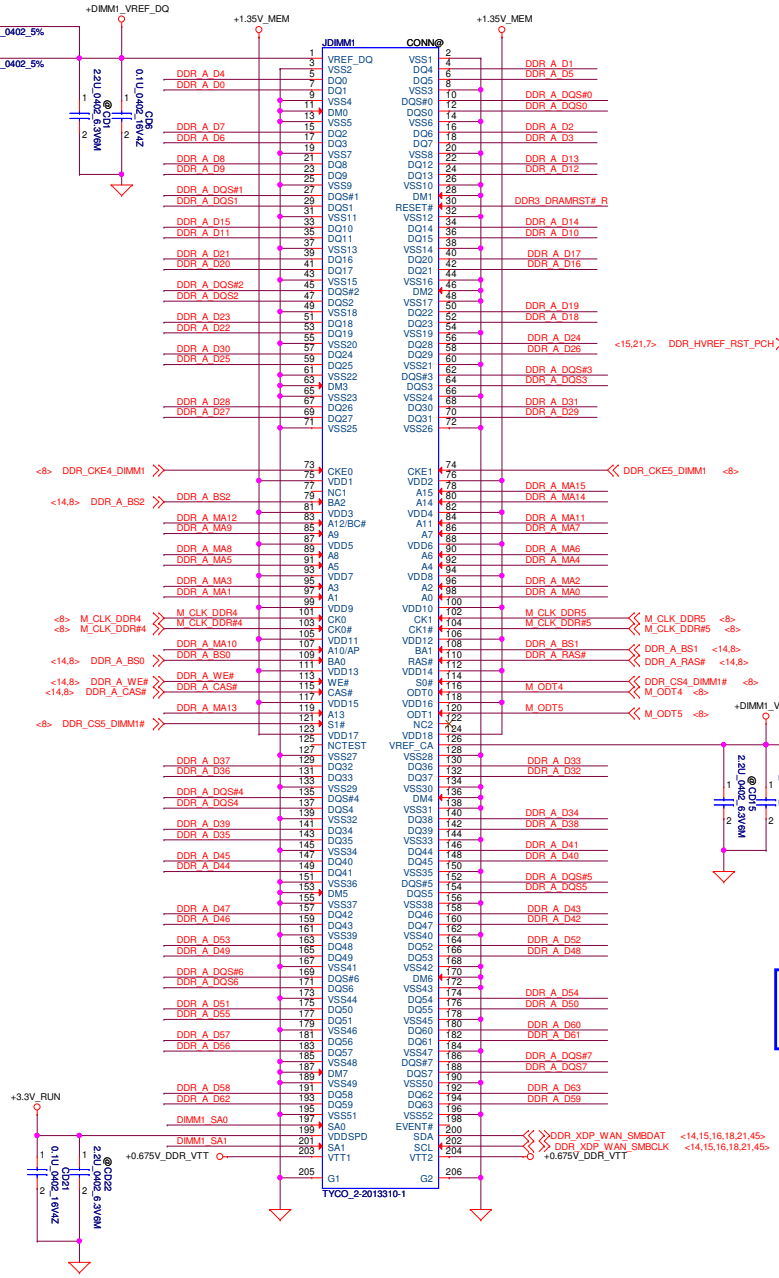


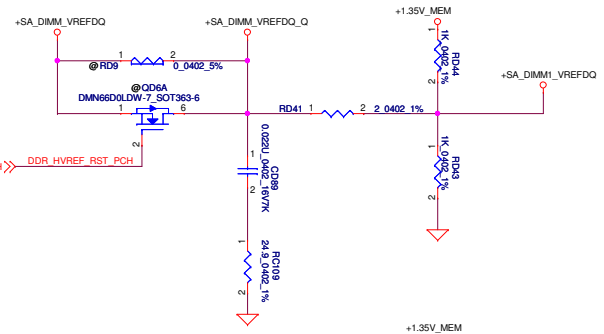
DIMM Select

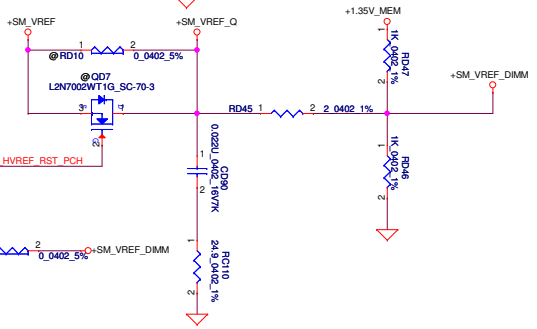
	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1

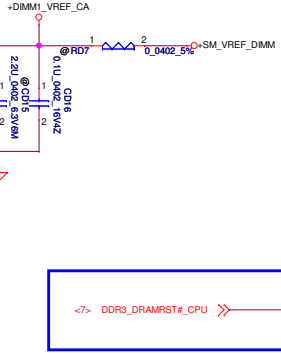
*

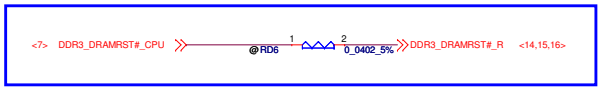












Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

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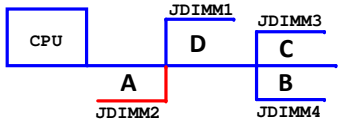
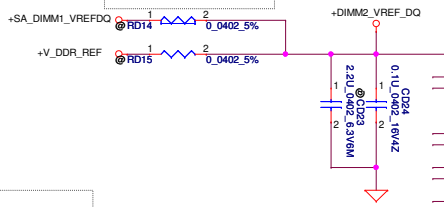
JDIMM2 STD Type H=5.2

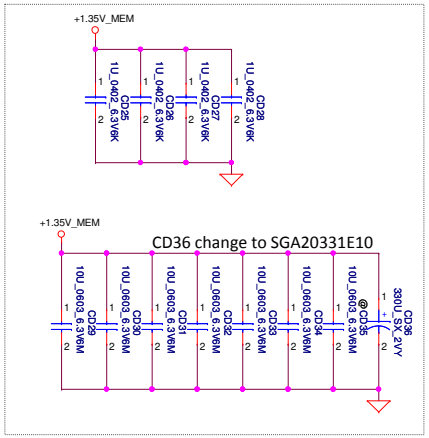
All VREF traces should have 10 mil trace width

Top Side

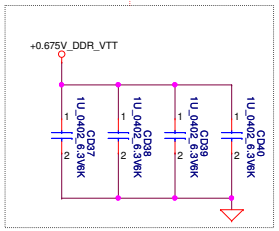


Bottom Side



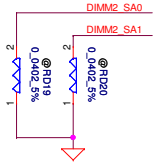


Layout Note:
Place near JDIMM2.Pin 203,204



DIMM Select

*	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1



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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

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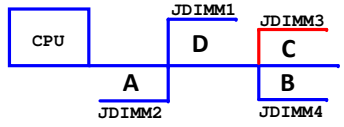
All VREF traces should have 10 mil trace width

JDIMM3 STD Type H=5.2

Top Side



Bottom Side

<16,8> DDR_B_DQS#[0..7]
<16,8> DDR_B_DQS[0..7]
<16,8> DDR_B_D[0..63]
<16,8> DDR_B_MA[0..15]

+SB_DIMM2_VREFDQ — @RD23 0_0402_5%
+V_DDR_REF — @RD24 0_0402_5%
+DIMM3_VREF_DQ — @CD49 2.2U_0402_6.3V6M, CD45 0.1U_0402_16V4Z

+1.35V_MEM — CD50 1U_0402_6.3V6K, CD46 1U_0402_6.3V6K, CD47 1U_0402_6.3V6K, CD48 1U_0402_6.3V6K

+1.35V_MEM — CD51 10U_0603_6.3V6M, CD52 10U_0603_6.3V6M, CD53 10U_0603_6.3V6M, CD54 10U_0603_6.3V6M, CD55 10U_0603_6.3V6M, CD56 10U_0603_6.3V6M, CD57 10U_0603_6.3V6M, CD58 330U_SX_2V_Y

Layout Note:
Place near JDIMM3.Pin 203,204

+0.675V_DDR_VTT — CD59 1U_0402_6.3V6K, CD60 1U_0402_6.3V6K, CD61 1U_0402_6.3V6K, CD62 1U_0402_6.3V6K

DIMM Select

+3.3V_RUN — @RD226 0_0402_5%, @RD227 0_0402_5%
DIMM3_SA1
DIMM3_SA0

	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
* DIMM3	1	1

JDIMM3 CONN@ — TYCO_2-2013289-1~D

+1.35V_MEM — +1.35V_MEM

DDR_B_D0 DDR_B_D4 DDR_B_D7 DDR_B_D3 DDR_B_D8 DDR_B_D9 DDR_B_DQS#1 DDR_B_DQS1 DDR_B_D11 DDR_B_D13 DDR_B_D21 DDR_B_D20 DDR_B_DQS#2 DDR_B_DQS2 DDR_B_D22 DDR_B_D23 DDR_B_D29 DDR_B_D24 DDR_B_D31 DDR_B_D30

<8> DDR_CKE6_DIMM3 — DDR_CKE7_DIMM3 <8>
<16,8> DDR_B_BS2
DDR_B_MA12 DDR_B_MA9 DDR_B_MA8 DDR_B_MA5 DDR_B_MA3 DDR_B_MA1
<8> M_CLK_DDR6 <8> M_CLK_DDR#6 — M_CLK_DDR7 <8> M_CLK_DDR#7 <8>
DDR_B_MA10 DDR_B_BS0
<16,8> DDR_B_BS0 — DDR_B_BS1 <16,8>
<16,8> DDR_B_WE# — DDR_B_RAS# <16,8>
<16,8> DDR_B_CAS# — DDR_CS6_DIMM3# <8>
M_ODT6 <8>
DDR_B_MA13 — M_ODT7 <8>
<8> DDR_CS7_DIMM3#

DDR_B_D37 DDR_B_D33 DDR_B_DQS#4 DDR_B_DQS4 DDR_B_D38 DDR_B_D34 DDR_B_D44 DDR_B_D40 DDR_B_D46 DDR_B_D47 DDR_B_D48 DDR_B_D53 DDR_B_DQS#6 DDR_B_DQS6 DDR_B_D55 DDR_B_D50 DDR_B_D57 DDR_B_D56 DDR_B_D62 DDR_B_D58

DDR_B_D1 DDR_B_D5 DDR_B_DQS#0 DDR_B_DQS0 DDR_B_D2 DDR_B_D6 DDR_B_D14 DDR_B_D15 DDR3_DRAMRST#_R — DDR3_DRAMRST#_R <13,14,16> DDR_B_D10 DDR_B_D12 DDR_B_D17 DDR_B_D16 DDR_B_D19 DDR_B_D18 DDR_B_D26 DDR_B_D25 DDR_B_DQS#3 DDR_B_DQS3 DDR_B_D27 DDR_B_D26 DDR_HVREF_RST_PCH — <13,21,7> DDR_HVREF_RST_PCH

DDR_B_D36 DDR_B_D32 DDR_B_D35 DDR_B_D39 DDR_B_D41 DDR_B_D45 DDR_B_DQS#5 DDR_B_DQS5 DDR_B_D43 DDR_B_D42 DDR_B_D52 DDR_B_D49 DDR_B_D51 DDR_B_D54 DDR_B_D60 DDR_B_D61 DDR_B_DQS#7 DDR_B_DQS7 DDR_B_D63 DDR_B_D59

DIMM3_SA0 DIMM3_SA1

DDR_XDP_WAN_SMBDAT <13,14,16,18,21,45>
DDR_XDP_WAN_SMBCLK <13,14,16,18,21,45>

+0.675V_DDR_VTT — +0.675V_DDR_VTT

+3.3V_RUN — CD63 0.1U_0402_16V4Z, CD64 2.2U_0402_6.3V6M

+SB_DIMM_VREFDQ — @RD11 0_0402_5%
+SB_DIMM_VREFDQ_Q — @QD6B DMN66D0LDW-7_SOT363-6 — RD48 2_0402_1% — CD91 0.022U_0402_16V7K, RC111 24.9_0402_1%
+1.35V_MEM — RD50 1K_0402_1%, RD49 1K_0402_1%
+SB_DIMM2_VREFDQ

+DIMM3_VREF_CA — @RD25 0_0402_5% — +SM_VREF_DIMM — @CD83 2.2U_0402_6.3V6M, CD84 0.1U_0402_16V4Z

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT3

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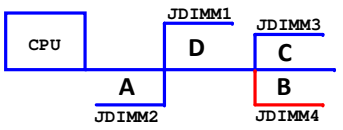
JDIMM4 REV Type H=5.2

All VREF traces should have 10 mil trace width

Top Side



Bottom Side

Layout Note:
Place near JDIMM4.Pin 203,204

DIMM Select

	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1

*

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT4

Size: | Document Number: LA-B541P | Rev: 0.1

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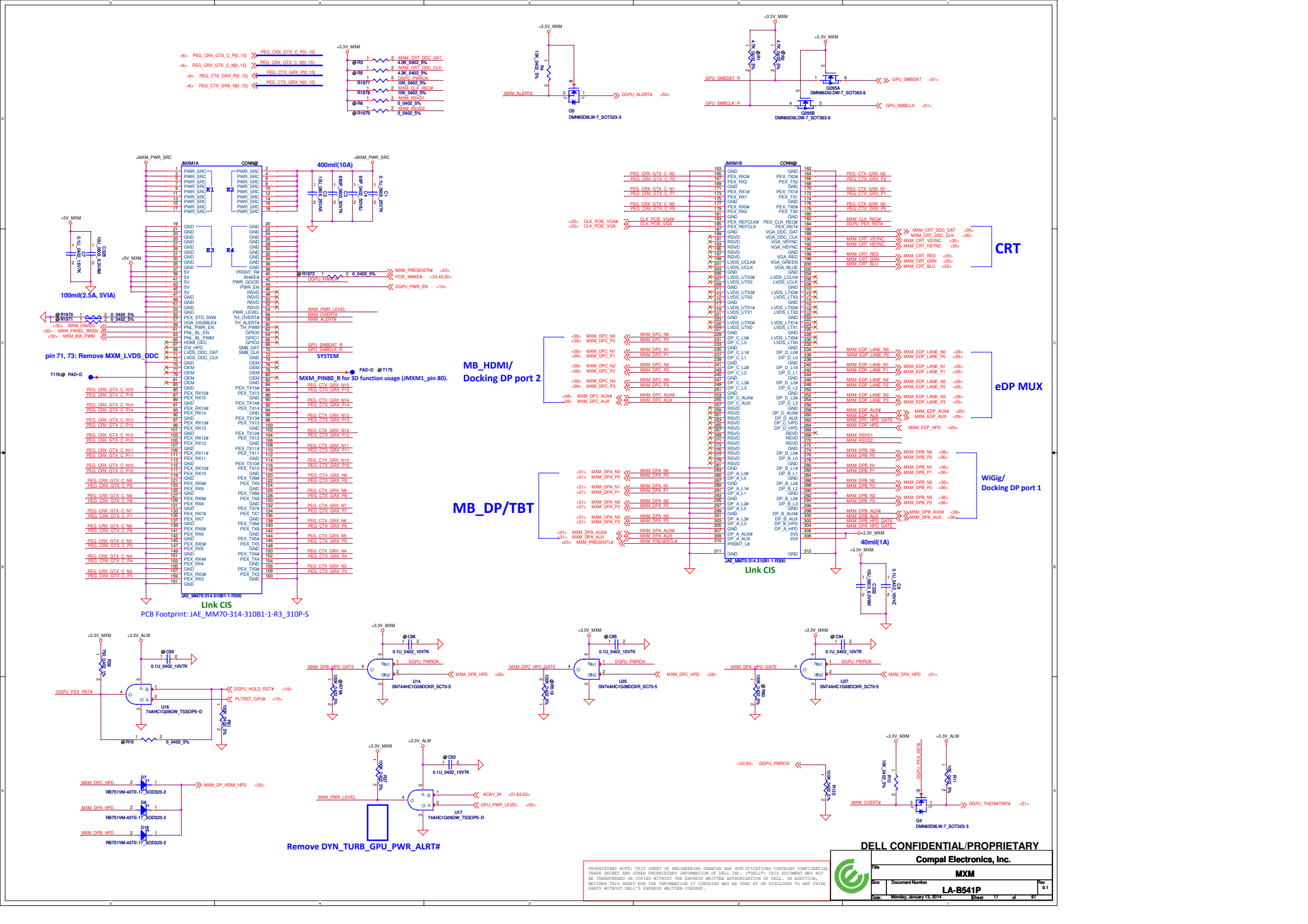
JMXM1A
JMXM1B
CONN@
JAE_MM70-314-310B1-1-R300
400mil(10A)
100mil(2.5A, 5VIA)
40mil(1A)
CRT
eDP MUX
WiGig/
Docking DP port 1
MB_HDMI/
Docking DP port 2
MB_DP/TBT
SYSTEM
LInk CIS
pin 71, 73: Remove MXM_LVDS_DDC
MXM_PIN80_R for 3D function usage (JMXM1_pin 80).
PCB Footprint: JAE_MM70-314-310B1-1-R3_310P-S
Remove DYN_TURB_GPU_PWR_ALRT#
Q5
DMN65D8LW-7_SOT323-3
Q295A
DMN66D0LDW-7_SOT363-6
Q295B
DMN66D0LDW-7_SOT363-6
Q4
DMN65D8LW-7_SOT323-3
U14
SN74AHC1G08DCKR_SC70-5
U25
SN74AHC1G08DCKR_SC70-5
U27
SN74AHC1G08DCKR_SC70-5
U16
74AHC1G09GW_TSSOP5-D
U17
74AHC1G09GW_TSSOP5-D
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
MXM
LA-B541P
Monday, January 13, 2014

PCH XDP

2 chip XDP debug component list - PCH side(PXDP@)			
item	Qty	Part reference	Part description
1	1	CH2	SE00000G880 (S CER CAP 0.1U 25V K X5R 0402)
2	21	RH3,RH4,RH6,RH7,RH8,RH9,RH10,RH11,RH12, RH13,RH14,RH16,RH17,RH19,RH20,RH22,RH24, RH25,RH28,RH30,RH31	SD028000080 (S RES 1/16W 0 +-5% 0402)
3	2	RH26,RH27	SD028100180 (S RES 1/16W 1K +-5% 0402)
4	1	JXDP2	SP02000L900 (S W-CONN SAMTEC BSH-030-01-L-D-A-TR 60P)

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

ME_FWP PCH has internal 20K PD. (suspend power rail)

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short

ME_FWP PCH has internal 20K PD. (suspend power rail)

HDA for Codec

Change PN from SA00005NE2L to SA00006P30L

CMOS place near DIMM

SATA Impedance Compensation

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

Compal Electronics, Inc.
Title: PCH (1/9)
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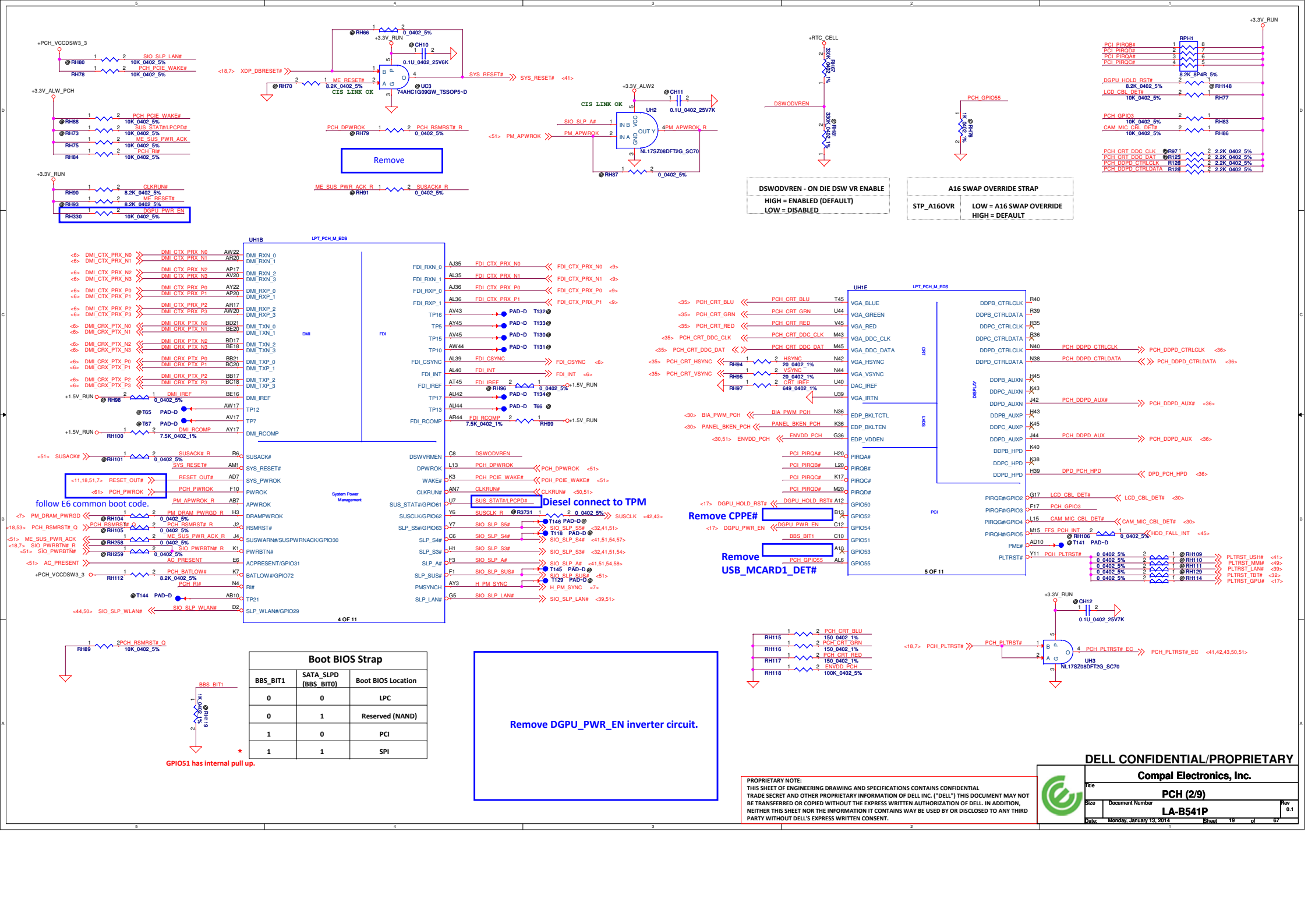
+PCH_VCCDSW3_3
SIO_SLP_LAN#
PCH_PCIE_WAKE#
+3.3V_ALW_PCH
PCH_PCIE_WAKE#
SUS_STAT#/LPCPD#
ME_SUS_PWR_ACK
PCH_RI#
+3.3V_RUN
CLKRUN#
ME_RESET#
DGPU_PWR_EN
XDP_DBRESET#
ME_RESET#
CIS LINK OK
SYS_RESET#
PCH_DPWROK
PCH_RSMRST# R
ME_SUS_PWR_ACK_R
SUSACK# R
Remove
+RTC_CELL
DSWODVREN
PCH_GPIO55
PM_APWROK
SIO_SLP_A#
PCI_PIRQB#
PCI_PIRQD#
PCI_PIRQA#
PCI_PIRQC#
DGPU_HOLD_RST#
LCD_CBL_DET#
PCH_GPIO3
CAM_MIC_CBL_DET#
PCH_CRT_DDC_CLK
PCH_CRT_DDC_DAT
PCH_DDPD_CTRLCLK
PCH_DDPD_CTRLDATA
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED
A16 SWAP OVERRIDE STRAP
STP_A16OVR
LOW = A16 SWAP OVERRIDE
HIGH = DEFAULT
UH1B
LPT_PCH_M_EDS
DMI
FDI
System Power Management
4 OF 11
follow E6 common boot code.
Diesel connect to TPM
Remove CPPE#
Remove USB_MCARD1_DET#
UH1E
VGA
LVDS
DISPLAY
PCI
5 OF 11
Remove DGPU_PWR_EN inverter circuit.
GPIO51 has internal pull up.
Boot BIOS Strap
BBS_BIT1
SATA_SLPD (BBS_BIT0)
Boot BIOS Location
0 0 LPC
0 1 Reserved (NAND)
1 0 PCI
1 1 SPI
UH3
NL17SZ08DFT2G_SC70
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Title
PCH (2/9)
Size
Document Number
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Rev
0.1
Date: Monday, January 13, 2014
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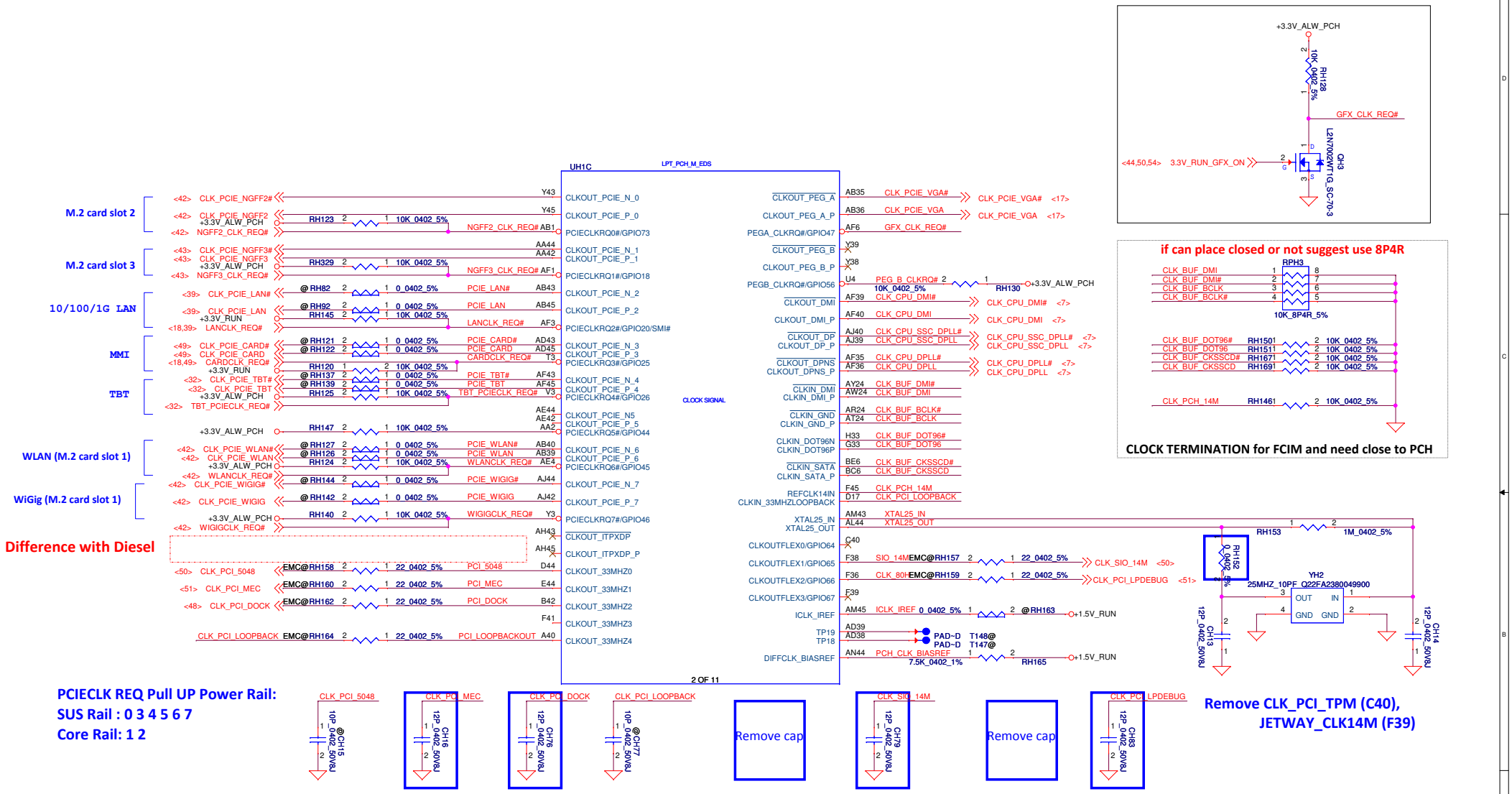

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Title: PCH (3/9)

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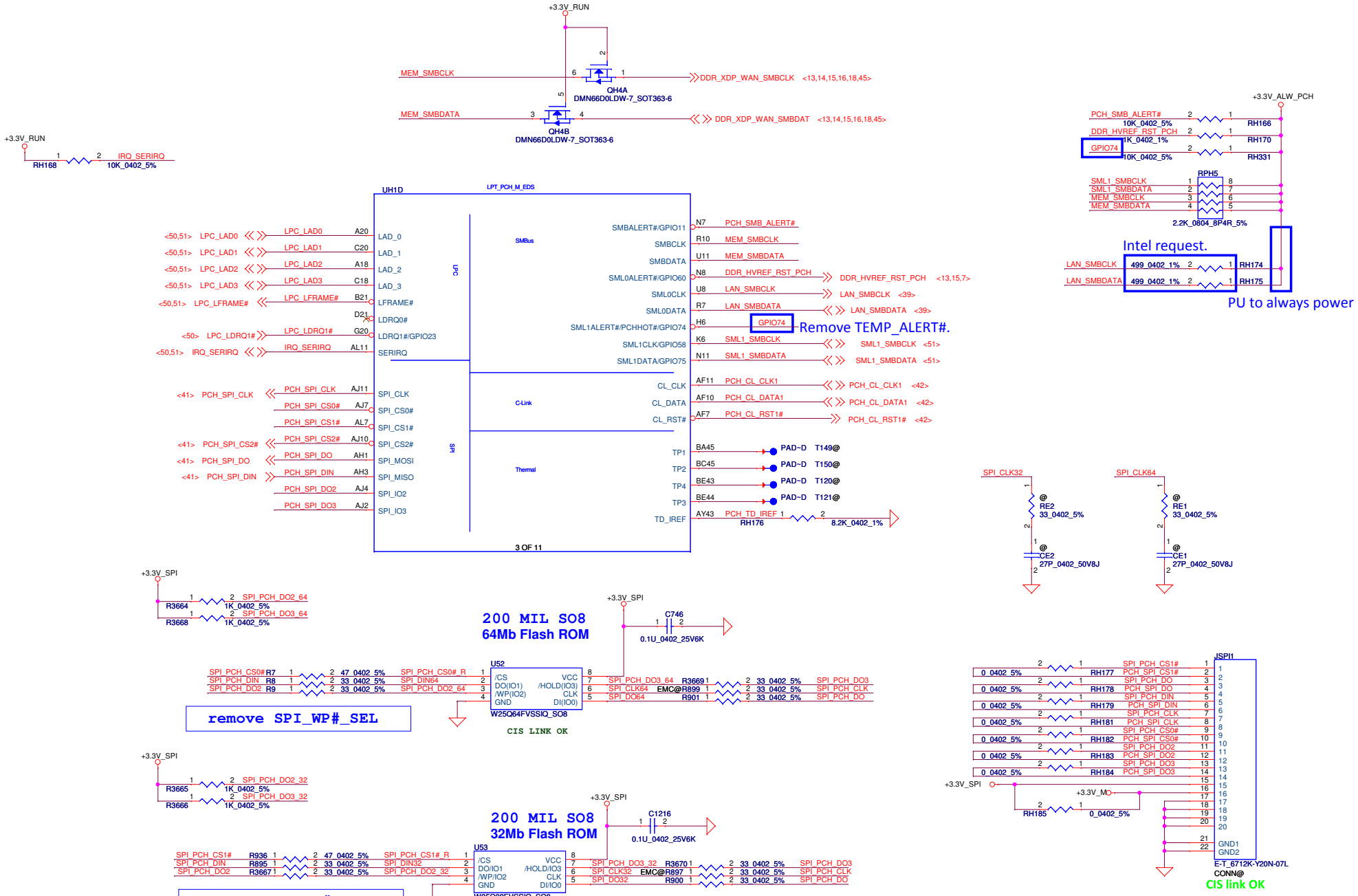

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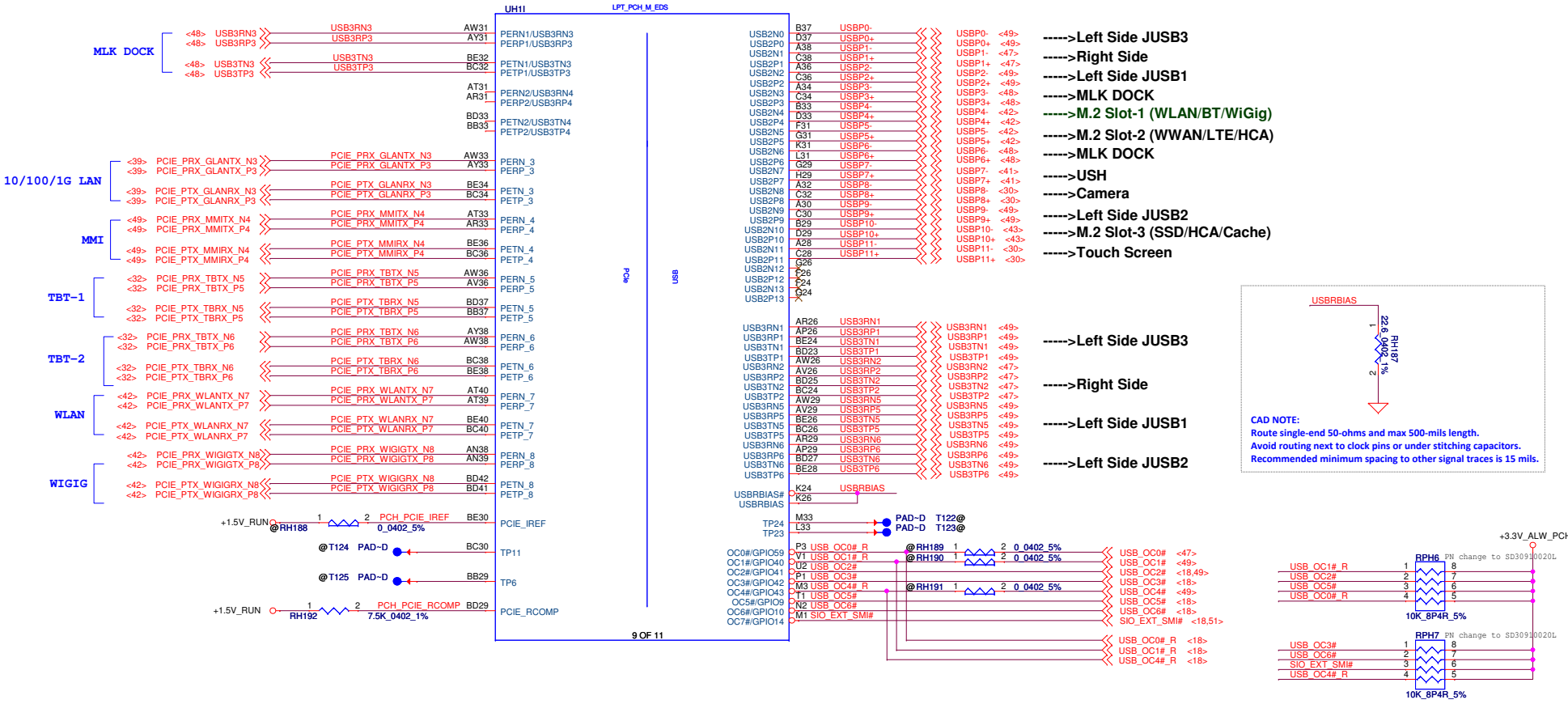

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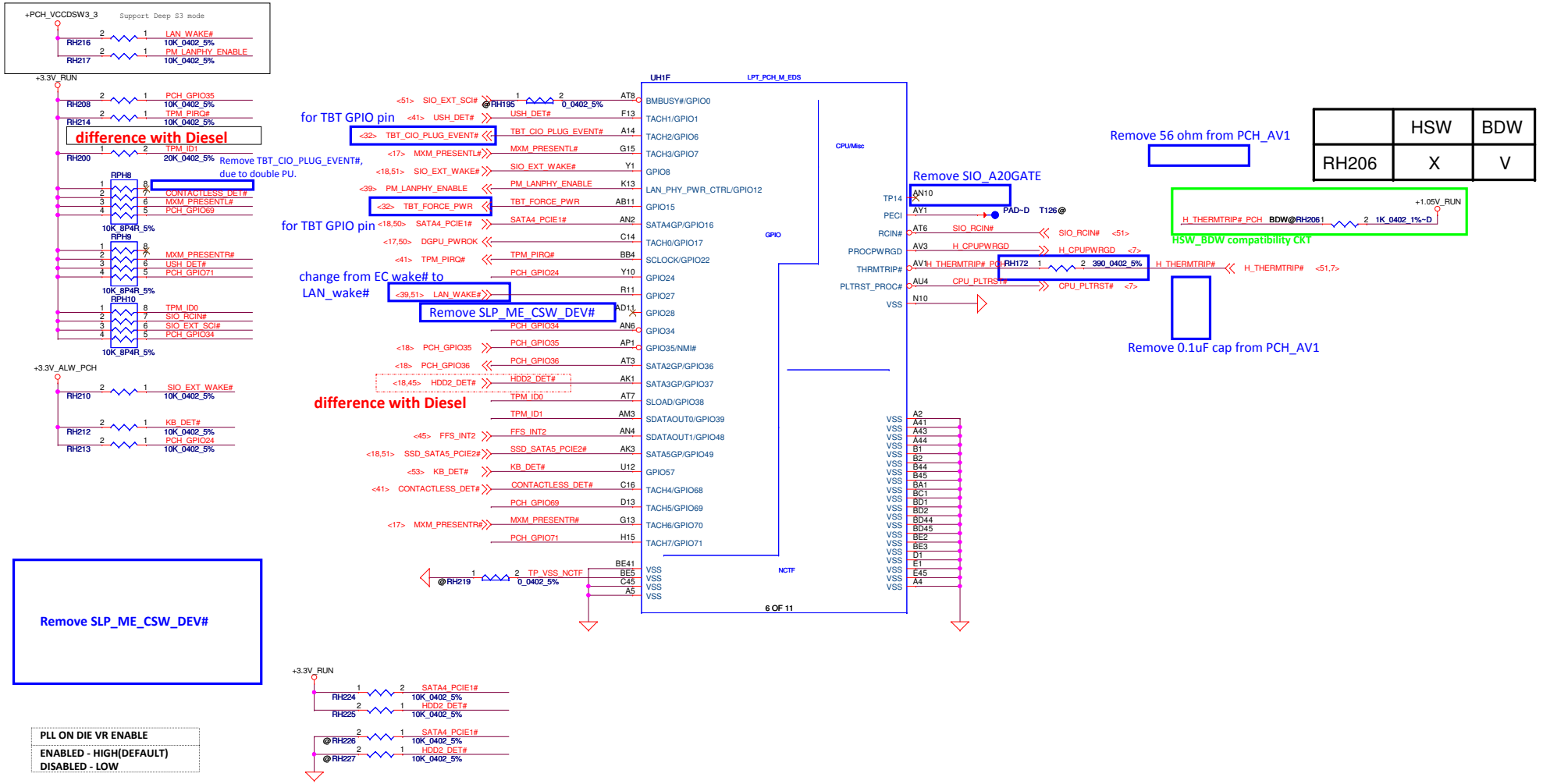

	HSW	BDW
RH206	X	V

Note: GPIO strap option is only available for SATA/PCIE muxed signals to support mSATA/mini PCIE port switching

GPIO16	GPIO49
0: PCIE1	0: PCIE2
1: SATA4	1: SATA5

00b or 01b: Assign muxed signal to desired port
10b: Reserved
11b: Assign desired port based on GPIO

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB31	USB32	USB35	USB36	PCIE1 (00) / USB33 (01)	PCIE2 (00) / USB34 (01)	PCIE3	PCIE4	PCIE5	PCIE6	PCIE7	PCIE8	SATA4 (00) / PCIE1 (01)	SATA5 (00) / PCIE2 (01)	SATA0	SATA1	SATA2	SATA3

SATA2GP/GPIO36 , SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK. WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOLD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

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Title: PCH (6/9)
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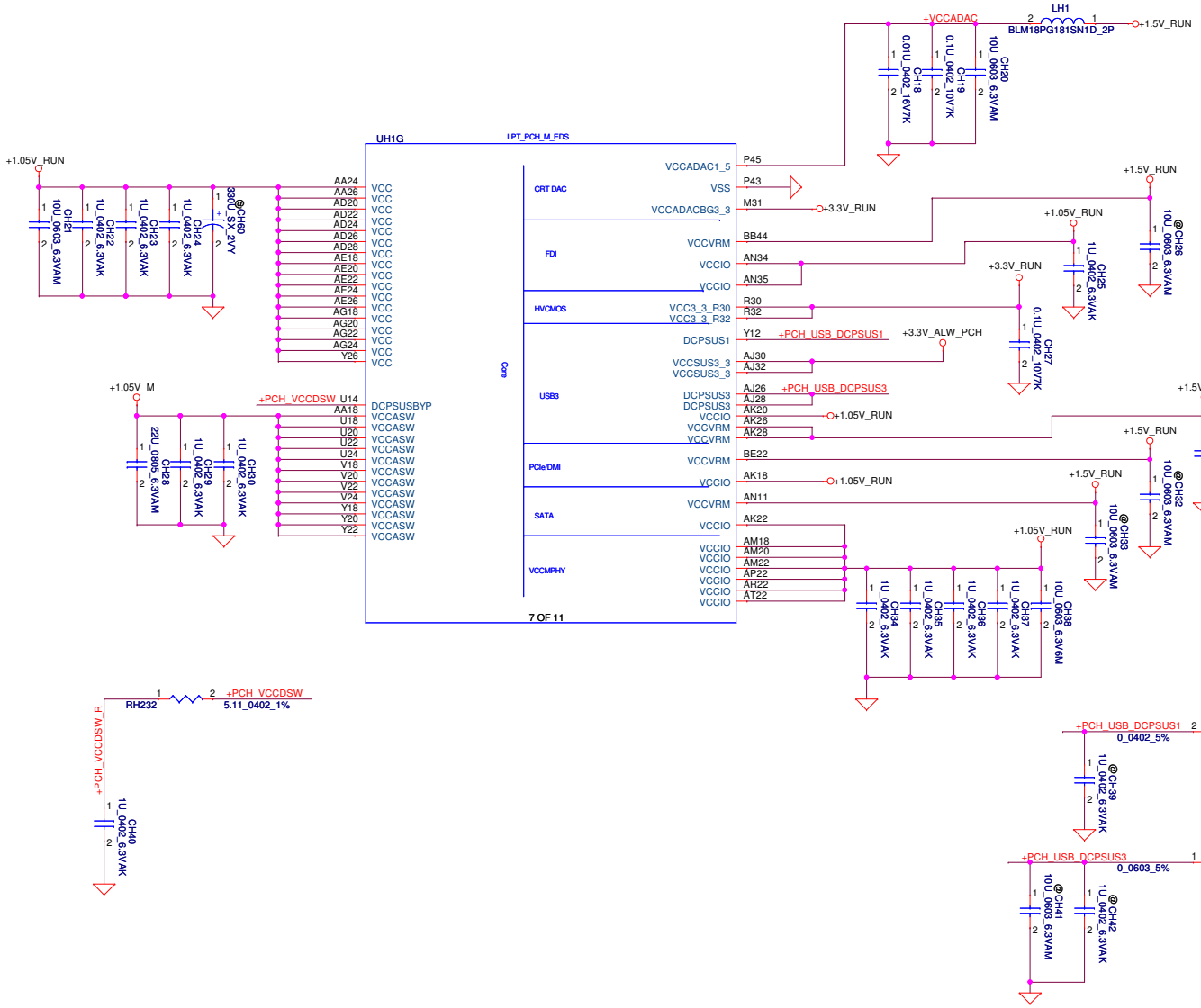

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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Title: PCH (7/9)

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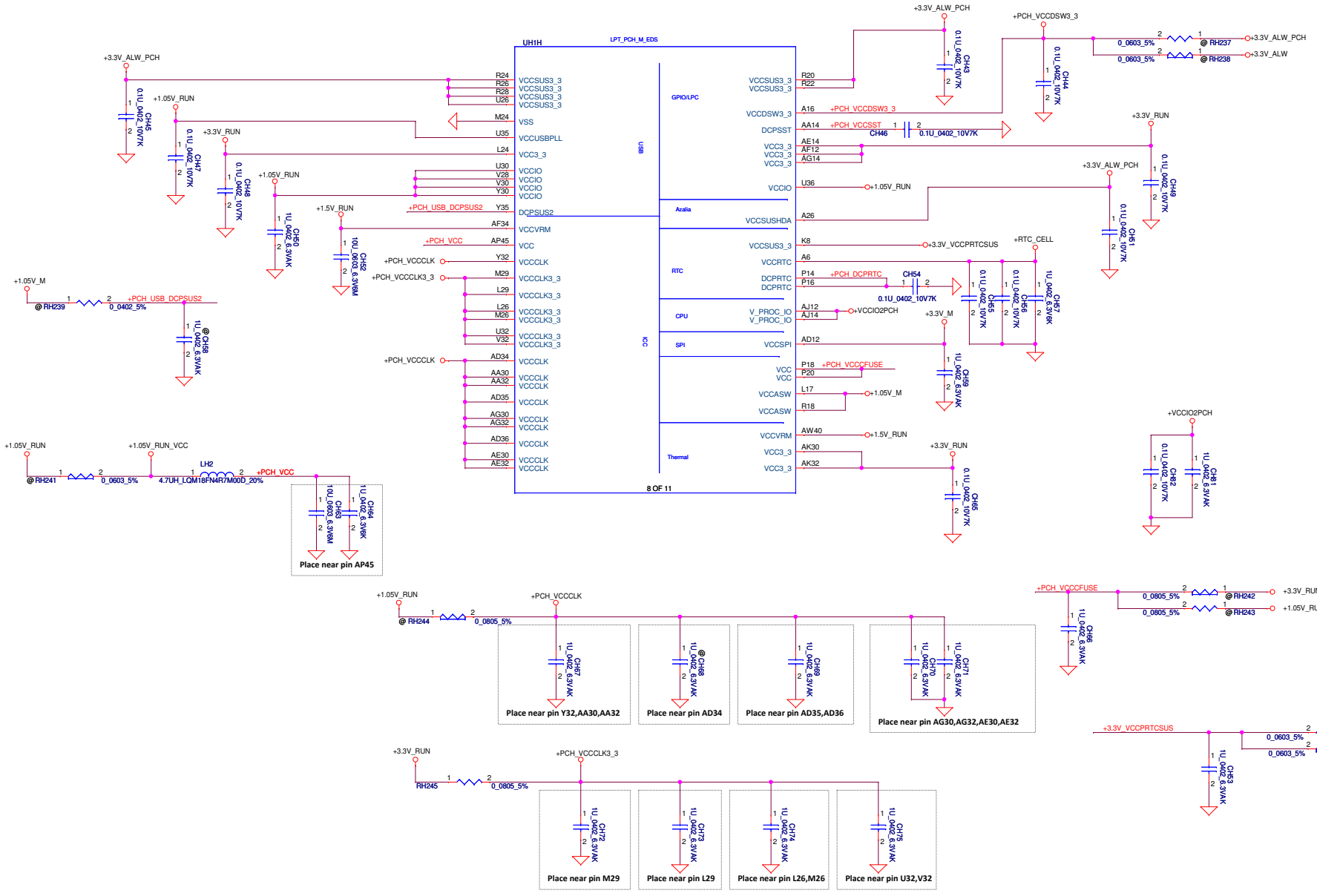
Support DEEP SX: populated RH238/RH246, de-populated RH237/RH240



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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Title: PCH (8/9)

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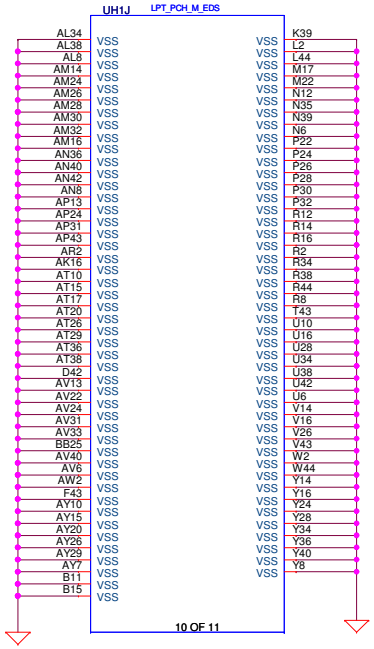

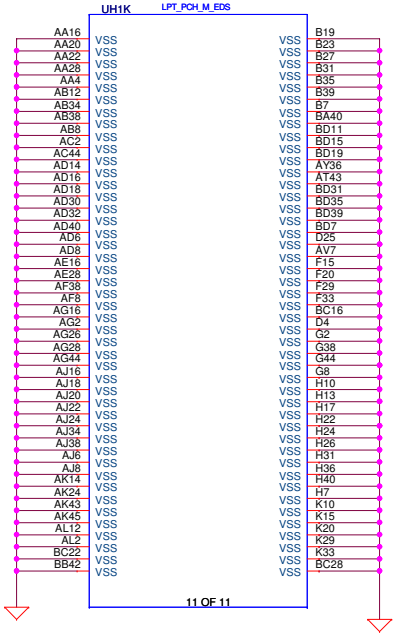

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Title: PCH (9/9)

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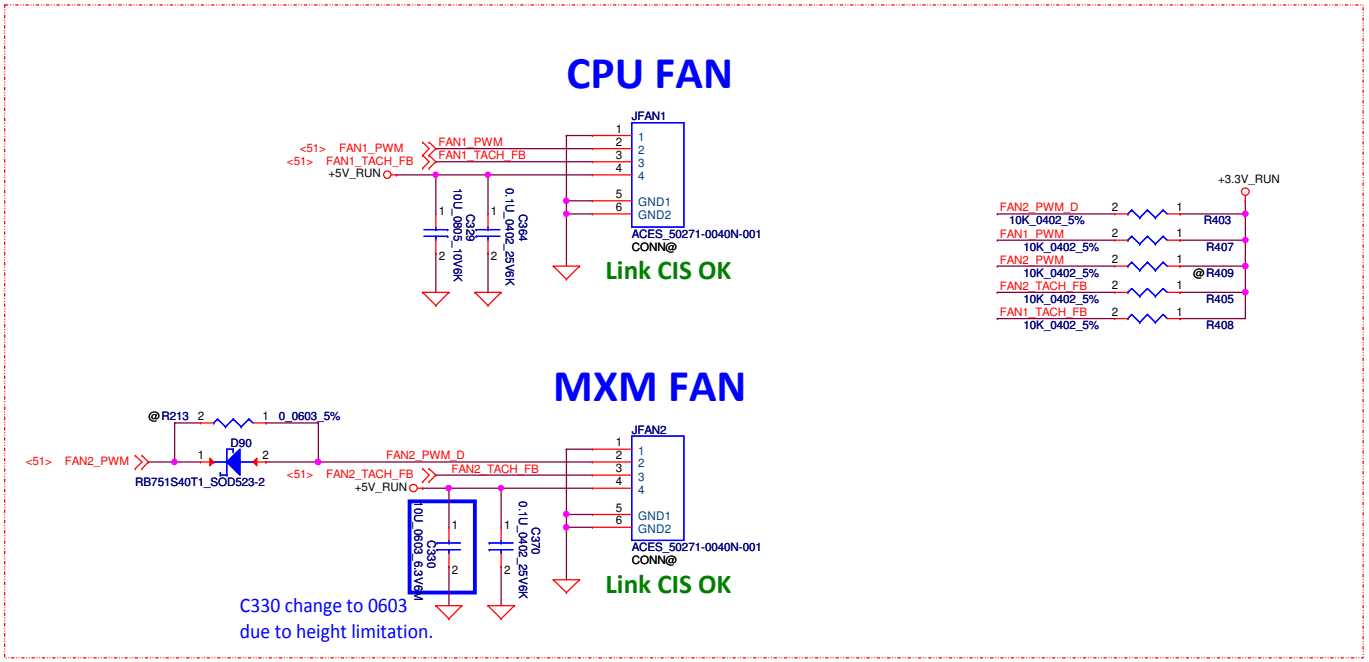
Difference with Diesel



Compal Electronics, Inc.

Title: FAN control

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Remove current sensor Monitor (SW solution)

Remove current sensor Monitor (HW solution)

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Compal Electronics, Inc.		
Title: Current Sensor		
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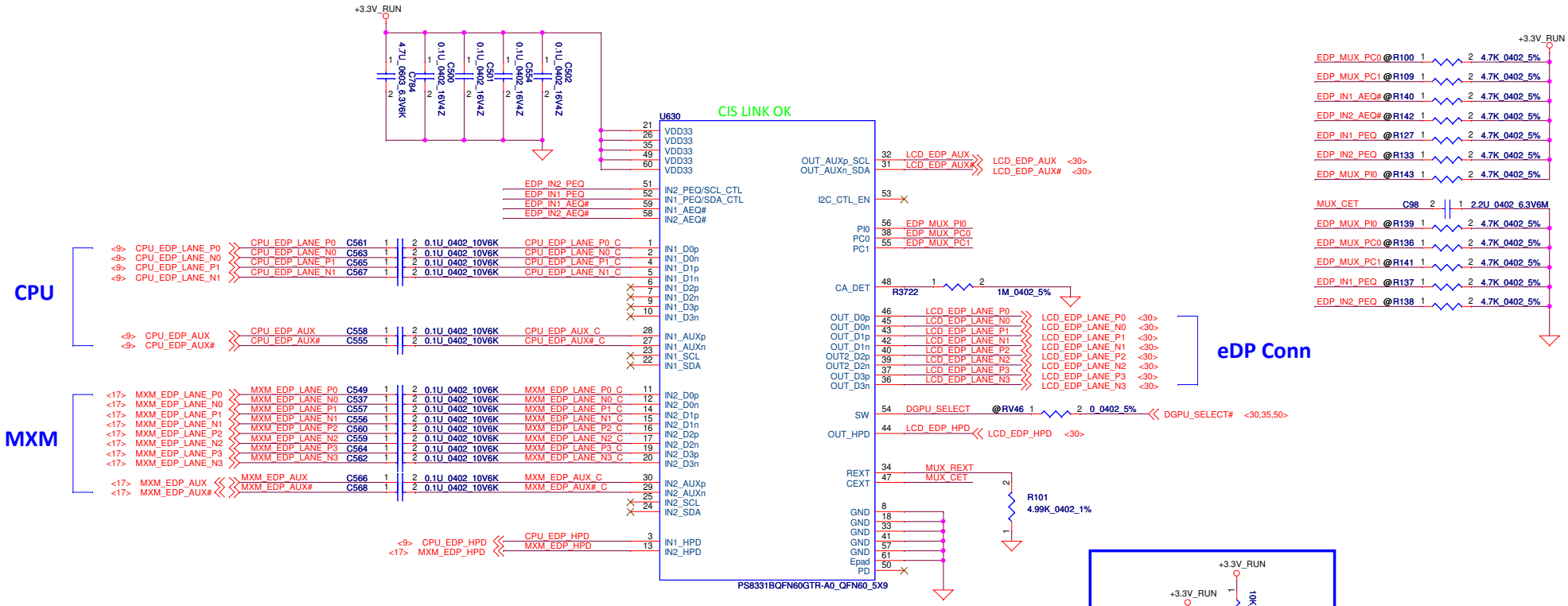

for DP Lane bus layout routing smoothly.

INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

Compal Electronics, Inc.

Title: eDP MUX (PS8331)

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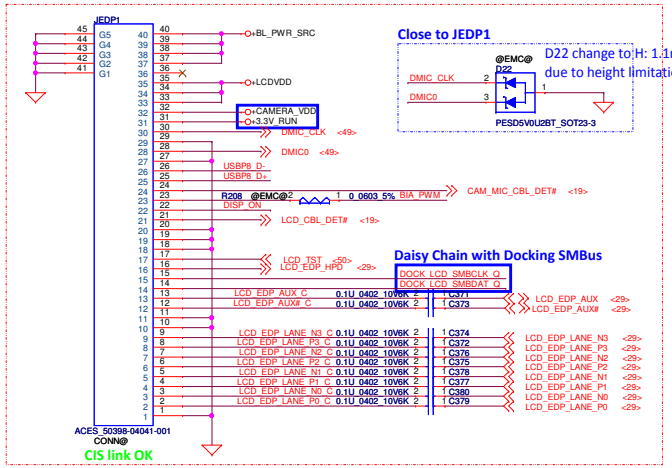
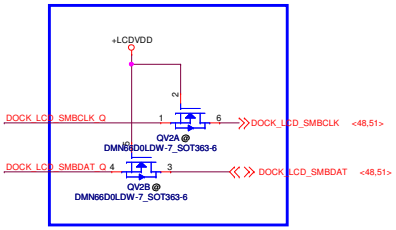
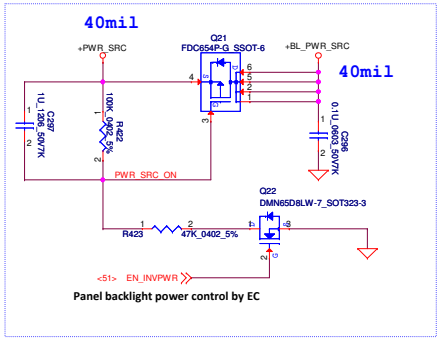
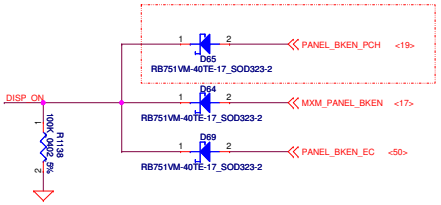
Difference with Diesel

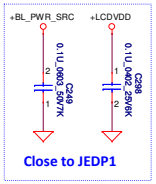


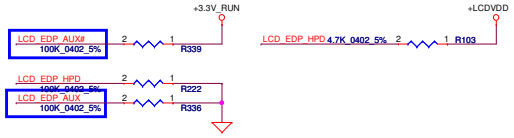




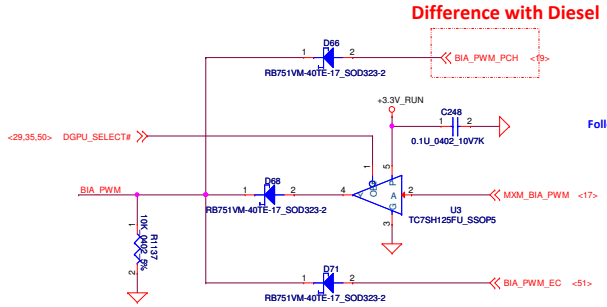
Difference with Diesel



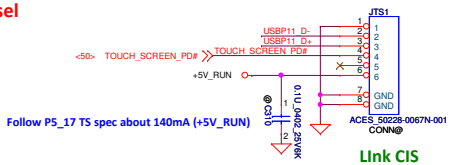


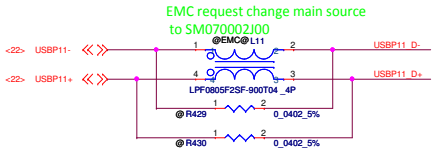


Difference with Diesel

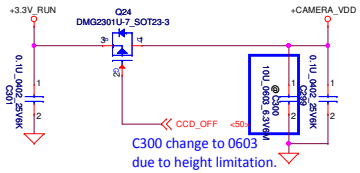


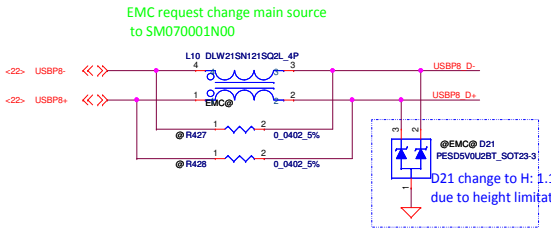
Touch Screen



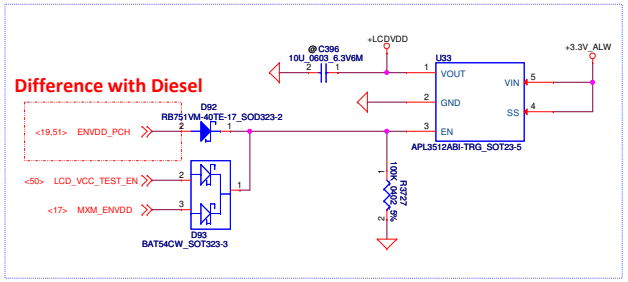


Webcam PWR CTRL





LCD Power



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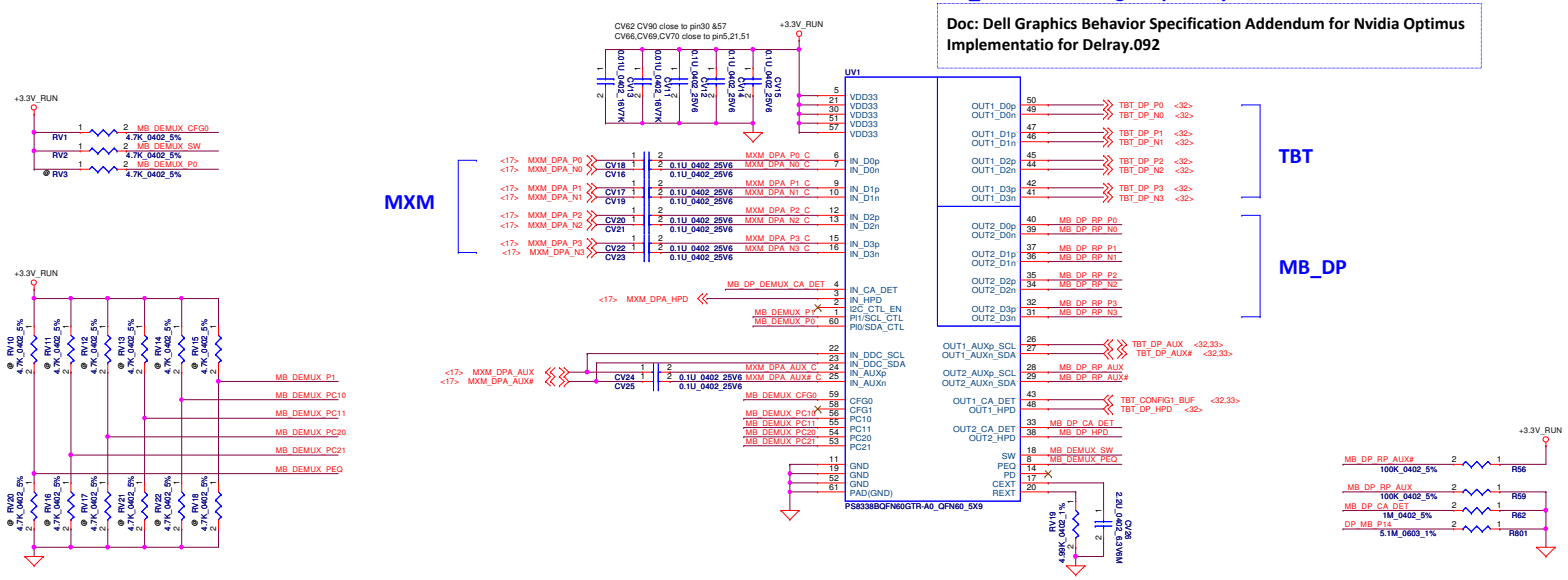
MB_DP will have higher priority over TBT.

Doc: Dell Graphics Behavior Specification Addendum for Nvidia Optimus Implementatio for Delray.092

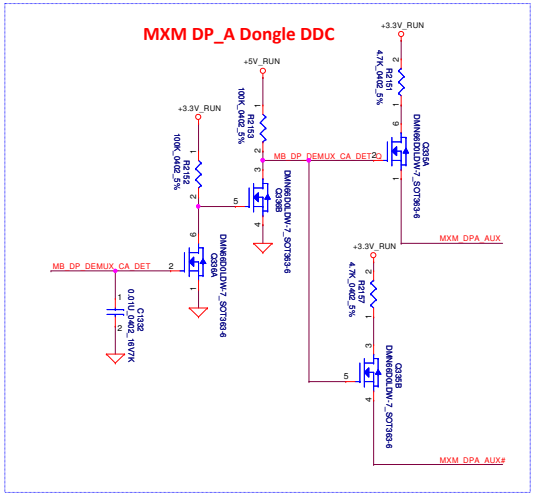


Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected

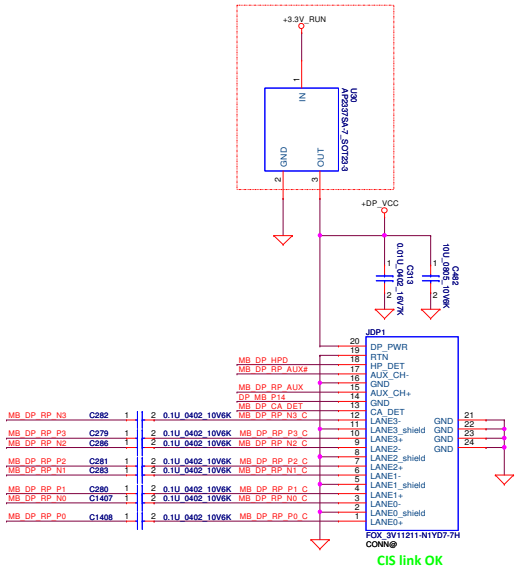
For Automatic Switching Mode (CFG0 = H): (By OUT1_HPD and OUT2_HPD)
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

	H	L
CFG0	V	
SW	V	

MXM DP_A Dongle DDC



Difference with Diesel



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Title	DP SW (PS8338) & DP Conn
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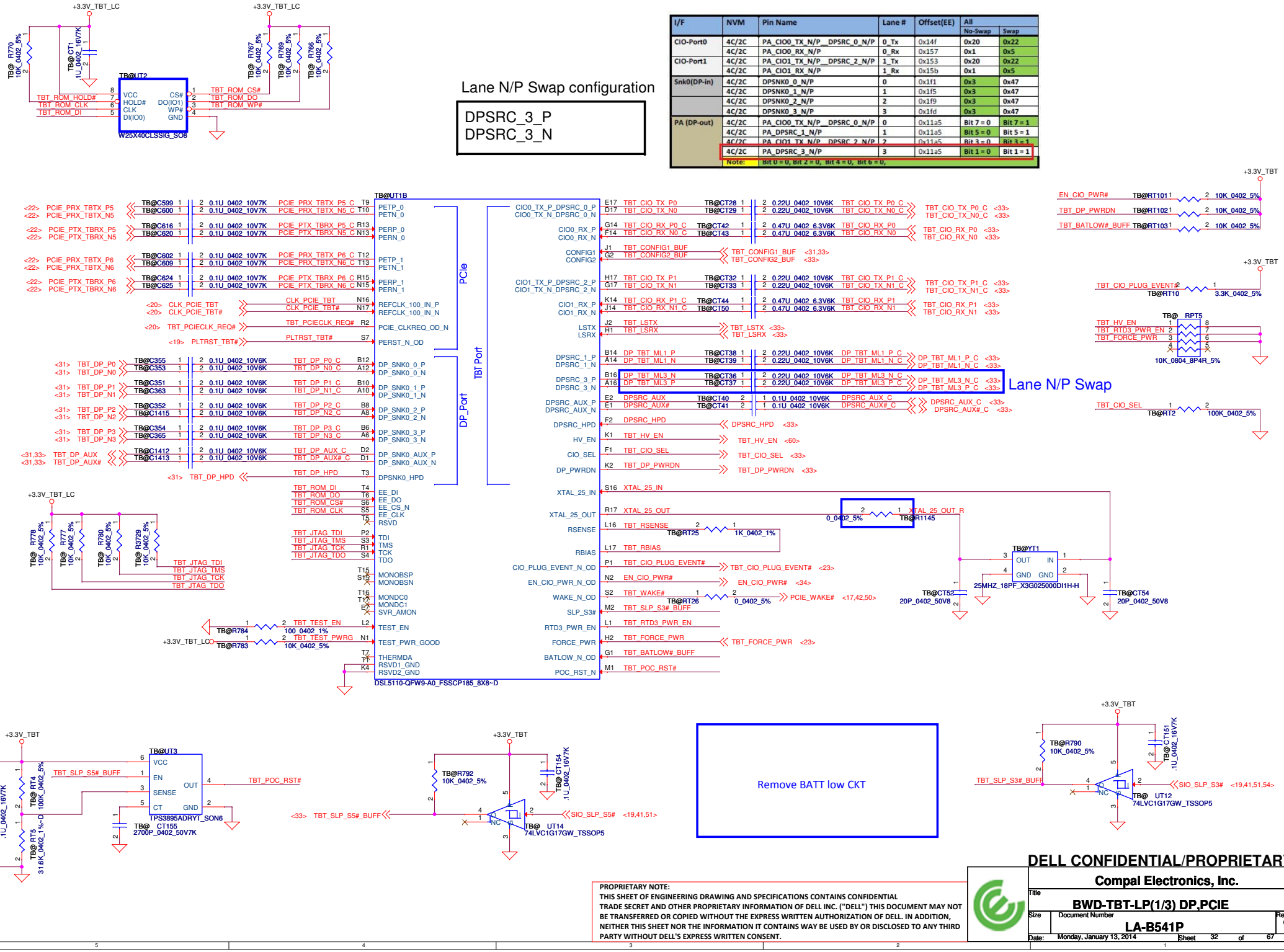
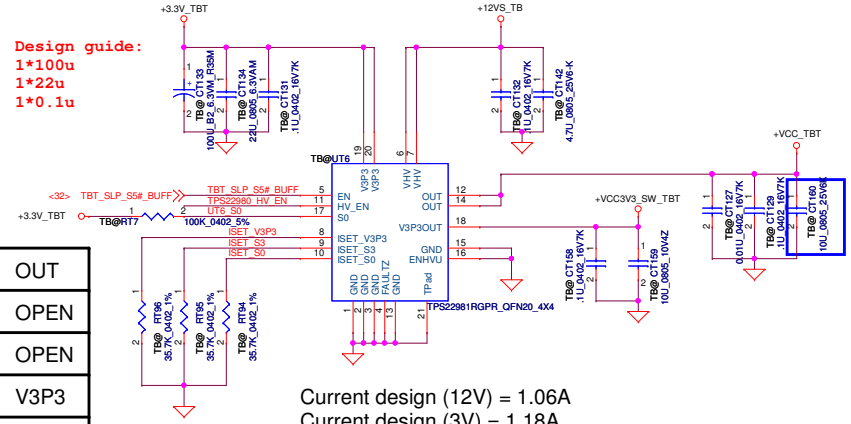
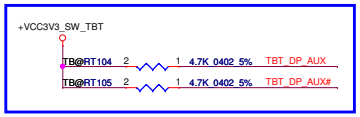
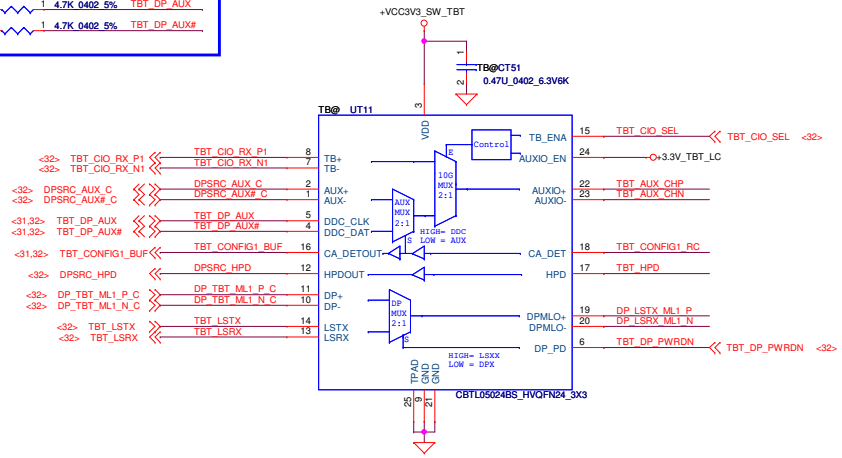


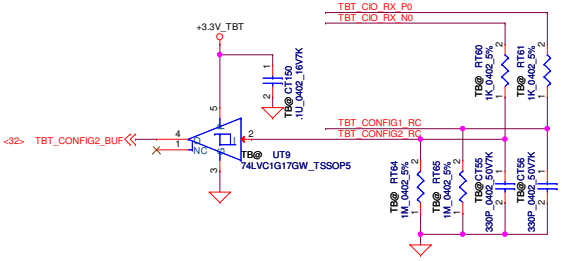
I/F	NVM	Pin Name	Lane #	Offset(EE)	All	
					No-Swap	Swap
CIO-Port0	4C/2C	PA_CIO0_TX_N/P__DPSRC_0_N/P	0_Tx	0x14f	0x20	0x22
	4C/2C	PA_CIO0_RX_N/P	0_Rx	0x157	0x1	0x5
CIO-Port1	4C/2C	PA_CIO1_TX_N/P__DPSRC_2_N/P	1_Tx	0x153	0x20	0x22
	4C/2C	PA_CIO1_RX_N/P	1_Rx	0x15b	0x1	0x5
Snk0(DP-in)	4C/2C	DPSNK0_0_N/P	0	0x1f1	0x3	0x47
	4C/2C	DPSNK0_1_N/P	1	0x1f5	0x3	0x47
	4C/2C	DPSNK0_2_N/P	2	0x1f9	0x3	0x47
	4C/2C	DPSNK0_3_N/P	3	0x1fd	0x3	0x47
PA (DP-out)	4C/2C	PA_CIO0_TX_N/P__DPSRC_0_N/P	0	0x11a5	Bit 7 = 0	Bit 7 = 1
	4C/2C	PA_DPSRC_1_N/P	1	0x11a5	Bit 5 = 0	Bit 5 = 1
	4C/2C	PA_CIO1_TX_N/P__DPSRC_2_N/P	2	0x11a5	Bit 3 = 0	Bit 3 = 1
	4C/2C	PA_DPSRC_3_N/P	3	0x11a5	Bit 1 = 0	Bit 1 = 1
	Note:	Bit 0 = 0, Bit 2 = 0, Bit 4 = 0, Bit 6 = 0,				

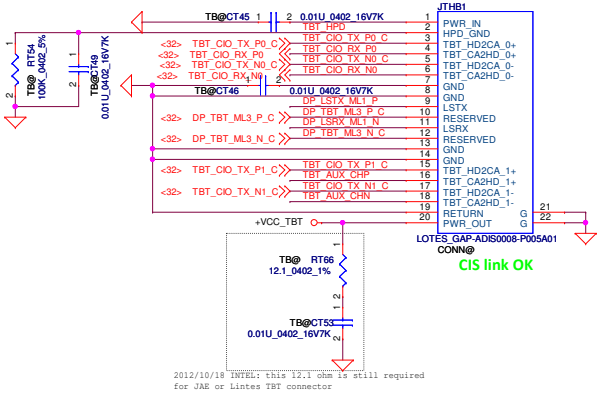


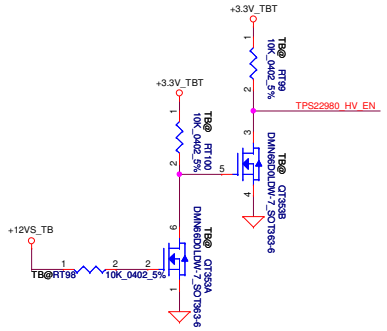
EN	HV_EN	OUT
0	0	OPEN
0	1	OPEN
1	0	V3P3
1	1	VHV











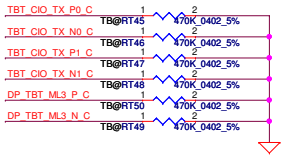


Table 3-1. Cable Type Indications

HPD	CONFIG1	CONFIG2	LSRX	Cable Type	Comments
0	X	0	X	None	Cable is disconnected
1	0	0	X	DisplayPort	
1	1	X	X	DVI/HDMI	Host/Source software determines DVI or HDMI
0	0	1	0	Thunderbolt	Thunderbolt Technology cable attached but no Thunderbolt Host/Device attached
0	0	1	1	Thunderbolt	Thunderbolt Technology operation

Compal Electronics, Inc.

Title: BWD-TBT-LP(2/3) HOST,mDP

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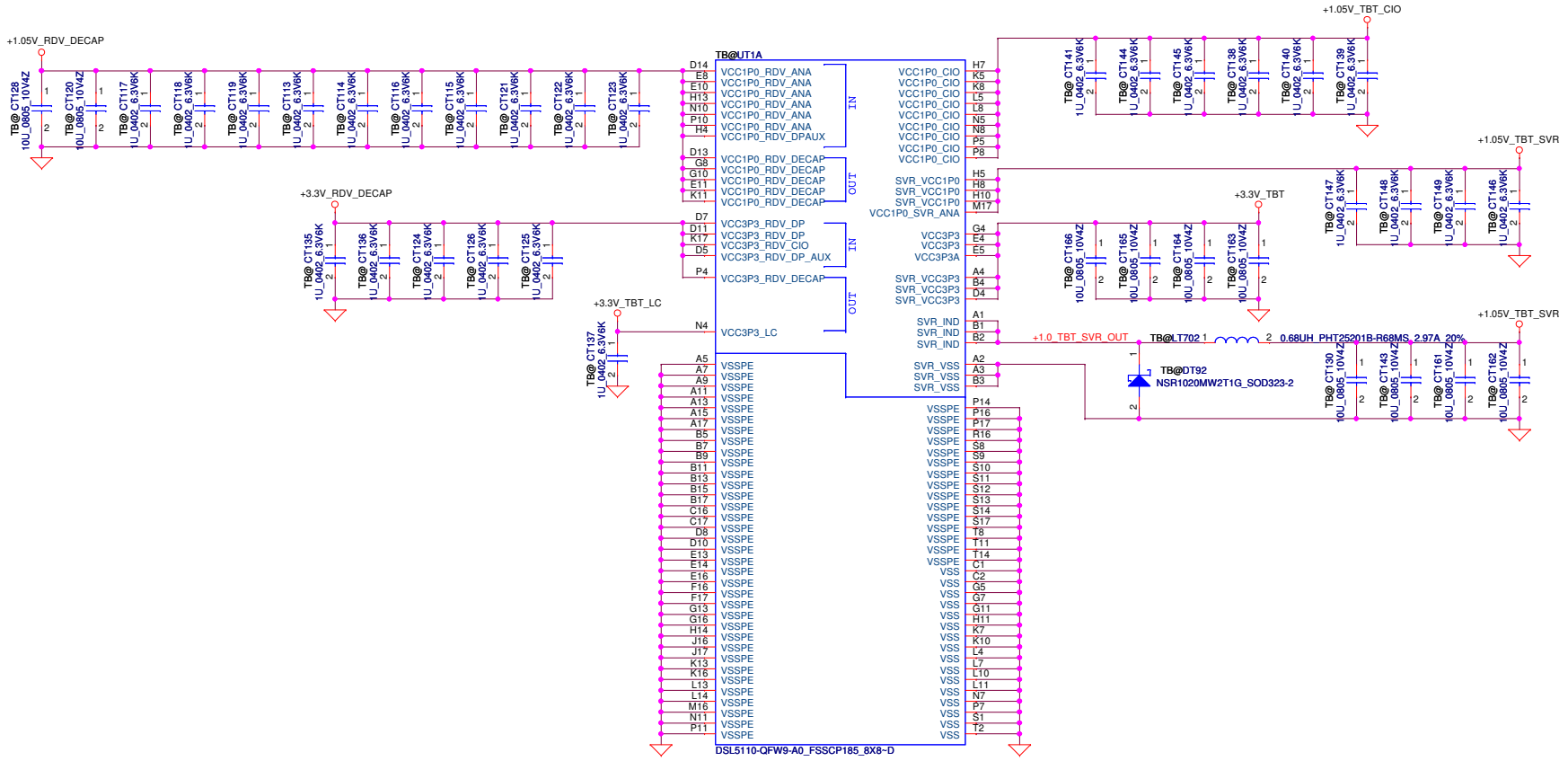
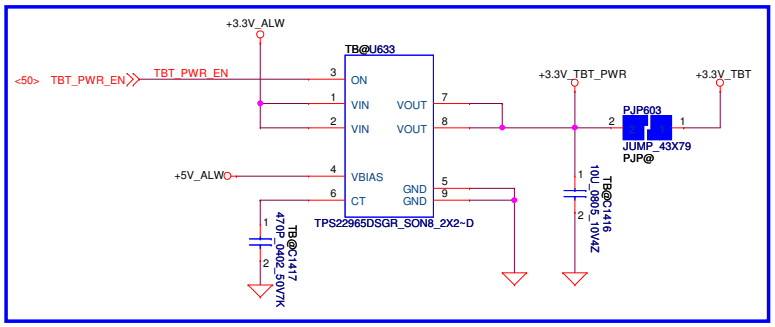
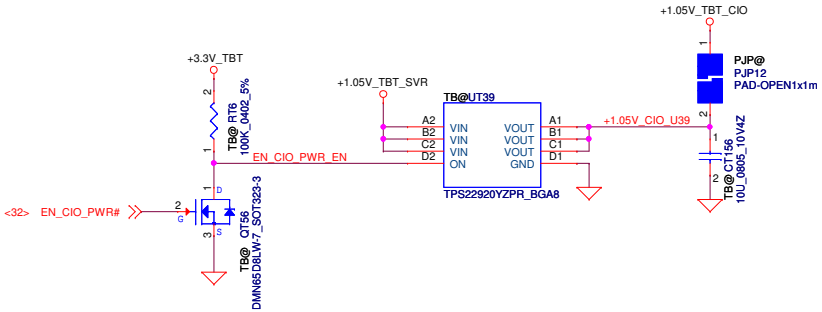


TBT Power circuit





Compal Electronics, Inc.		
Title: BWD-TBT-LP(3/3) VCC/VSS		
Size	Document Number: LA-B541P	Rev: 0.1
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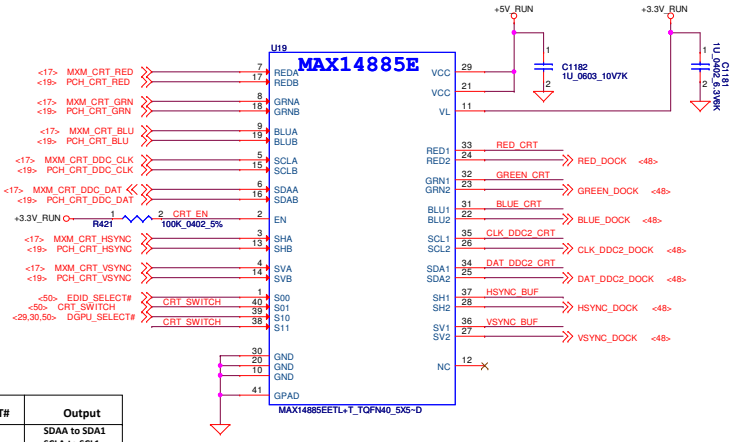
Channel A (MXM)

Channel B (PCH)

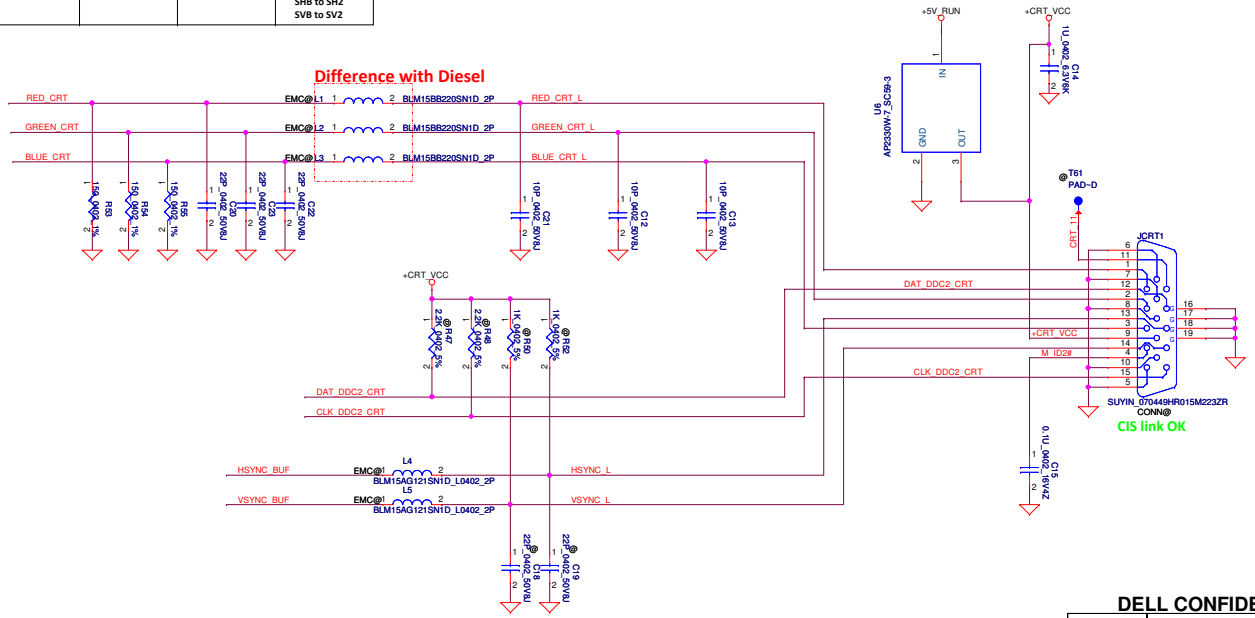


Port 1 (MB_CRT)

Port 2 (Dock_CRT)

	CRT_SWITCH	DGPU_SELECT#	EDID_SELECT#	Output
DSC mode output to MB VGA	0	0	0	SDAA to SDA1 SCLA to SCL1 REDA to RED1 GRNA to GRN1 BLUA to BLU1 SHA to SH1 SVA to SV1
DSC mode output to docking VGA	1	0	0	SDAA to SDA2 SCLA to SCL2 REDA to RED2 GRNA to GRN2 BLUA to BLU2 SHA to SH2 SVA to SV2
UMA mode output to MB VGA	0	1	1	SDAB to SDA1 SCLB to SCL1 REDB to RED1 GRNB to GRN1 BLUB to BLU1 SHB to SH1 SVB to SV1
UMA mode output to docking VGA	1	1	1	SDAB to SDA2 SCLB to SCL2 REDB to RED2 GRNB to GRN2 BLUB to BLU2 SHB to SH2 SVB to SV2

Difference with Diesel



Compal Electronics, Inc.

Title: VGA CONN

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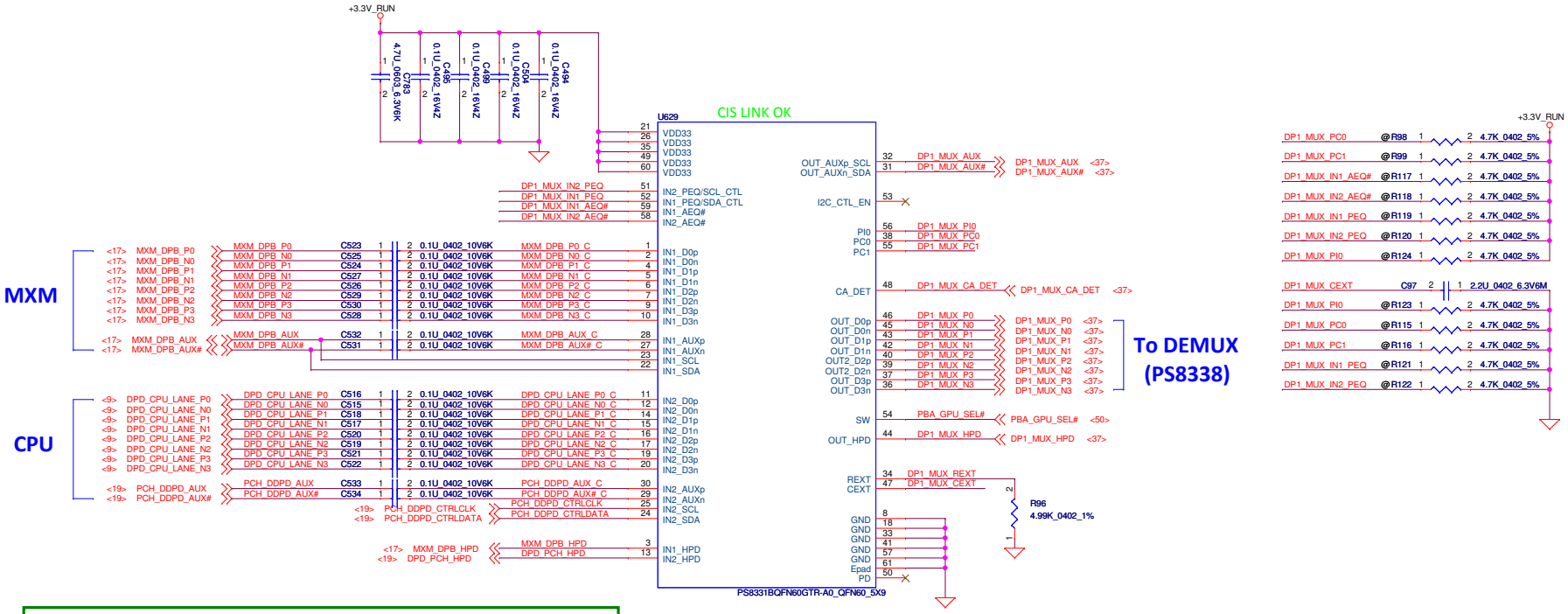

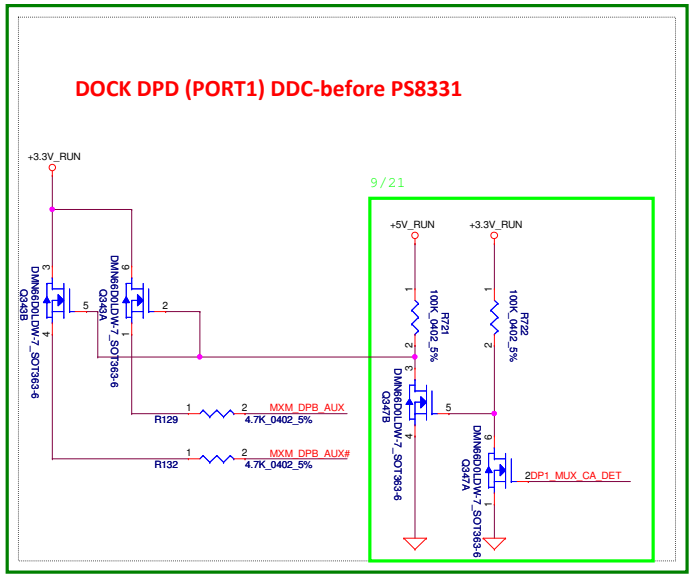


```
INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2
```

```
INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable
```

```
PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable
```

```
PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB
```

```
PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%
```


Compal Electronics, Inc.	
Title	MXM/CPU MUX(PS8331)
Size	Document Number: LA-B541P
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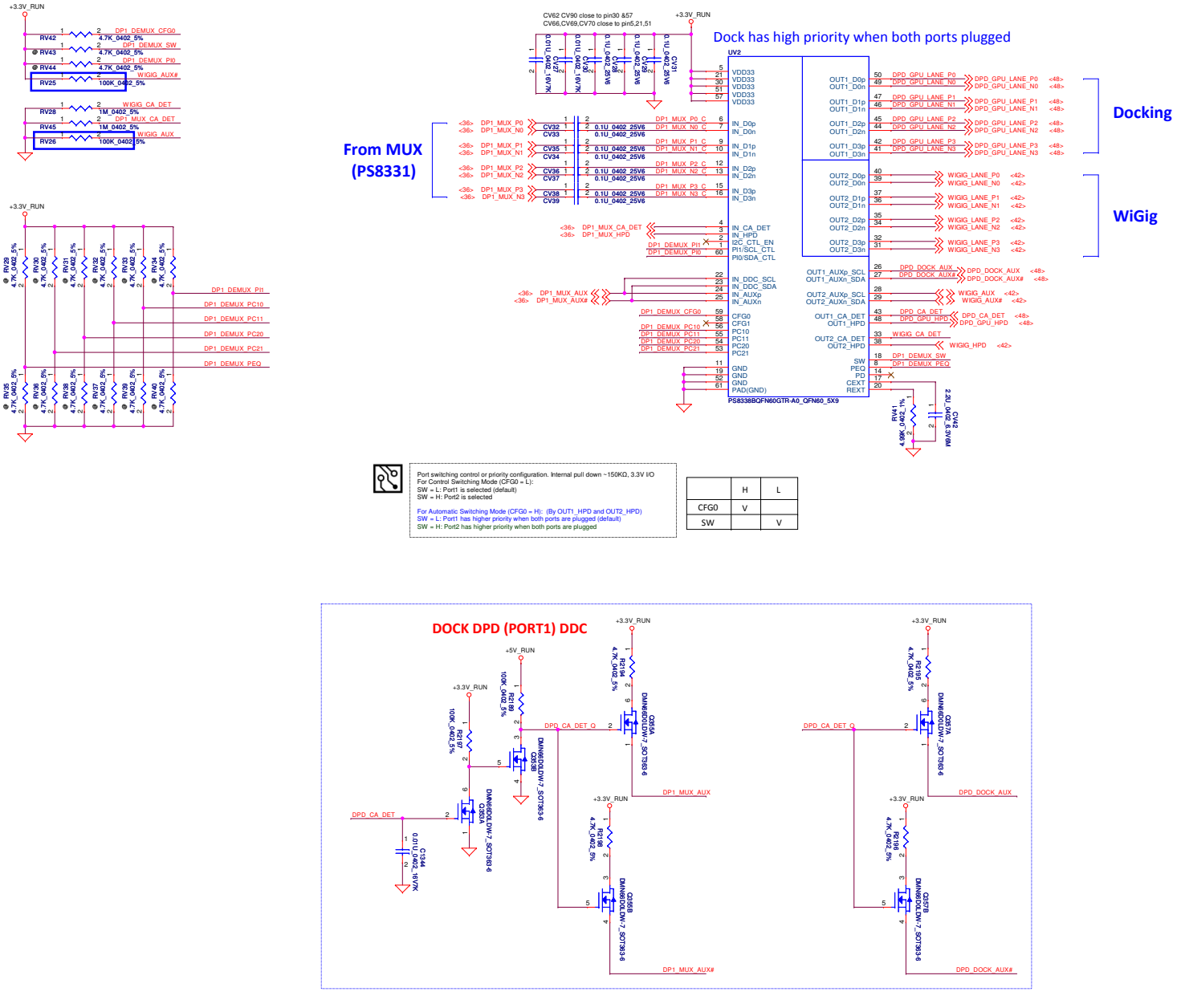
Dock has high priority when both ports plugged
From MUX (PS8331)
Docking
WiGig
DOCK DPD (PORT1) DDC
PS8338BQFN60GTR-A0_QFN60_5X9
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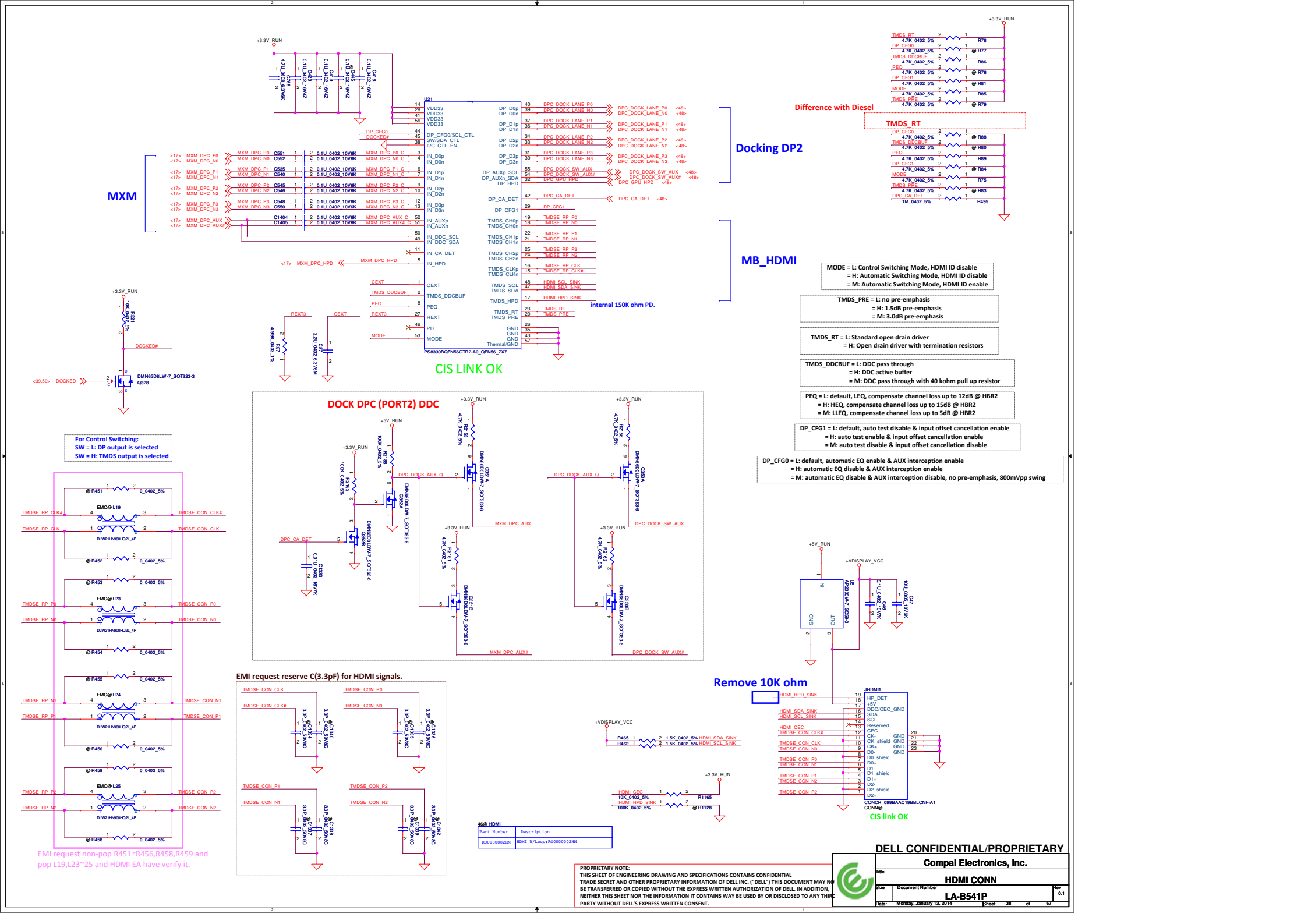
Compal Electronics, Inc.
DP DeMUX (PS8338)
LA-B541P
Monday, January 13, 2014


MXM
Docking DP2
MB_HDMI
Difference with Diesel
TMDS_RT
CIS LINK OK
internal 150K ohm PD.
DOCK DPC (PORT2) DDC
For Control Switching:
SW = L: DP output is selected
SW = H: TMDS output is selected
EMI request reserve C(3.3pF) for HDMI signals.
EMI request non-pop R451~R456,R458,R459 and pop L19,L23~25 and HDMI EA have verify it.
MODE = L: Control Switching Mode, HDMI ID disable
= H: Automatic Switching Mode, HDMI ID disable
= M: Automatic Switching Mode, HDMI ID enable
TMDS_PRE = L: no pre-emphasis
= H: 1.5dB pre-emphasis
= M: 3.0dB pre-emphasis
TMDS_RT = L: Standard open drain driver
= H: Open drain driver with termination resistors
TMDS_DDCBUF = L: DDC pass through
= H: DDC active buffer
= M: DDC pass through with 40 kohm pull up resistor
PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
= H: HEQ, compensate channel loss up to 15dB @ HBR2
= M: LLEQ, compensate channel loss up to 5dB @ HBR2
DP_CFG1 = L: default, auto test disable & input offset cancellation enable
= H: auto test enable & input offset cancellation enable
= M: auto test disable & input offset cancellation disable
DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
= H: automatic EQ disable & AUX interception enable
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing
Remove 10K ohm
CIS link OK
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PROPRIETARY NOTE:
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Compal Electronics, Inc.
HDMI CONN
LA-B541P
Monday, January 13, 2014
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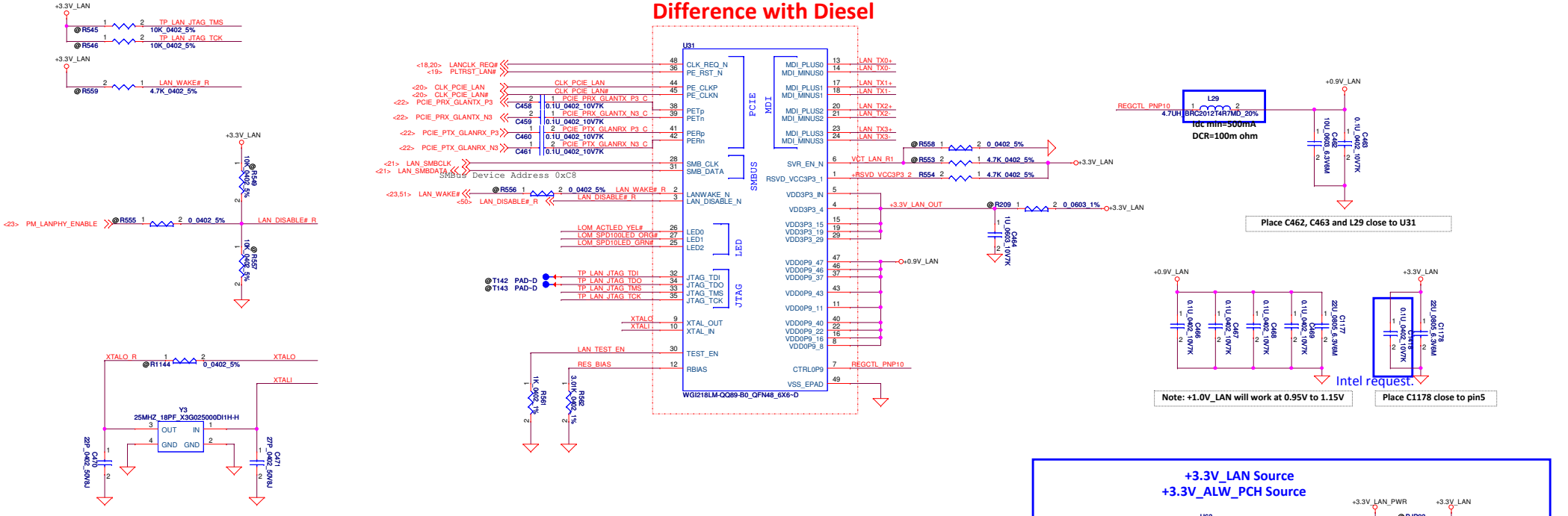
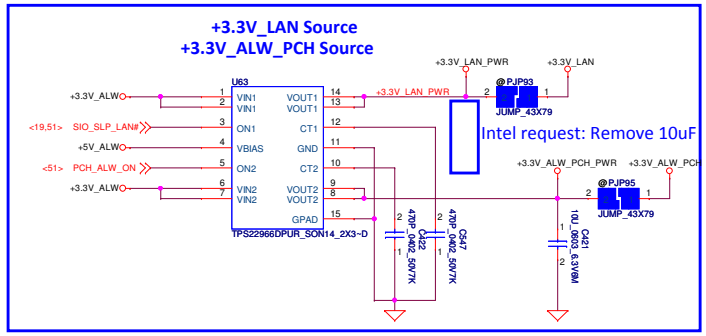
0.1

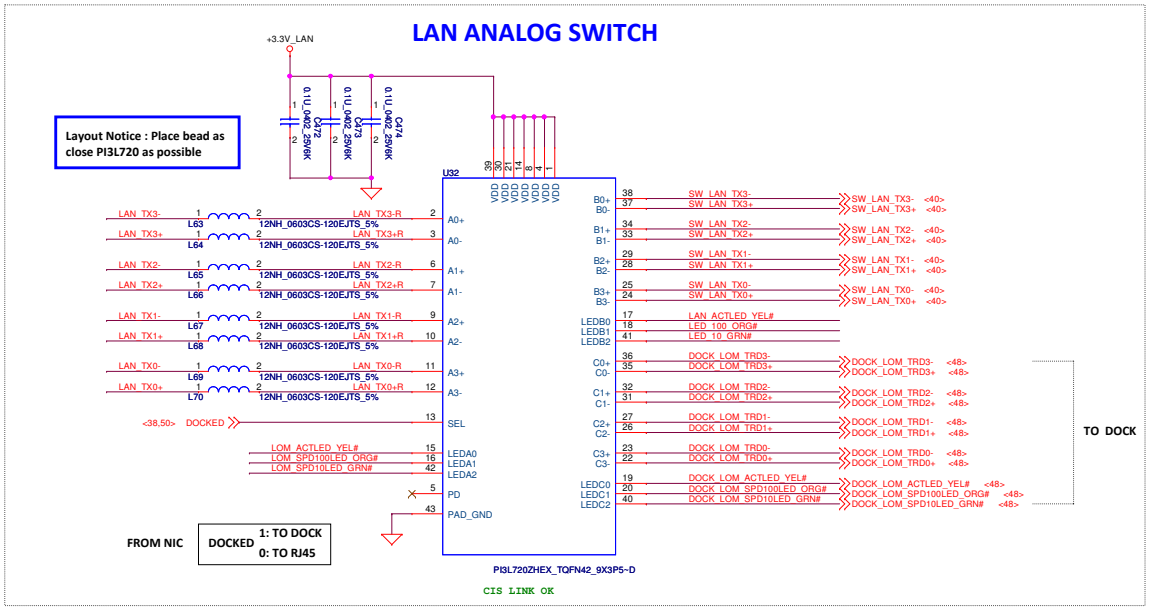
Difference with Diesel

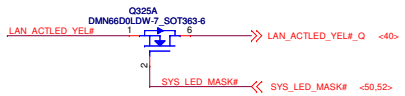


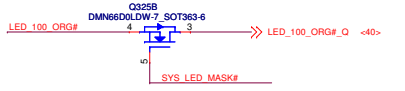
+3.3V_LAN Source
+3.3V_ALW_PCH Source

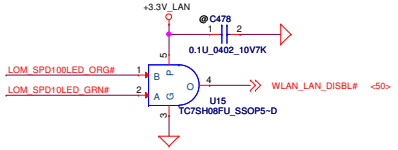


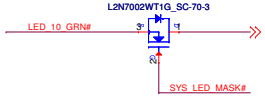
LAN ANALOG SWITCH











Compal Electronics, Inc.

Title: LAN/LAN SW

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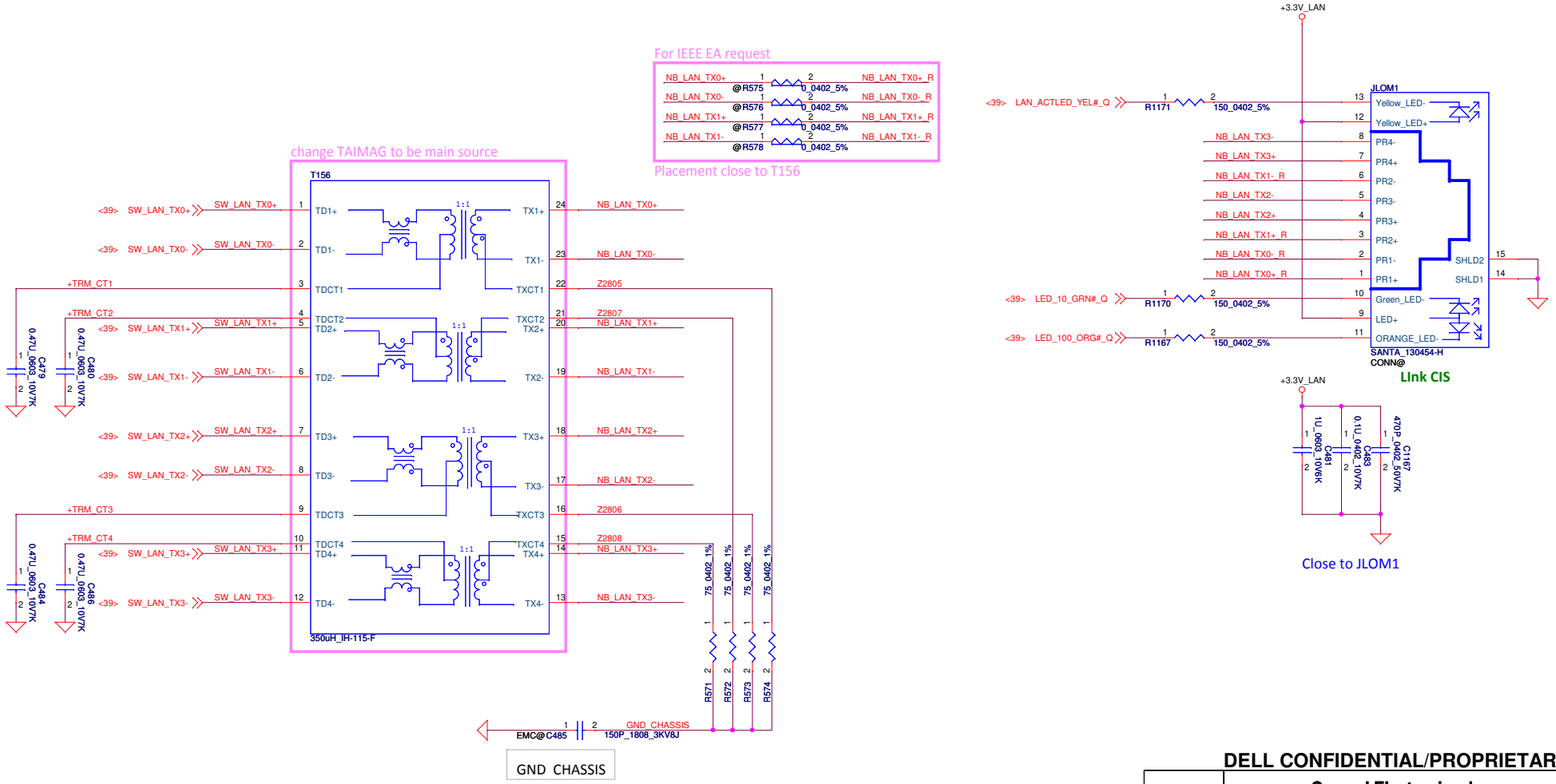
+3.3V_LAN/+3.3V_LAN_LOM:20mils



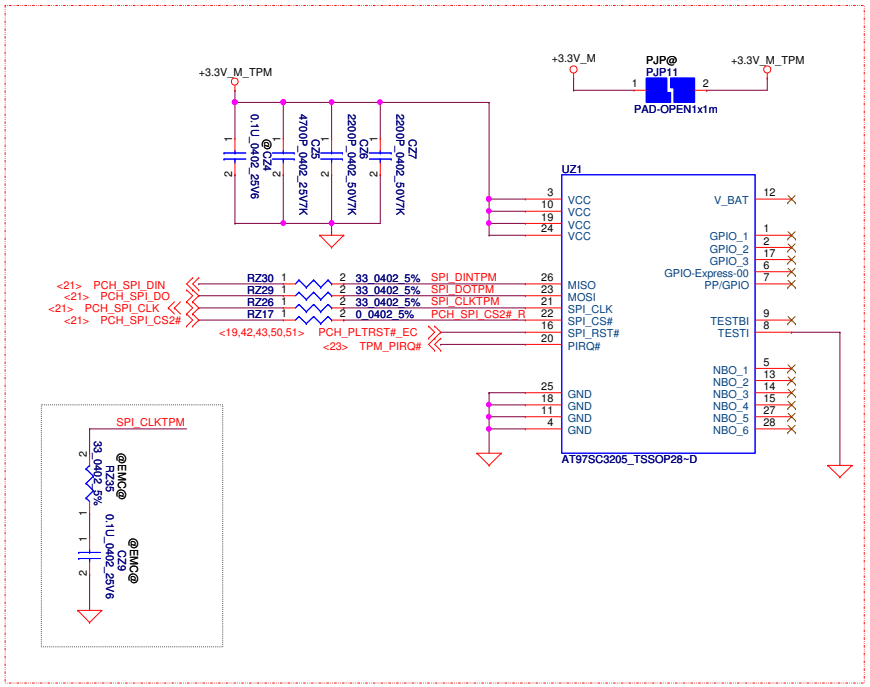
Compal Electronics, Inc.

Title: RJ45

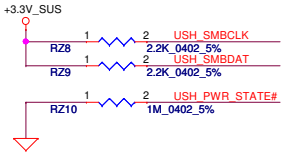
Size | Document Number: LA-B541P | Rev: 0.1

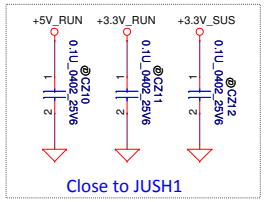
Date: Monday, January 13, 2014 | Sheet 40 of 67

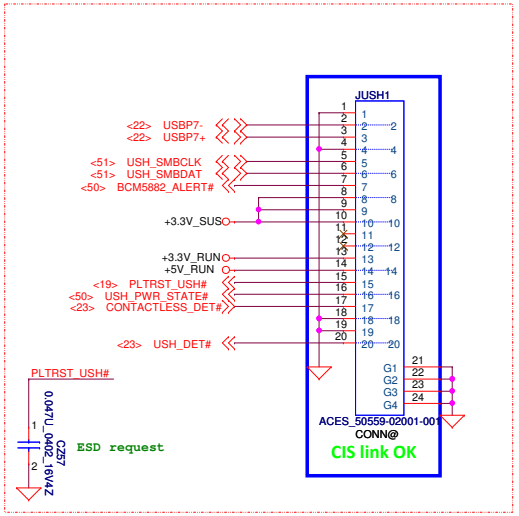
Difference with Diesel

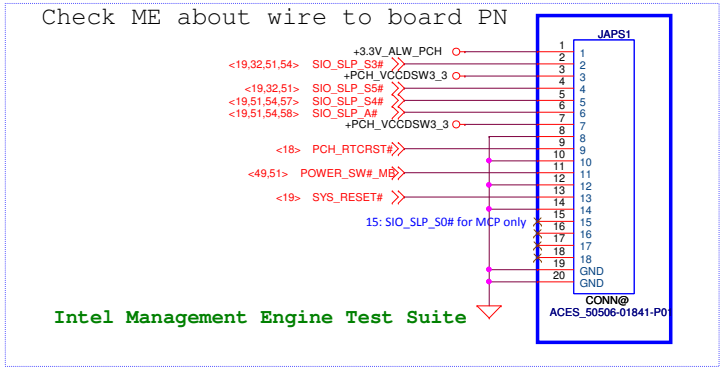


Difference with Diesel









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Title: TPM/USH

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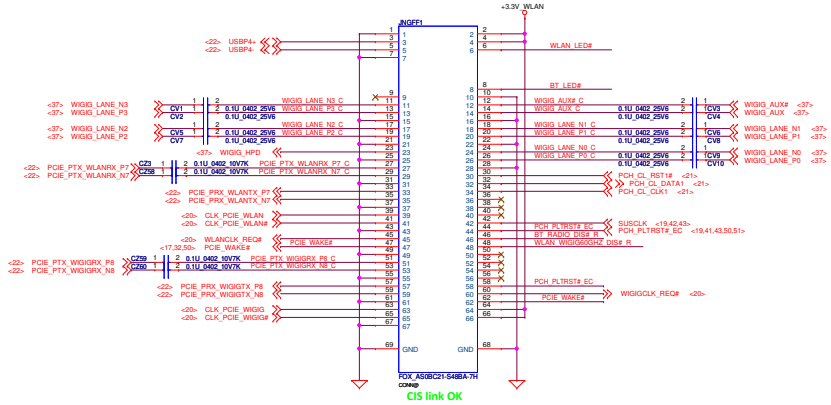
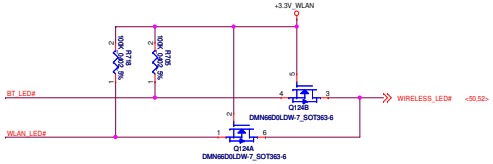
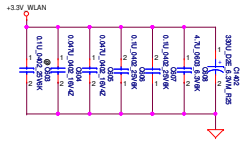
WLAN/BT/WiGig

NGFF slot_1 Key A



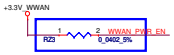
CIS link OK

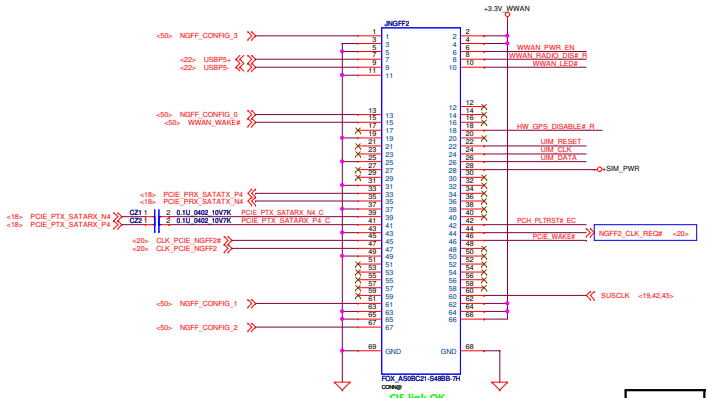




WWAN/LTE/HCA/Cache

NGFF slot_2 Key B





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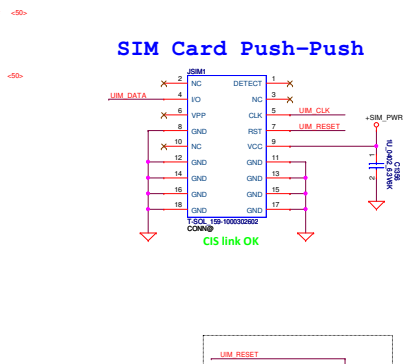
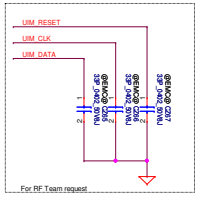
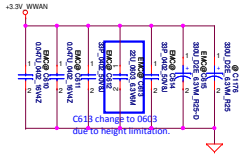


SIM Card Push-Push

CIS link OK





C613 change to 0603 due to height limitation.

C615 footprint change to C_APXK2R5ARA331MF451

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	0	0	0	0	SSD-SATA
8	1	0	0	0	WWAN
14	1	0	1	1	HCA-PCIE
15	1	1	1	1	NA

Compal Electronics, Inc.

Title	M.2 Card-1/2	
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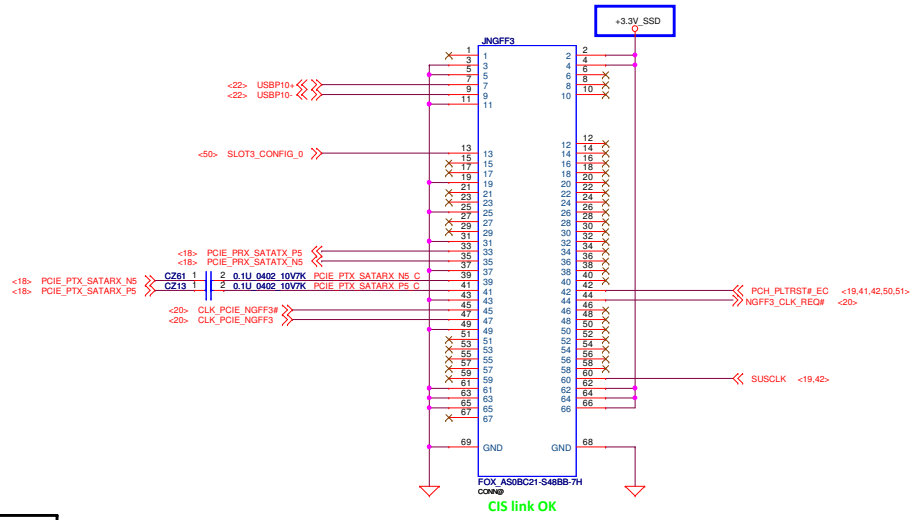
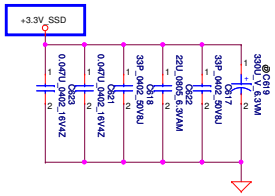
SSD/HCA/Cache

NGFF slot_3 Key B



CIS link OK

STATE #	CONFIG_0	Module Type
0	0	SSD-SATA
14	1	HCA-PCIE



Compal Electronics, Inc.

Title: M.2 Card-2/2

Size: Document Number: LA-B541P Rev: 0.1

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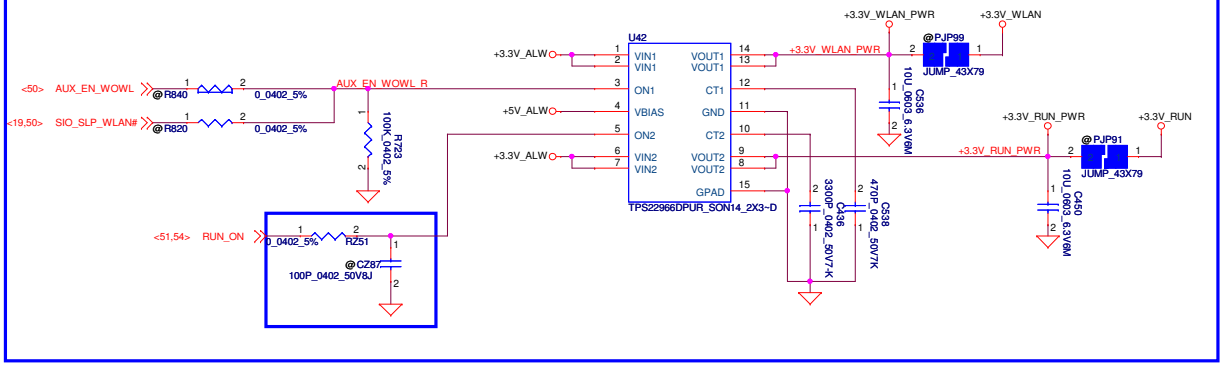
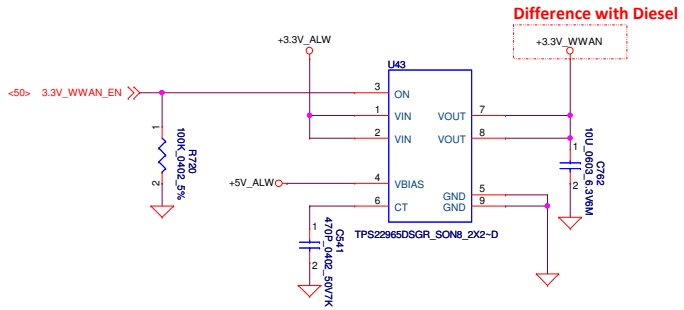
Power Control for M.2 slot 1.
& +3.3V_RUN Source

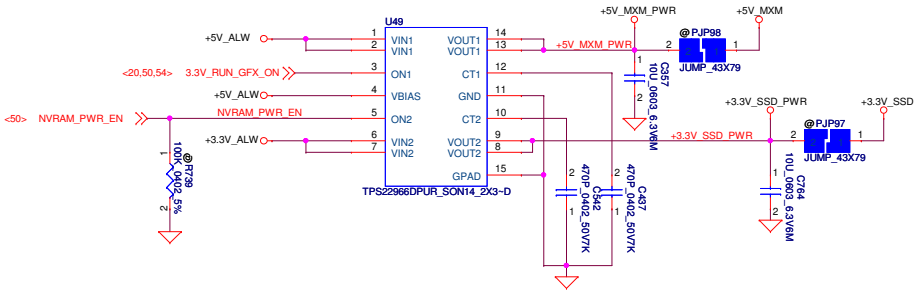


Power Control for M.2 slot 2.

Difference with Diesel



Power Control for M.2 slot 3.
& +5V_MXM Source



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Compal Electronics, Inc.

Title: M.2 Card PWR

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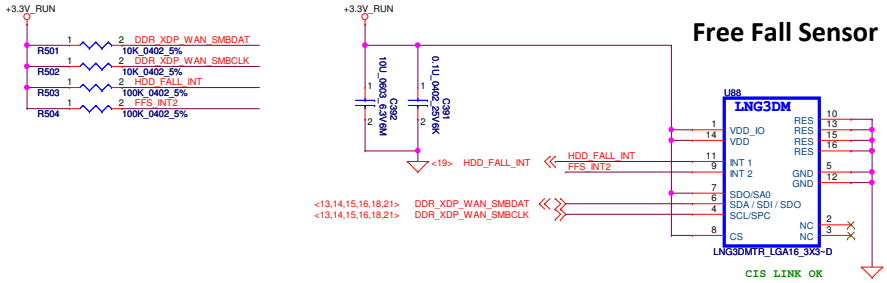

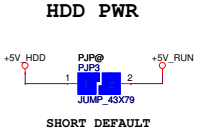

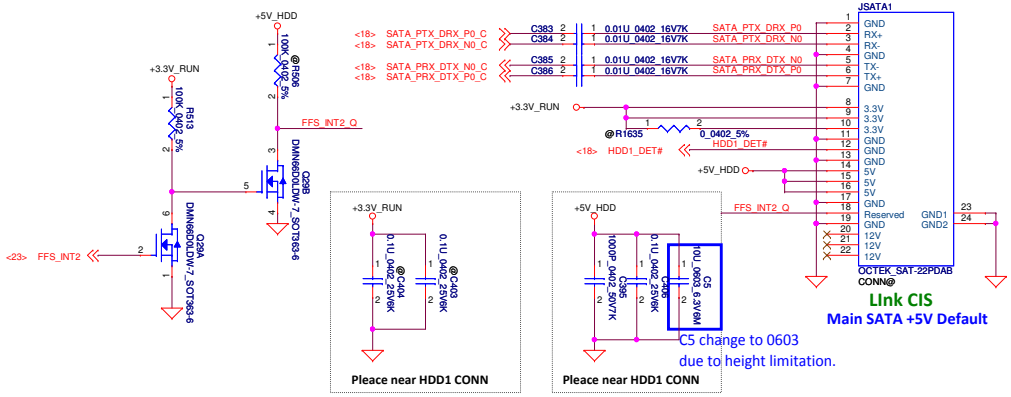

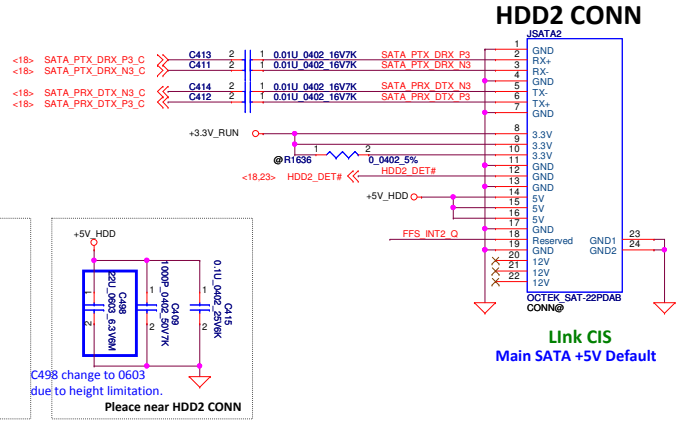

Compal Electronics, Inc.

Title: HDD CONN

Size: | Document Number: LA-B541P | Rev: 0.1

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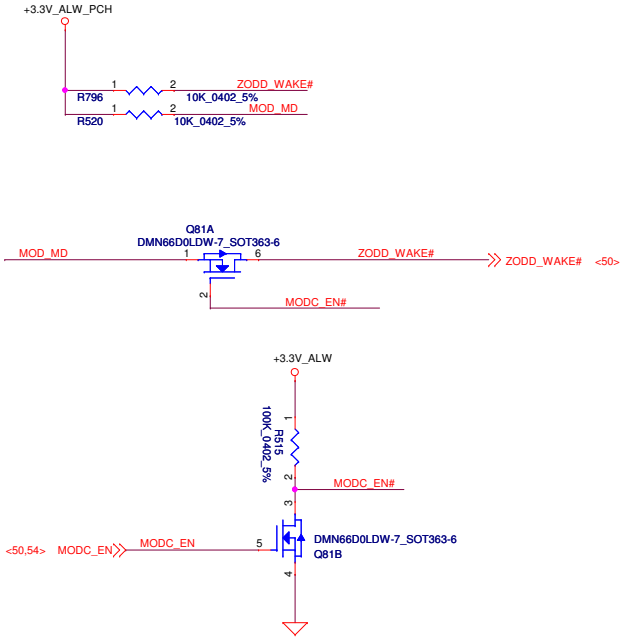
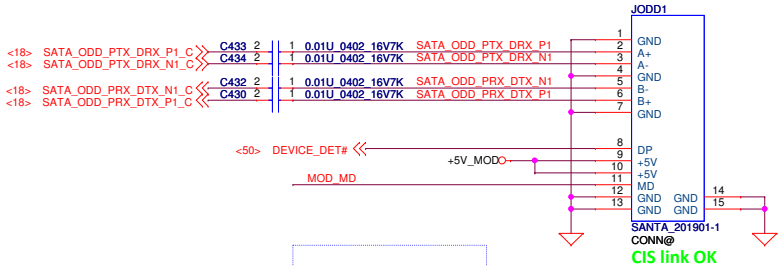
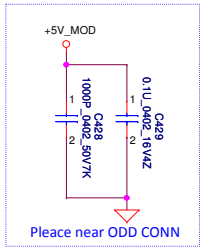
Combine +5VMOD with +5V_RUN



ODD CONN





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Compal Electronics, Inc.		
Title: ODD CONN		
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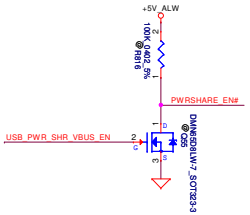
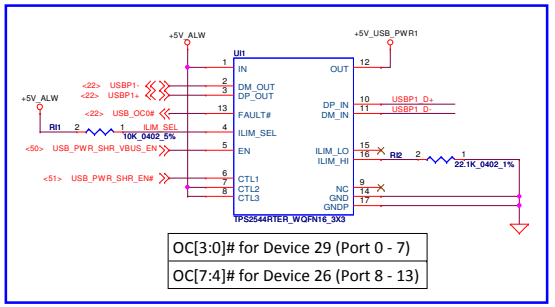
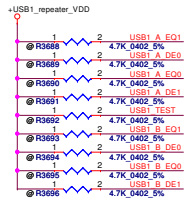
Remove TPS2560

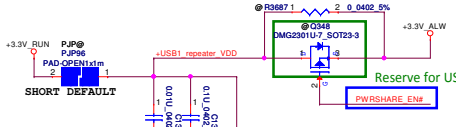




OC[3:0]# for Device 29 (Port 0 - 7)
OC[7:4]# for Device 26 (Port 8 - 13)

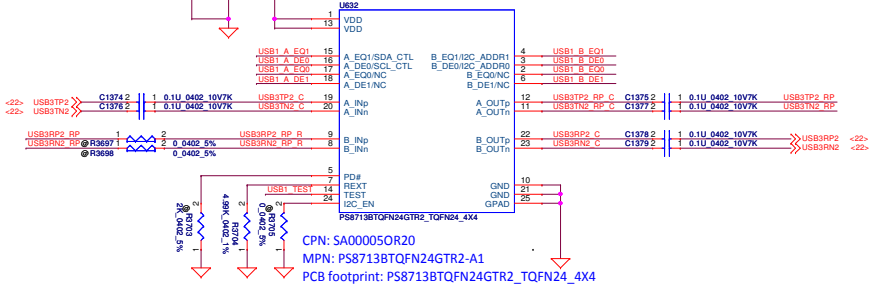
Remove SLG55594





Reserve for USB3 reconnect issue from S3 to S0

LInk CIS ok



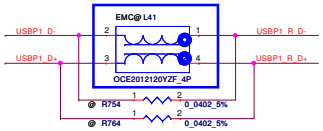
CPN: SA00005OR20
MPN: PS8713BTQFN24GTR2-A1
PCB footprint: PS8713BTQFN24GTR2_TQFN24_4X4

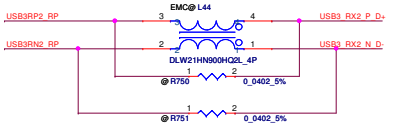
Difference with Diesel

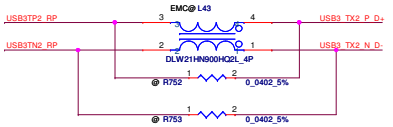
Parade_PS8713B

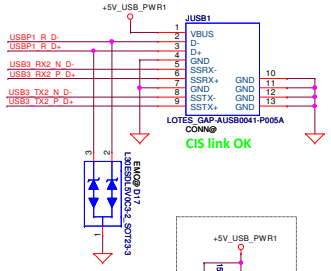
A_EQ0	A_EQ1	B_EQ0	B_EQ1	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 4.5dB
1	0	1	0	loss up to 13dB
1	1	1	1	loss up to 7.5dB

Both A_EQ&B_EQ have internal pull-down 150k

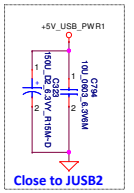






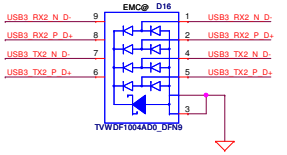


CIS link OK



Close to JUSB2

For ESD request

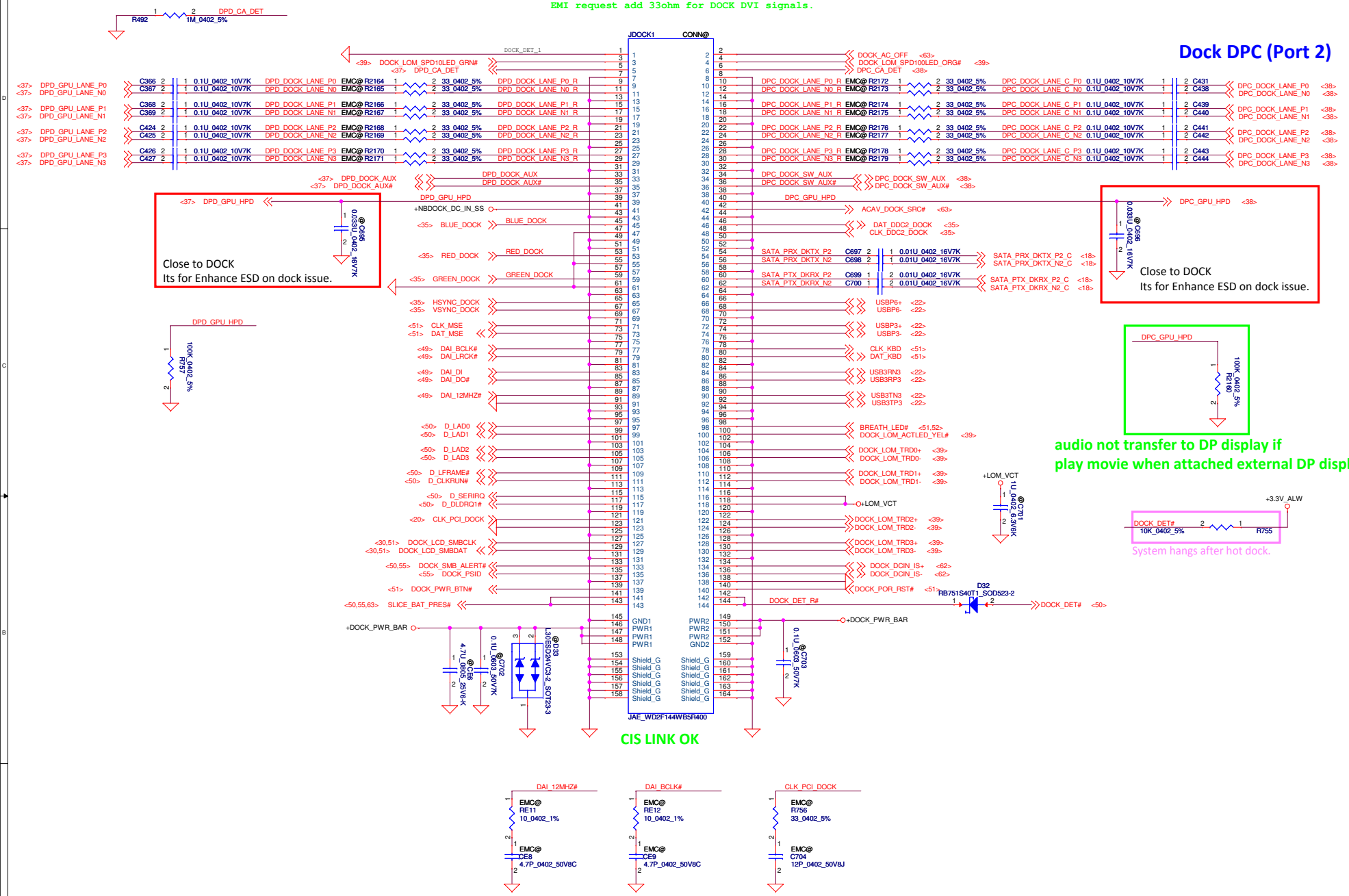


Compal Electronics, Inc.

Title	USB3.0	
Size	Document Number: LA-B541P	Rev: 0.1
Date: Monday, January 13, 2014	Sheet 47 of 67	

EMI request add 33ohm for DOCK DVI signals.

Dock DPC (Port 2)



Compal Electronics, Inc.

Title: Docking

Size | Document Number: LA-B541P | Rev: 0.1

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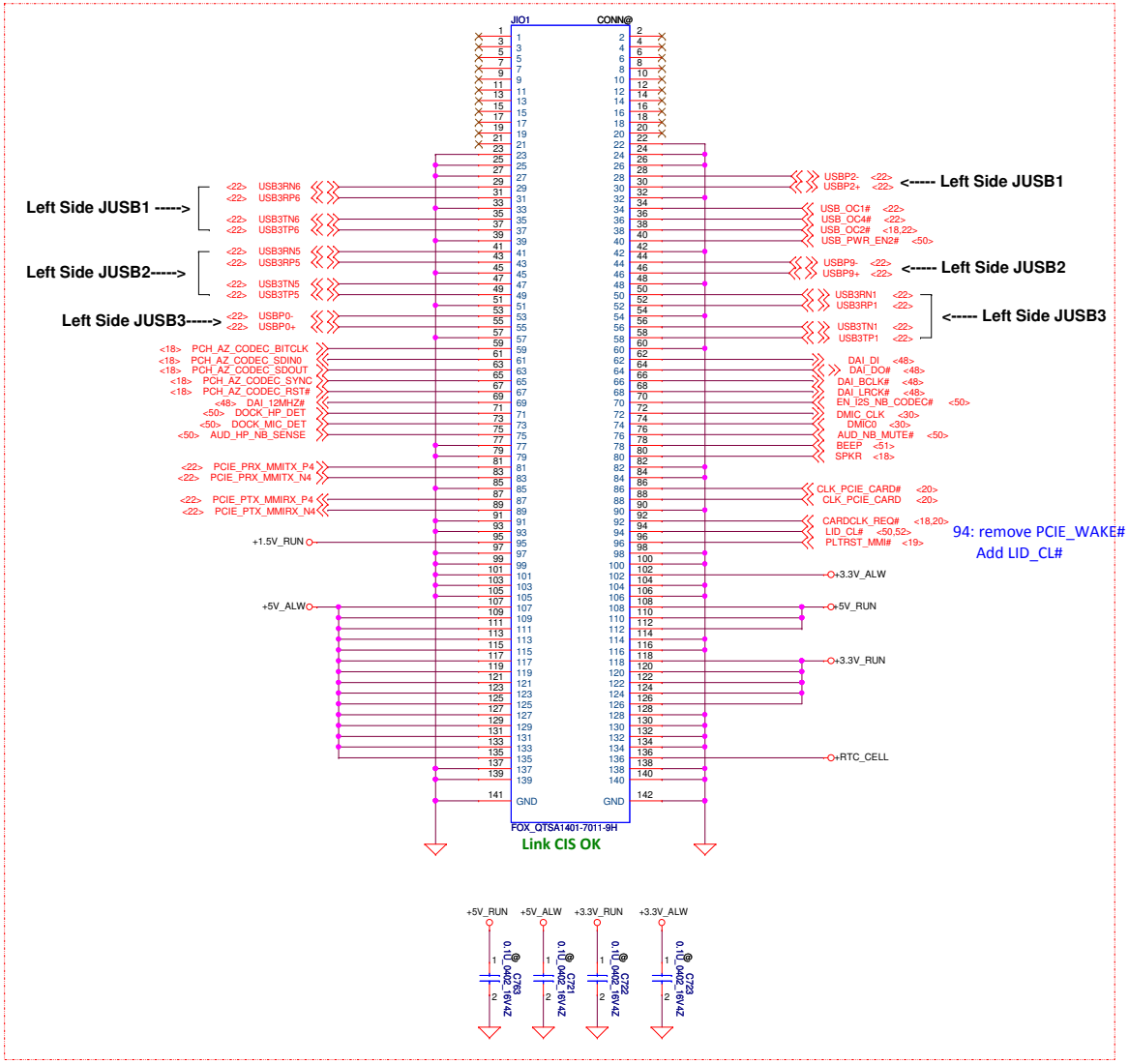
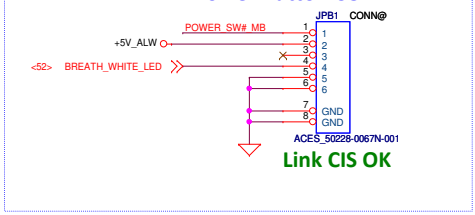
Difference with Diesel



Difference with Diesel

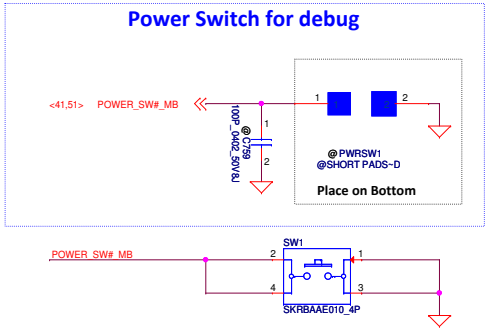
WireLess ON/OFF CONN

Power Button CONN



Link CIS OK

Power Switch for debug



Compal Electronics, Inc.

Title: IO / PWR Button

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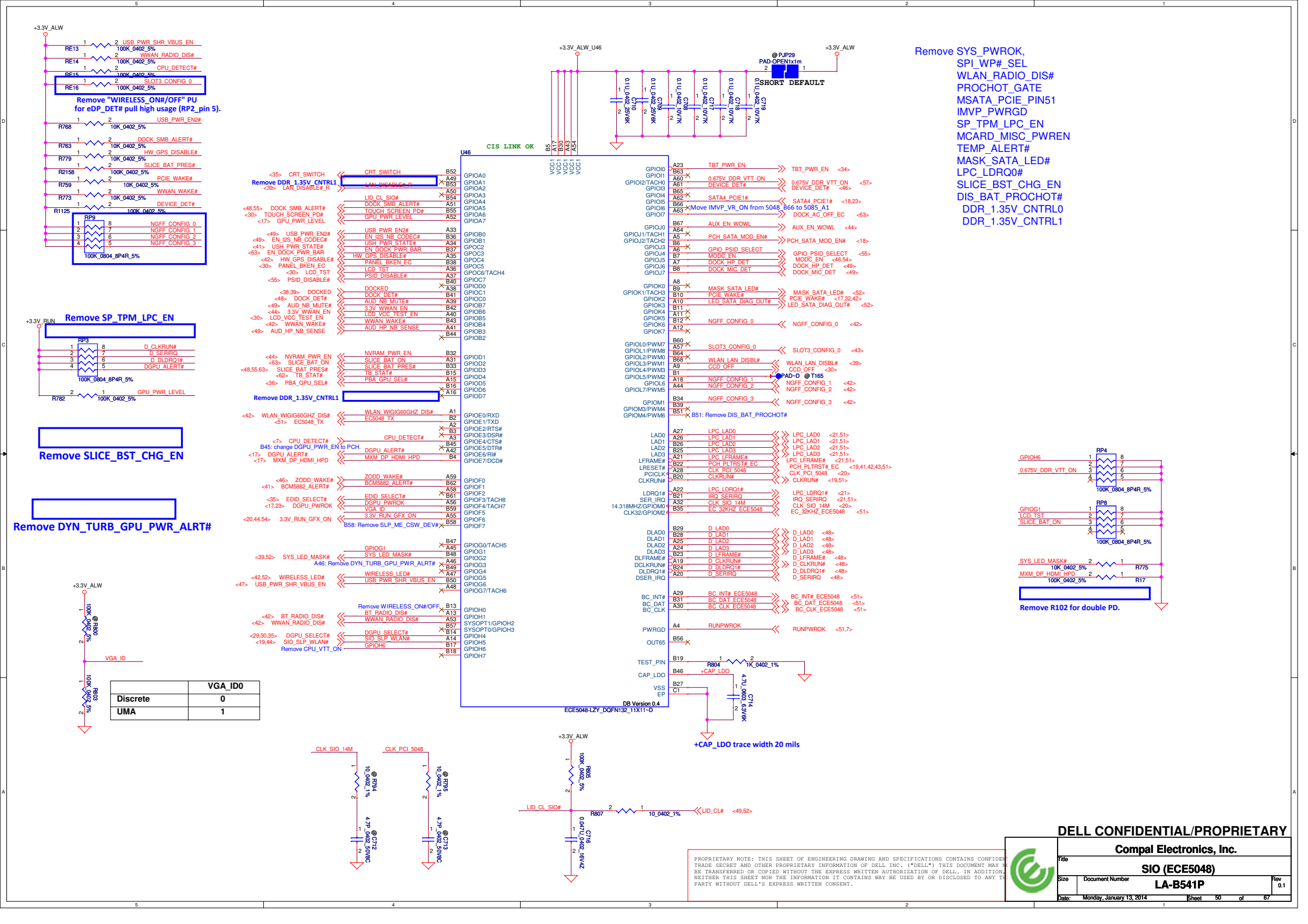
Date: Monday, January 13, 2014 | Sheet 49 of 67



	VGA_ID0
Discrete	0
UMA	1

Remove LCD_SMBDAT,
LCD_SMBCLK,
CARD_SMBDAT
CARD_SMBCLK
VOL_MUTE
EMC4021_BC_DAT
EMC4021_BC_CLK
1.35V_SUS_PWRGD
VOL_DOWN
CPU1.5V_S3_GATE
SYSTEM_ID
HOST_DEBUG_RX
EC_WAKE#
1.05V_A_PWRGD
DYN_TUR_CURRNT_SET#
EMC4021_BC_INT#

remove EC wake circuit.

remove "HOST_DEBUG_RX" PU (5085_B46)

remove "VOL_MUTE" PU
remove "VOL_DOWN" PU
remove "VOL_UP" PU

remove "CPU1.5V_S3_GATE" PD (5085_A36)

CIS LINK OK

By pass PROCHOT CKT.

remove "DYN_TUR_CURRNT_SET#" PU (5085_A35)

SHORT DEFAULT

Place close pin A21

Place close pin A29

32 KHz Clock

ESR <2ohms

1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings

C292 Place near U51.A48

C1343, C1350, C1351, C1346 Place near U51

Remove THERMATRIP3# CKT.

R866 close to U51 at least 250mils

Rest=1.33k, Tp=93degree

R875	C744	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
4.3K	4700p	***
2K	4700p	***
1K	4700p	A00

BOARD_ID rise time is measured from 5%~68%.

DP1/DN1 for CPU OTP on Q16, place Q16 close to CPU and C273 close to Q16.
DN1a/DP1a for CPU VR on Q26, place Q26 close to CPU and C339 close to Q26

DP2/DN2 for MXM(TOP side) on Q27, place Q27 close to MXM(TOP side) and C291 close to Q27.
DN2a/DP2a for MXM(BOT) on Q17, place Q17 close to MXM(BOT) and C340 close to Q17

DP3/DN3 for SODIMM(TOP) on Q14, place Q14 close to SODIMM(TOP) and C272 close to Q14

DP4/DN4 for WiGig on Q15, place Q15 close to WiGig and C288 close to Q15

Channel	Location
DP1/DN1	CPU OTP
DP1a/DN1a	CPU VR
DP2/DN2	MXM(TOP)
DP2a/DN2a	MXM(BOT)
DP3/DN3	DIMM(TOP)
DP4/DN4	WiGig

Difference with Diesel

Difference with Diesel

remove SYSTEM_ID (5085_A10)

remove Q52

CIS link OK

Compal Electronics, Inc.
KBC (MEC5085)
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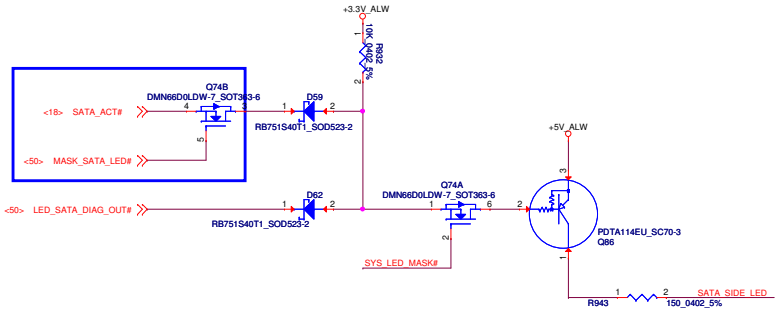
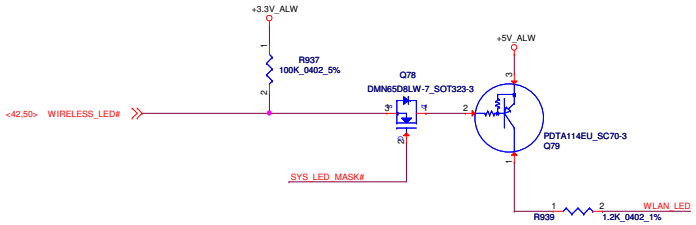
Difference with Diesel

HDD LED

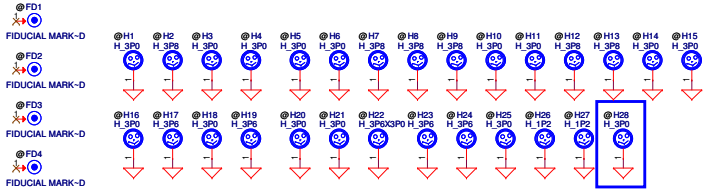


WWAN/WLAN LED

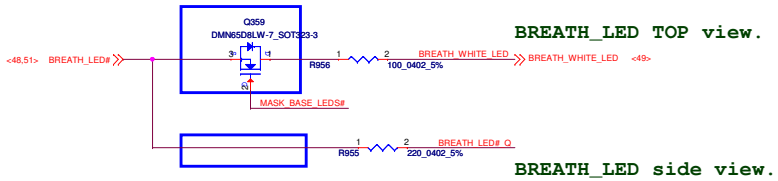


LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark



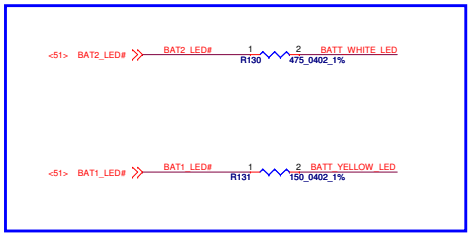
Breath LED

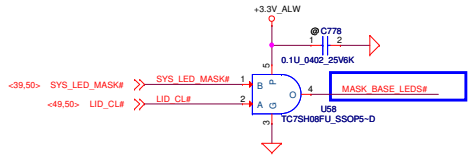


BREATH_LED TOP view.

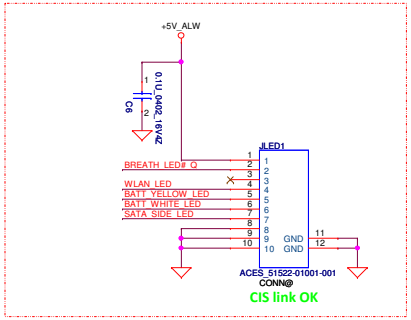
BREATH_LED side view.

BATT LED





Difference with Diesel



CIS link OK

Compal Electronics, Inc.		
Title: LED / Screw hole		
Size	Document Number: LA-B541P	Rev: 0.1
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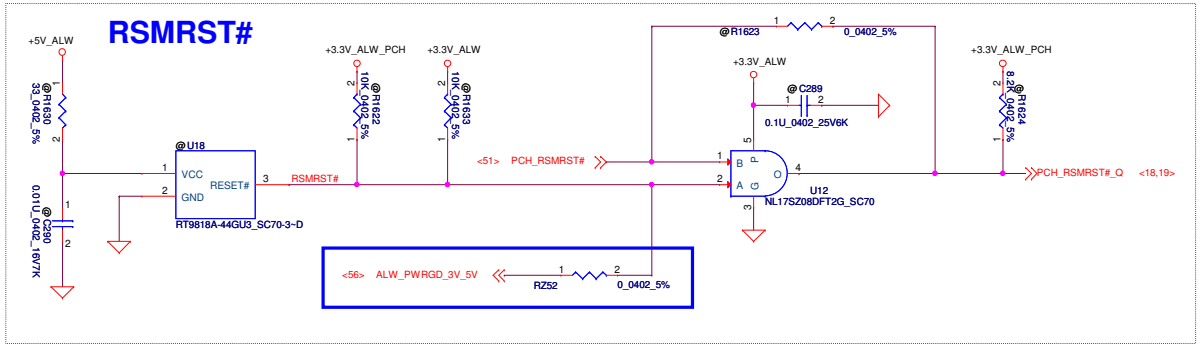
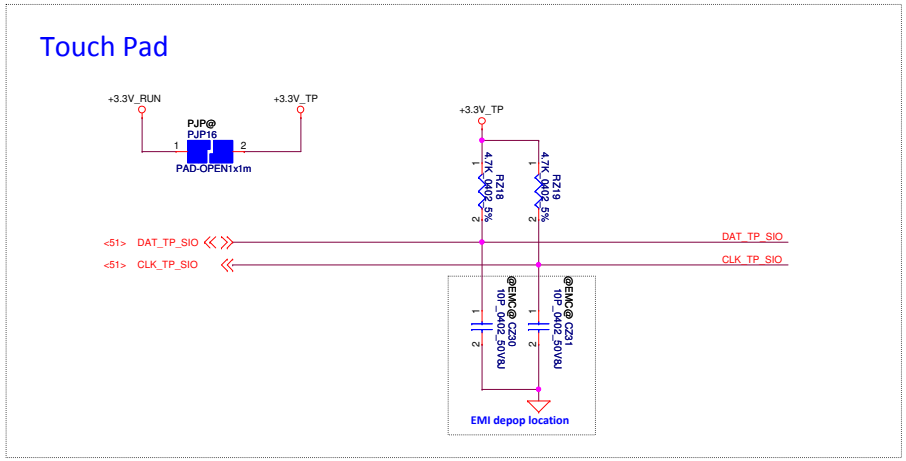
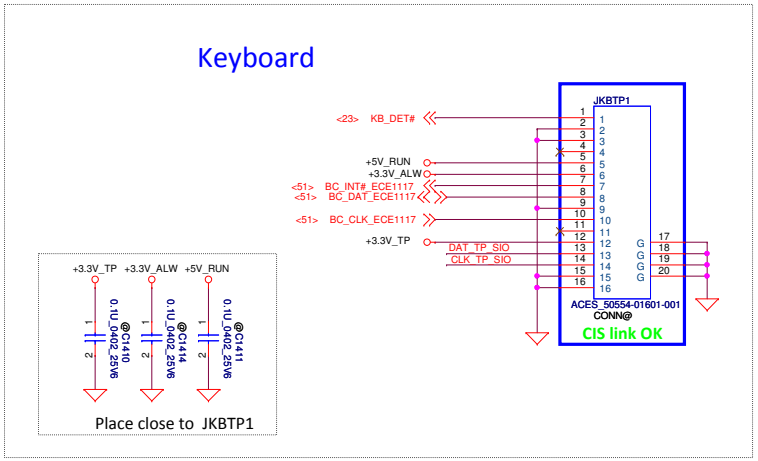


Remove RSMRST cost down circuit.





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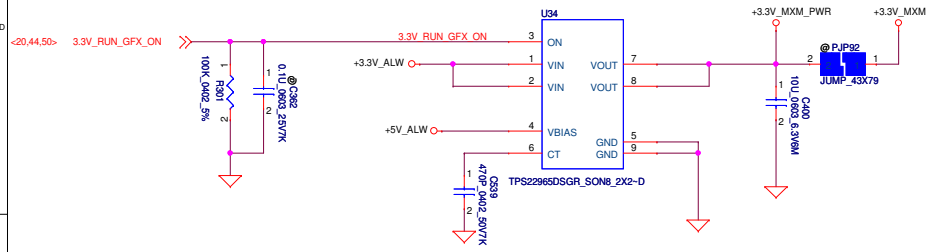
Compal Electronics, Inc.

Title: KB / TP / RSMRST#

Size | Document Number: LA-B541P | Rev: 0.1

Date: Monday, January 13, 2014 | Sheet 53 of 67

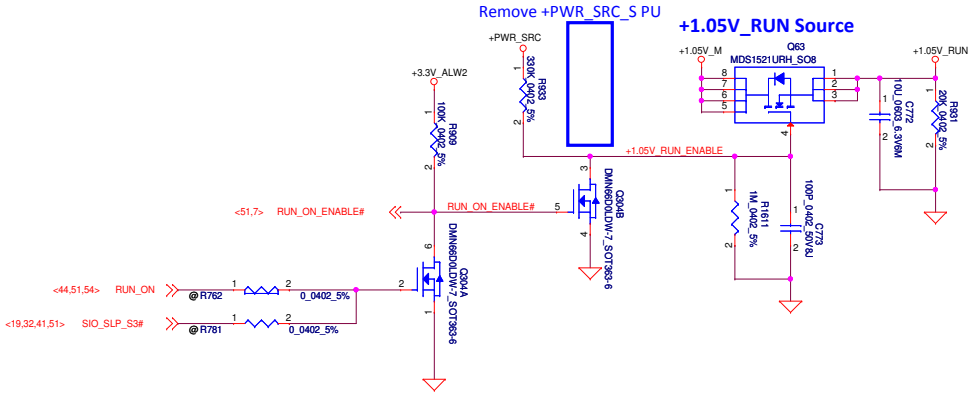
+3.3V_ALW to +3.3V_MXM



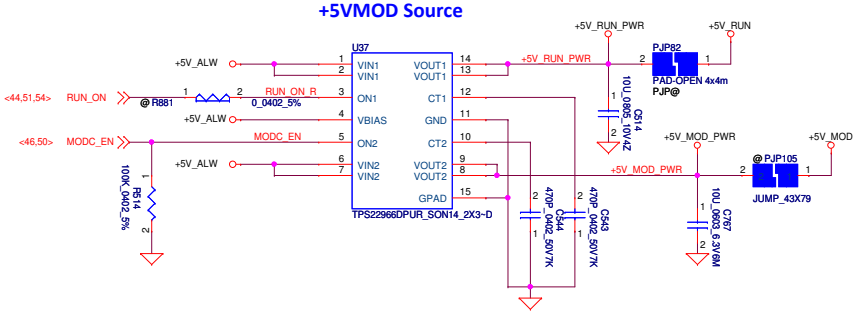
Combine +3.3V_SSD and +5V_MXM into M.2 card power control page

Remove +PWR_SRC_S PU

+1.05V_RUN Source



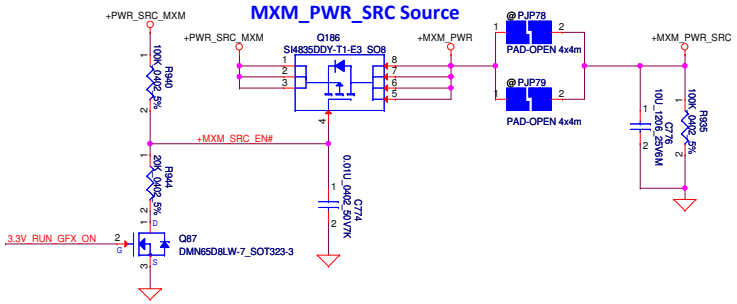
+5V_RUN Source
+5VMOD Source

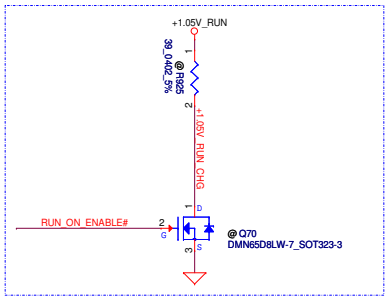


Combine +3.3V_WLAN and +3.3V_RUN into M.2 card power control page.

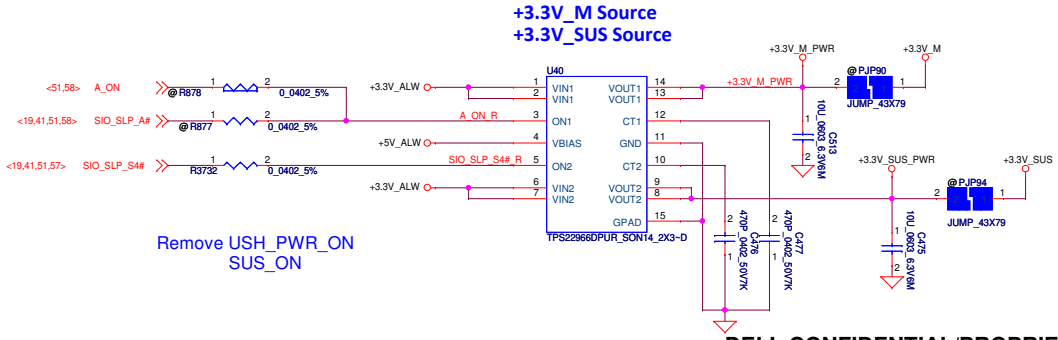
Combine +3.3V_LAN and +3.3V_ALW_PCH into LAN page

MXM_PWR_SRC Source





+3.3V_M Source
+3.3V_SUS Source



Remove USH_PWR_ON
SUS_ON

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: Power Control		
Size	Document Number: LA-B541P	Rev: 0.1
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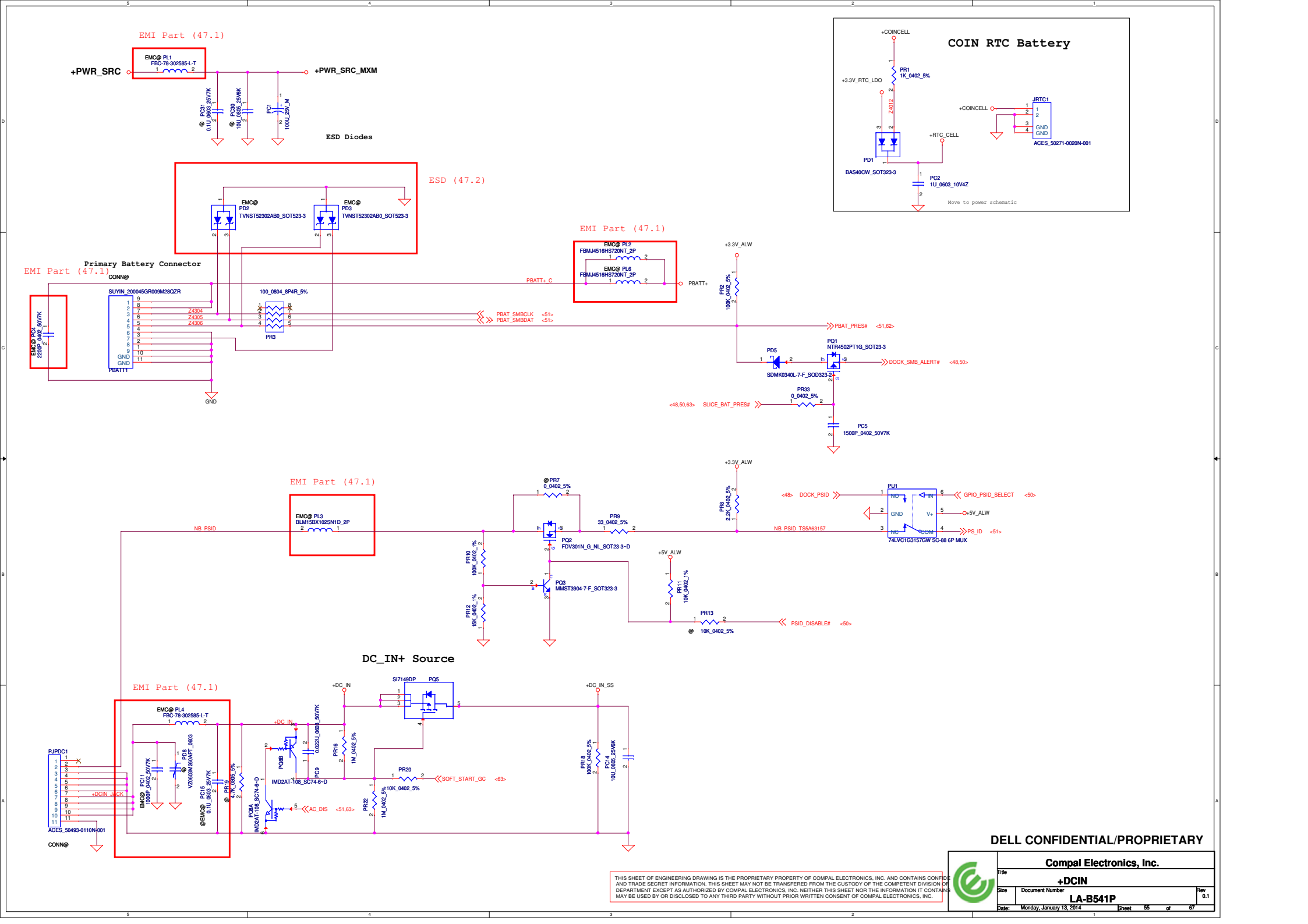
EMI Part (47.1)
+PWR_SRC
EMC@ PL1
FBC-78-302585-L-T
+PWR_SRC_MXM
PC31
0.1U_0603_25V7K
PC30
10U_0805_25V6K
PC1
100U_25V_M
ESD Diodes
ESD (47.2)
EMC@
PD2
TVNST52302AB0_SOT523-3
EMC@
PD3
TVNST52302AB0_SOT523-3
COIN RTC Battery
+COINCELL
PR1
1K_0402_5%
+3.3V_RTC_LDO
PD1
BAS40CW_SOT323-3
+RTC_CELL
PC2
1U_0603_10V4Z
Move to power schematic
JRTC1
ACES_50271-0020N-001
Primary Battery Connector
EMI Part (47.1)
CONN@
SUYIN_200045GR009M28QZR
PBAT11
EMC@ PC4
22KP_0402_50V7K
100_0804_8P4R_5%
PR3
Z4304
Z4305
Z4306
GND
EMI Part (47.1)
EMC@ PL2
FBMJ4516HS720NT_2P
EMC@ PL6
FBMJ4516HS720NT_2P
PBATT+_C
PBATT+
+3.3V_ALW
PR2
100K_0402_5%
PBAT_SMBCLK <51>
PBAT_SMBDAT <51>
PBAT_PRES# <51,62>
PD5
SDMK0340L-7-F_SOD323-2
PQ1
NTR4502PT1G_SOT23-3
DOCK_SMB_ALERT# <48,50>
PR33
0_0402_5%
<48,50,63> SLICE_BAT_PRES#
PC5
1500P_0402_50V7K
EMI Part (47.1)
EMC@ PL3
BLM15BX102SN1D_2P
NB_PSID
@PR7
0_0402_5%
PR9
33_0402_5%
PQ2
FDV301N_G_NL_SOT23-3-D
PR8
2.2K_0402_5%
<48> DOCK_PSID
PU1
74LVC1G3157GW SC-88 6P MUX
GPIO_PSID_SELECT <50>
+5V_ALW
PS_ID <51>
NB_PSID_TS5A63157
PR10
100K_0402_1%
PR12
15K_0402_1%
PQ3
MMST3904-7-F_SOT323-3
PR11
10K_0402_1%
PR13
@ 10K_0402_5%
PSID_DISABLE# <50>
DC_IN+ Source
EMI Part (47.1)
EMC@ PL4
FBC-78-302585-L-T
PJPDC1
ACES_50493-0110N-001
CONN@
+DCIN_JACK
PC11
1000P_0402_50V7K
PD8
@
V20603M280APT_0603
PC15
@EMC@ 0.1U_0603_25V7K
PR19
@ 4.7K_0805_5%
PQ8A
IMD2AT-108_SC74-6-D
PQ8B
IMD2AT-108_SC74-6-D
0.022U_0603_50V7K
PC9
PR16
1M_0402_5%
PR20
10K_0402_5%
SOFT_START_GC <63>
PR22
1M_0402_5%
AC_DIS <51,63>
+DC_IN
SI7149DP
PQ5
+DC_IN_SS
PR18
100K_0402_5%
PC14
10U_0805_25V6K
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Compal Electronics, Inc.
+DCIN
LA-B541P
Monday, January 13, 2014
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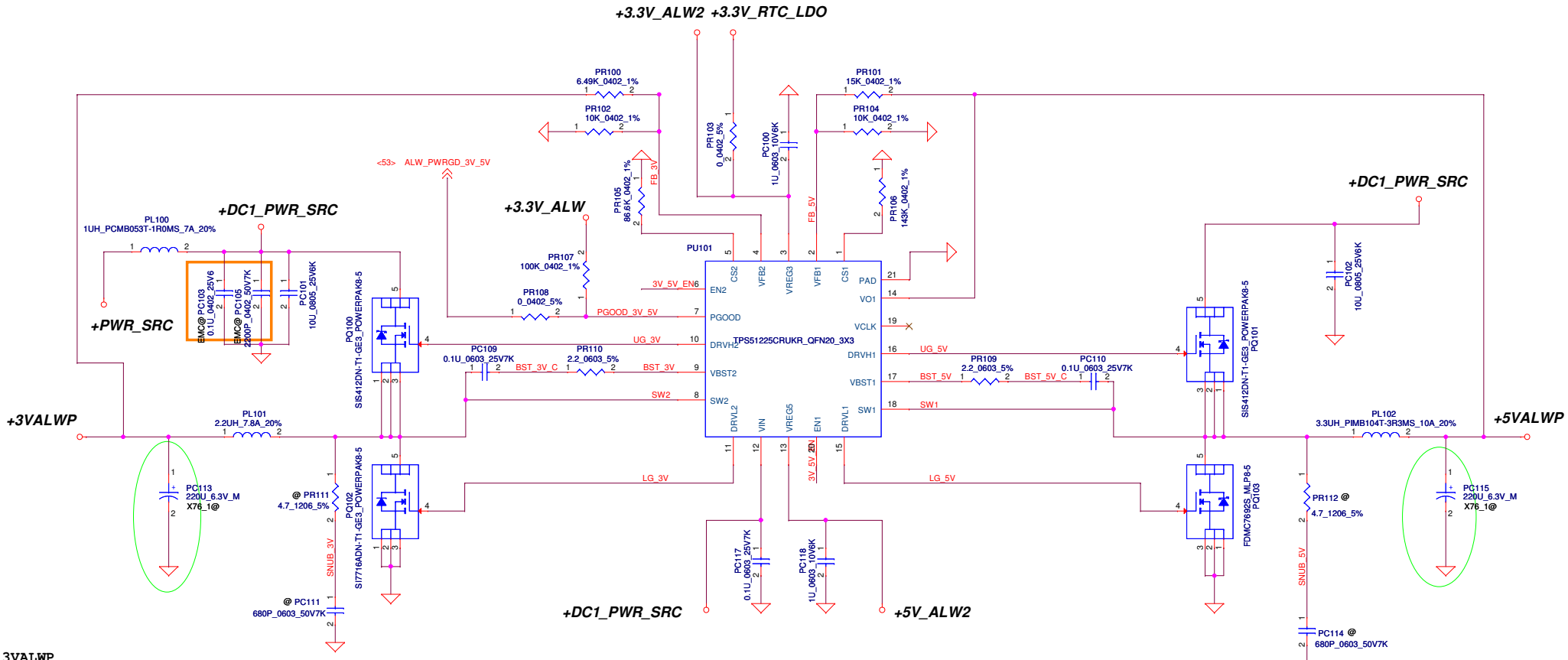

3VALWP
Ripple voltage –
Static load 3% / Dynamic load 5%
Frequency 350kHz
TDC 4.5 A
Peak Current 6.5 A
OCP current 7.8 A

	TYP	MAX
H/S Rds(on)	24mohm ,	30mohm
L/S Rds(on)	13.5mohm ,	16.5mohm

Choke DCR:15.5
Bulk cap ESR 15mohm

5VALWP
Ripple voltage –
Static load 3% / Dynamic load 5%
Frequency 300kHz
TDC 7.8 A
Peak Current 11.15 A
OCP current 13.38 A

	TYP	MAX
H/S Rds(on)	24mohm ,	30mohm
L/S Rds(on)	10.8mohm ,	13.6mohm

Choke DCR Max:11.8mohm
Choke Ityp:10A / Isat:16A
Bulk cap ESR 15mohm

Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

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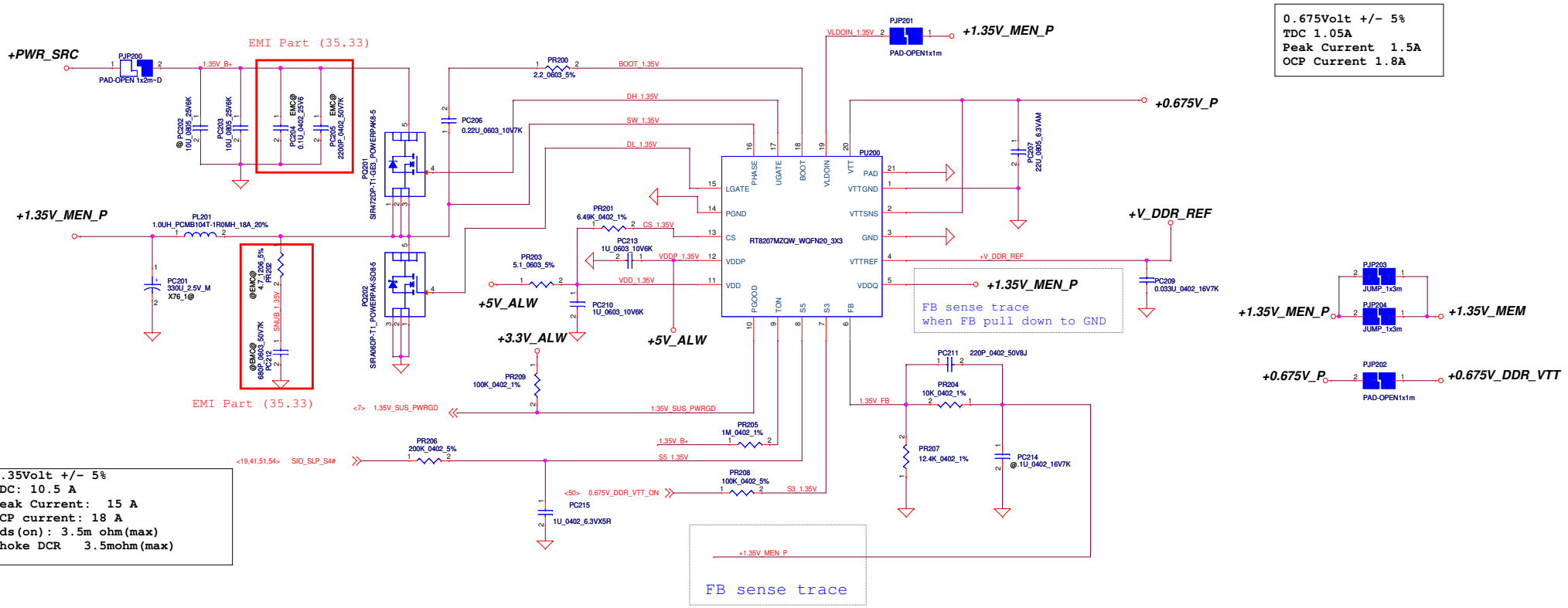

0.675Volt +/- 5%
TDC 1.05A
Peak Current 1.5A
OCP Current 1.8A

1.35Volt +/- 5%
TDC: 10.5 A
Peak Current: 15 A
OCP current: 18 A
Rds(on): 3.5m ohm(max)
Choke DCR 3.5mohm(max)

Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off(Hi-Z)
S0	H	H	on	on	on

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: 1.35VP/0.675VSP

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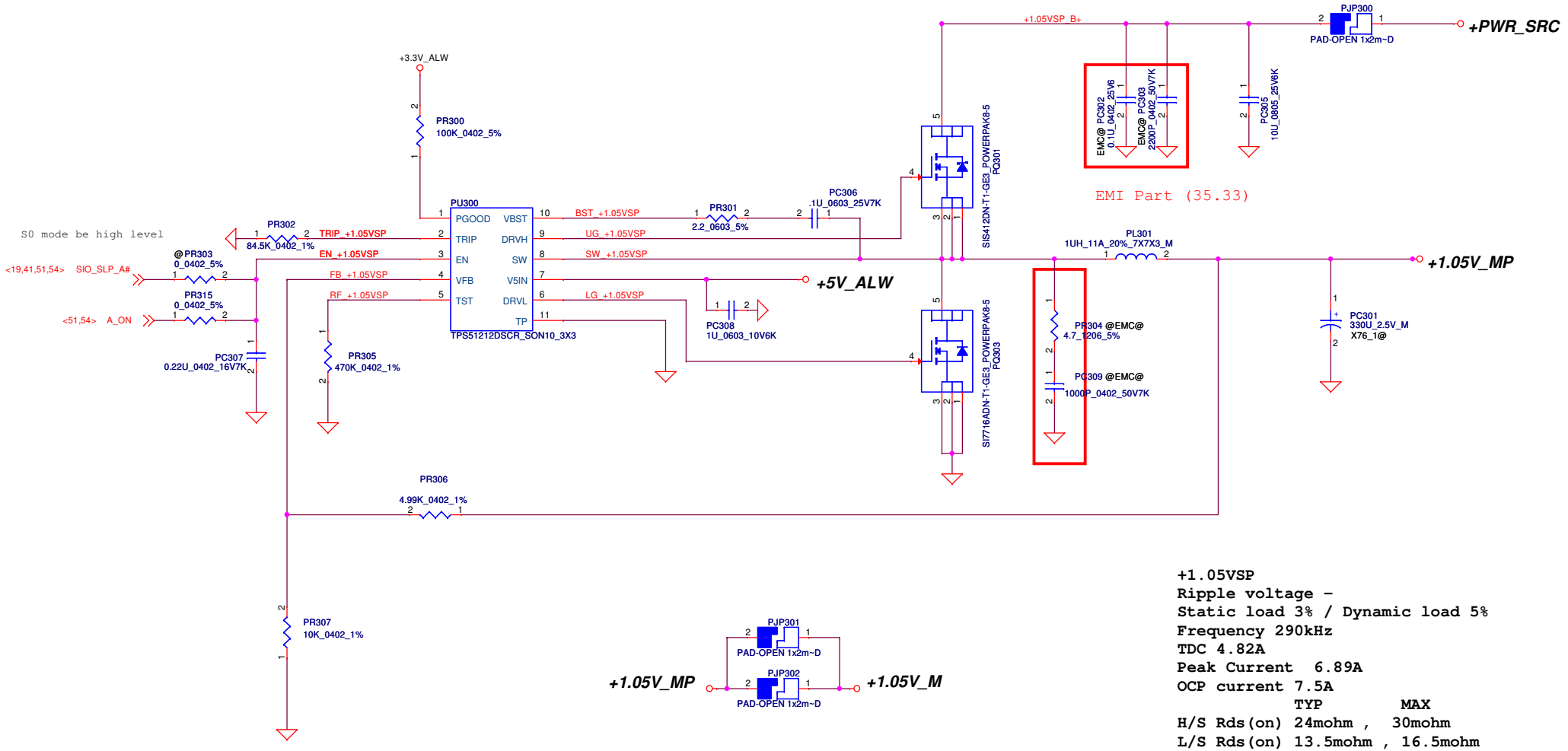

+1.05VSP
Ripple voltage –
Static load 3% / Dynamic load 5%
Frequency 290kHz
TDC 4.82A
Peak Current 6.89A
OCP current 7.5A

	TYP	MAX
H/S Rds(on)	24mohm ,	30mohm
L/S Rds(on)	13.5mohm ,	16.5mohm

Choke DCR 11mohm
Bulk cap ESR 17mohm

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Title	+1.05V_M	
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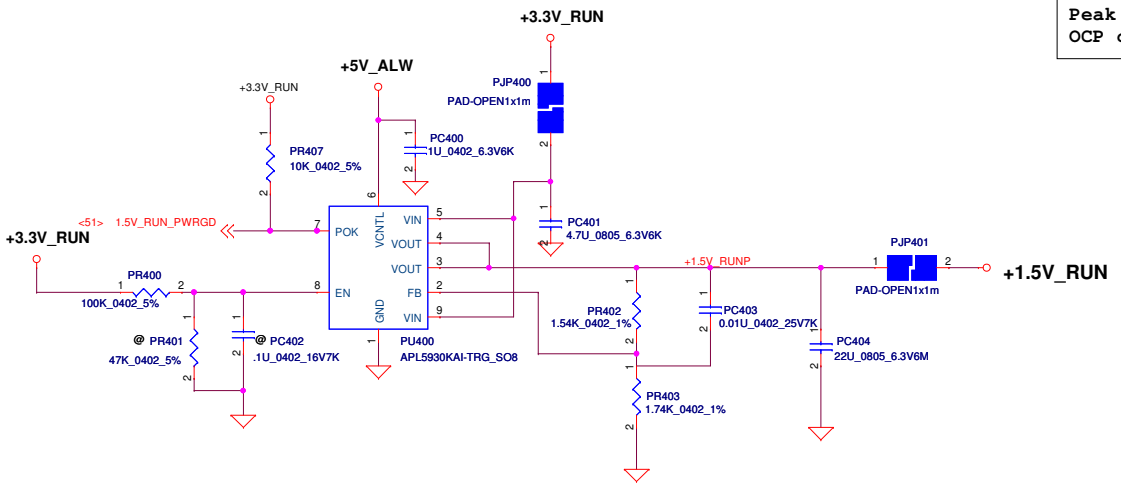
1.5Volt +/- 5%
TDC: 0.15A
Peak Current: 0.2 A
OCP current: 4 A



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Title	+1.5V_RUN	
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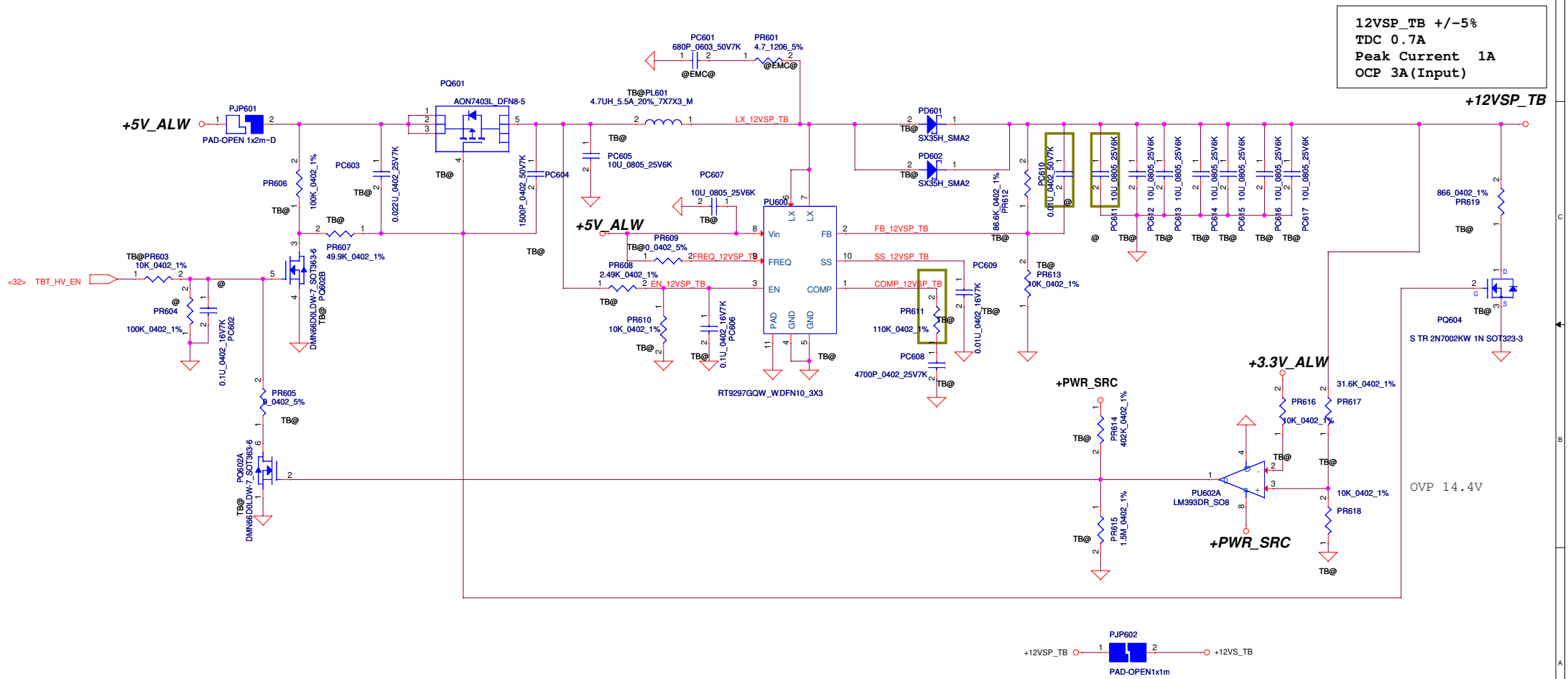

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Title: 12VS_TB

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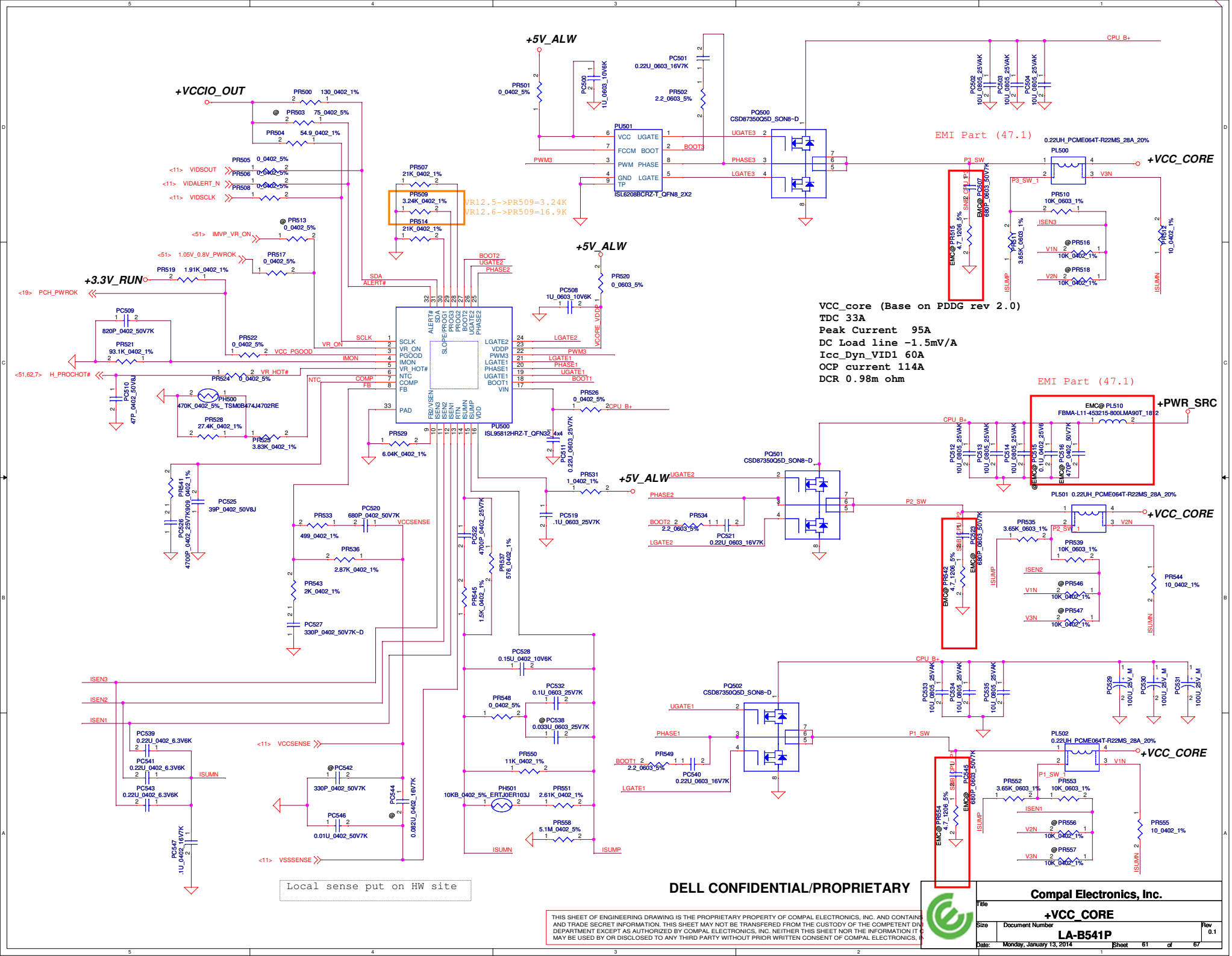
+VCCIO_OUT
+5V_ALW
+3.3V_RUN
+VCC_CORE
+PWR_SRC
PU500 ISL95812HRZ-T_QFN32_4x4
PU501 ISL6208BCRZ-T_QFN8_2X2
PQ500 CSD87350Q5D_SON8~D
PQ501 CSD87350Q5D_SON8~D
PQ502 CSD87350Q5D_SON8~D
PL500 0.22UH_PCME064T-R22MS_28A_20%
PL501 0.22UH_PCME064T-R22MS_28A_20%
PL502 0.22UH_PCME064T-R22MS_28A_20%
EMI Part (47.1)
EMI Part (47.1)
VR12.5->PR509=3.24K
VR12.6->PR509=16.9K
VCC_core (Base on PDDG rev 2.0)
TDC 33A
Peak Current 95A
DC Load line -1.5mV/A
Icc_Dyn_VID1 60A
OCP current 114A
DCR 0.98m ohm
Local sense put on HW site
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+VCC_CORE
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Iada=0~12.3A240W)

ADP_I = 20*Iadapter*Rsense

EMI Part (47.1)

EMI Part (47.1)

EMI Part (35.33)

AC Det (typ 2.4V)
Max:17.77V
Typ :17.60V
Min :17.42V

Current limit
Charger :5.12A Vilim=1.024V
8 Cell (0.8C)
Max Boost Charger :6.4A, Vilim=0.32V

+DC_IN

CMP_REF=2.3V
+DC_IN>17.6V then ACAV_IN_NB high

+3.3V_ALW

Compal Electronics, Inc.
Title: Charger
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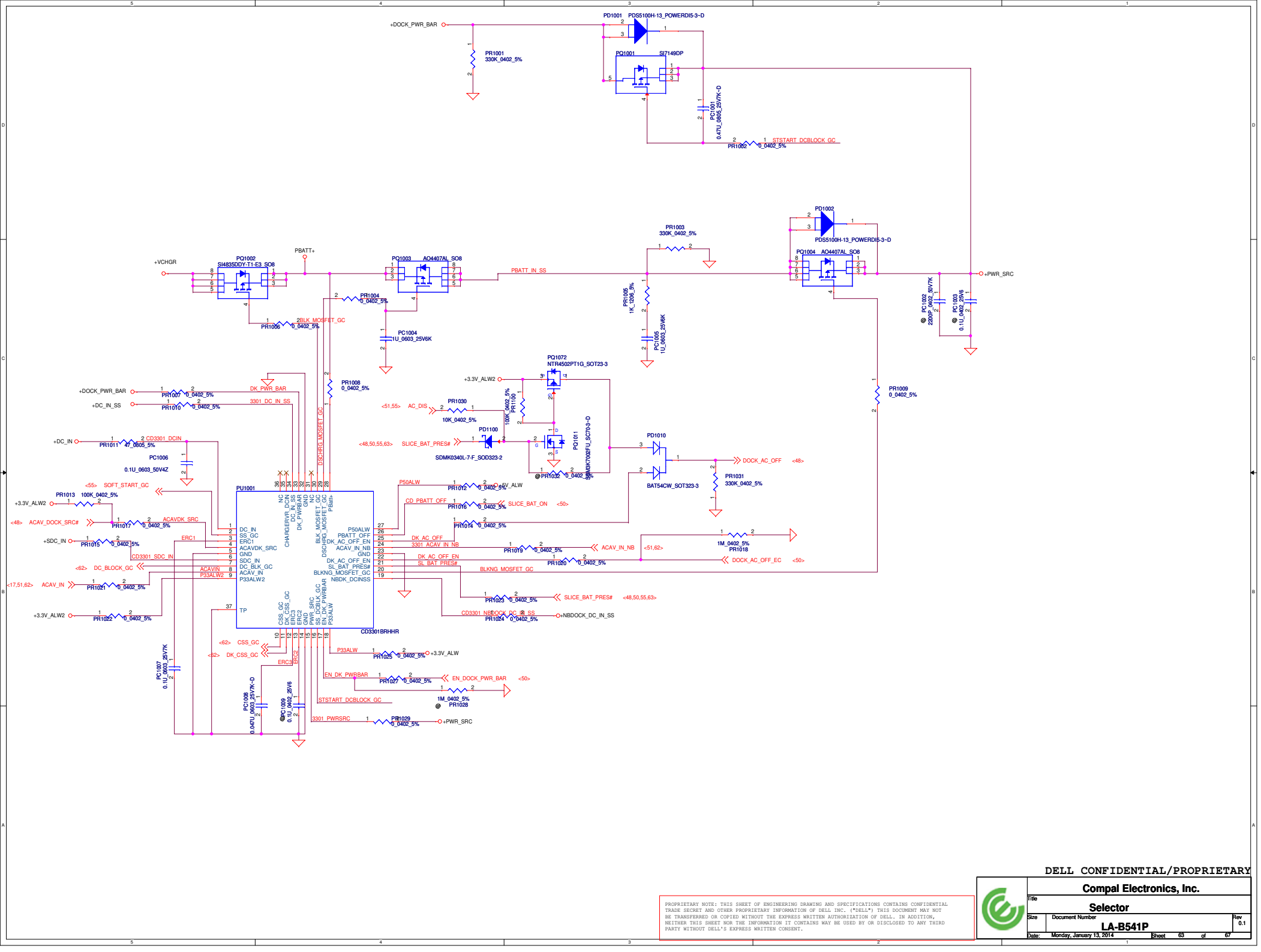

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Compal Electronics, Inc.	
Title	Selector
Size	Document Number: LA-B541P
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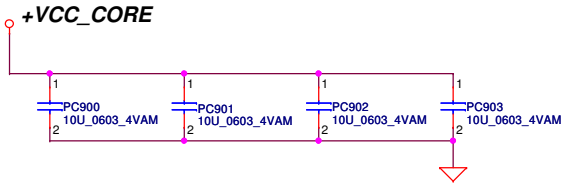
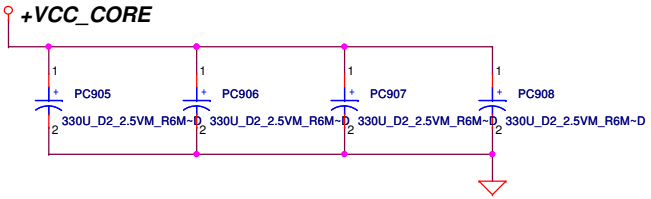
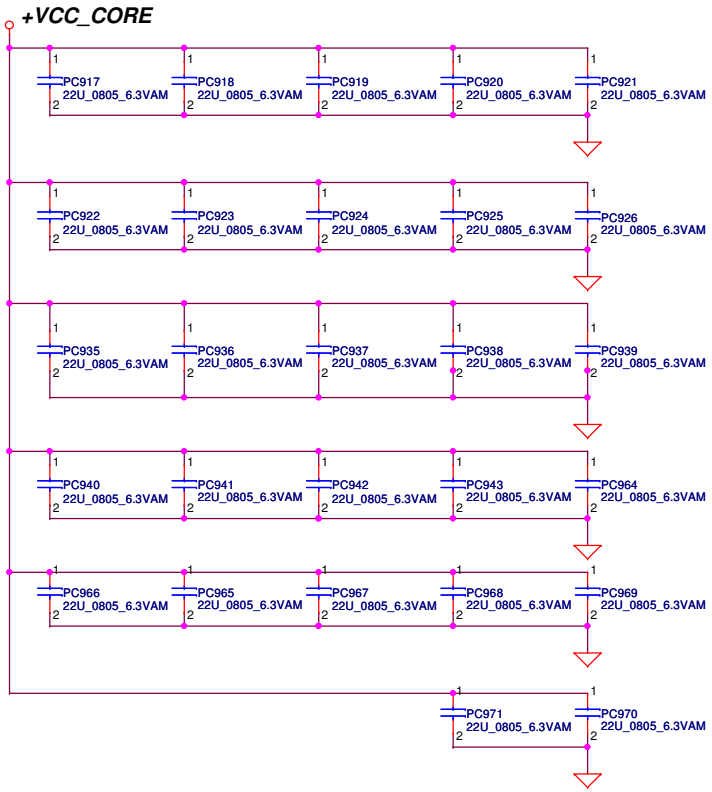
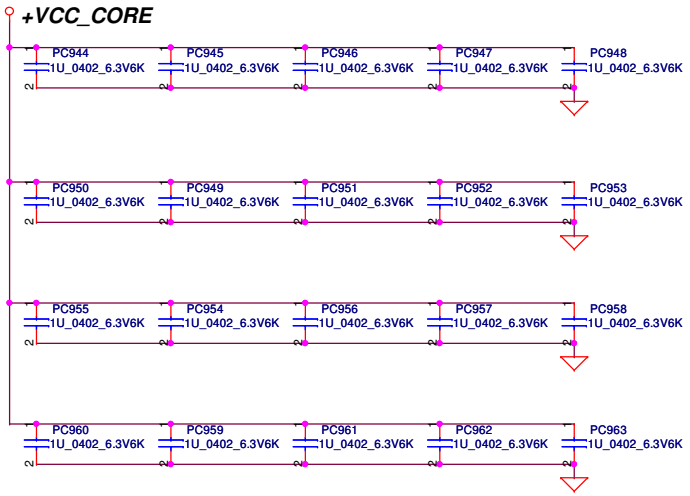
Based on SB PDDG rev 2.0 Table 5-2









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Title: PROCESSOR DECOUPLING

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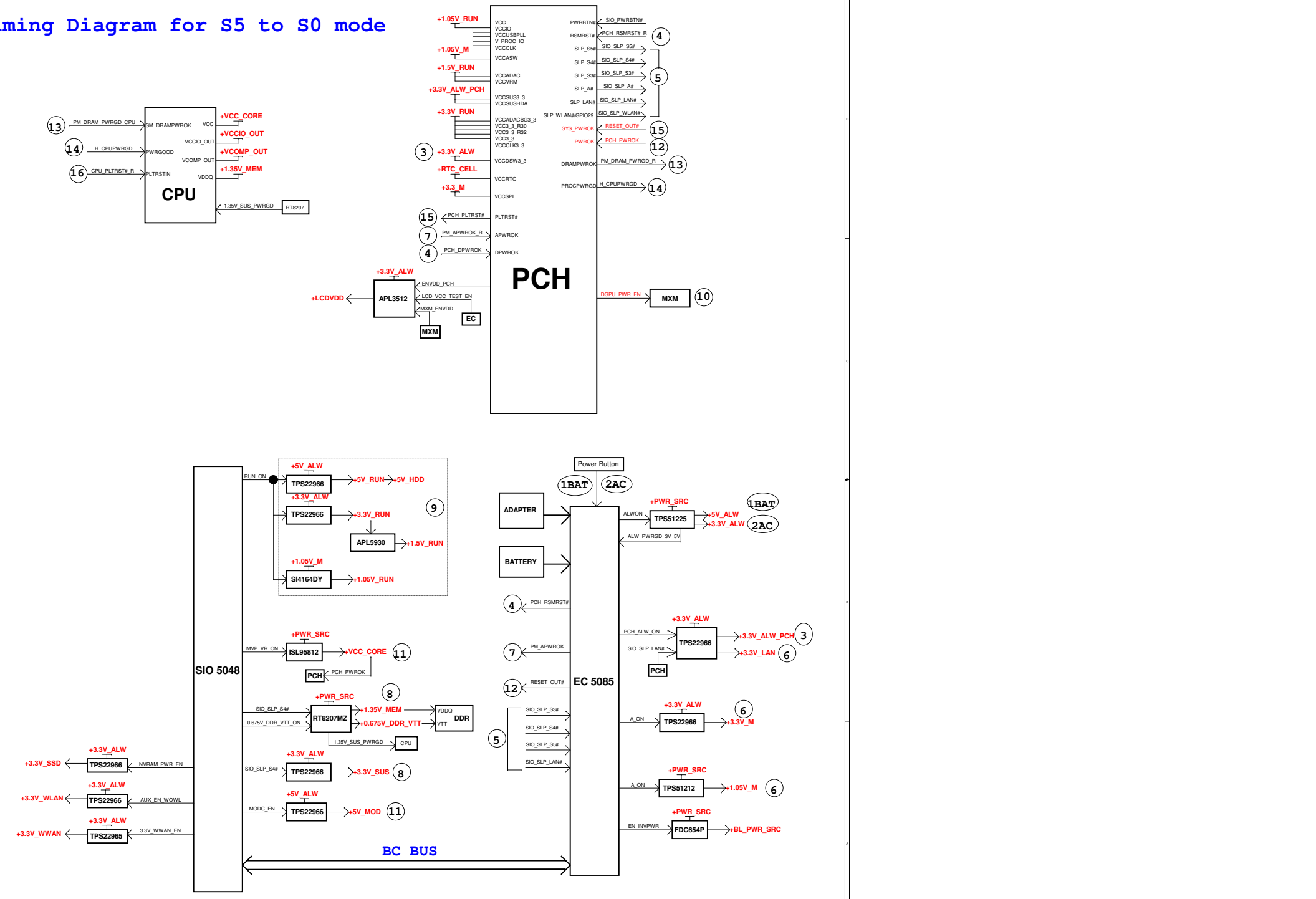
Timing Diagram for S5 to S0 mode



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Title: Power Sequence

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.