

Compal Confidential

JFWXX Schematics Document

Intel Merom Processor with SiSM672MX + DDRII + SiS968 + SiS307LV

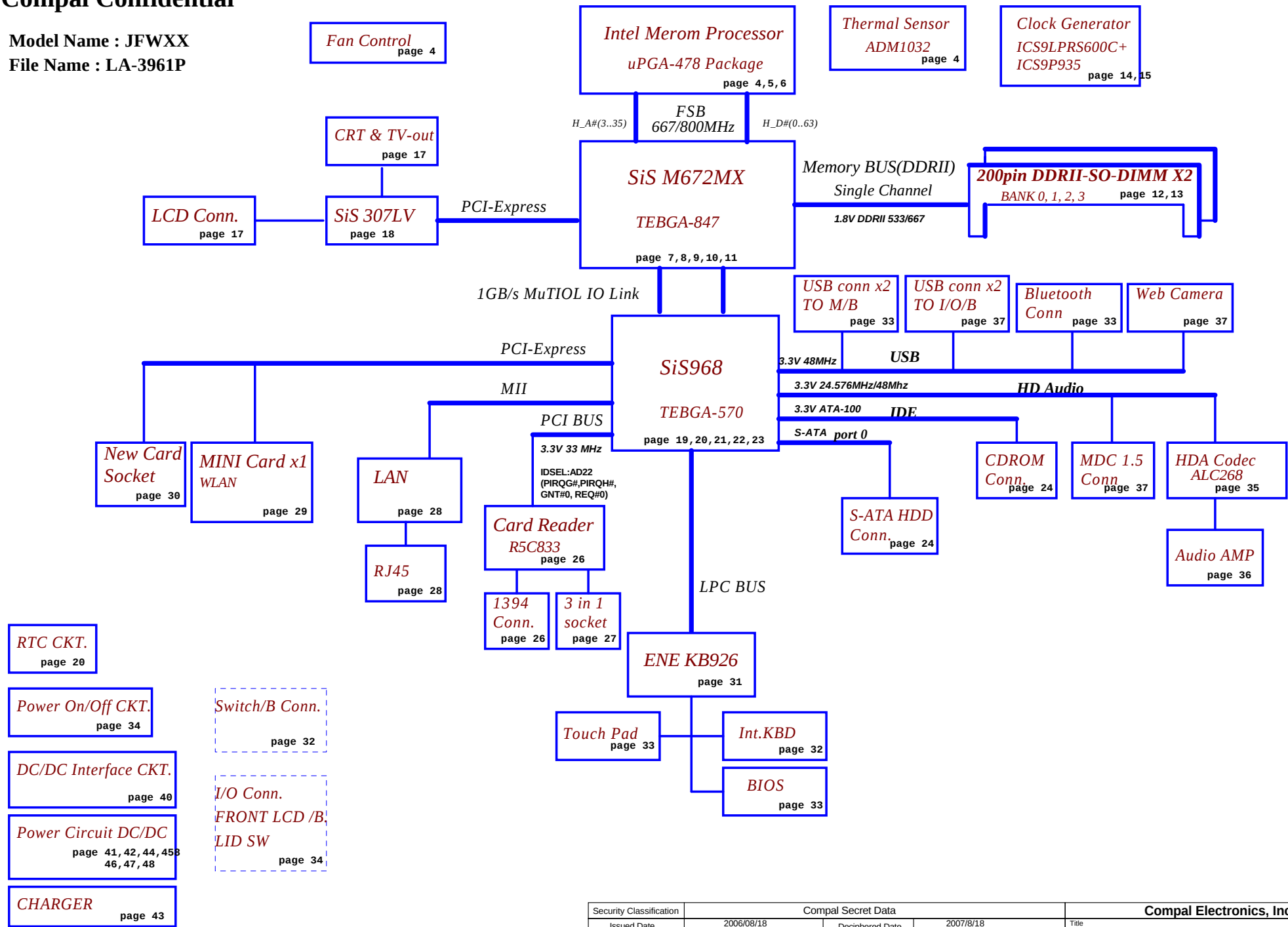
2007 - 09 - 06

REV: 0.3

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Model Name : JFWXX
File Name : LA-3961P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	PROJECT_ID
14W	R424 (Pull low)
15W	NA (Internal Pull High)

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

ICH8M SM Bus address

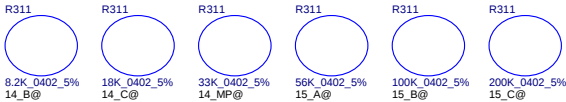
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Ra~ R312

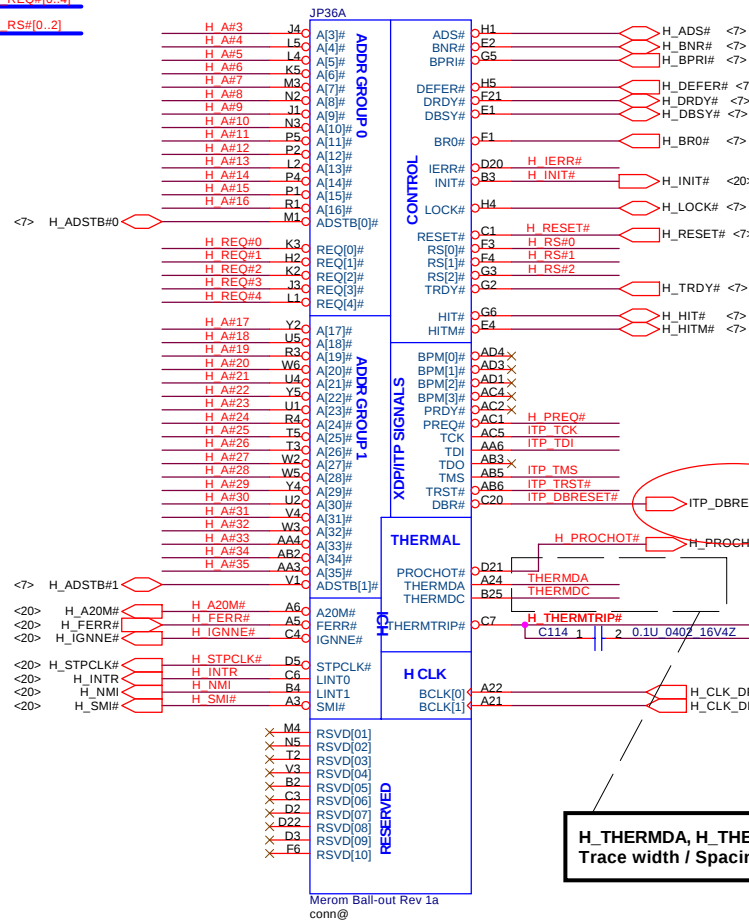
Rb~ R311



Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	Rb BOM Structure
0	0	0 V	0 V	0 V	14_A@
1	8.2K +/- 5%	0.217 V	0.250 V	0.288 V	14_B@
2	18K +/- 5%	0.439 V	0.503 V	0.575 V	14_C@ ✓
3	33K +/- 5%	0.721 V	0.819 V	0.926 V	14_MP@
4	56K +/- 5%	1.054 V	1.185 V	1.325 V	15_A@
5	100K +/- 5%	1.489 V	1.650 V	1.819 V	15_B@
6	200K +/- 5%	2.019 V	2.200 V	2.386 V	15_C@ ✓
7	NC	3.135V	3.300 V	3.465 V	15_MP@

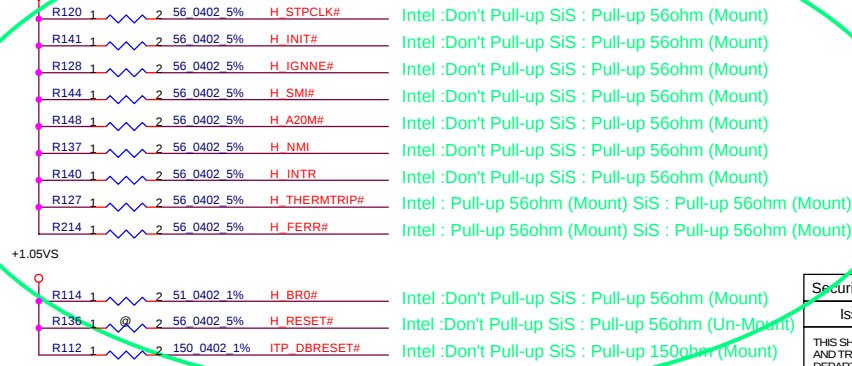
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<7> H_A# [3..35] H_A# [3..35]
<7> H_REQ# [0..4] H_REQ# [0..4]
<7> H_RS# [0..2] H_RS# [0..2]



H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

CPU to SB interface



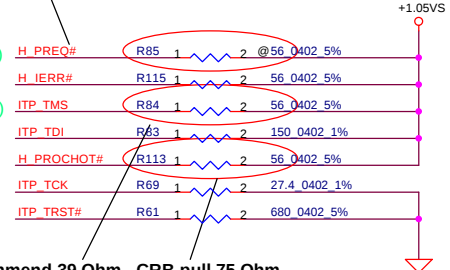
Trace length must short

Place close to CPU within 500mil

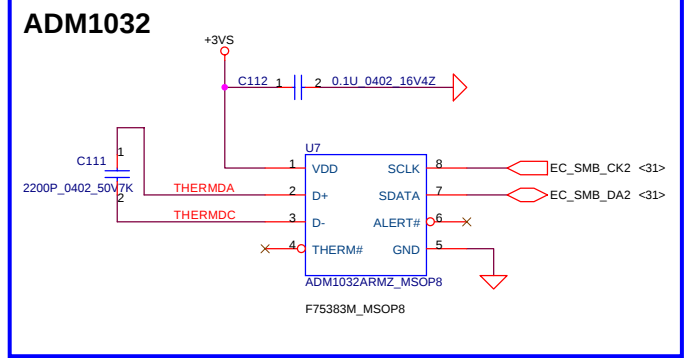
Intel :Pull-up 56ohm (Un-Mount) SiS : Pull-up 56ohm (Mount)

Intel :Pull-up 56ohm (Mount) SiS : Pull-up 54.9ohm (Mount)

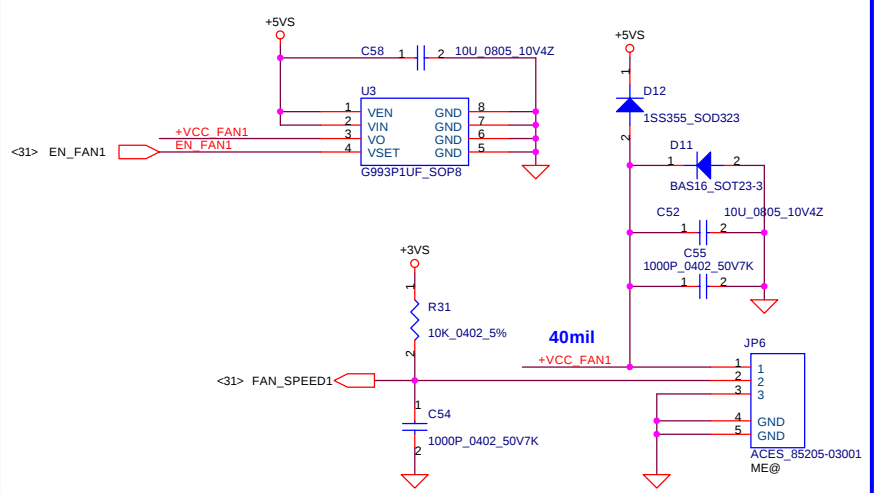
Intel :Pull-up 56ohm (Mount) SiS : Pull-up 75ohm (Mount)



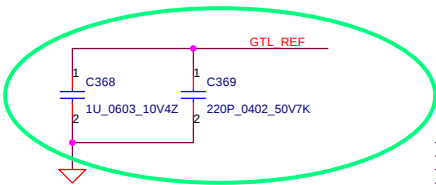
Checklist recommend 39 Ohm CRB pull 75 Ohm



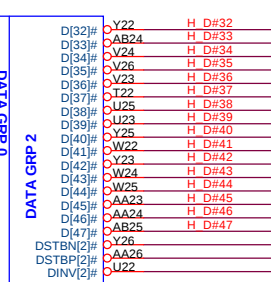
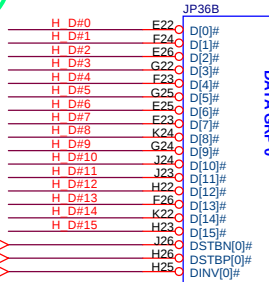
FAN1 Conn



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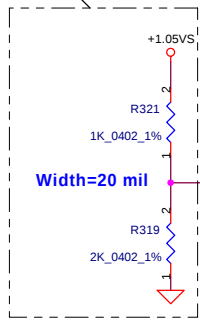
SIS Recommend



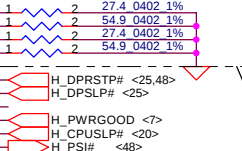
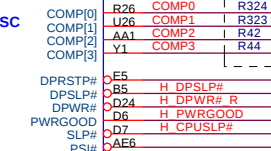
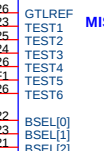
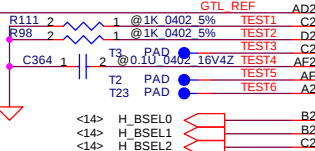
H_D#[0..63] <7>

+CPU_CORE

Close to CPU pin AD26 within 500mils.

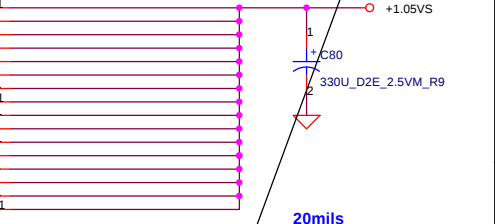


Width=20 mil



+CPU_CORE

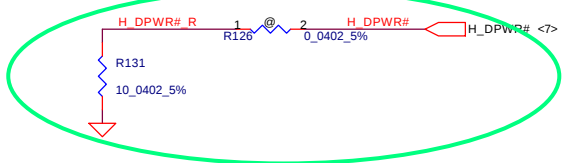
Place this cap more close to B26/C26 rather than 10UF



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

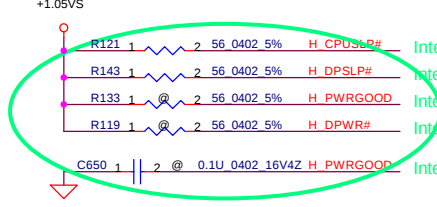
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1
200	0	1	0



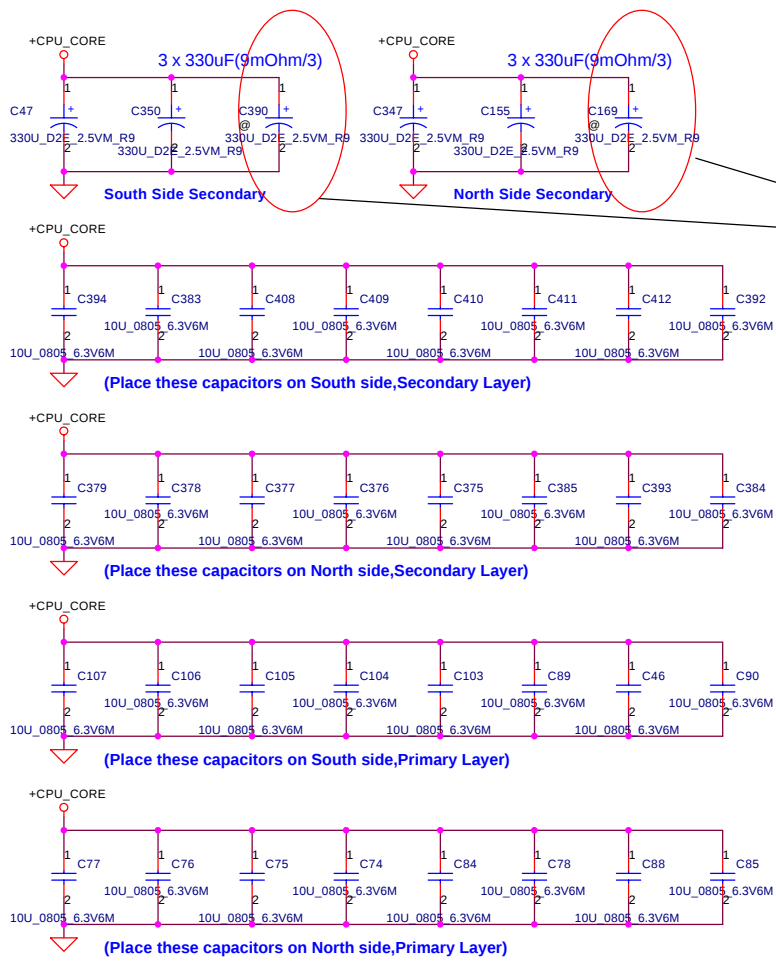
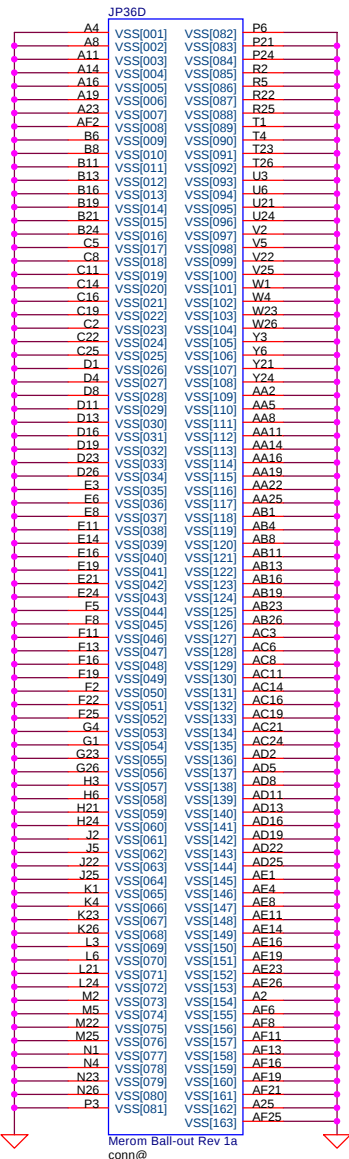
Length match within 25 mils. The trace width/space/other is 20/7/25.

Close to CPU pin within 500mils.

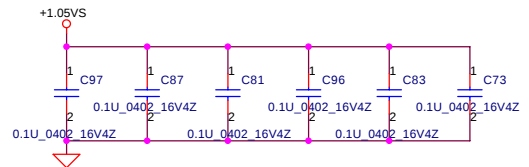


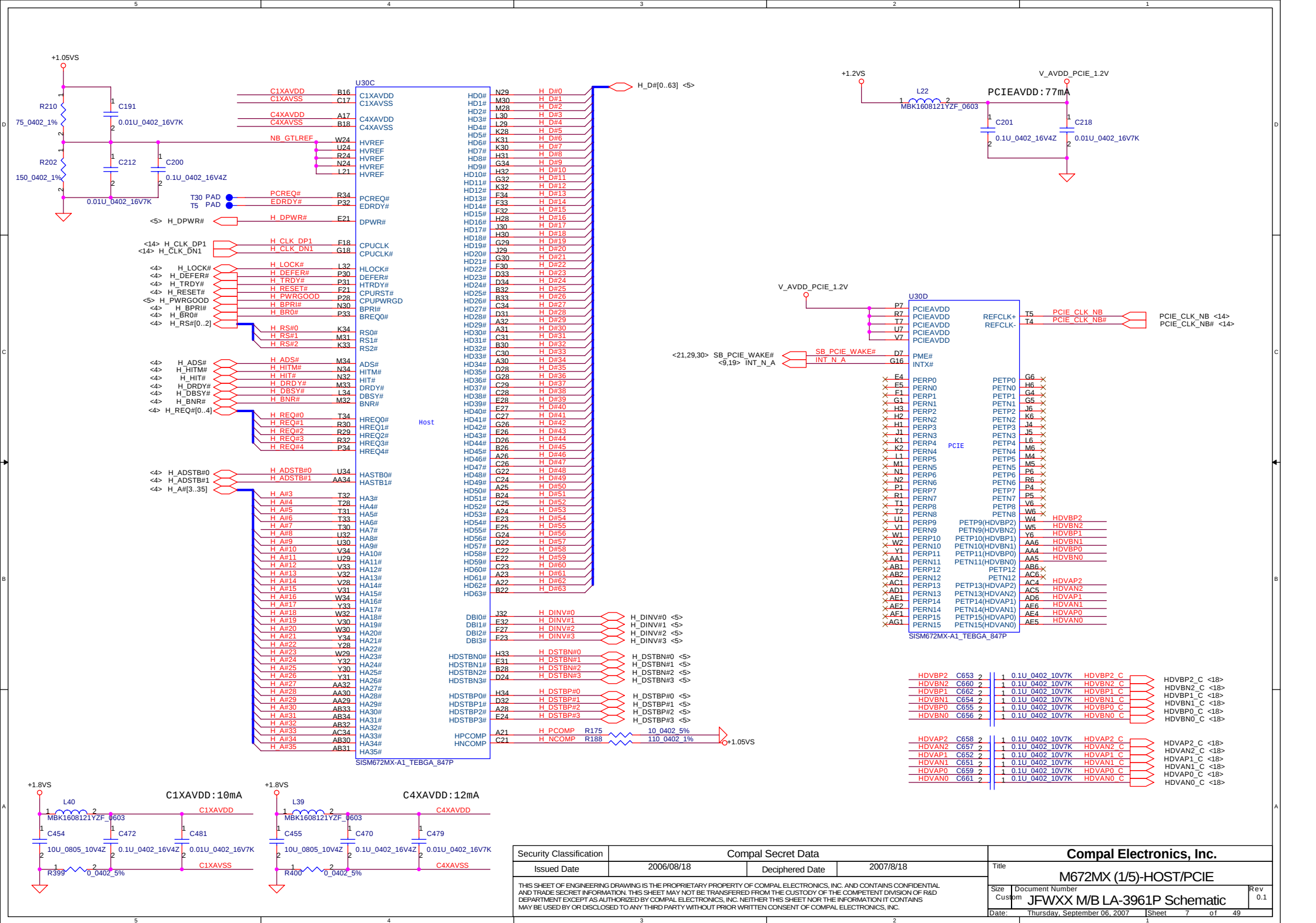
Int'l :Don't Pull-up SiS : Pull-up 56ohm (Mount)
Int'l :Pull-up 56ohm (Un-Mount) SiS : Pull-up 56ohm (Mount)
Int'l :Don't Pull-up (Connecte to ICH) SiS : Pull-up 56ohm (Un-Mount)
Int'l :Don't Pull-up SiS : Pull-up 56ohm (Un-Mount)
Int'l :Don't Pull-down SiS :Pull-down Cap (Un-Mount)

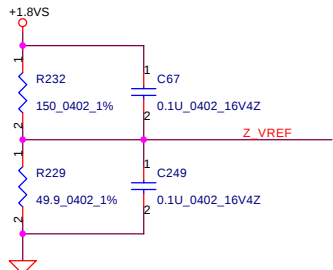
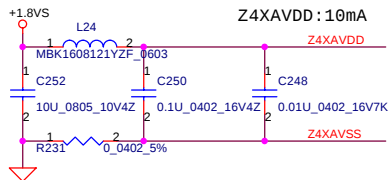
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+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

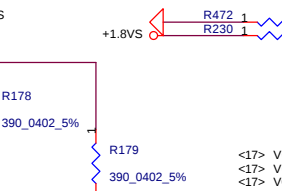




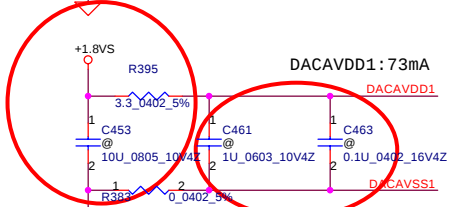
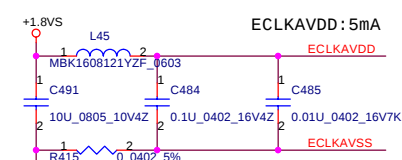
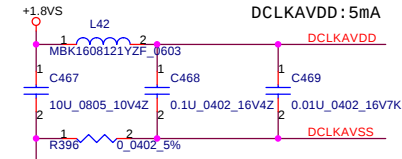


<17> VGA_CRT_HSYNC
<17> VGA_CRT_VSYNC
<17> GMCH_CRT_CLK
<17> GMCH_CRT_DATA

<19> ZAD[0..16] ZAD[0..16]



<7,19> INT_N_A INTA#
<14> REF_CLK0 VOSCI



DACAVDD1 Spec.
Voltage : 1.5V +/- 5%
Current : 100mA

7/30 modified to @

7/24 modified

<14> Z_CLK0 Z_CLK0 AH10
<19> ZDREQ ZDREQ AP8
<19> ZUREQ ZUREQ AN8
<19> ZSTB_DP0 ZSTB_DP0 AM7
<19> ZSTB_DN0 ZSTB_DN0 AL7
<19> ZSTB_DP1 ZSTB_DP1 AP4
<19> ZSTB_DN1 ZSTB_DN1 AP5

ZAD0 AK10
ZAD1 AM6
ZAD2 AK11
ZAD3 AJ11
ZAD4 AP7
ZAD5 AJ9
ZAD6 AP6
ZAD7 AN6
ZAD8 AK9
ZAD9 AM4
ZAD10 AK6
ZAD11 AK8
ZAD12 AN4
ZAD13 AK7
ZAD14 AL5
ZAD15 AM5
ZAD16 AM8

Z VREF AL9
Z COMP_P AP9
Z COMP_N AM9

Z4XAVDD AM10
Z4XAVSS AN10

<17> VGA_CRT_R VGA_CRT_R D13
<17> VGA_CRT_G VGA_CRT_G C12
<17> VGA_CRT_B VGA_CRT_B C13

A_HSYNC F12
A_VSYNC G12
A_DDC1CLK D11
A_DDC1DAT E12

VCOMP D15
VVBWN C15
VRSET C14

DACAVDD1 A12
DACAVSS1 B12

DACAVDD2 A13
DACAVSS2 B13

DCLKAVDD B10
DCLKAVSS A11

ECLKAVDD A9
ECLKAVSS B8

SISM672MX-A1_TEBGA_847P

U30A
ZCLK
ZDREQ
ZUREQ
ZSTB0#
ZSTB1#
ZSTB1#

ENTEST
TESTMODE0
TESTMODE1
TESTMODE2
TRAP0
TRAP1
TRAP2
TRAP3
TRAP4
TRAP5
TRAP6
TRAP7
TRAP8
TRAP9
TRAP10

AUXOK
PWROK
PCIRST#

AGPSTOP#
AGPBUSY#

VBVSYNC
VBHSYNC
VBHCLK
VBCLK
VBCAD
VACLK

NC0
NC1

AGPSTOP#
AGPBUSY#
VBVSYNC
VBHSYNC
VBHCLK
VBCLK
VBCAD
VACLK

AGPSTOP#
AGPBUSY#
VBVSYNC
VBHSYNC
VBHCLK
VBCLK
VBCAD
VACLK

AGPSTOP#
AGPBUSY#
VBVSYNC
VBHSYNC
VBHCLK
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VACLK

AGPSTOP#
AGPBUSY#
VBVSYNC
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AGPBUSY#
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AGPBUSY#
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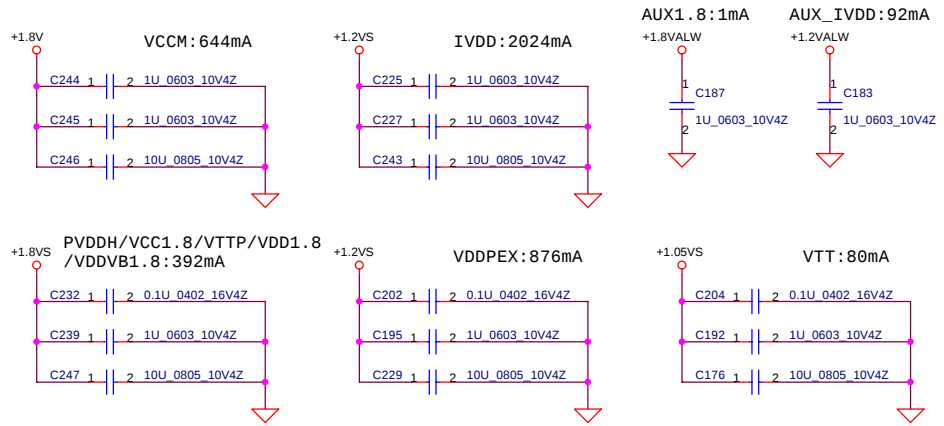
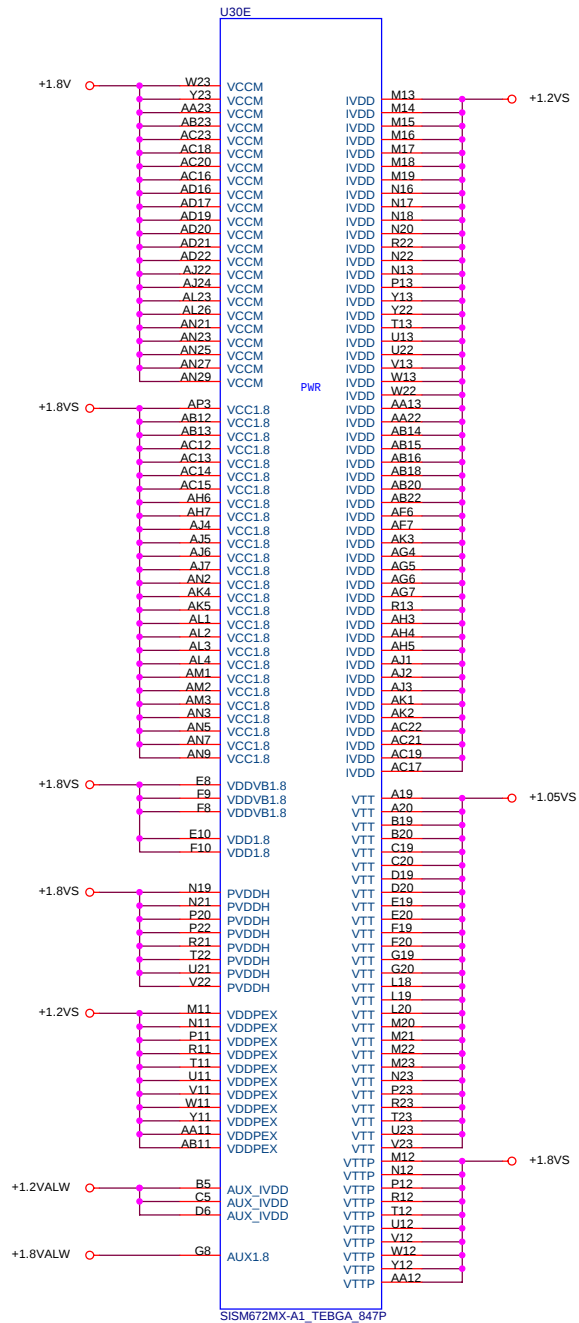
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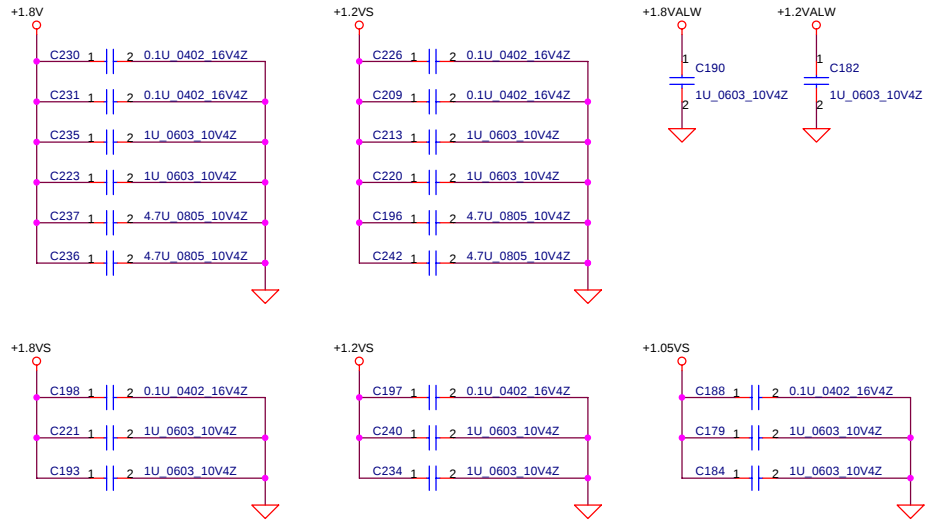
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VBCLK
VBCAD
VACLK

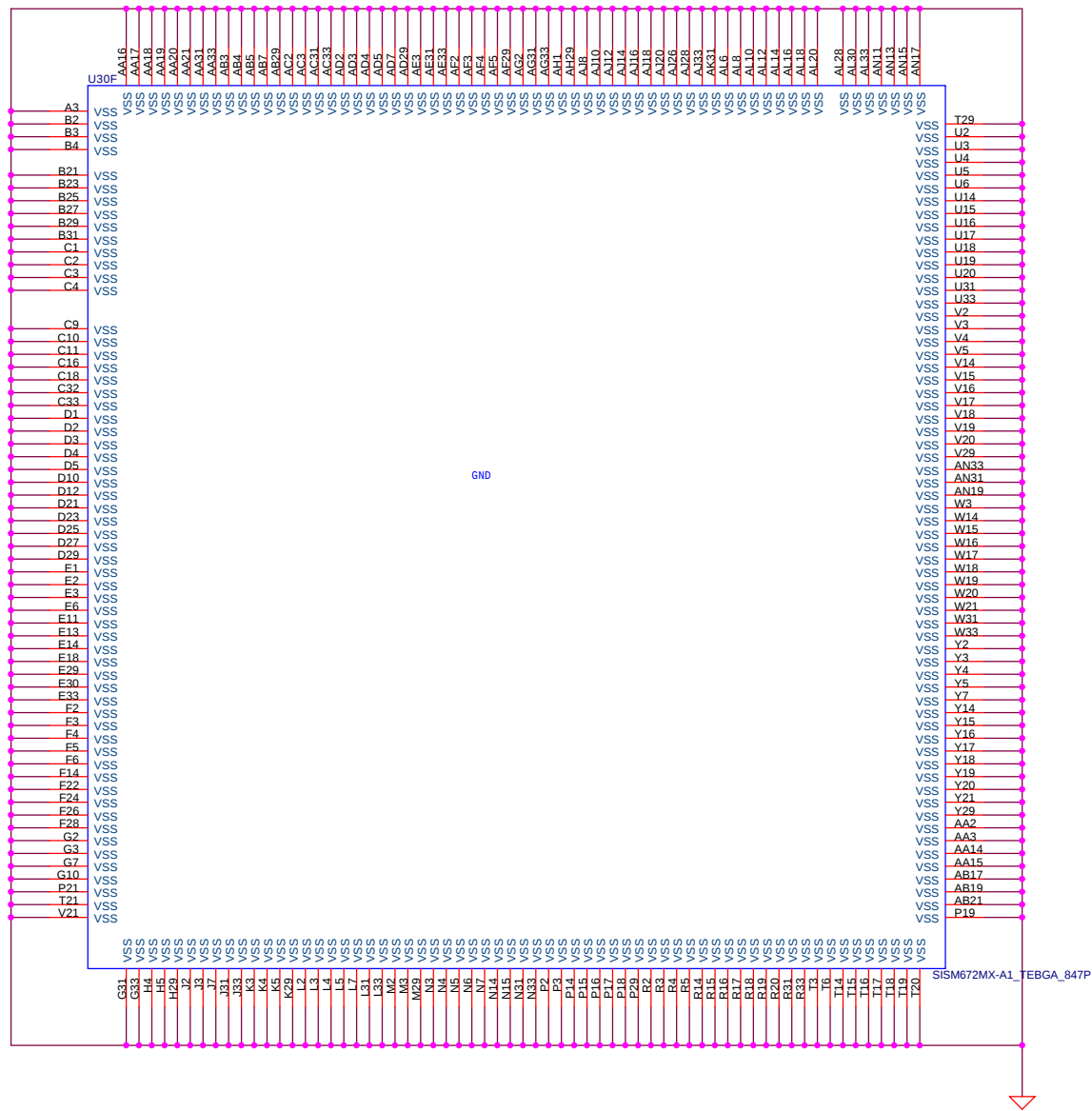
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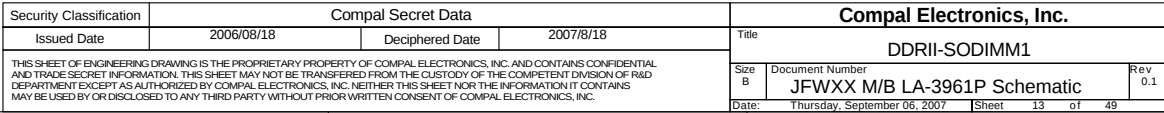
Place these Cap under M672MX solder side.

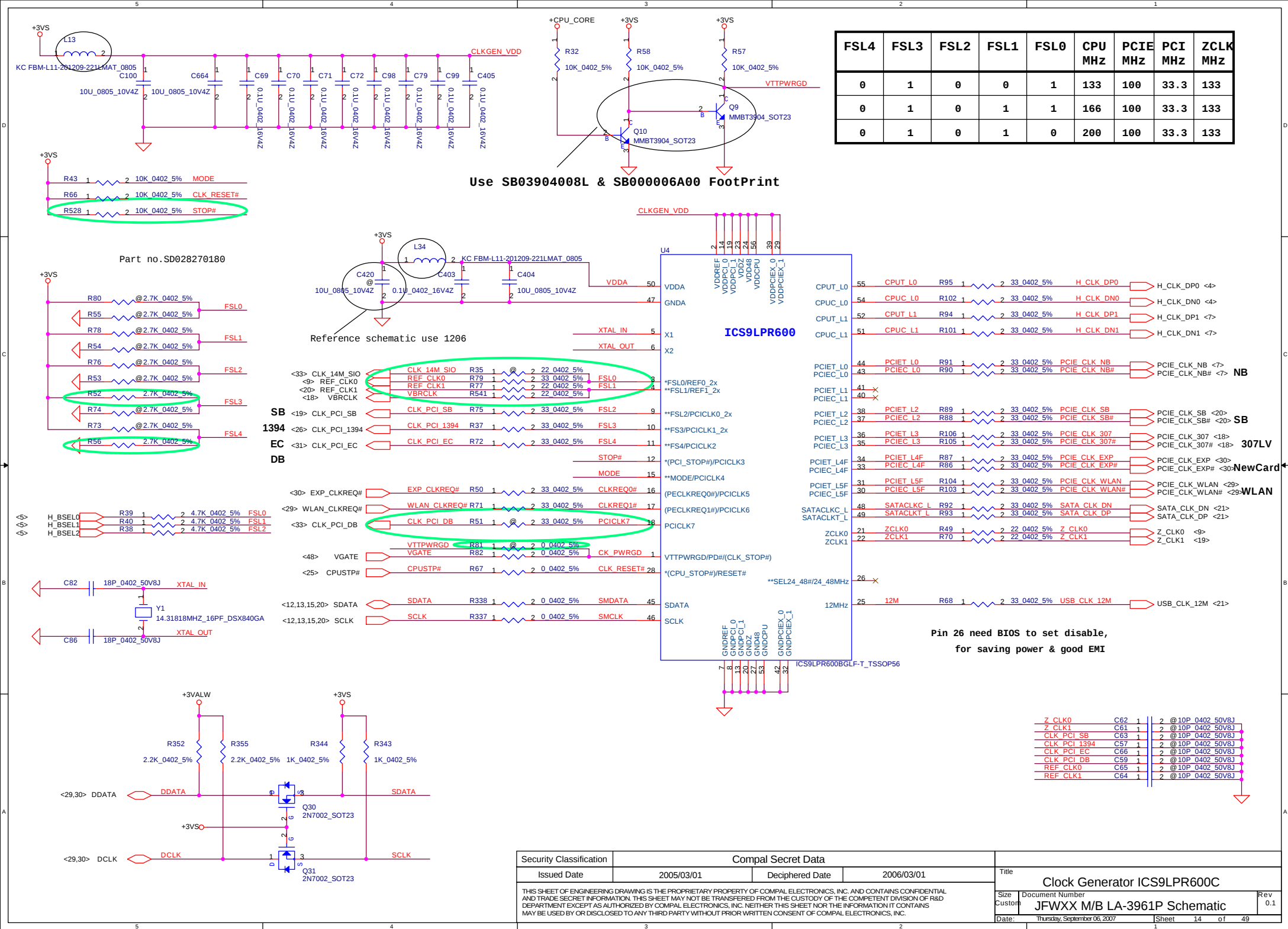


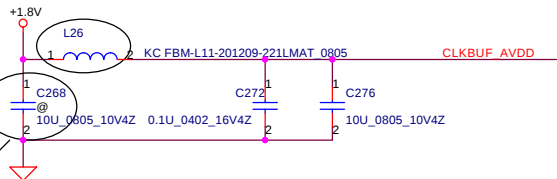
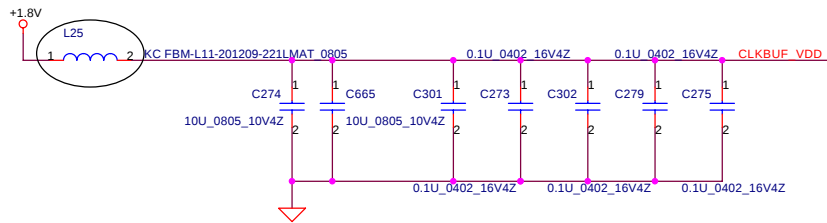
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size		Document Number		Rev	
Custom		JFWXX M/B LA-3961P Schematic		0.1	
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				Document Number	0.1
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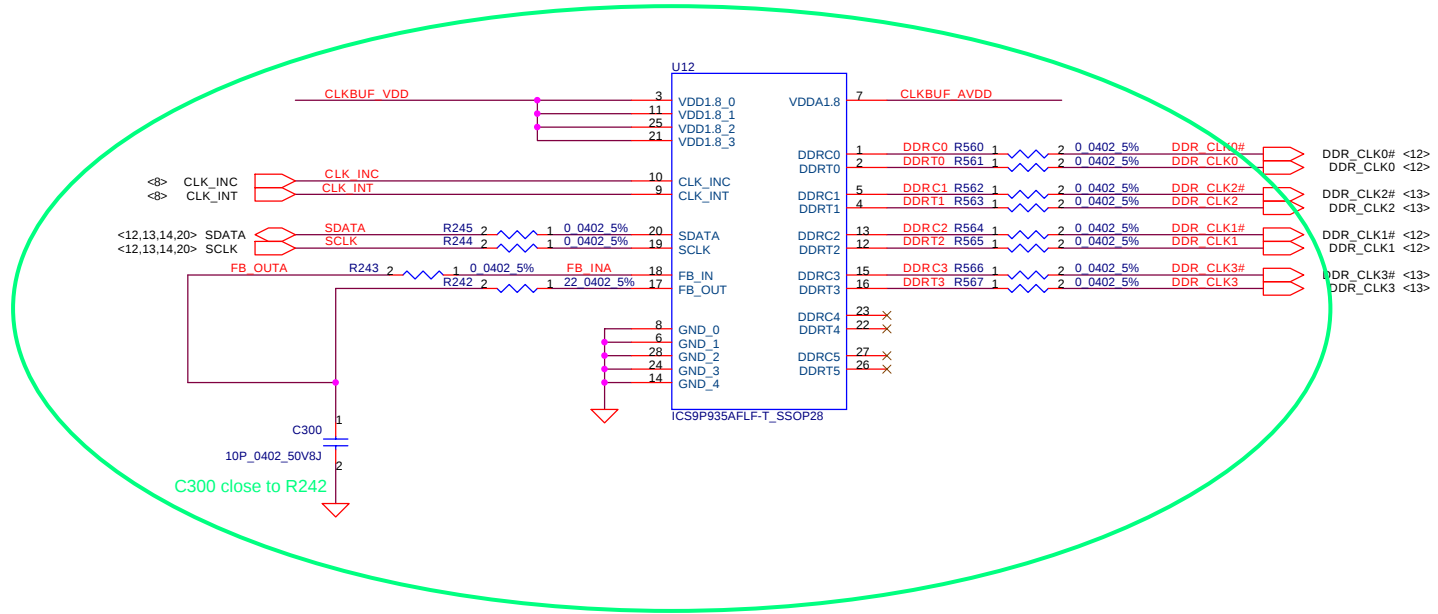






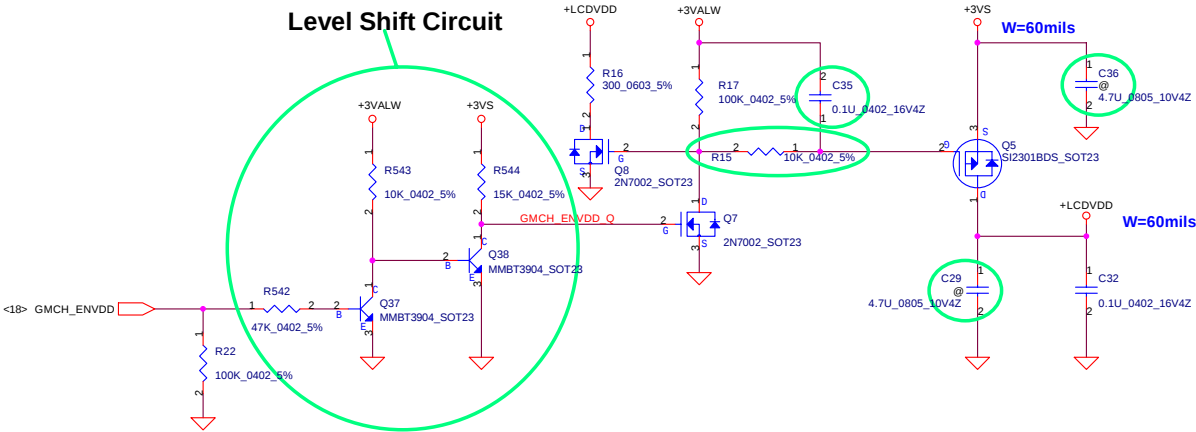
Reference schematic use 1206

Horizontal rotate

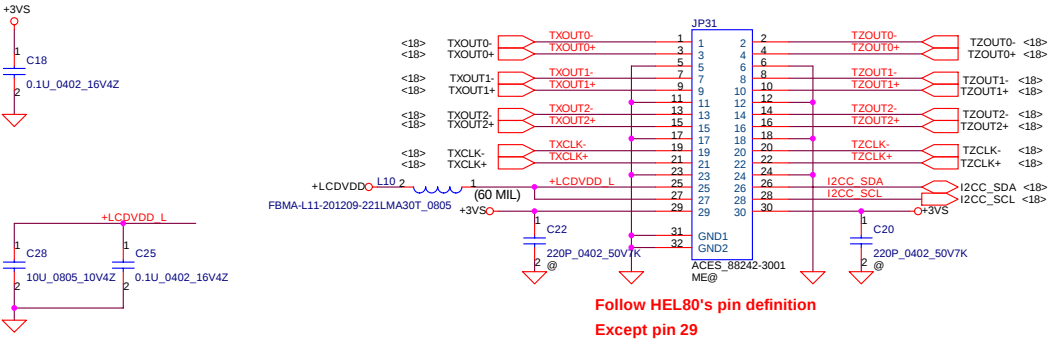


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LCD POWER CIRCUIT

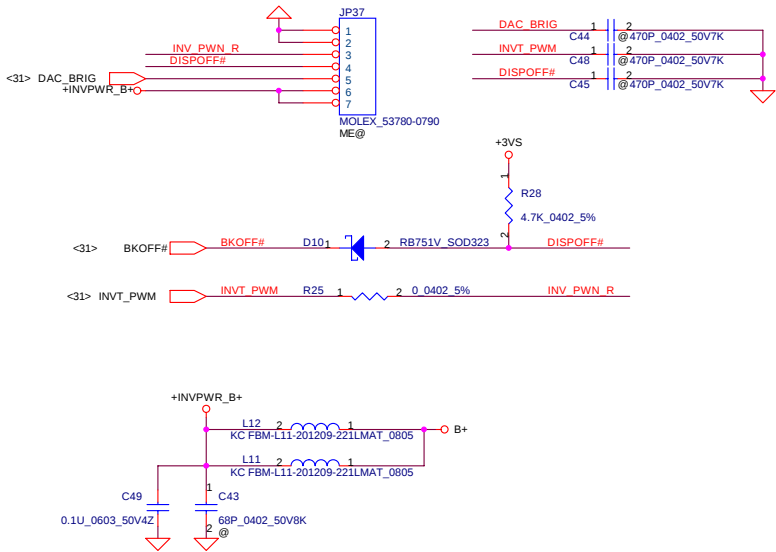


LCD/PANEL BD. Conn.



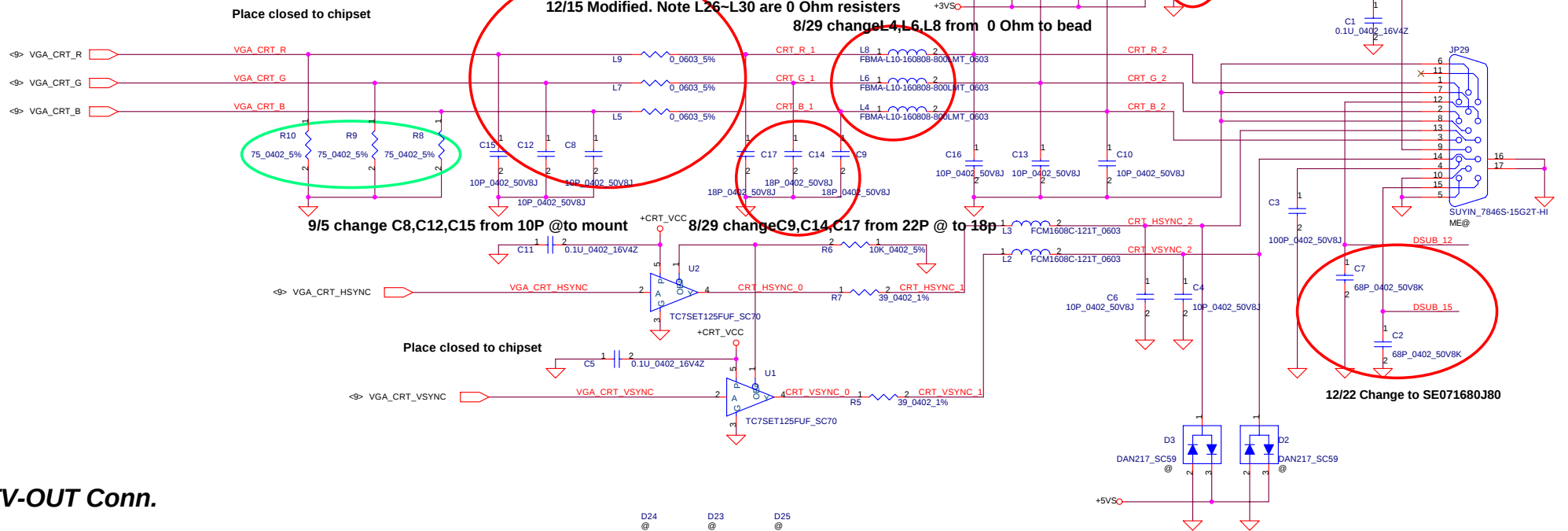
Follow HEL80's pin definition
Except pin 29

INVERTER Conn.

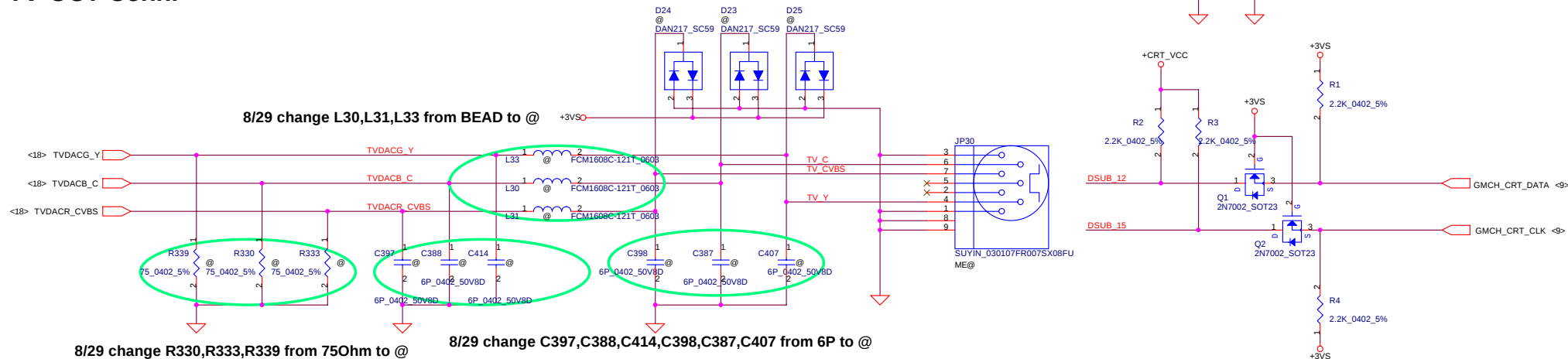


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Size B	Document Number	JFWXX M/B LA-3961P Schematic			Rev	0.1
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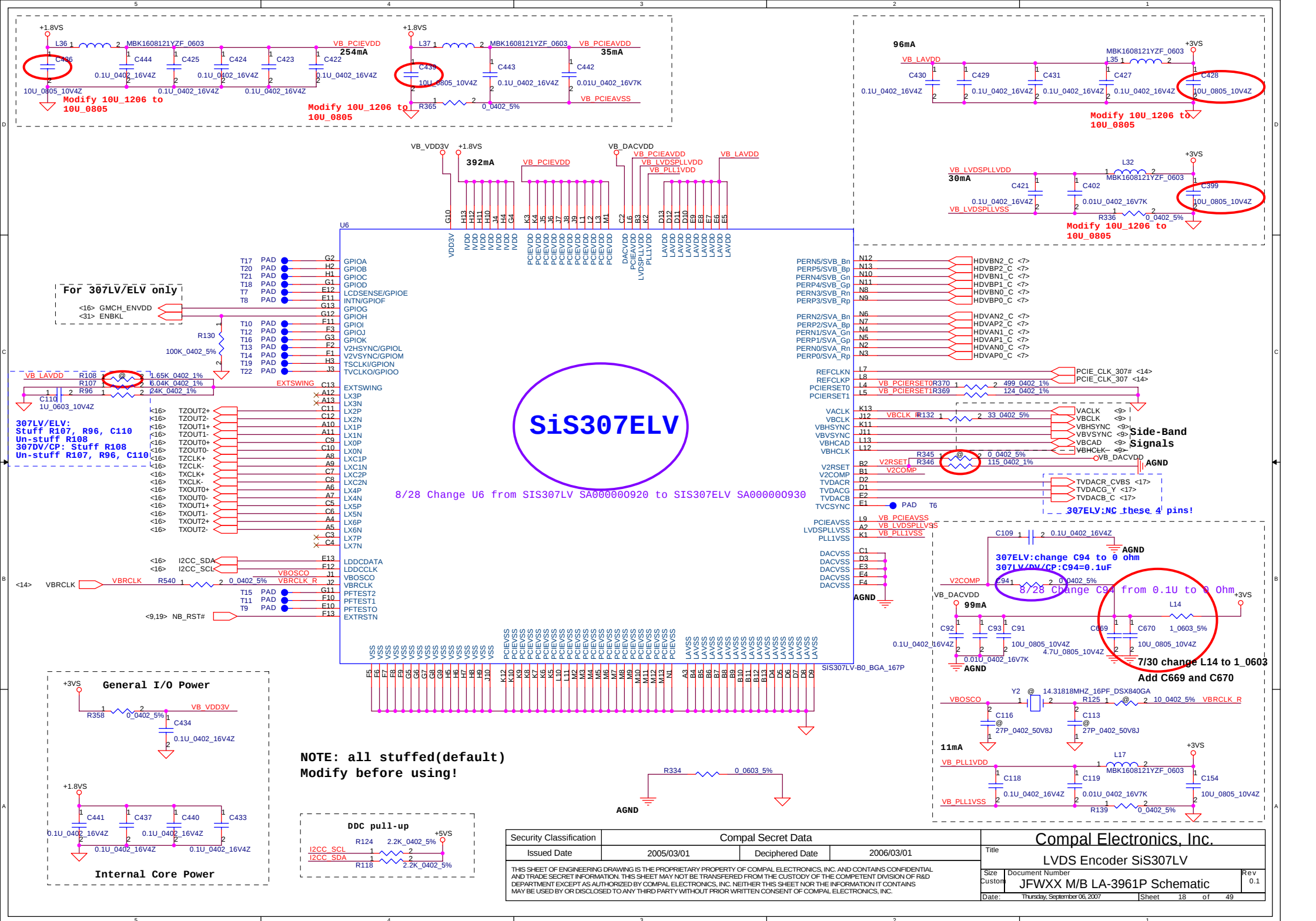
CRT Connector

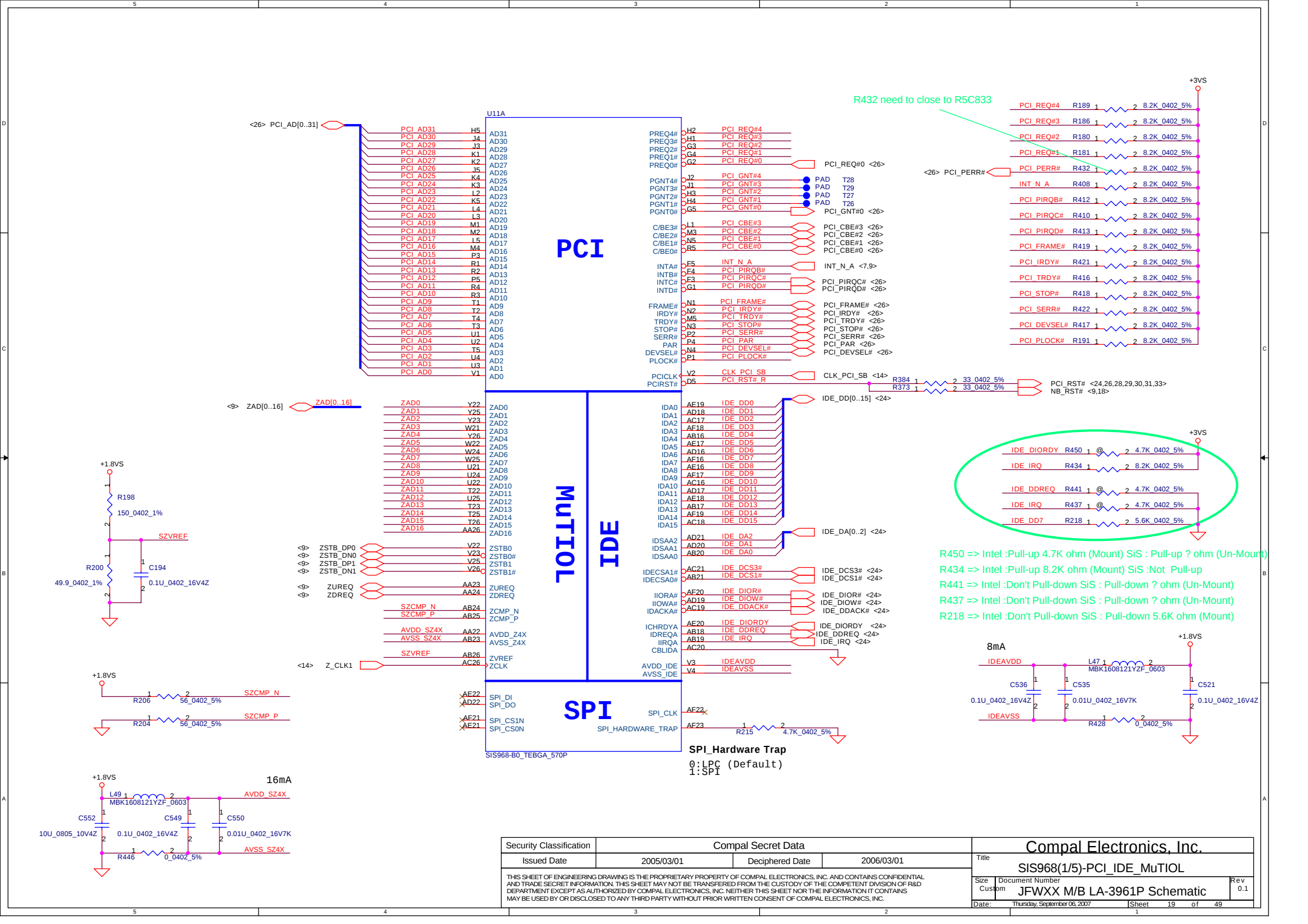


TV-OUT Conn.

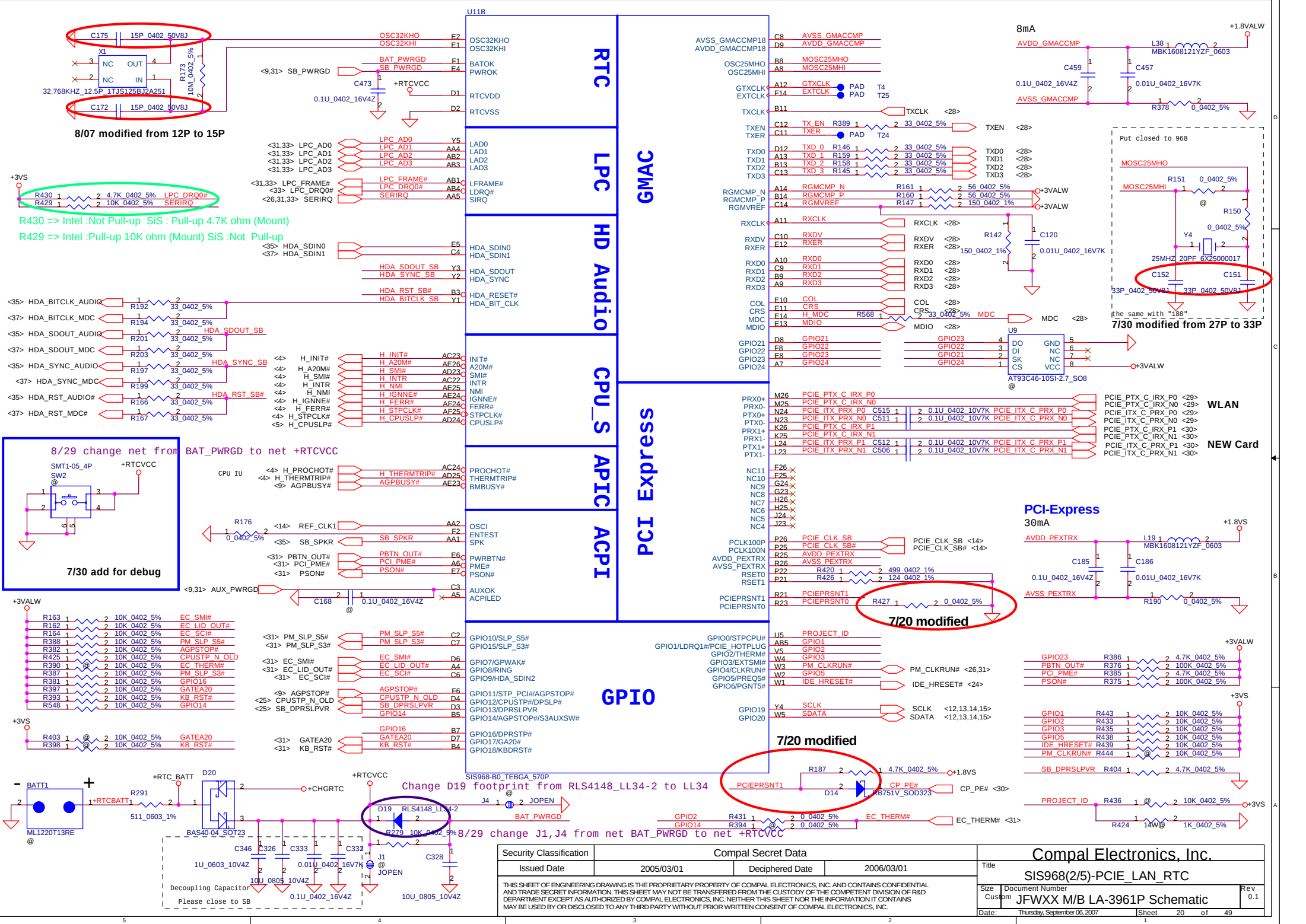


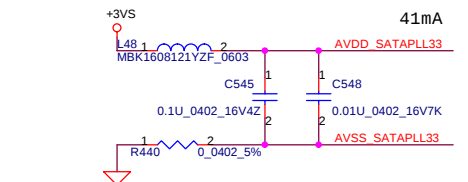
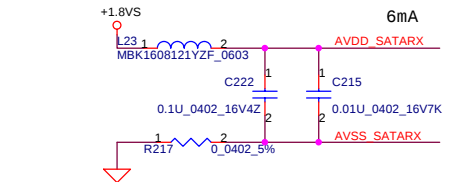
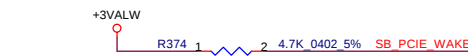
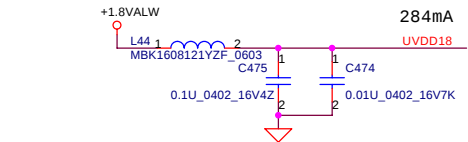
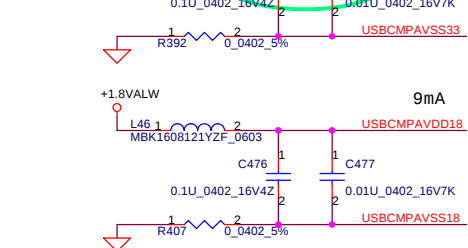
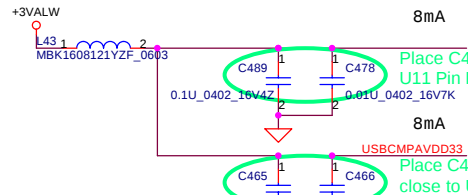
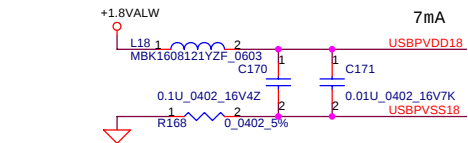
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				JFWXX M/B LA-3961P Schematic	
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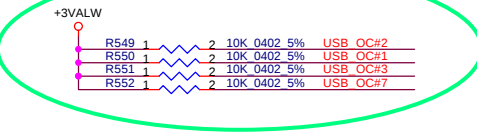
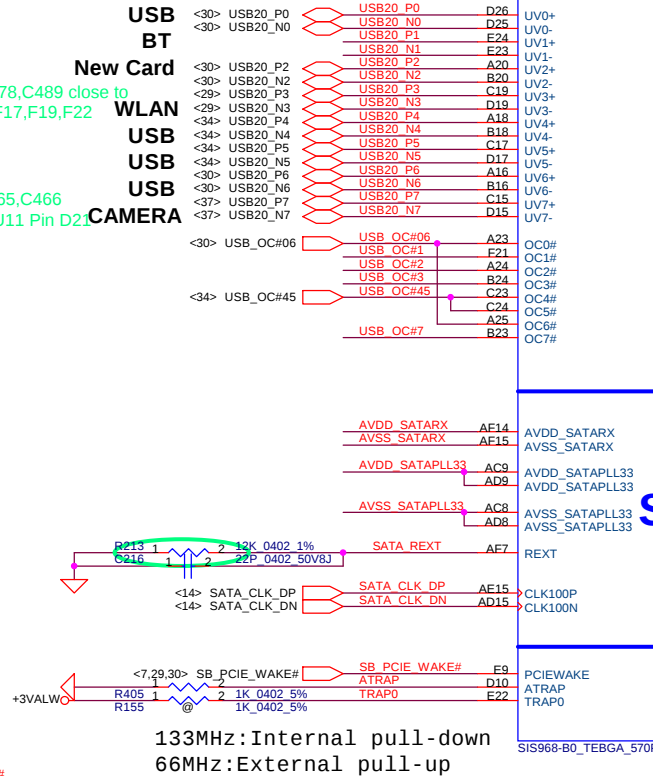
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Size	Document	Customer	Number	Rev	
JFWXX		M/B LA-3961P Schematic		0.1	
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USB BT
New Card
WLAN
USB
USB
CAMERA

Place C478,C489 close to U11 Pin F17,F19,F22
Place C465,C466 close to U11 Pin D21



USB

SATA

PCIEWAKE

SIS968-BO_TEBGA_570P

IPB_OUT0

IPB_OUT1

IPB_OUT2

IPB_OUT3

IPB_OUT4

IPB_OUT5

IPB_OUT6

IPB_OUT7

IPB_OUT8

IPB_OUT9

IPB_OUT10

IPB_OUT11

IPB_OUT12

IPB_OUT13

IPB_OUT14

IPB_OUT15

IPB_OUT16

IPB_OUT17

IPB_OUT18

IPB_OUT19

IPB_OUT20

IPB_OUT21

IPB_OUT22

IPB_OUT23

IPB_OUT24

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IPB_OUT26

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IPB_OUT30

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IPB_OUT42

IPB_OUT43

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IPB_OUT215

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IPB_OUT223

IPB_OUT224

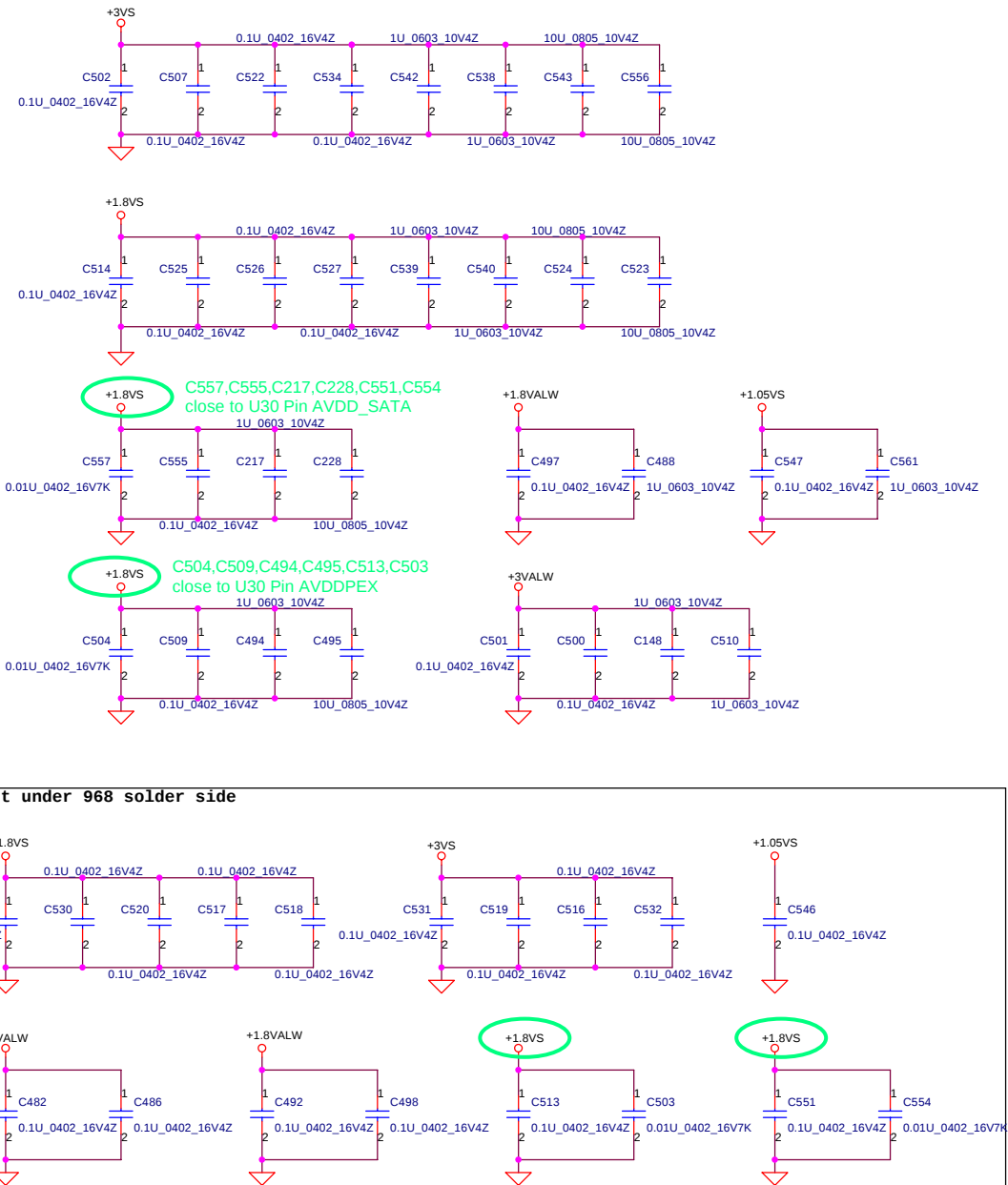
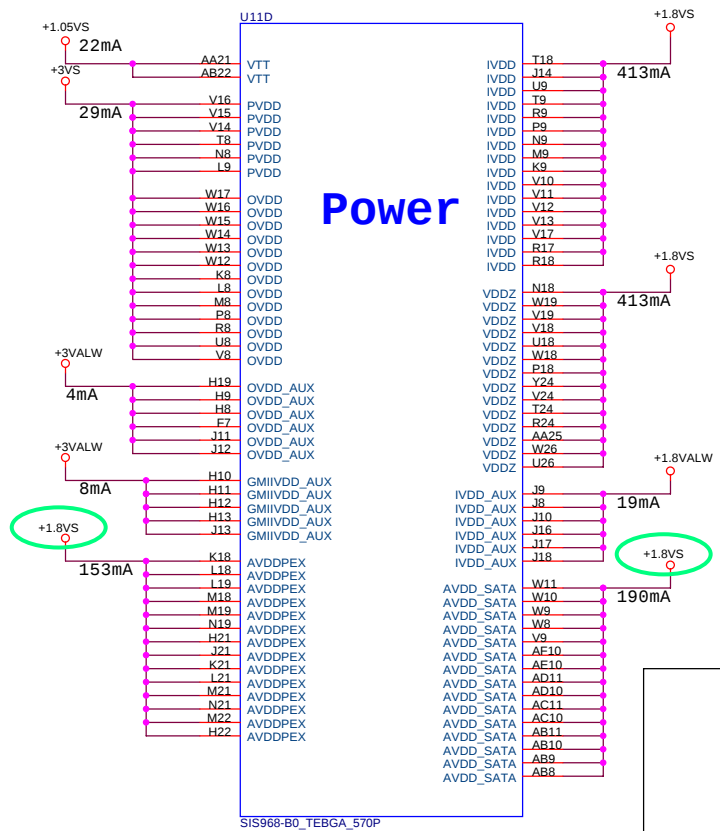
IPB_OUT225

IPB_OUT226

IPB_OUT227

IPB_OUT228

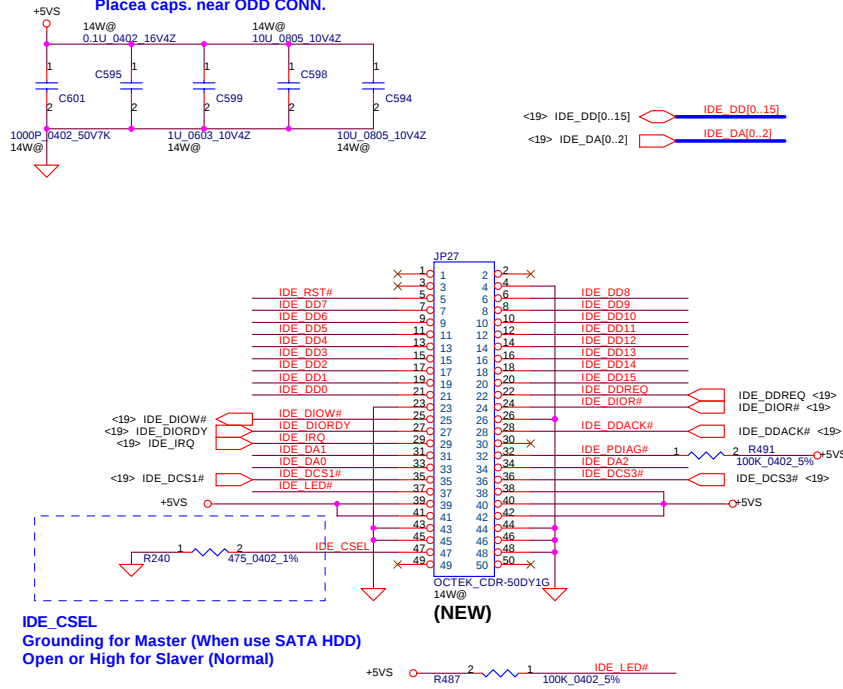
IPB_OUT229



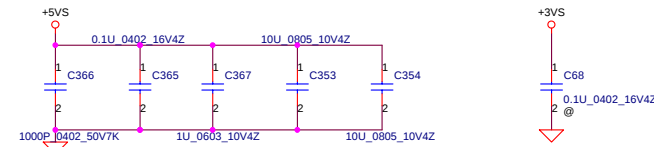
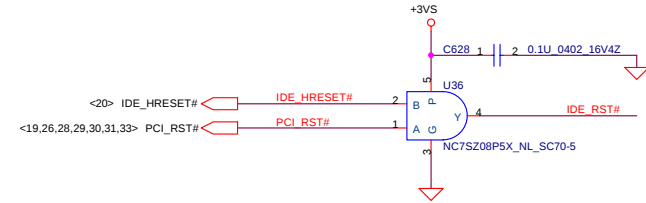
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Size		Document Number		Rev	
Custom		JFWXX M/B LA-3961P Schematic		0.1	
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14W ODD Conn.

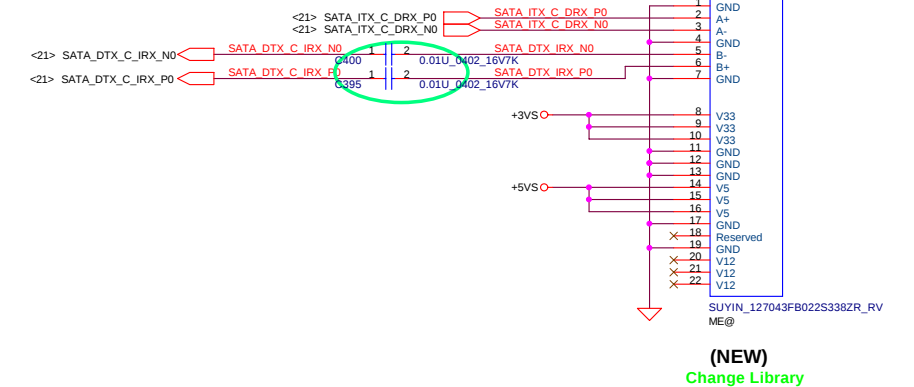
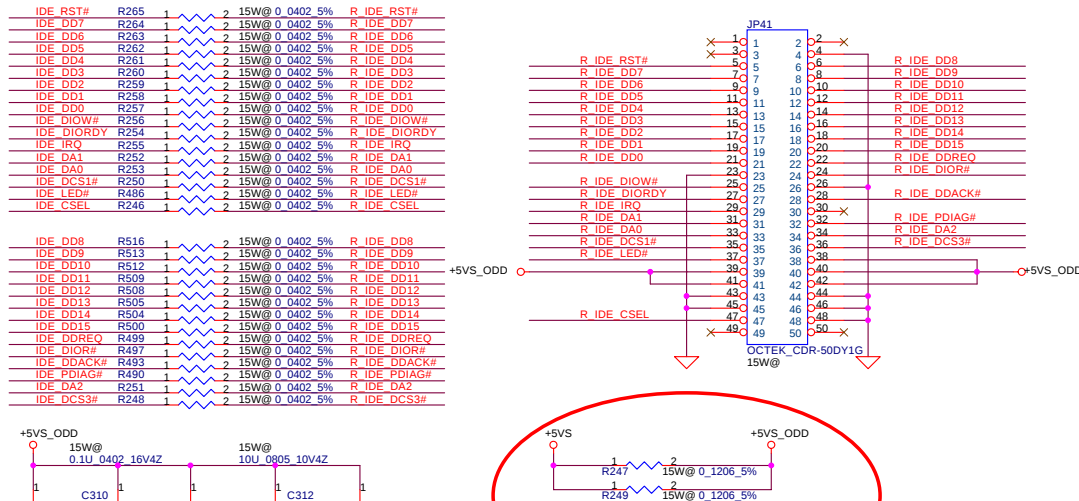
Place caps. near ODD CONN.



SATA HDD Conn.

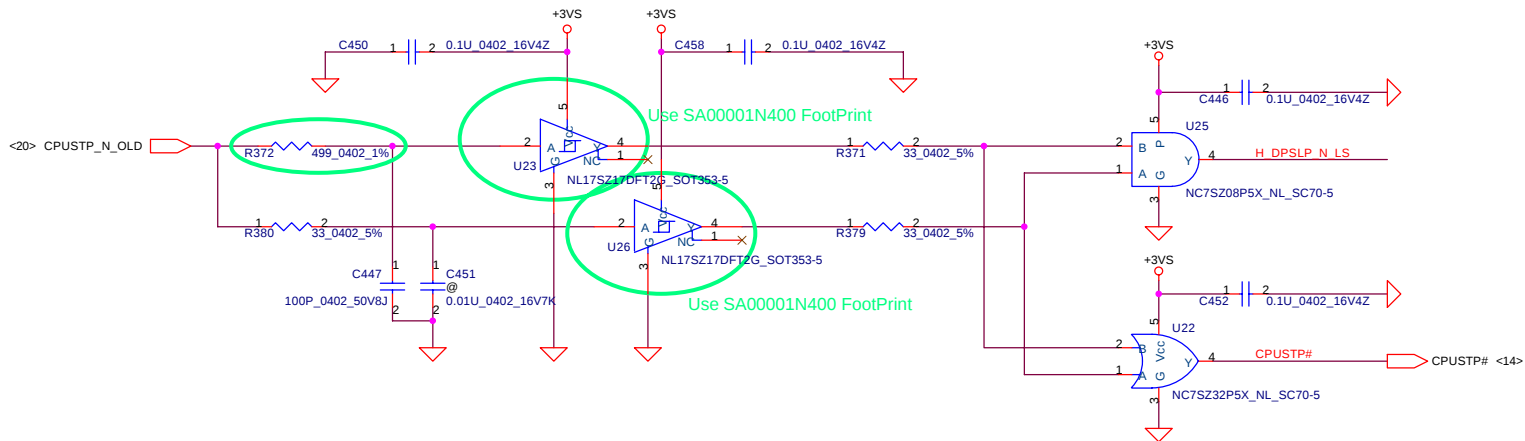
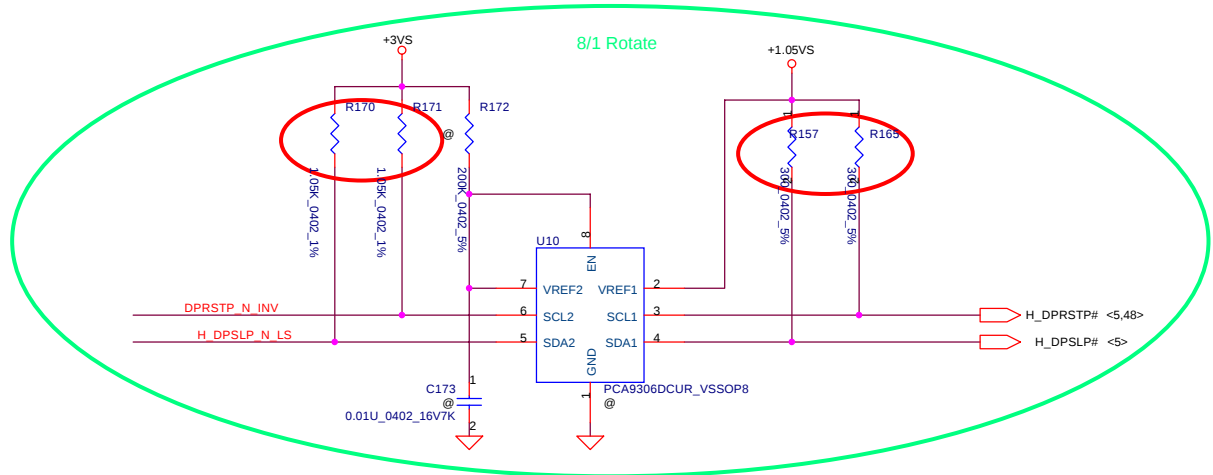
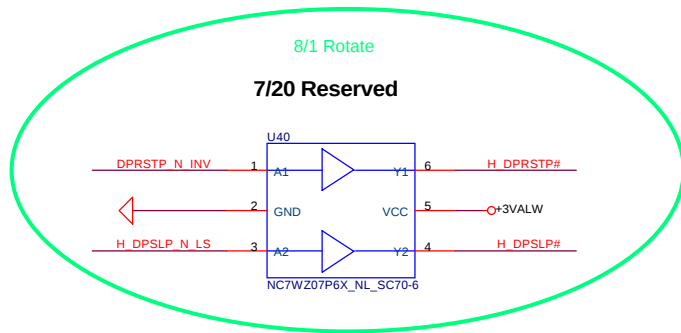
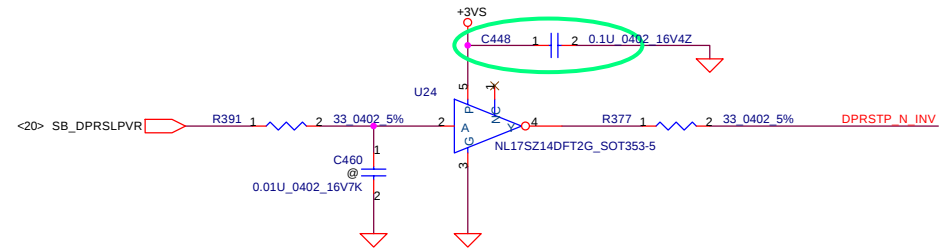
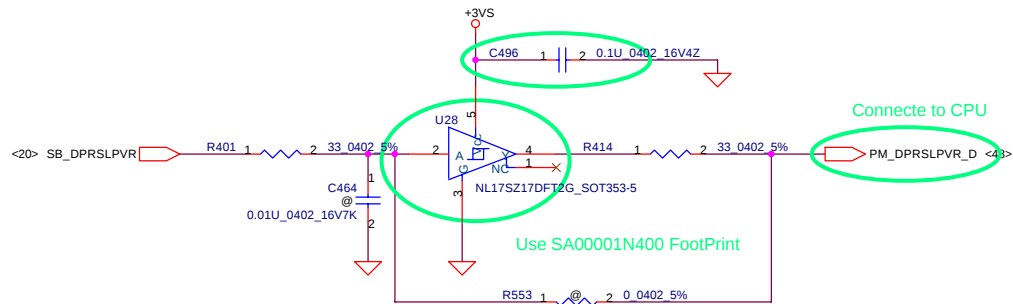


15W ODD Conn.

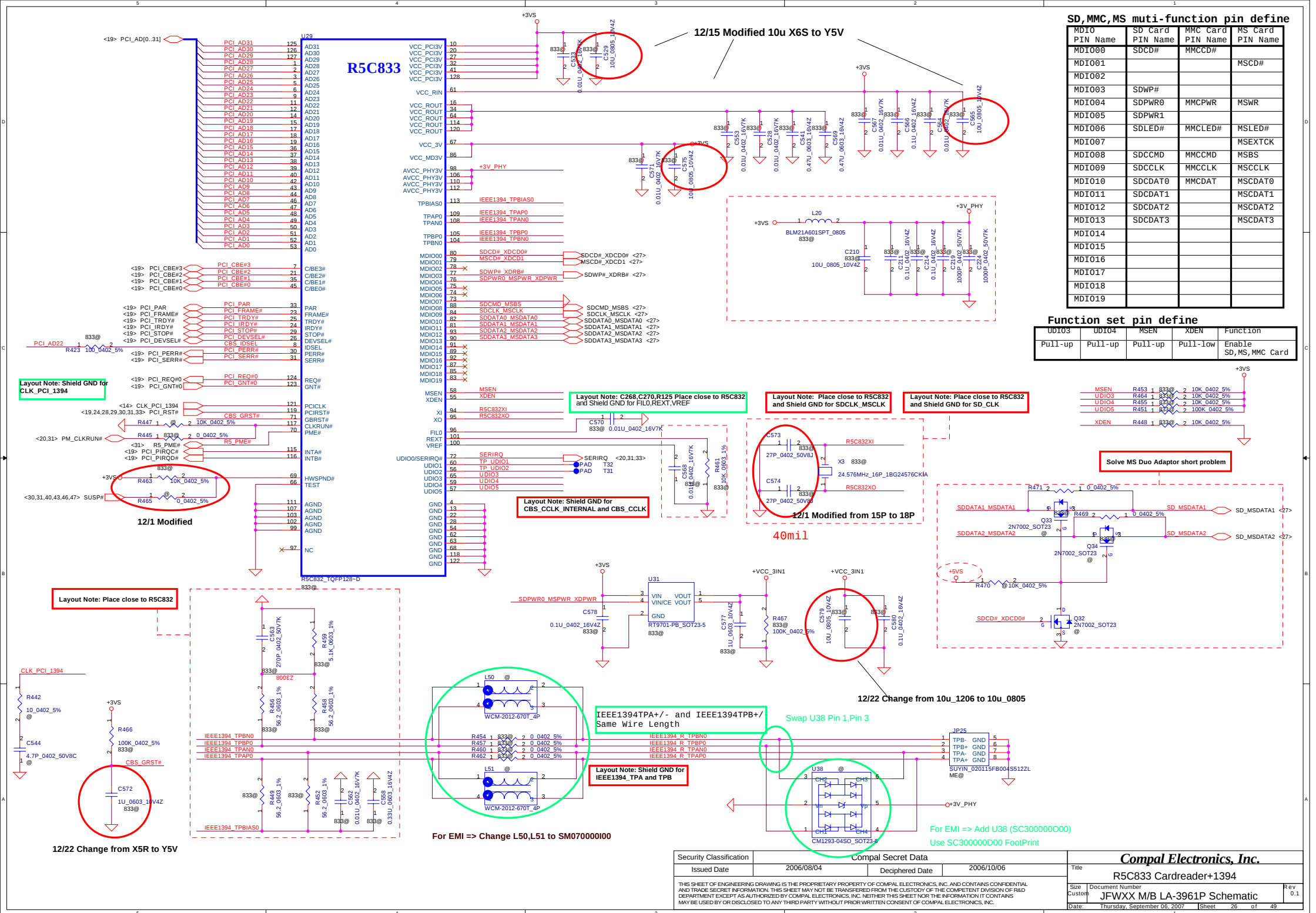


12/4 Change J7 to 2x0 Ohm 1/4W resistors

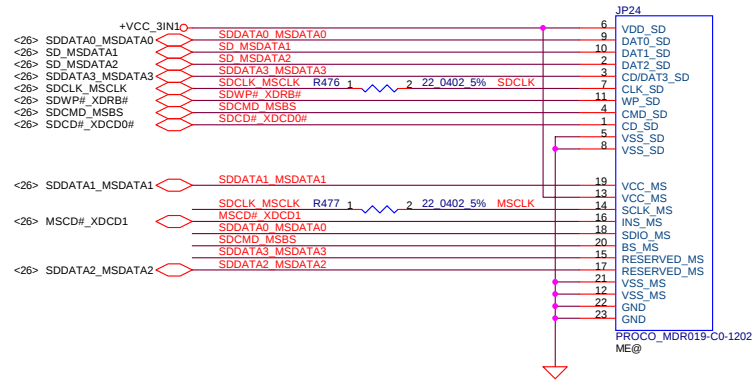
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	HDD & ODD Connector	
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				JFWXX M/B LA-3961P Schematic	
				Date:	Thursday, September 06, 2007
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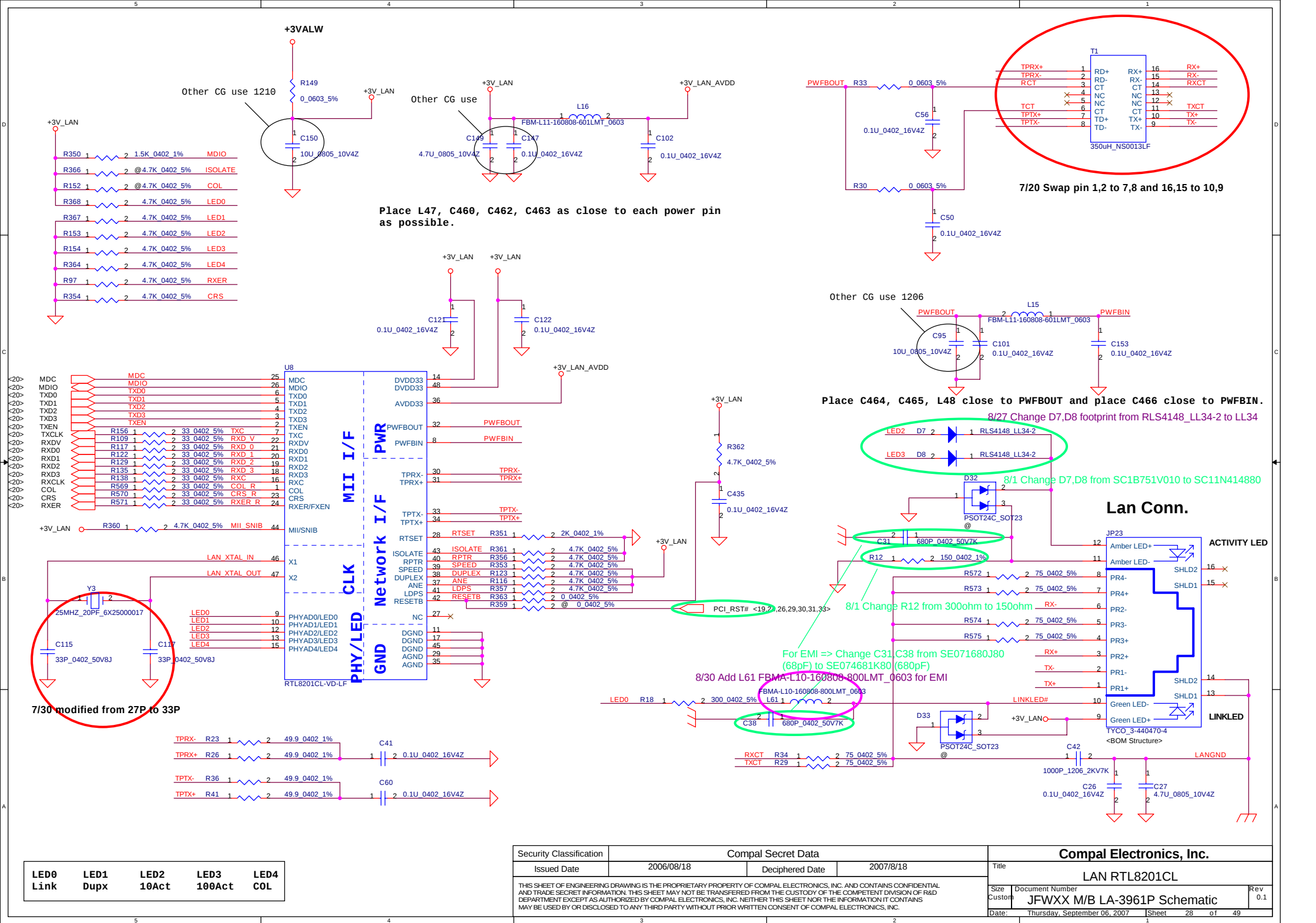
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3 in 1 Card Reader

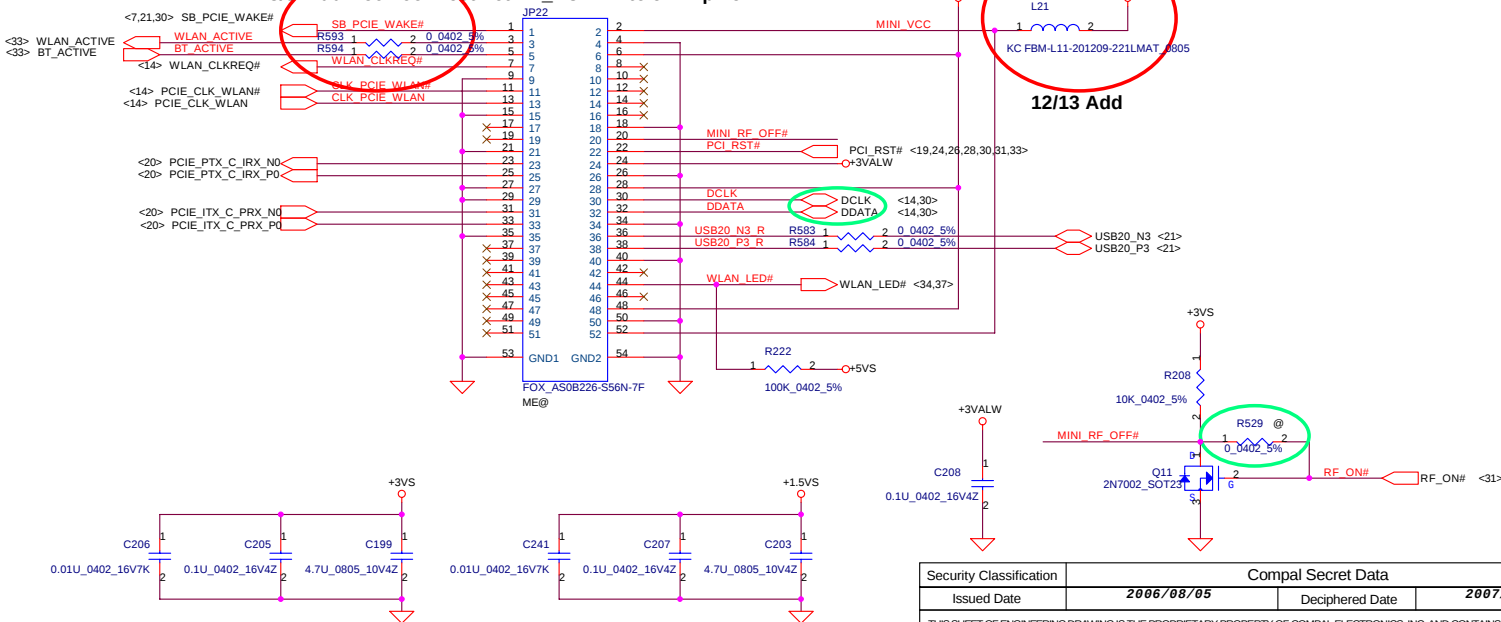


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				Size Custom	Document Number JFWXX M/B LA-3961P Schematic Rev 0.1
Date: Thursday, September 06, 2007		Sheet 27 of 49			

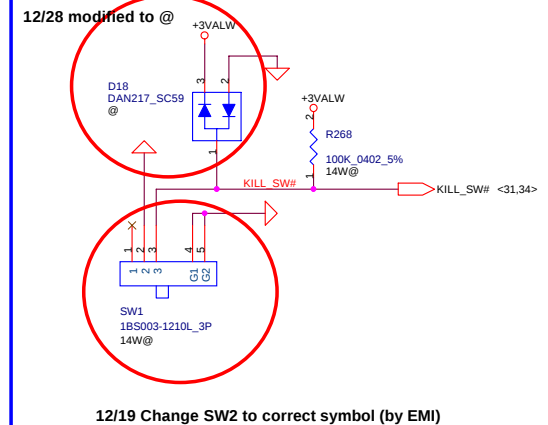


Mini-Express Card for WLAN

8/31 Add R593 connect net WLAN_ACTIVE to JP22 pin3
8/31 Add R594 connect net BT_ACTIVE to JP22 pin5

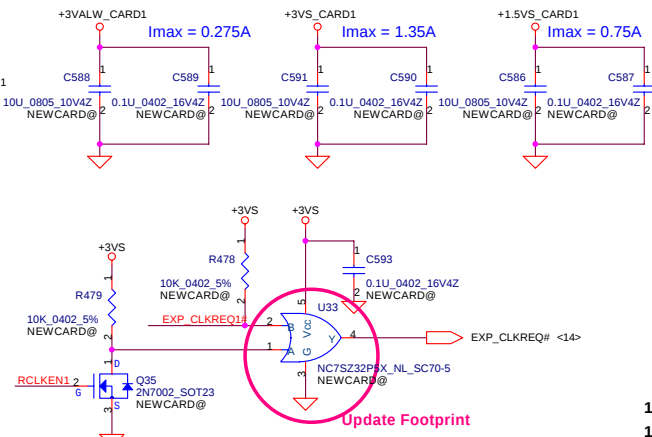
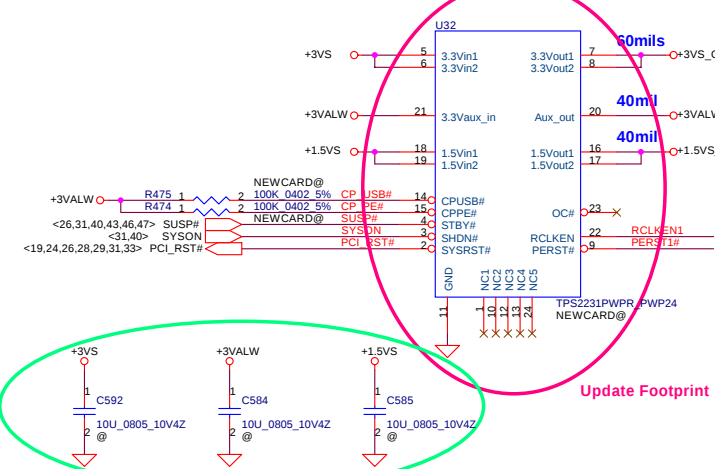


Kill SWITCH

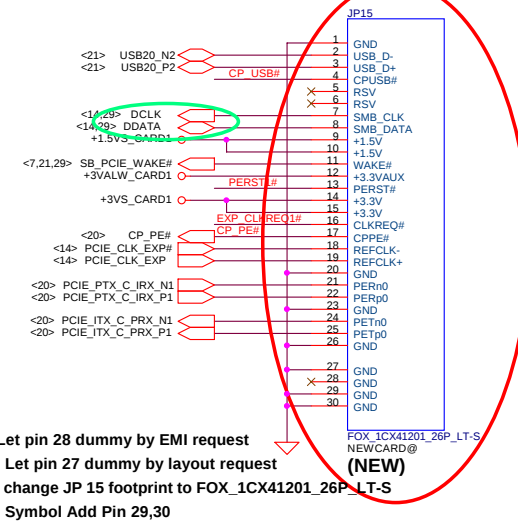


Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Mini-Card/Kill SW	
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				JFWXX M/B LA-3961P Schematic	Rev 0.1
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New Card Power Switch



New Card Socket (Left/TOP)



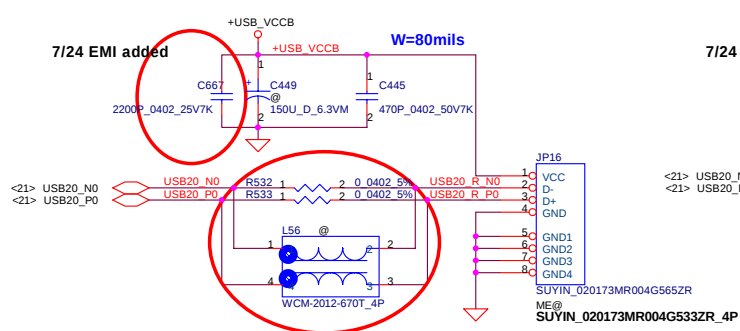
12/7 Let pin 28 dummy by EMI request

12/13 Let pin 27 dummy by layout request

12/27 change JP 15 footprint to FOX_1CX41201_26P_LT-S (NEW)

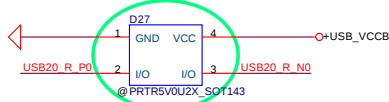
04/17 Symbol Add Pin 29,30

USB CONN. 1



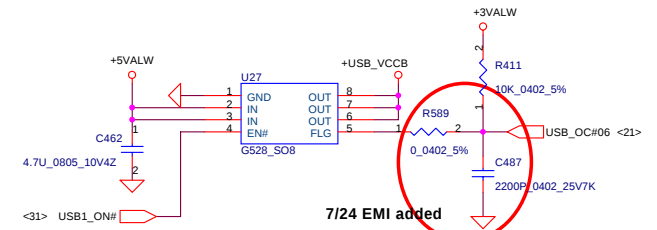
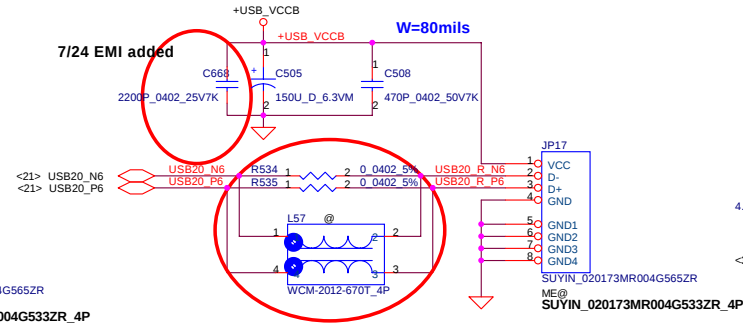
For EMI => Add R532,R533,R534,R535 (SD028000080), L56, L57 (SM070000I00)

7/30 change L56,57 to SM070000K00 by EMI request

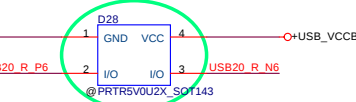


For EMI => Change D27,D28 from SC300000I00 to SC300000P00

USB CONN. 2

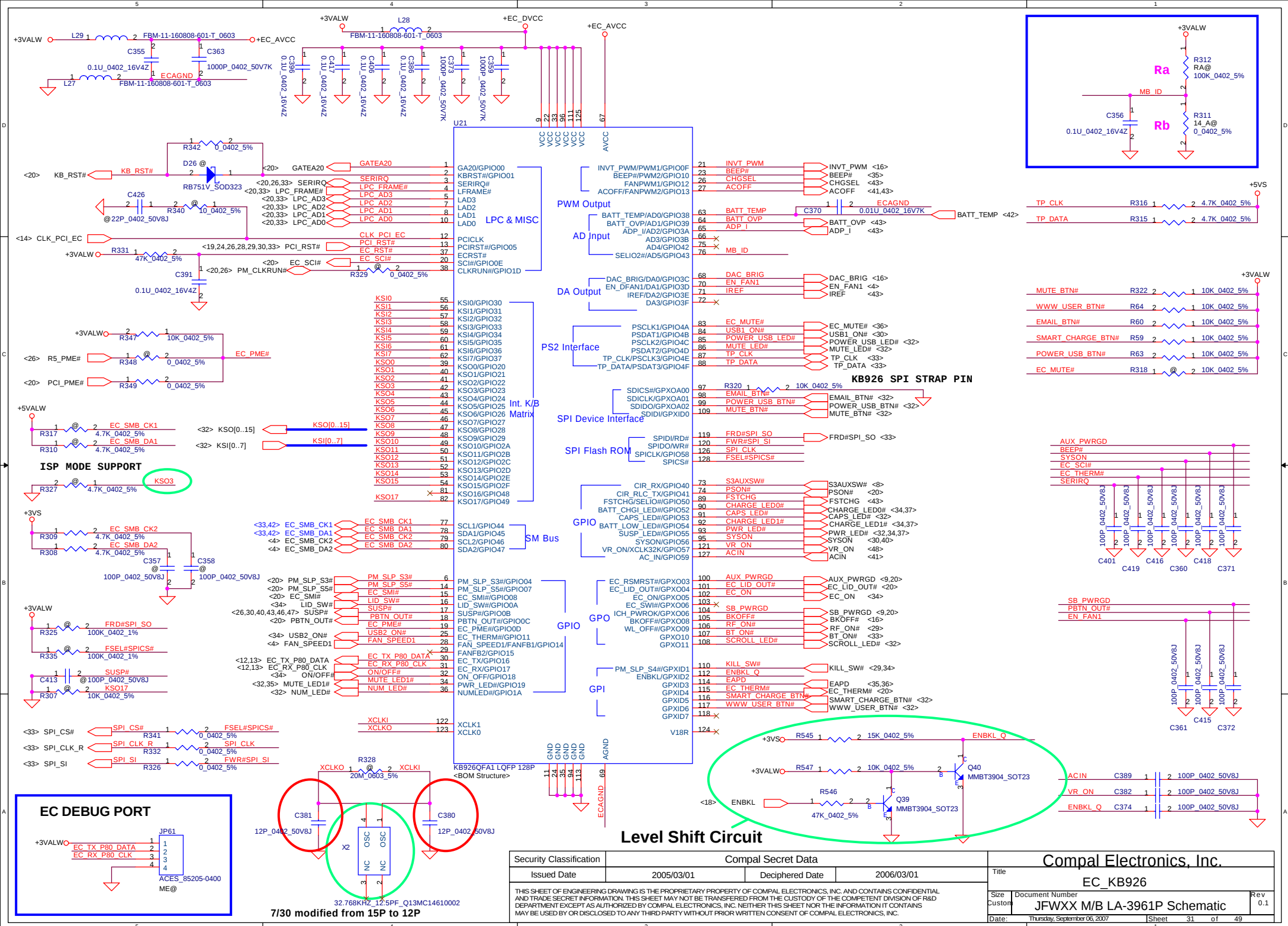


7/24 EMI added



For EMI => Change D27,D28 from SC300000I00 to SC300000P00

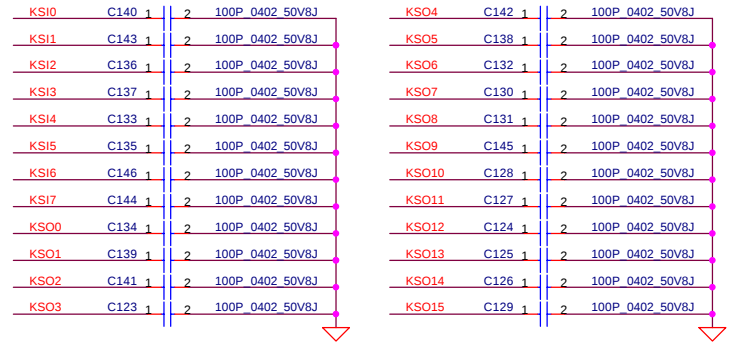
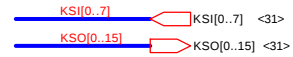
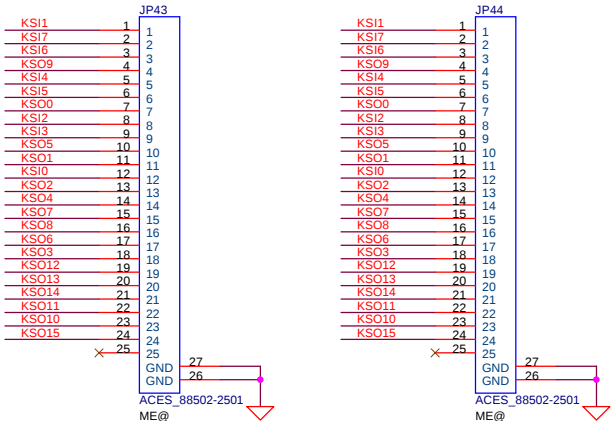
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Size	B	Document Number	JFWXX M/B LA-3961P Schematic	Rev	0.1
Date	Thursday, September 06, 2007	Sheet	30	of	49



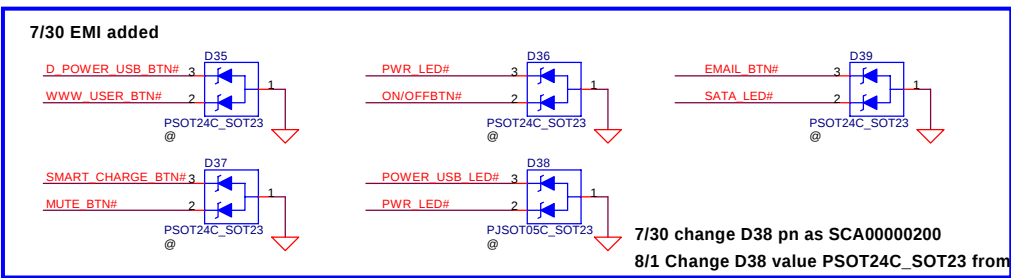
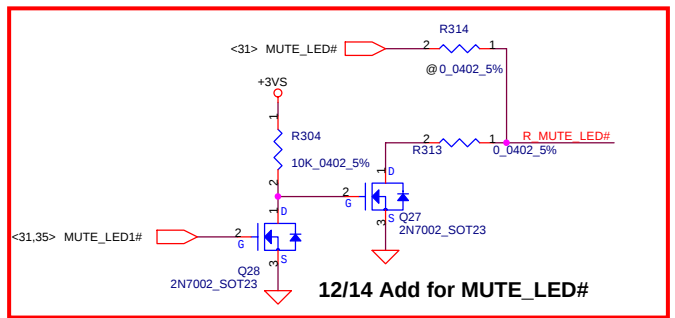
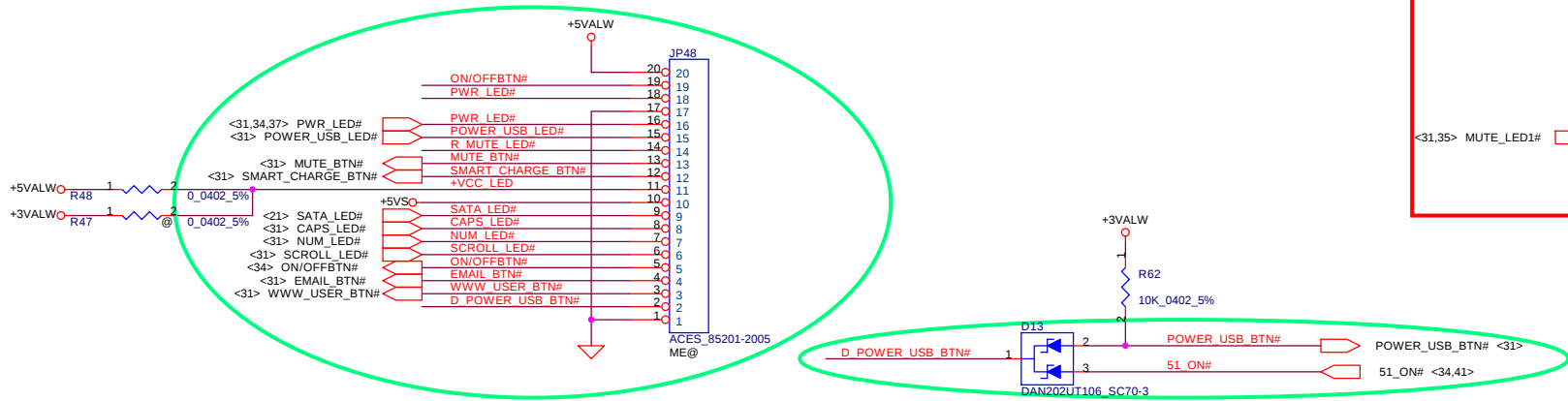
INT_KBD Conn.

For JFW91

For JFW01

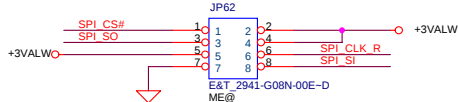
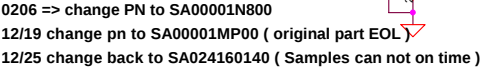


Switch Board Conn.



7/30 change D38 pn as SCA00000200
8/1 Change D38 value PSOT24C_SOT23 from to PJSOT05C_SOT23 , Add D39

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		2007/8/18		Title	
				KB /SW Conn.	
				Size	
				Document Number	
				JFWXX M/B LA-3961P Schematic	
				Date	
				Thursday, September 06, 2007	
				Sheet	
				32 of 49	
				Rev	
				0.1	



JP12

1
2
3
4
5
6
7
8
GND
9

TP_CLK
TP_DATA
+5VS
GND

ACES_85201-06051
ME@

+5VS
C189
0.1U_0402_16V4Z

TP_CLK
TP_DATA
D15
@
PSOT24C_SOT23

Update Footprint

[illegible]

The schematic shows two USB signals being swapped at the connector level:

- R582**: A blue zigzag wire labeled "2" connects **USB20_N1_2** to pin 2 of **JP56**.
- R581**: A red zigzag wire labeled "2" connects **USB20_P1_2** to pin 1 of **JP56**.

Other labels near the connector include:

- BT ACTIVE**
- WLAN ACTIVE**
- BT ON LED**
- USB20_N1_2 R**
- USB20_P1_2 R**
- +BT_VCC_1O**
- ACES_87122-080**
- ME@**

A large red circle highlights the connection area.

Diagram illustrating the connection of the ACES_85201-1005N connector (JP57) to the system power and data lines.

Pin Connections:

- Pin 1: +3VS
- Pin 2: CLK_PCI_DB
- Pin 3: LPC_AD0
- Pin 4: LPC_AD1
- Pin 5: LPC_AD2
- Pin 6: LPC_AD3
- Pin 7: LPC_FRAME#
- Pin 8: LPC_FRAME#
- Pin 9: PCI_RST#
- Pin 10: PCI_RST#
- Pin 11: Common bus for pins 19, 24, 26, 28, 29, 30, 31
- Pin 12: GND

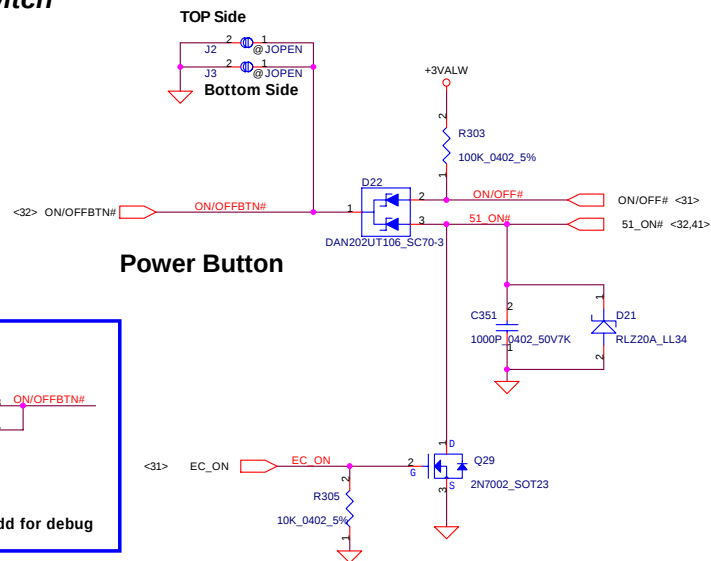
Resistor and Capacitor Connections:

- Resistor (576) connected between Pin 1 and Pin 2.
- Capacitor (0.1uF) connected between Pin 2 and Pin 3.

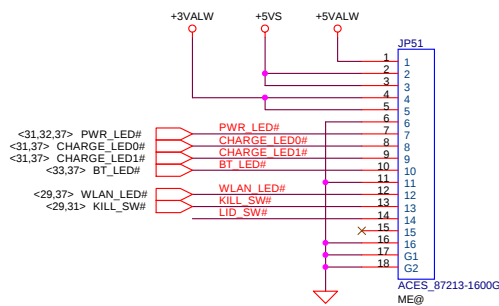
Pin configuration diagram for the ACES_05201-2005 ME0 connector. The diagram shows 21 pins connected to various signals. Pin 1 is +5V, Pin 3 is +3V, Pin 6 is CLK_14M_SIO, Pin 10 is LPC AD0, Pin 11 is LPC AD1, Pin 12 is LPC AD2, Pin 13 is LPC AD3, Pin 14 is LPC FRAME#, Pin 15 is LPC DRQ0#, Pin 16 is PCI_RST#, Pin 17 is CLK_PCI_DB, Pin 18 is SERIRQ, Pin 19 is an unconnected pin, Pin 20 is an unconnected pin, and Pin 21 is an unconnected pin. The CLK_14M_SIO signal is highlighted with a red oval.

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				Size B	Document Number	Rev 0.1
				JFWXX M/B LA-3961P Schematic		
Date:				Thursday, September 06, 2007	Sheet 33 of 49	

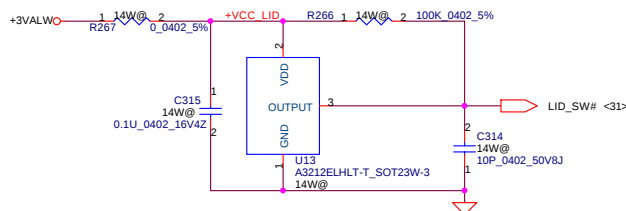
ON/OFF switch



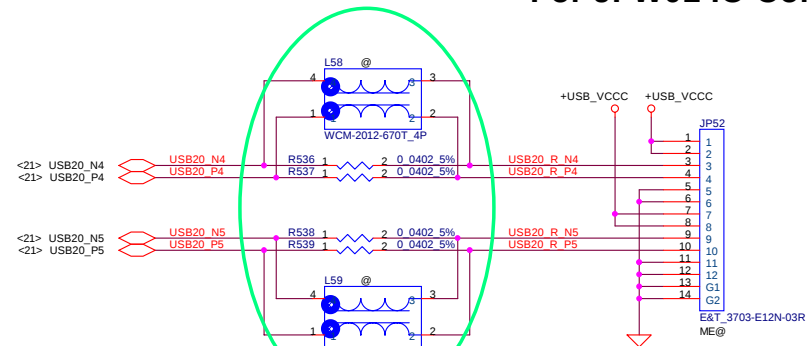
Front LED Board



Lid Switch



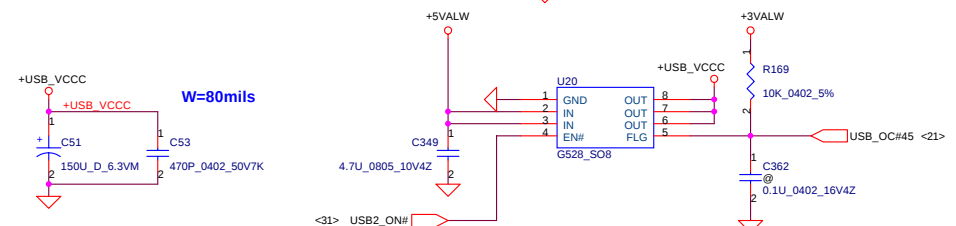
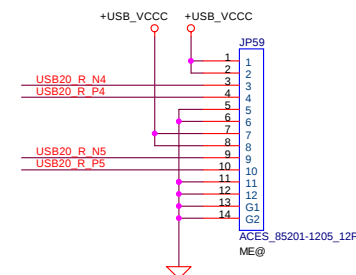
For JFW01 IO Conn.



For EMI => Add R536,R537,R538,R539 (SD028000080) ,L58,L59 (SM070000I00)
Swap L58,L59 Pin 1 & Pin 4 , Pin 2 & Pin 3

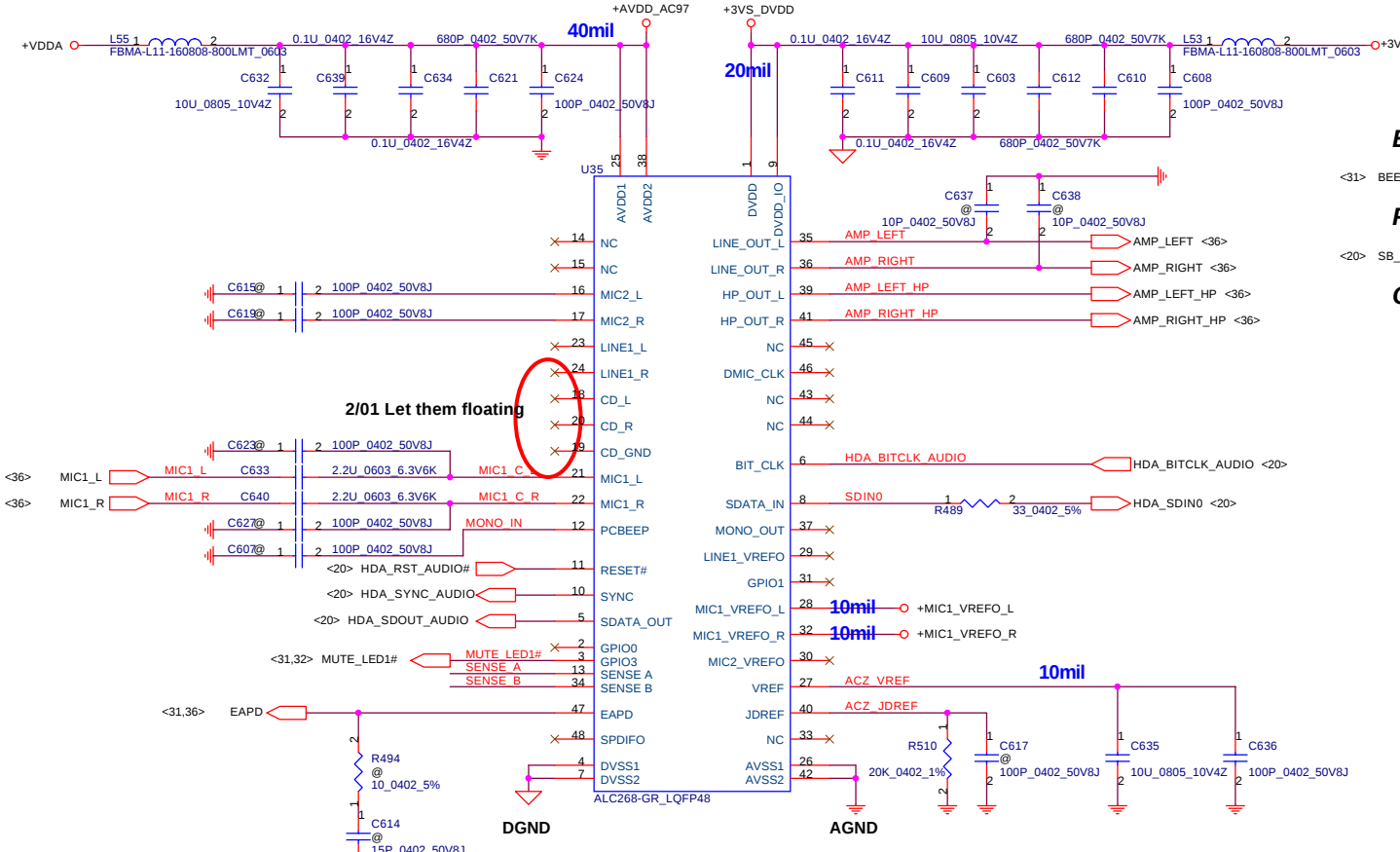
7/30 change L58,59 to SM070000K00 by EMI request

For JFW91 IO Conn.



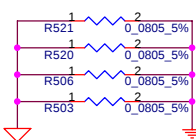
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title PWROK/LID/Front/IO Board		
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				JFWXX M/B LA-3961P Schematic		
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HD Audio Codec



Sense Pin	Impedance	Codec Signals	Funncion
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
SENSE B	5.1K	PORT-D (PIN 35, 36)	LINE Out
	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

Moat Bridge

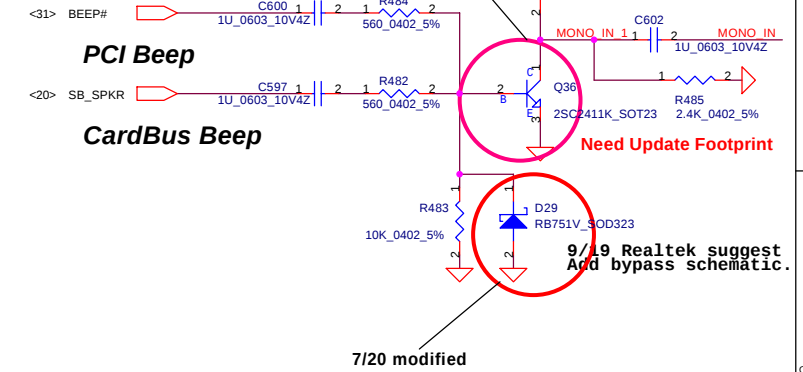


9/22 Update footprint, Need to check

EC Bleep

PCI Bleep

CardBus Bleep

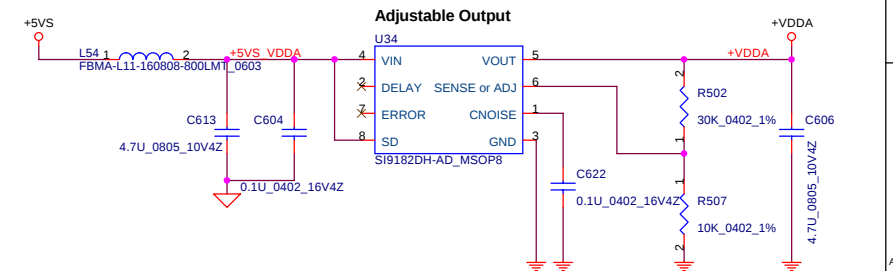


Need Update Footprint

9/19 Realtek suggest And bypass schematic.

7/20 modified

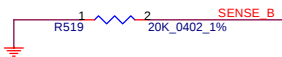
Regulator for CODEC



SENSE FOR Ext. Mic.



SENSE FOR Solo Int. Mic.



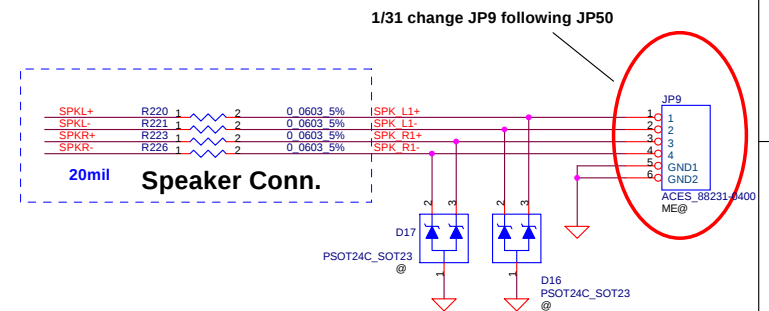
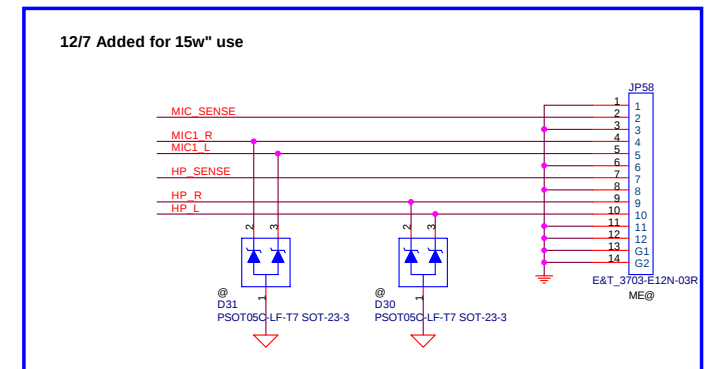
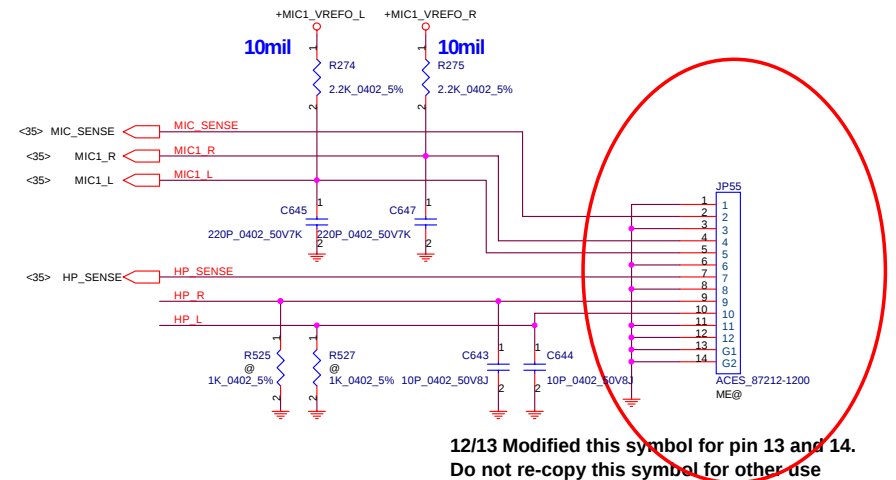
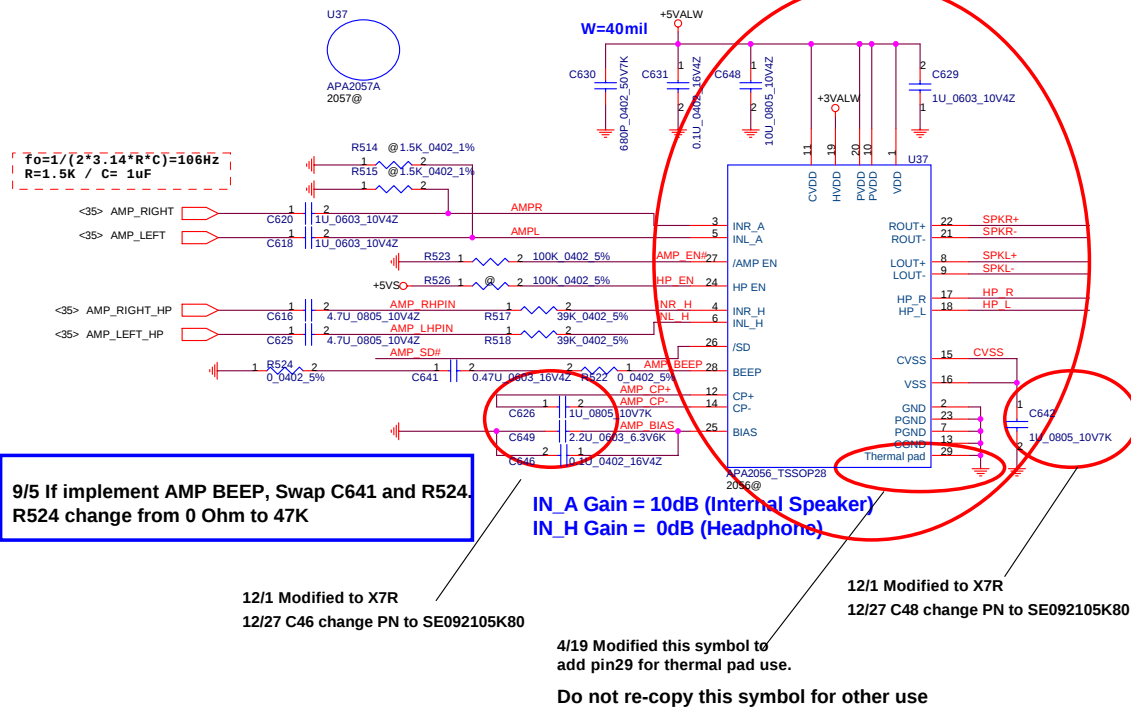
SENSE FOR HP



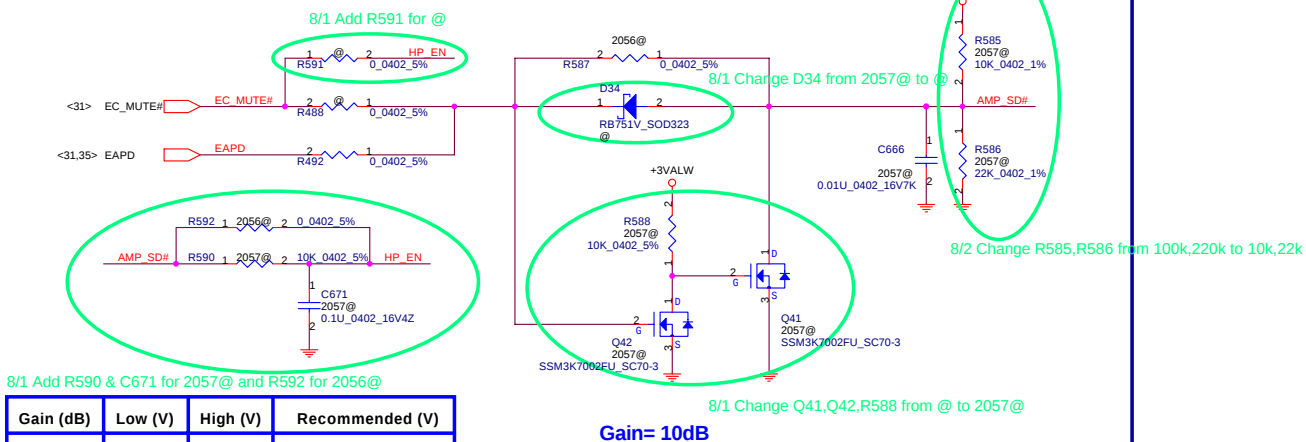
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				Custom	LA-3541P	0.1
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APA2056 SPK/HP Amplifier

7/20 Add U37 for APA2057A SA00001QD00



7/20 Add below circuit for APA2057 gain tuning use



Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82
15	4.02	4.07	4.05

+5VALW assume equal 5.1V
10 dB ---> $5.1 \times 220 / 320 = 3.5$

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Title		AMP/VR/Audio Jack/MIC				
Size	Document Number				Rev	
Custom	LA-3541P				0.1	
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Diagram illustrating the MDC Rev1.5 connector (JP2) and its connections:

- Connector Pins (JP2):**
 - 1: GND1
 - 3: IAC_SDATA_OUT
 - 5: GND2
 - 7: IAC_SYNC
 - 9: IAC_SDATA_IN
 - 11: IAC_RESET#
 - 12: IAC_BITCLK
- External Connections:**
 - Pin 1: Connected to HDA_SDOOUT_MDC.
 - Pin 3: Connected to HDA_SYNC_MDC.
 - Pin 5: Connected to HDA_SDIN1.
 - Pin 7: Connected to HDA_RST_MDC#.
 - Pin 9: Connected to IAC_SYNC.
 - Pin 11: Connected to IAC_SDATA_IN.
 - Pin 12: Connected to IAC_RESET#.
- Internal Connections:**
 - Pin 1: Connected to Pin 2 via a 330k resistor (R306).
 - Pin 2: Connected to Pin 1 via a 22pF capacitor (C352).
- Signal Labels:**
 - HDA_SDOOUT_MDC
 - HDA_SYNC_MDC
 - HDA_SDIN1
 - HDA_RST_MDC#
 - IAC_SYNC
 - IAC_SDATA_IN
 - IAC_RESET#
 - IAC_BITCLK
 - IAC_BITCLK_MDC
- Other Labels:**
 - 20mil
 - 3V3VALW
 - ACES_88018-124G
 - ME@

9/3 change R531,C30,R191,R201,R578 from CAM@ to mount

For EMI => Add L60 (SM070000100)

7/30 change L60 to SM070000K00 by EMI request

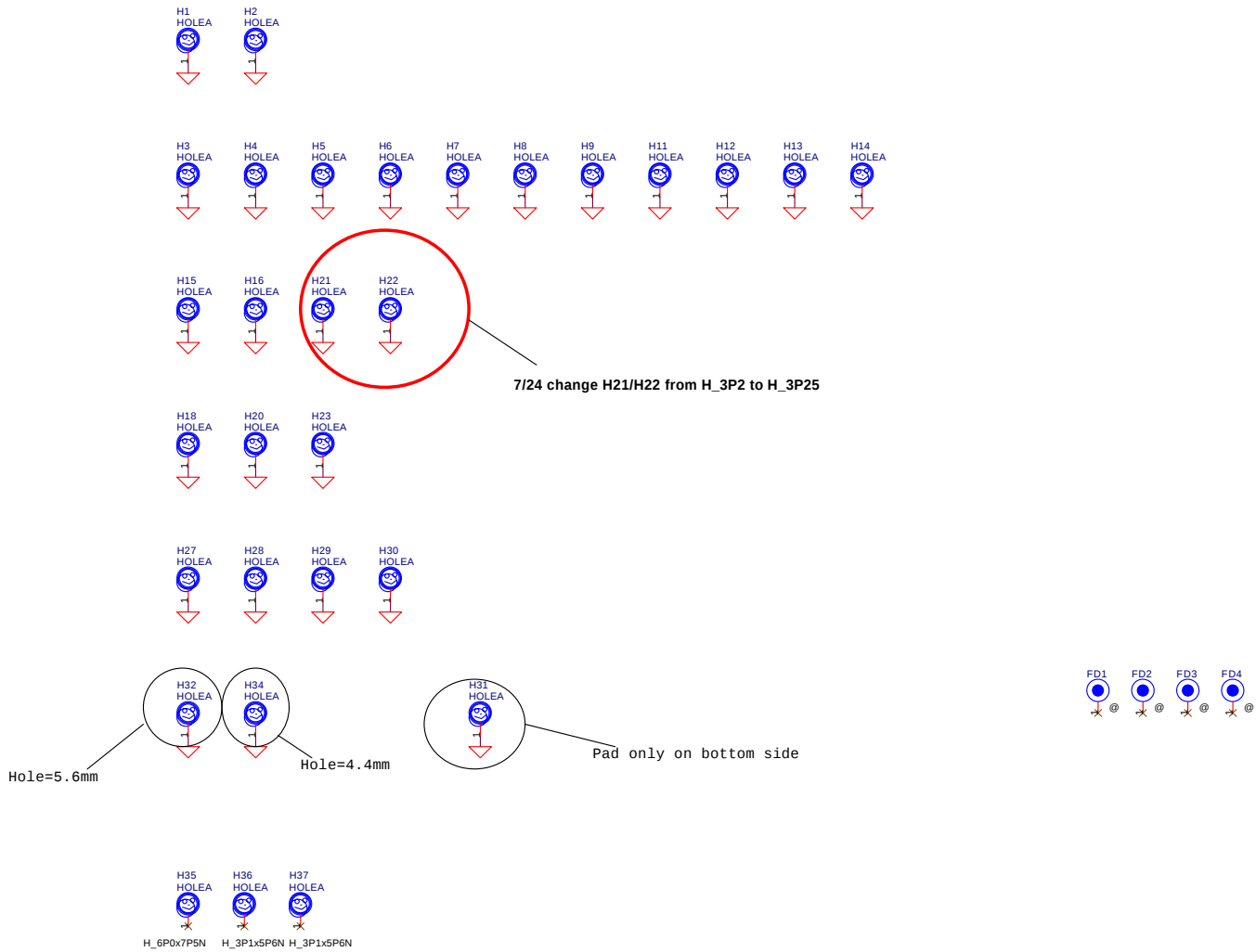
For EMI => Change D9 from SC300000100 to SC300000P00

R269 14W@
 4.3K_0402_5%
 +5VALW@ 1 2
 HT-191NB_BLUE_0603
 14W@
 LED1
 PWR_LED# <31,32,34>

R273 14W@
 3.3K_0402_5%
 +5VALW@ 1 2
 R272 14W@
 3.3K_0402_5%
 +5VALW@ 1 2
 HT-297UD/CB_BLUE/AMB_0603
 14W@
Blue&Amber
 LED3
 CHARGE_LED0# <31,34>
 CHARGE_LED1# <31,34>

R270 14W@
 3.3K_0402_5%
 +5VS 1 2
 R271 14W@
 3.3K_0402_5%
 +5VS 1 2
 HT-297UD/CB_BLUE/AMB_0603
 14W@
Blue&Amber
 LED2
 BT_LED# <33,34>
 WLAN_LED# <29,34>

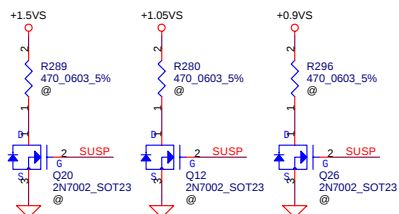
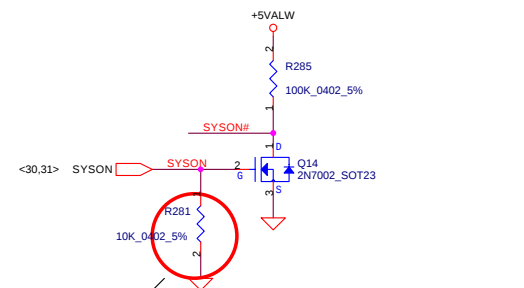
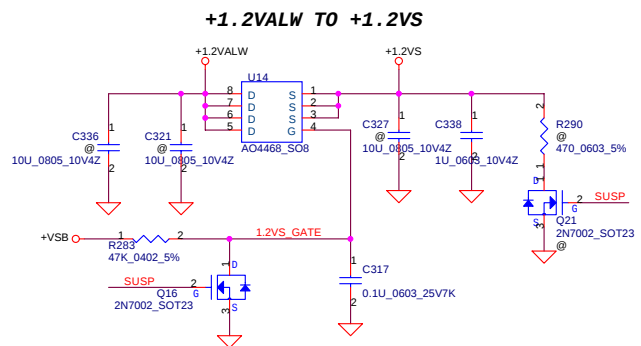
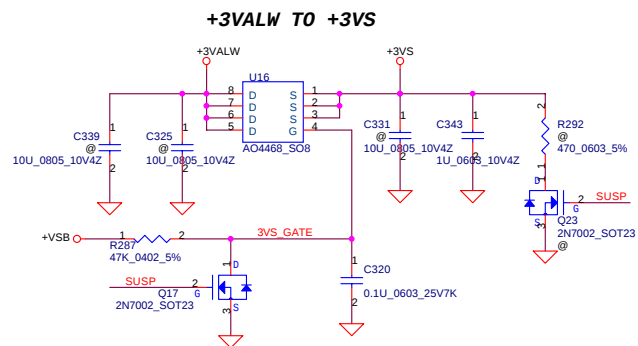
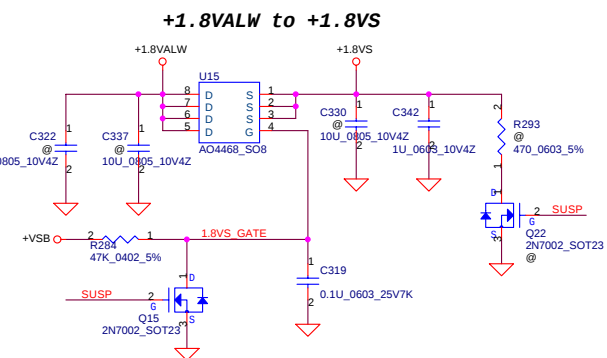
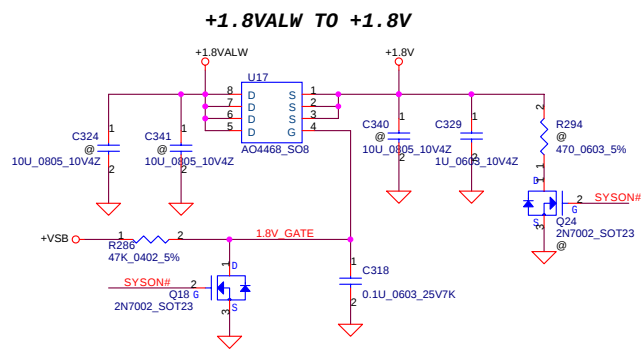
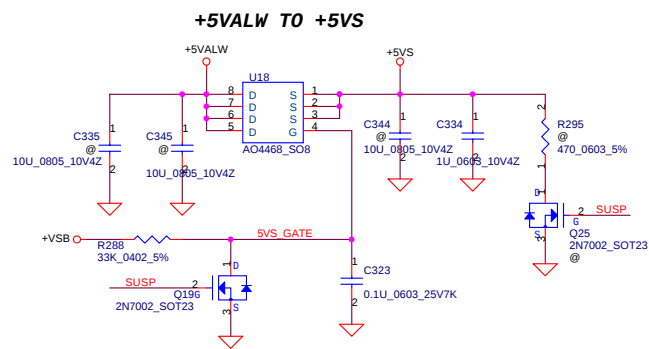
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				LED/MDC/CAMERA				
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				JFWXX M/B LA-3961P Schematic				
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		FAN & Screw Hole			
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				Date: Thursday, September 06, 2007	Rev 0.1
				Sheet 39 of 49	1



7/24 Change R281 from 100K to 10K

<26,30,31,43,46,47> SUSP#

3/14 Change R16 from 100K to 10K

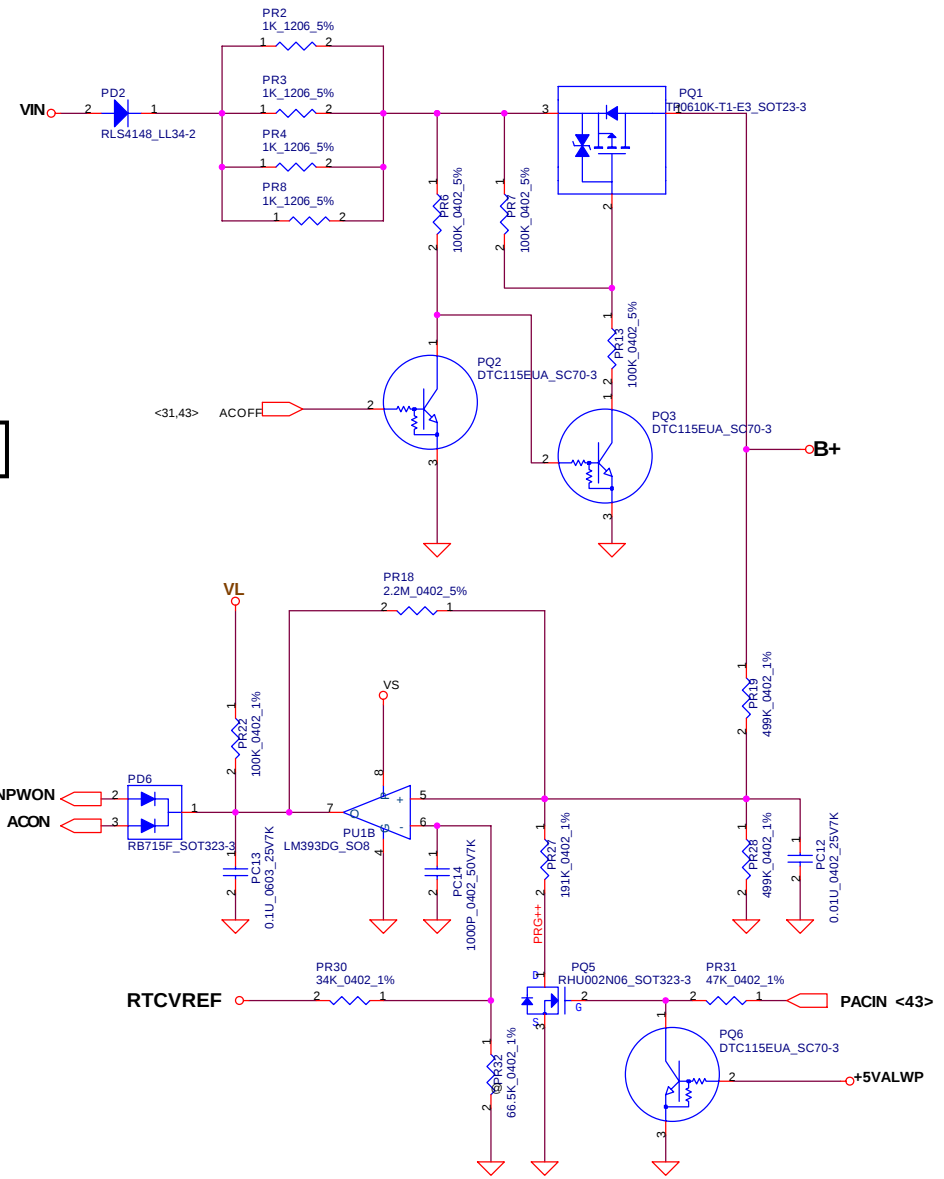
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	DC Interface	
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				Date: Thursday, September 06, 2007	Rev 0.1
				Sheet 40 of 49	

Vin Detector
High 18.764
Low 17.745

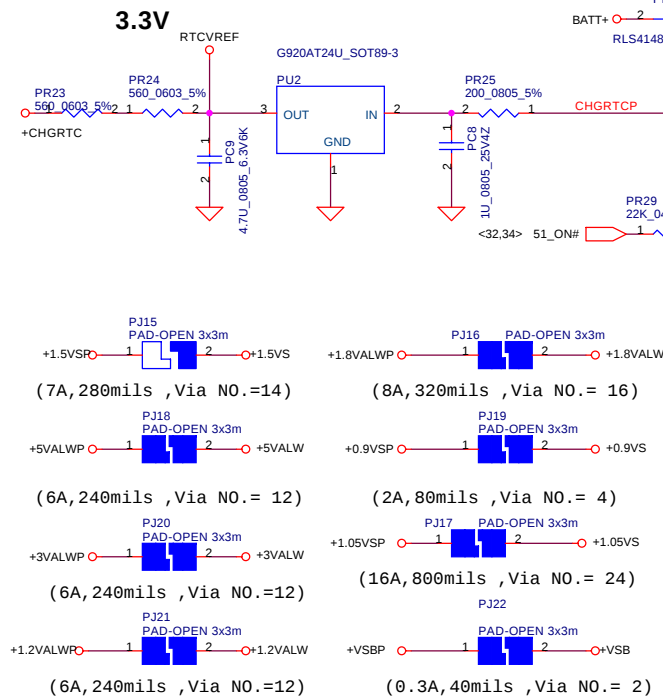
High	18.764	17.901	17.063
Low	17.745	16.9	16.03

	Precharge detector		
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

	Precharge detector		
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

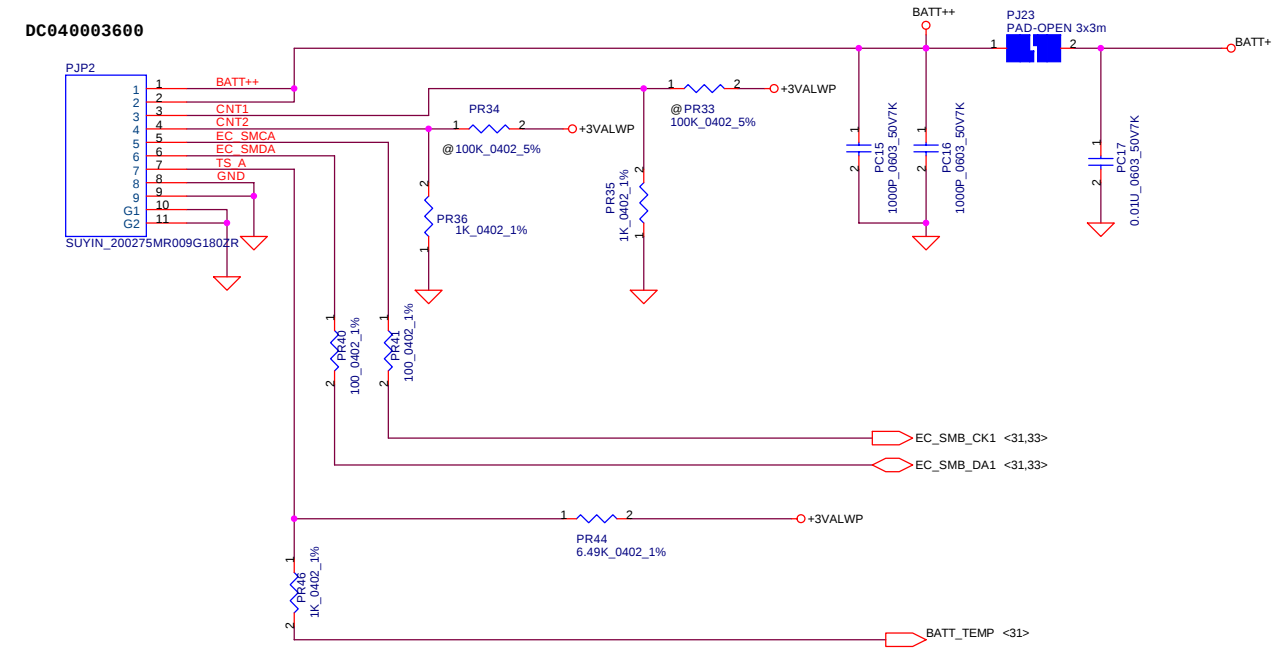


PACIN <43>



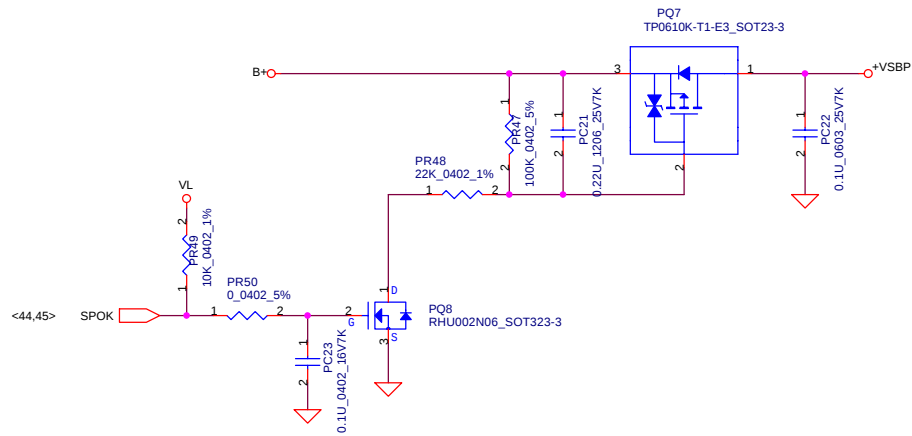
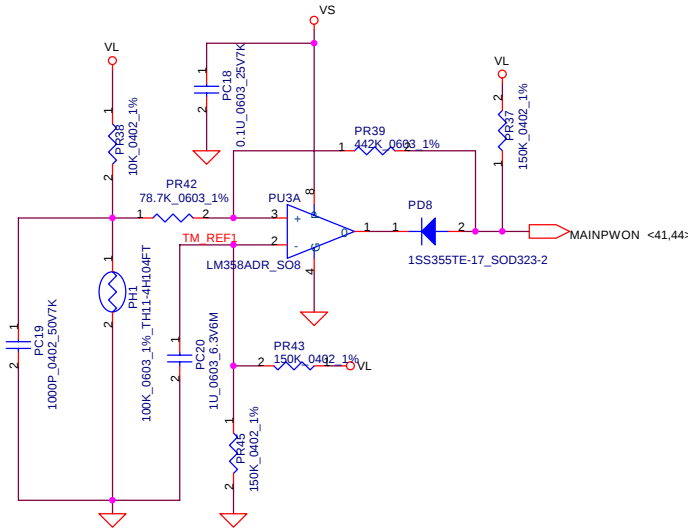
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DC040003600



2/16 Change to 89 degree C for thermal request

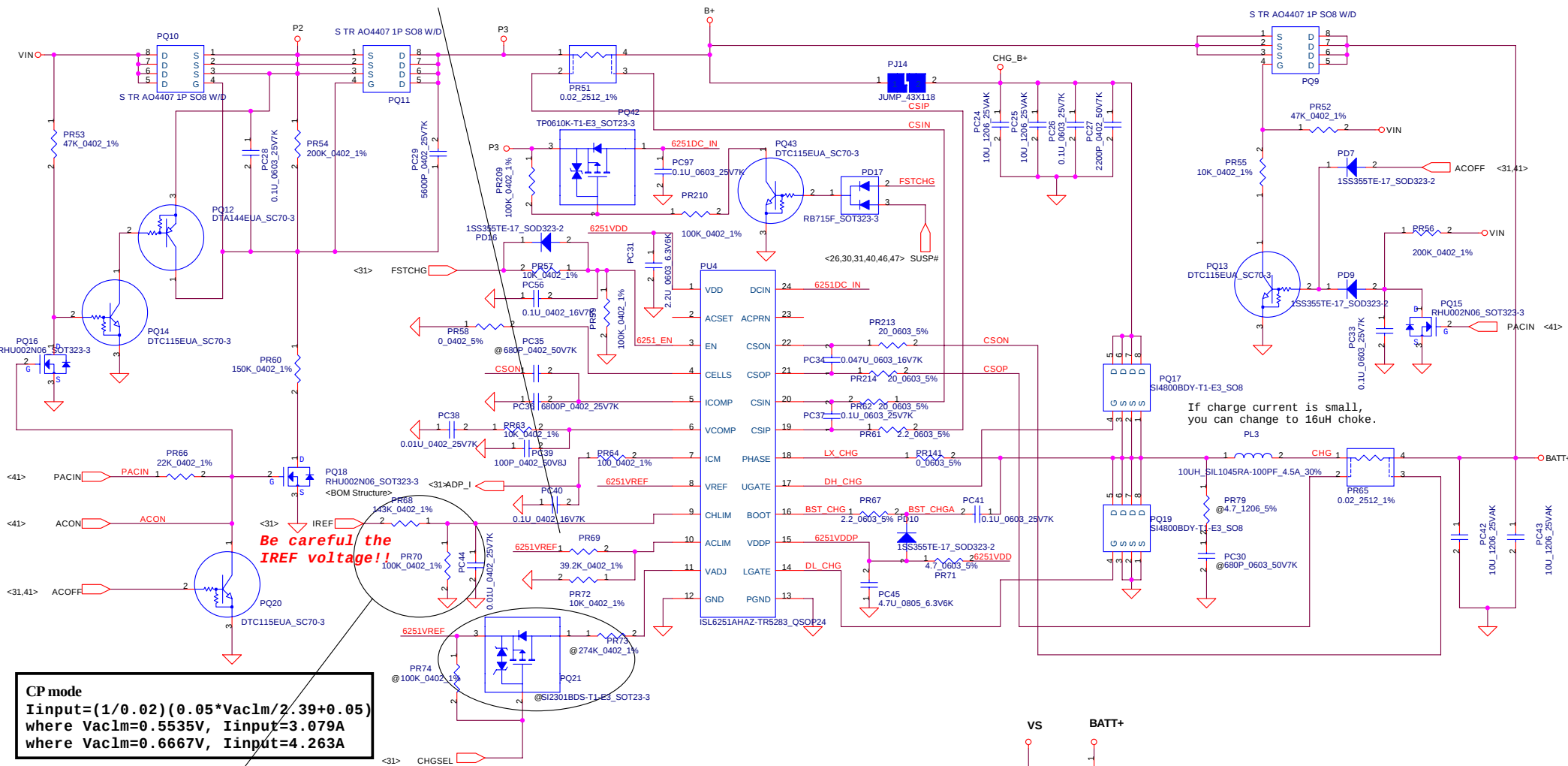
PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR74=39.2K, CP=3.079A

ADP_I = 19.9*Iadapter*Rsense



Be careful the IREF voltage!!

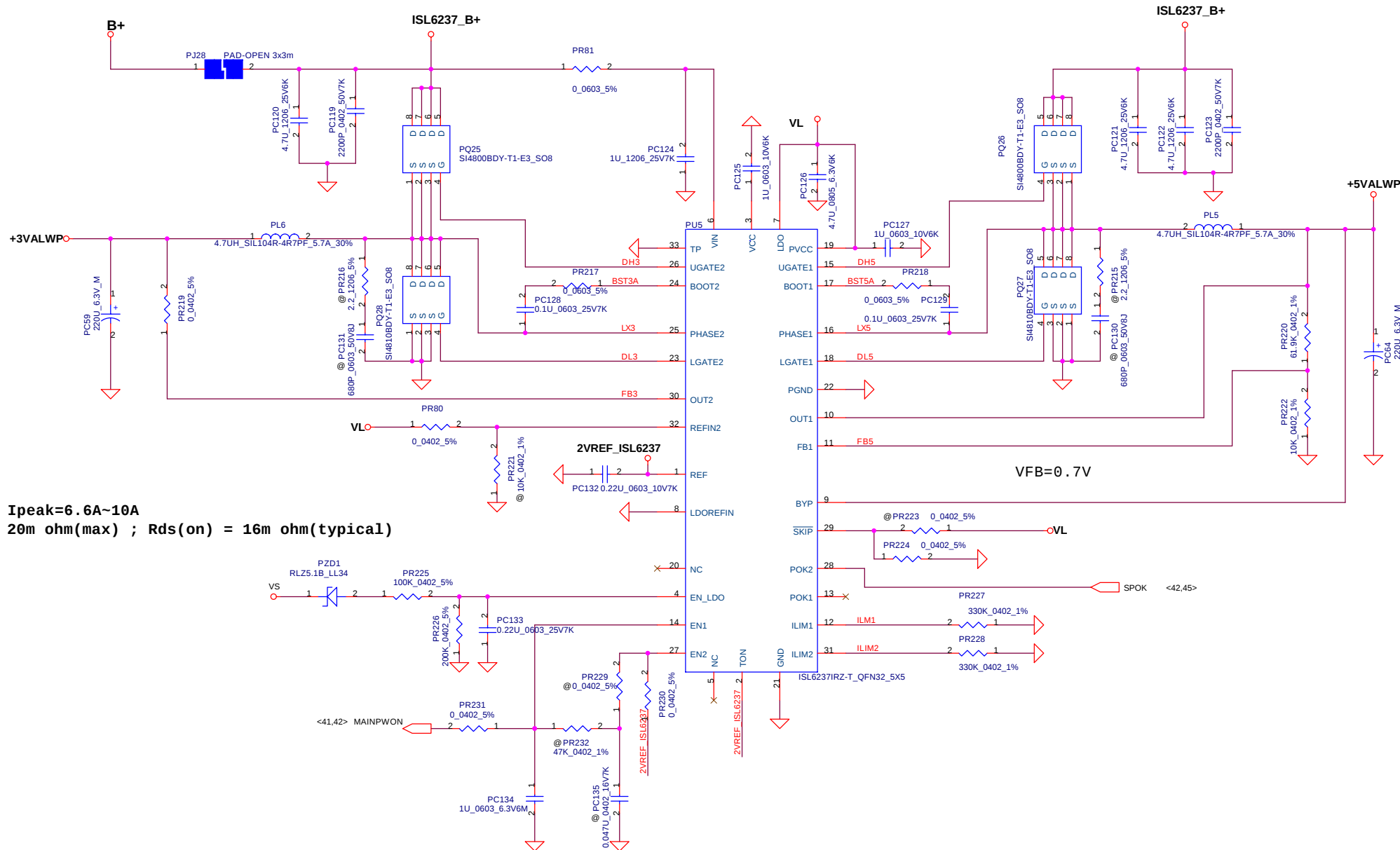
CP mode
 $I_{input} = (1/0.02)(0.05 * V_{ac1m}/2.39 + 0.05)$
 where $V_{ac1m} = 0.5535V$, $I_{input} = 3.079A$
 where $V_{ac1m} = 0.6667V$, $I_{input} = 4.263A$

CC=0.6~3.4A
 $V_{CHLM} = 0.24V \sim 1.36V$
 $I_{REF} = 0.972 * I_{charge}$
 $I_{REF} = 0.5832V \sim 3.3V$

If this area float, Charge voltage is 4.2V/cell

BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V

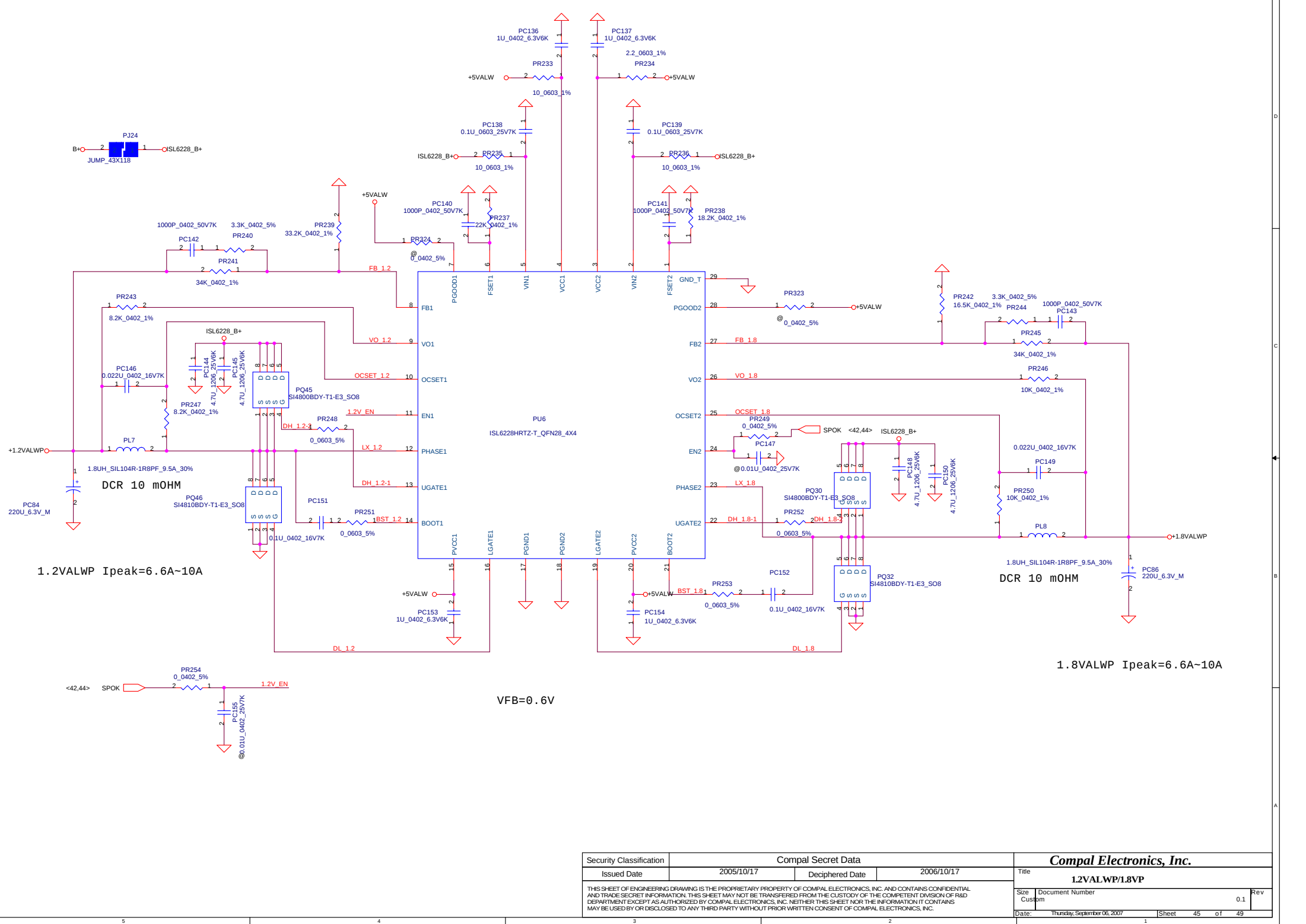
OVP voltage :
 LI-3S : 13.50V -- BATT-OVP=1.5V
 BATT-OVP=0.111*BATT+



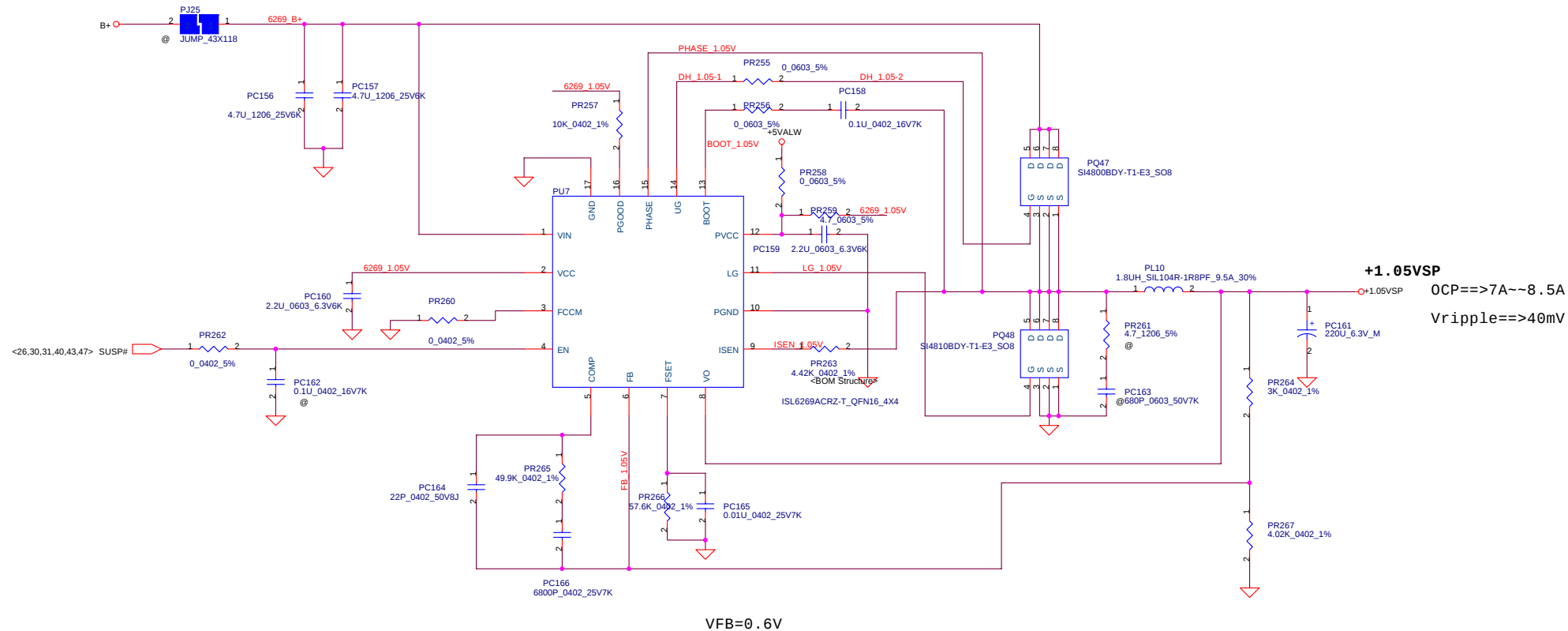
3.3VALWP Ipeak=6.6A~10A
Rds(on) = 20m ohm(max) ; Rds(on) = 16m ohm(typical)

5VALWP Ipeak=6.6A~10A
Rds(on) = 20m ohm(max) ; Rds(on) = 16m ohm(typical)

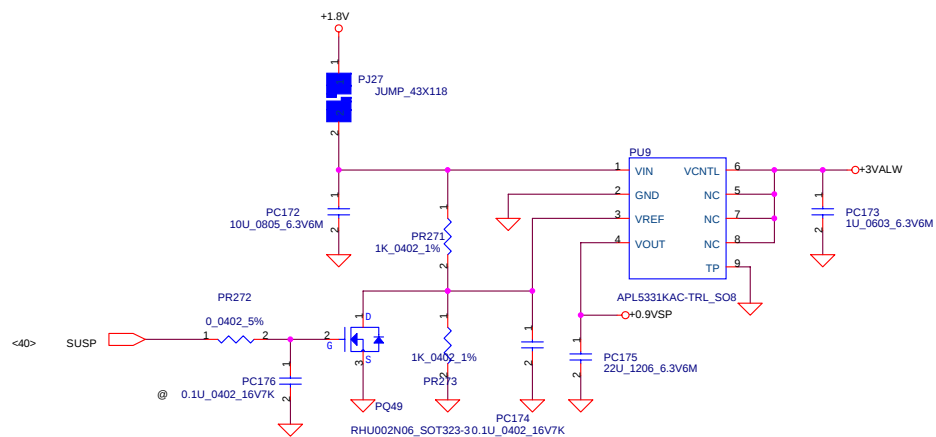
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				+5VALWP/+3VALWP	
				0.1	



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								1.2VALWP/1.8VP			
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