

Compal Confidential

ZIWB2/ZIWB3/ZIWE1 DIS M/B Schematics Document

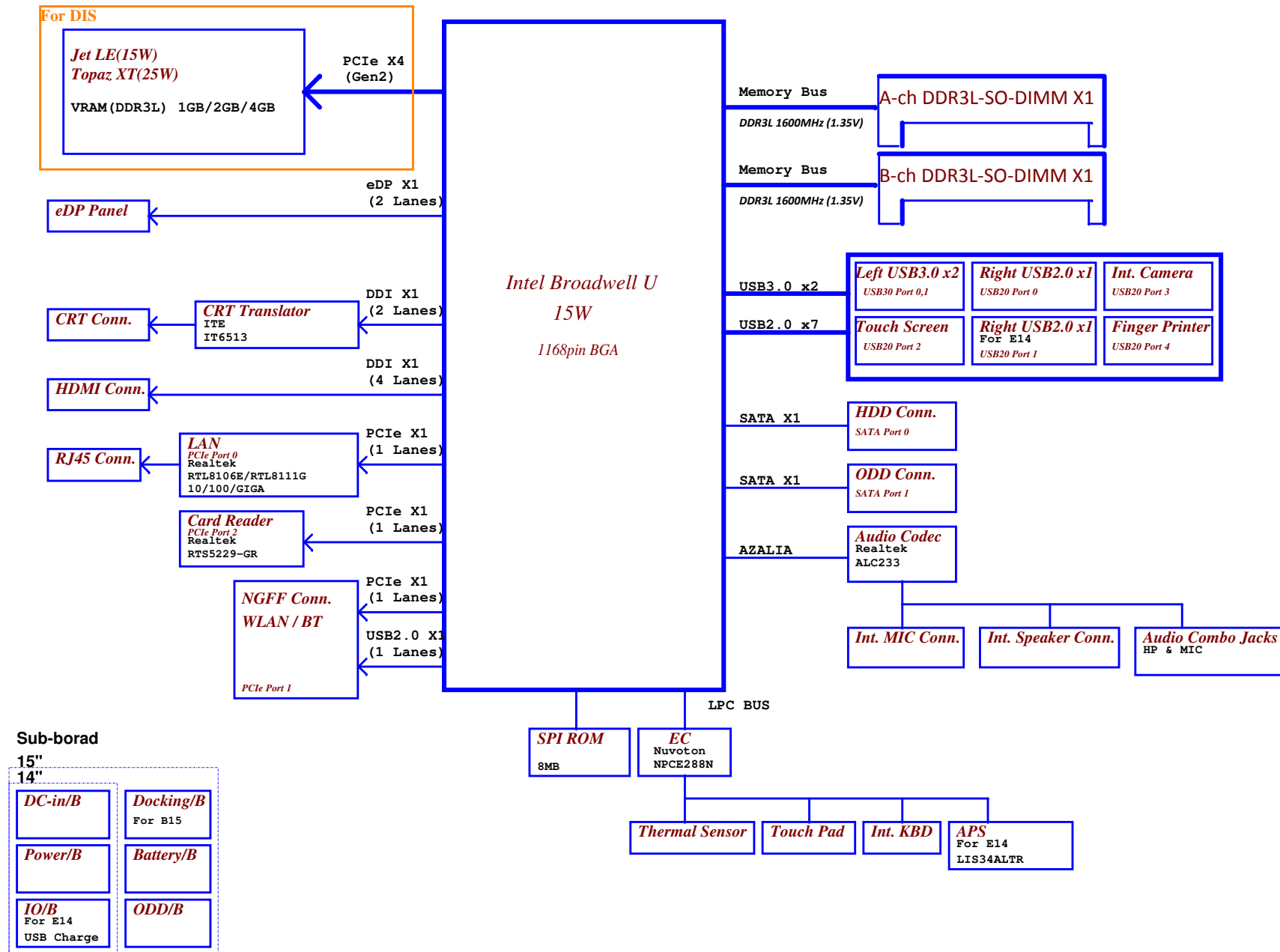
Intel Boardwell U Processor with DDR3L

2014-02-10

LA-B092P

REV : 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title Cover Page	
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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1_05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

USB Port Table

	USB 2.0 Port	3 External USB Port
EHC11	UHCI0	0 USB Port (Left Side) USB3.0
		1 USB Port (Left Side) USB3.0
	UHCI1	2 Touch Screen
		3 Camera
	UHCI2	4
EHC12	UHCI3	5
		6
	UHCI4	7
		8
	UHCI5	9 USB Port (Right Side USB-BD)
		10 Mini Card(WLAN)
	UHCI6	11 Card Reader
		12
		13

BOM Structure Table

Item	BOM Structure
ZIWB2 (14")	B14@
ZIWB3 (15")	B15@
ZIWE1 (14")	E14@
CPU_SA00006SM20	15_4200U@
CPU_SA00007AM00	QFSY@
CPU_SA00006SU30	13_4100U@
CPU_SA000072Q10	13_4005U@
CPU_SA00006SX20	13_4010U@
LAN 10/100 Transformer	100@
LAN GIGA Transformer	GIGA@
LAN Switch mode	SWITCH@
LAN RTL8106E-CG	8106ELDO@
LAN RTL8111GS-CG	8111GLDO@
LAN RTL8106EUS-CG	8106ESW@
LAN RTL8111GUS-CG	8111GSW@
Audio 233	233@
Audio 233VB	233VB@
For B15	Docking@
For B14, E14	NoDocking@
For Deep Sleep	DS3@
For No Deep Sleep	NoDS3@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NoISCT@
For Intel ZERO ODD	ZODD@
For No Intel ZERO ODD	NoZODD@
For Green CLK	GCLK@
For No Green CLK	NoGCLK@
For No Green CLK	NoGCLKDIS@
Green CLK IC For DIS	GCLKDIS@
Green CLK IC For UMA	GCLKUMA@
GPU support Single Rank	SR@
GPU support Dual Rank	DR@
GPU Jet LE	JET@
GPU Topaz XT	TOPAZ@
For DIS	PX@
For UMA	UMA@
Camera	COMS@
APS (G-sensor)	GS@
Touch Screen	TS@
HDMI	HDMI@
USB 2.0	USB2@
USB 3.0	USB3@
Full HD Panel (2 Lane)	FHD@
ENE EC 9012	9012@
HDMI Royalty	45@
Connector	ME@
VRAM indentify	X76@
Un-pop component for EMI	@EMI@
Un-pop component for ESD	@ESD@
DA600140000	PCB_14_DIS@
DA600141000	PCB_14_UMA@
DA600140100	PCB_15_DIS@
DA600141100	PCB_15_UMA@

Only in DIS Schematic

Only in DIS Schematic

No USE

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011x	Thermal Sensor	0100 1100

PCH SM Bus address

AMD-GPU SM Bus address

Device	Address	Device	Address
DDR_IDIMM1	1010 000x A0h	Internal thermal sensor	0100 0001 41h
DDR_IDIMM2	1010 010x A4h		

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	+3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	+3VGS	X	X	X	X	+3VS	+3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	+3VS	+3VS	X	X
PCH_SMLCLK PCH_SMLDATA	PCH +3VALW	X	X	X	X	X	X	X
SMLCLK SMLDATA	PCH +3VALW	+3VGS	X	+3VS	X	X	+3VS	X

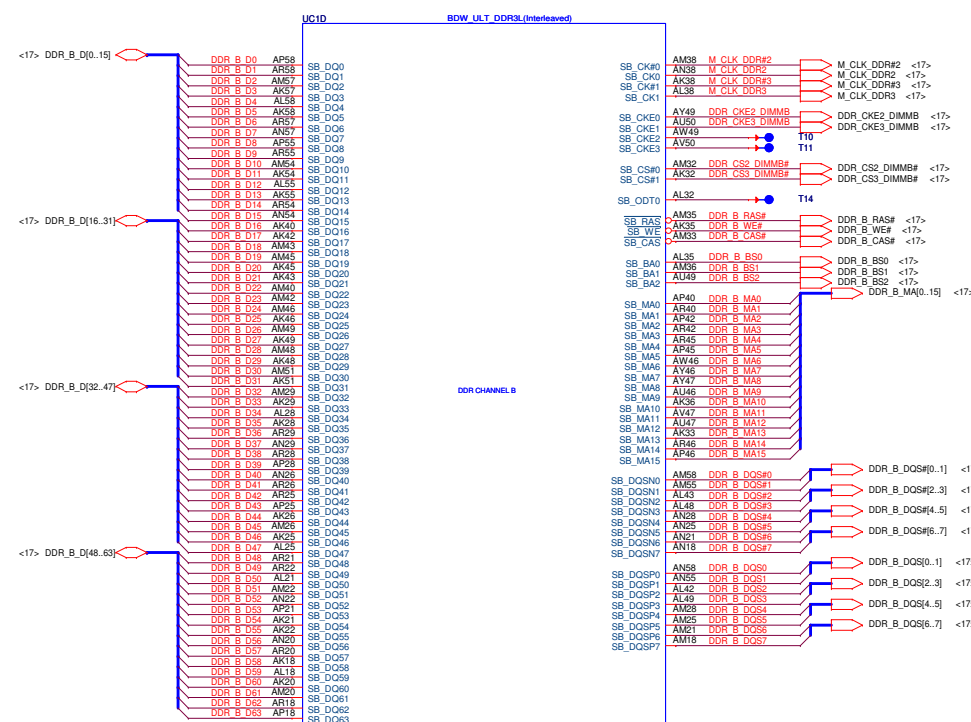
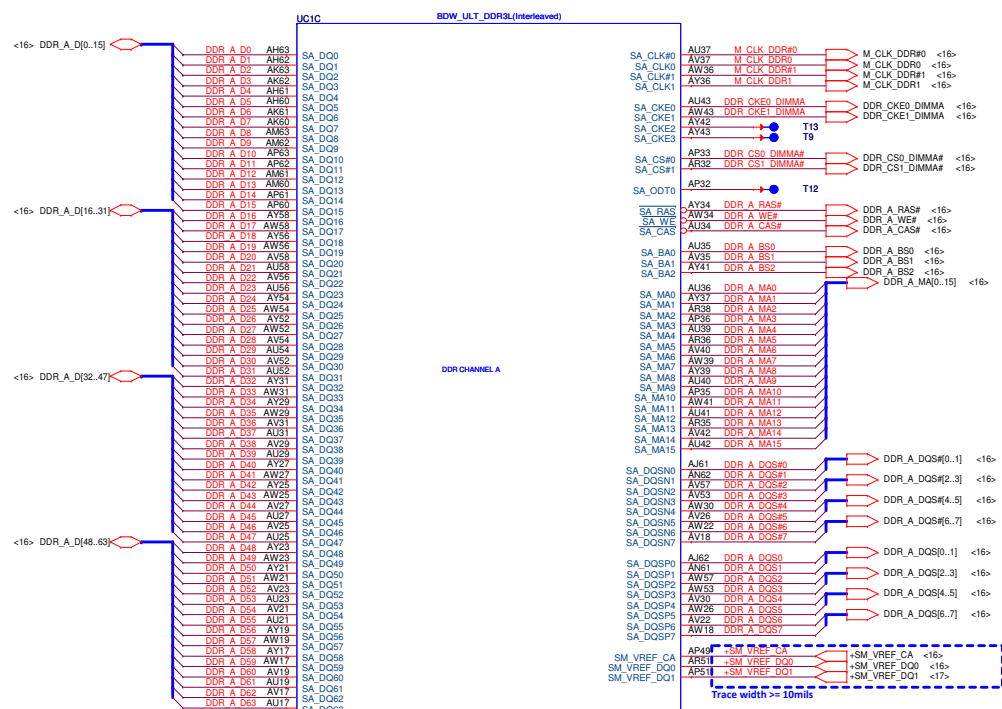
STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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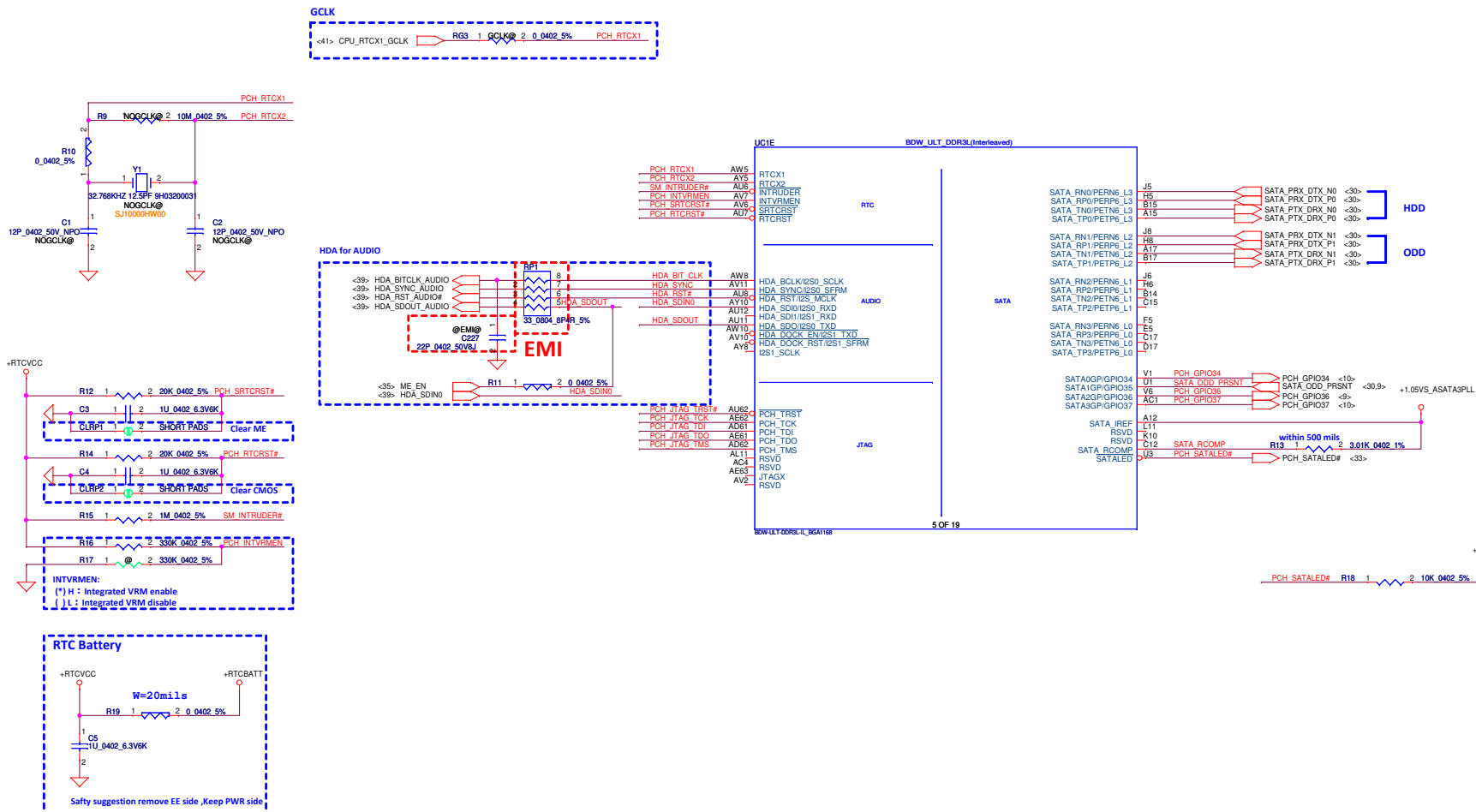
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A				A																																								
<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td>Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2011/06/24</td><td>Deciphered Date</td><td>2012/07/12</td><td>Title</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size</td></tr><tr><td colspan="4"></td><td>Document Number</td></tr><tr><td colspan="4"></td><td>Rev</td></tr><tr><td colspan="4"></td><td>1.0</td></tr><tr><td colspan="4"></td><td>Date: Tuesday, February 18, 2014</td></tr><tr><td colspan="4"></td><td>Sheet 4 of 53</td></tr></table>					Security Classification	Compal Secret Data			Compal Electronics, Inc.	Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size					Document Number					Rev					1.0					Date: Tuesday, February 18, 2014					Sheet 4 of 53
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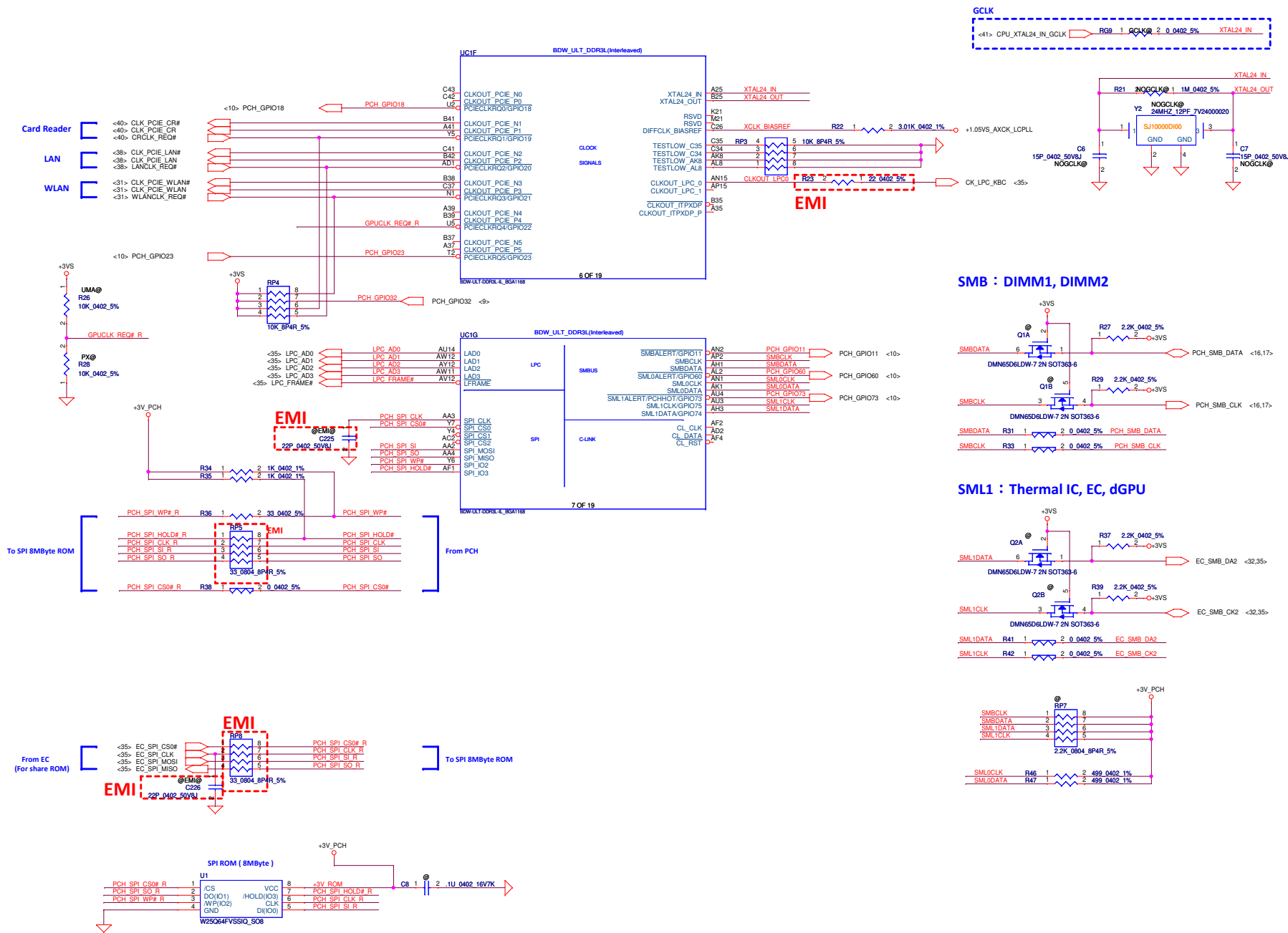
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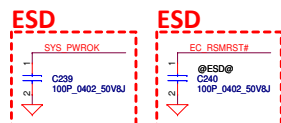
Interleaved Memory



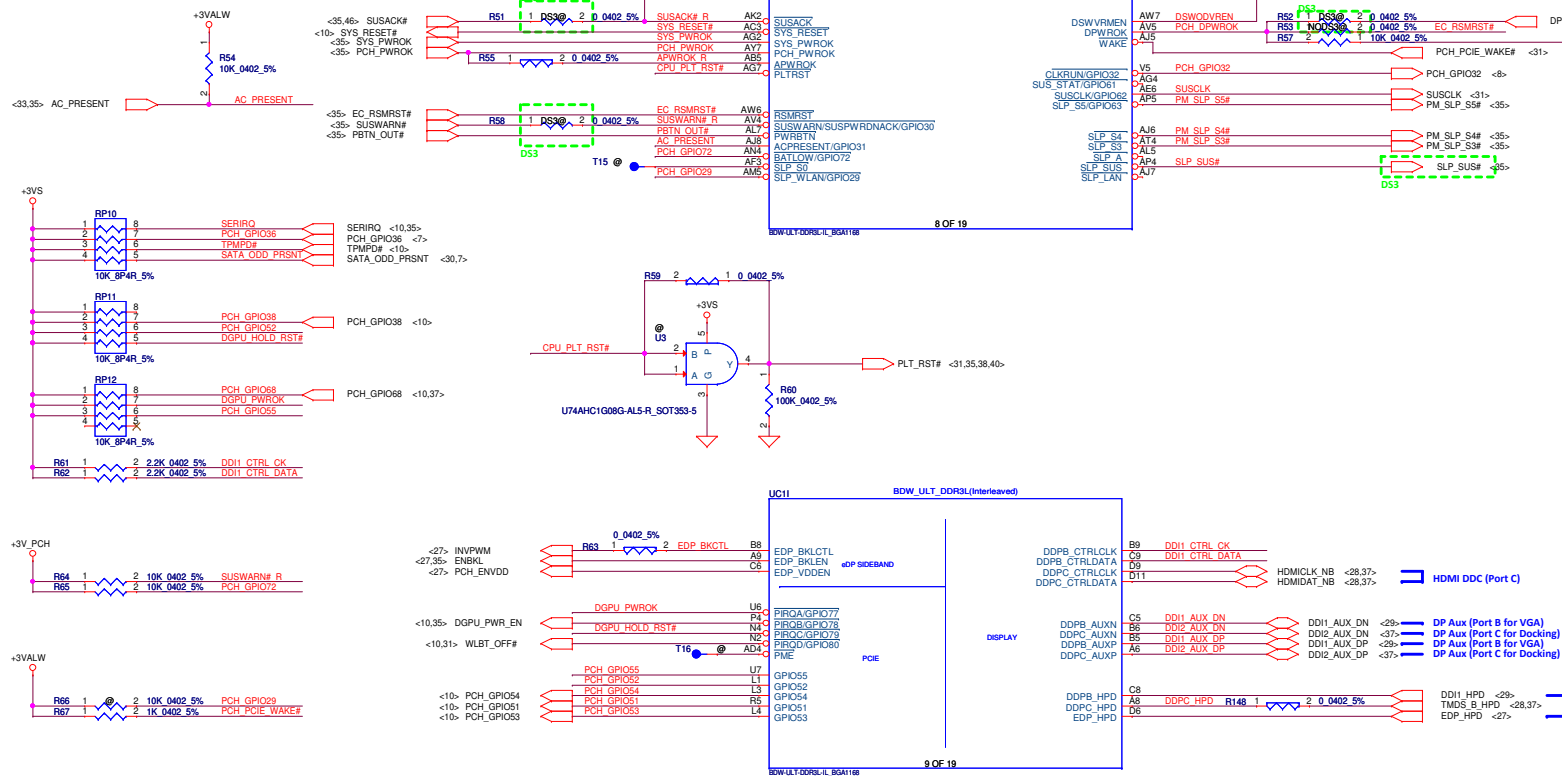
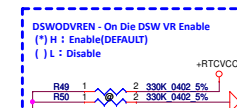
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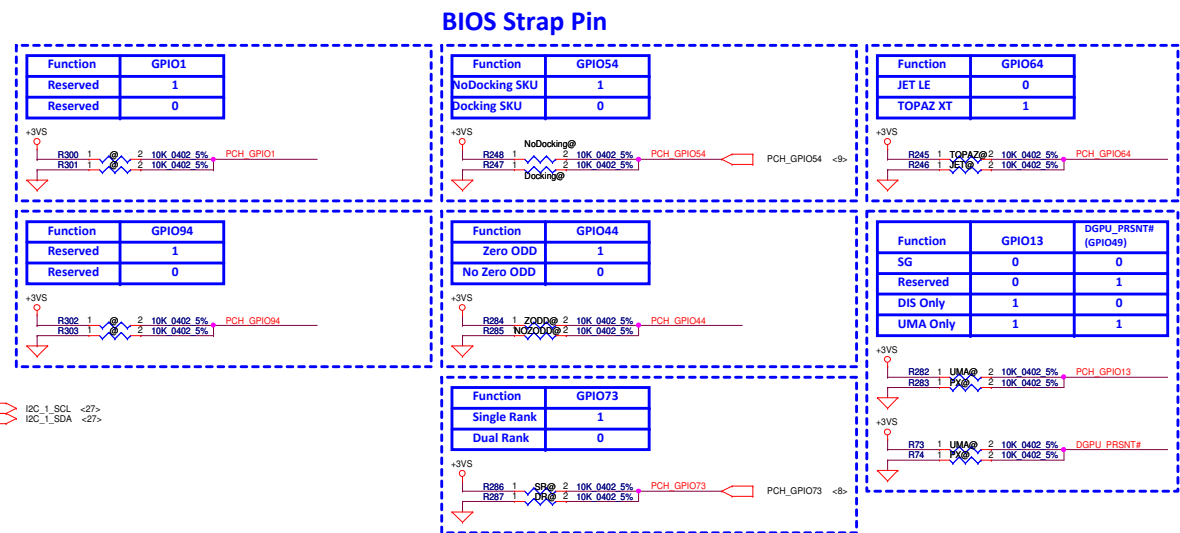
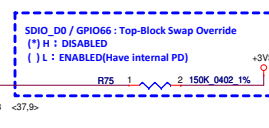


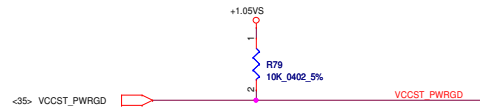




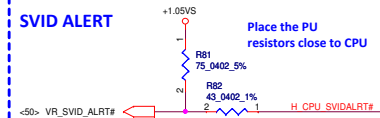
Function	(X)DS3 (X)SBA	(O)DS3 (X)SBA	(X)DS3 (O)SBA
R51	X	O	X
R55	O	O	X
R56	X	X	O
R58	X	O	X
R52	X	O	X
R53	O	X	O





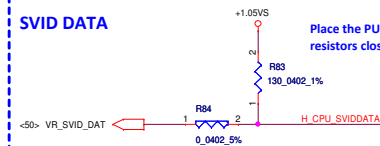


SVID ALERT

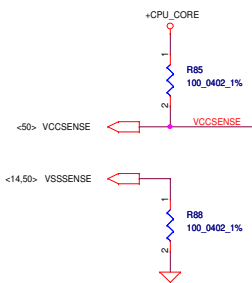


Place the PU resistors close to CPU

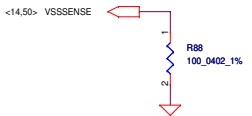
SVID DATA



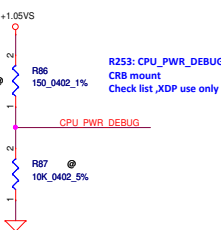
Place the PU resistors close to CPU



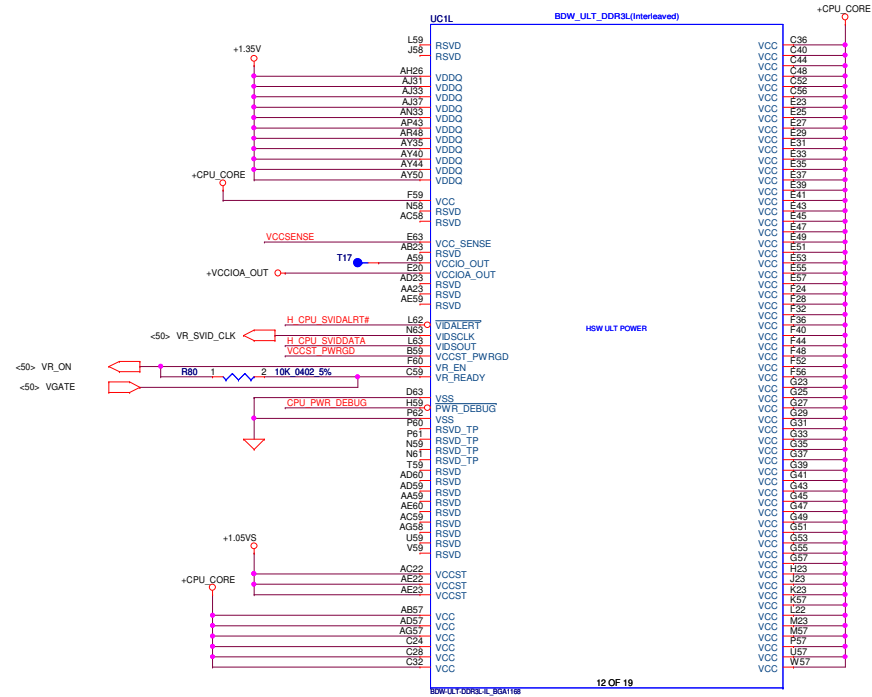
PU resistor should be close to CPU



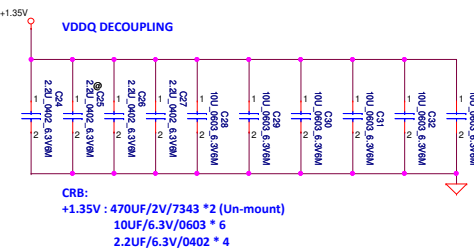
PD resistor should be close to CPU



R253: CPU_PWR_DEBUG
CRB mount
Check list_XDP use only

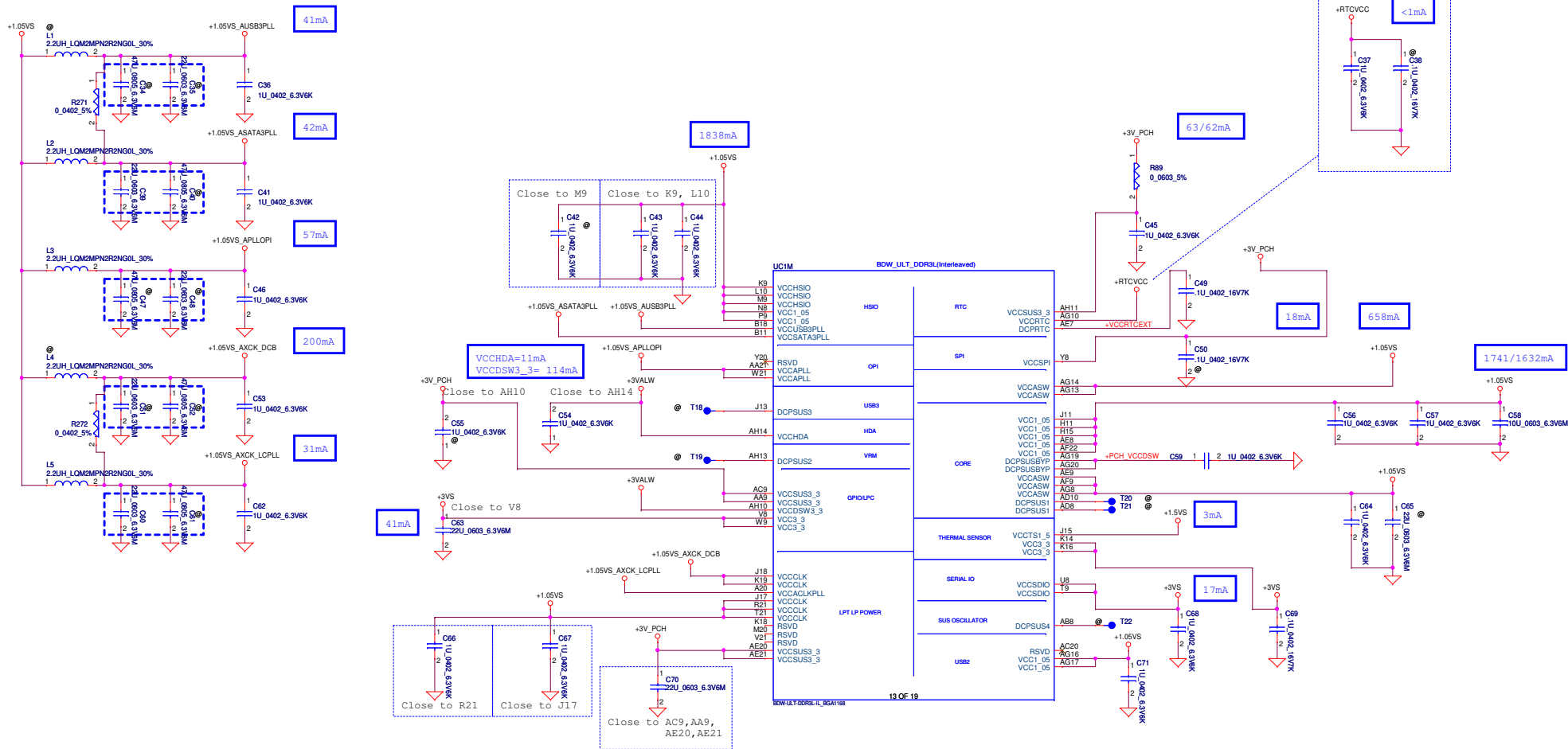


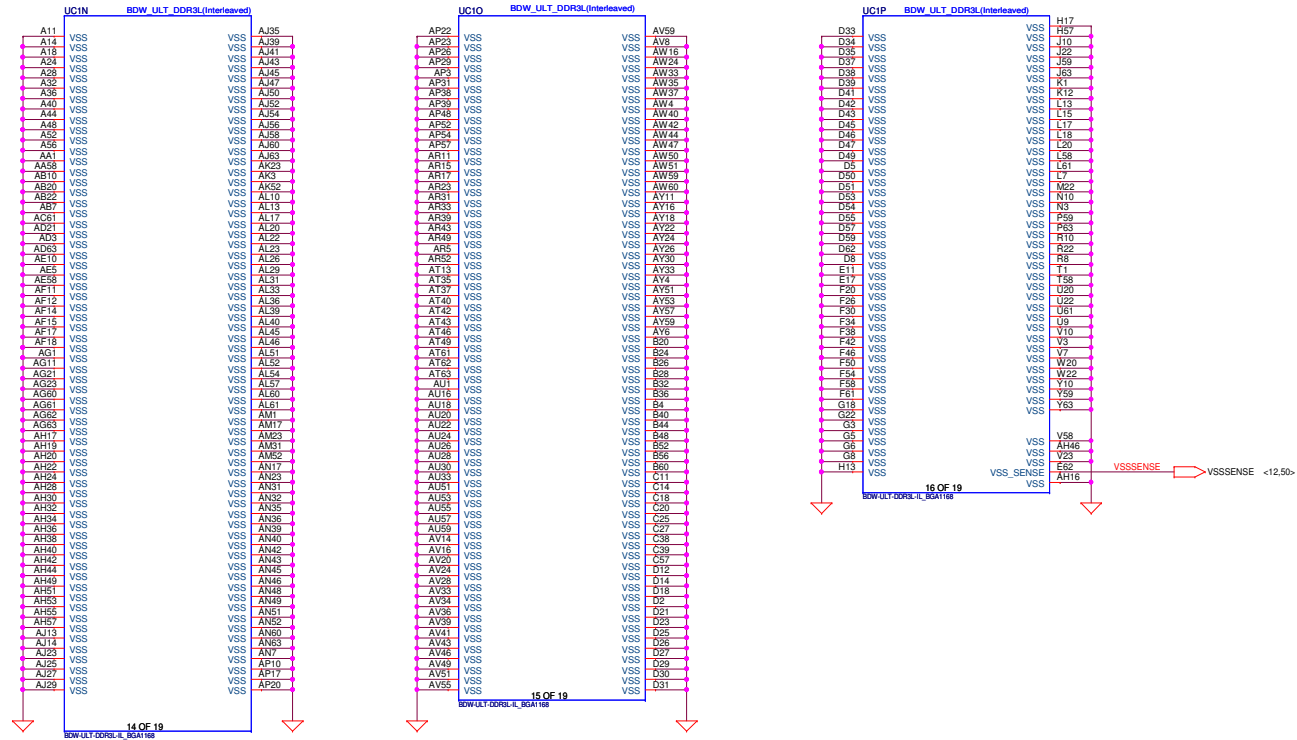
VDDQ DECOUPLING

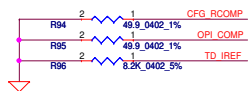


CRB:
+1.35V : 470UF/2V/7343 * 2 (Un-mount)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

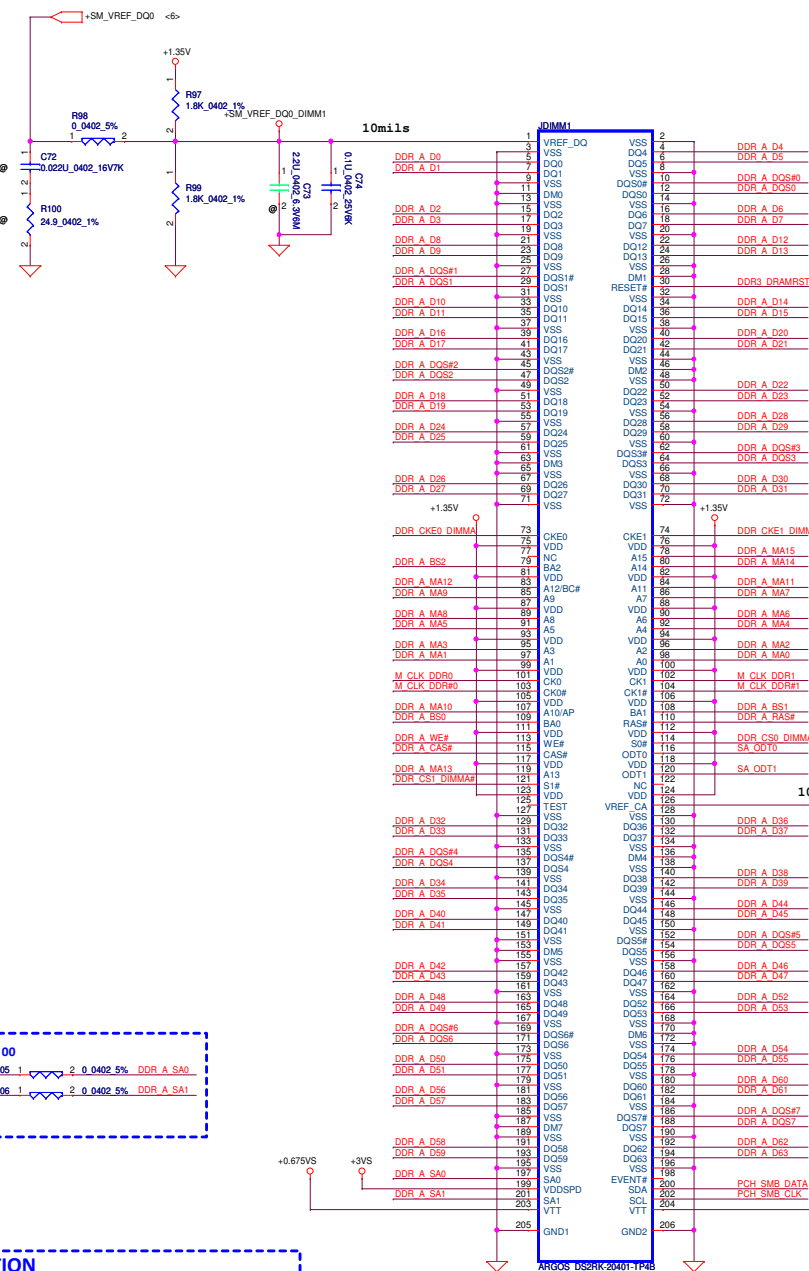
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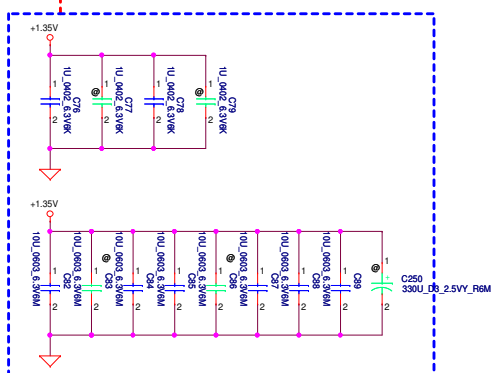


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				HSW MCP(11/11) RSVD	
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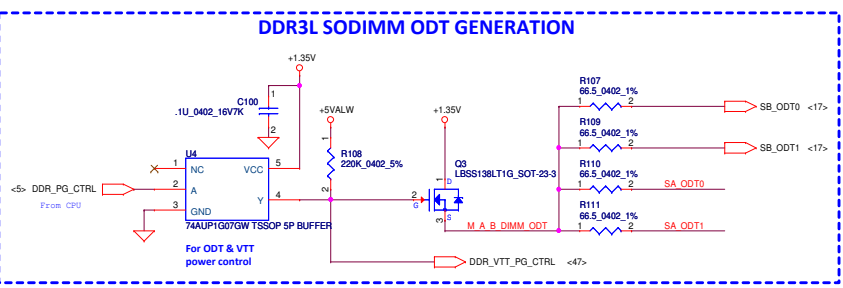
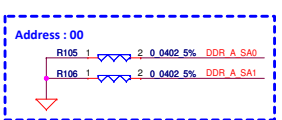
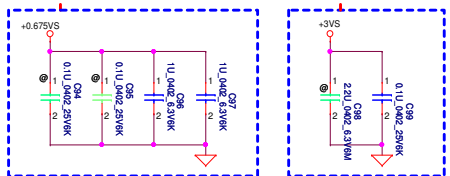
DIMM1
Reverse Type
Near CPU

Layout Note:
Place near JDIMM1



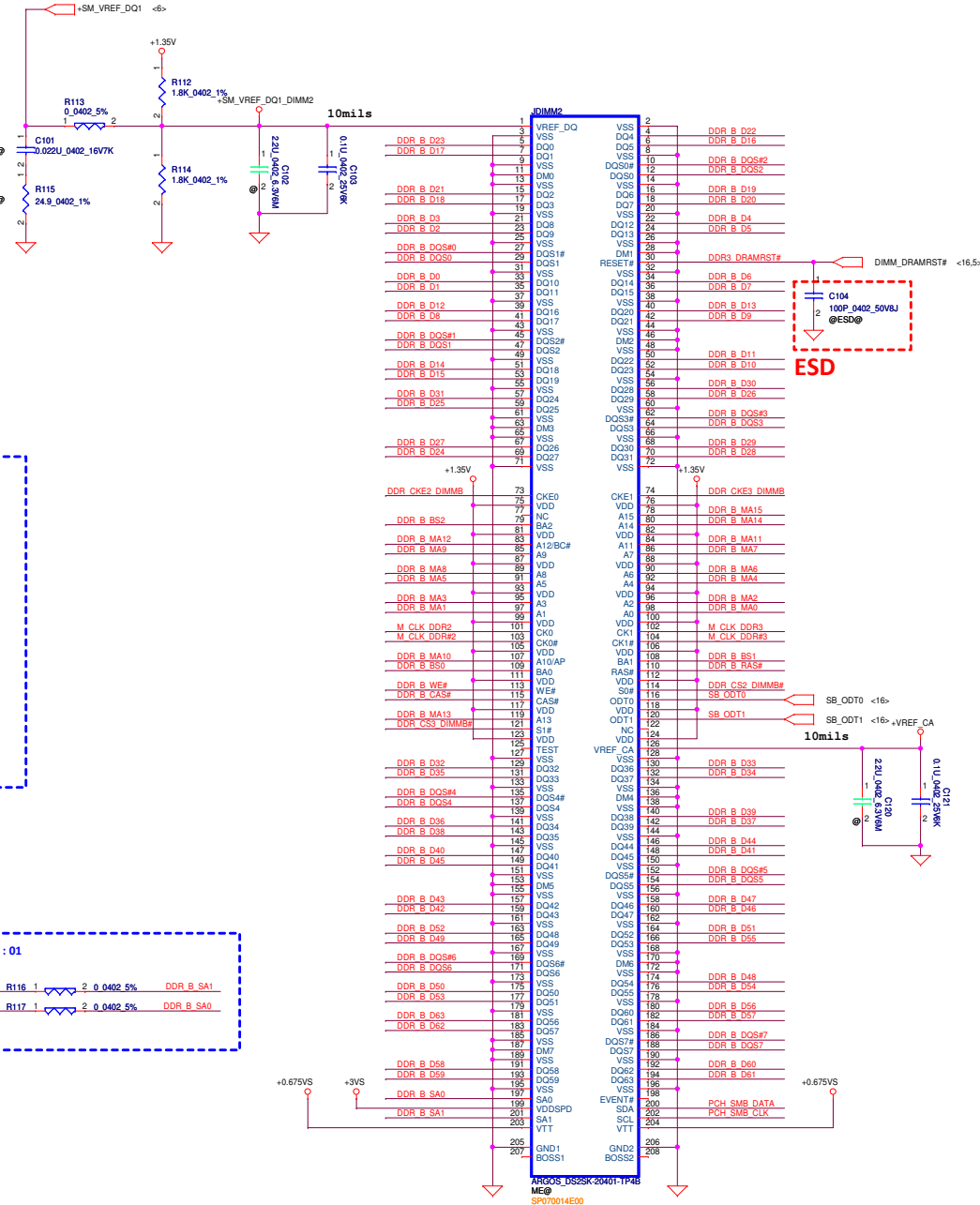
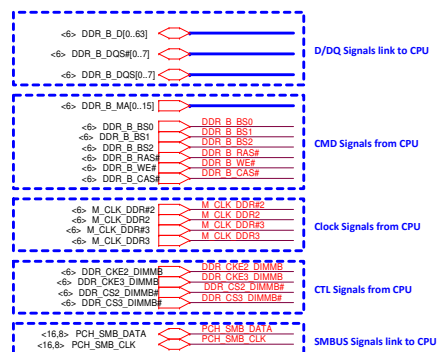
Layout Note:
Place near JDIMM1.203,204

Layout Note:
Place near JDIMM1.199



Interleaved Memory

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DIMM2
Standard Type
Near User

Layout Note:
Place near JDIMM2

ESD

Layout Note:
Place near JDIMM2.203,204

Layout Note:
Place near JDIMM2.199

Address : 01

Interleaved Memory

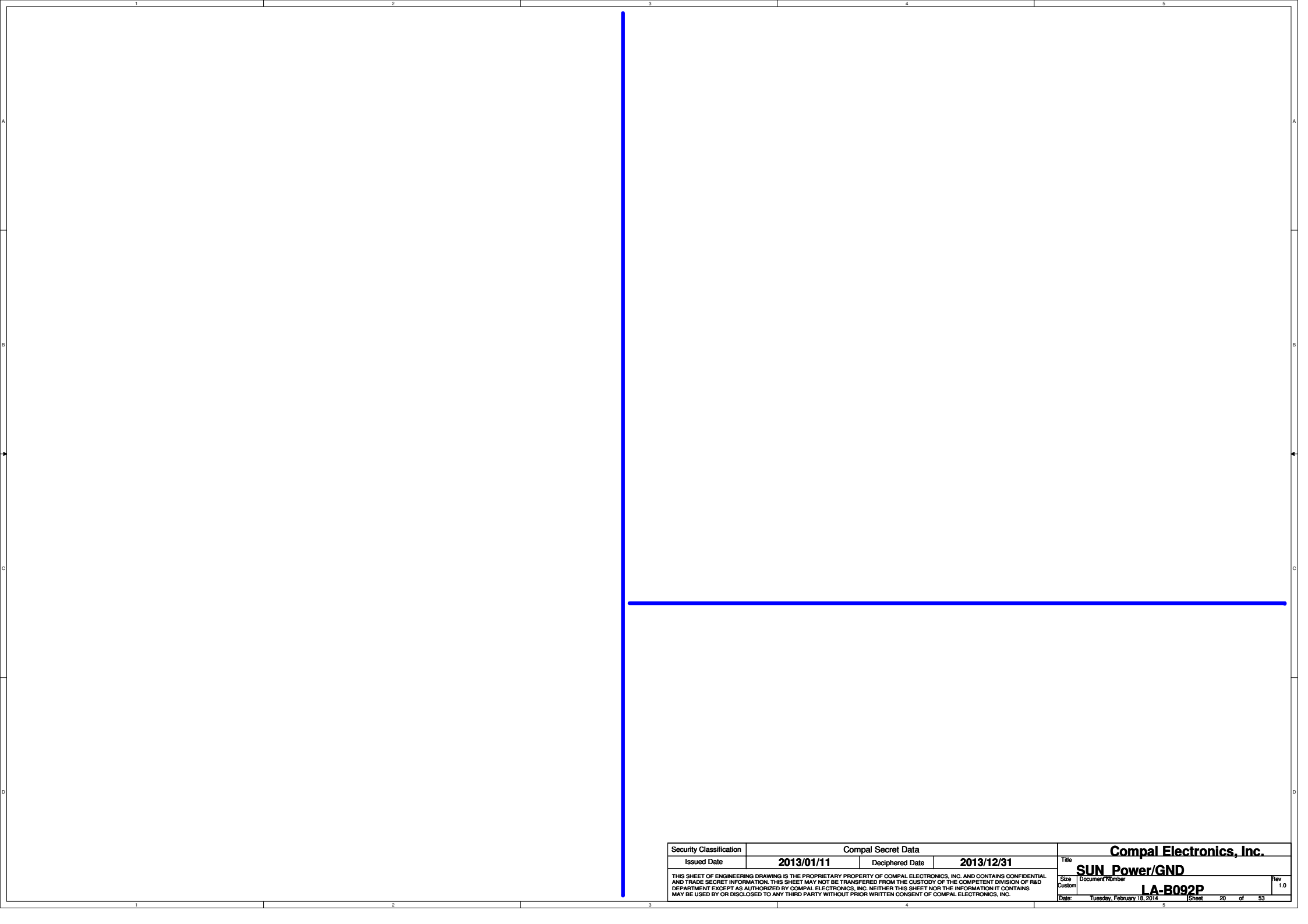
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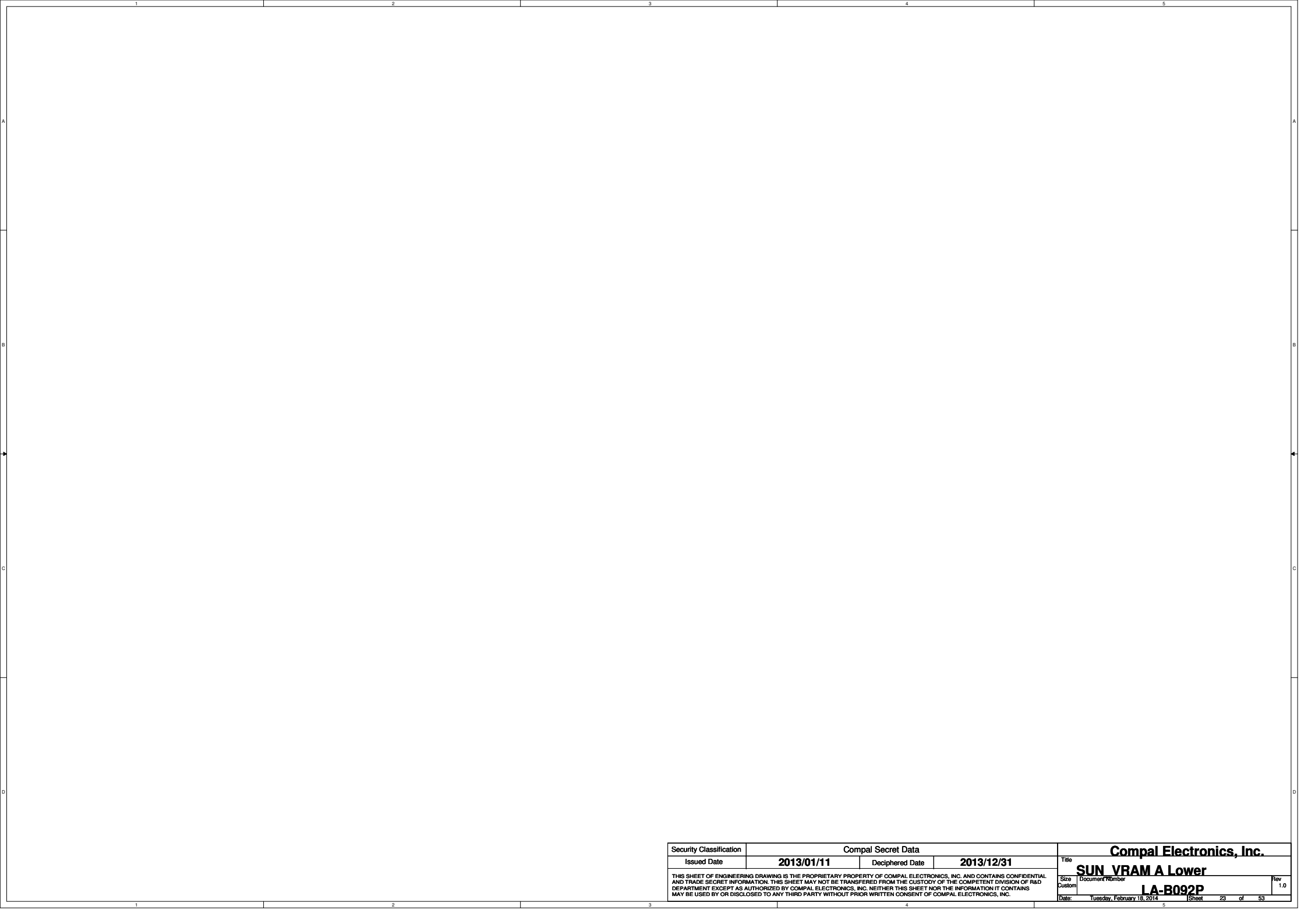
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				Date	Tuesday, February 18, 2014
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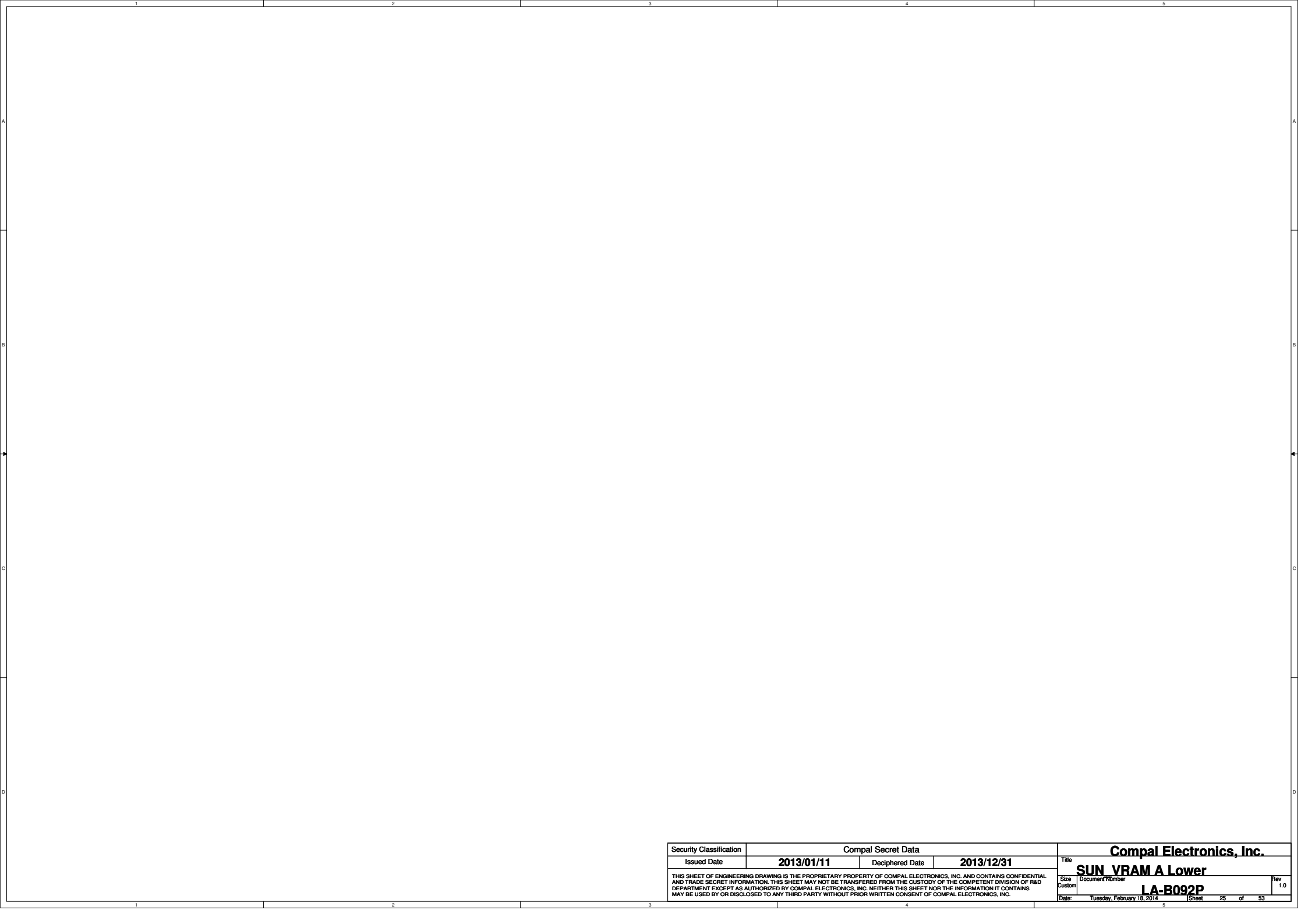
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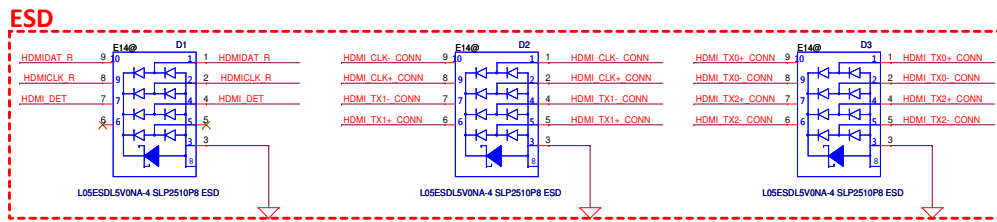
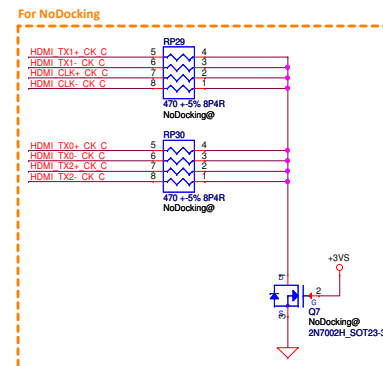
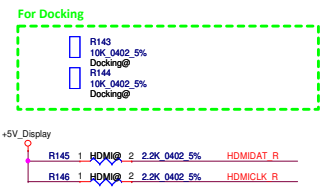
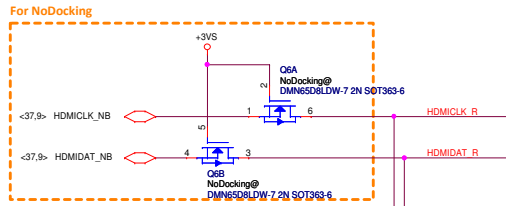
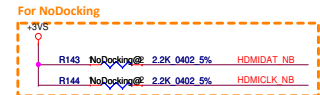
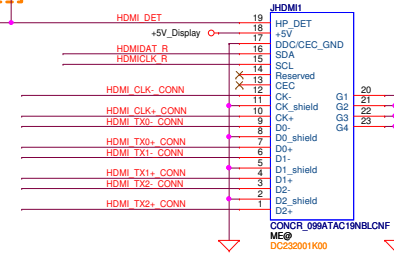
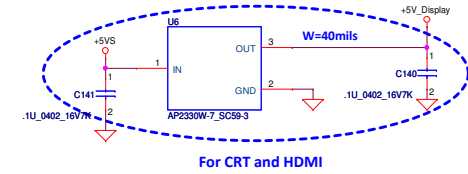
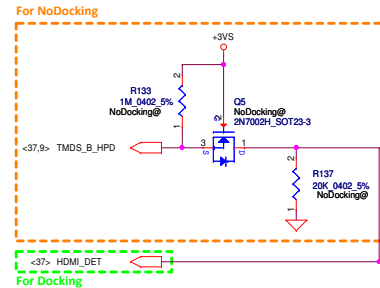
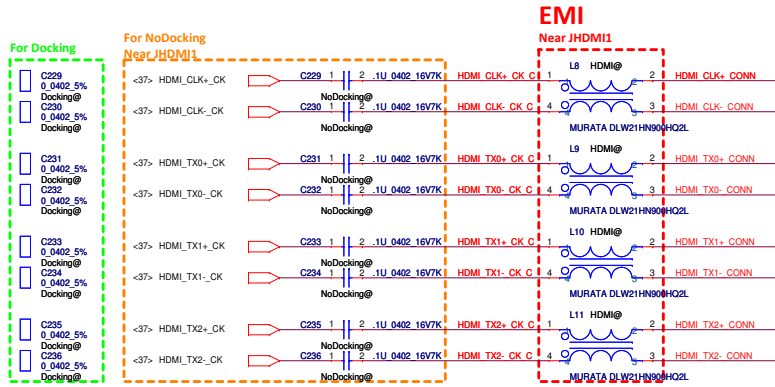
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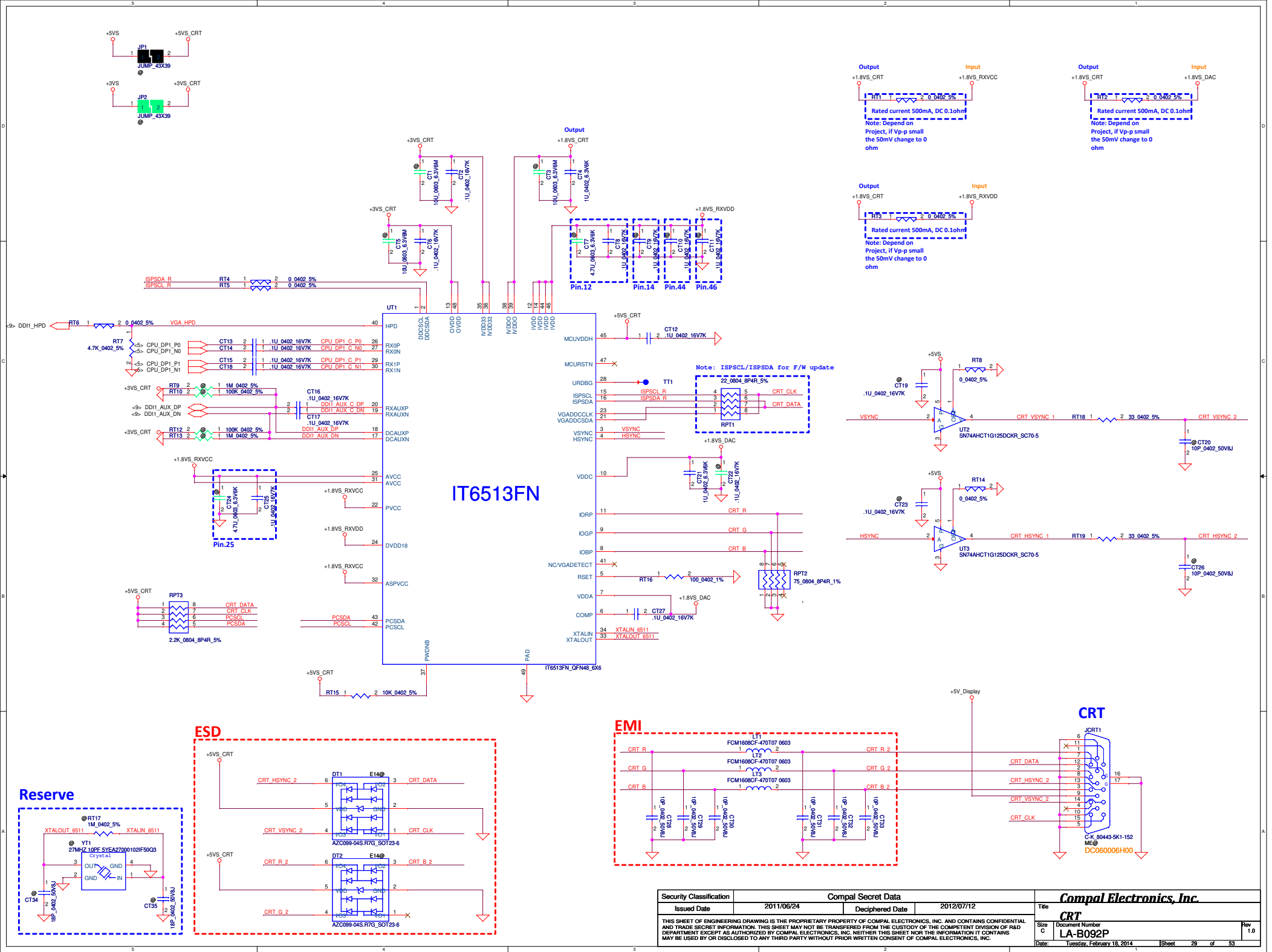
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	SUN VRAM A Lower	
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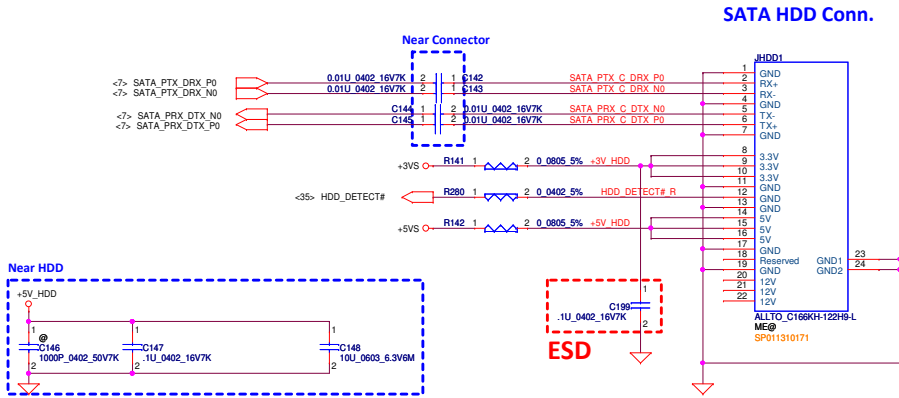
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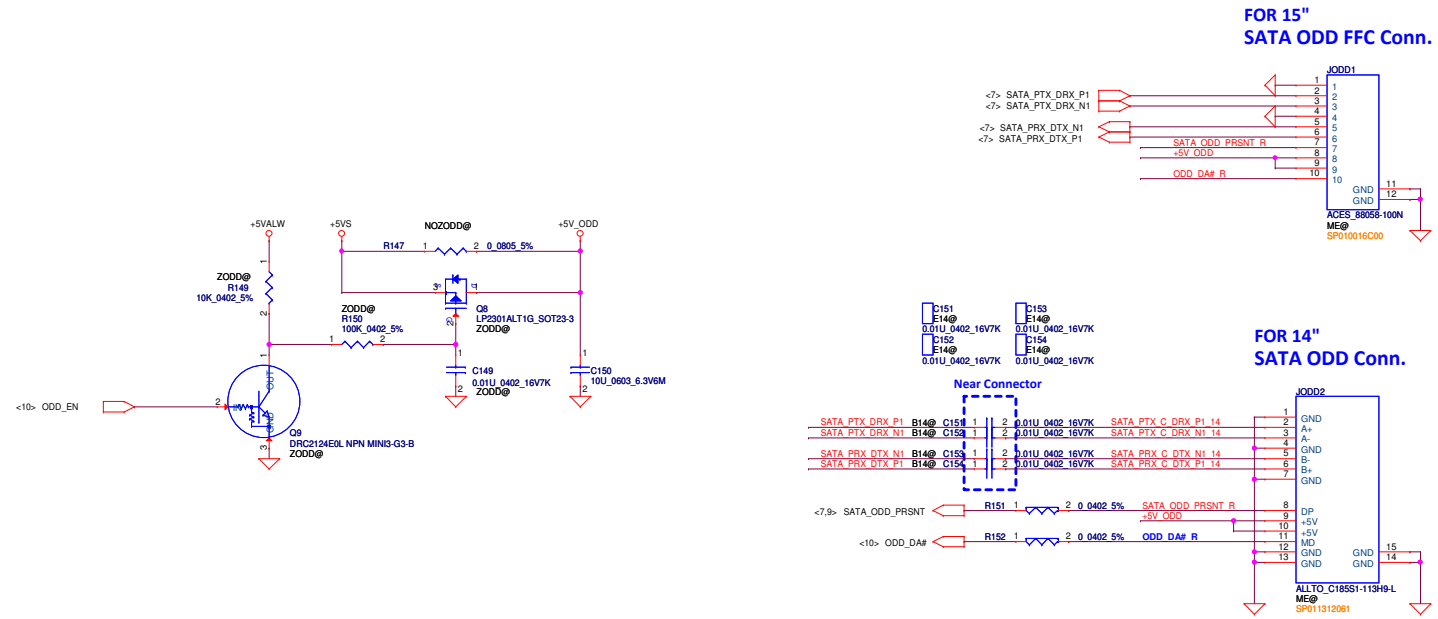
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Deciphered Date	2012/07/12	LA-B092P
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HDD



ODD



NGFF for WLAN / BT (Key E)
Support ISCT (Intel Smart Connect Technology)

BT

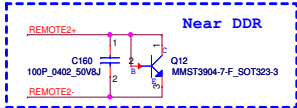
WLAN

For ISCT

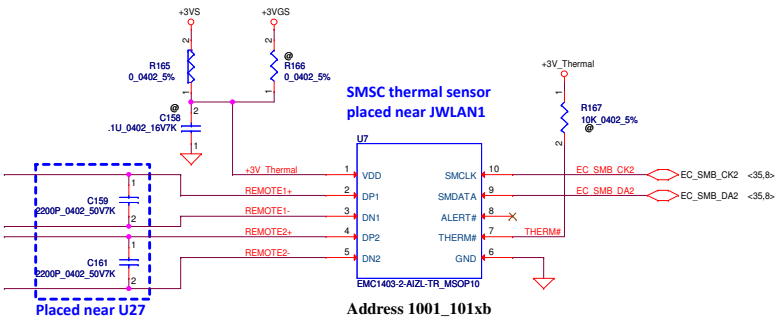
Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

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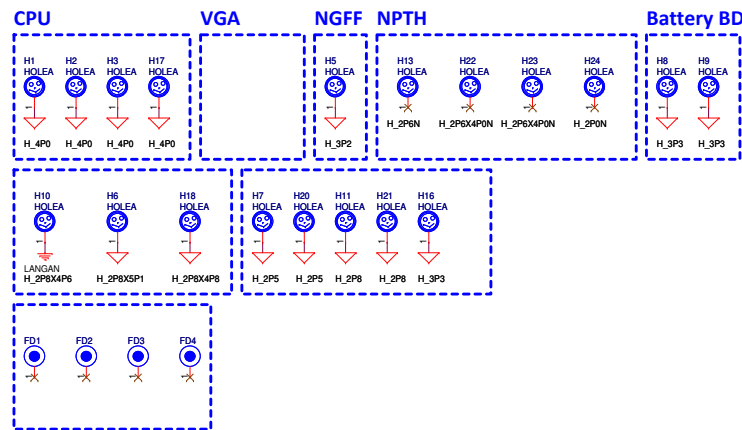
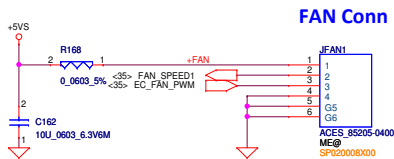
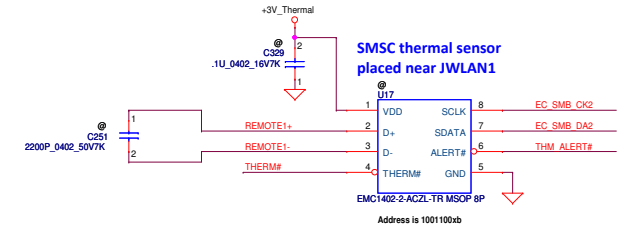
3 Channel

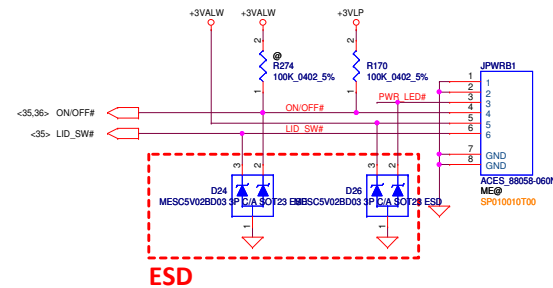


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



2 Channel



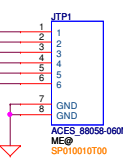
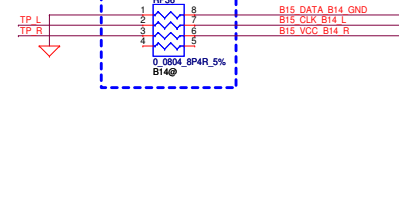
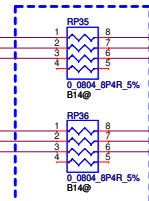
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RP33
0_0804_8P4R_5%
E14@

RP34
0_0804_8P4R_5%
E14@

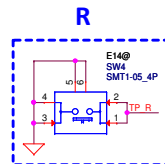
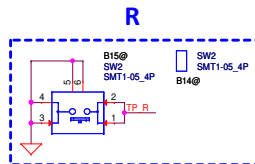
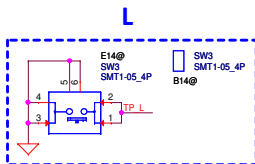
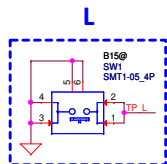
RP33
0_0804_8P4R_5%
B15@

RP34
0_0804_8P4R_5%
B15@

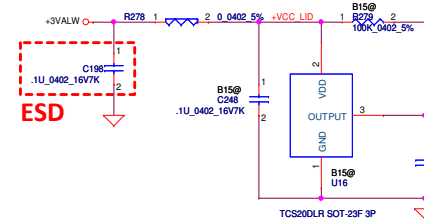
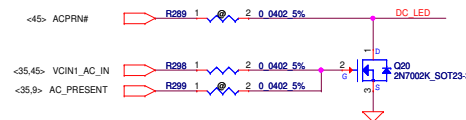


1	1	VCC	1	VCC
2	2	CLK	2	CLK
3	3	DAT	3	DAT
4	4	GND	4	L
5	5	L	5	R
6	6	R	6	GND

6	1	VCC	1	VCC
5	2	CLK	2	CLK
4	3	DAT	3	DAT
3	4	GND	4	L
2	5	L	5	R
1	6	R	6	GND

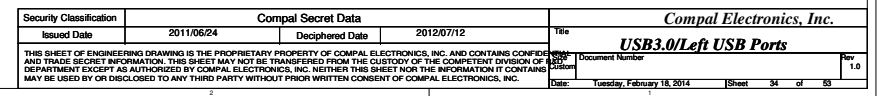
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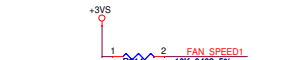
Pinout diagram for the ACES 88514-02501-071 ME@ SFO1000R500. The diagram shows a 28-pin connector with pins numbered 1 to 28. Pins 1 through 26 are labeled with their functions: KS11, KS17, KS18, KS19, KS14, KS15, KS20, KS12, KS13, KS05, KS01, KS10, RS02, KS04, KS07, KS08, KS06, KS03, KS02, RS012, KS13, RS014, RS011, RS010, RS015, CAPS LED#, CAPS LED#, and CAPS LED#. Pins 27 and 28 are labeled GND2 and GND1 respectively. The diagram also shows a 1000R500 resistor connected to pins 27 and 28.



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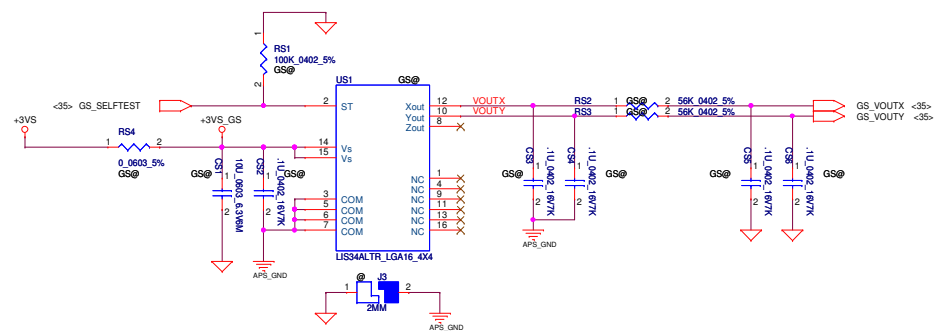
USB2.0_Port



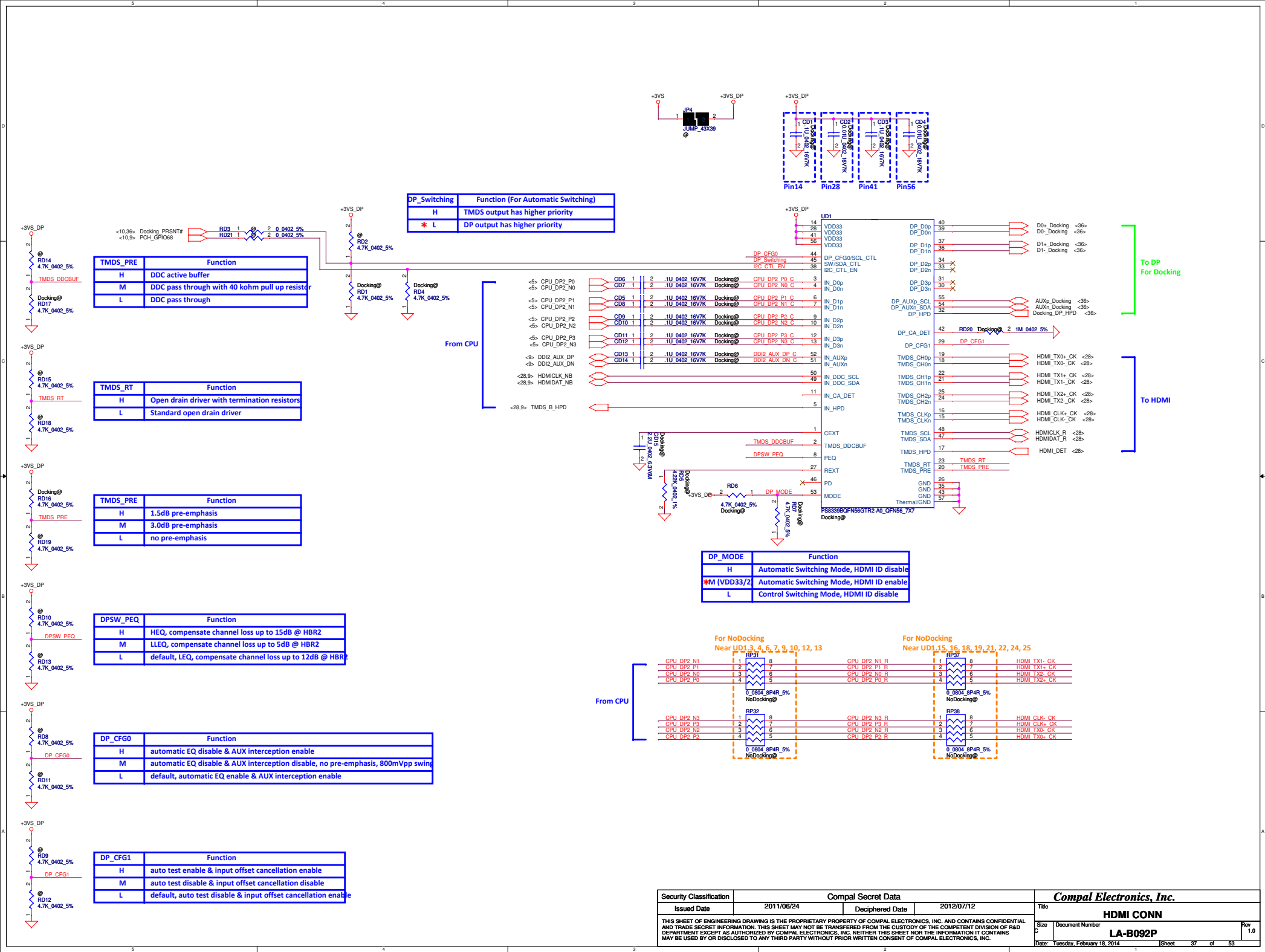


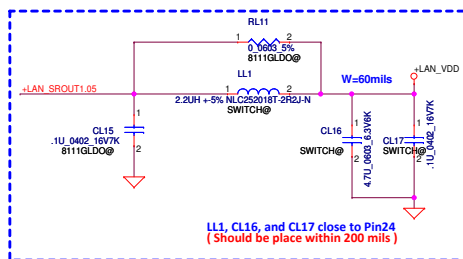
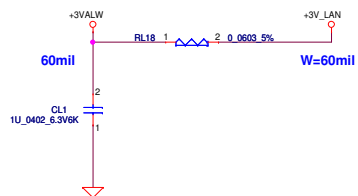
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APS (G-Sensor)



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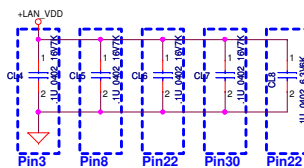
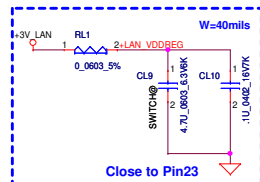
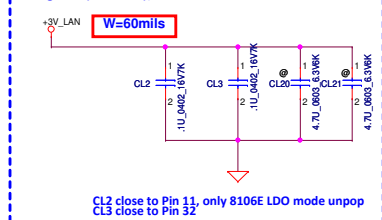
SA00005V700

SA000065Y00

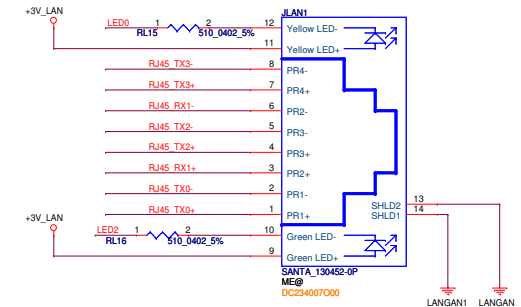
	1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
RTL8111G	LDO	X	X	X	O	O
RTL8111G	External	X	X	X	X	O
RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
RTL8106E	LDO	X	X	X	X	X

Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.

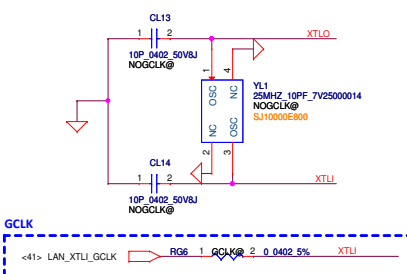
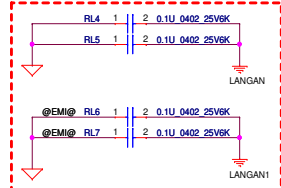
Rising time (10%~90%)要>1mS and <100mS



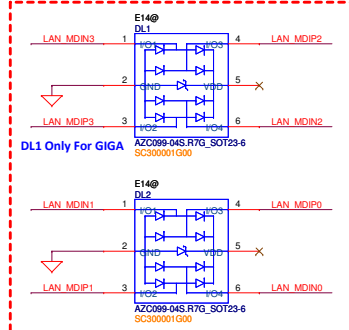
RJ-45 CONN.



EMI



ESD



EMI



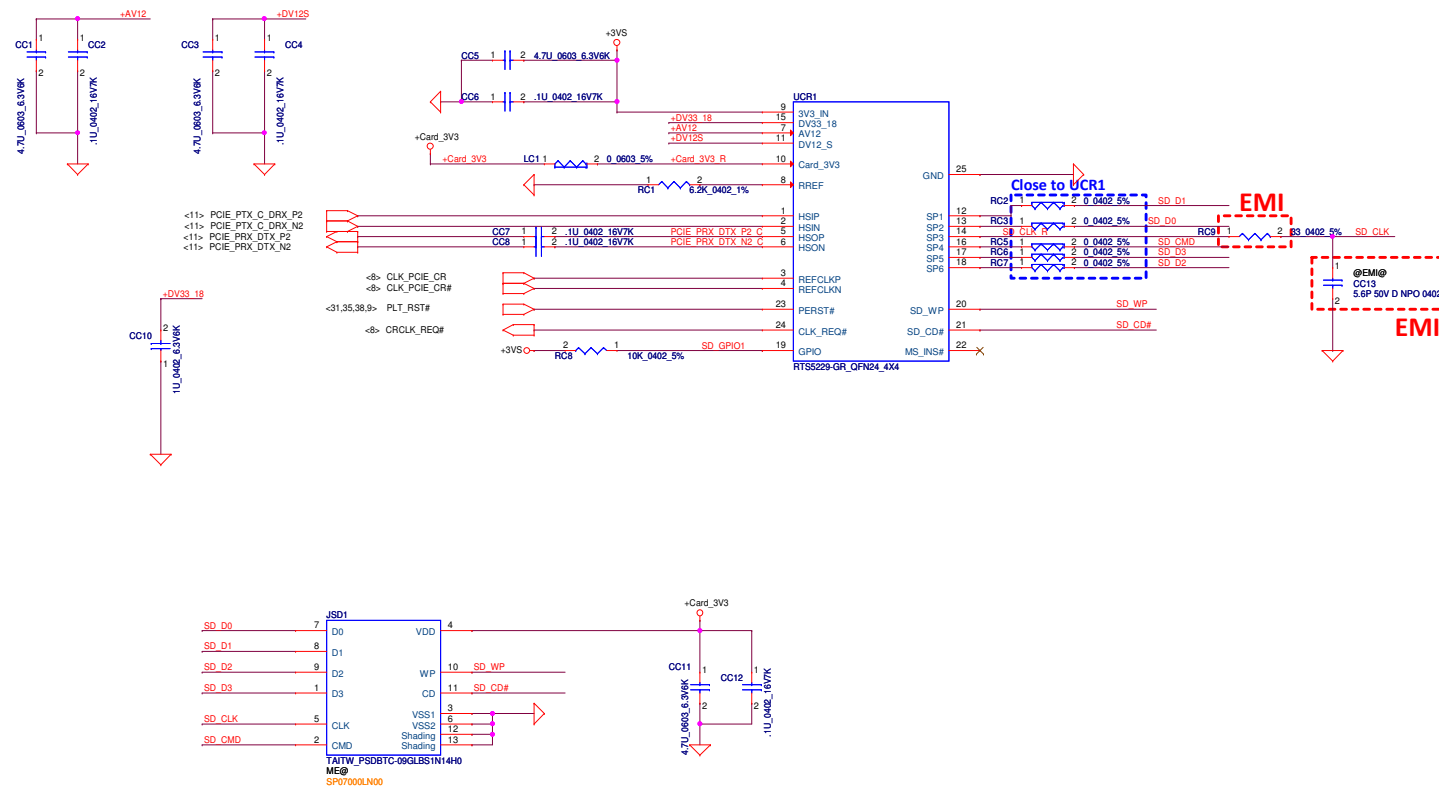
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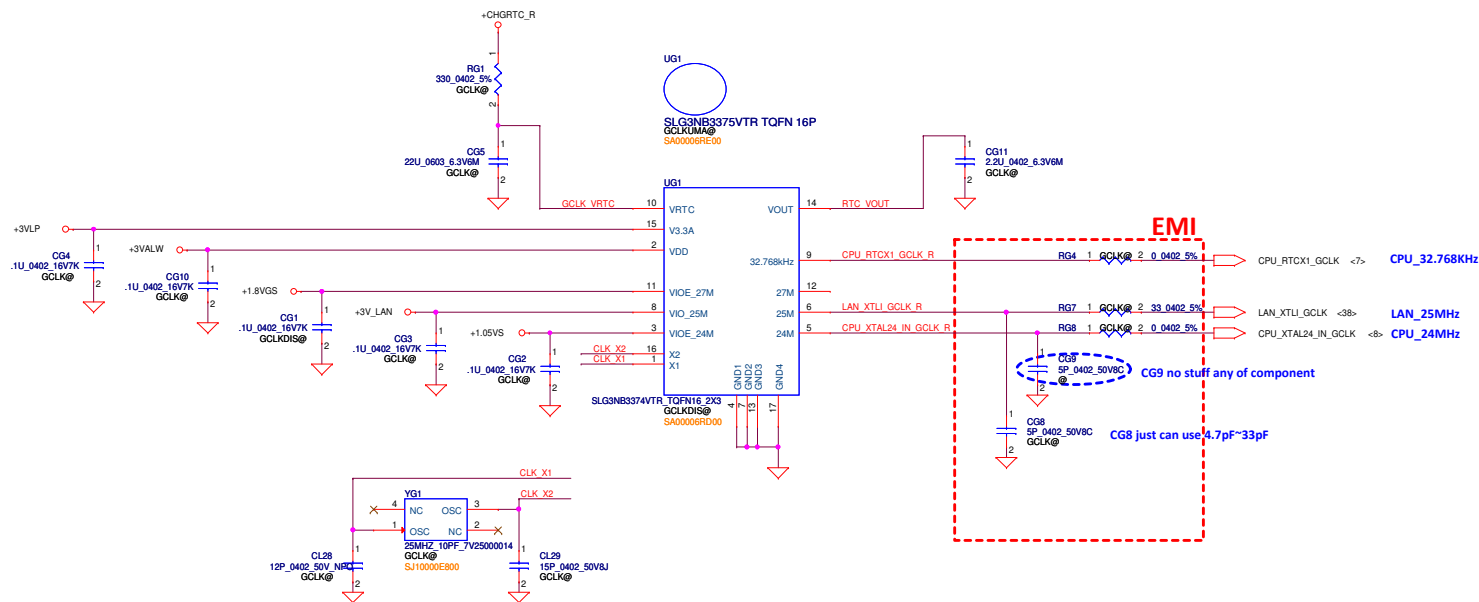


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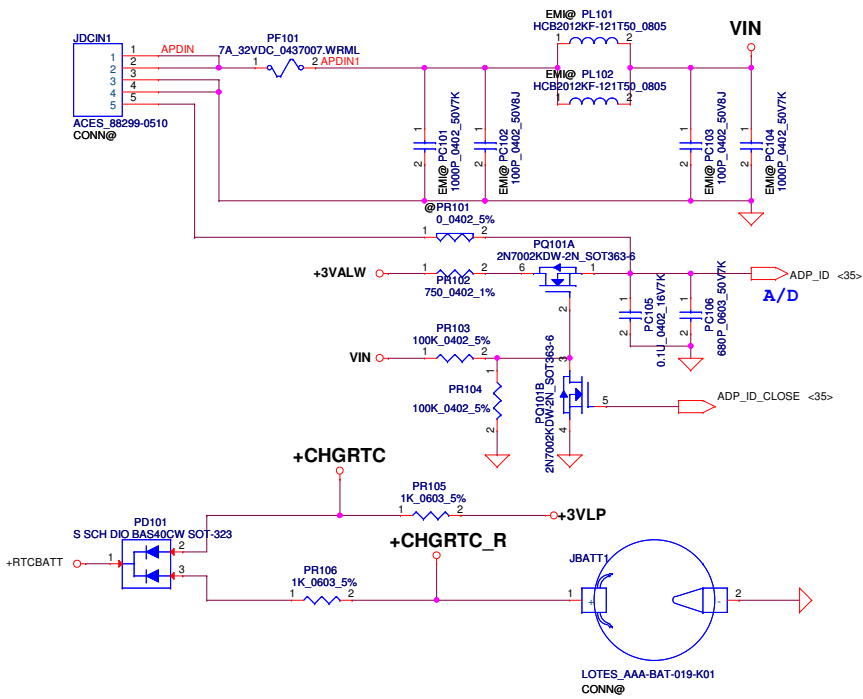


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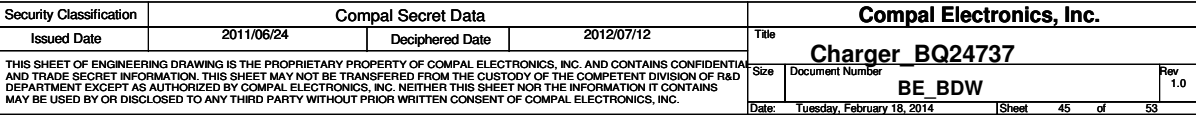
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RTC Battery

ADP_ID

AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98



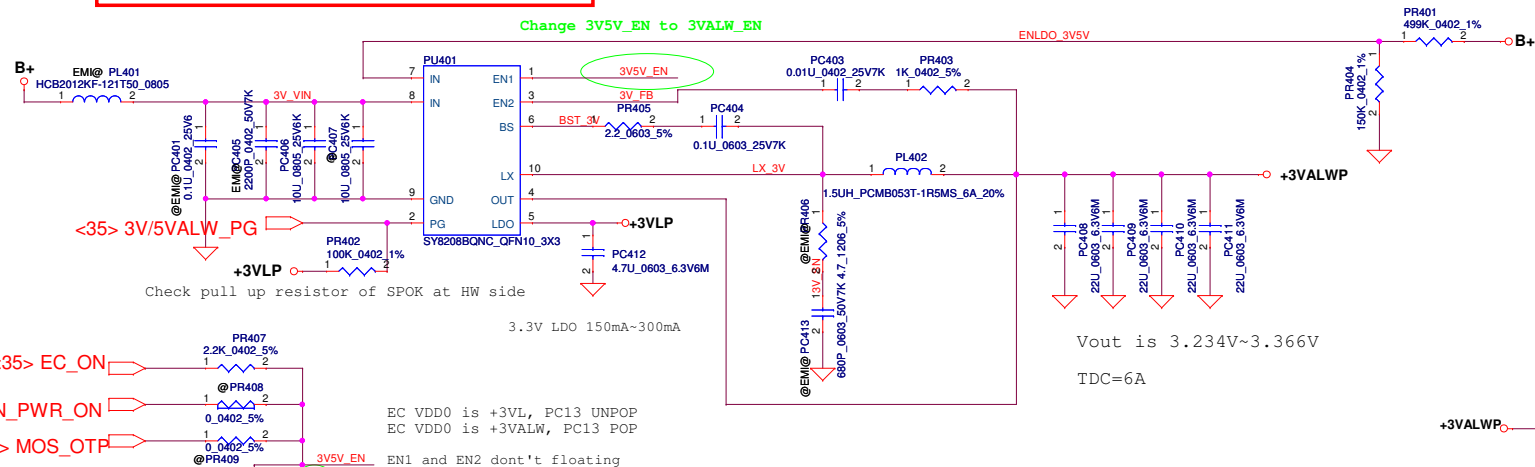
Module model information

SY8208B_V2.mdd

EN1 and EN2 don't floating

Change 3V5V_EN to 3VALW_EN

ENLDO_3V5V

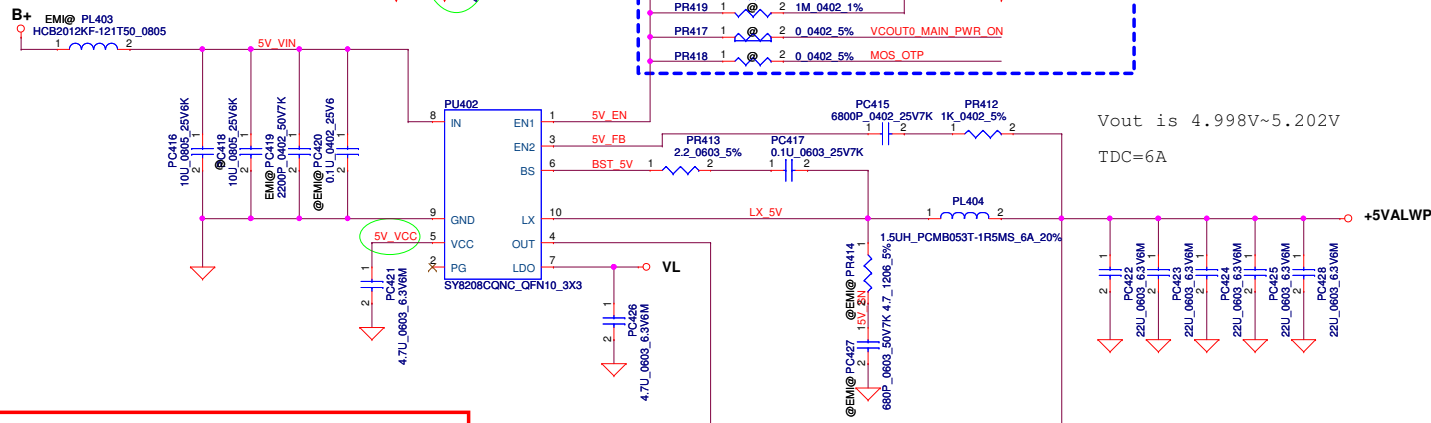


<35> EC_ON

<35> VCOUT0_MAIN_PWR_ON

<44> MOS_OTP

Reserve for USB Charger



Module model information

SY8208C_V2.mdd

5V LDO 150mA~300mA

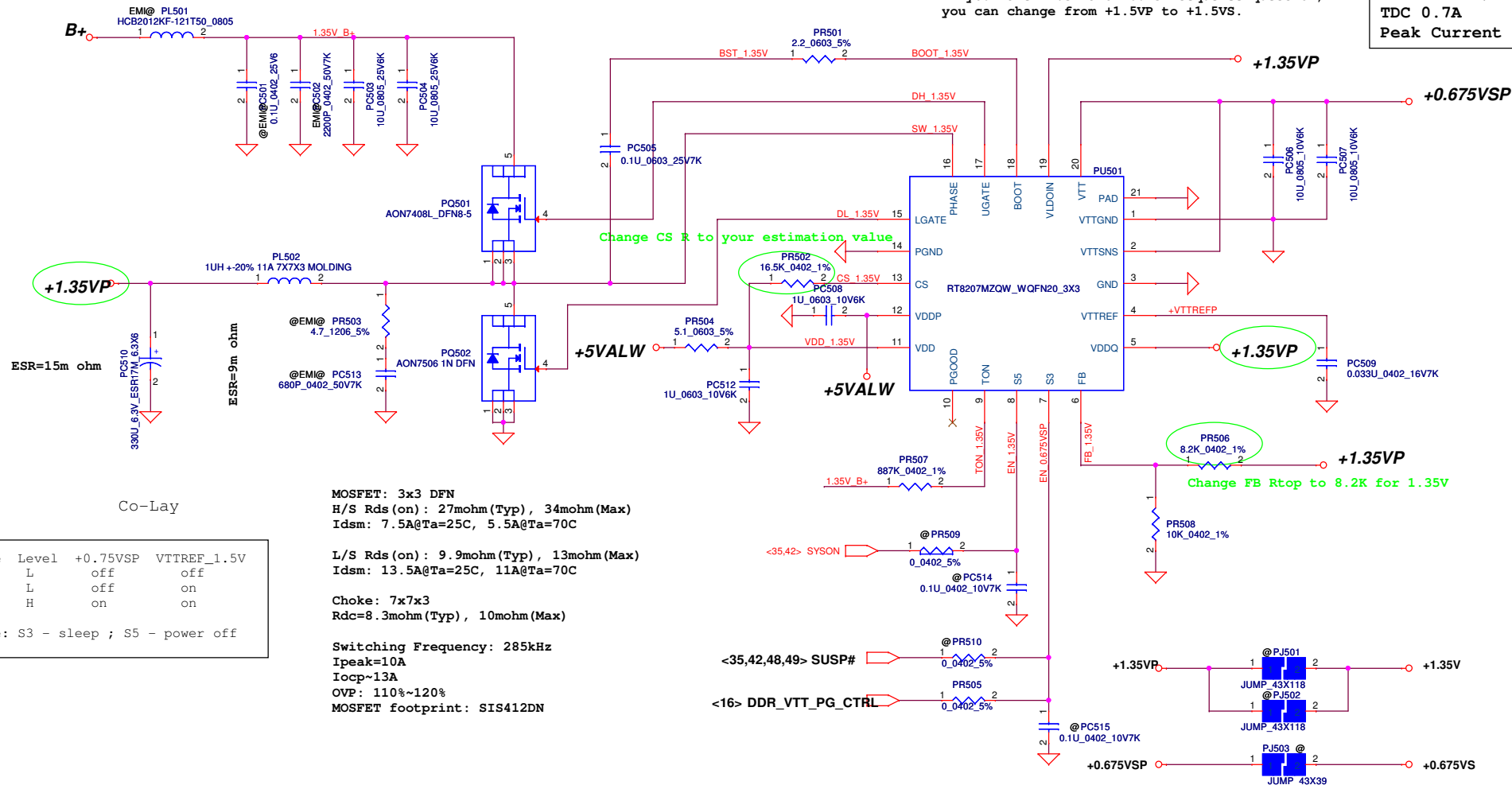
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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



Co-Lay

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds (on) : 27mohm (Typ) , 34mohm (Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on) : 9.9mohm (Typ) , 13mohm (Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

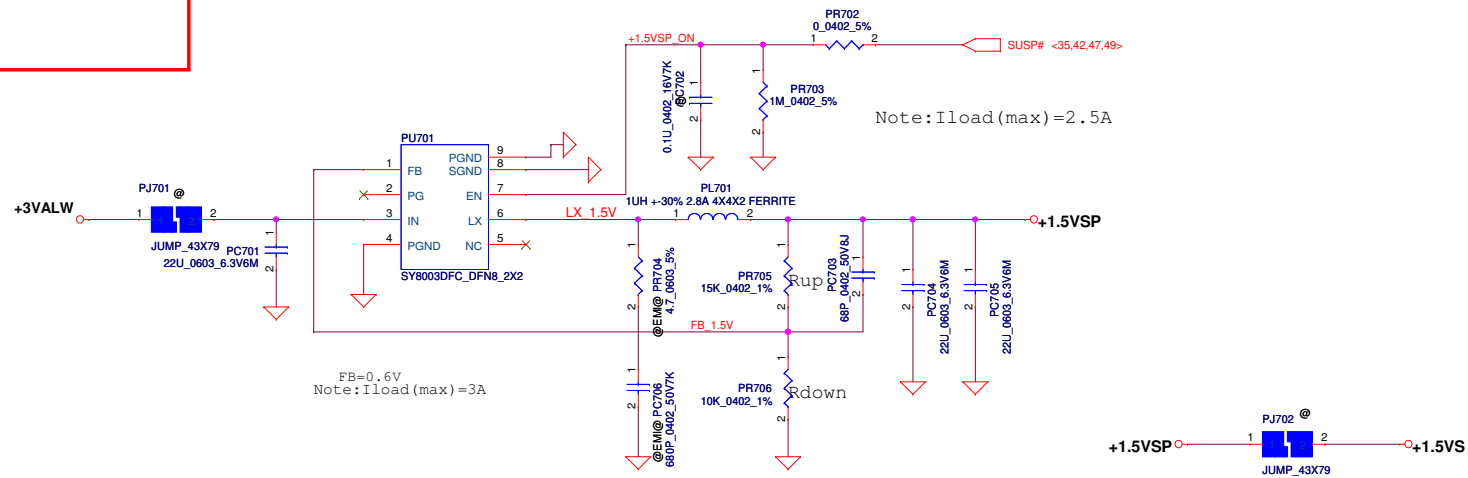
Choke: 7x7x3
Rdc=8.3mohm (Typ) , 10mohm (Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
MOSFET footprint: SIS412DN

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Module model information

SY8003_V1.mdd



Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

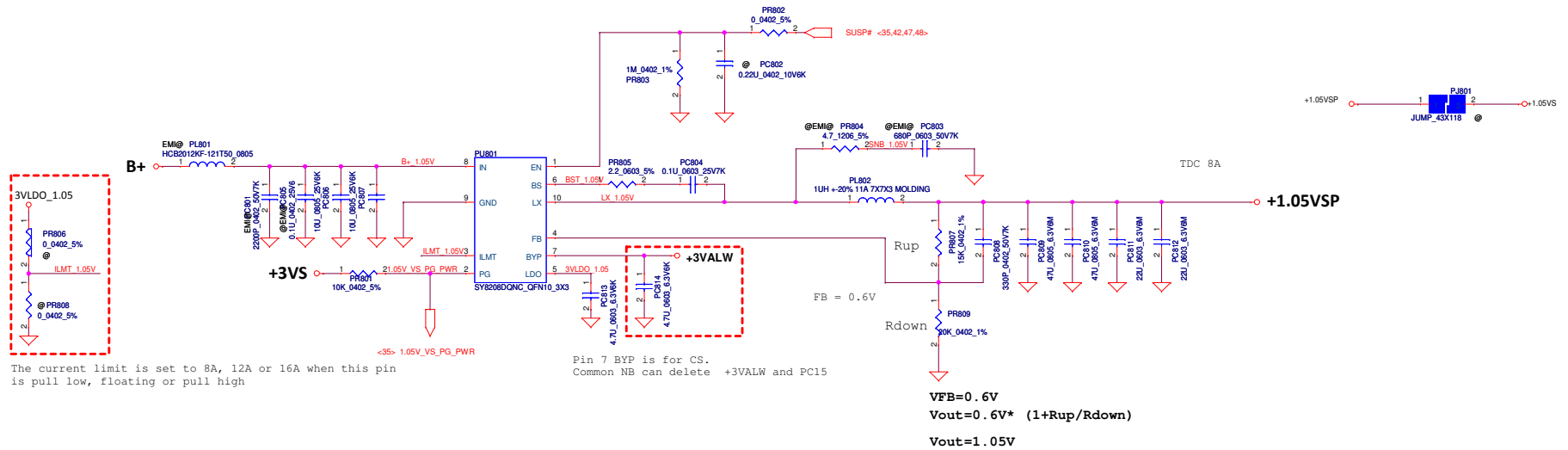
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



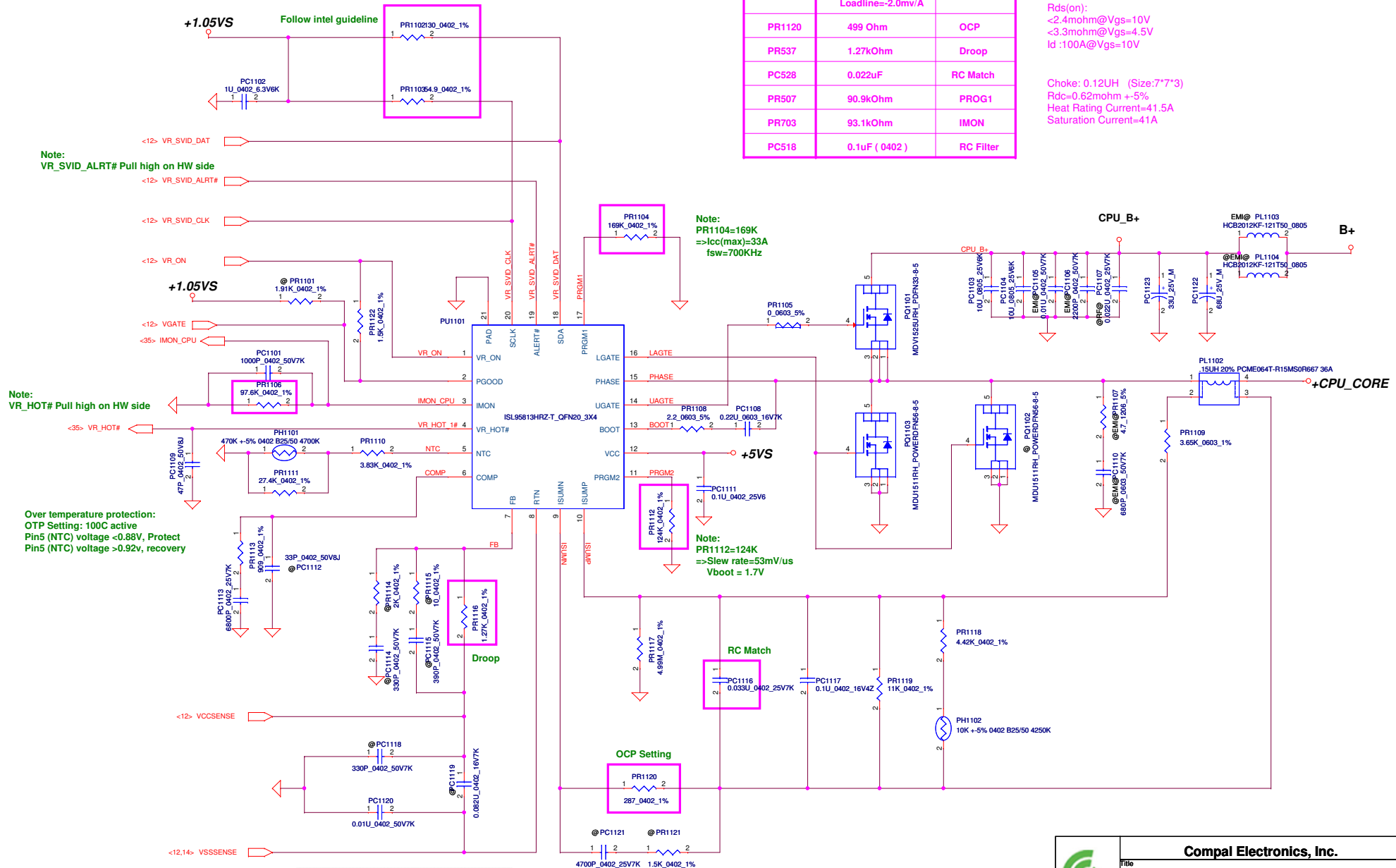
Module model information:
ISL95813 (for 15W & 28W CPU)

Base on BDW PDDG Rev_0_73		
Location	15W	Note
	TDC 14A	
	MAX 32A	
	OCp 39A	
	Loadline=-2.0mv/A	
PR1120	499 Ohm	OCp
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12UH (Size:7*7*3)
Rdc=0.62mohm +-5%
Heat Rating Current=41.5A
Saturation Current=41A



Local sense put on HW site



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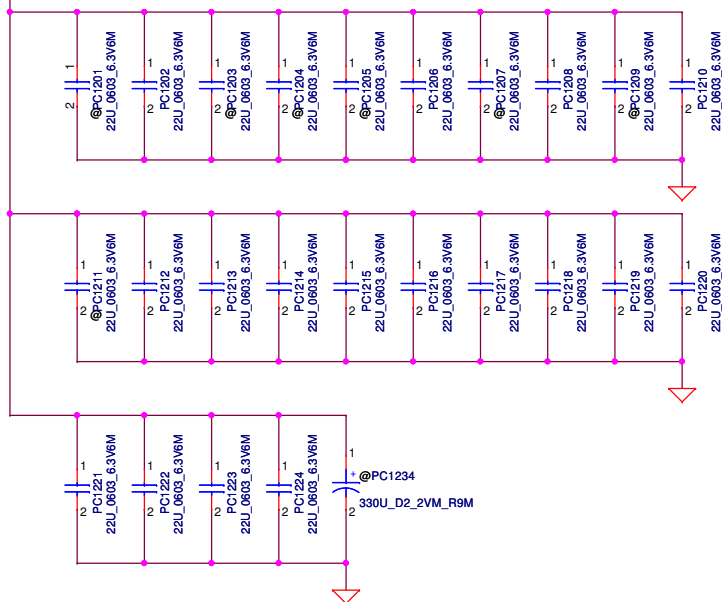
Title
ISL95813 for BDW-Y&U(15W/28W) CPU

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	BE BDW	

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+CPU_CORE

24 X 22u/0603



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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

ZIWB2/ZIWB3/ZIWE1 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE	
				. EVT TO DVT
1	P. 36	Modify DP_SEL schematic	Because the first design is wrong.	
2	P. 34	Delete D28	It already reserve in sub BD	
3	P. 36	Modify HPD schematic	Because the first design is wrong.	
4	P. 36	Modify DP AUX schematic	Cap already reserve in sub BD	
5	P. 20	Reserve +1.05VS to +0.95VGS	AMD' s suggestion	
6	P. 33	Add D26 for ESD		
7	P. 42	Add RV198, RV199	AMD' s suggestion	
				. DVT TO PVT
1	P. 35	change U11.111 power rail to +3VLP	It only use +3VLP	
2	P. 33	un-pop R294, pop R295.	B series's LED need to follow E series	
3	P. 10	Add R247, R248	For BIOS Stap Pin	
4	P. 37	Change DP Switch IC solution	For HDMI audio issue	
5	P. 35	Add C197 for ESD		
6	P. 33	Add C198 for ESD		
7	P. 30	Add C199 for ESD		
				. PVT TO PRE-MP
1	P. 33	Reserve R298, R299 for DC-in LED control	To avoid LED shimmer	
2	P. 38	Change DL1 and DL2 footprint for ESD		