

**SAMSUNG**

GSM TELEPHONE  
SGH-X430

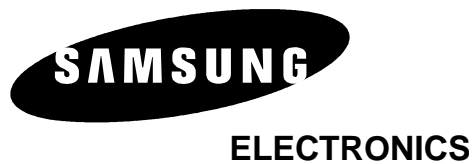
# ***SERVICE*** *Manual*

GSM TELEPHONE



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# 1. SGH-X430 Specification

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## 1. GSM General Specification

	GSM900 Phase 1	EGSM 900 Phase 2	DCS1800 Phase 1
Freq. Band[MHz] Uplink/Downlink	890~915 935~960	880~915 925~960	1710~1785 1805~1880
ARFCN range	1~124	0~124 & 975~1023	512~885
Tx/Rx spacing	45MHz	45MHz	95MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~13dBm	33dBm~5dBm	30dBm~0dBm
Power Class	5pcl ~ 15pcl	5pcl ~ 19pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm	-100dBm
TDMA Mux	8	8	8
Cell Radius	35Km	35Km	2Km

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# 1. SGH-X430 Specification

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## 2. GSM TX power class

<b>TX Power control level</b>	<b>GSM900</b>	<b>TX Power control level</b>	<b>DCS1800</b>
5	33 ±2 dBm	0	30 ±3 dBm
6	31 ±2 dBm	1	28 ±3 dBm
7	29 ±2 dBm	2	26 ±3 dBm
8	27 ±2 dBm	3	24 ±3 dBm
9	25 ±2 dBm	4	22 ±3 dBm
10	23 ±2 dBm	5	20 ±3 dBm
11	21 ±2 dBm	6	18 ±3 dBm
12	19 ±2 dBm	7	16 ±3 dBm
13	17 ±2 dBm	8	14 ±3 dBm
14	15 ±2 dBm	9	12 ±4 dBm
15	13 ±2 dBm	10	10 ±4 dBm
16	11 ±3 dBm	11	8 ±4dBm
17	9 ±3dBm	12	6 ±4 dBm
18	7 ±3 dBm	13	4 ±4 dBm
19	5 ±3 dBm	14	2 ±5 dBm
		15	0 ±5 dBm

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## 2. SGH-X430 Circuit Description

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### 1. SGH-X430 RF Circuit Description

#### 1) RX PART

##### 1. ASM(U201)

⇒ Switching Tx, Rx path for GSM900, DCS1800 by logic controlling.

##### 2. ASM Control Logic (U501, U502)

⇒ Truth Table

	VC1	VC2
GSM Tx Mode	L	H
DCS Tx Mode	H	L
GSM / DCS Rx Mode	L	L

#### 3. FILTER

To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

##### - GSM FILTER (F100)

⇒ For filtering the frequency band between 925 ~ 960 MHz

##### - DCS FILTER (F101)

⇒ For filtering the frequency band 1805 and 1880 MHz.

#### 4. VCTCXO (OSC100)

To generate the 13MHz reference clock to drive the logic and RF.

After additional process, the reference clock is applied to the U100 Rx IQ demodulator and Tx IQ modulator.

The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

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## 2. SGH-X430 Circuit Description

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### 5. Si 4205 (U100)

This chip integrates three differential-input LNAs.

The GSM input supports the E-GSM, DCS input supports the DCS1800, PCS input supports the PCS1900. The LNA inputs are matched to the 200 ohm differential output SAW filters through external LC matching network.

Image-reject mixer downconverts the RF signal to a 100 KHz intermediate frequency(IF) with the RFLO from SI4133T frequency synthesizer.

The RFLO frequency is between 1737.8 ~ 1989.9 MHz.

The Mixer output is amplified with an analog programmable gain amplifier(PGA), which is controlled by AGAIN.

The quadrature IF signal is digitized with high resolution A/D converts (ADC).

The SI4205 down-converts the ADC output to baseband with a digital 100 KHz quadrature LO signal.

Digital decimation and IIR filters perform channel selection to remove blocking and reference interface signals. After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN. DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, RXQN pins to interface to standard analog-input baseband IC.

### 2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U100 chip.

SI4205 chip generates modulator signal which power level is about 1.5dBm and fed into Power Amplifier(U200).

The PA output power and power ramping are well controlled by Auto Power Control circuit. We use offset PLL below,

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		DCS	-35dBc
		PCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		DCS	-65dBc
		PCS	-66dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		DCS	-68dBc
		PCS	-75dBc

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## 2. SGH-X430 Circuit Description

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### 2. Baseband Circuit description of SGH-X430

#### 1) PSC2106

##### 1. Power Management

Seven low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life.

A programmable LDO provides support for 1.8V, 3.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as two LED drivers and two call-alert drivers, aid in reducing both board area and system complexity.

A four-wire serial interface unit(SIU) provides access to control and configuration registers. This interface gives a microprocessor full control of the PSC2106 and enables system designers to maximize both standby and talk times. Error reporting is provided via an interrupt signal and status register.

Supervisory functions, including a reset generator, an input voltage monitor, and a thermal monitor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

##### 2. Battery Charge Management

A battery charge management block, incorporating an internal PMOS switch, and an 8-bit ADC, provides fast, efficient charging of single-cell Li-Ion battery. Used in conjunction with a current-limited voltage source, this block safely conditions near-dead cells and provides the option of having fast-charge and top-off controlled internally or by the system's microprocessor.

##### 3. Backlight LED Driver

The backlight LED driver is a low-side, programmable current source designed to control the brightness of the keyboard and LCD illumination. LED1\_DRV is controlled via LED1\_[0:2] and can be programmed to sink from 15mA to 60mA in 7.5mA steps. LED2\_DRV is controlled via LED2\_[0:2] and can be programmed to sink from 5mA to 40mA in 5mA steps. Both LED drivers are capable of sinking their maximum output current at a worst-case maximum output voltage of 0.6V. For efficient use, the LEDs is connected between the battery and the LED\_DRV output.

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## 2. SGH-X430 Circuit Description

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### 4. Vibrator Motor Driver

The vibrator motor driver is a low-side, programmable voltage source designed to drive a small dc motor that silently alerts the user of an incoming call. The driver is controlled by VIB[0:1] and can be programmed to maintain a motor voltage of 1.3V, 2.0V, or 2.5V(relative to VBAT) while sinking up to 100mA. For efficient use, the vibrator motor should be connected between the main battery and the VIB\_DRV output.

### 2) Connector

#### 1. LCD Connector

LCD is consisted of main LCD(color 65K UFB LCD). Chip select signals of EMI part in the trident, CLCD\_EN, can enable main LCD. LED\_EN signal enables white LED of main LCD and EL\_EN signal enables dimming mode of main LCD.

These two signals are from IO part of the DSP in the trident. RST signal from 2106 initiates the initial process of the LCD.

16-bit data lines(D(0)~D(15)) transfers data and commands to LCD through emi\_filter. Data and commands use A(2) signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data. The signal which informs the input or output state to LCD, is required. But this system is not necessary this signal. So CP\_WEN signal is used to write data or commands to LCD.

Power signals for LCD are +VBATT and VCCD.

SPK1P and SPK1N from CSP1093 are used for audio speaker. And YMU\_VIB\_EN from MA-3 enables the motor.

#### 2. JTAG Connector

Trident has two JTAG ports which are for ARM core and DSP core(DSP16000). So this system has two port connector for these ports. Pins' initials for ARM core are 'CP\_' and pins' initials for DSP core are 'DSP\_'.

CP\_TDI and DSP\_TDI signal are used for input of data. CP\_TDO and DSP\_TDO signals are used for the output of the data. CP\_TCK and DSP\_TCK signals are used for clock because JTAG communication is a synchronous. CP\_TMS and DSP\_TMS signals are test mode signals. The difference between these is the RESET\_INT signal which is for ARM core RESET.



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## 2. SGH-X430 Circuit Description

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### 3. Keypad connector

This is consisted of key interface pins in the trident, KEY\_ROW[0~4] and KEY\_COL[0~4]. These signals compose the matrix. Result of matrix informs the key status to key interface in the trident. Some pins are connected to varistor for ESD protection. And power on/off key is separated from the matrix.

So power on/off signal is connected with PSC2106 to enable PSC2106.

SVC\_GREEN, SVC\_RED and SVC\_BLUE are from OCTL of CSP1093.

These signals decide the color of LED, service indicator.

Nine key LED use the +VBATT supply voltage. These are connected to BACKLIGHT signal in the PSC2106.

This signal enables LEDs with current control. FLIP\_SNS informs the status of folder (open or closed) to the trident. This uses the hall effect IC, A3210ELH.

A magnet under main LCD enables A3210ELH which is on the main PCB.

### 4. EMI Filtering

This system uses the EMI Filter to reduce noise from LCD part. Some control signals are connected to LCD without EMI filtering.

### 3) IF connetor

It is 23-pin connector, and uses 18-pin at present. They are designed to use SDS, DEBUG, DLC-DETECT, JIG\_ON, VEXT, VTEST, VF, +VBATT and GND. They connected to power supply IC, microprocessor and signal processor IC.

### 4) Audio

AOUTAP, AOUTAN from CSP1093 is connected to the speaker via analog switch. AOUTBP and AOUTBN are connected to the ear-mic speaker via ear-jack. MICIN and MICOUT are connected to the main MIC. And AUXIN and AUXOUT are connected to the Ear-mic.

YMU762MA3 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decoder that are included in this device.

As a synthesis, YMU762MA3 is equipped 16 voices with different tones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects.

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## 2. SGH-X430 Circuit Description

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Since the play data of YMU762MA3 are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexibly support application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.

YMU762 includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibrator and a circuit for controlling LEDs synchronous with music.

For the headphone, it is provided with a stereophonic output terminal.

For the purpose of enabling YMU762MA3 to demonstrate its full capabilities, Yamaha purpose to use "SMAF:Synthetic music Mobile Application Format" as a data distribution format that is compatible with multimedia. Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for training karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU762MA3 directly interprets and plays blocks relevant to synthesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

### 5) Memory

This system uses SHARP's memory, LRS1828.

It is consisted of 128M bits flash memory and 32M bits SCRAM. It has 16 bit data line, D[0~15] which is connected to trident, LCD or CSP1093. It has 22 bit address lines, A[1~22]. They are connected too. CP\_CSROMEN and CO\_CSROM2EN signals, chip select signals in the trident enable two memories. They use 3 volt supply voltage, VCCD.

During writing process, CP\_WEN is low and it enables writing process to flash memory and SCRAM. During reading process, CP\_OEN is low and it output information which is located at the address from the trident in the flash memory or SCRAM to data lines. Each chip select signals in the trident select memory among 2 flash memory and SCRAM. Reading or writing procedure is processed after CP\_WEN or CP\_OEN is enabled. Memories use FLASH\_RESET, which is buffered signal of RESET from PSC2106, for ESD protection. A[0] signal enables lower byte of SCRAM and UPPER\_BYTE signal enables higher byte of SCRAM.

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## 2. SGH-X430 Circuit Description

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### 6) Trident

Trident is consisted of ARM core and DSP core. It has 20K\*16bits RAM 144K\*16bits ROM in the DSP. It has 4K\*32bits ROM and 2K\*32bits RAM in the ARM core. DSP is consisted of timer, one bit input/output unit(BIO), JTAG, EMI and HDS(Hardware Development System). ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACCs(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface.

DSP\_AB[0~8], address lines of DSP core and DSP\_DB[0~15], data lines of DSP core are connected to CSP1093. A[0~20], address lines of ARM core and D[0~15], data lines of ARM core are connected to memory, LCD and YMU762. ICP(Interprocessor Communication Port) controls the communication between ARM core and DSP core.

CSROMEN, CSRAMEN and CS1N to CS4N in the ARM core are connected to each memory. WEN and OEN control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, YMU, Ear-jack, Ear-mic and CSP1093, need the compatible process.

Some PPI pins has many special functions. CP\_KB[0~9] receive the status from key FPCB and are used for the communications using data link cable(DEBUG\_DTR/RTS/TXD/RXD/CTS/DSR).

And UP\_CS/SCLK/SDI, control signals for PSC2106 are outputted through PPI pins. It has signal port for charging(CHG\_DET), SIM\_RESET and FLIP\_SNS with which we know open/closed status of folder. It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It receives 13MHz clock in CKI pin from external TCXO and receives 32.768KHz clock from X1RTC.

ADC(Analog to Digital Converter) part receives the status of temperature, battery type and battery voltage. And control signals(DSP\_INT, DSP\_IO and DSP\_RWN) for DSP core are used. It enables main LCD with DSP IP pins.

### 7) CSP1093

CSP1093 integrates the timing and control functions for GSM 2+ mobile application with the ADC and DAC functions. The CSP1093 interfaces to the trident, via a 16-bit parallel interface. It serves as the interface that connects a DSP to the RF circuitry in a GSM 2+ mobile telephone. DSP can load 148 bits of burst data into CSP1093's internal register, and program CSP1093's event timing and control register with the exact time to send the burst. When the timing portion of the event timing and control register matches the internal quarter-bit counter and internal frame counter, the 148 bits in the internal

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## 2. SGH-X430 Circuit Description

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register are GMSK modulated according to GSM 2+ standards. The resulting phase information is translated into I and Q differential output voltages that can be connected directly to an RF modulator at the TXOP and TXON pins. The DSP is notified when the transmission is completed. For receiving baseband data, a DSP can program CSP1093's event timing and control register with the exact time to start receiving I and Q samples through TXIP and TXIN pins. When that time is reached, the control portion of the event timing and control register will start the baseband receive section converting I and Q sample pairs. The samples are stored in a double-buffered register until the register contains 32 sample pairs. CSP1093 then notifies the DSP which has ample time to read the information out before the next 32 sample pairs are stored. The voice band ADC converter issues an interrupt to the DSP whenever it finishes converting a 16-bit PCM word. The DSP then reads the new input sample and simultaneously loads the voice band output DAC converter with a new PCM output word. The voice band output can be connected directly to a speaker via AOUTAN and AOUTAP pins and be connected to a Ear-mic speaker via AOUTBN and AOUTBP pins.

### 8) X-TAL(13MHz)

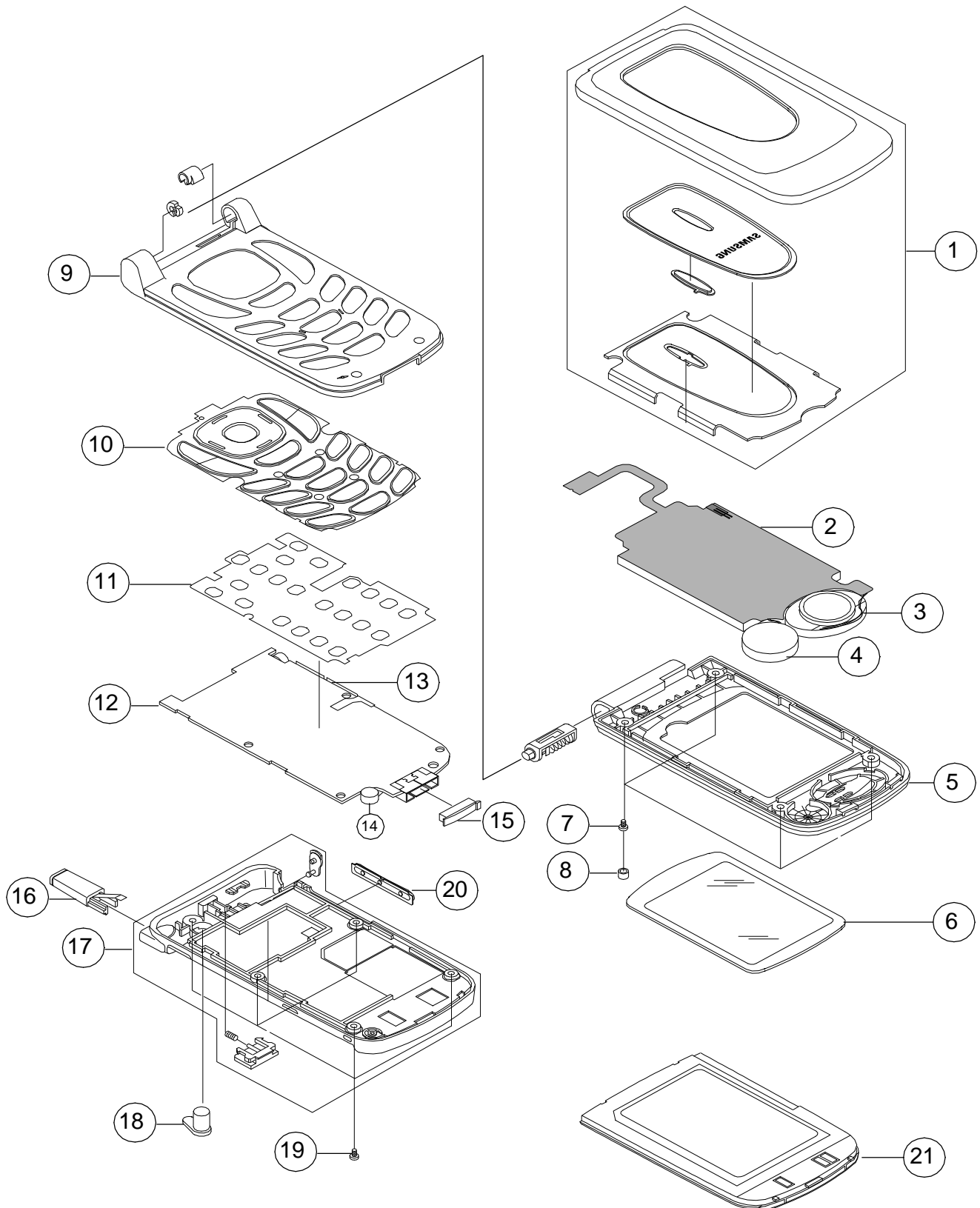
This system uses the 13MHz TCXO, TCO-9141B, Toyocom. AFC control signal from CSP1093 controls frequency from 13MHz x-tal. It generates the clock frequency. This clock is fed to CSP1093, Trident, YMU762 and Silab solution.

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### 3. SGH-X430 Exploded View and its Parts list

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#### 1. Cellular phone Exploded View



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## 2. Cellular phone Parts list

Location NO.		Description	SEC CODE	Remark
1		FOLDER UPPER	GH75-03664B	
2		LCD	GH07-00410A	
3		SPEAKER	3001-001448	
4		MOTOR	GH31-00067A	
5		FOLDER LOWER	GH75-03669A	
6		WINDOW LCD	GH75-03666A	
7		SCREW	6001-001478	
8		FOLDER SCREW CAP	GH73-02274A	
9		FRONT COVER	GH75-03663A	
10		KEYPAD	GH75-03668A	
11		DOMESHEET	GH59-00931A	
12		MAIN PBA	GH92-01606A	
13		VOLKEY FPCB	GH59-00934A	
14		MIC	GH30-00054A	
15		IF COVER	GH73-01331A	
16		ANTENNA	GH42-00341C	
17		REAR COVER	GH75-03385B	
18		RF COVER	GH73-02490B	
19		SCREW	6001-001479	
20		SIDE KEY	GH72-08862A	
21		BATTERY	GH43-01070B	

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### 3. Test Jig (GH80-00865A)



3-1. RF Test Cable  
(GH39-00182A)



3-2. Test Cable  
(GH39-00127A)



3-3. Serial Cable



3-4. Power Supply Cable



3-5. DATA CABLE  
(GH39-00159A)



3-6. TA  
(GH44-00482A)



#### 4. SGH-X430 MAIN Electrical Parts List

Design LOC	SEC CODE	Design LOC	SEC CODE
ZD800	0406-001083	V908	1405-001082
ZD801	0406-001083	V909	1405-001082
Q1000	0501-000225	V910	1405-001082
Q300	0504-000168	V911	1405-001082
U501	0504-001151	V806	1405-001093
U502	0504-001151	V900	1405-001112
D900	0601-001094	V901	1405-001112
D901	0601-001094	V902	1405-001112
D902	0601-001094	R103	2007-000138
D903	0601-001094	R211	2007-000138
D904	0601-001094	R1018	2007-000140
D905	0601-001094	R802	2007-000140
D906	0601-001094	R803	2007-000140
D907	0601-001094	R804	2007-000140
D908	0601-001094	R805	2007-000140
SW900	1009-001010	R806	2007-000140
U600	1109-001274	R811	2007-000140
U300	1203-002902	R1009	2007-000141
U1000	1204-001960	R1011	2007-000141
U500	1204-001984	R1006	2007-000148
U401	1209-001219	R1012	2007-000148
V805	1405-001018	R1019	2007-000148
V1000	1405-001082	R305	2007-000157
V1001	1405-001082	R400	2007-000157
V1002	1405-001082	R402	2007-000157
V1003	1405-001082	R800	2007-000157
V700	1405-001082	R801	2007-000157
V702	1405-001082	R808	2007-000157
V703	1405-001082	R1021	2007-000159
V704	1405-001082	R1000	2007-000162
V705	1405-001082	R1003	2007-000162
V706	1405-001082	R1008	2007-000162
V800	1405-001082	R1014	2007-000162
V801	1405-001082	R504	2007-000162
V802	1405-001082	R505	2007-000162
V803	1405-001082	R910	2007-000162
V804	1405-001082	R304	2007-000167
V808	1405-001082	R401	2007-000170
V903	1405-001082	R1013	2007-000171
V904	1405-001082	R1016	2007-000171
V905	1405-001082	R105	2007-000171
V907	1405-001082	R204	2007-000171

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Design LOC	SEC CODE	Design LOC	SEC CODE
R214	2007-000171	R224	2007-000171
R302	2007-000171	R308	2007-008263
R310	2007-000171	C1005	2203-000233
R501	2007-000171	C1028	2203-000233
R600	2007-000171	C1030	2203-000233
R807	2007-000171	C108	2203-000233
R809	2007-000171	C110	2203-000233
R911	2007-000171	C111	2203-000233
R1001	2007-000172	C112	2203-000233
R1002	2007-000172	C113	2203-000233
R101	2007-000172	C313	2203-000233
R300	2007-000172	C324	2203-000233
R407	2007-000172	C602	2203-000233
R601	2007-000172	C708	2203-000233
R700	2007-000172	C801	2203-000233
R810	2007-000566	C117	2203-000254
R303	2007-000758	C118	2203-000254
R1004	2007-000775	C119	2203-000254
R1005	2007-000775	C120	2203-000254
R1010	2007-001119	C228	2203-000254
R102	2007-001308	C314	2203-000254
R1007	2007-001325	C400	2203-000254
R1017	2007-001333	C401	2203-000254
R100	2007-002797	C402	2203-000254
R900	2007-007009	C403	2203-000254
R901	2007-007009	C407	2203-000254
R902	2007-007009	C409	2203-000254
R903	2007-007009	C410	2203-000254
R904	2007-007009	C411	2203-000254
R905	2007-007009	C412	2203-000254
R906	2007-007009	C417	2203-000254
R907	2007-007009	C508	2203-000254
R908	2007-007009	C509	2203-000254
R405	2007-007107	C510	2203-000254
R301	2007-007137	C511	2203-000254
R306	2007-007142	C512	2203-000254
R403	2007-007142	C513	2203-000254
R502	2007-007200	C514	2203-000254
R503	2007-007200	C515	2203-000254
R404	2007-007308	C604	2203-000254
R406	2007-007308	C700	2203-000254
R223	2007-000171	C104	2203-000278

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#### 4. SGH-X430 MAIN Electrical Parts List

Design LOC	SEC CODE	Design LOC	SEC CODE
C1023	2203-000330	C1000	2203-002443
C1011	2203-000386	C102	2203-005050
C115	2203-000386	C103	2203-005050
C209	2203-000386	C518	2203-005052
C1014	2203-000438	C1001	2203-005061
C1021	2203-000438	C1002	2203-005061
C1022	2203-000438	C1003	2203-005061
C707	2203-000438	C1007	2203-005061
C1006	2203-000585	C1015	2203-005061
C100	2203-000628	C300	2203-005061
C414	2203-000628	C302	2203-005061
C416	2203-000628	C405	2203-005061
C406	2203-000679	C415	2203-005061
C1012	2203-000812	C418	2203-005061
C1019	2203-000812	C506	2203-005061
C225	2203-000812	C600	2203-005061
C227	2203-000812	C601	2203-005061
C303	2203-000812	C1009	2203-005065
C304	2203-000812	C1018	2203-005065
C305	2203-000812	C504	2203-005065
C501	2203-000812	C105	2203-005234
C507	2203-000812	C107	2203-005234
C710	2203-000812	C208	2203-005393
C711	2203-000812	C106	2203-005450
C1013	2203-000885	C519	2203-005450
C203	2203-000995	C224	2203-005482
C1010	2203-001072	C322	2203-005482
C503	2203-001153	C701	2203-005482
C1020	2203-001239	C702	2203-005482
C1008	2203-001259	C715	2203-005482
C408	2203-001405	C900	2203-005482
C116	2203-001412	C901	2203-005482
C301	2203-001598	C109	2203-005496
C307	2203-001598	C223	2203-005496
C308	2203-001598	C226	2203-005496
C309	2203-001598	C404	2203-005496
C310	2203-001598	C413	2203-005496
C311	2203-001598	C505	2203-005496
C312	2203-001598	C703	2203-005509
C315	2203-001598	C902	2203-006053
C316	2203-001598	C323	2203-006105
C903	2203-001598	C306	2203-006257

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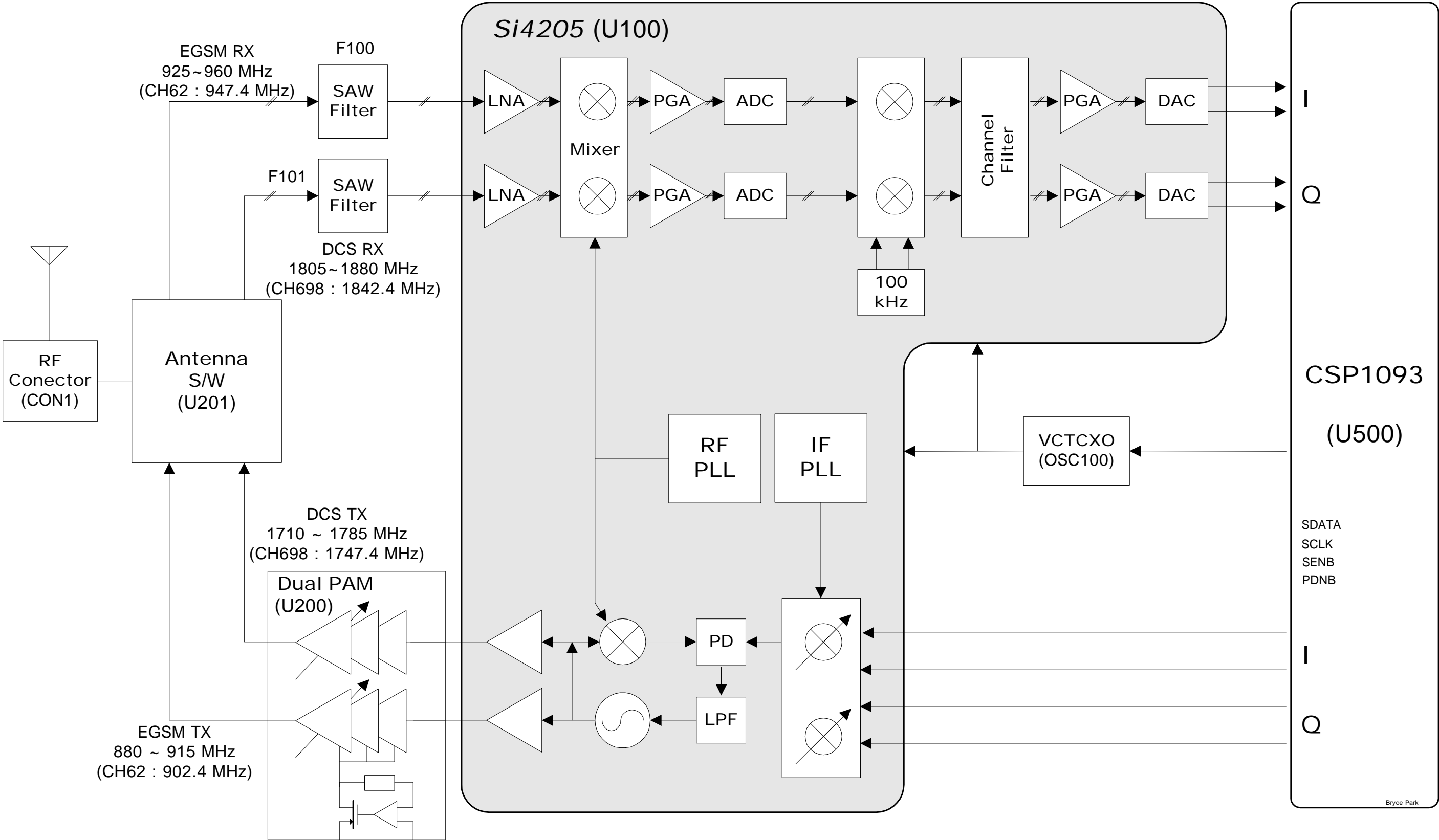
#### 4. SGH-X430 MAIN Electrical Parts List

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Design LOC	SEC CODE
C202	2404-001020
C318	2404-001105
C200	2404-001134
C1016	2404-001305
C1004	2404-001268
C319	2404-001268
C800	2404-001268
C705	2503-001041
C706	2503-001041
L209	2703-002202
L102	2703-002203
L210	2703-002203
L105	2703-002205
L204	2703-002207
L205	2703-002207
L106	2703-002365
L103	2703-002484
L100	2703-002485
OSC400	2801-003747
OSC100	2809-001260
F100	2904-001417
F101	2904-001419
U201	2909-001197
CON1	3705-001287
CN300	3709-001244
CN700	3711-005078
CN1000	3722-001715
M300	4302-001130
U400	GH09-00023A

5. SGH-X430 Block Diagrams

1. RF Solution Block Diagram

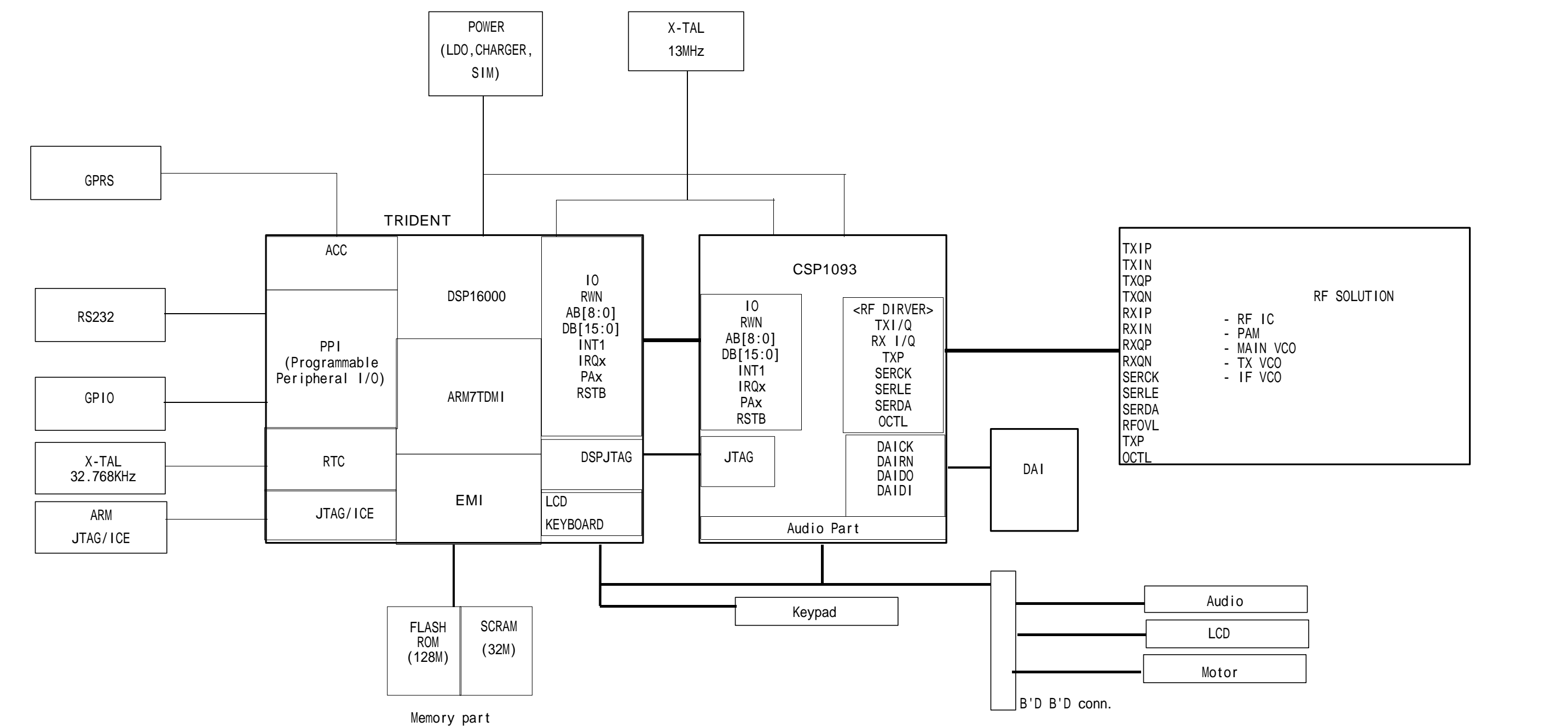


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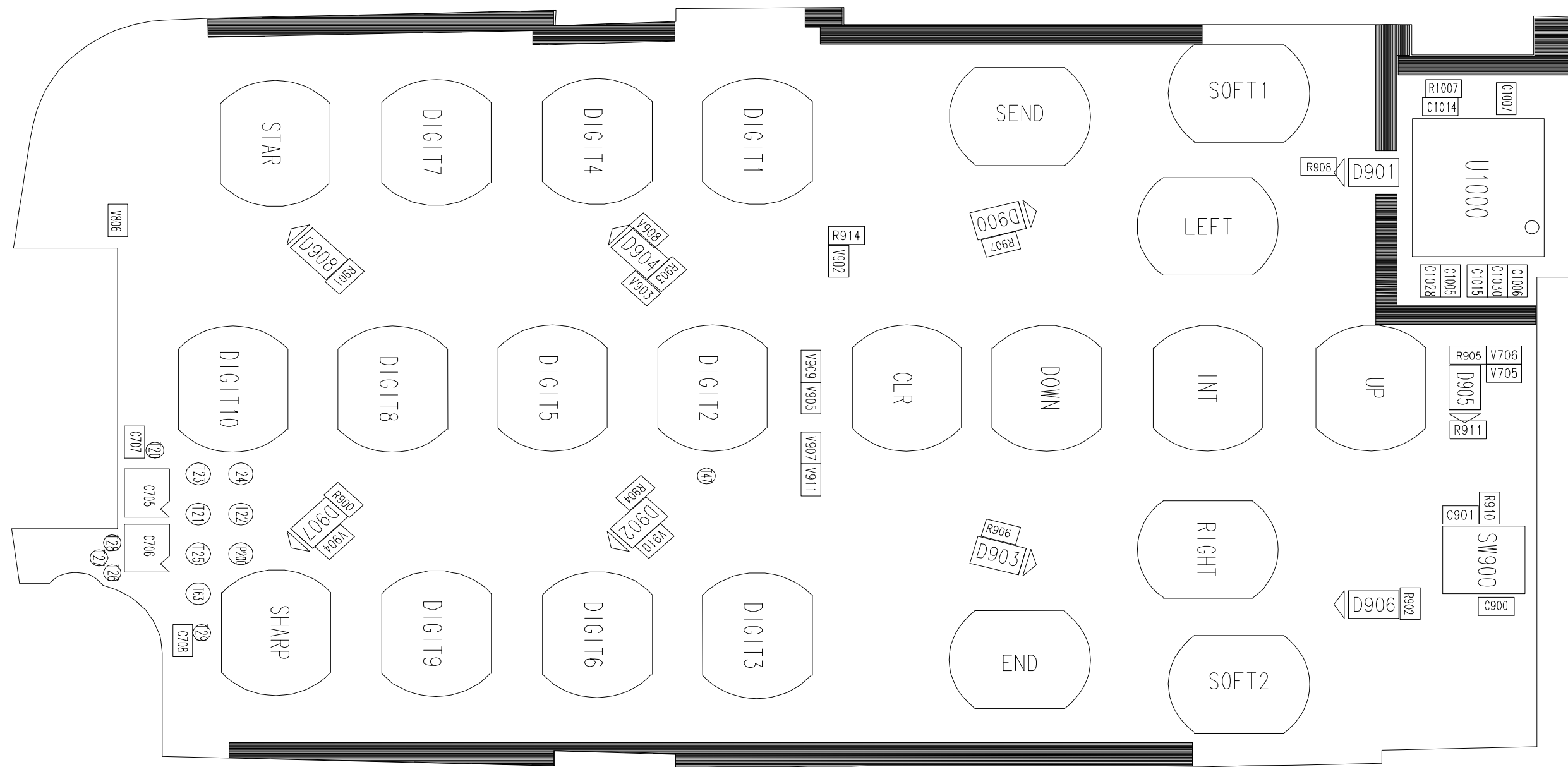
5. SGH-X430 Block Diagrams

2. Base Band Solution Block Diagram



6. SGH-X430 PCB Diagrams

1. Main PCB Top Diagram



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## 6. SGH-X430 PCB Diagrams

## 2. Main PCB Bottom Diagram

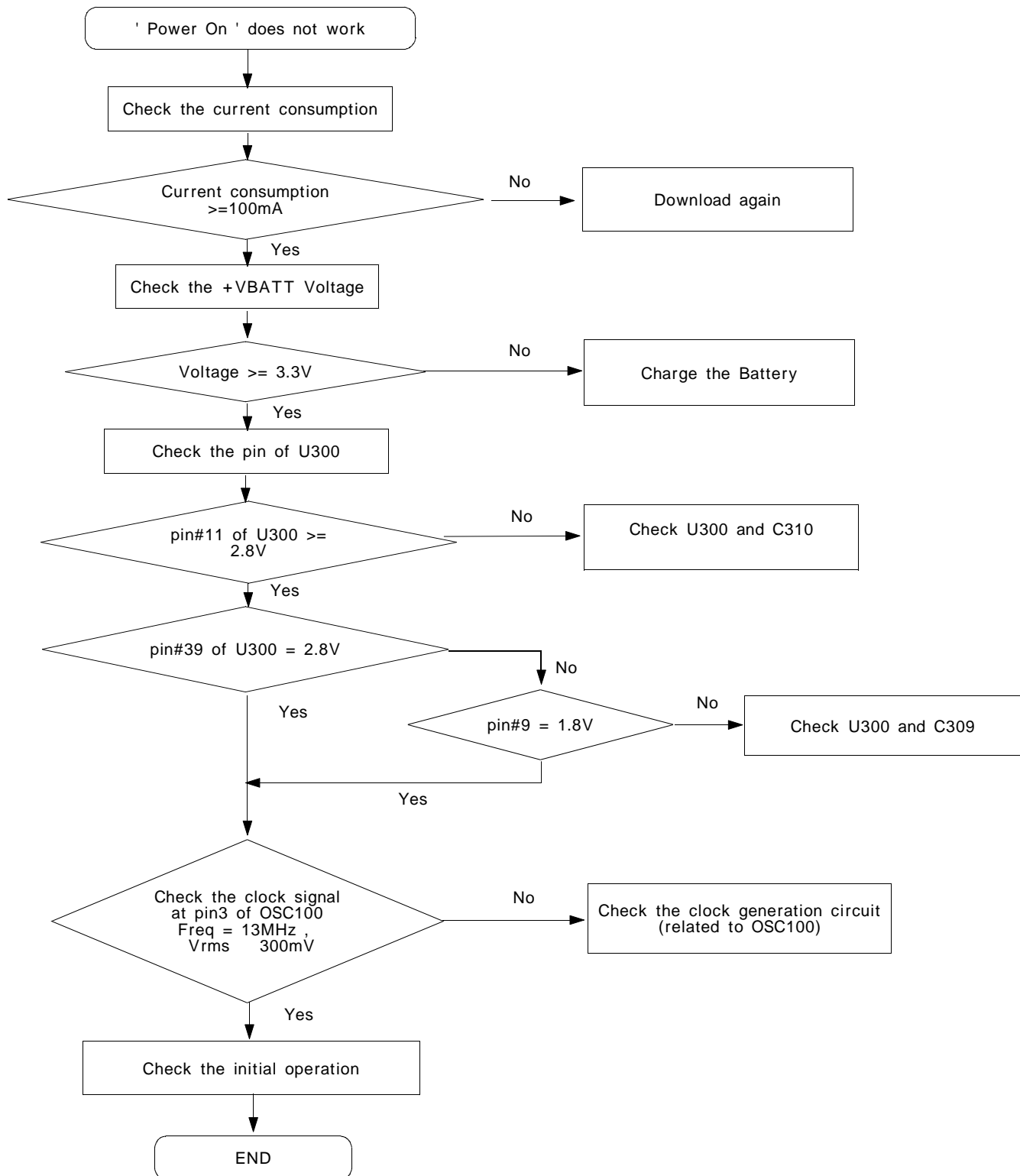


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## 7. SGH-X430 Flow Chart of Troubleshooting

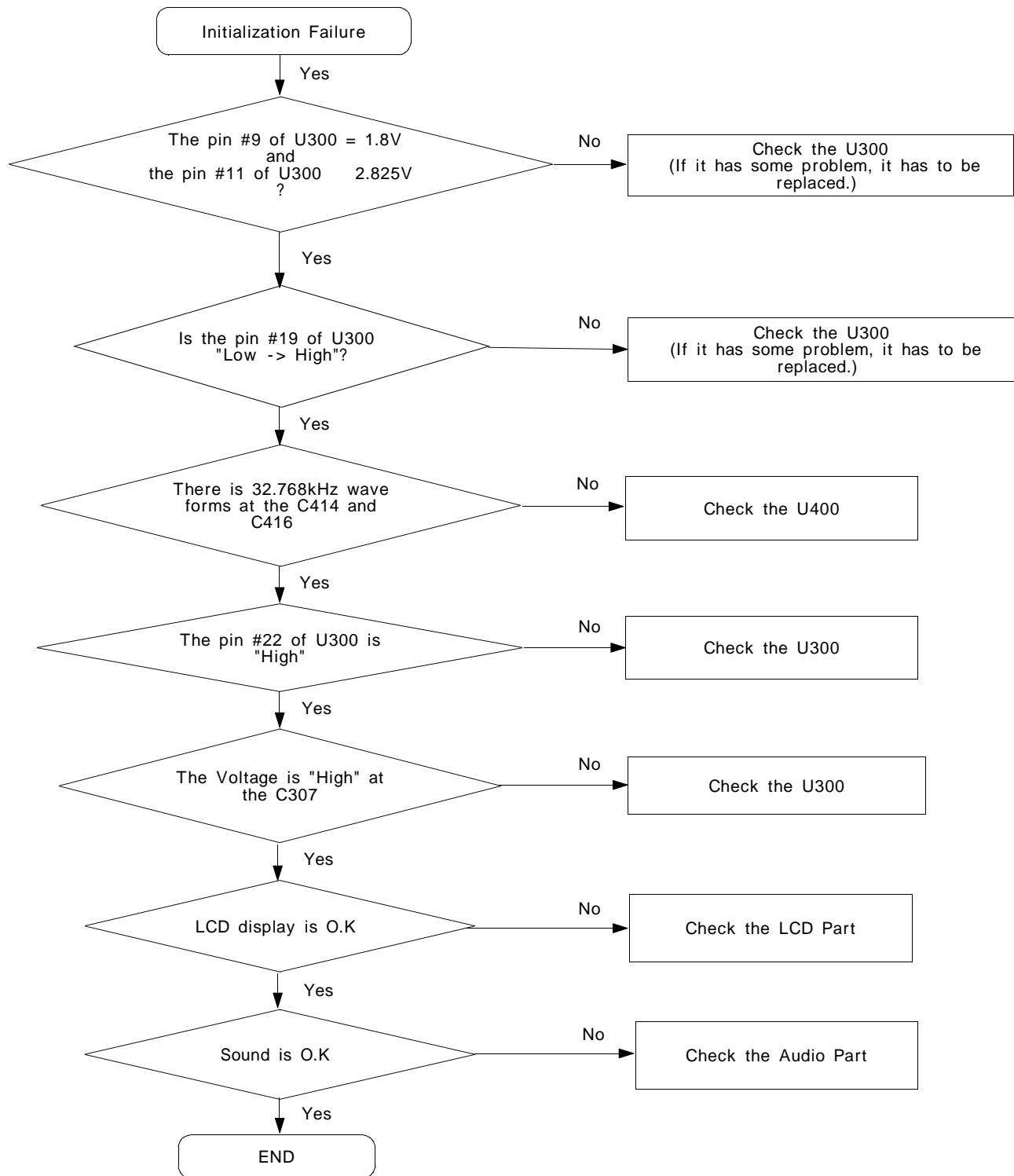
### 1. Power On





## 7. SGH-X430 Flow Chart of Troubleshooting

### 2. Initial

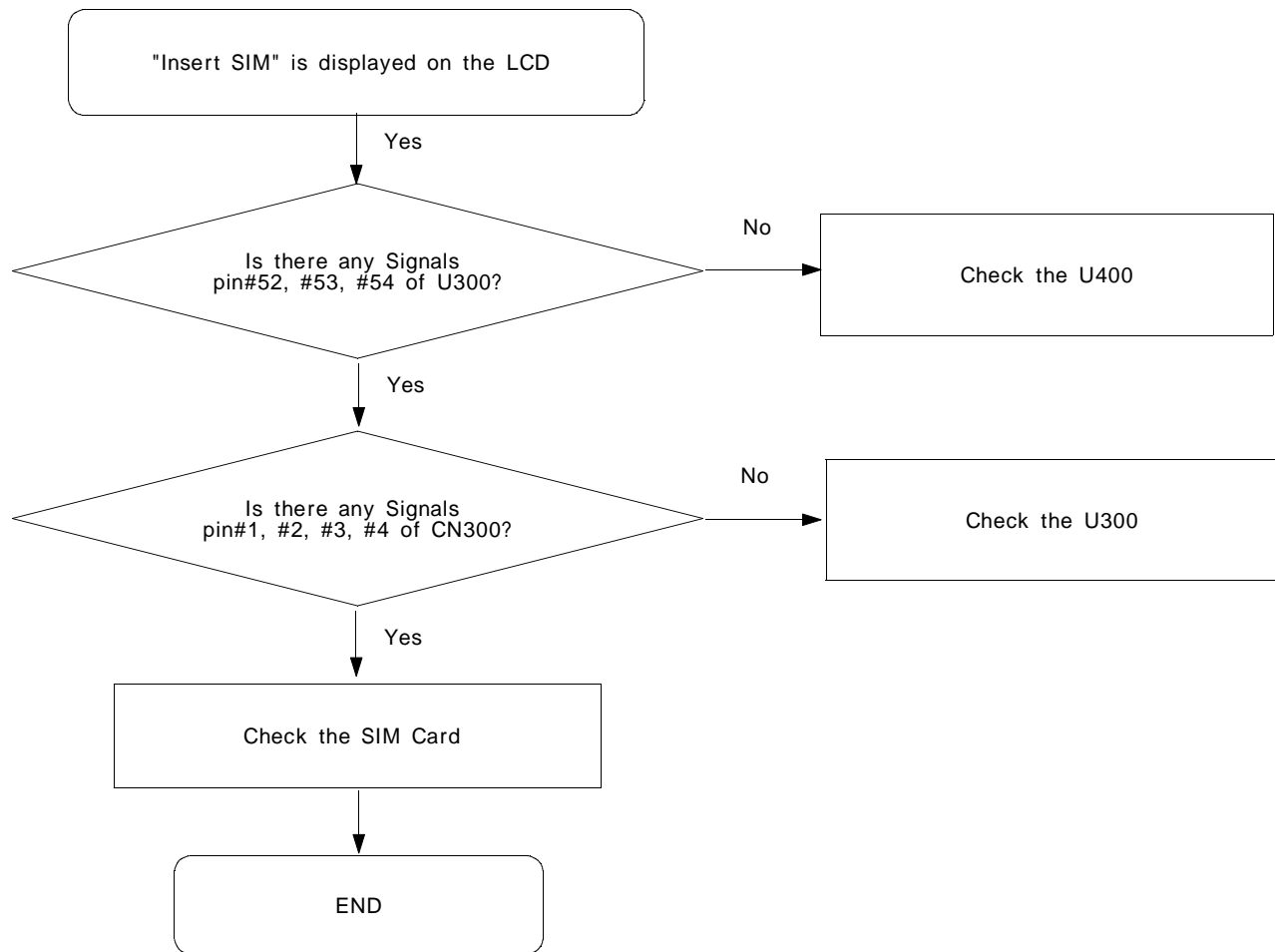


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## 7. SGH-X430 Flow Chart of Troubleshooting

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### 3. Sim Part

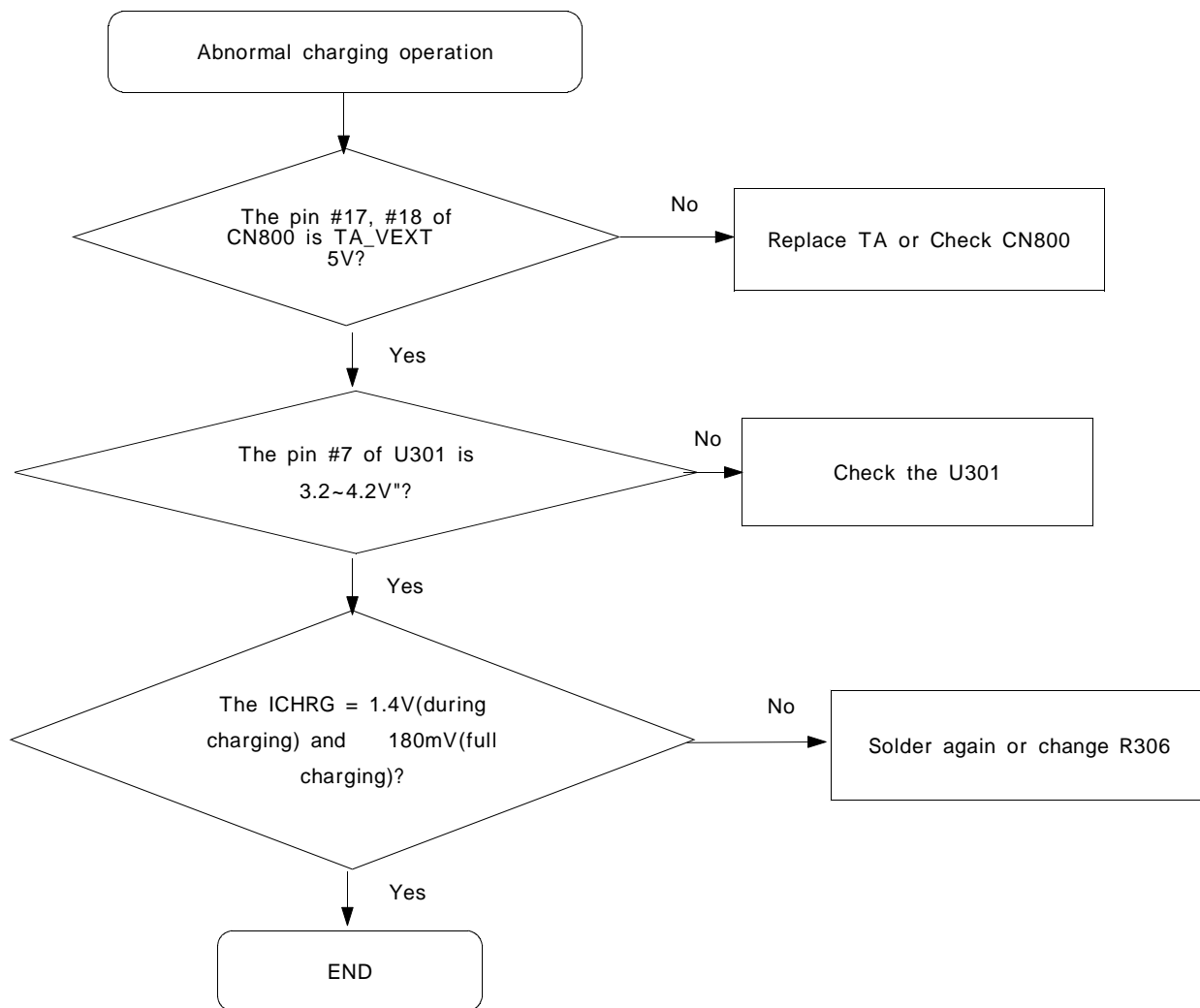


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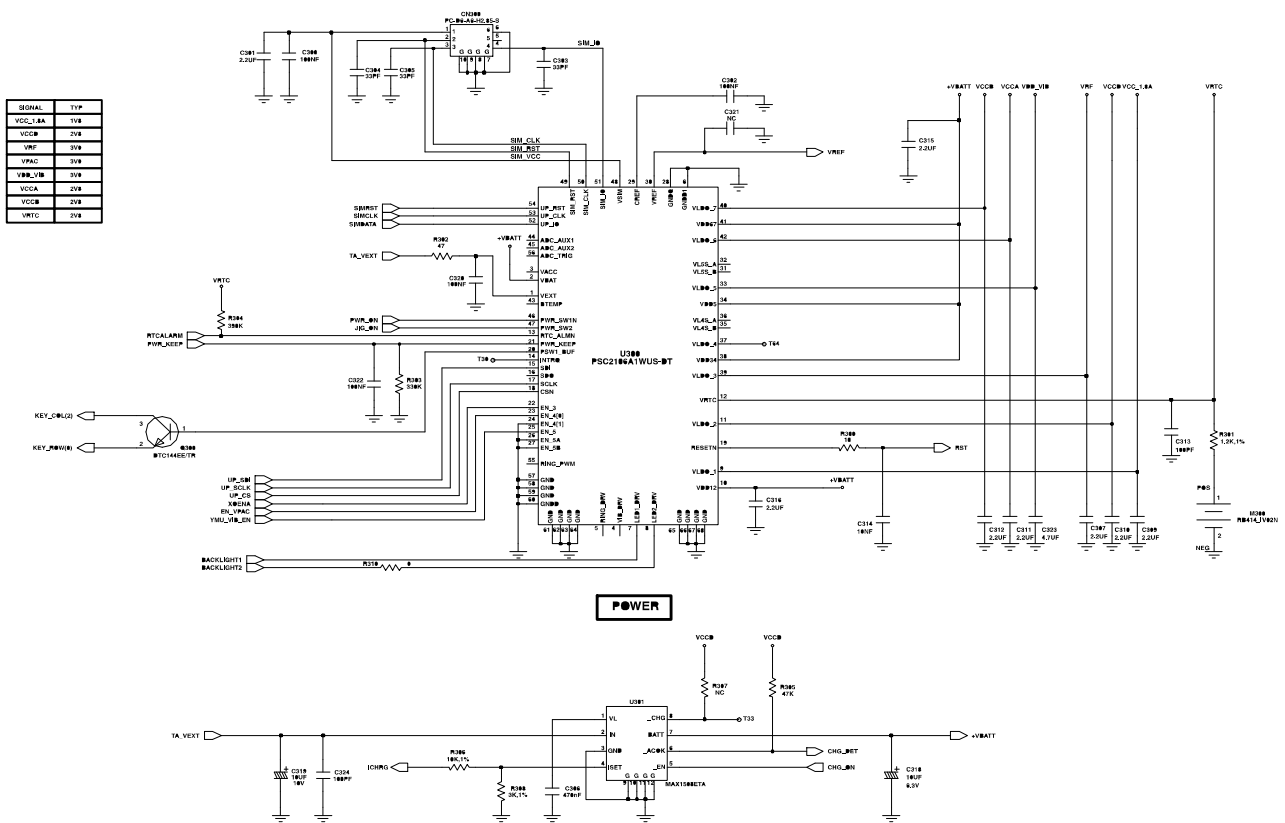
## 7. SGH-X430 Flow Chart of Troubleshooting

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### 4. Charging Part



## 7. SGH-X430 Flow Chart of Troubleshooting



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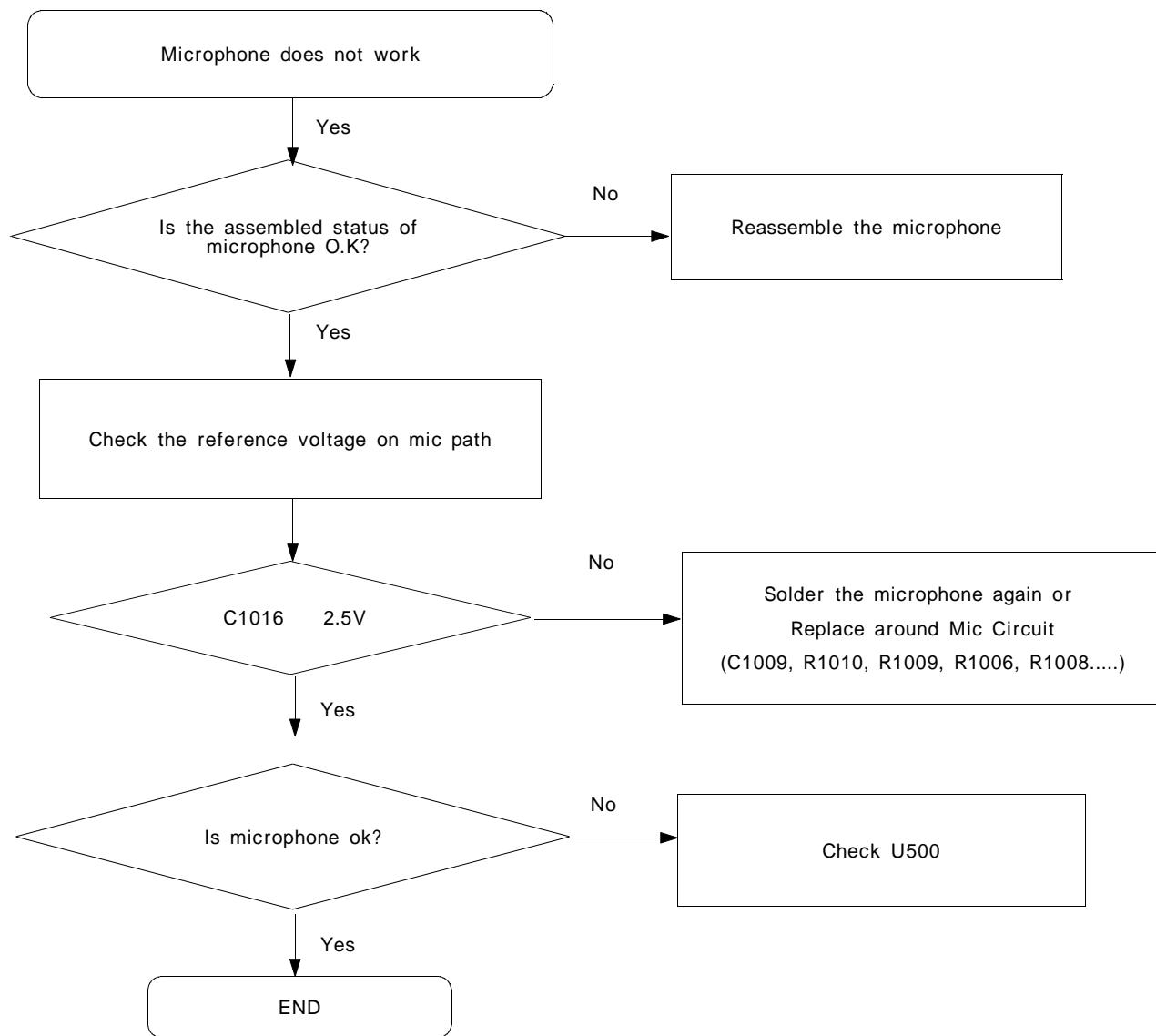
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## 7. SGH-X430 Flow Chart of Troubleshooting

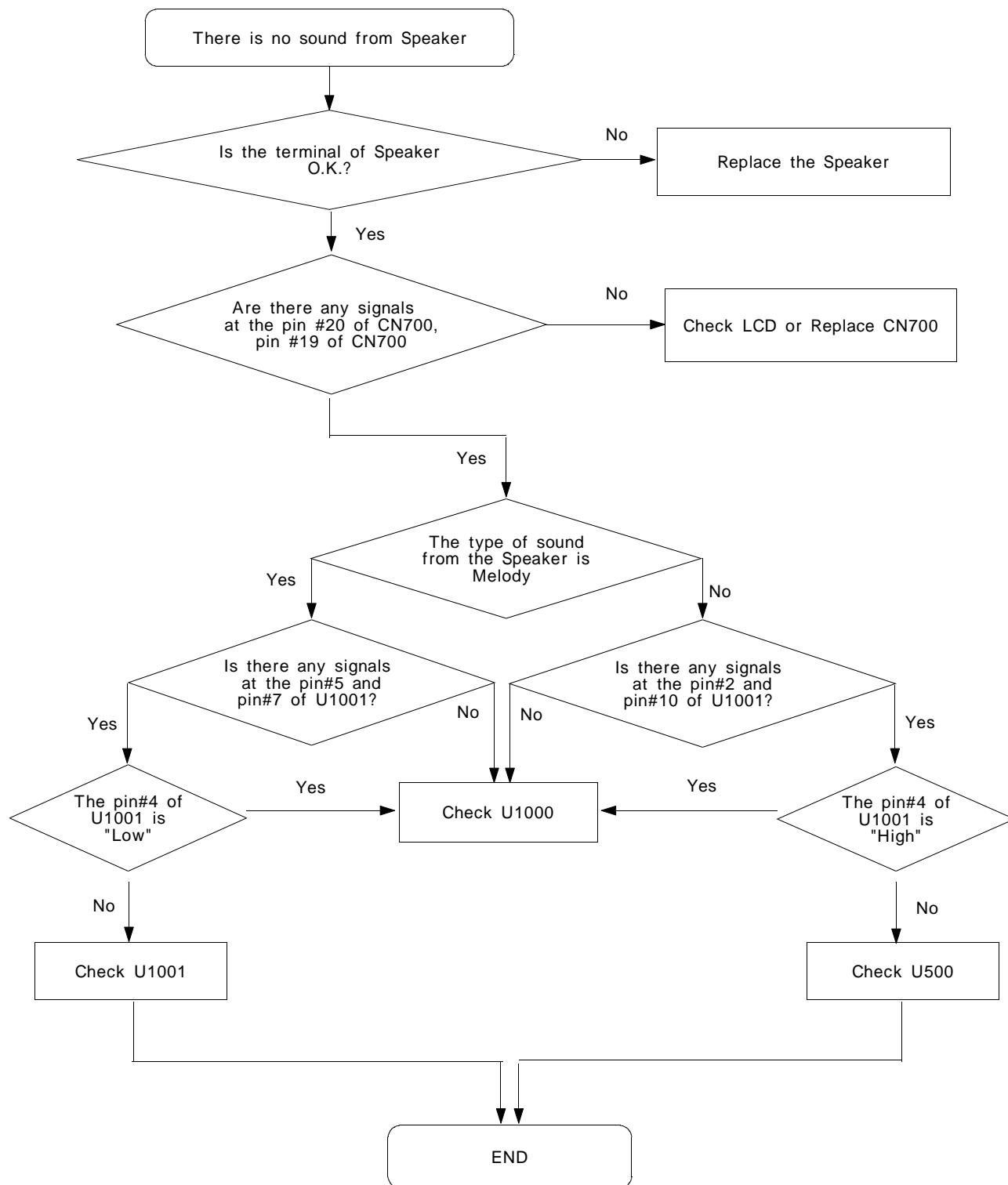
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### 5. Microphone Part

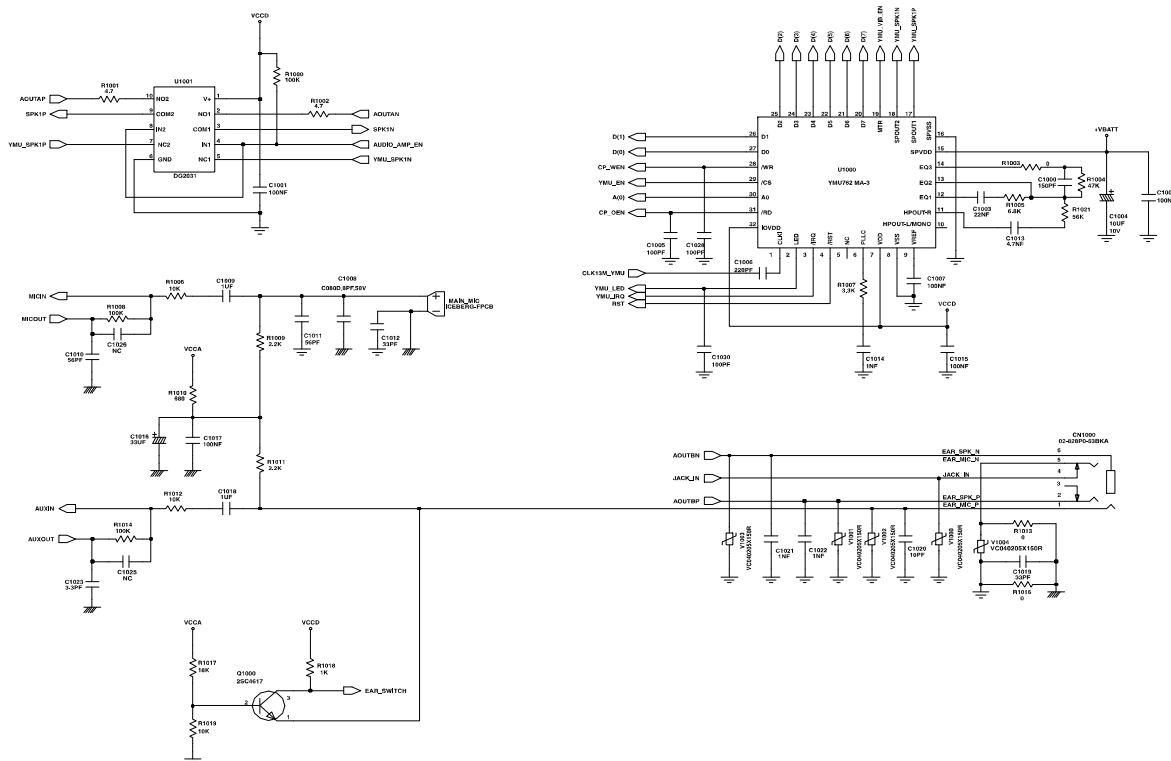


## 7. SGH-X430 Flow Chart of Troubleshooting

### 6. Speaker Part



## 7. SGH-X430 Flow Chart of Troubleshooting

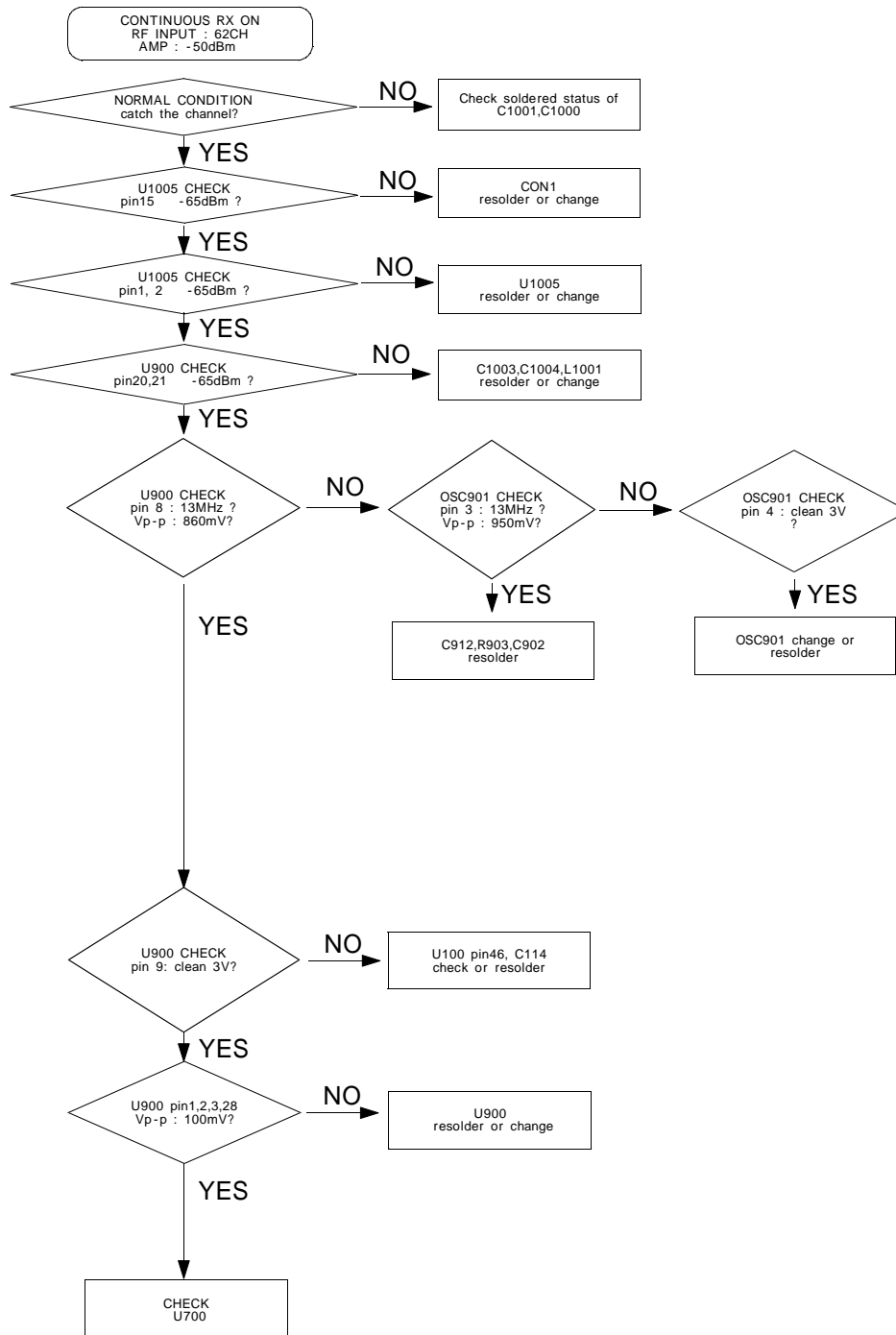


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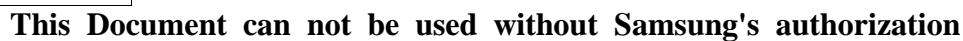
## 7. SGH-X430 Flow Chart of Troubleshooting

### 8. EGSM Receiver



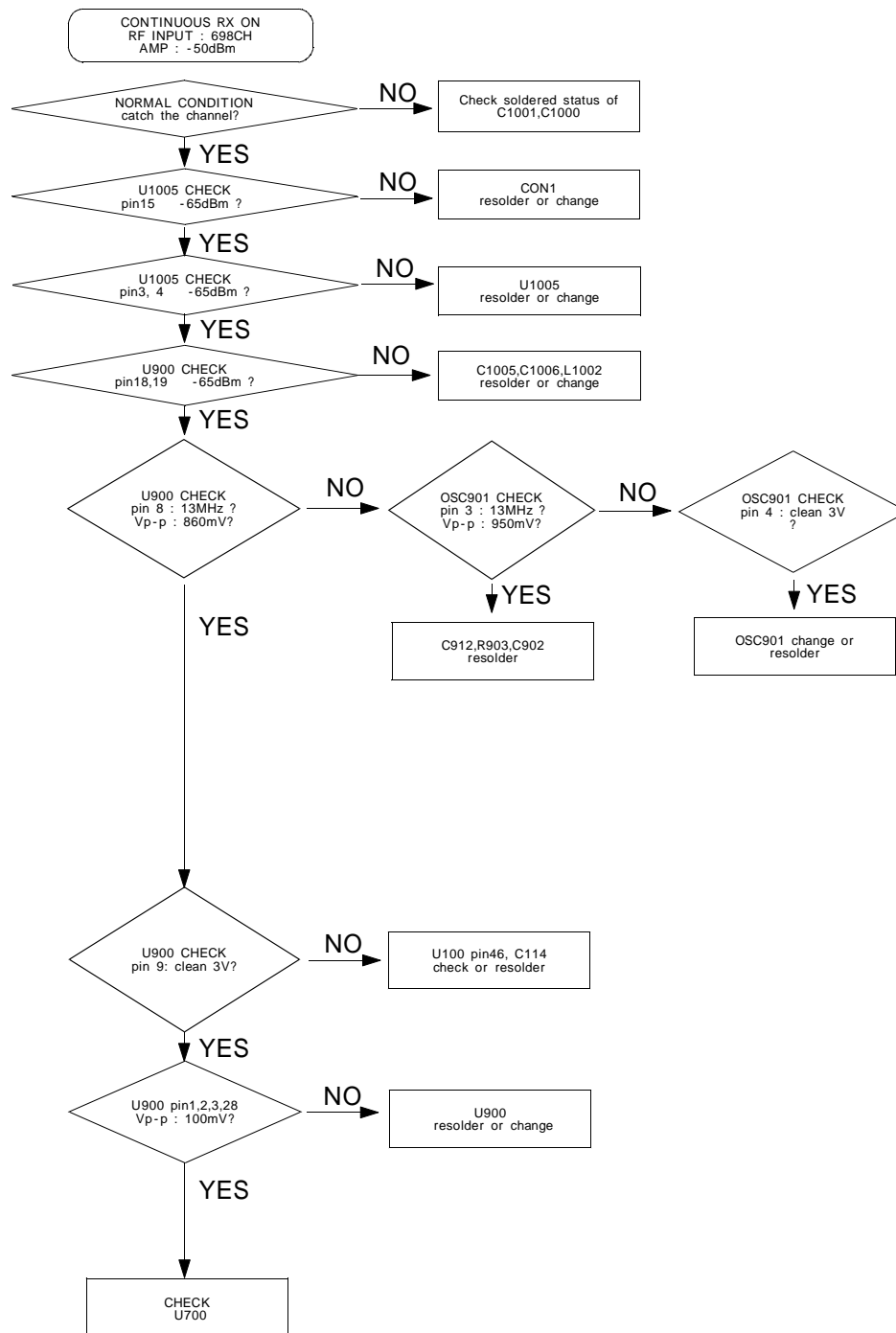


## 9. EGSM transmitter



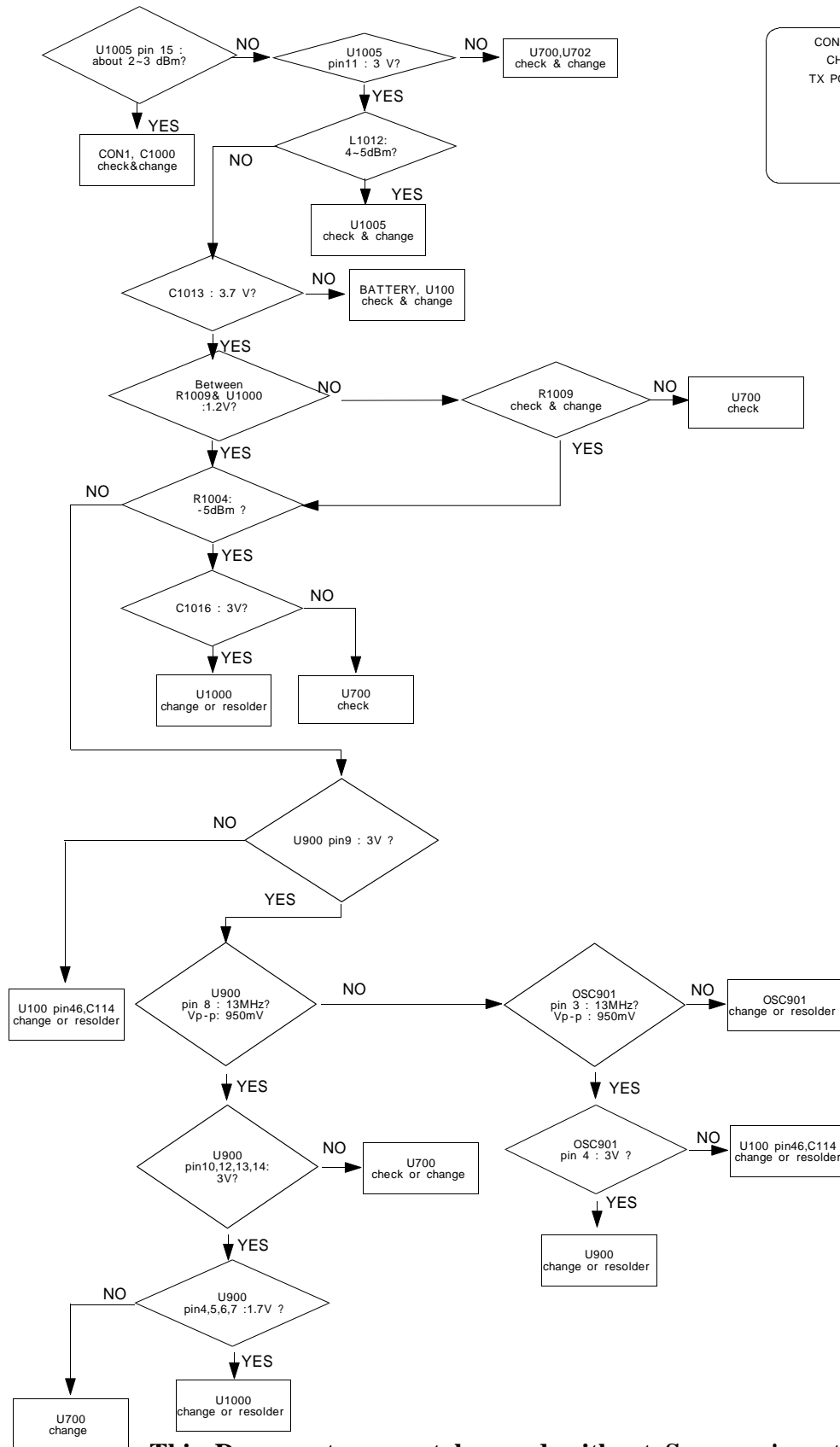
## 7. SGH-X430 Flow Chart of Troubleshooting

### 10. DCS Receiver



## 7. SGH-X430 Flow Chart of Troubleshooting

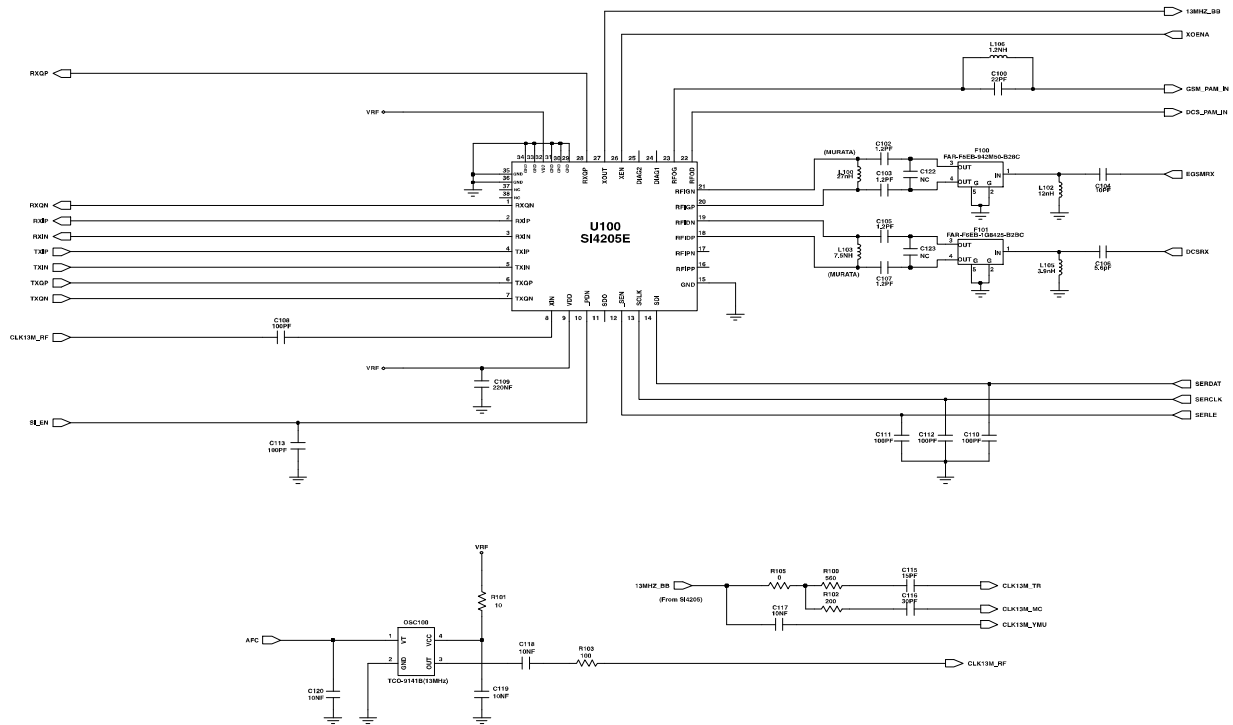
### 11. DCS transmitter



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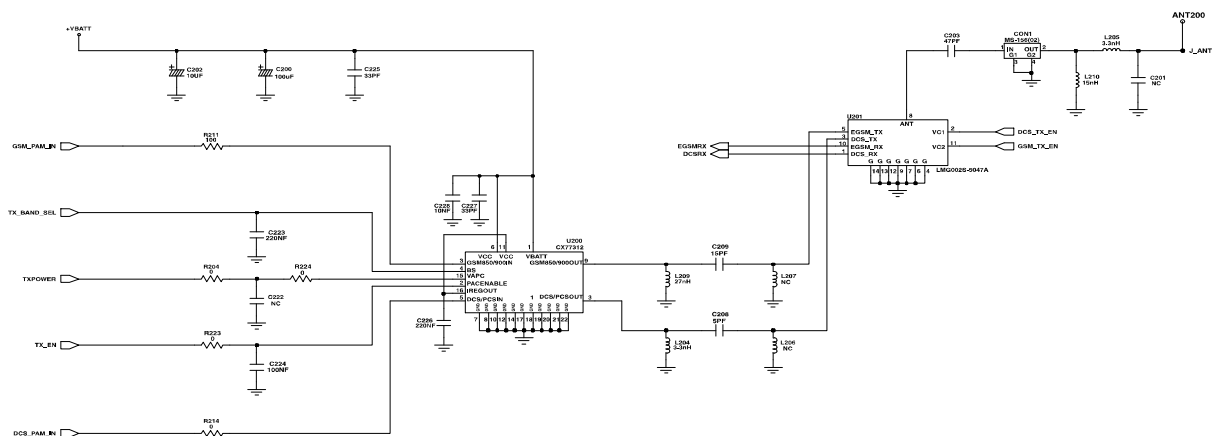
## 7. SGH-X430 Flow Chart of Troubleshooting



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## 7. SGH-X430 Flow Chart of Troubleshooting



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