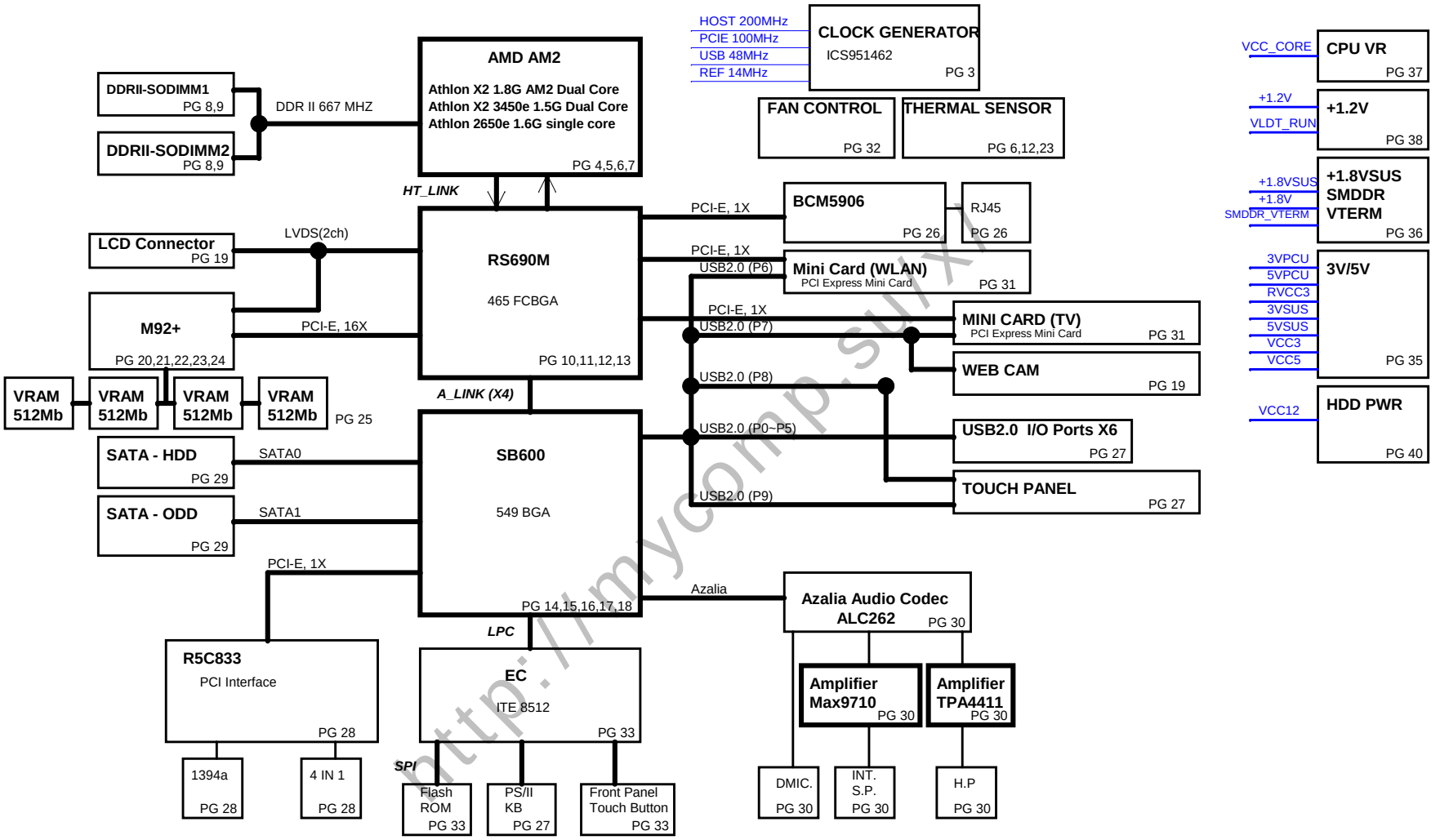
QU1T SYSTEM BLOCK DIAGRAM



Quanta Computer Inc.
PROJECT : QU1T

Size	Document Number	Rev
	BLOCK DIAGRAM	B

Date: Tuesday, September 01, 2009 Sheet 1 of 44

Voltage Rails

Power	Voltage	S0~S2	S3	S4	S5	Ctl Signal
VIN	19V	V	V	V	V	
5VPCU	5V	V	V	V	V	3V5V_EN
3VPCU	3V	V	V	V	V	3V5V_EN
15VPCU	15V	V	V	V	V	3V5V_EN
+3.3VALW	3V	V	V	V	V	STB_ON
+1.2VALW	1.2V	V	V	V	V	STB_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
VCC2.5	2.5V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
CPU_VDDA	2.5V	V				MAINON
VCC_NB	1.2V	V				MAINON
SMDDR_VTERM	0.9V	V				MAINON
VCC_CORE	By CPU	V				VR_ON
VCC1.1	1.1V	V				MAINON

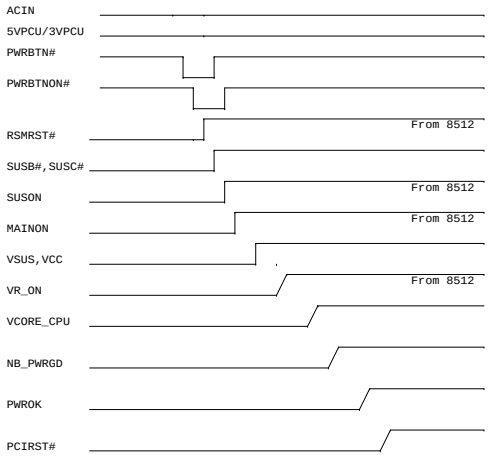
PCI DEVICES IRQ ROUTING

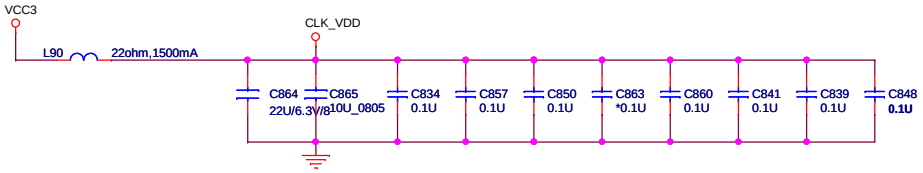
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLK
NB VGA	NA	A		
SB	AD31(INT)	NA	NA	
AC97/AZALIA	AD31	NA	B	INT
USB	AD30	NA	D	INT
R5C843	AD16	0	E/F/G	PCLK0

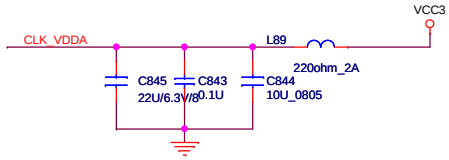
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : GND
LAYER 5 : VCC
LAYER 6 : IN2
LAYER 7 : GND
LAYER 8 : BOT

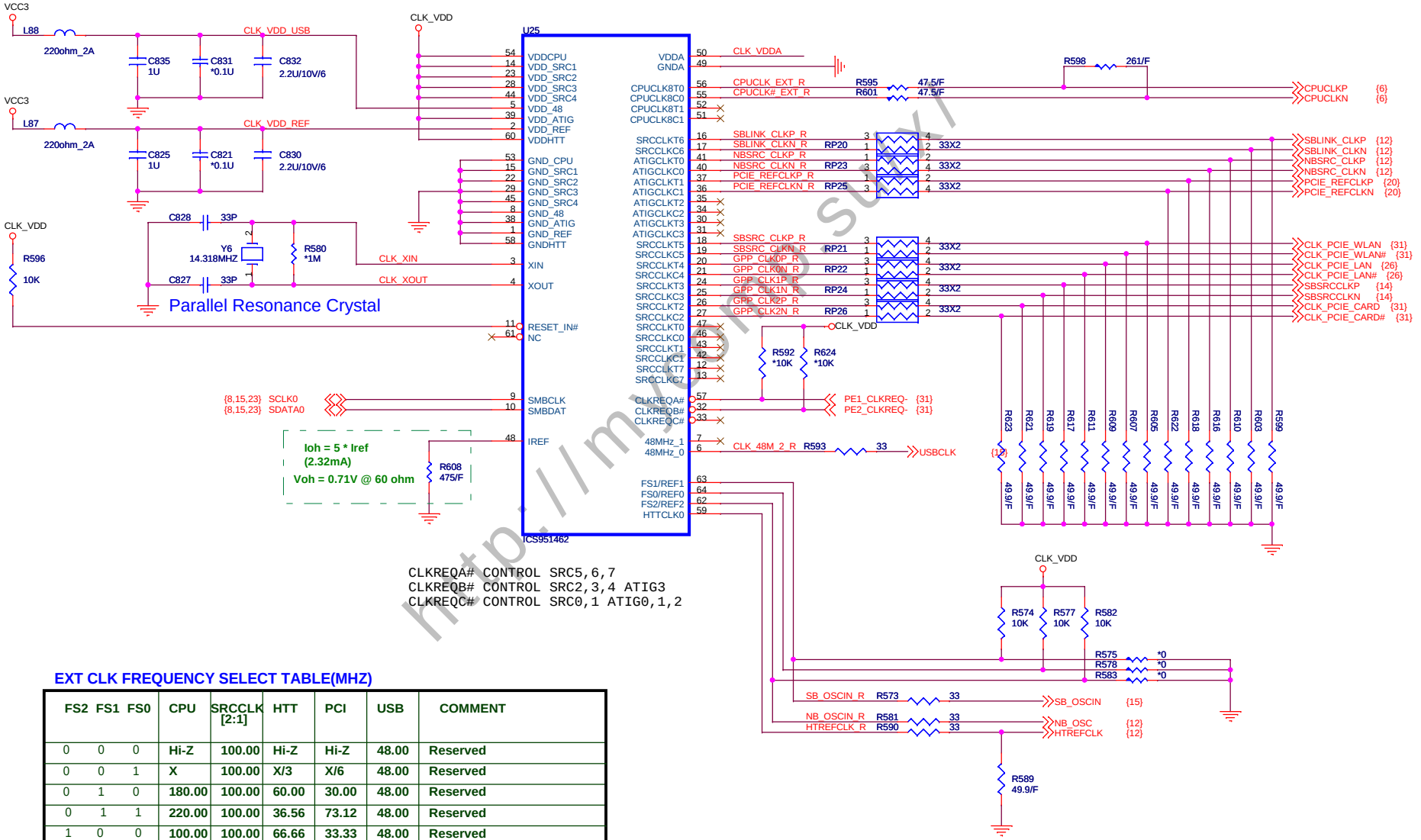
Power On Sequence







Put Decoupling Caps close to Clock Fen. power pin



CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4 ATIG3
CLKREQC# CONTROL SRC0,1 ATIG0,1,2

EXT CLK FREQUENCY SELECT TABLE(MHZ)

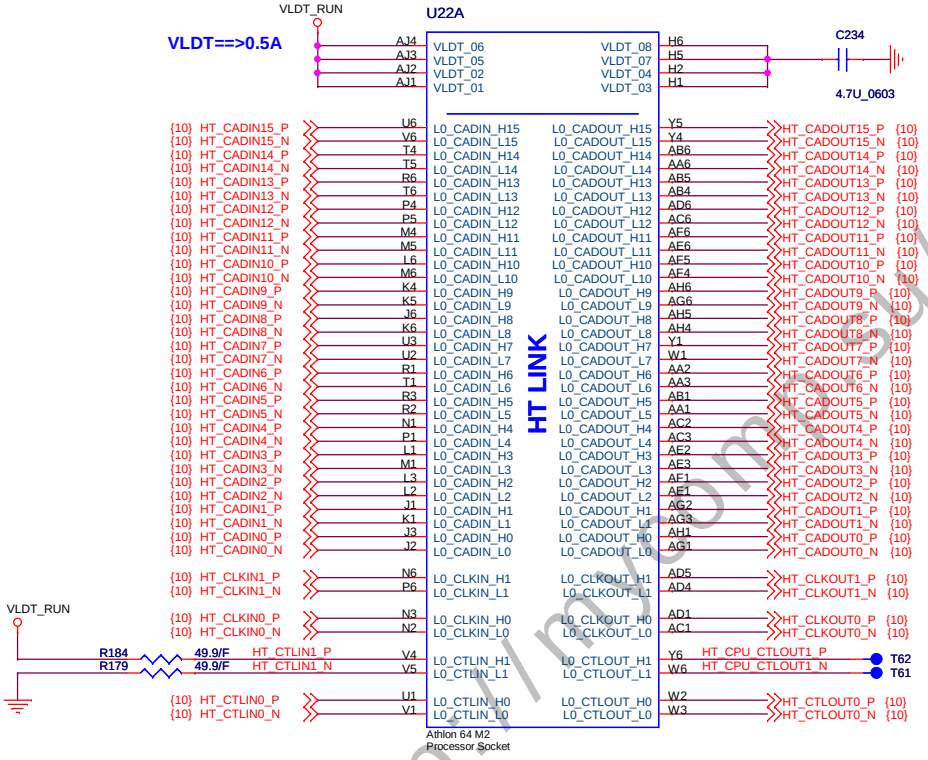
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

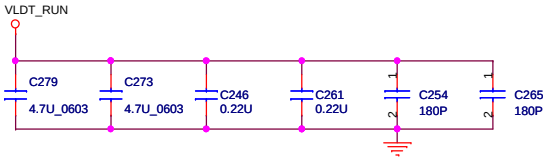
Check AMD clock

Quanta Computer Inc.
PROJECT : QU1T
Size | Document Number: Clock Generator | Rev B
Date: Tuesday, September 01, 2009 | Sheet 3 of 44

CPU HyperTransport Interface

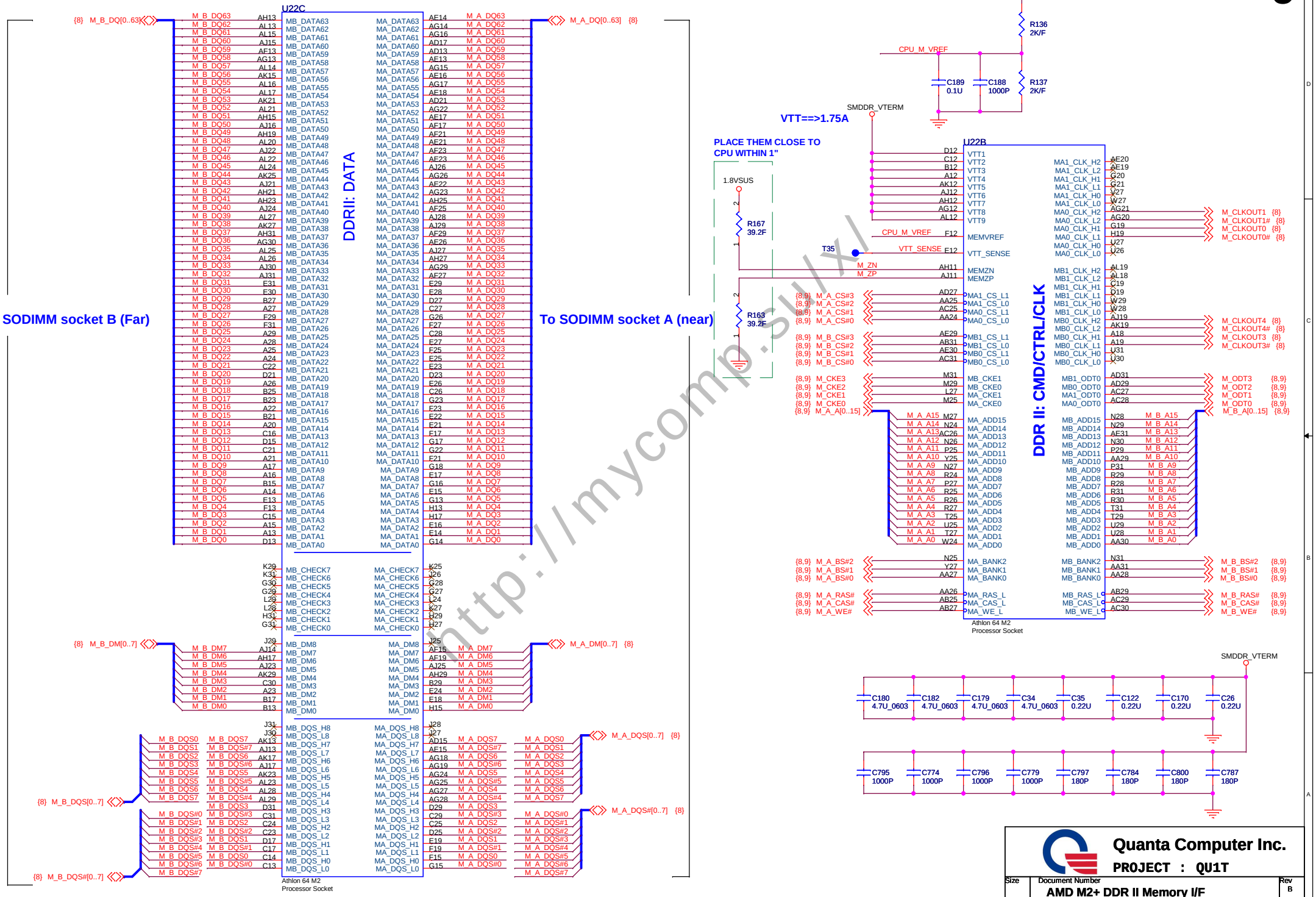
VDDLDTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.





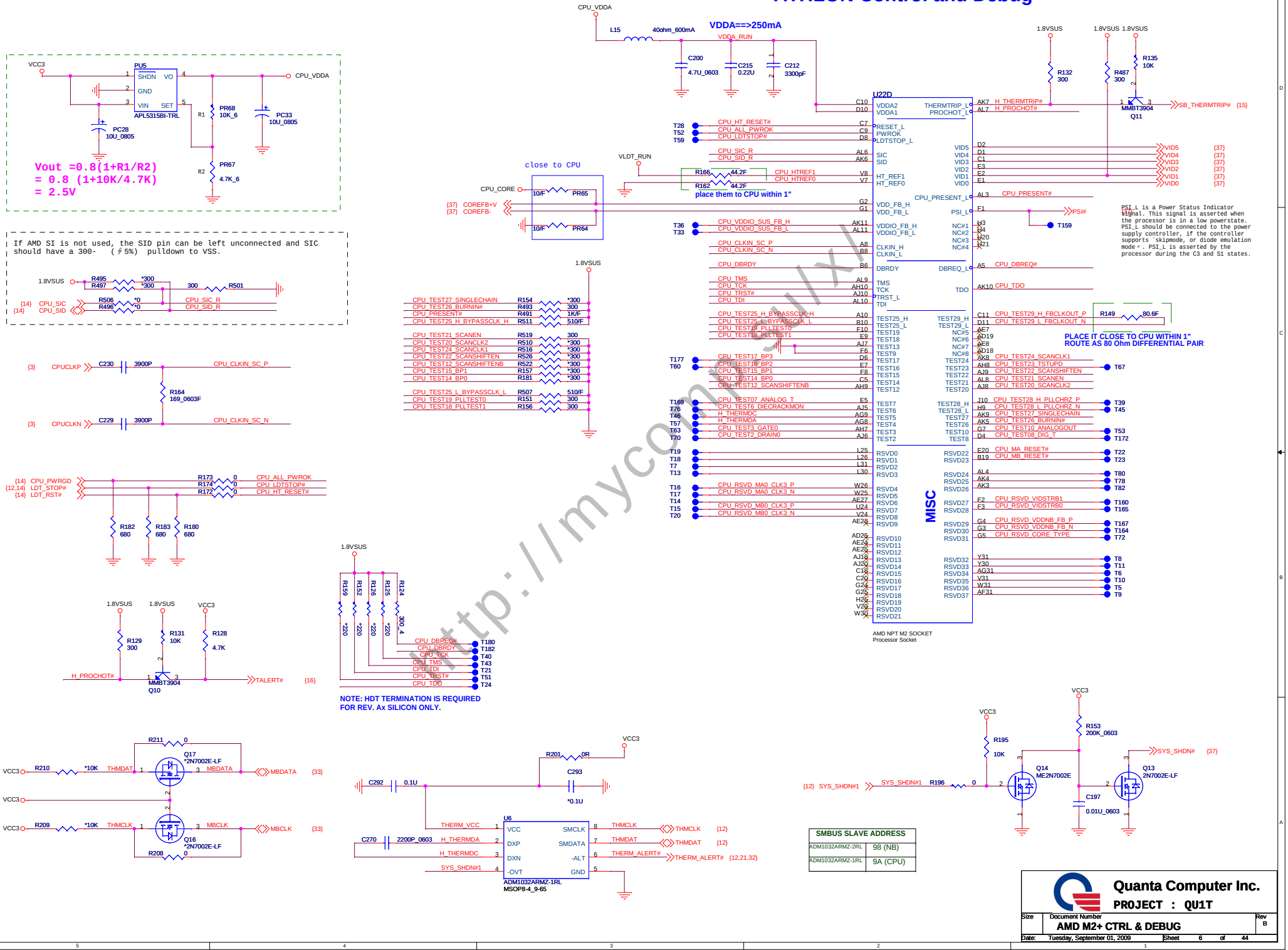
Quanta Computer Inc.		
PROJECT : QU1T		
Size	Document Number: AMD M2+ HT I/F	Rev: B
Date: Tuesday, September 01, 2009	Sheet 4 of 44	

Processor DDR2 Memory Interface



Quanta Computer Inc.			
PROJECT : QU1T			
Size	Document Number		Rev
	AMD M2+ DDR II Memory I/F		B
Date: Tuesday, September 01, 2009	Sheet 5 of 44		

ATHLON Control and Debug



PROCESSOR POWER AND GROUND

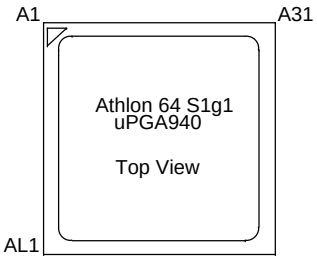
VDDIO==>3.6A

U22E — POWER1 — CPU_CORE — Athlon 64 M2 Processor Socket

U22F — POWER2 — CPU_CORE — 1.8VSUS

U22G — GND1 — Athlon 64 M2 Processor Socket

U22H — GND2



BOTTOMSIDE DECOUPLING

CPU_CORE

C223 0.22U, C224 0.22U, C222 0.01U, C225 180P

1.8VSUS

C144 10U_0805, C143 10U_0805, C166 0.22U, C169 0.22U

CPU_CORE

C204 10U_0603, C205 10U_0603, C203 10U_0603, C206 10U_0603, C207 10U_0603, C208 10U_0603, C209 10U_0603, C211 10U_0603, C210 10U_0603

CPU_CORE

C193 22U/6.3V_8, C194 22U/6.3V_8, C191 22U/6.3V_8, C192 22U/6.3V_8, C195 22U/6.3V_8, C183 22U/6.3V_8, C756 22U/6.3V_8, C759 22U/6.3V_8, C770 22U/6.3V_8, C185 22U/6.3V_8, C173 22U/6.3V_8, C174 22U/6.3V_8, C175 22U/6.3V_8, C176 22U/6.3V_8, C178 22U/6.3V_8

DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

1.8VSUS

C146 4.7U_0603, C145 4.7U_0603, C151 4.7U_0603, C147 4.7U_0603, C157 0.22U, C150 0.22U, C154 0.22U, C160 0.22U, C159 0.22U, C164 0.22U, C158 0.01U, C165 180P

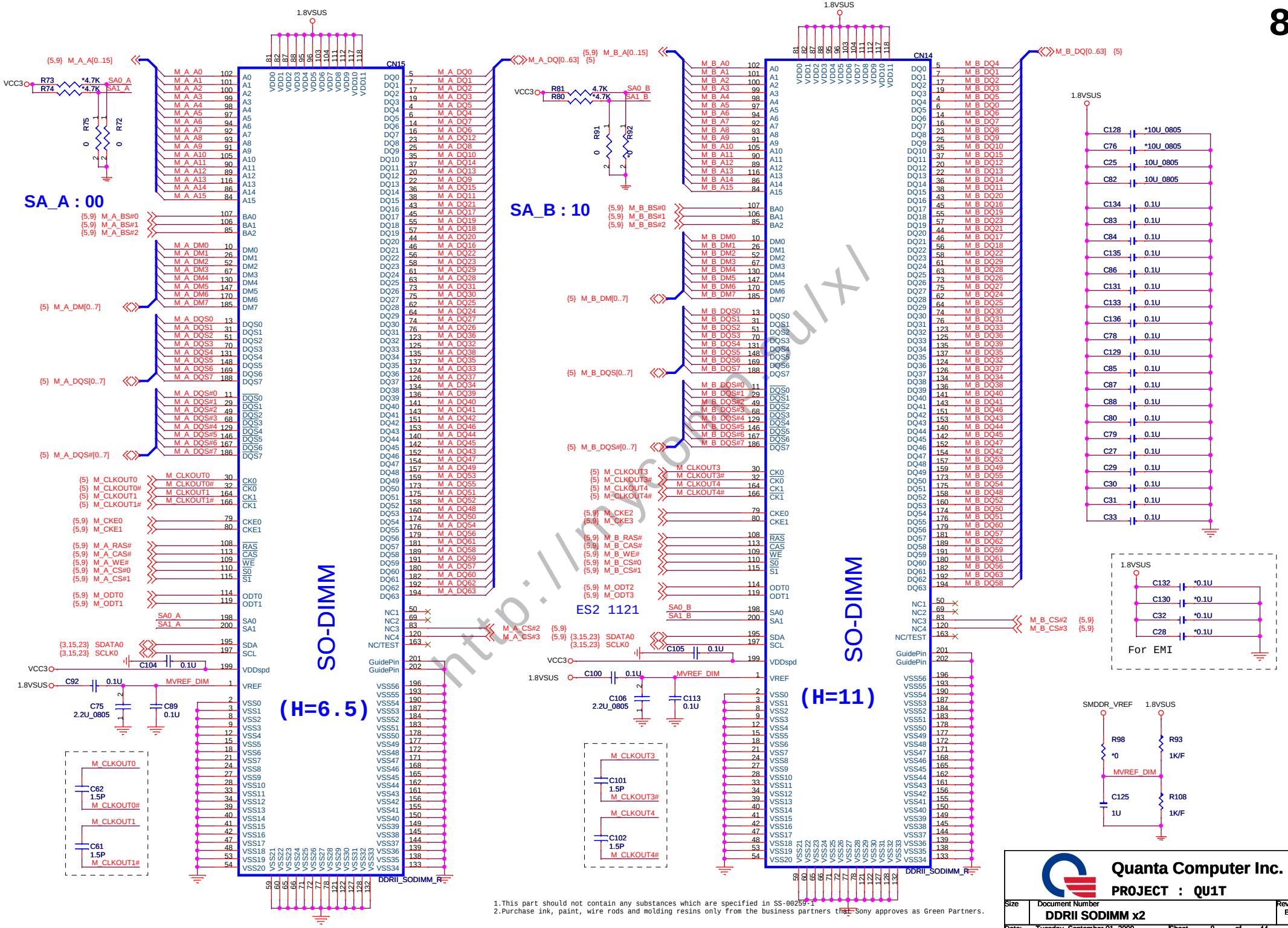
1.8VSUS

C153 0.01U, C155 180P, C167 180P

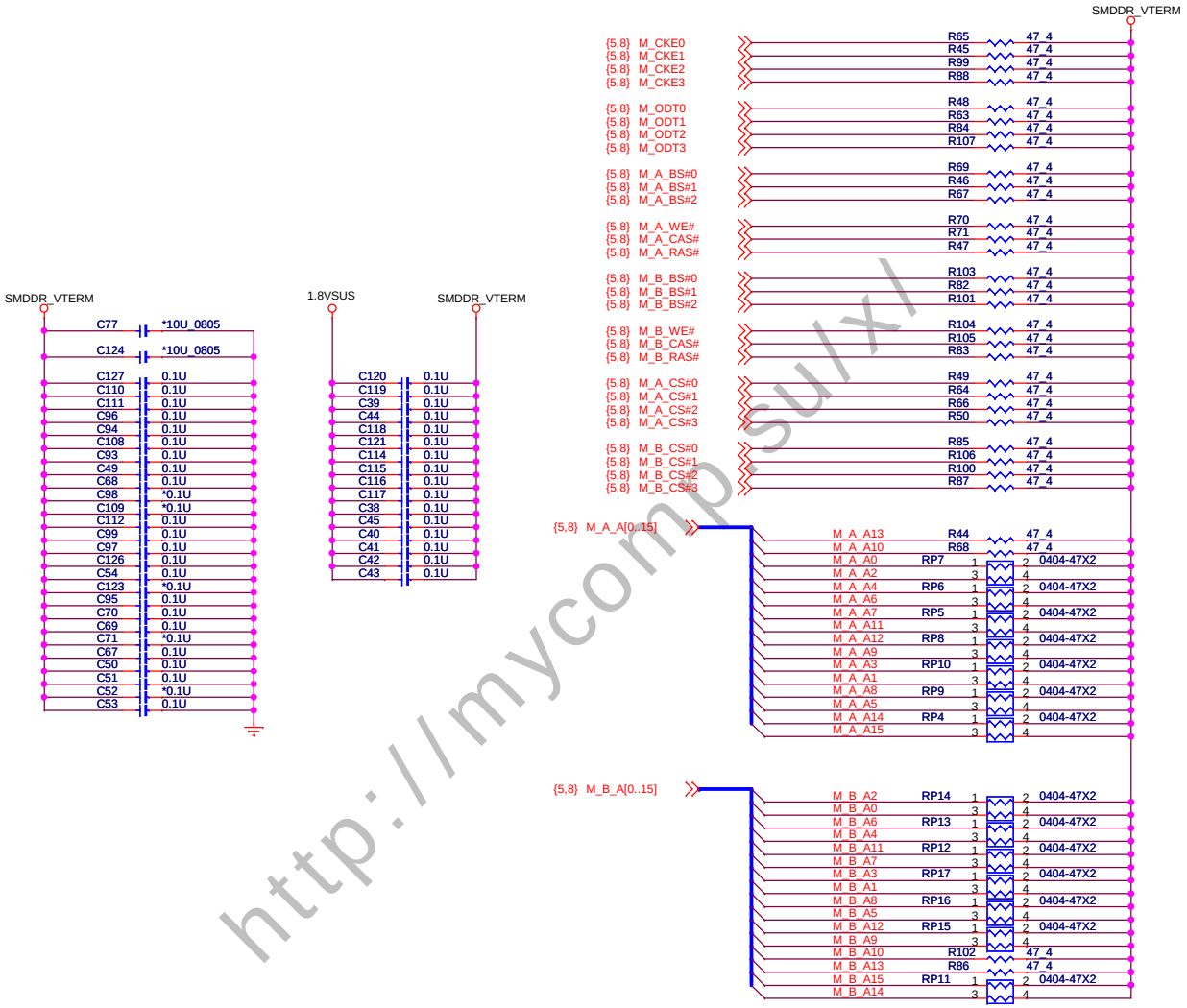
Quanta Computer Inc.

PROJECT : QU1T

Size	Document Number	Rev
	AMD M2+ PWR & GND	B
Date: Tuesday, September 01, 2009	Sheet 7 of 44	



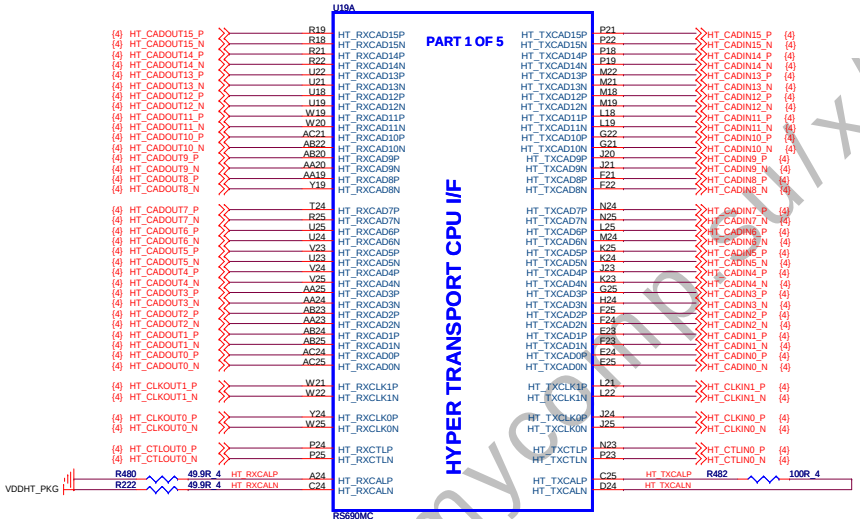
1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.



Quanta Computer Inc.

PROJECT : QU1T

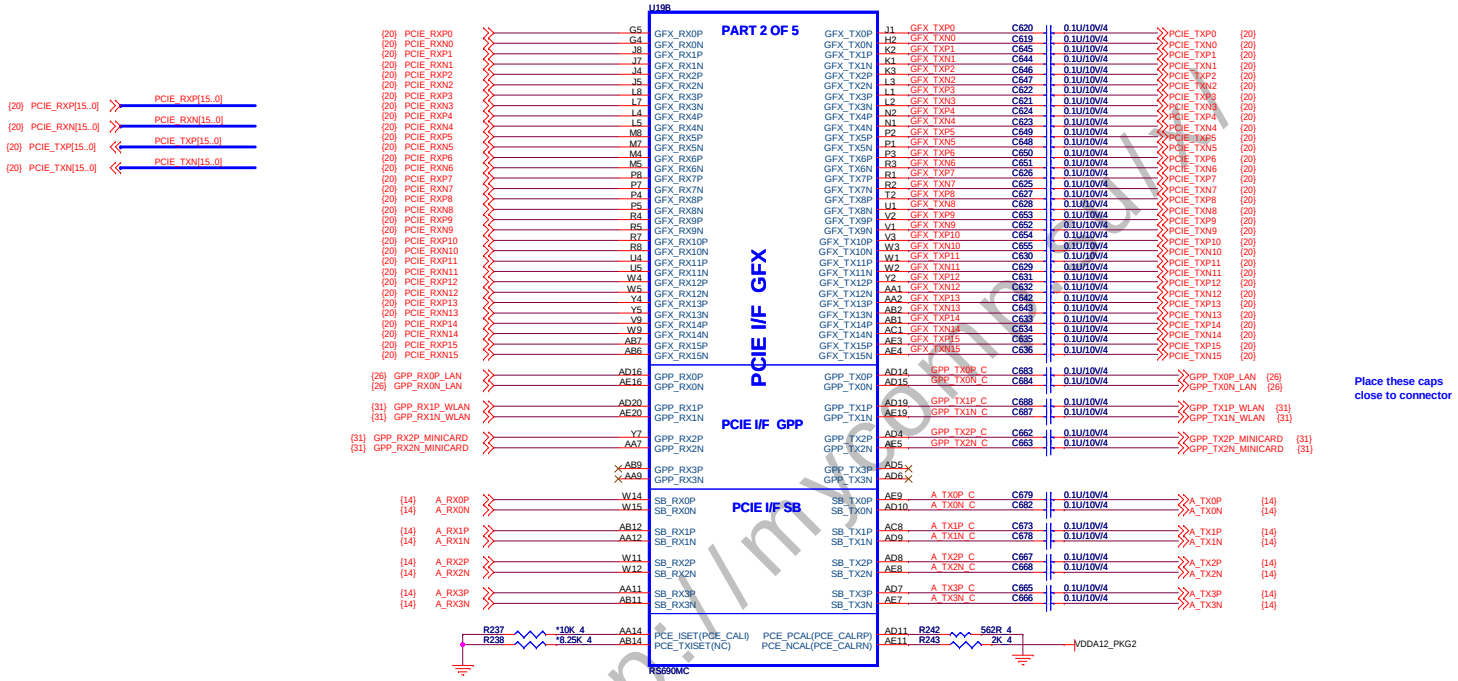
Size	Document Number	Rev
	DDRII TERMINATION	B
Date: Tuesday, September 01, 2009	Sheet 9 of 44	



Quanta Computer Inc.
PROJECT : QU1T

Size	Document Number	Rev
	RS690MC HT LINK I/F	B

Date: Tuesday, September 01, 2009 Sheet 10 of 44



Quanta Computer Inc.		
PROJECT : QU1T		
Size	Document Number: RS690MC PCIE LINK I/F	Rev: B
Date: Wednesday, November 25, 2009	Sheet 11 of 44	

HTPVDD==>2.98mA(min)/3.03mA(MAX)

VCC1.8 — L24 220ohm_2A — HTPVDD — C313 *10U/6.3V/6 — C311 2.2U/10V/6

PLLVDD==>3.54mA(min)/3.61mA(MAX)

VCC1.8 — L64 220ohm_2A — PLLVDD — C670 *10U/6.3V/6 — C669 2.2U/10V/6

AVDDQ==>0.1mA(min)/0.11mA(MAX)

VCC1.8 — L70 220ohm_2A — AVDDQ — C694 *10U/6.3V/6 — C693 2.2U/10V/6

AVDD_NB==>5.42mA(min)/5.44mA(MAX)

VCC3 — L26 22ohm,1500mA — AVDD_NB — C321 2.2U/10V/6 — C323 *0.1U/25V/4

VCC1.8 — R473 0R_6 — AVDDI — C689 2.2U/10V/6

AVDDI==>0mA(min)/0mA(MAX)

VCC1.8 — R260 10K_4 — VCC3 — R259 10K_4

{6,14} LDT_STOP# — Q21 MMBT3904 — LDT_STOP#_NB

PLLVDD12 — C671 2.2U/10V/6

3VPCU — C318 0.1U/25V/4 — C319 *0.1U/25V/4

U7 ADM1032ARMZ-2R MSOP8-4_9-65

THERM_NB_VCC — VCC — SMCLK — THMCLK {6}

C325 2200P/50V/4 — NB_THERMDA — DXP — SMDATA — THMDAT {6}

NB_THERMDC — DXN — -ALT — THERM_ALERT# {6,21,32}

{6} SYS_SHDN#1 — -OVT — GND

VCC3 — R689 10K_4

VCC3 — R468 *10K_4 STRP_DATA

R465 10K_4 TV_SWITCH

U19C RS690MC

PART 3 OF 5

CRT/TVOUT: AVDD_NB, AVDDI, AVDDQ, C692 *0.1U/25V/4, AVDD1, AVDD2, AVSSN1, AVSSN2, AVDDDI, AVSSDI, AVDDQ, AVSSQ, C, Y, COMP, RED, GREEN, BLUE, DACVSYNC, DACHSYNC, RSET, DACSCL, DACSDA

CLOCKs: R474 715R_4, PLLVDD, PLLVDD18, PLLVSS, HTPVDD, HTPVSS, VDDA12, L65 60ohm,500mA, PLLVDD12, TV_SWITCH, TVCLKIN, OSCIN, OSCOUT(PLLVDD12), GFX_CLKP, GFX_CLKN, SB_CLKP, SB_CLKN

RUN PWR: {14} NB_RST#, {19,33} NB_PWRGD, LDT_STOP# NB, {14} ALLOW_LDTSTOP, R219 10K_4, {3} HTREFCLK, SYSRESET#, POWERGOOD, LDTSTOP#, ALLOW_LDTSTOP, HTTSTCLK, HTREFCLK

MIS.: {3} NB_OSC, {3} NBSRC_CLKP, {3} NBSRC_CLKN, {3} SBLINK_CLKP, {3} SBLINK_CLKN, R250 *3K_4, R256 *3K_4 DFT_GPIO0, LOAD_ROM#, R471 *3K_4 DFT_GPIO2, R253 *3K_4 DFT_GPIO3, R469 *3K_4 DFT_GPIO4, R470 *3K_4 DFT_GPIO5, DFT_GPIO0, DFT_GPIO1, DFT_GPIO2, DFT_GPIO3, DFT_GPIO4, DFT_GPIO5, R467 *0R_4, {14} BMREQ#, {19} NB_LVDS_CLK, {19} NB_LVDS_DAT, {23} NB_THERMDA, {23} NB_THERMDC, BMREQ#, I2C_CLK, I2C_DATA, THERMALDIODE_P, THERMALDIODE_N, TMDS_HPD, DDC_DATA, TESTMODE, STRP_DATA, {41} STRP_DATA, R261 4.7K_4

LVDS: TXOUT_L0P..L3P, TXOUT_L0N..L3N, TXOUT_U0P..U3P, TXOUT_U0N..U3N, TXCLK_LP, TXCLK_LN, TXCLK_UP, TXCLK_UN, LVDS_DIGON, LVDS_BLON, LVDS_BLEN

DEBUG: DEBUG_6 T110, DEBUG_9 T107, DEBUG_10 T104, DEBUG_15 T136, DEBUG_0 T112, DEBUG_2 T109, DEBUG_1 T113, DEBUG_14 T108, DEBUG_13 T105

LPVDD==>4.86mA(min)/4.9mA(MAX)

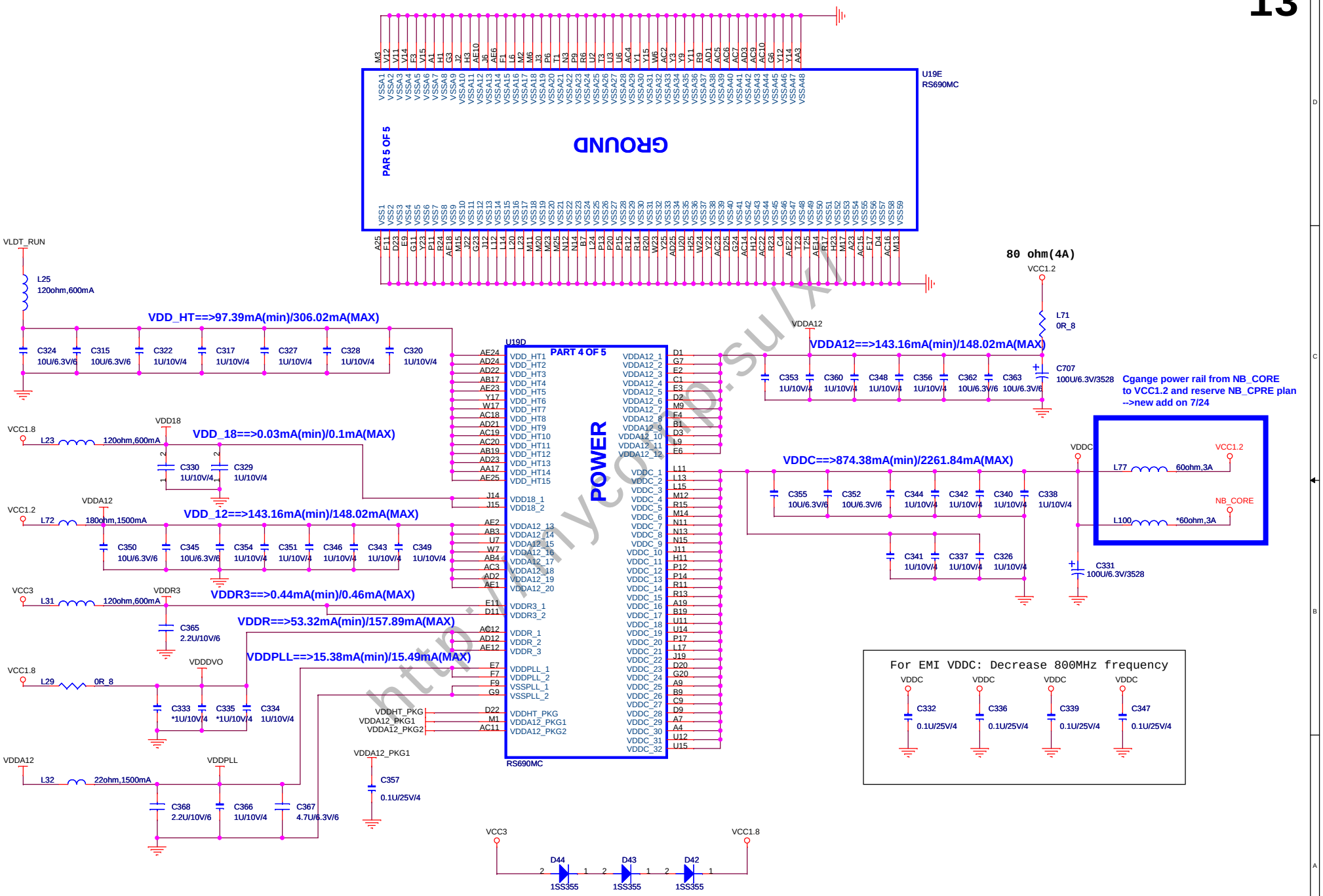
LVDDR18D==>40.2mA(min)/43.84mA(MAX)

LVDDR33==>76.77mA(min)/78.64mA(MAX)

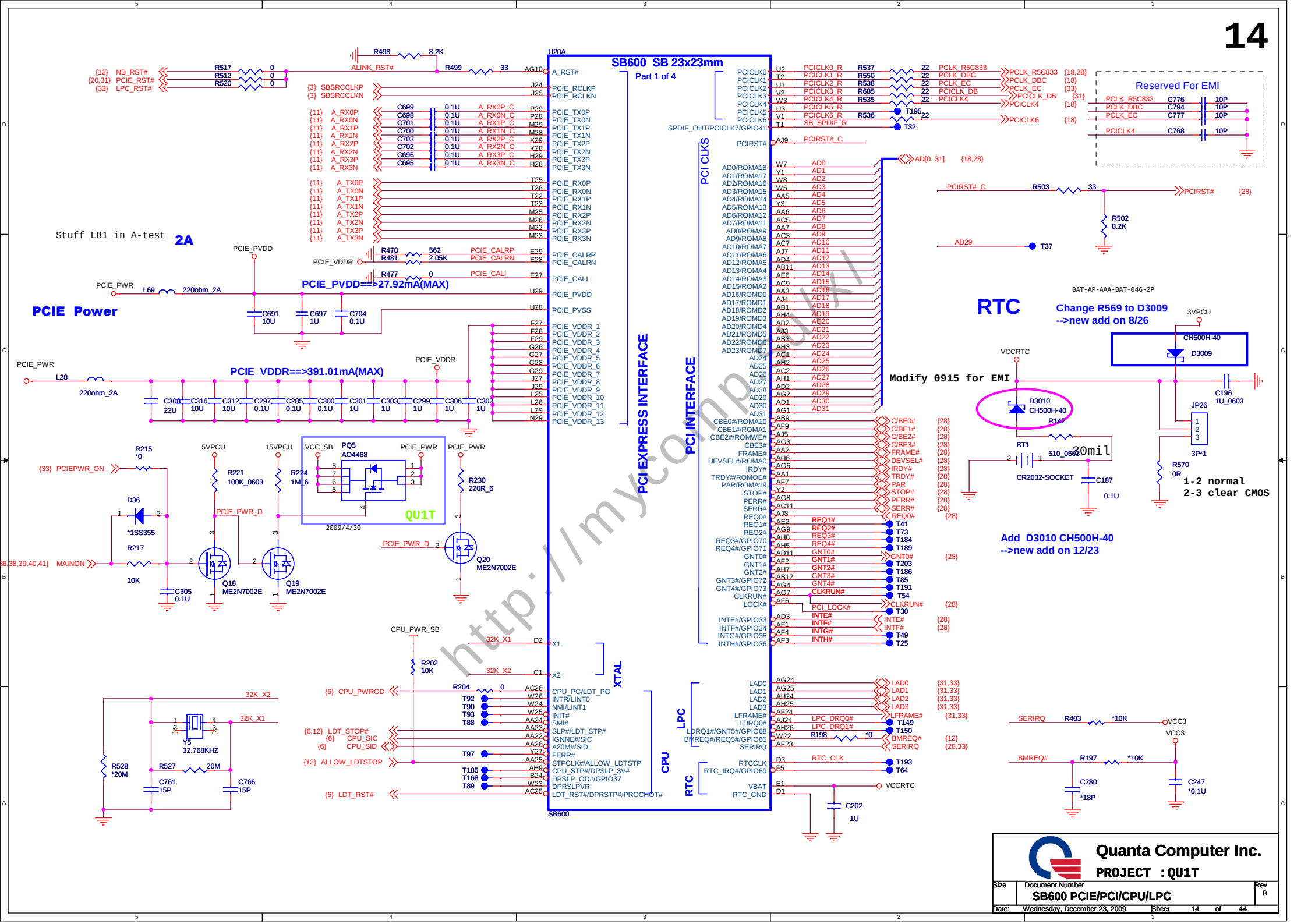
LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

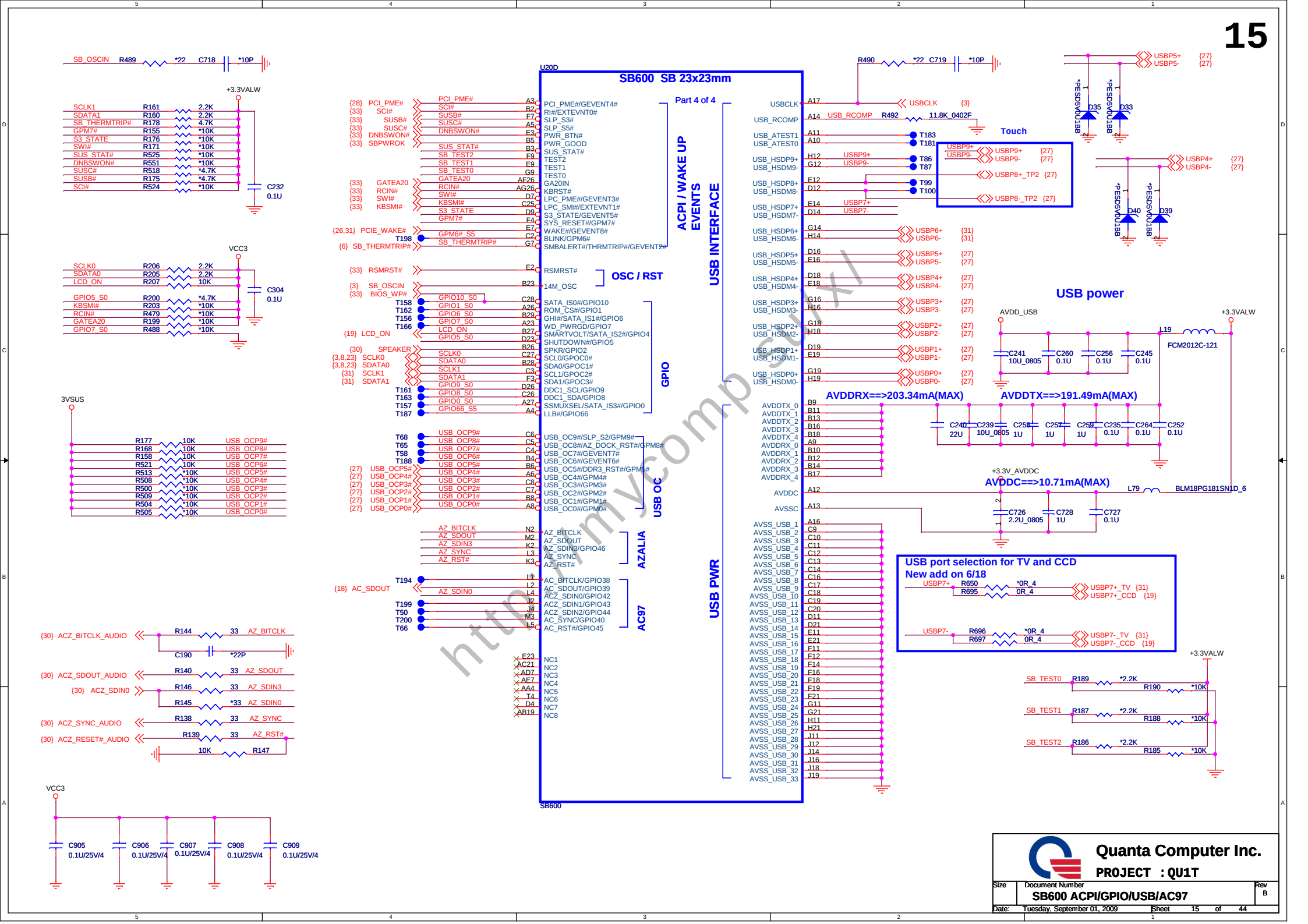
Quanta Computer Inc.
PROJECT : QU1T
Size | Document Number: RS690MC PLL & VEDIO I/F | Rev B
Date: Tuesday, September 01, 2009 | Sheet 12 of 44

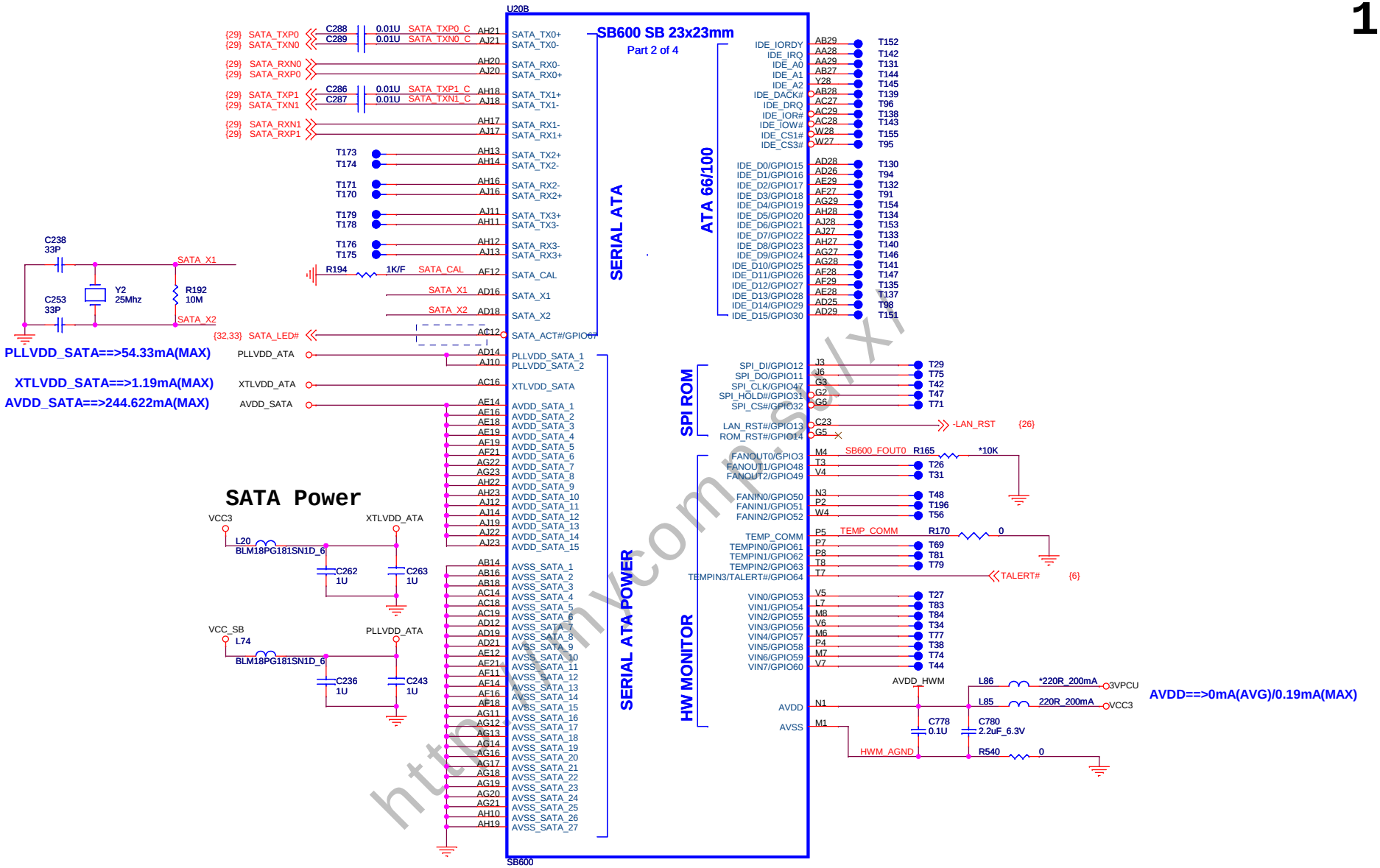


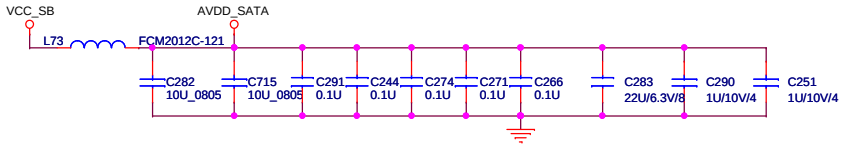
Quanta Computer Inc.			
PROJECT : QU1T			
Size	Document Number		Rev
	RS690MC POWER		B
Date: Tuesday, September 01, 2009	Sheet 13 of 44		



Quanta Computer Inc.	
PROJECT : QU1T	
Size	Document Number: SB600 PCIE/PCI/CPU/LPC
Rev	B
Date: Wednesday, December 23, 2009	Sheet 14 of 44

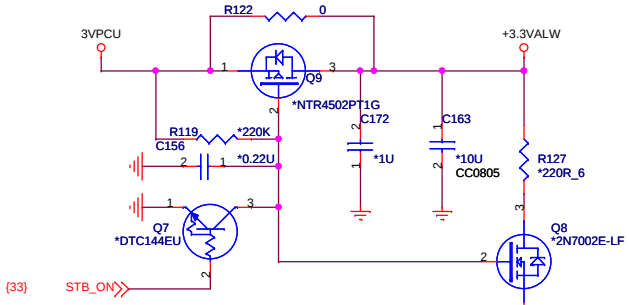

SB600 SB 23x23mm
U20D
Part 4 of 4
SB600
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
Touch
USB power
AVDDRX==>203.34mA(MAX)
AVDDTX==>191.49mA(MAX)
AVDDC==>10.71mA(MAX)
USB port selection for TV and CCD
New add on 6/18
Quanta Computer Inc.
PROJECT : QU1T
SB600 ACPI/GPIO/USB/AC97
Tuesday, September 01, 2009
http://mycomp.xxx/

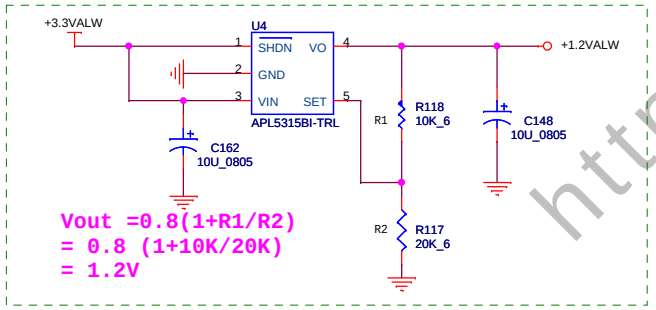


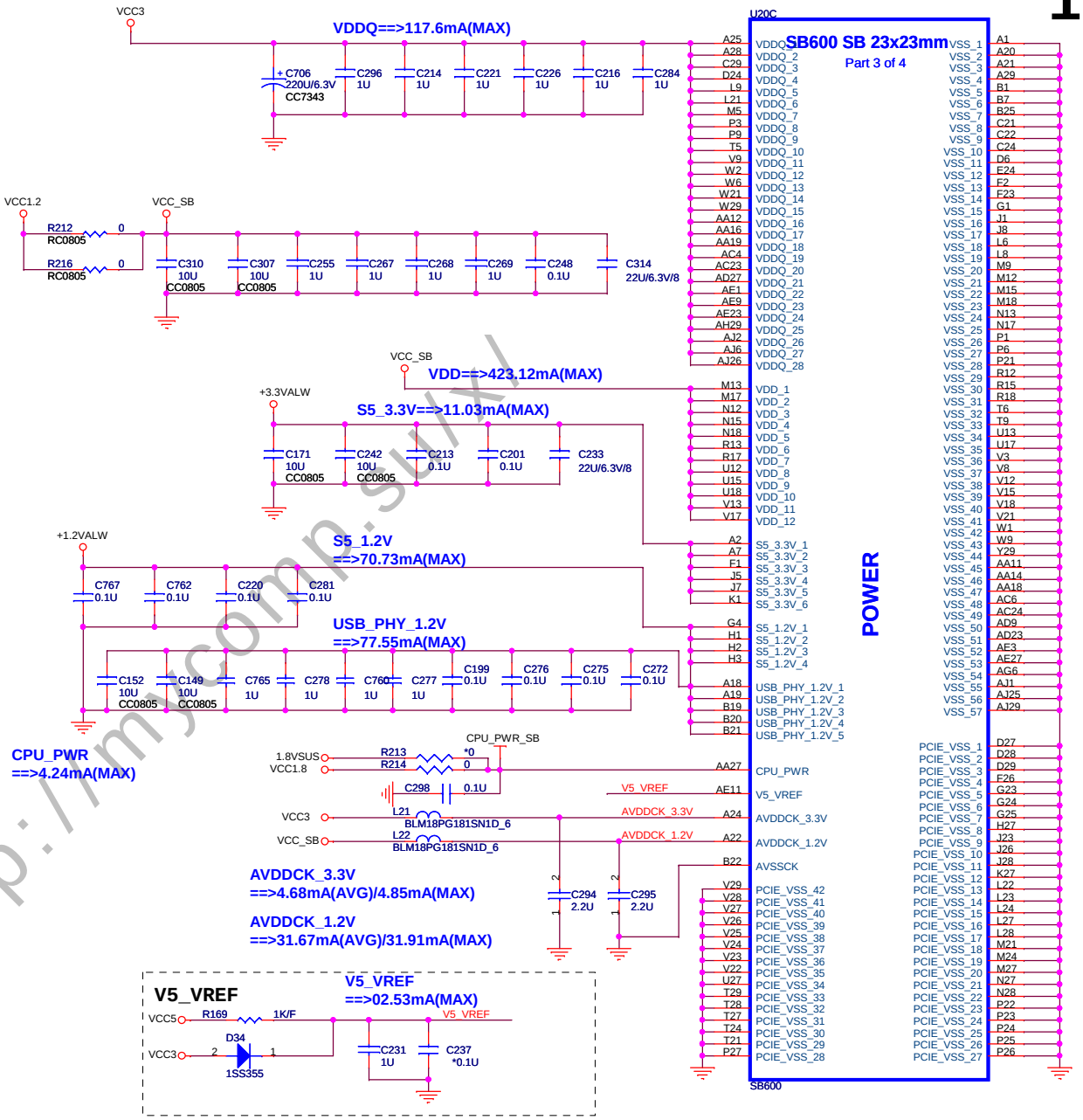


Quanta Computer Inc.			
PROJECT : QU1T			
Size	Document Number		Rev
	SB600 HDD		B
Date:	Tuesday, September 01, 2009	Sheet 16 of 44	

12/21 ADD R122 for HW Lose



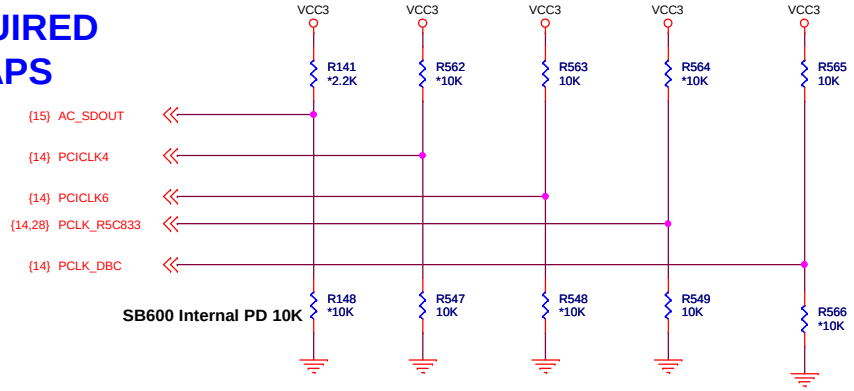




Quanta Computer Inc.
PROJECT : QU1T

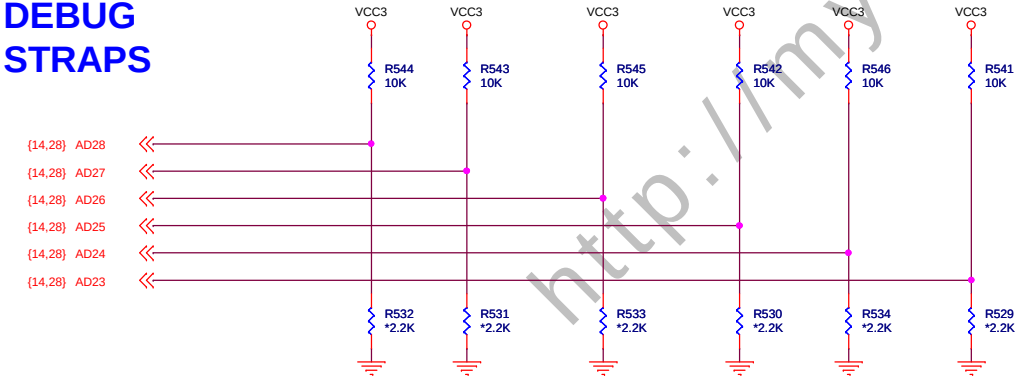
Size	Document Number	Rev
	SB600 POWER/DECOUPLING	B
Date: Thursday, December 24, 2009	Sheet 17 of 44	

REQUIRED STRAPS



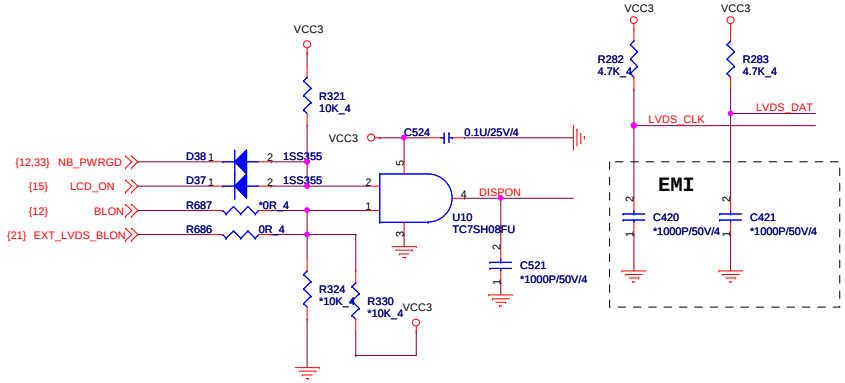
	AC_SDOUT	PCICLK4	PCICLK6	PCLK_R5C843 PCI_CLK0	PCLK_DBC PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

DEBUG STRAPS

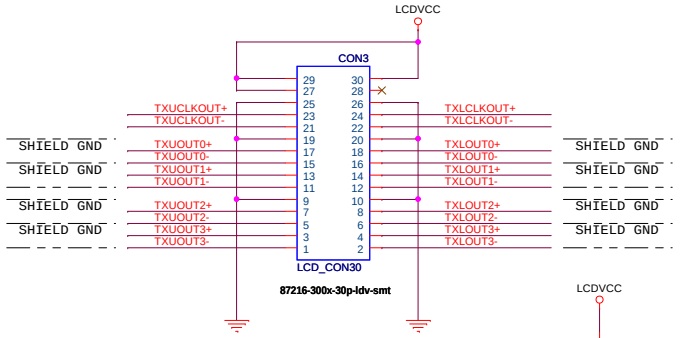


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

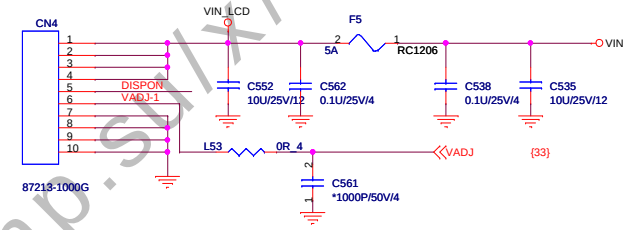
BACKLIGHT CONTROL



LCD CONNECTOR

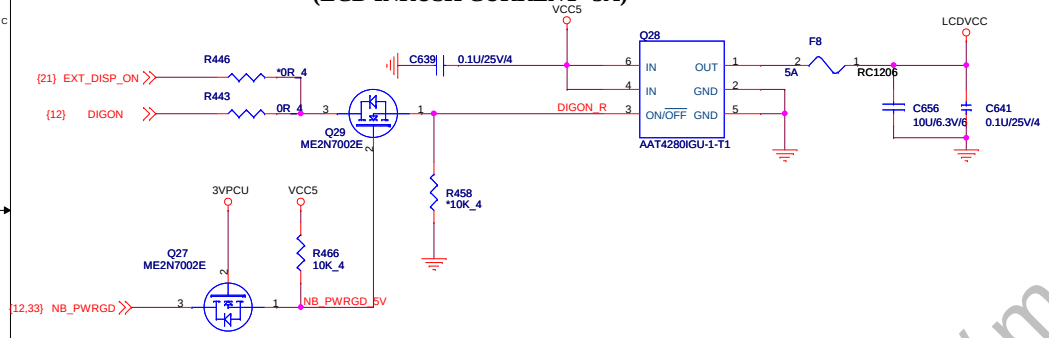


TO INVERTER POWER

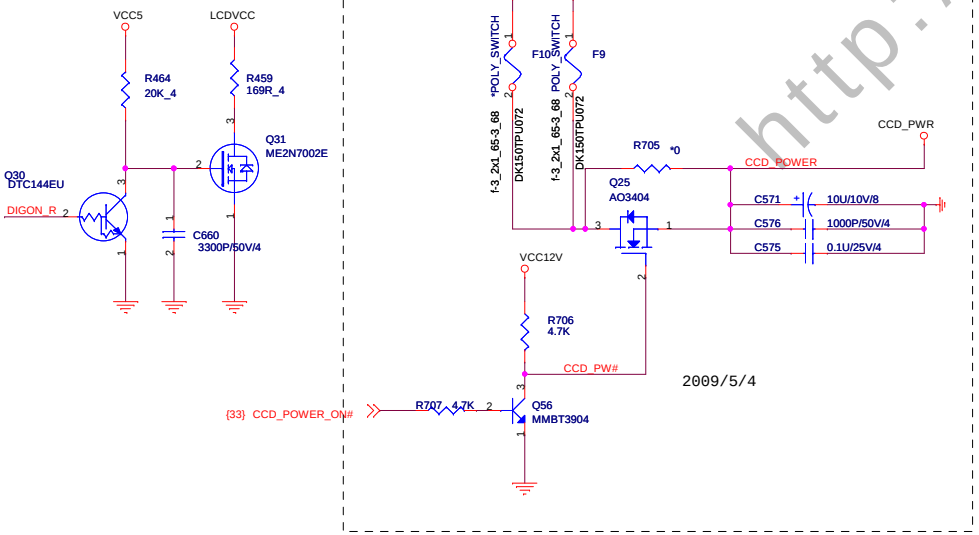


PANEL VCC CONTROL

(LCD INRUSH CURRENT=3A)

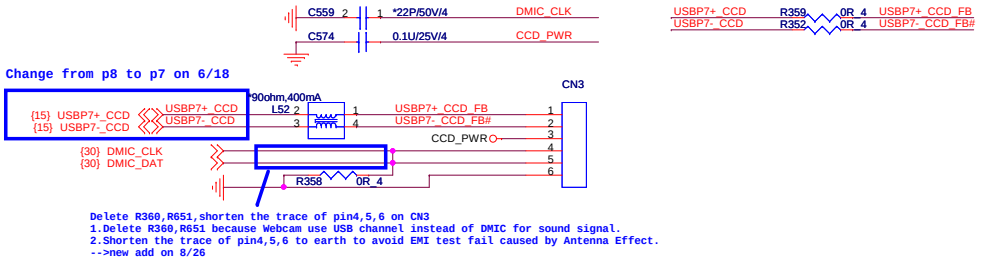


CAMERA POWER



WEB CAM MODULE

FOR EMI



Delete R360,R651,shorten the trace of pin4,5,6 on CN3
1.Delete R360,R651 because Webcam use USB channel instead of DMIC for sound signal.
2.Shorten the trace of pin4,5,6 to earth to avoid EMI test fail caused by Antenna Effect.
-->new add on 8/26

Quanta Computer Inc.
PROJECT : QU1T

Size	Document Number	Rev
	LCD PANEL/WEBCAM	B
Date: Friday, November 27, 2009	Sheet 19 of 44	

{11} PCIE_TXP[15..0] ← PCIE_TXP[15..0]
{11} PCIE_TXN[15..0] ← PCIE_TXN[15..0]
{11} PCIE_RXP[15..0] → PCIE_RXP[15..0]
{11} PCIE_RXN[15..0] → PCIE_RXN[15..0]

U17A
PART 1 OF 7
PCI-EXPRESS INTERFACE

PCIE_TXP15	AK33	PCIE_RX0P	PCIE_TX0P	AG31	C_PEG_RXP15	C414	0.1U/25V/4	PCIE_RXP15
PCIE_TXN15	AJ33	PCIE_RX0N	PCIE_TX0N	AG30	C_PEG_RXN15	C415	0.1U/25V/4	PCIE_RXN15
PCIE_TXP14	AJ35	PCIE_RX1P	PCIE_TX1P	AF31	C_PEG_RXP14	C406	0.1U/25V/4	PCIE_RXP14
PCIE_TXN14	AJ34	PCIE_RX1N	PCIE_TX1N	AF30	C_PEG_RXN14	C407	0.1U/25V/4	PCIE_RXN14
PCIE_TXP13	AH35	PCIE_RX2P	PCIE_TX2P	AF28	C_PEG_RXP13	C412	0.1U/25V/4	PCIE_RXP13
PCIE_TXN13	AH34	PCIE_RX2N	PCIE_TX2N	AF27	C_PEG_RXN13	C413	0.1U/25V/4	PCIE_RXN13
PCIE_TXP12	AG35	PCIE_RX3P	PCIE_TX3P	AD31	C_PEG_RXP12	C405	0.1U/25V/4	PCIE_RXP12
PCIE_TXN12	AG34	PCIE_RX3N	PCIE_TX3N	AD30	C_PEG_RXN12	C404	0.1U/25V/4	PCIE_RXN12
PCIE_TXP11	AF33	PCIE_RX4P	PCIE_TX4P	AD28	C_PEG_RXP11	C384	0.1U/25V/4	PCIE_RXP11
PCIE_TXN11	AF33	PCIE_RX4N	PCIE_TX4N	AD27	C_PEG_RXN11	C385	0.1U/25V/4	PCIE_RXN11
PCIE_TXP10	AE35	PCIE_RX5P	PCIE_TX5P	AB31	C_PEG_RXP10	C383	0.1U/25V/4	PCIE_RXP10
PCIE_TXN10	AE34	PCIE_RX5N	PCIE_TX5N	AB30	C_PEG_RXN10	C382	0.1U/25V/4	PCIE_RXN10
PCIE_TXP9	AD35	PCIE_RX6P	PCIE_TX6P	AB28	C_PEG_RXP9	C403	0.1U/25V/4	PCIE_RXP9
PCIE_TXN9	AD34	PCIE_RX6N	PCIE_TX6N	AB27	C_PEG_RXN9	C402	0.1U/25V/4	PCIE_RXN9
PCIE_TXP8	AC35	PCIE_RX7P	PCIE_TX7P	AA31	C_PEG_RXP8	C386	0.1U/25V/4	PCIE_RXP8
PCIE_TXN8	AC34	PCIE_RX7N	PCIE_TX7N	AA30	C_PEG_RXN8	C387	0.1U/25V/4	PCIE_RXN8
PCIE_TXP7	AB33	PCIE_RX8P	PCIE_TX8P	AA28	C_PEG_RXP7	C409	0.1U/25V/4	PCIE_RXP7
PCIE_TXN7	AA33	PCIE_RX8N	PCIE_TX8N	AA27	C_PEG_RXN7	C410	0.1U/25V/4	PCIE_RXN7
PCIE_TXP6	AA35	PCIE_RX9P	PCIE_TX9P	W31	C_PEG_RXP6	C389	0.1U/25V/4	PCIE_RXP6
PCIE_TXN6	AA34	PCIE_RX9N	PCIE_TX9N	W30	C_PEG_RXN6	C388	0.1U/25V/4	PCIE_RXN6
PCIE_TXP5	Y35	PCIE_RX10P	PCIE_TX10P	W28	C_PEG_RXP5	C400	0.1U/25V/4	PCIE_RXP5
PCIE_TXN5	Y34	PCIE_RX10N	PCIE_TX10N	W27	C_PEG_RXN5	C401	0.1U/25V/4	PCIE_RXN5
PCIE_TXP4	W35	PCIE_RX11P	PCIE_TX11P	V31	C_PEG_RXP4	C398	0.1U/25V/4	PCIE_RXP4
PCIE_TXN4	W34	PCIE_RX11N	PCIE_TX11N	V30	C_PEG_RXN4	C399	0.1U/25V/4	PCIE_RXN4
PCIE_TXP3	V33	PCIE_RX12P	PCIE_TX12P	V28	C_PEG_RXP3	C391	0.1U/25V/4	PCIE_RXP3
PCIE_TXN3	U33	PCIE_RX12N	PCIE_TX12N	V27	C_PEG_RXN3	C390	0.1U/25V/4	PCIE_RXN3
PCIE_TXP2	U35	PCIE_RX13P	PCIE_TX13P	U31	C_PEG_RXP2	C397	0.1U/25V/4	PCIE_RXP2
PCIE_TXN2	U34	PCIE_RX13N	PCIE_TX13N	U30	C_PEG_RXN2	C396	0.1U/25V/4	PCIE_RXN2
PCIE_TXP1	T35	PCIE_RX14P	PCIE_TX14P	U28	C_PEG_RXP1	C395	0.1U/25V/4	PCIE_RXP1
PCIE_TXN1	T34	PCIE_RX14N	PCIE_TX14N	U27	C_PEG_RXN1	C394	0.1U/25V/4	PCIE_RXN1
PCIE_TXP0	R35	PCIE_RX15P	PCIE_TX15P	R31	C_PEG_RXP0	C392	0.1U/25V/4	PCIE_RXP0
PCIE_TXN0	R34	PCIE_RX15N	PCIE_TX15N	R30	C_PEG_RXN0	C393	0.1U/25V/4	PCIE_RXN0

Clock
{3} PCIE_REFCLKP ↔ PCIE_REFCLKP (AJ31)
{3} PCIE_REFCLKN ↔ PCIE_REFCLKN (AJ30)

SM Bus
AK35 NC_SMB_DATA
AK34 NC_SMBCLK

{14,31} PCIE_RST# ↔ PCIE_RST# (AM32) PERSTB

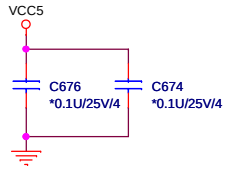
Calibration
PCIE_CALRN AG26 — R298 2K_4 — +1.1V PCIE_VDDC
PCIE_CALRP AJ27 — R296 1.27K_4

NC_DRAM_0 AF3
NC_DRAM_1 AG9
NC_AC_BATT AK29
NC_FAN_TACH AK14

M92-M+

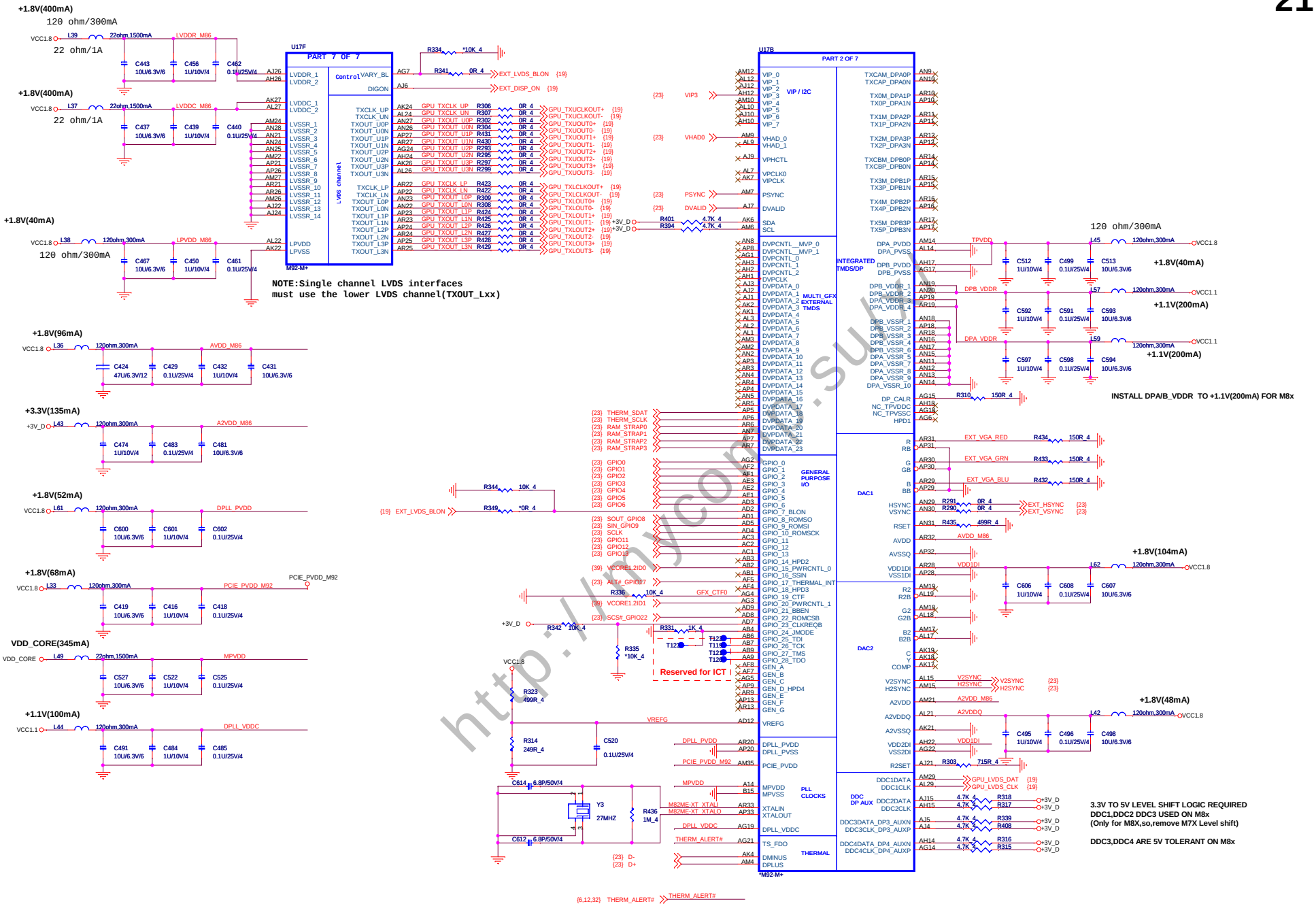
	Quantat	Lenovo
M92-M+	AJ072800T16	AJ072800T17
M82-M	AJ070700T13	AJ070700T12

EMI CAP.



Quanta Computer Inc.
PROJECT : QU1T

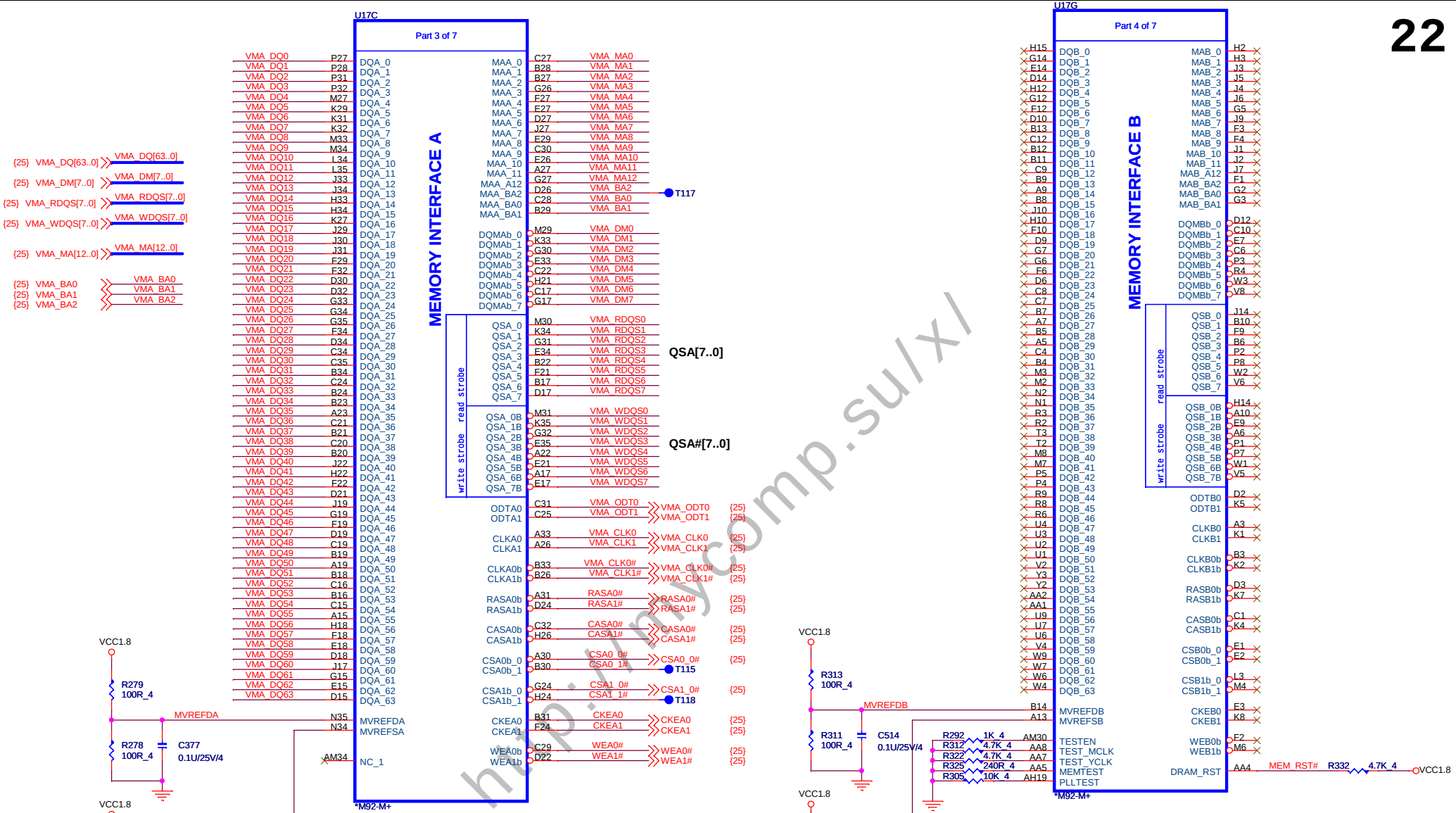
Size	Document Number	Rev
	M82-M PCI-E	B
Date: Wednesday, November 25, 2009	Sheet 20 of 44	



Quanta Computer Inc.
PROJECT : QU1T

Size	Document Number	Rev
	M82-M LVDS\RGB\TMDS	B

Date: Wednesday, November 25, 2009 Sheet 21 of 44



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V

0.5*VDDQ 0.713*VDDQ

Quanta Computer Inc.
PROJECT : QU1T

Size	Document Number	Rev
	M82-M MEMORY I/F	B
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STRAP

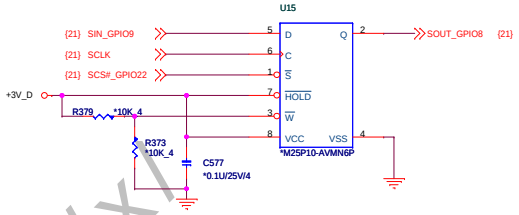
CONFIGURATION STRAPS

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE RSVD = ATI RESERVED (DO NOT INSTALL) M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M7x/M8x-M)	NA	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M82-S)	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA_DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

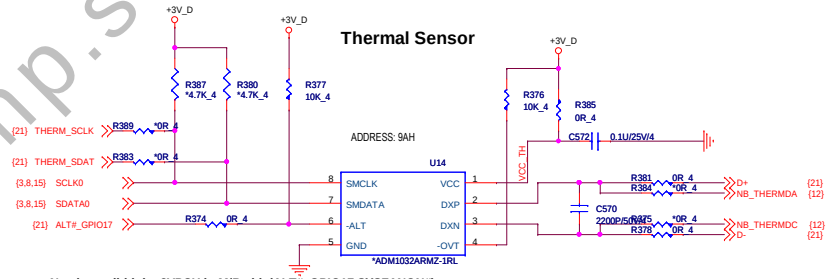
HDCP FUNCTION

W#	HDCP
0	**Enable**
1	Disable

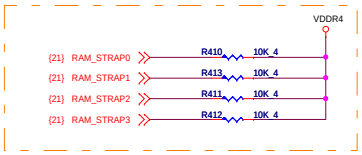
EEPROM



Thermal Sensor



Need to pull-high +3VPCU in M/B side(ALT#_GPIO17,SYSFANON#)



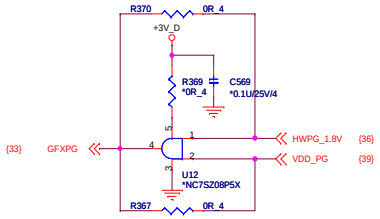
M86 DDR2 Memory Aperture size

Vendor	Size	RAM_STRAP3 DVPDATA_23	RAM_STRAP2 DVPDATA_22	RAM_STRAP1 DVPDATA_21	RAM_STRAP0 DVPDATA_20
Hynix (400MHZ)	**256M**	**1**	**1**	**1**	**1**
Samsung (400MHz)	**256M**	**1**	**1**	**1**	**0**

M82 DDR2 Memory Aperture size

Vendor	Size	RAM_STRAP3 DVPDATA_23	RAM_STRAP2 DVPDATA_22	RAM_STRAP1 DVPDATA_21	RAM_STRAP0 DVPDATA_20
Hynix (500MHZ)	**512M**	**1**	**1**	**0**	**1**
Samsung (500MHz)	**512M**	**1**	**0**	**1**	**1**

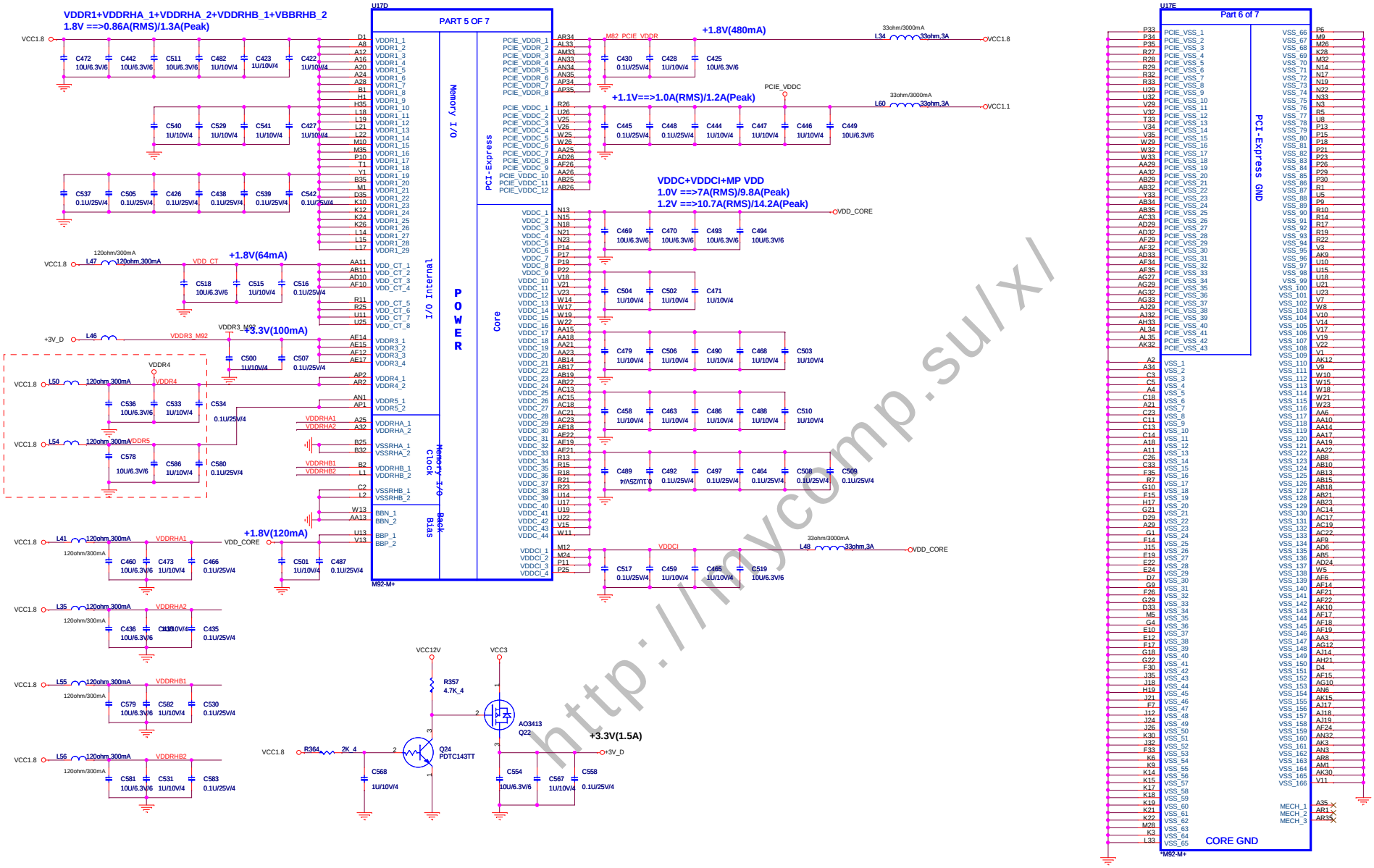
Fine-tune Power-on sequence



Quanta Computer Inc.
PROJECT : QU1T

Size	Document Number	Rev
	M82-M Thermal\Strap\EEPROM	B

Date: Wednesday, November 25, 2009 Sheet 23 of 44



Quanta Computer Inc.
PROJECT : QU1T

Size	Document Number	Rev
	M82-M Power and GND	B
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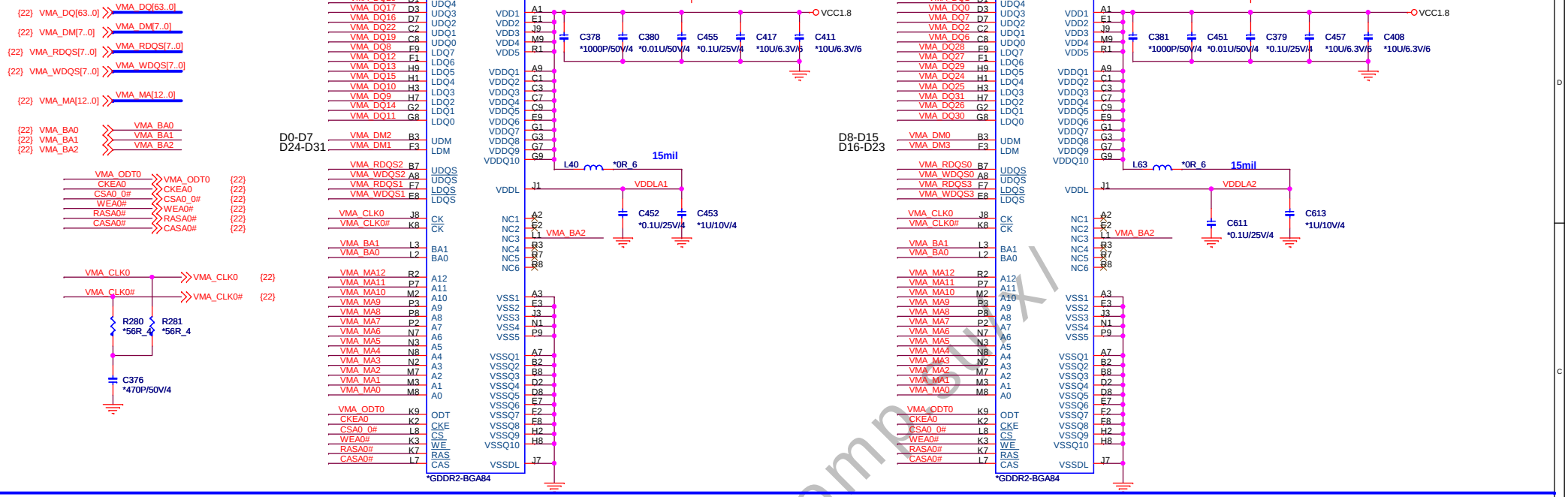
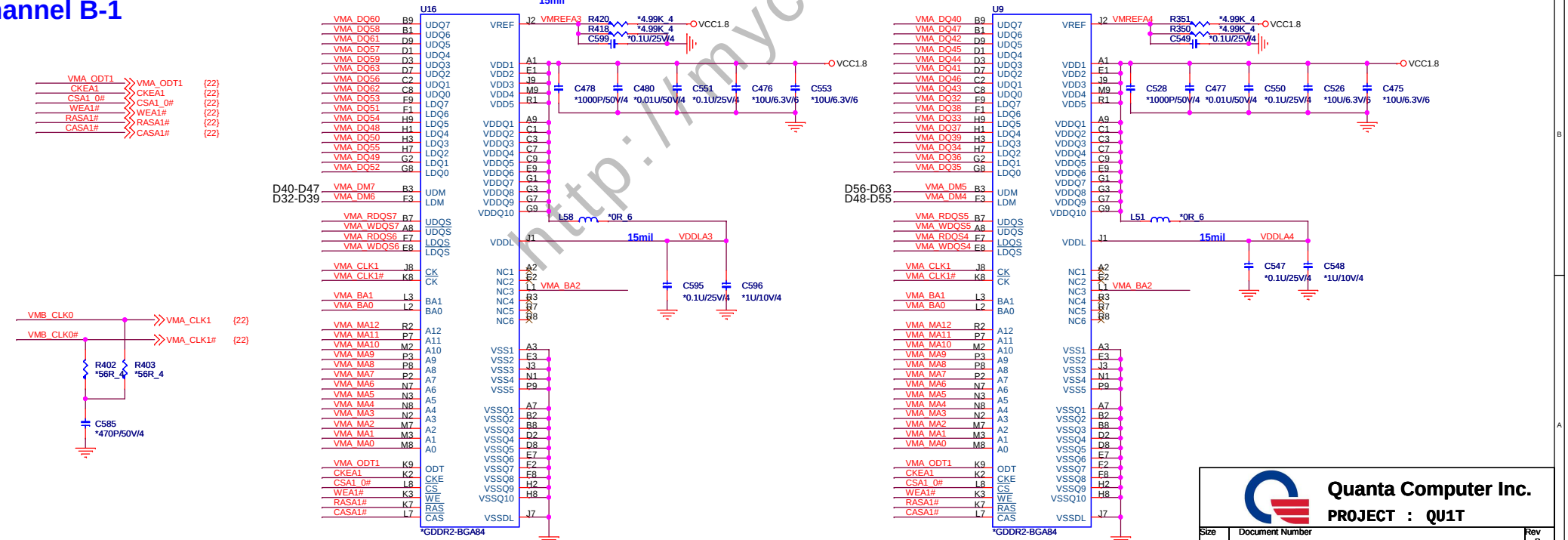
Channel A-1



Channel B-1

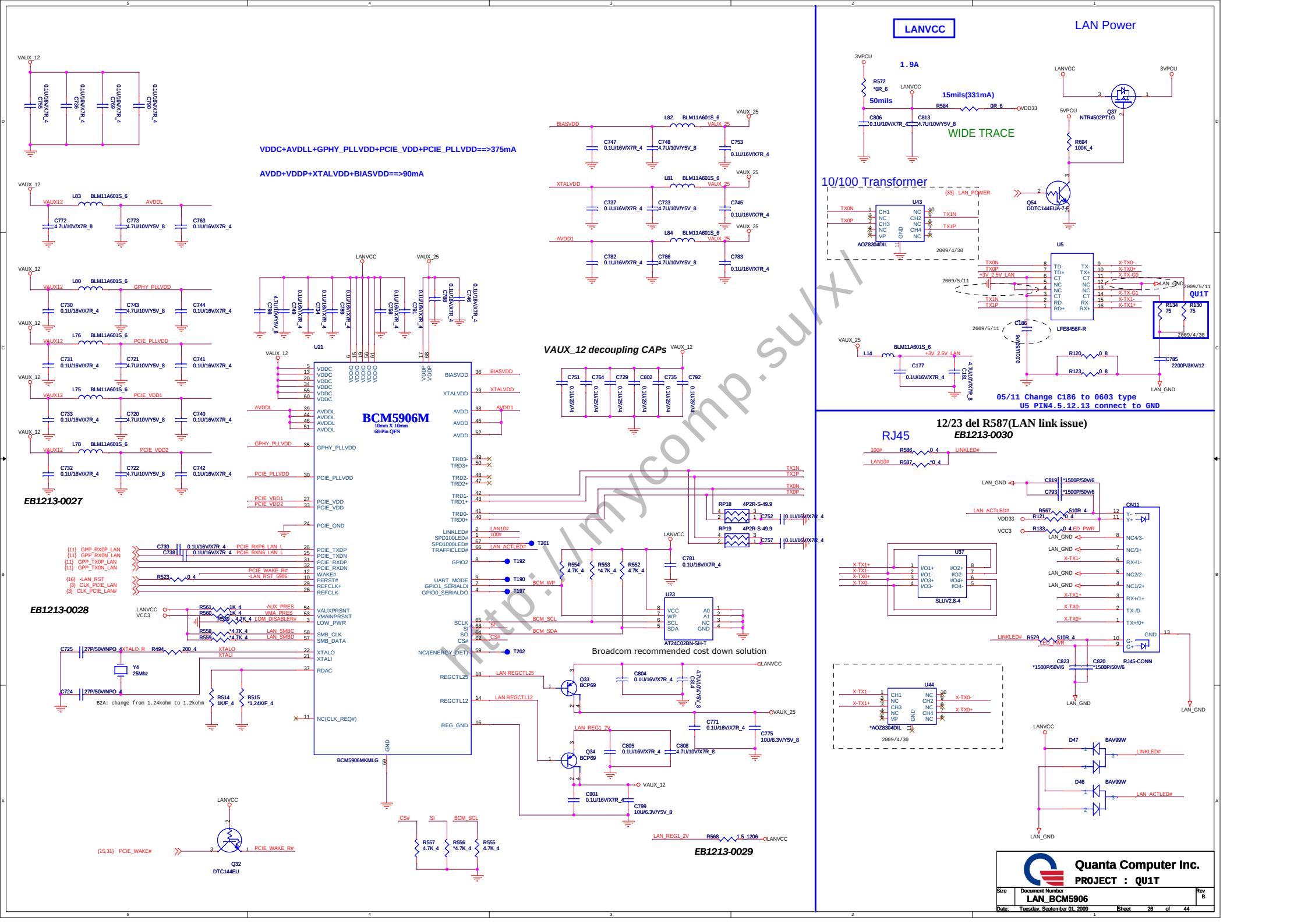


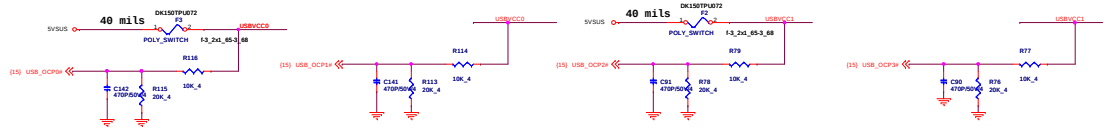
Quanta Computer Inc.

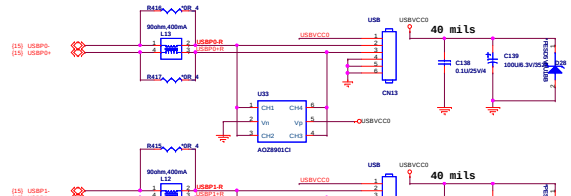
PROJECT : QU1T

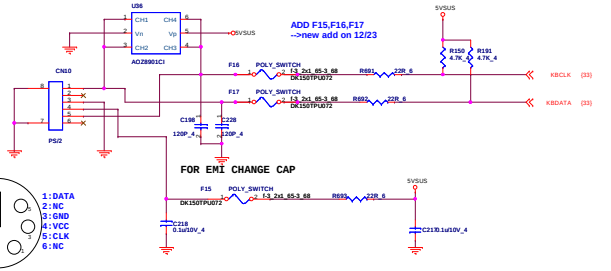
Size	Document Number	Rev
	VRAM_1 GDDR2 BGA84	B

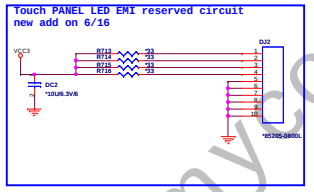
Date: Tuesday, September 01, 2009 Sheet 25 of 44

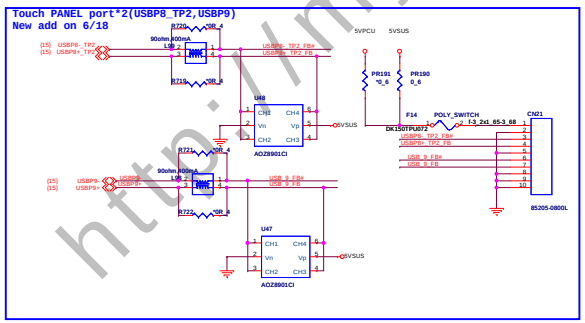


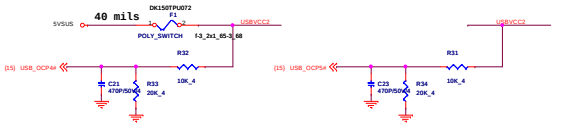


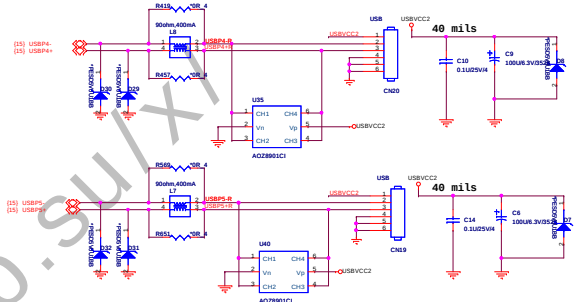


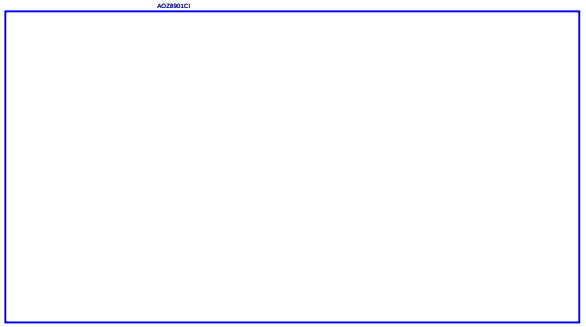












Quanta Computer Inc.			
PROJECT : QU1T			
Size	Document Number		Rev
	USB Port		B
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12/10 Change Q35 PN:BAM45020007

500mA

ES1

UDIO4=GND : MMC Controller Disable
R600 => N/A

Shield to GND

R5C837-->INTE# Pin115
R5C833-->INTF# Pin116

Note:

	SD/MMC	MS	XD
MDIO00	SD_CD#		XD-CD#
MDIO01		MS_INS	
MDIO02			
MDIO03	SD_WP#		
MDIO04	SD_PWR0		
MDIO05	SD_PWR1		
MDIO06	SD_LED#		
MDIO07	SD_EXTCK		
MDIO08	SD_CMD	MS_BS	
MDIO09	SD_CLK	MS_CLK	
MDIO10	SD_DAT0	MS_DAT0	XD_DAT0
MDIO11	SD_DAT1	MS_DAT1	XD_DAT1
MDIO12	SD_DAT2	MS_DAT2	XD_DAT2
MDIO13	SD_DAT3	MS_DAT3	XD_DAT3
MDIO14			XD_DAT4
MDIO15			XD_DAT5
MDIO16			XD_DAT6
MDIO17			XD_DAT7
MDIO18			XD_CLE
MDIO19			XD_ALE

CLOSED CHIP

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

R5C837-->Pin94,pin95,pin101,pin100 NC
R5C833-->Add 833 PLL could support 50Mhz SD

Quanta Computer Inc.
PROJECT : QU1T

Size	Document Number	Rev
	R5C833 / 1394	B
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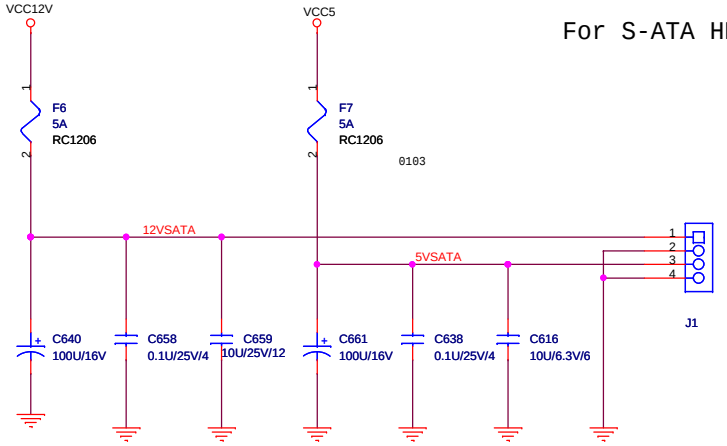
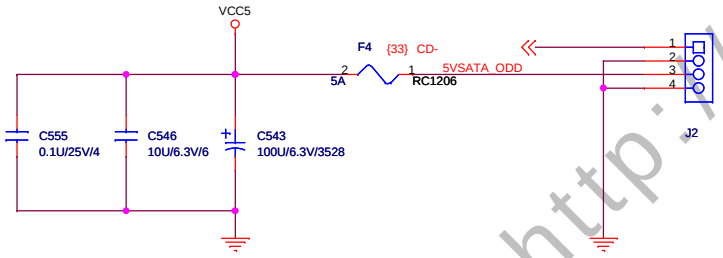
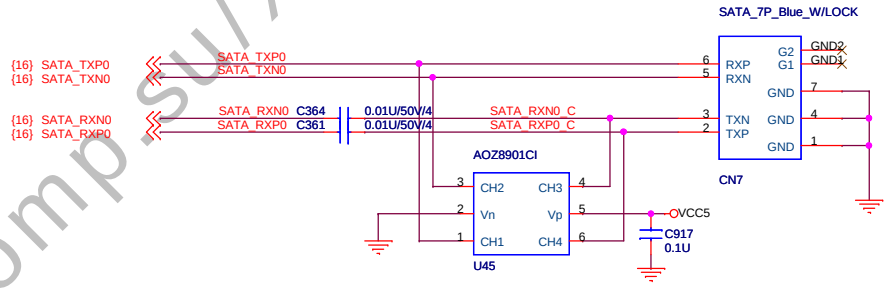
60 mils

For S-ATA HDD POWER

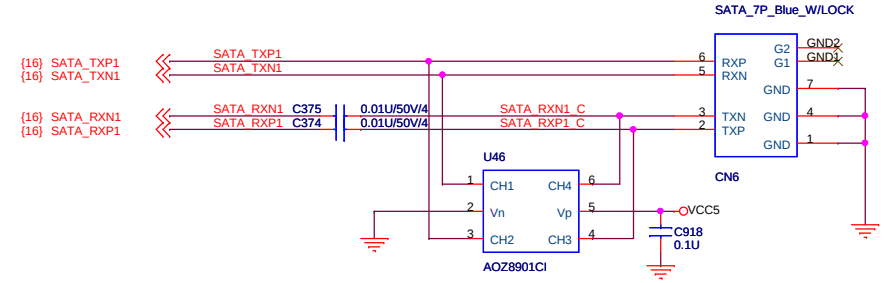




SATA HDD CONNECTOR

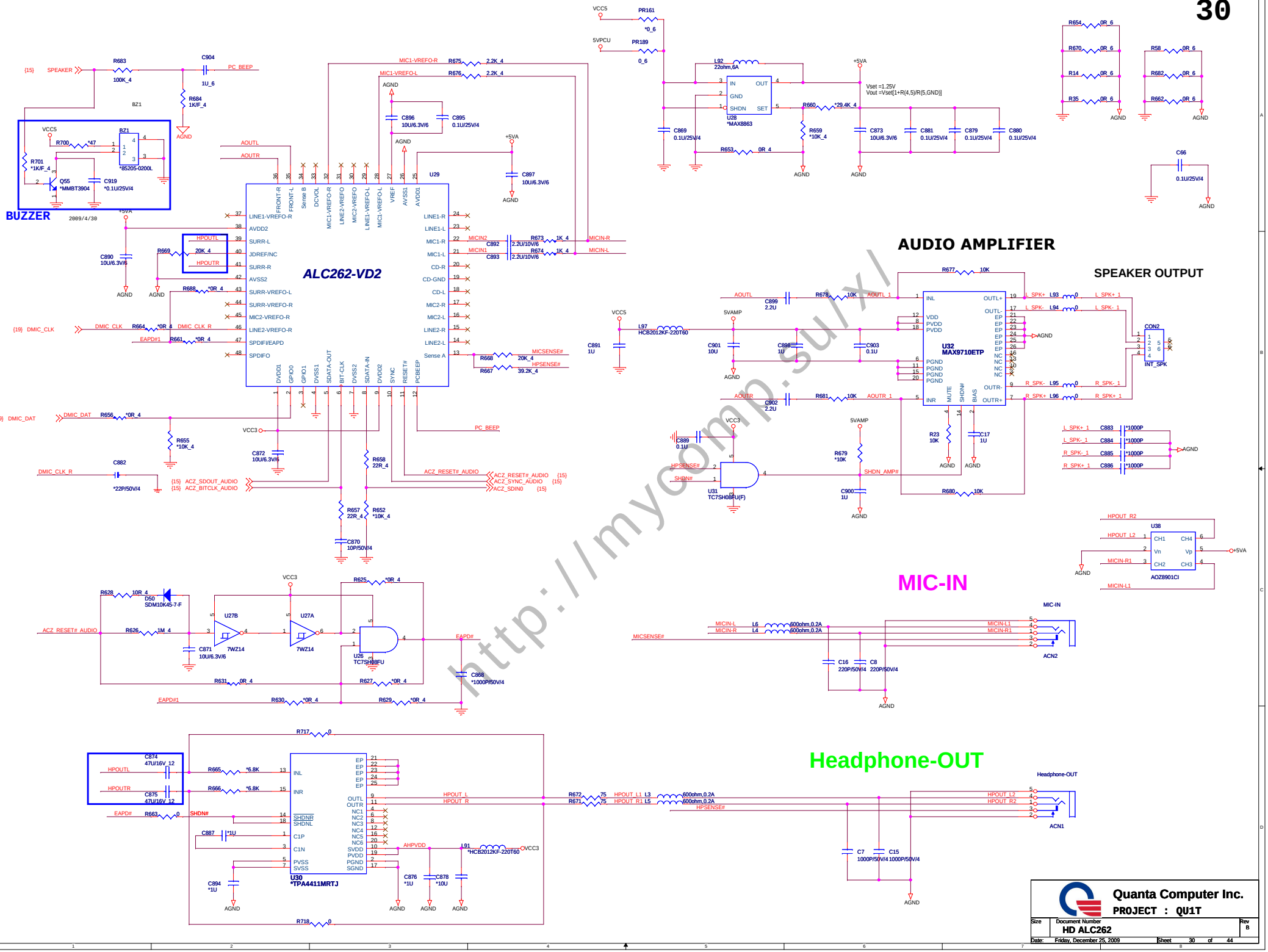


SATA ODD CONNECTOR

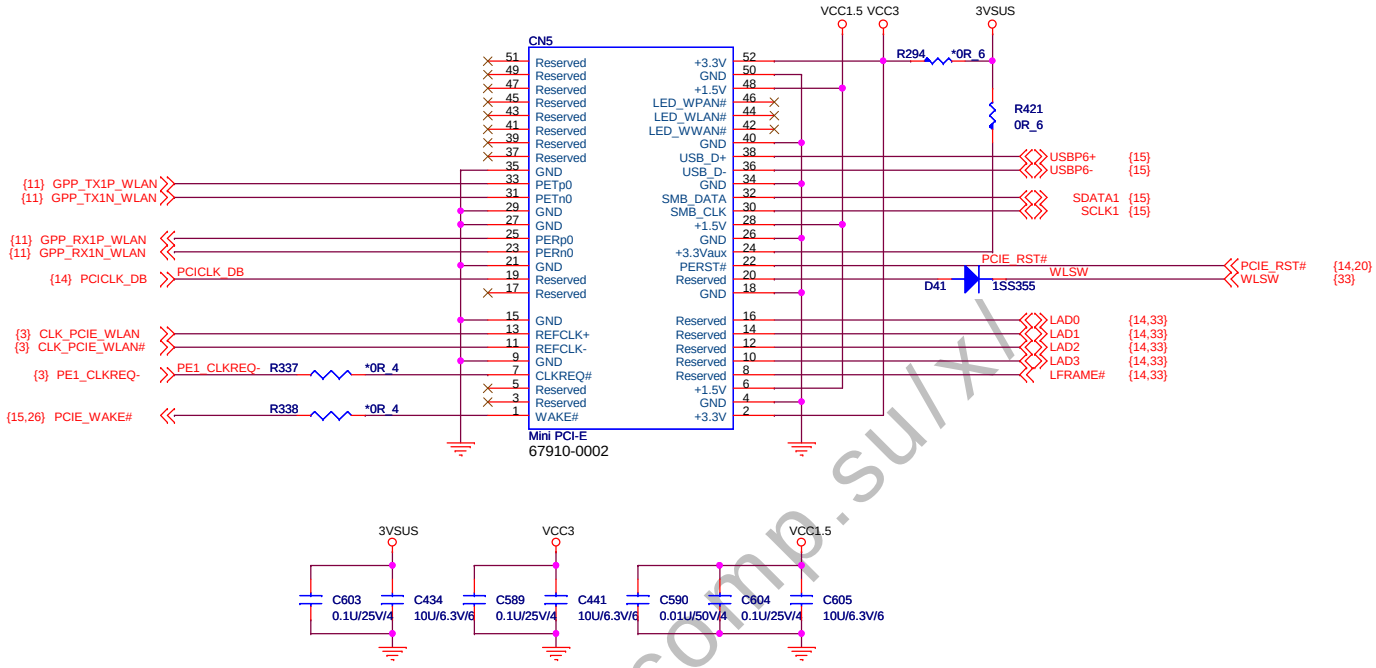


Quanta Computer Inc.
PROJECT : QU1T

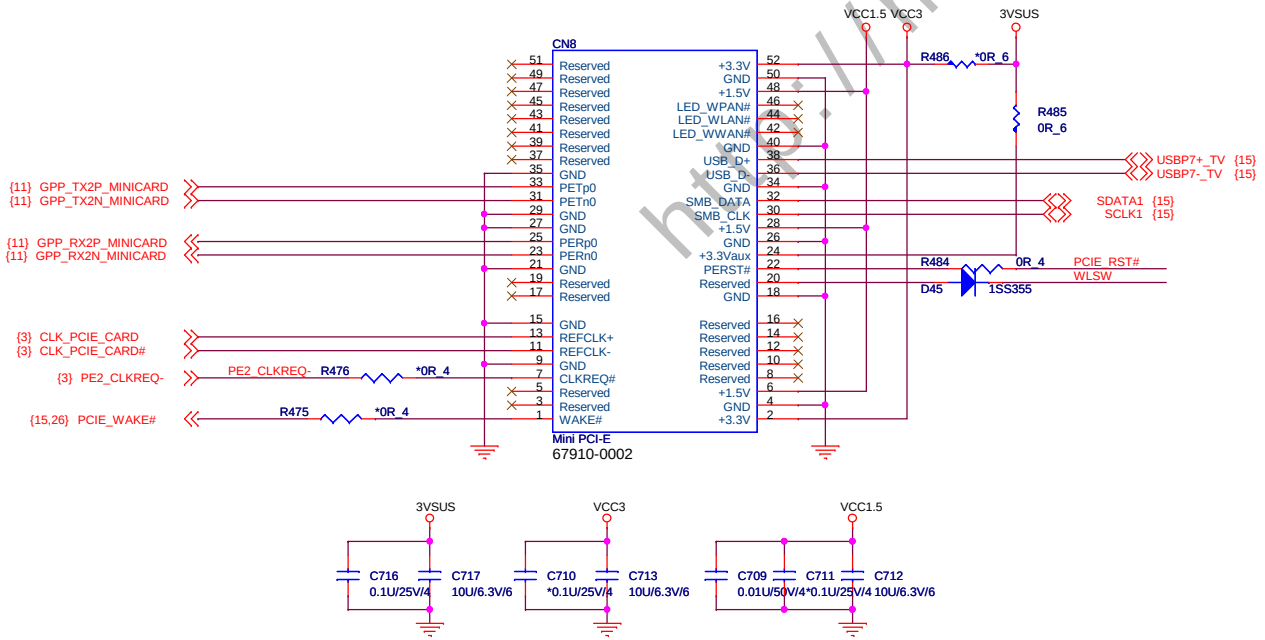
Size	Document Number	Rev
	SATA HDD/ODD	B
Date: Tuesday, September 01, 2009	Sheet 29 of 44	



Mini Card (WLAN)

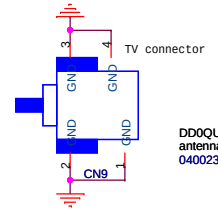


Mini Card (TV Card)



TV ANTENNA CONNECTOR

ANT. CONNECTOR



Z = 75 OHM

DD0QU1TH000
antenna-040023fs001g-4p-nb3
040023FS001G105NA

Quanta Computer Inc.		
PROJECT : QU1T		
Size	Document Number: MINI CARD	Rev: B
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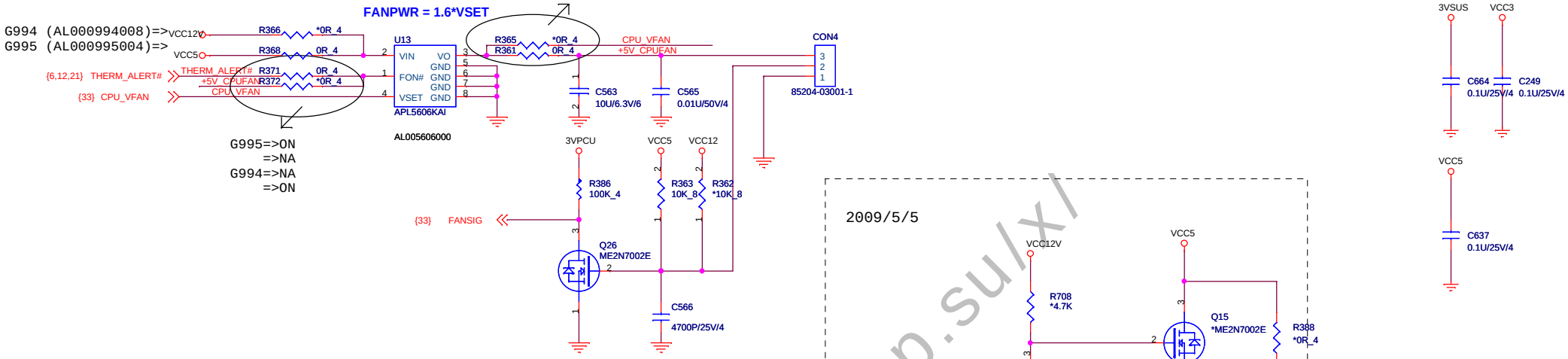
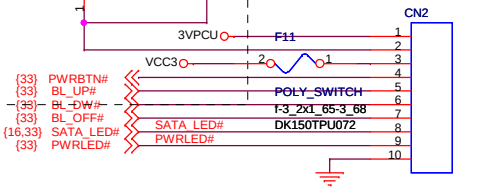
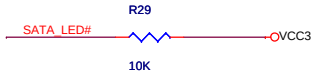
FAN CONN

G994=> ON
=> NA
G995=> NA
=> ON

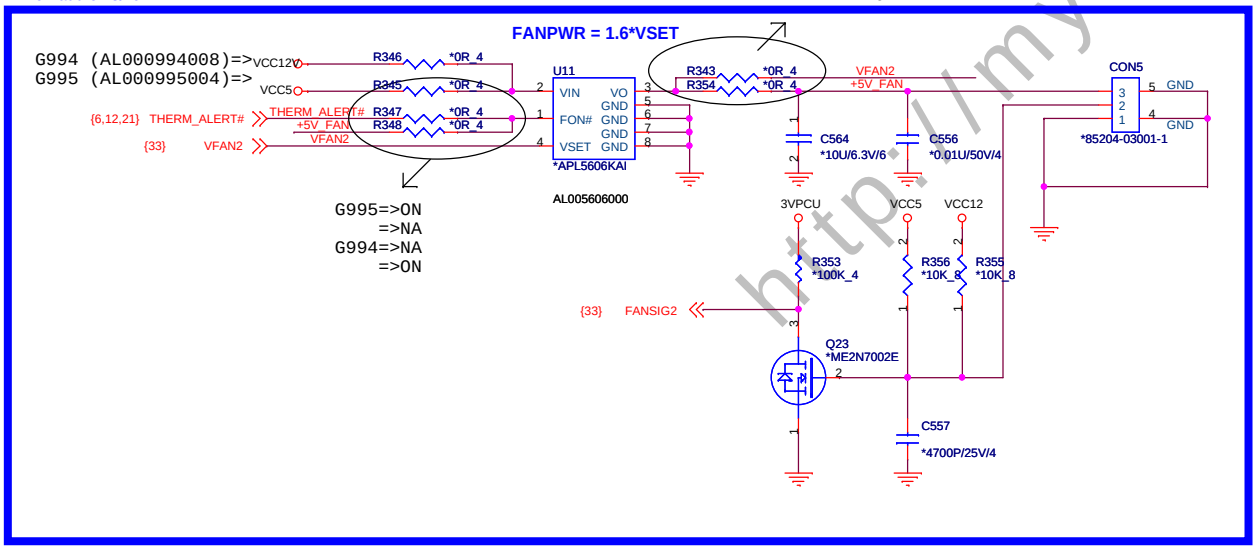






Delete fan speed control IC U11 because HDD FAN is cost down already, and also delete surrouding parts
-->new add on 8/26

G994=> ON
=> NA
G995=> NA
=> ON



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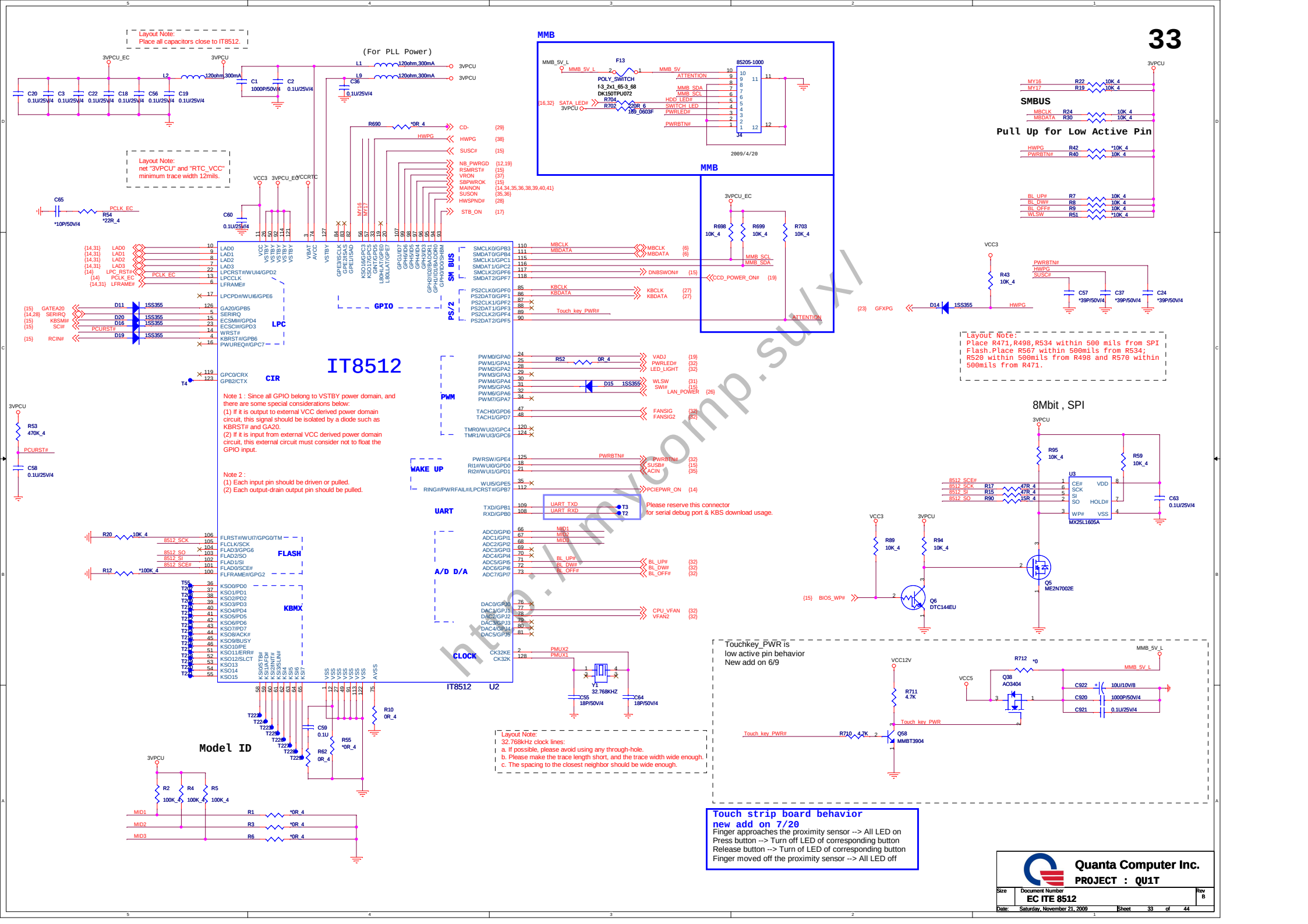
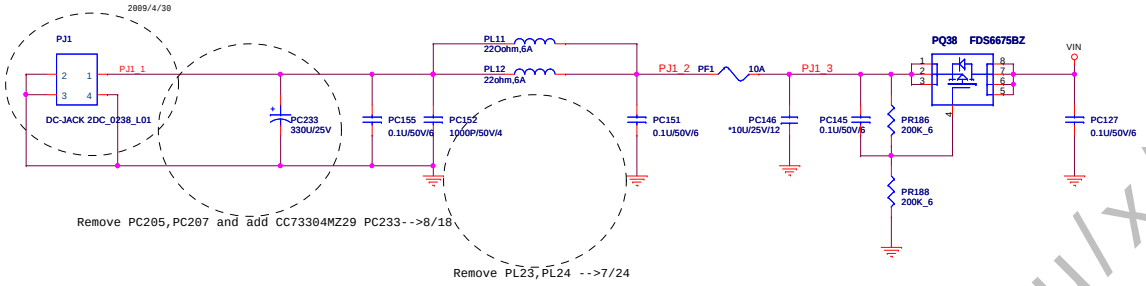
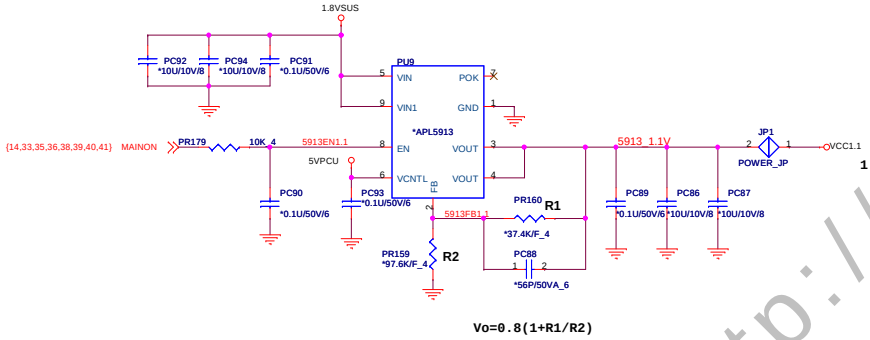


ACIN

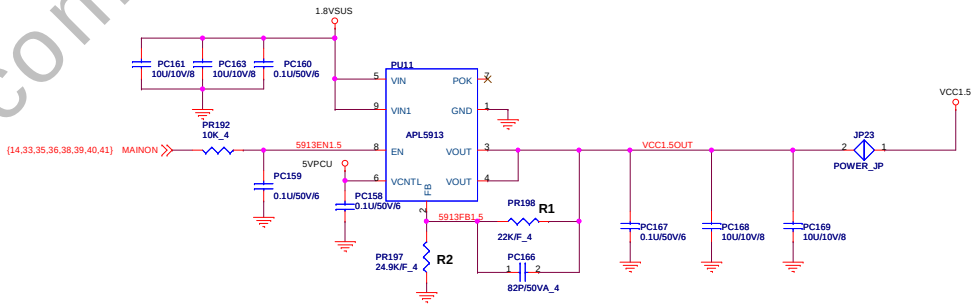


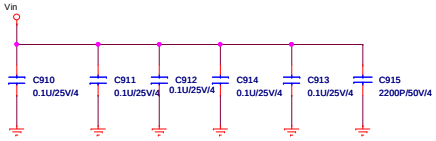
+1.1V



Vo=0.8(1+R1/R2)

MINI CARD POWER





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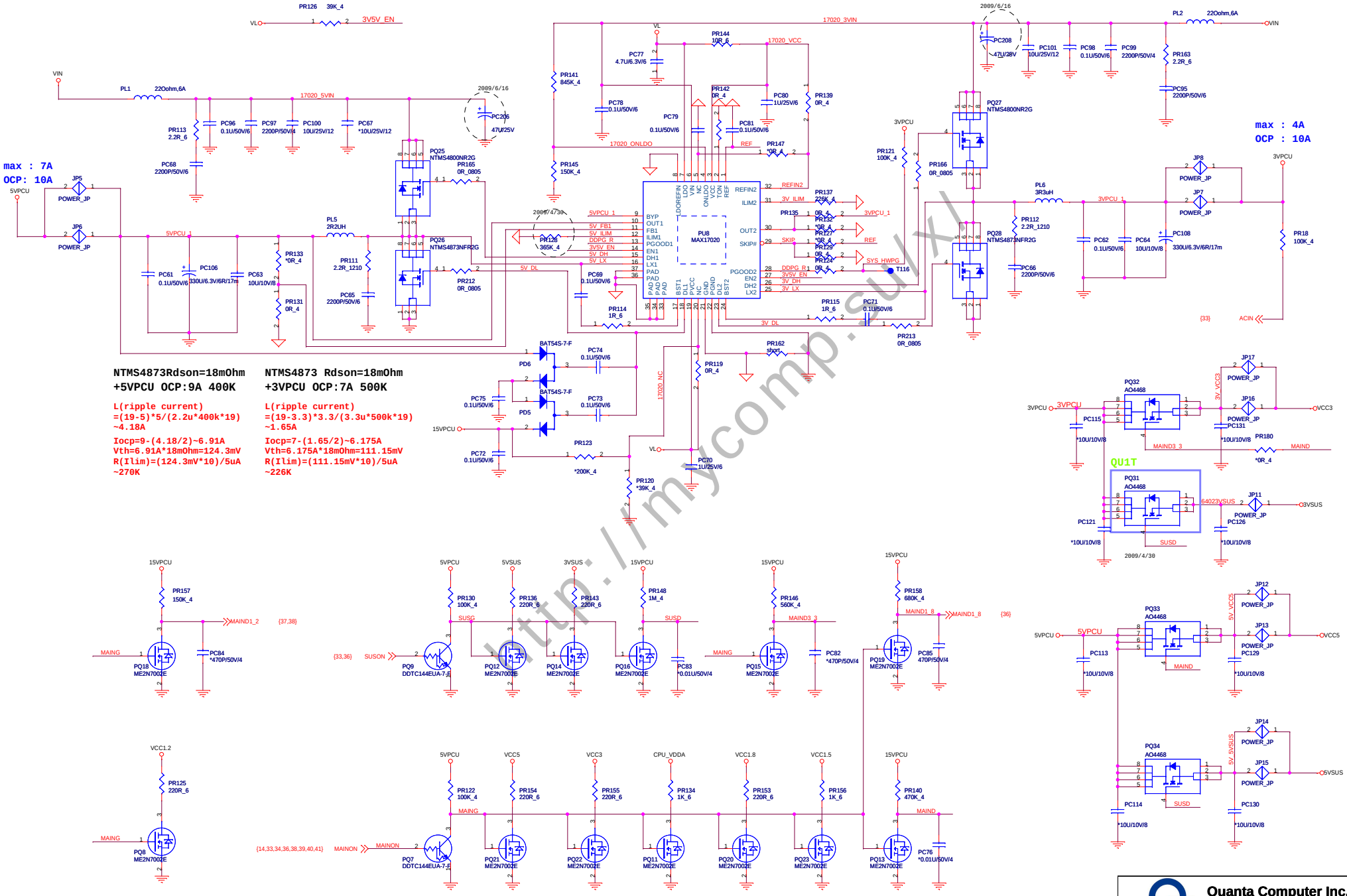

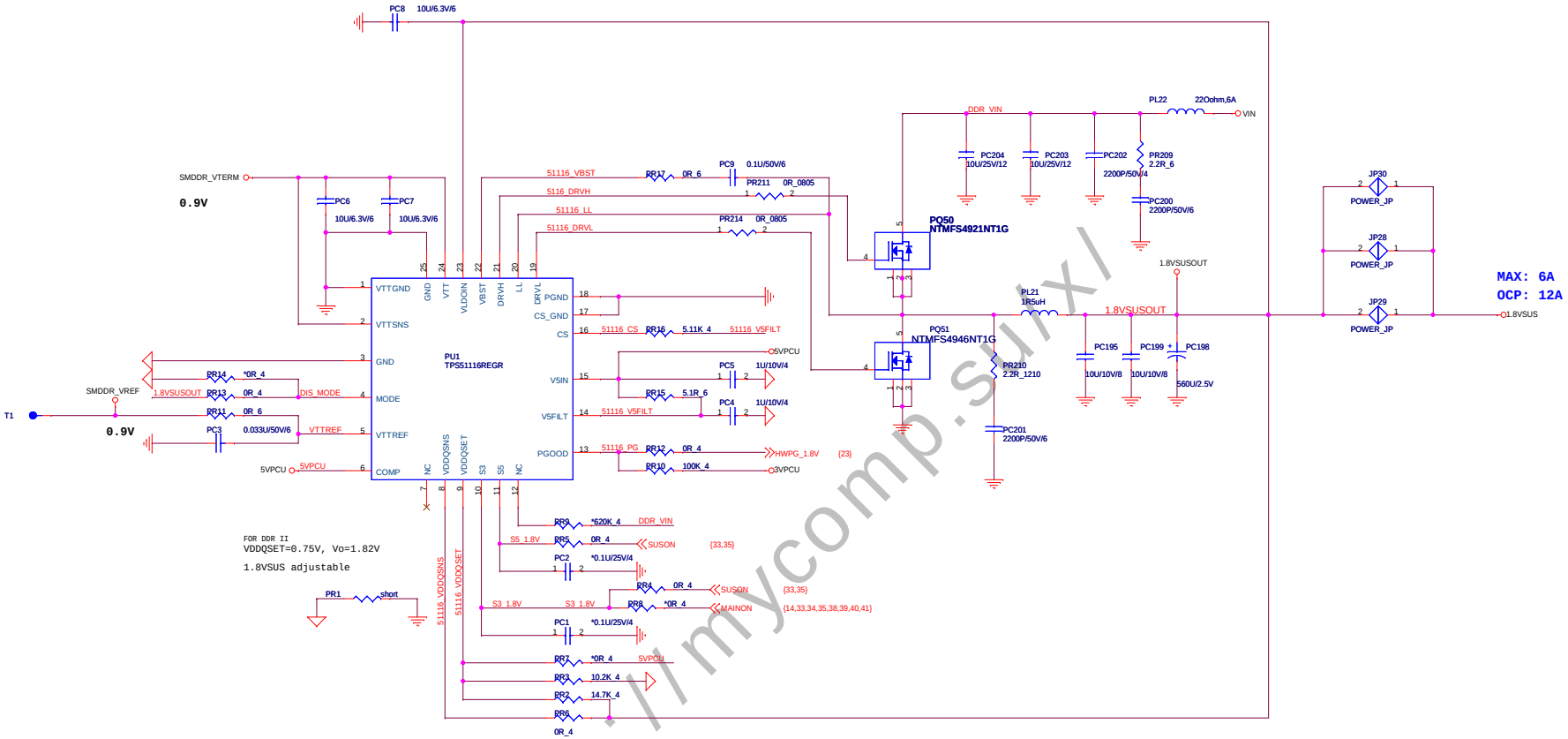

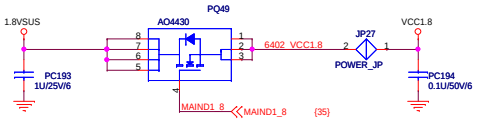

NTMFS4946Rdson=3.8~4.6mOhm

L(ripple current)
=(19-1.8)*1.8/(1.5u*400k*19)
~2.72A

4.6m*(12-(2.72/2))=RILIM*10uA
RILIM=5.11K
((10u*PR67)/Rdson)+(Delta_I/2)=Iocp

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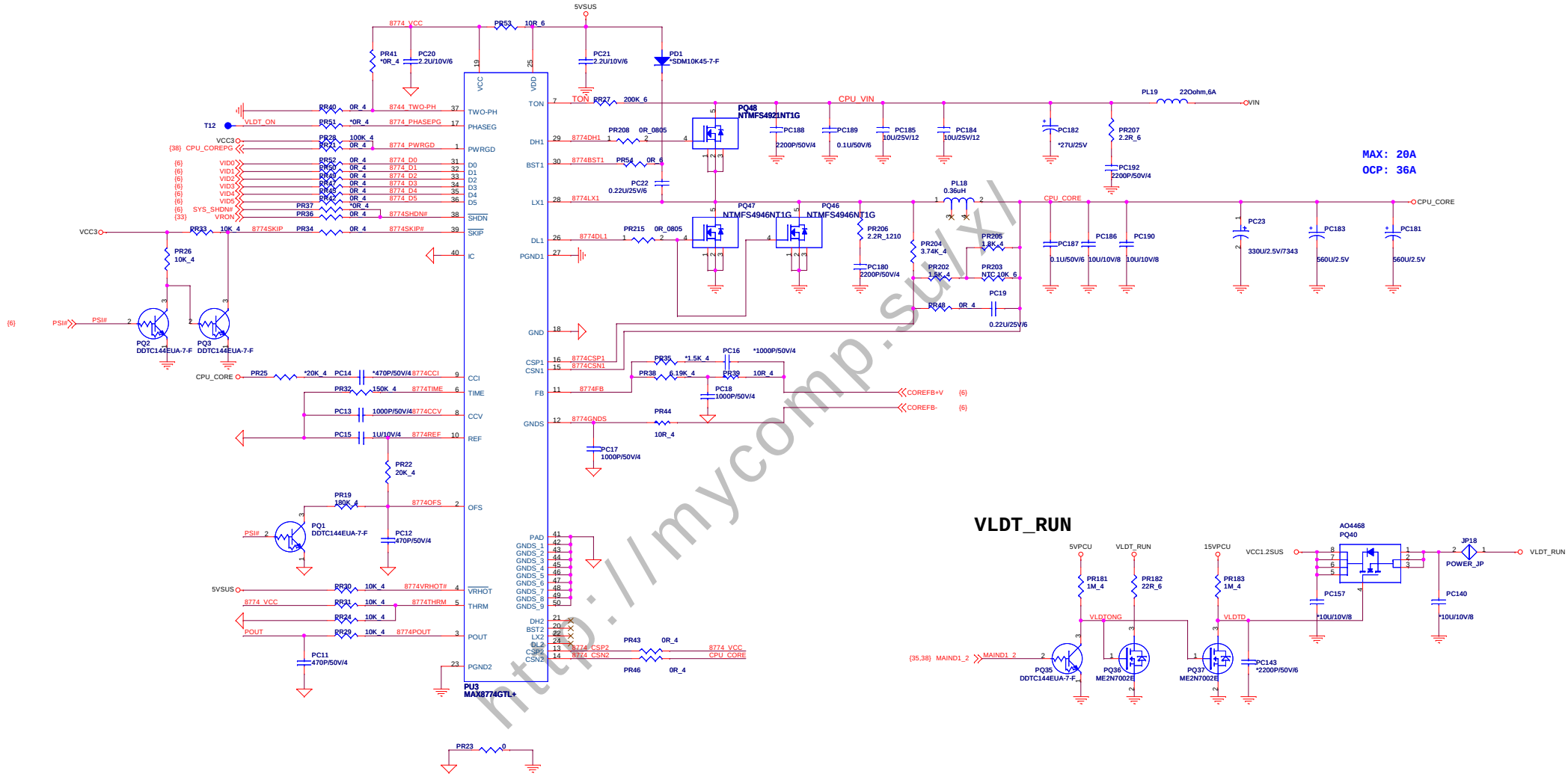
CPU CORE



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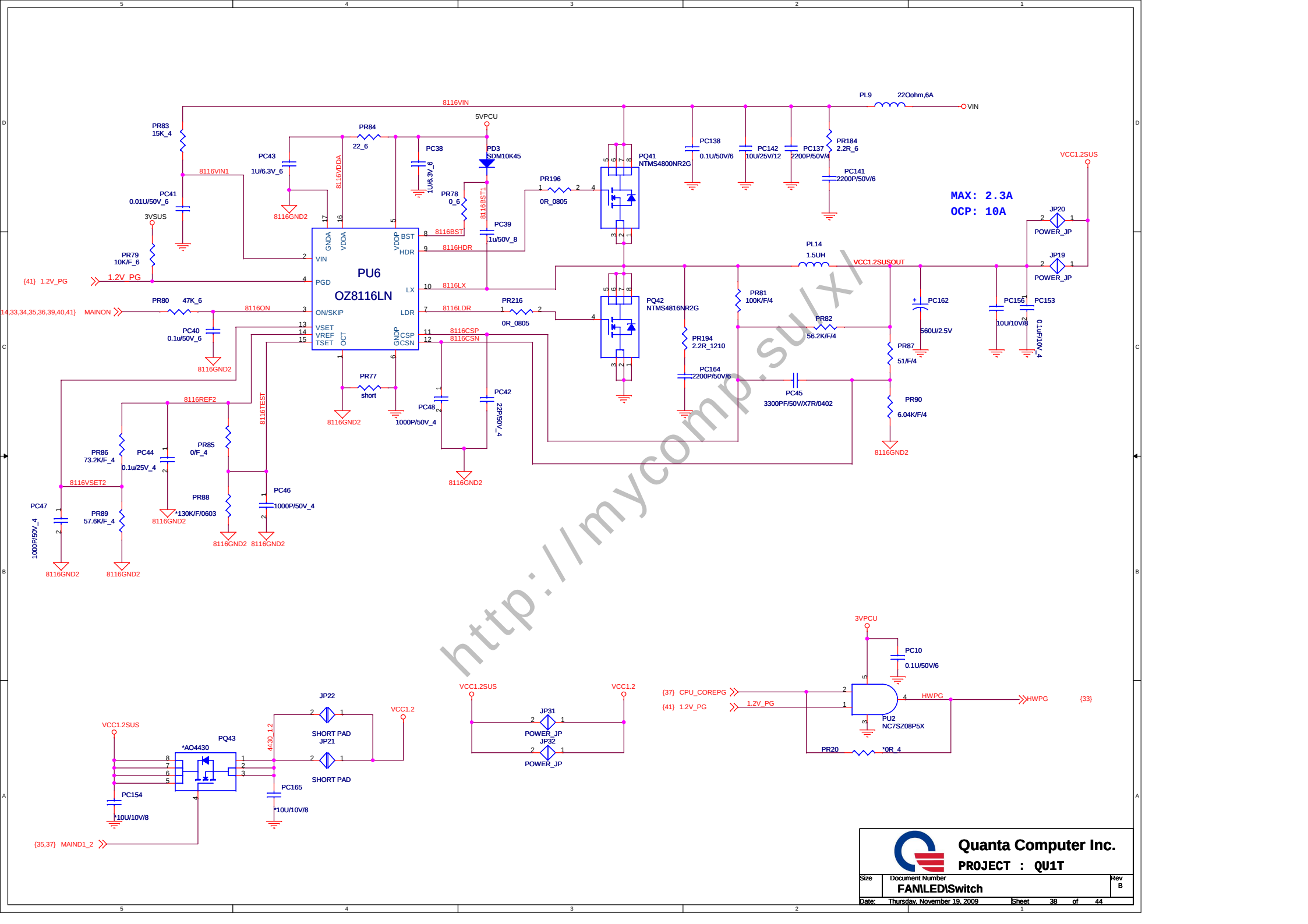

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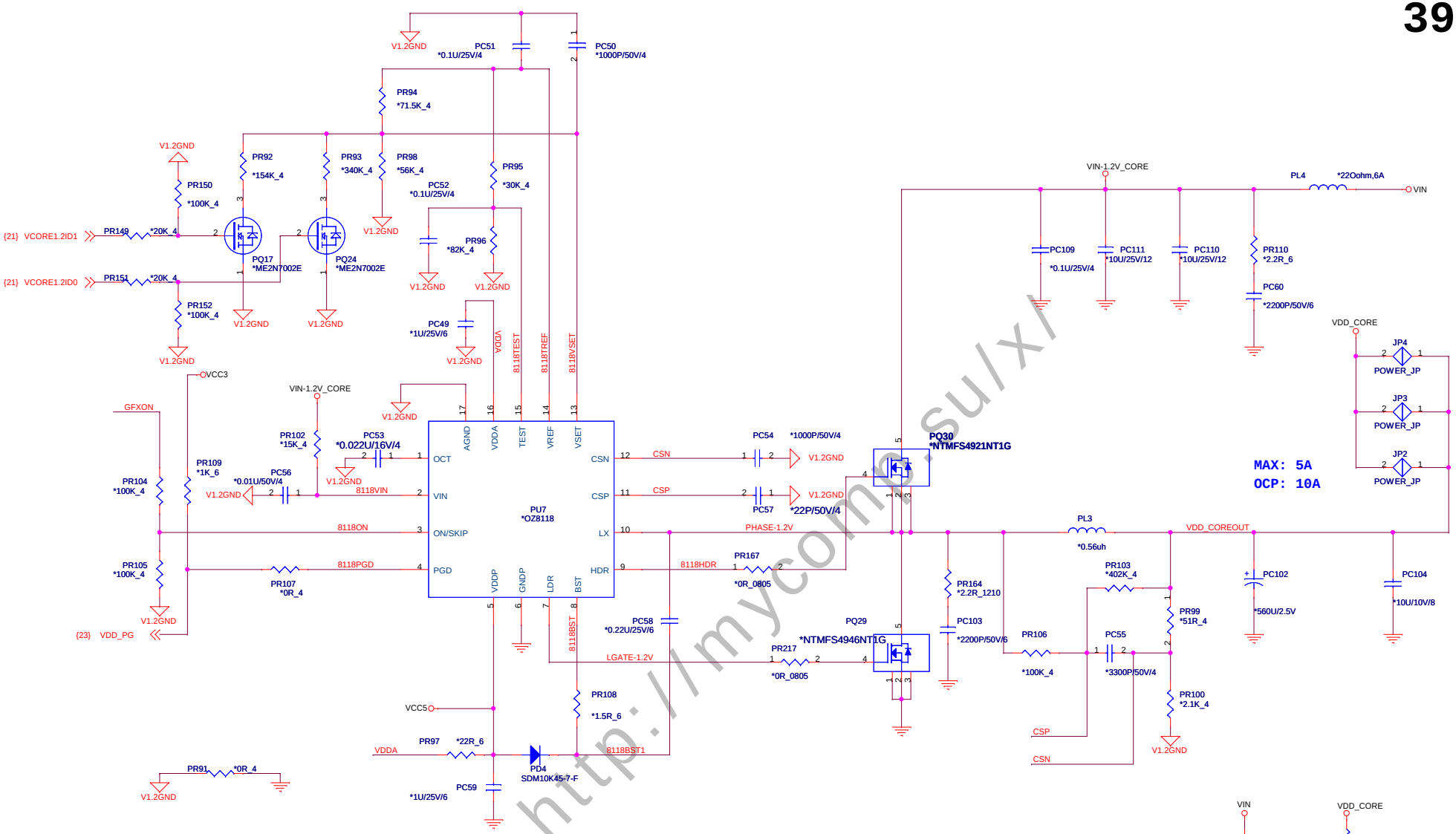

M86 TABLE

PR228: 82.5K
PR229: 226K
PR230: 374K

VID[1:0]		
VID1	VID0	
0	0	1.1V
0	1	1.0V
1	0	0.95V
1	1	0.9V

M92 TABLE

PR228: 71.5K
PR229: 154K
PR230: 340K

VID[1:0]		
VID1	VID0	
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

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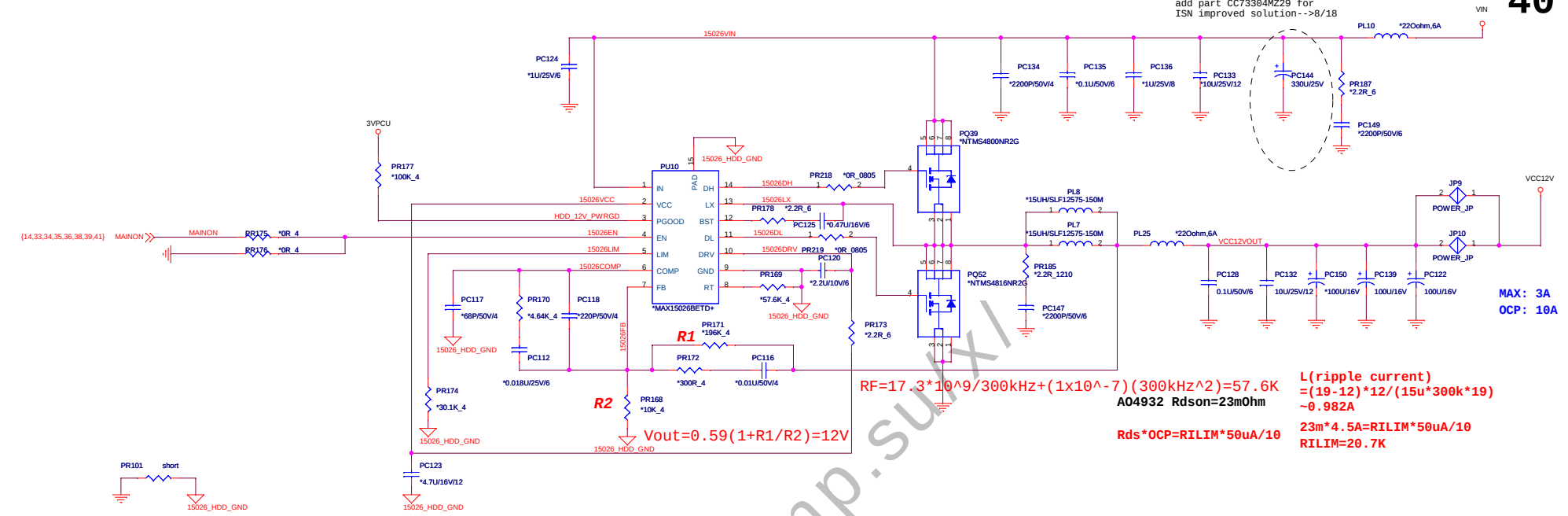
Change PC144 footrpint and
add part CC73304MZ29 for
ISN improved solution-->8/18



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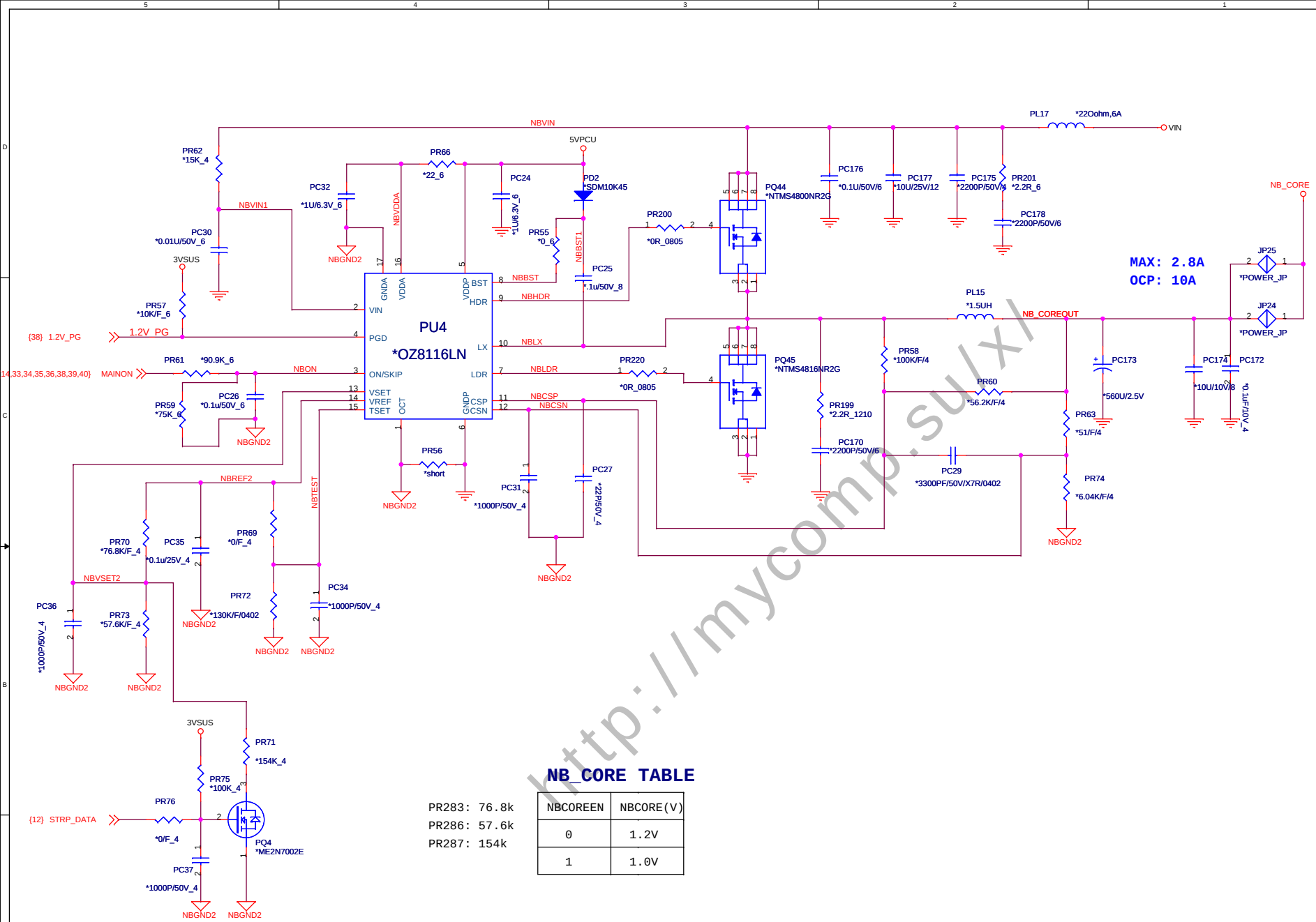

NB_CORE TABLE

PR283: 76.8k
PR286: 57.6k
PR287: 154k

NBCOREEN	NBCORE(V)
0	1.2V
1	1.0V

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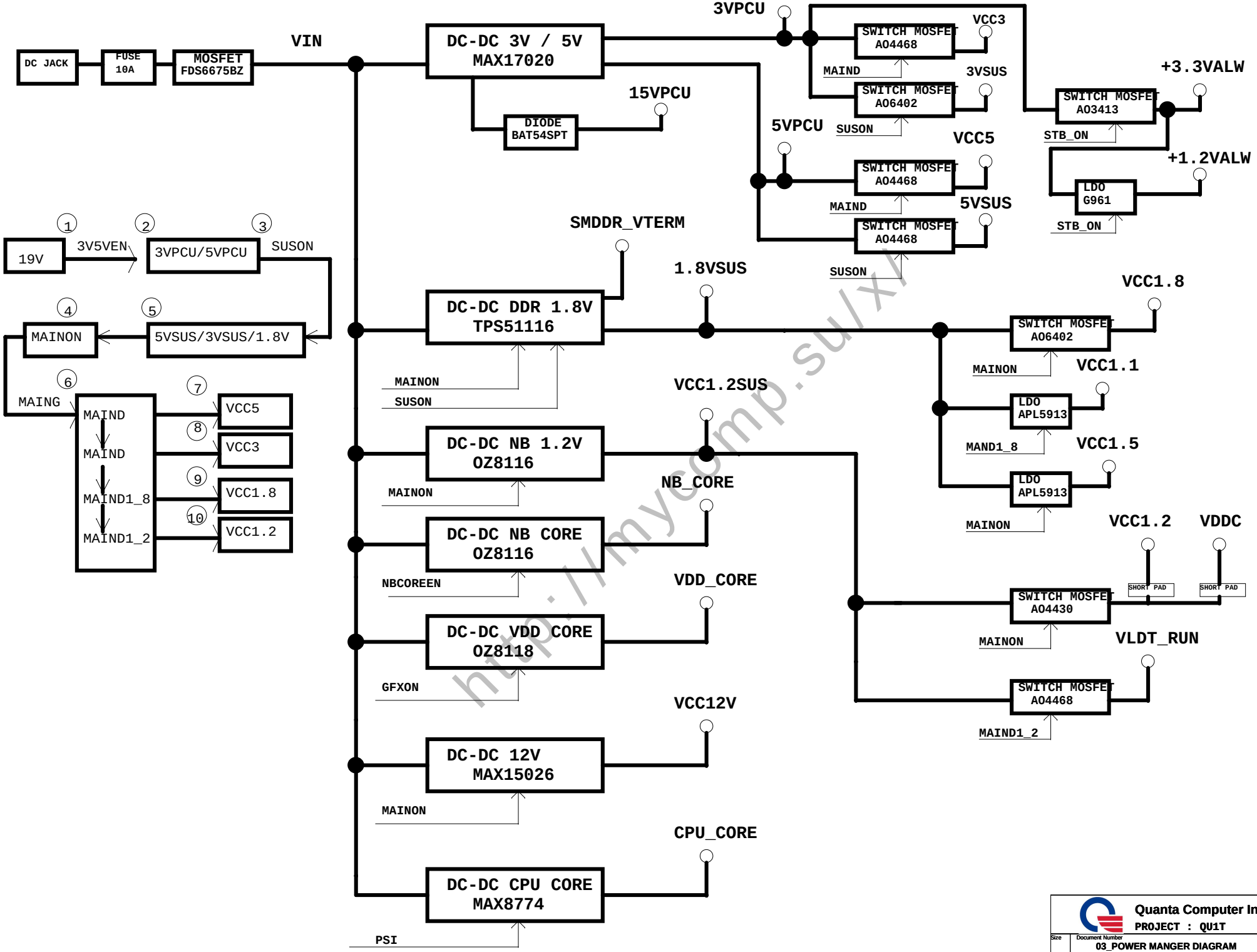

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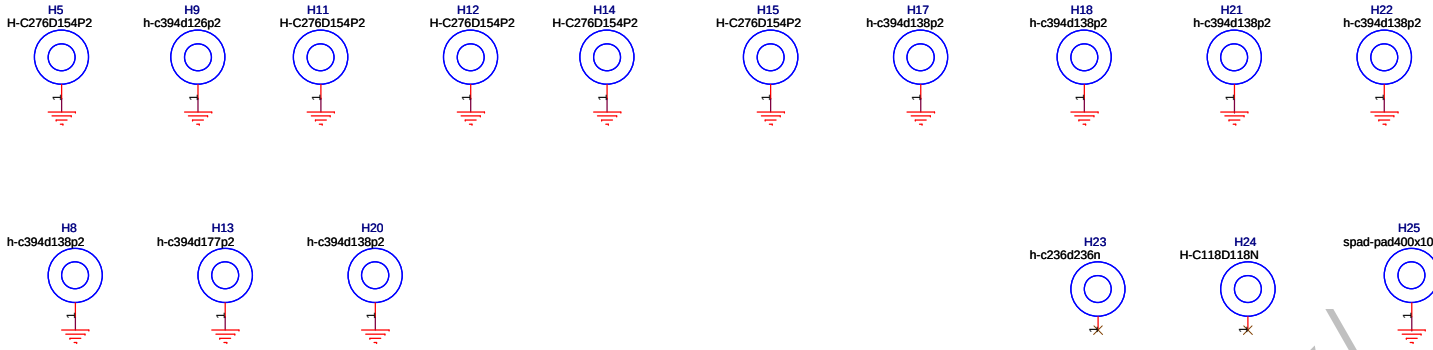

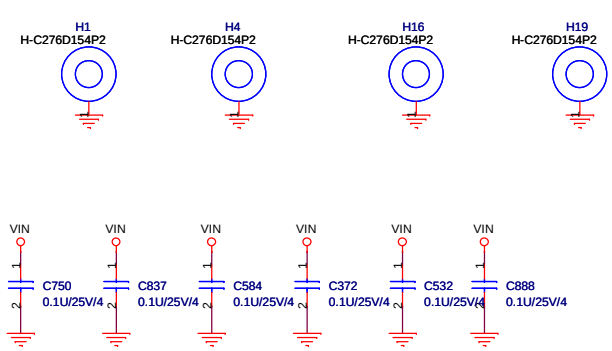

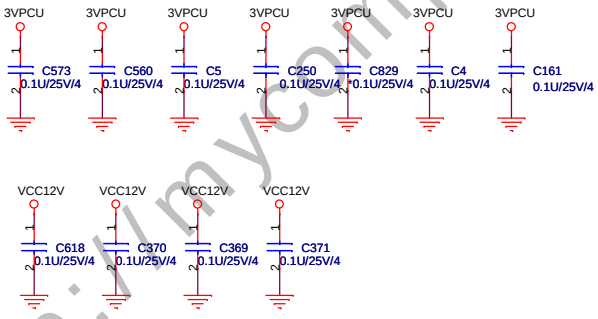

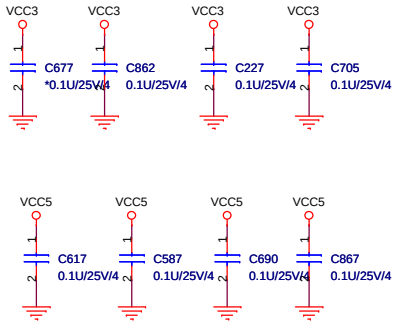

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A Stage:Base on QU1 Rev. F Schematics to modify.

1. (P. 26)Change R130, R134 footprint from 0603 to 1206-->new add on 5/13
2. (P. 27)Add Touch Panel USB interface connector.->new add on 5/13
3. (P. 33)Add Multi-Media Board I2C interface connector.->new add on 5/13
4. (P. 30)Add Buzzer Connector.->new add on 5/13
5. (P. 14, P. 35)Change PQ5 and PQ31 package by POWER request.->new add on 5/13
6. (P.27)del R112.R110,R111,R109,R61,R57,R60,R56,R27,R28,R25,R26->new add on 5/13
7. (P 26)Change U43 Surge IC->new add on 5/13
8. (P 35)PR128 change to 365K ->new add on 5/13
9. (P 34)PJ1 change footprint from (dcjk-2dc-0238-r05-a1-2p) to (dcjk-2dc-0238-r06-5p-v)->new add on 5/13
10. (P 19)Modify CAMERA POWER->new add on 5/13
11. (P 32) Modify CAMERA HOT KEY->new add on 5/13
12. (P 34) add PL23 ,PL24 by power request->new add on 5/13
13. (P 26) Change C186 to 0603 type, US PIN4.5.12.13 connect to GND->new add on 5/13
14. (P 33) Add Touch_key_pwr circuits to control touch strip board power-->new add on 6/4
15. (P 15) Add R695,R697 to select TV or touch panel use USB port7-->new add on 6/8
16. (P 27) Add L99,U48,F14,CN21 and DEL J3 to support touch panel using USB port7,9-->new add on 6/9
17. (P 34) Add PC205,PC207 to reserve ISN issue--> new add on 6/15
18. (P 27)Add Touch PANEL LED EMI reserved circuit--> new add on 6/16
19. (P 27)DEL KEYBOARD MATRIX CIRCUIT-->new add on6/16
20. (P 35)Add PC206,PC208 for ISN issue reserve-->new add on 6/16
21. (P 35)Change layer PC101.PC98.PC99.PC95.PR163 to TOP layer-->new add on 6/17
22. (P 15,19,27)Update for USB port 7 to selection with TV and CCD and port8,9 use to Touch screen port -->new add on 6/18

B Stage:Base on QU1T A stage Schematics to modify.

1.Pag.34 PR161 , PL23 , PL24 delete-->new add on 7/24
2.Pag.36 PC196 , PC197 delete , PC198 change to 560u/2.5v-->new add on 7/24
3.Pag.37 PC191 , PC179 delete , PC181 , PC183 change to 560u/2.5v-->new add on 7/24
4.Pag.38 PC148 delete , PC162 change to 560u/2.5v-->new add on 7/24
5.Pag.39 PC105 , PC107 , PC119 delete , PC102 change to 560u/2.5v->new add on 7/24
6.Pag.40 12v PWR circuit NA , add 12V LDO circuit .-->new add on 7/24
7.Pag.41 NB_CORE circuit NA .-->new add on 7/24
8.PC203 , PC264 , PC185 , PC184 , PC142 , PC111 , PC110 , PC133 , PC132 , PC177 Quanta P/N change to CH6104K9207 .-->new add on 7/24
9.Pag.40 Cgange power rail from NB_CORE to VCC1.2-->new add on 7/24
10.Pag34 Remove PC205,PC207 and add CC73304MZ29 PC233-->8/18
11.Pag40 Change PC144 footrpint and add part CC73304MZ29-->8/18
12.Pag35 NA PC101 -->8/18
13.Pag12 NA C318,C325,U7 for cost down-->8/26
14.Pag13 Add reserved power plan NB_CORE-->8/26
15.Pag14 Change R569 to D3009-->new add on 8/26
16.Pag19 Delete R360,R651,shorten the trace of pin4,5,6 on CN3-->new add on 8/26
17.Pag38 Delete U30 H_P amplifier, connect HPOUTL to HPOUT_L1, HPOUTR to HPOUT_R1-->new add on 8/26
18.Pag32 DEL C557,C564,C556,R345,R347,R354,R353,R356,Q23,U11,CON5 for fan cost down-->new add on 8/26

C Stage:Base on QU1T B stage Schematics to modify.

1.Pag.27 add U41,U42,U33,U34 For ESD issue---->new add 11/15

2.Pag.30 add C874,C875,R671,R672,R717,R718 ,PR161,PR189 connect HPOUT_L1 to HPOUTL,HPOUT_R1 to HPOUTR---->new add 11/18