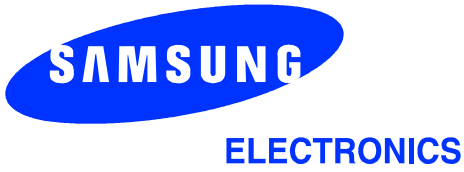
SAMSUNG

SAMSUNG Anycall
SGH-X480
SGH-X480C
SGH-X488

SERVICE *Manual*

SAMSUNG Anycall

CONTENTS



ELECTRONICS

Code No.: GH68-06818A
BASIC.

1. Specification

1. GSM General Specification

	EGSM 900 Phase 2	DCS 1800 Phase 1	PCS 1900 Phase 1
Freq. Band[MHz] Uplink/Downlink	880~915 925~960	1710~1785 1805~1880	1850~1910 1930~1960
ARFCN range	0~124 & 975~1023	512~885	512~810
Tx/Rx spacing	45MHz	95MHz	80MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~5dBm	30dBm~0dBm	30dBm~0dBm
Power Class	5pcl ~ 19pcl	0pcl ~ 15pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-100dBm	-100dBm
TDMA Mux	8	8	8
Cell Radius	35Km	2Km	2Km
Operating Temperature	-20 ℃ ~ +50 ℃		

2. Circuit Description

1. SGH-X480, SGH-X480C, SGH-X488 RF Circuit Description

1) RX PART

1. ASM(F900) → Switching Tx, Rx path for GSM900, DCS1800 and PCS1900 by logic controlling.

2. ASM Control Logic Truth Table

	VC1	VC2	VC3
Tx (GSM900)	H	L	L
Tx (DCS1800/ PCS1900)	L	H	L
Rx (GSM900)	L	L	L
Rx (DCS1800)	L	L	L
Rx (PCS 1900)	L	L	H

3. Saw FILTER

To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

- GSM FILTER (F800) → For filtering the frequency band between 925 and 960 MHz.
- DCS FILTER (F800) → For filtering the frequency band between 1805 and 1880 MHz
- PCS FILTER (F801) → For filtering the frequency band between 1930 and 1990 MHz.

4. Crystal (U802)

To generate the 26MHz reference clock to drive the logic and RF.

After additional process, the reference clock applies to the U801 Rx IQ demodulator and Tx IQ modulator.

The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. Si4210 (U801)

The receive section integrates four differential-input low noise amplifiers LNAs supporting the GSM850, EGSM900, DCS1800 and PCS1900 bands. The LNA inputs are matched to the 150 ohm balanced-output SAW filters through externa LC matching network.

A quadrature Image-reject mixer downconverts the RF signal to a 200 KHz intermediate frequency(IF). The mixer output is amplified with an analog programmable gain amplifier(PGA) that is controlled with the AGAIN. The quadrature IF ? ? is digitized with high resolution analog-to-digital converts (ADC).

The ADC output is downconverted to baseband with a digital quadrature LO signal. Digital decimation and FIR filters perform digital filtering and remove ADC quantization noise, blockers and reference interferers.

After filtering, the digital output is scaled with a digital PGA, which is controlled with the DGAIN. DACs drive a differential I and Q analog signal onto the BIP, BIN, BQP and BQN pins to interface to standard analog-input baseband ICs.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U801 chip. The transmit section of U801 consist of an I/Q baseband upconverter, an offset phase-locked loop (OPLL) and two 50 ohm output buffers that can drive an external Power Amplifier(PA). Si4210 chip generates modulator signal which power level is about 1.5dBm and fed into Power Amplifier(U900). The PA output power and power ramping are well controlled by Auto Power Control circuit.
We use offset PLL below.

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		DCS	-35dBc
		PCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		DCS	-65dBc
		PCS	-66dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		DCS	-68dBc
		PCS	-75dBc

2. Baseband Circuit description of SGH-X480,SGH-X480C,SGH-X488

1) CSP2200B1

1. Power Management

Seven low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable LDO provides support for 1.8V, 3.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as two LED drivers and two call-alert drivers, aid in reducing both board area and system complexity. A four-wire serial interface unit(SIU) provides access to control and configuration registers. This interface gives a microprocessor full control of the CSP2200B1 and enables system designers to maximize both standby and talk times. Error reporting is provided via an interrupt signal and status register. Supervisory functions. including a reset generator, an input voltage monitor, and a thermal monitor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

2. Battery Charge Management

A battery charge management block, incorporating an internal PMOS switch, and an 8-bit ADC, provides fast, efficient charging of single-cell Li-Ion battery. Used in conjunction with a current-limited voltage source, this block safely conditions near-dead cells and provides the option of having fast-charge and top-off controlled internally or by the system's microprocessor.

3. Backlight LED Driver

The backlight LED driver is a low-side, programmable current source designed to control the brightness of the keyboard illumination. LED1_DRV is controlled via LED1_[0:2] and can be programmed to sink from 15mA to 60mA in 7.5mA steps. LED2_DRV is controlled via LED2_[0:2] and can be programmed to sink from 5mA to 40mA in 5mA steps.
Both LED drivers are capable of sinking their maximum output current at a worst-case maximum output voltage of 0.6V. For efficient use, the LEDs is connected between the battery and the LED_DRV output.

4. Vibrator Motor Driver

The vibrator motor driver is a independent voltage regulator to drive a small dc motor that silently alerts the user of an incoming call. The driver is a 3.3V constant source while sinking up to 140mA and controlled by enable signal of main chip. For efficient use and safety, the vibrator motor should be connected between the regulator output and the ground.

2) Connector

1. LCD Connector

LCD is consisted of main LCD(color 65K STN LCD). Chip select signals of EMI part in the trident, LCD_CS, can enable main LCD. LED+ signal enables white LED of main LCD. In sleep mode, white LED are turned off.
These two signals are from IO part of the DSP in the trident. RST signal from CSP2200B1 initiates the initial process of the LCD.
8-bit data lines(D(0)~D(7)) transfers data and commands to LCD through emi_filter. Data and commands use A(2) signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data.
The signals which inform the input or output state to LCD, are required. But this system is not necessary for read enable signal. CP_WEN signal is only used to write data or commands to LCD.
Power signal for operating LCD driver is VCCD.

2. JTAG Connector

Trident has two JTAG ports which are for ARM core and DSP core(DSP16000). So this system has two port connector for these ports. Pins' initials for ARM core are 'CP_' and pins' initials for DSP core are 'DSP_'.
CP_TDI and DSP_TDI signal are used for input of data. CP_TDO and DSP_TDO signals are used for the output of the data. CP_TCK and DSP_TCK signals are used for clock because JTAG communication is a synchronous. CP_TMS and DSP_TMS signals are test mode signals. The difference between these is the RESET_INT signal which is for ARM core RESET.

3. Keypad connector

This is consisted of key interface pins in the trident, KEY_ROW[0~4] and KEY_COL[0~4]. These signals compose the matrix. Result of matrix informs the key status to key interface in the trident. Some pins are connected to varistor for ESD protection. And power on/off key is seperated from the matrix.
So power on/off signal is connected with CSP2200 to enable CSP2200.
Nine key LED use the +VBATT supply voltage. These are connected to BACKLIGHT signal in the CSP2200.
This signal enables LEDs with current control.

4. EMI Filtering

This system uses the EMI Filter to reduce noise from LCD part. Some control signals are connected to LCD without EMI filtering.

3) IF connetor

It is 24-pin connector, and separated into two parts. One is a power supply part for main system. And the other is designed to use SDS, DEBUG, DLC-DETECT, JIG_ON, VEXT, VTEST, VF, and GND. They connected to power supply IC, microprocessor and signal processor IC.

4) Audio

AOUTAP, AOUTAN from CSP2200 is connected to the speaker via analog switch. AOUTBP and AOUTBN are connected to the ear-mic speaker via ear-jack. MICIN and MICOUT are connected to the main MIC. And AUXIN and AUXOUT are connected to the Ear-mic.
YMU762MA3 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decorder that are included in this device.
As a synthesis, YMU762MA3 is equipped 16 voices with different tones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects. Since the play data of YMU762MA3 are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexibly support application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.
YMU762 includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibartor and a circuit for controlling LEDs synchornous with music.
For the headphone, it is provided with a stereophonic output terminal.
For the purpose of enabling YMU762MA3 to demonstrate its full capabilities, Yamaha purpose to use "SMAF:Synthetic music Mobile Application Format" as a data distribution format that is compatible with multimedia.

Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for training karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU762MA3 directly interprets and plays blocks relevant to synthesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

5) Memory

This system uses SHARP's memory, LRS18B0.
It is consisted of 256M bits flash memory and 64M bits SCRAM. It has 16 bit data line, D[0~15] which is connected to trident, LCD or CSP2200. It has 23 bit address lines, A[1~23]. They are also connected. CP_CSROMEN signal, chip select signal in the trident, enable flash memories. They use supply voltages, VCCD and VCC_1.8A.
During wrting process, CP_WEN is low and it enables writing process to flash memory and SCRAM. During reading process, CP_OEN is low and it output information which is located at the address from the trident in the flash memory or SCRAM to data lines. Each chip select signals in the trident select flash memory or SCRAM. Reading or writing procedure is processed after CP_WEN or CP_OEN is enabled. Memories use FLASH_RESET, which is buffered signal of RESET from CSP2200, for ESD protection. A[0] signal enables lower byte of SCRAM and UPPER_BYTE signal enables higher byte of SCRAM.

6) Trident

Trident is consisted of ARM core and DSP core. It has 20K*16bits RAM 144K*16bits ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of timer, one bit input/output unit(BIO), JTAG, EMI and HDS(Hardware Development System). ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACCs(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface.
DSP_AB[0~8], address lines of DSP core and DSP_DB[0~15], data lines of DSP core are connected to CSP2200. A[0~20], address lines of ARM core and D[0~15], data lines of ARM core are connected to memory, LCD and YMU762.
ICP(Interprocessor Communication Port) controls the communication between ARM core and DSP core.
CSROMEN, CSRAMEN and CS1N to CS4N in the ARM core are connected to each memory. WEN and OEN control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, YMU, Ear-jack, Ear-mic and CSP1093, need the compatible process.
Some PPI pins has many special functions. CP_KB[0~9] receive the status from key FPCB and are used for the communications using data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR).
And UP_CS/SCLK/SDI, control signals for CSP2200 are outputted through PPI pins. It has signal port for charging(CHG_DET), SIM_RESET and FLIP_SNS with which we knows open.closed status of folder. It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It recieves 13MHz clock in CKI pin from external TCXO and receives 32.768KHz clock from X1RTC. ADC(Analog to Digital Convertor) part receives the status of temperature, battery type and battery voltage. And control signals(DSP_INT, DSP_IO and DSP_RWN) for DSP core are used. It enables main LCD with DSP IP pins.

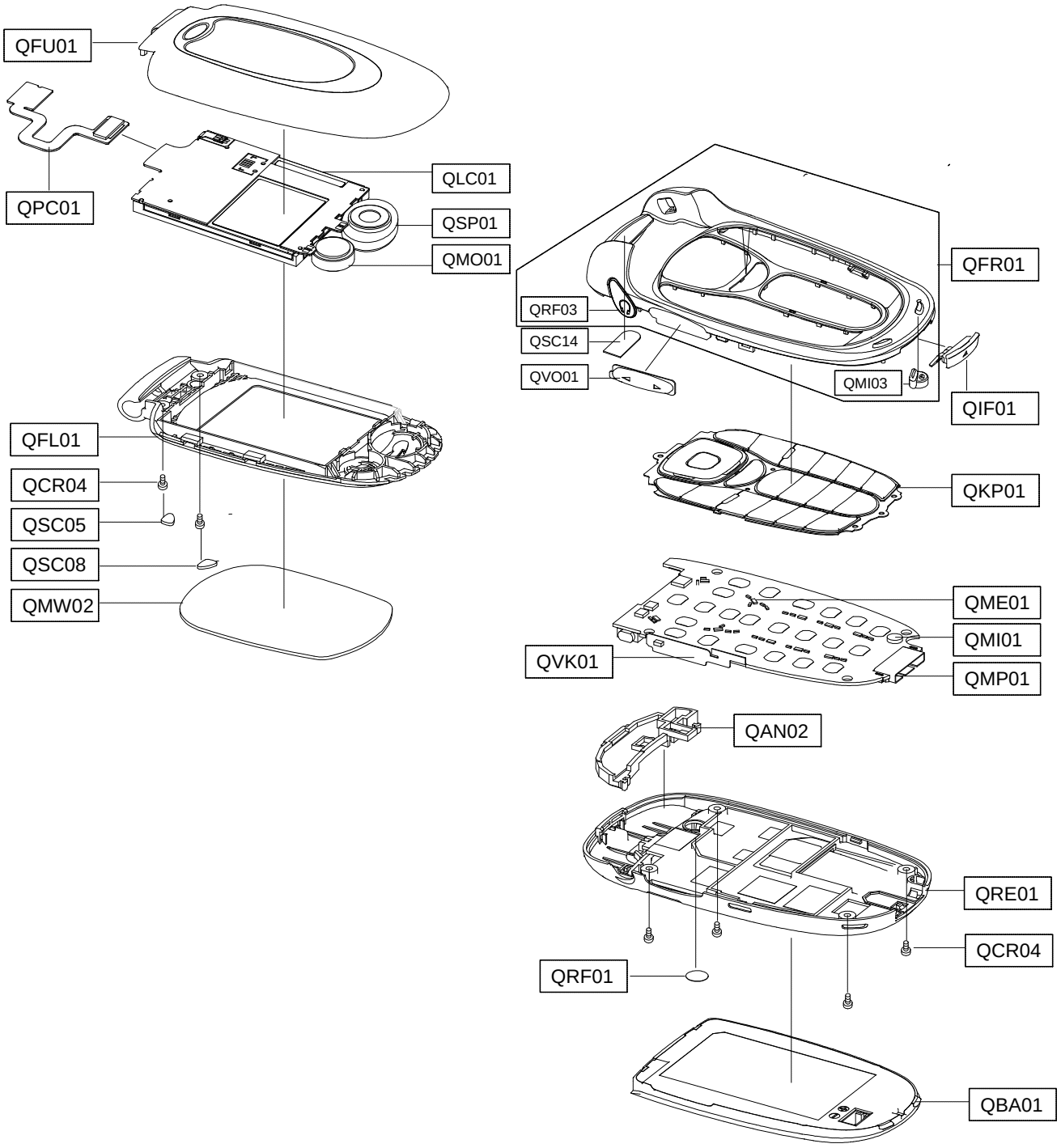
7) CSP2200

CSP2200 is integrated the timing and control functions for GSM 2+ mobile application with the ADC and DAC functions, and power management block. The CSP2200 interfaces to the trident, via a 16-bit parallel interface. It serves as the interface that connects a DSP to the RF circuitry in a GSM 2+ mobile telephone. DSP can load 148 bits of burst data into CSP2200's internal register, and program CSP2200's event timing and control register with the exact time to send the burst. When the timing portion of the event timing and control register matches the internal quarter-bit counter and internal frame counter, the 148 bits in the internal register are GMSK modulated according to GSM 2+ standards. The resulting phase information is translated into I and Q differential output voltages that can be connected directly to an RF modulator at the TXOP and TXON pins. The DSP is notified when the transmission is completed. For receiving baseband data, a DSP can program CSP2200's event timing and control register with the exact time to start receiving I and Q samples through TXIP and TXIN pins. When that time is reached, the control portion of the event timing and control register will start the baseband receive section converting I and Q sample pairs. The samples are stored in a double-buffered register until the register contains 32 sample pairs. CSP2200 then notifies the DSP which has sample time to read the information out before the next 32 sample pairs are stored. The voice band ADC converter issues an interrupt to the DSP whenever it finishes converting a 16-bit PCM word. The DSP then reads the new input sample and simultaneously loads the voice band output DAC converter with a new PCM output word. The voice band output can be connected directly to a speaker via AOUTAN and AOUTAP pins and be connected to a Ear-mic speaker via AOUTBN and AOUTBP pins.

There are 7 LDOs which are power sources of microprocessor, LCD, etc. These 7 LDOs output are programmable.

3. Exploded View and Parts list

1. Cellular phone Exploded View-1



2. Cellular phone Parts list

Location NO.		Description	SEC CODE		
			SGH-X480	SGH-X480C	SGH-X488
QFR01		FRONT COVER	GH75-06162A	GH75-06162A	GH75-06162A
	QRF03	EAR COVER	GH72-19072A	GH72-19072A	GH72-19072A
	QMI03	MIC HOLDER	GH73-04031A	GH73-04031A	GH73-04031A
QSC14		FRONT SHEET	GH74-13673A	GH74-13673A	GH74-13673A
QVO01		SIDE KEY	GH72-19086A	GH72-19086A	GH72-19086A
QIF01		IF COVER	GH72-19085A	GH72-19085A	GH72-19085A
QKP01		KEYPAD	GH75-06188A	GH75-06663A	GH75-06663A
QME01		UNIT METAL DOME	GH59-01925A	GH59-01925A	GH59-01925A
QMI01		MICROPHONE ASSY	GH30-00119A	GH30-00119A	GH30-00119A
QMP01		MAIN PBA	GH92-02033A	GH92-02033A	GH92-02033A
QVK01		UNIT VOLUME KEY	GH59-01927A	GH59-01927A	GH59-01927A
QAN02		INTENNA	GH42-00528A	GH42-00528A	GH42-00528A
QRE01		REAR COVER	GH75-06165A	GH75-06165A	GH75-06165A
QCR04		SCREW MACHINE	6001-001479	6001-001479	6001-001479
QRF01		TAPE RF SWITCH	GH74-12570A	GH74-12570A	GH74-12570A
QBA01		BATTERY	GH43-01661A	GH43-01729A	GH43-01729A
QFU01		FOLDER UPPER	GH75-06163A	GH75-06662A	GH75-06662A
QPC01		FPCB	GH41-00772A	GH41-00772A	GH41-00772A
QLC01		LCD	GH07-00655A	GH07-00655A	GH07-00655A
QSP01		SPEAKER	3001-001737	3001-001737	3001-001737
QMO01		MOTOR DC	GH31-00148A	GH31-00148A	GH31-00148A
QFL01		FOLDER LOWER	GH75-06164A	GH75-06164A	GH75-06164A
QCR04		SCREW MACHINE	6001-001479	6001-001479	6001-001479
QSC05		SCREW CAP R	GH74-12568A	GH74-12568A	GH74-12568A
QSC08		SCREW CAP L	GH74-12569A	GH74-12569A	GH74-12569A
QMW02		WINDOW MAIN	GH72-19120A	GH72-19120A	GH72-19120A

3. Test Jig (GH80-00865A)

3-1. RF Test Cable
(GH39-00283A)

3-2. Test Cable
(GH39-00127A)

3-3. Serial Cable

3-4. Power Supply Cable

3-5. DATA CABLE
(GH39-00143B)

3-6. TA
(GH44-00184A)

4. Electrical Parts List

SEC Code	Design LOC
0403-001387	ZD302
0403-001427	ZD303
0406-001190	U901
0406-001190	ZD304
0406-001190	ZD305
0406-001190	ZD306
0406-001201	V714
0406-001201	V715
0406-001201	V716
0501-000225	Q400
0504-000168	Q100
0505-001518	Q201
0801-000796	U102
1001-001294	U402
1009-001010	U702
1201-002174	U900
1203-003105	U206
1203-003105	U701
1203-003105	U703
1203-003304	U100
1204-002161	U401
1209-001219	U602
1405-001082	V203
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1405-001082	V405
1405-001082	V410
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1405-001082	V701
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1405-001082	V710

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2007-000142	R414
2007-000145	R437
2007-000146	R406
2007-000148	R410
2007-000148	R618
2007-000148	R809
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2007-000566	R302

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2203-006324	C706
2203-006438	C615
2404-001105	C425
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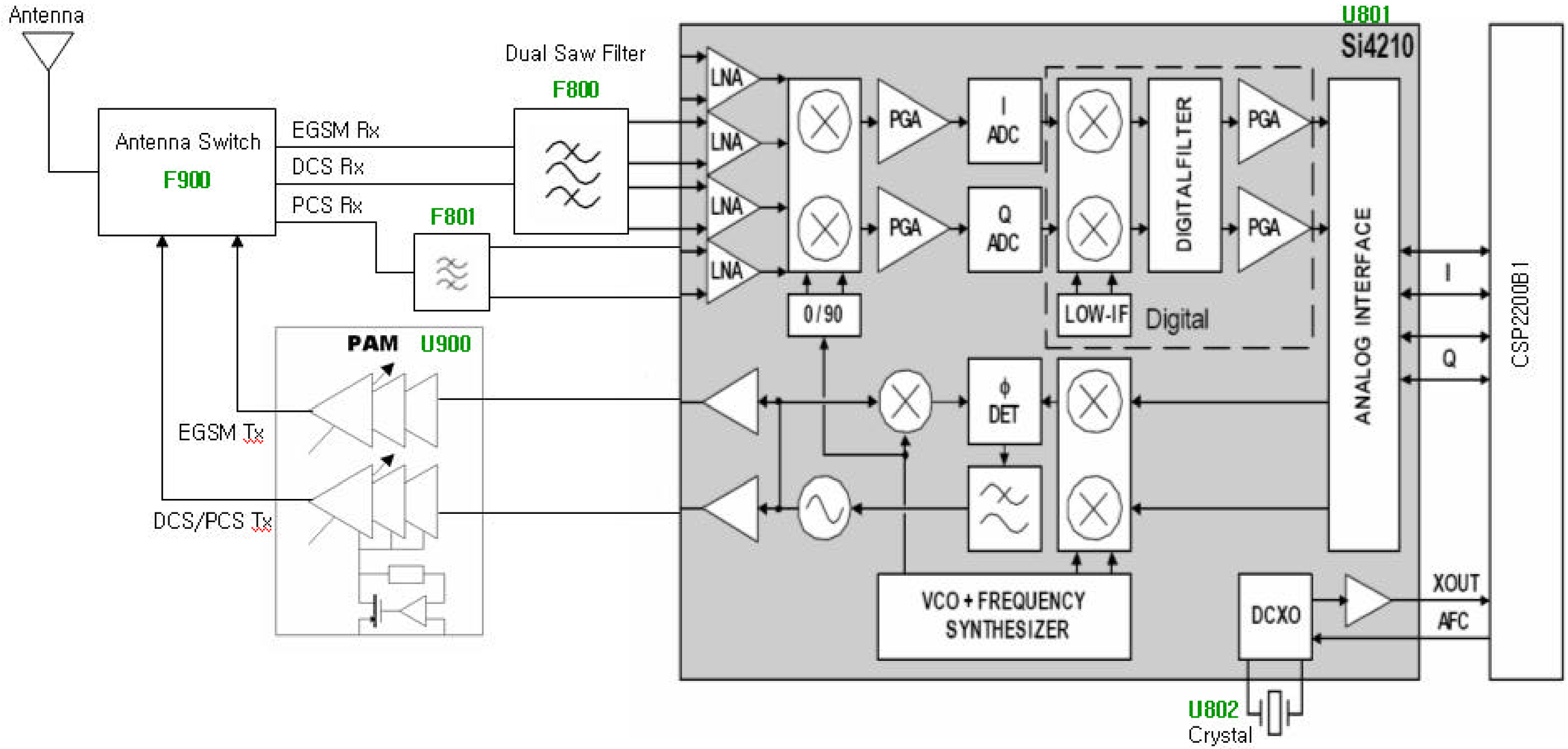
2404-001151	C423
2404-001239	C910
2404-001240	C111
2404-001268	C123
2404-001268	C125
2404-001268	C303
2404-001268	C402
2503-001041	C220
2503-001041	C221

SEC Code	Design LOC
2703-002170	L807
2703-002170	L901
2703-002199	L803
2703-002201	L903
2703-002201	L904
2703-002202	L401
2703-002202	L402
2703-002205	L805
2703-002339	L201
2703-002367	L902
2703-002558	L802
2703-002608	L806
2703-002815	L804
2801-003856	OSC600
2901-001286	U201
2901-001286	U202
2901-001286	U203
2904-001480	F801
2904-001523	F800
3301-001659	L301
3301-001729	L701
3705-001355	CON901
3709-001298	CN100
3710-001994	CN300
3711-005829	CN301
4302-001177	BAT100
GH09-00036A	U600
1108-000009	U500
1203-003663	U101
1203-003674	U200
2203-006562	C217
2203-006636	C216
2801-004426	U802
2911-000002	F900
3711-005885	CN200
3722-002067	CN401
0601-002020	D701
0601-002020	D702
0601-002020	D703

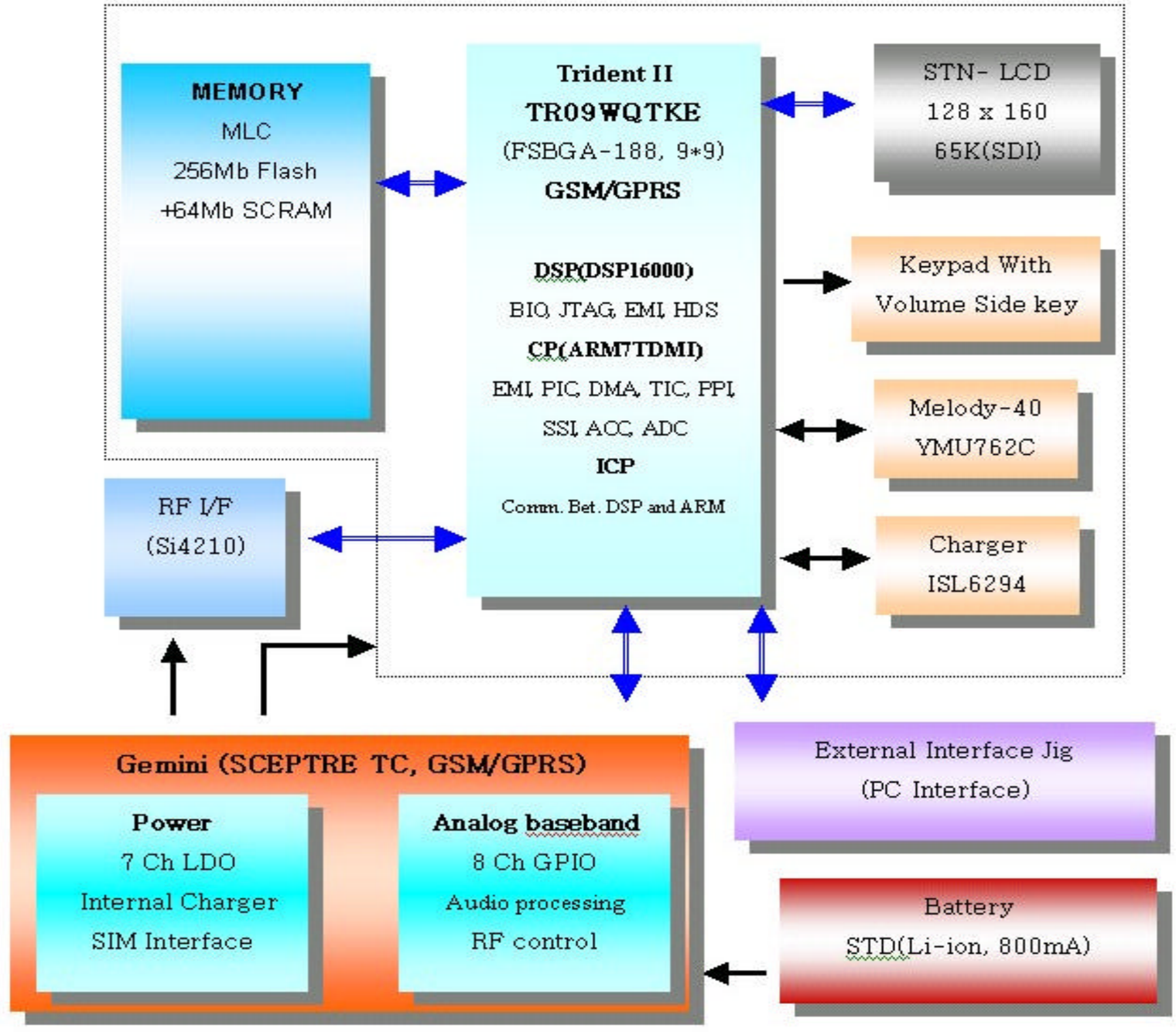
SEC Code	Design LOC
0601-002020	D704
0601-002020	D705
0601-002020	D706
0601-002020	D707
0601-002020	D708
0601-002020	D709
0601-002020	D711
1205-002683	U801

5. Block Diagrams

1. RF Solution Block Diagram

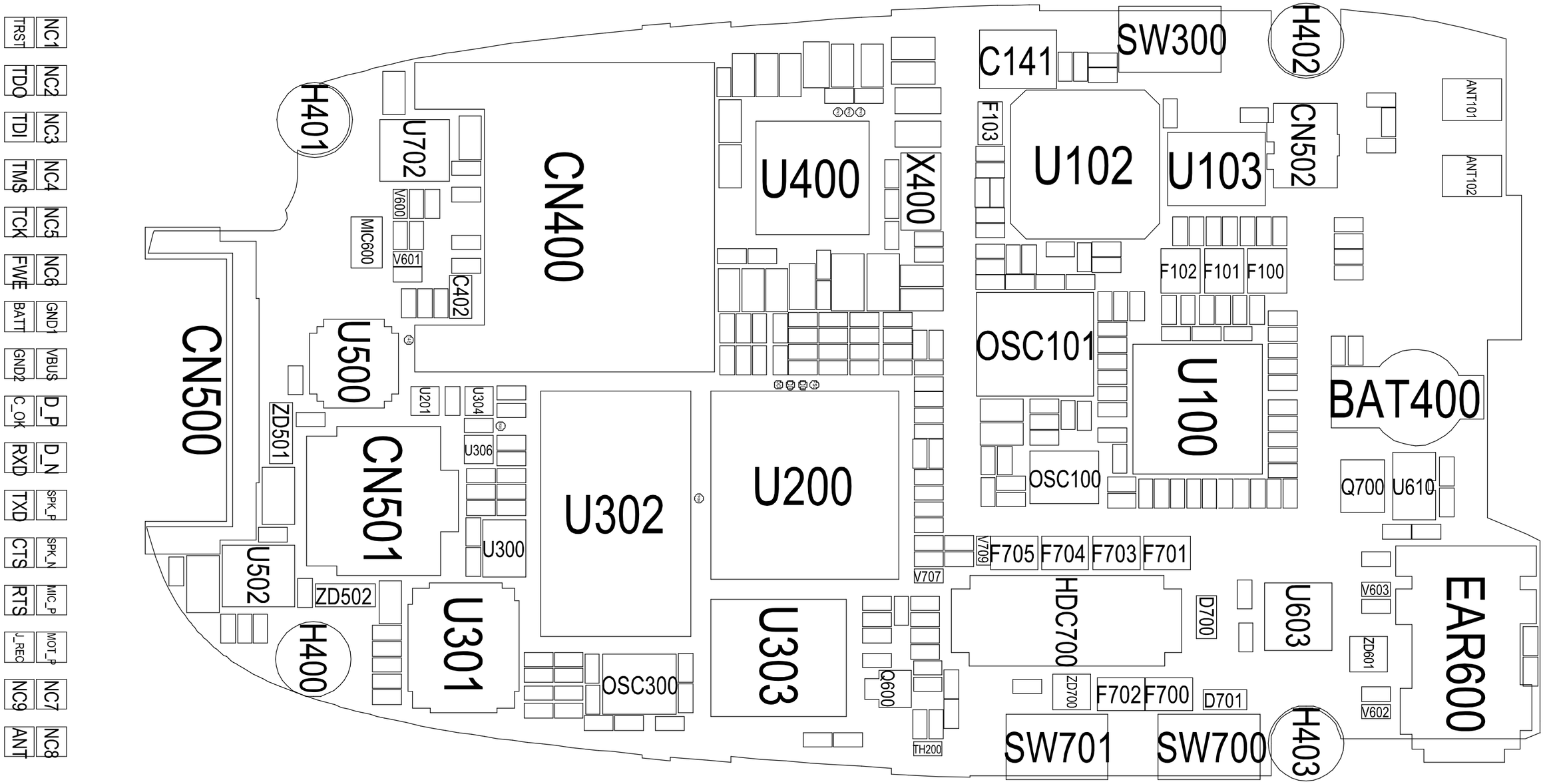


2. Base Band Solution Block Diagram

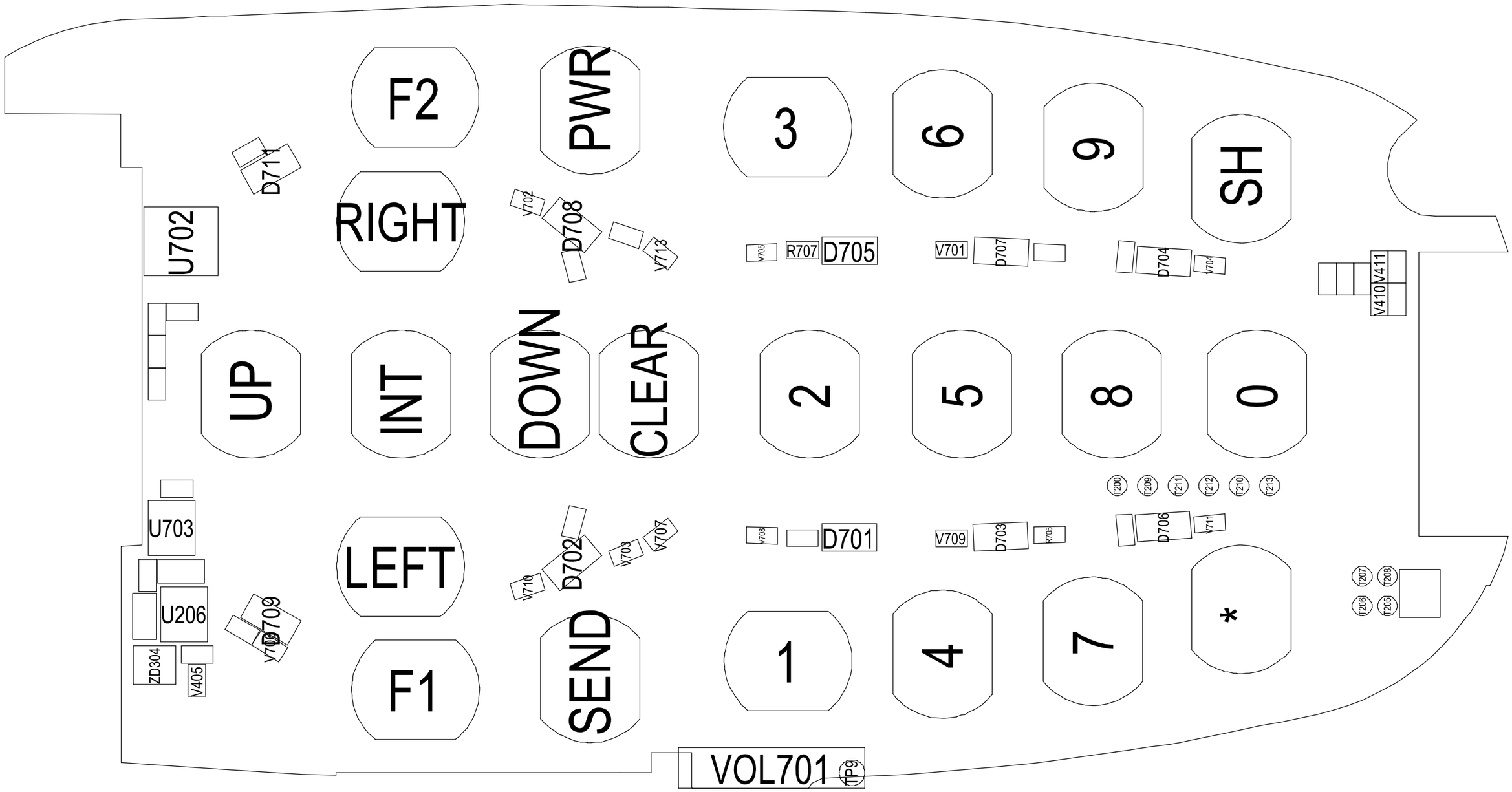


6. PCB Diagrams

1. Main PCB Top Diagram

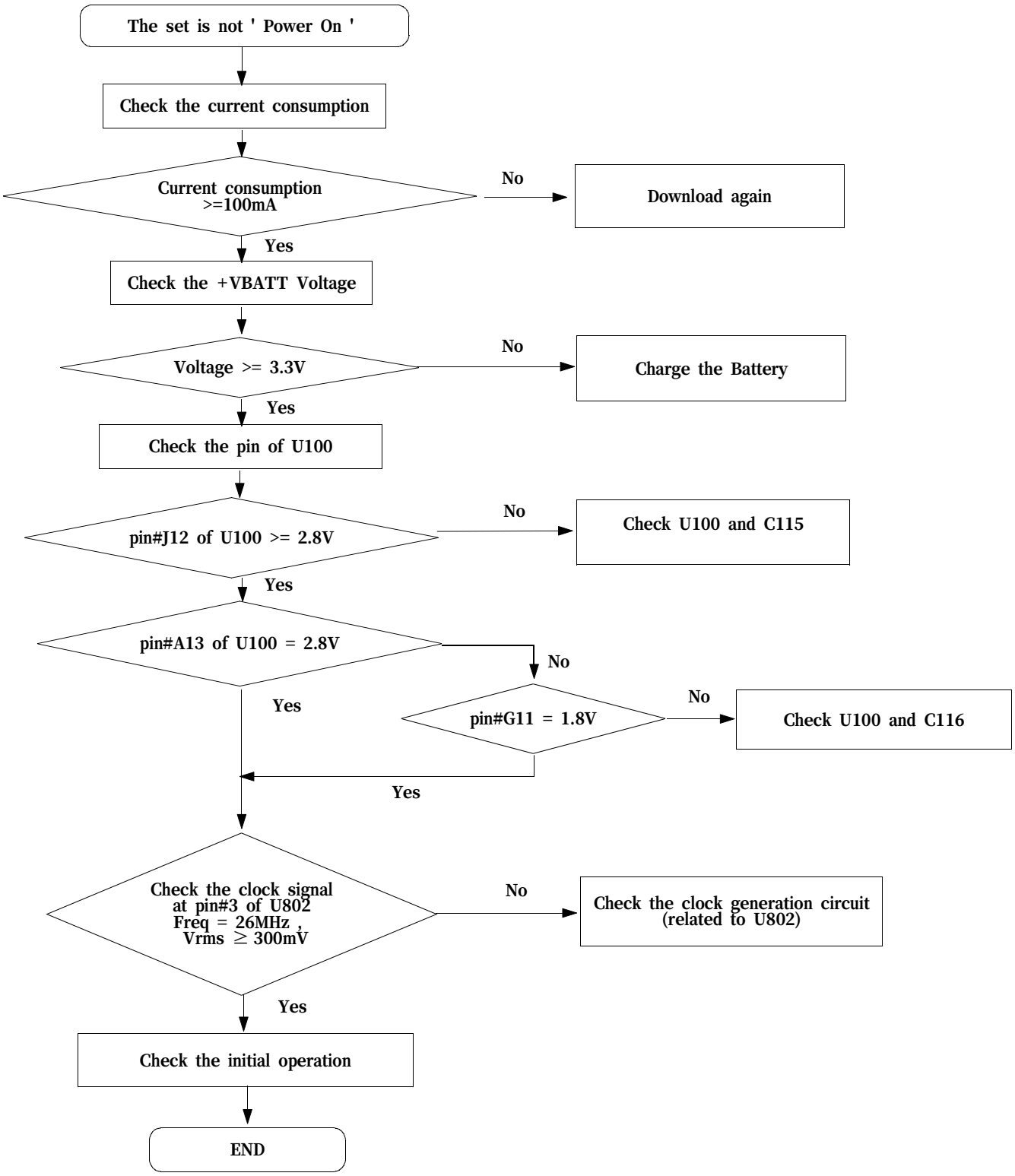


2. Main PCB Bottom Diagram

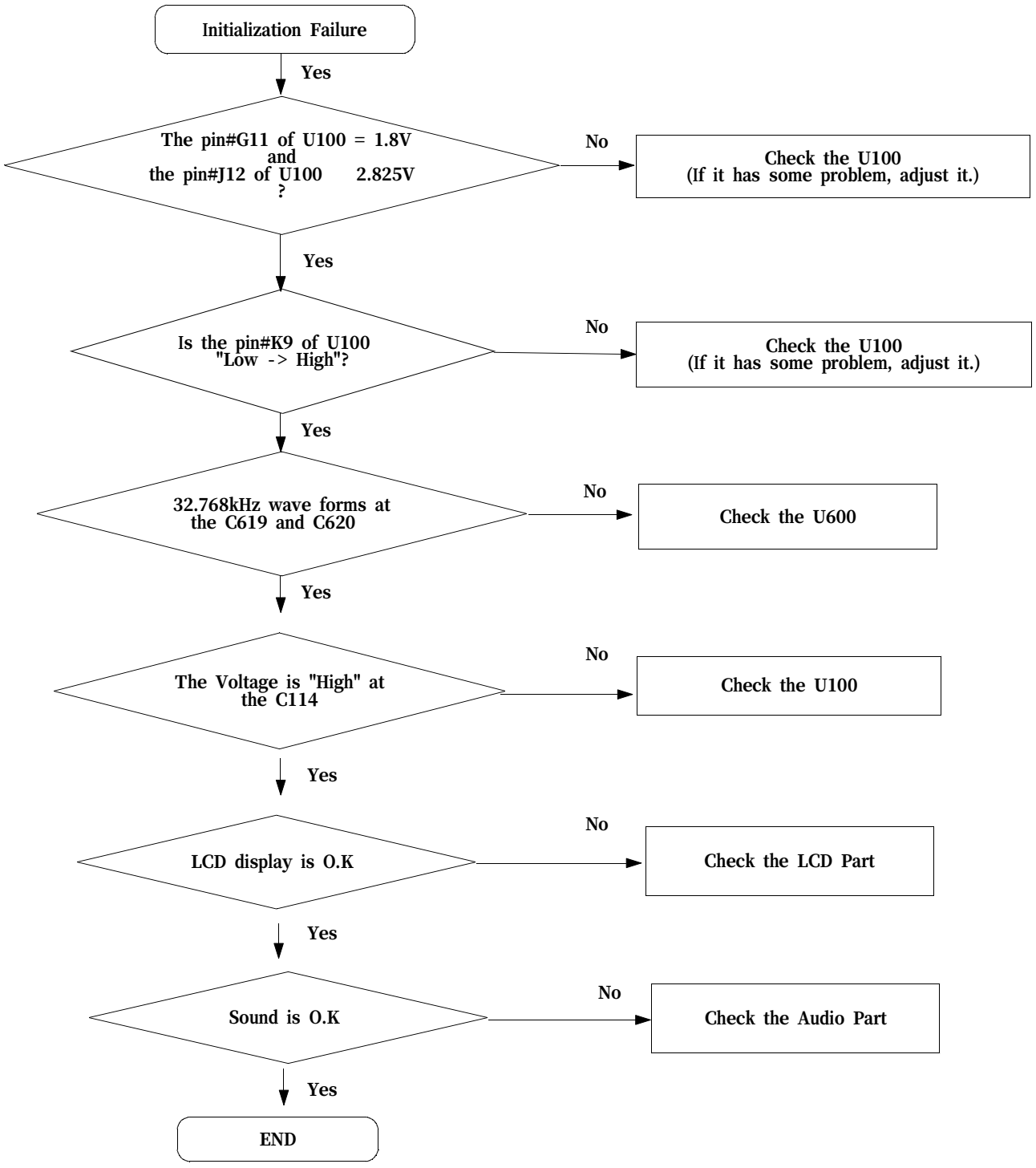


7. Flow Chart of Troubleshooting

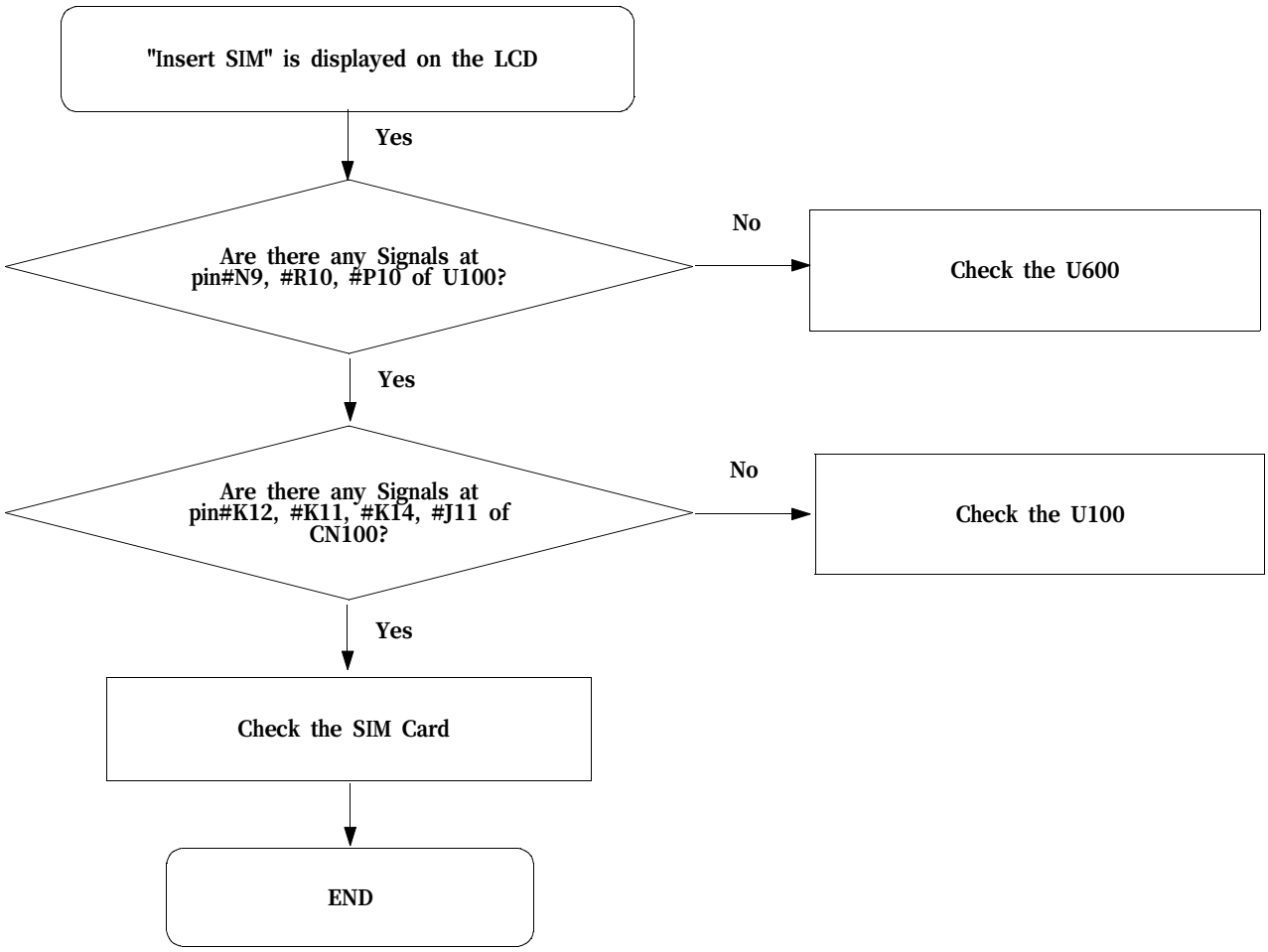
1. Power On



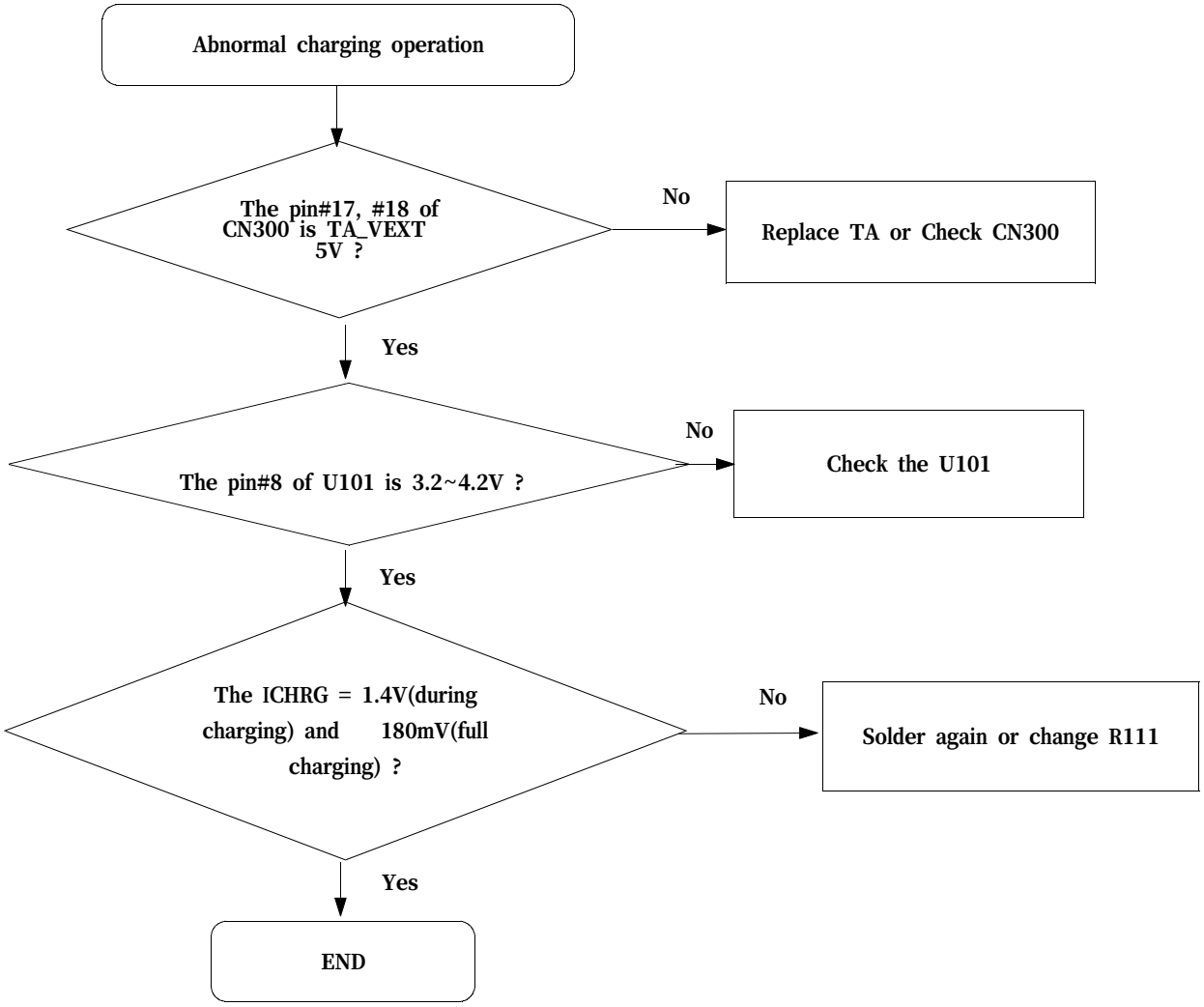
2. Initial

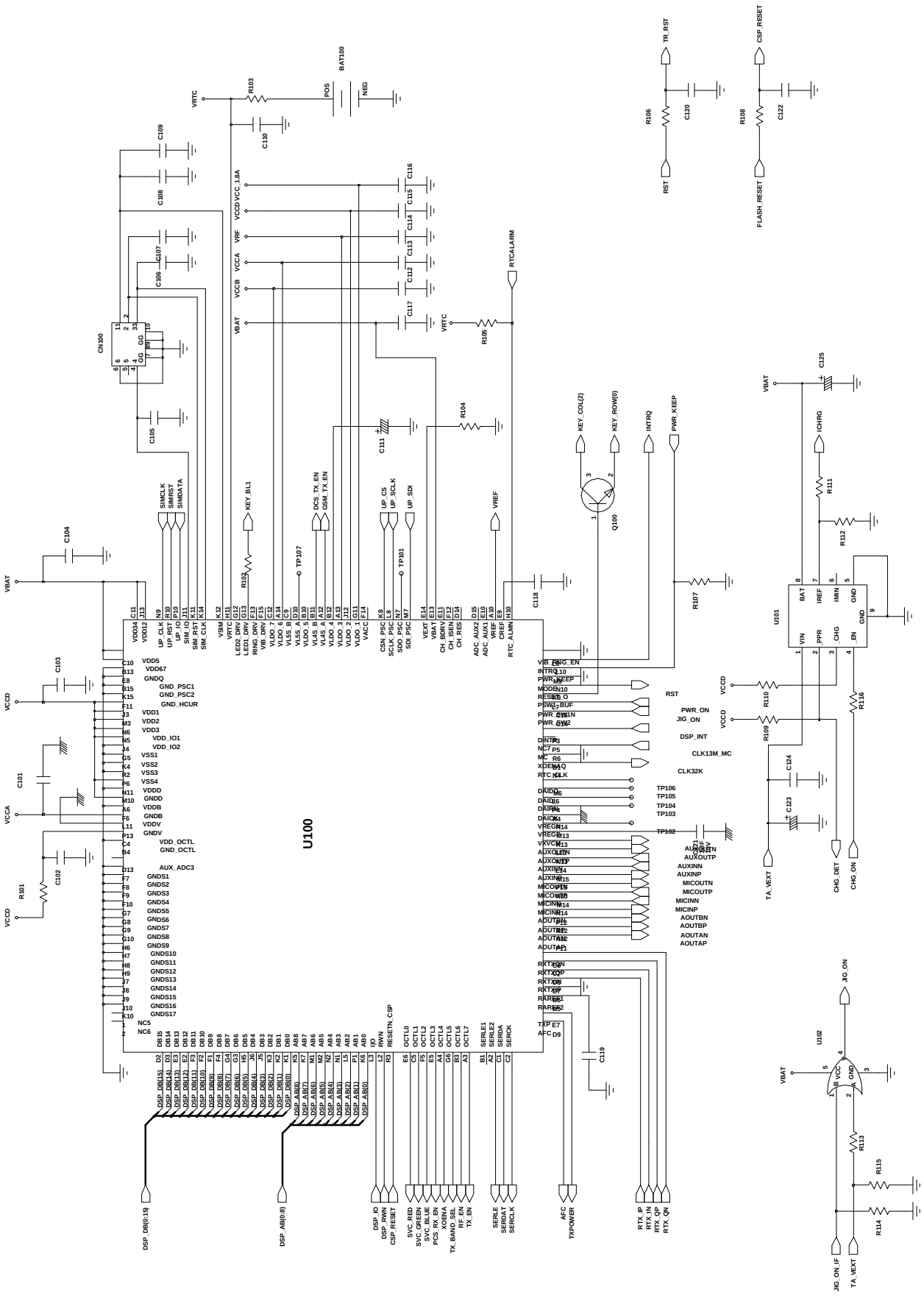


3. SIM Part

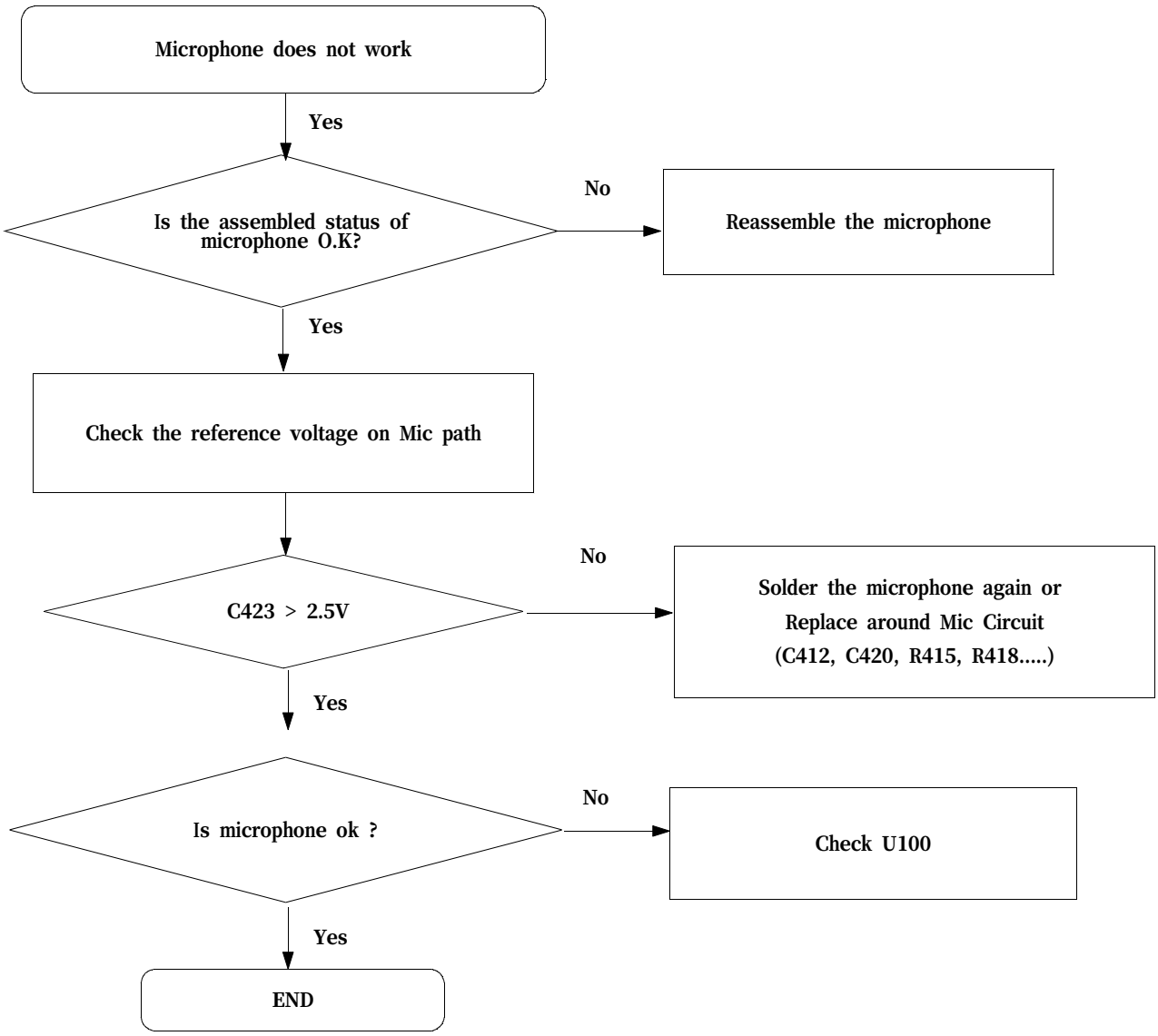


4. Charging Part

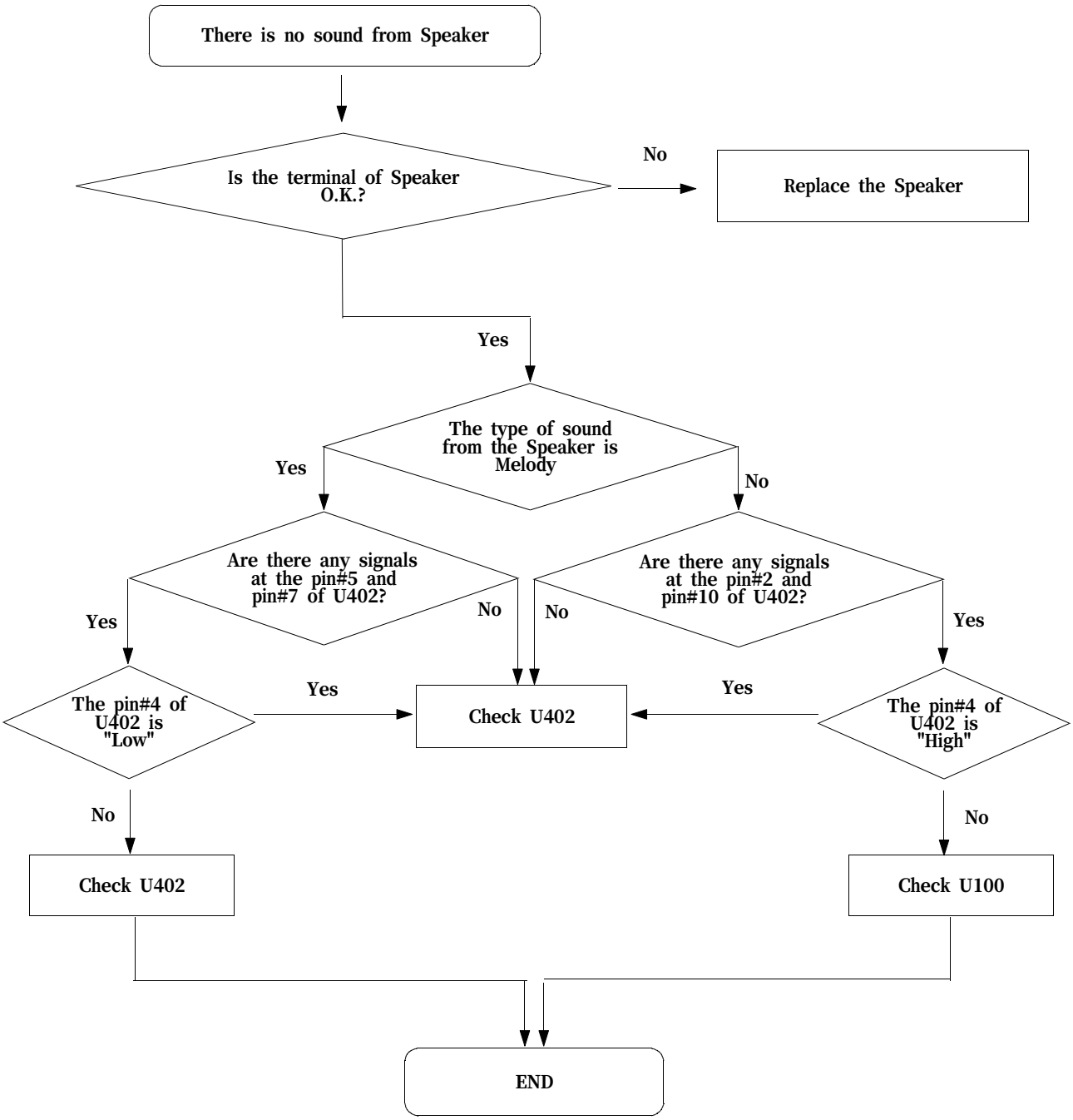


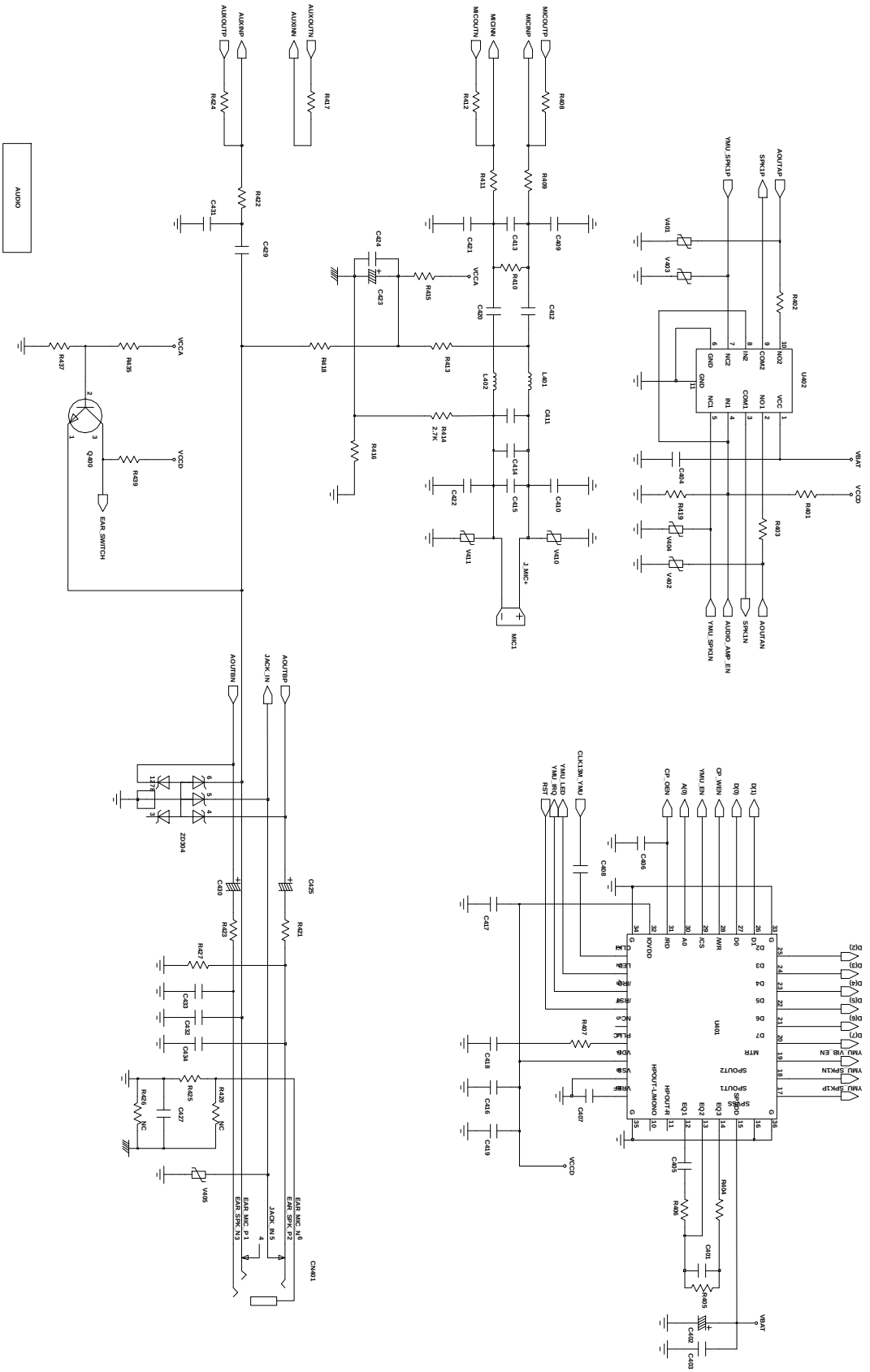


5. Microphone Part

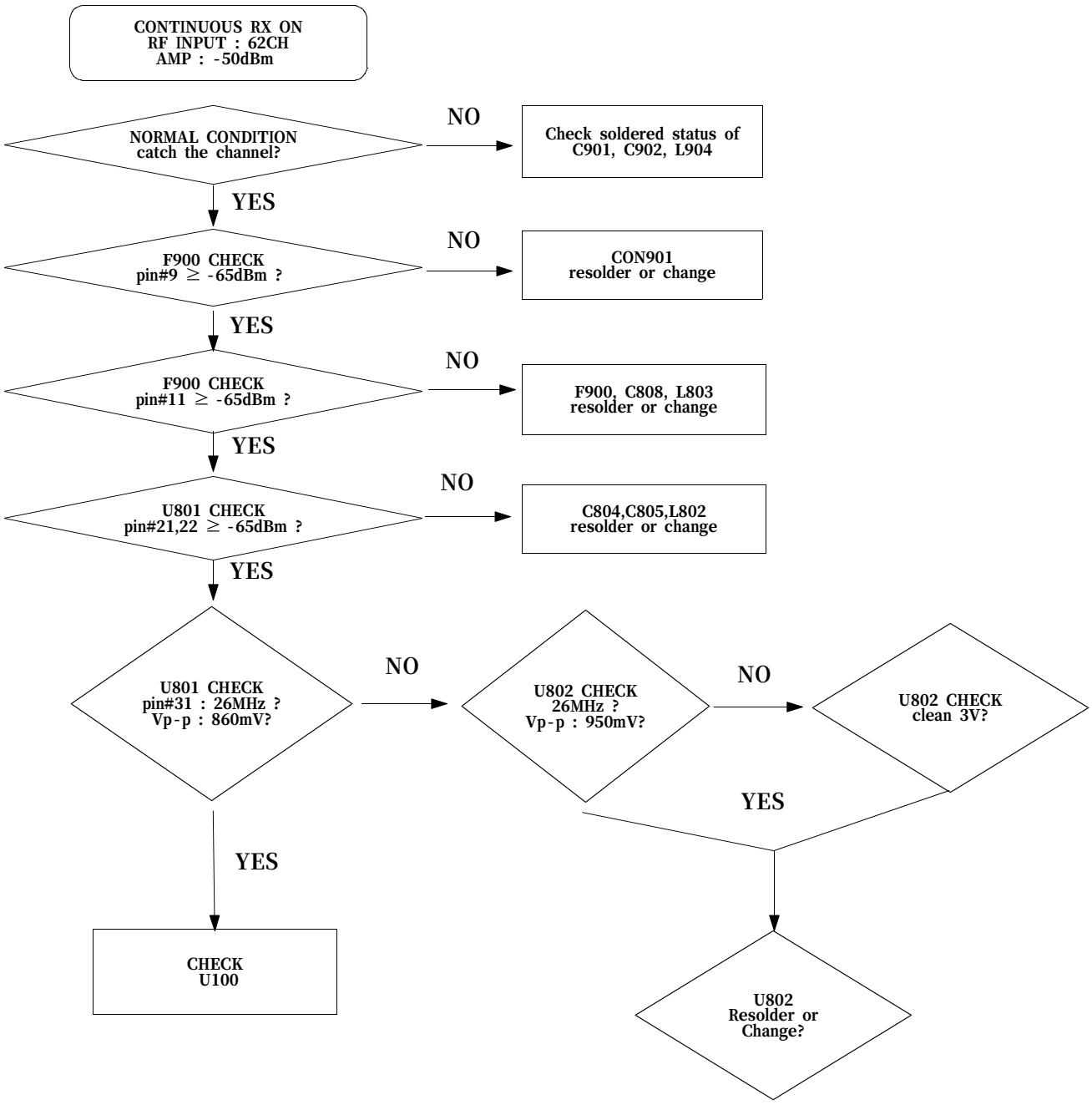


6. Speaker Part

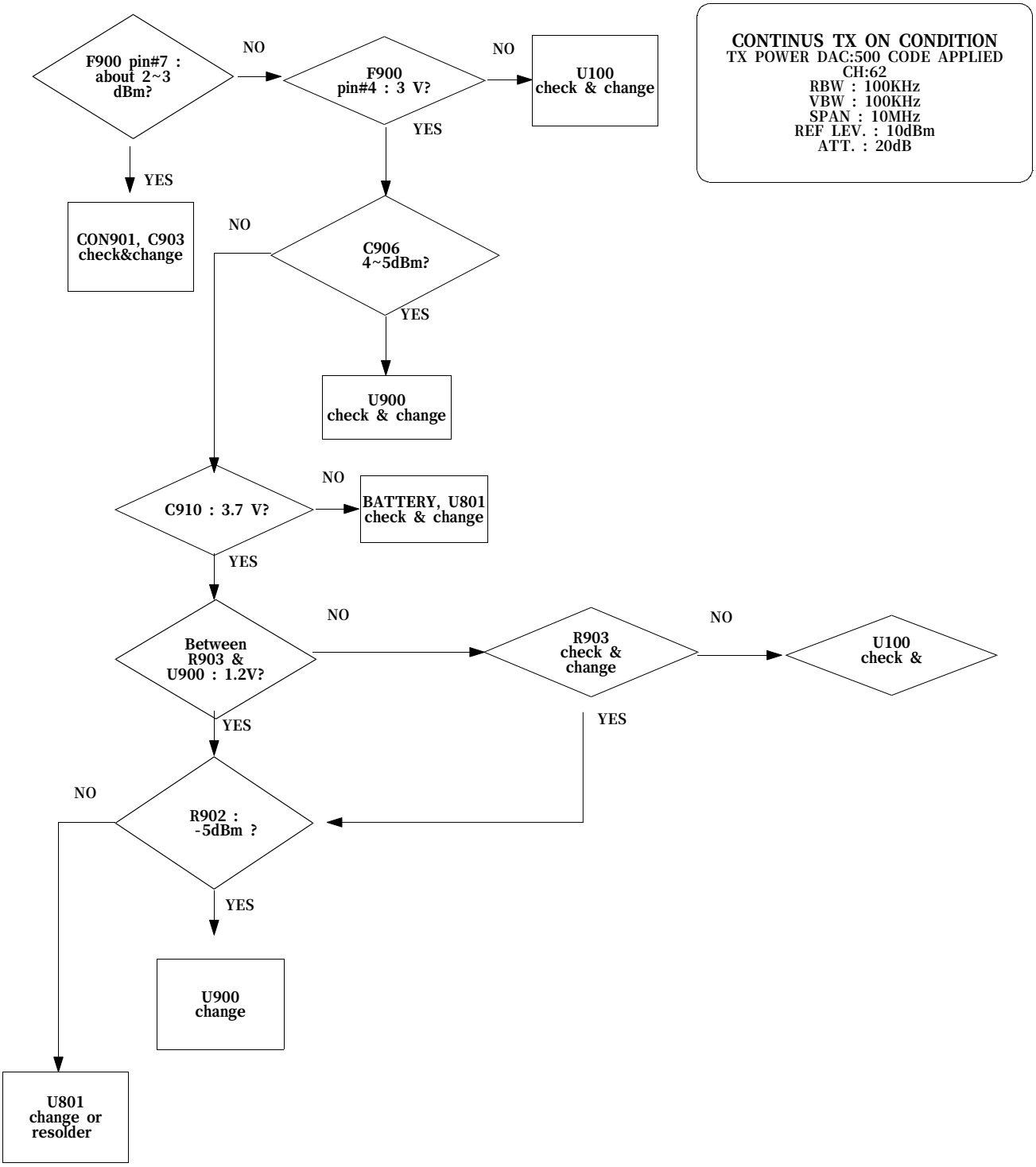




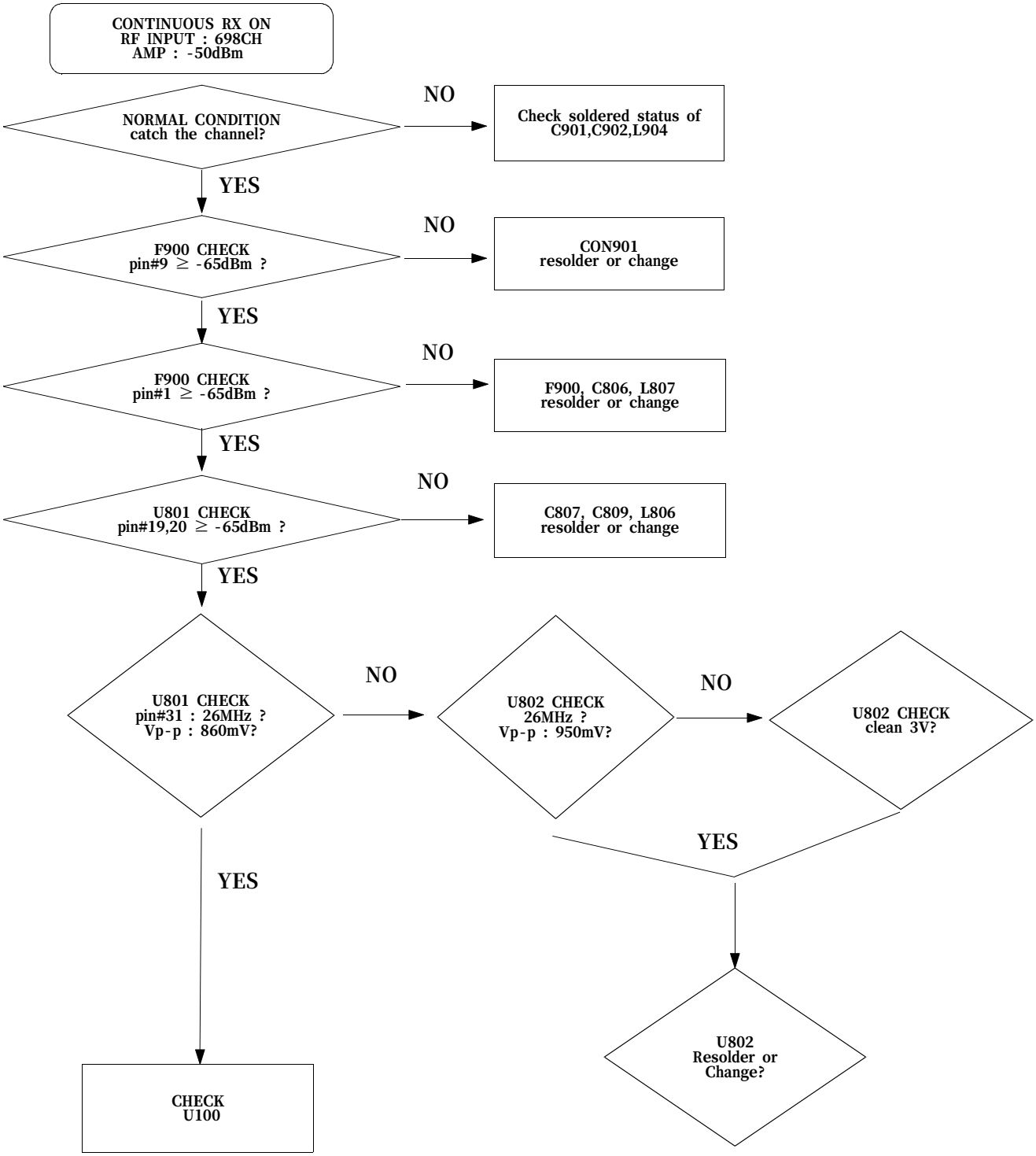
8. EGSM Reciever



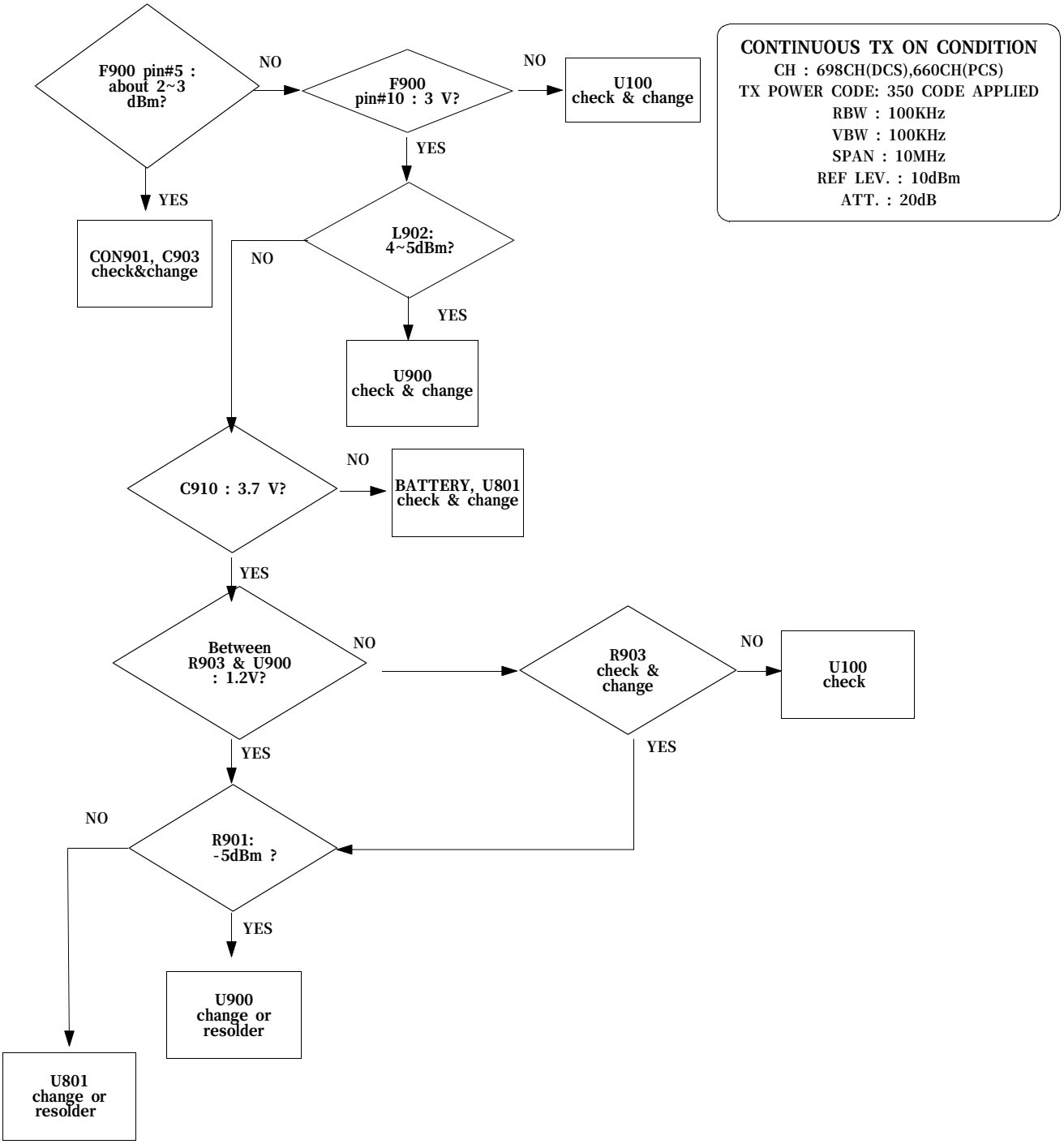
9. EGSM transmitter



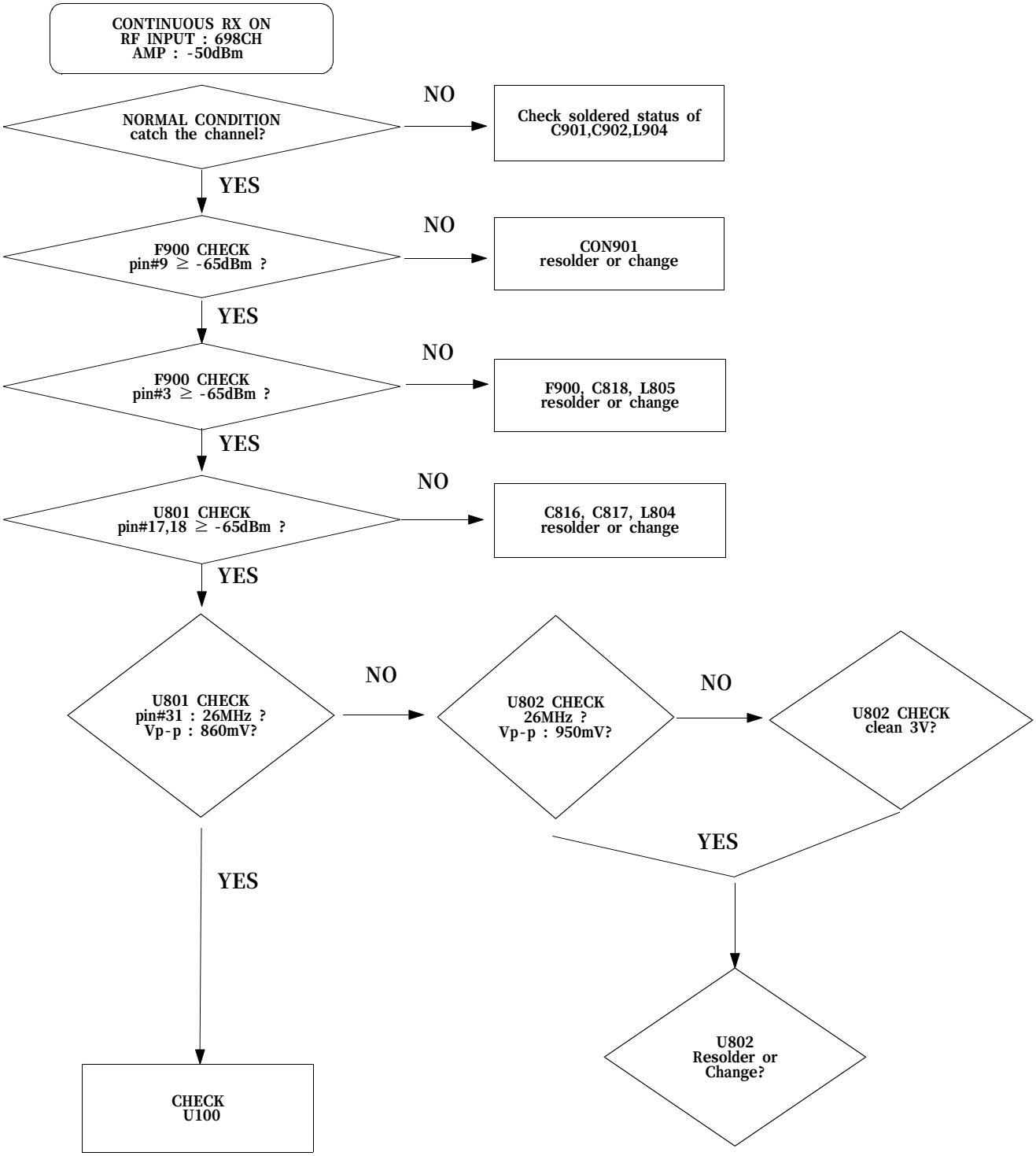
10. DCS Receiver



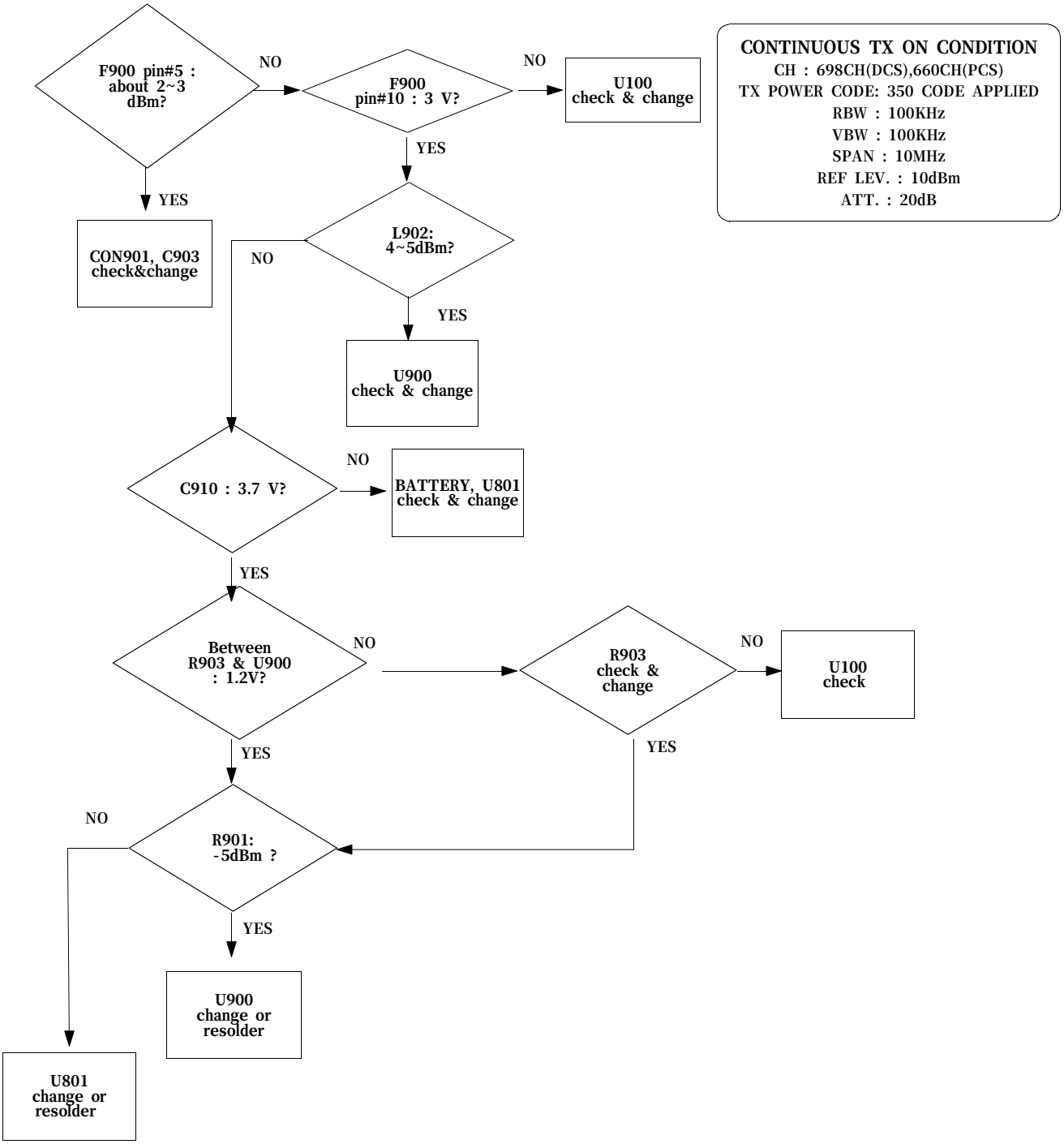
11. DCS transmitter

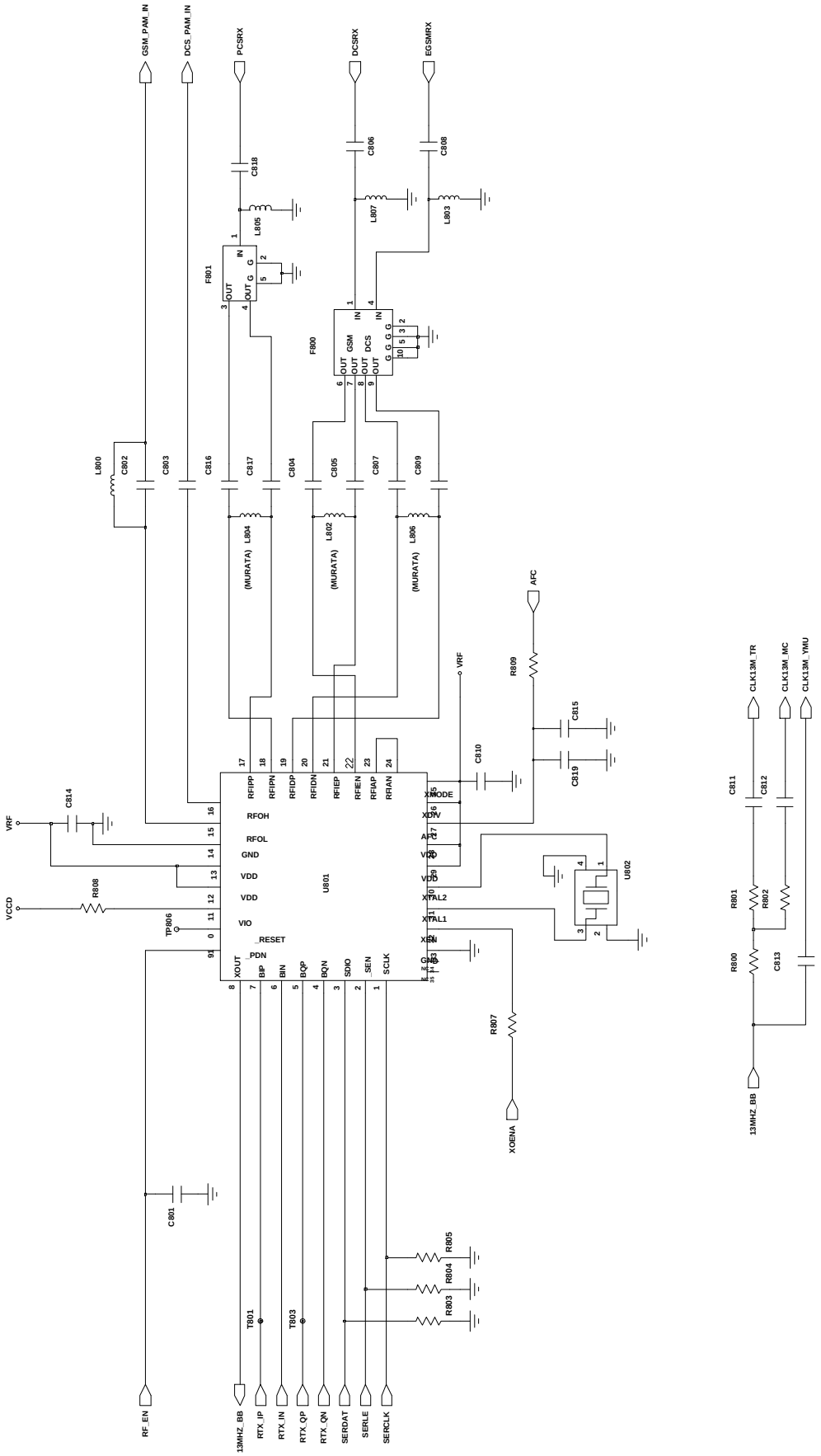


12. PCS Receiver



13. PCS transmitter





1) Toyocom & KSS to be reviewed
2) Toyocom samples to be reviewed starting 5/26/04 ; to coordinate with Toyocom on behalf of Mr.Park/Samsung