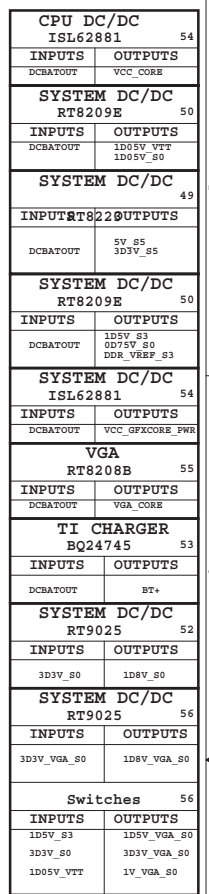


Project code: 91.4NI01.001 (JE43-CP)



PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1 (HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

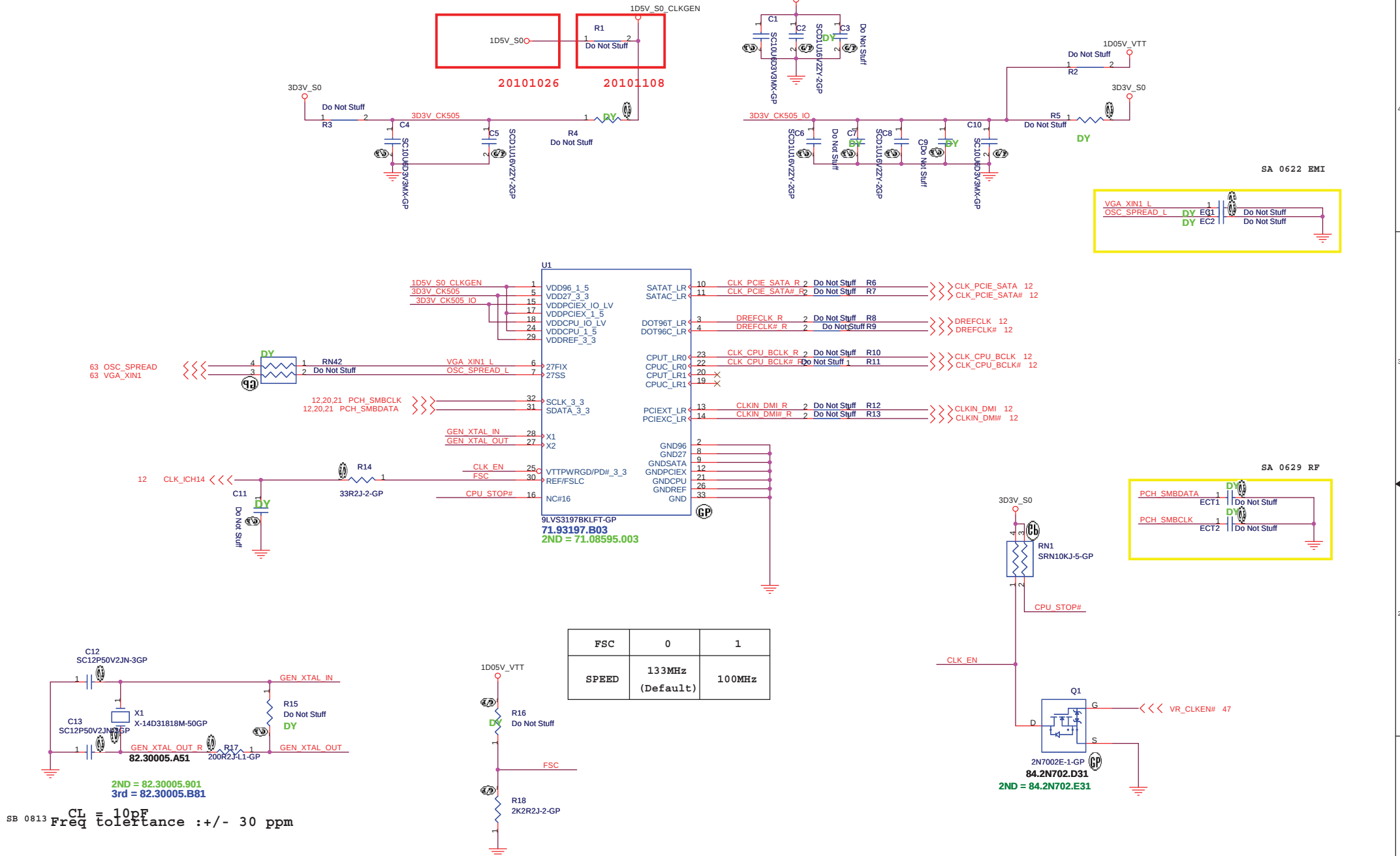
PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

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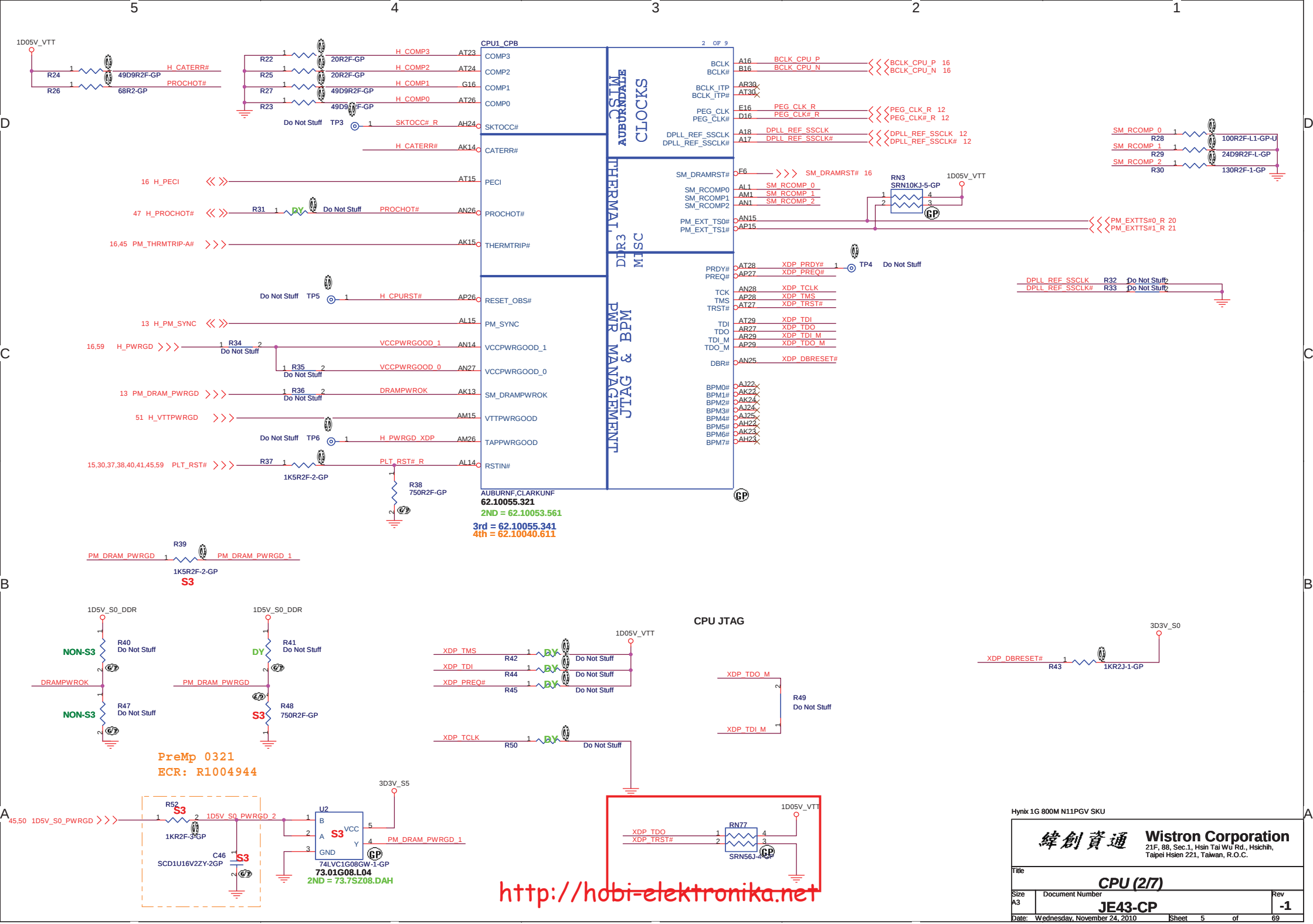
Hynix 1G 800M N11PGV SKU

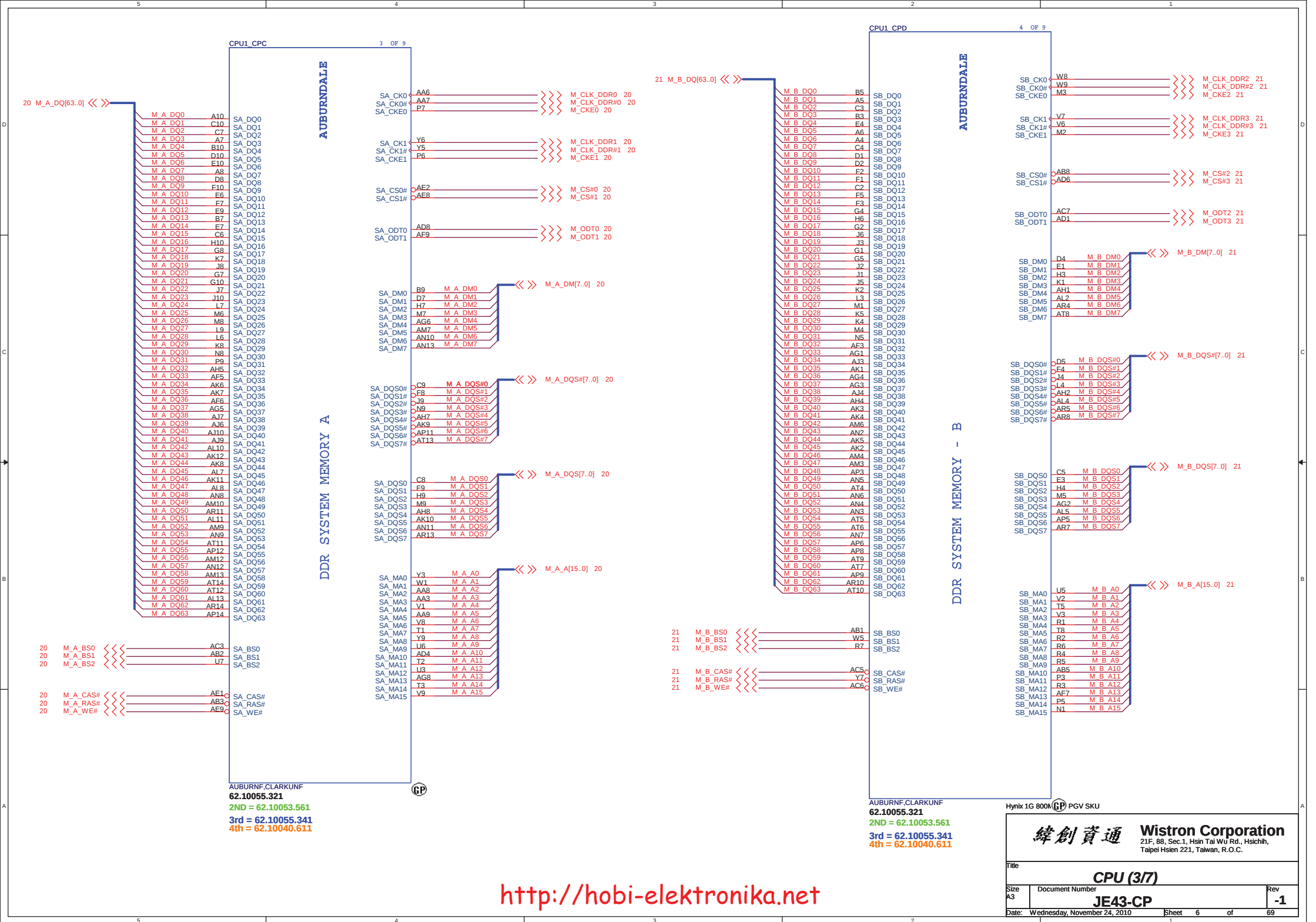
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Title			
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Size A3	Document Number		Rev
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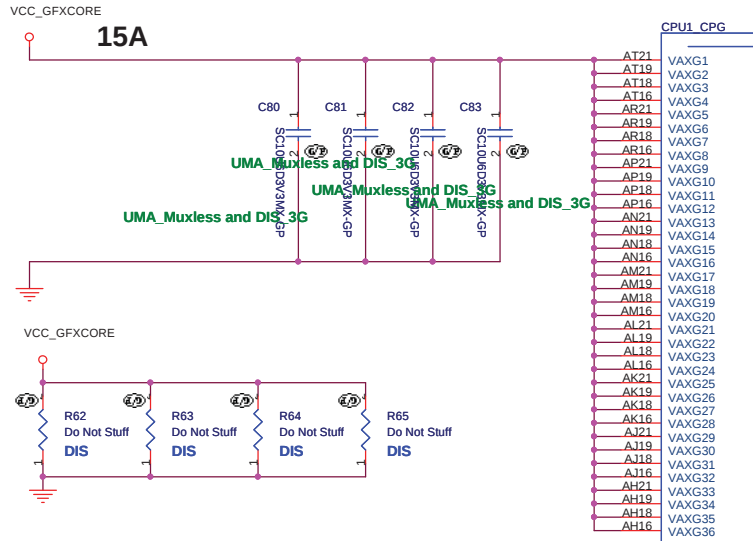


Hynix 1G 800M N11PGV SKU

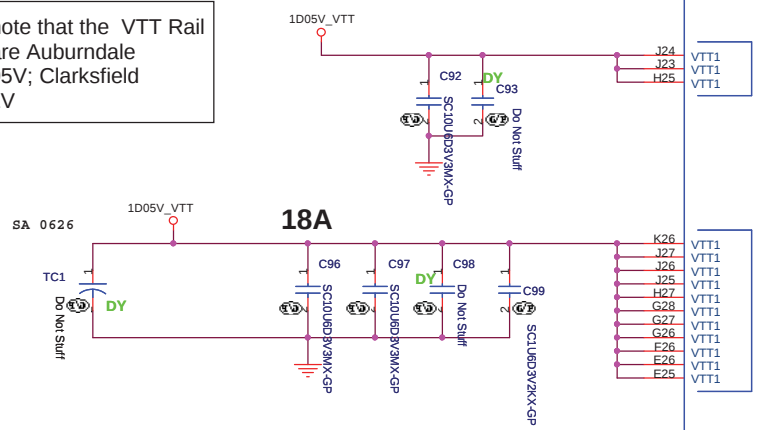
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.







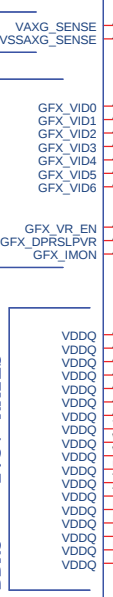
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



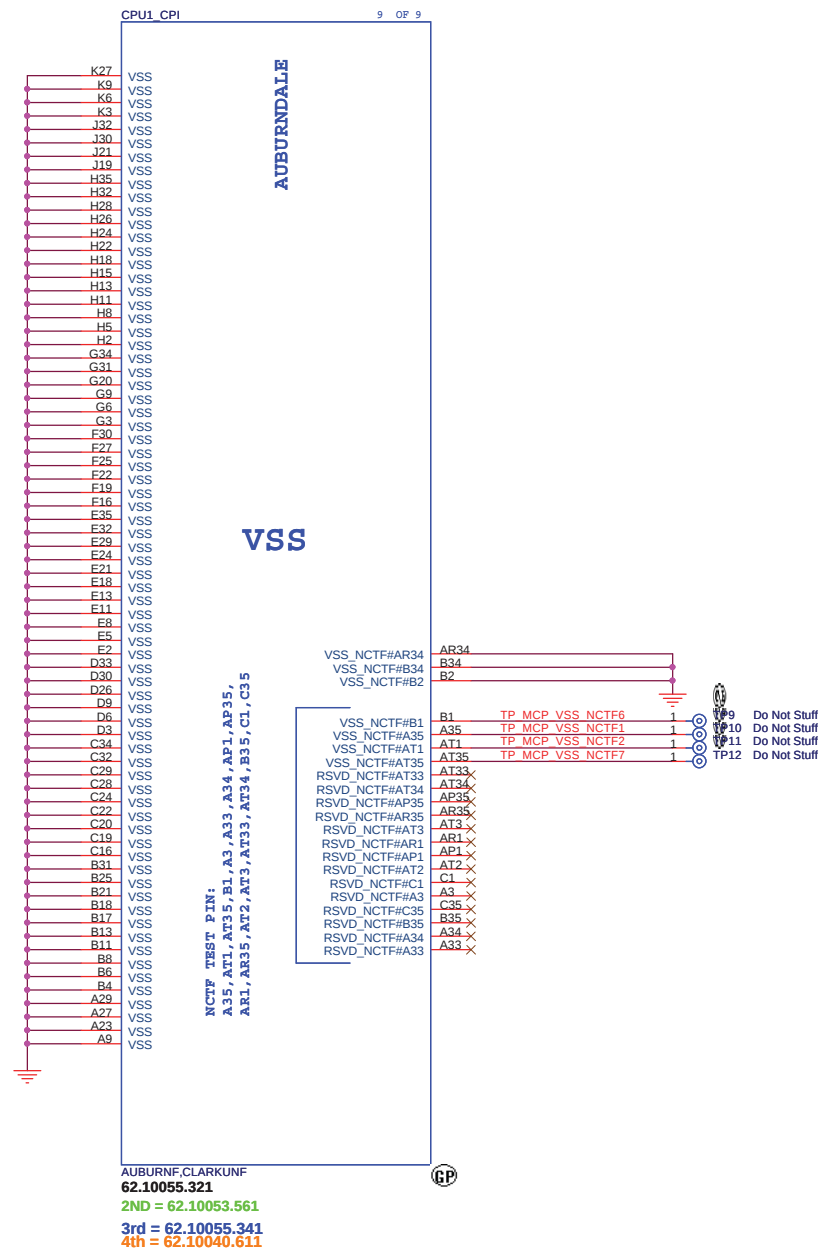
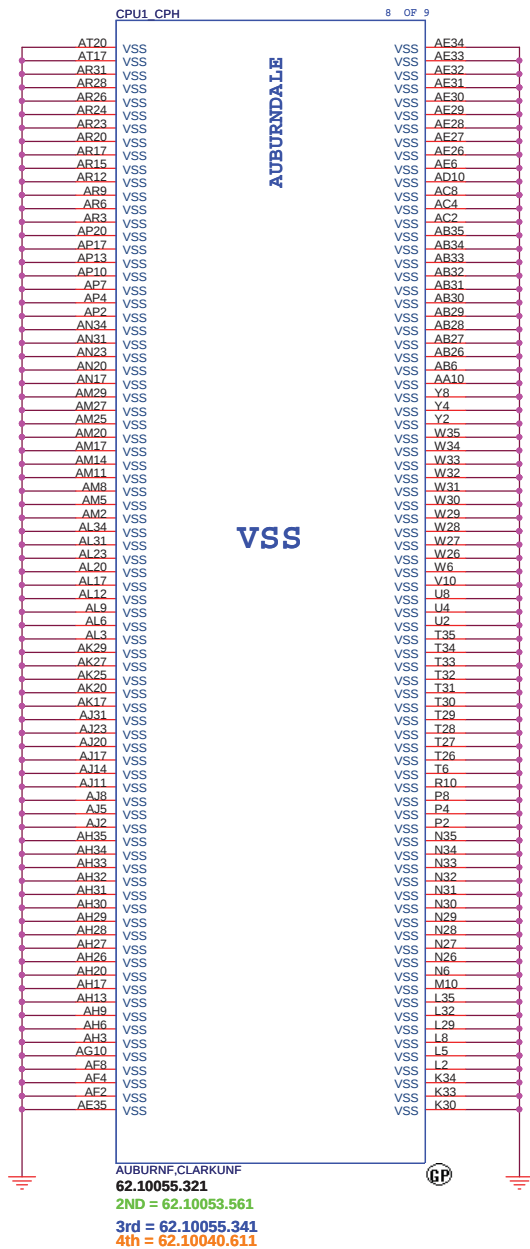
AUBURN, CLARKUNF
62.10055.321
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10040.611

POWER

GRAPHICS



Hynix 1G 800M N11PGV SKU



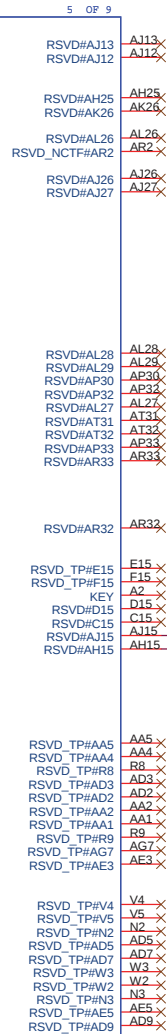
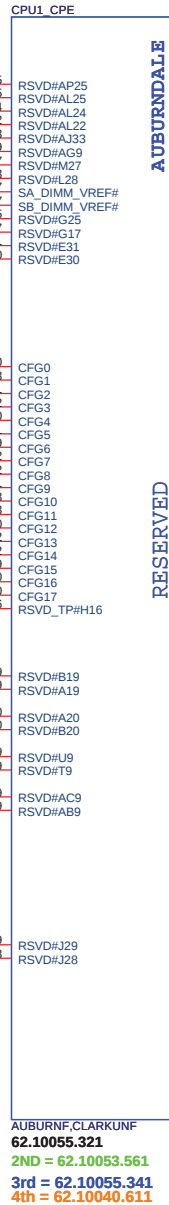
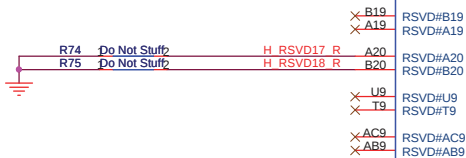
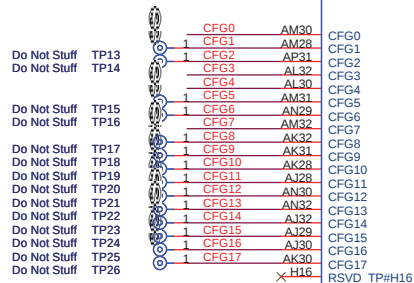
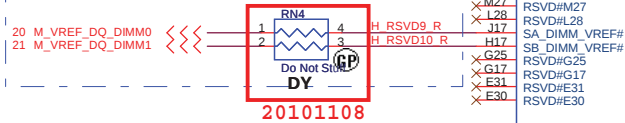
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CPU (6/7)		
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SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor



1130 -SC

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

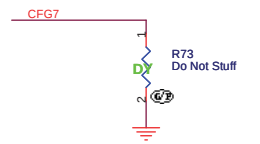
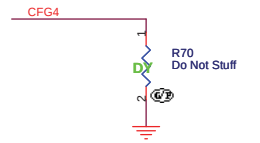
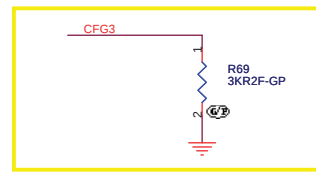
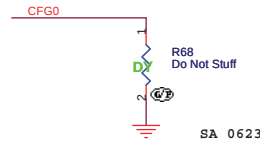
Processor Strapping

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

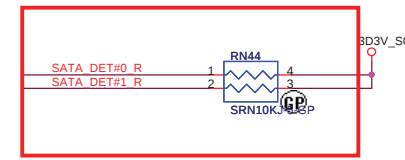
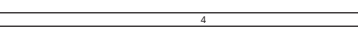
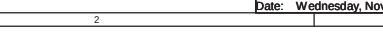
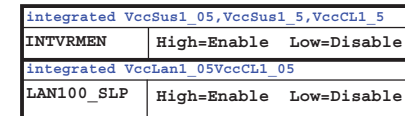


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LAN

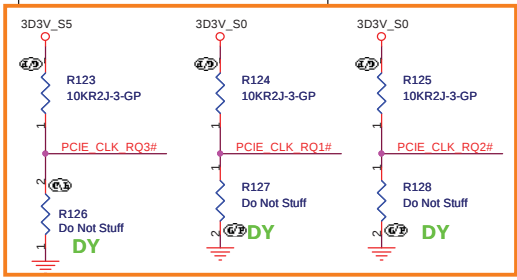
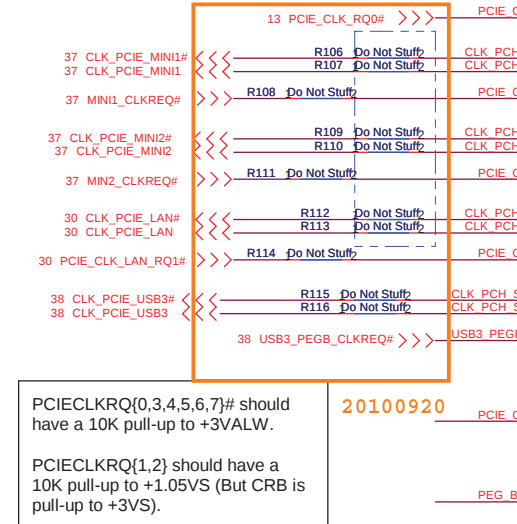
MINICARD1

MINICARD2

USB3.0

0721

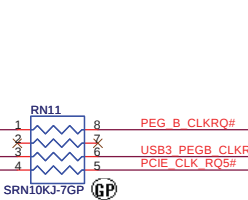
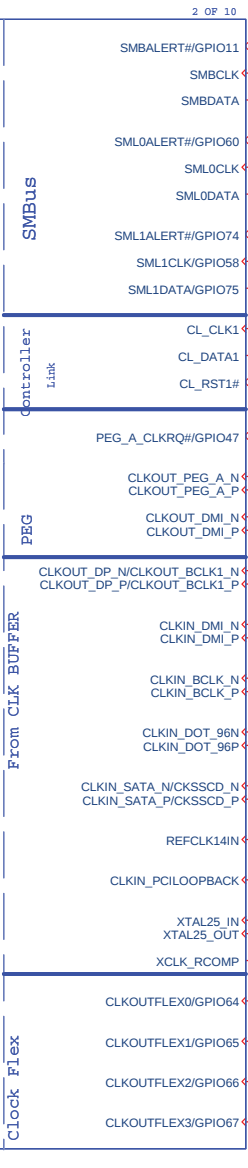
1.R108 2.R111 3.R114
the three resistors should be moated



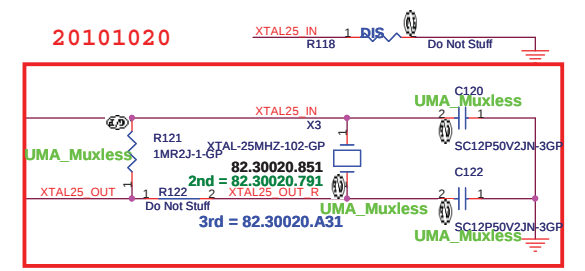
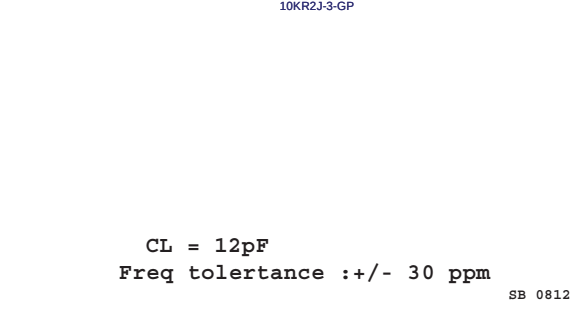
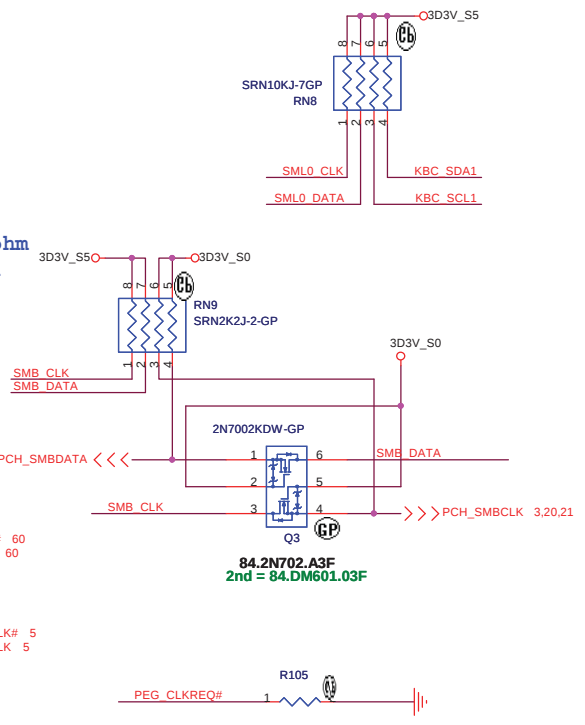
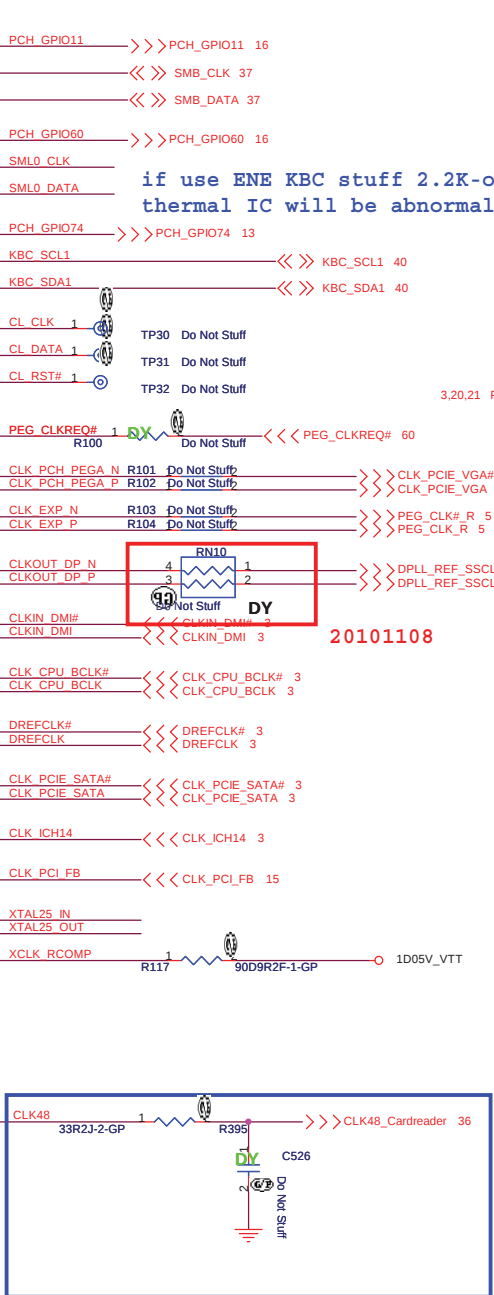
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PCH1_CPB 2 OF 10

PCI-E*



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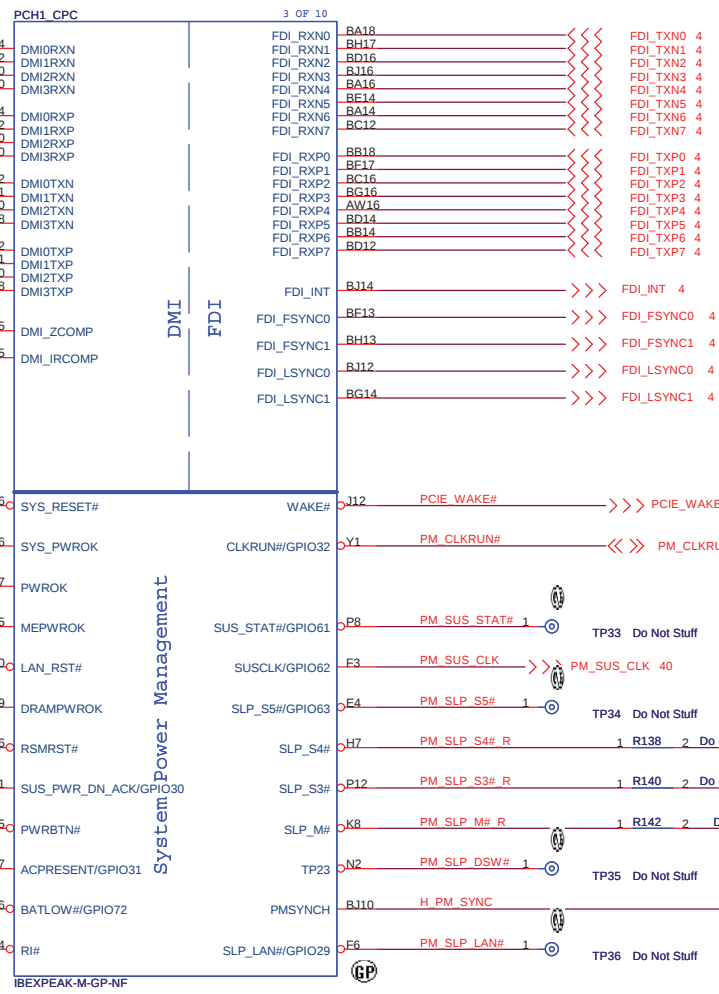
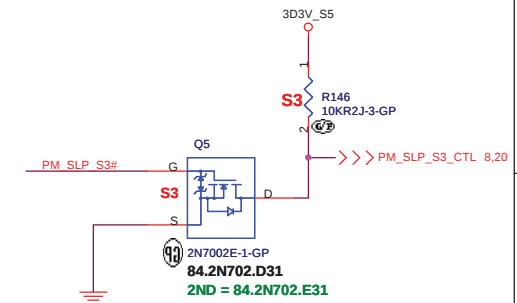
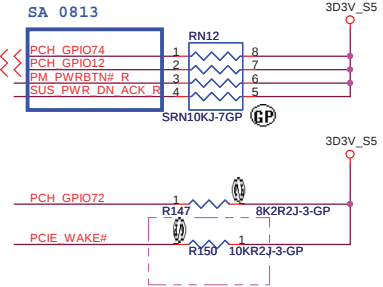
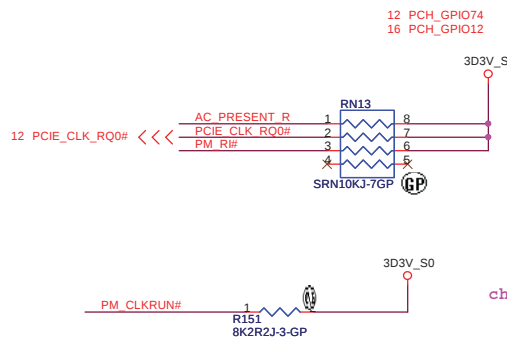
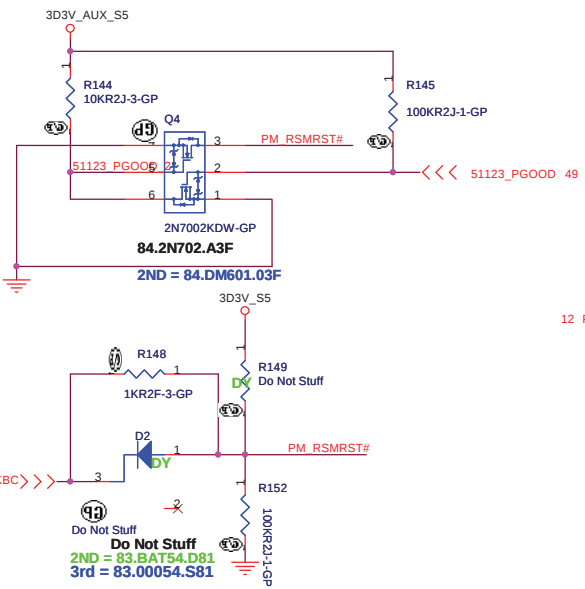
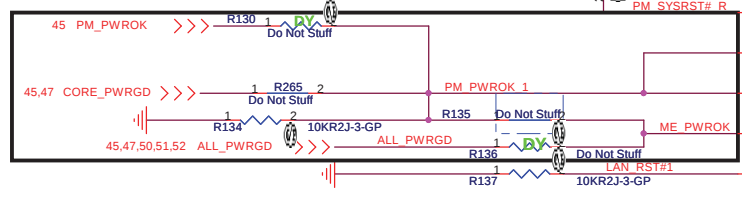
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PCH (2/9)

Size A3 Document Number JE43-CP Rev -1

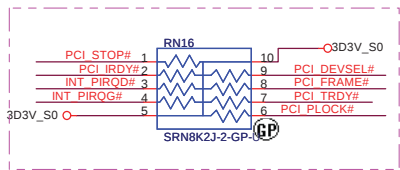
Date: Wednesday, November 24, 2010 Sheet 12 of 69

0804 SA
1.cause of thermal sensor
2.solution by JM31-CP

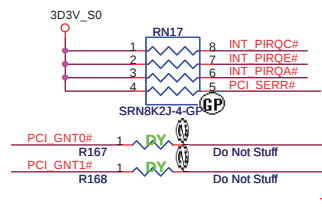
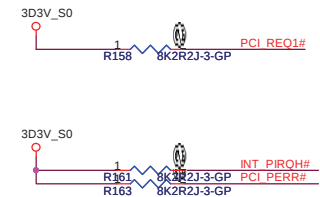
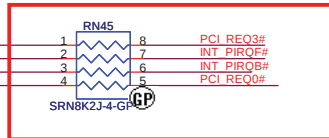


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These pins are left as NC,
because the function is disable.

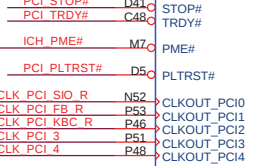
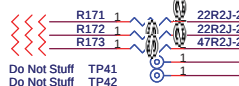


PCH strapping

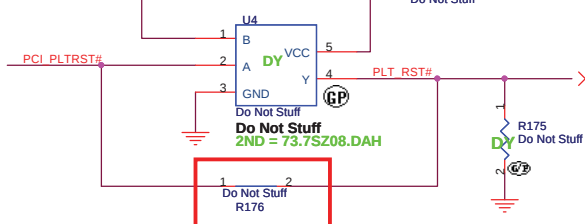
BOOT BIOS Strap		
GNT#0	GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
floating	0	PCI
floating	floating	SPI (Default)

PCI_GNT#1	
1	Default (internal pull-up)
0	Configures DMI for ESI compatible operation (Not for Mobile platform)

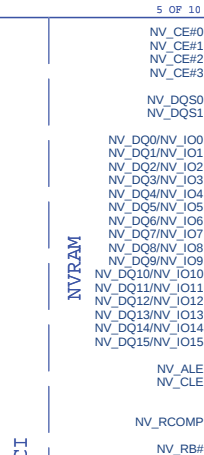
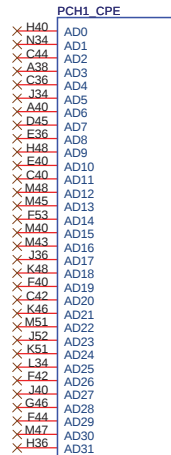
41 CLK_FWH
42 CLK_PCI_FB
40 CLK_PCI_KBC



Near R439
PLT_RST# 5,30,37,38,40,41,45,59



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PCI

USB

IBEXPEAK-M-GP-NF

These pins are left as NC,
because the function is disable.



PCH strapping

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PCH strapping

NV_CLE	DMI termination voltage
floating	internal pull-up

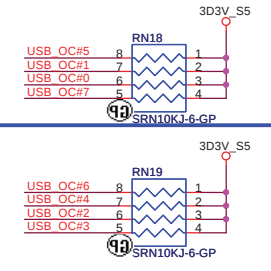
NV_ALE	
1	Enable Anti-Theft Tech
floating	Disable (internal pull-down)

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

USB

Pair	Device
0	I/O USB2.0
1	USB2.0
2	NC
3	MINICARD1 (WLAN)
4	WECAM
5	NC
6	NC
7	NC
8	3G SIM Card
9	USB 2.0
10	NC
11	Blue Tooth
12	MINIC2 (3G)
13	Cardreader

0806 SA for GPIO_table



SA 0813

Hynix 1G 800M N11GPV SKU

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (5/9)

Size A3

Document Number

JE43-CP

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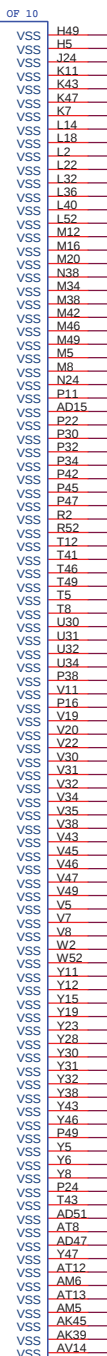
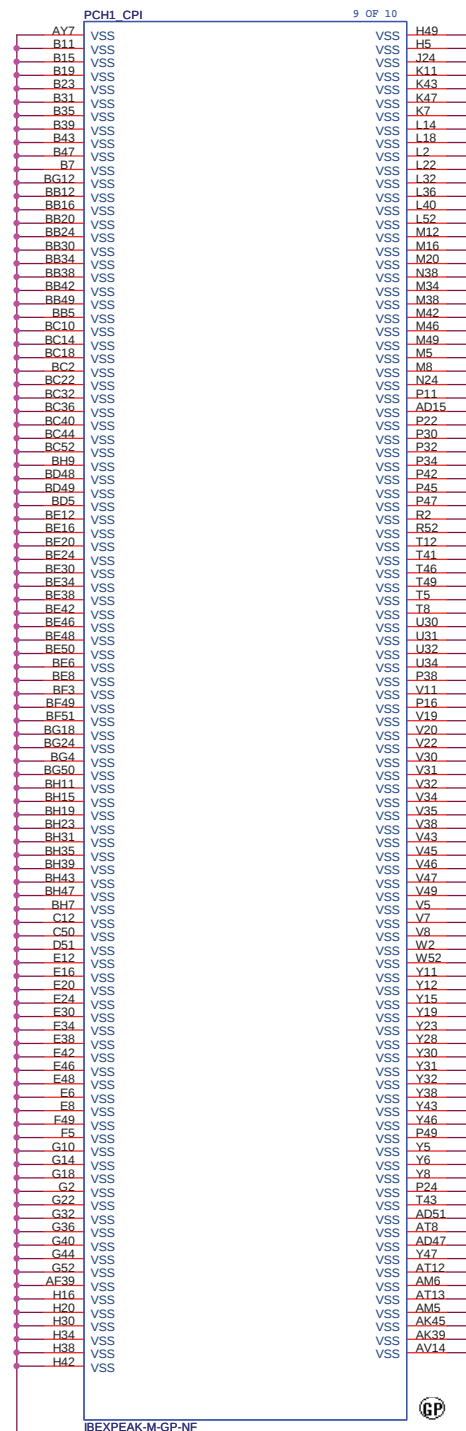
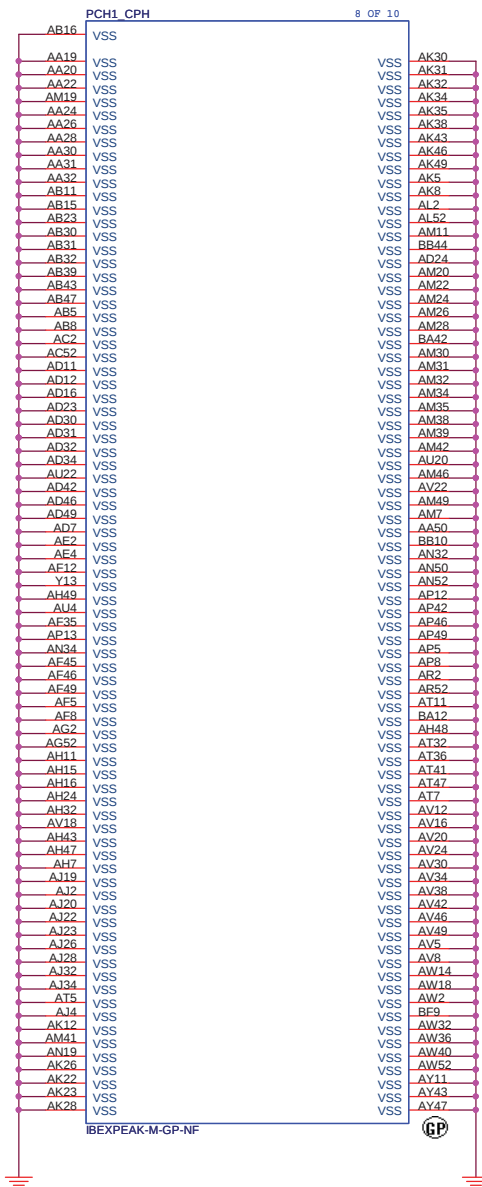
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Rev

-1

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

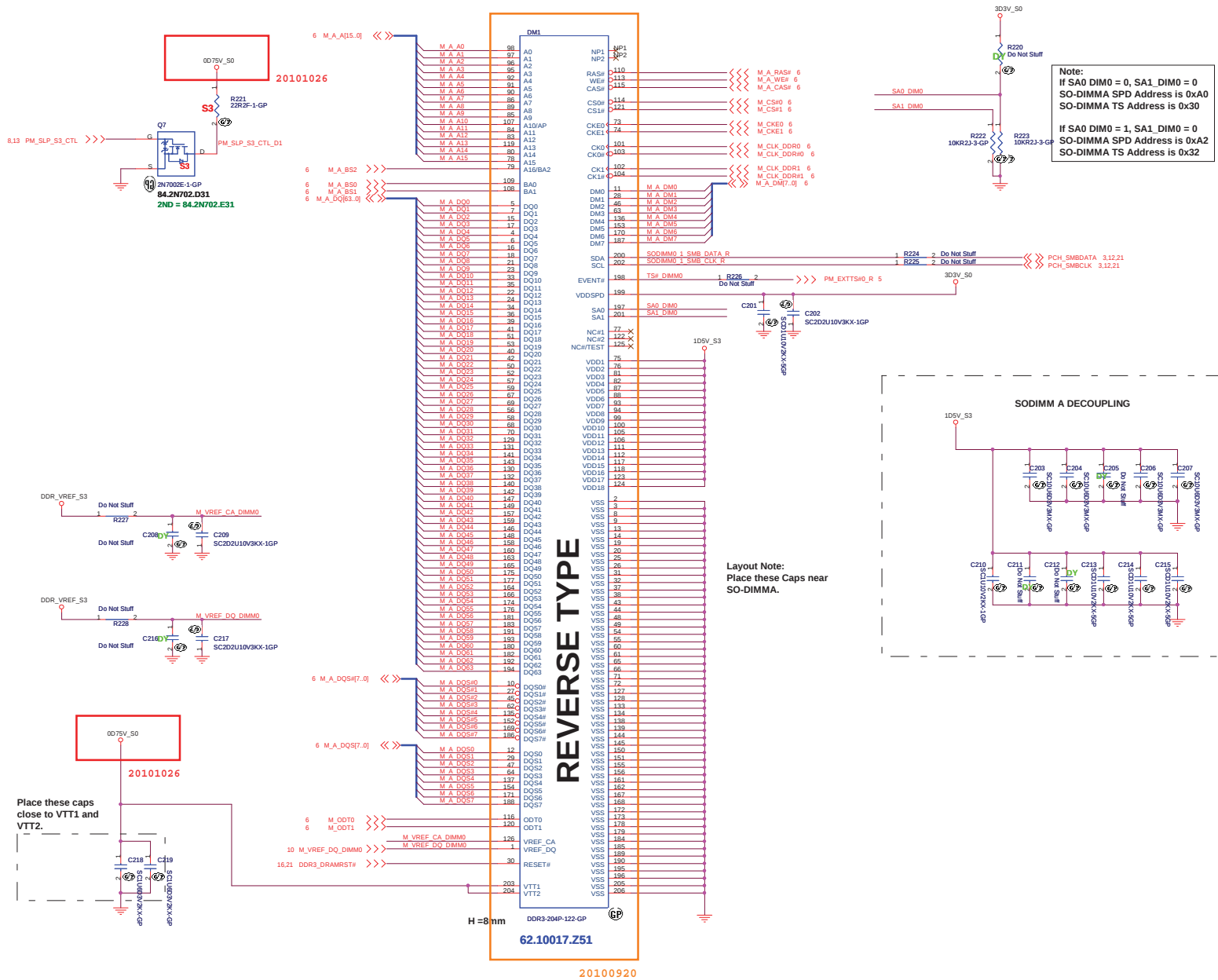




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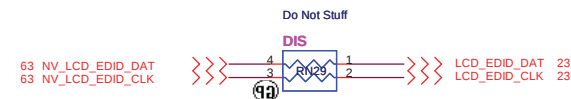
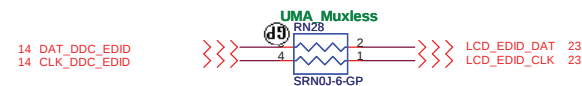
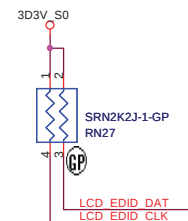
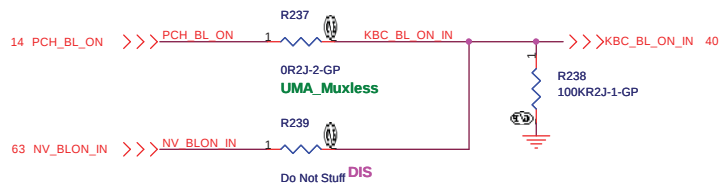
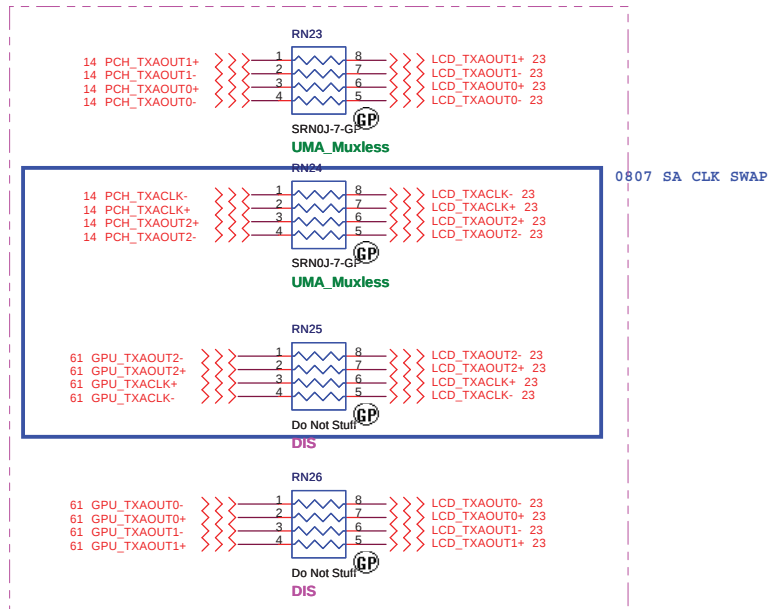
Hynix 1G 800M N11PGV SKU

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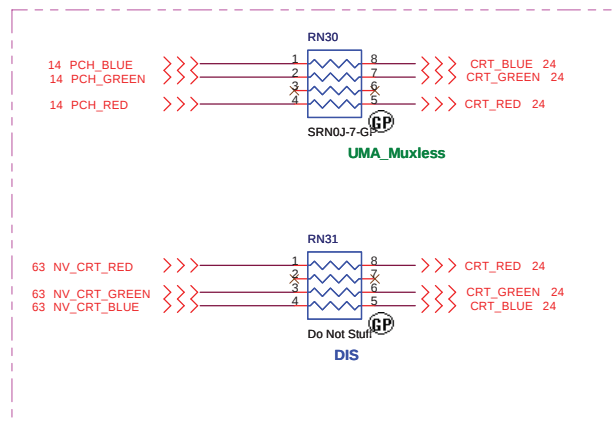


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LCD



CRT

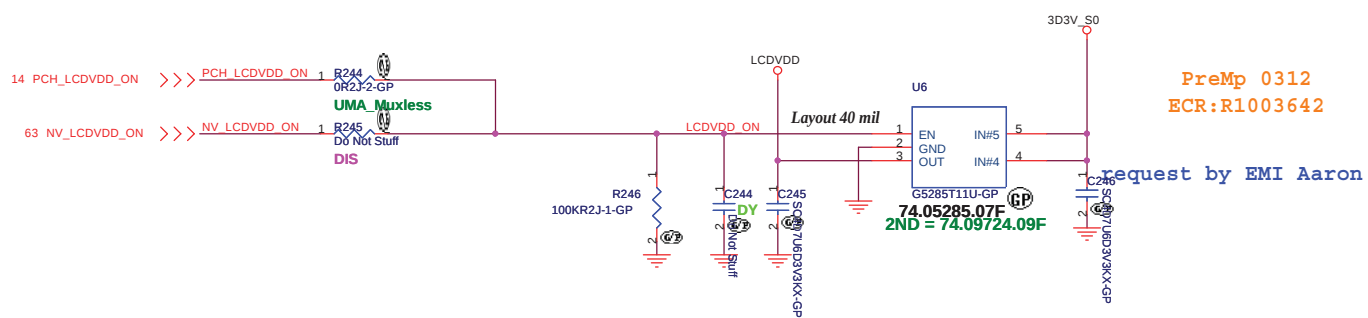
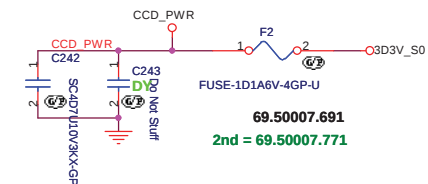
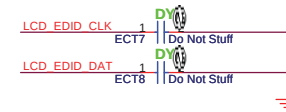
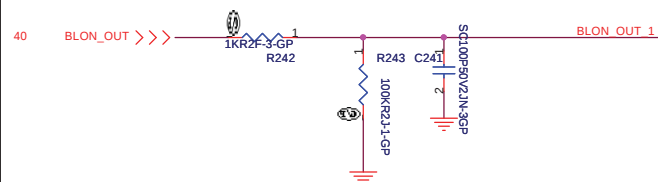
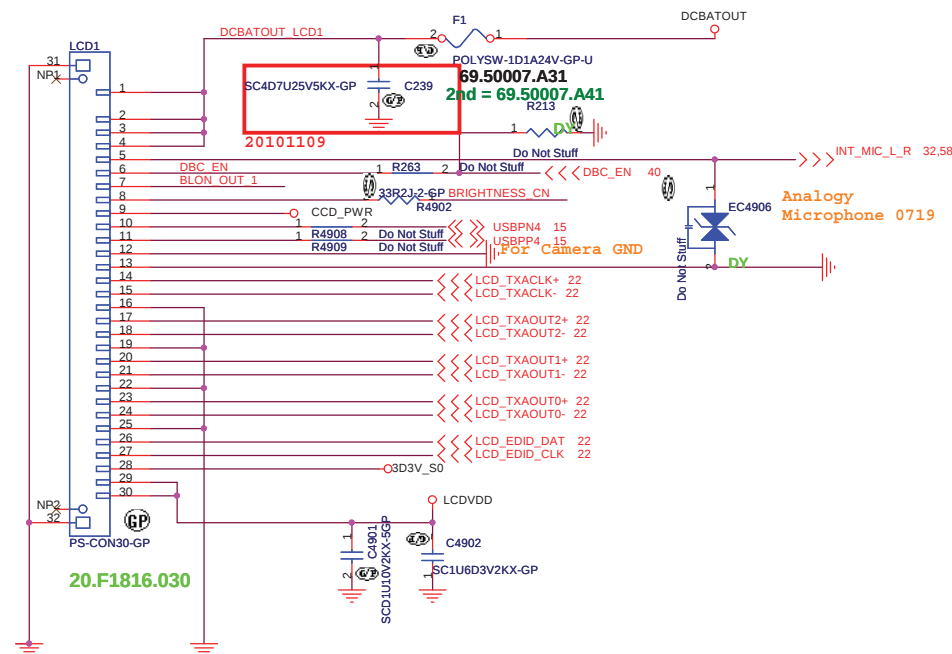


<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
LCD CRT SWITCHABLE	
Size A3	Document Number JE43-CP
Date: Wednesday, November 24, 2010	Sheet 22 of 69
Rev -1	

LCD/INVERTER/CCD CONN LCD/CCD CONN



Hynix 1G 800M N11PGV SKU

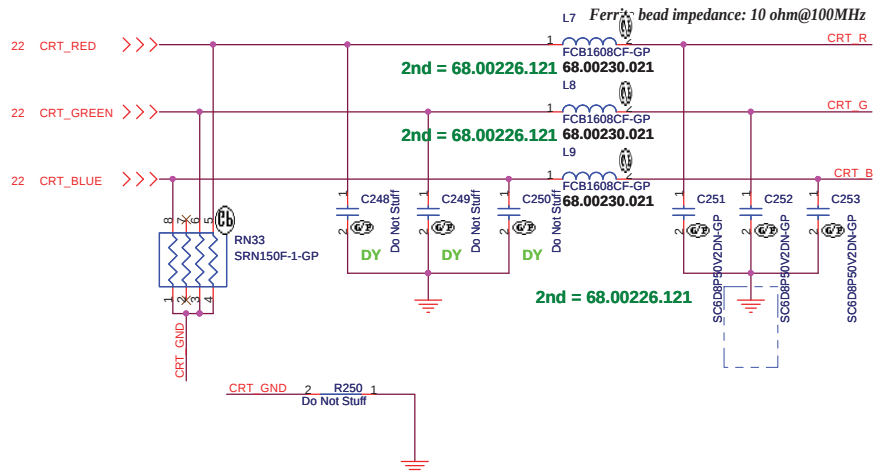
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			
LCD CONN			
Size	Document Number	Rev	
	JE43-CP	-1	
Date:	Wednesday, November 24, 2010	Sheet	23 of 69

<http://hobi-elektronika.net>

Layout Note:
Place these resistors
close to the CRT-out
connector

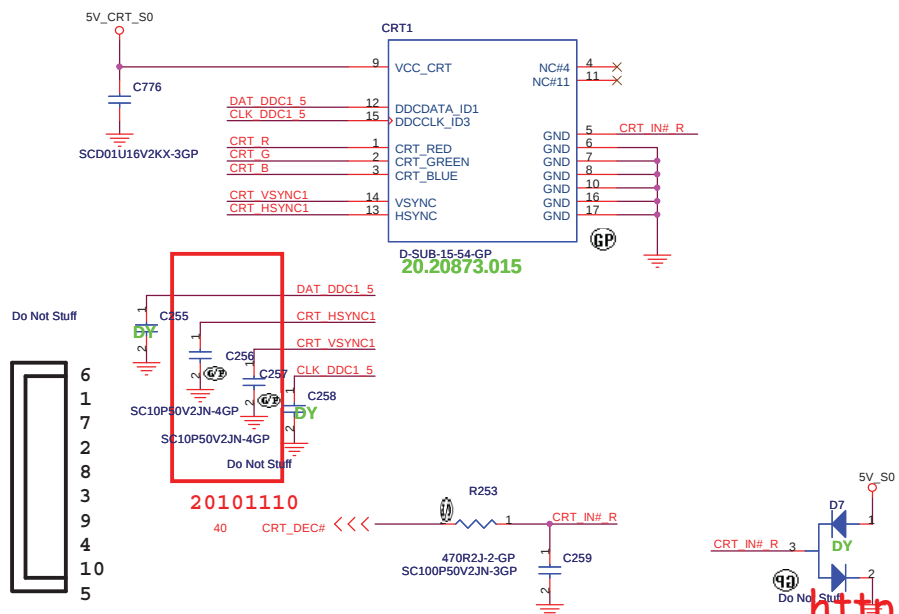


Layout Note:

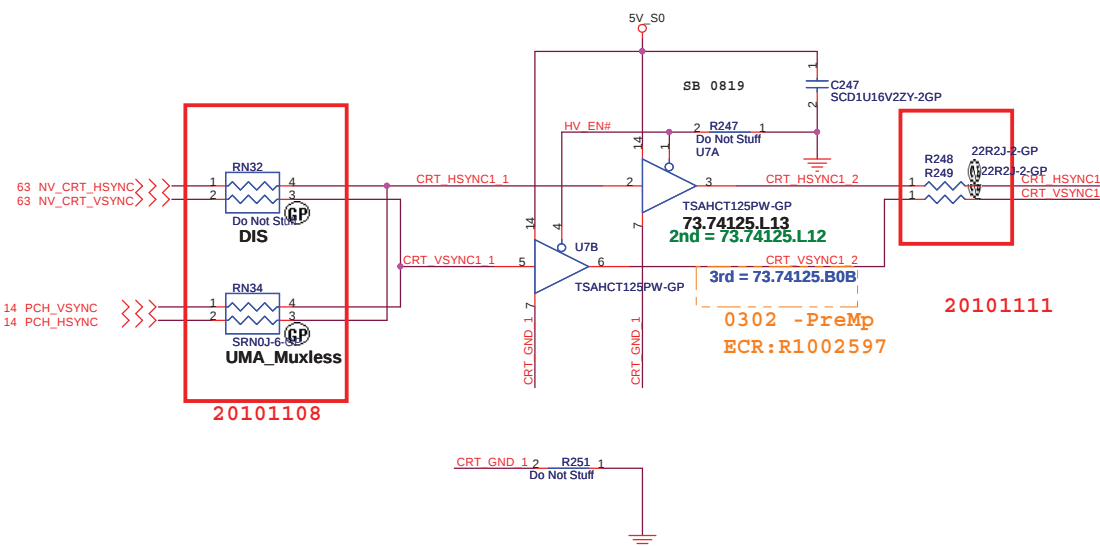
* Must be a ground return path between this ground and the ground on the VGA connector.

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

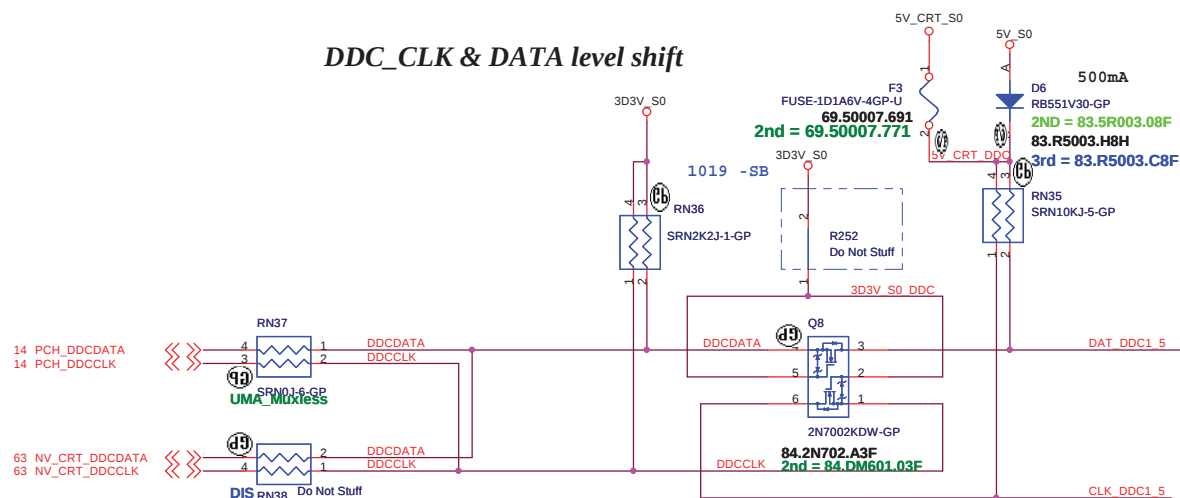
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift



Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

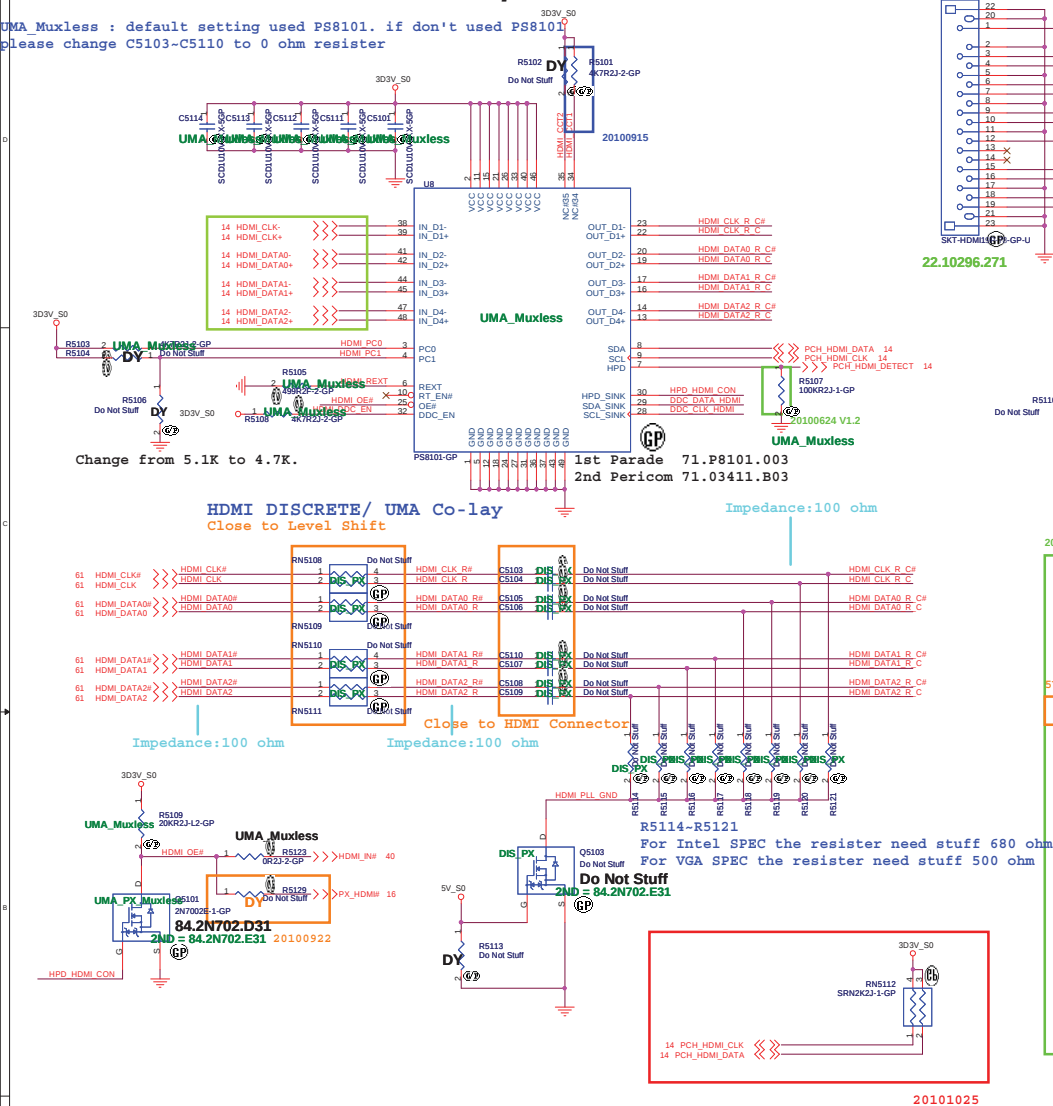
Title			CRT CONN	
Size	Document Number		JE43-CP	
Date:	Wednesday, November 24, 2010	Sheet	24	of 69

<http://hobi-elektronika.net>

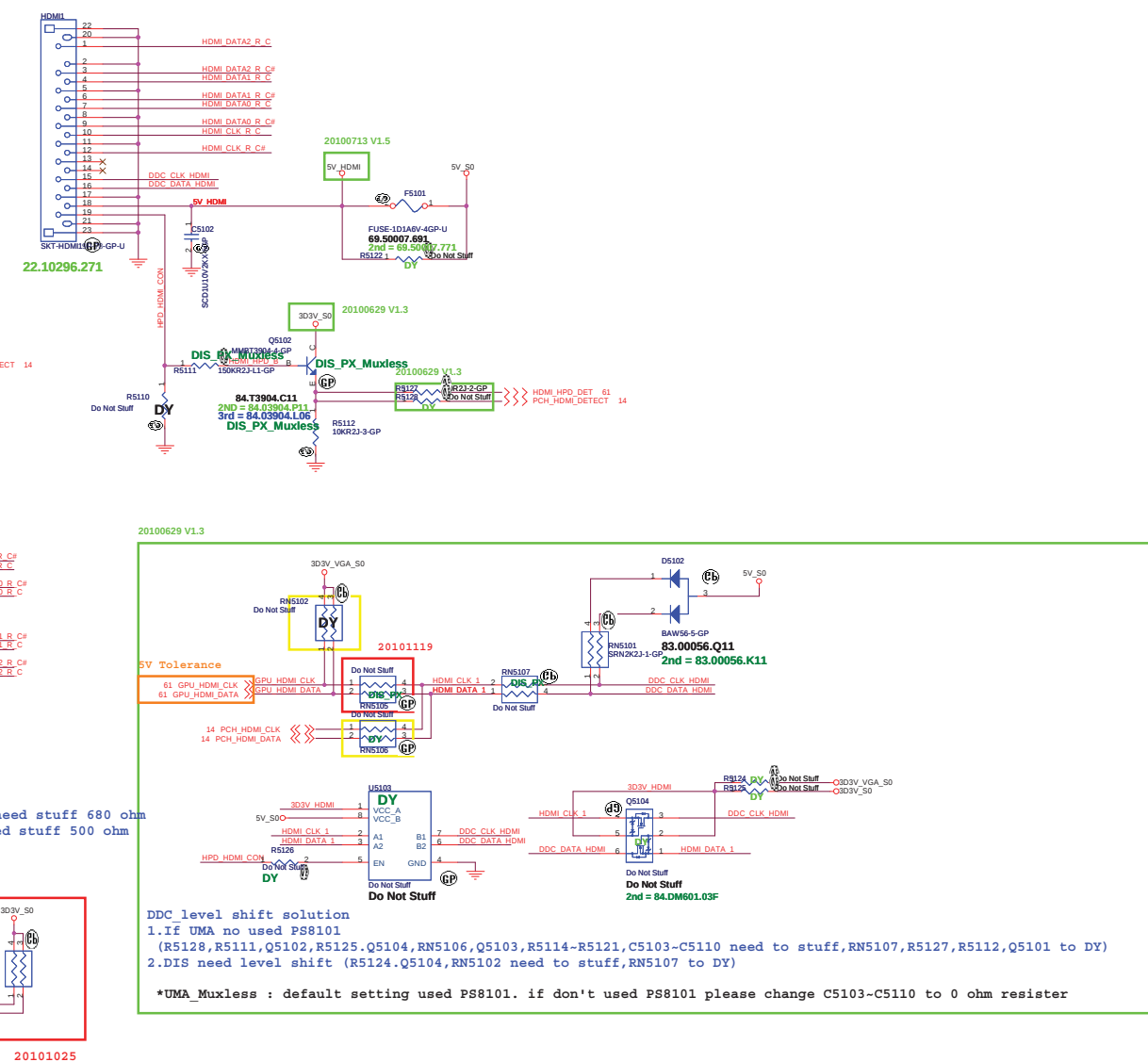
```
SSID = VIDEO
```

HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resistor



HDMI CONN



Hynix 1G 800M N11PGV SKU

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Date	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page

HDMI CONN

Size	Document Number
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JE43-CP

Date: Wednesday, November 24, 2010

4.3-CP
Sheet

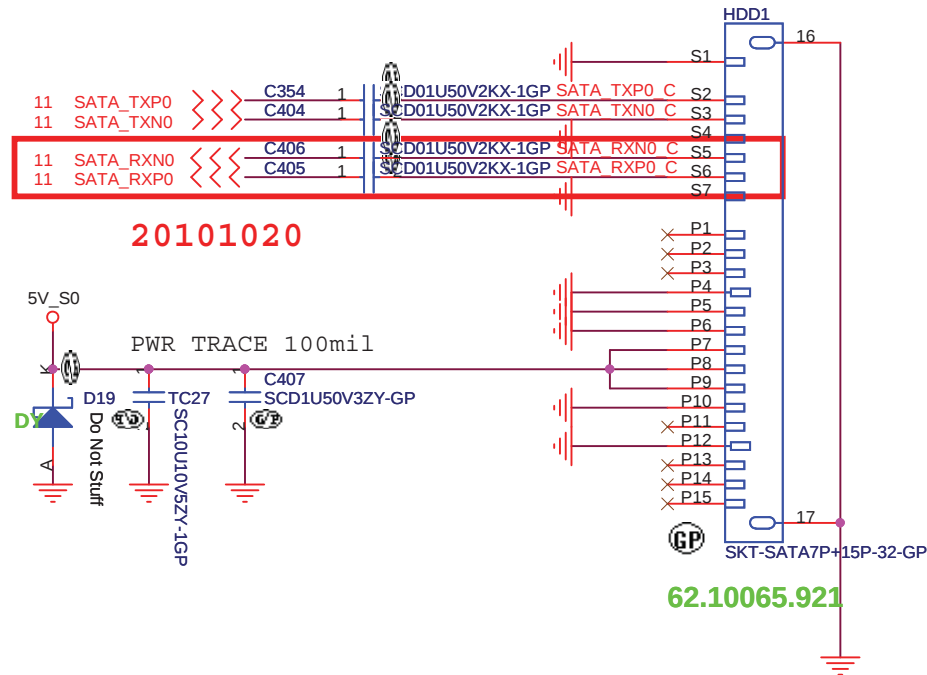
Rev	
-----	--

REV
-1

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<http://hobi-elektronika.net>

SATA Connector



Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD CONN			
Size	Document Number		Rev
	JE43-CP		-1
Date:	Wednesday, November 24, 2010	Sheet 26 of	69

<http://hobi-elektronika.net>

D



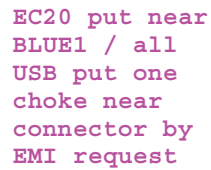
B

A

-1

69

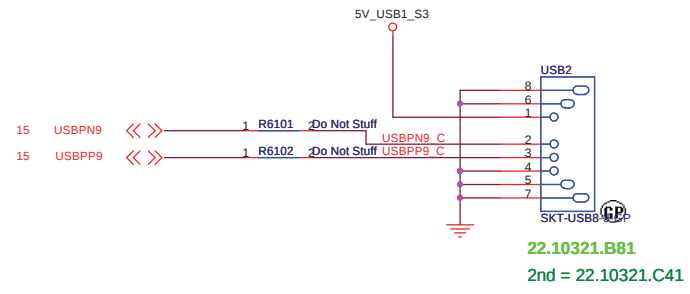
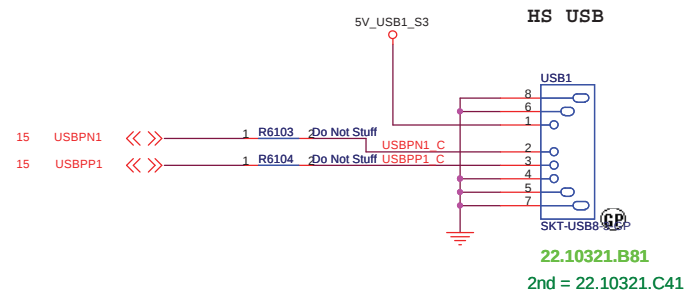
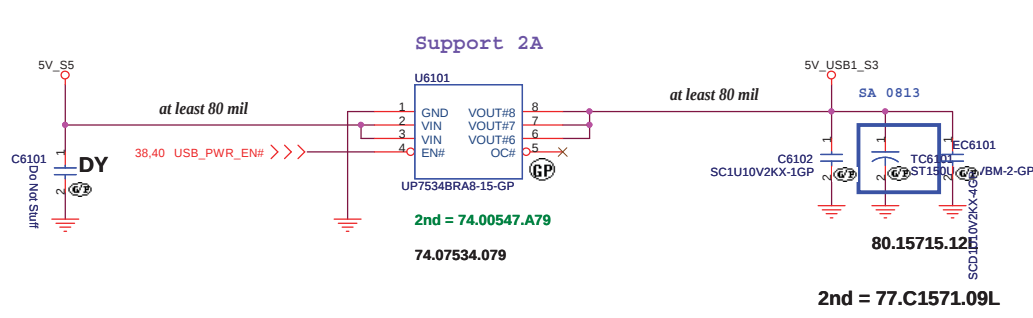
A



<http://hobi-elektronika.net>

緯創資通

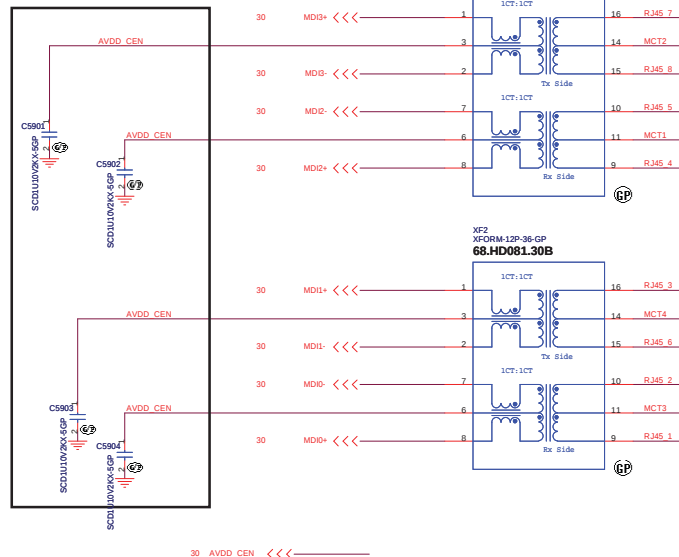
Sheet	28	of	69
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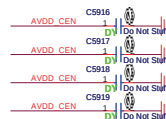
<http://hobi-elektronika.net>

GIGA Lan Transformer

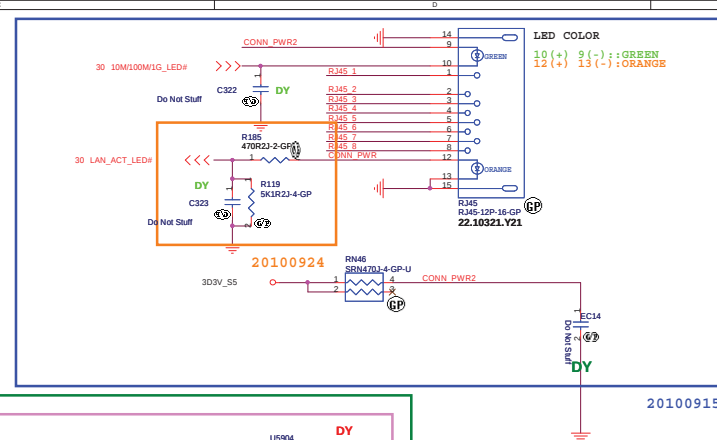
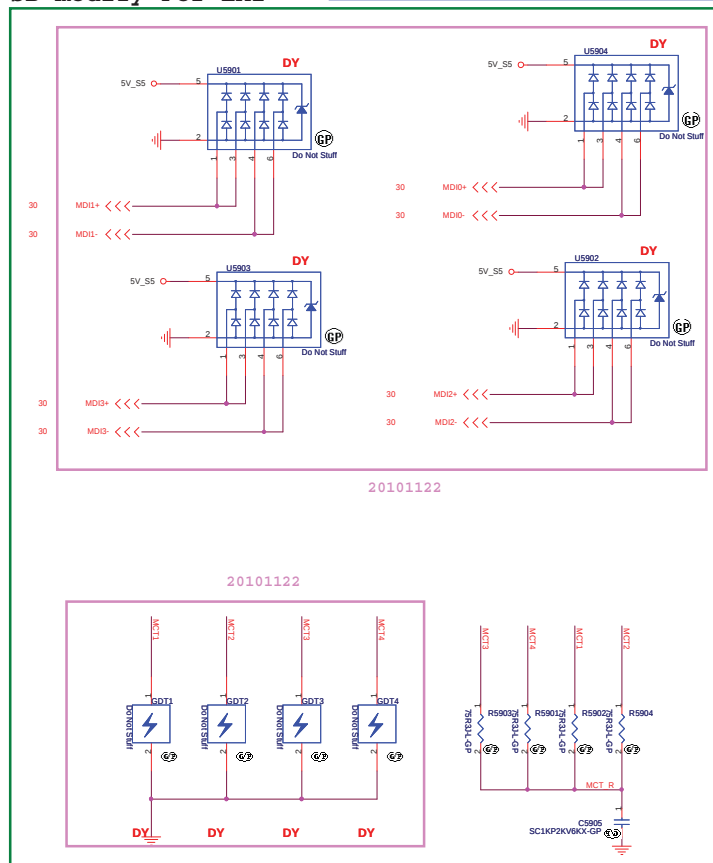
SSID = LOM



20100915



SB modify For EMI



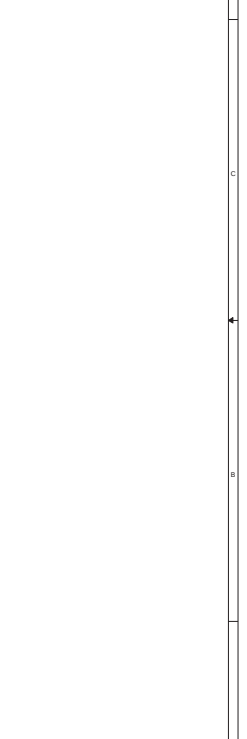
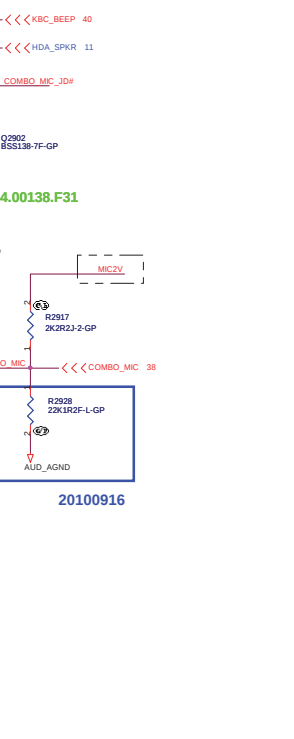
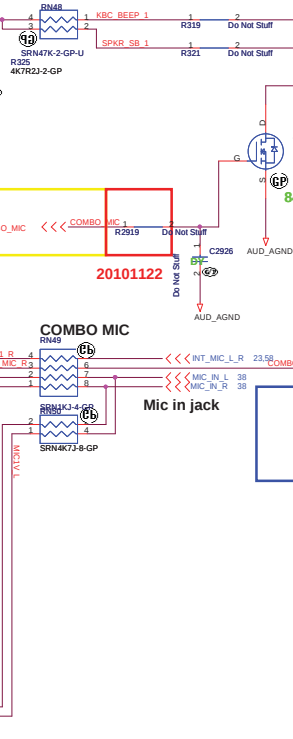
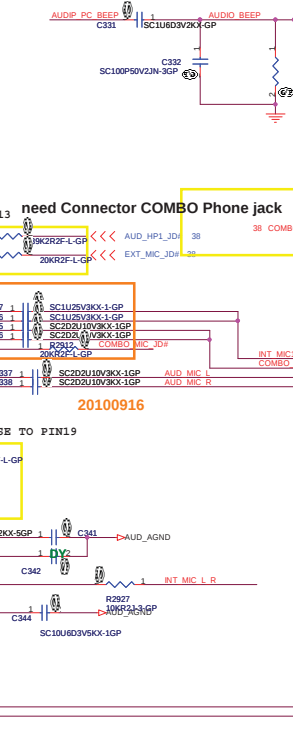
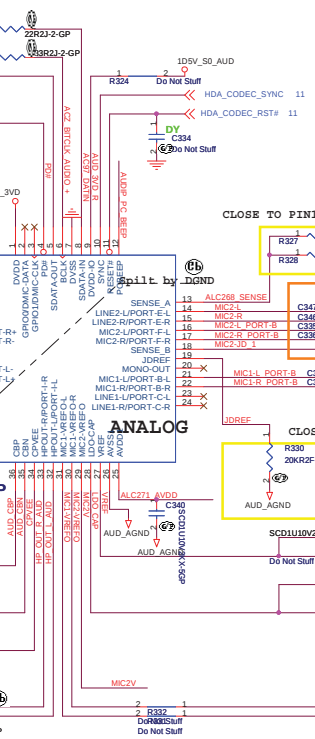
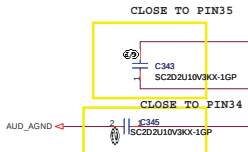
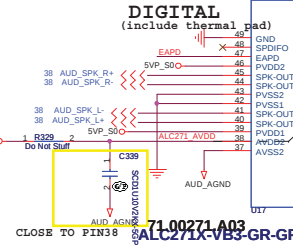
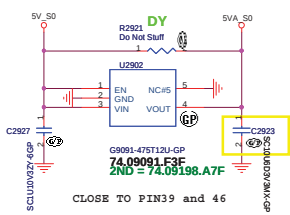
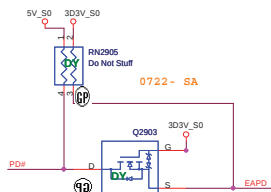
Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.		Title	
Size A2		Document Number	
Date: Wednesday, November 24, 2010		Sheet 31 of 69	
LAN CONN		JE43-CP	
Rev		-1	

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ALC271X Co-layout ALC277X

pin 37 AVSS2 CPVREF
pin 47 RAPD REGREF



Hynix 1G 800M N11PGV SKU	
緯創資通 Wistron Corporation	
21F, 8B, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
File	AUDIO CODEC(ALC271)
Size	Document Number
Custom	JE43-CP
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	Rev -1

	A	B	C	D	E
4					
3					
2					
1					

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Hynix 1G 800M N11PGV SKU

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

JE43-CP

Rev

-1

Date:

Wednesday, November 24, 2010

Sheet

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of

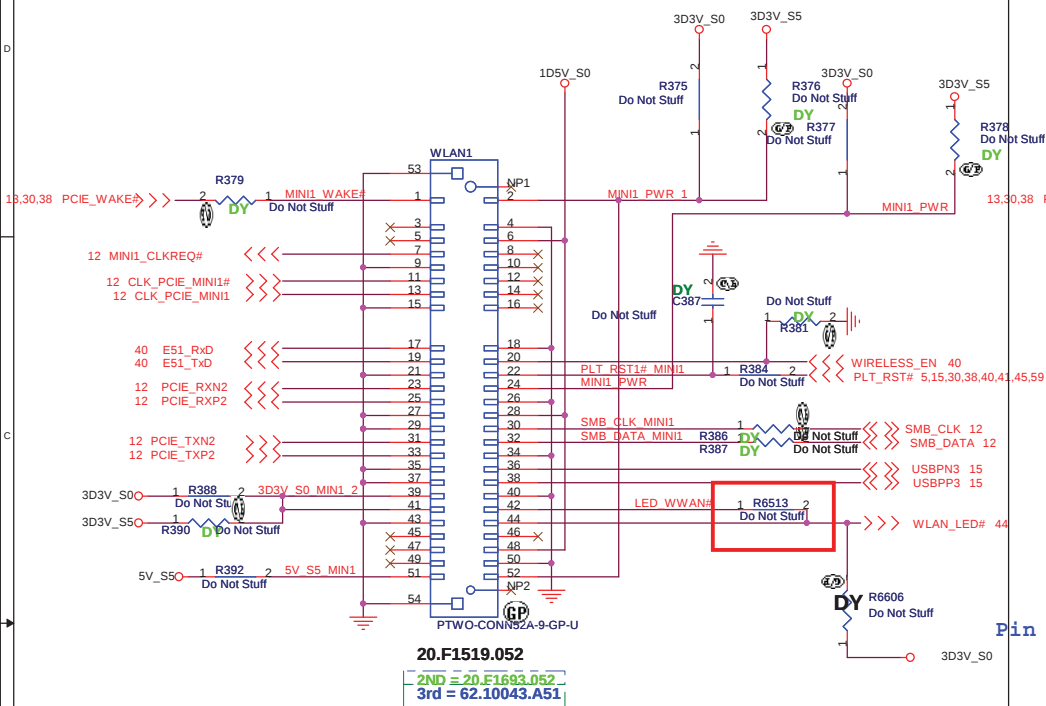
69

E

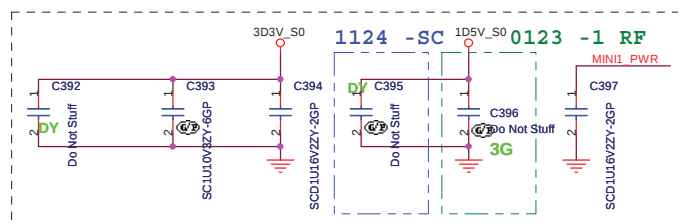
Hylix 1G 800M N11PGV SKU				A
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.		
Title				

Size	Document Number			Rev
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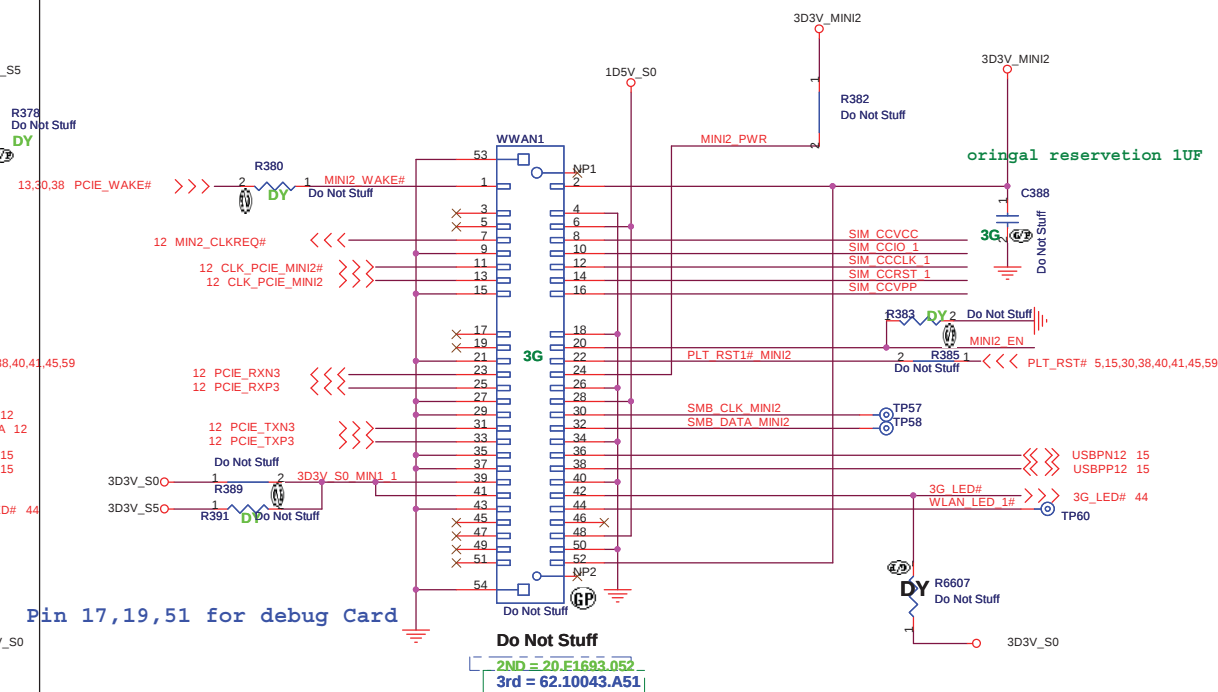
Mini Card Connector(WLAN) Support debug-card



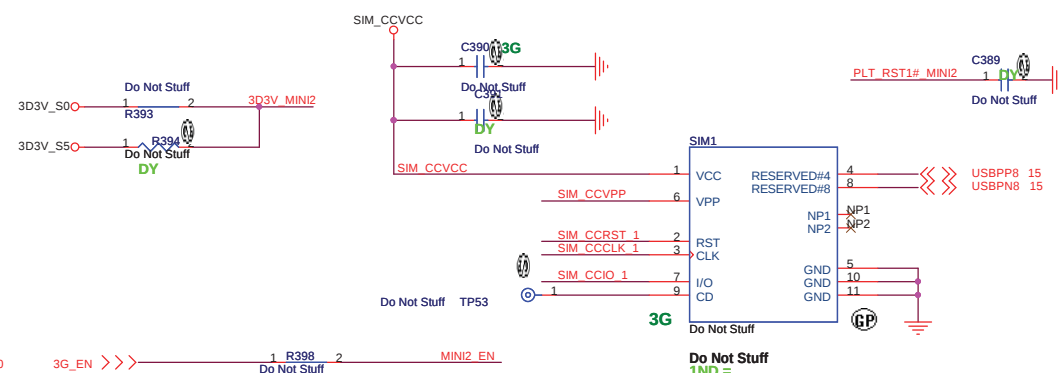
Place near MINI1



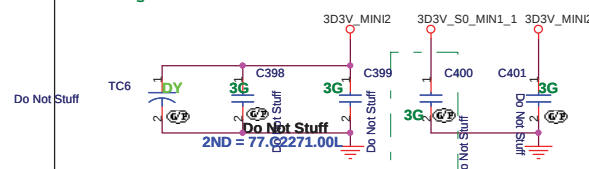
Mini Card Connector(Robson2 and 3G)



Pin 17,19,51 for debug Card



original reservation 10UF

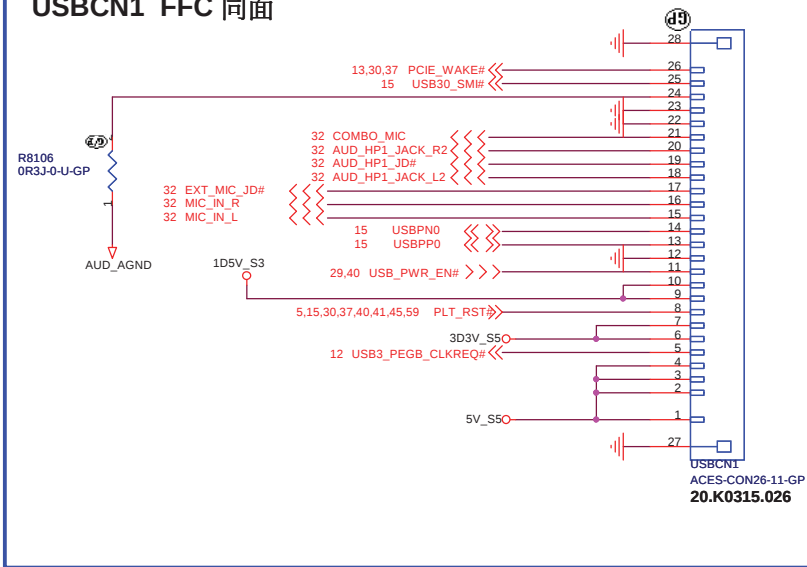


Hynix 1G 800M N11PGV SKU

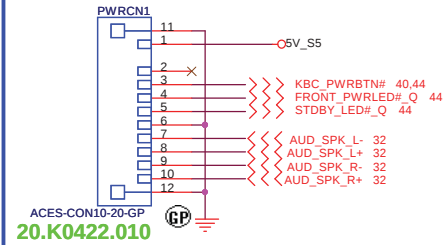
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
MINI CARD			
Size A3	Document Number		Rev
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USBCN1 FFC 同面

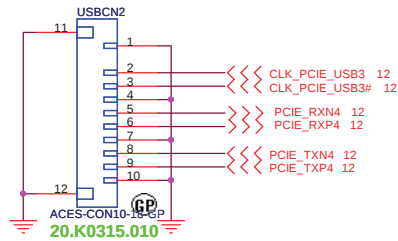


PWRCN1 FFC 異面



20100915

USBCN2 FFC 同面

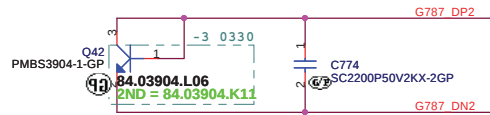


<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

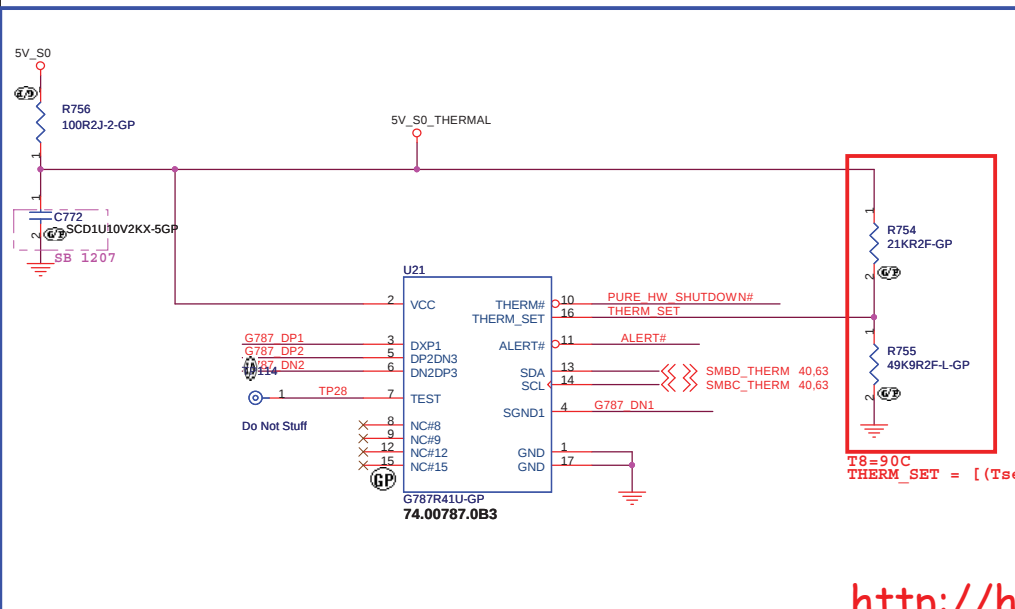
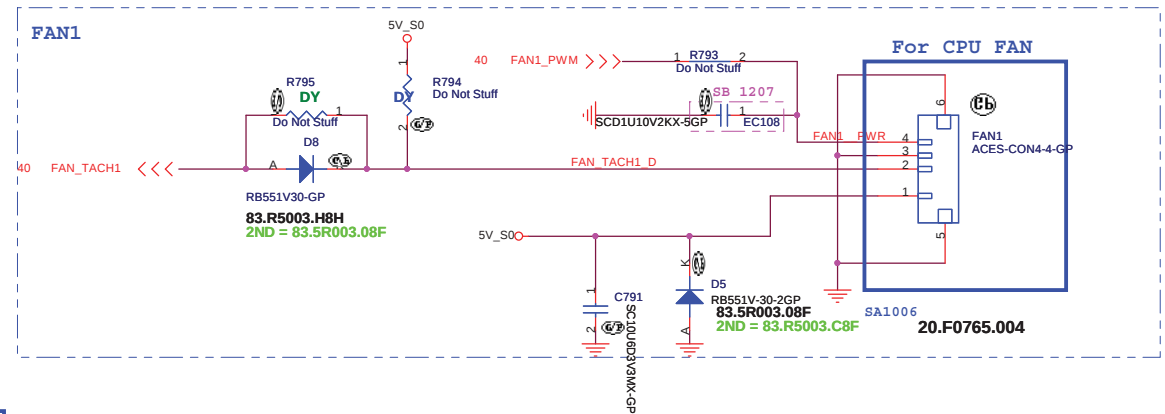
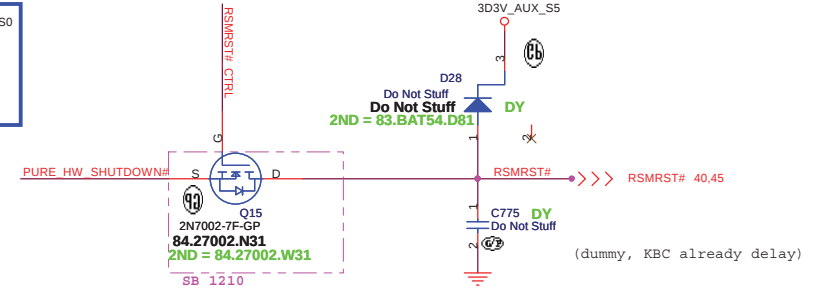
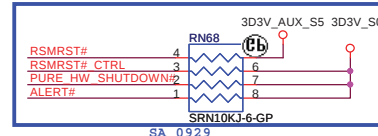
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
I/O Board			
Size A3	Document Number	Rev	
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for T8 thermal diode



C82 & C561 CLOSE TO G787

for system thermal diode



$$T8=90^{\circ}\text{C}$$

$$\text{THERM_SET} = [(T_{\text{set}}-72) \times 0.02+0.34] \times \text{VCC}$$

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Hynix 1G 800M N11PGV SKU

5	4	3	2	1
D				D
C				C
B				B
A				A

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Hynix 1G 800M N11PGV SKU

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

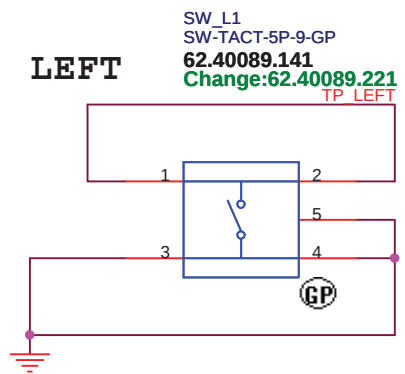
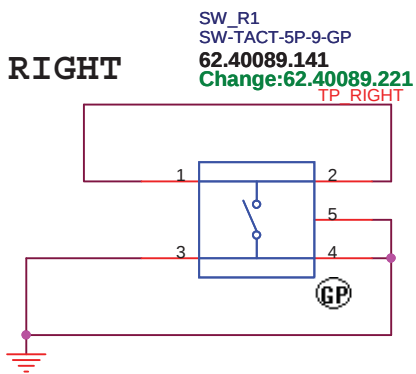
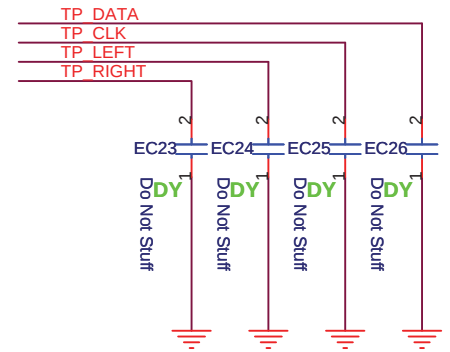
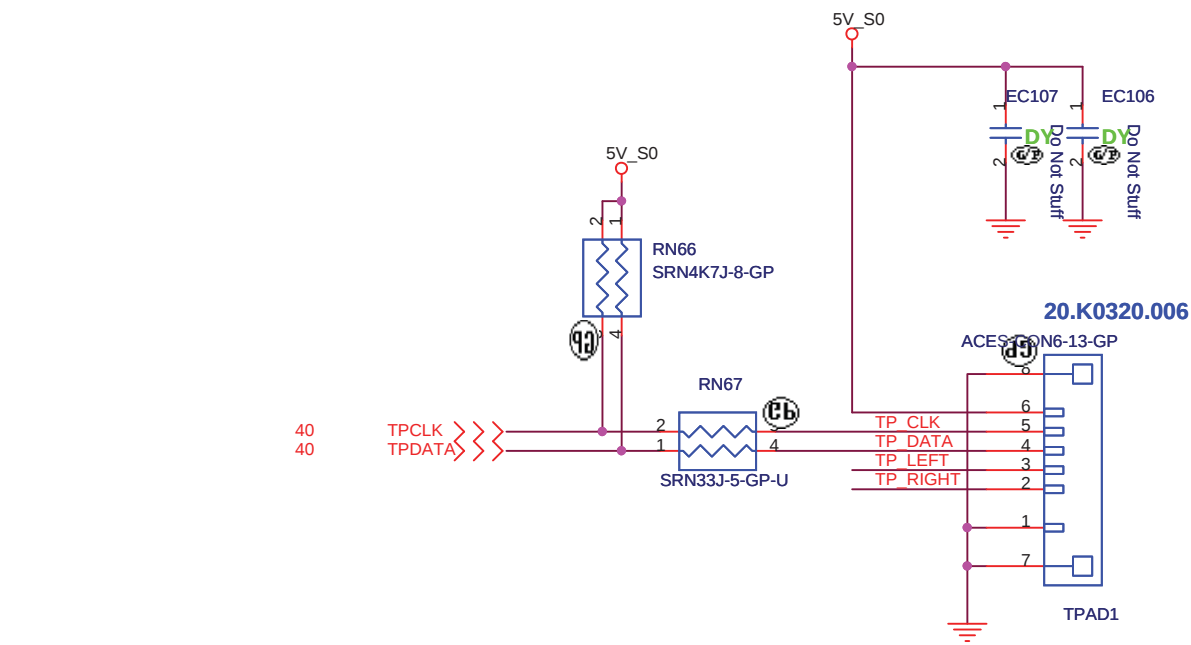
Size
A3

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-1

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Hynix 1G 800M N11PGV SKU

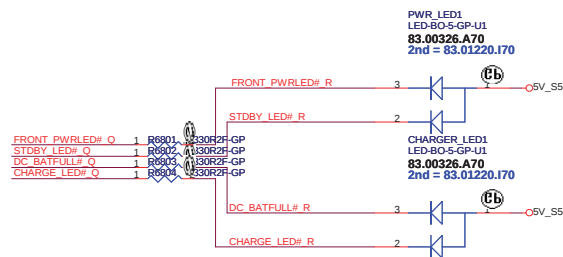
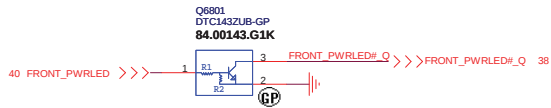
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Touch PAD_FP CONN

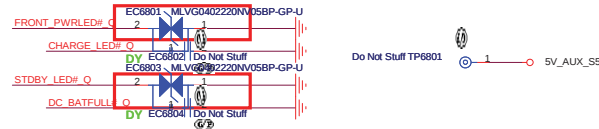
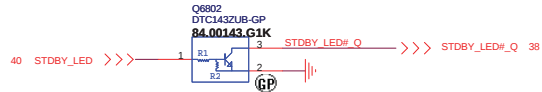
Size	Document Number	Rev
		-1

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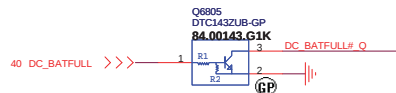
Power button LED



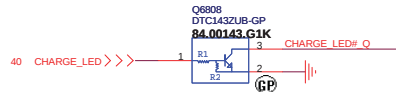
Power STDBY_LED



Battery LED2 (DC_BATFULL)

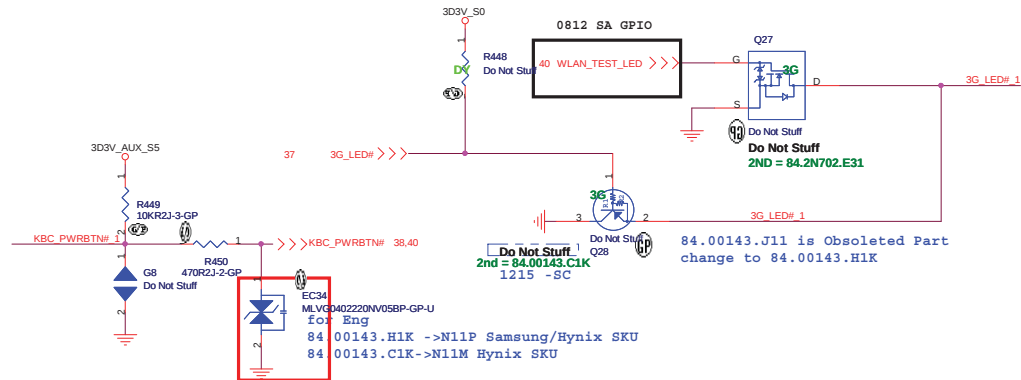


Battery LED1 (CHARGE)

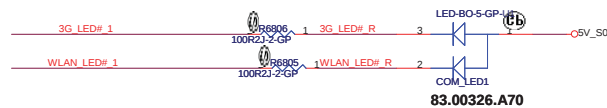


EC6801, EC6803, EC34 請幫忙上件 22p 5.5V 的 Varistor料號是 69.80024.011

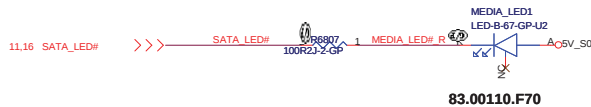
For 2010 Acer Project, WLAN and 3G LED control by KBC



Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net



SATA HDD LED



Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

1208 -SC

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
23F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED&POWERBD CONN		
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97,38,40,41,59 PLT_RST# <<>>

R460
4K7R2J-2-GP

R461
2K2R2J-2-GP

40,49,59 SS_ENABLE <<<

D17
BAS16-1-GP

84.02222.V11

2nd = 84.02222.R11

3rd = 84.02222.S11

change 84.02222.U11 to 84.02222.R11

JV50-CP and JV71-CP have stuff in BOM

PM_THRMTRIP-A# 516

MMBT2222A-3-GP
Q32

PLT_RST# 2

RSMRST# 39,40

83.00016.B11

2ND = 83.00016.K11

3rd = 83.00016.F11

13,47 CORE_PWRGD >>>

13,47,50,51,52 ALL_PWRGD >>>

40 S0_PWR_GOOD >>>

R466

Do Not Stuff

R467

Do Not Stuff

U30

74LVC1G08GW-1-GP

73.01G08.L04

2ND = 73.75Z08.DAH

3D3V_S5

C436

SCD1U10V2KX-5GP

R468

Do Not Stuff

R469

Do Not Stuff

IMVP_VR_EN 4

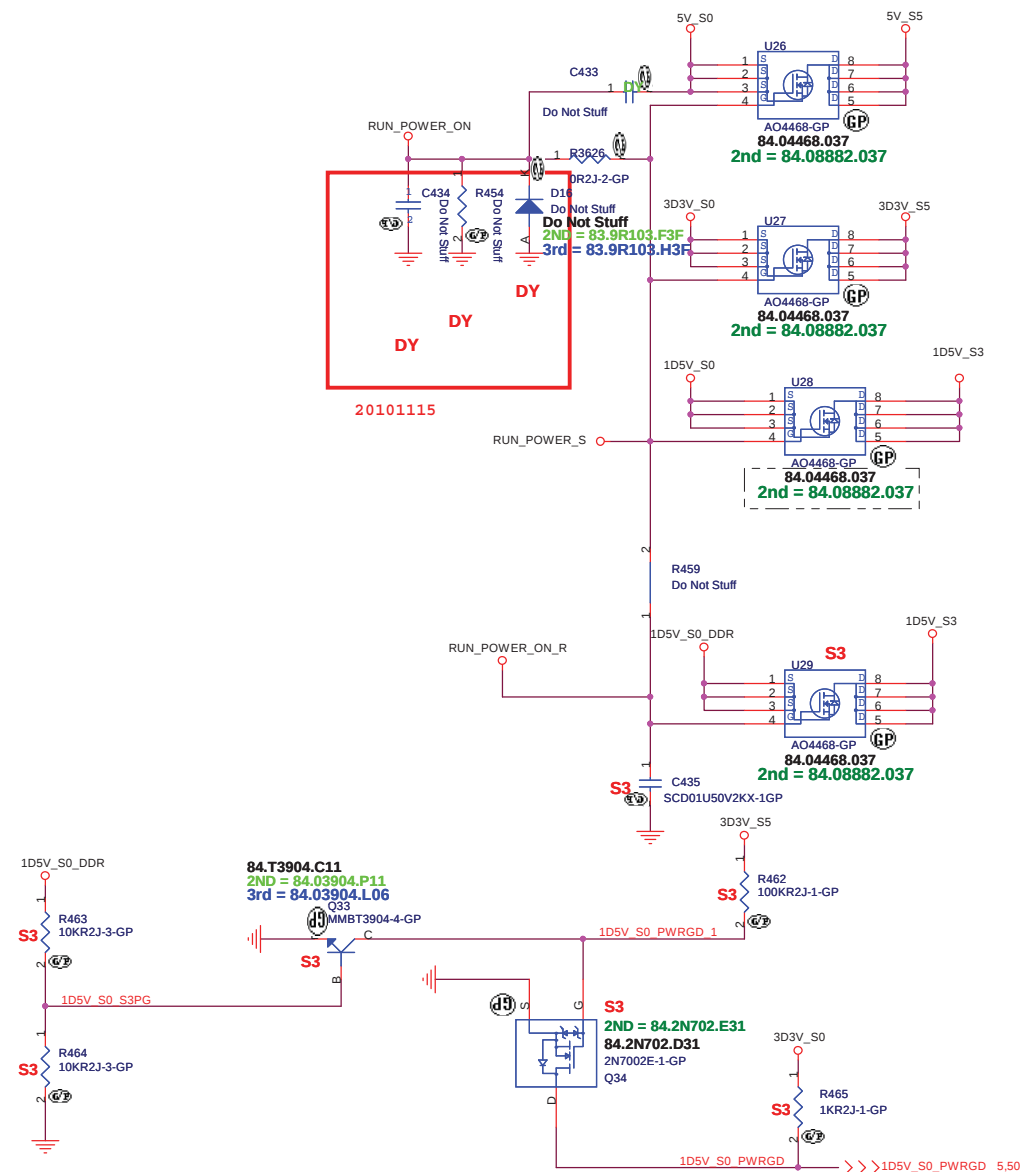
PM_PWROK 13

S0 PWR GOOD

R470

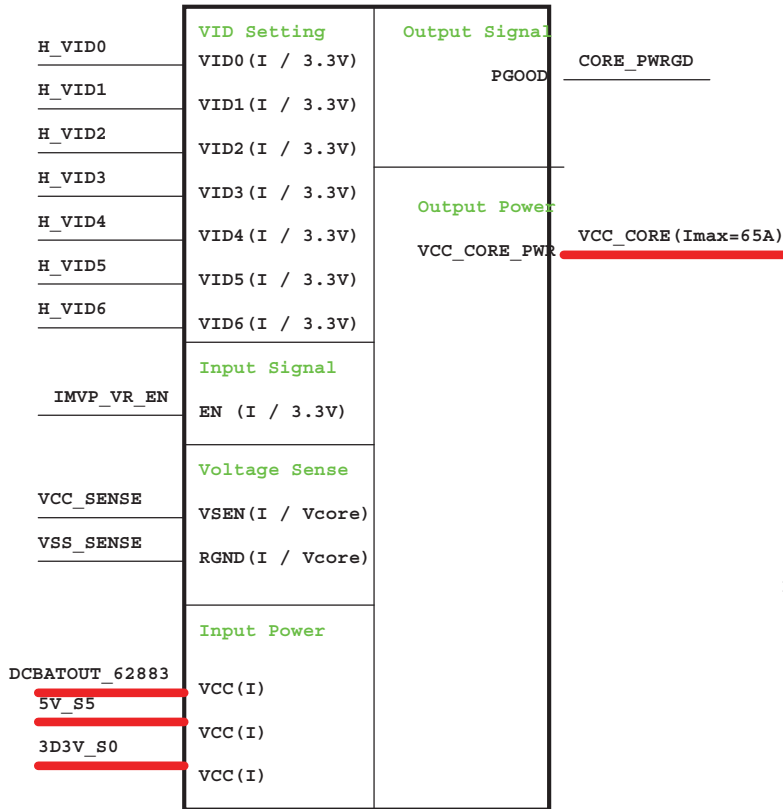
IMVP VR EN

Do Not Stuff

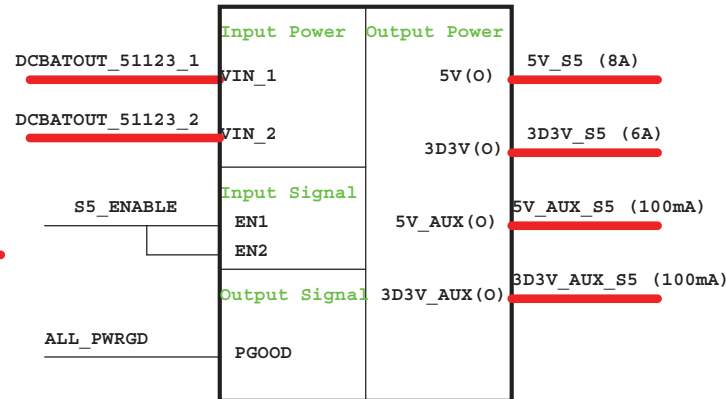


PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S
0	0	0	0
1	1	1	1

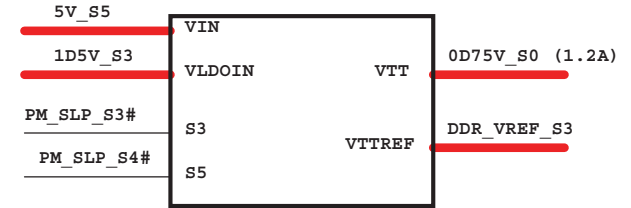
ISL62883 VCC_CORE



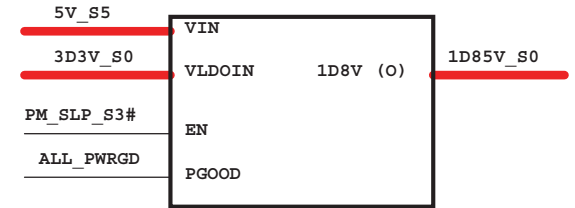
TPS51123 5V/3D3V



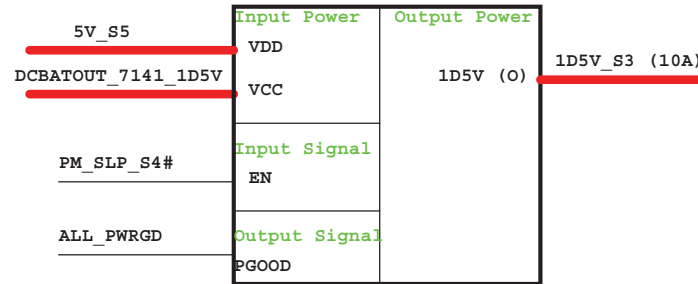
RT9026 0D75V_S0



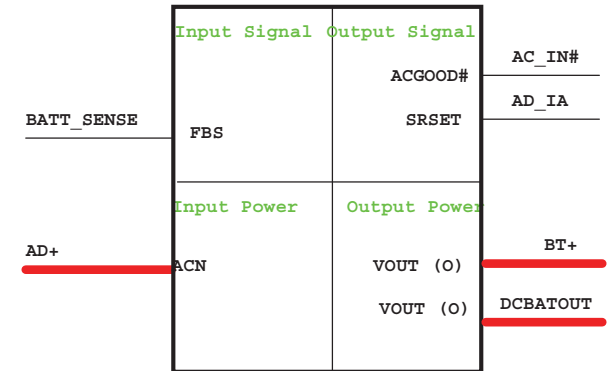
RT9025 1D8V



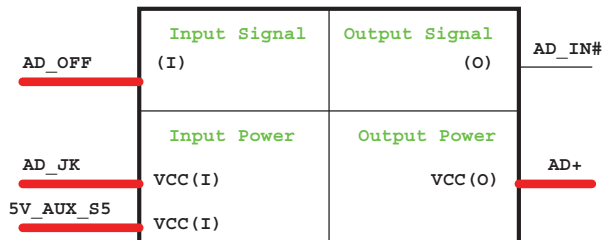
RT9025 1D5V



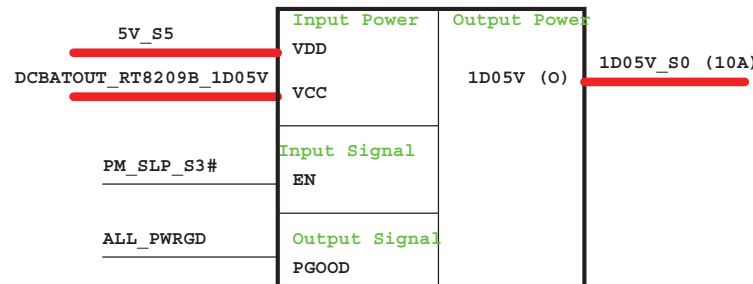
Charger BQ24745



Adapter



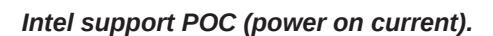
RT8209B 1D05V



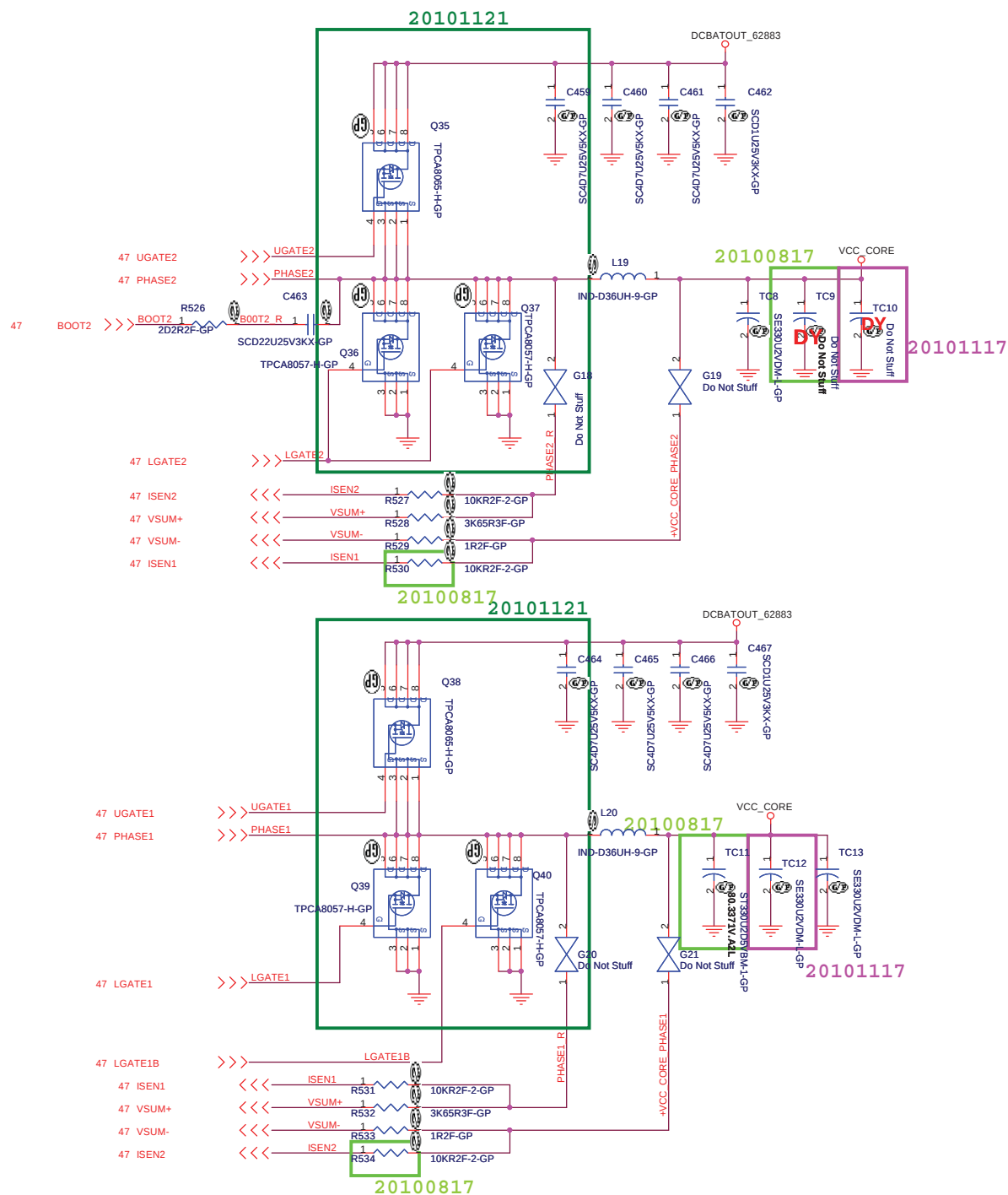
Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Power Block Diagram		
Size	Document Number	Rev
	JE43-CP	-1
Date:	Wednesday, November 24, 2010	Sheet 46 of 69



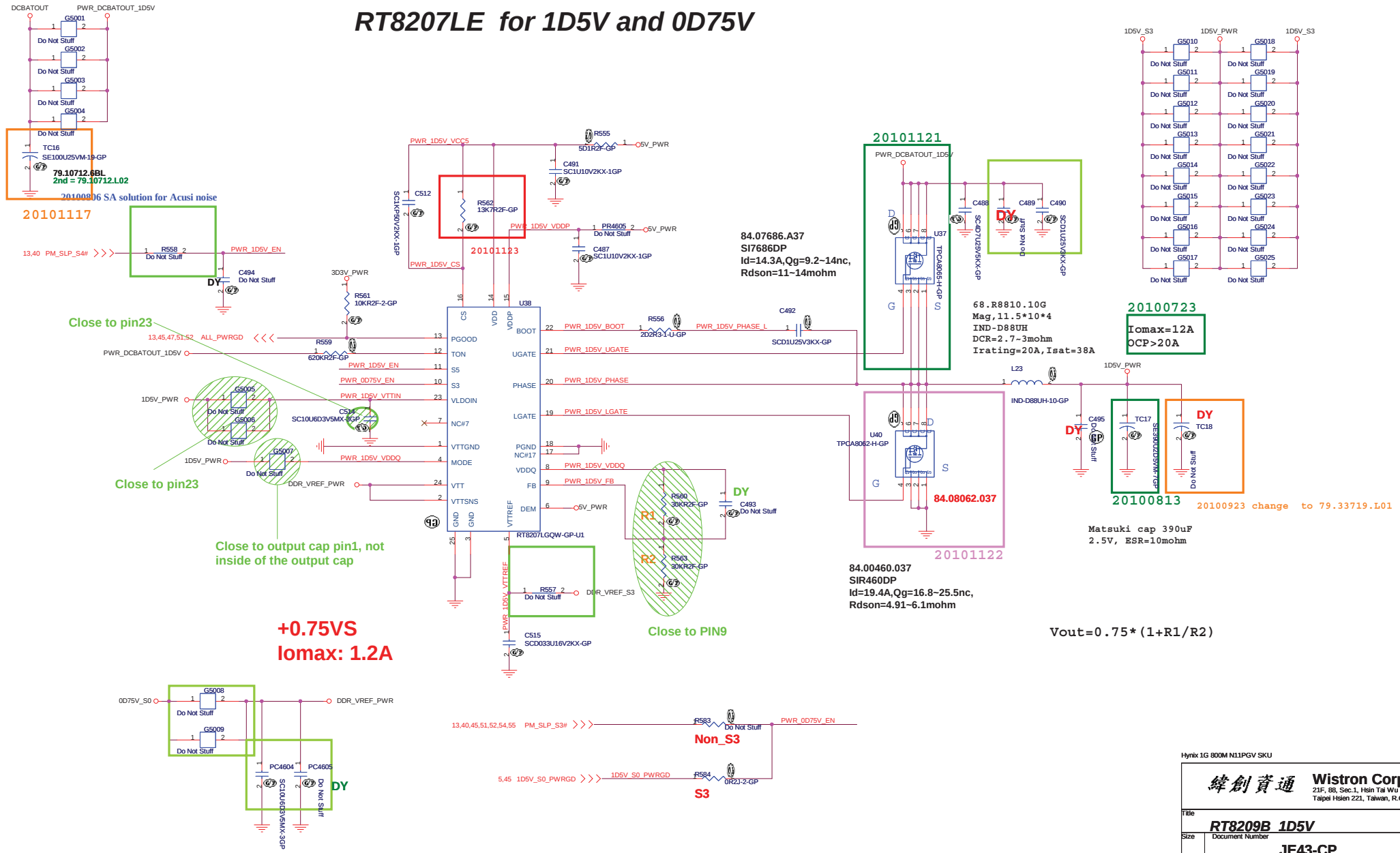
Title			
ISL62882 CPU CORE (1/2)			
Size	Document Number		Rev
	JE43-CP		-1
Date:	Wednesday, November 24, 2010	Sheet 47 of	69



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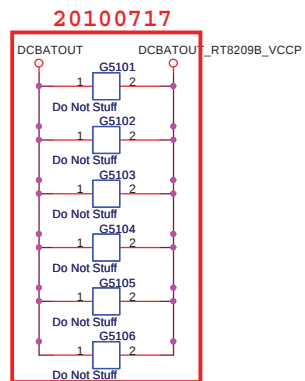
Hynix 1G 800M N11PGV SKU

RT207LE for 1D5V and 0D75V

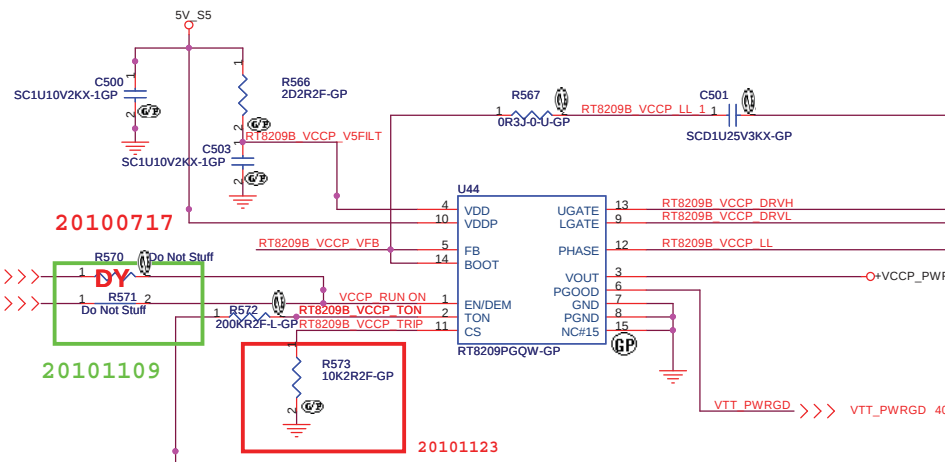


Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
RT8209B 1D5V	
Size	Document Number
JE43-CP	
Date	Wednesday, November 24, 2010
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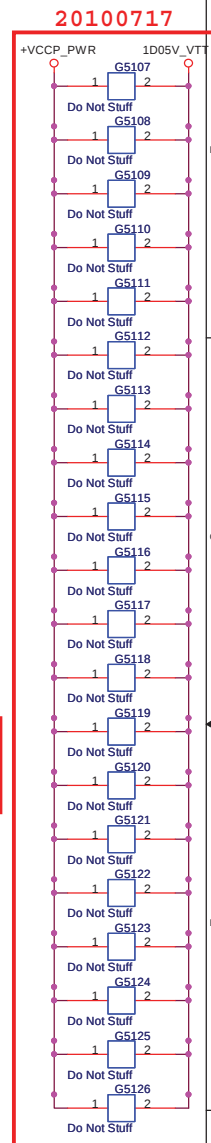
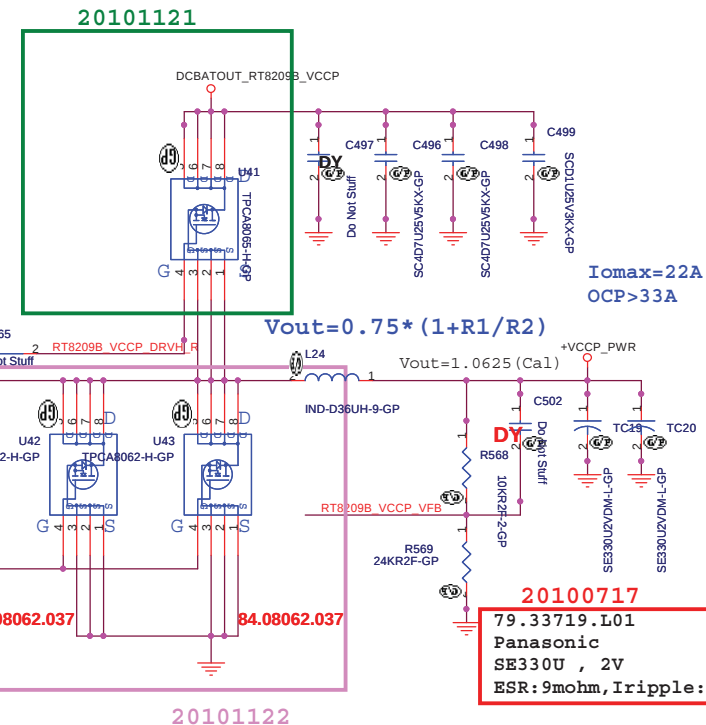
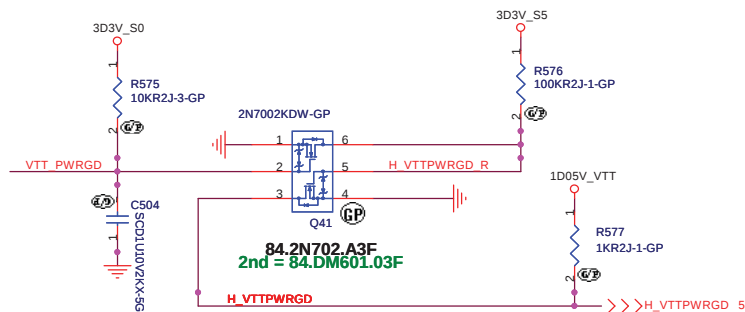


RT8209E for VCCP



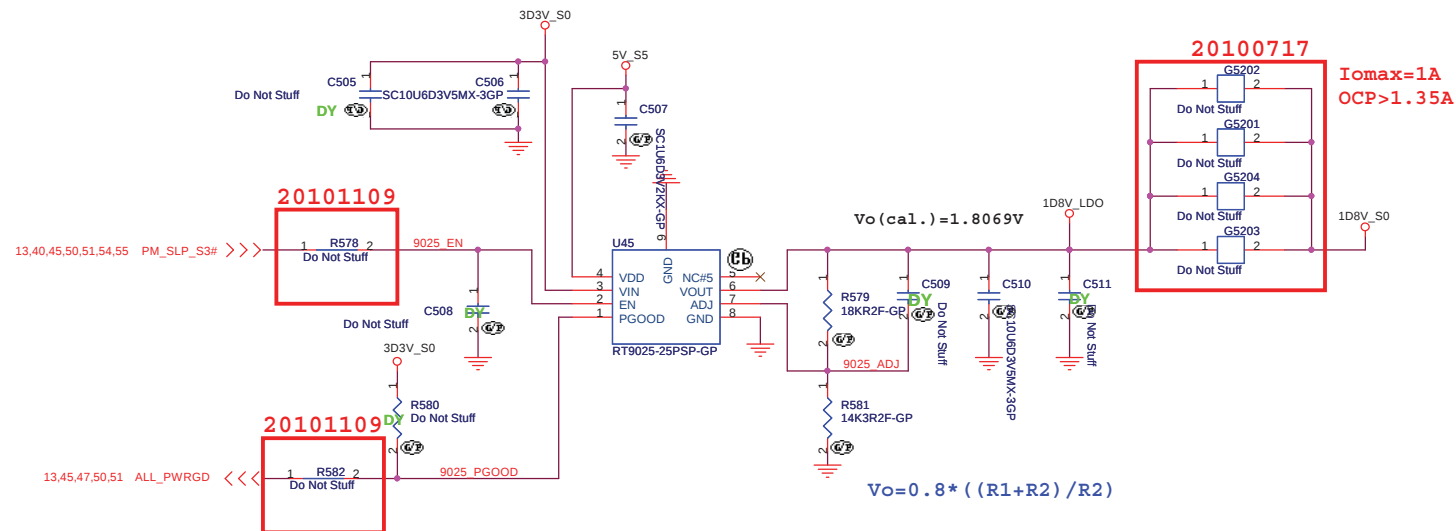
Freq=360KHz

because of 1.05V_S0 and 1.05V_VTT combin together
use PM_SLP_S3# Enable 1.05V power



RT9025 for 1D8V_S0

20090915



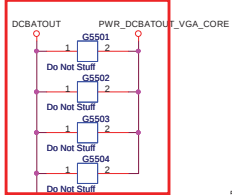
<http://hobi-elektronika.net>

Hynix 1G 800M N11PGV SKU

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT9025 1D8V/RT9026 0D75		
Size	Document Number	Rev
	JE43-CP	-1
Date: Wednesday, November 24, 2010	Sheet 52 of 69	

20100717



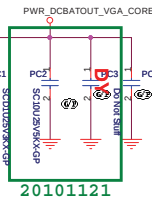
SSID = PWR.Plane.Regulator_GFX

N12P-GV and N11P-GV, PR6換成9.1K
(part number: 64.91015.6DL) , MOSFET 請用TPCA8065-H

+TPCA8062-Hx2 上一下二

20100813

20101121

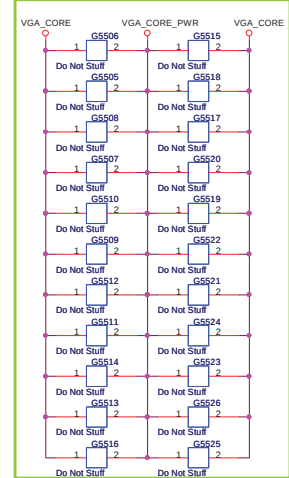


$$V_{out} = 0.75V * (R1 + R2) / R2$$

84.07686.A37
CYNTEC, 11.5*10*4
IND-D36UH
DCR=1.05mohm
Irating=30A, Isat=60A

Design Current = 21.94A
24.14A < OCP < 28.53A

20100813



RT8208B +VGA CORE
20101123



N11P-GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	0.90V
P0 - COLD	H	L	0.95V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEP5X0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.05V
	H	H	

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.02V
	H	H	

N12P GS:PR11=10K,PR14=100K,PR13=49.9K,PR15=33.2K

N12P GV: PR11=10K,PR14=75K,PR13=49.9K,PR15=43K

N11P GV: PR11=10K,PR14=75K,PR13=150K,PR15=75K

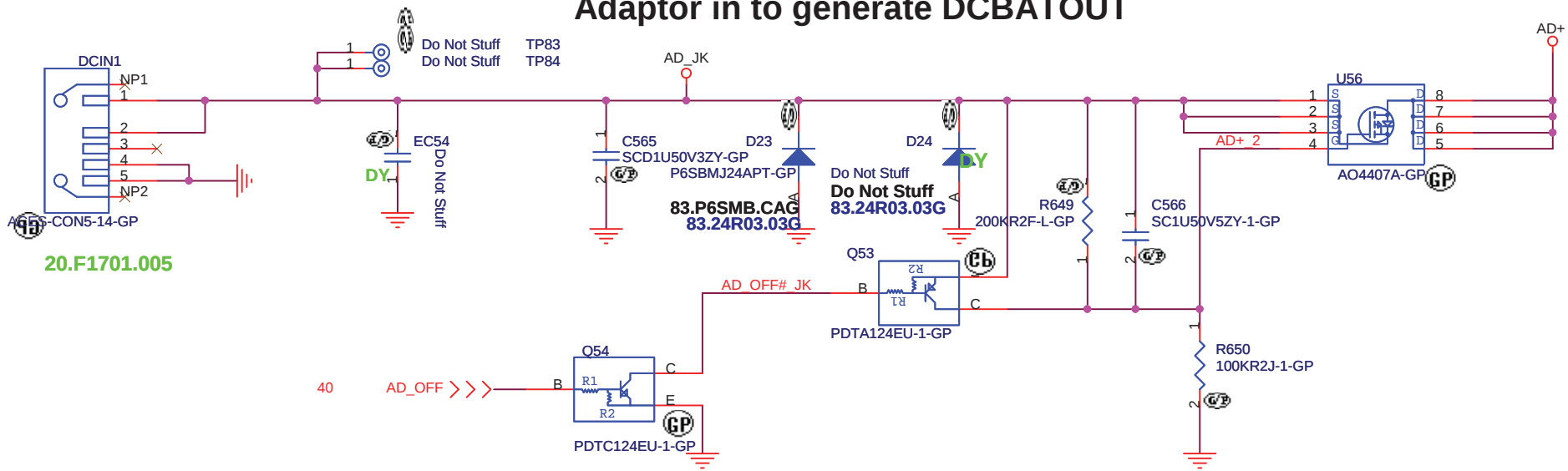
33.2K=64.33225.6DL
43K=64.43025.6DL
75K=64.75025.6DL
100K=64.10035.6DL
150K=64.15035.6DL

Hynix 1G 800M N11PGV SKU

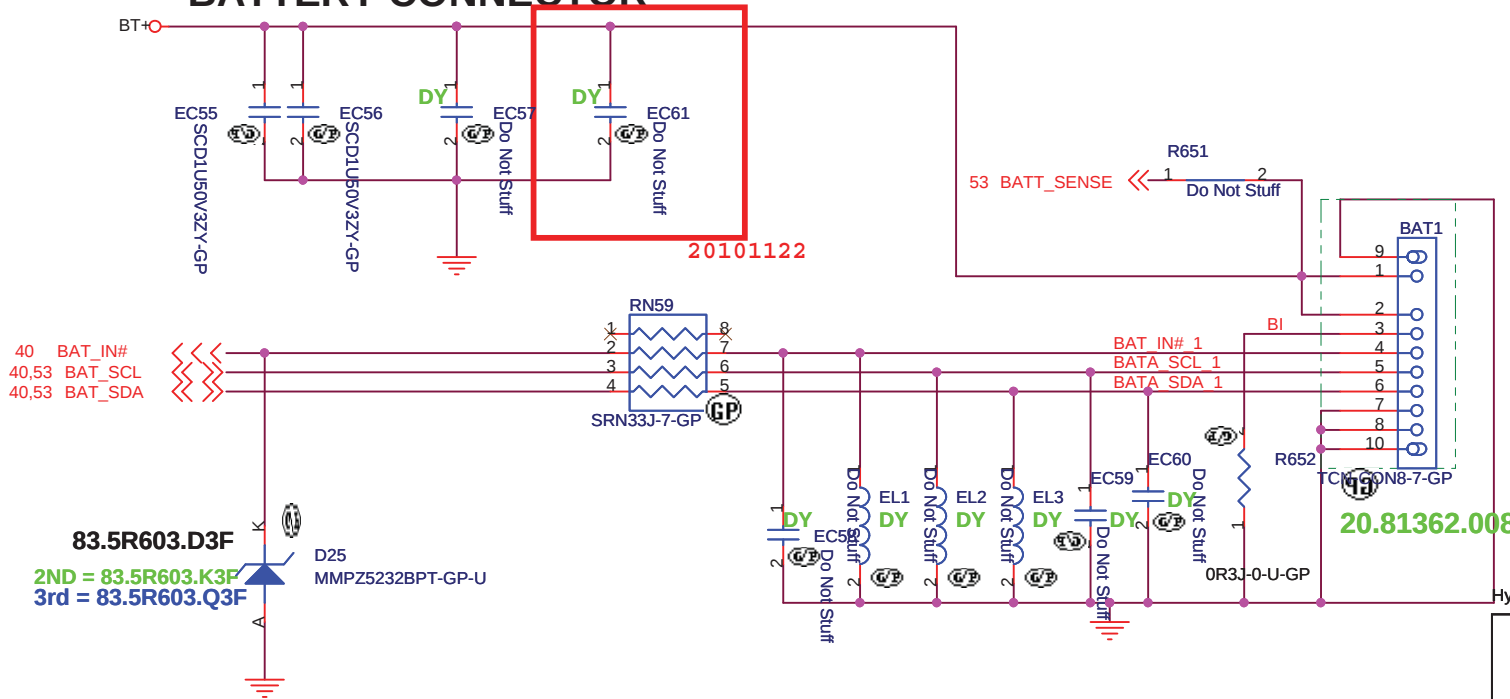
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: RT8208B +VGA CORE
Size: Custom
Document Number: JE43-CP
Date: Wednesday, November 24, 2010 Sheet 55 of 69

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

Hynix 1G 800M N11PGV SKU

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size

Document Number

JE43-CP

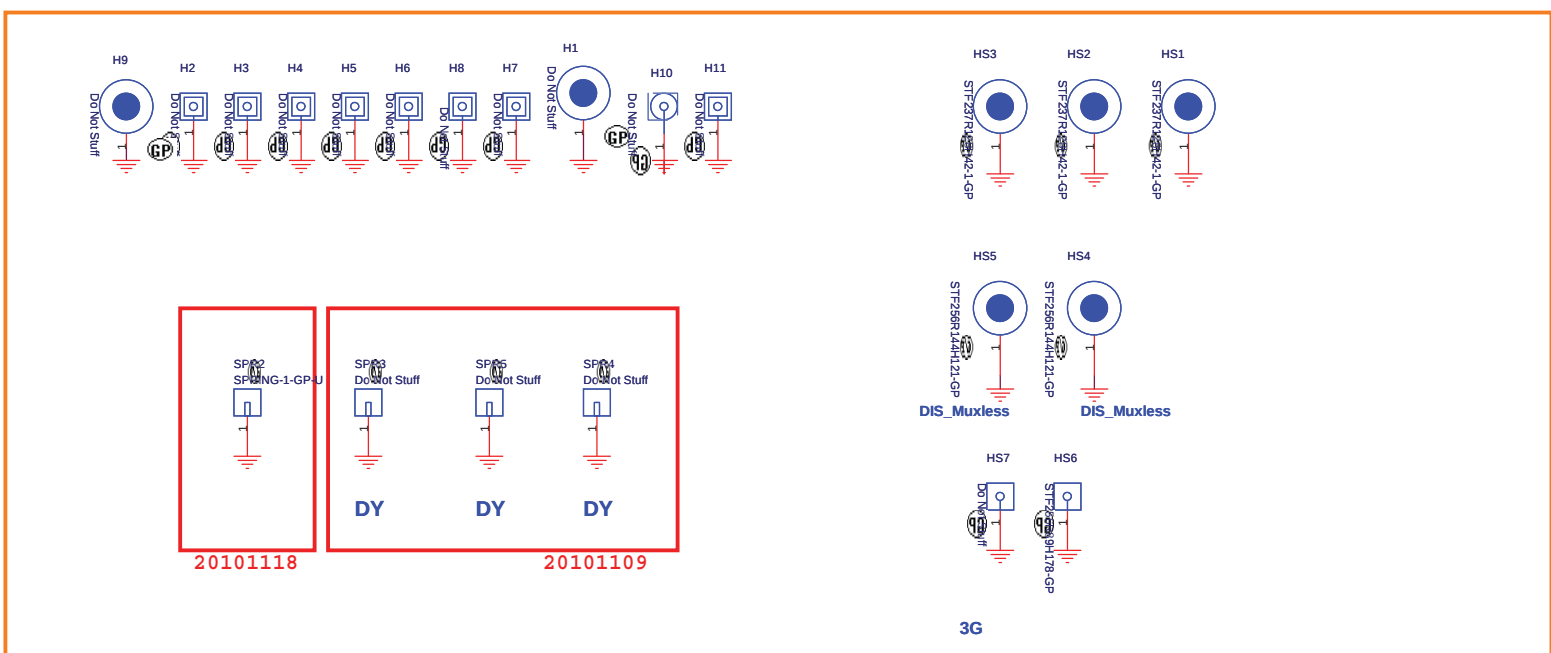
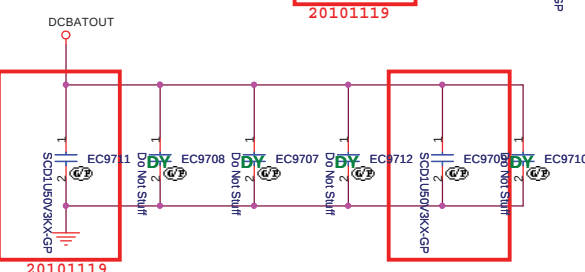
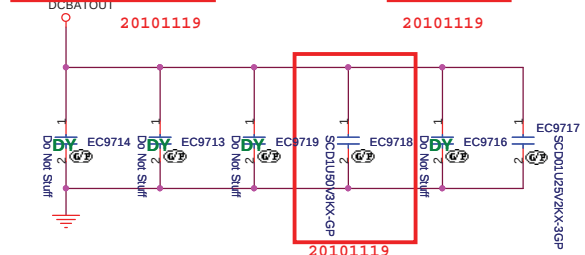
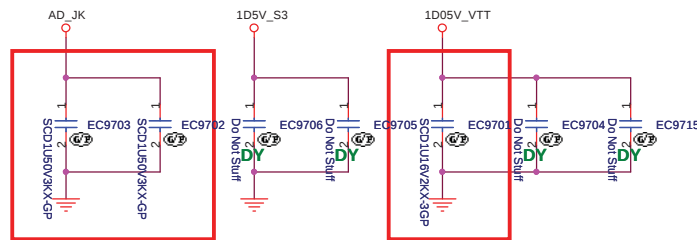
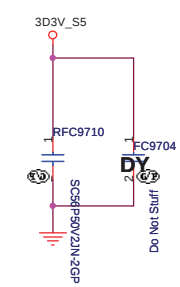
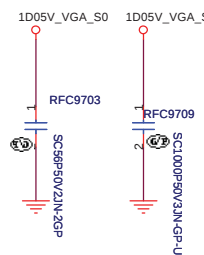
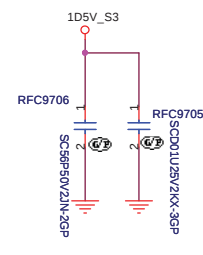
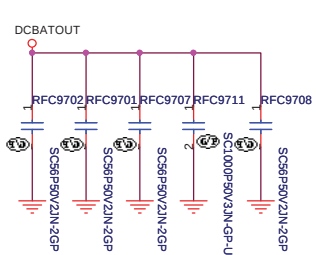
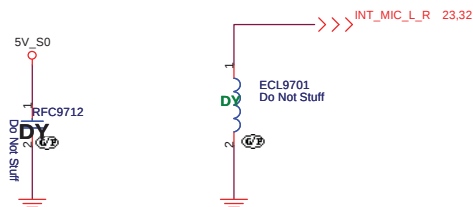
Rev

-1

Date: Wednesday, November 24, 2010

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20100920
<http://hobi-elektronika.net>

Check test point

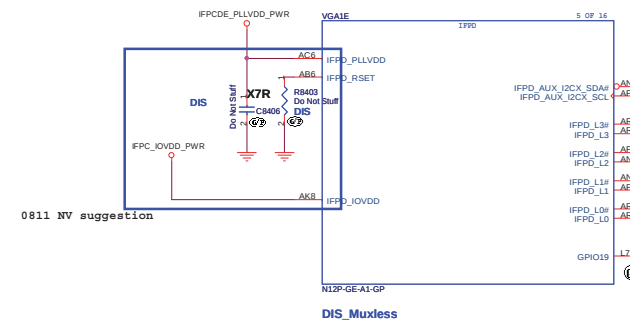
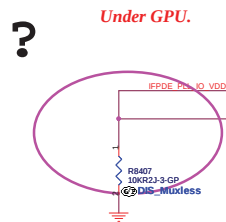
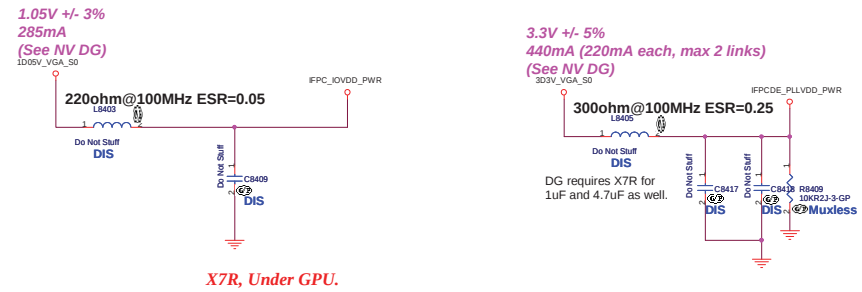
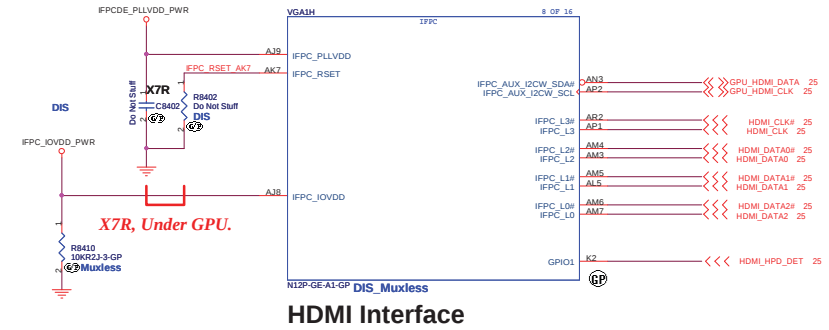
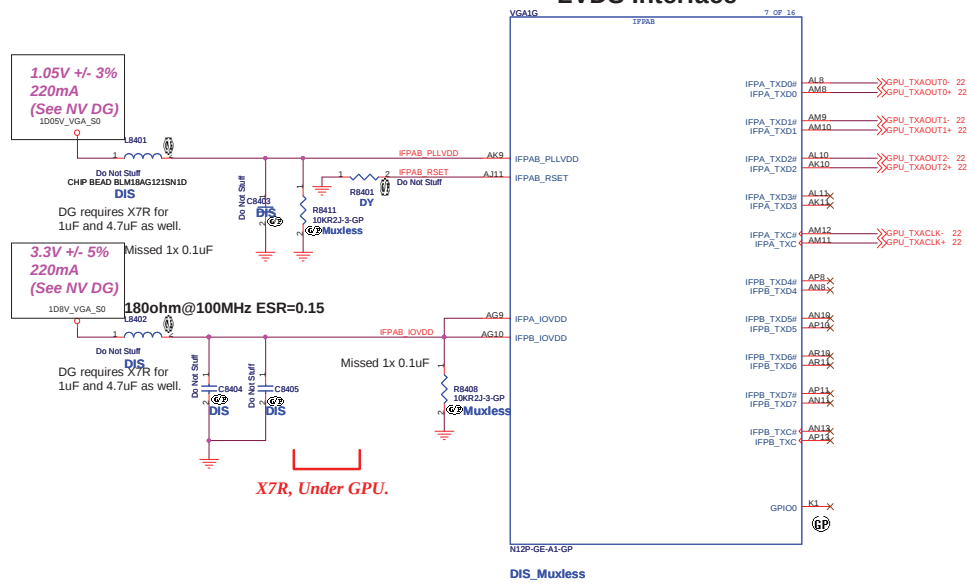
~~delete 3D3V_S0 test point~~



Test Point放在Dimm Door打開可量測處



LVDS Interface

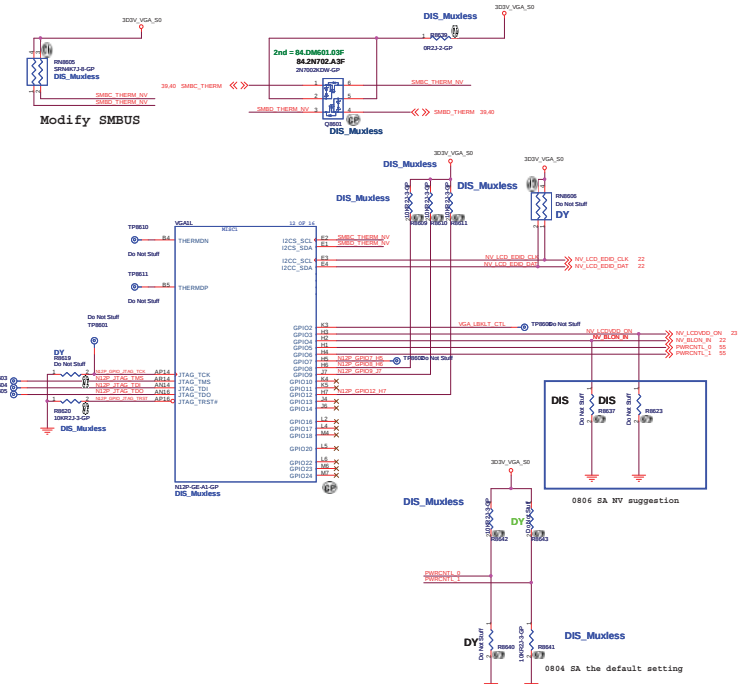


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Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation	
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPU DIGITAL_OUT(2/5)	
Size	Document Number JE43-CP
Customer	Rev -1
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VGA Thermal sensor 787



NVIDIA TABLE

	Hynix 2G 0010 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 0011 64*16*4 800MHZ	Samsung 2G 0011 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

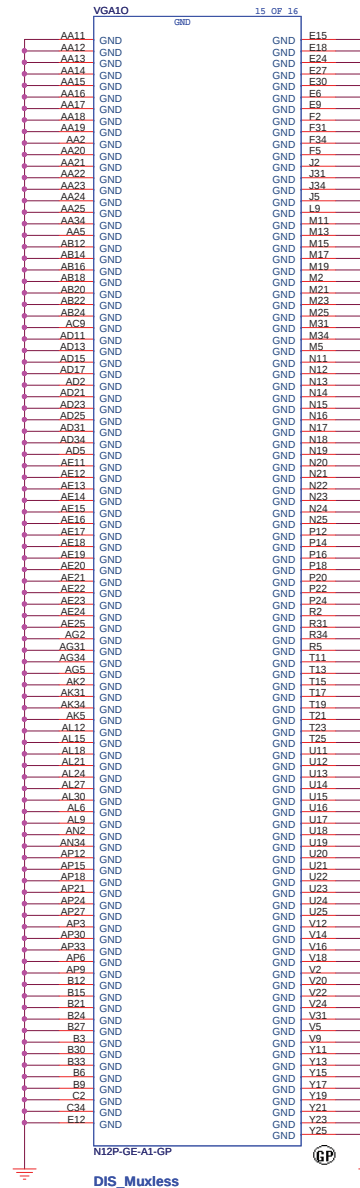
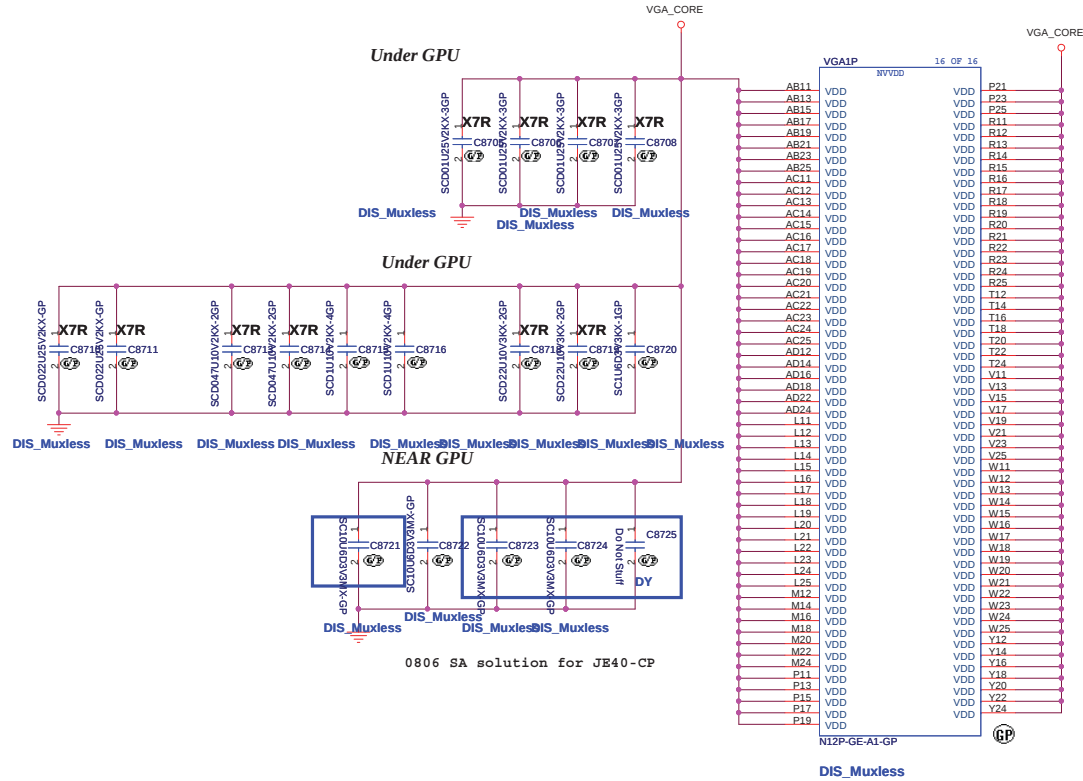
GPU_ROM_S1	for 10bit	for 20bit	for 10bit	for 20bit	Logical Strap Bit Mapping
					Resistor Pull-up Pull-down
					150ohm 1000 0000
					150ohm 1001 0001
					150ohm 1010 0010
					150ohm 1011 0011
					150ohm 1100 0100
					150ohm 1101 0101
					150ohm 1110 0110
					150ohm 1111 0111

TABLE

NVIDIA	71.0N12P.E0U	71.0N12P.A0U			
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x0DF7	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GV DEV ID: 0x0DF5 (0101)
STRAP2 PU R8634	25Kohm 64.24925.6DL	45Kohm 64.45325.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

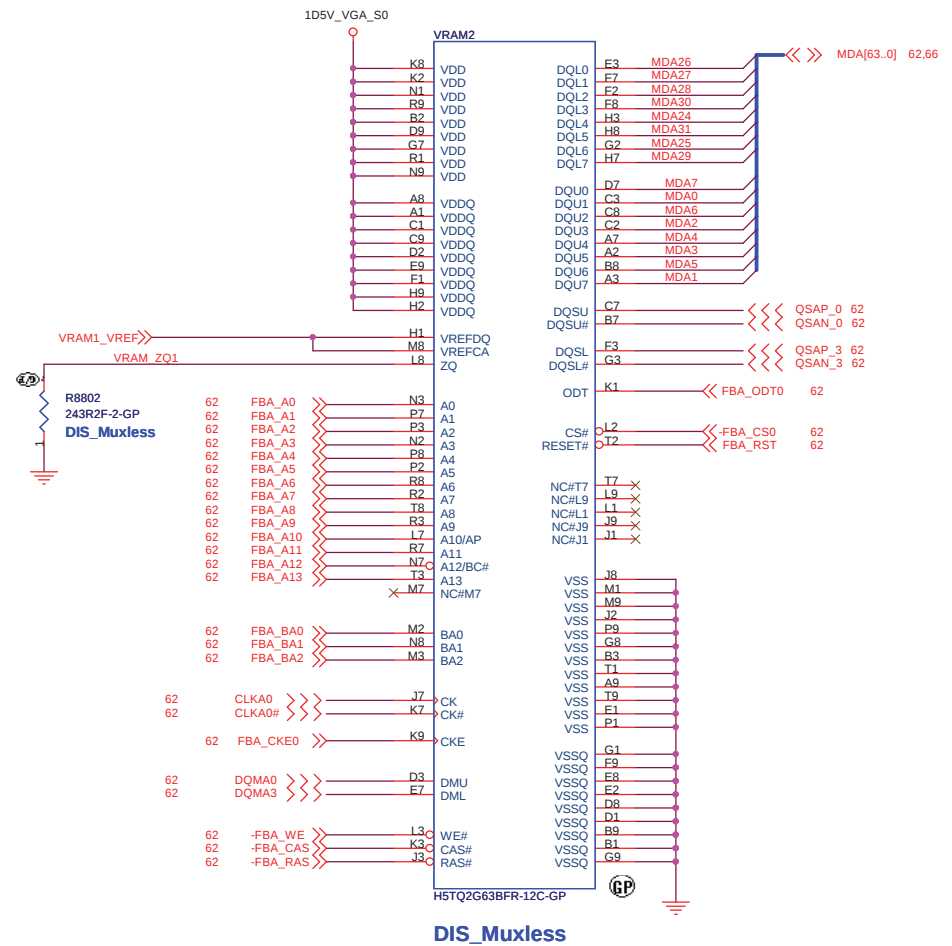
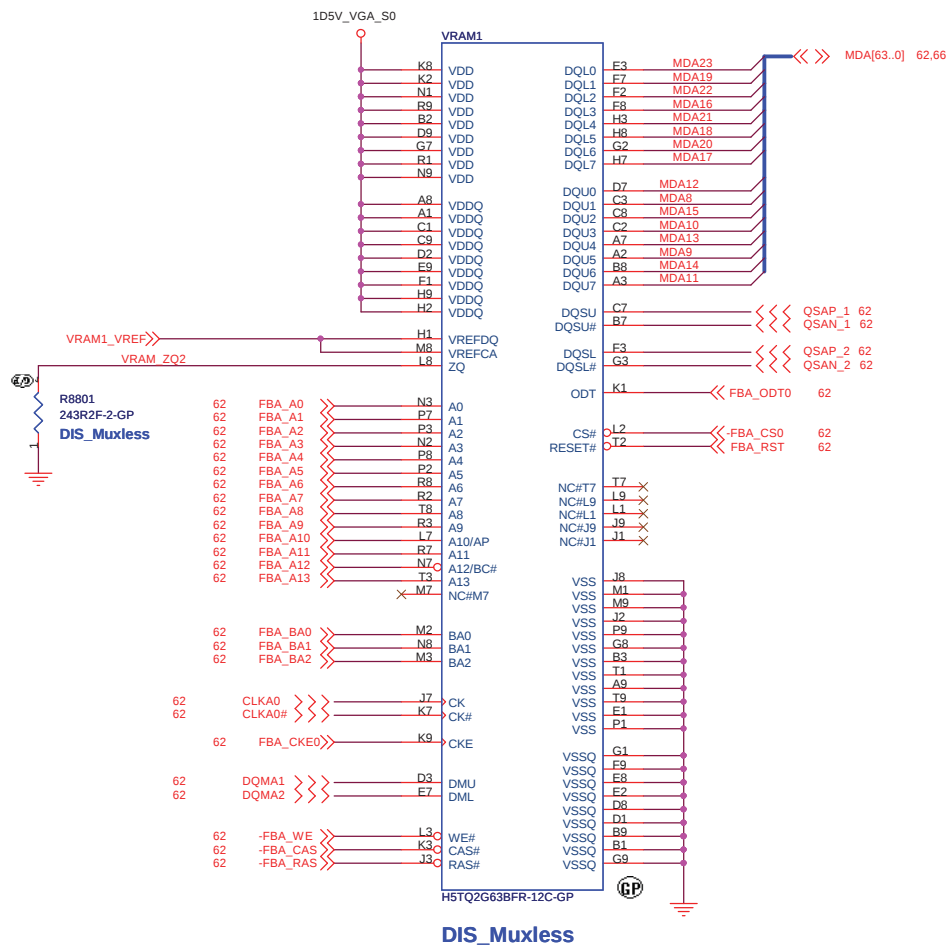
STRAP0	USER[0]=1 USER[2]=1 USER[3]=1	N12P-GS USE 1111 (45K)	N12P-GV	N11P-GE Pull Low	N11P-GS Pull Low	N12P-GE
STRAP1	3GIO_PADCPU[0]=0 3GIO_PADCPU[1]=1 3GIO_PADCPU[2]=1 3GIO_PADCPU[3]=1	USE 0110 (35K)				
STRAP2	PCI_DRVID[0]=1 PCI_DRVID[1]=1 PCI_DRVID[2]=1 PCI_DRVID[3]=1	N12P-GS N12P-GV N11P-GE Fermi N11P-GS Fermi	0x0DF4 (0x4) 0x0DF7 (0x7) 0x0DF0 (0x0) 0x0DF1 (0x1)			

EDP 50A (TDP 37W)

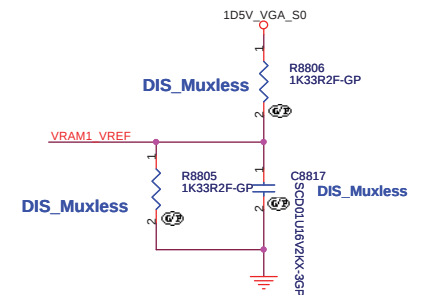
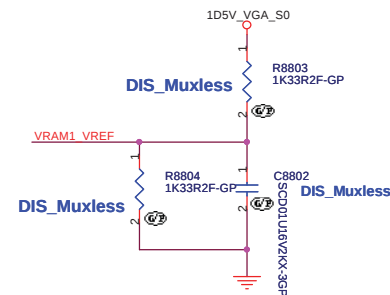
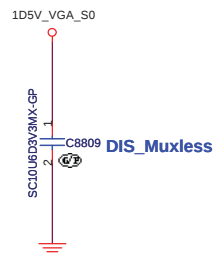
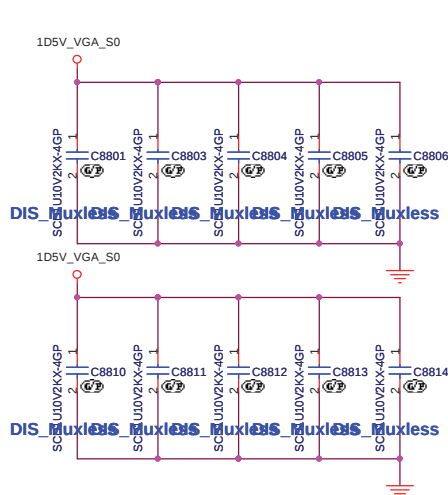


Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU DPPWR/GND(5/5)			
Size	Document Number	Rev	
Custom	JE43-CP	-1	
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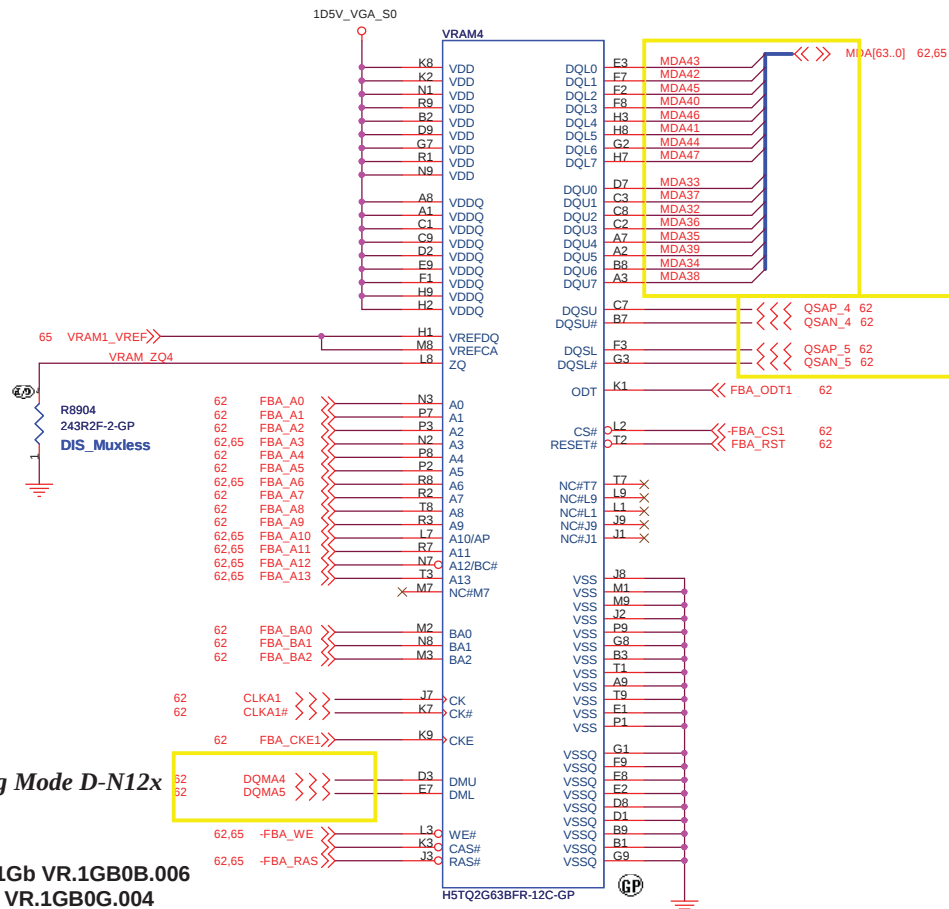
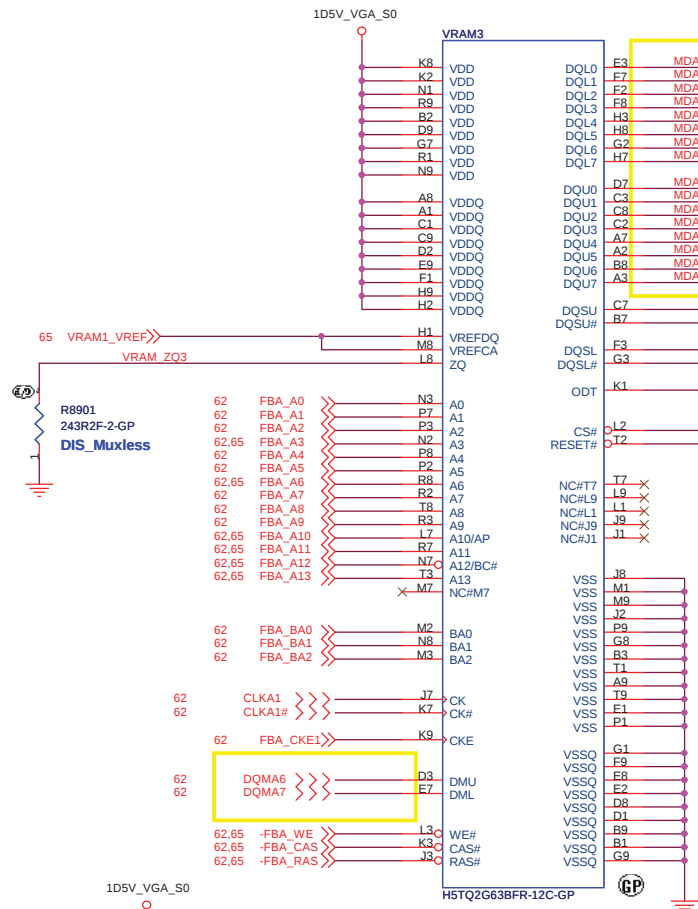
Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX4_VR.1GB0G.004,Sam512X4_VR.1GB0B.006



Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
GPU-VRAM1,2 (1/4)	
Size A3	Document Number
	JE43-CP
Date: Wednesday, November 24, 2010	Sheet 65 of 69

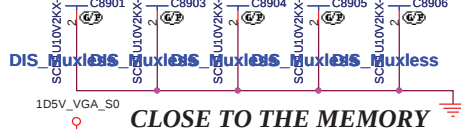
<http://hobi-elektronika.net>



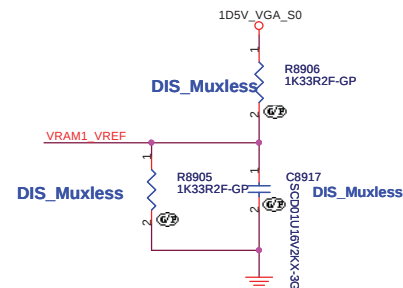
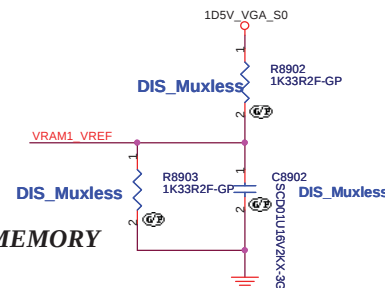
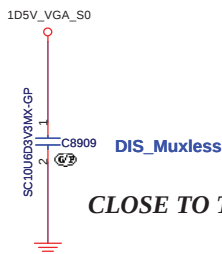
FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb VR.1GB0G.004
VRAM HYNIX 2Gb VR.2GB0G.001

FOR VRAM3



FOR VRAM4

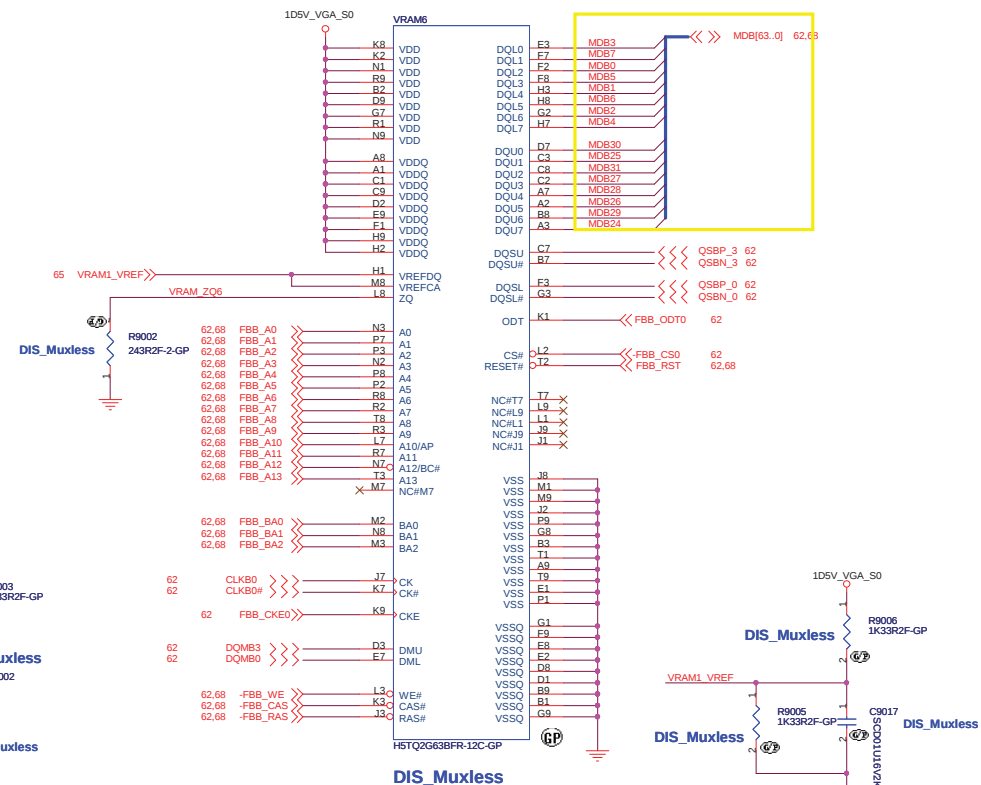


Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

GPU-VRAM3,4 (2/4)			
Size A3	Document Number	JE43-CP	
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<http://hobi-elektronika.net>

[illegible]

1D5V_VGA_S0

SC10U6D3V3MX-GP

C9009 DIS_Muxless

CLOSE TO THE MEMORY

Hyrix 1G 800M N11PGV SKU

緯創資通

Wistron Corporation

235, 88, Sec.1, Hsuan Tai Wu Rd., Hsuehshih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Modify History		
Size	Document Number	Rev
JE43-CP		-1
Date: Wednesday, November 24, 2010		Sheet 69 of 69