

COMPAL CONFIDENTIAL

MODEL NAME : *NLM01*
PCB NO : *LA-6132P (DA80000I500) DAZ0DD00200*
BOM P/N : *43185331L01 (K325)*
43185331L02 (K125)
43185331L03 (V105)

M10 Andros
AMD ASB2/ RS880M / SB820M

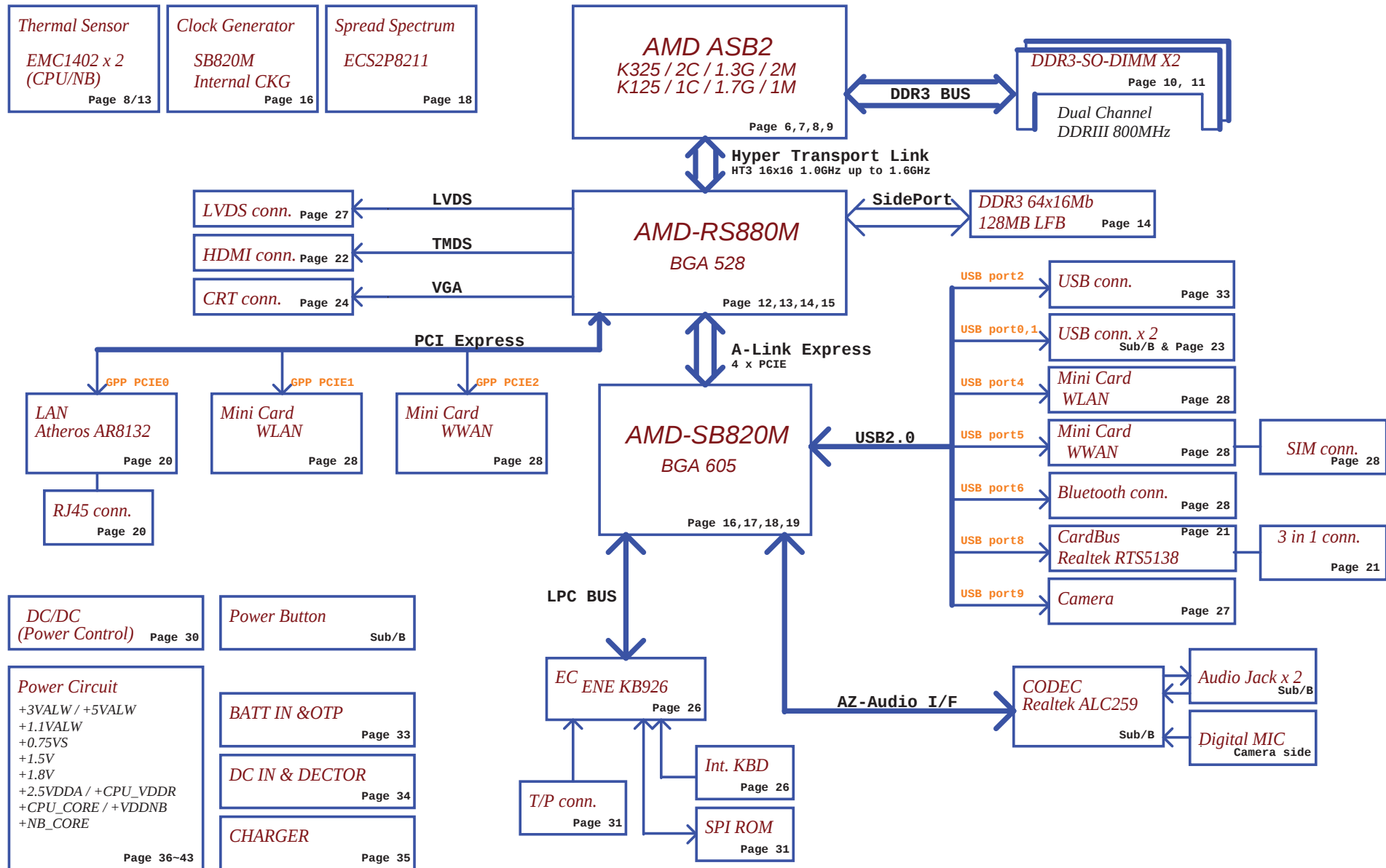
2010 - 05 - 11
REV : 1.0(A00)

@ : Nopop Component
WWAN@: WWAN function
NONWWAN@: NON WWAN function
CONN@: Connector only

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	ON
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	B+ +5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.1VS +0.75VS +2.5VDDA +CPU_VDDR +NB_CORE +CPU_CORE +VDDNB
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

SB820M

USB PORT#	DESTINATION
0	USB (Right)
1	USB (Right)
2	USB (Left)
3	None
4	MINI CARD - WLAN
5	MINI CARD - WWAN
6	Bloetooth
7	None
8	Card Reader
9	Camera
10	None
11	None
12	None
13	None

RS880M

PCIE	DESTINATION
Lane 1	10 / 100 LAN
Lane 2	MINI CARD - WLAN
Lane 3	MINI CARD - WWAN
Lane 4	None
Lane 5	None

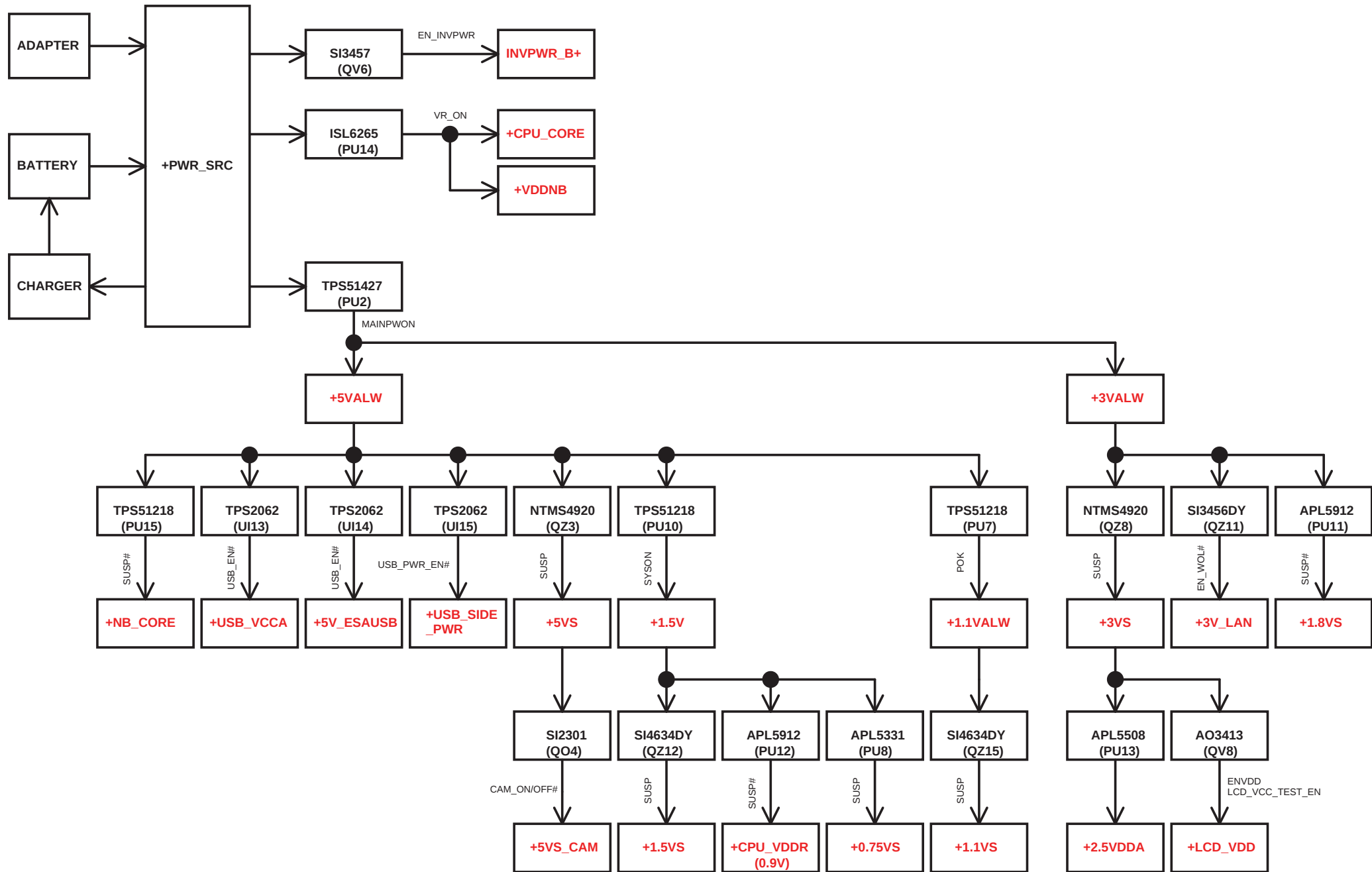
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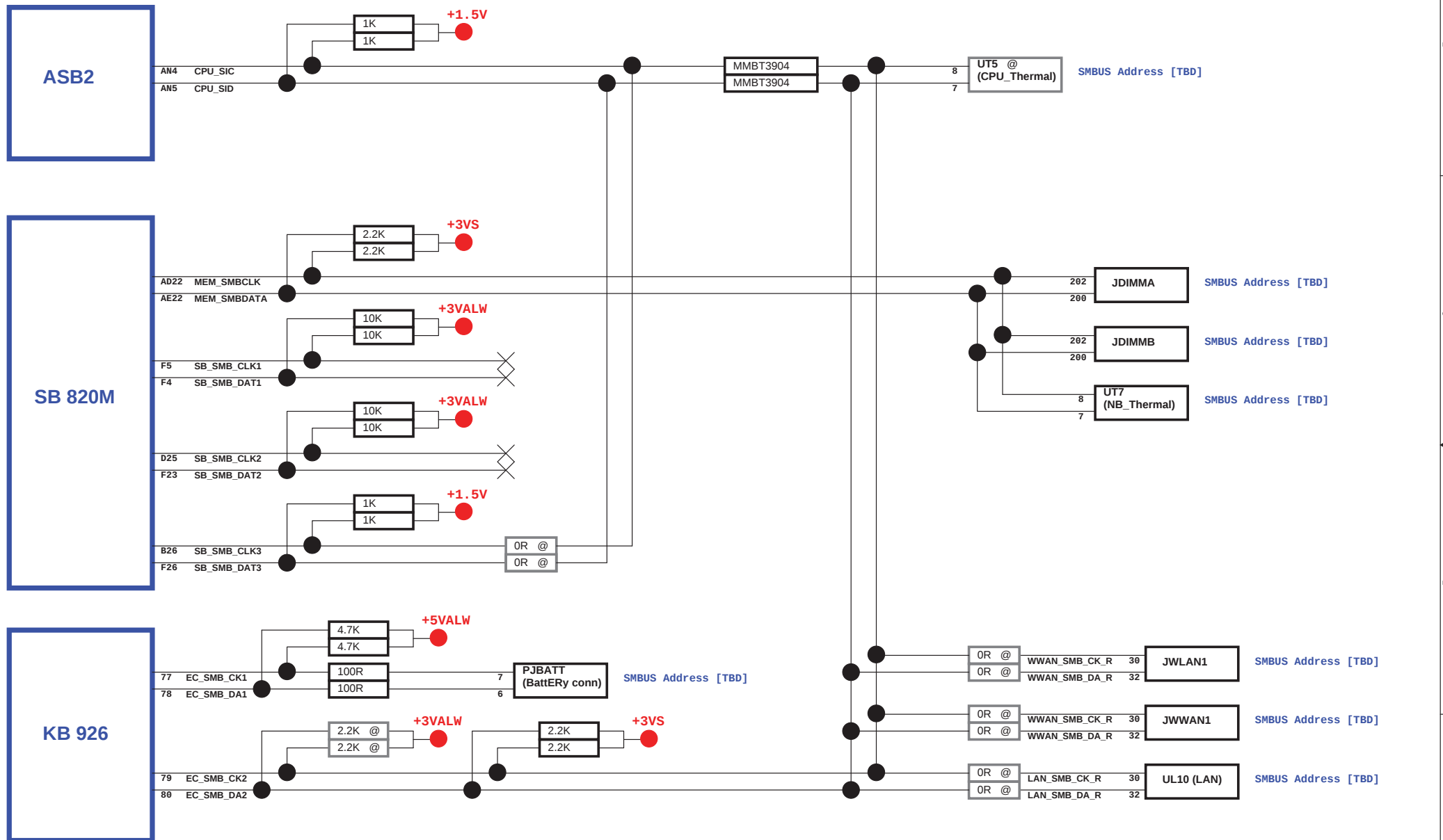


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Power Rail			
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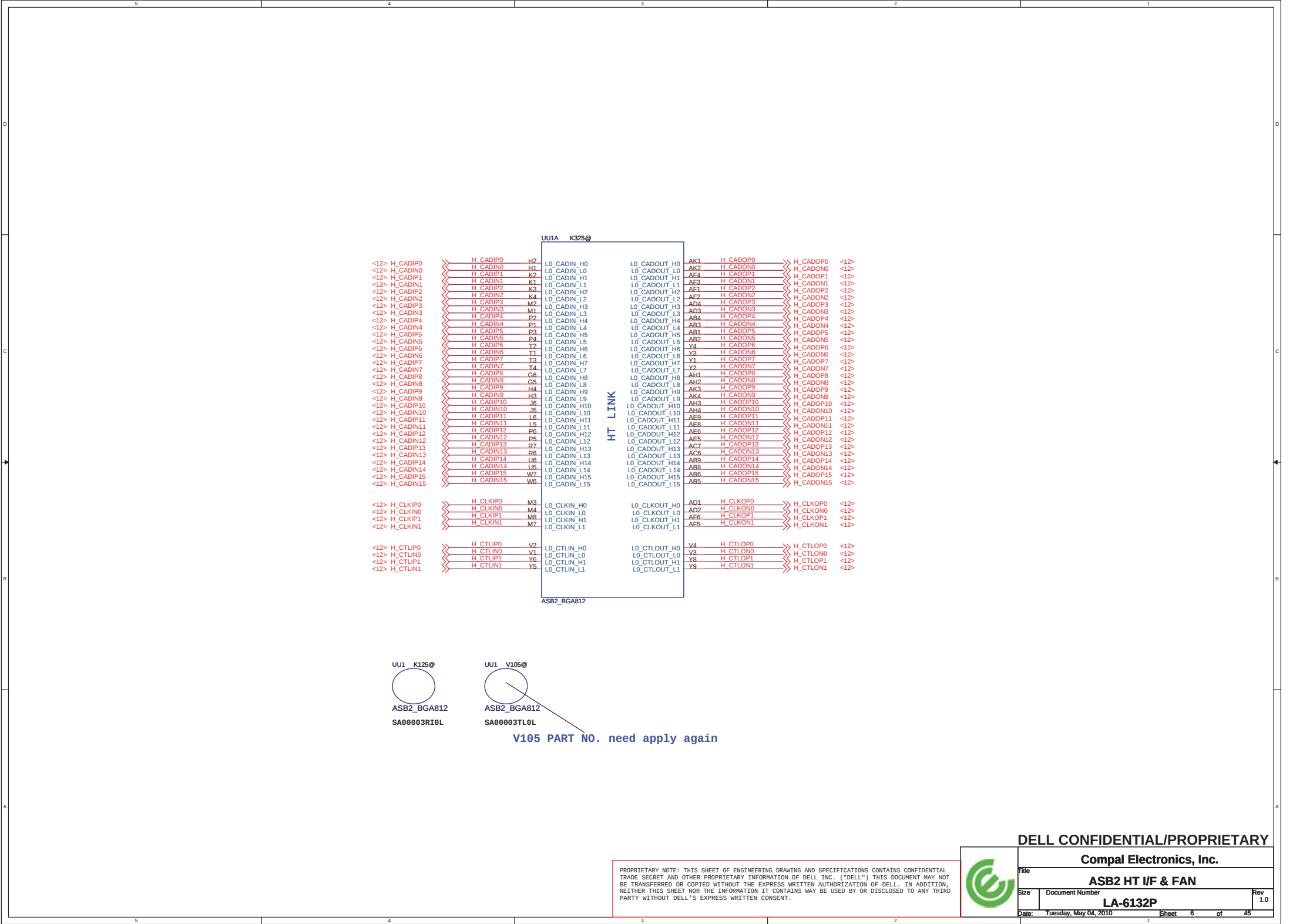


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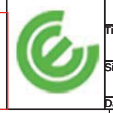


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SMBus Topology			
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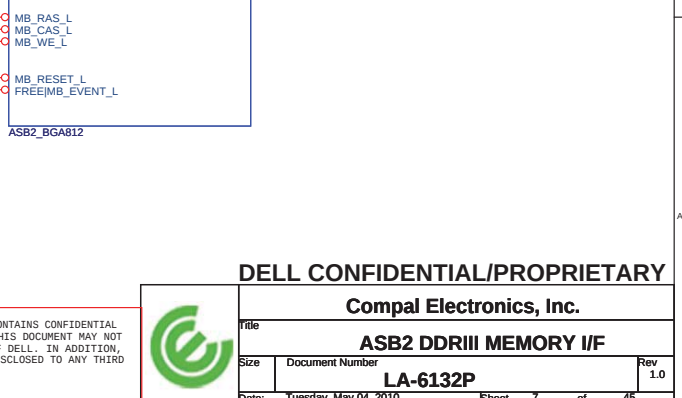
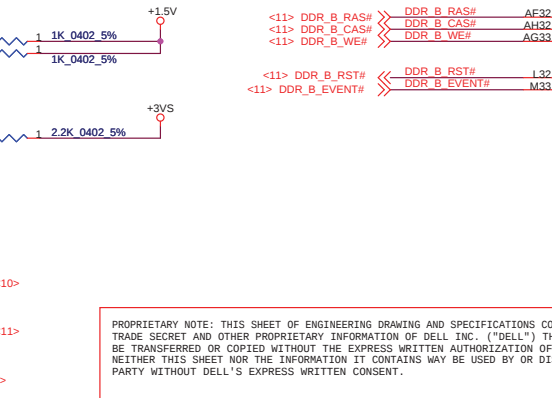
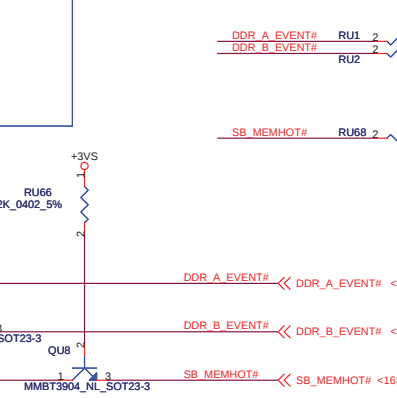
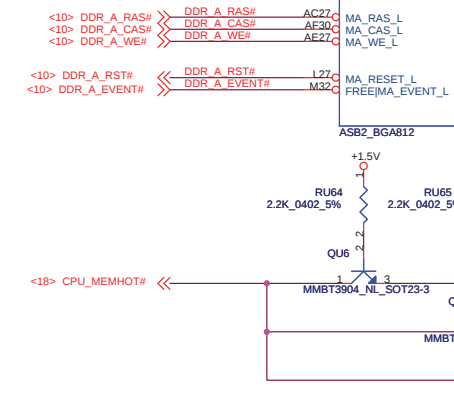
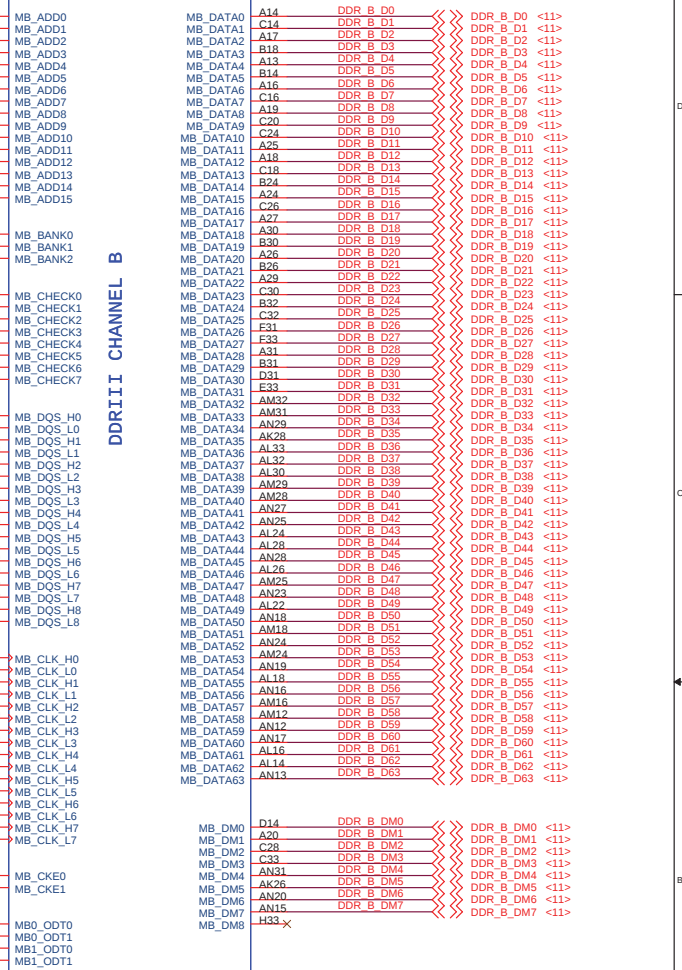
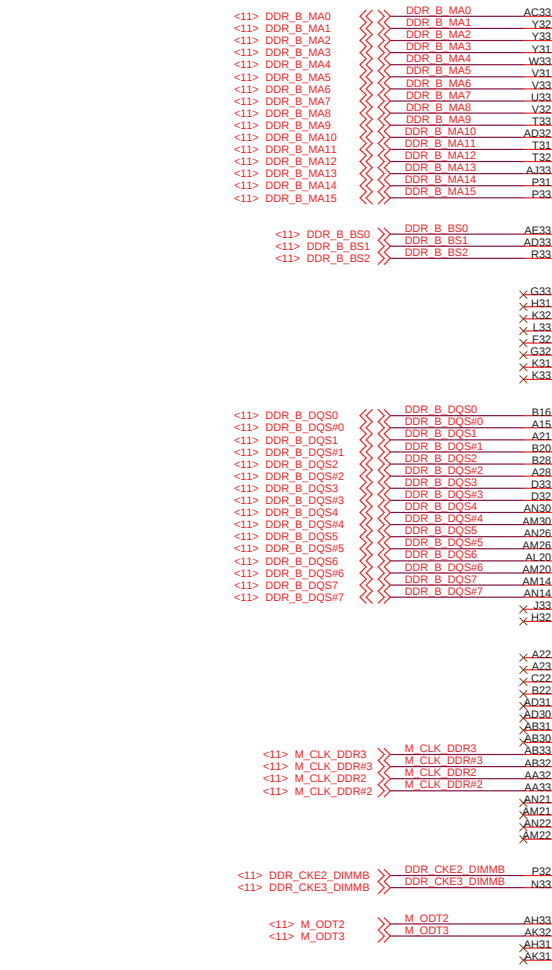
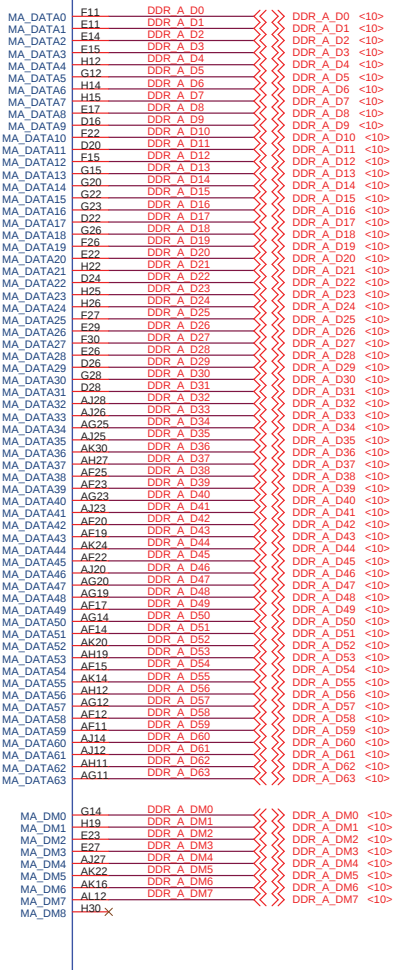
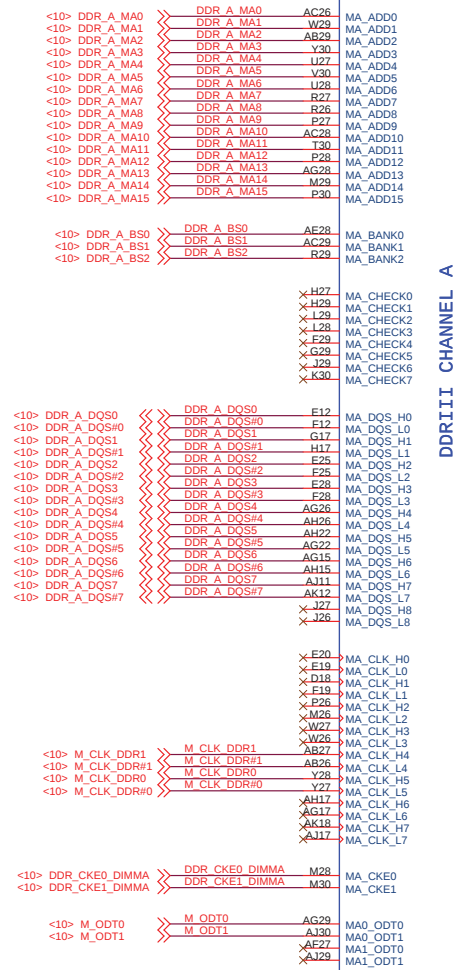
Processor DDR3 Memory Interface

UUIB K325@

UUIB K325@

DDR11 CHANNEL A

DDR11 CHANNEL B

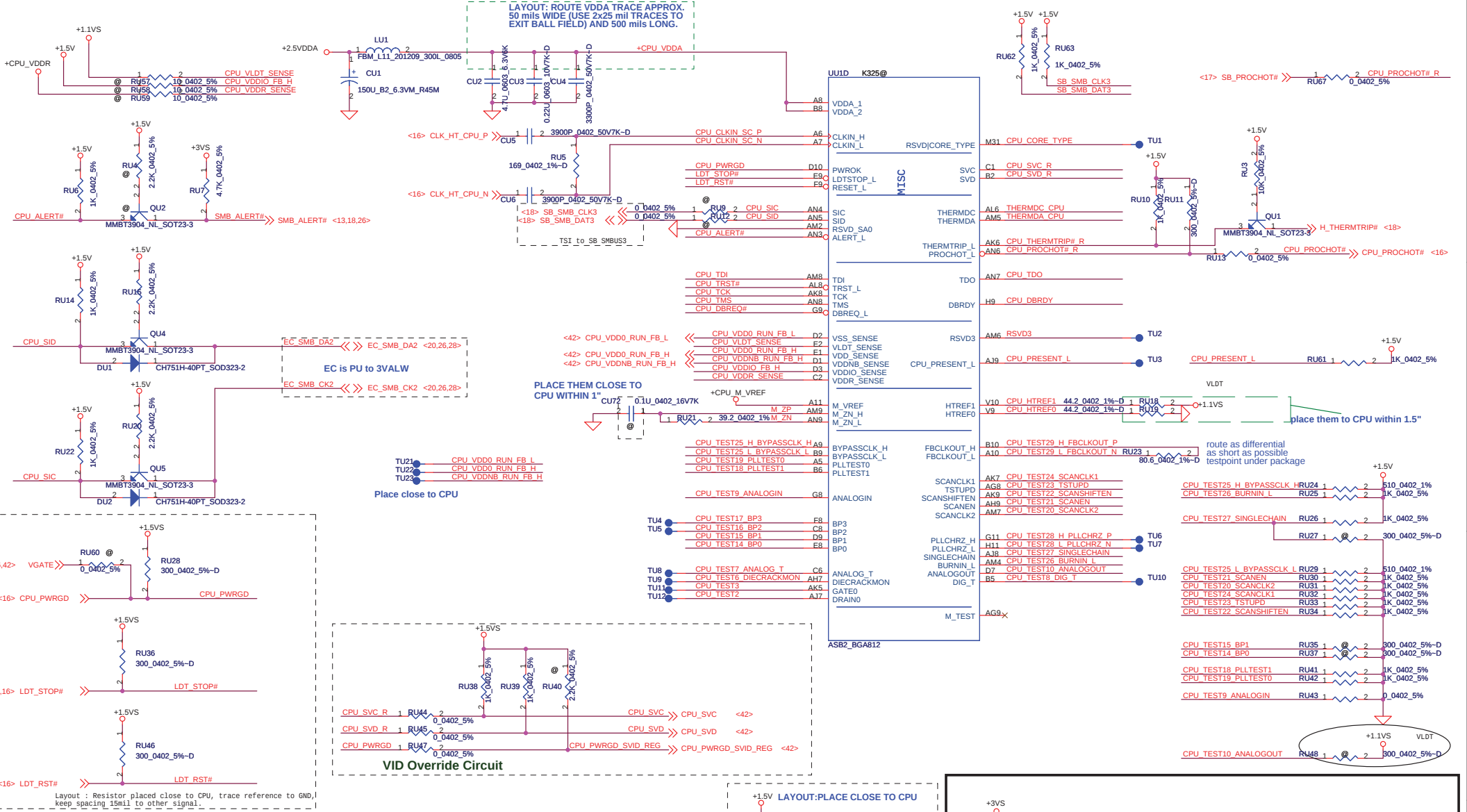


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ASB2 DDR11 MEMORY I/F	
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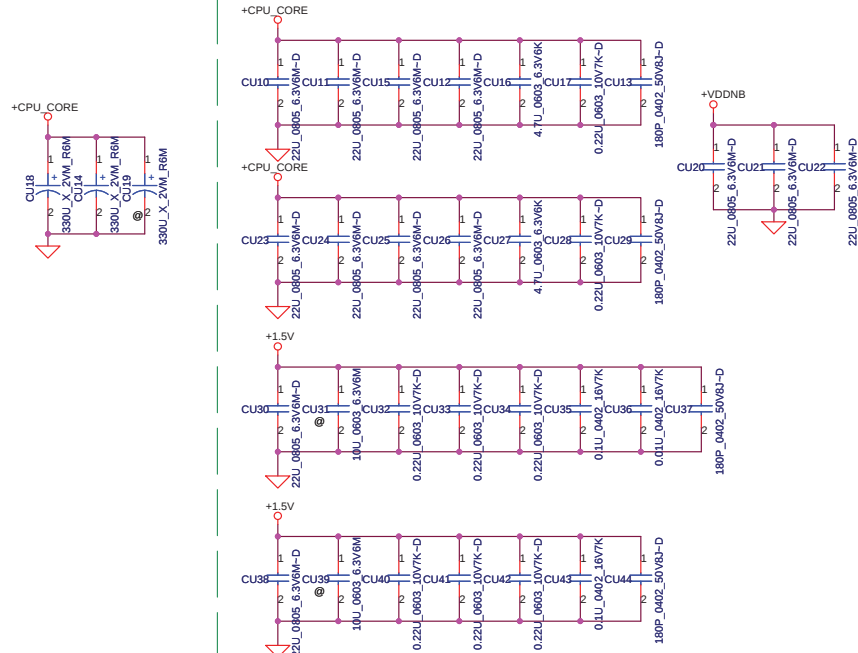
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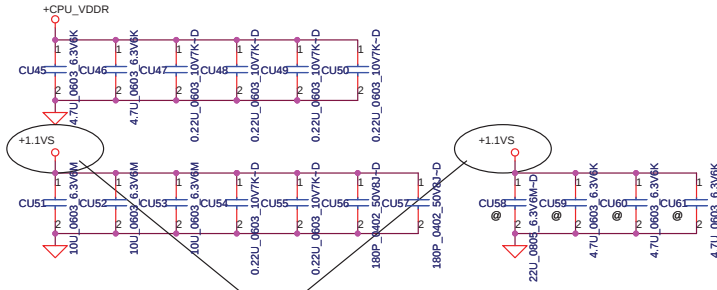
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CPU BOTTOMSIDE DECOUPLING

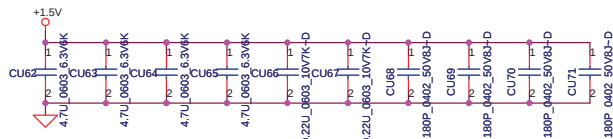


Place close to CPU

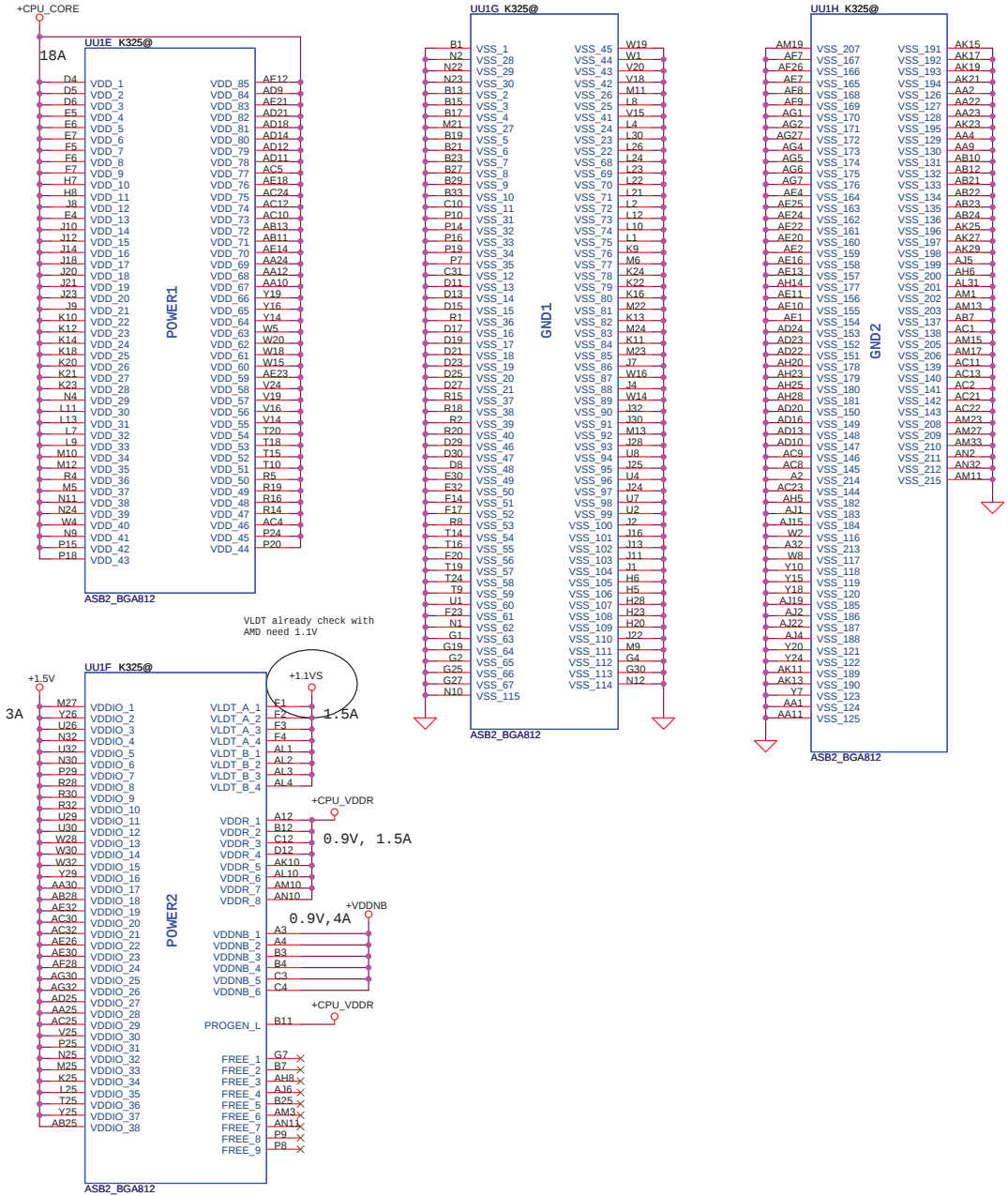


Placement need check

DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



Need discuss with AMD



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ASB2 PWR & GND

LA-6132P

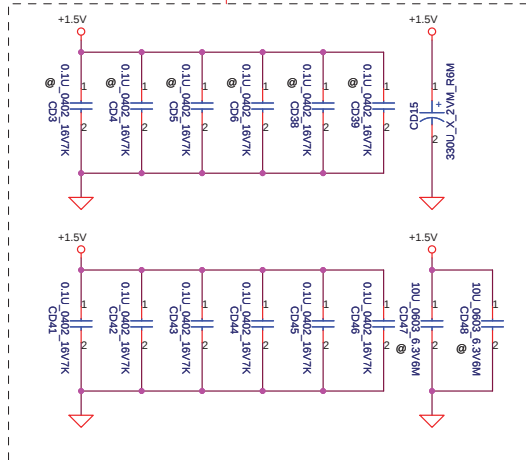
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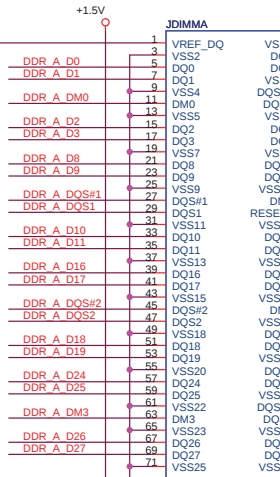
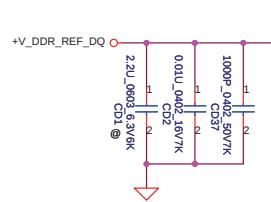
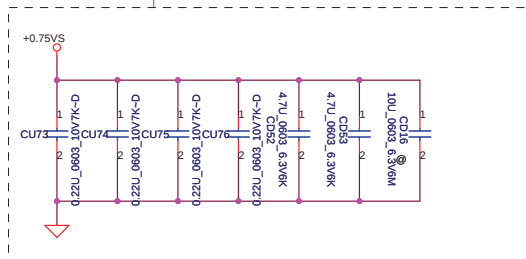
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<7> DDR_A_MA4 <> DDR_A_MA4
<7> DDR_A_MA5 <> DDR_A_MA5
<7> DDR_A_MA6 <> DDR_A_MA6
<7> DDR_A_MA7 <> DDR_A_MA7
<7> DDR_A_MA8 <> DDR_A_MA8
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Layout Note:
Place near JDIMMA



Layout Note:
Place near JDIMMA.203,204



<7> DDR_CKE0_DIMMA <> DDR_CKE0_DIMMA

<7> DDR_A_BS2 <> DDR_A_BS2

<7> M_CLK_DDR0 <> M_CLK_DDR0

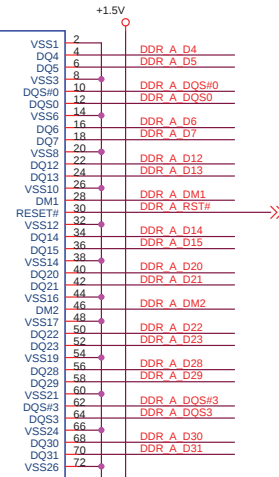
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<7> DDR_A_BS0 <> DDR_A_BS0

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<7> DDR_A_CAS# <> DDR_A_CAS#

<7> DDR_CS1_DIMMA# <> DDR_CS1_DIMMA#



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<7> M_CLK_DDR1 <> M_CLK_DDR1

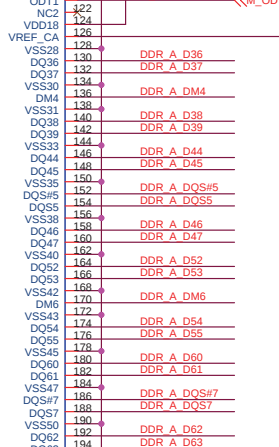
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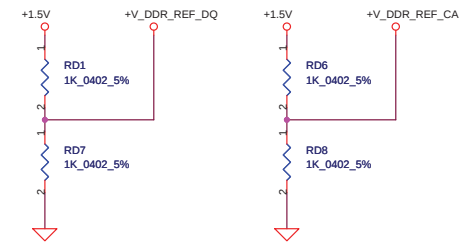
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SP07000J500

REVERSE TYPE

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DDRIII DIMM A

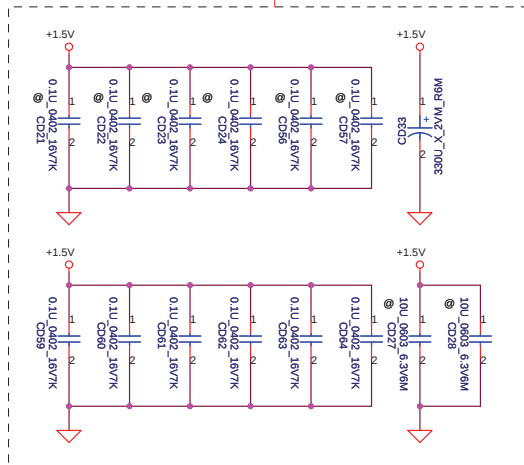
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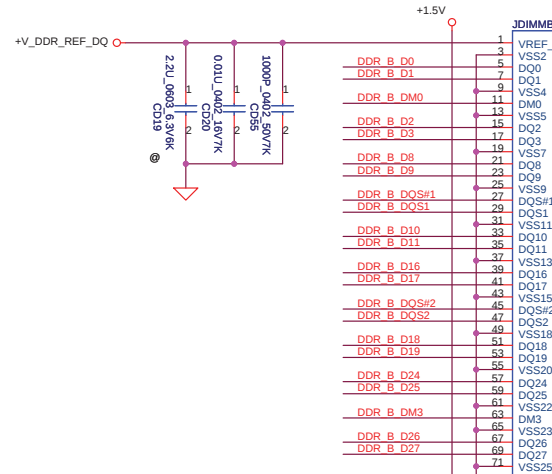
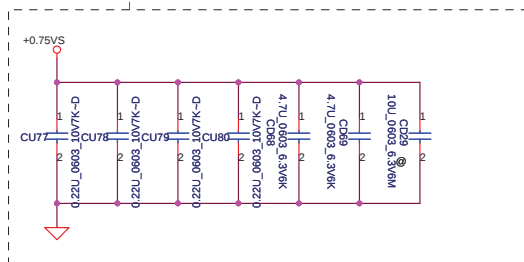
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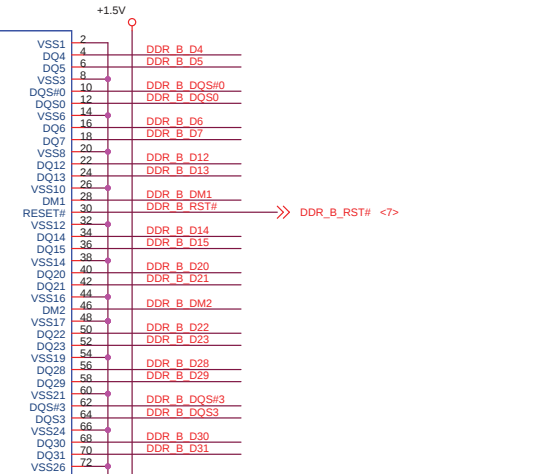
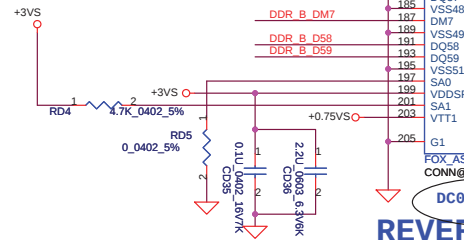
Layout Note:
Place near JDIMMB



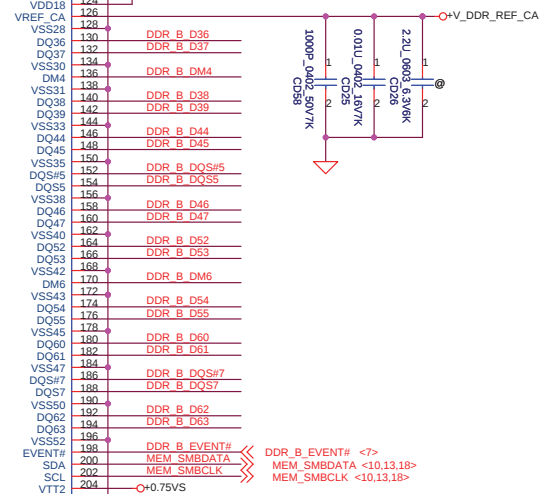
Layout Note:
Place near JDIMMB.203,204



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<7> DDR_B_BS0 DDR_B_BS0
<7> DDR_B_WE# DDR_B_WE#
<7> DDR_B_CAS# DDR_B_CAS#
<7> DDR_CS3_DIMMB# DDR_CS3_DIMMB#



<7> DDR_CKE3_DIMMB# DDR_CKE3_DIMMB#
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<7> M_ODT2 M_ODT2
<7> M_ODT3 M_ODT3



DDR_B_D0 DDR_B_D0
DDR_B_D1 DDR_B_D1
DDR_B_D2 DDR_B_D2
DDR_B_D3 DDR_B_D3
DDR_B_D4 DDR_B_D4
DDR_B_D5 DDR_B_D5
DDR_B_D6 DDR_B_D6
DDR_B_D7 DDR_B_D7
DDR_B_D8 DDR_B_D8
DDR_B_D9 DDR_B_D9
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DDR_B_DM0 DDR_B_DM0
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DDR_B_DM3 DDR_B_DM3
DDR_B_DM4 DDR_B_DM4
DDR_B_DM5 DDR_B_DM5
DDR_B_DM6 DDR_B_DM6
DDR_B_DM7 DDR_B_DM7

REVERSE TYPE

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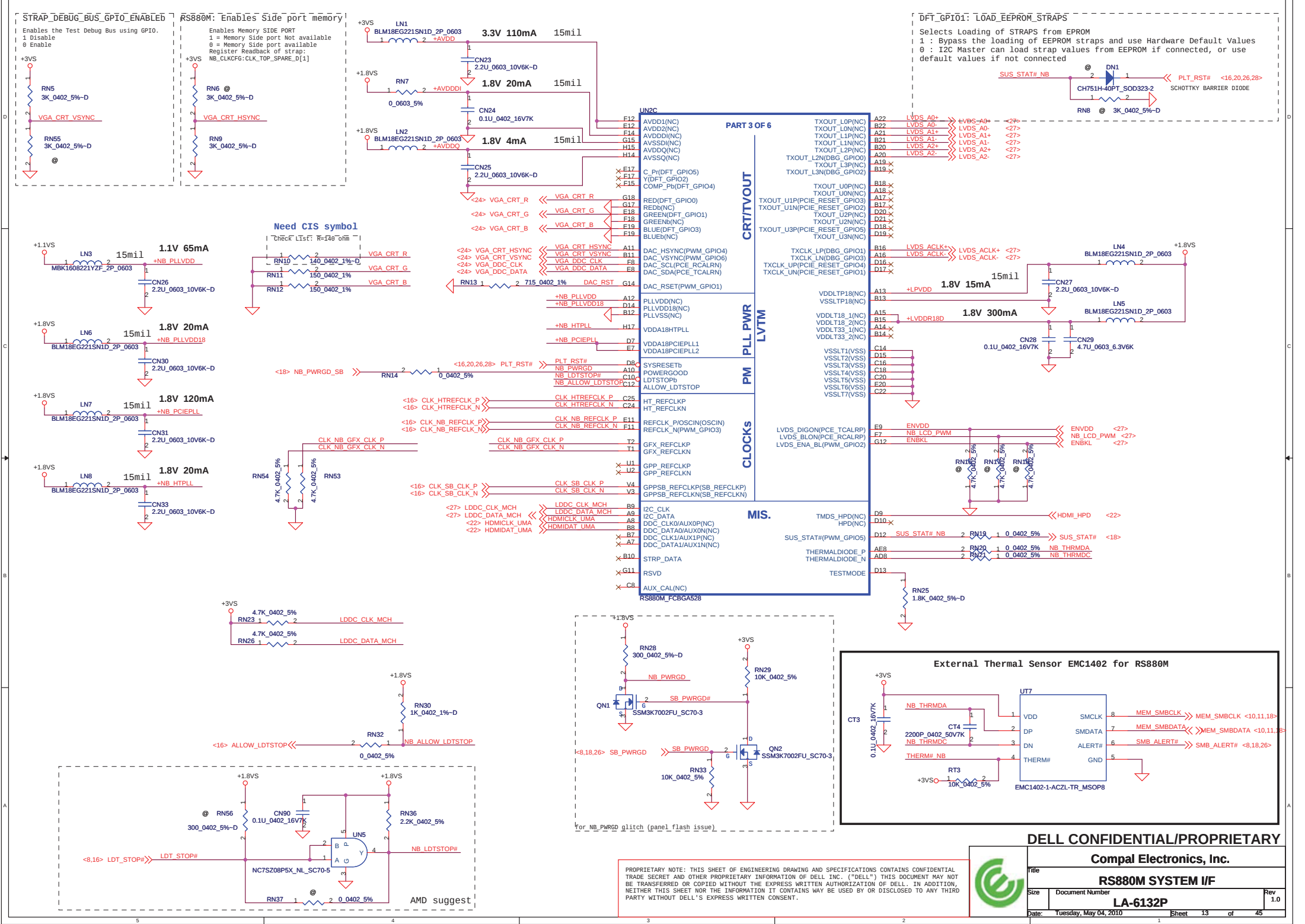
Compal Electronics, Inc.

DDRIII DIMM B

LA-6132P

Rev 1.0

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Compal Electronics, Inc.

RS880M SYSTEM I/F

LA-6132P

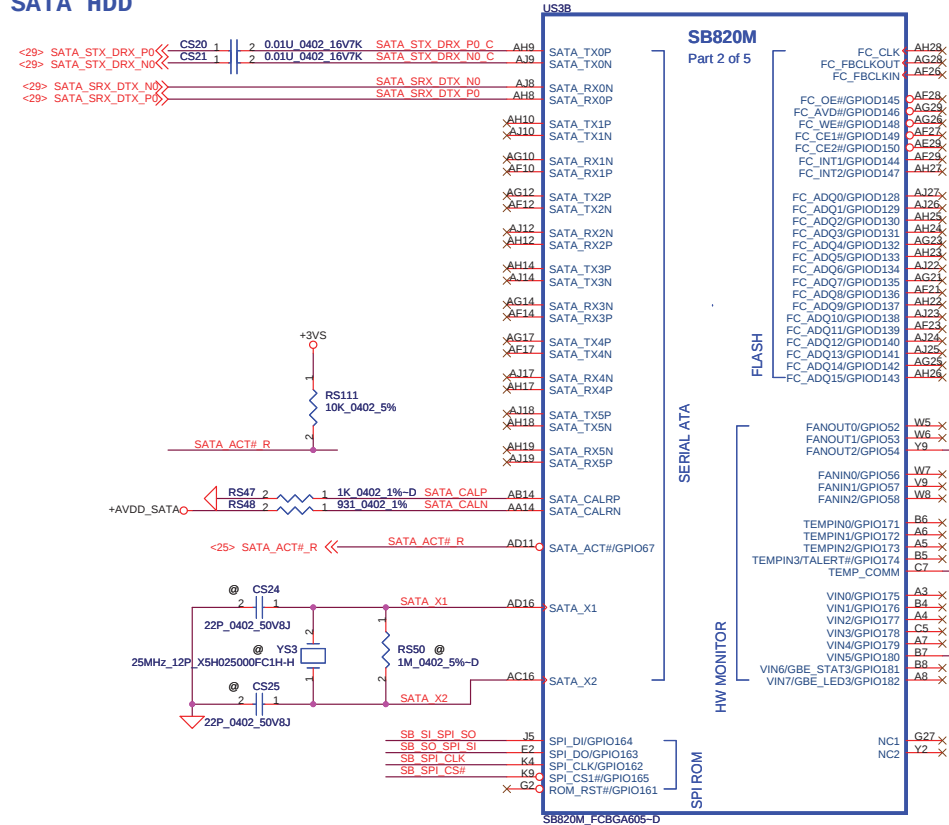
Rev 1.0

Date: Tuesday, May 04, 2010 Sheet 13 of 45

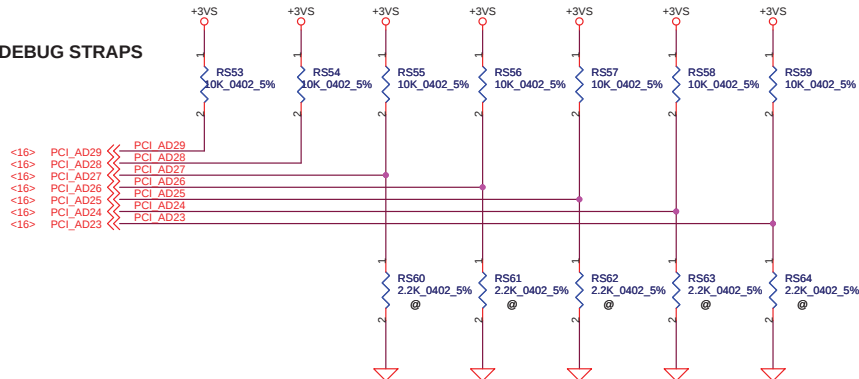


Rev	
1.0	

SATA HDD



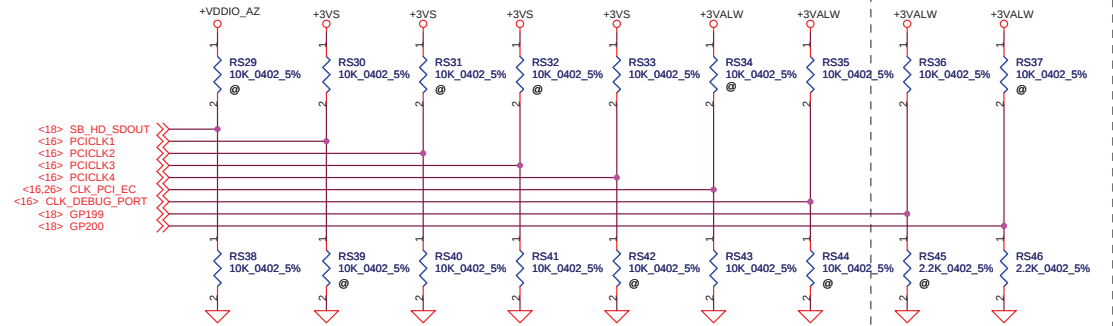
DEBUG STRAPS



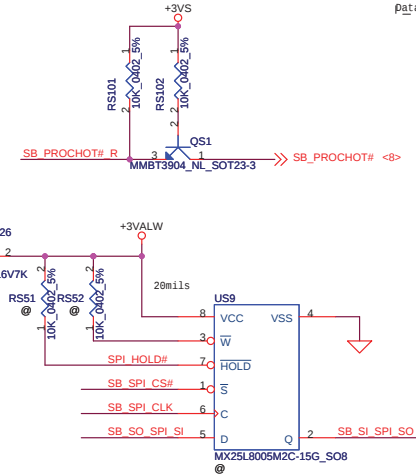
SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PULL HIGH	SB_HD_SDOUT	PCICLK1	PCICLK2	PCICLK3	PCICLK4	CLK_PCI_EC	CLK_DEBUG_PORT	GPIO200	GPIO199
	LOW POWER MODE DEFAULT	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled DEFAULT	USE DEBUG STRAP DEFAULT	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT		
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED		

REQUIRED STRAPS



check list: LCP ROM: GP199=NC, GP298=PD
Datasheet: LCP ROM: GP199=PU, GP298=PD



PULL HIGH	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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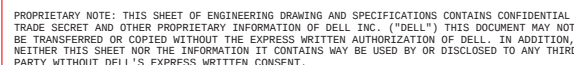
Compal Electronics, Inc.

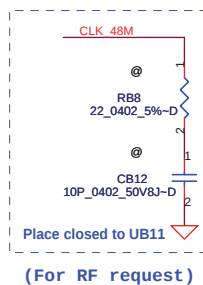
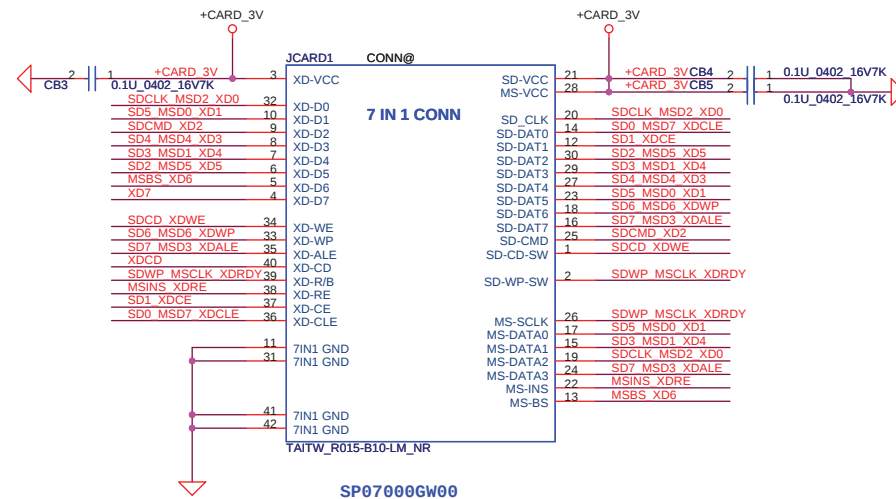


SB820M SATA/FLASH/Strap		Rev 1.0
Size	Document Number	
LA-6132P		
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Compal Electronics, Inc.

Card Reader RTS5138

LA-6132P

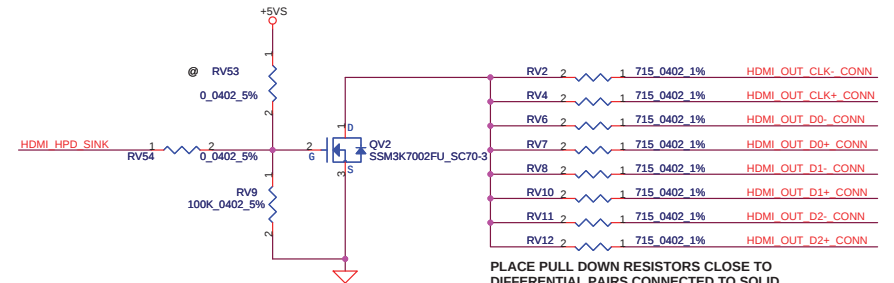
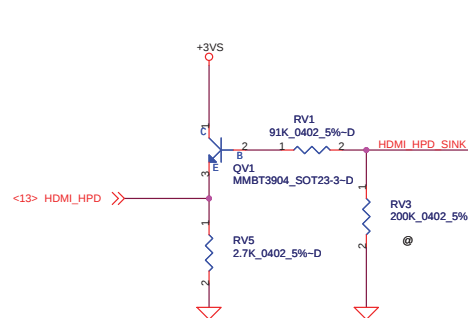
Rev
1.0

Date: Tuesday, May 04, 2010 Sheet 21 of 45

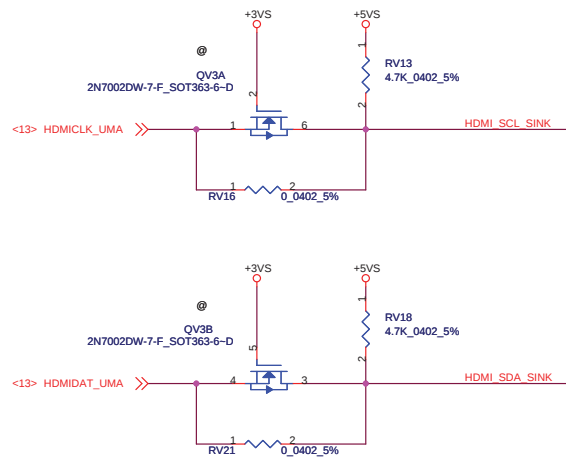
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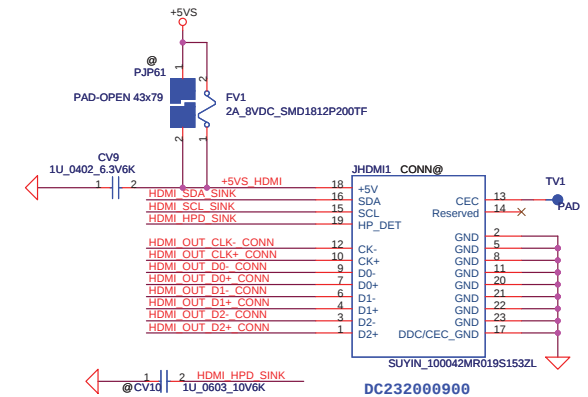
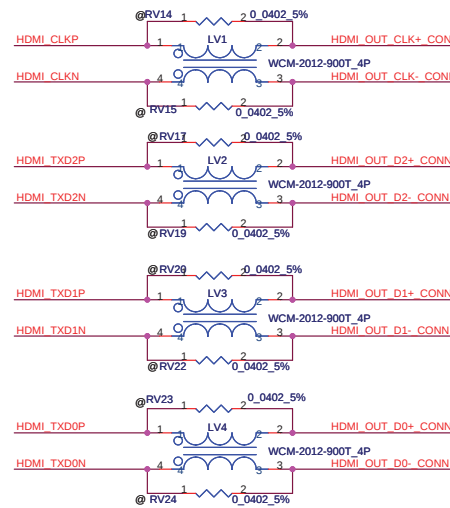
<12> HDMI_TXD2P >> HDMI_TXD2P
 <12> HDMI_TXD2N >> HDMI_TXD2N
 <12> HDMI_TXD1P >> HDMI_TXD1P
 <12> HDMI_TXD1N >> HDMI_TXD1N
 <12> HDMI_TXD0P >> HDMI_TXD0P
 <12> HDMI_TXD0N >> HDMI_TXD0N
 <12> HDMI_CLKP >> HDMI_CLKP
 <12> HDMI_CLKN >> HDMI_CLKN



PLACE PULL DOWN RESISTORS CLOSE TO
 DIFFERENTIAL PAIRS CONNECTED TO SOLID
 GROUND FLOOD WHICH IS CONTROLLED
 BY THE FET
 AVOID STUBS TO ALL DIFFERENTIAL TRACES



Place close JHDMI1



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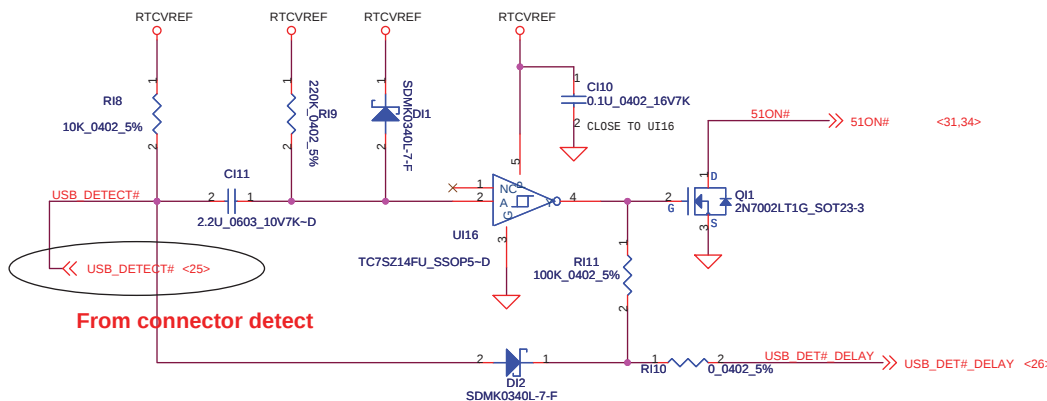
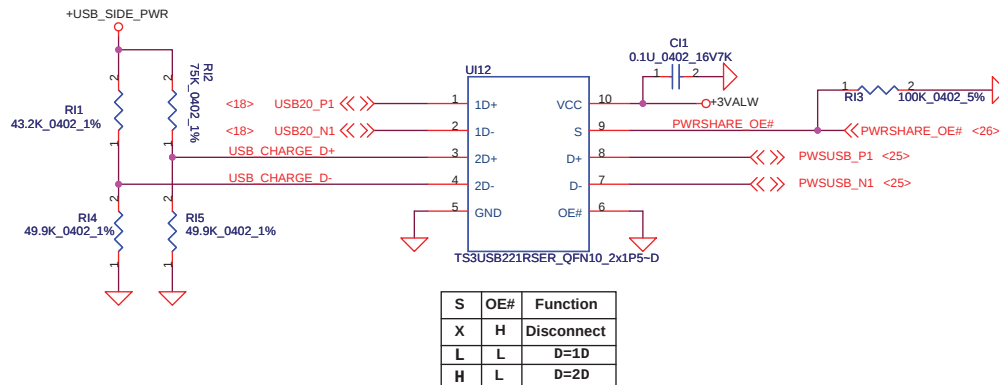
Compal Electronics, Inc.

HDMI Conn.

LA-6132P

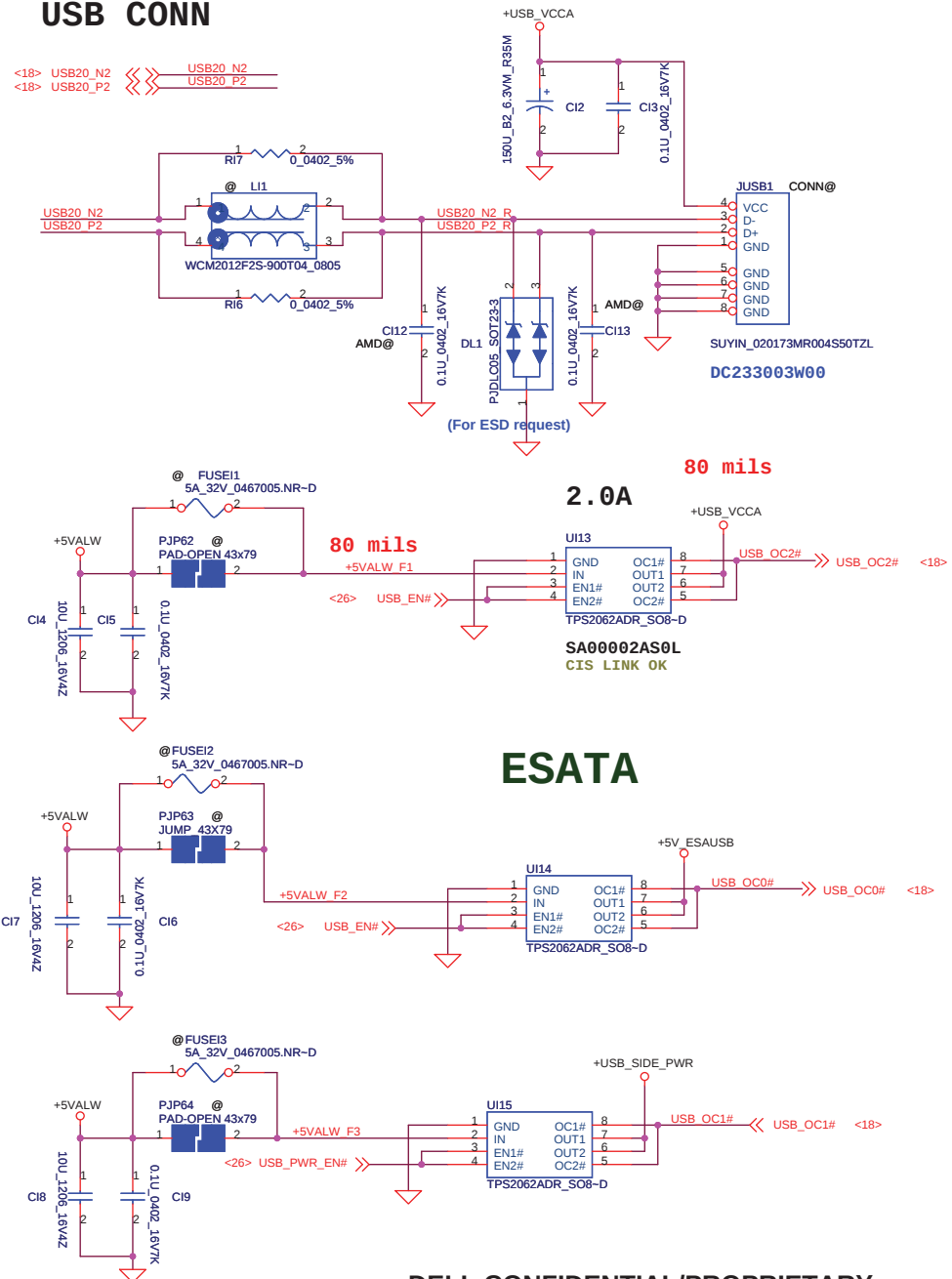
Date: Tuesday, May 04, 2010 Sheet 22 of 45

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Power share

USB CONN



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Compal Electronics, Inc.			
Title			
USB/POWER Share			
Size	Document Number		Rev
	LA-6132P		1.0
Date	Tuesday, May 04, 2010		Sheet 23 of 45

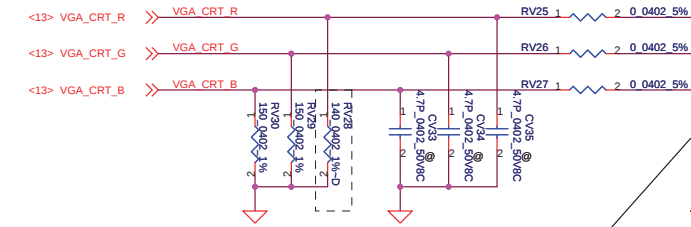
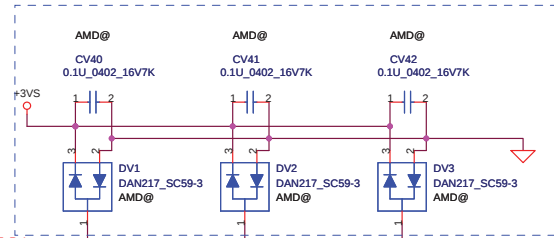
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CRT

Intel USE BLM15BB470SS1D (47 OHM BEAD)

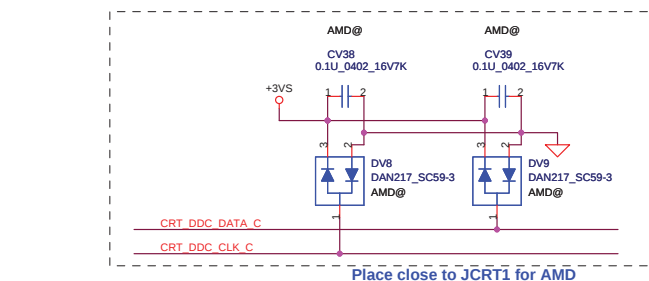
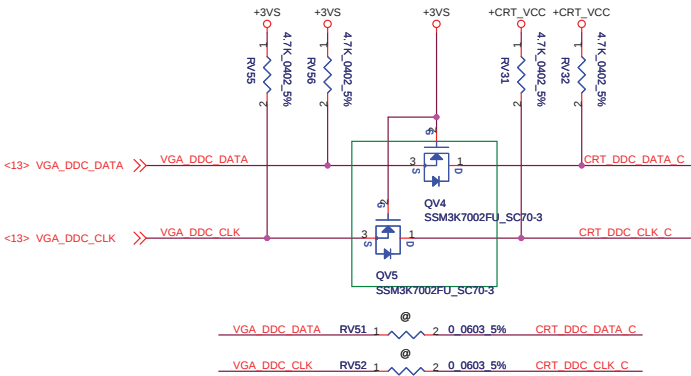
FOOT PRINT is Different

Place close to JCRT1 for AMD

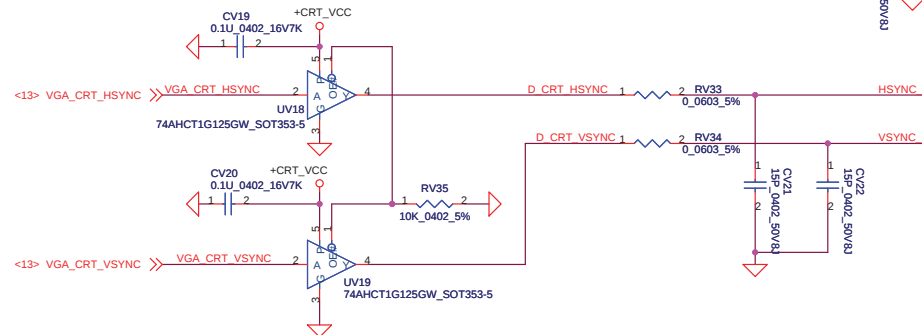
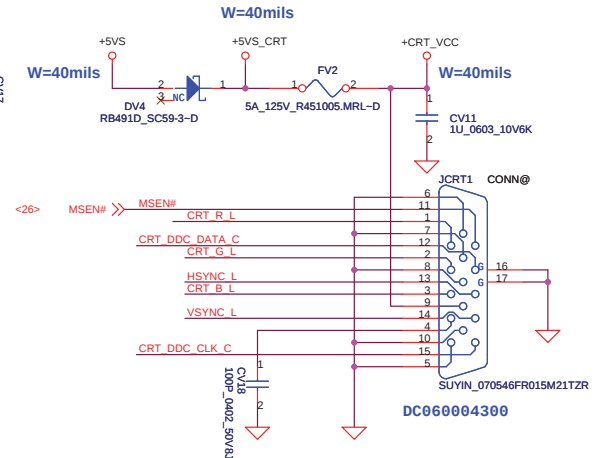


AMD Check List: R=148 ohm
Need CIS symbol

SE00000AY80
change to 6P_0402
Need apply CIS symbol



Place close to JCRT1 for AMD



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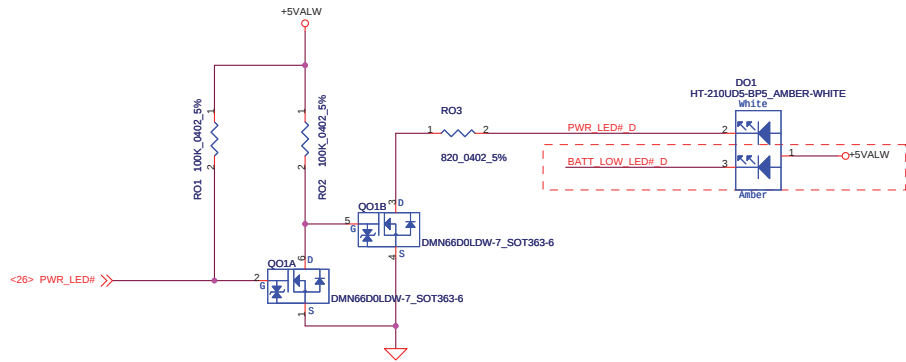
VGA Conn.

LA-6132P

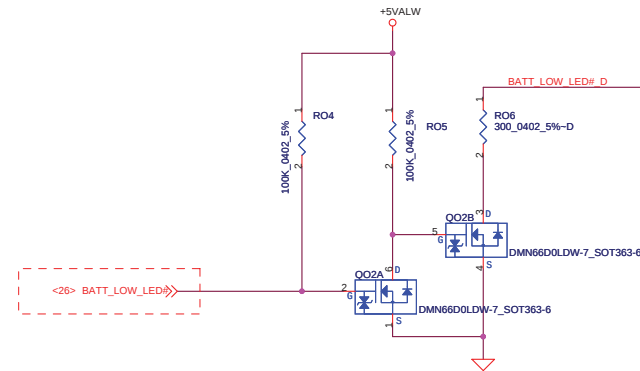
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Size	24	1.0
Date	Monday, May 10, 2010	Sheet 24 of 45

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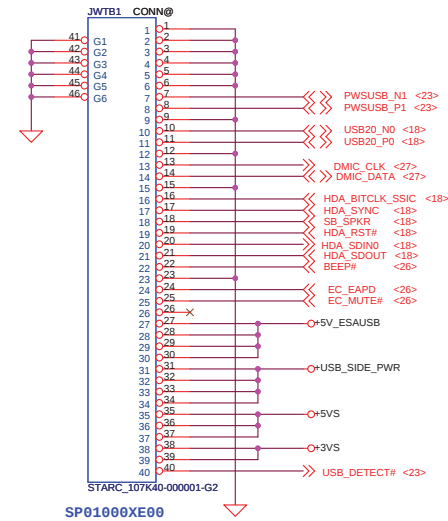
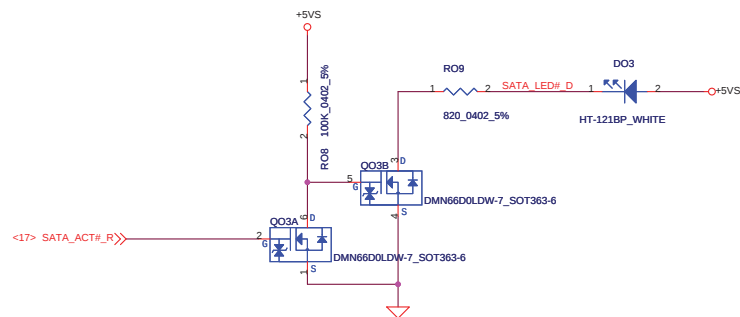
Power LED



BATT CHARGE



HD LED



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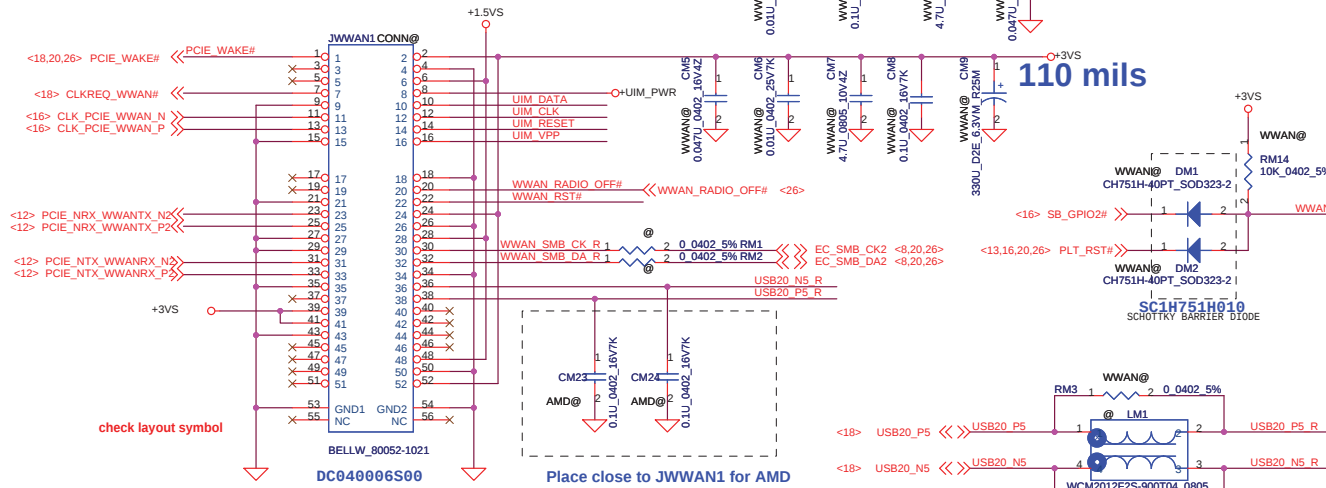
Compal Electronics, Inc.

WTB Conn/LED

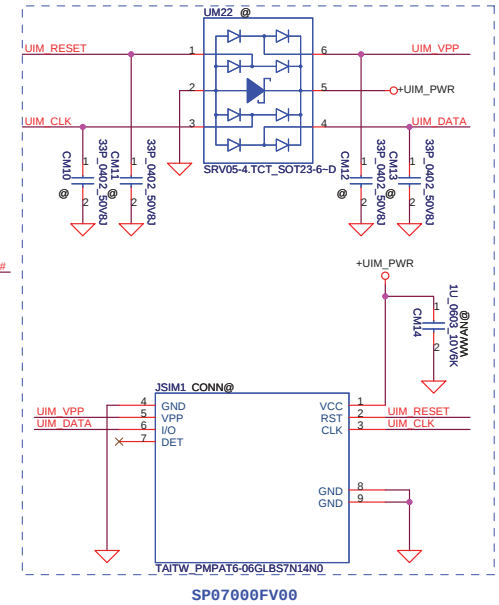
Size Document Number LA-6132P Rev 1.0
Date: Tuesday, May 04, 2010 Sheet 25 of 45

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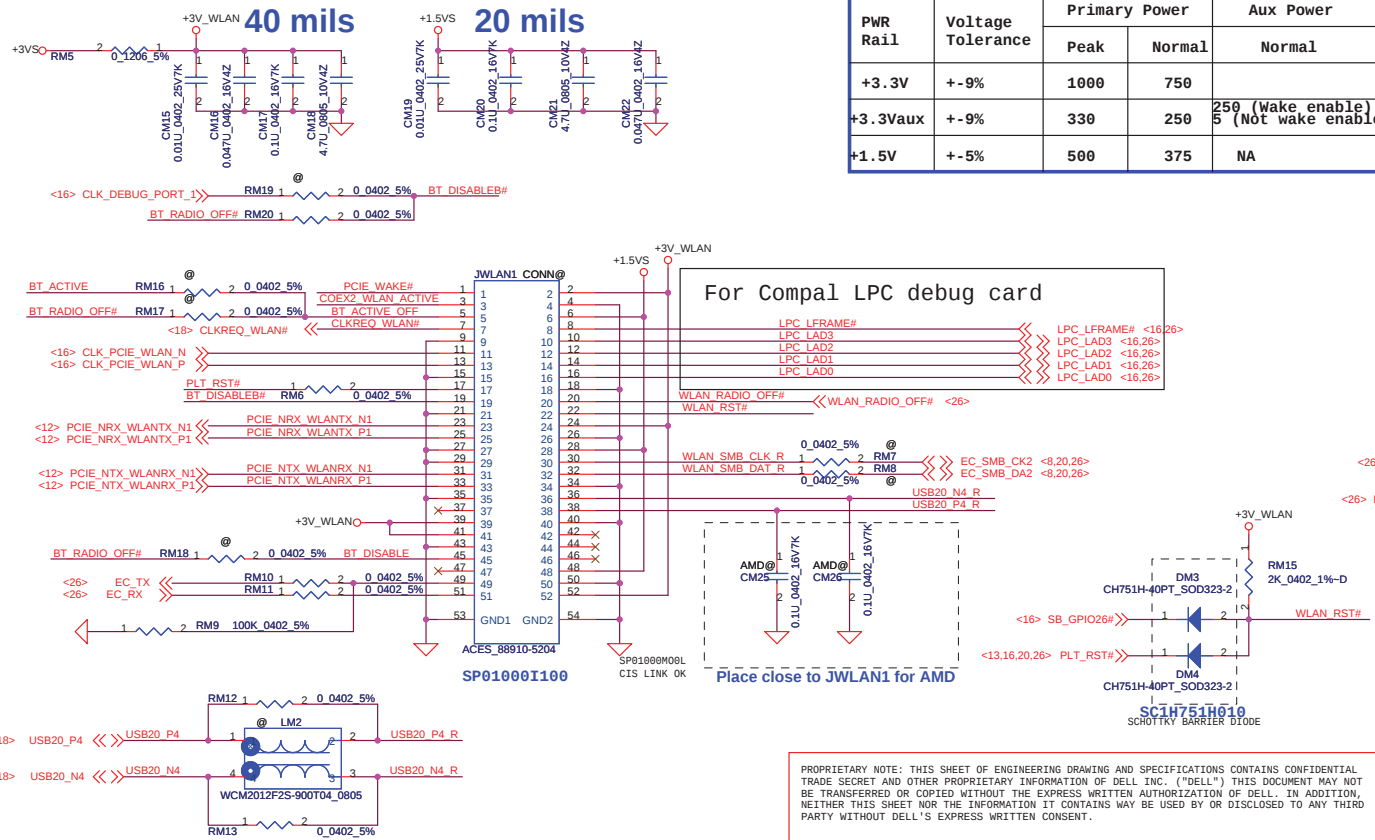
WWAN PCIE MiniCard



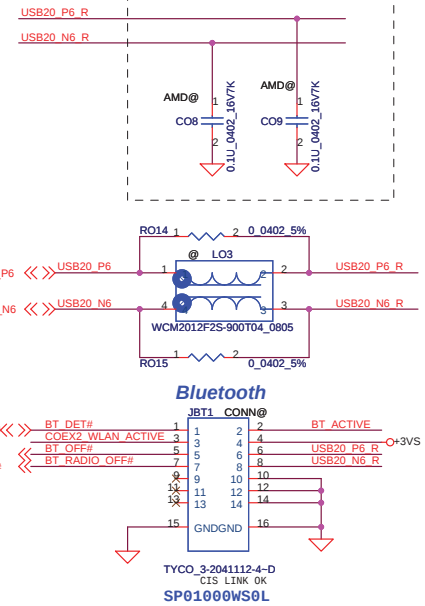
SIM Card



WLAN/WIMAX PCIE Mini Card



Place close to JBT1 for AMD



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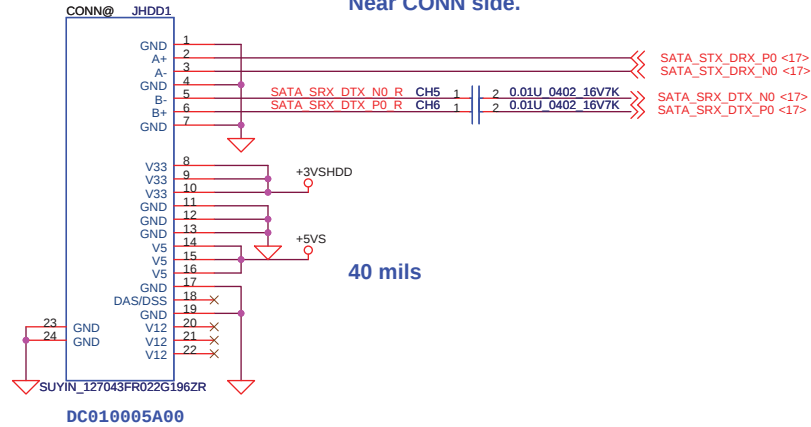
Compal Electronics, Inc.

Title		WLAN/WWAN/BT	
Size	Document Number	LA-6132P	
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Rev	1.0		

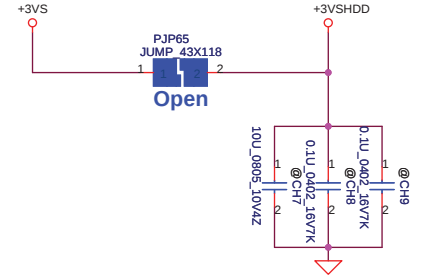
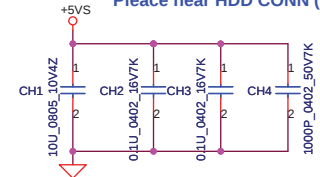
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HDD Connector

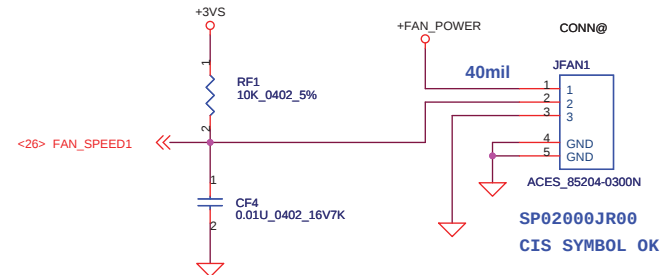
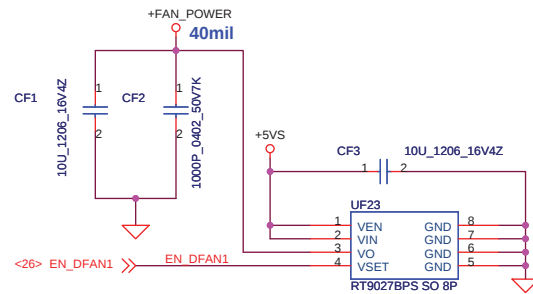
Near CONN side.



Place near HDD CONN (JHDD1)



FAN Control circuit



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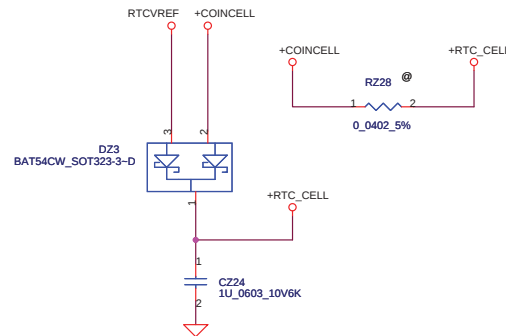


Compal Electronics, Inc.

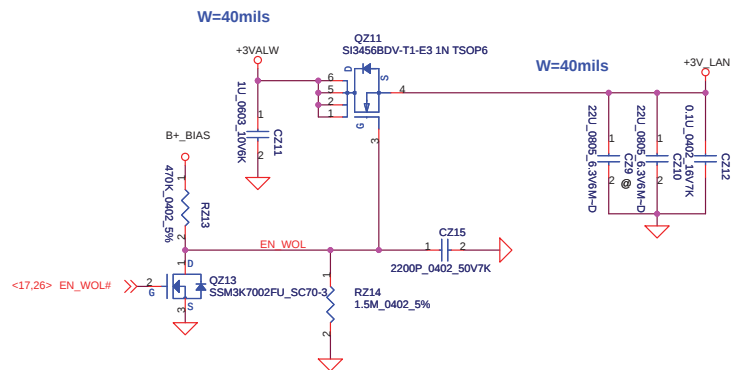
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FAN/HDD		
Size	Document Number	Rev
	LA-6132P	1.0
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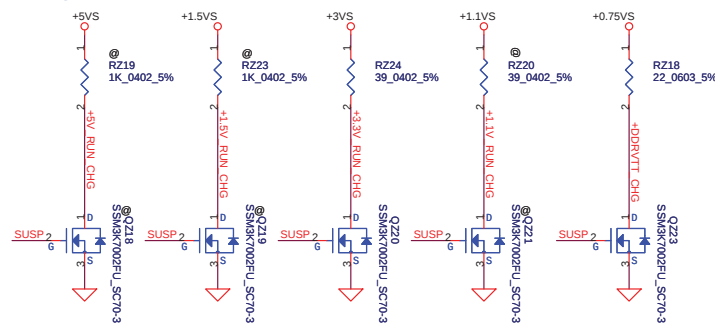
DC/DC Interface



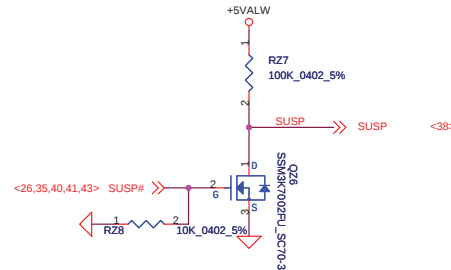
+3VALW to +3LAN Transfer



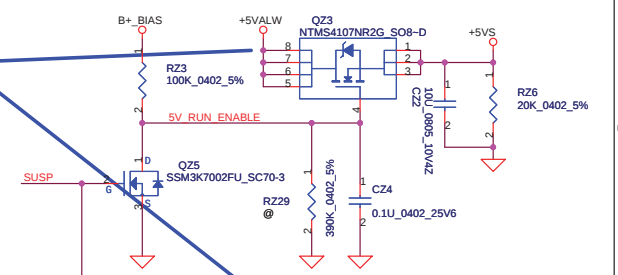
Discharg Circuit



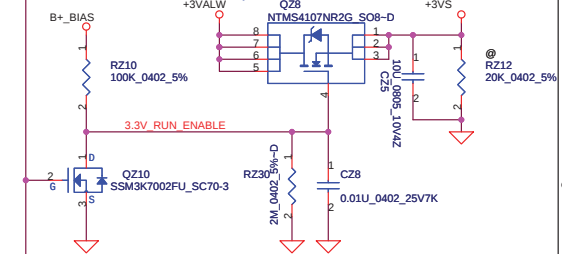
SB00000N90L (NTMS4920NR2G)



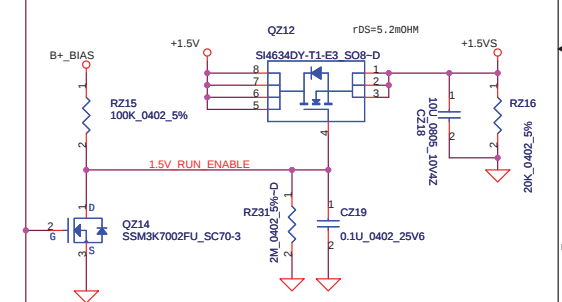
+5VRUN Source



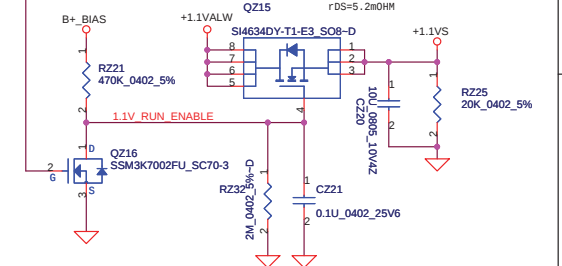
+3.3V_RUN Source



+1.5V_RUN Source



+1.1V_RUN Source



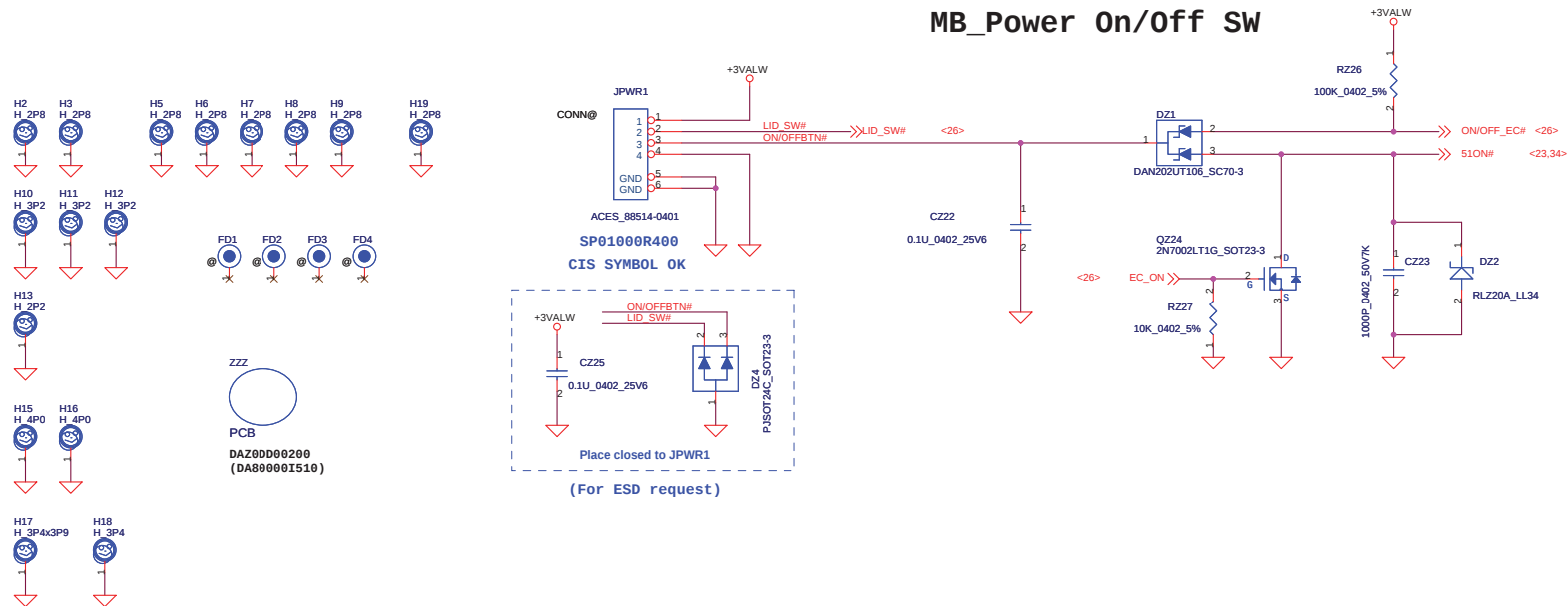
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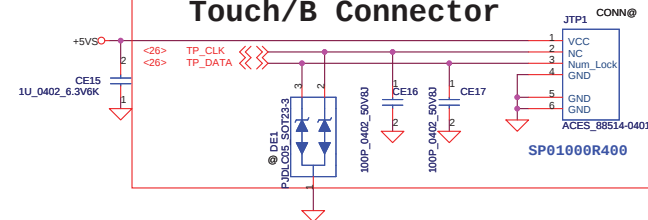
Compal Electronics, Inc.			
Title			
DC/DC (Power control)			
LA-6132P			
Size	Document Number	Rev	1.0
Date	Tuesday, May 04, 2010	Sheet	30 of 45

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MB_Power On/off SW

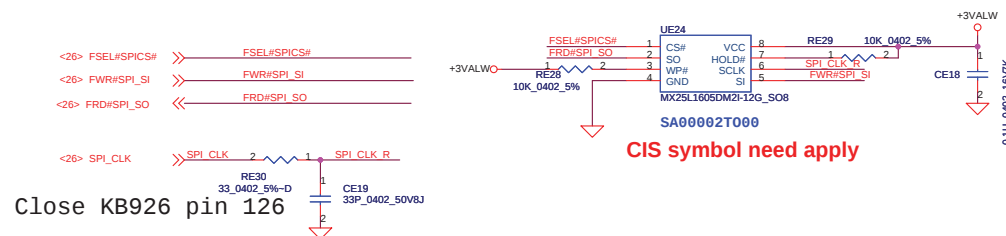


Touch/B Connector



Vendor pin defined
1. VDD
2. PS2CLK
3. PS2DATA
4. GND

System SPI Flash ROM (16Mb)



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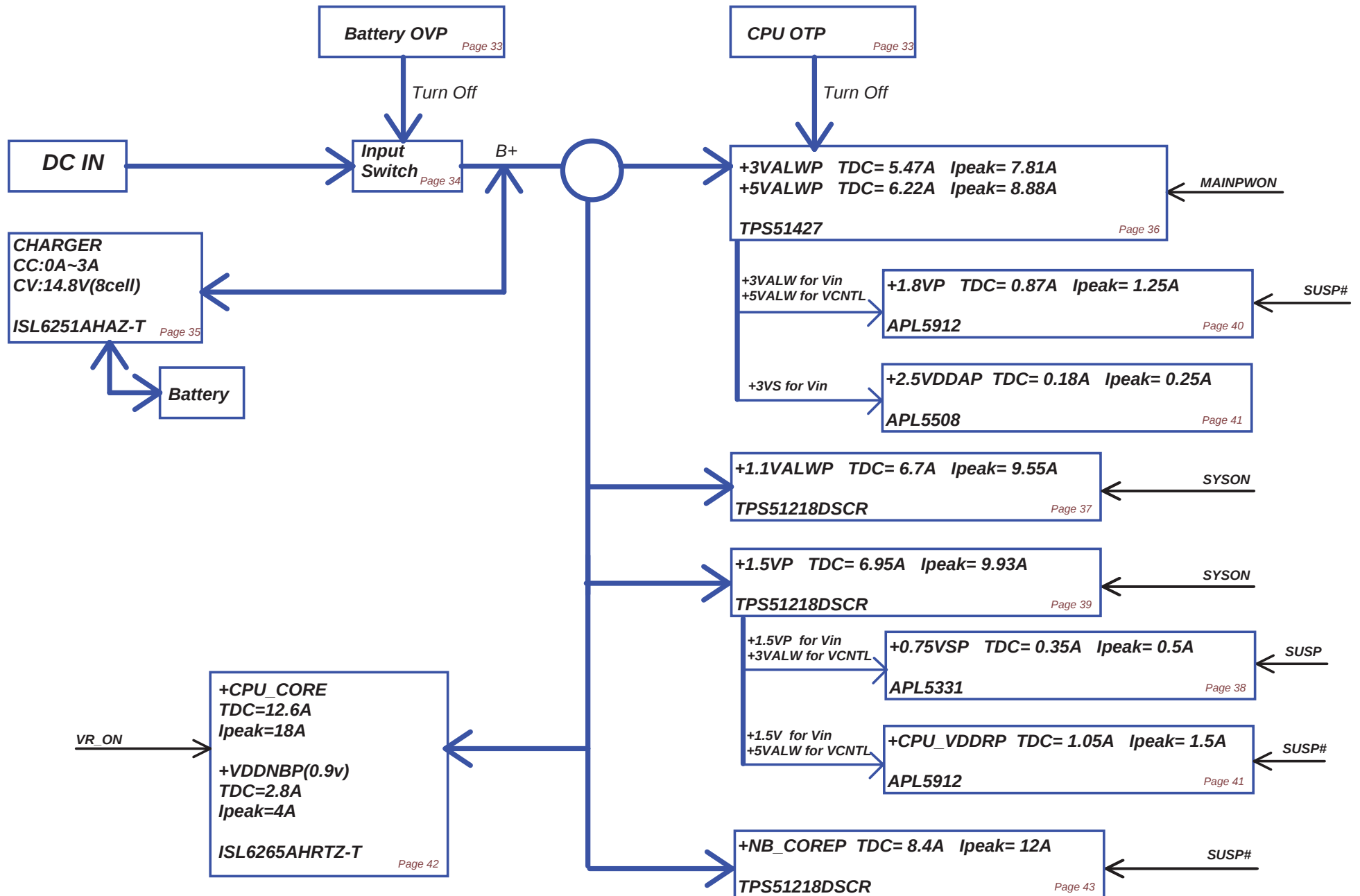
SW/ROM/TP/PWR/SCREW

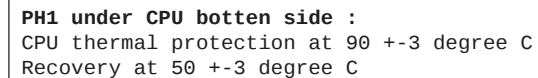
LA-6132P

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Power block



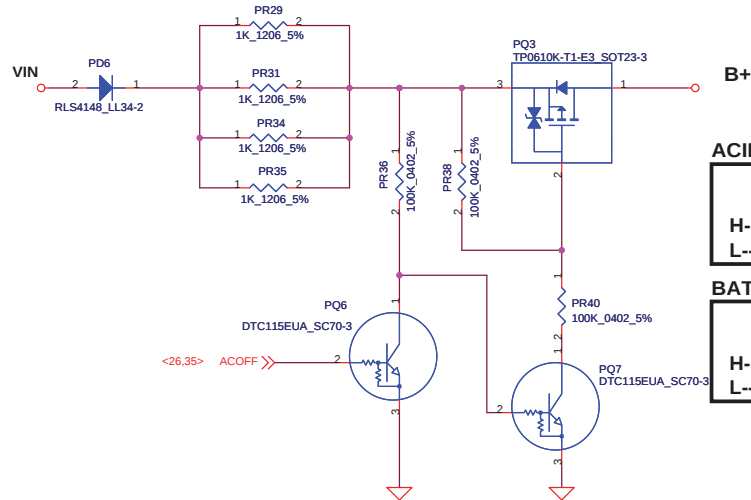
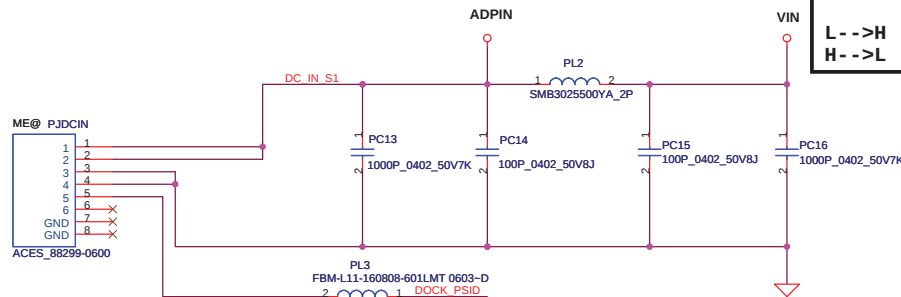


LI-3S :13.5V---BATT-OVP=1.5V
BATT-OVP=0.111*BATT+

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Issued Date	2009/2/6	Deciphered Date	2010/2/6	Title	
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				Size	Document Number
				Custom	LA-6132P
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				Rev	0.2

Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

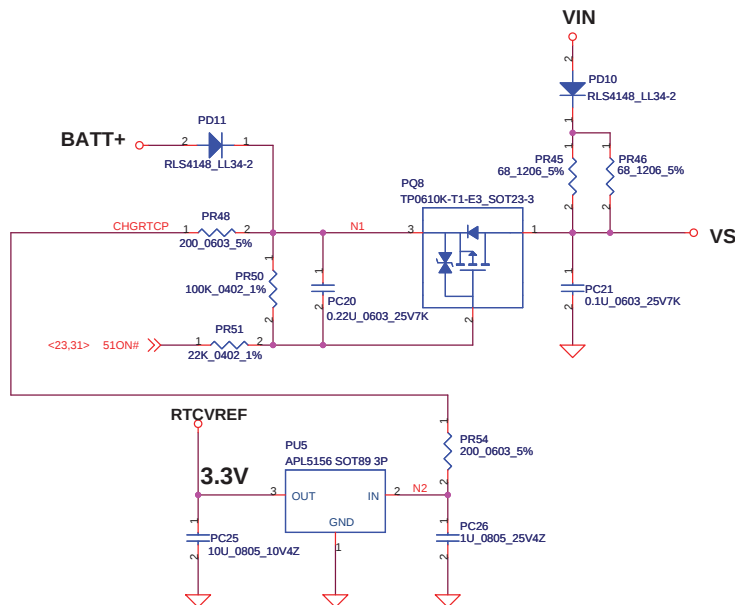


ACIN

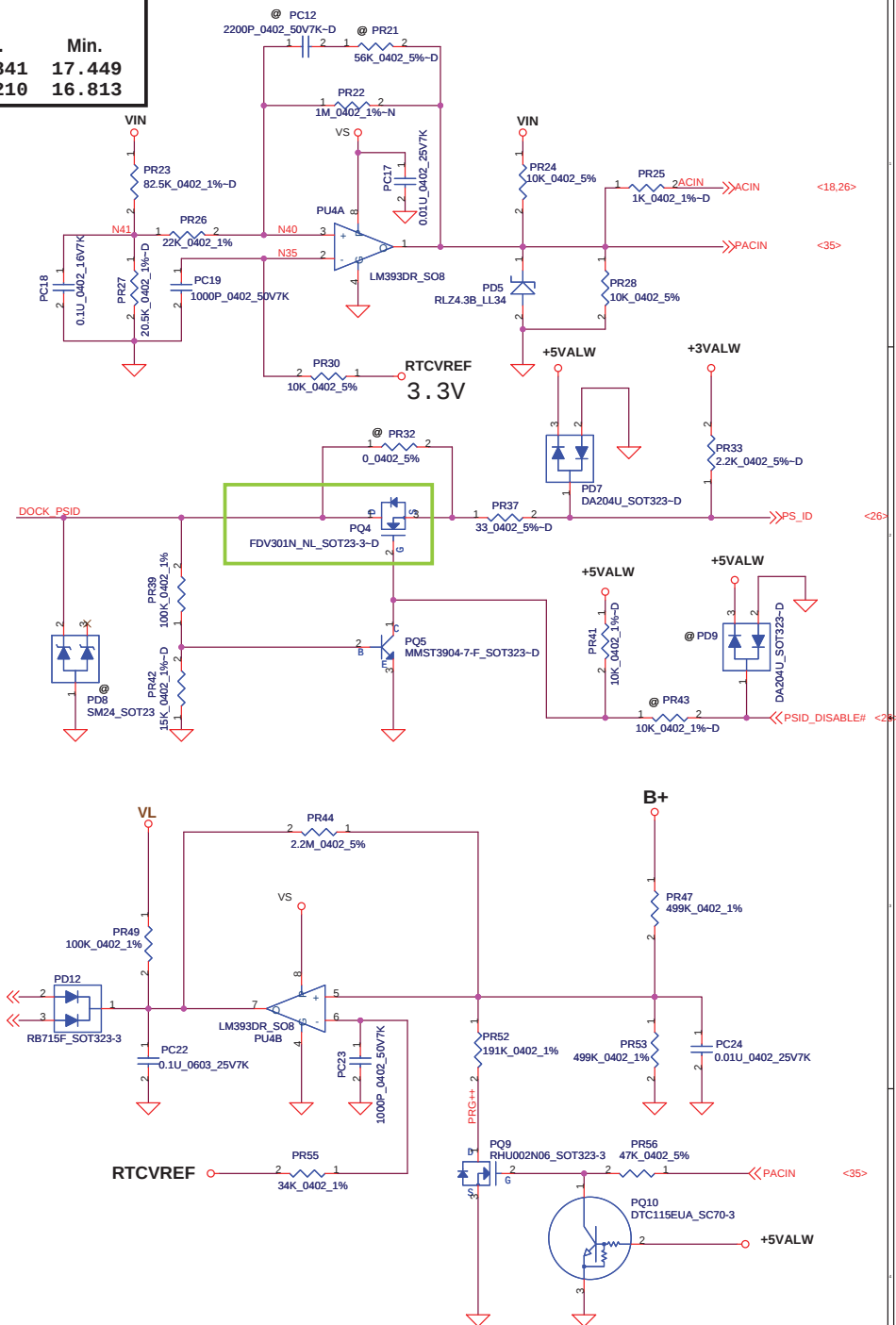
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



<33,36> MAINPWON
<35> ACON

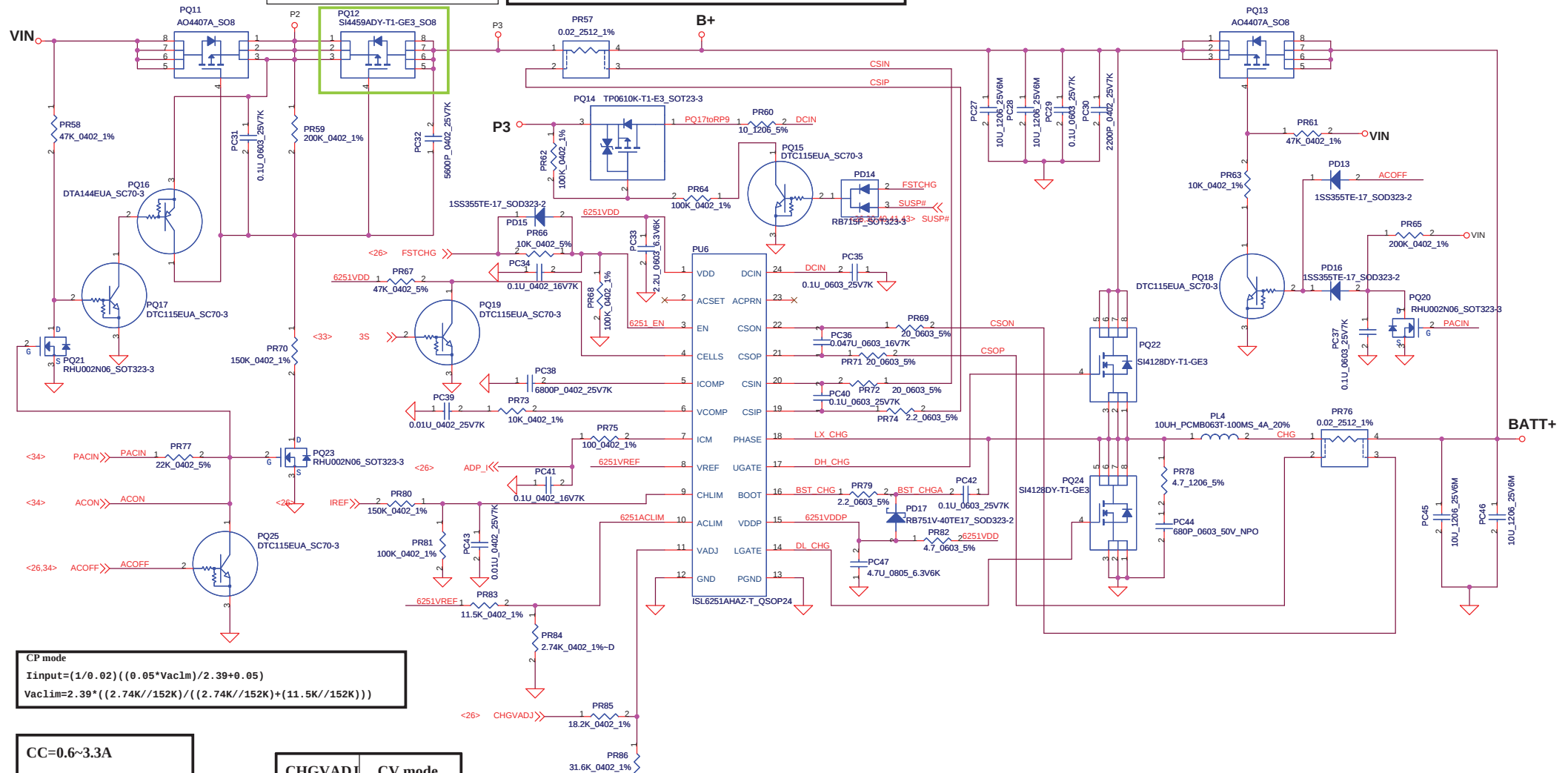


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/2/6				DCIN & DETECTOR			
Deciphered Date				2010/2/6				LA-6132P			
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I_{ada}=0~3.34A(65W)

$$ADP_I = 19.9 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$

CP = 90%*Iadapter (rating); CP = 3.003A

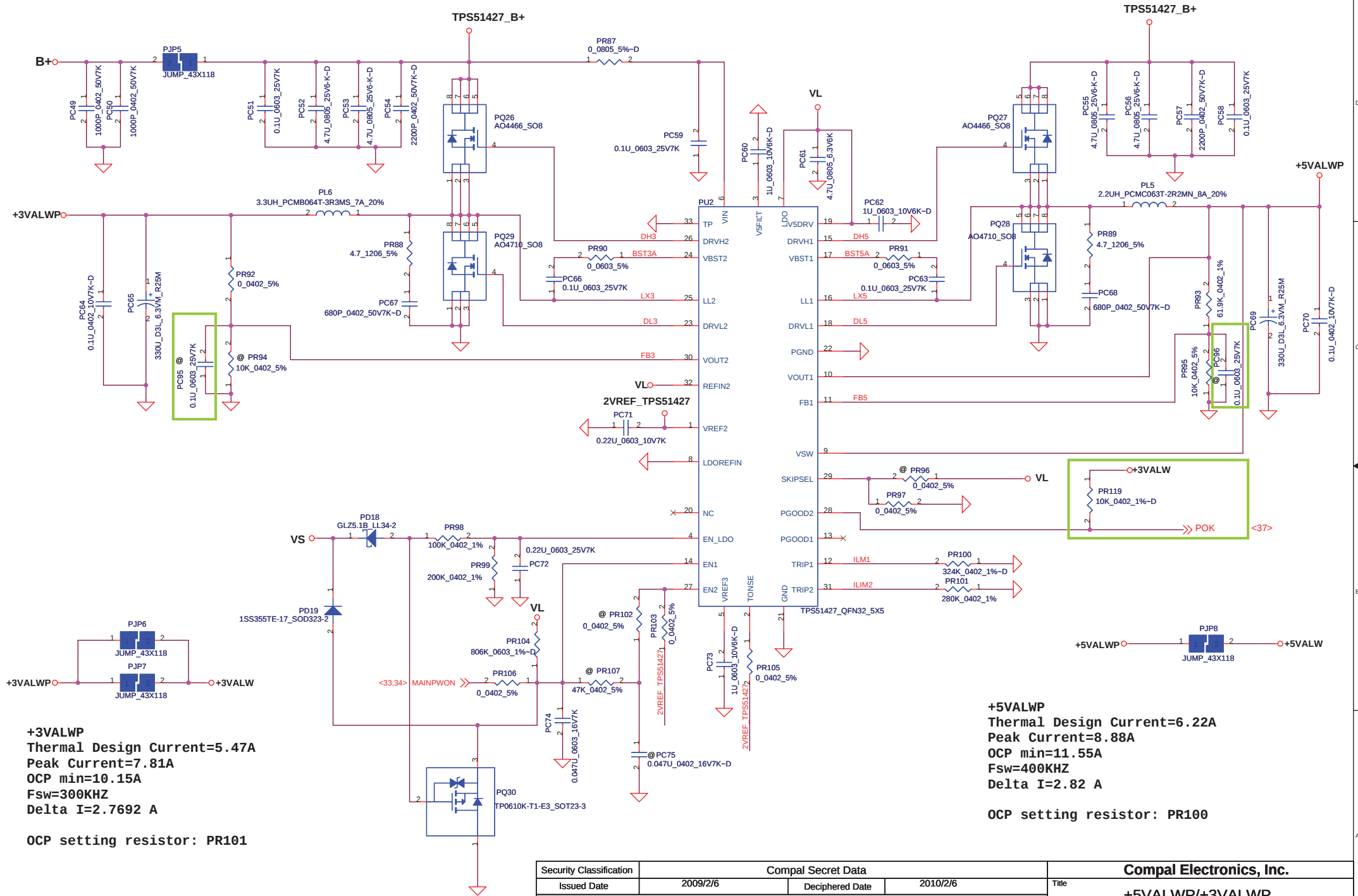


```
CP mode
Iinput=(1/0.02)*((0.05*Vac1m)/2.39+0.05)
Vac1m=2.39*((2.74K//152K)/((2.74K//152K)+(11.5K//152K)))
```

CC=0.6~3.3A
IREF=1*Icharge
IREF=0.6V~3.3V

CHGVADJ	CV mode
0V	3.99V per cell
1.91V	4.2V per cell
3.3V	4.35V per cell

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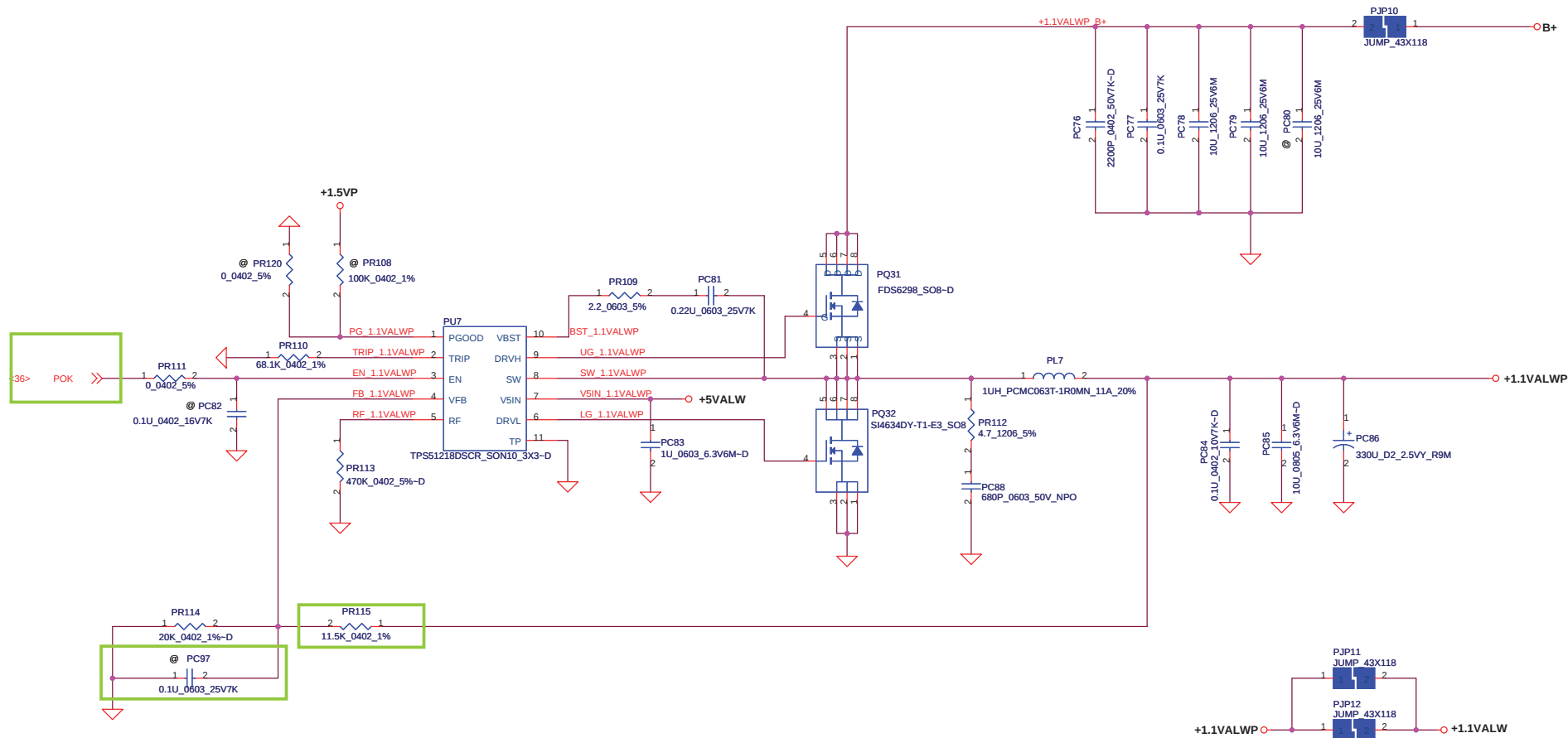
+3VALWP
Thermal Design Current=5.47A
Peak Current=7.81A
OCP min=10.15A
Fsw=300KHZ
Delta I=2.7692 A

OCP setting resistor: PR101

+5VALWP
Thermal Design Current=6.22A
Peak Current=8.88A
OCP min=11.55A
Fsw=400KHZ
Delta I=2.82 A

OCP setting resistor: PR100

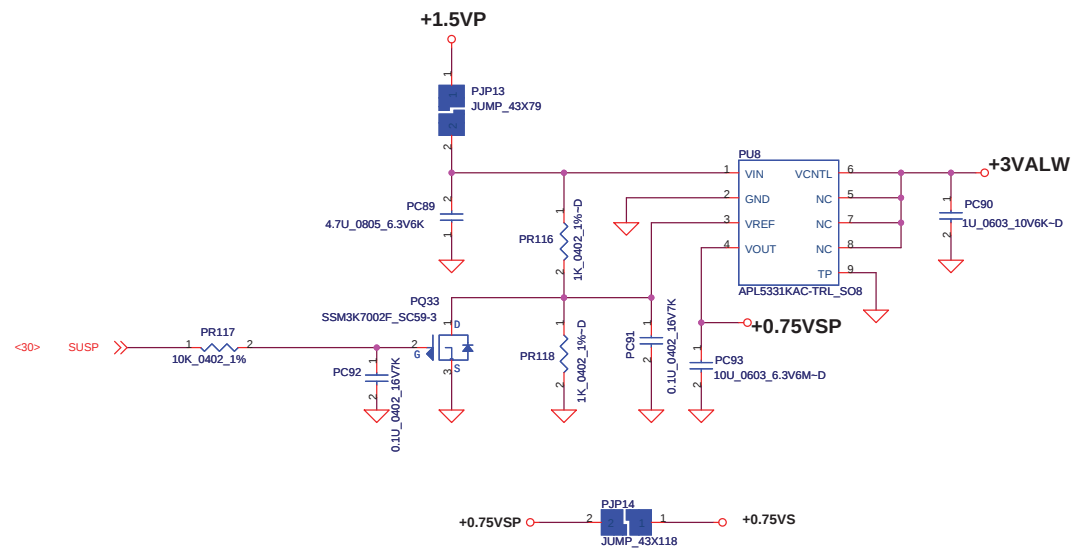
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								+5VALWP/+3VALWP	
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+1.1VALWP
 Thermal Design Current=6.7A
 Peak Current=9.55A
 OCP min=12.42A
 Fsw=290KHZ

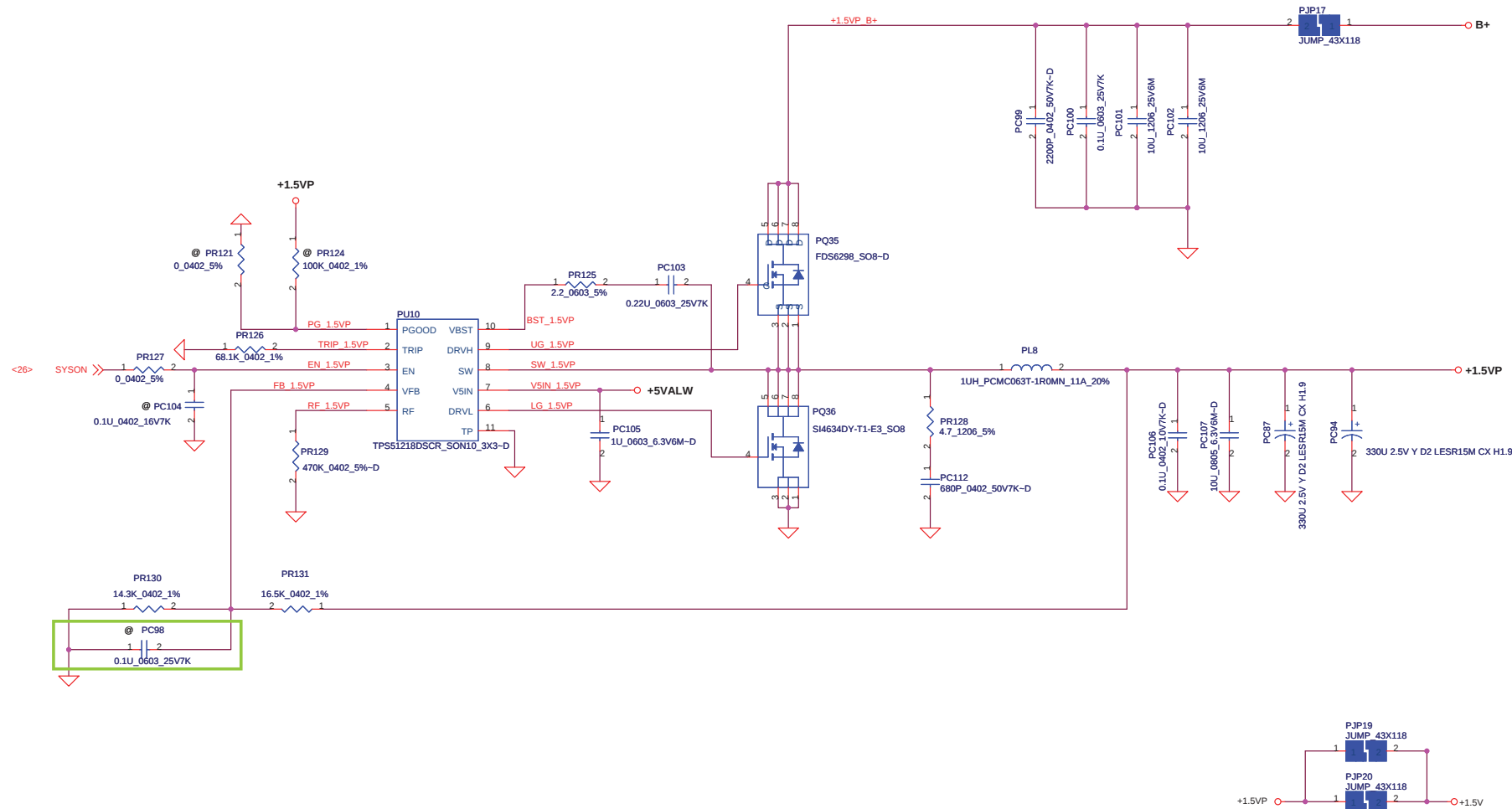
Delta I=3.5791A
 L/S MOS Rds(on)=5.5m (Typ) ; 6.7m (Max)

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+0.75VSP
 Thermal Design Current=0.35A
 Peak Currnet=0.5A
 OCP min=0.65A

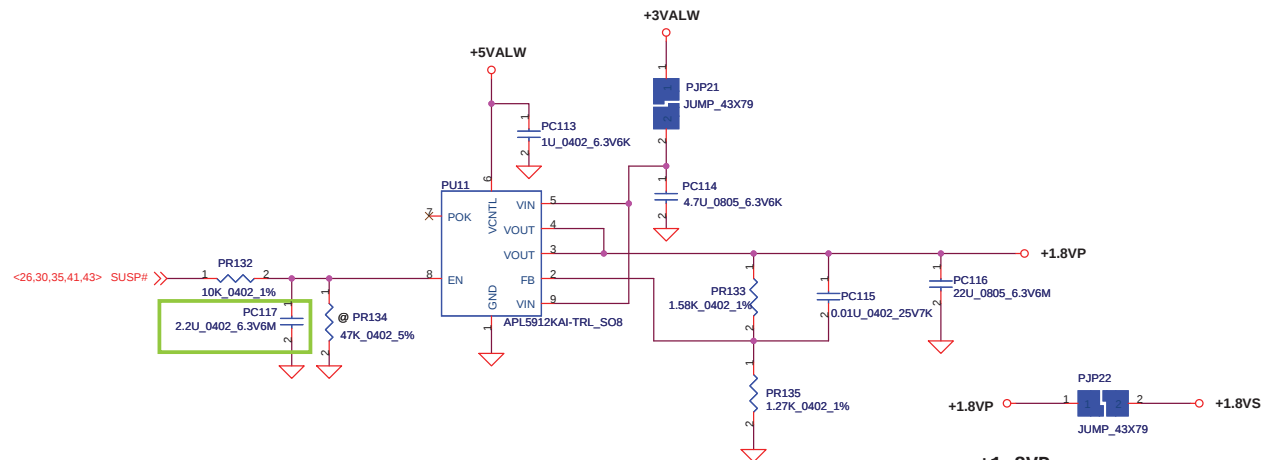
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Issued Date	2008/2/5	Deciphered Date	2008/6/05	Title +0.75VSP		
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+1.5VP
 Thermal Design Current=6.95A
 Peak Current=9.93A
 OCP min=12.9A
 Fsw=290KHZ

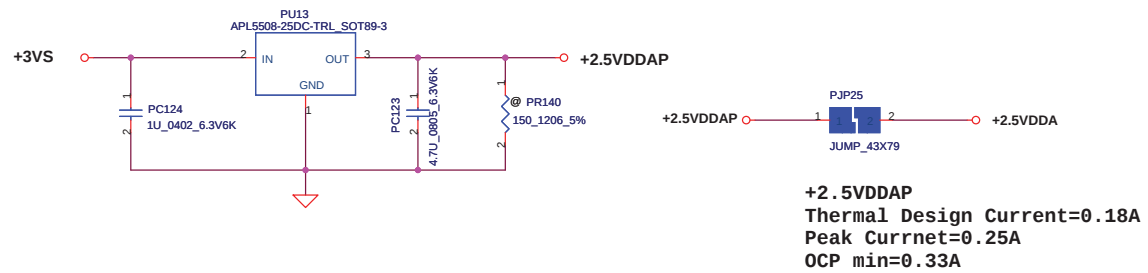
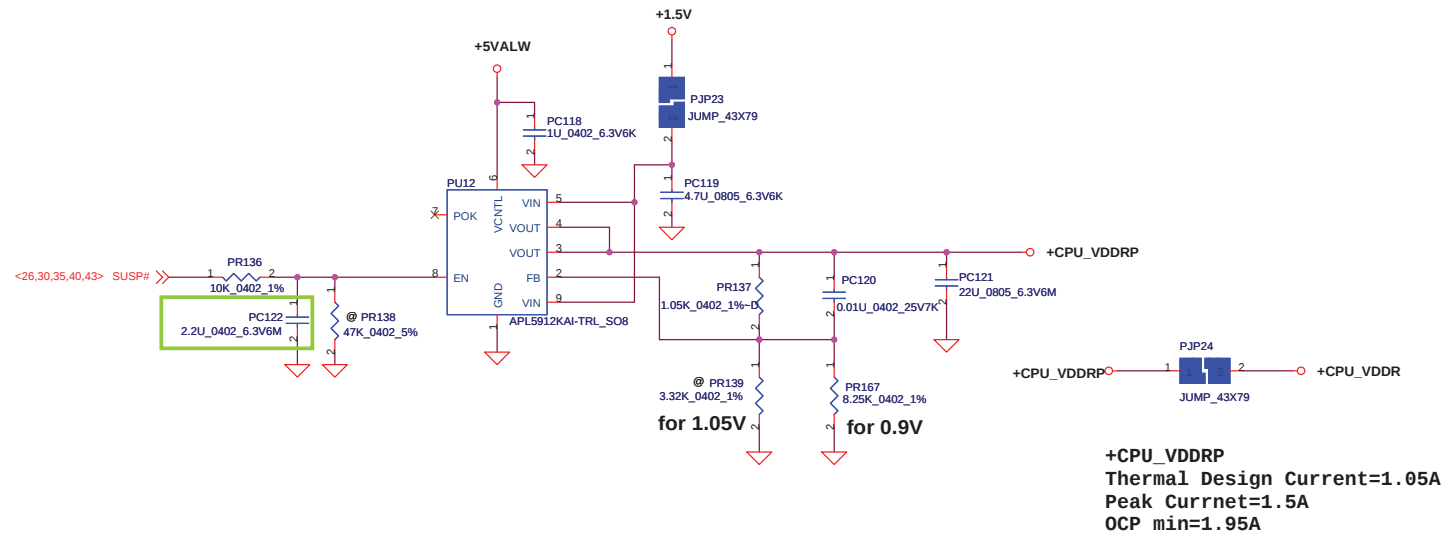
Delta I=4.7745A
 L/S MOS Rds(on)=5.5m (Typ) ; 6.7m (Max)

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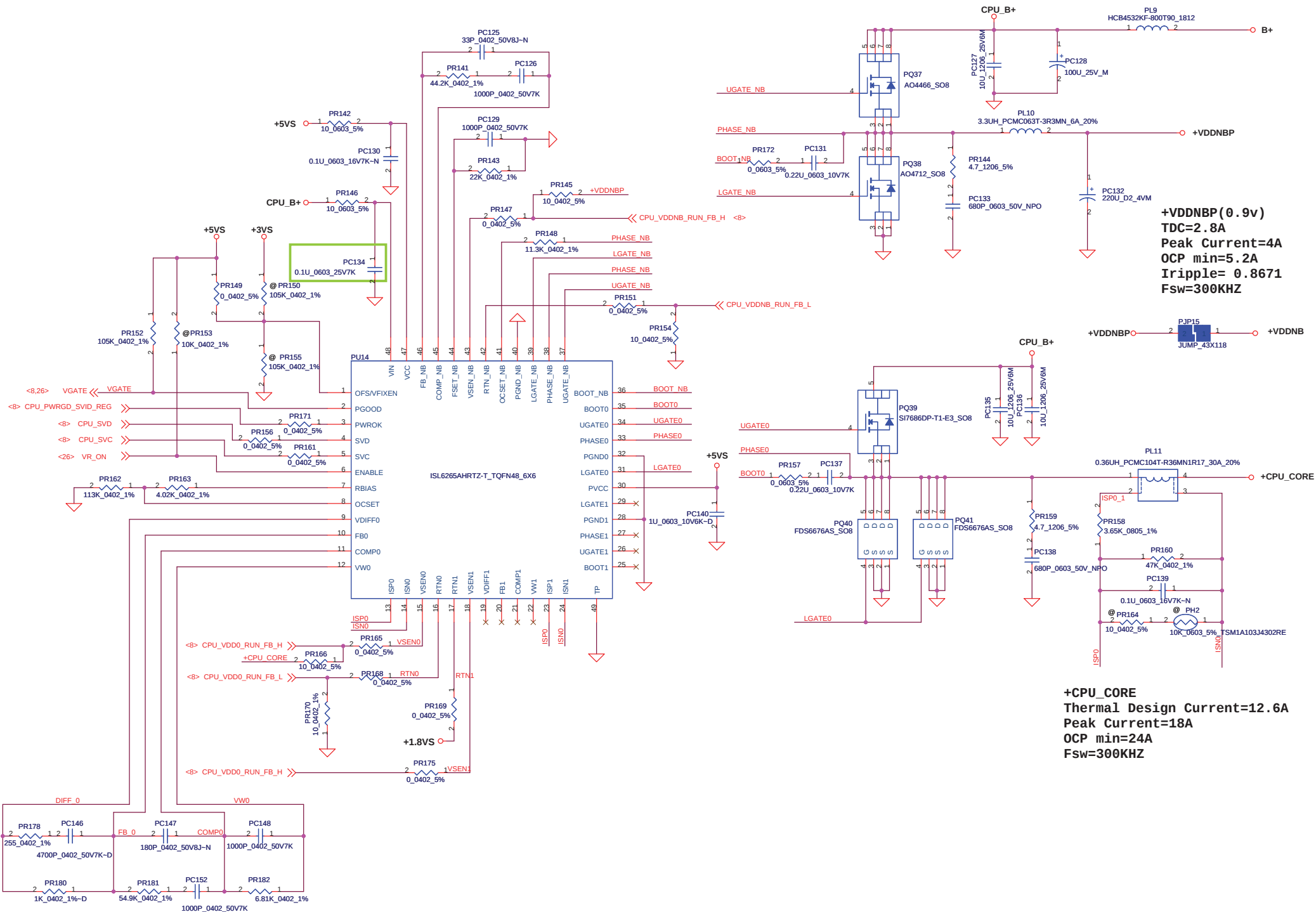


+1.8VP
 Thermal Design Current=0.87A
 Peak Currnet=1.25A
 OCP min=1.62A

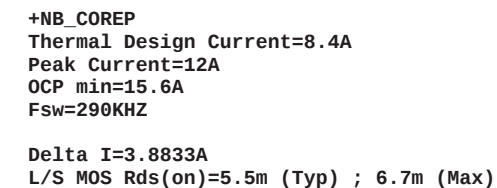
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	+2.5VDDAP/+CPU_VDDRP
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	DCIN & DETECTOR	2009/12/30	Compal	Dell has seen a couple of field return systems at the other ODM with the ESD damaged N-FET of PSID signal.	Change PQ4 from SB00000960L (S TR SSM3K7002FU 1N SC70-3) to SB503010010 (S TR FDV301N 1N SOT23-3)	X01
2	42	+CPU_CORE /+VDDNBP	2009/12/30	Compal	Over component rated voltage spec.	Change PC134 from SE026104KN0 (S CER CAP .1U 16V K X7R 0603) to SE042104K80(S CER CAP .1U 25V K X7R 0603)	X01
3	36	+5VALWP/+3VALWP	2009/12/30	Compal	HW modify +1.1VALWP power sequence	1 Add PR119 (P/N :SD034100280) (S RES 1/16W 10K +-1% 0402) pull up +3VALW at POK	X01
	37	+1.1VALWP				2. Change +1.1VALWP enable signal name from "SYSON" to "POK" at Node PR111.1	
4	36	+5VALWP/+3VALWP	2009/12/30	Compal	For QAD Temp/Volt margin test	1. [+3VALWP portion] Add @PC95 parallel at @PR94 [+5VALWP portion] Add @PC96 parallel at PR95	X01
	37	+1.1VALWP				2. [+1.1VALWP portion] Add @PC97 parallel at PR114	
	39	+1.5VP				3. [+1.5VP portion] Add @PC98 parallel at PR130	
	43	+NB_COREP				4. [+NB_COREP portion] Add @PC108 parallel at PR194	
5	35	CHARGER	2009/12/30	Compal	To prevent PQ5 damage issue	Change PQ12 from SB00000DL00 (S TR A04407A 1P S08) to SB00000I600 (S TR SI4459ADY-T1-GE3 1P S08)	X01
6	40	+1.8VP	2010/02/05	Compal	HW modify +1.8VP, +CPU_VDDRP power sequence	Change [+1.8VP portion] PC117 and [+CPU_VDDRP portion] PC122 from SE076104K80 (S CER CAP .1U 16V K X7R 0402) to SE00000888L (S CER CAP 2.2U 6.3V M X5R 0402)	X01
	41	+2.5VDDAP /+CPU_VDDRP					
7	43	+NB_COREP	2010/02/05	Compal	HW modify power budget for +NB_COREP portion +NB_COREP output change from 1.2v to 1.1v	Change PR195 from SD00000QM80 (S RES 1/16W 14.3K +-1% 0402) to SD034113280 (S RES 1/16W 11.3K +-1% 0402)	X01
8	37	+1.1VALWP	2010/02/05	Compal	AMD measure (location :LN12) VDDPCIE Vmin under Spec follow AMD suggestion to adjust voltage level to meet spec.	Change PR115 from SD034113280 (S RES 1/16W 11.3K +-1% 0402) to SD034115280 (S RES 1/16W 11.5K +-1% 0402)	X01
9	42	+CPU_CORE /+VDDNBP	2010/03/08	Compal	change N0 suffix P/N to meet Dell suffix P/N (80 or 8L)	1. Change PC130, PC139 from SE026104KN0 (S CER CAP .1U 16V K X7R 0603) to SE026104K8L (S CER CAP .1U 16V K X7R 0603) 2. Change PC125 from SE068330KN0 (S CER CAP 33P 50V J NPO 0402) to SE071330J80 (S CER CAP 33P 50V J NPO 0402) 3. Change PC147 from SE071181JN0 (S CER CAP 180P 50V J NPO 0402)to SE071181J8L (S CER CAP 180P 50V J NPO 0402)	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	16	SB	2010/01/19	HW	Boou up issue	POP RS27	X01
2	17	SB	2010/01/19	HW	Boou up issue	UNPOP RS34, POP RS43	X01
3	17	SATA	2010/01/19	HW	SATA LED active	ADD RS111	X01
4	17	SB	2010/01/19	HW	Disable function	UNPOP YS3, RS50, CS24, CS25	X01
5	19	CODEC	2010/01/19	HW	CODEC voltage	Change RS92 to 0 ohm, UNPOP RS93	X01
6	23	USB	2010/01/19	ESD	ESD request	POP DL1	X01
7	26	EC	2010/01/19	ESD	ESD request	ADD CE25	X01
8	30	PWR	2010/01/19	HW	Boot up issue	Change CZ4, CZ8, CZ19, CZ21 to 0.1U	X01
9	24	VGA	2010/01/22	Safety	Safety request reserve fuse to meet LPS specification	Add FV2	X01
10	30	PWR	2010/01/22	Sourcer	Fairchild FDS8878 will EOL	Modify QZ3, QZ8 to NTMS4107	X01
11	27	LVDS	2010/01/22	EC	Reserve LVDS VDD control by EC	Change RV40 to DV10	X01
12	18	SMBus	2010/01/25	HW	SMBus waveform fixed	Add RS25, RS28 (22ohm) on signal MEM_SMBCLK/MEM_SMBDATA	X01
13	16, 20, 26	X'tal	2010/01/27	Vendor	For X'tal EA test result	Change CE12, CE13, CS14, CS15, CS16, CS17, CL16, CL17 for vendor recommended	X01
14	17, 25	USB	2010/01/27	DELL	Delete eSATA function	Delete eSATA function and follow NLM00 change sleep charge function to USB1	X01
15	26	EC	2010/01/27	ESD	ESD request	ADD CE25 location for ESD	X01
16	26, 27	LVDS	2010/01/27	DELL	Add LCD panel feature	Add CE_ENABLE and DBC_ENABLE	X01
17	30	PWR	2010/01/27	Sourcer	FDS8878/NTMS4107 will EOL	Modify QZ3, QZ8 to NTMS4920NR26	X01
18	26	EC	2010/01/27	EC	Change board version to 0.2(X01)	POP RE1, RE7 UNPOP RE4	X01
19	18	HDA	2010/01/28	EMI	Reserve SSIC for EMI concern	Add US10, RS112, RS115, RS117, RS118, RS119 and CS81, CS82	X01
20	18, 26	ACIN	2010/02/02	HW	Prevent ACIN signal to drop down from SB and EC code	Add RE32, DE2 and QS2	X01
21	28	WLAN	2010/02/03	HW	Reserve BT_RADIO_OFF# to ON/OFF all BT function	Add NET_BT_RADIO_OFF# to control on/off BT function	X01
22	27	LVDS	2010/02/04	HW	Add 0 ohm to prevent different PANEL spec.	Reserve RV57, RV58	X01
23	13, 30	Sequence	2010/02/05	HW	Solve NB_PWRGD sequence issue	POP RN29, RN33, QN1, QN2, and Change CZ21 to 2.2U, CZ8 to 0.01U	X01
24	23	PWR Rail	2010/03/17	HW	Solve Sleeping charge issue	Change +5V_ESAUSB to +USB_SIDE_PWR	X02
25	27	New Panel	2010/03/17	SED	Enable New Panel feature	POP RV57, RV58	X02
26	30	PWR	2010/03/18	HW	Change component for voltage issue	Change CZ4, CZ10, CZ21 to 0.1U/25V, CZ8 to 0.01U/25V Change RZ21 to 470k OHM	X02
27	26	EC	2010/03/23	EC	For EC team common design	Add RE33 and UNPOP	X02
28	28	WLAN	2010/03/23	RF	For RF team common design	Add RM18 to disable BT, and support BT365 module, POP RM17	X02
29	31	PWR button	2010/03/25	ESD	For ESD issue from power button	Add CZ25, DZ4	X02
30	18, 21	RF issue	2010/03/25	RF	For RF issue	Add CS22, RB8, CB12, Change RS119 to 33 OHM and Del RS118, RB3	X02
31	27	LVDS	2010/03/25	HW	For reserve LVDS pannel sequence	Add QV11, QV12, RV59, RV60, RV61	X02
32	28	WLAN	2010/03/25	RF	Solve Athros B95 WLAN Card issue	Change RM15 to 2k OHM	X02
33	16, 28	BT	2010/05/03	RF	For RF team common design	Add RM19, RM20, RS113 and UNPOP RM18, RM19, RS113	A00
34	18	SSIC	2010/05/11	RF	For WWAN & NON-WWAN design	Change SSIC BOM structure & CS22 to 8.2p for RF	A00

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