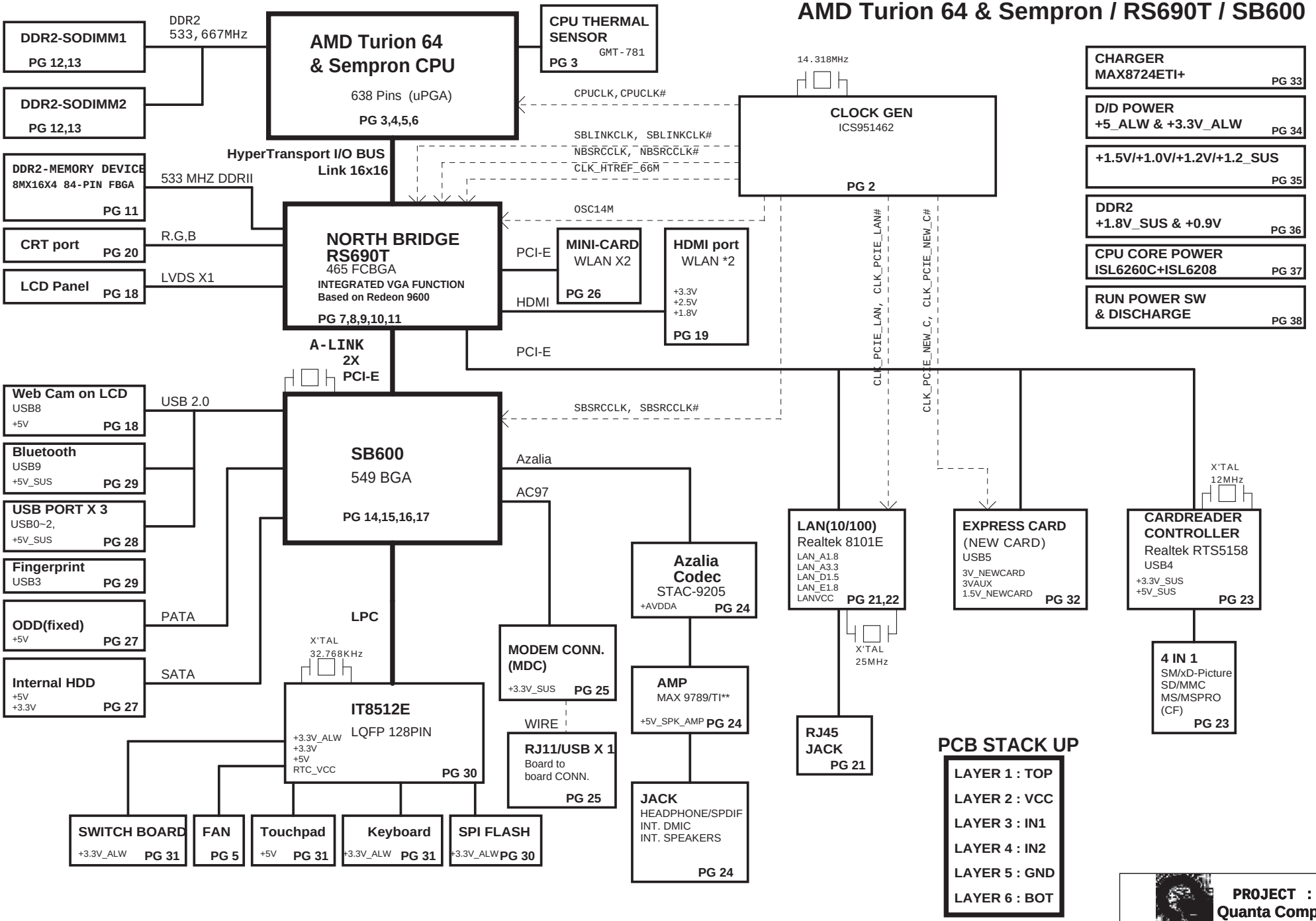
SA1A BLOCK DIAGRAM

AMD Turion 64 & Sempron / RS690T / SB600



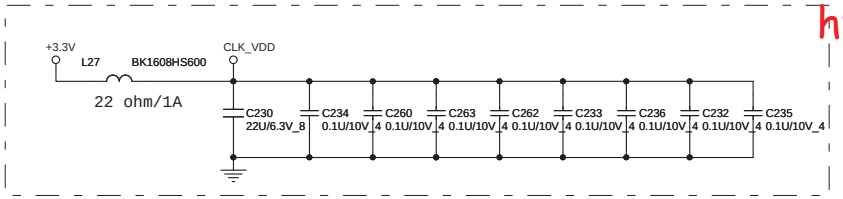
PCB STACK UP

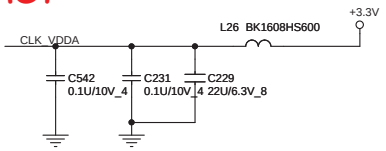
LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	3A

Date: Thursday, January 31, 2008 Sheet 1 of 39



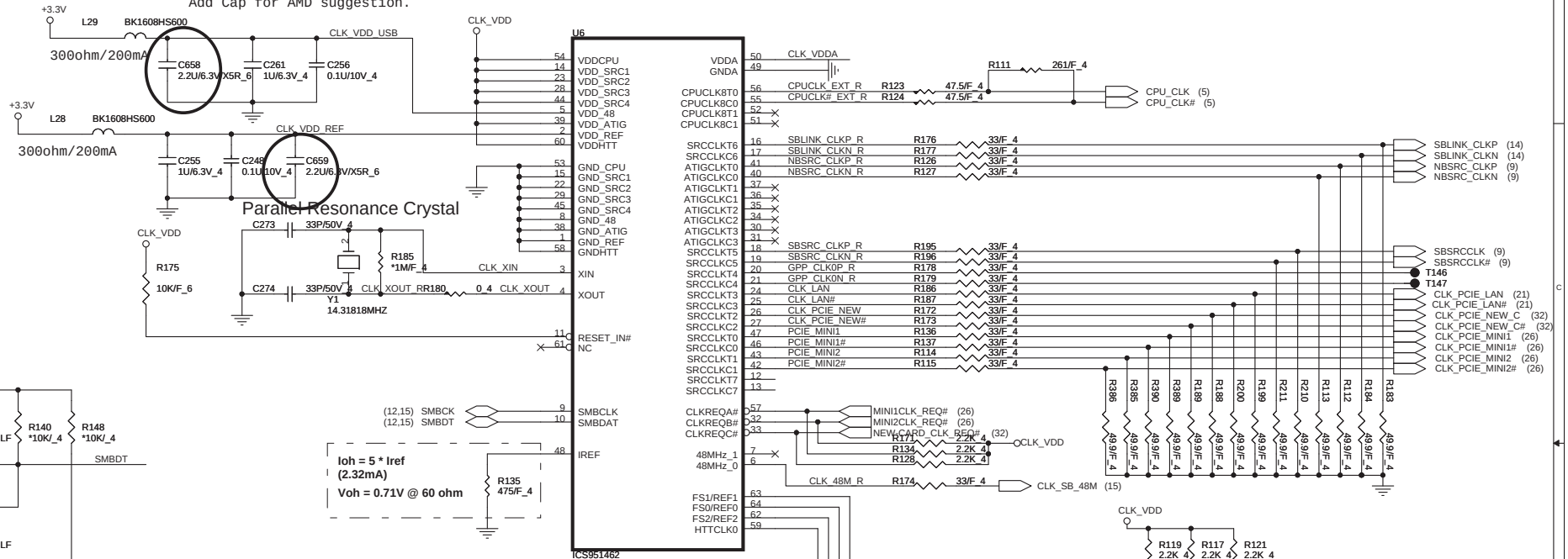


B01

Add Cap for AMD suggestion.

1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800

2- PUT DECOUPLING CAPS CLOSE TO Clock Gen.POWER PIN



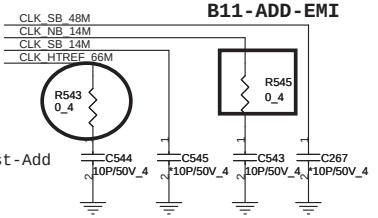
CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4
CLKREQC# CONTROL SRC0,1

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

B11-ADD-EMI



A01

C-test-Add

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	3A
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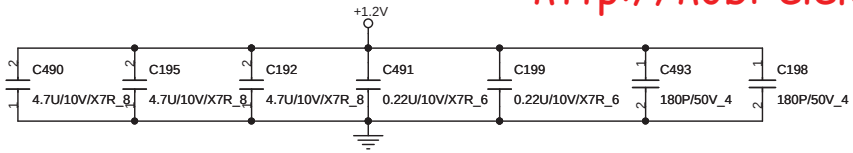
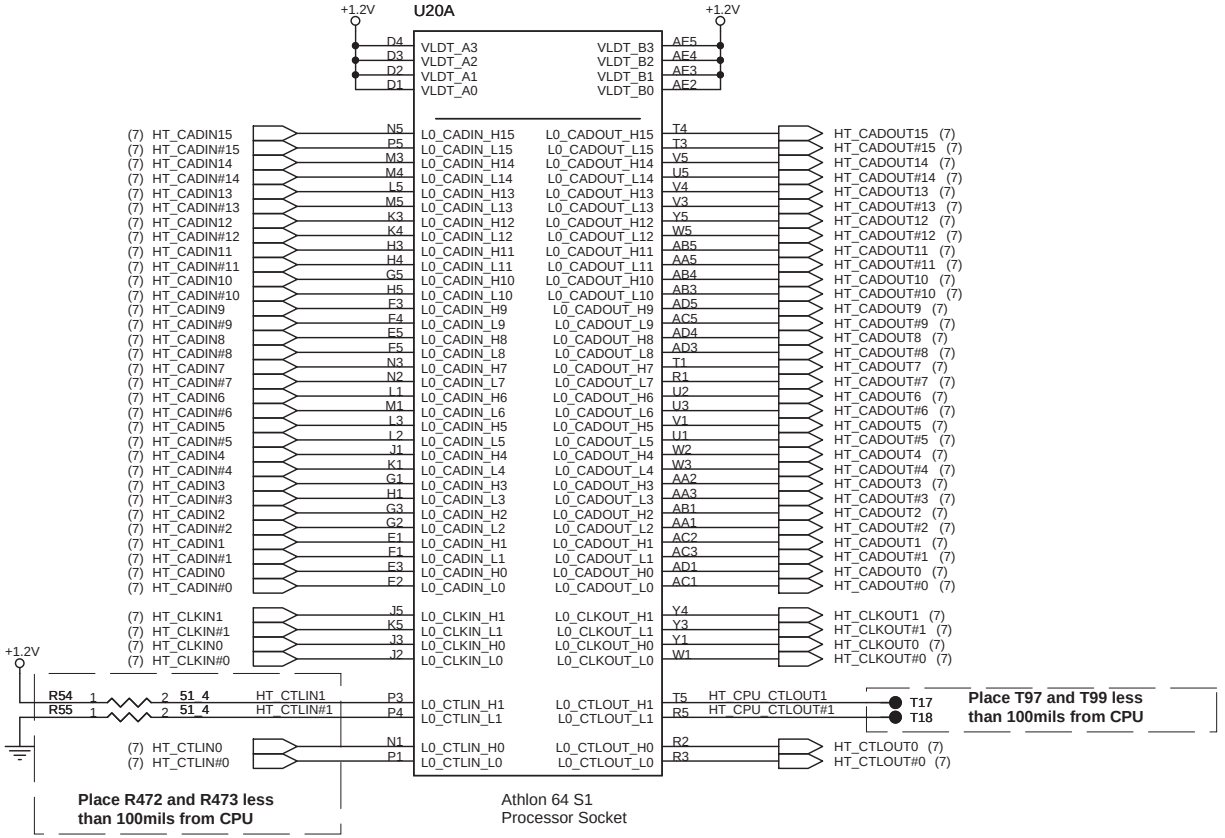


LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



	PROJECT : SA1A Quanta Computer Inc.	
Size B	Document Number ATHLON64 HT I/F	Rev 3A
Date: Thursday, January 31, 2008	Sheet 3 of 39	

Notes for the SODIMM locations:
DIMMA = Far = Bottom
DIMMB = Near = Top

Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

+1.8V_SUS

C67 0.1U/10V/X7R_4
R48 1K/F_6

CPU_VTT_SUS_SENSE should be routed as 10mils and 10mils spacing from any adjacent signals in X, Y, Z directions.

+0.9V_CPU_M_VREF_SUS

C76 0.1U/10V/X7R_4
C73 1000P/50V_4
R47 1K/F_6

for +0.9V_DDR_VTT feedback

Place Capacitors for +0.9V_CPU_M_VREF_SUS < 1" from the RS690. +0.9V_CPU_M_VREF_SUS trace length < 6", trace width > 15mils and 20mils spacing from any adjacent signals in X, Y, Z directions.

+1.8V_SUS

R351 39.2/F_4
R352 39.2/F_4

KEEP TRACE TO RESISTORS LESS THAN 1.5" FROM CPU PIN

U20B

(36) CPU_VTT_SENSE

W17	MEMVREF	
Y10	VTT_SENSE	
AE10	MEMZN	M_ZN
AF10	MEMZP	M_ZP

T16 DDR_CS3_DIMMA#
T32 DDR_CS2_DIMMA#

V19	MA0_CS_L3	
J22	MA0_CS_L2	
V22	MA0_CS_L1	(12,13) DDR_CS1_DIMMA#
T19	MA0_CS_L0	(12,13) DDR_CS0_DIMMA#

T14 DDR_CS3_DIMMB#
T33 DDR_CS2_DIMMB#

Y26	MB0_CS_L3	
J24	MB0_CS_L2	
W24	MB0_CS_L1	(12,13) DDR_CS1_DIMMB#
U23	MB0_CS_L0	(12,13) DDR_CS0_DIMMB#

H26	MB_CKE1	(12,13) DDR_CKE1_DIMMB
J23	MB_CKE0	(12,13) DDR_CKE0_DIMMB
J20	MA_CKE1	(12,13) DDR_CKE1_DIMMA
J21	MA_CKE0	(12,13) DDR_CKE0_DIMMA

(12,13) DDR_A_MA[0..15]

K19	MA_ADD15	DDR_A_MA15
K20	MA_ADD14	DDR_A_MA14
V24	MA_ADD13	DDR_A_MA13
K24	MA_ADD12	DDR_A_MA12
L20	MA_ADD11	DDR_A_MA11
R19	MA_ADD10	DDR_A_MA10
L19	MA_ADD9	DDR_A_MA9
L22	MA_ADD8	DDR_A_MA8
L21	MA_ADD7	DDR_A_MA7
M19	MA_ADD6	DDR_A_MA6
M20	MA_ADD5	DDR_A_MA5
M24	MA_ADD4	DDR_A_MA4
M22	MA_ADD3	DDR_A_MA3
N22	MA_ADD2	DDR_A_MA2
N21	MA_ADD1	DDR_A_MA1
R21	MA_ADD0	DDR_A_MA0

K22	MA_BANK2	(12,13) DDR_A_BS2
R20	MA_BANK1	(12,13) DDR_A_BS1
T22	MA_BANK0	(12,13) DDR_A_BS0

T20	MA_RAS_L	(12,13) DDR_A_RAS#
U20	MA_CAS_L	(12,13) DDR_A_CAS#
U21	MA_WE_L	(12,13) DDR_A_WE#

DDR II: CMD/CTRL/CLK

+0.9V_DDR_VTT

D10	VTT1	
C10	VTT2	
B10	VTT3	
AD10	VTT4	
W10	VTT5	
AC10	VTT6	
AB10	VTT7	
AA10	VTT8	
A10	VTT9	

Y16	MA0_CLK_H2	M_CLK_DDR1 (12,13)
AA16	MA0_CLK_L2	M_CLK_DDR#1 (12,13)
E16	MA0_CLK_H1	M_CLK_DDR0 (12,13)
F16	MA0_CLK_L1	M_CLK_DDR#0 (12,13)
AF18	MB0_CLK_H2	M_CLK_DDR3 (12,13)
AE17	MB0_CLK_L2	M_CLK_DDR#3 (12,13)
A17	MB0_CLK_H1	M_CLK_DDR2 (12,13)
A18	MB0_CLK_L1	M_CLK_DDR#2 (12,13)

W23	MB0_ODT1	M_ODT3 (12,13)
W26	MB0_ODT0	M_ODT2 (12,13)
V20	MA0_ODT1	M_ODT1 (12,13)
U19	MA0_ODT0	M_ODT0 (12,13)

J25	MB_ADD15	DDR_B_MA15
J26	MB_ADD14	DDR_B_MA14
W25	MB_ADD13	DDR_B_MA13
L23	MB_ADD12	DDR_B_MA12
L25	MB_ADD11	DDR_B_MA11
U25	MB_ADD10	DDR_B_MA10
L24	MB_ADD9	DDR_B_MA9
M26	MB_ADD8	DDR_B_MA8
L26	MB_ADD7	DDR_B_MA7
N23	MB_ADD6	DDR_B_MA6
N24	MB_ADD5	DDR_B_MA5
N25	MB_ADD4	DDR_B_MA4
N26	MB_ADD3	DDR_B_MA3
P24	MB_ADD2	DDR_B_MA2
P26	MB_ADD1	DDR_B_MA1
T24	MB_ADD0	DDR_B_MA0

DDR_B_MA[0..15] (12,13)

K26	MB_BANK2	DDR_B_BS2 (12,13)
T26	MB_BANK1	DDR_B_BS1 (12,13)
U26	MB_BANK0	DDR_B_BS0 (12,13)

U24	MB_RAS_L	DDR_B_RAS# (12,13)
V26	MB_CAS_L	DDR_B_CAS# (12,13)
U22	MB_WE_L	DDR_B_WE# (12,13)

Athlon 64 S1
Processor Socket

U20C

(12) DDR_B_D[0..63]

AD11	MB_DATA63	DDR_B_D63
AE11	MB_DATA62	DDR_B_D62
AE14	MB_DATA61	DDR_B_D61
AE14	MB_DATA60	DDR_B_D60
Y11	MB_DATA59	DDR_B_D59
AB11	MB_DATA58	DDR_B_D58
AC12	MB_DATA57	DDR_B_D57
AE13	MB_DATA56	DDR_B_D56
AE15	MB_DATA55	DDR_B_D55
AF16	MB_DATA54	DDR_B_D54
AC18	MB_DATA53	DDR_B_D53
AF19	MB_DATA52	DDR_B_D52
AD14	MB_DATA51	DDR_B_D51
AC14	MB_DATA50	DDR_B_D50
AE18	MB_DATA49	DDR_B_D49
AD18	MB_DATA48	DDR_B_D48
AD20	MB_DATA47	DDR_B_D47
AC20	MB_DATA46	DDR_B_D46
AF23	MB_DATA45	DDR_B_D45
AF24	MB_DATA44	DDR_B_D44
AF20	MB_DATA43	DDR_B_D43
AE20	MB_DATA42	DDR_B_D42
AD22	MB_DATA41	DDR_B_D41
AC22	MB_DATA40	DDR_B_D40
AE25	MB_DATA39	DDR_B_D39
AD26	MB_DATA38	DDR_B_D38
AA25	MB_DATA37	DDR_B_D37
AA26	MB_DATA36	DDR_B_D36
AE24	MB_DATA35	DDR_B_D35
AD24	MB_DATA34	DDR_B_D34
AA23	MB_DATA33	DDR_B_D33
AA24	MB_DATA32	DDR_B_D32
G24	MB_DATA31	DDR_B_D31
G23	MB_DATA30	DDR_B_D30
D26	MB_DATA29	DDR_B_D29
C26	MB_DATA28	DDR_B_D28
G26	MB_DATA27	DDR_B_D27
G25	MB_DATA26	DDR_B_D26
E24	MB_DATA25	DDR_B_D25
E23	MB_DATA24	DDR_B_D24
C24	MB_DATA23	DDR_B_D23
B24	MB_DATA22	DDR_B_D22
C20	MB_DATA21	DDR_B_D21
B20	MB_DATA20	DDR_B_D20
C25	MB_DATA19	DDR_B_D19
D24	MA_DATA18	DDR_B_D18
A21	MA_DATA17	DDR_B_D17
D20	MA_DATA16	DDR_B_D16
D18	MA_DATA15	DDR_B_D15
C18	MA_DATA14	DDR_B_D14
D14	MA_DATA13	DDR_B_D13
C14	MA_DATA12	DDR_B_D12
A20	MA_DATA11	DDR_B_D11
A19	MA_DATA10	DDR_B_D10
A16	MA_DATA9	DDR_B_D9
A15	MA_DATA8	DDR_B_D8
A13	MA_DATA7	DDR_B_D7
D12	MA_DATA6	DDR_B_D6
E11	MA_DATA5	DDR_B_D5
G11	MA_DATA4	DDR_B_D4
B14	MA_DATA3	DDR_B_D3
A14	MA_DATA2	DDR_B_D2
A11	MA_DATA1	DDR_B_D1
C11	MA_DATA0	DDR_B_D0

(12) DDR_B_DM[0..7]

AD12	MB_DM7	DDR_B_DM7
AC16	MB_DM6	DDR_B_DM6
AF22	MB_DM5	DDR_B_DM5
AB26	MB_DM4	DDR_B_DM4
E25	MB_DM3	DDR_B_DM3
A22	MB_DM2	DDR_B_DM2
B16	MB_DM1	DDR_B_DM1
A12	MB_DM0	DDR_B_DM0

AF12	MB_DQS_H7	DDR_B_DQS7
AE12	MB_DQS_L7	DDR_B_DQS#7
AF16	MB_DQS_H6	DDR_B_DQS6
AD16	MB_DQS_L6	DDR_B_DQS#6
AF21	MB_DQS_H5	DDR_B_DQS5
AF22	MB_DQS_L5	DDR_B_DQS#5
AC25	MB_DQS_H4	DDR_B_DQS4
AC26	MB_DQS_L4	DDR_B_DQS#4
F26	MB_DQS_H3	DDR_B_DQS3
F26	MB_DQS_L3	DDR_B_DQS#3
A24	MB_DQS_H2	DDR_B_DQS2
A23	MB_DQS_L2	DDR_B_DQS#2
D16	MB_DQS_H1	DDR_B_DQS1
C16	MB_DQS_L1	DDR_B_DQS#1
C12	MB_DQS_H0	DDR_B_DQS0
B12	MB_DQS_L0	DDR_B_DQS#0

DDR DATA

AA12	MA_DATA63	DDR_A_D63
AB12	MA_DATA62	DDR_A_D62
AA14	MA_DATA61	DDR_A_D61
AB14	MA_DATA60	DDR_A_D60
W11	MA_DATA59	DDR_A_D59
Y12	MA_DATA58	DDR_A_D58
AD13	MA_DATA57	DDR_A_D57
AB13	MA_DATA56	DDR_A_D56
AD15	MA_DATA55	DDR_A_D55
AB15	MA_DATA54	DDR_A_D54
AB17	MA_DATA53	DDR_A_D53
Y17	MA_DATA52	DDR_A_D52
Y14	MA_DATA51	DDR_A_D51
W14	MA_DATA50	DDR_A_D50
W16	MA_DATA49	DDR_A_D49
AD17	MA_DATA48	DDR_A_D48
Y18	MA_DATA47	DDR_A_D47
AD19	MA_DATA46	DDR_A_D46
AD21	MA_DATA45	DDR_A_D45
AB21	MA_DATA44	DDR_A_D44
AB18	MA_DATA43	DDR_A_D43
AA18	MA_DATA42	DDR_A_D42
AA20	MA_DATA41	DDR_A_D41
Y20	MA_DATA40	DDR_A_D40
AA22	MA_DATA39	DDR_A_D39
Y22	MA_DATA38	DDR_A_D38
W21	MA_DATA37	DDR_A_D37
W22	MA_DATA36	DDR_A_D36
AA21	MA_DATA35	DDR_A_D35
AB22	MA_DATA34	DDR_A_D34
AB24	MA_DATA33	DDR_A_D33
Y24	MA_DATA32	DDR_A_D32
H22	MA_DATA31	DDR_A_D31
H20	MA_DATA30	DDR_A_D30
F22	MA_DATA29	DDR_A_D29
E21	MA_DATA28	DDR_A_D28
J19	MA_DATA27	DDR_A_D27
H24	MA_DATA26	DDR_A_D26
F22	MA_DATA25	DDR_A_D25
F20	MA_DATA24	DDR_A_D24
C23	MA_DATA23	DDR_A_D23
B22	MA_DATA22	DDR_A_D22
F18	MA_DATA21	DDR_A_D21
E18	MA_DATA20	DDR_A_D20
E20	MA_DATA19	DDR_A_D19
D22	MA_DATA18	DDR_A_D18
C19	MA_DATA17	DDR_A_D17
G18	MA_DATA16	DDR_A_D16
G17	MA_DATA15	DDR_A_D15
C17	MA_DATA14	DDR_A_D14
F14	MA_DATA13	DDR_A_D13
E14	MA_DATA12	DDR_A_D12
H17	MA_DATA11	DDR_A_D11
E17	MA_DATA10	DDR_A_D10
E15	MA_DATA9	DDR_A_D9
H15	MA_DATA8	DDR_A_D8
E13	MA_DATA7	DDR_A_D7
C13	MA_DATA6	DDR_A_D6
H12	MA_DATA5	DDR_A_D5
H11	MA_DATA4	DDR_A_D4
G14	MA_DATA3	DDR_A_D3
H14	MA_DATA2	DDR_A_D2
E12	MA_DATA1	DDR_A_D1
G12	MA_DATA0	DDR_A_D0

DDR_A_DM[0..7] (12)

Y13	MA_DM7	DDR_A_DM7
AB16	MA_DM6	DDR_A_DM6
Y19	MA_DM5	DDR_A_DM5
AC24	MA_DM4	DDR_A_DM4
F24	MA_DM3	DDR_A_DM3
F19	MA_DM2	DDR_A_DM2
C15	MA_DM1	DDR_A_DM1
E12	MA_DM0	DDR_A_DM0

W12	MA_DQS_H7	DDR_A_DQS7
W13	MA_DQS_L7	DDR_A_DQS#7
Y15	MA_DQS_H6	DDR_A_DQS6
W15	MA_DQS_L6	DDR_A_DQS#6
AB19	MA_DQS_H5	DDR_A_DQS5
AB20	MA_DQS_L5	DDR_A_DQS#5
AD23	MA_DQS_H4	DDR_A_DQS4
AC23	MA_DQS_L4	DDR_A_DQS#4
G22	MA_DQS_H3	DDR_A_DQS3
G21	MA_DQS_L3	DDR_A_DQS#3
C22	MA_DQS_H2	DDR_A_DQS2
C21	MA_DQS_L2	DDR_A_DQS#2
G16	MA_DQS_H1	DDR_A_DQS1
G15	MA_DQS_L1	DDR_A_DQS#1
G13	MA_DQS_H0	DDR_A_DQS0
H13	MA_DQS_L0	DDR_A_DQS#0

(12) DDR_B_DQS[0..7]

DDR_B_DQS0
DDR_B_DQS1
DDR_B_DQS2
DDR_B_DQS3
DDR_B_DQS4
DDR_B_DQS5
DDR_B_DQS6
DDR_B_DQS7

(12) DDR_B_DQS#[0..7]

DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
DDR_B_DQS#6
DDR_B_DQS#7

(12) DDR_A_DQS[0..7]

DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7

(12) DDR_A_DQS#[0..7]

DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7

To SODIMM socket B (Near/TOP)

To SODIMM socket A (Far/Bottom)

Athlon 64 S1
Processor Socket

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATHLON64 DDRII MEMORY	3A

Date: Thursday, January 31, 2008 Sheet 4 of 39

SB600 ONLY

(14) CPU_PWRGD — CPU_PWRGD — R376 680_4 — C210 *1000P/16V/X7R_4 — R91 1 2 0_4 — LDT_STOP_R#

A02 C-test-Del

+1.8V — R99 *0_4 — +1.8V_SUS — R97 *0_4

A03 C-test-Change

D4 *SDMK0340L-7-F

(9,14) LDT_STOP# — R98 *10K/F_4 — U4 *NL17SZ17DFT2G — R96 680_4

R100 *680_4 — C221 *0.1U/16V_4 — C217 *47P/50V_4

NOTE: R7516 and C7598 close to JCPU pin F10

A03 C-test-Change

(14) LDT_RST# — LDT_RST# — R377 680 — C540 *1000P/16V/X7R_4

NOTE: Place R7090 on the top of the board that is iaccessible, and that shorting across this resistor will toggle the hyper Transport reset signal.

A02 C-test-Del

L65 ferrite bead with an approximate impedance of 33 , a maximum DC resistance of 0.025 ohm , and a current rating of at least 3000mA.

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG. This trace should be kept at least 20 mils away from all other signals.

+2.5V_CPU_VDDA_RUN

+2.5V — L25 <Size> BLM18PG330SN1D — +2.5V_CPU_VDDA_RUN — +2.5V_CPU_VDDA_RUN

C532 100U/6.3V_3528 — C224 4.7U/10V_8 — C223 0.22U/10V_6 — C218 3300P/X7R/_4

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

The AMD SI feature has errata, and will not be plemented.

Place R78 and R77 < 1.5". Route CPU_HTREF1/0 with 5mils trace width and 10mils spacing from other signals in X, Y, Z directions

+1.2V — R353 300_4 CPU_SIC — R354 *0_4 CPU_SID — R361 44.2/F_4 CPU_HTREF1 — R358 44.2/F_4 CPU_HTREF0

To Power (37) CPU_VDD_RUN_FB_H — (37) CPU_VDD_RUN_FB_L — T42 — T49

(36) VDDIO_FB_H — (36) VDDIO_FB_L

T15 VDDIO_FB_H — T13 VDDIO_FB_L — T58 CPU_CLK — T59 CPU_CLK# — T47 CPU_TEST29_H_FBCLKOUT_P — T46 CPU_TEST29_L_FBCLKOUT_N

U2D

F8 VDDA2 — F9 VDDA1 — B7 RESET_L — A7 PWROK — E10 LDTSTOP_L — AE4 SIC — AE5 SID — P6 HT_REF1 — R6 HT_REF0 — F6 VDD_FB_H — E6 VDD_FB_L — W9 VDDIO_FB_H — Y9 VDDIO_FB_L — A9 CLKIN_H — A8 CLKIN_L

LDT_RST# — CPU_PWRGD — LDT_STOP_R#

CPU_DBRDY — G10 DBRDY

CPU_TMS — AA9 TMS — CPU_TCK — AC9 TCK — CPU_TRST# — AD9 TRST_L — CPU_TDI — AF9 TDI

THERMTRIP_L — AF6 THERMTRIP# — PROCHOT_L — AC7 CPU_PROCHOT# — DBREQ_L — F10 CPU_DBREQ# — TDO — AE9 CPU_TDO

CPU_PRESENT_L — AC6 CPU_PRESENT# — PSI_L — A3 CPU_PSI# (37)

T51

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

TEST29_H — C9 CPU_TEST29_H_FBCLKOUT_P — R89 80.6/F_4 — TEST29_L — C8 CPU_TEST29_L_FBCLKOUT_N

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

T41 CPU_TEST25_H_BYPASSCLK_H — T44 CPU_TEST25_L_BYPASSCLK_L — T38 CPU_TEST19_PLLTEST0 — T35 CPU_TEST18_PLLTEST1

T45 CPU_TEST17_BP3 — T43 CPU_TEST16_BP2 — T139 CPU_TEST15_BP1 — T54 CPU_TEST14_BP0 — T9 CPU_TEST12_SCANSHIFTENB

H_THERMDC — H_THERMDA

TEST25_H — TEST25_L — TEST19 — TEST18 — TEST13 — TEST9 — TEST24 — TEST23 — TEST22 — TEST21 — TEST20 — TEST28_H — TEST28_L — TEST27 — TEST26 — TEST10 — TEST8 — TEST7 — TEST6 — TEST5 — TEST4 — TEST3 — TEST2

TEST24 — CPU_TEST24_SCANCLK1 — T4
TEST23 — CPU_TEST23_TSTUPD — T6
TEST22 — CPU_TEST22_SCANSHIFTEN — T8
TEST21 — CPU_TEST21_SCANEN — T10
TEST20 — CPU_TEST20_SCANCLK2 — T3
TEST27 — CPU_TEST27_SINGLECHAIN — T5
TEST26 — CPU_TEST26_BURNIN# — T7

T26 CPU_RSVD_MA0_CLK3_P — T25 CPU_RSVD_MA0_CLK3_N — T29 CPU_RSVD_MA0_CLK0_P — T28 CPU_RSVD_MA0_CLK0_N — RSVD0 P20 — RSVD1 P19 — RSVD2 N20 — RSVD3 N19

T23 CPU_RSVD_MB0_CLK3_P — T22 CPU_RSVD_MB0_CLK3_N — T27 CPU_RSVD_MB0_CLK0_P — T19 CPU_RSVD_MB0_CLK0_N — RSVD4 R26 — RSVD5 R25 — RSVD6 P22 — RSVD7 R22

RSVD8 H16 — CPU_MA_RESET# — T39
RSVD9 B18 — CPU_MB_RESET# — T50
RSVD10 R3 — CPU_RSVD_VIDSTRB1 — T138
RSVD11 C1 — CPU_RSVD_VIDSTRB0 — T137
RSVD12 H6 — CPU_RSVD_VDDNB_FB_P — T34
RSVD13 G6 — CPU_RSVD_VDDNB_FB_N — T40
RSVD14 D5 — CPU_RSVD_CORE_TYPE — T48
RSVD15 R24 — CPU_RSVD_15 — T21
RSVD16 W18 — CPU_RSVD_16 — T12
RSVD17 R23 — CPU_RSVD_17 — T20
RSVD18 AA8 — CPU_RSVD_18 — T11
RSVD19 H18 — CPU_RSVD_19 — T36
RSVD20 H19 — CPU_RSVD_20 — T37

MISC

AMD NPT S1 SOCKET Processor Socket

+1.8V_SUS — R38 10K_4 — R34 *4.7K — R41 300_4 — R22 300_4 — R104 300_4 — THERM_B1

Q1 MMST3904 — C49 0.1U/16V_4 — H_THERMTRIP# (15)

VID5 (37) — VID4 (37) — VID3 (37) — VID2 (37) — VID1 (37) — VID0 (37)

(2) CPU_CLK — C529 3900P/50V_4 — CPU_CLKIN_SC_P — CPU_CLKIN_SC_N — R373 169/F_4 — (2) CPU_CLK# — C528 3900P/50V_4

1.KEEP TRACE TO RESISTOR LESS THAN 600MILS FROM CPU PIN AND TRACE TO AC CAPS LESS THAN 1250MILS.

2. CPUCLK and CPUCLK# mismatch < 35 mils.

+1.8V_SUS

CPU_TEST27_SINGLECHAIN — R347 *300_4
CPU_TEST26_BURNIN# — R346 300_4
CPU_PRESENT# — R44 1K/F_4
CPU_TEST25_H_BYPASSCLK_H — R90 510/F_4

CPU_TEST21_SCANEN — R26 300_4
CPU_TEST20_SCANCLK2 — R45 *300_4
CPU_TEST24_SCANCLK1 — R349 *300_4
CPU_TEST22_SCANSHIFTEN — R350 *300_4
CPU_TEST12_SCANSHIFTENB — R27 *300_4
CPU_TEST15_BP1 — R94 *300_4
CPU_TEST14_BP0 — R93 *300_4
CPU_TEST25_L_BYPASSCLK_L — R95 510/F_4
CPU_TEST19_PLLTEST0 — R64 300_4
CPU_TEST18_PLLTEST1 — R65 300_4

If no use which Net need pull-up or down

+1.8V_SUS — +3.3V — R40 *10K_4 — R42 *4.7K_4 — Q2 *MMBT3904 — CPU_PROCHOT# — SB_CPU_PROCHOT# (16) — VR_TT# (37)

HDT CONNECTOR

+1.8V_SUS — *220_4 ×6 — R32 R28 R48 R29

JHDT1

1	GND	GND	2
3	Resreved1	GND	4
5	Resreved2	GND	6
7	DBREQ_L	GND	8
9	DBRDY	GND	10
11	TCK	GND	12
13	TMS	GND	14
15	TDI	GND	16
17	TRST_L	GND	18
19	TDO	GND	20
21	VDDIO1	GND	22
23	VDDIO2	RESET_L	24
		GND	25

*HDT conn

CPU_DBREQ# — CPU_DBRDY — CPU_TCK — CPU_TMS — CPU_TDI — CPU_TRST# — CPU_TDO

+3.3V — R379 4.7K_4 — +1.8V — R381 4.7K_4 — CPU_RESET# — Q37 MMBT3904 — LDT_RST#

R380 *100K_4

C671 0.1U/10V/X7R_4 — C672 0.1U/10V/X7R_4 — C673 0.1U/10V/X7R_4 — C674 0.1U/10V/X7R_4 — C675 0.1U/10V/X7R_4 — C670 0.1U/10V/X7R_4 — C689 0.1U/10V/X7R_4

EC C-01

NOTE:HDT TERMINATION IS REQUIRED FOR REV.Ax SILICON ONLY.

CPU Thermal monitor

+3.3V — Q4 2N7002W-7-F — (30) ABCLK — ABCLK — THCLK_SMB

Q6 2N7002W-7-F — (30) ABDATA — ABDATA — THDAT_SMB

(16) THERM_ALERT# — R85 *0_4

Q7 2N7002W-7-F — (34) SYS_SHDN# — 6648OVERT#

+3.3V — R88 220_6 — 6648VCC — C207 0.1U/10V/X5R_4

R82 10K_4 — R83 10K_4 — R84 10K_4 — R87 *10K_4

U3

SCLK	8	VCC	1
SDA	7	DXP	2
ALERT#	6	DXN	3
OVERT#	4	GND	5

G781P8 ADDRESS: 98H

H_THERMDA — C208 2200P/50V_6 — H_THERMDC

Layout Note: Routing 10:10 mils and away from noise source with ground gard

+5V — 30 mil — U21 G993P1U — VEN VIN VO SET GND GND GND GND — C539 1U/10V/X5R_6 — C536 0.1U/10V/X5R_4 — C537 10U/10V/X5R_8 — C548 1000P/16V/X7R_4

(30) PWM_FAN1 — R378 0_4 — +5V_FAN — C534 *0.1U/10V/X5R_4

EC C-02

30 mil — +5V_FAN — CN21 FAN

+3.3V — Q39 PDTA124EU — (30) FANSIG1 — R409 100K_4

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Quanta Computer Inc.		
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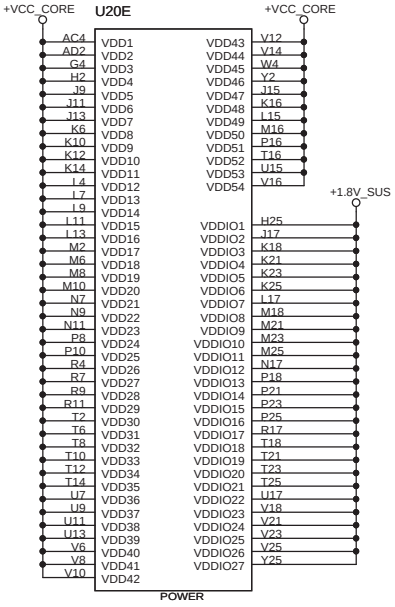
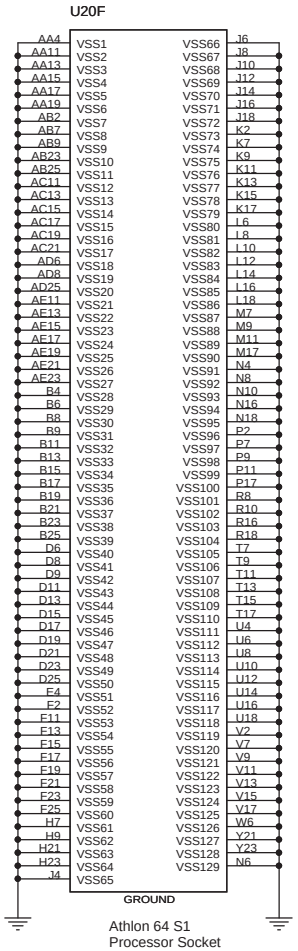
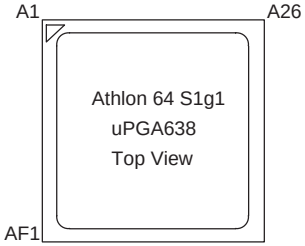
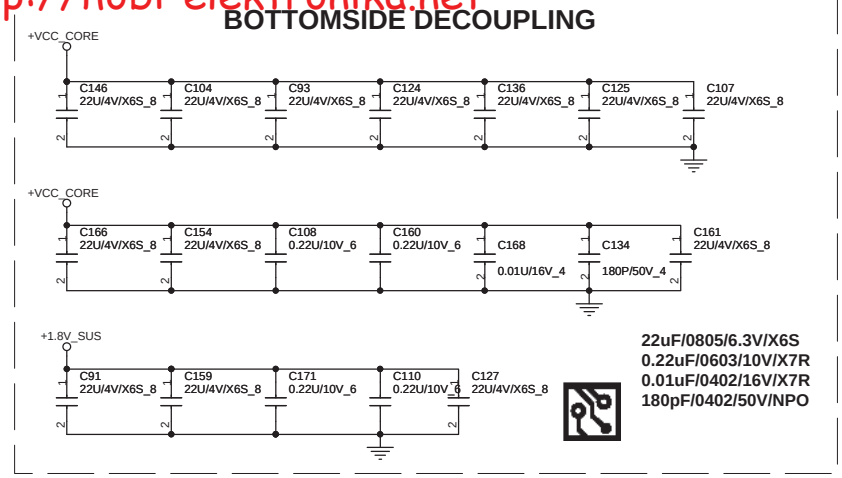


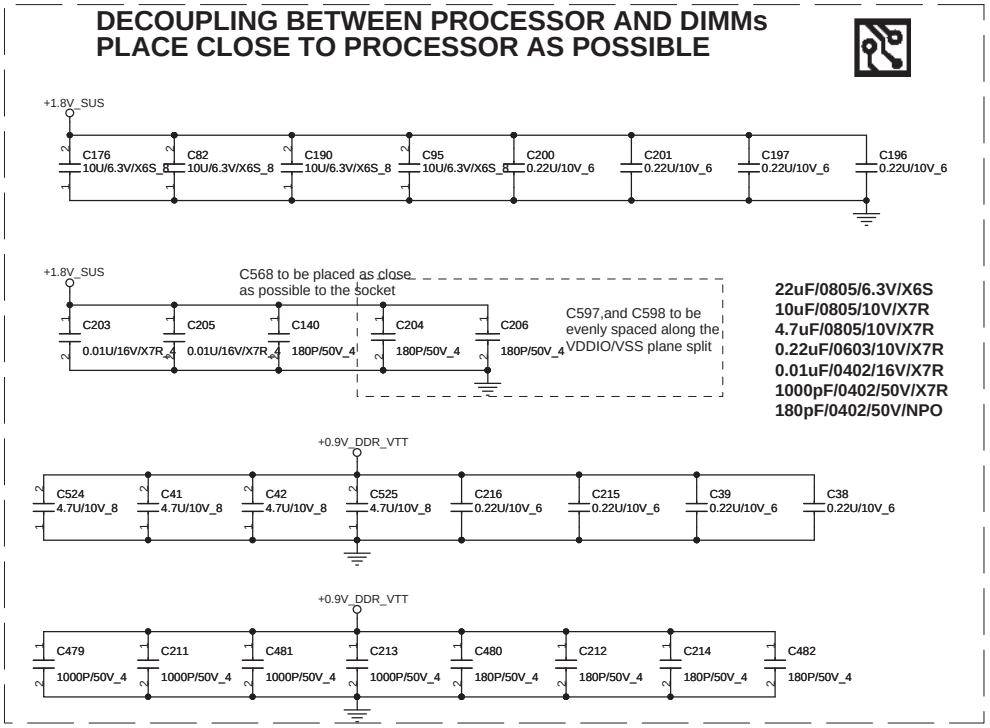
Athlon 64 S1
Processor Socket



Athlon 64 S1
Processor Socket







PROCESSOR POWER AND GROUND

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Quanta Computer Inc.

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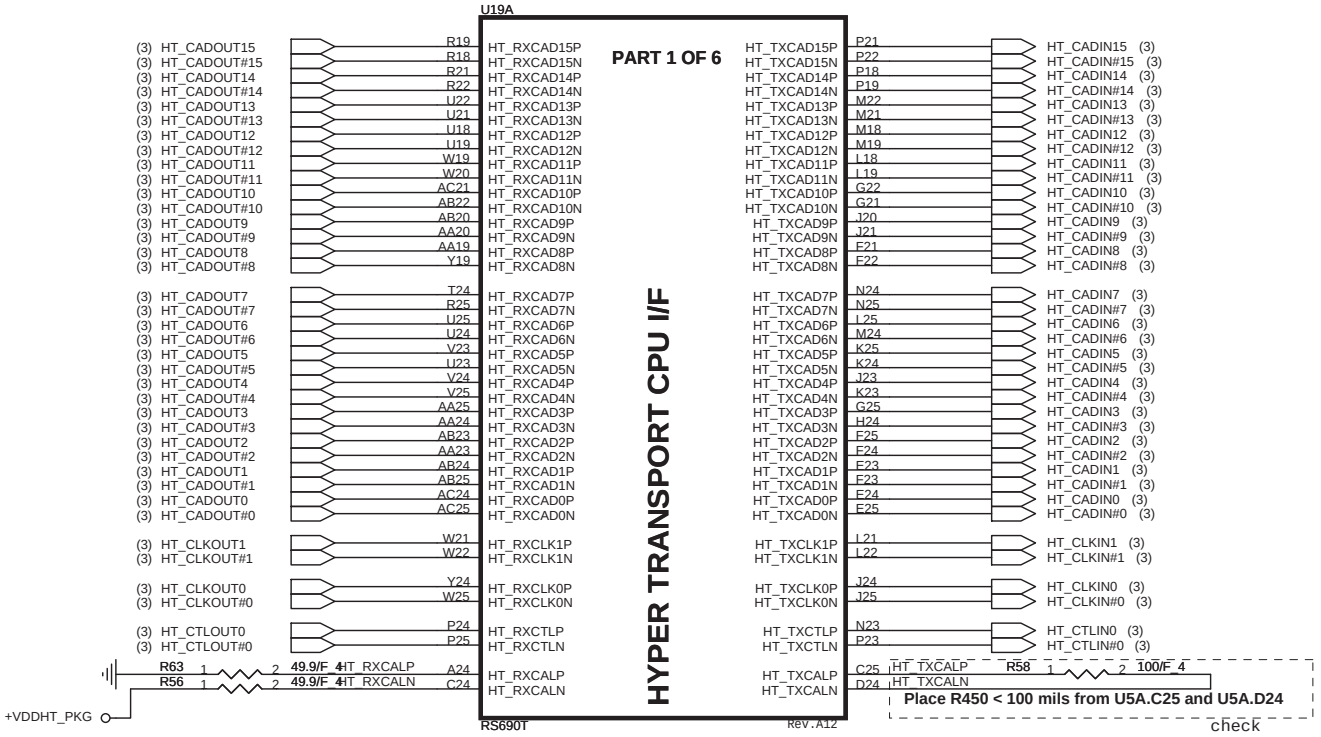
Change Part Number



PROJECT : SA1A Quanta Computer Inc.		
Size: B	Document Number: RS690T-HT LINK0 I/F	Rev: 3A
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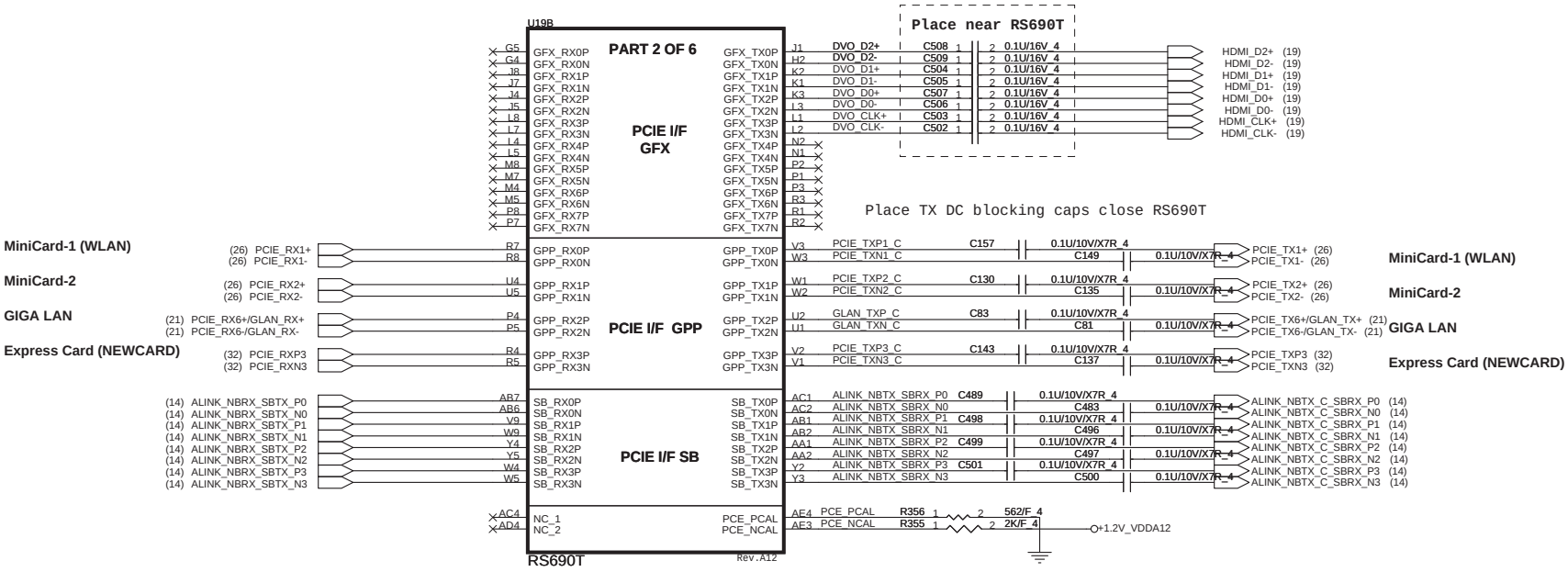

PROJECT : SA1A
Quanta Computer Inc.

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+1.8V L53 BLM15AG221SN1D +1.8V_AVDDQ C523 *10U/10V_8 C181 2.2U/10V_6
+1.8V L52 BLM15AG221SN1D +1.8V_PLLVDD C522 *10U/10V_8 C518 2.2U/10V_6
+1.8V L51 BLM15AG221SN1D +1.8V_HTPVDD C514 *10U/10V_8 C517 4.7U_6.3V_6 C513 1U/6.3V_4

+3.3V L54 BLM18PG330SN1D +3.3V_AVDD C521 2.2U/10V_6 — 20mil Width
+1.8V R366 0_4 +1.8V_RUN_AVDDDI C520 2.2U/10V_6 — 20mil Width
+1.8V_AVDDQ — 20mil Width

U19C RS690T

AVDD1 B22	AVDD2 C22	AVSSN1 G17
AVSSN2 H17	AVDDDI A20	AVSSDI B20
AVDDQ A21	AVSSQ A22	
C_R C21	Y_G C20	COMP_B D19
RED F19	GREEN F19	BLUE G19
DACVSYNC C6	DACHSYNC A5	RSET B21
DACSCL B6	DACSDA A6	
PLLVDD18(PLLVDD) A10	PLLVSS B10	
HTPVDD B24	HTPVSS B25	
VDDPLL_1(VDDA12) F7	VDDPLL_2(VDDA12) F7	VSSPLL_1(VSSA12) F9
VSSPLL_2(VSSA12) G9		
SYSRESET# C10	POWERGOOD C11	LDTSTOP# C5
ALLOW_LDTSTOP# B5		
HTTSTCLK C23	HTREFCLK B23	TVCLKIN C2
OSCIN B11	PLLVDD12(OSCOUT) A11	
GFX_CLKP F2	GFX_CLKN E1	
SB_CLKP G1	SB_CLKN G2	
BMREQb B2	I2C_CLK A2	I2C_DATA B4
THERMALDIODE_P AD5	THERMALDIODE_N AE5	
TMDS_HPD C14	DDC_DATA B3	TESTMODE C3
STRP_DATA A3		

PART 3 OF 6 — CRT/TVOUT — PLL PWR — PM — CLOCKs — MIS.

TXOUT_L0P B14	TXOUT_L0N B15	TXOUT_L1P B13
TXOUT_L1N A13	TXOUT_L2P H14	TXOUT_L2N G14
TXOUT_L3P D17	TXOUT_L3N E17	
TXOUT_U0P A15	TXOUT_U0N B16	TXOUT_U1P C17
TXOUT_U1N C18	TXOUT_U2P B17	TXOUT_U2N A17
TXOUT_U3P A18	TXOUT_U3N B18	
TXCLK_LP F15	TXCLK_LN D15	TXCLK_UP H15
TXCLK_UN G15		
LPVDD D14	LPVSS E14	
LVDDR18D_1 A12	LVDDR18D_2 B12	LVDDR33A_1 C12
LVDDR33A_2 C13		
LVSSR1 A16	LVSSR3 A14	LVSSR5 D12
LVSSR6 C19	LVSSR7 C15	LVSSR8 C16
LVSSR12 F14	LVSSR13 F15	
LVDS_DIGON E12	LVDS_BLON G12	LVDS_BLEN F12
DFT_GPIO0 D6	DFT_GPIO1 D7	DFT_GPIO2 C8
DFT_GPIO3 C7	DFT_GPIO4 B8	DFT_GPIO5 A8

R446,R455,R461 CLOSE TO NB

(20) INT_CRT_RED, (20) INT_CRT_GRN, (20) INT_CRT_BLU — R59 150_4, R53 150_4, R51 150_4
(20) INT_VSYNC, (20) INT_HSYNC — R60 715/F
(20) INT_CRT_DDCCLK, (20) INT_CRT_DDCDAT
+1.8V_PLLVDD — 20mil Width
+1.8V_HTPVDD — 20mil Width

+1.2V_VDDA12 L15 BLM21PG221SN1D <Imax> <Size> +1.2V_VDDPLL C116 4.7U_6.3V_0603 C123 1U — 30mil Width
RS690: 220 Ohm 2A FB

(14,20,21,26,27,32) PLTRST# — R73 0_4
(30) NB_PWRGD — R62 0_4
(14) ALLOW_LDTSTOP — LDT_STOP# NB

AC Term closely clock pin for length: 50 mils
(2) CLK_HTREF_66M — R61 *22 C156 *22P
(15,30) SUS_STAT# — R362 10K_4, R360 0_4
(2) CLK_NB_14M — R66 33 C177 22P
+1.2V_PLLVDD12
AC Term closely clock pin for length: 50 mils

(2) NBSRC_CLKP, (2) NBSRC_CLKN
(2) SBSRCCLK, (2) SBSRCCLK#
BMREQ# D
(18) INT_LVDS_EDIDCLK, (18) INT_LVDS_EDIDDATA
NB_THERMDA, NB_THERMDC
TMDS_HPD
(35) NB_VCORE_CNTRL — R364 4.7K

+1.2V_VDDA12 L20 BLM15AG221SN1D +1.2V_PLLVDD12 C179 2.2U/10V_6
+3.3V R359 4.7K_4 SUS_STAT#

+3.3V R371 4.7K, R372 10K_4 — Q36 MMBT3904
(5,14) LDT_STOP# — LDT_STOP#_NB

+3.3V R363 10K_4 — B2-USB performance
Add R363 and Del R365
(14) BMREQ# — C512 *15P/50V_4 — D25 *SDMK0340L-7-F — R365 *0_4 — BMREQ# D

+3.3V U2 *AT24C04N-10SU-2.7 — R77 *10K_4, R68 *2K_4
INT_LVDS_EDIDCLK, NB_VCORE_CNTRL
C188 *0.1U/16V_4, R78 *2K_4

A04
C-test-For HDMI Hot Plug
R79 and R86 Change to 0 ohm
Del-C193 and R80 and D3
(19) HDMI_DET — R79 0_4 — EC C-13 — R86 0_4 — TMDS_HPD
C193 *0.01U, R80 100K_4, D3 *UDZ2.4B-TE-17

B3
Change P/N
+3.3V R69 39K — INT_LVDS_EDIDCLK — Q3 FDV301N — +5V R67 15K/F_4 — HDMI_CTRLCLK — HDMI_CTRLCLK (19)
+3.3V R368 39K, R369 39K — INT_LVDS_EDIDDATA — R370 *0_4 — Q5 FDV301N — +5V R81 15K/F_4 — HDMI_CTRLDATA — HDMI_CTRLDATA (19)
DDC_DATA — R367 0_4

+1.8V R76 10K — EC C-03

R52 100K_4

	PU by internal	PD by external
DFT_GPIO0	Side-Port Memory Disable	Side-Port Memory Enable (Default)
DFT_GPIO1	Bypassing EEPROM, use default values (Default)	Using EEPROM Strapping
DFT_GPIO[4:2]	Set PCI-E GPP mode to Conf. E	Select PCI-E GPP mode
DFT_GPIO5	Use default values (Default)	Use the memory data bus for debug bus output

NOTE: ACCESS TO STRAP_DATA and I2C_CLK PINS IS MANDATORY.

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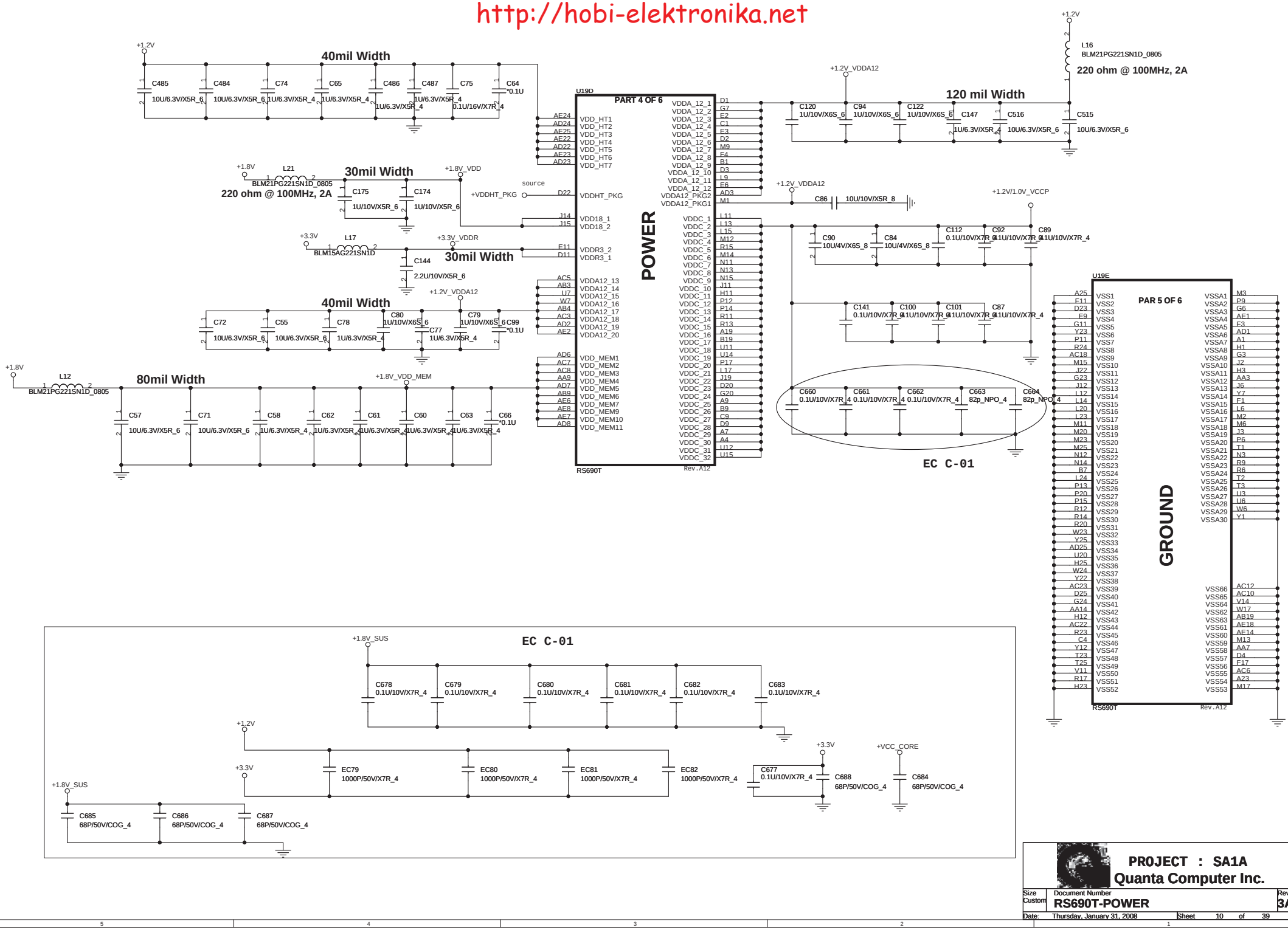

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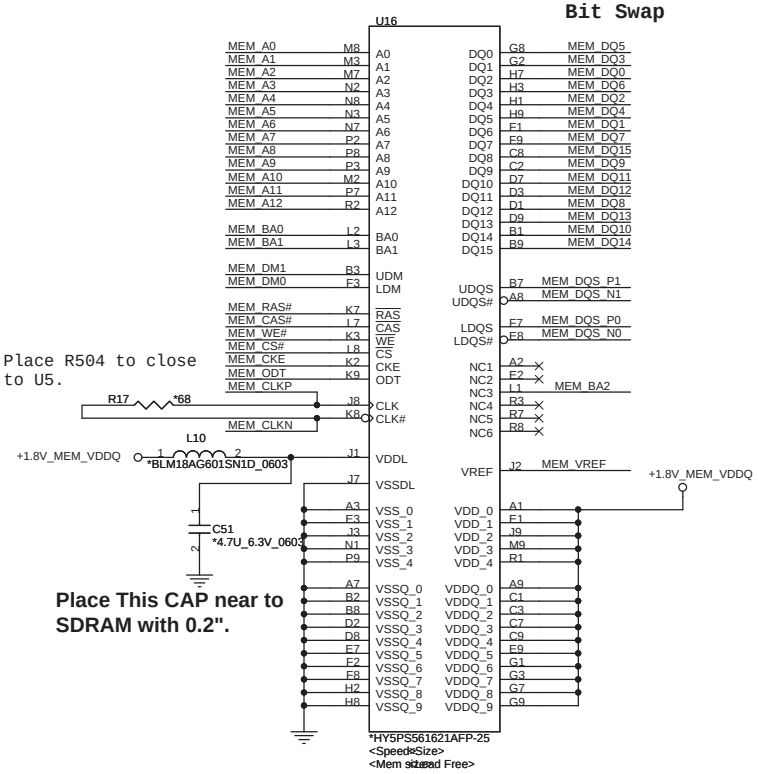
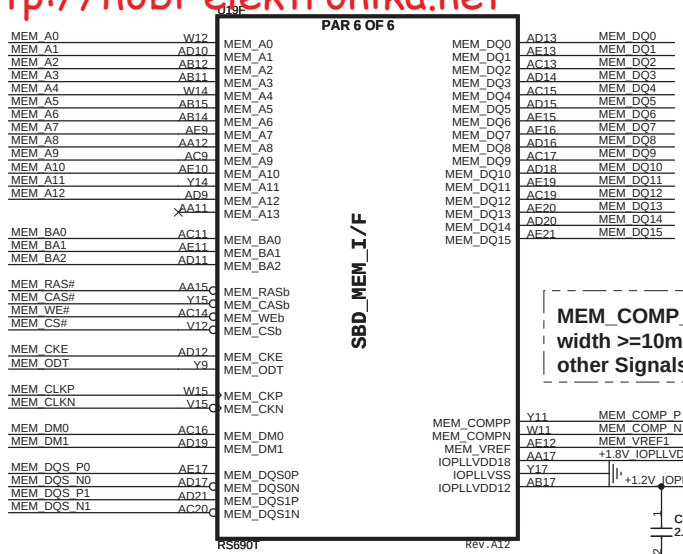
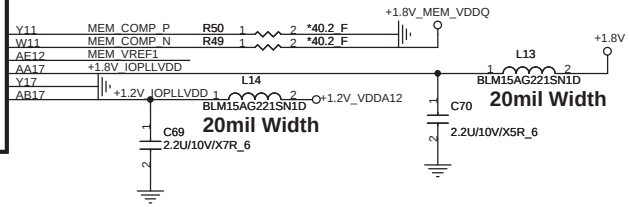
Bit Swap

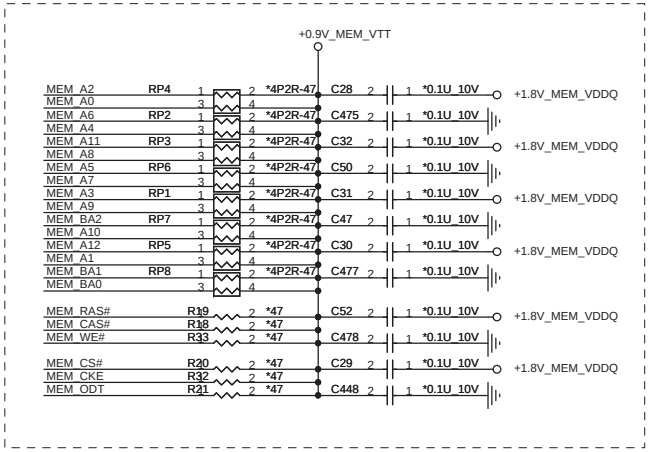


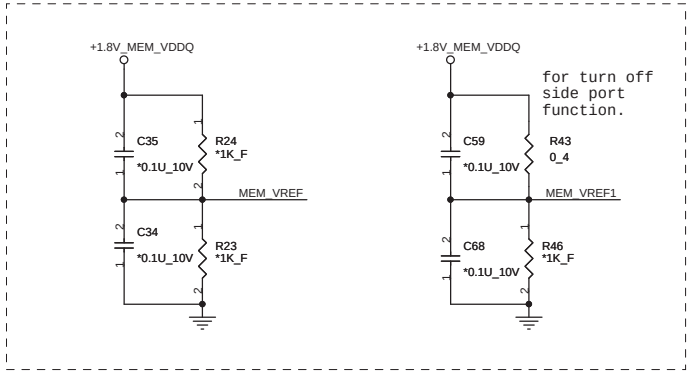
256-Mbit DDR2 16Mbit*16(4bank)

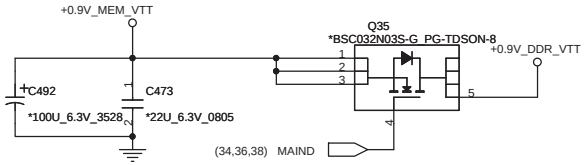


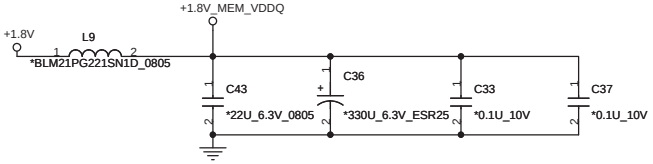
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions











Local Frame Buffer(64MB) DDRII Power

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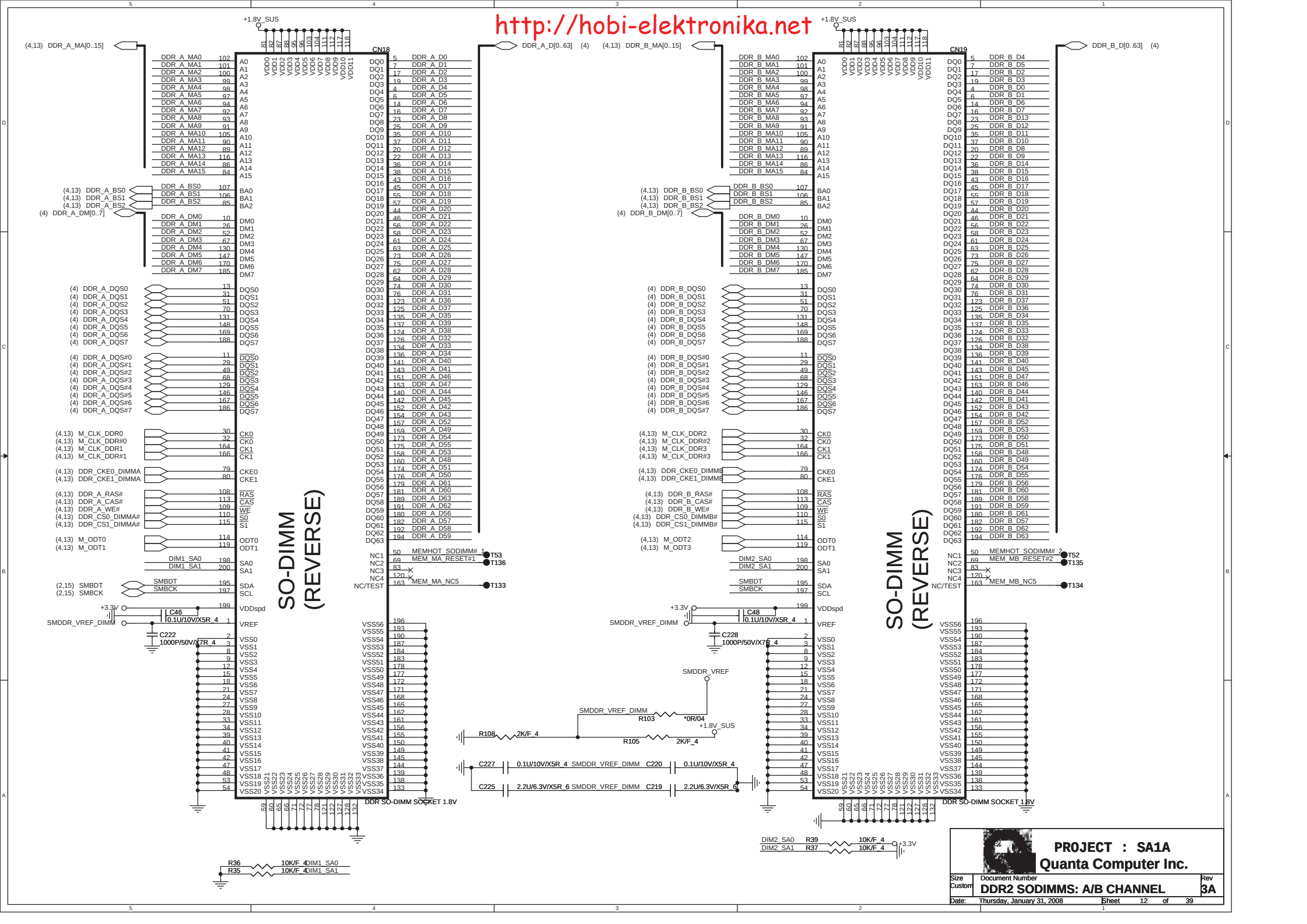
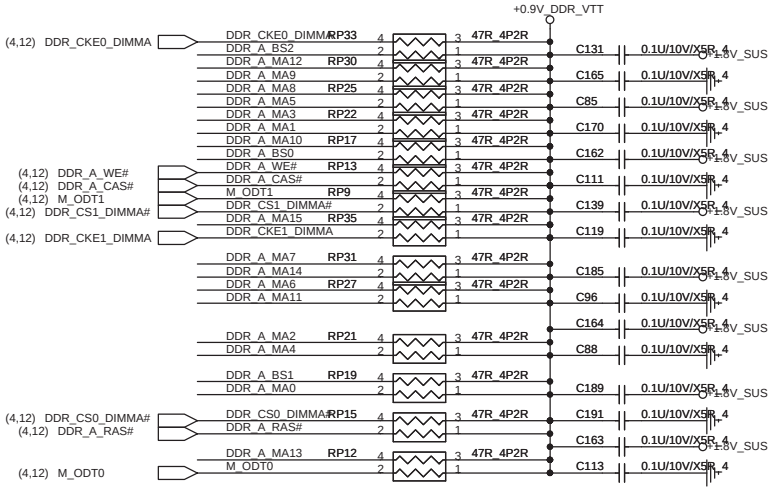
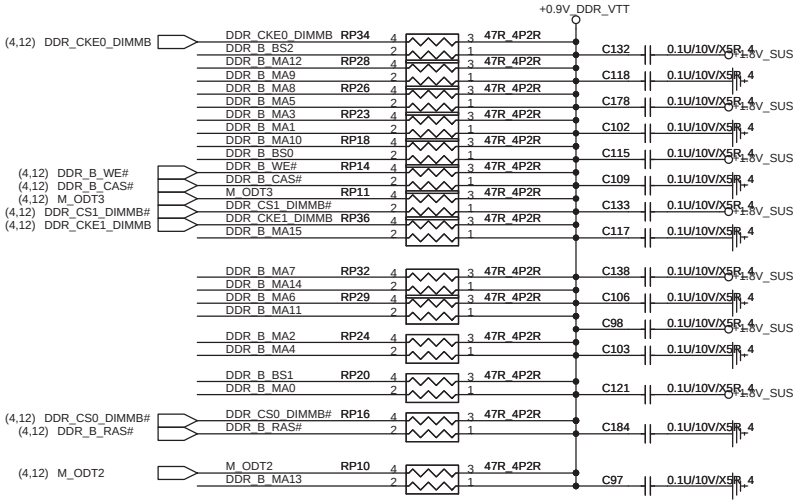
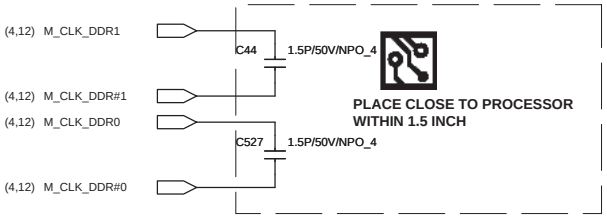


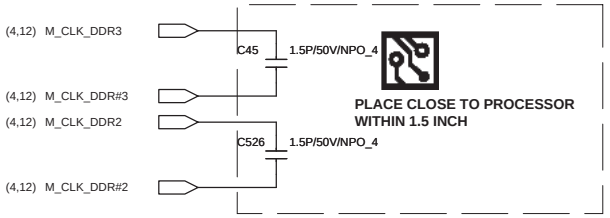
(4,12) DDR_A_MA[0..15] — DDR_A_MA[0..15]
(4,12) DDR_A_BS[0..2] — DDR_A_BS[0..2]

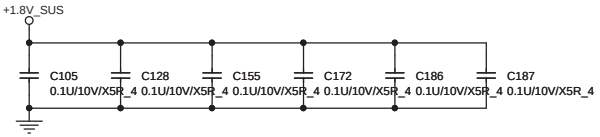
(4,12) DDR_B_MA[0..15] — MEM_MB_ADD[0..15]
(4,12) DDR_B_BS[0..2] — DDR_B_BS[0..2]

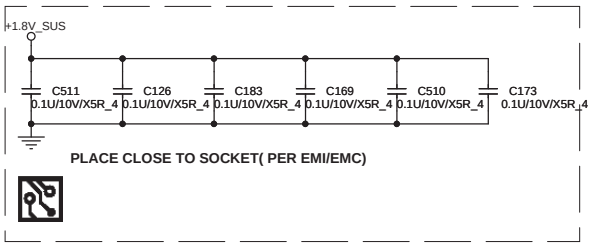












PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	3A
Date: Thursday, January 31, 2008	Sheet 13 of 39	

SB600 SB 27x27mm
Part 1 of 4

Place R346,R348,R344
< 100mils from pins E27,E28,E29

20mil Width

PCIE Power

50mil Width

NOTE: Nopop L68. Keep in case ATI provides a fixed SB600. Can pop L68 and Nopop L74 and the +1.2V_PCIE_PVDD switch circuit for cost savings.

ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.

EC C-03

EC C-04

H_DPSLP# should be put down , reserve R592 for verifing

EC C-16

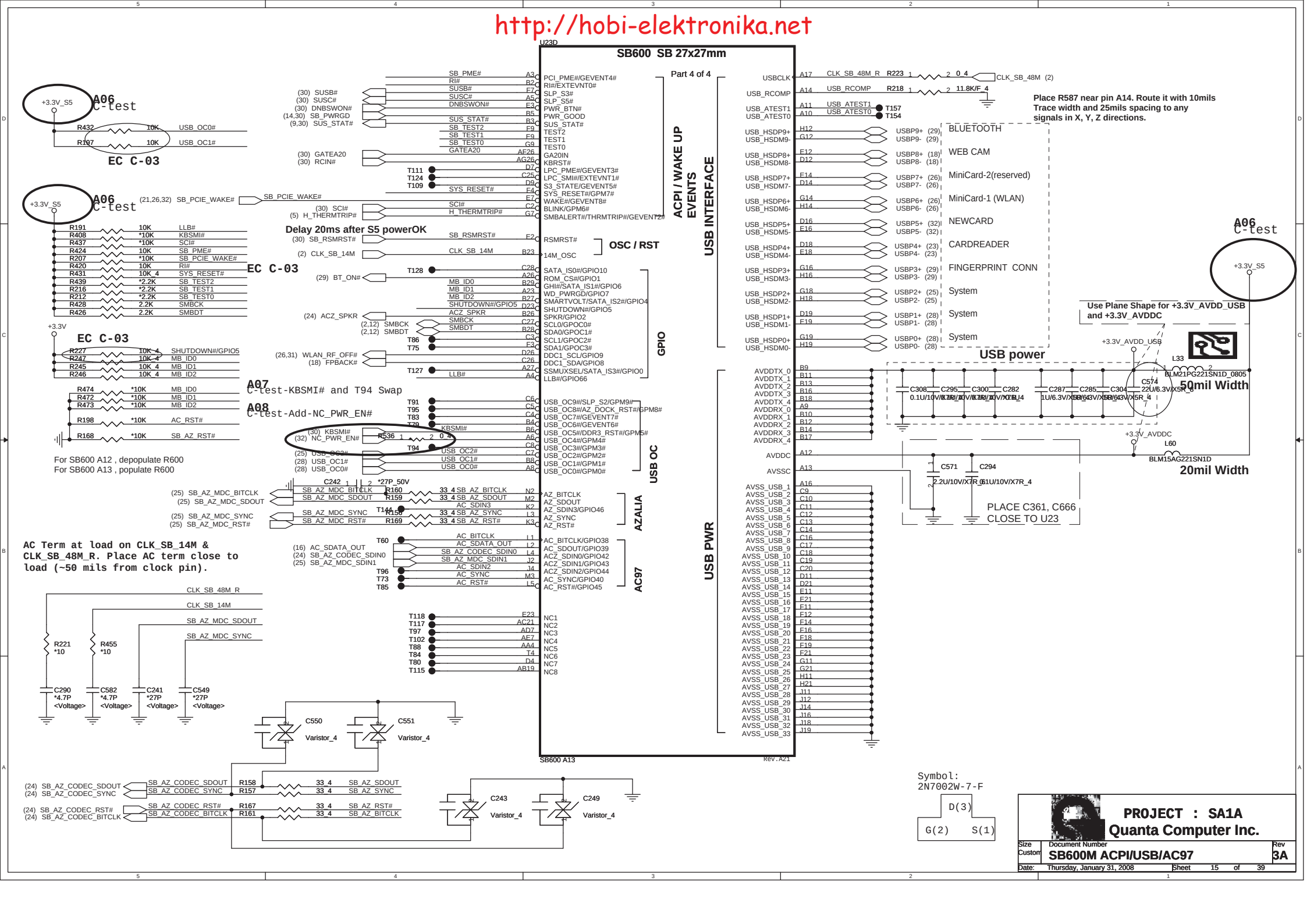
Option to "Disable" clkrun. Pulling it down will keep the clocks running.

RTC

A05
C-test-Pin define

SB600 A13

PROJECT :	SA1A
Quanta Computer Inc.	
Size: Custom	Document Number: SB600M-PCIE/PCI/LPC
Rev: 3A	
Date: Thursday, January 31, 2008	Sheet 14 of 39



SB600 SB 27x27mm

Part 2 of 4

U23B

SATA clock

C292 27P/50V/NPO_4 — Y5 25MHZ — R224 10M_4 — C323 27P/50V/NPO_4

SATA_X1 — SATA_X2

SATA Power

+3.3V — L31 BLM15AG221SN1D — +3.3V_XTLVDD_SATA

C305 1U/10V/X6S_6 — C311 *0.1U

CAP CLOSE TO THE BALL OF SB600

+1.2V — L32 BLM15AG221SN1D — +1.2V_PLLVDD_SATA

C289 1U/6.3V/X5R_4 — C296 *0.1U — C280 22U/6.3V/X5R_8

+1.2V — L34 BLM21PG221SN1D <Size> — +1.2V_AVDD_SATA

C328 22U/6.3V/X5R_8 — C314 1U/6.3V/X5R_4 — C320 1U/6.3V/X5R_4 — C318 0.1U/10V/X7R_4 — C312 0.1U/10V/X7R_4

+1.2V_AVDD_SATA

C324 *0.1U — C298 *0.1U — C301 *0.1U

+5V — R206 4.7K_4 — +3.3V — R192 4.7K_4 — R215 1K/F_4 <Tolerance> — SATA_CAL

Q13 MMBT3904 — (31) SATA_LED# — SATA_ACT#

+1.2V_PLLVDD_SATA — +3.3V_XTLVDD_SATA — +1.2V_AVDD_SATA

SERIAL ATA

(27) SATA_TX0+	C586 0.01U/16V/X7R_4 SATA_TX0+_C	AH21 SATA_TX0+
(27) SATA_TX0-	C584 0.01U/16V/X7R_4 SATA_TX0-_C	AJ21 SATA_TX0-
(27) SATA_RX0-	SATA_RX0-	AH20 SATA_RX0-
(27) SATA_RX0+	SATA_RX0+	AJ20 SATA_RX0+
	T167	AH18 SATA_TX1+
	T163	AJ18 SATA_TX1-
	T162	AH17 SATA_RX1-
	T161	AJ17 SATA_RX1+
	T114	AH13 SATA_TX2+
	T112	AH14 SATA_TX2-
	T113	AH16 SATA_RX2-
	T160	AJ16 SATA_RX2+
	T156	AJ11 SATA_TX3+
	T155	AH11 SATA_TX3-
	T158	AH12 SATA_RX3-
	T159	AJ13 SATA_RX3+
		AE12 SATA_CAL
SATA_X1		AD16 SATA_X1
SATA_X2		AD18 SATA_X2
SATA_ACT#		AC12 SATA_ACT#/GPIO67

ATA 66/100

IDE_IORDY	AB29	IDE_DIORDY (27)
IDE_IRQ	AA28	IDE_IRQ (27)
IDE_A0	AA29	IDE_DA0 (27)
IDE_A1	AB27	IDE_DA1 (27)
IDE_A2	Y28	IDE_DA2 (27)
IDE_DACK#	AB28	IDE_DDACK# (27)
IDE_DRQ	AC27	IDE_DDREQ (27)
IDE_IOR#	AC29	IDE_DIOR# (27)
IDE_IOW#	AC28	IDE_DIOW# (27)
IDE_CS1#	W28	IDE_DCS1# (27)
IDE_CS3#	W27	IDE_DCS3# (27)
IDE_D0/GPIO15	AD28	IDE_DD0
IDE_D1/GPIO16	AD26	IDE_DD1
IDE_D2/GPIO17	AE29	IDE_DD2
IDE_D3/GPIO18	AE27	IDE_DD3
IDE_D4/GPIO19	AG29	IDE_DD4
IDE_D5/GPIO20	AH28	IDE_DD5
IDE_D6/GPIO21	AJ28	IDE_DD6
IDE_D7/GPIO22	AJ27	IDE_DD7
IDE_D8/GPIO23	AH27	IDE_DD8
IDE_D9/GPIO24	AG27	IDE_DD9
IDE_D10/GPIO25	AG28	IDE_DD10
IDE_D11/GPIO26	AE28	IDE_DD11
IDE_D12/GPIO27	AF29	IDE_DD12
IDE_D13/GPIO28	AE28	IDE_DD13
IDE_D14/GPIO29	AD25	IDE_DD14
IDE_D15/GPIO30	AD29	IDE_DD15

IDE_DD[0..15] (27)

A10 C-test-Change

SPI ROM

SPI_DI/GPIO12	J3	T87
SPI_DO/GPIO11	J6	T63
SPI_CLK/GPIO47	G3	T76
SPI_HOLD#/GPIO31	G2	T67
SPI_CS#/GPIO32	G6	T100
LAN_RST#/GPIO13	C23	T168
ROM_RST#/GPIO14	G5	T99

SERIAL ATA POWER

FANOUT0/GPIO3	M4	T103
FANOUT1/GPIO48	T3	
FANOUT2/GPIO49	V4	
FANIN0/GPIO50	N3	T77
FANIN1/GPIO51	P2	T72
FANIN2/GPIO52	W4	T82
TEMP_COMM	P5	R429 0_4
TEMPIN0/GPIO61	P7	T71
TEMPIN1/GPIO62	P8	T105
TEMPIN2/GPIO63	T8	T107
TEMPIN3/TALERT#/GPIO64	T7	R163 0_4 SB_CPU_PROCHOT#

SB_CPU_PROCHOT# (5)

BIOS should not enable the internal GPIO pull up resistor

VIN0/GPIO53	V5	THERM_ALERT# (5)
VIN1/GPIO54	L7	LAN_DISABLE# (21)
VIN2/GPIO55	M8	LOM_PCIE_RST#
VIN3/GPIO56	V6	NC_GPIO56 T110 T98
VIN4/GPIO57	M6	LBF_ID0
VIN5/GPIO58	P4	LBF_ID1
VIN6/GPIO59	M7	LBF_ID2
VIN7/GPIO60	V7	

HW MONITOR

+3.3V_AVDD_HWM — +3.3V

AVDD N1 — AVSS M1

20mil Width

L30 BLM15AG221SN1D — L65 *BLM15AG221SN1D — +3.3V_S5

C265 2.2U/10V/X5R_6 — C270 0.1U/10V/X7R_4

HWM_AGND — R166 0_4

HWM_AGND TRACE AT LEAST 10MIL WIDE

Close to SB600

B04 Requirement from AMD.

SB600 A13

REQUIRED STRAPS

15K internal PU for RTC_CLK
,External PU/PD is not required.
SB600 has 15K internal PD for AC_SDOUT

+3.3V — R145 *2.2K — R397 *10K — R396 10K_4 — R194 *10K_4 — R146 10K

(15) AC_SDATA_OUT

(14) CLK_PCI_DOCK

(14,26) PCLK_LPC_DEBUG

(14) PCI_CLK0

(14) PCI_CLK1

A09 C-test-Del — A09 C-test-Add

R398 10K_4 — R182 10K — R147 *10K_4

A09 C-test-Add — A09 C-test-Del

Net Name	AC_SDOUT	CLK_PCI_DOCK	CLK_PCI_PCCARD	PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 Default	H, H = PCI ROM Default H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS Default	USE EXT. 48MHZ Default	CPU IF=P4	

+3.3V — R144 *10K — R155 *10K — R152 *10K

R143 10K_4 — LBF_ID0
R154 10K_4 — LBF_ID1
R153 10K_4 — LBF_ID2

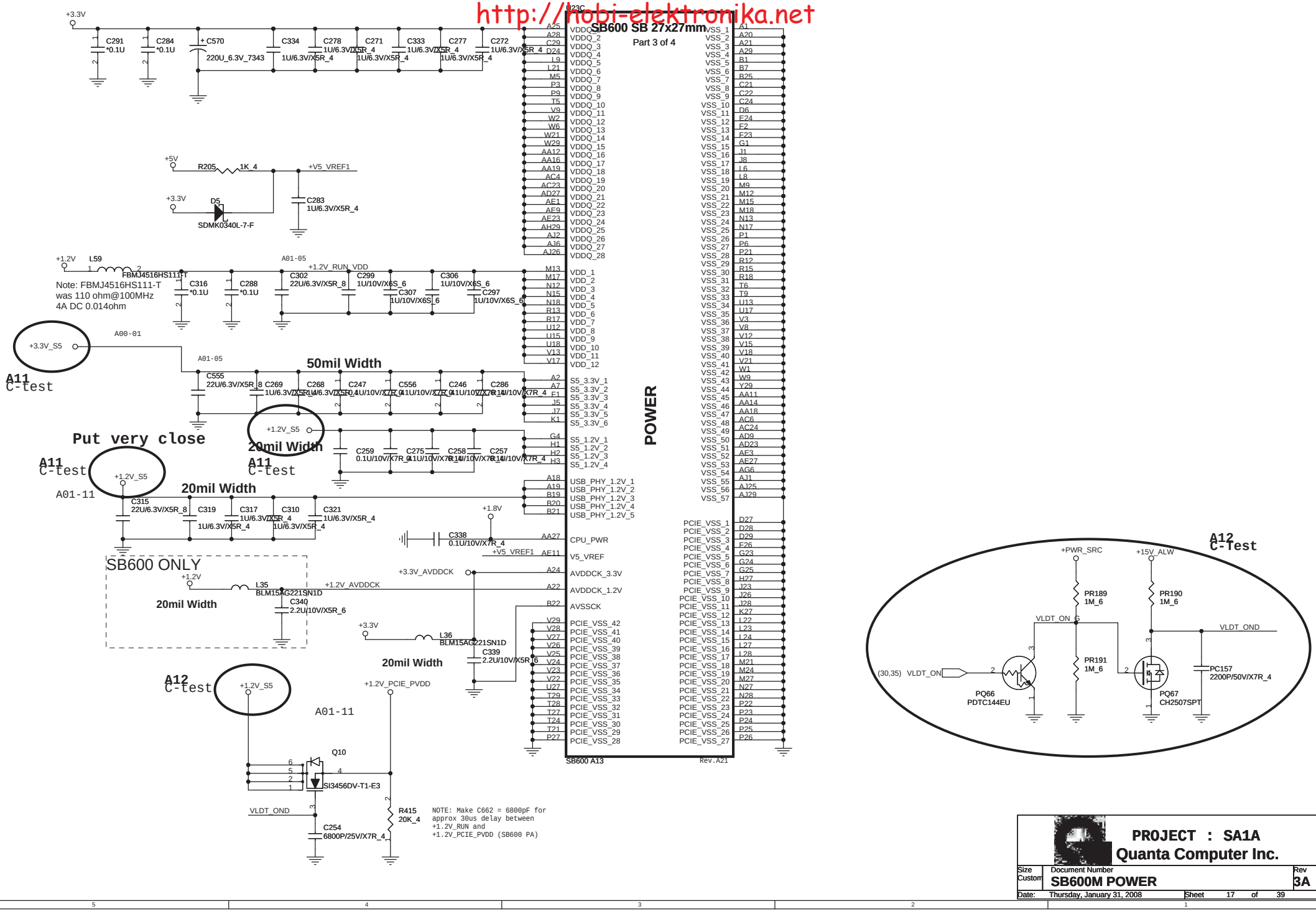
Memory Vendor	LBF_ID2	LBF_ID1	LBF_ID0
Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0

NC_GPIO56	R162	*20K
THERM_ALERT#	R202	*20K
LAN_DISABLE#	R208	*20K
LOM_PCIE_RST#	R214	*20K

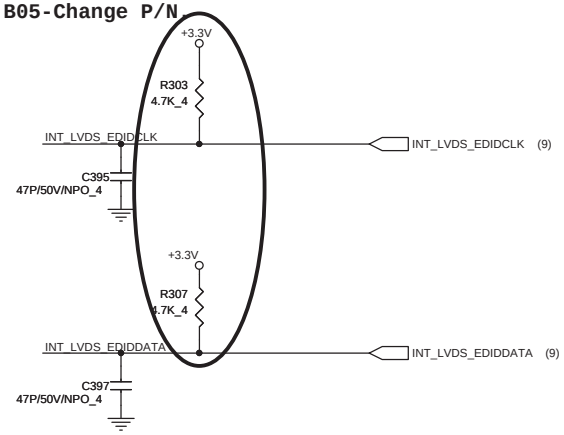
PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB600M HDD/POWER	3A

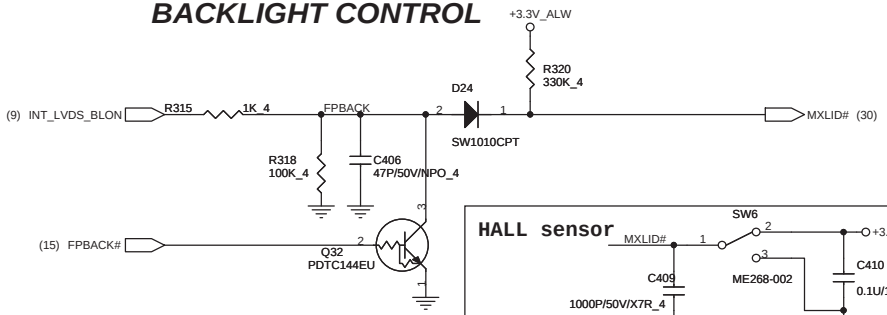
Date: Thursday, January 31, 2008 Sheet 16 of 39

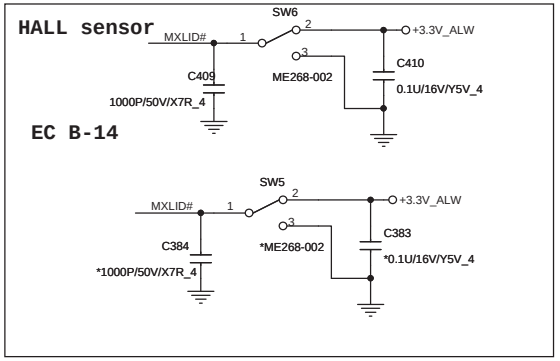


B05-Change P/N

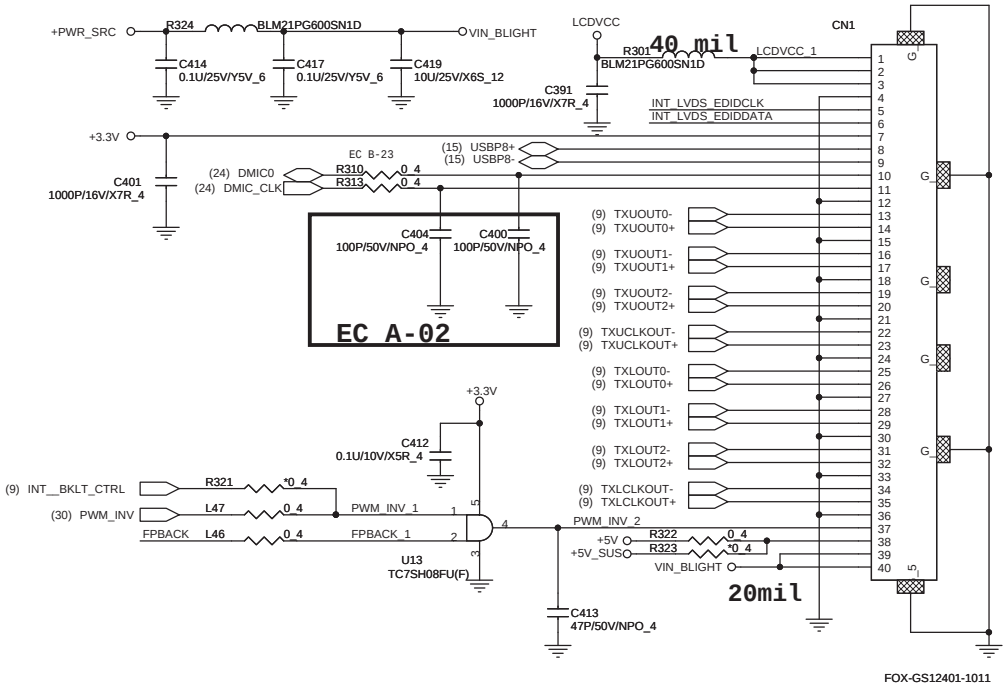


BACKLIGHT CONTROL



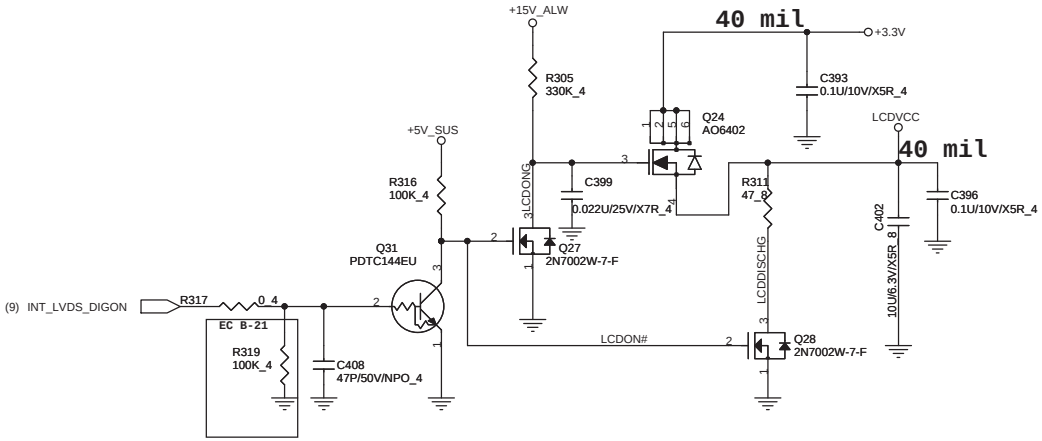


LCD CONNECTOR(Include WEB CAM function)



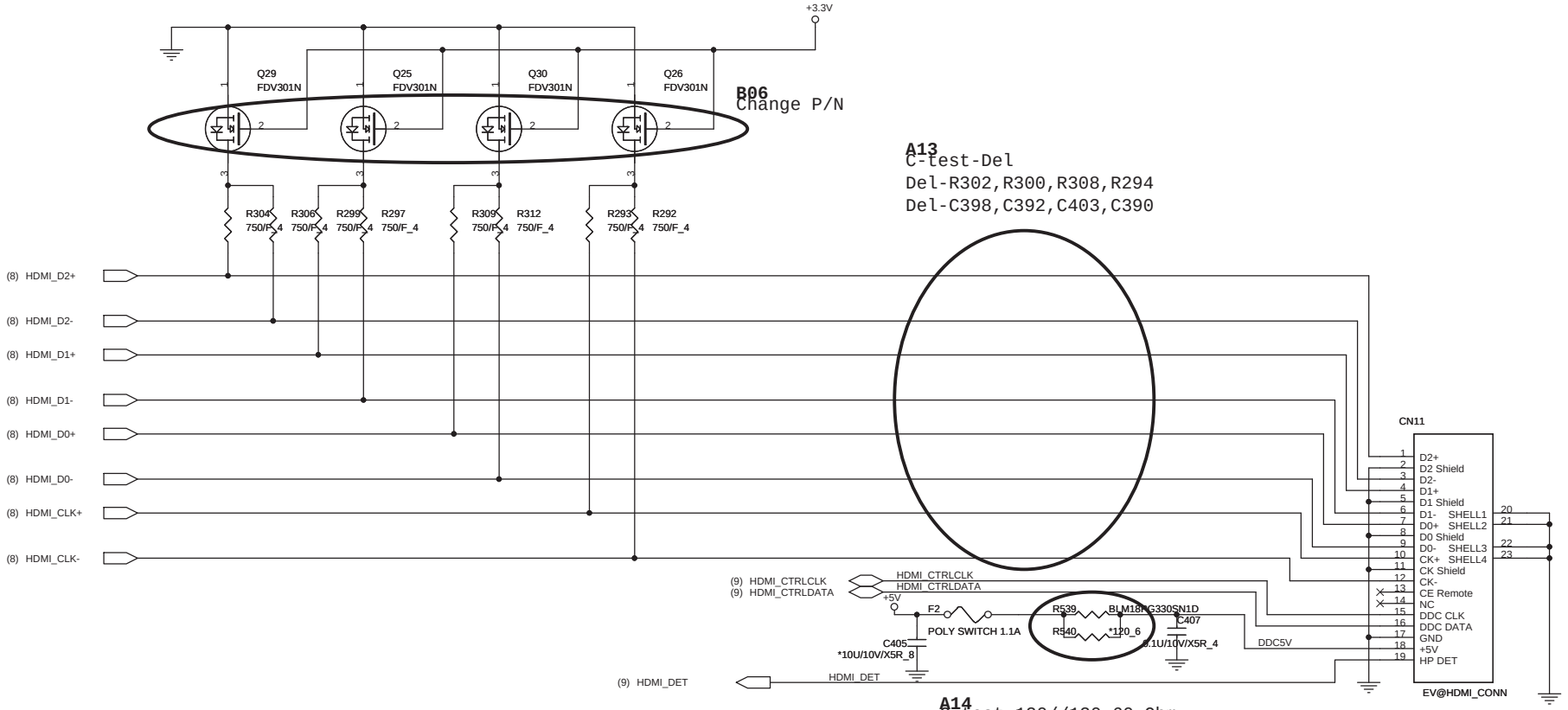
TO PANEAL

PANEL VCC CONTROL



PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS/LCD CONN/LID/WEB CAM	3A
Date: Thursday, January 31, 2008	Sheet 18 of 39	

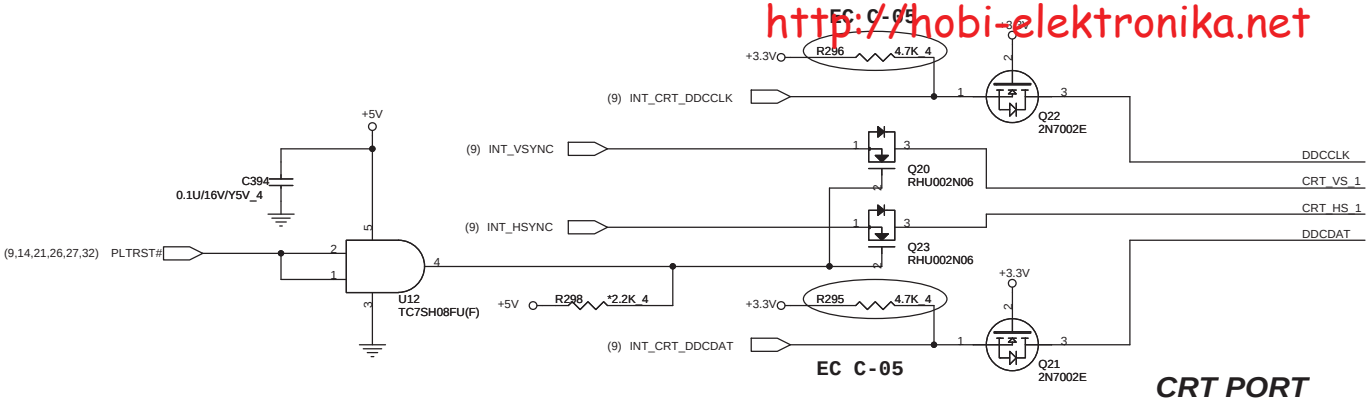


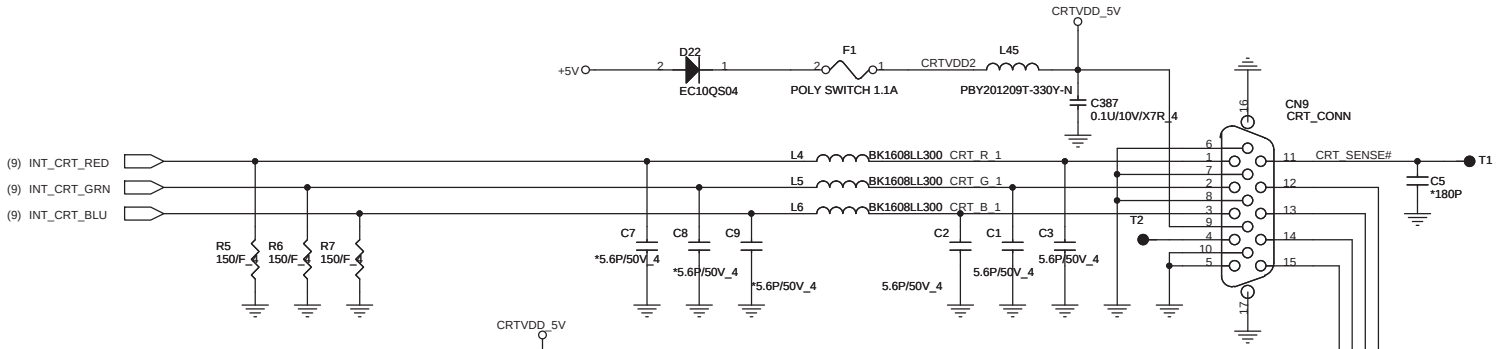
LANCELOT

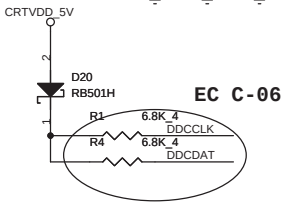
	PROJECT : SA1A Quanta Computer Inc.	
Size: Custom	Document Number: HDMI CONNECTOR	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 19 of 39	

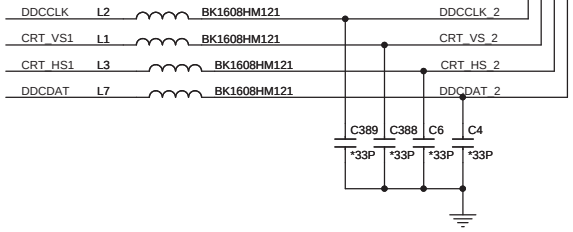
CRT PORT

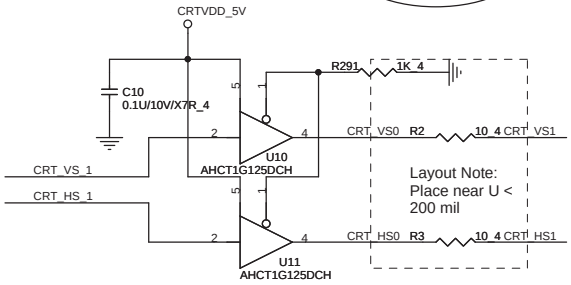
ESD PORTECTION

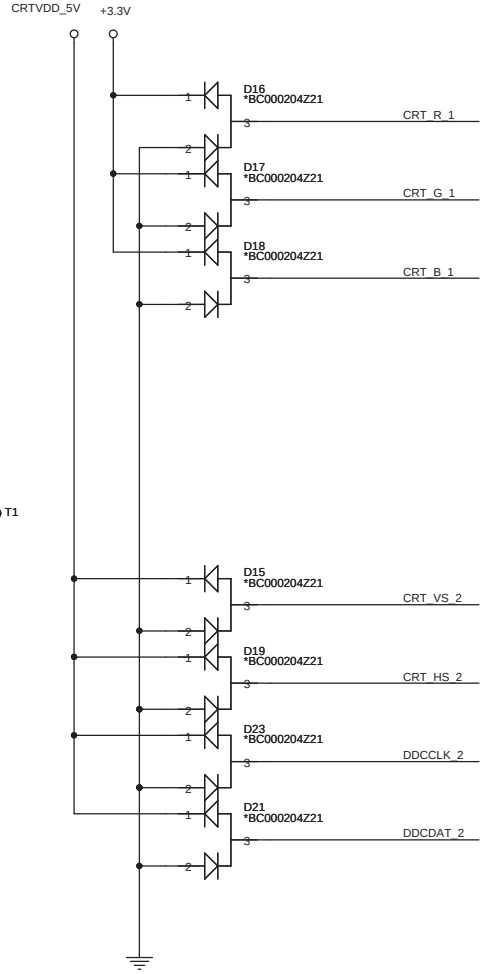






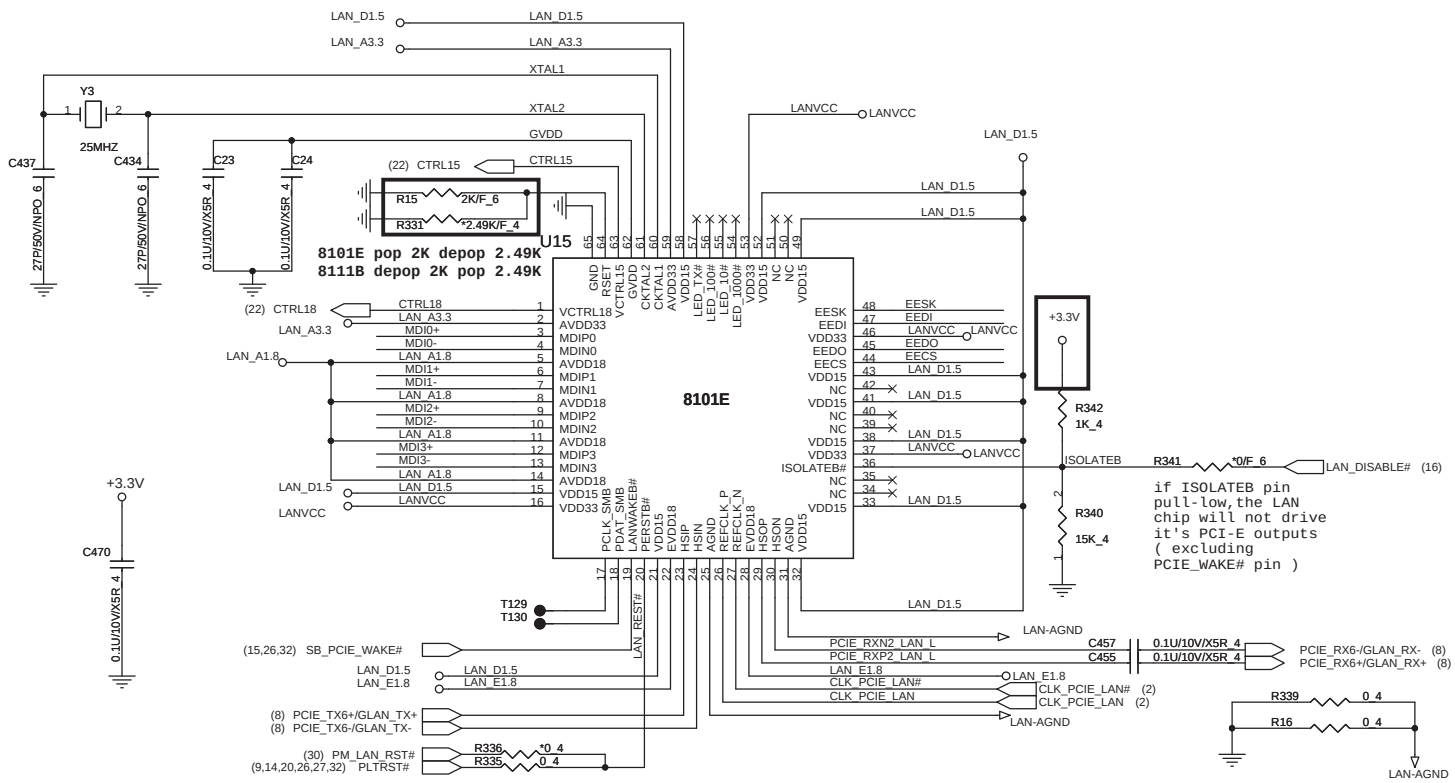




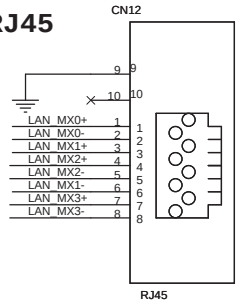


PROJECT : SA1A		
Quanta Computer Inc.		
Size: Custom	Document Number: CRT PORT	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 20 of 39	

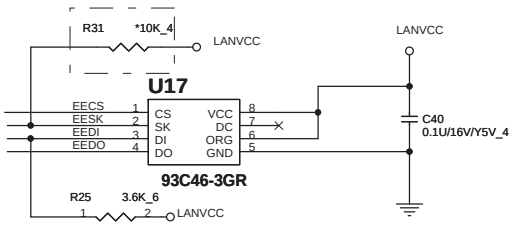
E : Stuffed for 8101E(10/100)

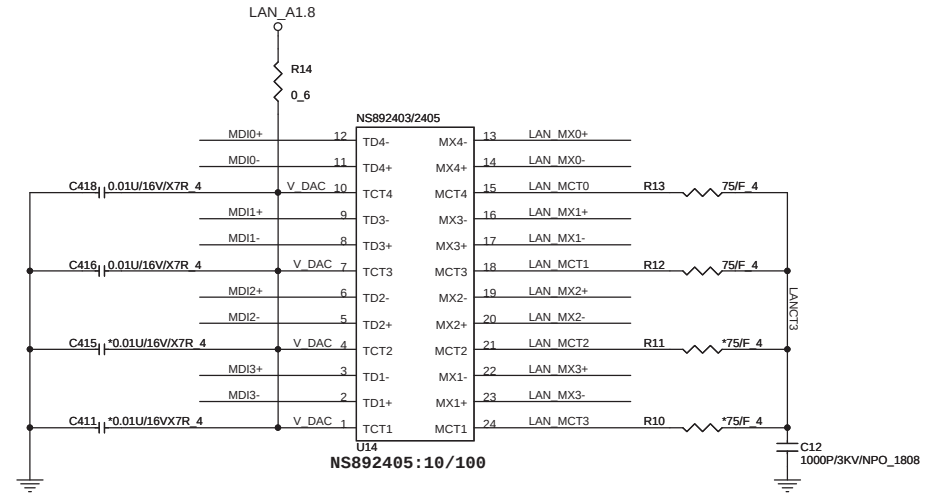


RJ45

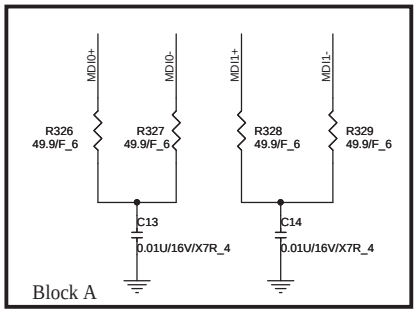


for 93C56 used. NC if 93C46 is used.





BLOCK A is only for RTL8101E application.



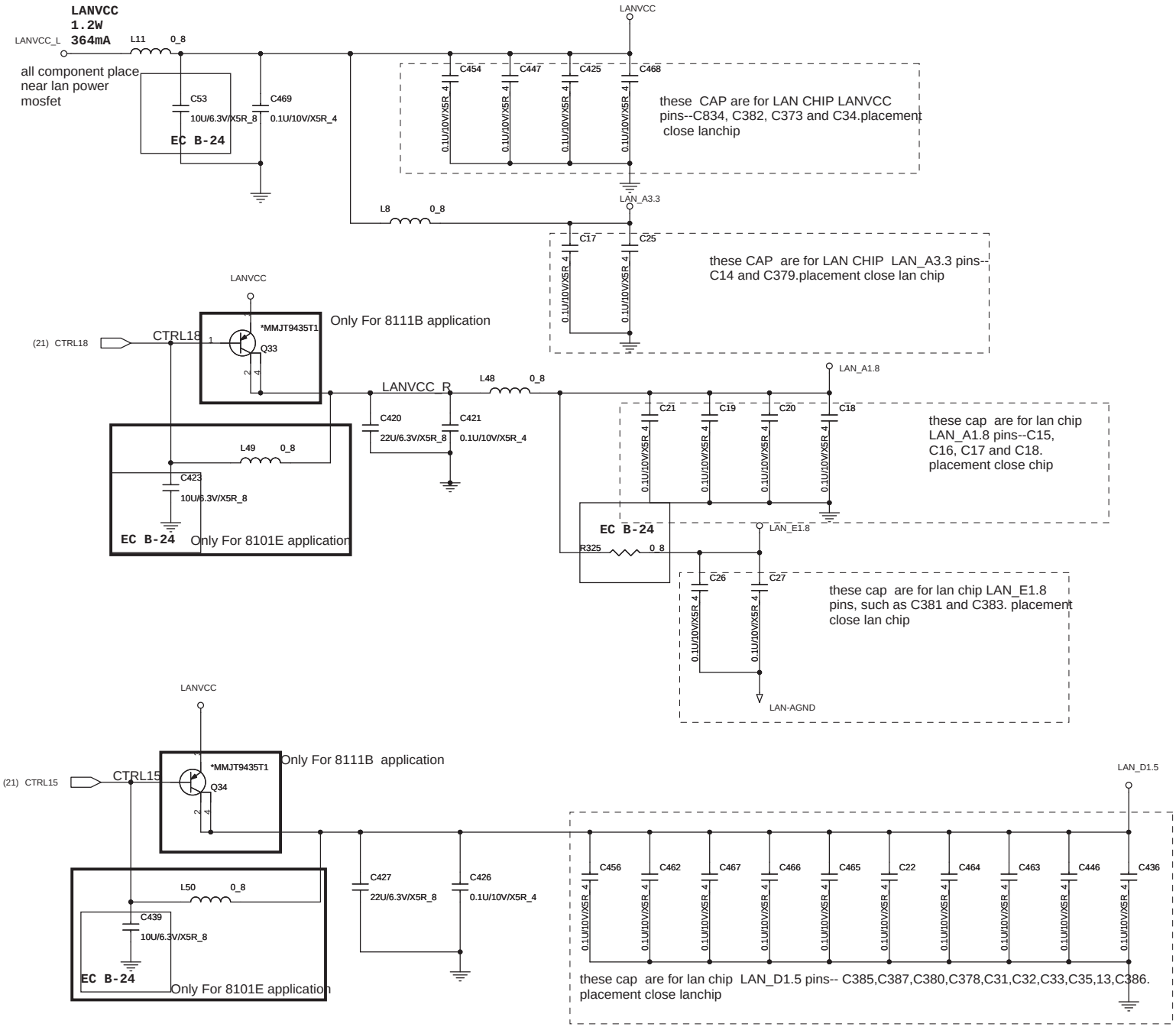
	10/100M	1G
R14 R15 R16 R17	ASM	NoASM

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN(REALTEK 8101E)	3A
Date: Thursday, January 31, 2008	Sheet 21 of 39	

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E
LANVCC	*3.3V*
LAN_D1.8	*1.8V*
LAN_A1.8	*1.8V*
LAN_D1.5	*1.5V*

	Q23	Q24
RTL8111B	*Need*	*Need*
RTL8101E	*N/A*	*N/A*

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN POWER	3A
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Note:

	SD/MMC	MS	XD
SP0			
SP1	SD_WP		XD_CD#
SP2			
SP3	SD_CD#		
SP4			XD_D4
SP5		MS_BS	XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

U9

Realtek RTS5158

A15
C-test-Change

A16
C-test-Del R230 and Add new one

A17
C-test-Del

5V to 3V3 as digital power

3.3V Power for all cards

5V to 3V3 as analog power

7 IN1 CARD-READER (PUSH-PUSH)

Support SD/MS/xD/SM/RS-MMC/MMC/miniSD Cards

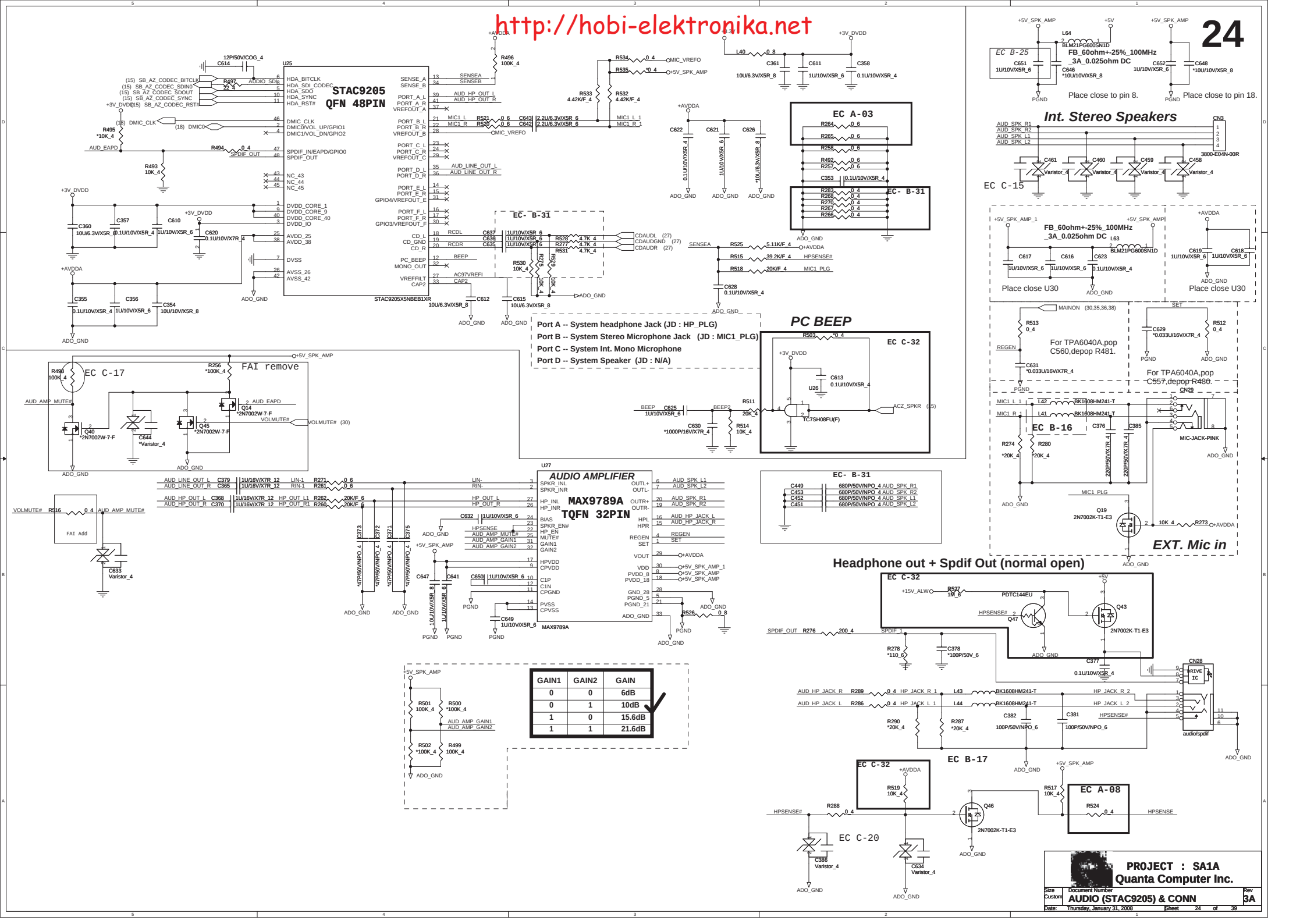
CN8

R015-212-LM

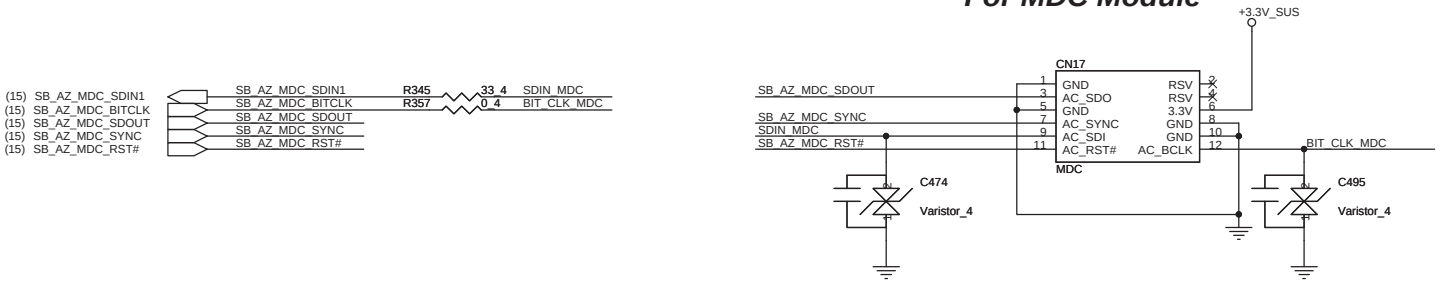
PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	REALTEK RTS5158	3A

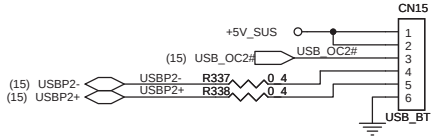
Date: Thursday, January 31, 2008 Sheet 23 of 39



For MDC Module



TO RJ11/USB PORT



	PROJECT : SA1A Quanta Computer Inc.	
Size: Custom	Document Number: MODEM(MDC)/RJ11 BOARD	Rev: 3A
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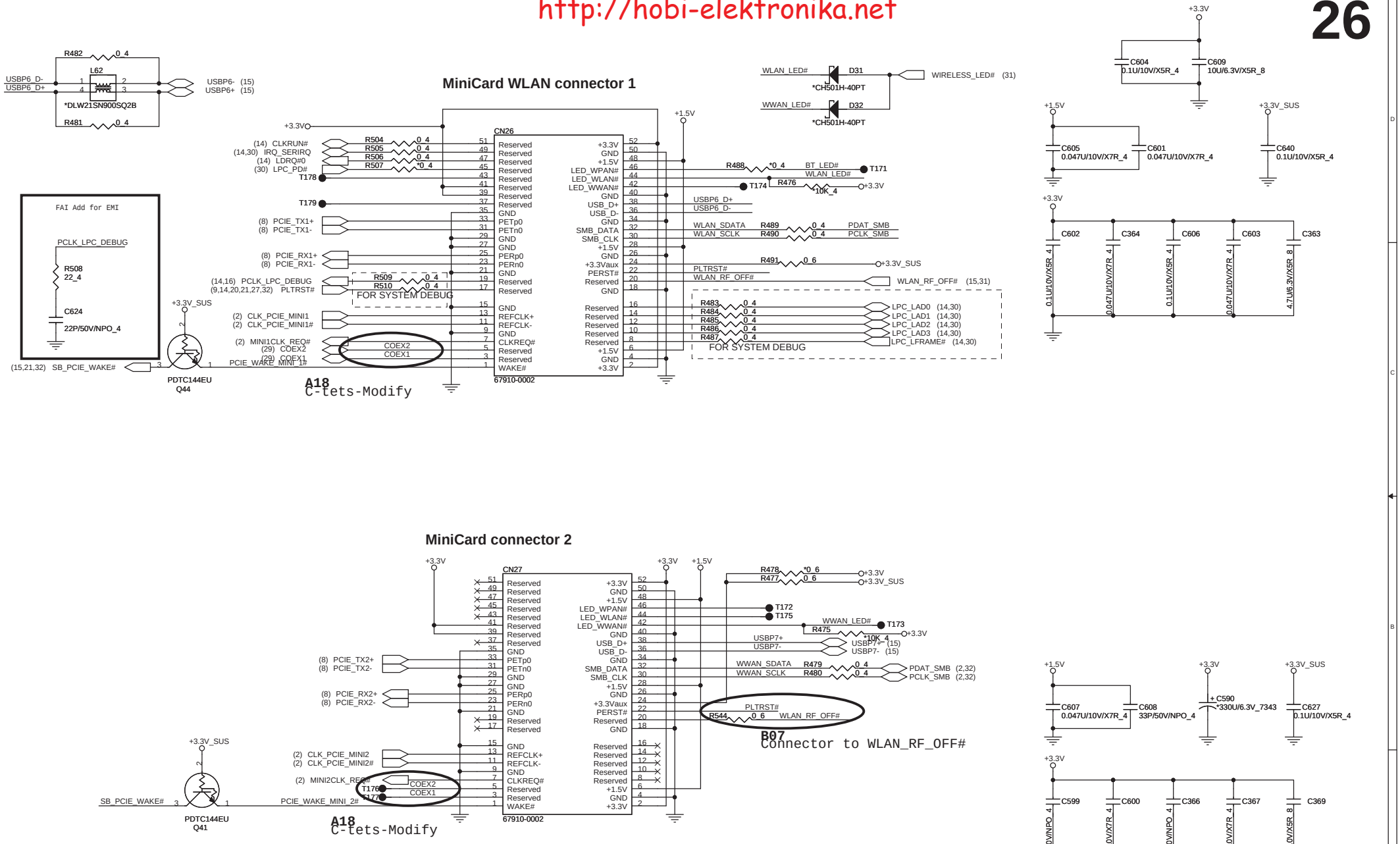
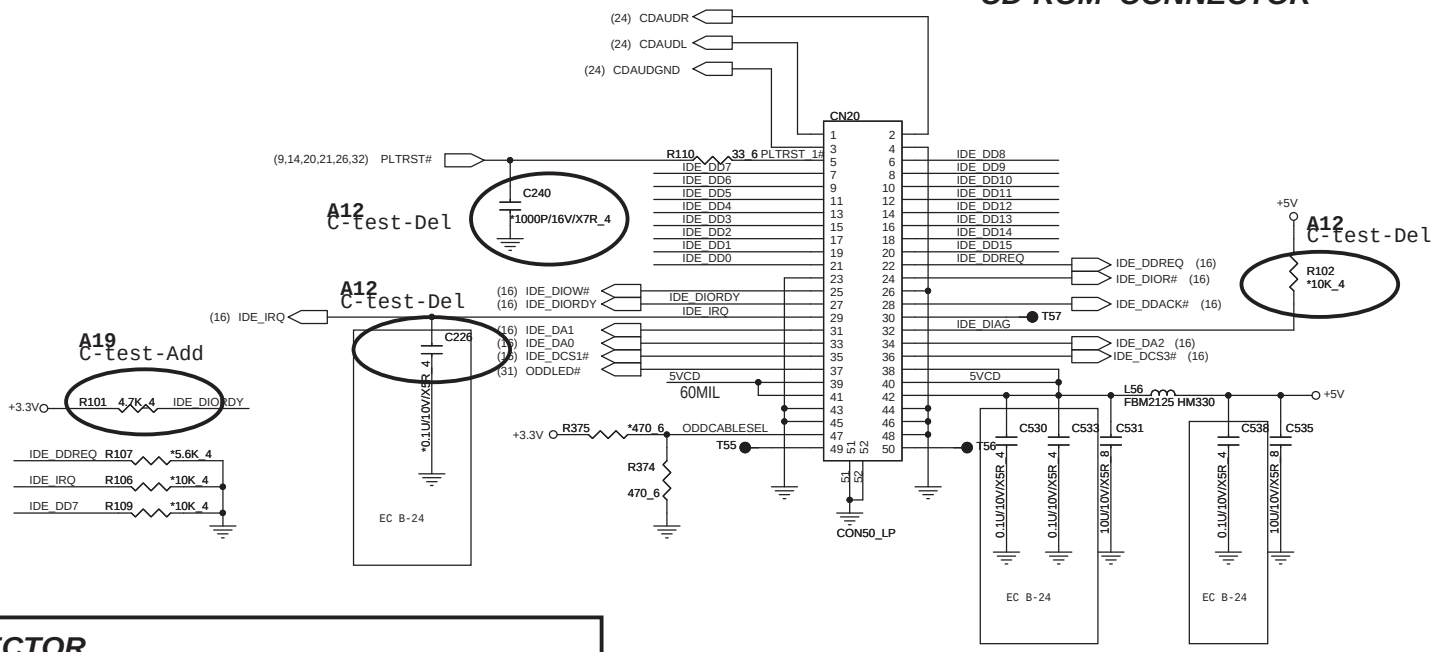


	PROJECT : SA1A Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCI-E Card	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 26 of 39	

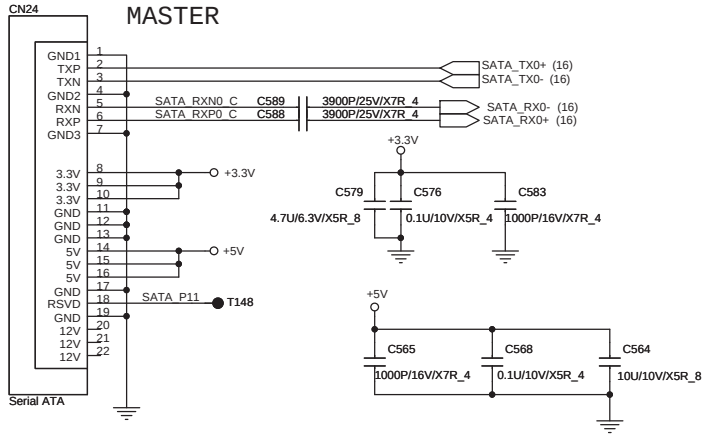
(16) IDE_DD[0..15] IDE_DD[0..15]

For fix ODD

CD-ROM CONNECTOR



SATA CONNECTOR



	PROJECT : SA1A Quanta Computer Inc.	
Size: Custom	Document Number: SATA HDD,ODD	Rev: 3A
Date: Thursday, January 31, 2008	Sheet 27 of 39	

NB SCREW HOLE

HOLE12 H-C236D142P2

HOLE17 H-C236D142P2

MINI PCI-E SCREW HOLE 2

HOLE21 H-C236D142P2

HOLE24 H-C236D142P2

MINI PCI-E SCREW HOLE 1

HOLE23 H-C236D142P2

HOLE22 H-C236D142P2

MDC SCREW HOLE

HOLE11 H-C236D142P2

HOLE7 H-TC236BS4D142P2

CPU SCREW HOLE

HOLE10 *h-ts315bs256d169p2

HOLE15 *h-ts315bs256d169p2

HOLE9 *h-ts315bs256d169p2

HOLE14 *h-ts315bs256d169p2

USB-0

60MIL

(14,18,23,25,34,37,38) +5V_SUS

+5V_SUS

U18 CM3512-04SN

VCC, OUT1, OUT2, EN1, EN2, GND, OC1, OC2

USB0PWR C476 4.7U/10V/Y5V_8

USB1PWR C494 4.7U/10V/Y5V_8

USB_OC0# (15)

USB_OC1# (15)

USB0PWR

C56 Varistor_4

C54 0.1U/10V/X5R_4

+C488 100U/6.3V/TAN_6

USBP_0-

USBP_0+

CN16 USB_CONN_straddle

C471 Clamp-Diode_4

C472 Clamp-Diode_4

EC E-33

FAI Change to 0402

USB-1

(15) USBP0-

(15) USBP0+

(15) USBP1-

(15) USBP1+

R343 0_4 USBP_0-

R344 0_4 USBP_0+

R330 0_4 USBP_1-

R334 0_4 USBP_1+

EC B-08

USB1PWR

C15 Varistor_4

C16 0.1U/10V/X5R_4

+C422 100U/6.3V/TAN_6

USBP_1-

USBP_1+

CN14 USB_CONN_straddle

C424 Clamp-Diode_4

C435 Clamp-Diode_4

EC E-33

FAI Change to 0402

EMI Use

EC A-01

+3.3V

EC33 EC62 EC50 EC9 EC7 0.1U/10V/X5R_4

EC32 EC34 EC35 EC28 0.1U/10V/X5R_4 SI Use

EC20 0.1U/10V/X5R_4

EC21 EC61 EC29 *0.1U/10V_4

EC24 EC27 0.1U/10V/X5R_4

+5V_SUS

EC17 EC19 EC66 EC18 EC48 EC51 EC60 EC58 EC57 0.1U/10V/X5R_4

EC22 0.1U/10V/X5R_4

+1.8V

EC15 EC16 EC13 0.1U/10V/X5R_4

EC59 *0.1U/10V_4

EC12 *0.1U/10V_4

VCCAN_A1.8

EC6 EC8 EC53 0.1U/10V/X5R_4

EC54 *0.1U/10V_4

EC3 *0.1U/10V_4

+PWR_SRC

EC B-30

EC63 EC4 EC56 EC55 EC46 EC45 EC52 EC5 EC64 EC10 1000P/50V/X7R_4

+3.3V_ALW

EC2 EC44 EC65 EC1 EC23 EC43 EC14 EC11 0.1U/10V/X5R_4

+15V_ALW

EC67 EC26 EC37 EC47 EC41 EC42 EC38 EC49 0.1U/25V/X5R_4

+PWR_SRC

EC B-30

EC40 EC39 EC36 EC30 EC31 1000P/50V/X7R_4

HOLE1 *h-ts4bs8d110p2

HOLE2 *h-ts8bs8d110p2

HOLE8 *h-ts1-be354x354d110p2

HOLE6 *h-ts7bs8d110p2

HOLE16 *H-TS354BC280D110P2

HOLE3 *h-c118d118n

HOLE5 *H-C98D98N

HOLE26 *H-TS314BS1D110P2

HOLE27 *h-te433bs354d110p2

HOLE25 *H-TC276BC354D110P2

HOLE4 *h-ts5bs6d110p2

HOLE13 *h-bb355x453d197x295p2

HOLE18 *h-ts2bs2d110p2

C-test-Modify

HOLE28 *H-C236D110P2

ADO_GND

HOLE20 *h-ts314bs354d119p2

HOLE19 *H-TC276TD110RB

PROJECT : SA1A

Quanta Computer Inc.

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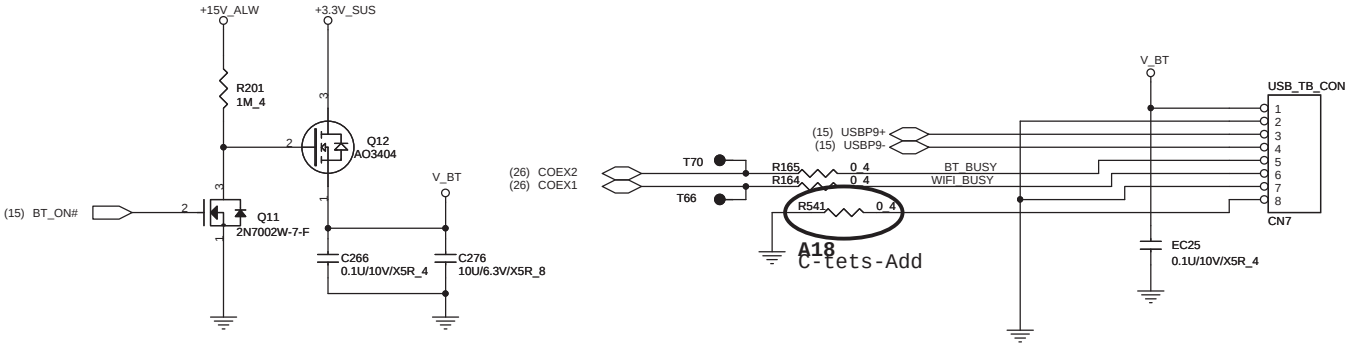
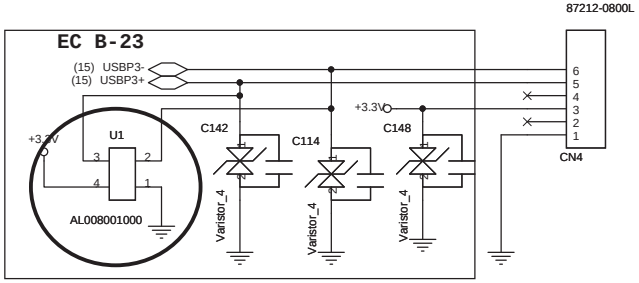
BLUETOOTH CONNECTOR



FINGERPRINT CONNECTOR



PROJECT : SA1A Quanta Computer Inc.		
Size: Custom	Document Number: BT/FG/CONNECTOR	Rev: 3A
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IT8512

POWER SWITCH

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R3444	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

(For PLL Power)

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

RF ON/OFF SLIDE SWITCH

8Mbit (1M Byte), SPI

Layout Note:
Place R428,R416,R420 within 500 mils from SPI Flash.

Please reserve this connector for serial debug port & KBS download usage.

A21
C-test-Swap

PROJECT : SA1A
Quanta Computer Inc.

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Custom	KBC-IT8502	3A
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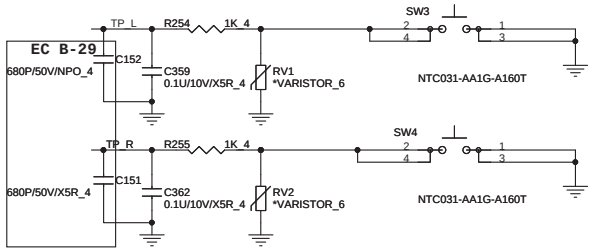
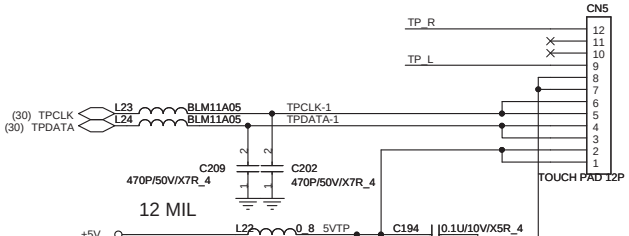
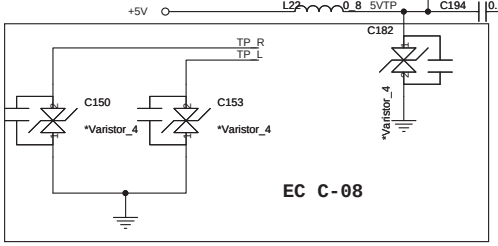
TOUCHPAD SWITCH CONN

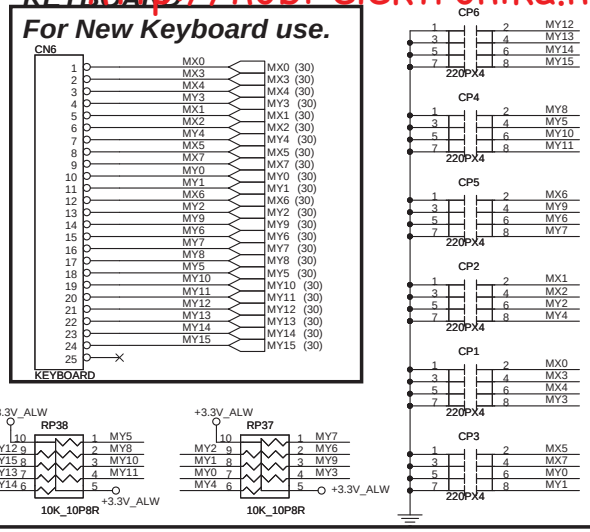




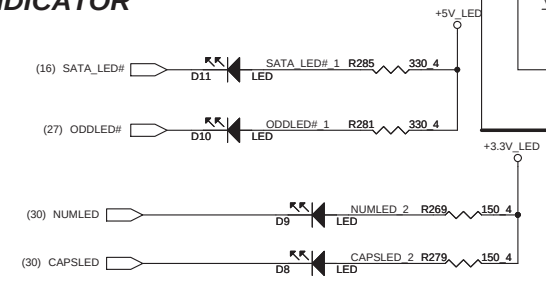


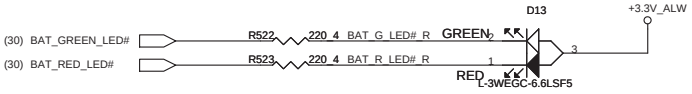
KEYBOARD

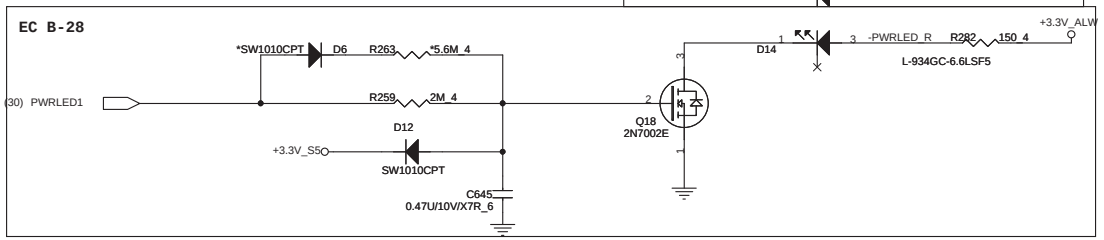
For New Keyboard use.

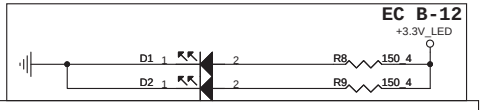


LED INDICATOR

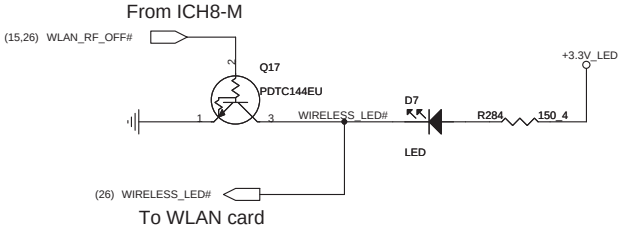


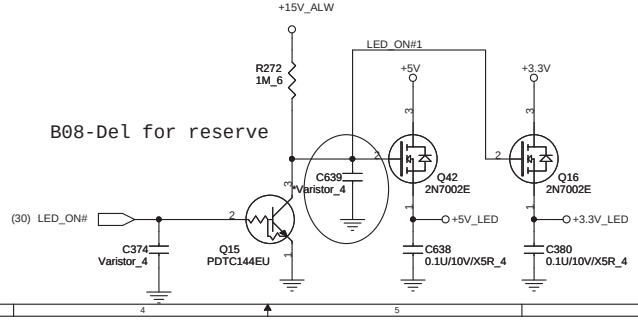


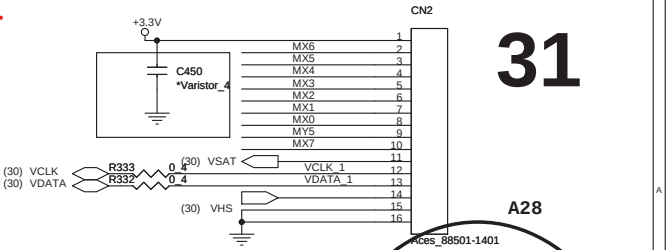


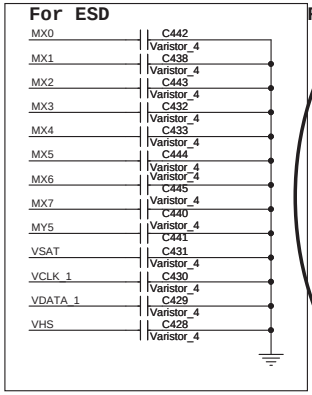


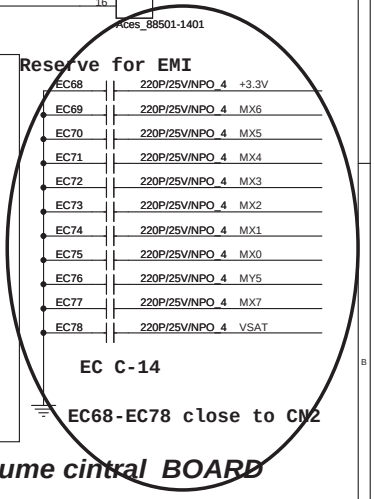
WIRELESS LED











SWITCH/Volume cintral BOARD

PROJECT : SA1A		
Quanta Computer Inc.		
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NEWCARD

(15) USBP5-
(15) USBP5+
R445 0_4
R444 0_4
USBCONP5-
USBCONP5+

+3.3V
CPUSB# R151 10K_4
CPPE# R393 *10K_4
2231_SHDN# R141 10K_4
2231_STBY# R139 10K_4

A08
C-test-Del

A08
C-test-Add

(15) NC_PWR_EN#
R538 0_4
R537 0_4
T64 *PAD
T62 *PAD
R150 *10K_4
R142 *0_4

U7
R5538
2231_STBY# 1
+3.3V_SUS 17
3VAUX 15
CP_RST# 6
CPPE# 10
CPUSB# 9
PERST# 8
2231_SHDN# 20
RCLKEN 18
OC# 19
GND 7
STBY# 2
AUXIN 4
AUXOUT
SYSRST# 12
CPPE# 14
CPUSB#
PERST# 3
SHDN# 5
RCLKEN
OC# 11
GND 13
3.3VIN
3.3VIN
1.5VIN
1.5VIN
3.3VOUT
3.3VOUT
1.5VOUT
1.5VOUT
+3.3V
+1.5V
3V_NEWCARD
1.5V_NEWCARD

1.35A need 60 mil
0.75A need 30~40 mil

A08
C-test-Change

A08
C-test-Change

1.35A need 60 mil
3V_NEWCARD

(2,26) PCLK_SMB
(2,26) PDAT_SMB
0.75A need 30~40 mil
1.5V_NEWCARD
(15,21,26) SB_PCIE_WAKE#
3VAUX
PERST#
(2) NEW-CARD_CLK_REQ#
R239 0_4
CLK_NEW_OE#
NC_PWR_EN#
(2) CLK_PCIE_NEW_C#
(2) CLK_PCIE_NEW_C
(8) PCIE_RXN3
(8) PCIE_RXP3
(8) PCIE_TXN3
(8) PCIE_TXP3

CN23
USBCONP5-
USBCONP5+
NC_PWR_EN#
GND4
USB_D-
USB_D+
CPUSB#
RESERVED2
RESERVED1
SMB_CLK
SMB_DATA
+1.5V2
+1.5V1
WAKE#
+3.3VAUX
PERST#
+3.3V2
+3.3V1
CLKREQ#
CPPE#
REFCLK-
REFCLK+
GND3
PERn0
PERp0
GND2
PETn0
PETp0
GND1
SHIELD6
SHIELD5
SHIELD4
SHIELD3
SHIELD2
SHIELD1
331-1CX43201-ZG-X2_NEW_CARD

+3.3V_SUS
C239
0.1U/10V/X5R_4
(9,14,20,21,26,27) PLTRST#
CP_RST#
U5
TC7SH08FU(F)

3V_NEWCARD
3VAUX
1.5V_NEWCARD
C237 0.1U/10V/X5R_4
C238 0.1U/10V/X5R_4
C253 0.1U/10V/X5R_4
C252 0.1U/10V/X5R_4
C251 0.1U/10V/X5R_4
C250 0.1U/10V/X5R_4

EC B-24

PROJECT : SA1A
Quanta Computer Inc.

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BATTERY CHARGER

A24
10/29 Change to 65W

C1
12/28 Change footprint to
DCJK-2DC-G213X200-V-SA7

TOP DC_JACK 65W
CN10 DC-JACK 65W-BLK
HI0805R800R/5A_8 PL2
HI0805R800R/5A_8 PL3
PC59 .1U/50V/X7R_6
PC58 .1U/50V/X7R_6
PD7 PDS1040-13
A25 C-Test
PD14 PASMAJ20A
EC C-09
PR96 RL3720WT-R020
R1
CSIP 1P
CSIN 2P
PR1 *0_4
PR2 *200K/F_6
PR3 *200K/F_6
PC1 *0.1U/50V/X7R_6
PR4 *0_4
PQ2 *IMD2
D/C#
PR97 *0_4
PC60 1U/25V/X7R_8
PQ24 SUD45P03-15
PC2 0.1U/50V/X7R_6
PQ1 DTA124EU
PR98 10K/F_6
ACOK_IN
PQ3 *2N7002K-T1-E3
PR11 *33.2K/F_6
PR5 *10K/F_6
PR10 *0_4
+PWR_SRC
PR12 200K/F_6
PR6 100K/F_6
PQ25 SI4425BDY-T1-E3
Place close to EC,
PL5 HI0805R800R/5A_8
PL4 HI0805R800R/5A_8
BAT_CONN
BATT+
CN13
PR173 100K/F_6
MBATV
PR172 14K/F_6
PC129 0.01U/50V/X7R_6
PR9 330/F_4
PR8 330/F_4
SMC
SMD
+3.3V_ALW
PR7 10K/F_4
PC3 .01U/16V/X7R_4
TEMP_MBAT (30)
MBDATA (30)
MBCLK (30)
PD2 UDZS5.6BTE-17
PD1 UDZS5.6BTE-17
C1
PR128 2_6
PR124 20_6
CSIP_1
CSIN_1
PC82 .1U/50V/X7R_6
ISL6251_VDD
PC78 1U/6.3V/X5R_4
PR107 4.7_6
ISL6251_VDDP
PC88 4.7U/6.3V/X5R_6
CH501H-40PT
PD11
Place these CAPs close to FETs
+PWR_SRC
B09-ADD-EMI
PC73 1N/50V/X7R_4
PC72 .1U/50V/X7R_6
PC67 10U/25V/X6S_12
PC68 10U/25V/X6S_12
R546 2.2_8
C653 1500P/50V/X7R_4
PQ33 Si4800BDY
PR117 20_6
PR113 20_6
PC81 0.047U/10V/X5R_4
A25 C-Test
PR146 0_6
PC91 .1U/50V/X7R_6
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE
PL6 SIL104R-100PF/10UH/4.4A
6251LR
R2
PR104 RL3720WT-R020
BAT+
PC74 10U/25V/X6S_12
PC75 10U/25V/X6S_12
PC76 .01U/50V/X7R_4
PR23 2.2_8
PC16 1500P/50V/X7R_4
PQ32 Si4800BDY
CSOP
CSON
CSOP 1 21
CSON 1 22
CSOP
CSON
ACOK#
DCIN
6251ACIN
ACSET
EN
ACPRN
DCIN
BOOT
UGATE
PHASE
LGATE
PGND
GND
VADJ
ACLIM
CELLS
ICOMP
VCOMP
ICM
VREFE
CHLIM
CSIP
CSIN
VDD
VDDP
A25 C-Test
PD9 SW1010CPT
PR106 10_6
PC79 1U/25V/X5R_8
PR110 100K/F_4
PR108 12.4K/F_4
Setting the Vin min to 12V For ACSET 1.26V
PR112 150K/F_4
PR115 10K/F_4
Setting the Vin min to 17V For EN = 1.06V
6251EN
A23
PR143 178K/F_4 Rhigh
PR144 *100K/F_4
PR142 29.4K/F_4 Rlow
PR145 *100K/F_4
VADJ =
VERF >> 4.2V +5%
Float >> 4.2V
GND >> 4.2 -5%
6251VREF
VADJ
ACLIM
PU5 ISL6251A
A25 C-Test
PC84 6800P/25V/X7R_4
6251VREF
VREF = 2.39V
PR139 0_4
CC_SET (30)
V ACLIM = VREF * (Rlow // 152K) / (Rhigh // 152K + Rlow// 152K)
Iin_max = (1/R1)((0.05/Vref) * Vaclim + 0.05)
PC21 100P/50V/X7R_4
PR140 *100K/F_4
Charging Curret setting =>
I chg = 165mV / R2 * (Vchlim / 3.3V)
PR130 10K/F_4
PR136 100/F_4
SYS_I
PC89 3300P/50V/X7R_4
Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)
PC19 100P/50V/X7R_4
PC86 0.1U/16V/X7R_4
ACOK
PR34 100K/F_4
PQ6 2N7002K-T1-E3
PD4 SW1010CPT
A22 C-Test
A22 Ramp-PC18-Del
PC15 *1U/25V/X5R_6
PC18 *1N/50V/X7R_4
PR28 475K/F_6
PR36 10K/F_4
PQ7 2N7002K-T1-E3
D/C# (30)
+5V_ALW
PU2 G1331
PD3 SW1010CPT
PR27 332K/F_6
PC17 *1N/50V/X7R_4
PR35 10K/F_4
PR37 *0_4
PQ4 CH2507SPT
Battery Low 7.5V
BL/C# (30)
A22 Ramp-PC17-Del
ACOK
ISL6251_VDD
PR122 10K/F_4
PQ34 DTA124EU
(30) ACIN
PR127 15K/F_4
6251ACIN
PC83 1U/25V/X5R_8
ACOK#
CH2507SPT PQ36
PD10 SW1010CPT
PR138 1M_4
PR123 100K/F_4
PR118 100K/F_4
6251CELLS_1
A25 C-Test
EC C-10
(30) CELL_SLT
CH2507SPT PQ5
CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

ADP TYPE	PR143	P/N
65W	178K/F_4	CS41782FB11
90W	11K/F_4	CS31102FB11

A22 Ramp-PQ4 P/N Change to PQ7

PROJECT : SA1A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER	3A
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TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

+5Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A

Vout=0.7(Ra+Rb)/Rb

Rb around 49.9k

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

Place these CAPs close to FETs

A25 Del 10/29

A25 C-Test

+3.3Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A

C3 Change Part for SMT

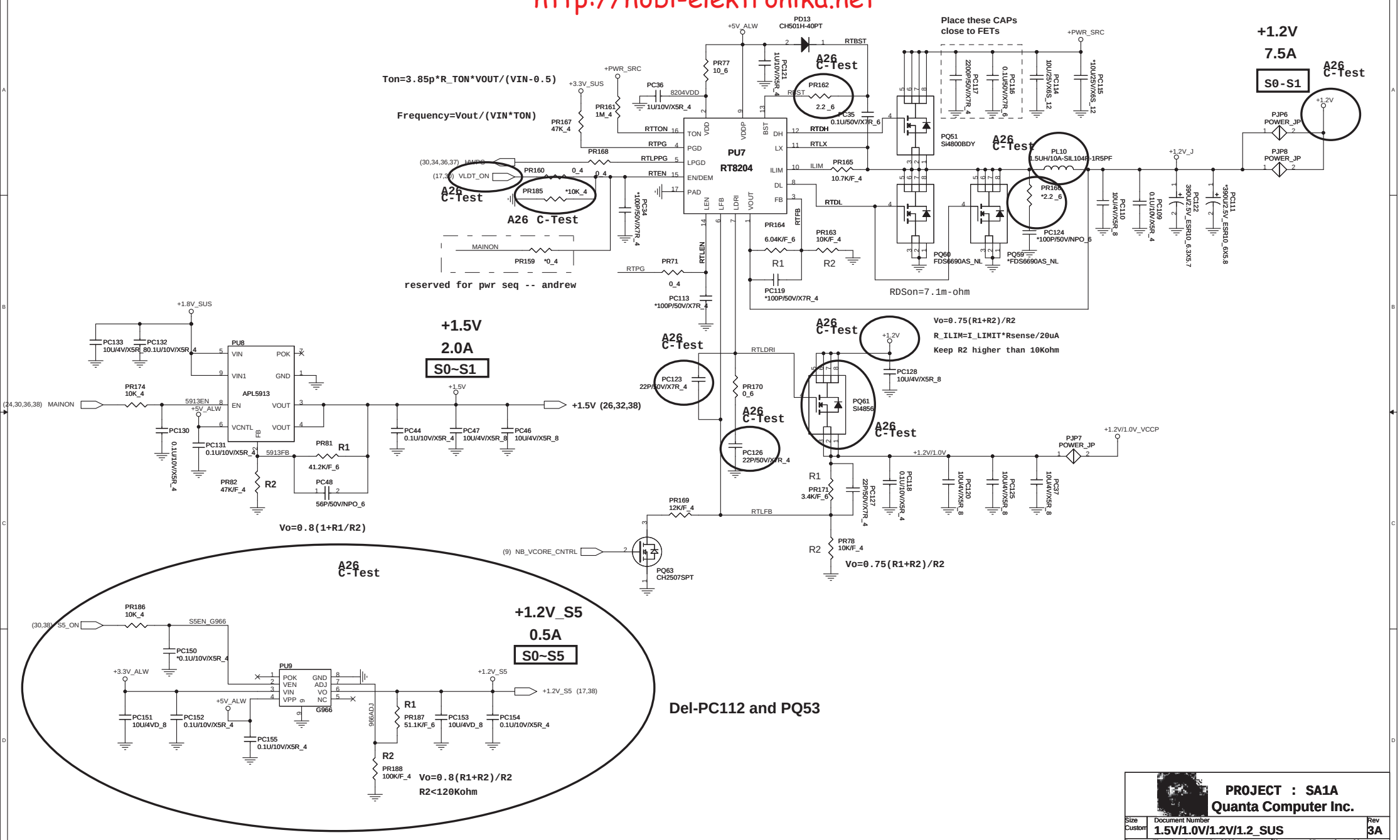
Rds(on) 15m ohm

+5V 5A S0-S1

+5VSUS 4A S0-S3

+3V 5.76A S0-S1

PROJECT :	SA1A
Quanta Computer Inc.	
Size: Custom	Document Number: 3V/5V/10V /15V
Rev:	3A
Date: Thursday, January 31, 2008	Sheet 34 of 39



PROJECT : SA1A			
Quanta Computer Inc.			
Size: Custom	Document Number: 1.5V/1.0V/1.2V/1.2_SUS		Rev: 3A
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+1.8VSUS
18A
S0~S3

+PWR_SRC
PC61 100U/25V_6.3X7.7
PC94 100U/25V_6.3X7.7
PC25 *10U/25V/X6S_12
PC102 10U/25V/X6S_12

Place these CAPs close to FETs
PC100 0.1U/50V/X7R_6
PC101 2200P/50V/X7R_4

Ra=(Vout-0.75)/0.75*Rb
Rb value from 100K to 300K ohm

+1.8V_SUS
PJP3 POWER_JP
PJP4 POWER_JP
PJP5 POWER_JP
+1.8V_SUS_J
PC106 390U/2.5V_ESR10_6.3X5.7
PC105 390U/2.5V_ESR10_6.3X5.7
PC107 0.1U/10V/X5R_4
PC96 *100P/50V/X7R_4

PL9 MPO104-1R5/1.5U/20A
PR46 *2.2_8
PC26 *100P/50V/NPO_6

PQ40 SI7686DP
PQ41 SI7636DP
PQ8 *SI7636DP

A25 C-Test
Ra
PR150 *2K/F_4
PR152 0_4
Rb
PR39 *10K/F_4
PR154 *0_4
PR24 *0_4
VDDIO_FB_H (5)
Differential Pair
VDDIO_FB_L (5)

Fix 1.8V Output
PR40 0_4
51116_V5FILT

Rds(on) 7.25m ohm

I_lim(Valley)=10uA*R_ILIM/RDS_ON
For OCP set.

+5V_ALW
PR156 10_6
51116_V5FILT
PC98 2.2U/6.3V/X5R_6
PC104 0.1U/50V/X7R_6 2.2_6
PR157 51116_BST
PC22 1U/10V/X5R_4
+3.3V_SUS
PR38 *10K_4
PR43 7.15K/F_6
PR153 0_4
HWPG (30,34,35,37)

PU6 TI51116
VBST V5IN V5FILT CS PGOOD DRVH LL DRVL S5 S3 VLDOIN VTTGND MODE VDDQSNS VDDQSET VTT VTTSNS COMP NC NC PGND PAD GND VTTREF CS_GND

1.8V_DH 1.8V_LX 1.8V_DL 1.8V_OUT 1.8V_FB COMP

S5SON PR149 0_4 SUSON (30,38)
S3SON PR151 0_4
+1.8V_SUS_J
PC103 1U/10V/X5R_4
PC99 10U/4V/X5R_8
PC24 10U/4V/X5R_8
+0.9V_DDR_VTT
+0.9V_DDR_VTT (4,6,11,13,38)
VTTSNS PR45 0_4
PR42 *0_4
CPU_VTT_SENSE (4)
MODE PR44 0_4 +1.8V_SUS_J
PR41 0_4
SMDDR_VREF
PR155 0_6
PC97 0.033U/25V/X7R_6

+0.9V
1.53A
S0~S3

+2.5V
0.25A
S0~S1

Close to CPU
SI power

PU3 G913C
(24,30,35,38) MAINON
PR51 10K_4
+3.3V_ALW
PC30 0.1U/10V/X5R_4
PC29 1U/10V/X5R_4
SHDN VOUT VIN GND SET
+2.5V
R1 PR56 100K/F_4
PC32 4.7U/6.3V/X5R_6
R2 PR57 100K/F_4
Vout=1.25(1+R1/R2)

+1.8V_SUS
(11,34,38) MAIND
PQ35 SI4856

+1.8V
6A
S0~S1

+1.8V
+1.8V (5,9,10,11,14,17,28,38)
PC80 10U/4V/X5R_8
PC156 10U/4V/X5R_8

A25 C-Test

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Custom	1.8V_SUS/1.8V/2.5V	3A
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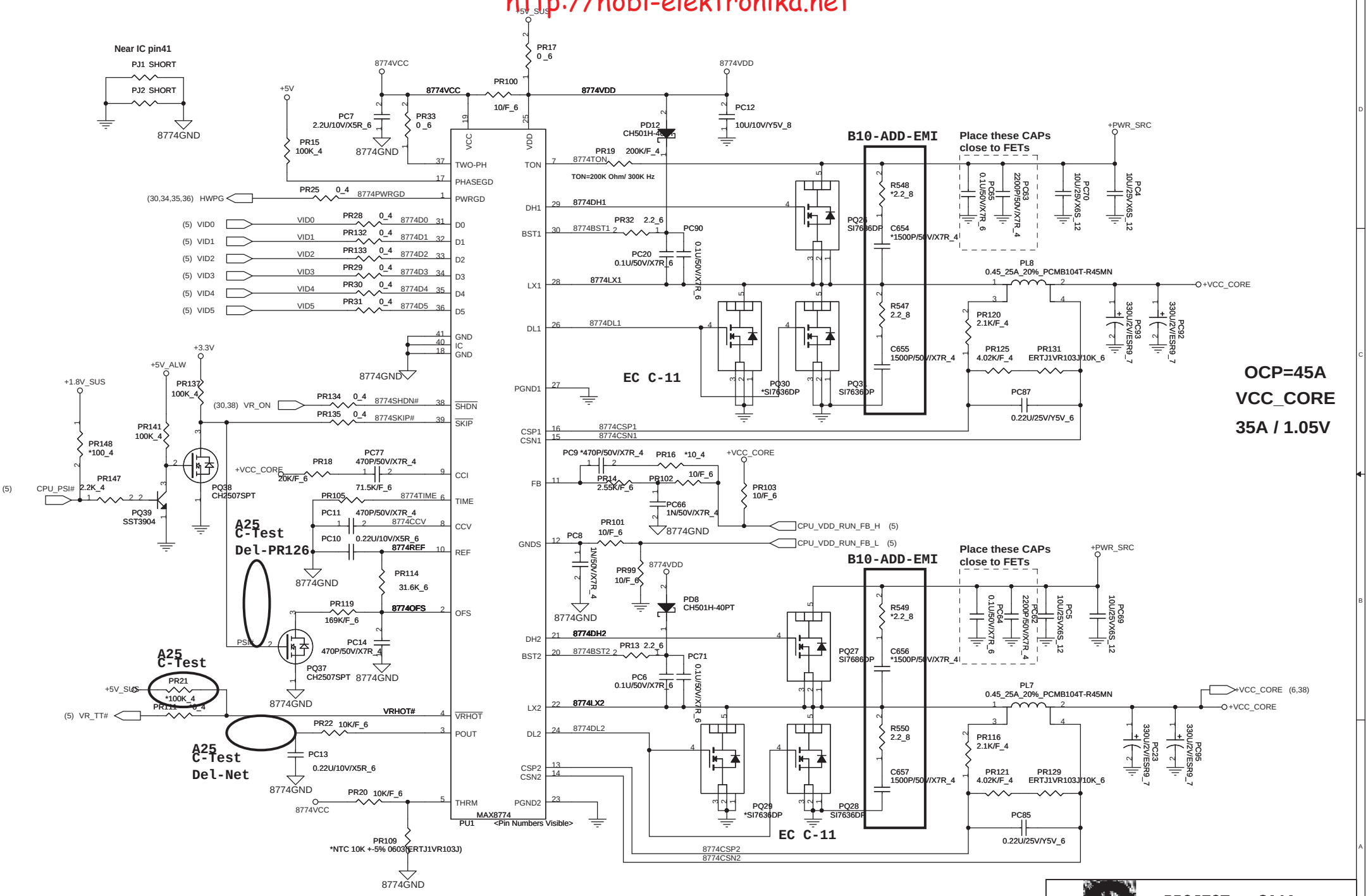

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Quanta Computer Inc.		
Size: Custom	Document Number: CPU VCC CORE	Rev: 3A
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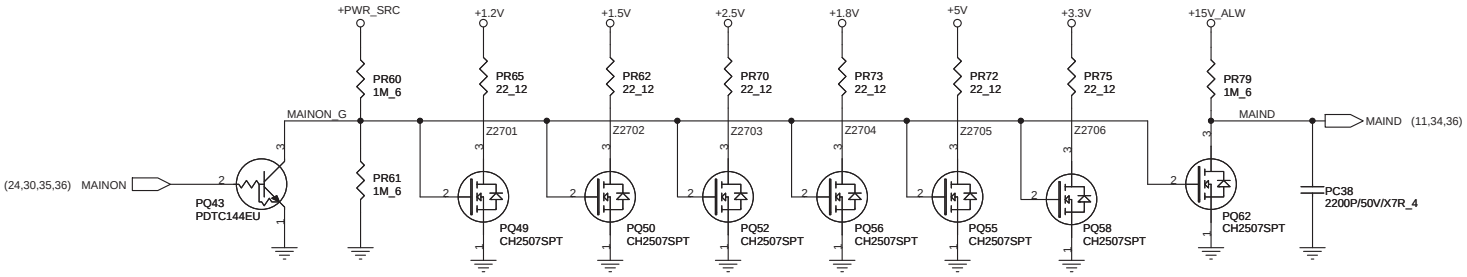
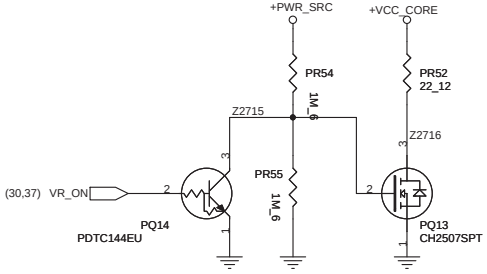
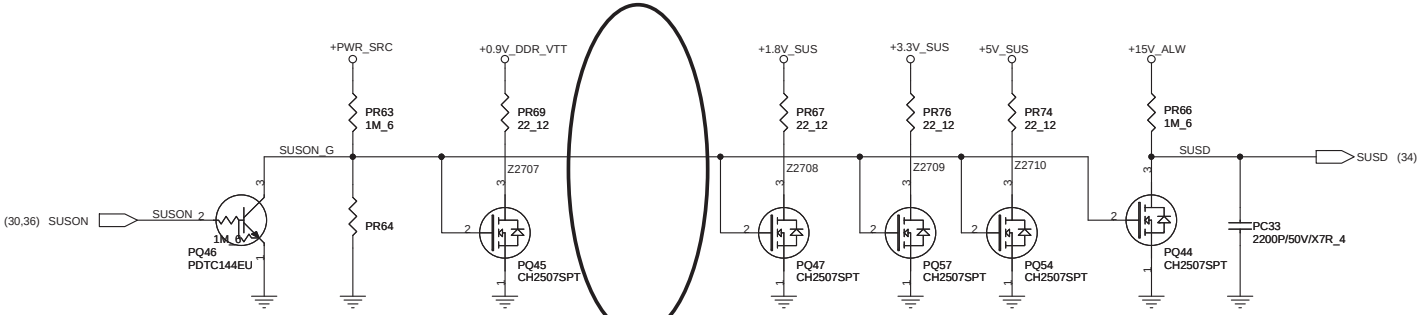
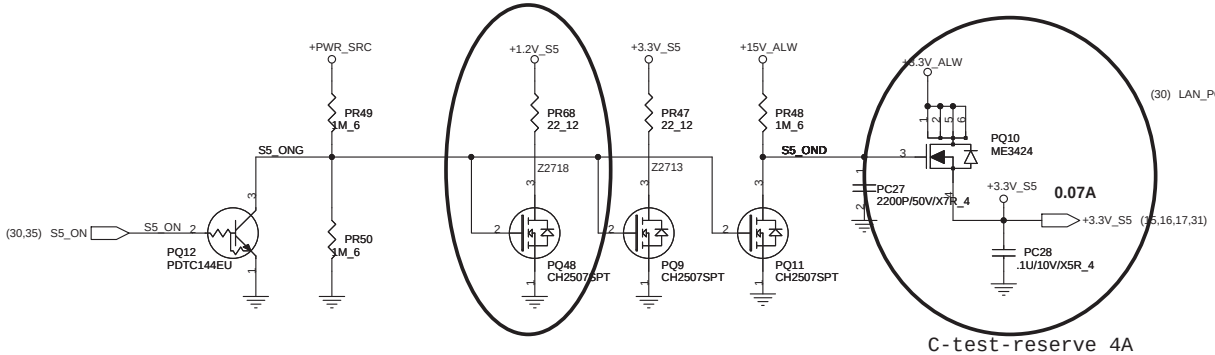


C-test-Del +1.2V_SUS

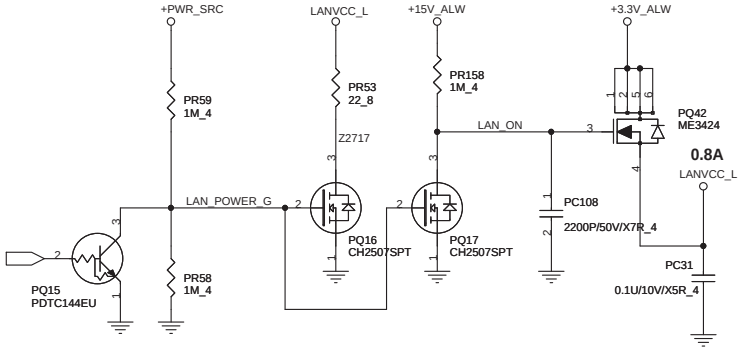




A27
C-test-Add +1.2V_S5



C-test-reserve 4A



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A01. For EMI reserve but no stuff.
A02. Reference AMD demo circuit don`t add capacitor.
A03. ADM suggest by pass directly, for single core and dure core start-up issue.
A04. ADM suggest by pass HDMI_DET directly for TMDS directly.
A05. Change CN22 Pin connection.
A06. Change Power rail.
A07. Change KBSMI# to new GPIO for S/W request.
A08. Add New-Card power controll Pin.
A09. Modify STRAP Pin setting.
A10. Solve Start-up "FF" issue.
A11. Change Power rail.
A12. Use +15V let Q10 turn-on fully.
A13. Base on AMD suggest and Demo circuit don`t connection those parts.
A14. AMD suggest use 60 Ohm Res , so we use 120//120=60 Ohm.
A15. Modify by Realtek suggestion for power saving.
A16. Change Power soucer by Realtek suggestion.
A17. Del capacitor by Realtek suggestion for signal loading capacitor.
A18. Modify Pin define for common design.
A19. Solve some ODD can't detection issue.
A20. Change ESD component P/N.
A21. Change EC net to correct function.
A22. Del PC17, PC18 and change PR35 ,PR36 to slove battery learnning can`t discharge issue.
A23. Change Resistor 65W charge setting.
A24. Modify P/N for common design.
A25. Change by Power for fine tune some part's volume or footprint.
A26. Change power circuit for power budget and slove leakge issue.
A27. Change Power rail.
A28. For EMI reserve.

B-01 / Page 2 / Add Cap for AMD suggestion.
B-02 / Page 9 / USB performance
B-03 / Page 9 / Change Value for AMD suggestion to PASS HDMI test.
B-04 / Page 16 / Requirement from AMD.
B-05 / Page 18 / Change value to solve HDMI issue.
B-06 / Page 19 / Change to FDV301N to solve HDMI issue.
B-07 / Page 26 / Connector to WLAN_RF_OFF#.
B-08 / Page 31 / Delete.
B-09 / Page 33 / Add for EMI suggestion.
B-10 / Page 37 / Add for EMI suggestion.
B-11 / Page 2 / Reserve for EMI suggestion.

EC C-01 / Page 5,10 / ADD EMI solution
EC C-02 / Page 5 / The PWM output do not need a series 100K and a 0.1u cap. So R378 change to 0 ohm , C534 remove Cap.
EC C-03 / Page 9,14,15 / Insert 10K resistor for ESD.
EC C-04 / Page 14 / Change to non-insert.
EC C-05 / Page 20 / Change Resistor from 2.2K to 4.7K.
EC C-06 / Page 20 / Change Resistor from 2.2K to 6.8K.
EC C-07 / Page 20 / Change to non-insert.
EC C-08 / Page 31 / Change to non-insert for ESD.
EC C-09 / Page 33 / Add PD14 for Power plug issue.
EC C-10 / Page 33 / Insert 100K for Battery charger issue.
EC C-11 / Page 37 / PQ29 Change TO PQ28 , PQ30 Change TO PQ31 for EMI.
EC C-12 / Page 19 / Base on AMD requirement we will change R539 to CX8PG330007 , Change R540 to non-insert.(Change FAI stage).
EC C-13 / Page 09 / Insert 100K for HDMI hot plug issue(Change FAI stage).
EC C-14 / Page 31 / Change Capacitor from 0.1U to 220P for EMI(Change FAI stage).
EC C-15 / Page 24 / C461,C460,C459,C458 change to ASM(Change FAI stage).
EC C-16 / Page 14 / R391 change to ASM(Change FAI stage).
EC C-17 / Page 24 / R498 change to ASM(Change FAI stage).

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