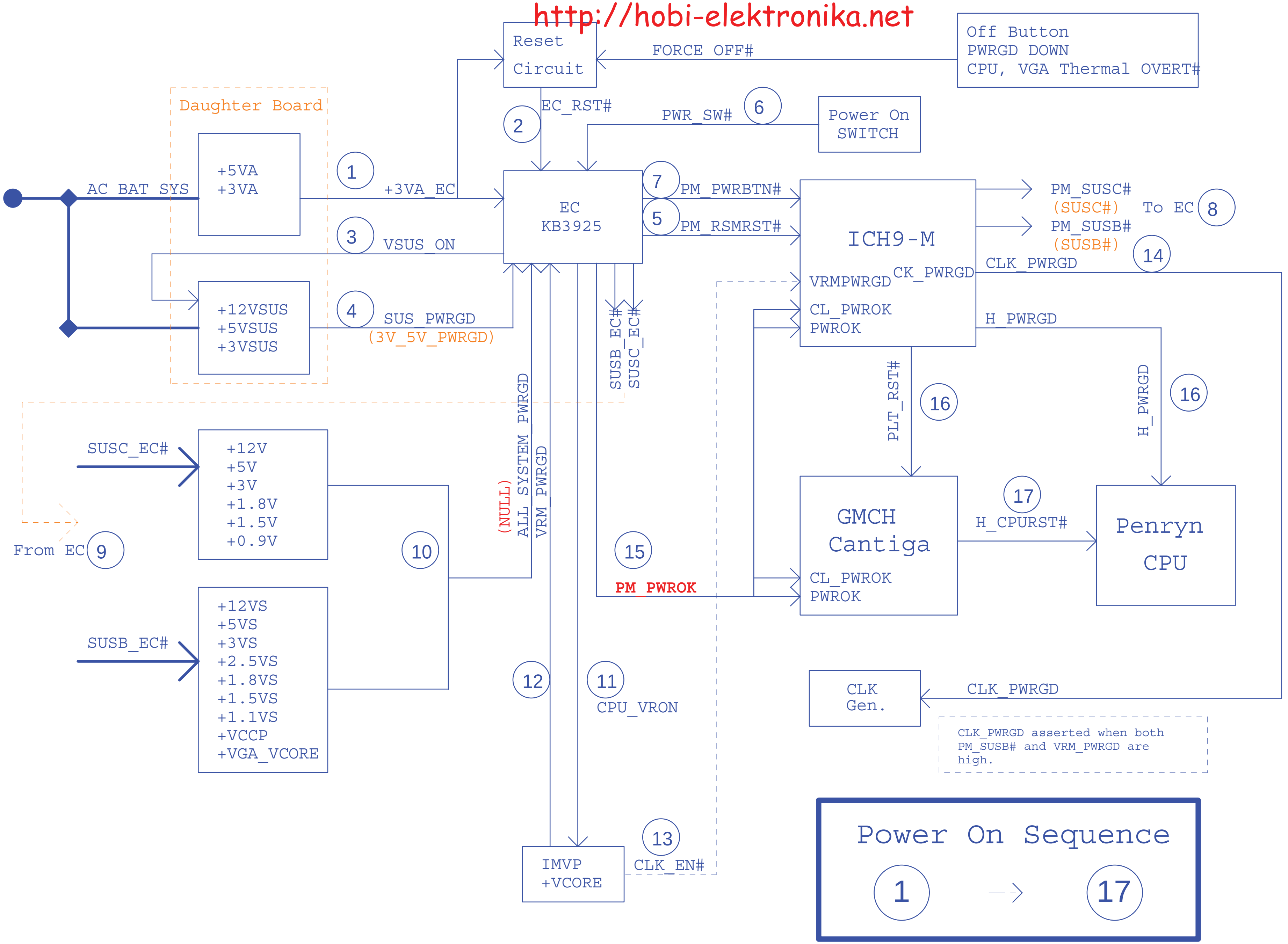
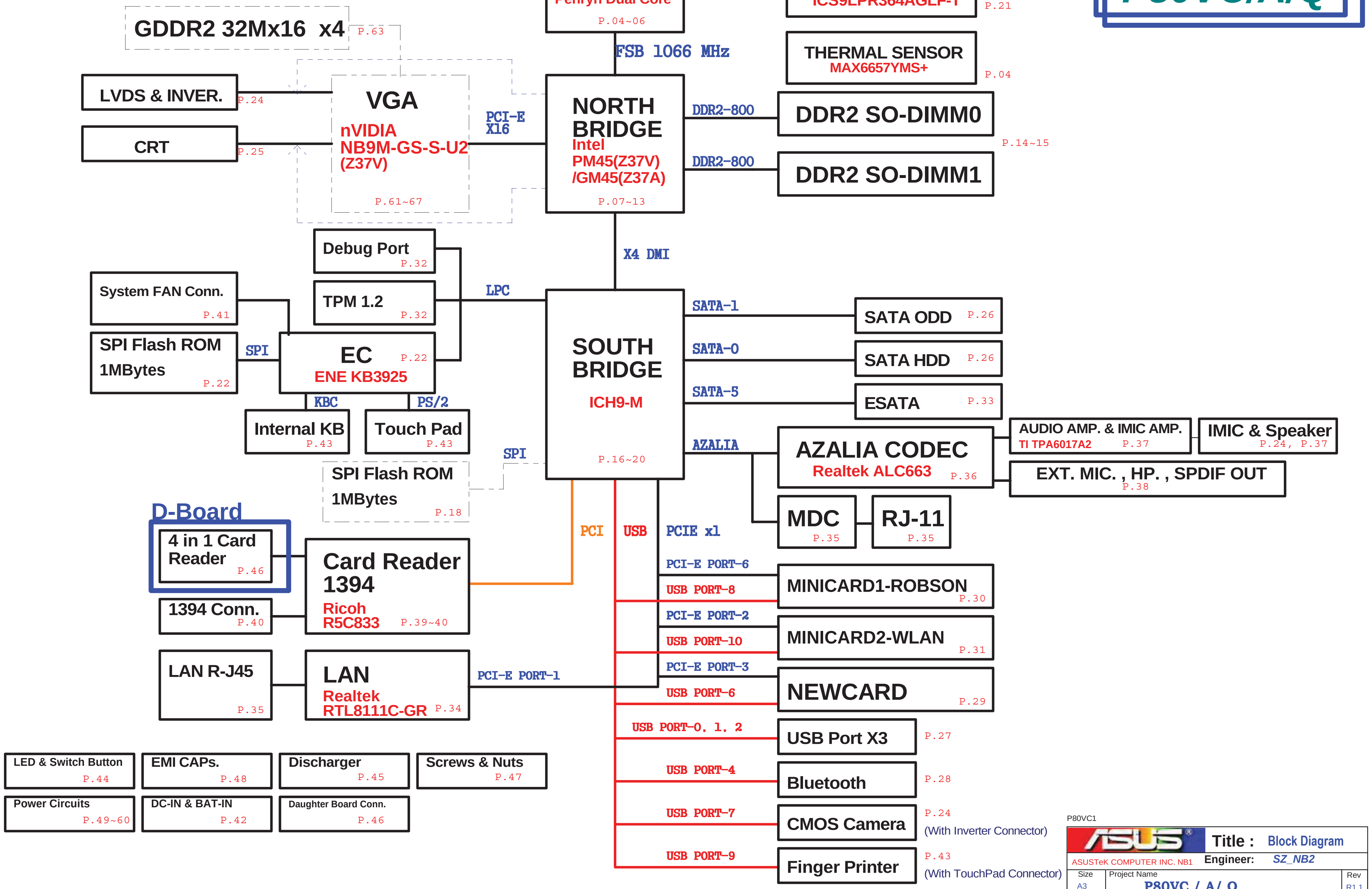


P80VC1

ASUS	Title : Power-On Sequence	
ASUSTeK COMPUTER INC. NB1	Engineer: SZ_NB2	
Size A3	Project Name P80VC / A/ Q	Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 1 of 52	

P80VC/A/Q



P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Block Diagram		
	Engineer: SZ_NB2		
Size A3	Project Name P80VC / A/ Q		Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 2	of 52	

Z37V/A Schematic Index

INT PU*: PU or PD in special time

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	Native	PMSYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]# EXT PU to +3VS	+5VS
GPIO 06	GPI	**WLBT_SW#** EXT PU	+3VS
GPIO 07	GPI	-	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN EXT PD	+3VSUS
GPIO 10	GPI	**RTLAN_DSM#** EXT PU	+3VSUS
GPIO 11	Native	SMBALERT# EXT PU	+3VSUS
GPIO 12	GPI	EXT_SCI# EXT PU	+3VSUS
GPIO 13	GPI	-	+3VSUS
GPIO 14	Native	AC_PRESENT EXT PU	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD*	+3VS
GPIO 17	GPI	-	+3VS
GPIO 18	GPO	**GPU_PWR_SB** EXT PU NS	+3VS
GPIO 19	GPO	BT_LED EXT PU NS	+3VS
GPIO 20	GPO	**GPU_RST_SB#** EXT PU NS	+3VS
GPIO 21	GPO	WLAN_LED EXT PU NS	+3VS
GPIO 22	GPI	**ODC#** EXT PU	+3VS
GPIO 23	Native	LPC_LDRQ1# INT PU*	+3VS
GPIO 24	GPO	-	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	-	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5# EXT PU	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7# EXT PU	+3VSUS
GPIO 32	GPO	PM_CLKRUN# EXT PU	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPO	WLAN_ON EXT PU NS	+3VS
GPIO 37	GPO	BT_ON EXT PU NS	+3VS
GPIO 38	GPI	-	+3VS
GPIO 39	GPO	**CLK_PWRSAVE#** EXT PU	+3VS
GPIO 40	Native	USB_CON_OC01#	+3VSUS
GPIO 41	Native	USB_CON_OC2#	+3VSUS
GPIO 42	Native	USB_OC3# EXT PU	+3VSUS
GPIO 43	Native	USB_OC4# EXT PU	+3VSUS
GPIO 44	Native	USB_OC8# EXT PU	+3VSUS
GPIO 45	Native	USB_OC9# EXT PU	+3VSUS
GPIO 46	Native	USB_OC10# EXT PU	+3VSUS
GPIO 47	Native	USB_OC11# EXT PU	+3VSUS
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	- INT PU*	+3VS
GPIO 50	Native	PCI_REQ#1 EXT PU to +3VS	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU*	+3VS
GPIO 52	Native	PCI_REQ#2 EXT PU to +3VS	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU*	+3VS
GPIO 54	Native	PCI_REQ#3 EXT PU to +3VS	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_CON_OC01#	+3VSUS
GPIO 60	Native	PM_LINKALERT# EXT PU	+3VSUS

GPIO33 Internal Pull High, Go Low= Flash Descriptor Security will be overriden

EC GPIO	Use As	Signal Name	Power
GPIO02	GPO	PM_RSMRST#	
GPIO03	GPO	LCD_BACKOFF#	
GPIO04	GPI	EMAIL_SW#	
GPIO06	-	-	
GPIO07	-	-	
GPIO08	GPO	EXT_SMI#	
GPIO09	-	-	
GPIO0A	GPI	LID_EC#	
GPIO0B			
GPIO0C			
GPIO0D	GPI	DISTP_SW#	
GPIO11	GPO		
GPIO18			
GPIO19			

EC GPIO	Use As	Signal Name	Power

P80VC1

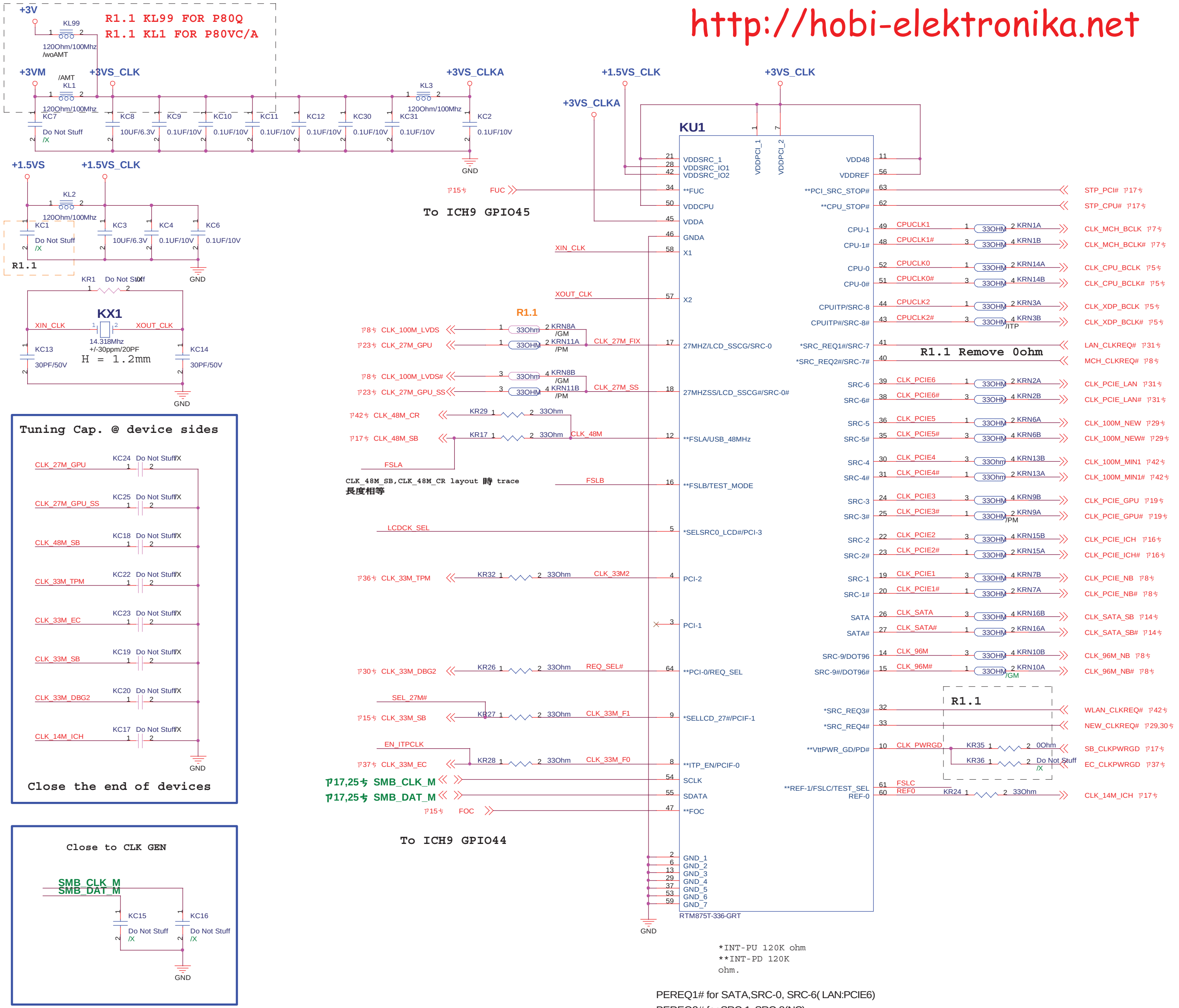
ASUSTeK COMPUTER INC. NB1

Title : System Information

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 3 of 52



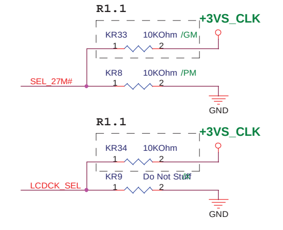
*INT-PU 120K ohm
**INT-PD 120K ohm.

PEREQ1# for SATA,SRC-0, SRC-6(LAN:PCIE6)
PEREQ2# for SRC-1, SRC-8(NC)
PEREQ3# for SRC-2,SRC-4(WLAN PCIE4)
PEREQ4# for SRC-3,SRC-5, SRC-7(NEWCARD PCIE5)

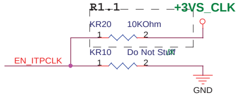
FSB Freq. Strap

FSC	FSB	FSA	CPU
0	0	0	266
0	0	1	133
0	1	0	200
0	1	1	166
1	0	0	333
1	0	1	100
1	1	0	400
1	1	1	200

LCDCK_SEL PIN 5 (IPU)	SEL_27M# PIN 9 (IPU)	PIN14, 15	PIN17	PIN18	
0	0	SRC-9	27FIX	27SS	
0	1	DOT96	DOT96SS	DOT96SS	
1	0	DOT96	27FIX	27SS	/PM
1	1	DOT96	SRC-0	SRC-0	/GM

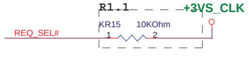


PIN 8 ITP_EN/PCIF-0
Select PIN43, 44 as CPUITP or SRC8



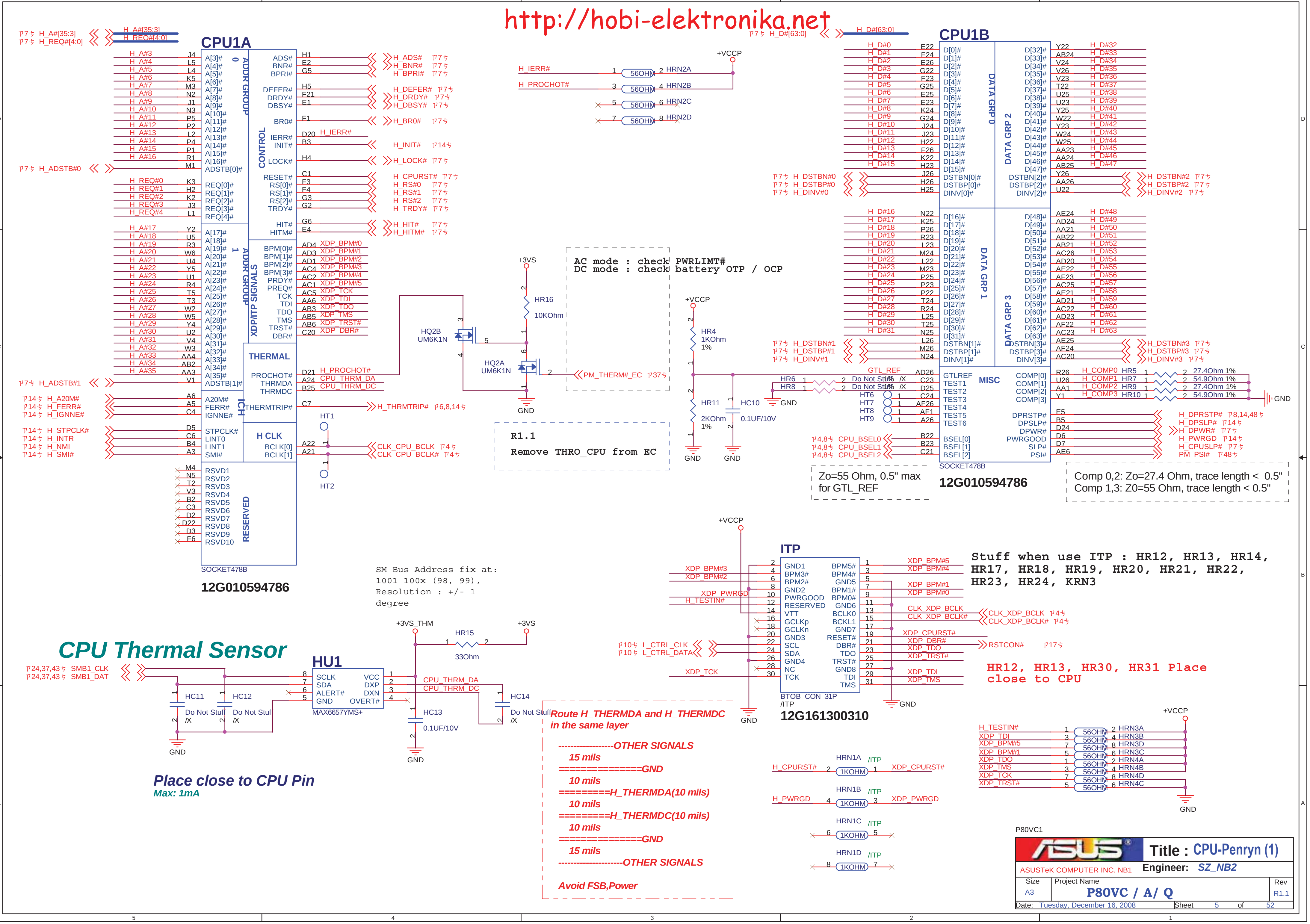
0 :SRC8
1 :CPUITP

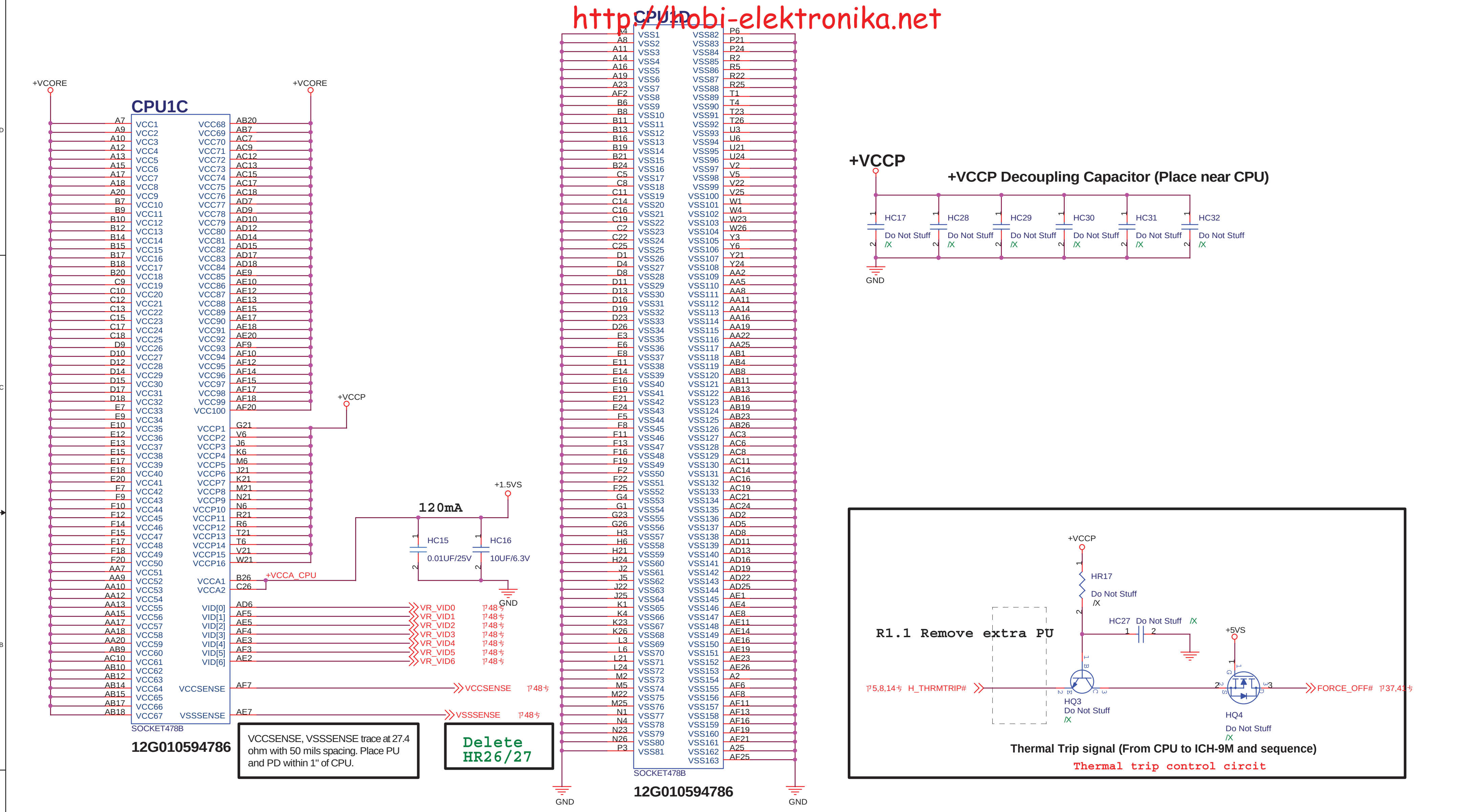
PIN 64 (IPD)PCI-0/REQ_SEL
Select PIN40, 41 as SRC_REQ# or SRC7



0 :SRC-7
1 :SRC_REQ#

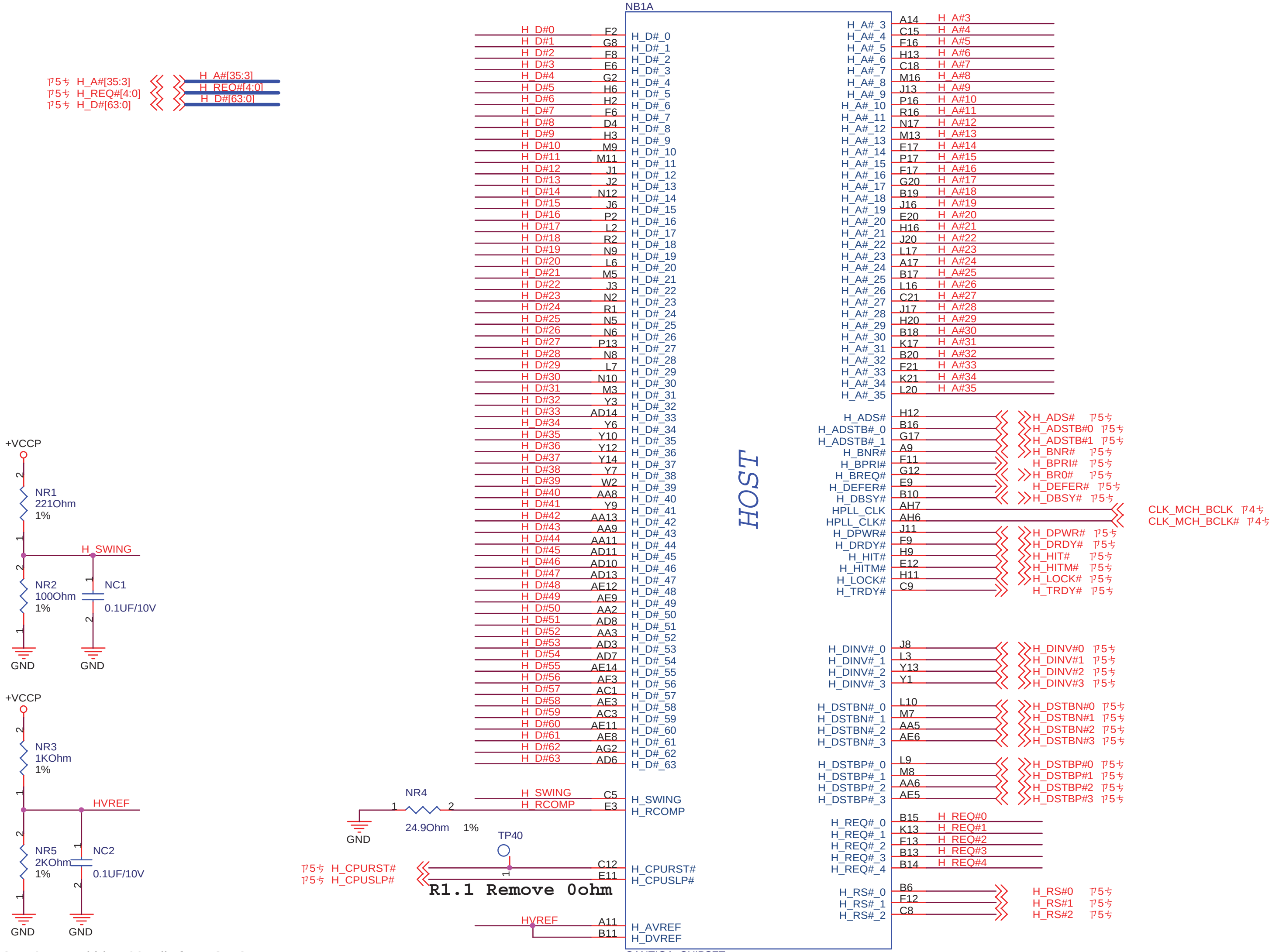
P80VC1
ASUSTeK COMPUTER INC. NB6
Title : Main Clock-1
Engineer: SZ_NB2
Size A2 | Project Name P80VC / A/ Q | Rev R1.1
Date: Tuesday, December 16, 2008 | Sheet 4 of 52


http://hobi-elektronika.net
CPU1A
CPU1B
SOCKET478B
12G010594786
AC mode : check PWRLIMT#
DC mode : check battery OTP / OCP
R1.1
Remove THRO_CPU from EC
Zo=55 Ohm, 0.5" max
for GTL_REF
Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"
ITP
BTOB_CON_31P
/ITP
12G161300310
Stuff when use ITP : HR12, HR13, HR14, HR17, HR18, HR19, HR20, HR21, HR22, HR23, HR24, KRN3
HR12, HR13, HR30, HR31 Place close to CPU
SM Bus Address fix at:
1001 100x (98, 99),
Resolution : +/- 1
degree
CPU Thermal Sensor
HU1
MAX6657YMS+
Place close to CPU Pin
Max: 1mA
Route H_THERMDA and H_THERMDC in the same layer
-----------------OTHER SIGNALS
15 mils
===============GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
===============GND
15 mils
-----------------OTHER SIGNALS
Avoid FSB,Power
P80VC1
ASUSTeK COMPUTER INC. NB1
Title : CPU-Penryn (1)
Engineer: SZ_NB2
Size A3
Project Name P80VC / A/ Q
Rev R1.1
Date: Tuesday, December 16, 2008
Sheet 5 of 52



P80VC1

ASUSTeK COMPUTER INC. NB1	Title : CPU-Penryn (2)	Engineer: SZ_NB2	
Size A3	Project Name P80VC / A/ Q		Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 6 of 52		

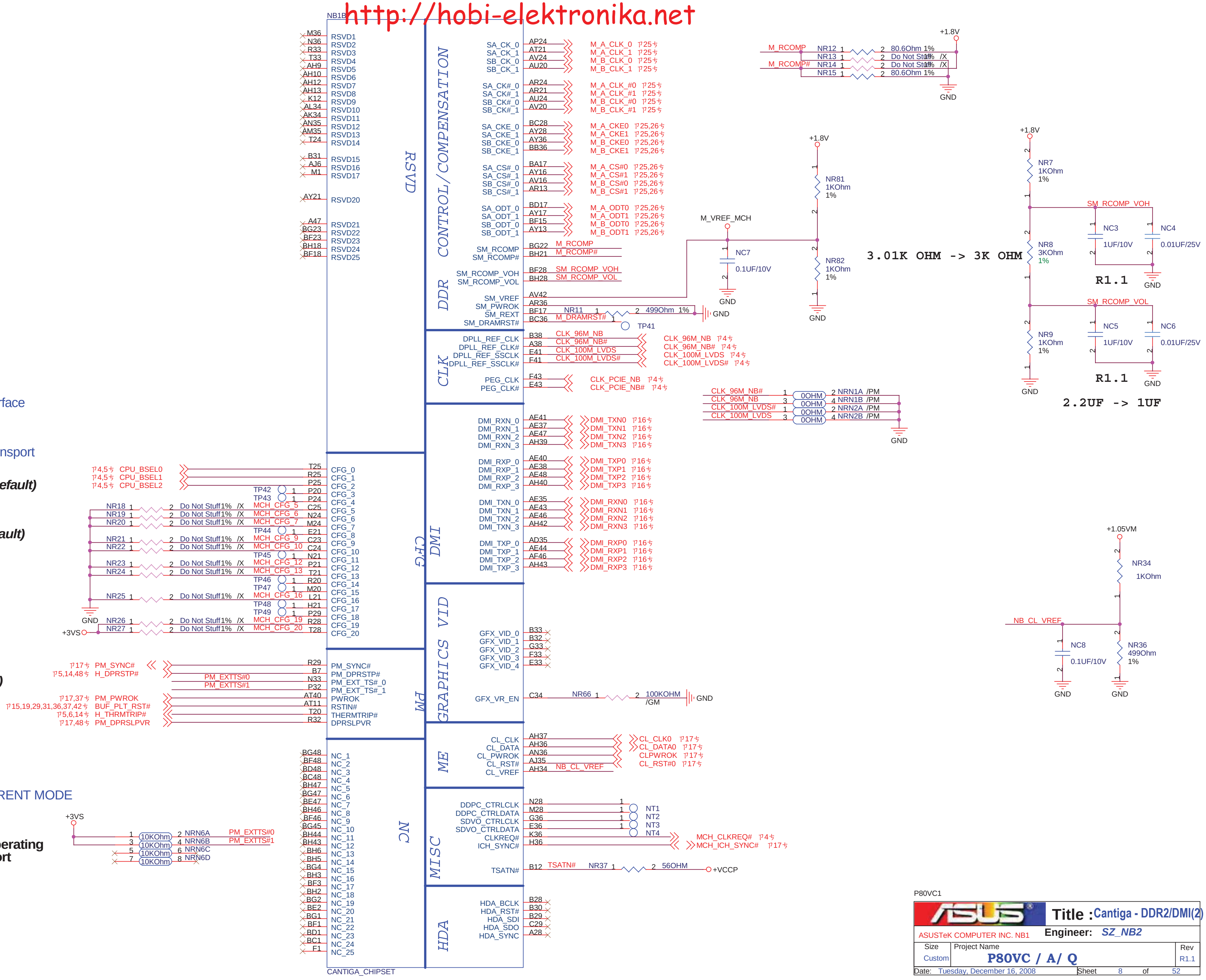


Cap 0.1uF within 100 mils from GMCH

BOM:
GM45:02G010020030
PM45:02G010022520
GL40:02G010023900
or 02G010017532

P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - CPU(1)	
	Engineer: SZ_NB2	
Size A3	Project Name P80VC / A/ Q	Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 7 of 52	



CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

CFG6 : Integrated TPM Host Interface

HIGH = iTPM disable (Default)

LOW = iTPM enable

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite

HIGH = With confidentiality (Default)

LOW = Without confidentiality

CFG9 : PCIE GRAPHIC LANE

HIGH = Normal Operation (Default)

LOW = Reverse Lanes

CFG10 : PCIe Loopback

HIGH = Disable (Default)

LOW = Enable

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

CFG16 : FSB Dynamic ODT

HIGH = Ensable (Default)

LOW = Disable

CFG19 : DMI Lane Reversal

LOW = NORMAL (default)

HIGH = Reverse Lanes

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational (Default)

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

P80VC1

ASUSTeK COMPUTER INC. NB1

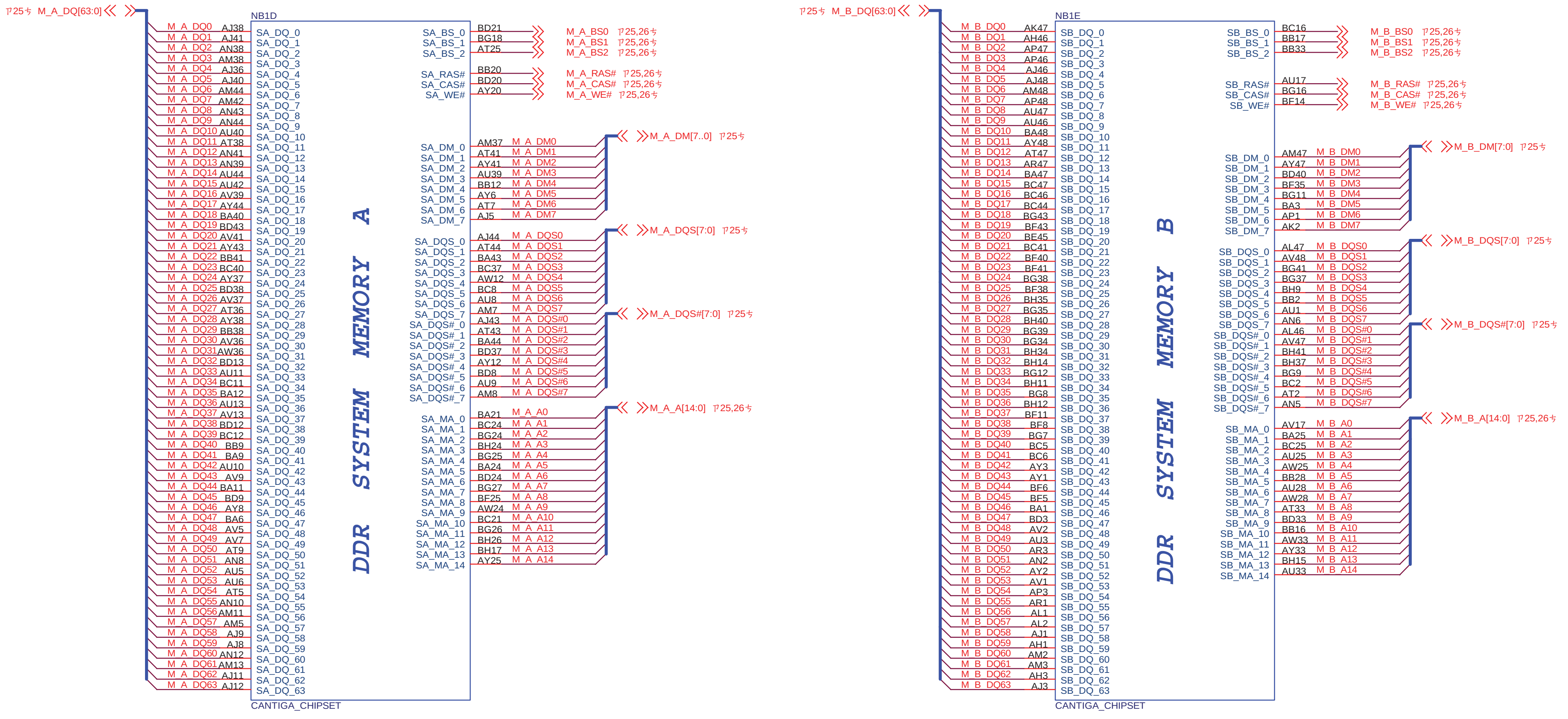
Title : Cantiga - DDR2/DMI(2)

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

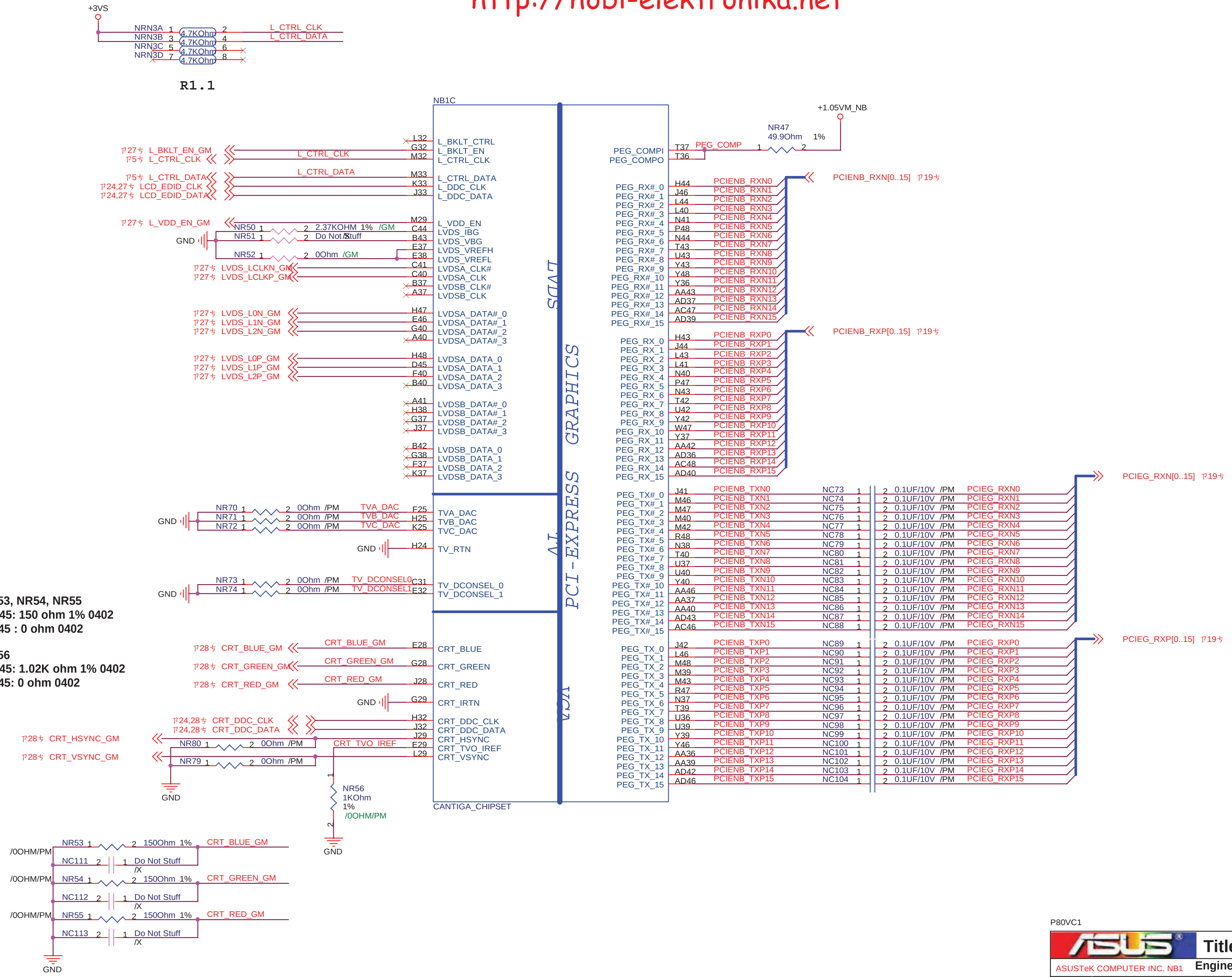
Date: Tuesday, December 16, 2008 Sheet 8 of 52

http://hobi-elektronika.net



P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - DDR2(3)	Engineer: SZ_NB2	
Size A3	Project Name P80VC / A/ Q		Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 9 of 52		



NR53, NR54, NR55
GM45: 150 ohm 1% 0402
PM45 : 0 ohm 0402

NR56
GM45: 1.02K ohm 1% 0402
PM45: 0 ohm 0402

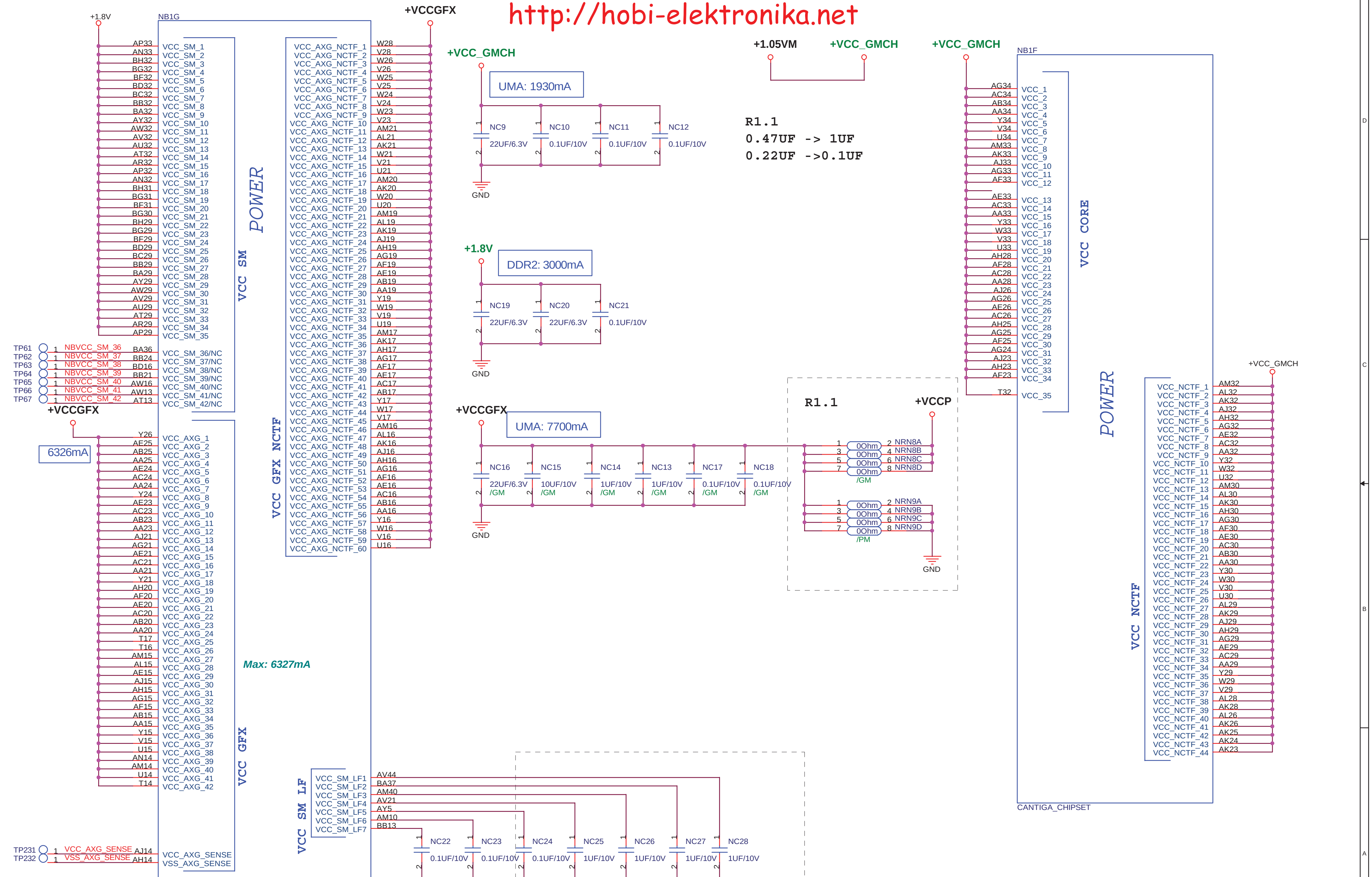
P80VC1

Title : Cantiga - PEG(4)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 10 of 52



P80VC1

ASUS

Title : Cantiga - POWER(5)

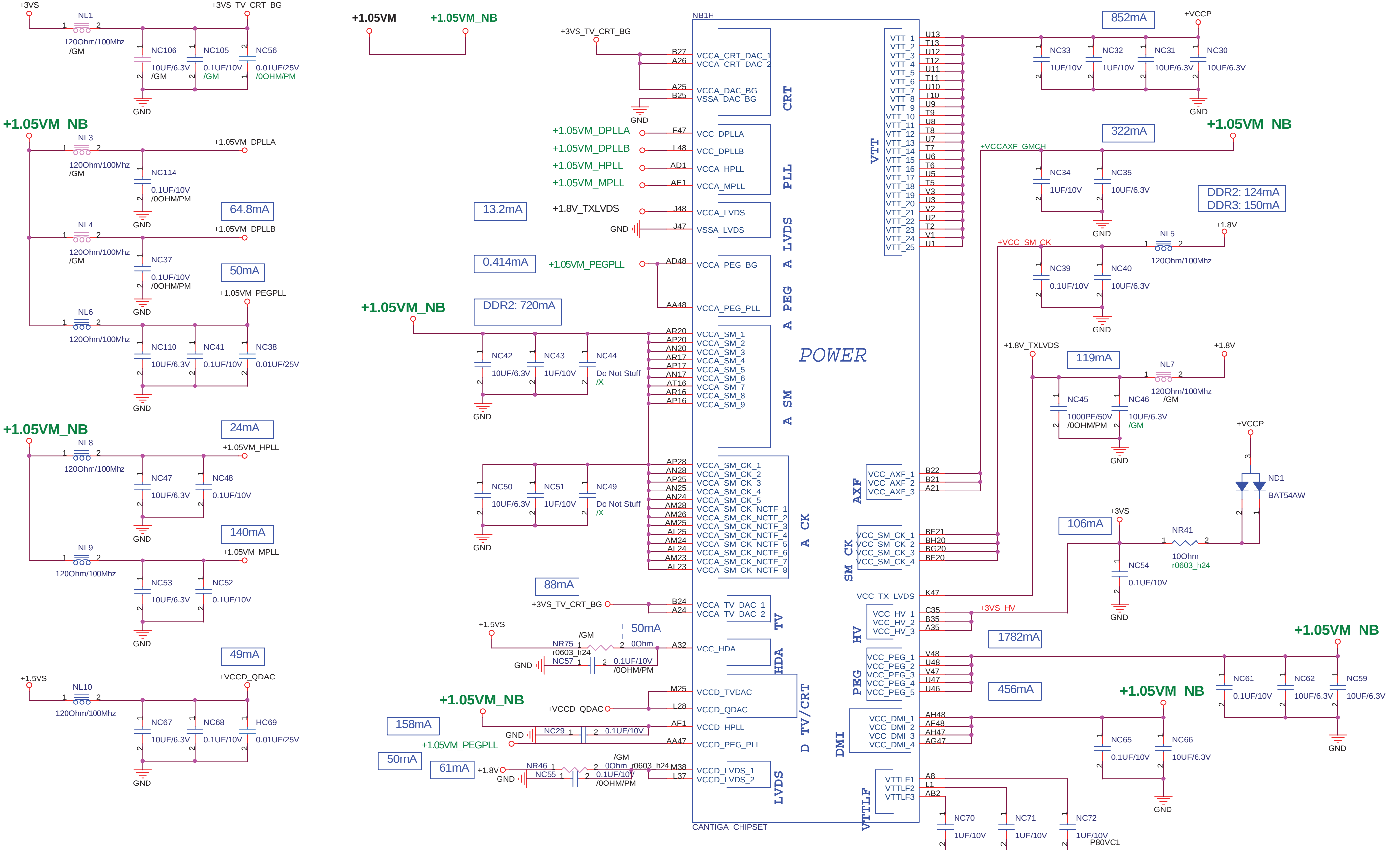
ASUSTeK COMPUTER INC. NB1

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 11 of 52

http://hobi-elektronika.net



ASUSTeK COMPUTER INC. NB1

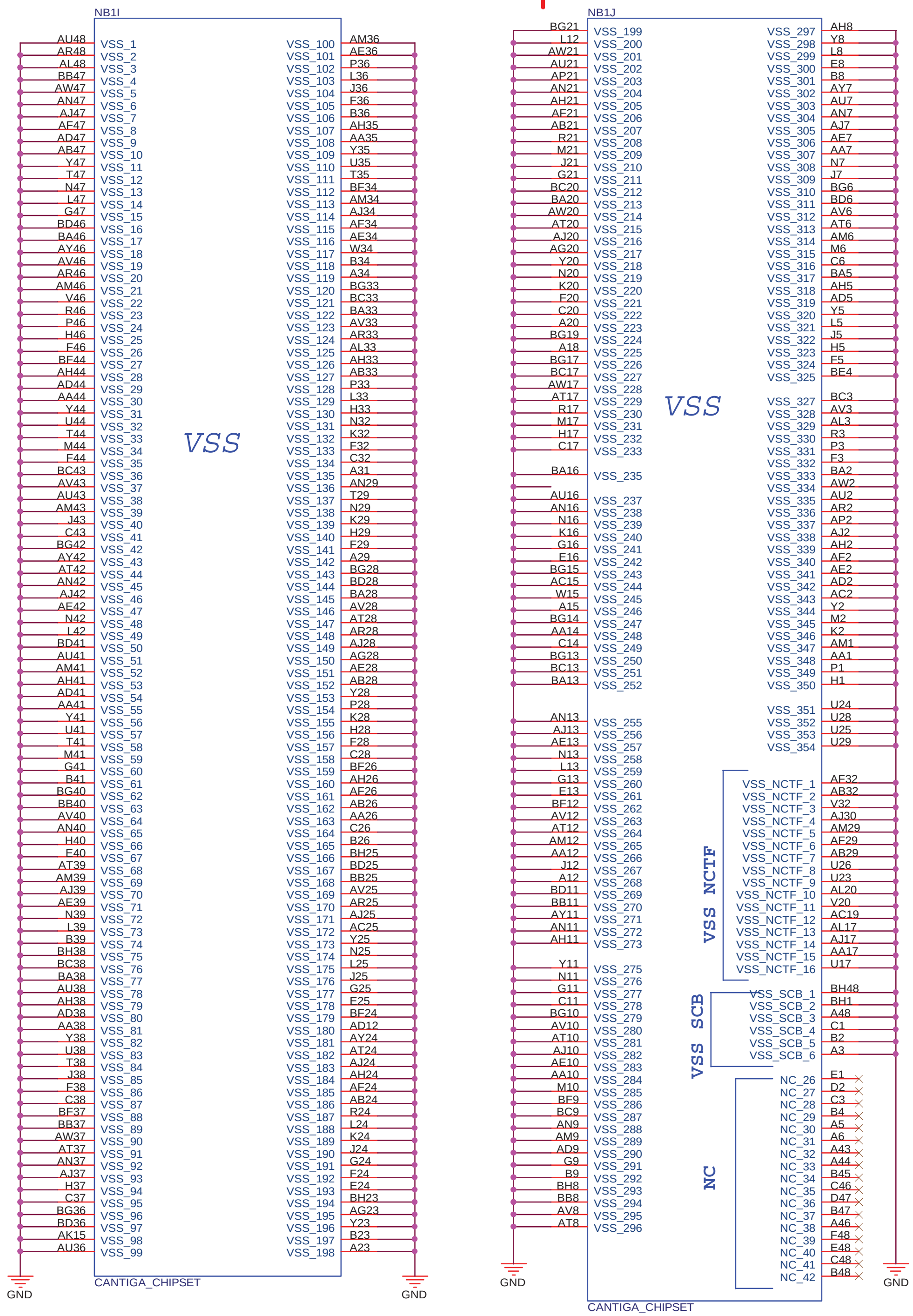
Title : Cantiga - POWER(6)

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 12 of 52

http://hobi-elektronika.net



Change NC-26/42 to NC from GND

P80VC1

ASUS

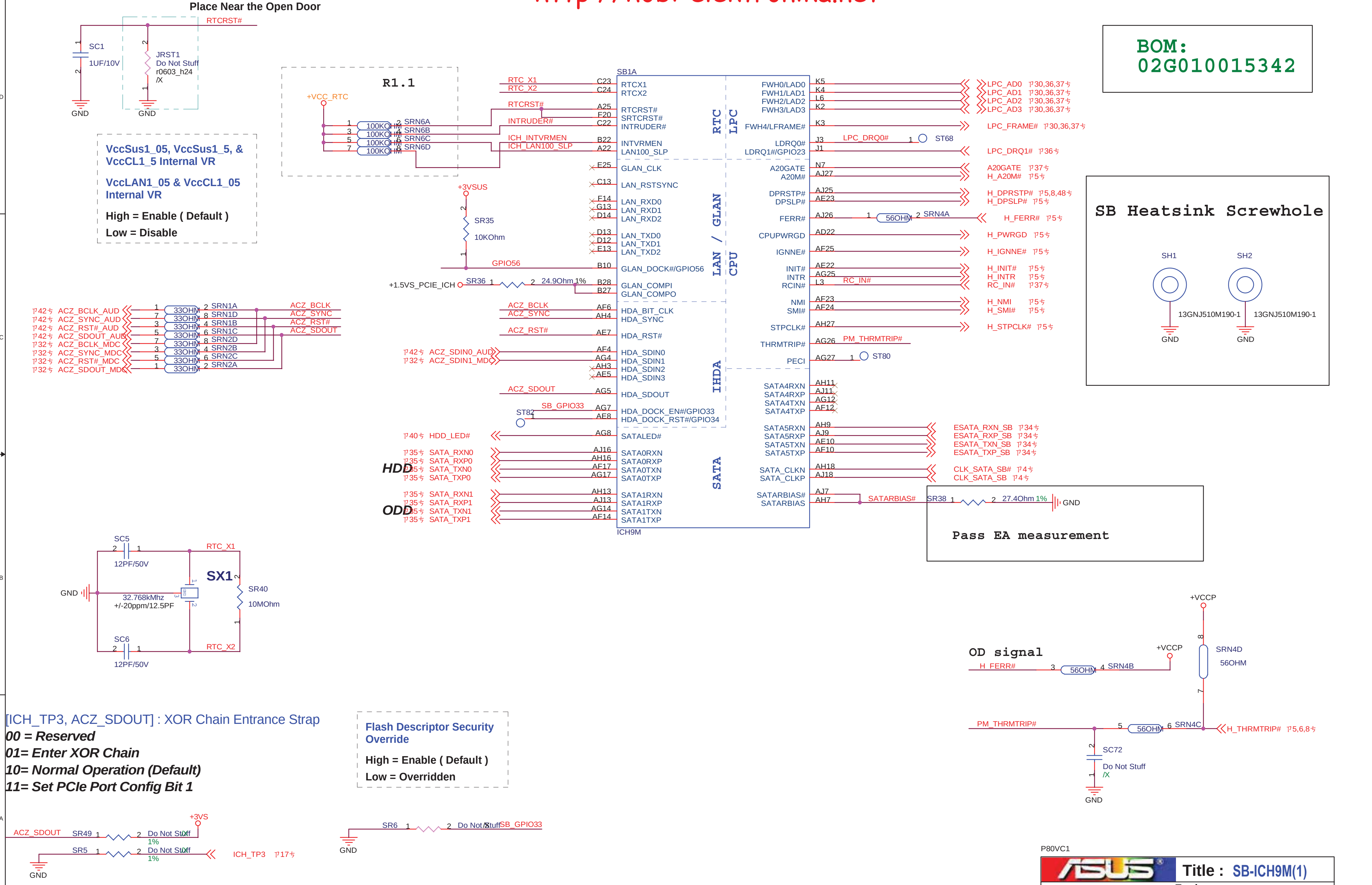
Title : Cantiga - GND(7)

ASUSTeK COMPUTER INC. NB1

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 13 of 52



BOM: 02G010015342

VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR

VccLAN1_05 & VccCL1_05 Internal VR

High = Enable (Default)

Low = Disable

[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved

01= Enter XOR Chain

10= Normal Operation (Default)

11= Set PCIe Port Config Bit 1

Flash Descriptor Security Override

High = Enable (Default)

Low = Overridden

P80VC1

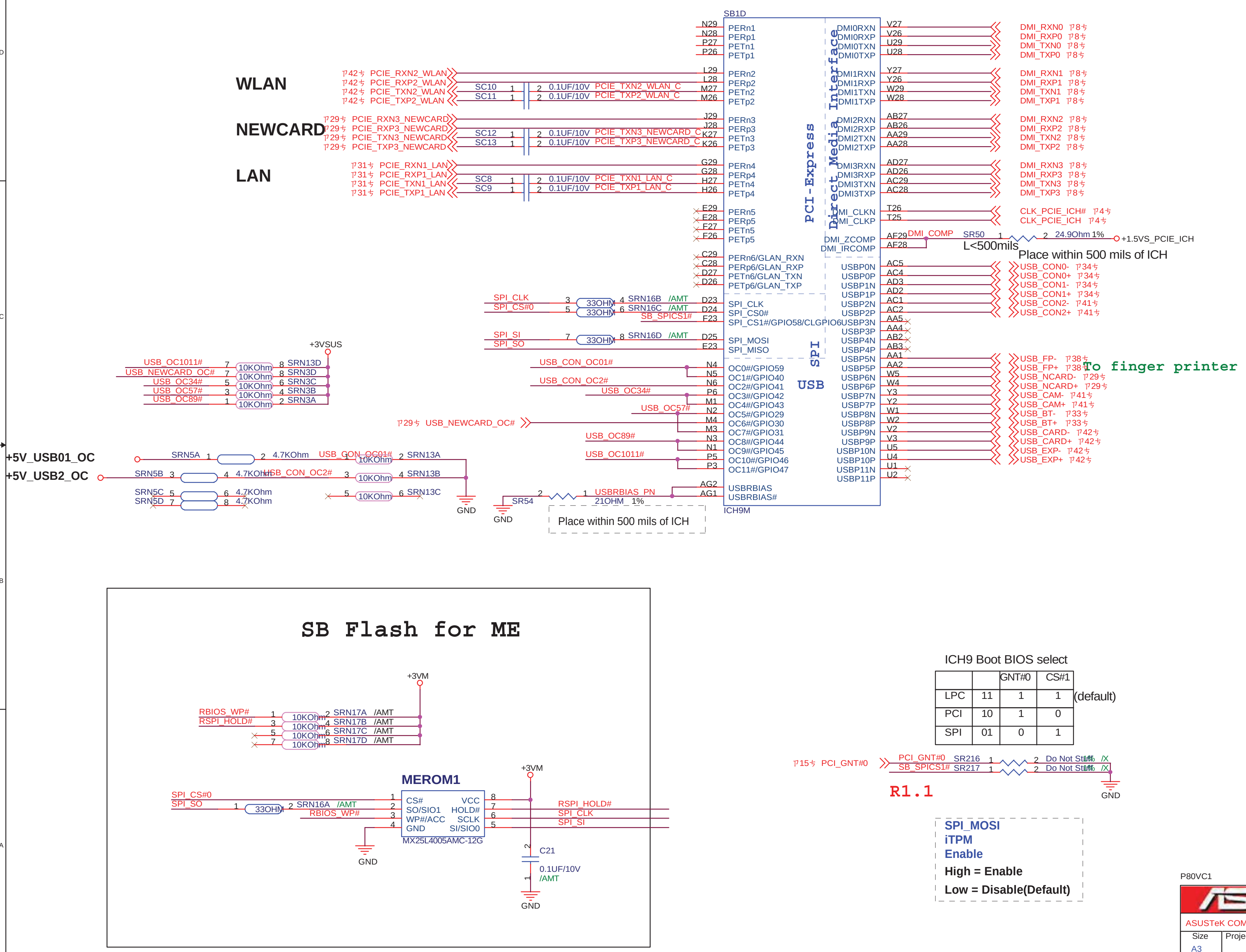
ASUS	Title : SB-ICH9M(1)		
ASUSTeK COMPUTER INC. NB1	Engineer: SZ_NB2		
Size A3	Project Name P80VC / A/ Q		Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 14 of 52		

UNUSED PCI temination

AD [31:0]	Can be left unconnected
C/BE [3:0]#	Can be left unconnected
DEVSEL#	8.2-k weak pull-up resistor to Vcc3_3
FRAME#	8.2-k weak pull-up resistor to Vcc3_3
IRDY#	8.2-k weak pull-up resistor to Vcc3_3
TRDY#	8.2-k weak pull-up resistor to Vcc3_3
STOP#	8.2-k weak pull-up resistor to Vcc3_3
PAR	Can be left unconnected
PERR#	8.2-k weak pull-up resistor to Vcc3_3
REQ0# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54	Requires a 8.2-k weak pull-up resistor to Vcc3_3. REQ [3:1] can be configured as GPIO instead.
GNT0# GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55	Can be left unconnected. GNT [3:1]# can be configured as GPIO instead. GNT [3:0] is sampled as a functional strapping;
PCICLK	Should remain connected to 33-MHz clock source
PCIRST#	Can be left unconnected
PLOCK#	8.2-k weak pull-up resistor to Vcc3_3
SERR#	8.2-k weak pull-up resistor to Vcc3_3
PIRQ [D:A]# PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5	Requires a 8.2-k weak pull-up resistor to Vcc3_3 PIRQ [H:E]# Can be configured as GPIO instead
SERIRQ	8.2-k pull-up to Vcc3_3
PME#	Can be left unconnected. Internally pull-up
CLKRUN#	8.2-k weak pull-up resistor to Vcc3_3

P80VC1

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH9M(2)
	Engineer: SZ_NB2
Size A3	Project Name P80VC / A/ Q — Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 15 of 52



USB0	CON
USB1	CON
USB2	CON
USB3	N/A
USB4	N/A
USB5	FingerPrint
USB6	NewCard
USB7	Camera
USB8	BT
USB9	Cardreader
USB10	MC (WLAN)
USB11	N/A

ICH9 Boot BIOS select

		GNT#0	CS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

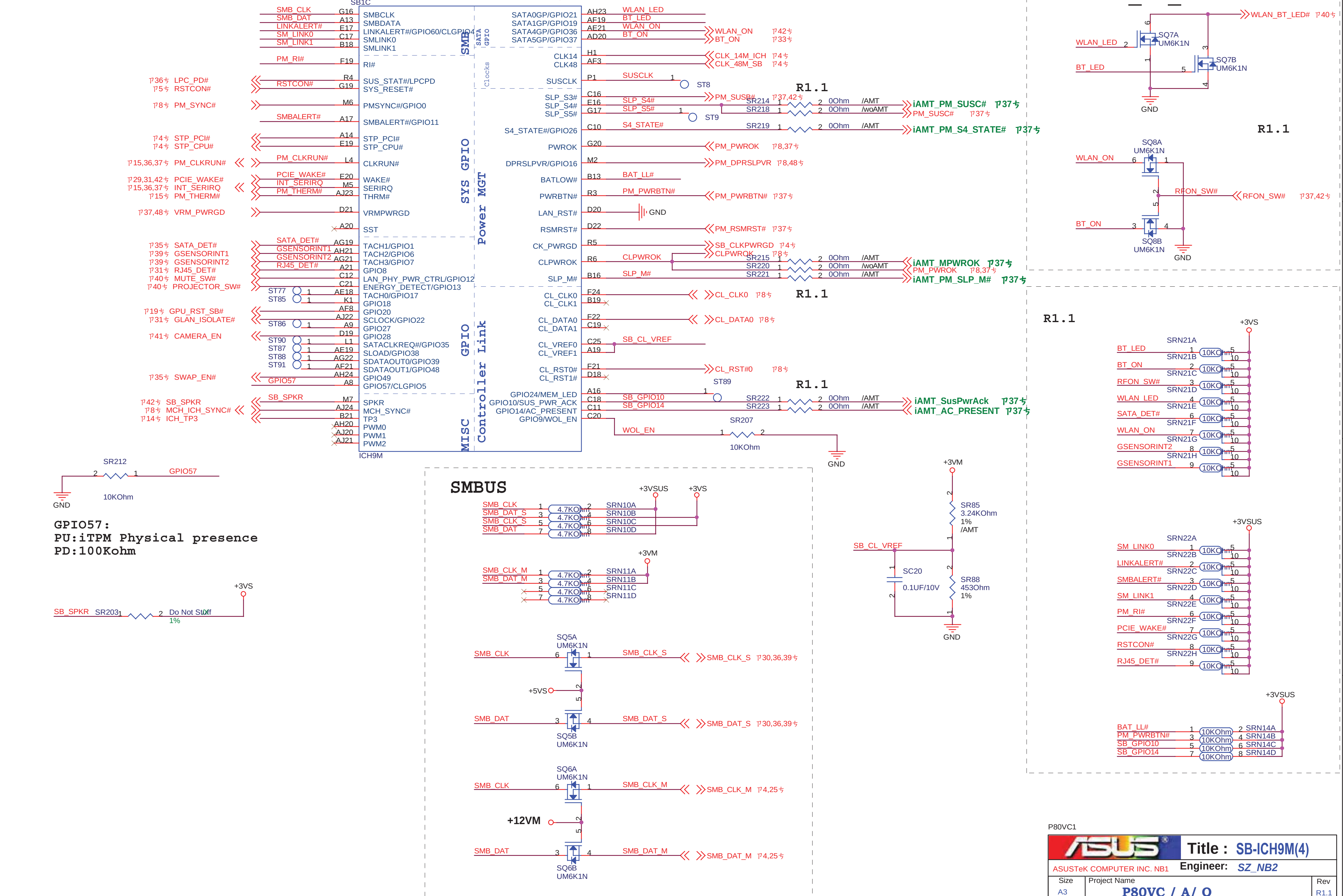
R1.1

SPI_MOSI
iTPM
Enable
High = Enable
Low = Disable(Default)

P80VC1

ASUSTeK COMPUTER INC. NB1
Title : SB-ICH9M(3)
Engineer: SZ_NB2
Size: A3 | Project Name: P80VC / A/ Q | Rev: R1.1
Date: Tuesday, December 16, 2008 | Sheet 16 of 52

http://hobi-elektronika.net



P80VC1

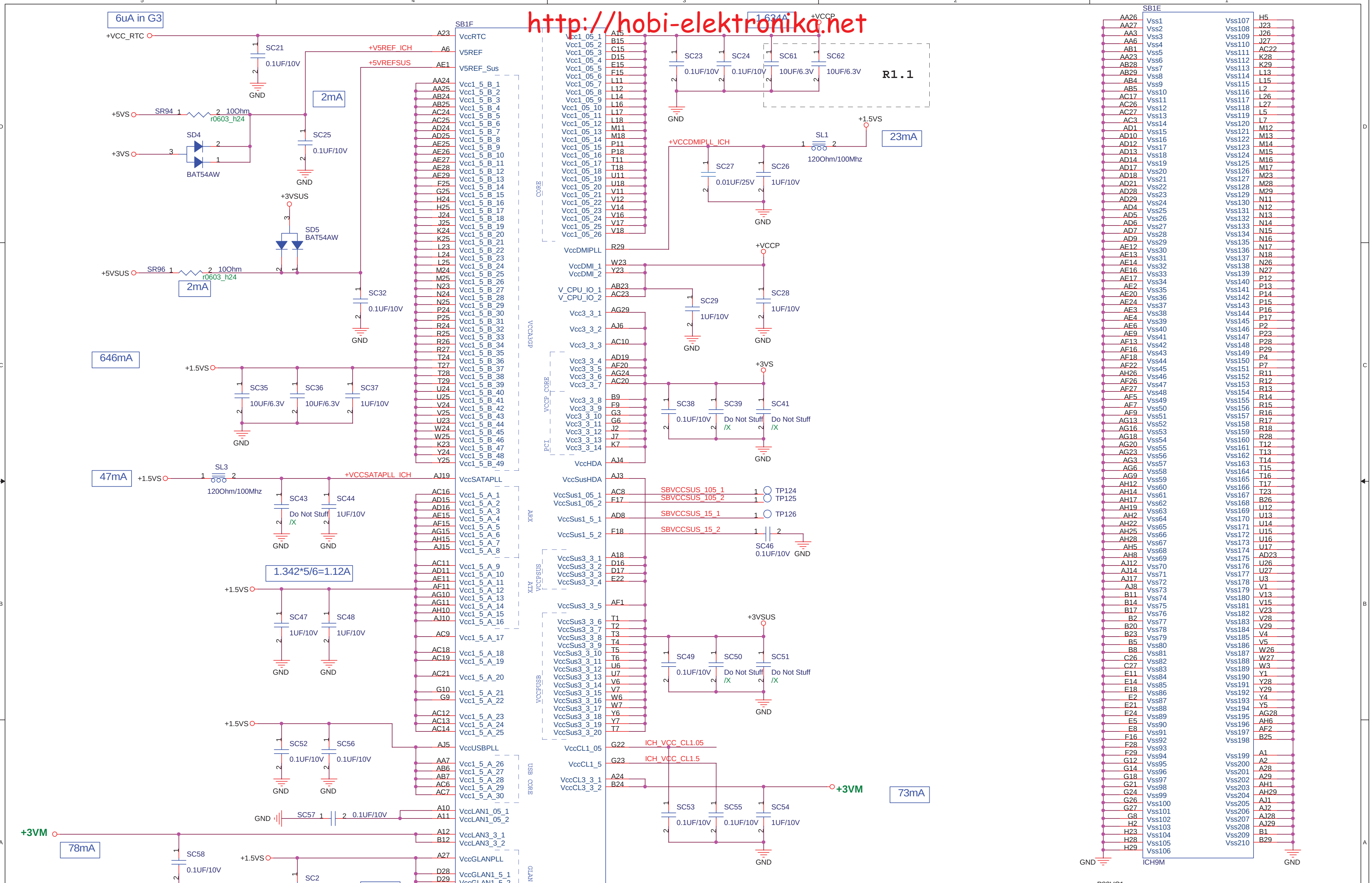
ASUSTeK COMPUTER INC. NB1

Title : SB-ICH9M(4)

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 17 of 52



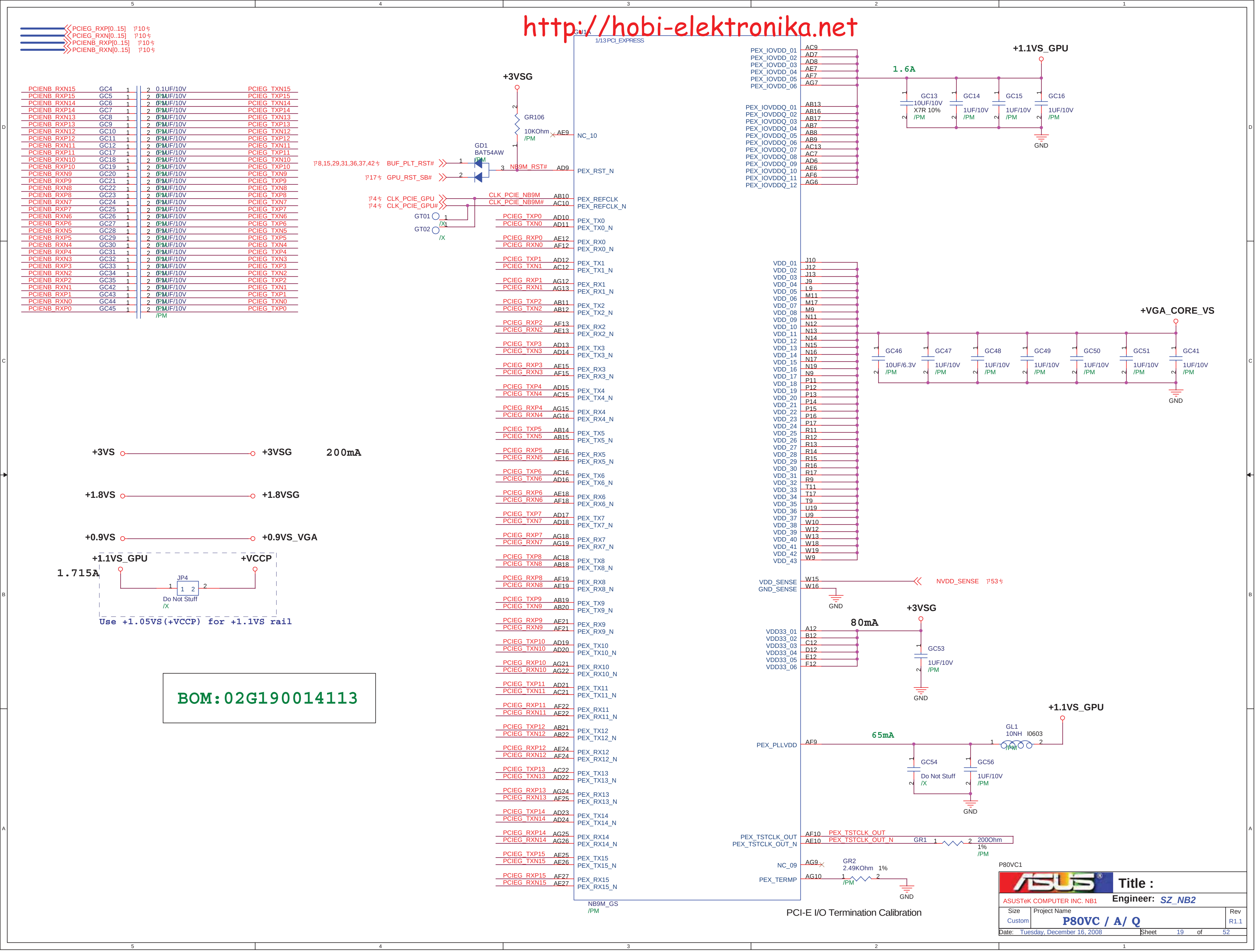
ASUSTeK COMPUTER INC. NB1

Title : SB-ICH9M(PWR)

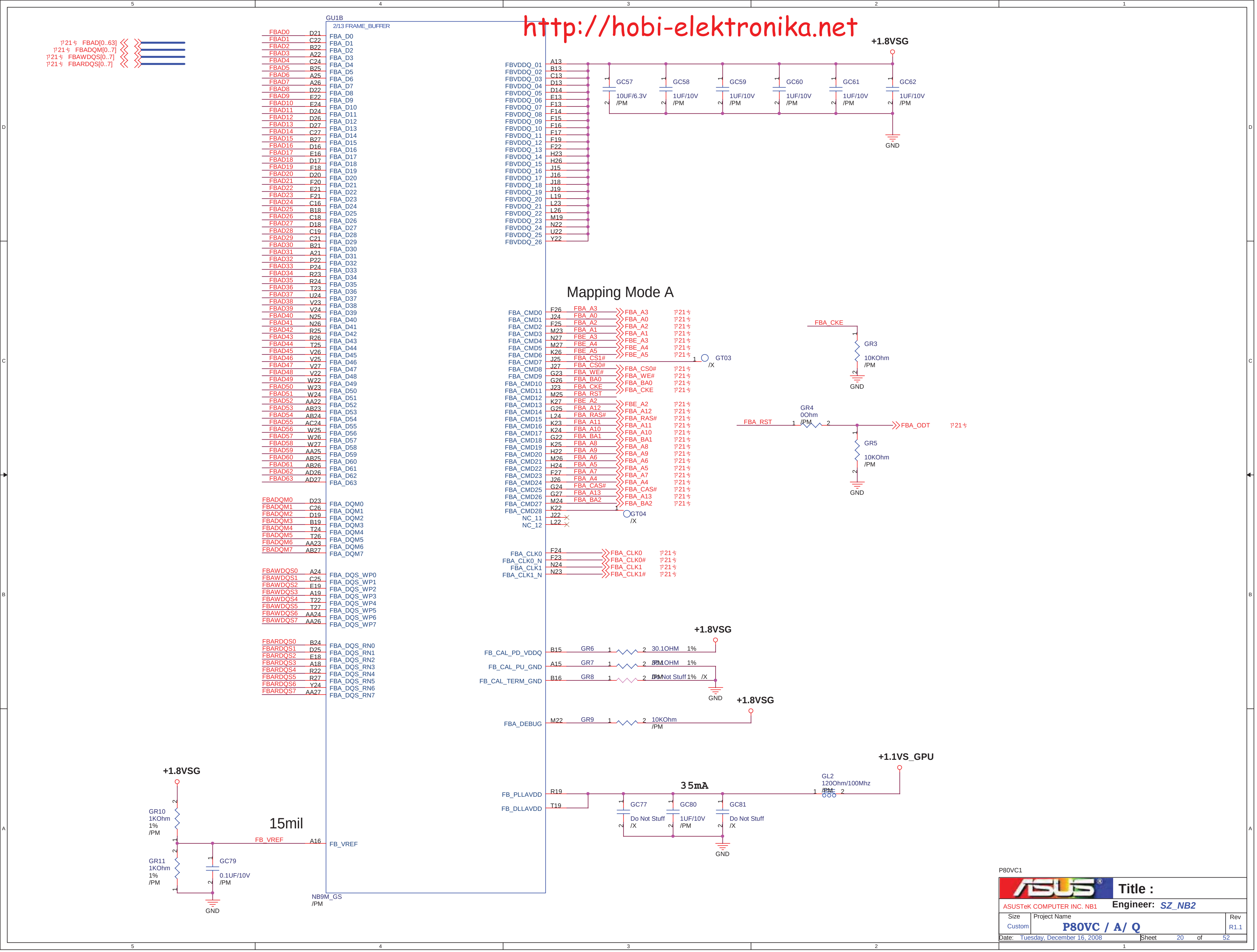
Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

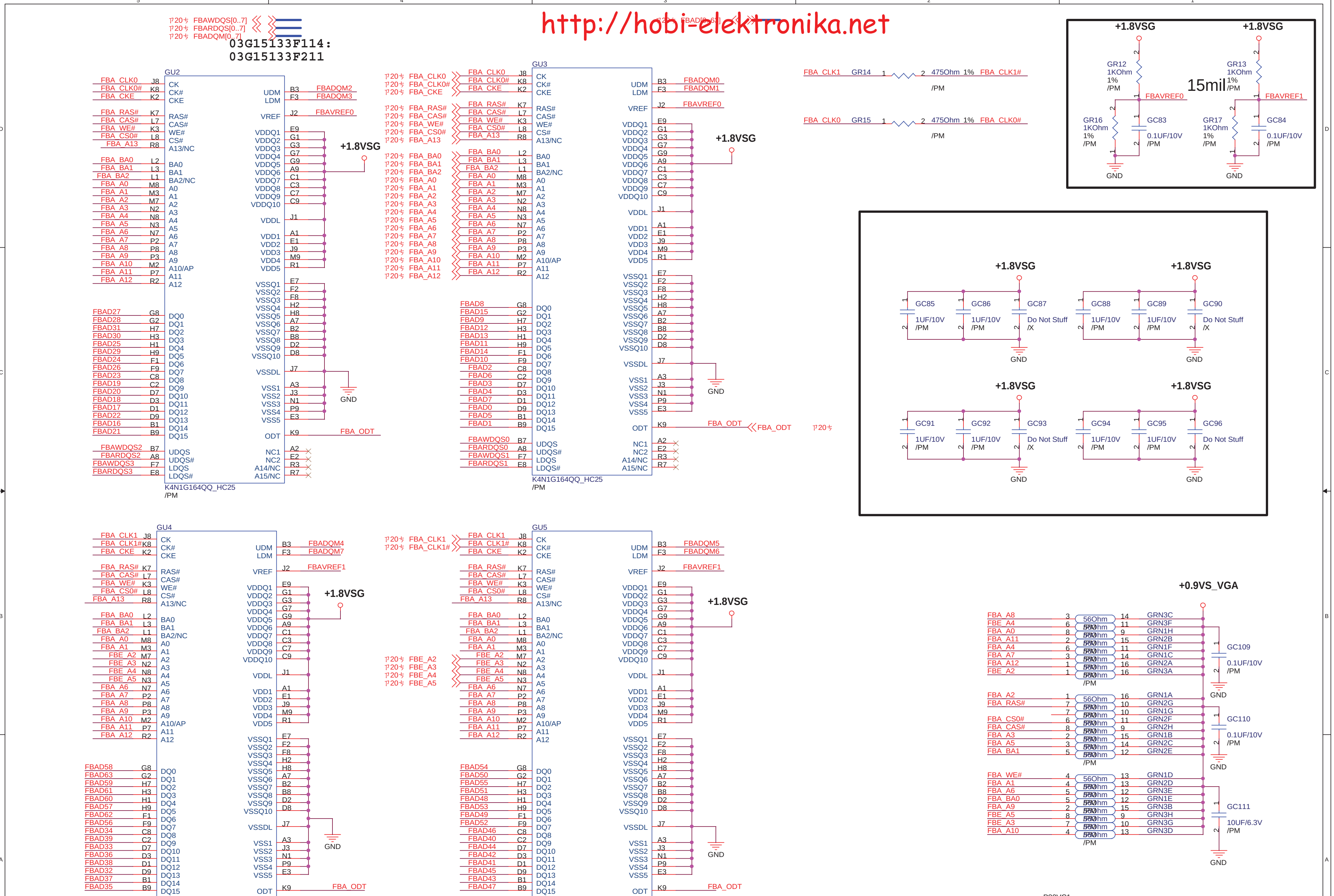
Date: Tuesday, December 16, 2008 Sheet 18 of 52



http://hobi-elektronika.net
PCIEG_RXP[0..15]
PCIEG_RXN[0..15]
PCIENB_RXP[0..15]
PCIENB_RXN[0..15]
1/13 PCI_EXPRESS
+3VSG
GR106
10KOhm
/PM
GD1
BAT54AW
BUF_PLT_RST#
GPU_RST_SB#
NB9M_RST#
CLK_PCIE_GPU
CLK_PCIE_GPU#
CLK_PCIE_NB9M
CLK_PCIE_NB9M#
GT01
GT02
NC_10
PEX_RST_N
PEX_REFCLK
PEX_REFCLK_N
+1.1VS_GPU
1.6A
GC13
10UF/10V
X7R 10%
GC14
GC15
GC16
1UF/10V
GND
+VGA_CORE_VS
GC46
10UF/6.3V
GC47
GC48
GC49
GC50
GC51
GC41
+3VS
+3VSG
200mA
+1.8VS
+1.8VSG
+0.9VS
+0.9VS_VGA
+1.1VS_GPU
+VCCP
1.715A
JP4
Do Not Stuff
/X
Use +1.05VS(+VCCP) for +1.1VS rail
BOM:02G190014113
VDD_SENSE
GND_SENSE
NVDD_SENSE
80mA
GC53
1UF/10V
65mA
PEX_PLLVDD
GL1
10NH
I0603
GC54
Do Not Stuff
GC56
1UF/10V
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
GR1
200Ohm
1%
NC_09
PEX_TERMP
GR2
2.49KOhm 1%
NB9M_GS
/PM
PCI-E I/O Termination Calibration
P80VC1
ASUS
Title :
ASUSTeK COMPUTER INC. NB1
Engineer: SZ_NB2
Size
Custom
Project Name
P80VC / A/ Q
Rev
R1.1
Date: Tuesday, December 16, 2008
Sheet 19 of 52



http://hobi-elektronika.net
GU1B
2/13 FRAME_BUFFER
FBAD[0..63]
FBADQM[0..7]
FBAWDQS[0..7]
FBARDQS[0..7]
FBAD0 … FBAD63
FBA_D0 … FBA_D63
FBADQM0 … FBADQM7
FBA_DQM0 … FBA_DQM7
FBAWDQS0 … FBAWDQS7
FBA_DQS_WP0 … FBA_DQS_WP7
FBARDQS0 … FBARDQS7
FBA_DQS_RN0 … FBA_DQS_RN7
FBVDDQ_01 … FBVDDQ_26
+1.8VSG
GC57 10UF/6.3V /PM
GC58 1UF/10V /PM
GC59 1UF/10V /PM
GC60 1UF/10V /PM
GC61 1UF/10V /PM
GC62 1UF/10V /PM
GND
Mapping Mode A
FBA_CMD0 … FBA_CMD28
NC_11
NC_12
FBA_A3
FBA_A0
FBA_A2
FBA_A1
FBE_A3
FBE_A4
FBE_A5
FBA_CS1#
FBA_CS0#
FBA_WE#
FBA_BA0
FBA_CKE
FBA_RST
FBE_A2
FBA_A12
FBA_RAS#
FBA_A11
FBA_A10
FBA_BA1
FBA_A8
FBA_A9
FBA_A6
FBA_A5
FBA_A7
FBA_A4
FBA_CAS#
FBA_A13
FBA_BA2
GT03 /X
GT04 /X
GR3 10KOhm /PM
GR4 0Ohm /PM
FBA_ODT
GR5 10KOhm /PM
FBA_CLK0
FBA_CLK0_N
FBA_CLK1
FBA_CLK1_N
FBA_CLK0#
FBA_CLK1#
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
GR6 30.1OHM 1%
GR7 40.2OHM 1% /PM
GR8 Do Not Stuff 1% /X
FBA_DEBUG
GR9 10KOhm /PM
+1.1VS_GPU
FB_PLLAVDD
FB_DLLAVDD
35mA
GL2 120Ohm/100Mhz /PM
GC77 Do Not Stuff /X
GC80 1UF/10V /PM
GC81 Do Not Stuff /X
GR10 1KOhm 1% /PM
GR11 1KOhm 1% /PM
15mil
FB_VREF
GC79 0.1UF/10V /PM
NB9M_GS /PM
P80VC1
ASUS
ASUSTeK COMPUTER INC. NB1
Title :
Engineer: SZ_NB2
Size Custom
Project Name P80VC / A/ Q
Rev R1.1
Date: Tuesday, December 16, 2008
Sheet 20 of 52



P80VC1

ASUSTeK COMPUTER INC. NB1

Title :

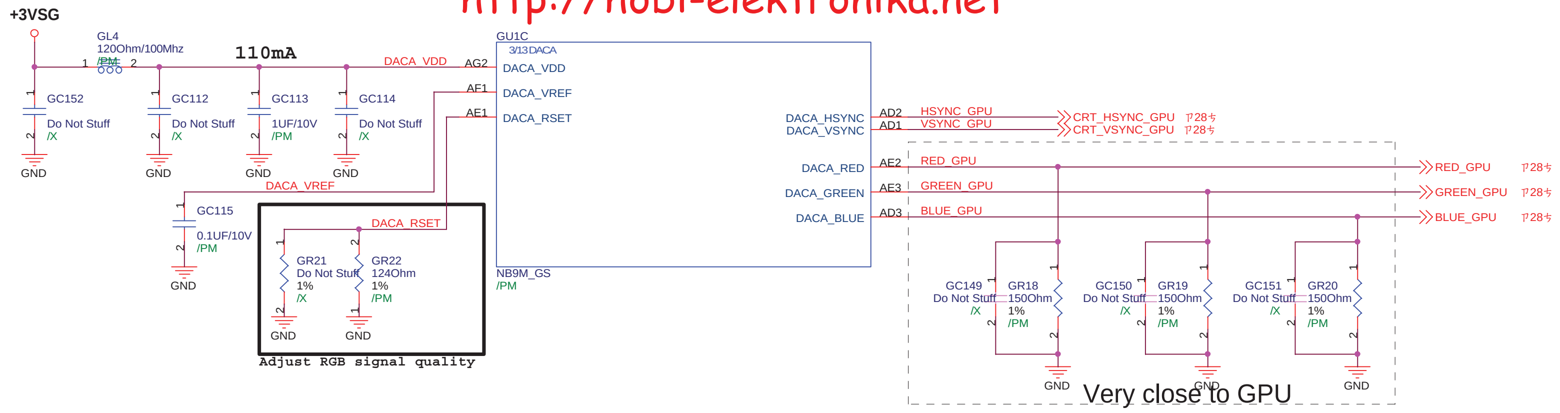
Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

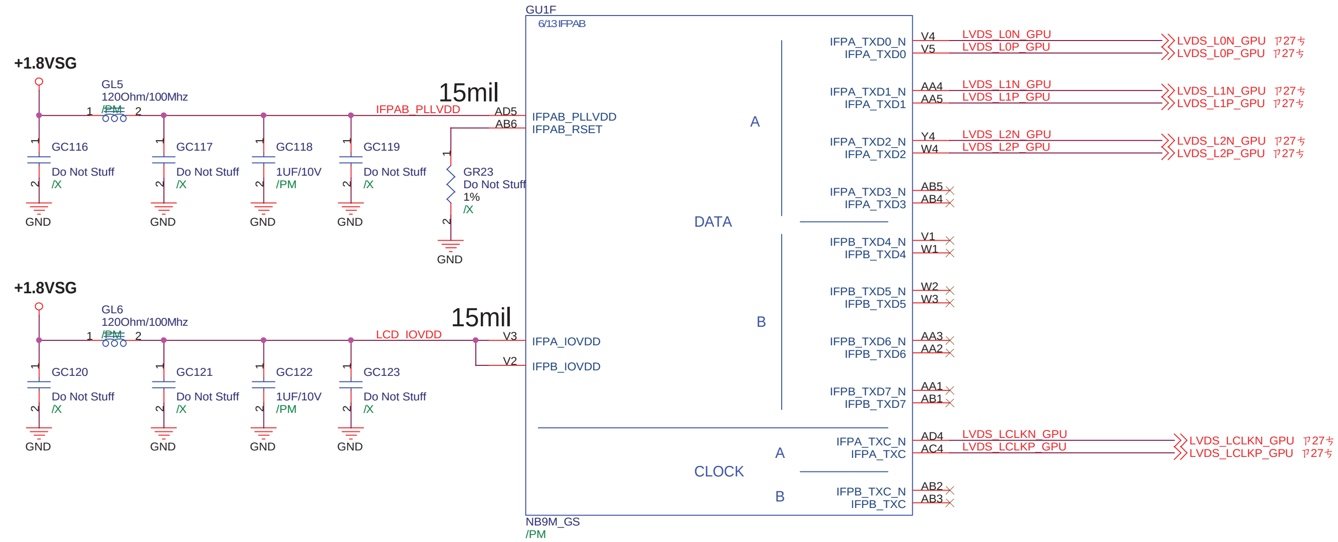
Date: Tuesday, December 16, 2008 Sheet 21 of 52

VGA

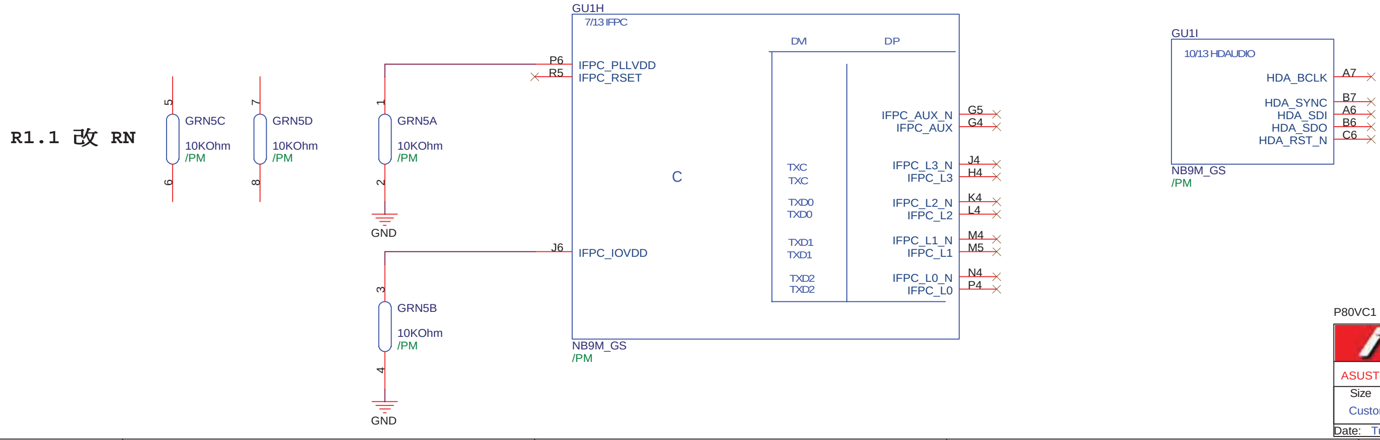
http://hobi-elektronika.net



LVDS



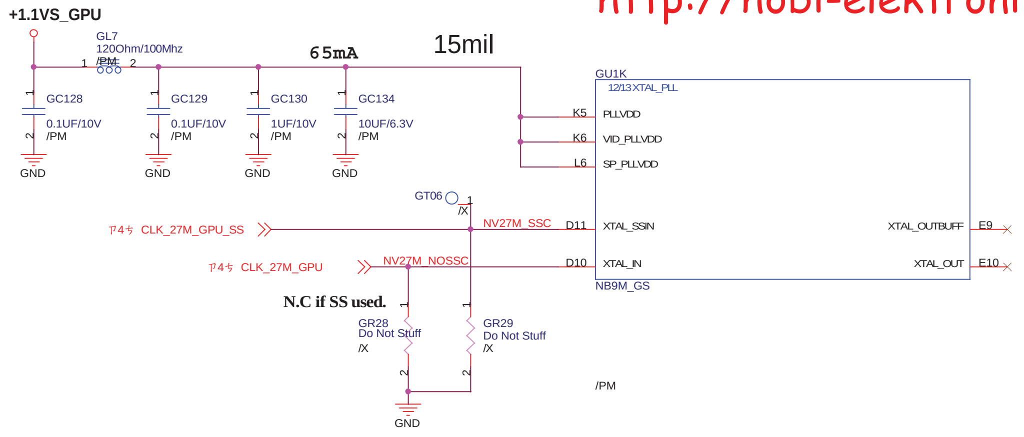
HDMI



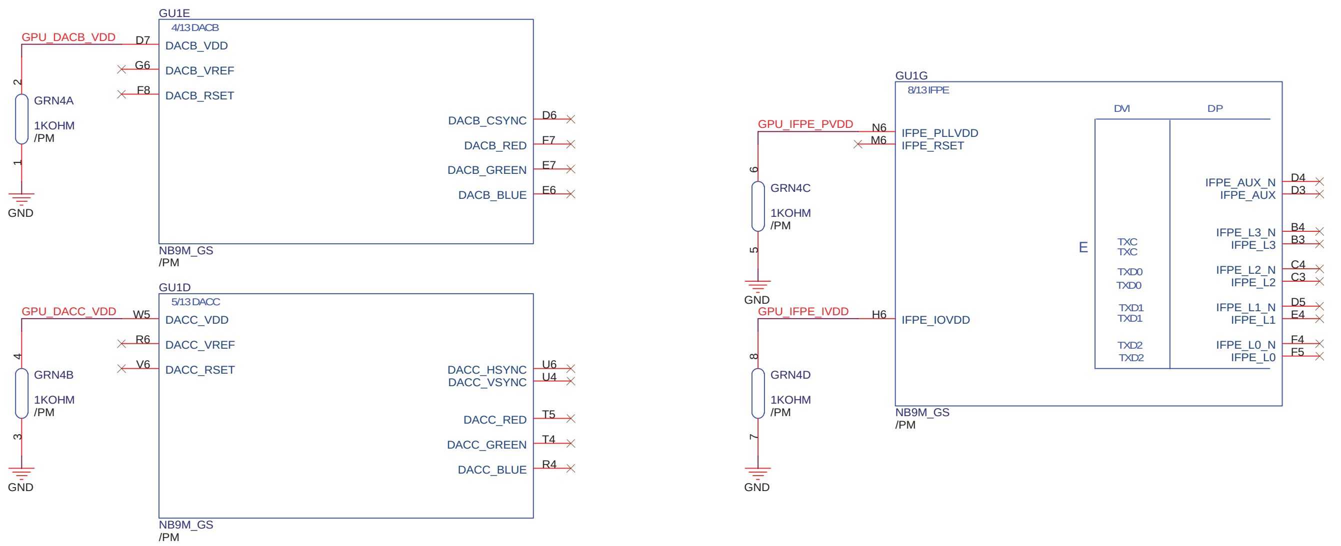
P80VC1

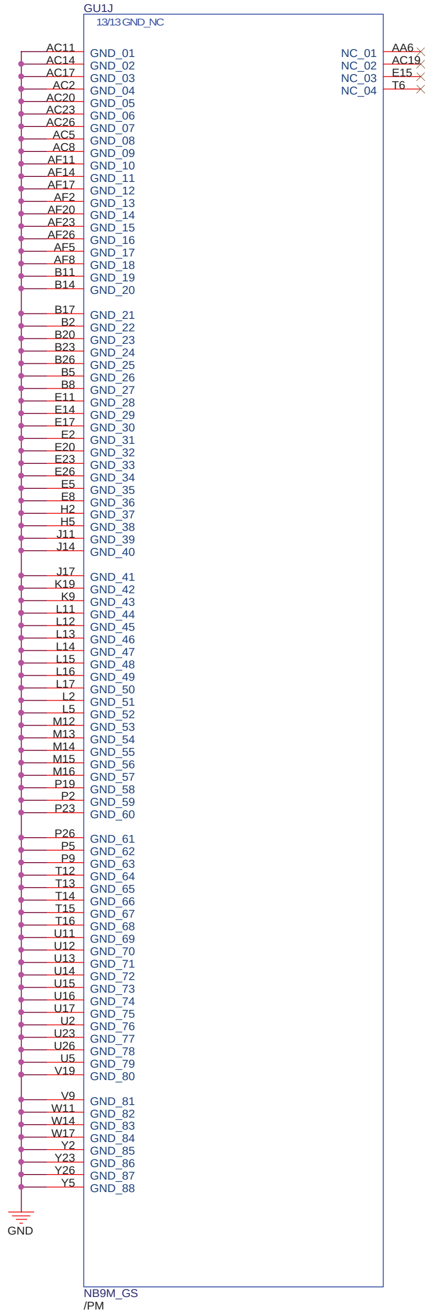
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 22 of 52	

Xtal



Other





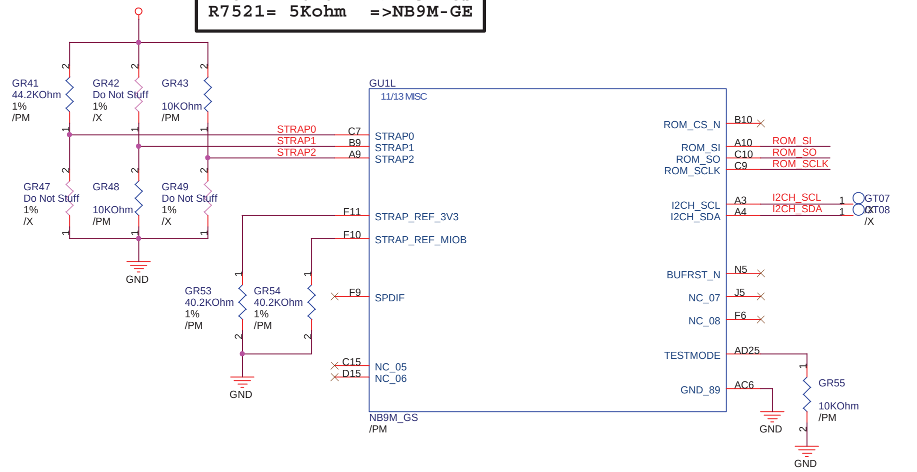
P80VC1

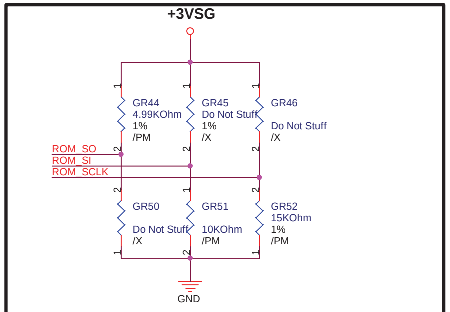
ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: SZ_NB2		
Size: Custom	Project Name: P80VC / A/ Q		Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 23 of 52		

http://hobi-elektronika.net

ROM

```
R7521= 10Kohm =>NB9M-GS
R7521= 5Kohm  =>NB9M-GE
```

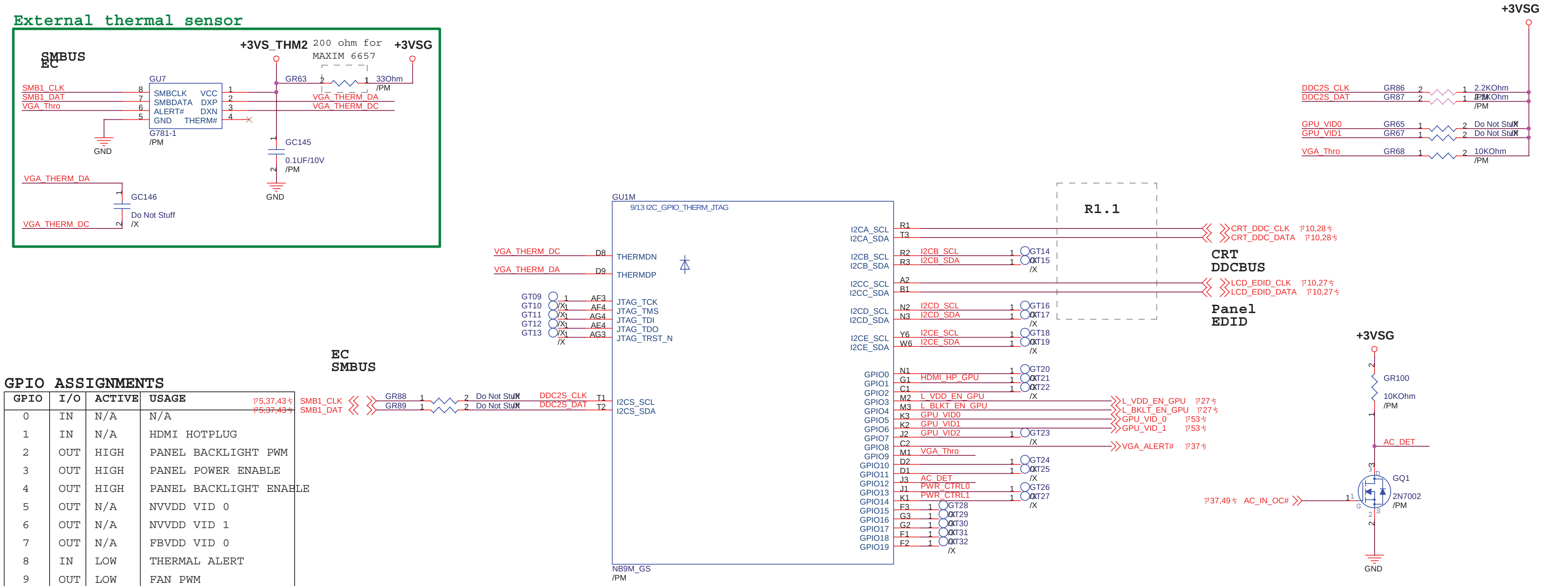




ROM_SI:
Sumsung K4N1G164QQ-HC25,10k PD to gnd

GPIO

External thermal sensor



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL

P80VC1

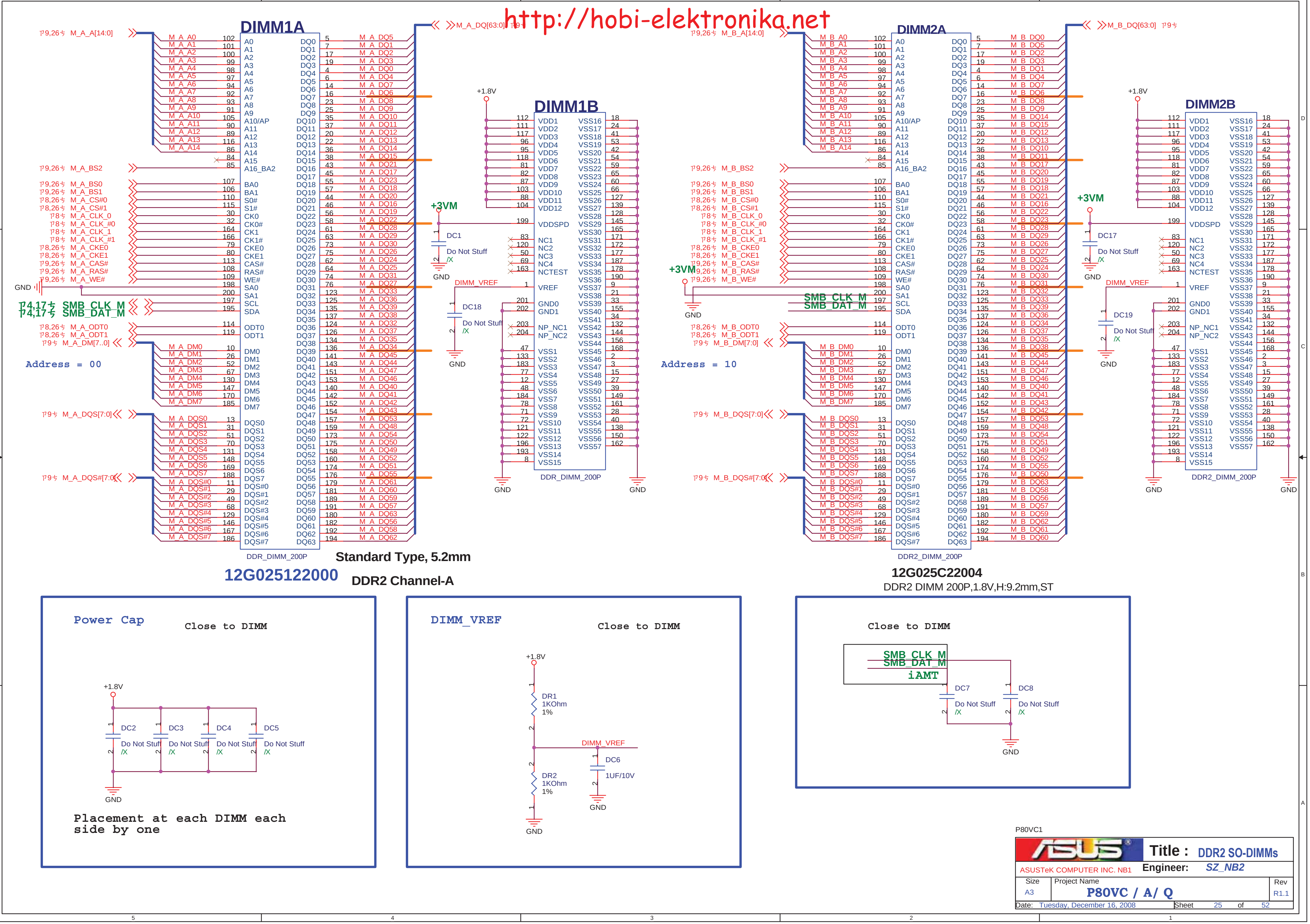
ASUSTeK COMPUTER INC. NB1

Title :

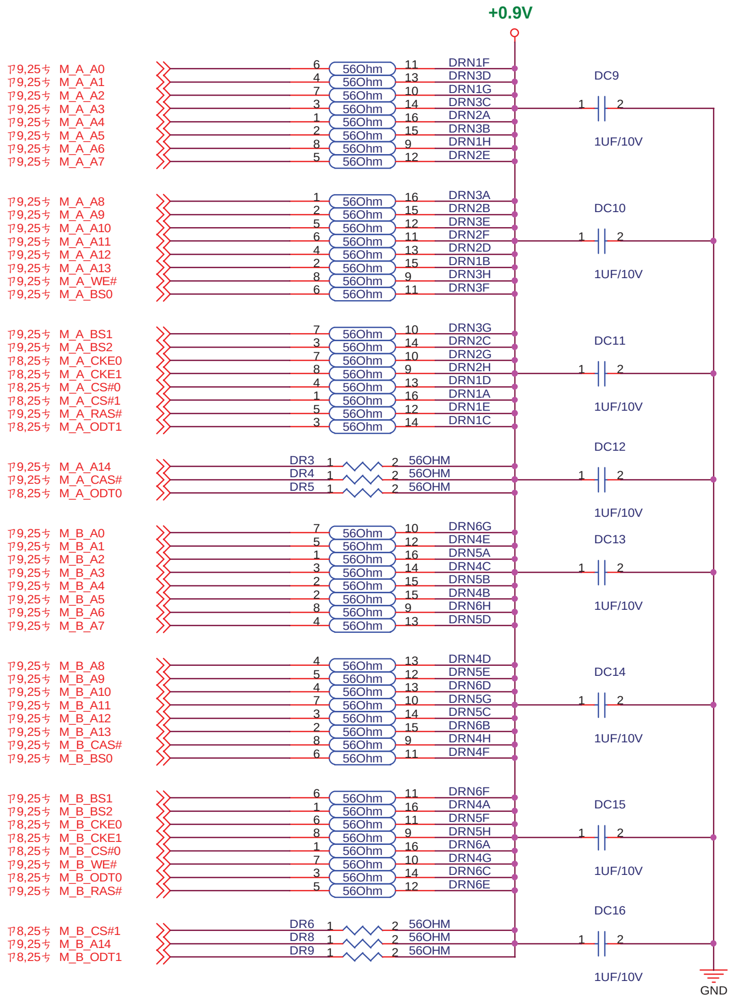
Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 24 of 52


http://hobi-elektronika.net
DIMM1A
DIMM1B
DIMM2A
DIMM2B
M_A_A[14:0]
M_A_DQ[63:0]
M_B_A[14:0]
M_B_DQ[63:0]
SMB_CLK_M
SMB_DAT_M
Address = 00
Address = 10
+1.8V
+3VM
DIMM_VREF
GND
DC1
DC17
DC18
DC19
Do Not Stuff
DDR_DIMM_200P
DDR2_DIMM_200P
Standard Type, 5.2mm
12G025122000
DDR2 Channel-A
12G025C22004
DDR2 DIMM 200P,1.8V,H:9.2mm,ST
Power Cap
Close to DIMM
DC2
DC3
DC4
DC5
Placement at each DIMM each side by one
DIMM_VREF
DR1
1KOhm
1%
DR2
1KOhm
1%
DC6
1UF/10V
iAMT
DC7
DC8
P80VC1
Title : DDR2 SO-DIMMs
ASUSTeK COMPUTER INC. NB1
Engineer: SZ_NB2
Size A3
Project Name P80VC / A/ Q
Rev R1.1
Date: Tuesday, December 16, 2008
Sheet 25 of 52

http://hobi-elektronika.net



P80VC1

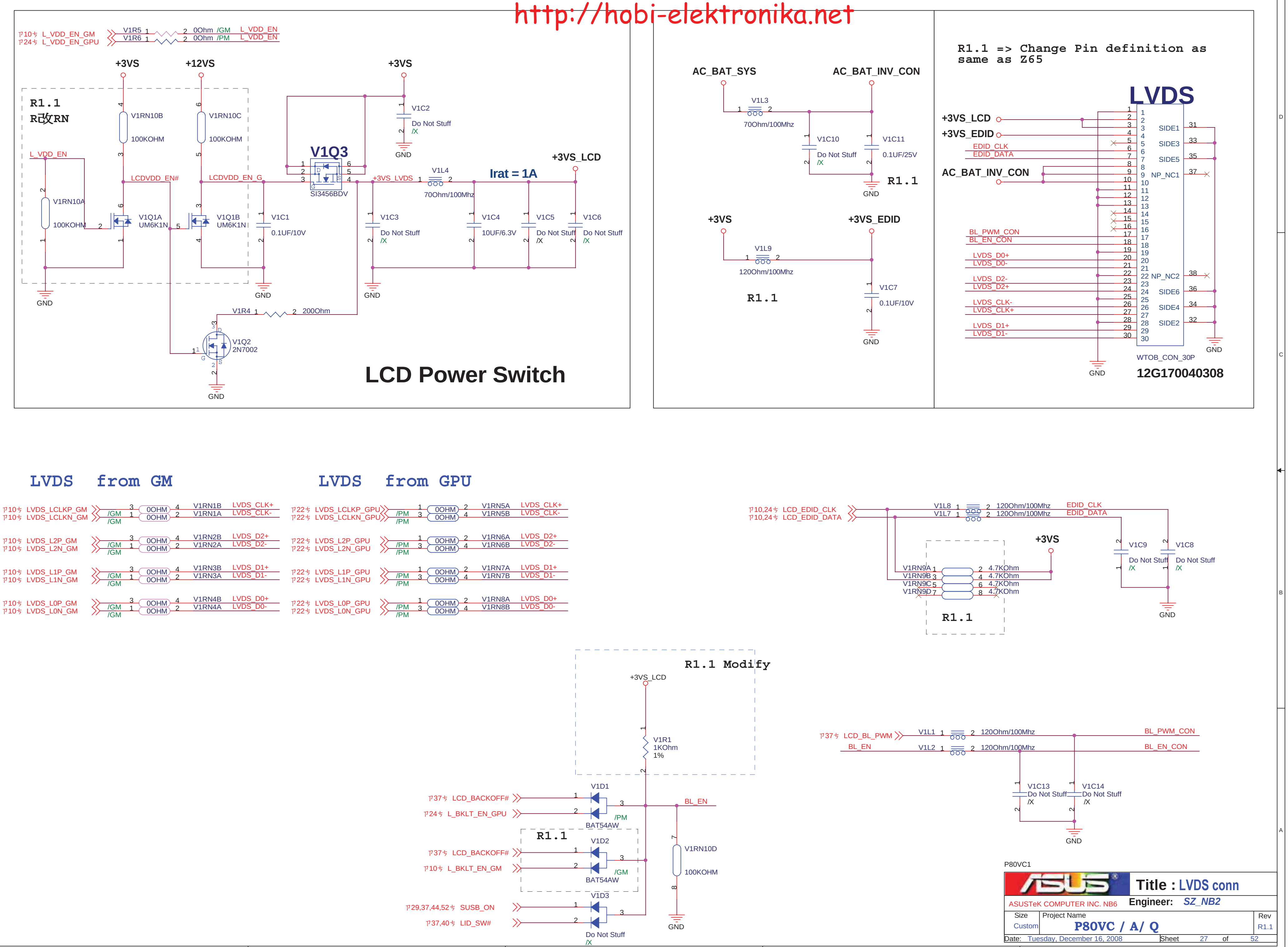
ASUSTeK COMPUTER INC. NB1

Title : DDR2 TERMINATION

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 26 of 52



P80VC1

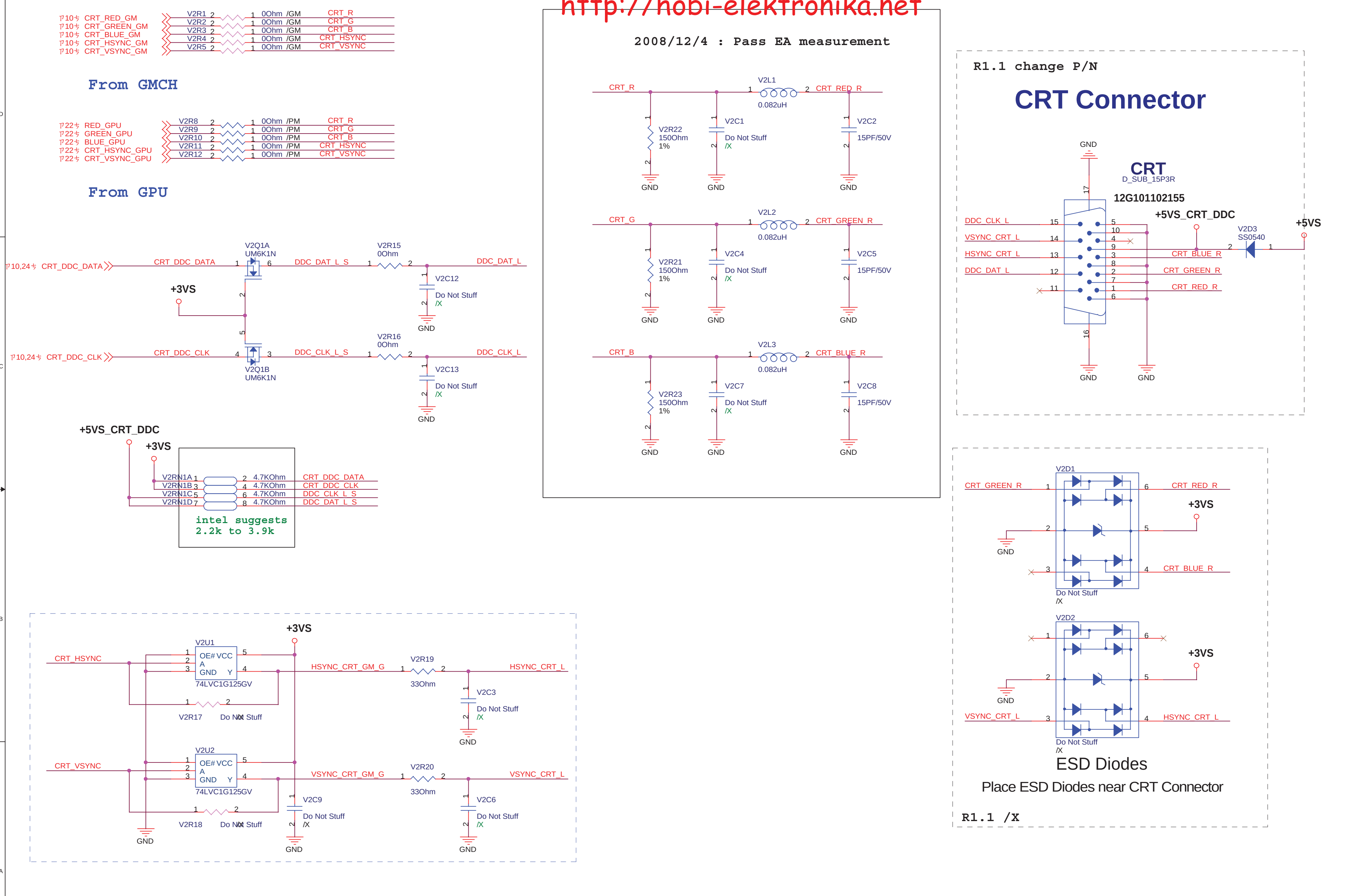
Title : LVDS conn

ASUSTeK COMPUTER INC. NB6

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

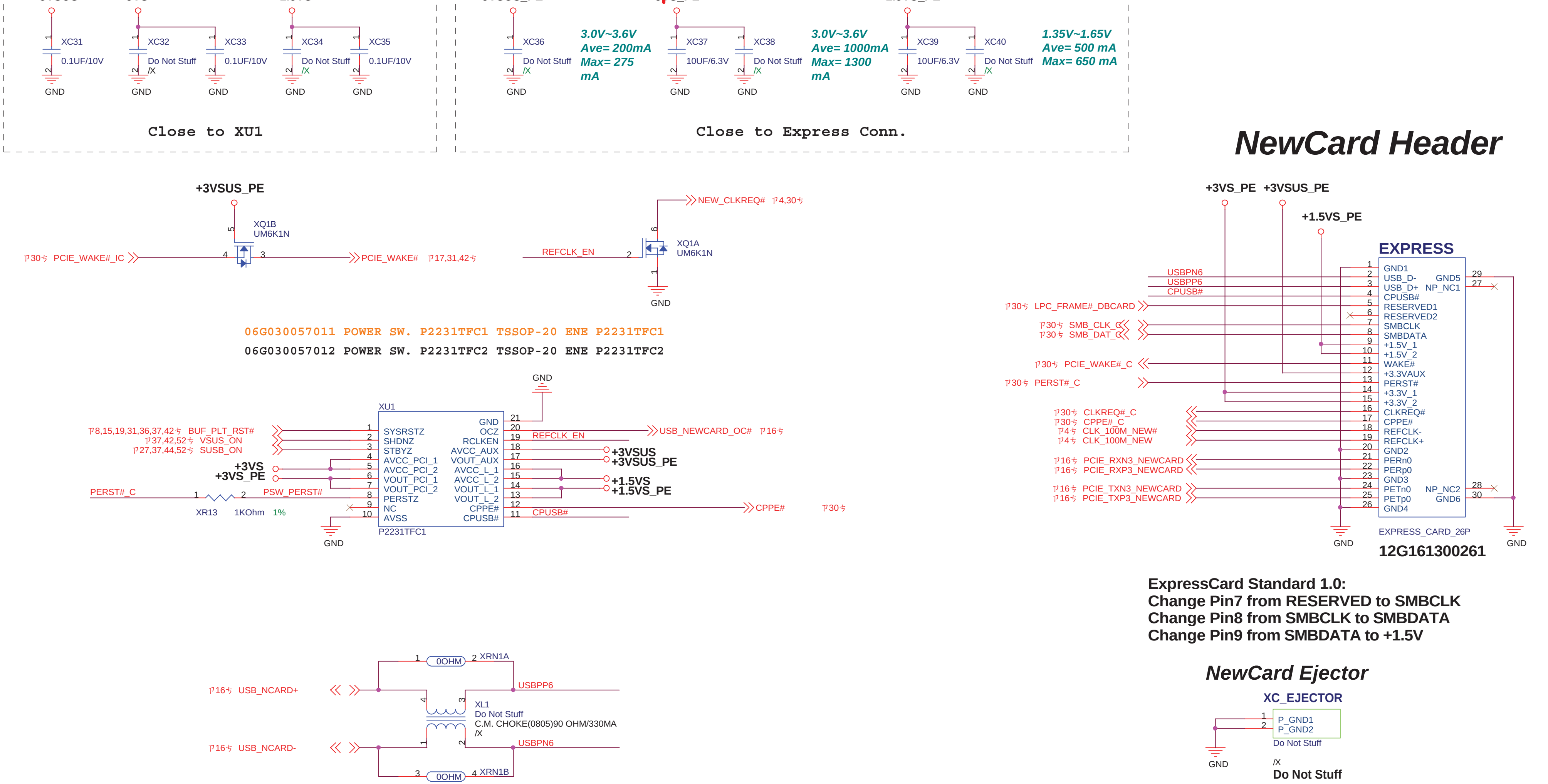
Date: Tuesday, December 16, 2008 Sheet 27 of 52



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : CRT conn	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 28 of 52	

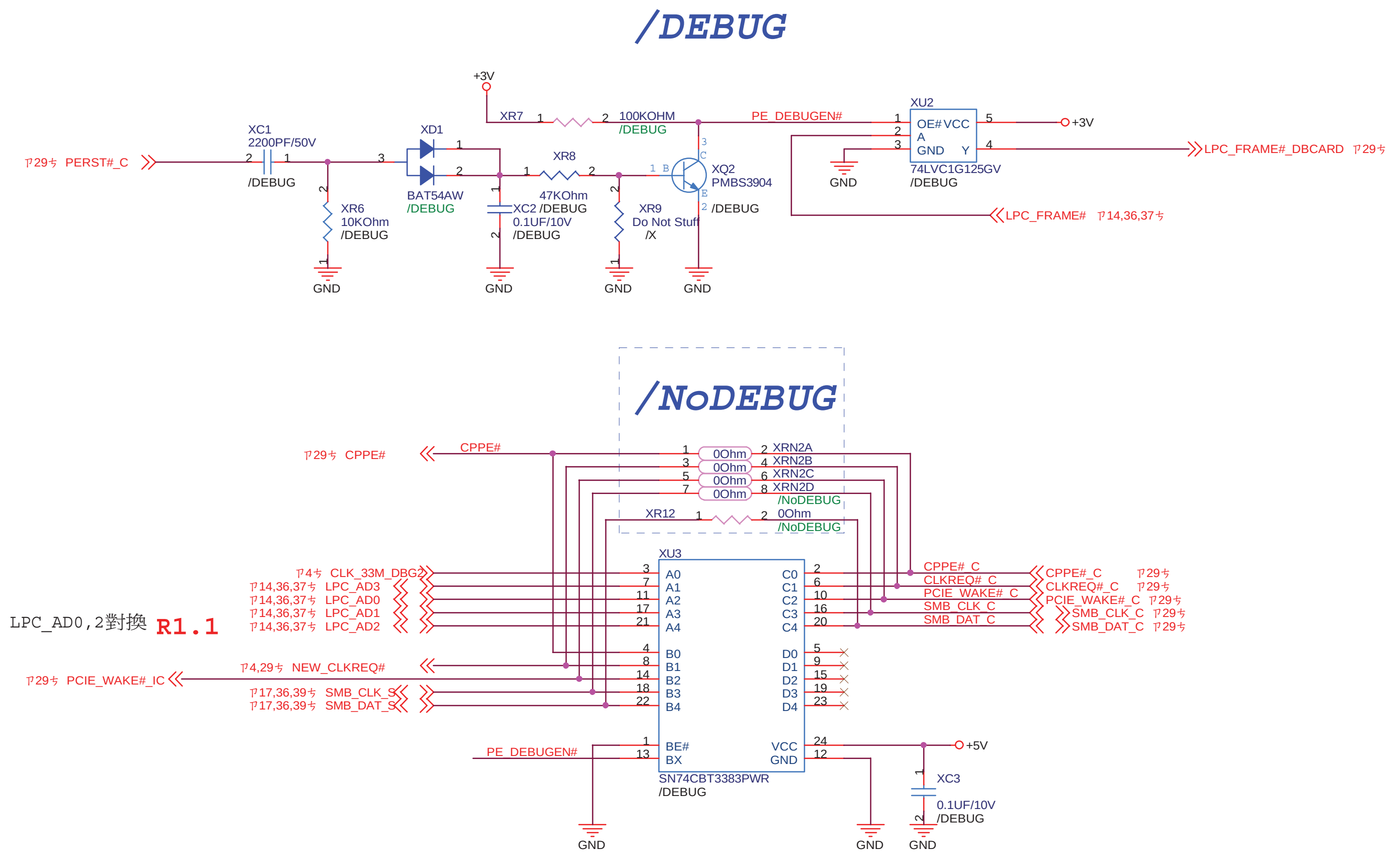
http://hobi-elektronika.net



P80VC1

ASUS	Title : NEWCARD		
ASUSTeK COMPUTER INC. NB6	Engineer: SZ_NB2		
Size: Custom	Project Name: P80VC / A/ Q		Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 29 of 52		

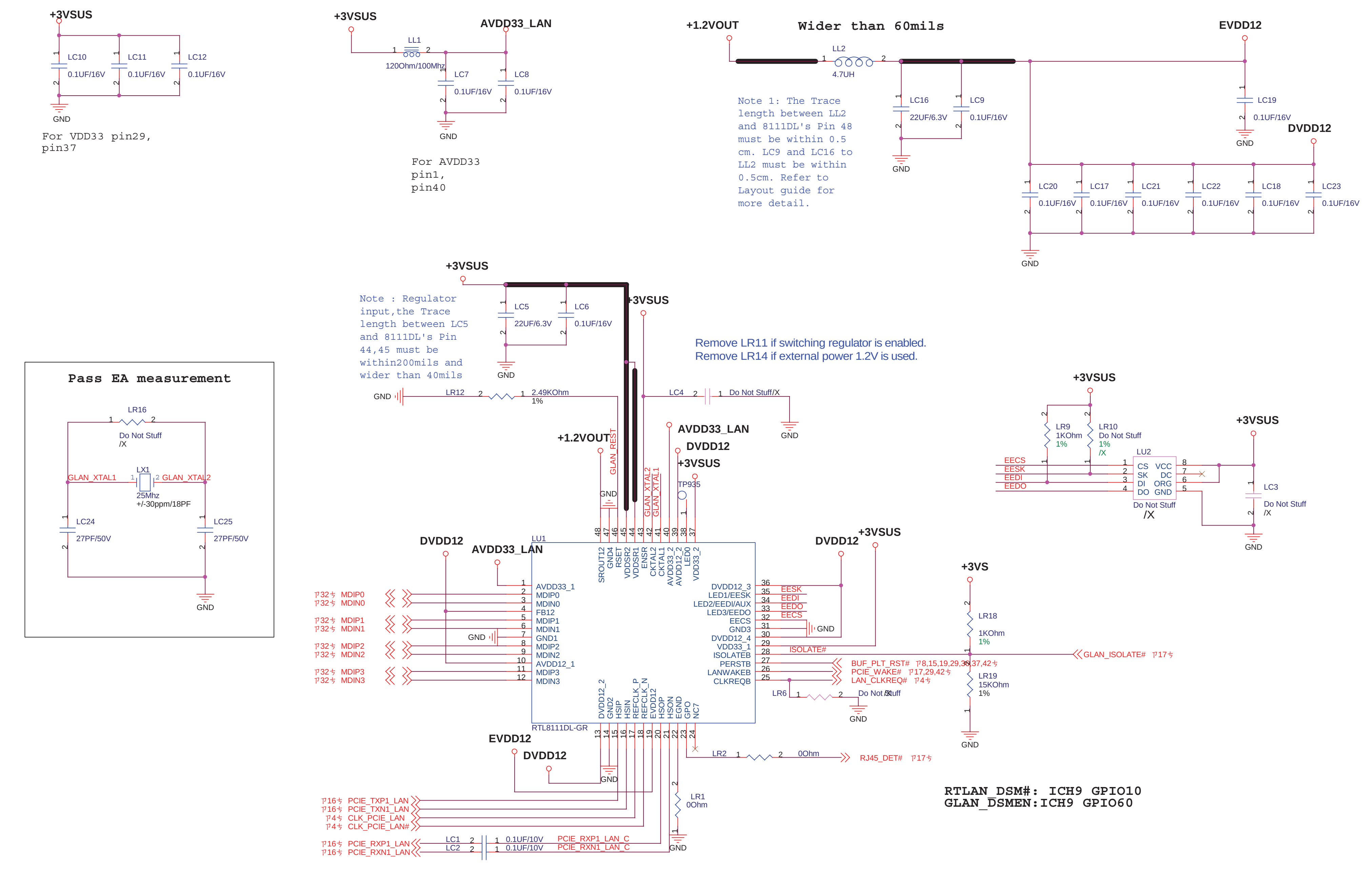
http://hobi-elektronika.net



If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (XRN2,XR12)

P80VC1

ASUS	Title : NEWCARD_DEBUG	
ASUSTeK COMPUTER INC. NB6	Engineer: SZ_NB2	
Size A3	Project Name P80VC / A/ Q	Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 30 of 52	



P80VC1

ASUS

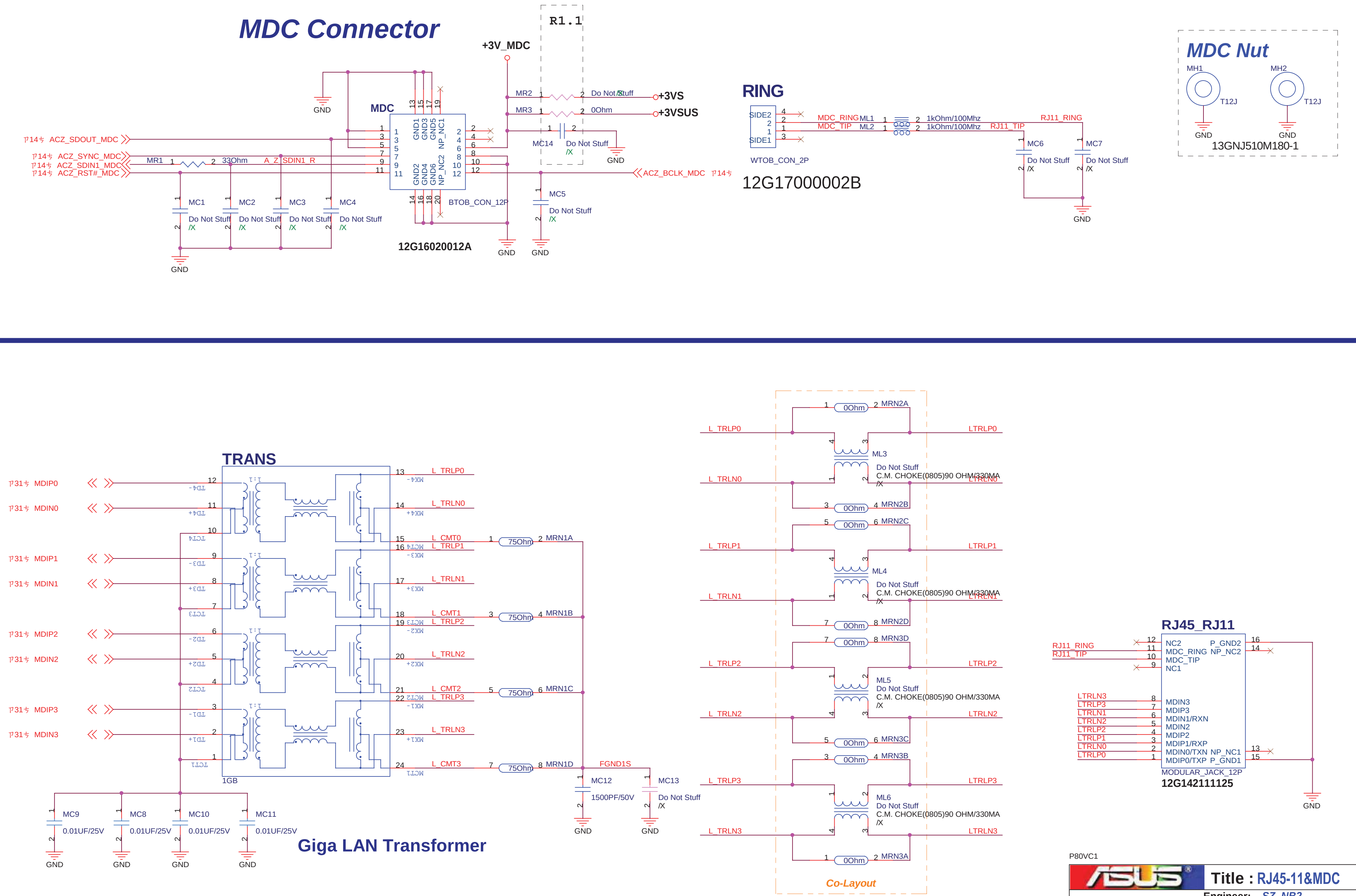
Title : SB-ICH9M(3)

ASUSTeK COMPUTER INC. NB1

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

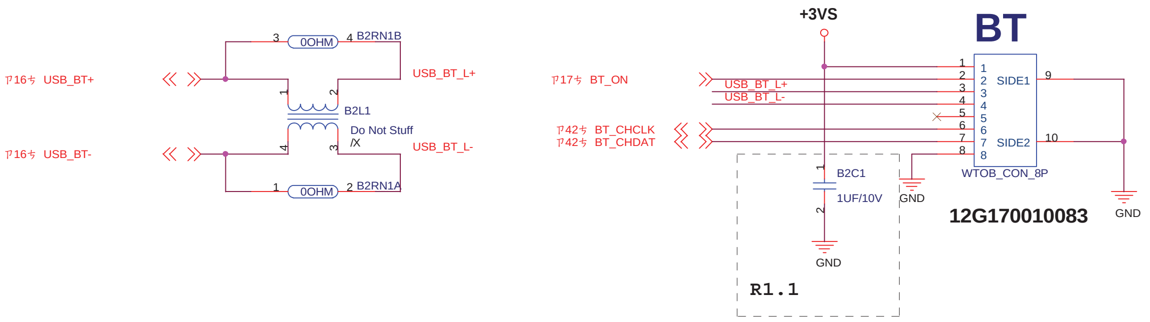
Date: Tuesday, December 16, 2008 Sheet 31 of 52



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : RJ45-11&MDC	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 32 of 52	

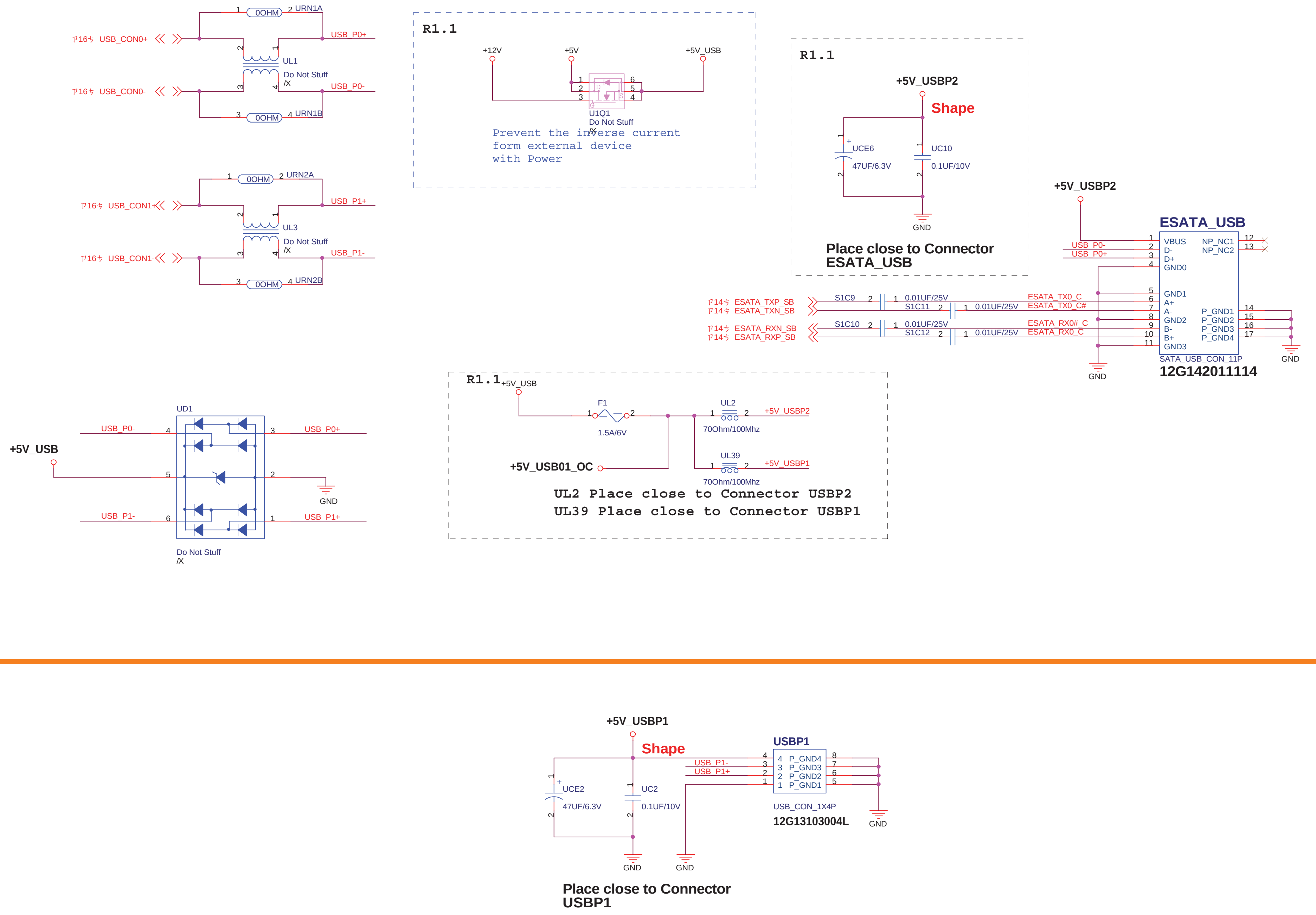
Bluetooth Connector



BT_ON : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled

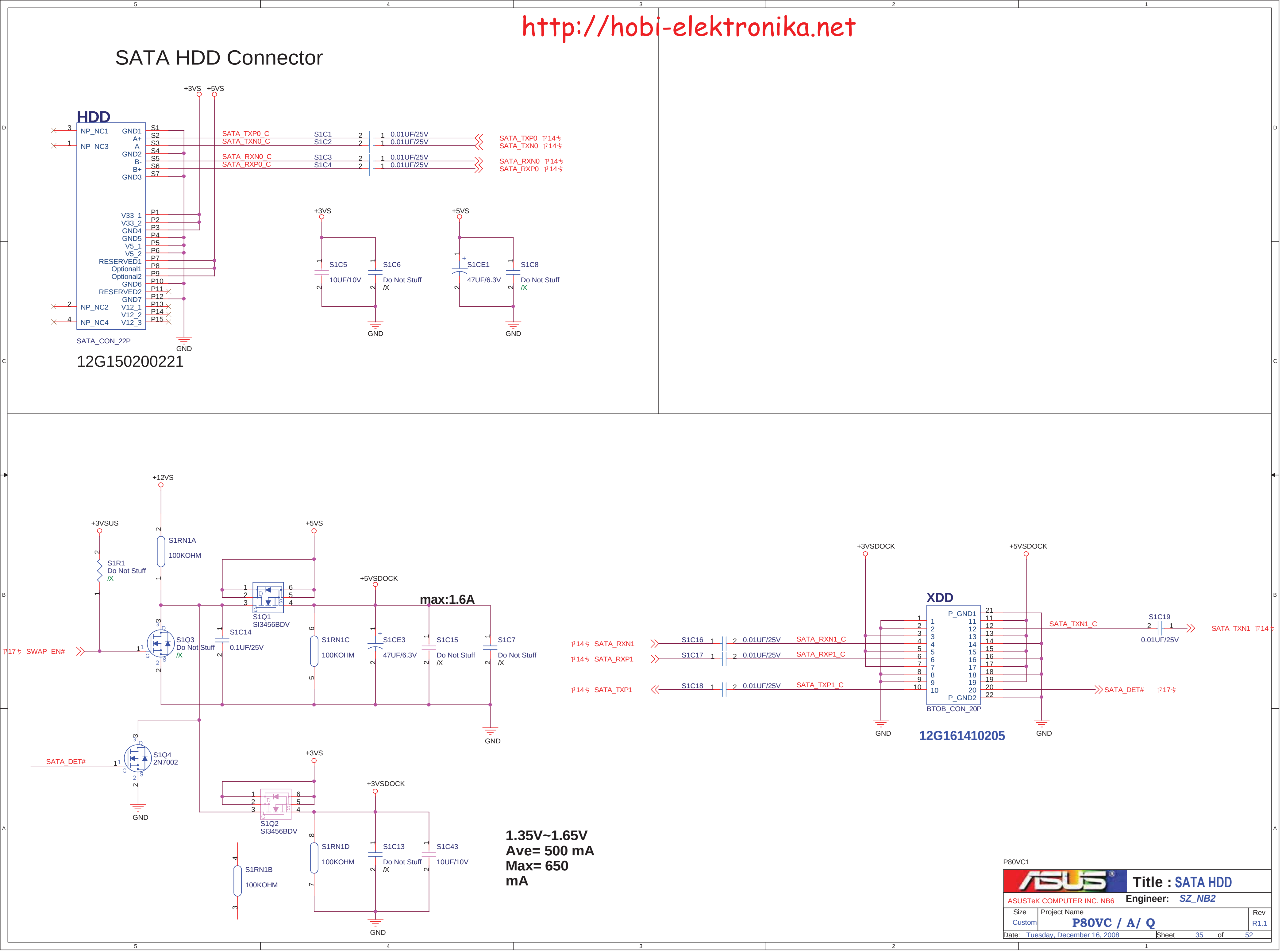
P80VC1

Title : BT&Launch	
ASUSTeK COMPUTER INC. NB6	Engineer: SZ_NB2
Size: Custom	Project Name: P80VC / A/ Q
Rev: R1.1	
Date: Tuesday, December 16, 2008	Sheet 33 of 52



P80VC1

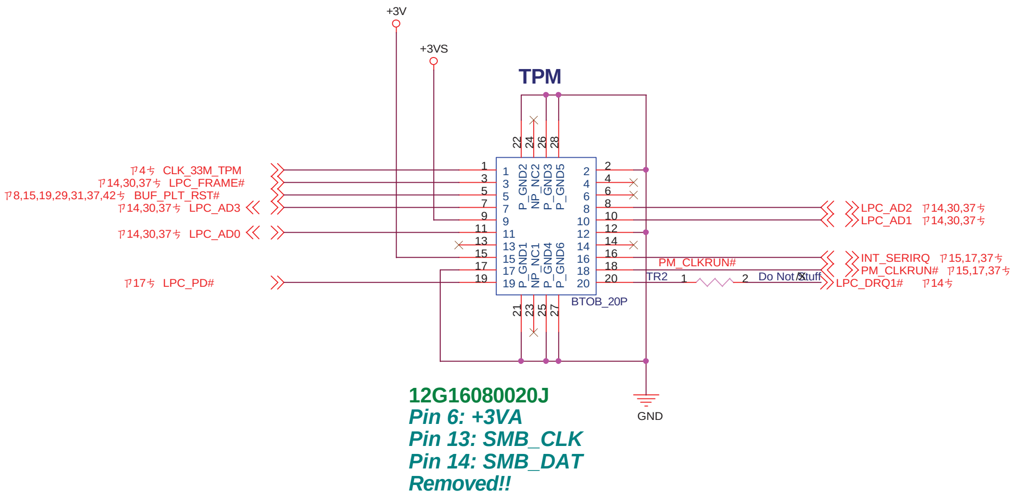
ASUSTeK COMPUTER INC. NB6	Title : Audio Brd con&USB x2
	Engineer: SZ_NB2
Size: Custom	Project Name: P80VC / A/ Q — Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 34 of 52



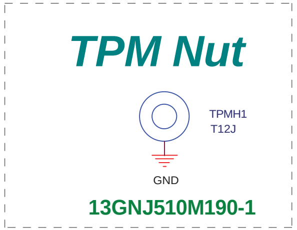
http://hobi-elektronika.net
SATA HDD Connector
HDD
NP_NC1
NP_NC3
GND1
A+
A-
GND2
B-
B+
GND3
V33_1
V33_2
GND4
GND5
V5_1
V5_2
RESERVED1
Optional1
Optional2
GND6
RESERVED2
GND7
NP_NC2
V12_1
V12_2
NP_NC4
V12_3
SATA_CON_22P
12G150200221
+3VS
+5VS
SATA_TXP0_C
SATA_TXN0_C
SATA_RXN0_C
SATA_RXP0_C
S1C1
S1C2
S1C3
S1C4
0.01UF/25V
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
S1C5
10UF/10V
S1C6
Do Not Stuff
/X
S1CE1
47UF/6.3V
S1C8
GND
+12VS
+3VSUS
S1R1
S1RN1A
100KOHM
S1Q3
SWAP_EN#
S1C14
0.1UF/25V
S1Q1
SI3456BDV
+5VSDOCK
max:1.6A
S1RN1C
S1CE3
S1C15
S1C7
SATA_DET#
S1Q4
2N7002
S1Q2
+3VSDOCK
S1RN1D
S1RN1B
S1C13
S1C43
1.35V~1.65V
Ave= 500 mA
Max= 650
mA
XDD
P_GND1
P_GND2
BTOB_CON_20P
12G161410205
SATA_RXN1
SATA_RXP1
SATA_TXP1
S1C16
S1C17
S1C18
SATA_RXN1_C
SATA_RXP1_C
SATA_TXP1_C
SATA_TXN1_C
S1C19
SATA_TXN1
P80VC1
Title : SATA HDD
ASUSTeK COMPUTER INC. NB6
Engineer: SZ_NB2
Size
Custom
Project Name
P80VC / A/ Q
Rev
R1.1
Date: Tuesday, December 16, 2008
Sheet 35 of 52

http://hobi-elektronika.net

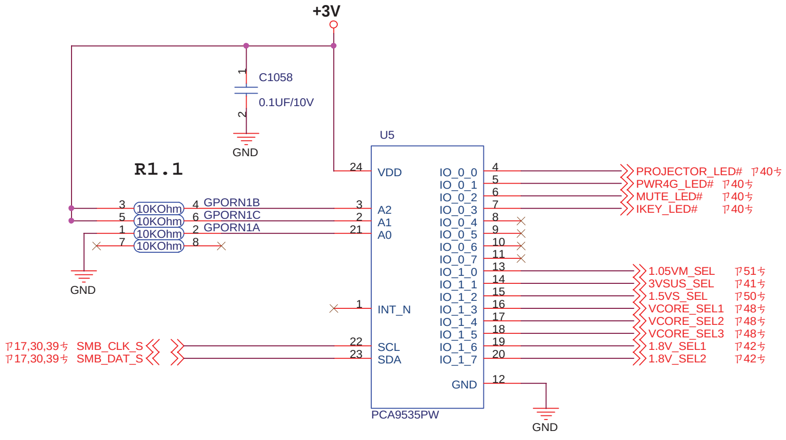
TPM Connector



TPM Nut

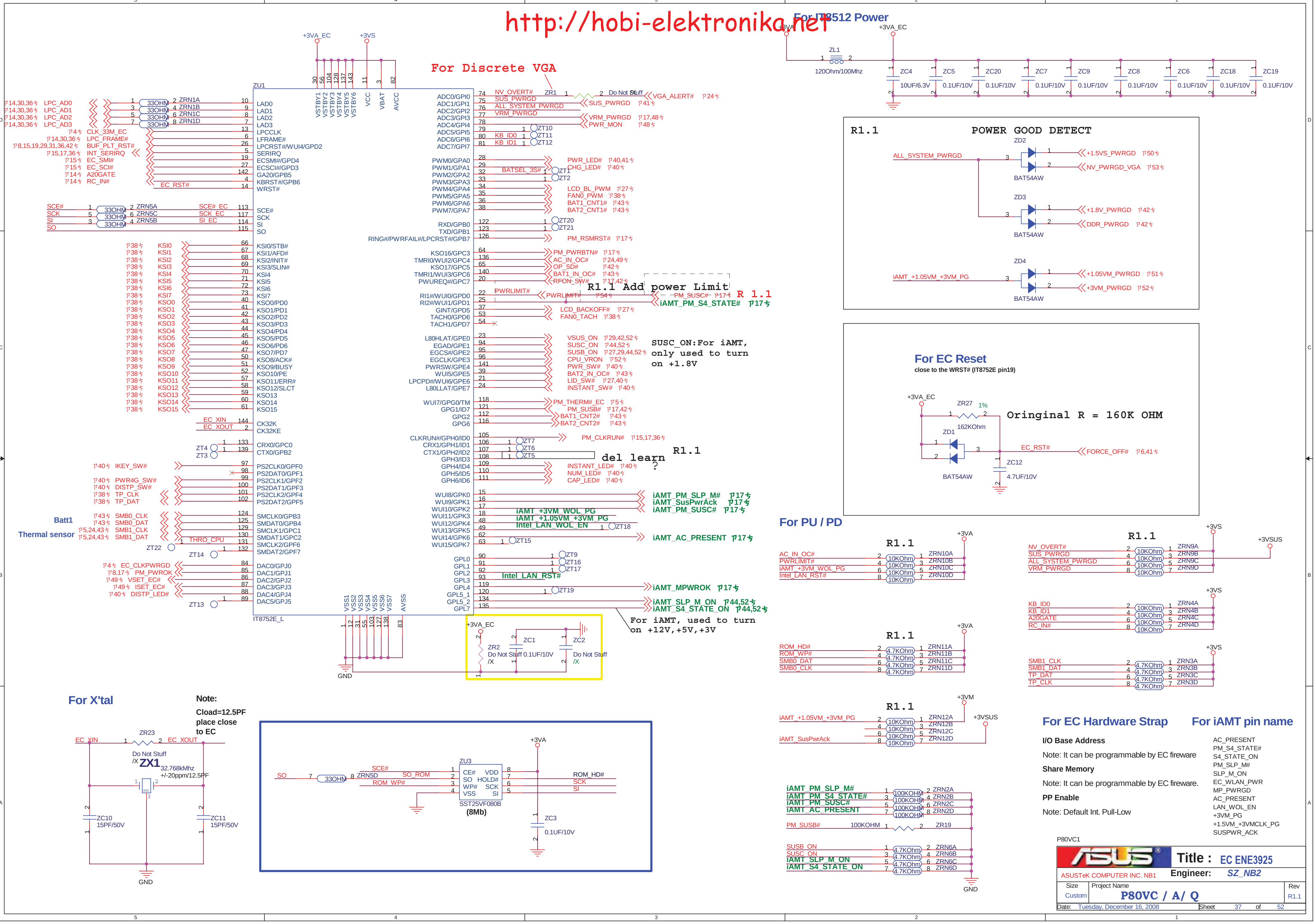


I2C GPIO Controller

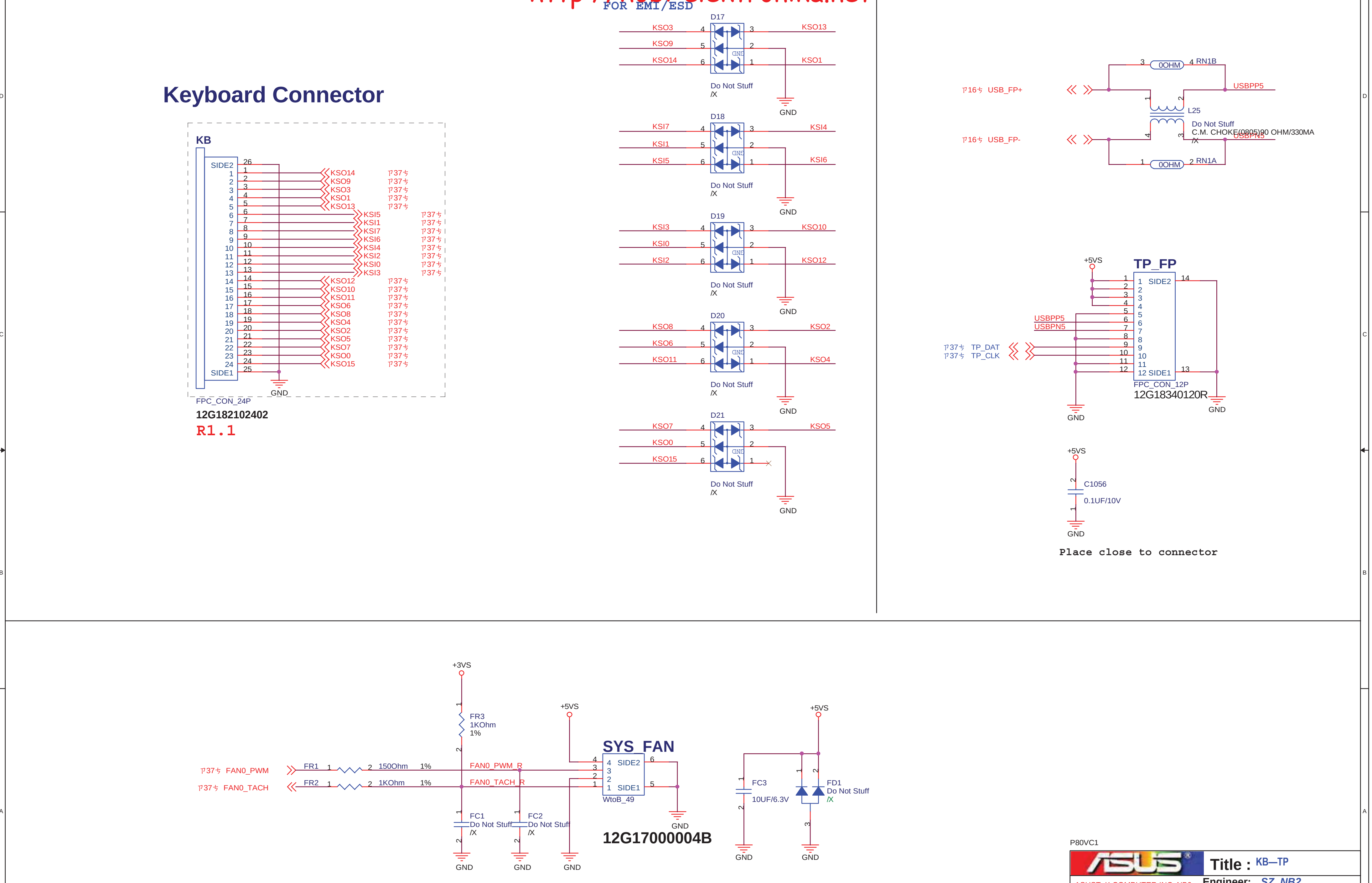


P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Debug&TPM&GPIO	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 36 of 52	


For IT8512 Power
For Discrete VGA
R1.1 POWER GOOD DETECT
BAT54AW
R1.1 Add power Limit
R 1.1
SUSC_ON:For iAMT, only used to turn on +1.8V
For EC Reset
close to the WRST# (IT8752E pin19)
Oringinal R = 160K OHM
del learn ?
R1.1
For iAMT, used to turn on +12V,+5V,+3V
IT8752E_L
Batt1
Thermal sensor
For PU / PD
For X'tal
Note:
Cload=12.5PF place close to EC
32.768kMhz +/-20ppm/12.5PF
SST25VF080B
(8Mb)
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
P80VC1
ASUSTeK COMPUTER INC. NB1
Title : EC ENE3925
Engineer: SZ_NB2
Size Custom
Project Name P80VC / A/ Q
Rev R1.1
Date: Tuesday, December 16, 2008
Sheet 37 of 52

Keyboard Connector



P80VC1

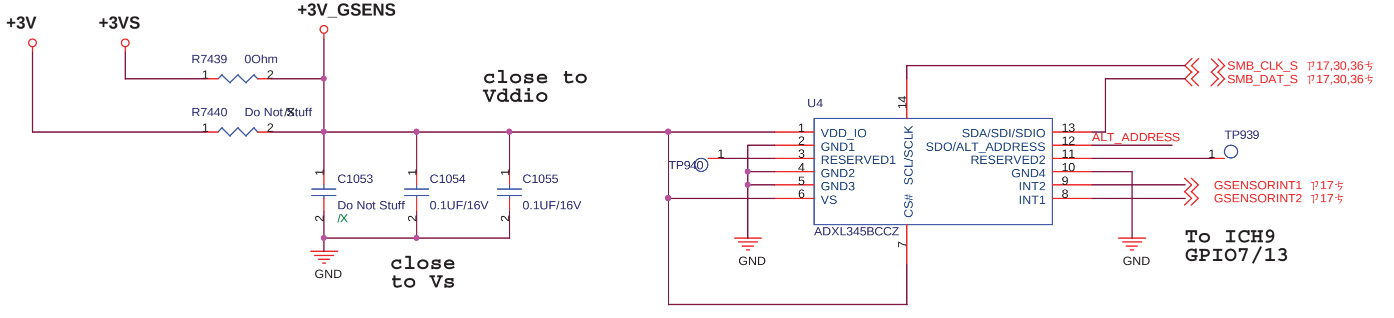
ASUSTeK COMPUTER INC. NB6

Title : KB—TP

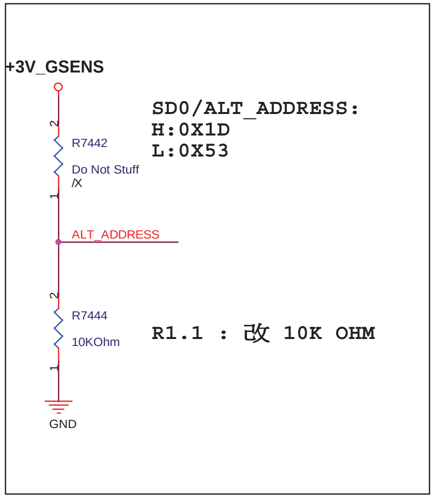
Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 38 of 52



RESERVED
PIN3: connect to Vs or NC
PIN11: connect to GND or NC
CS#: Tie to Vddio to enable I2C mode.



P80VC1

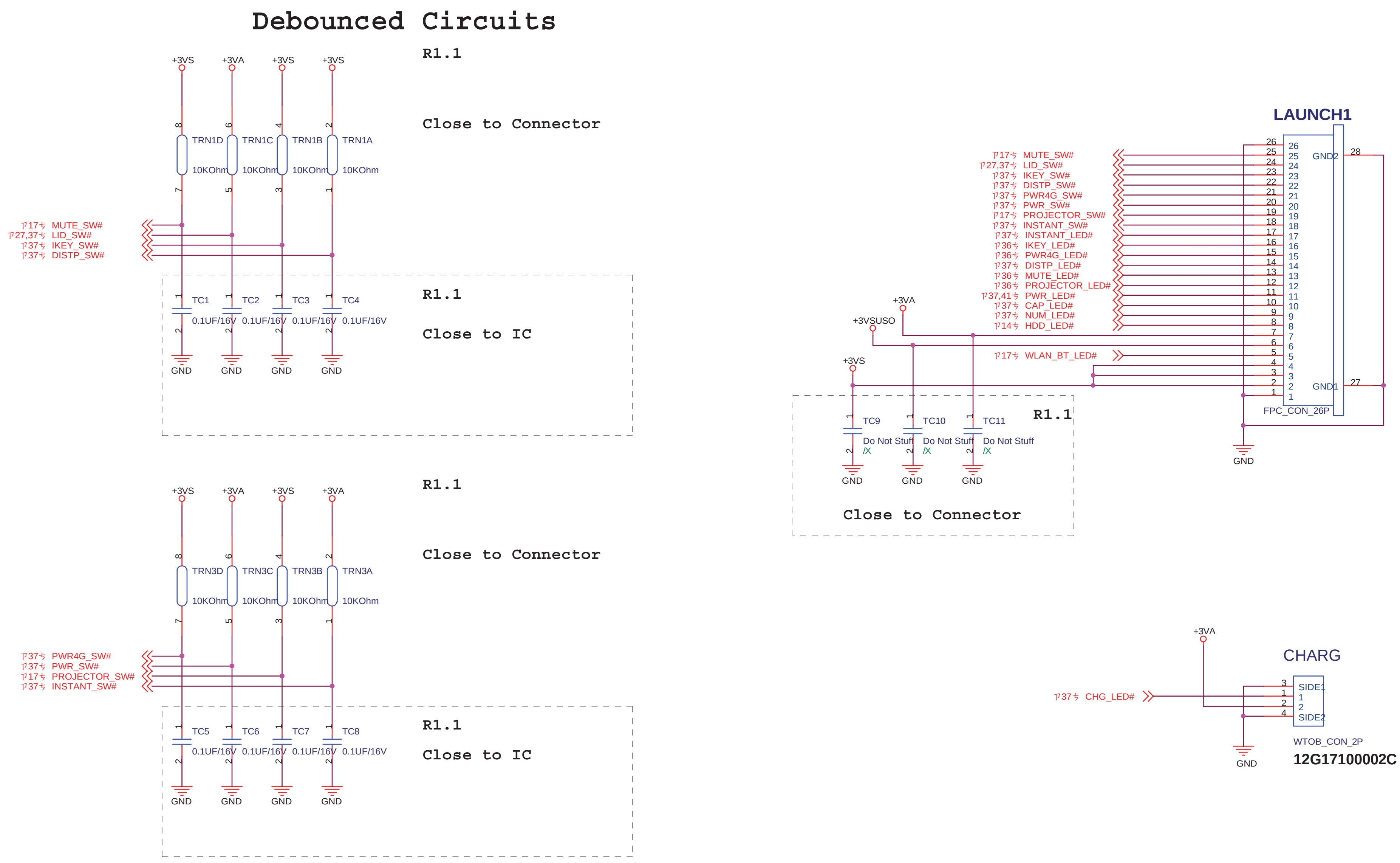
Title : Launch

ASUSTeK COMPUTER INC. NB6

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

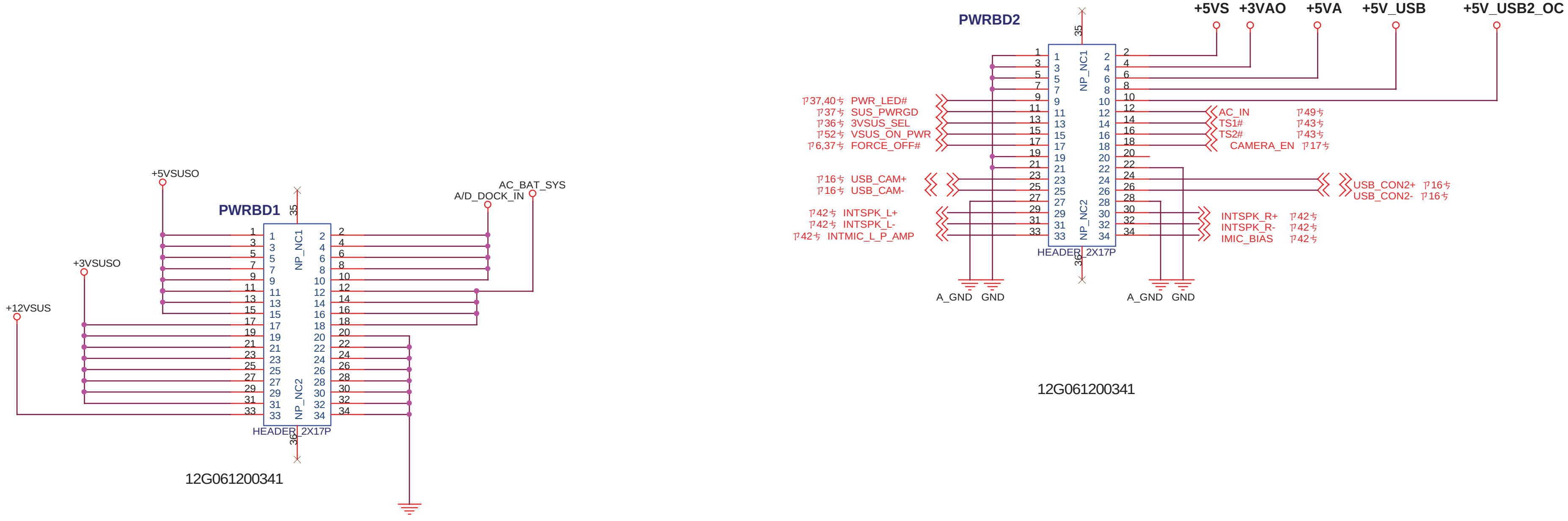
Date: Tuesday, December 16, 2008 Sheet 39 of 52



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Launch	
	Engineer: SZ_NB2	
Size A3	Project Name P80VC / A/ Q	Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 40 of 52	

http://hobi-elektronika.net



P80VC1

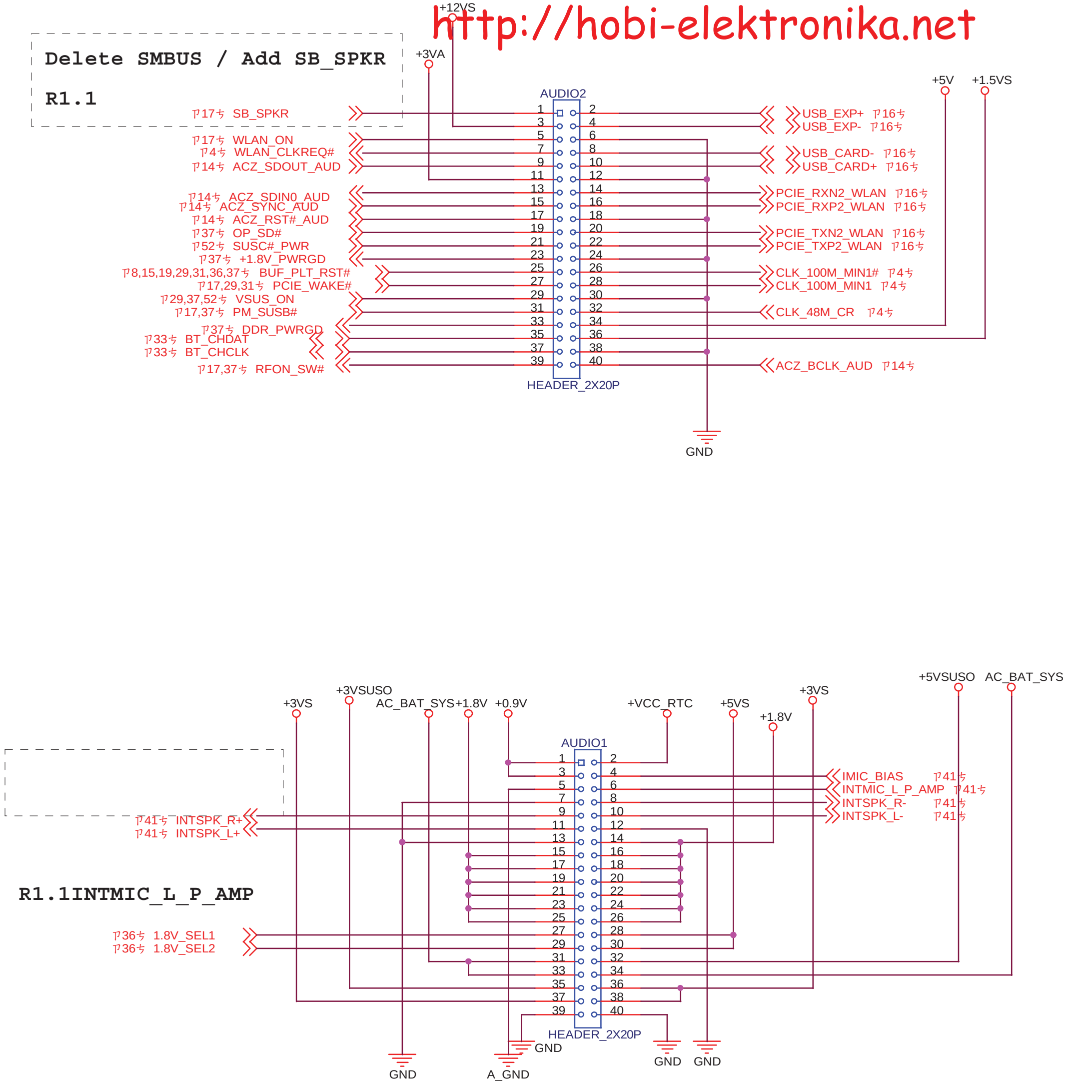
Title : other

ASUSTeK COMPUTER INC. NB6

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 41 of 52



P80VC1

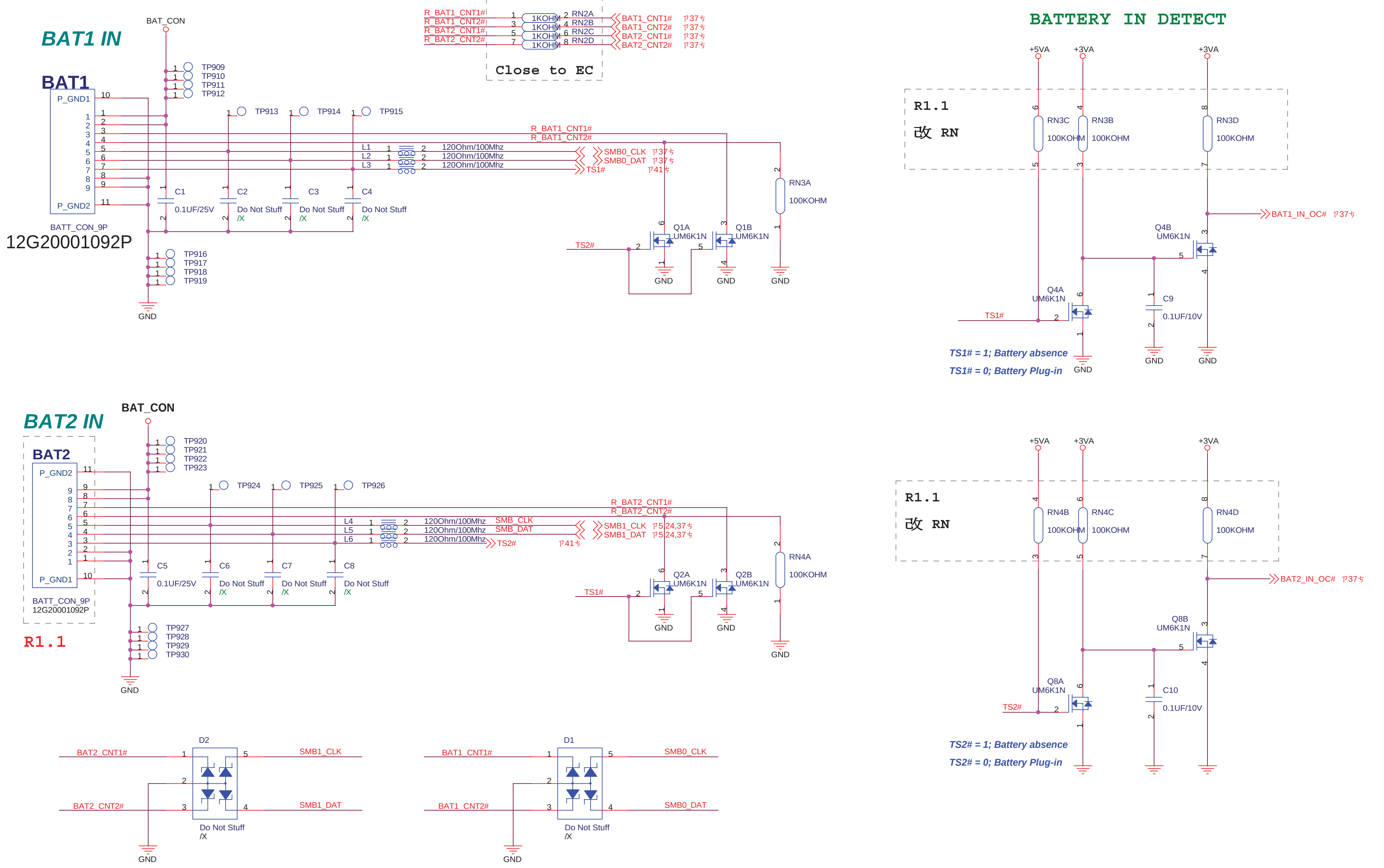
ASUSTeK COMPUTER INC. NB6

Title : other

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 42 of 52



P80VC1

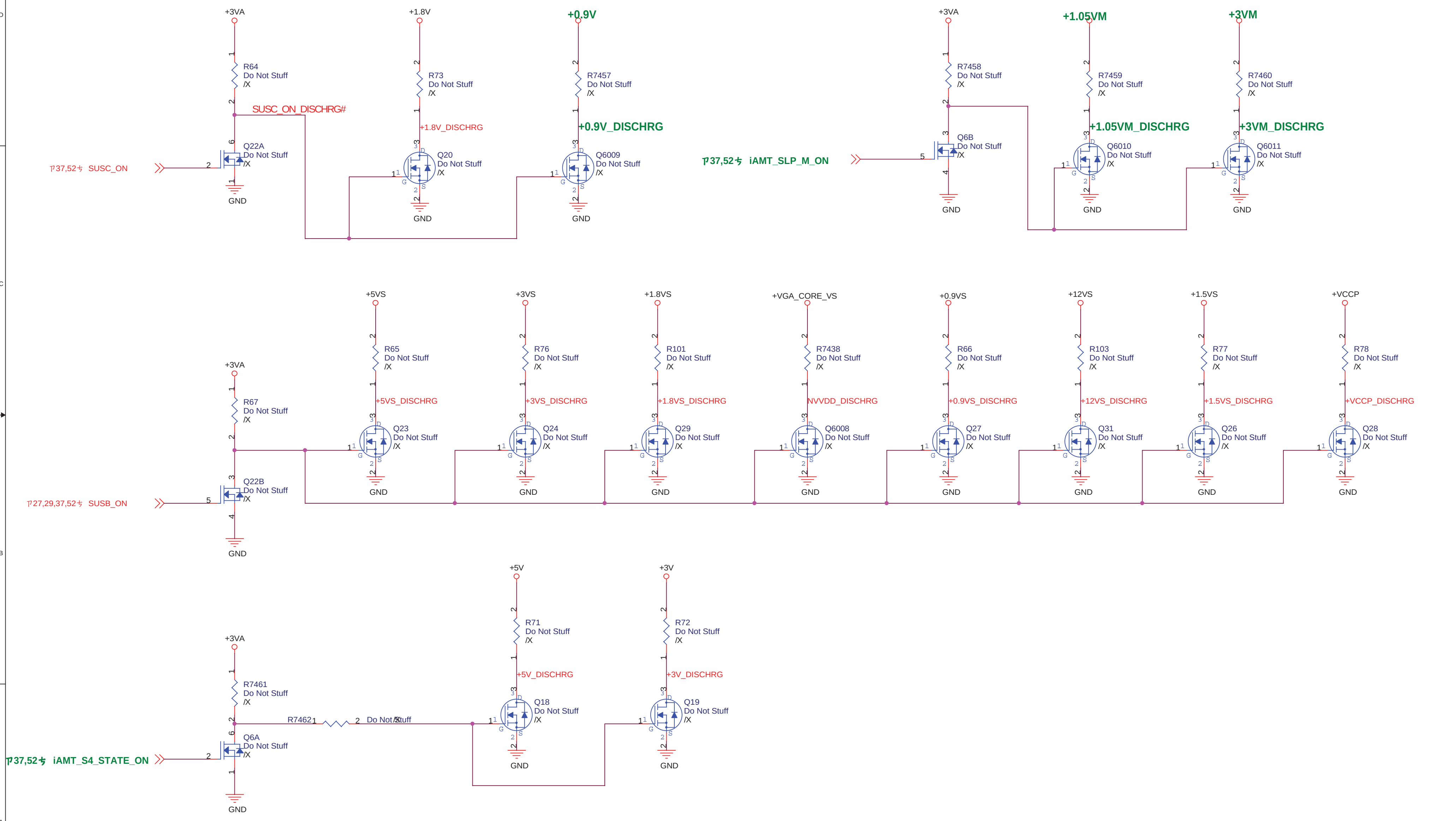
ASUSTeK COMPUTER INC. NB6

Title : DC-IN&BAT-IN

Engineer: SZ_NB2

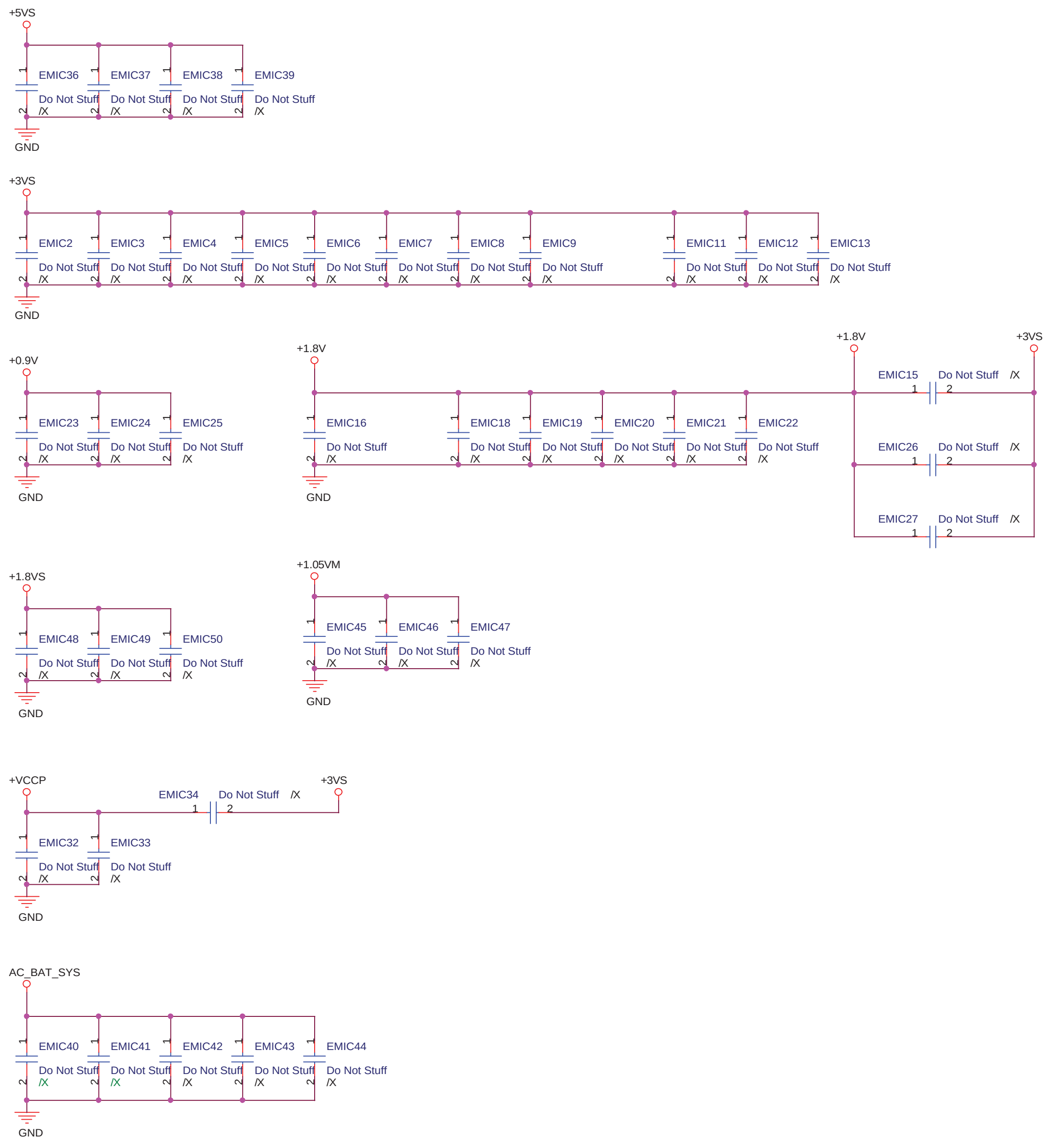
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 43 of 52



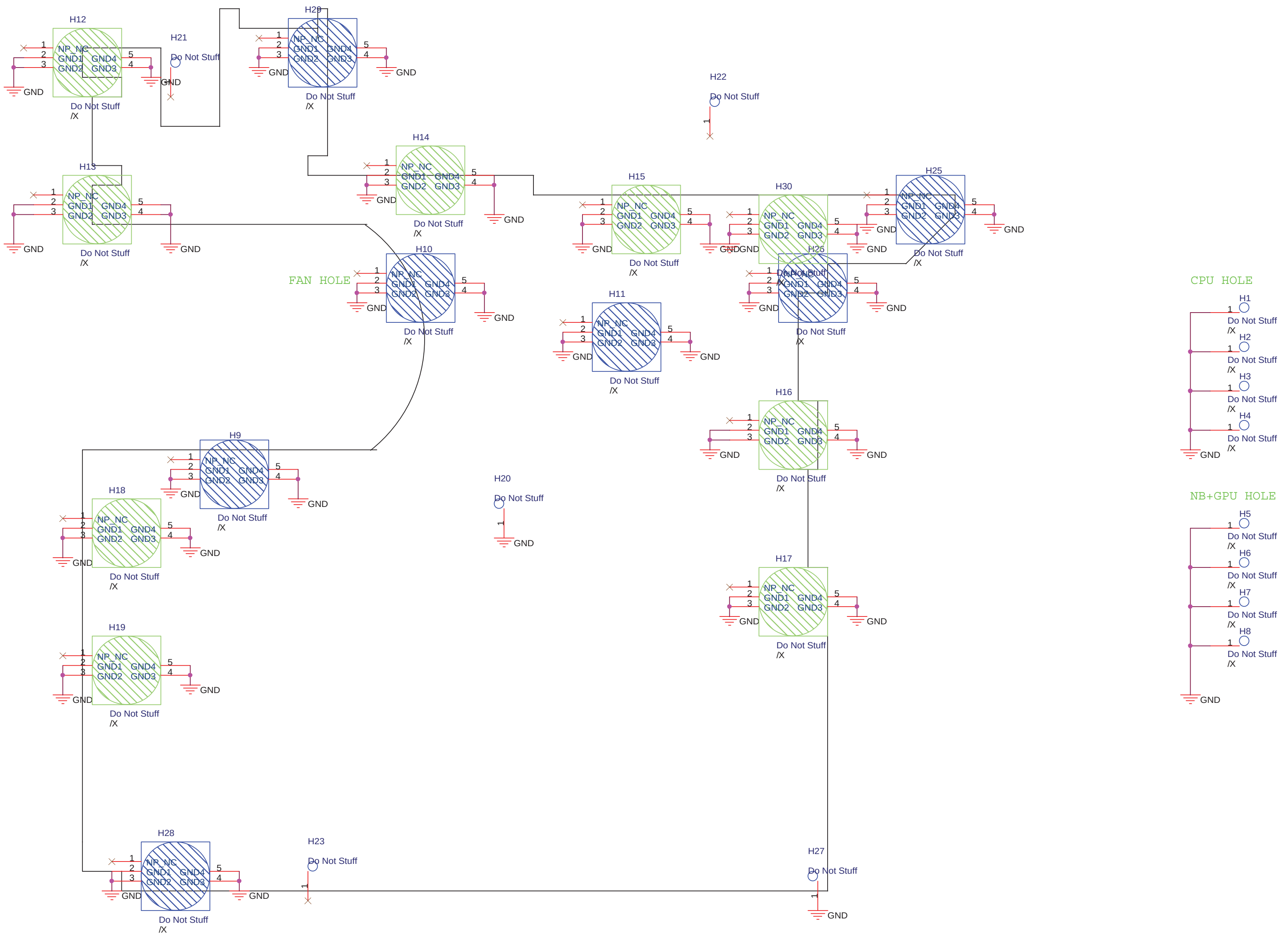
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Discharger	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 44 of 52	



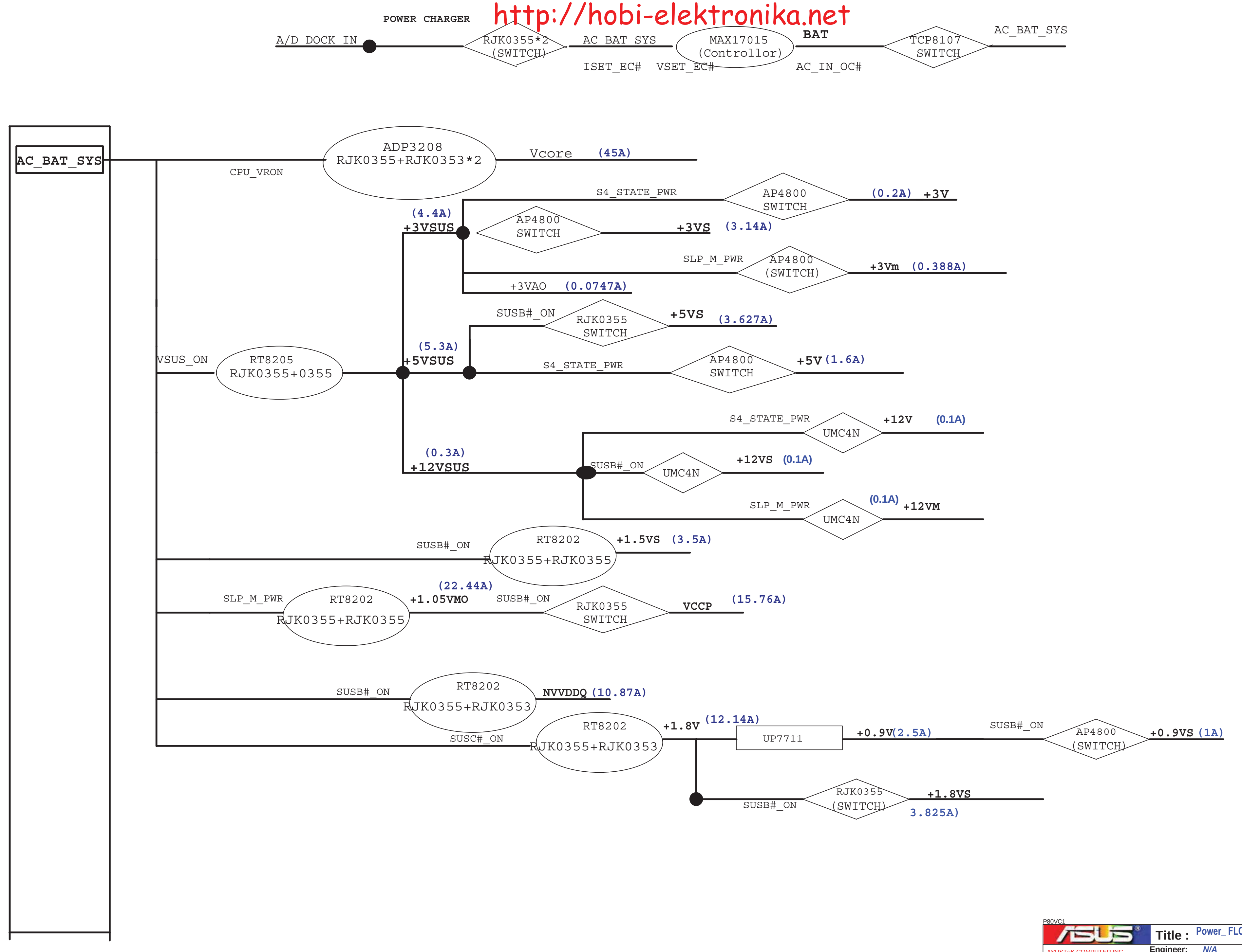
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : EMI CAP	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 45 of 52	



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Screw Hole	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 46 of 52	



P80VC1

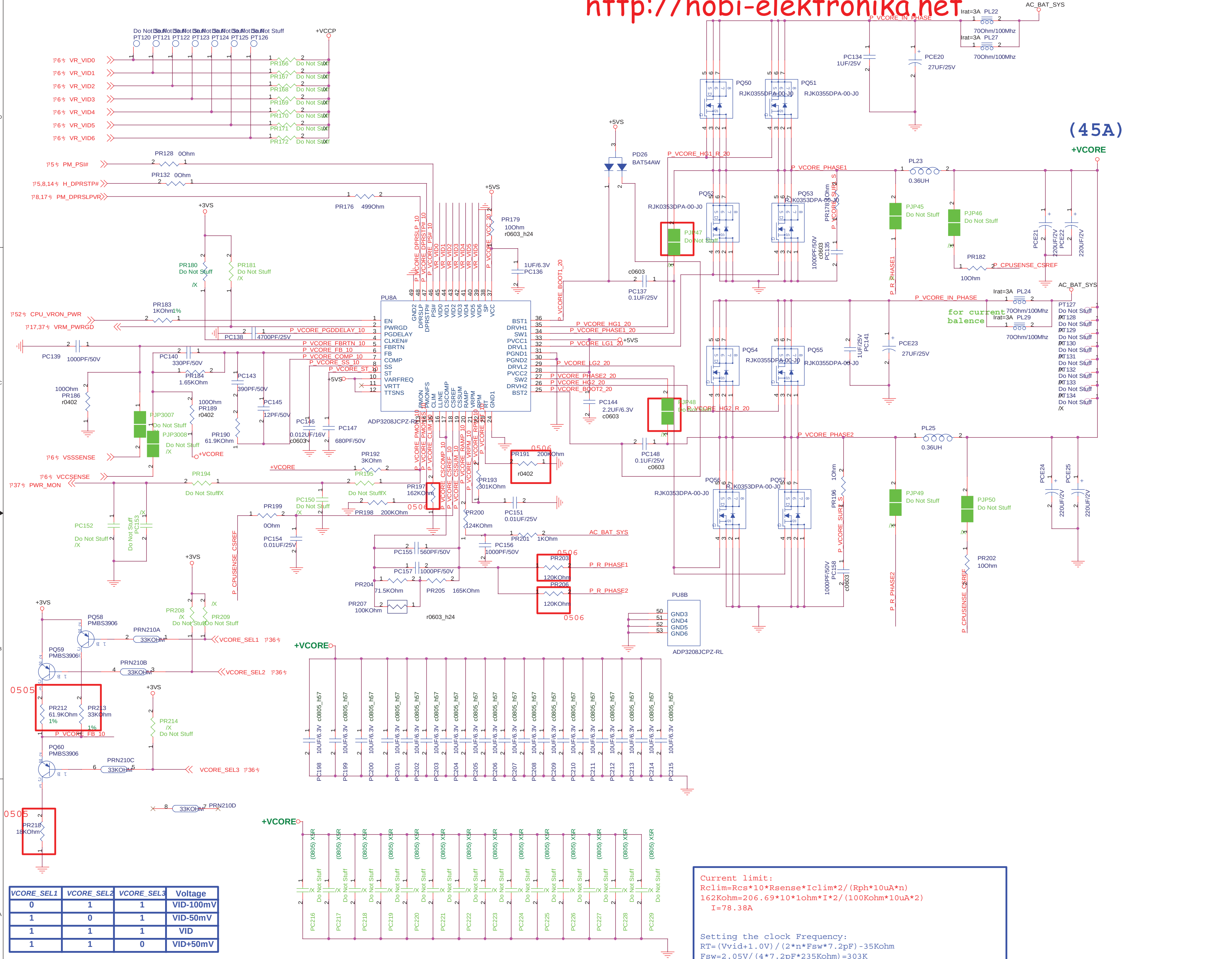
ASUSTeK COMPUTER INC

Title : Power_ FLOW

Engineer: N/A

Size	Project Name	Rev
C	P80M	1.1

Date: Tuesday, December 16, 2008 Sheet 47 of 54



VCORE_SEL1	VCORE_SEL2	VCORE_SEL3	Voltage
0	1	1	VID-100mV
1	0	1	VID-50mV
1	1	1	VID
1	1	0	VID+50mV

Power stage

1. I/P Current:

I in = Vo*Io/(0.75 * Vin) =1.33 A

2. Ripple Current:

Iripple=3A

3. Ripple Voltage:

Vripple=Iripple*ESR=13.5mV

4. Dynamic:

Ipeak=45A
ESR=4.5mohm
V=100mV

5. Inductor Spec:

Isat=26A
Idc=20.8A
Rdcmax=1.09mOhm
Rdcmtyp=1.02mOhm

6. MOSFET Spec:

H-side and L-side MOSFET:RJK0355/RJK0353
Rds(on)=11.8/5.4mOhm (Vgs=4.5V)
Icont=30/35A (T=25)/
Ipeak=120/140A (Pause<10us)

Controller

1. Voltage & Current:

+VCORE:1.1V/45A

2. Frequency:

Setting the clock Frequency:
RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
Fsw=2.05V/(4*7.2pF*235Kohm)=303K

3. OCP:

DCR*Imax*R2/(R1+R2)=22.5mV
Imax=10.87A

4. tss time:

TSS=1.8ms TSt=1.8ms

5.LoadLine:

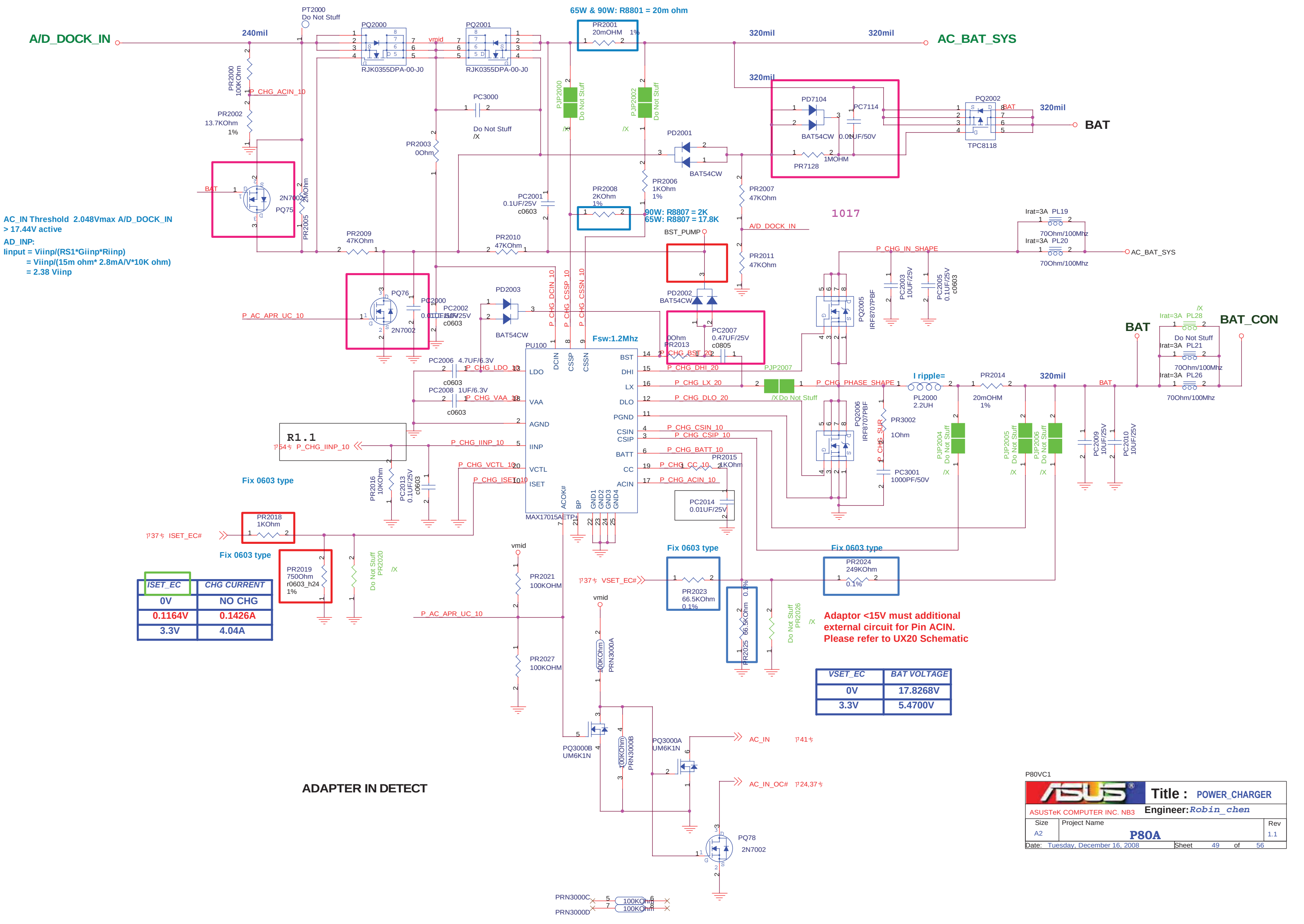
Out Droop Resistance :
Ro=Rcs*Rsense/Rph
=206.69Kohm*1.02mohm/120Kohm=1.76mohm

```
Current limit:
Rclim=Rcs*10*Rsense*Iclim*2/(Rph*10uA*n)
162Kohm=206.69*10*1ohm*I*2/(100Kohm*10uA*2)
  I=78.38A

Setting the clock Frequency:
RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
Fsw=2.05V/(4*7.2pF*235Kohm)=303K

Out Droop Resistance :
Ro=Rcs*Rsense/Rph
=206.69Kohm*1mohm/100Kohm=2.07mohm
```

P80VC1

Title :	POWER_VCORE
ASUSTek Computer INC.	Engineer: Robin_chen
Size: A2	Project Name: P80 · Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 48 of 56

POWER PATH & BAT_LEARN



AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active
AD_INP:
Iinput = Viinp/(RS1*Giinp*Riinp)
= Viinp/(15m ohm* 2.8mA/V*10K ohm)
= 2.38 Viinp

ISET_EC	CHG CURRENT
0V	NO CHG
0.1164V	0.1426A
3.3V	4.04A

VSET_EC	BAT VOLTAGE
0V	17.8268V
3.3V	5.4700V

ADAPTER IN DETECT

Power stage

1. Ripple Current:
   Iripple=3A
2. Inductor Spec:
   Isat=14A
   Idc=8A
   DCR=18mOhm
3. MOSFET Spec:
   H-side and L-side MOSFET:AP4800
   Rds(on)=21mOhm (Vgs=4.5V)
   Icont=9.6 (T=25)
   Ipeak=40 (Pause<10us)

Controller

1. Frequency:
   1.2MHZ
2. Current limit
   4.5A(90W)
   3.16A(65W)

P80VC1

ASUSTeK COMPUTER INC. NB3

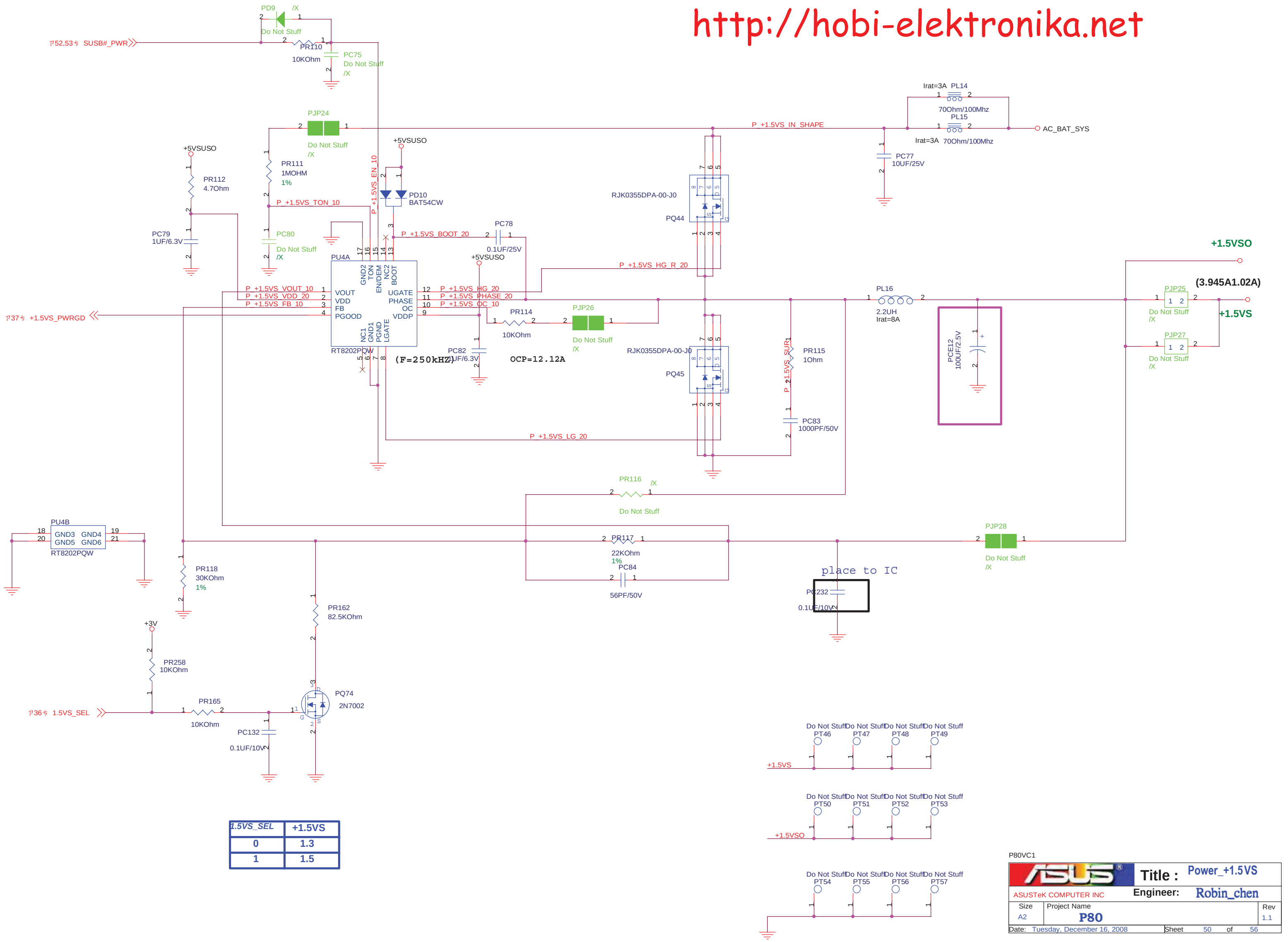
Title : POWER_CHARGER

Engineer: Robin_chen

Size	Project Name	Rev
A2	P80A	1.1

Date: Tuesday, December 16, 2008 Sheet 49 of 56

http://hobi-elektronika.net



1.5VS_SEL	+1.5VS
0	1.3
1	1.5

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.368A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=3.503A
   ESR/2=4.5mohm
   V=14.18mV
4. Inductor Spec:
   Isat=14A
   Idc=8A
   DCR=18mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30 (T=25)
   Ipeak=120 (Pause<10us)

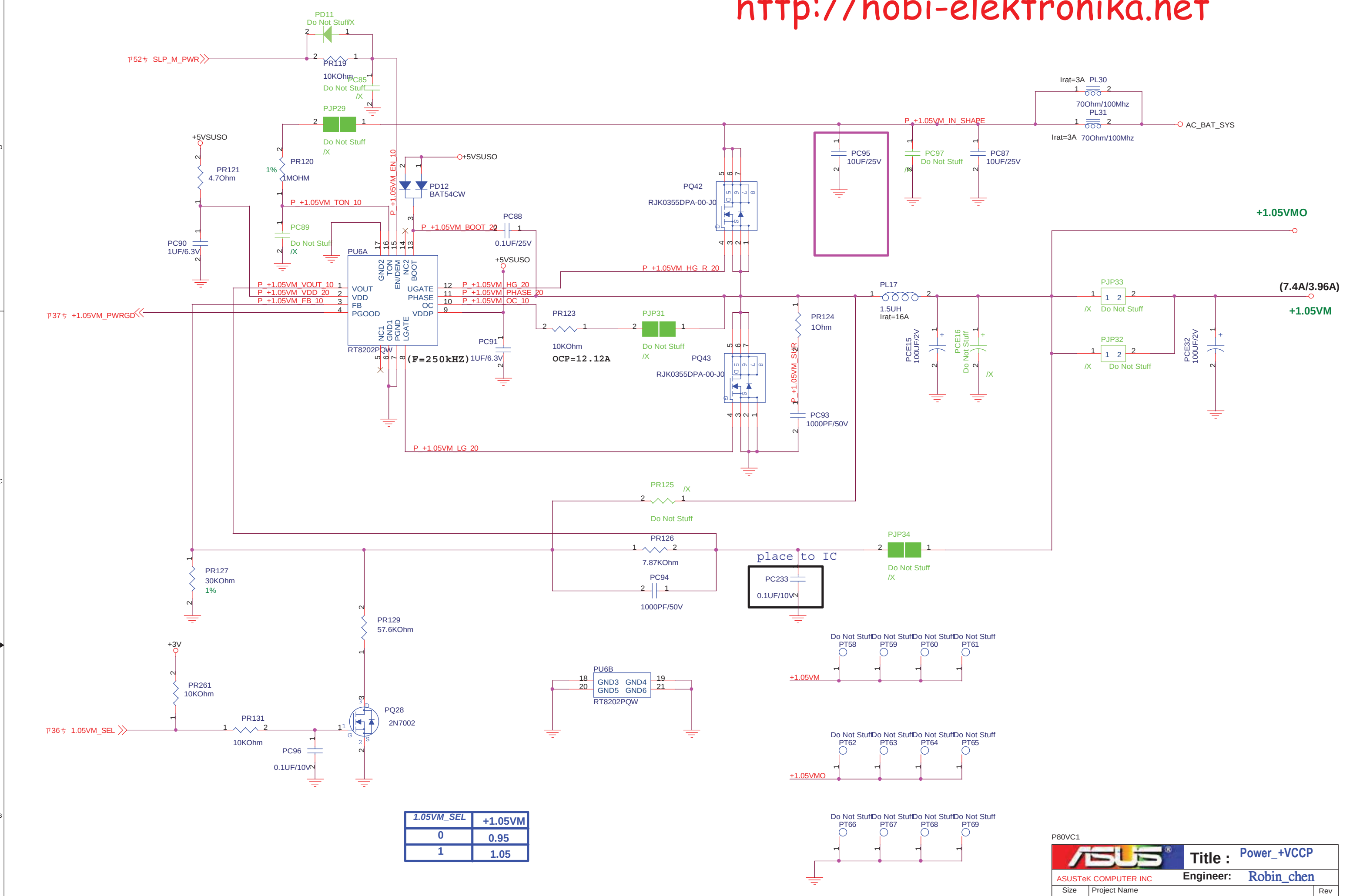
Controller

1. Voltage & Current:
   +1.5V&3.5A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=16.94A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

ASUSTeK COMPUTER INC

Title :	Power_+1.5VS		
Engineer:	Robin_chen		
Size A2	Project Name P80		Rev 1.1
Date: Tuesday, December 16, 2008	Sheet 50	of 56	



1.05VM_SEL	+1.05VM
0	0.95
1	1.05

Power stage

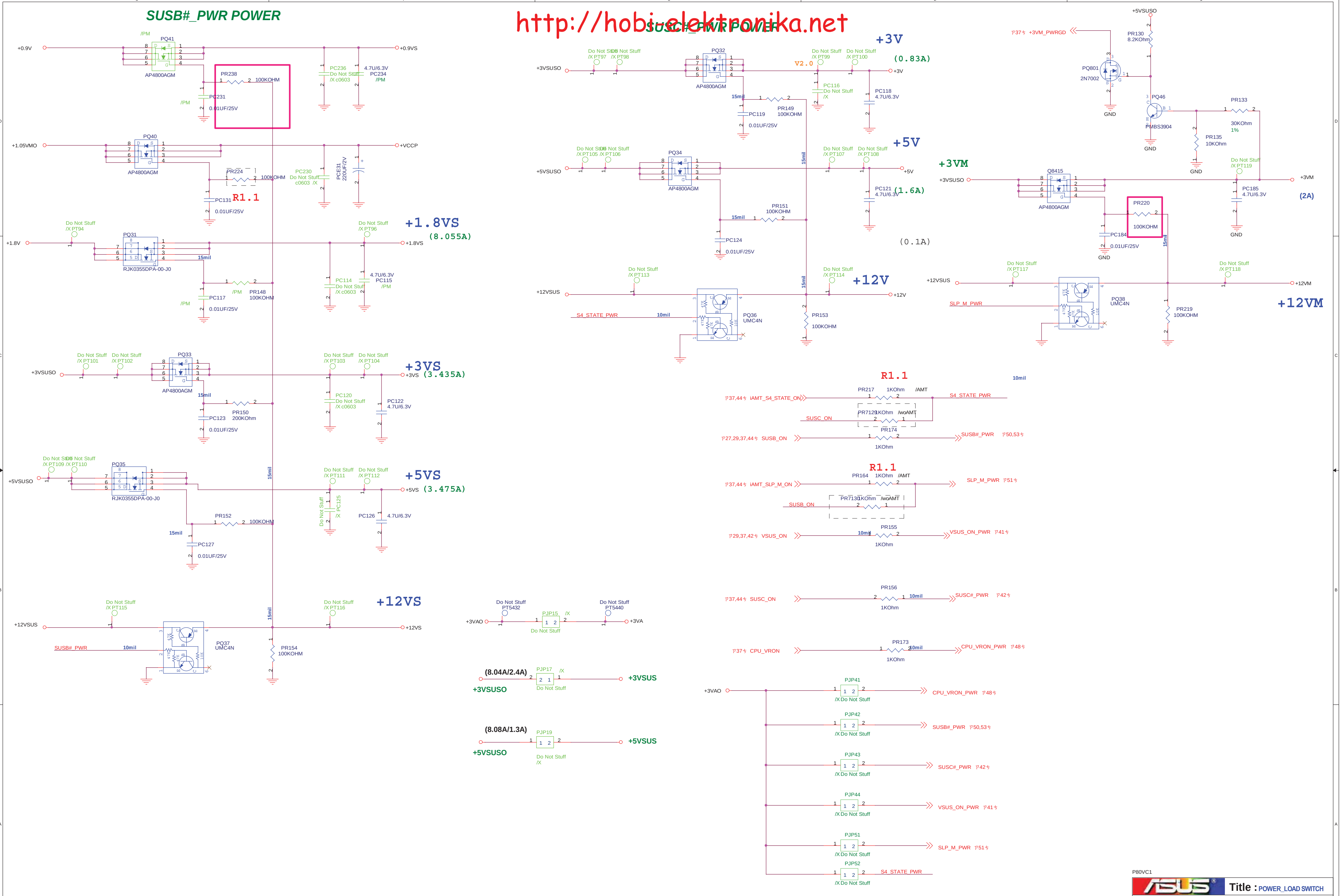
1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.65A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=22.44A
   ESR/2=9mohm
   V=162mV
4. Inductor Spec:
   Isat=33A
   Idc=16A
   DCR=3.8mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30 (T=25)
   Ipeak=120 (Pause<10us)

Controller

1. Voltage & Current:
   +1.05V&22.44A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=16.94A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

ASUSTeK COMPUTER INC	Title : Power_+VCCP	
	Engineer: Robin_chen	
Size A2	Project Name P80	Rev 1.1
Date: Tuesday, December 16, 2008	Sheet 51 of 56	



P80VC1

ASUS

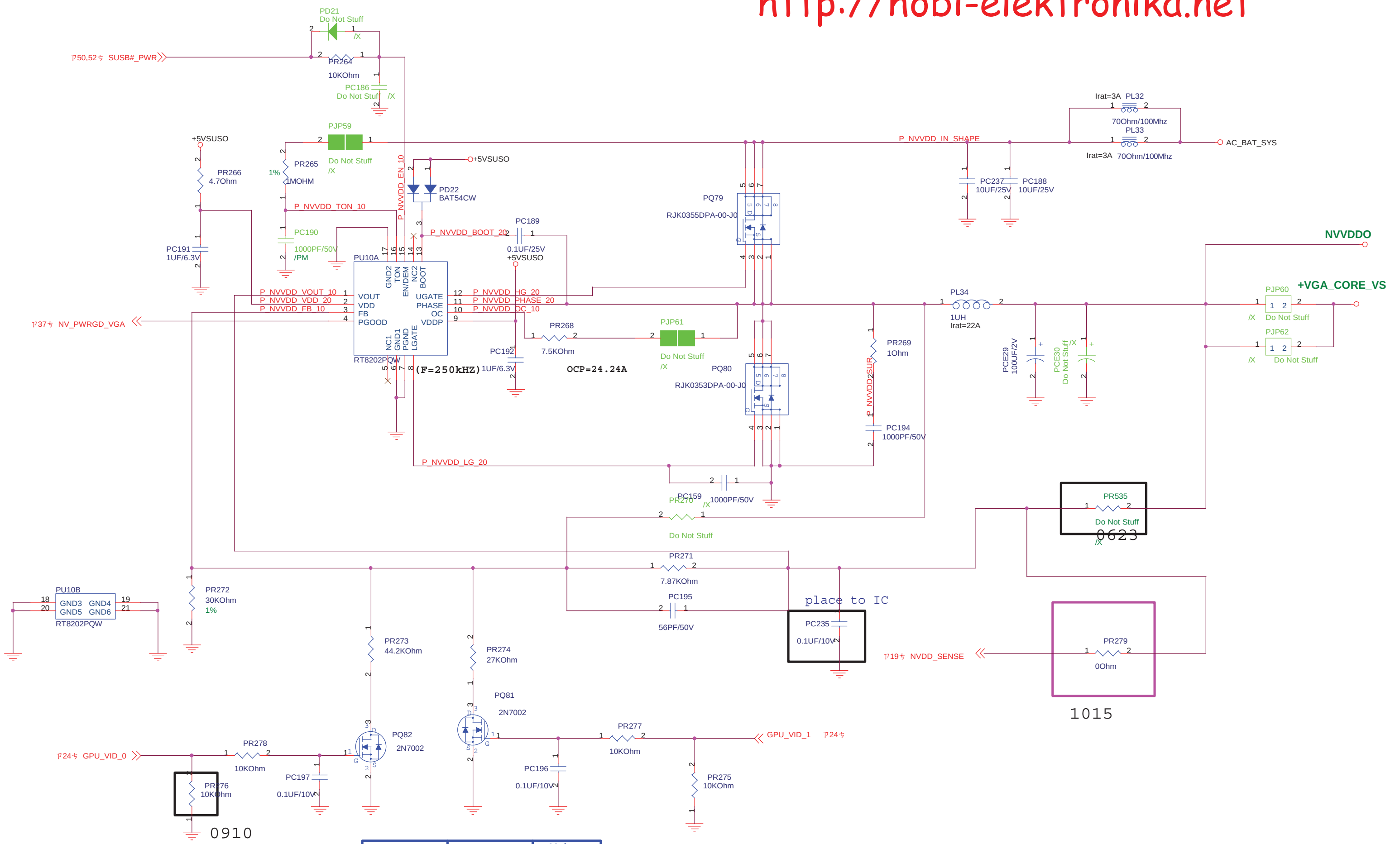
ASUSTek Computer INC.

Title : POWER_LOAD SWITCH

Engineer:

Size	Project Name	Rev
A2	P80	1.1

Date: Tuesday, December 16, 2008 Sheet 52 of 56



GPU_VID_0	GPU_VID_1	Voltage
L	L	0.946V
H	L	1.00V
L	H	1.17V
H	H	X

Power stage

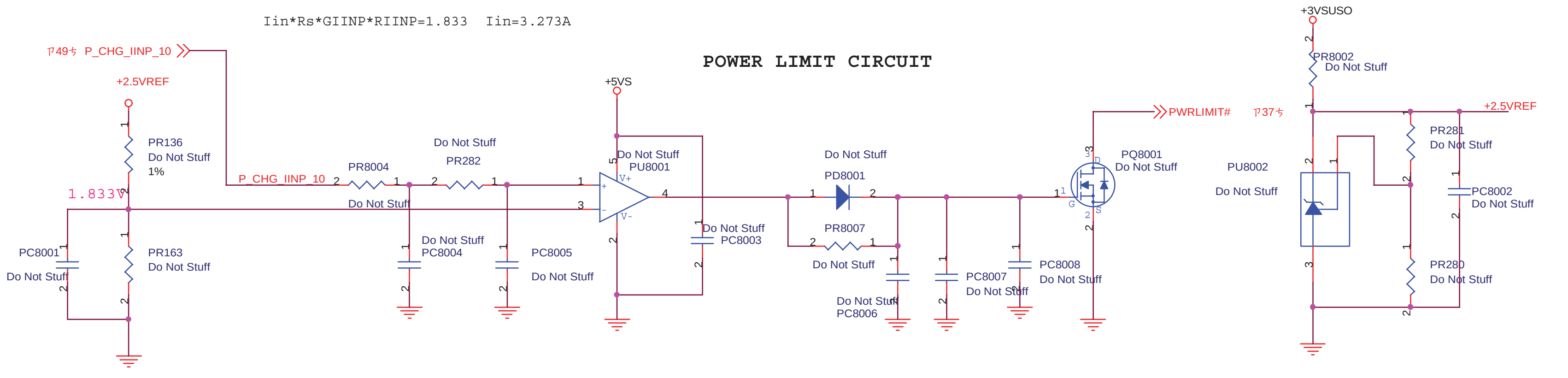
1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =2.3 A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=10.87A
   ESR/2=4.5mohm
   V=44mV
4. Inductor Spec:
   Isat=22A
   Idc=11A
   DCR=9mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355/RJK0353
   Rds(on)=11.8/5.4mOhm (Vgs=10V)
   Icont=30/35A (T=25)
   Ipeak=120/140A (Pause<10us)

Controller

1. Voltage & Current:
   +VGA:0.94&10.08A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=24A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

ASUS	Title :	Power_+VGA
ASUSTeK COMPUTER INC	Engineer:	robin_chen
Size A2	Project Name P80	Rev 1.1
Date: Tuesday, December 16, 2008	Sheet 53 of 56	



P80VC1

ASUSTek Computer INC.	Title : Power_Charger	
	Engineer: Robin_chen	
Size A3	Project Name P80	Rev R1.1
Date: Tuesday, December 16, 2008	Sheet 54 of 80	