

Compal Confidential

Tampa Bay NPVAA

LA-5841P Schematics Document

Intel PineView Processor/ Tiger point

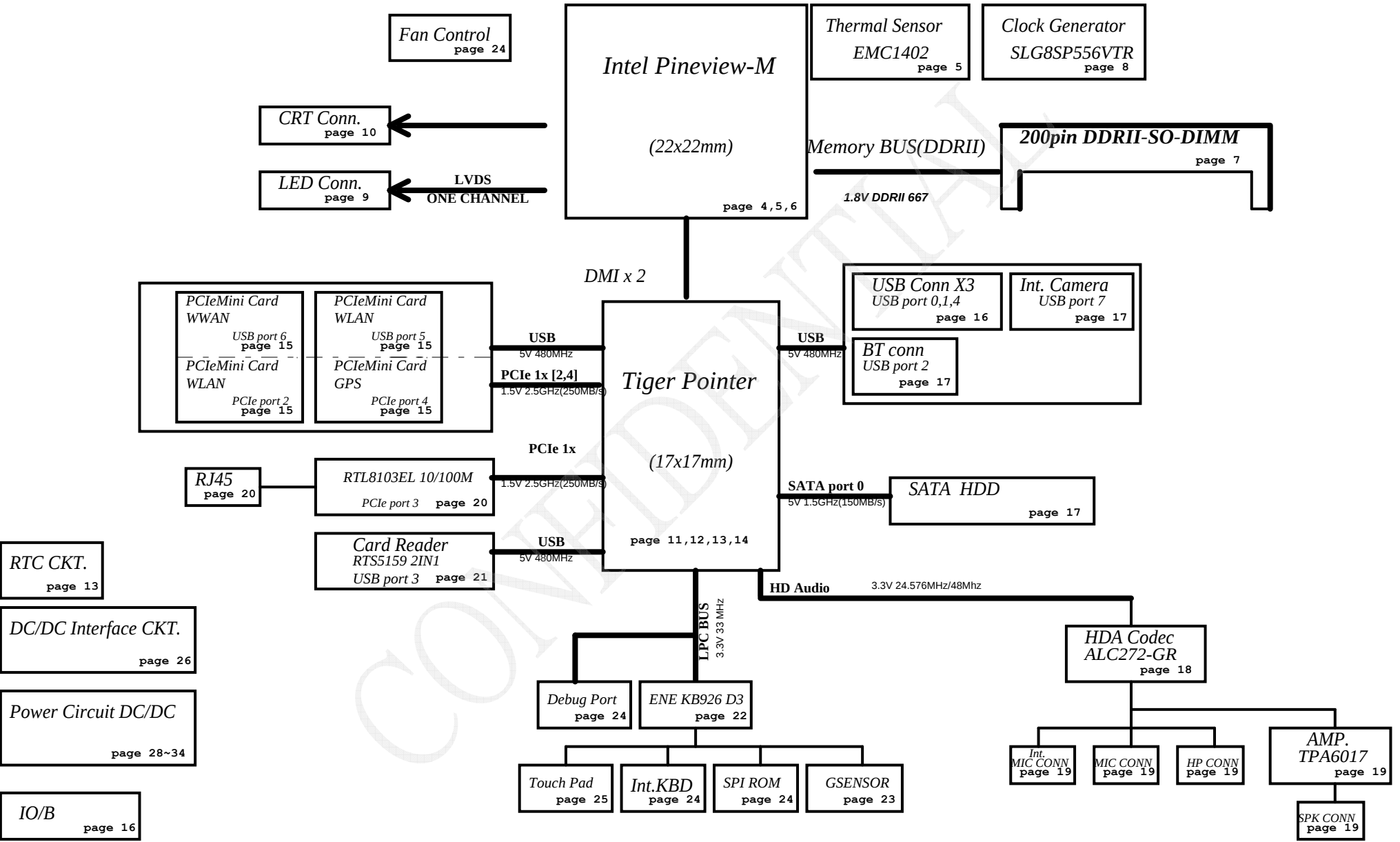
2009-10-21

REV: 1.0

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				Document Number	
				Custom	401799
				Date:	Tuesday, December 15, 2009
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Model Name : NPVAA
File Name : LA-5841P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				STAR			
description								
explain	Wi-Fi	WiMax	3GGPS	3G	POWER SAVING			
BTO	WLAN@	WIMAX@	3GGPS@	3G@	STAR@			

Function			
description			
explain			
BTO			

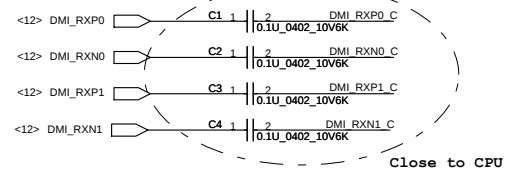
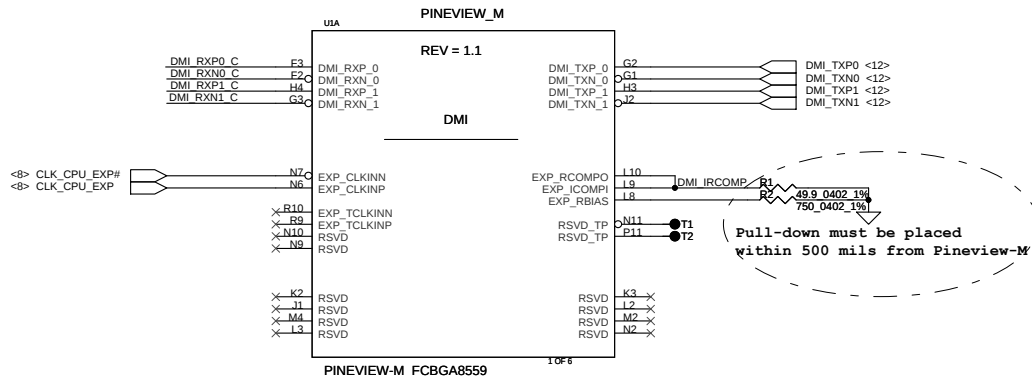
EC SM Bus1 address

EC SM Bus2 address

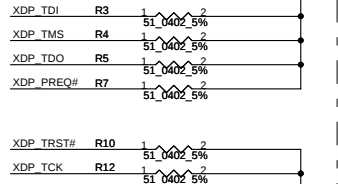
Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

Tiger point SM Bus address

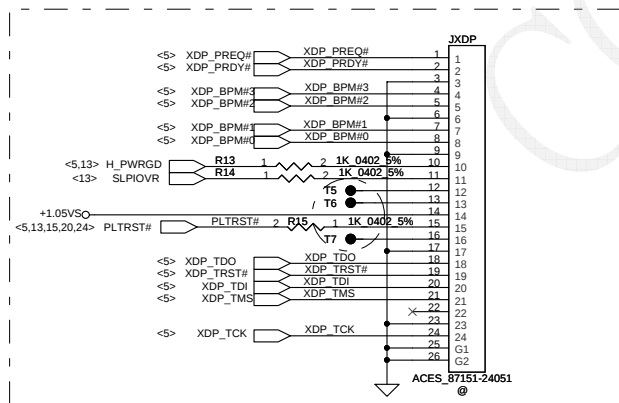
Device	Address
Clock Generator (SLG8SP56VTR)	1101 001Xb
DDR DIMMA	1010 000Xb



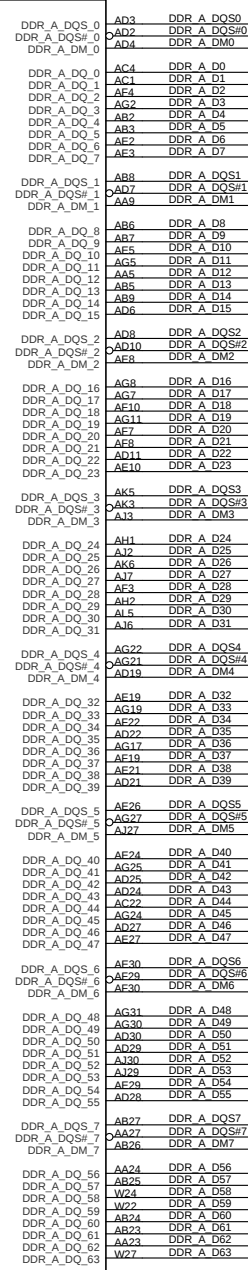
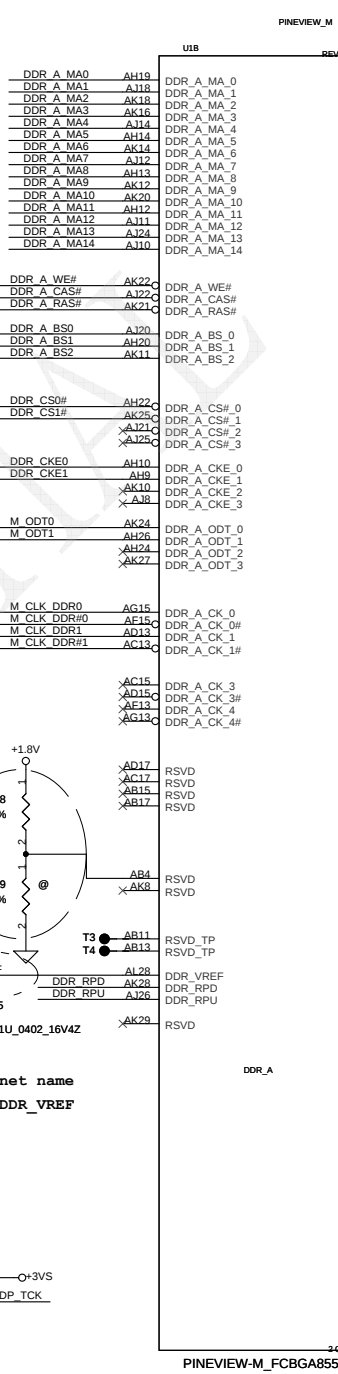
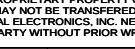
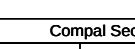
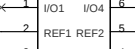
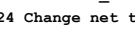
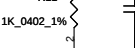
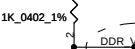
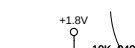
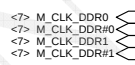
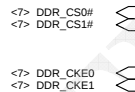
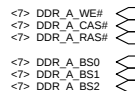
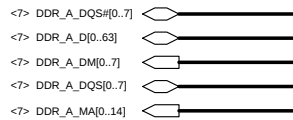
XDP Reserve



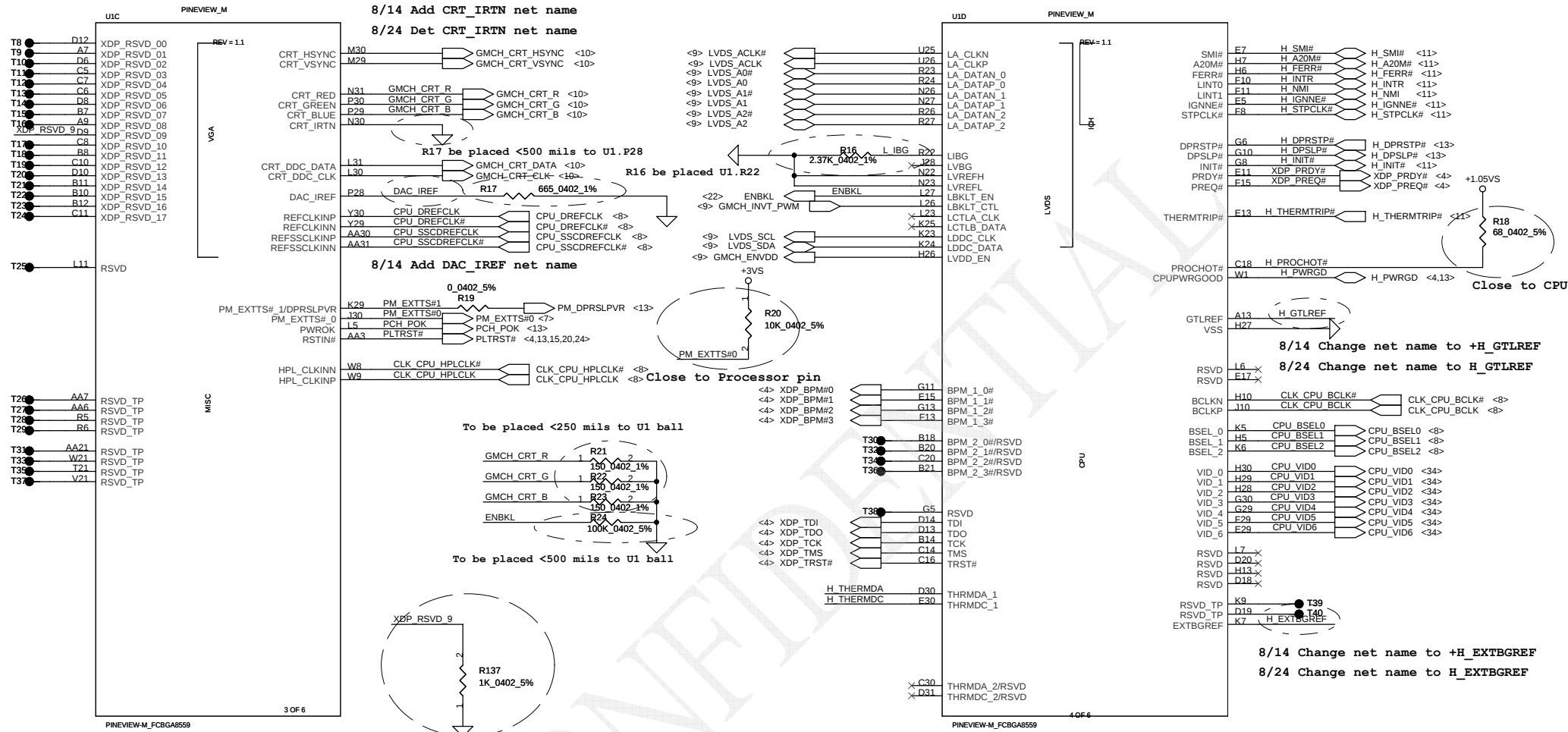
7/21 Add C302 to GND for Intel request
7/27 Change C302 to GND for +1.8V pull up



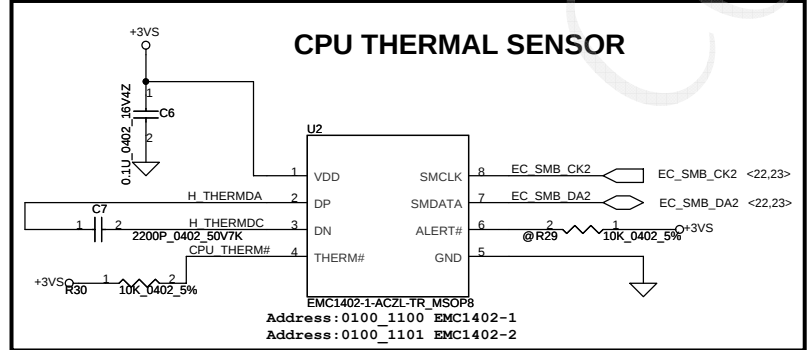
Place diff CPU side
10/19 Change footprint T5, T6 and T7 from TPC24 to TPC12



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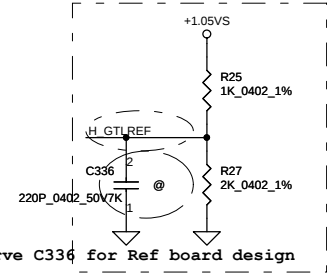
7/21 Pull down 1K to GND for Intel request



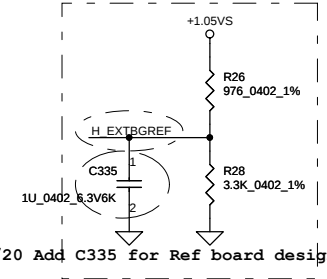
H DPRSTP#	C151	1	220P 0402 50V7K
H DPSLP#	C152	1	220P 0402 50V7K
H PWRGD	C154	1	220P 0402 50V7K
H A20M#	C134	1	220P 0402 50V7K
H IGNE#	C135	1	220P 0402 50V7K
H INIT#	C136	1	220P 0402 50V7K
H INTR	C137	1	220P 0402 50V7K
H FERR#	C138	1	220P 0402 50V7K
H NMI	C139	1	220P 0402 50V7K
H SMI#	C140	1	220P 0402 50V7K
H STPCLK#	C141	1	220P 0402 50V7K

7/20 Reserve C336 for Ref board design
ESD request

placed within 0.5" of processor pin.

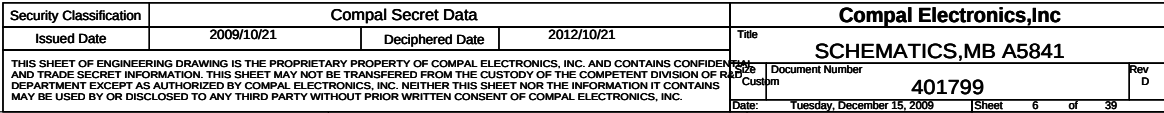


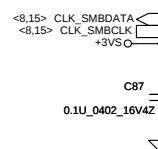
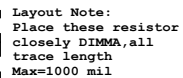
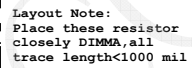
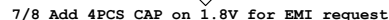
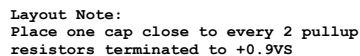
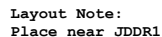
placed within 0.5" of processor pin and 5 mils spacing



7/20 Add C335 for Ref board design

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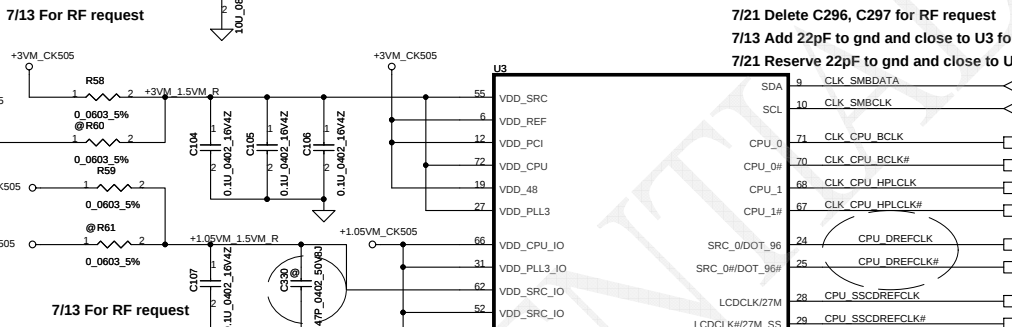
Three circuit diagrams for the SA000020K00 (Silego : SLG8SP556VTR) are shown, illustrating different power supply configurations and component annotations.

Top Diagram: Shows a +3VS supply connected to a circuit. Key components include R53, C89, C90, C91, C92, and C328. A current of 250 mA is indicated. Annotations include "7/13 For RF request" and "8/27 Delete C93, C94, C95, C102 for low p".

Middle Diagram: Shows a +1.05VSO supply connected to a circuit. Key components include R54, C96, C97, C98, C99, C100, C101, and C329. A current of 80 mA is indicated. Annotations include "7/13 For RF request" and "8/27 Delete C93, C94, C95, C102 for low p".

Bottom Diagram: Shows a +1.5VS supply connected to a circuit. Key components include R57 and C103. A current of 200 mA is indicated. Annotations include "8/27 Delete C93, C94, C95, C102 for low p".

SA000020K00 (Silego : SLG8SP556VTR)



REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	

CLKREQ# Pin Configuration

Pin 21: CLKREQ# (CLKREQ#)

Pin 22: VSS_PCI

Pin 23: VSS_REF

Pin 24: VSS_48

Pin 25: VSS_IO

Pin 26: VSS_CPU

Pin 27: VSS_PLL3

Pin 28: VSS_SRC

Pin 29: VSS_SRC

Pin 30: VSS

Pin 31: VSS

Pin 32: CLK_CPU_EXP

Pin 33: CLK_CPU_EXP#

Pin 34: SRC_2#

Pin 35: SRC_2#

Pin 36: SRC_3#

Pin 37: SRC_3#

Pin 38: SRC_4#

Pin 39: SRC_4#

Pin 40: SRC_4#

Pin 41: SRC_6#

Pin 42: SRC_6#

Pin 43: SRC_6#

Pin 44: SRC_7#

Pin 45: SRC_7#

Pin 46: SRC_8#

Pin 47: SRC_8#

Pin 48: SRC_9#

Pin 49: SRC_9#

Pin 50: SRC_10#

Pin 51: SRC_10#

Pin 52: SRC_11#

Pin 53: SRC_11#

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Pin 199: SRC_11#

Pin 200: SRC_11#

<

CLK_PCIE_SATA <11>

CLK_PCIE_SATA# <11>

CLK_PCIE_WLAN <15>

CLK_PCIE_WLAN# <15>

WLAN_CLKREQ# R67 2 1 10K 0402 5%

WWAN_CLKREQ# R68 2 1 10K 0402 5%

LAN_CLKREQ# R69 2 1 10K 0402 5%

+3V5

REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	

WLAN_CLKREQ# <15>

LAN_CLKREQ# <20>

WWAN_CLKREQ# <15>

LAN_CLKREQ# from REQ4 to REQ11

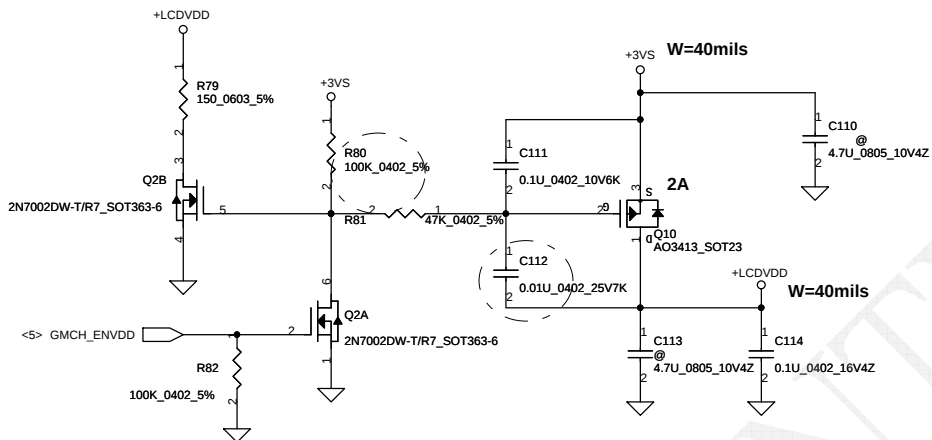
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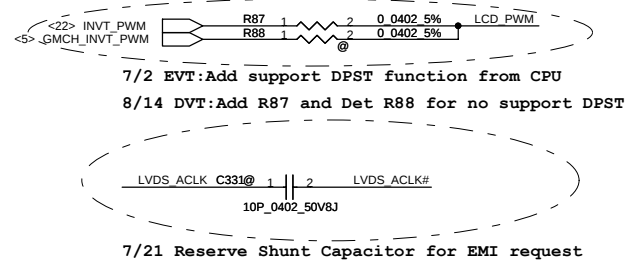
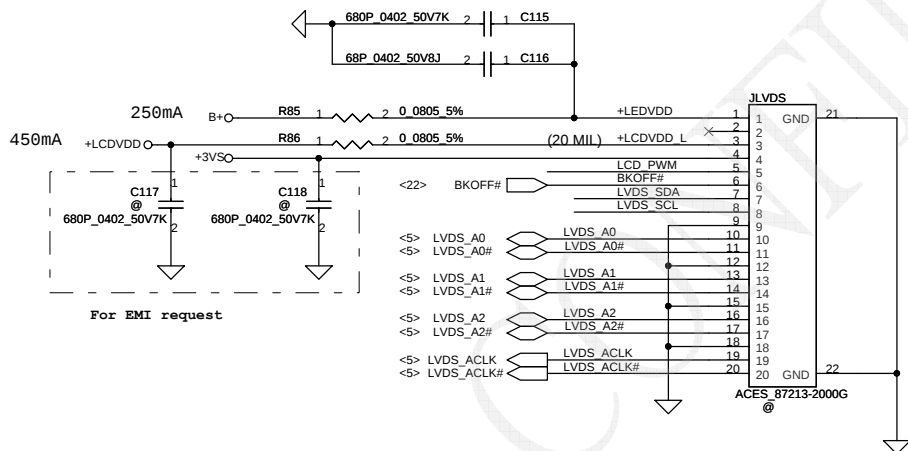
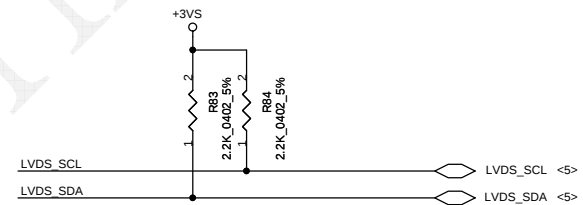
NC. AND CONTAINS CONFIDENTIAL INFORMATION IT CONTAINS ELECTRONICS, INC.

REV D

LCD POWER CIRCUIT



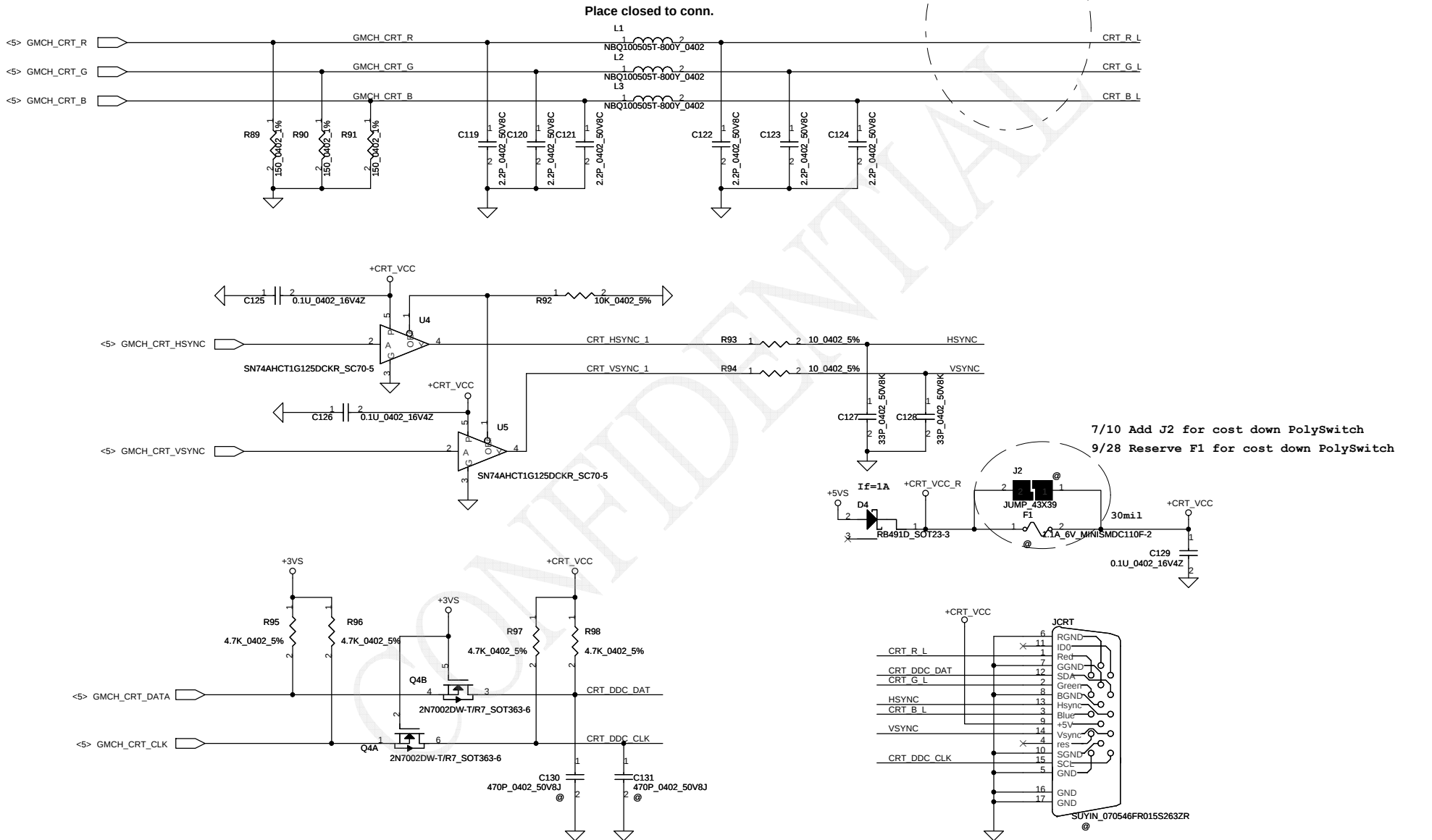
LED/PANEL BD. Conn.



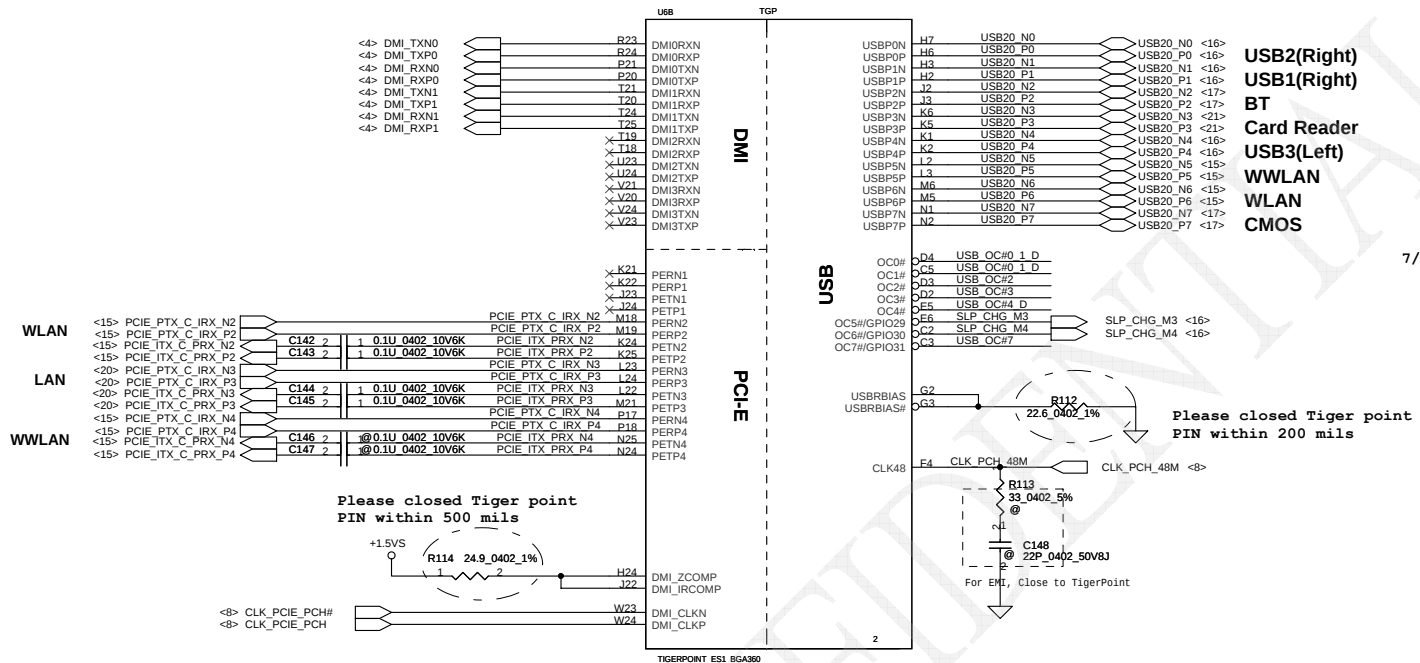
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CRT CONNECTOR

8/24 Det D1, D2, D3 for ESD request



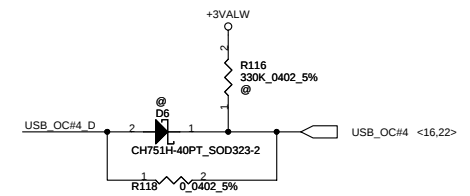
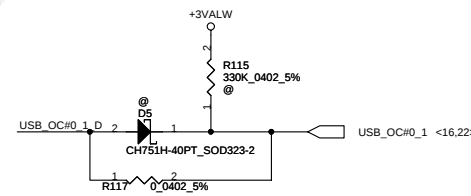
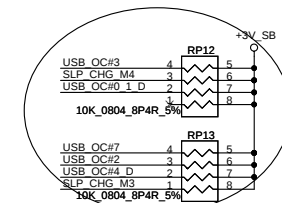
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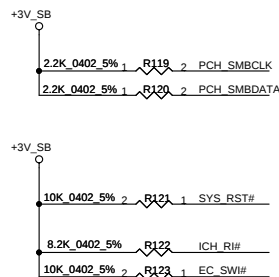


USB PORT LIST

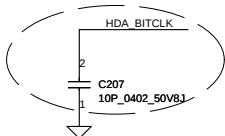
PORT	DEVICE	Modify
USB0	USB3(Left)	USB2(Right)
USB1	BT	USB1(Right)
USB2	Card Reader	BT
USB3	USB2(Right)	Card Reader
USB4	USB1(Right)	USB3(Left)
USB5	WWLAN	WWLAN
USB6	WLAN	WLAN
USB7	CMOS	CMOS

7/17 Reassign Tiger point USB port for TOSHIBA concern

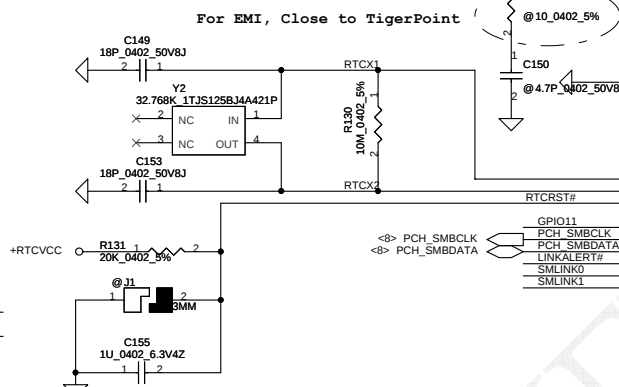
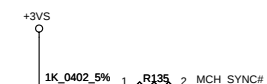
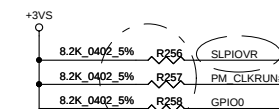
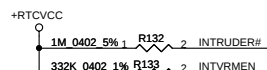
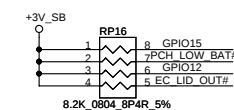
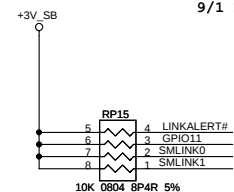




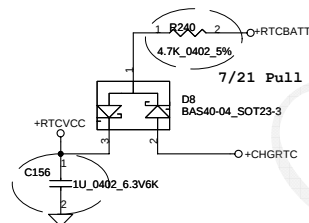
7/2 For EMI, Close to TigerPoint
9/1 C207 change to SE071100J80 for EMI request



9/1 R125 change to SM010027780 for EMI request

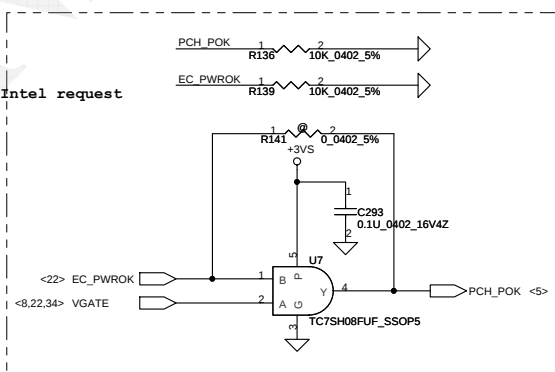


7/20 Add SLPIOV# pull up 8.2k to +3vs
9/23 Change RP17 to R256, R257, R258 for layout request

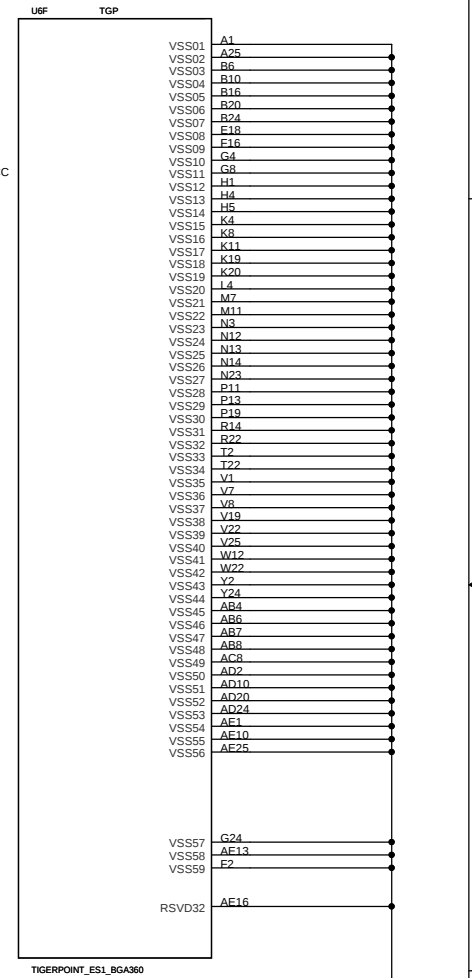
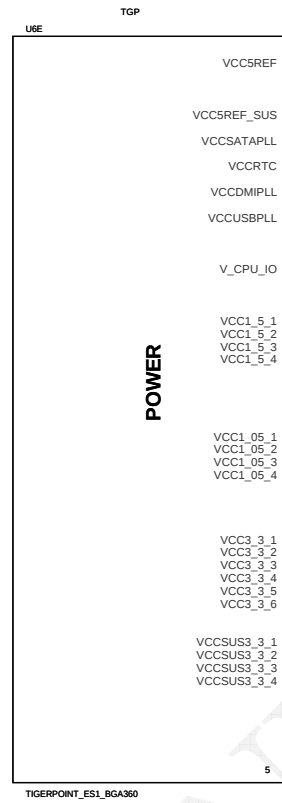
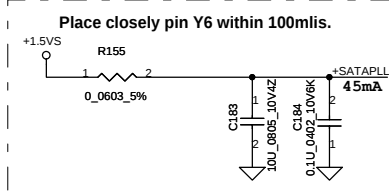
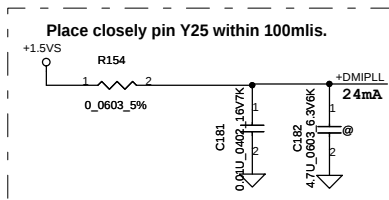
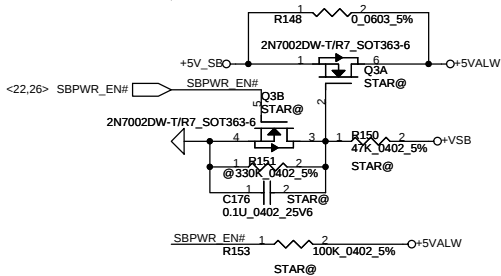
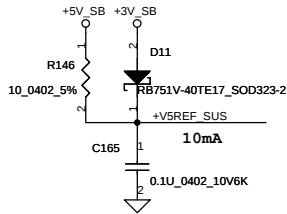
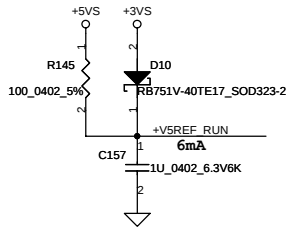


7/21 Change C156 to 1u for Intel request

7/21 Pull up 4.7K to +RTCBATT for Intel request

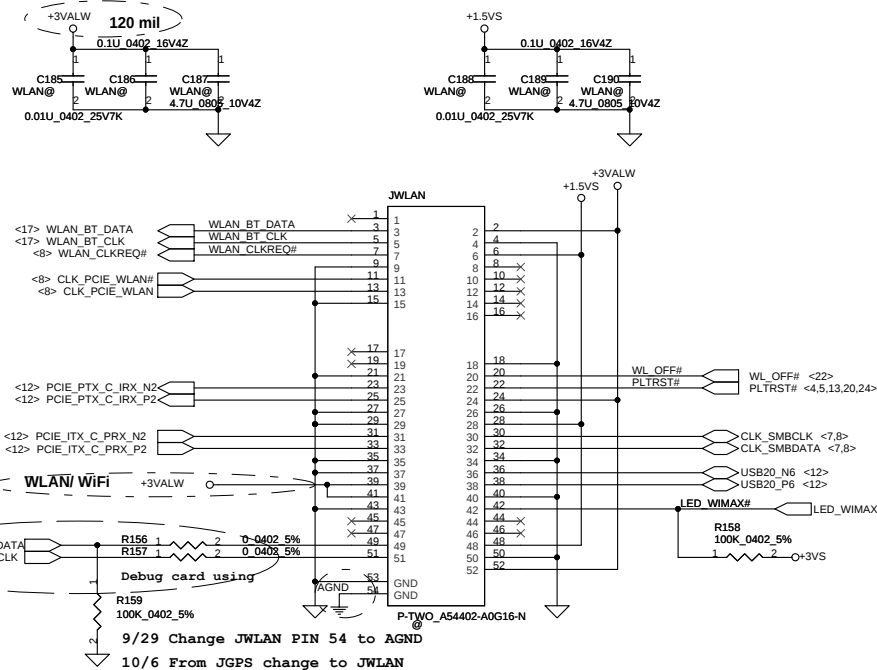


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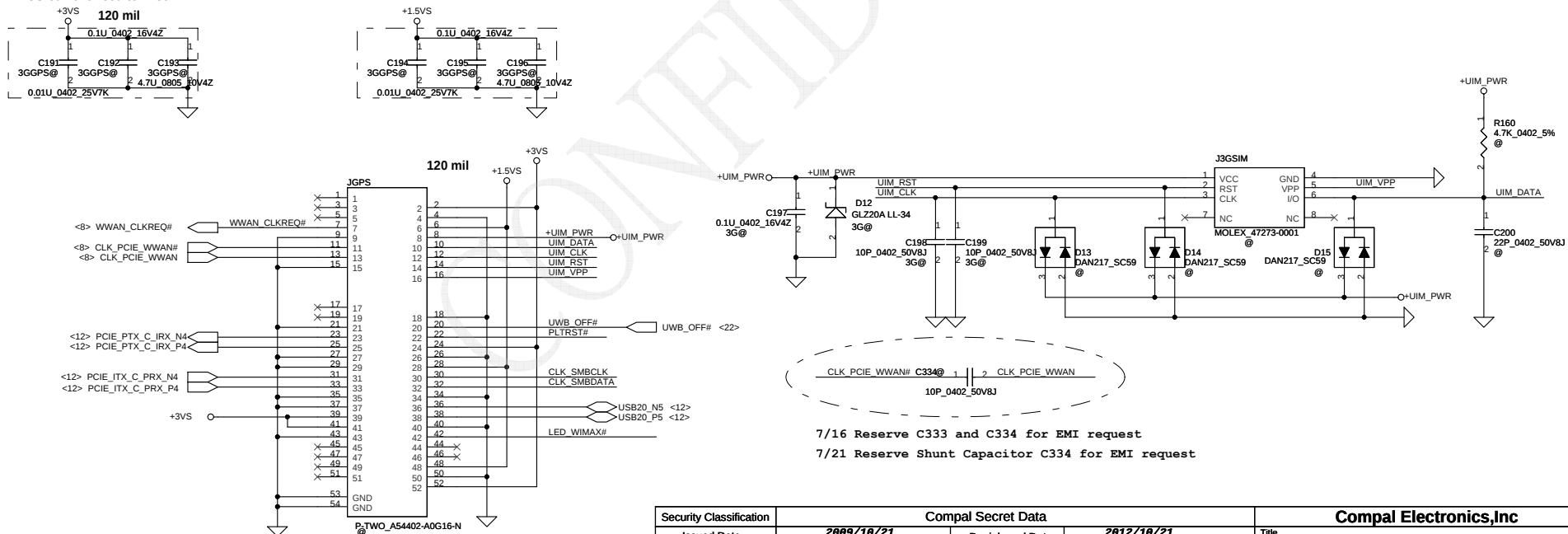
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Mini-Express Card for WLAN/WiMax



Mini-Express Card for 3G/GPS

3G current need to 2750mA

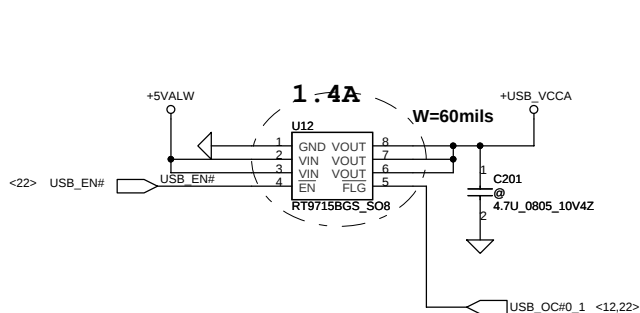


7/16 Reserve C333 and C334 for EMI request

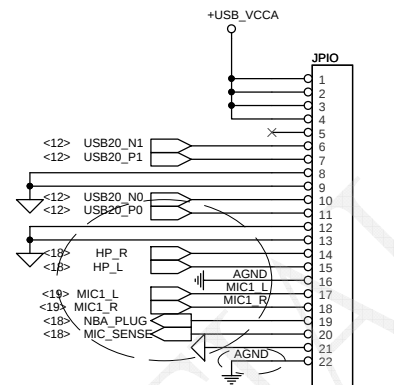
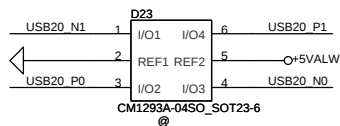
7/21 Reserve Shunt Capacitor C334 for EMI request

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USB CONN--Right



8/24 Change U12 to SA00002XX00 for discharge +USB_VCCA



7/8 Pin swap for AGND

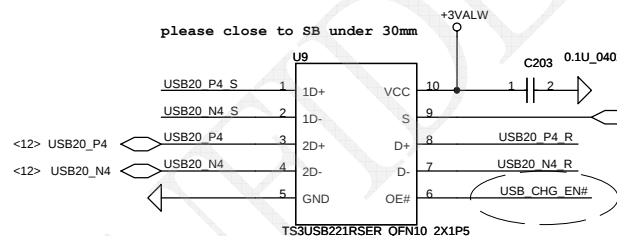
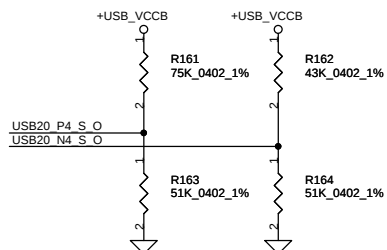
9/3 Add PIN 21, PIN 22 for GND pad

9/3 Change JPIO PIN 22 to AGND

7/8 ESD diode change location from Sub board to M/B

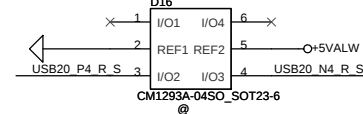
9/28 D36 for ESD request

USB Board--Left



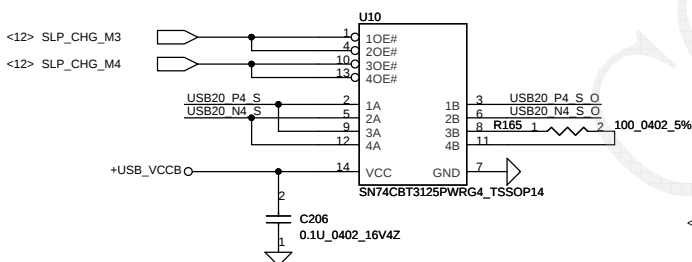
8/21 USB_CHG_EN# has to be connected to OE# pin for SPEC REV 0.5

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D



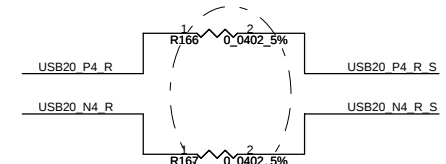
7/27 Swap USB20_P4_R_S and USB20_N4_R_S

8/19 Change JUSBC to DC233004W00 for ME request



7/16 USB_OC#0 dis-connect to +USB_VCCB

7/17 Change U11 to SA00002XX00 for discharge +USB_VCCB

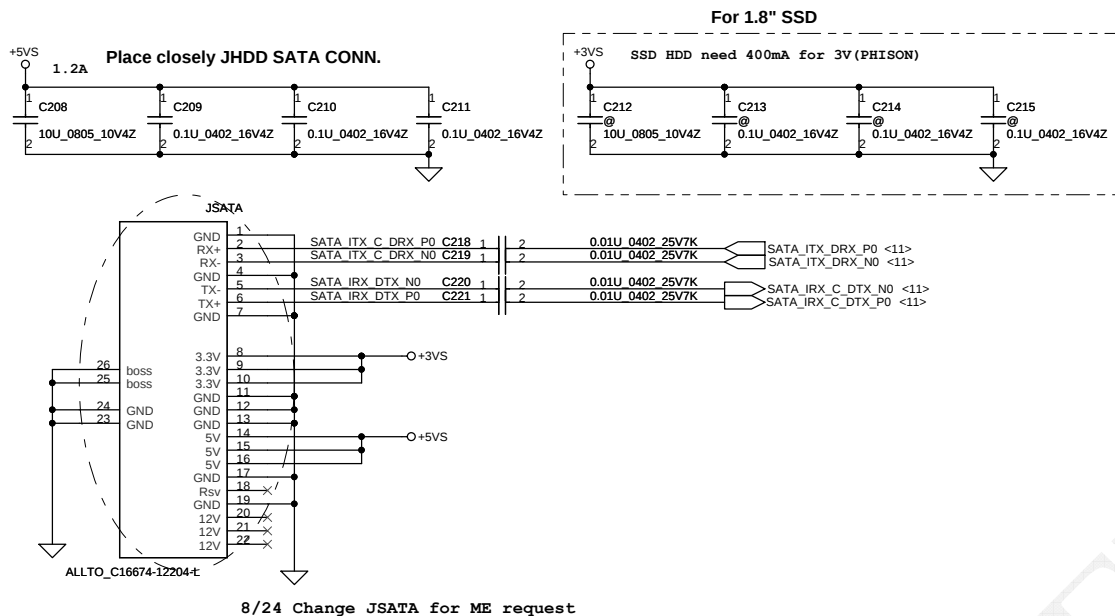


7/2 For EMI request and change to SM070001310

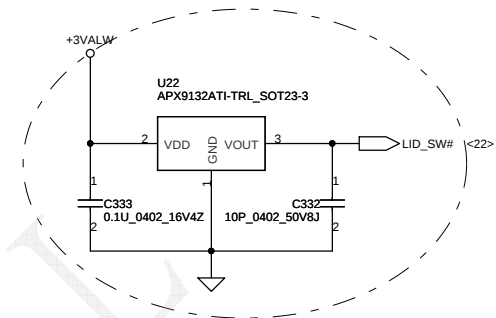
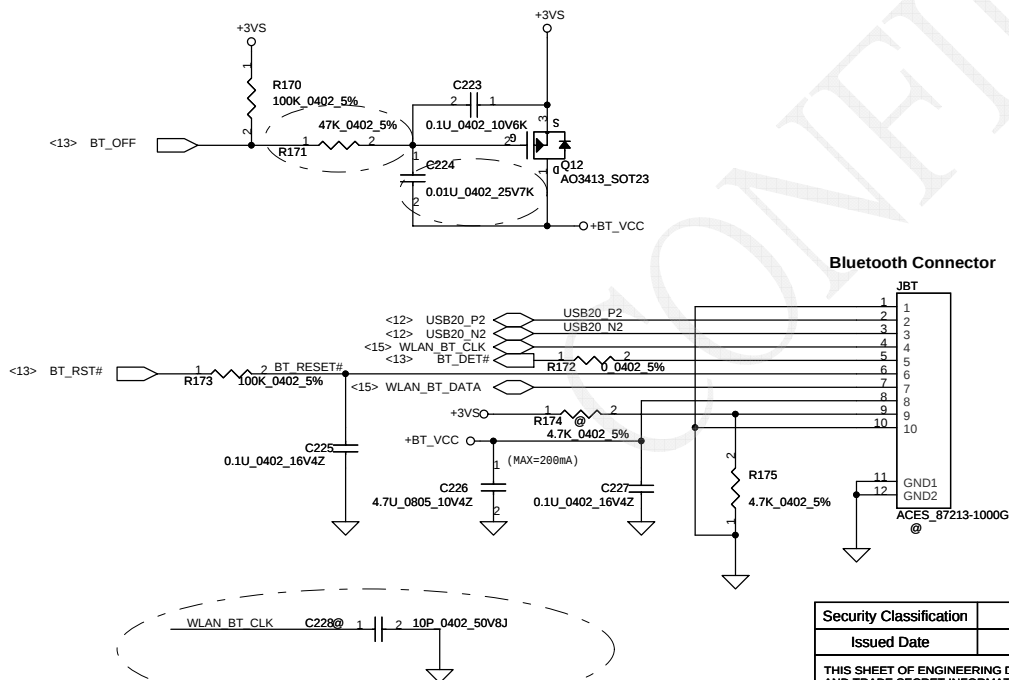
10/20 Delete L4 for EMI request

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

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SATA Conn.

Bluetooth Interface



8/19 Add Lid switch function on M/B for ME request

Camera Conn.

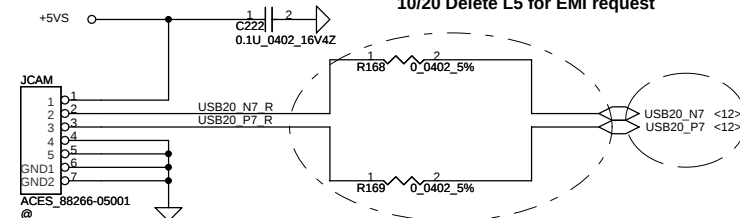
Int. Camera

W=20mils

7/21 Swap USB20_P7, USB20_N7 for layout request

8/14 Swap USB20_P7, USB20_N7 for layout request

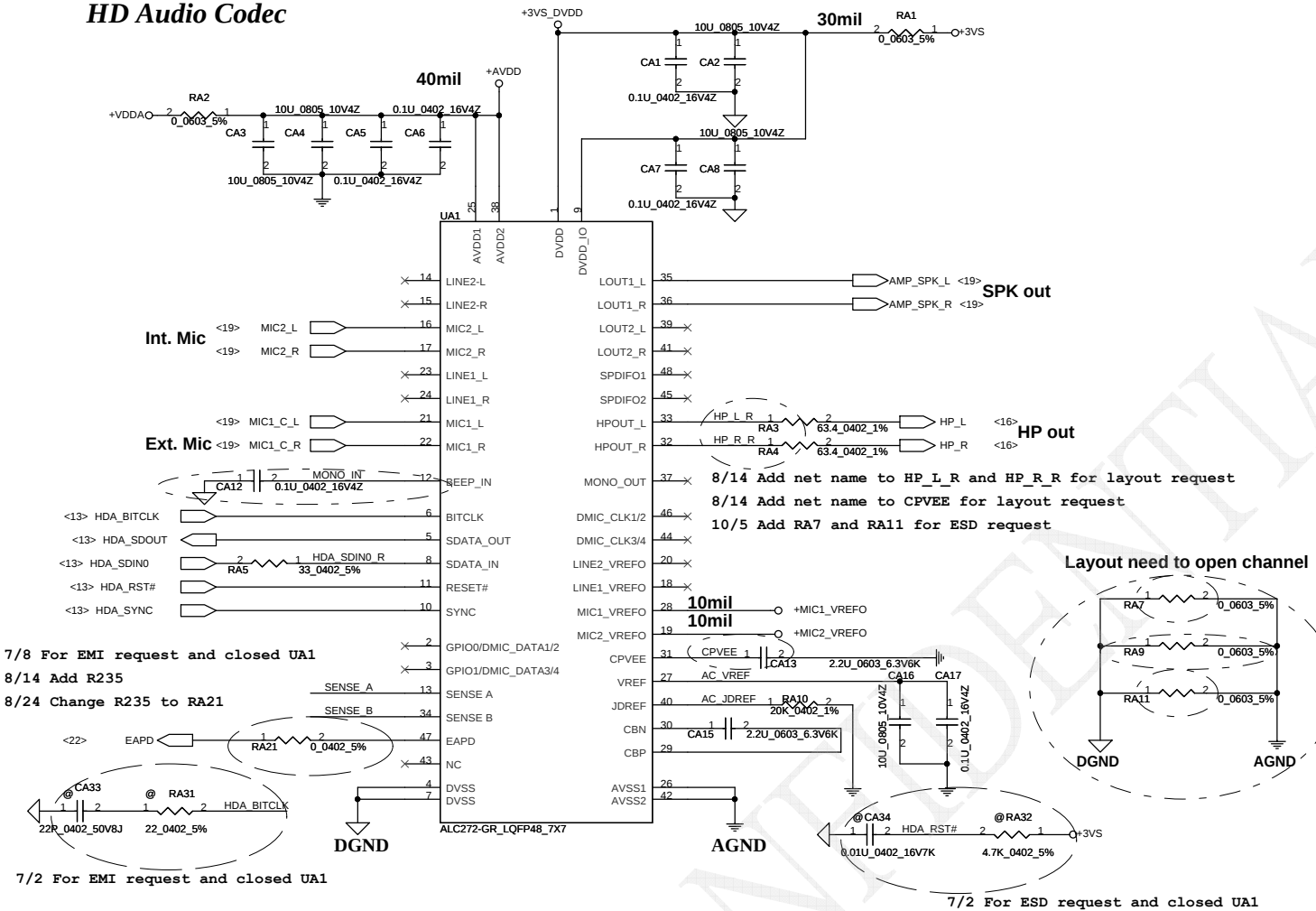
10/20 Delete L5 for EMI request



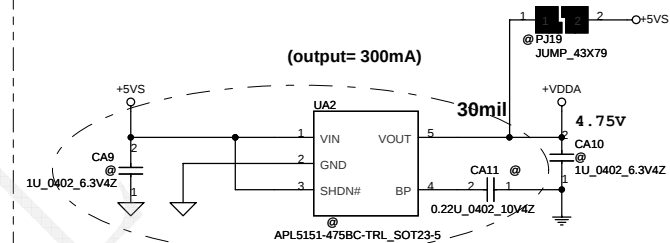
For EMI request

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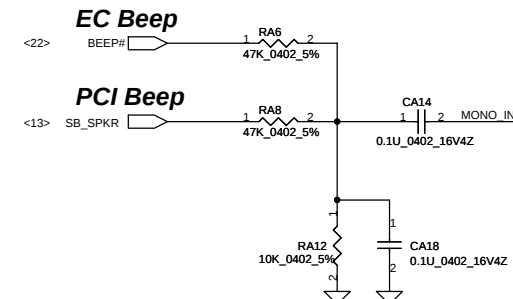
HD Audio Codec



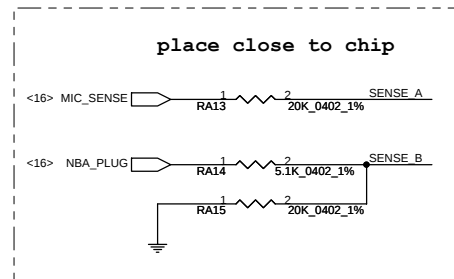
Audio regulator



Beep sound



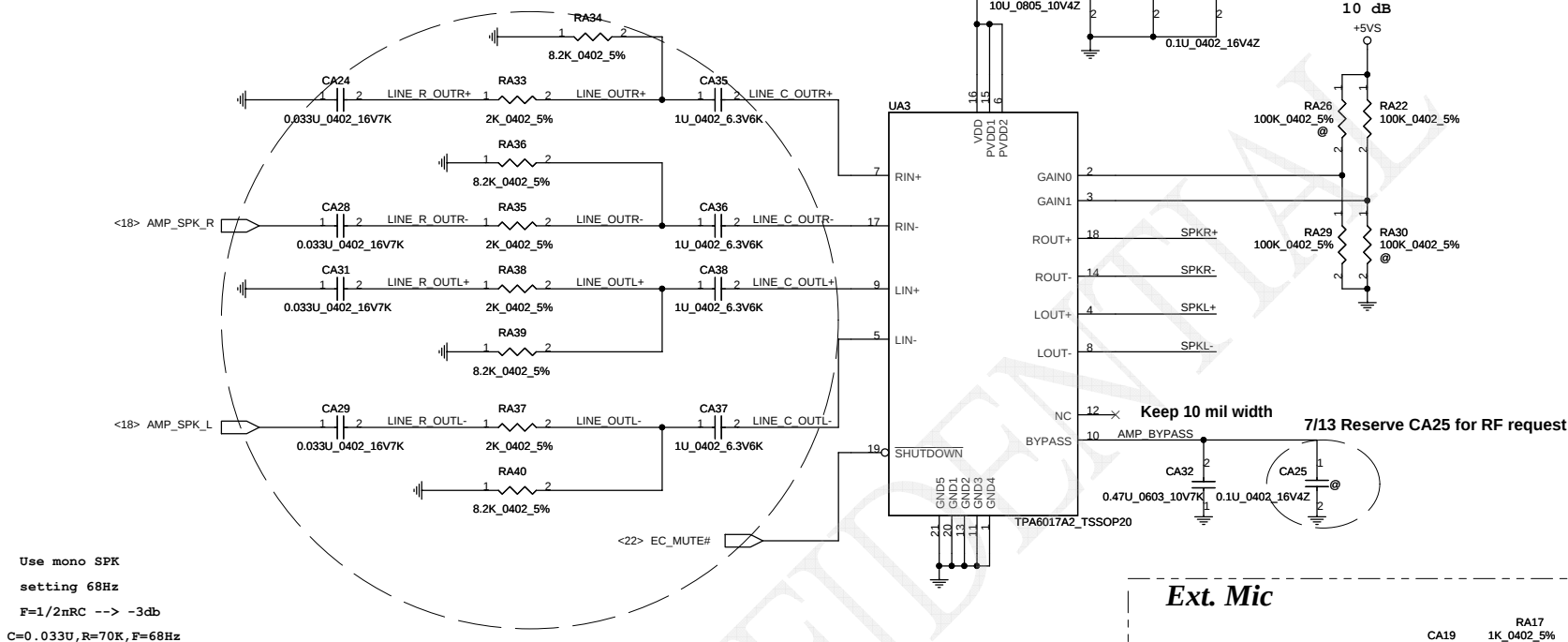
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Ext. MIC
	20K	PORT-B (PIN 21, 22)	
	10K	PORT-C (PIN 23, 24)	SPK out
	5.1K	PORT-D (PIN 35, 36)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	Int. MIC
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	Headphone out
	5.1K	PORT-I (PIN 32, 33)	



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TPA6017 Medium Range Amplifier

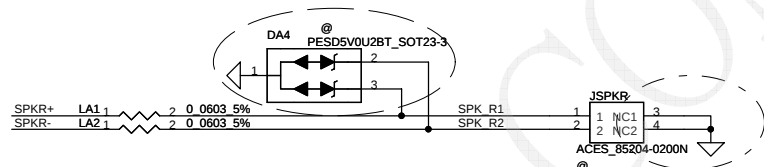
Rin = 70Kohm



Use mono SPK
setting 68Hz
F=1/2nRC --> -3db
C=0.033U, R=70K, F=68Hz

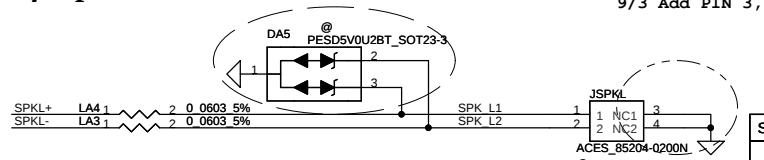
7/21 Add RA33-RA40, CA35-CA38 for AMP gain

Right Speaker Connector



7/3 Change to SCA00000T00 for ESD request

Left Speaker Connector

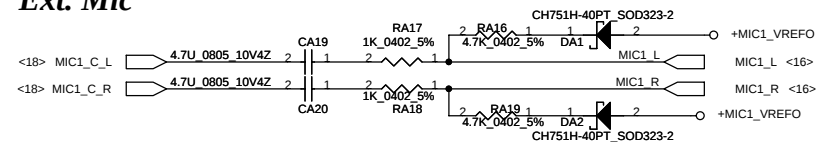


7/3 Change to SCA00000T00 for ESD request

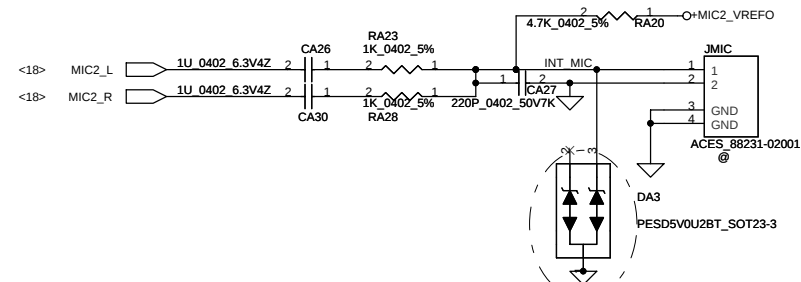
10/27 Delete DA4 and DA5 for ESD request

9/3 Add PIN 3, PIN 4 for GND pad

Ext. Mic

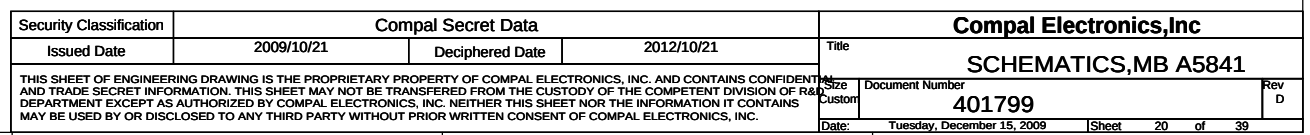
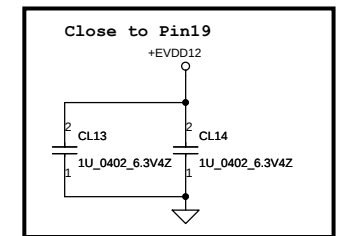


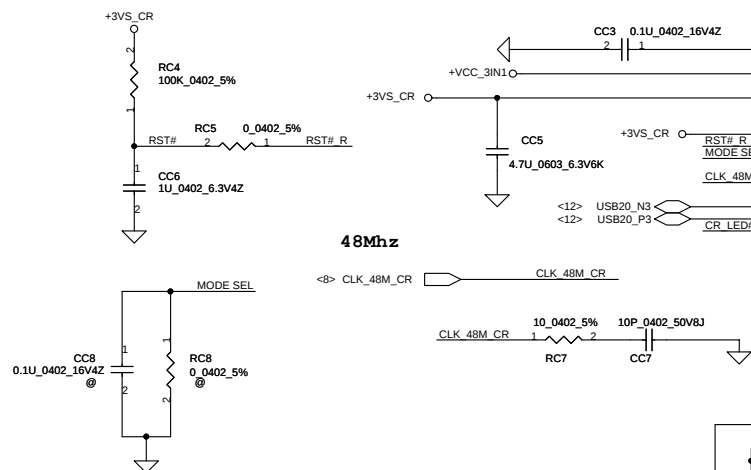
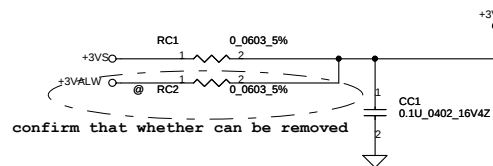
Int. Mic



7/3 Change to SCA00000T00 for ESD request

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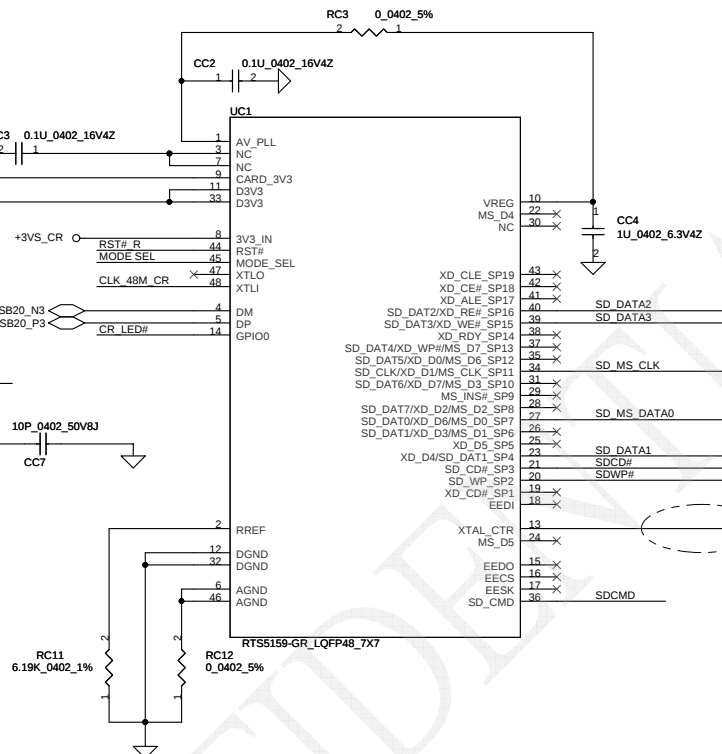
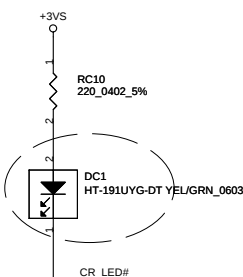




48Mhz

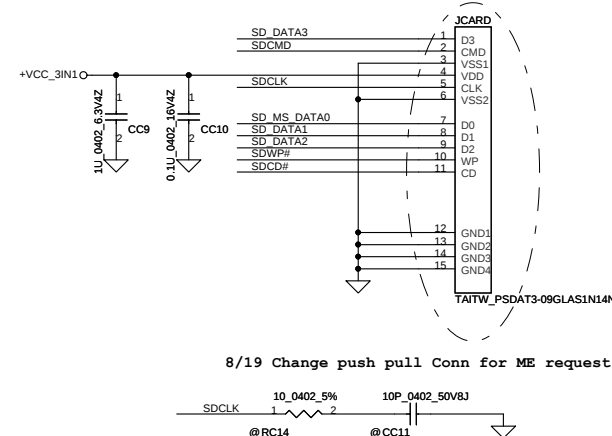
<8> CLK_48M_CR CLK_48M_CR

7/23 Change to TOP view LED



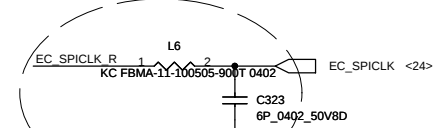
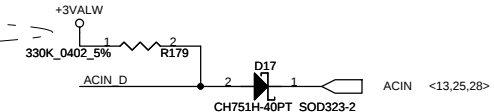
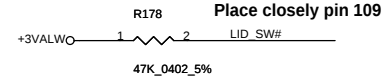
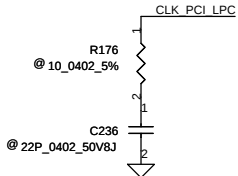
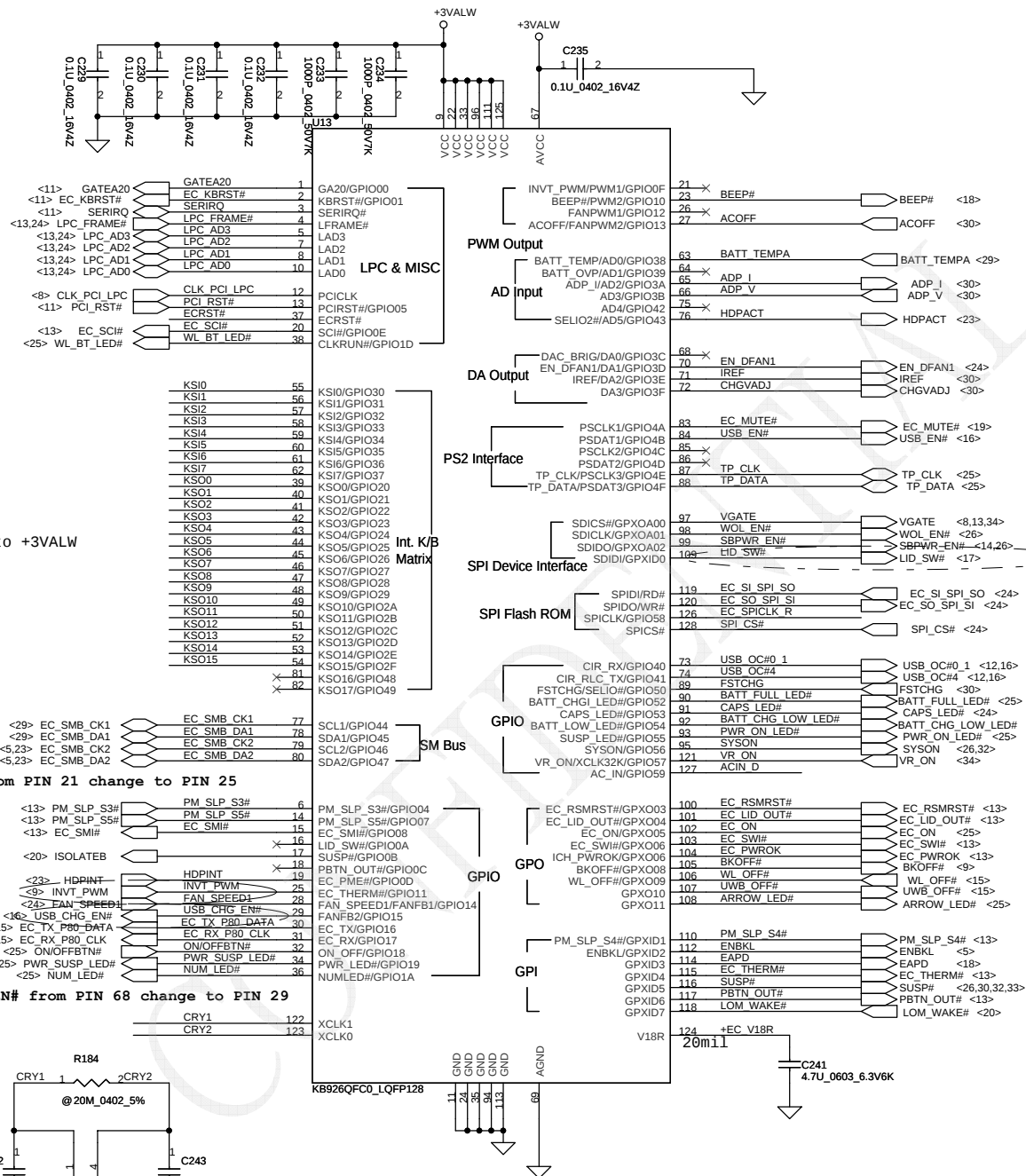
XTAL_CTR	Description
0	Use 12MHz Crystal
1	Use 48MHz CLK Gen

2 in 1 Card Reader



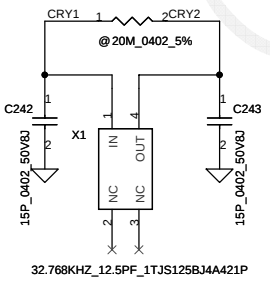
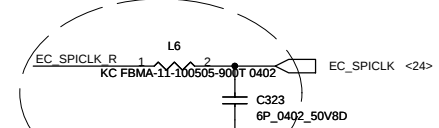
R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

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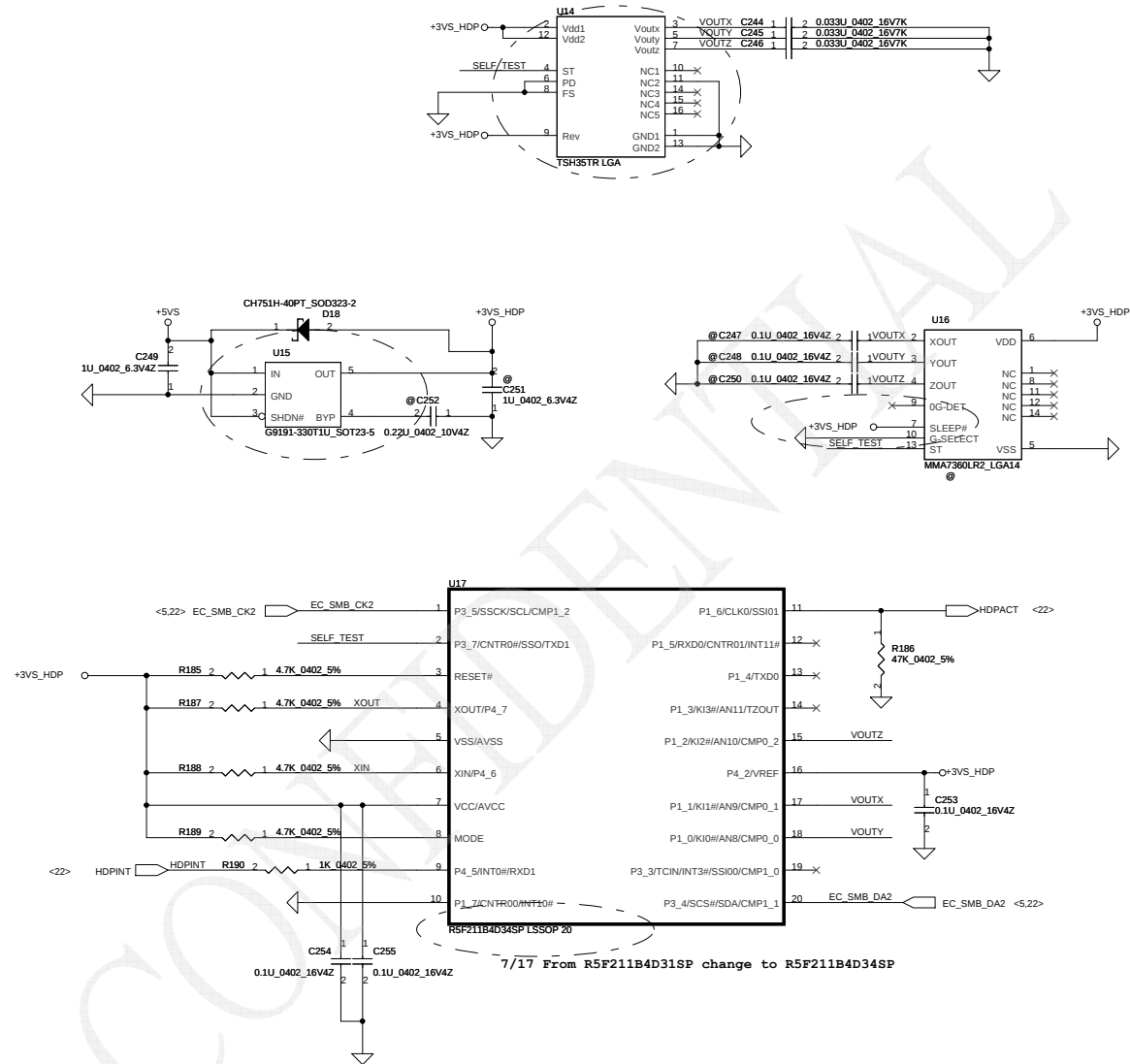
Add R235 and C233 for EMI and closed U13.126

7/6 Change R235 to L6 for EMI request



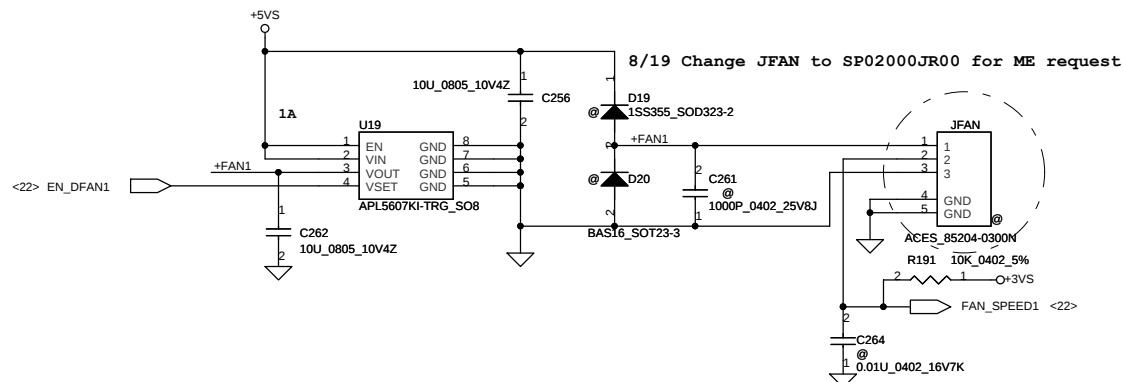
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G-Sensor

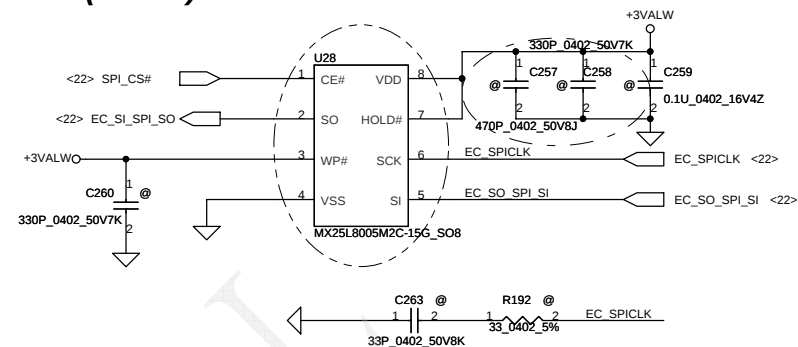


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FAN Control Circuit

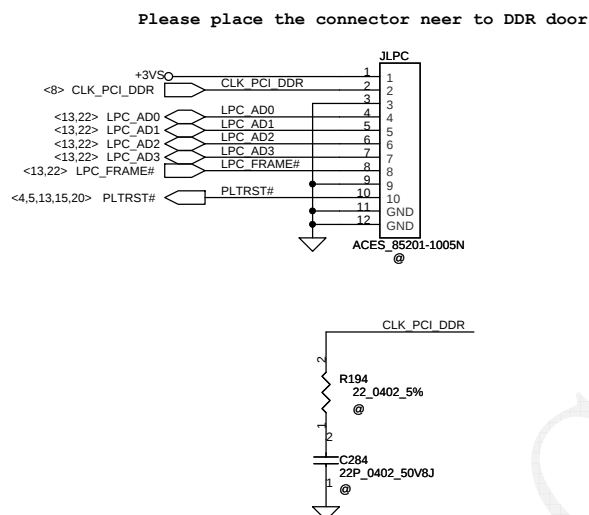


SPI Flash (8Mb*1)

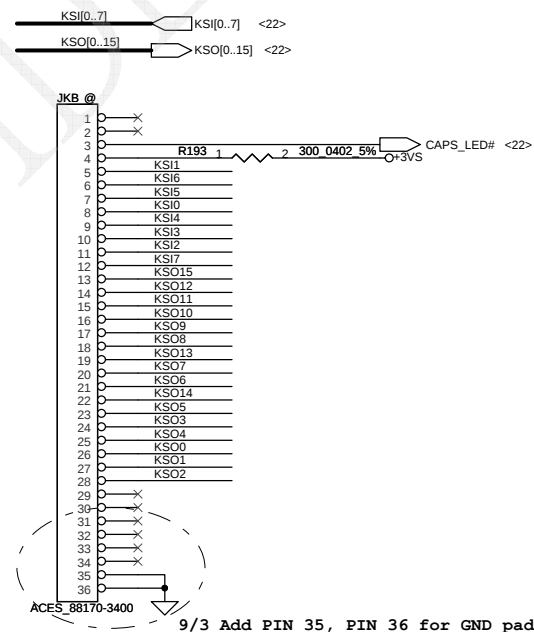


8/14 Change U28 from SA00000XT00 to SA00002T000 for BIOS ROM size
11/12 Change U28 from SA000002T00 to SA0000XT000 for BIOS ROM size

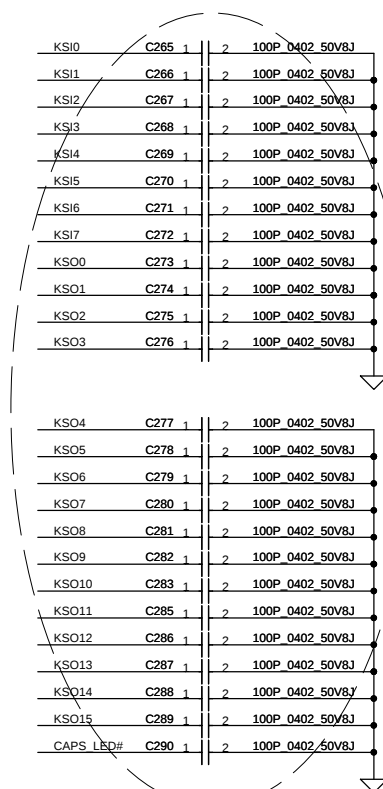
LPC Debug Port



KEYBOARD
CONN.



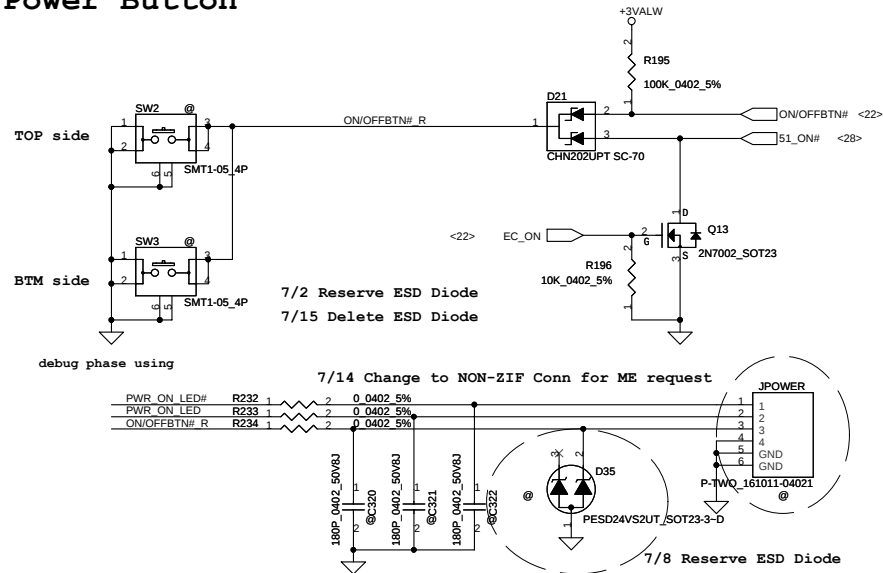
9/3 Add PIN 35, PIN 36 for GND pad



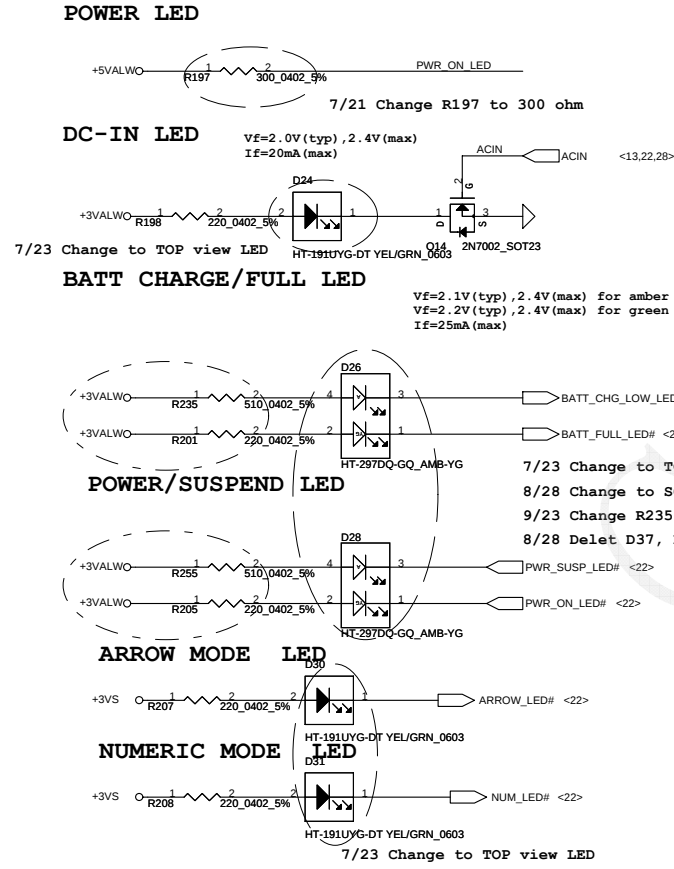
7/8 Add C265 to C290 for EMI request

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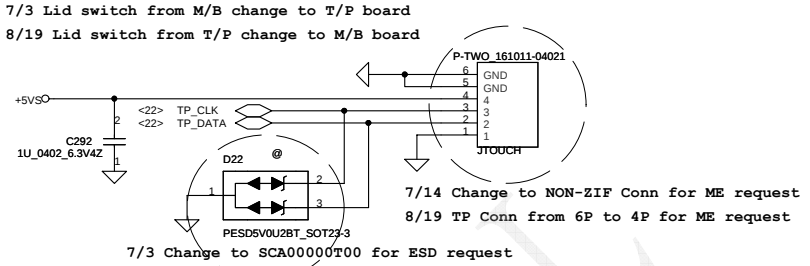
Power Button



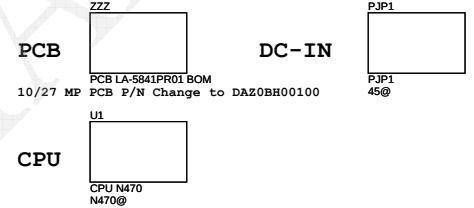
LED Conn



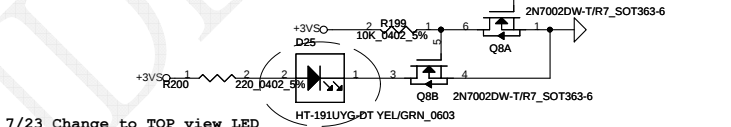
Touch/B Connector



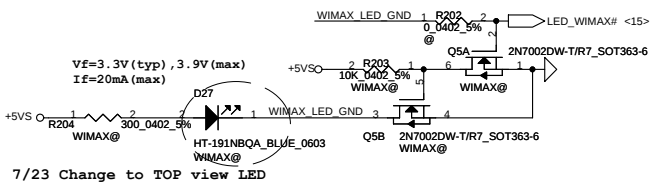
ISPD



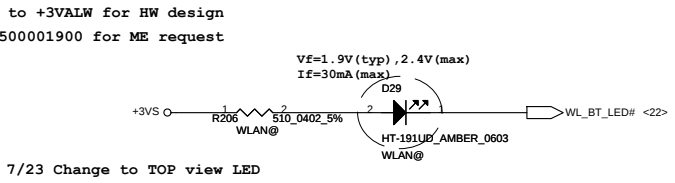
HDD LED



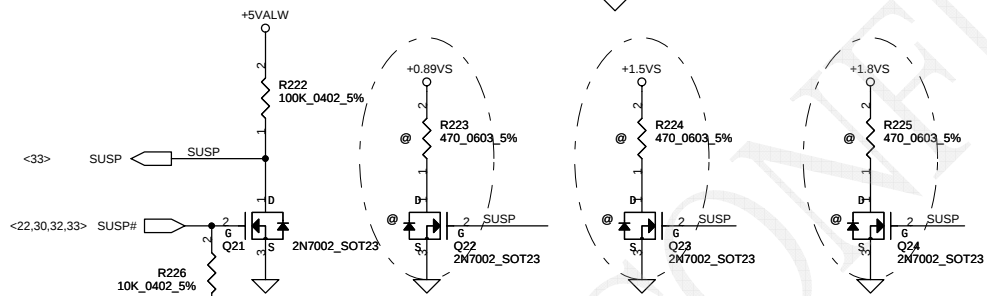
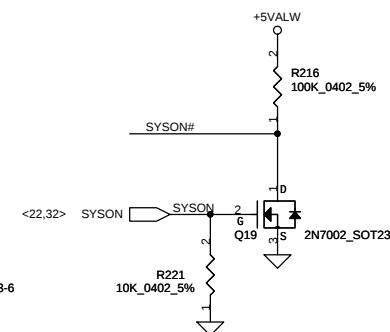
WiMAX&3G LED



WL&BT LED



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[illegible][illegible]

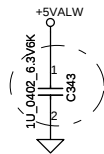
8/31 Change Q20 from SB000

8/31 Change Q20 from SB000002880 to SB000000DW00 for HW design

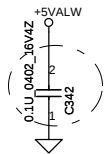
8/14 R237 for HW design

7/9 Add Q29, Q30, R228 for Intel power sequence

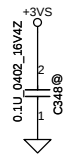
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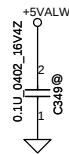
7/21 Placed closed H1



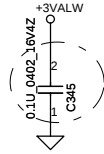
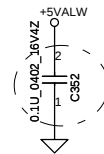
7/21 Placed closed H2



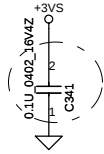
7/23 Placed closed R42



10/5 Placed closed H6



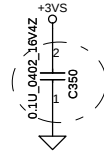
7/21 Placed closed H6



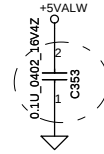
7/21 Placed closed H7



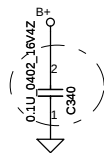
7/21 Placed closed H8



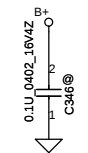
10/5 Placed closed Q2



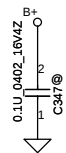
10/5 Placed closed H1



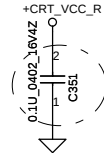
7/21 Placed closed H9



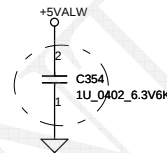
7/23 Placed closed PJ14



7/23 Placed closed PJ9



10/5 Placed closed H4



10/5 Placed closed H2

7/21 These cap for ESD request

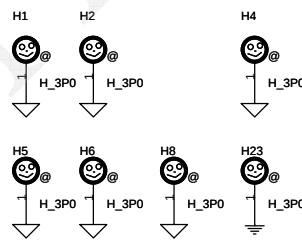
10/5 Add C339, C340~C342, C345, C350~C354 for ESD request

10/5 Change C343 to SE000000K80 for ESD request

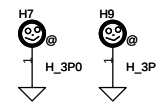
10/6 Change C354 to SE000000K80 for ESD request

Screw Hole

M/B

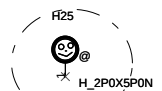
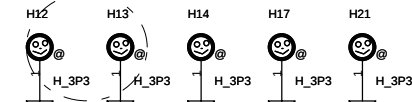


KB

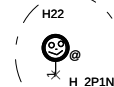


9/23 Change H12, H13 to 3P3 for ME request

FAN

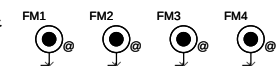


8/28 Add H25 with H_5P0X2P0N for ME request

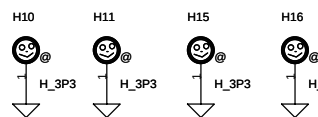


8/19 Add NON PTH hole H22 for Thermal module

FIDUCIAL_C40M80



MINI Card

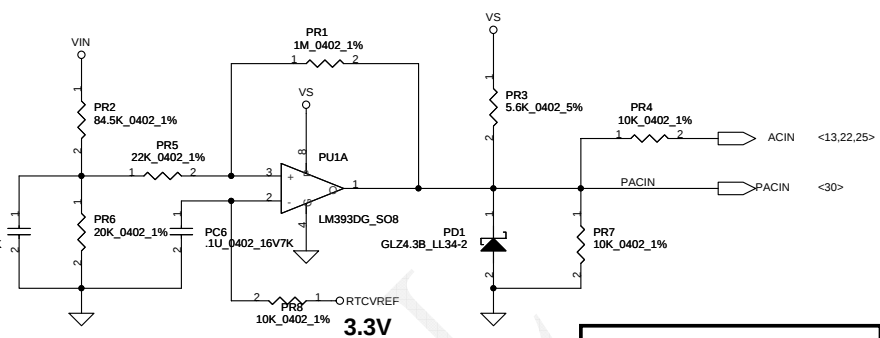
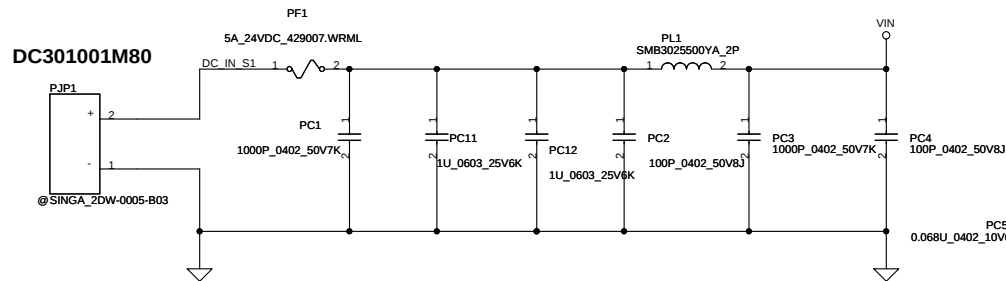


8/28 Add H24 with H_2P0X5P5N for ME request

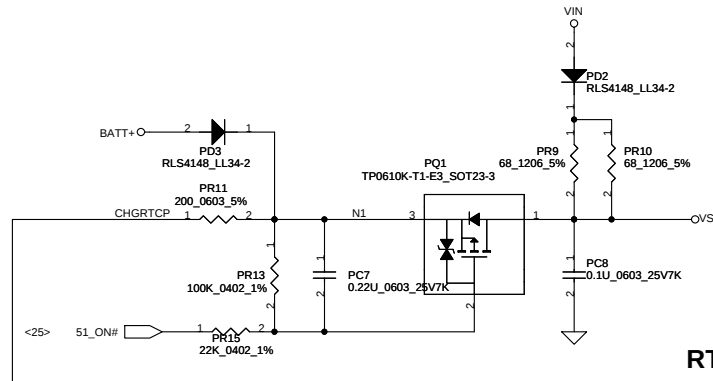
9/2 Det H24 with H_2P0X5P5N for ME request

9/29 Det H19 with H_2P0X5P5N for ME request

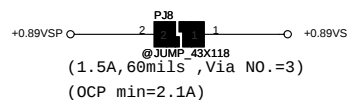
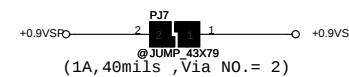
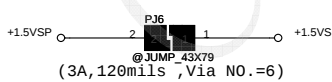
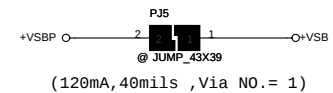
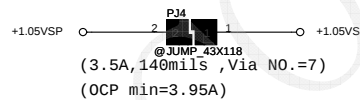
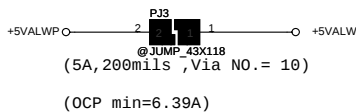
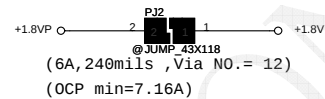
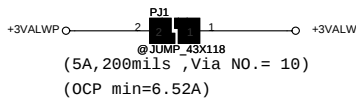
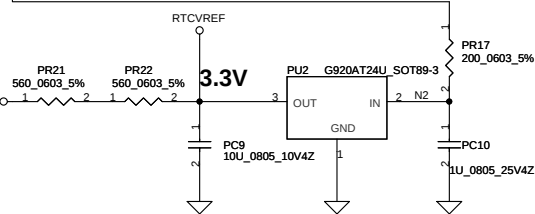
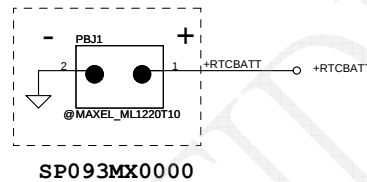
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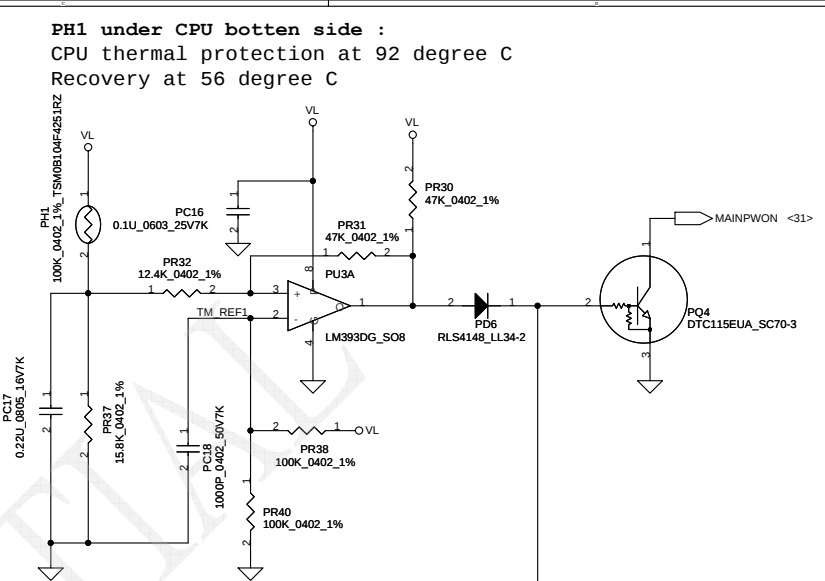
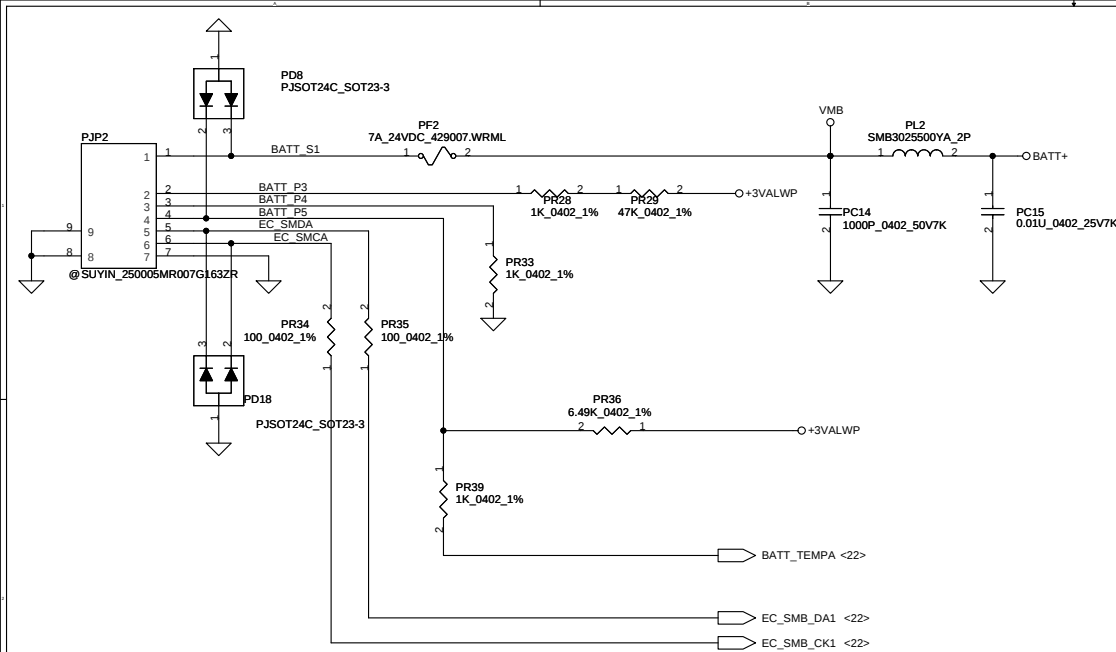
Vin Detector			
High	18.384	17.901	17.430
Low	17.728	17.257	16.976



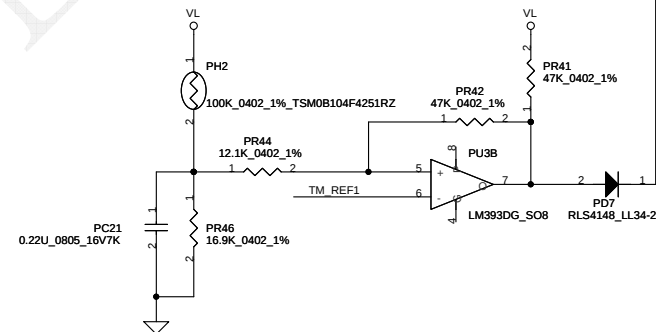
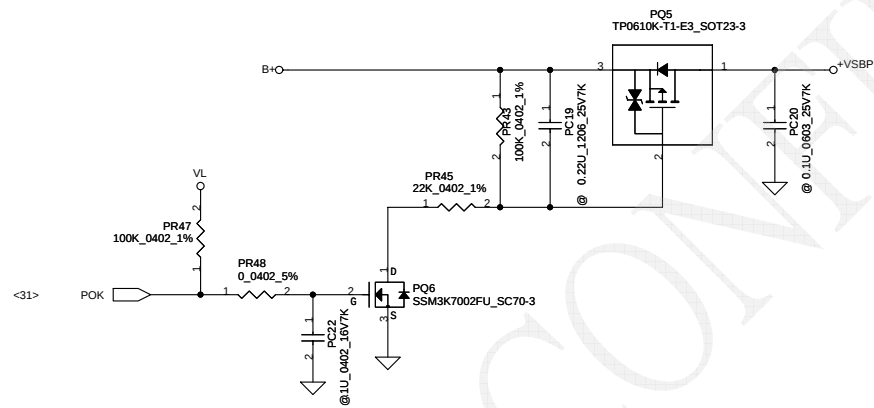
RTC Battery



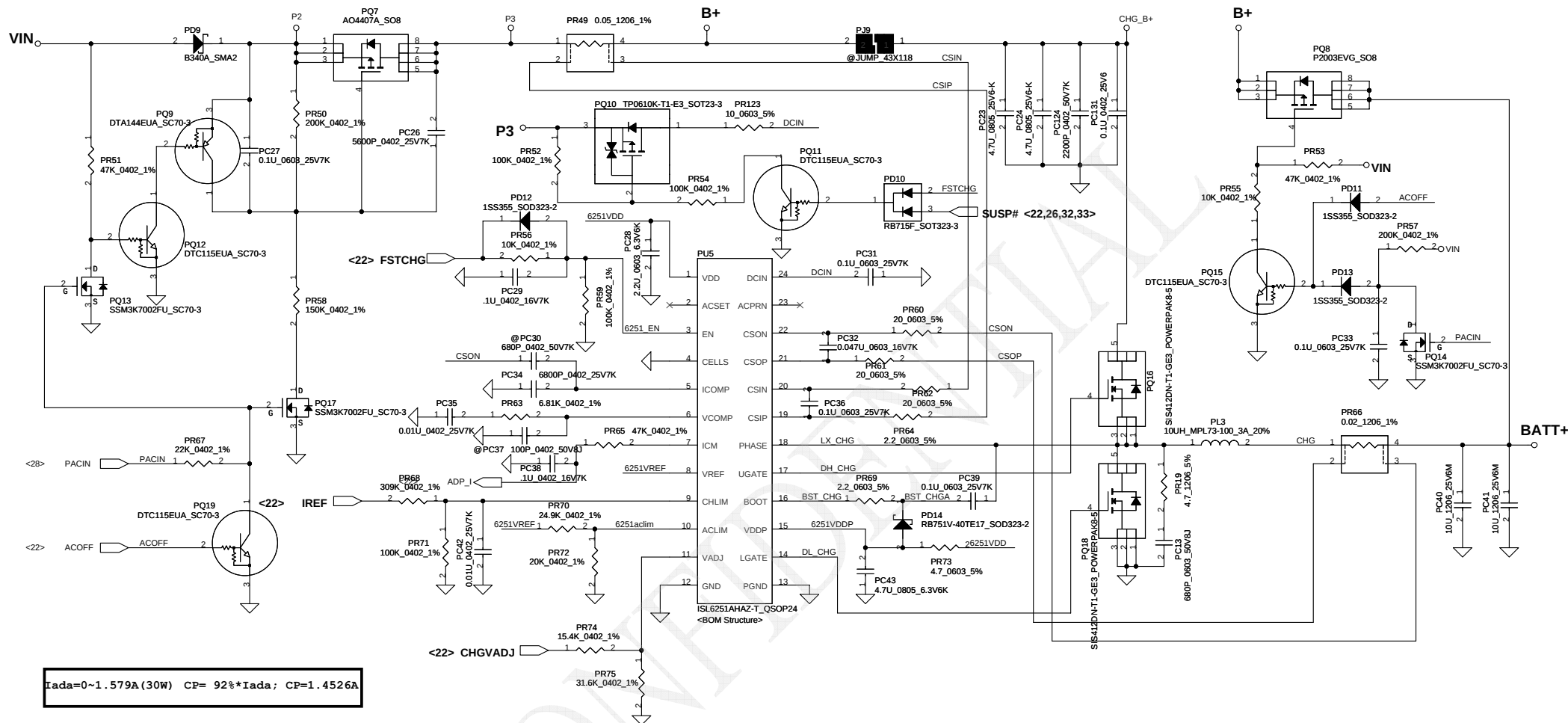
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PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 53 degree C



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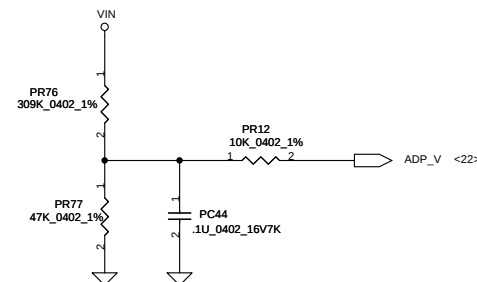
$I_{ada}=0\sim 1.579A(30W)$ $CP=92\% \cdot I_{ada}$; $CP=1.4526A$

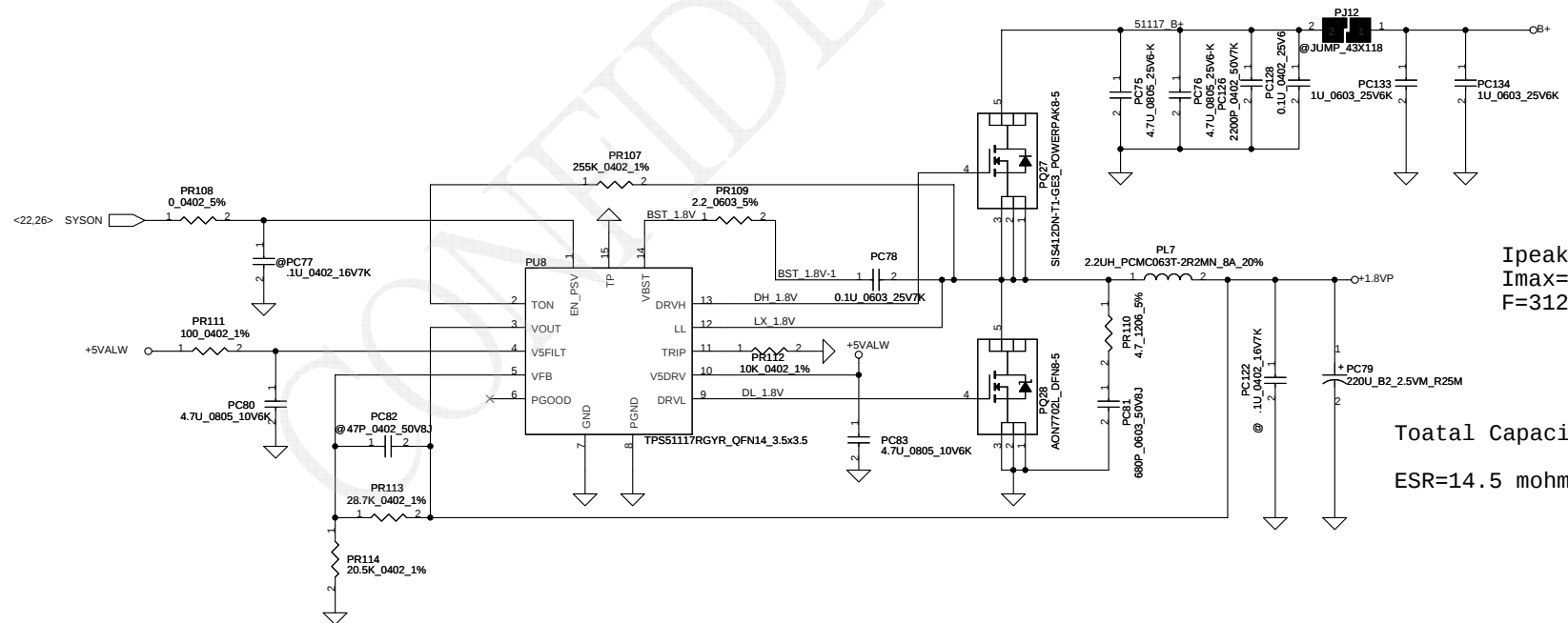
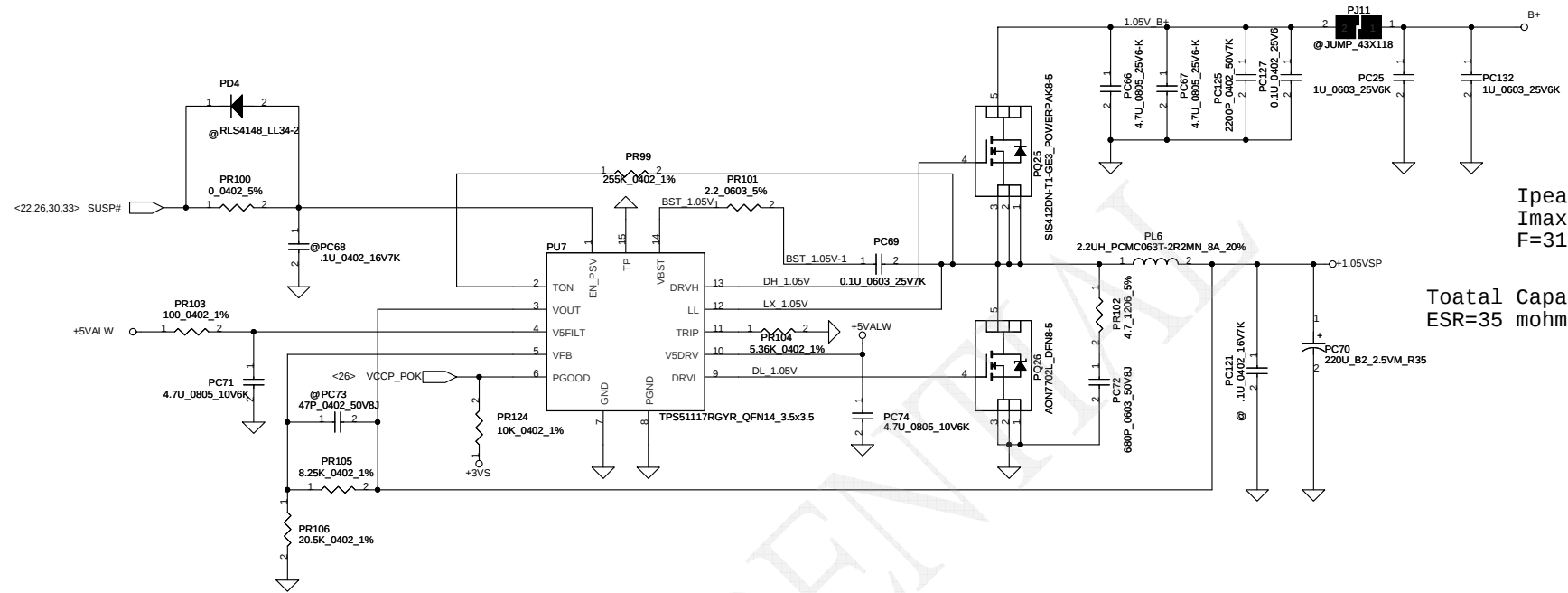
CP mode
 $V_{acim}=2.39 \cdot (20K//152K/(24.9K//152K+20K//152K))=1.0817V$
 $I_{input}=(1/0.05) \cdot ((0.05 \cdot V_{acim})/2.39+0.05)$
 where $V_{acim}=1.0817V$, $I_{input}=1.4526A$

$CC=0.25A \sim 2A$
 $I_{REF}=1.636 \cdot I_{charge}$
 $I_{REF}=0.409V \sim 3.272V$
 V_{CHLIM} need over 95mV

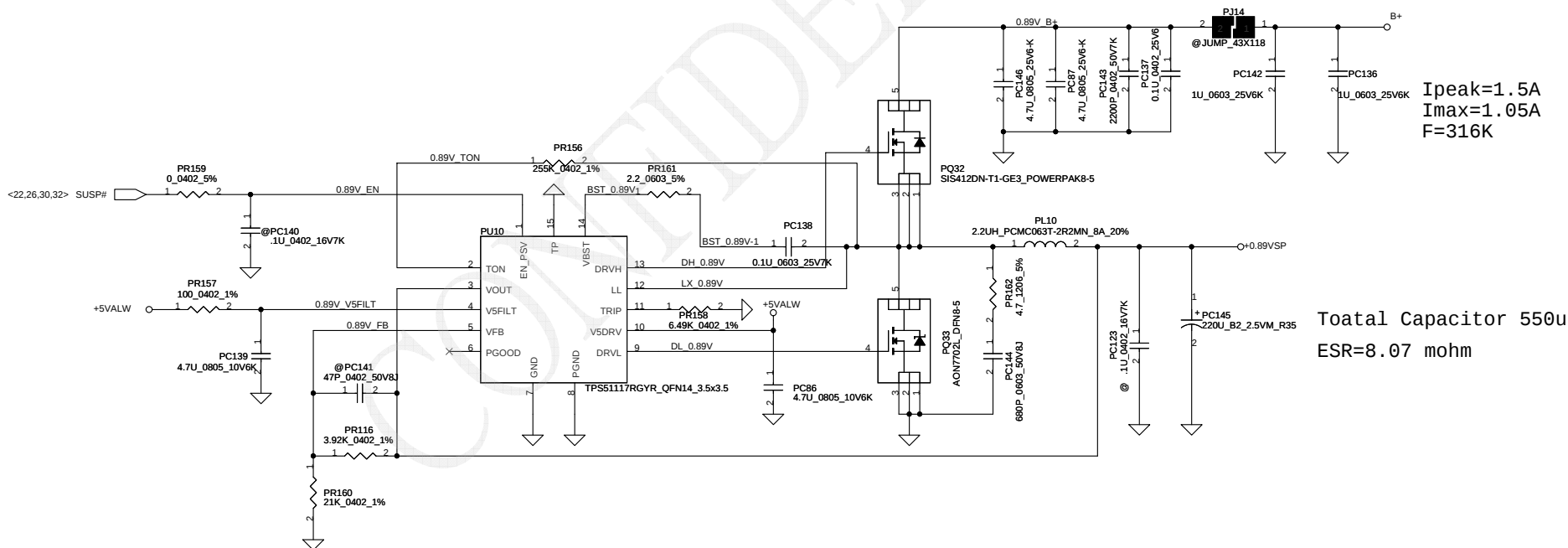
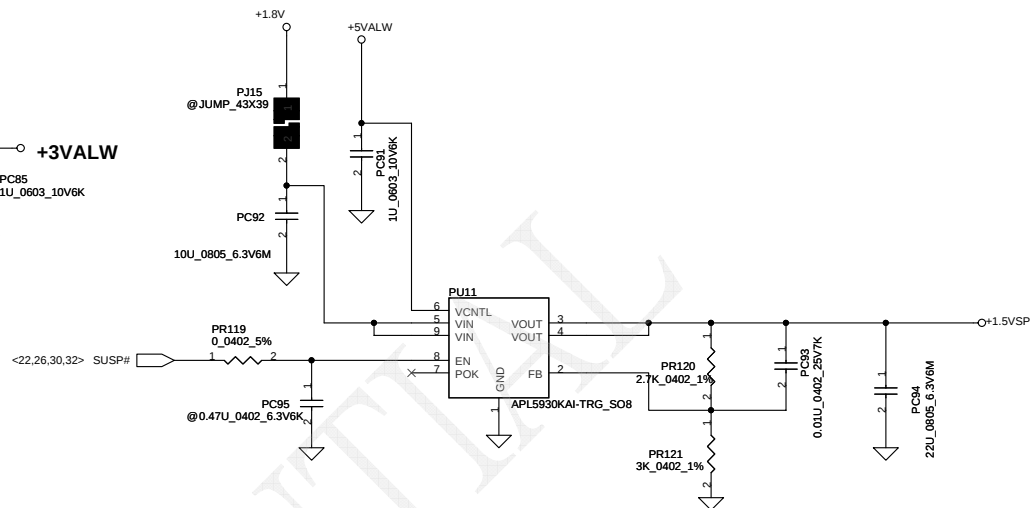
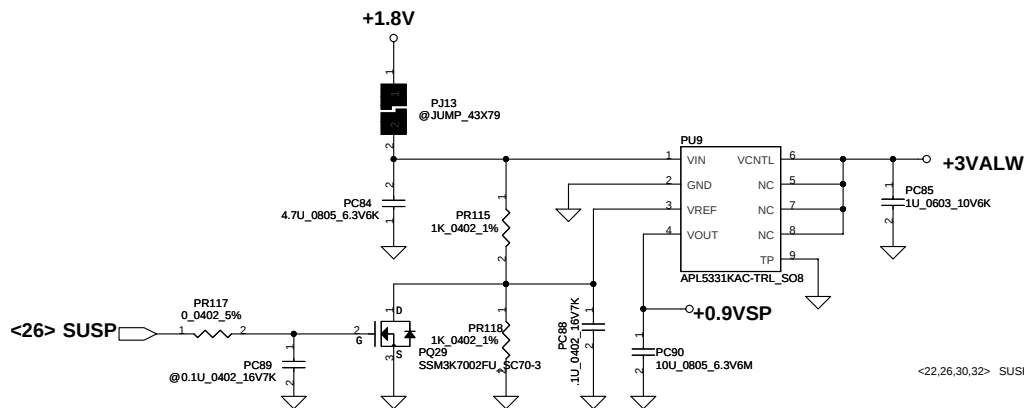
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.2V
4.35V	3.3V

CELLS	VDD	GND	Float
CELL number	4	3	2





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Ipeak=1.5A
Imax=1.05A
F=316K

Toatal Capacitor 550u
ESR=8.07 mohm

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NO	DATE	PAGE	MODIFICATION LIST		PURPOSE
EVT		P37-CPU_CORE	Change	PU15 SA00003DA0L --> SA00003DA00	Choice the A51 material
EVT		P35-1.05VSP/1.8VP	Change	PR124 422 ohm -->10K ohm	Deign change
DVT		P33-CHARGER	Delete	PD15	Deign change(Cause layout)
DVT		P35-1.05VSP/1.8VP	Change	PR104 13.7K-->5.36K	Deign change(OCP point)
DVT		P35-1.05VSP/1.8VP	Change	PR124 the same part number with PR4	Deign change(Use the same part number)
DVT		P32-Battery conn/otp	Reserve	the ESD diode	Deign change
PVT		P37-CPU_CORE	Change	PR209 1.8K-->2.8K	Change the OCP 6A-->9A
PVT		P34-+5VALWP/+3VALWP	Reserve	the sunnber PR82&PR81&PC58&PC59	EMI approve1
PVT		P28-DCIN&DECTOR	Change	PC7 1206-->0603	For cost down
PVT		P32-Battery conn/otp	Add	the ESD diode	EMI require
PVT		P28-DCIN&DECTOR	Change	DC-IN jack DC301009G00	Design change
pre-mp		P29-Battery conn / OTP	Change	PR32 -->12.4K , PR37-->15.8k,PR44-->12.1k,PR46-->16.9K	Thermal commond
pre-mp		P33-0.9VSP/1.5VSP/0.89VP	Change	PR158 2.49K-->6.49K	Design change

PIR (Product Improve Record)

KAVAA LA-5841P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1

DATE PAGE MODIFICATION LIST					PURPOSE
Item	Date	Page	Component	Solution	Request
1)	7/2	9	Reserve	R87 with 0 ohm	For support DPST function
2)	7/2	22	Add	R235 90 ohm bead and C323 with 6P	For EMI request
3)	7/2	13	Reserve	C207 with 22P	For EMI request
4)	7/2	18	Reserve	CA33 with 22P and RA31 with 22 ohm	For EMI request
5)	7/2	16	Change	Change L4 to SM070001310	For EMI request
6)	7/2	18	Reserve	CA34 with 0.01U to GND and RA32 with 4.7K ohm up +3VS	For ESD request
7)	7/2	25	Reserve	D32 with SCA00000R00	For ESD request
8)	7/3	25	Change	Lid switch from M/B change to T/P board	For design change
9)	7/3	19	Change	Change DA3,DA4,D22 to SCA00000T00	For ESD request
10)	7/3	4	Reserve	D33,D34 with SC300000000	For ESD request
11)	7/3	16	Reserve	D23 with SC300000000 from Sub board to M/B	For ESD request
12)	7/6	22	Change	Change R235 to L6 with SM010009E00	For EMI request
13)	7/8	24	ADD	Add C265-C290 with SE071101J80	For EMI request
14)	7/8	16	Swap	Pin swap for AGND	For layout
15)	7/8	18	Reserve	R235 withSD028000080	For EMI request
16)	7/8	27	Modify	Modify screw hole location	
17)	7/8	25	Reserve	D32 with SCA00000R00	For ESD request
18)	7/8	16	Reserve	D36 with SC300000000 from Sub board to M/B	For ESD request
19)	7/8	07	Add	C216,C217,C238,C291 with SE070104Z80	For EMI request
20)	7/9	26	Add	D29, D30 with SB570020020 and R228 with SD028100280	For power sequence
21)	7/9	13	Add	C293 with SE070104Z80	
22)	7/9	25	Change	R232, R233, R234 with SD028000080	Need to EMI confirm on EVT
23)	7/9	18,19	Modify	modify 2 SPK solution	For TOSHIBA request
24)	7/10	20	Change	UL1 with SA00002XC10	For low power solution
25)	7/10	16	Change	JUSBC1 to DC233004Q00	For ME suggest
26)	7/10	16	Swap	USB20_P0_R USB20_N0_R, USB20_P0_R_S, USB20_N0_R_S	For layout request
27)	7/10	10	Add	J2	For cost down PolySwitch
28)	7/13	8	Add	C296, C297 with SE071220J80	For RF request
29)	7/13	8	Add	C300, C301 with SE068330K80	For RF request
30)	7/13	8	Add	C302, C303, C324 with SE068330K80	For RF request
31)	7/13	8	Add	C325, C326, C327 with SE068330K80	For RF request
32)	7/13	8	Change	R53, R54, R57 to SM01000B200	For RF request
33)	7/13	8	Add	C328, C329, C330 with SE071470J80	For RF request
34)	7/13	19	Reserve	CA25 with SE070104Z80	For RF request
35)	7/14	21	Delete	YC1, CC12, CC13	For cost down
36)	7/14	25	Change	JTOUCH1 to NON-ZIF	For ME suggest
37)	7/14	25	Change	JPOWER1 to NON-ZIF	For ME suggest
38)	7/15	22	Change	INVT_PWM from PIN 21 change to PIN 25	For EC suggest
39)	7/15	22	Change	USB_CHG_EN# from PIN 68 change to PIN 29	For EC suggest
40)	7/15	5	Change	SB to CPU signal to CPU side	For placement
41)	7/15	16	Swap	USB20_N3 and USB20_P4 location	For layout request
42)	7/15	25	Delete	D32	For ESD request
43)	7/16	17	Delete	BT and Camera BTO item	For BOM request
44)	7/16	19	Delete	MIC BTO item	For BOM request
45)	7/16	21	Change	For RC8 change to reserve	For realtek request
46)	7/16	23	Delete	G-senser BTO item	For BOM request
47)	7/16	16	modify	USB_OC#0 dis-connect to +USB_VCCB	For schematic error
48)	7/16	26	modify	Change Q22 pull up from 0.89V to 0.89VS	For schematic error
49)	7/16	9	Reserve	C331 and C332 with SE071100J80	For EMI request
50)	7/16	9	Reserve	C333 and C334 with SE071100J80	For EMI request
51)	7/17	23	Change	U17 from R5F211B4D31SP change to R5F211B4D34SP	For TOSHIBA request
52)	7/17	12	Change	Reassign Tiger point USB port	For TOSHIBA concern
53)	7/17	21	Delete	RC13	For cost down
54)	7/17	20	Change	JLAN from SANTA 130452-3 13P-T to Santa_130452-8 8P-T	For not support LAN LED fu
55)	7/17	20	Delete	RL7, RL8, RL9, RL11, CL16, CL21	For not support LAN LED fu
56)	7/17	15	Change	R156, R157 for JWLAN1 change to JGPS1	For debug
57)	7/20	4	Add	R238, R239 with SD028100280	For Ref board design
58)	7/20	5	Add	C335 with SE000000K80	For Ref board design
59)	7/20	5	Reserve	C336 with SE074221K80	For Ref board design
60)	7/20	13	Delete	EC_THERM# pull up	Follow NIM10
61)	7/20	13	Add	T43, T44	Follow NIM10
62)	7/20	13	Add	SLPIOVR pull up 8.2k to +3vs	Follow NIM10
63)	7/21	3	Swap	XDP_TRST#, XDP_TDO, XDP_TDI, XDP_TCK, XDP_TMS	For layout request
64)	7/21	7	Reserve	C60 with SE107225K80	

PIR (Product Improve Record)

KAVAA LA-5841P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1-->0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
65)	7/21	8	Reserve	C303,C324,C325,C326,C327,C296,C297,C300,C301
66)	7/21	8	Change	WWAN CLKREQ# from REQ4 to REQ11
67)	7/21	9	Change	C331 to Shunt Capacitor
68)	7/21	15	Change	C334 to Shunt Capacitor
69)	7/21	17	Swap	USB20_N7, USB20_P7
70)	7/21	19	Add	RA33, RA34 with SD028820180
71)	7/21	25	Change	R197 to 300ohm
72)	7/21	4	Add	R137 to GND
73)	7/21	13	Add	R240 pull up to +RTCBATT
74)	7/21	13	Change	C156 with SE000000KR80
75)	7/21	27	Add	C339~C345 with SE070104Z80
76)	7/22	8	Add	R241 pull up to +3VS
77)	7/22	19	Add	RA33~RA40, CA35~CA38
78)	7/22	8	Delete	R64, R66
79)	7/22	8	Add	R242~R253
80)	7/23	20	Change	JLAN from Santa_130452-8 8P-T to SANTA_130452-6
81)	7/23	21	Change	JCARD with TAITW_PSDAT3-09GLASIN14N
82)	7/23	21	Change	DC1 for TOP view LED
83)	7/23	25	Change	D24~D31 for TOP view LED
84)	7/23	27	Reserve	C346~C348 with SE070104Z80
85)	7/27	4	Change	C302 to GND for +1.8V pull up
86)	7/27	16	Swap	USB20_P4_R_S and USB20_N4_R_S
87)	8/14	4	Add	DDR_VREF net name
88)	8/14	5	Add	CRT_IRTN net name
88)	8/14	5	Add	DAC_IREF net name
89)	8/14	5	Change	Net name from H_GTLREF to +H_GTLREF
90)	8/14	5	Change	Net name from H_EXTBGREF to +H_EXTBGREF
91)	8/14	8	Add	R250 pull up with SD028470080
92)	8/14	13	Add	R254 pull down with SD028100380
93)	8/14	17	Swap	USB20_N7, USB20_P7
94)	8/14	18	Add	R235 with SD028000080
95)	8/14	18	Add	Net name to HP_L_R and HP_R_R
96)	8/14	18	Add	Net name to CPVEE
97)	8/14	26	Add	R237 with SD028200380
98)	8/14	9	Add	R87 with SD028000080
99)	8/14	9	Det	R88 with SD028000080
100)	8/14	24	Change	U28 from SA000000XT00 to SA00002TO00
101)	8/19	25	Det	Lid switch from T/P change to M/B board
102)	8/19	17	Add	U22, C332, C333 for Lid function
103)	8/19	21	Change	JCARD for push pull Conn
104)	8/19	24	Change	JFAN to SP02000JR00
105)	8/19	16	Change	JUSBC to DC233004W00
106)	8/19	25	Change	JTOUCH to SP01000WX00
107)	8/19	27	Add	H22 NON PTH hole
108)	8/21	16	Add	USB_CHG_EN# has to be connected to OE# pin
109)	8/24	4	Change	+DDR_VREF to DDR_VREF
110)	8/24	5	Det	CRT_IRTN net name
111)	8/24	5	Change	+H_GTLREF to H_GTLREF
112)	8/24	5	Change	+H_EXTBGREF to H_EXTBGREF
113)	8/24	16	Change	U12 to SA00002XX00
114)	8/24	8	Change	Net name to FSB for U3.2
115)	8/24	10	Change	D1, D2, D3
116)	8/24	17	Change	JSATA to ALLTO_C16674-12204-L
117)	8/24	18	Change	R235 to RA21
118)	8/24	20	Change	JLAN for Deep connector
119)	8/24	20	Add	Connect ISOLATEB to EC
120)	8/24	21	Det	RC9
121)	8/23	27	Reserve	C343, C342, C345, C341, C339, C340
122)	8/27	8	Det	C93, C94, C95, C102
123)	8/27	8	Add	C303, C324, C325, C326, C327 to GND
124)	8/27	8	Det	296, C297
125)	8/28	27	Add	H24 with H_2P0X5P5N
126)	8/28	25	Change	SC5191UD000 and SC591UYG000
127)	8/31	27	Add	H25 with H_5P0X2P0N
128)	8/31	26	Change	Q20 from SB0000002880 to SB000000DW00
129)	9/1	13	Change	R125 to SM010027780
130)	9/1	13	Add	C207 to SE071100J80
131)	9/2	27	Det	H24 with H_2P0X5P5N
132)	9/3	16	Add	PIN 21, PIN 22 on JUSB
132)	9/3	16	Add	PIN 3, PIN 4 on JSPKR, JSPKL
132)	9/3	16	Add	PIN 35, PIN 36 on JKB
133)	9/4	7	Reserve	C66, C67, C68, C69, C72, C75, C77, C78, C79, C81, C83, C84, C85

PIR (Product Improve Record)

NPVAA LA-5841P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2-->0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
134)	9/23	13	Change	RP17 to R256, R257, R258
135)	9/23	27	Change	H12, H13 to 3P3
136)	9/23	25	Change	R235, R255 to SD028220080 and +5VALW to +3VALW
137)	9/28	16	Det	D36 with SC300000000
138)	9/28	10	Reserve	Reserve F1 for cost down PolySwitch
140)	10/5	27	Add	C339, C340-C342, C345, C350-C354 with SE070104Z80
141)	10/5	27	Change	C343 to SE000000K80
142)	10/5	18	Add	RA7 and RA11 with SD013000080
143)	10/5	26	Reserve	R223~R225, R229~R231 Q22~Q24, Q26~Q28 for HW cost down
144)	10/6	25	Change/Det	Delet D37, D38 and Change D26 and D28 to SC500001900
145)	10/6	15	Change	R156, R157 for JWLAN change to JGPS
146)	10/6	27	Change	C354 to SE000000K80

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NPVAA LA-5841P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3-->1.0

NO	DATE	PAGE	MODIFICATION	LIST	PURPOSE
147)	10/19	4	Change	footprint T5, T6 and T7 from TPC24 to TPC12	For layout request
148)	10/20	16,17	Det	L4, and L5	For EMI request
149)	10/27	19	Det	DA4 and DA5	For ESD request
150)	11/12	24	Change	U28 from SA000002T00 to SA0000XT000	For BIOS ROM size

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