1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,CORNHOLE,K19

PVT 04/24/2009

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7892	1	SCHEM,CORNHOLE,K19	SCH	CRITICAL	
820-2523	1	PCBF,CORNHOLE,K19	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Apr 24 15:23:24 2009

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

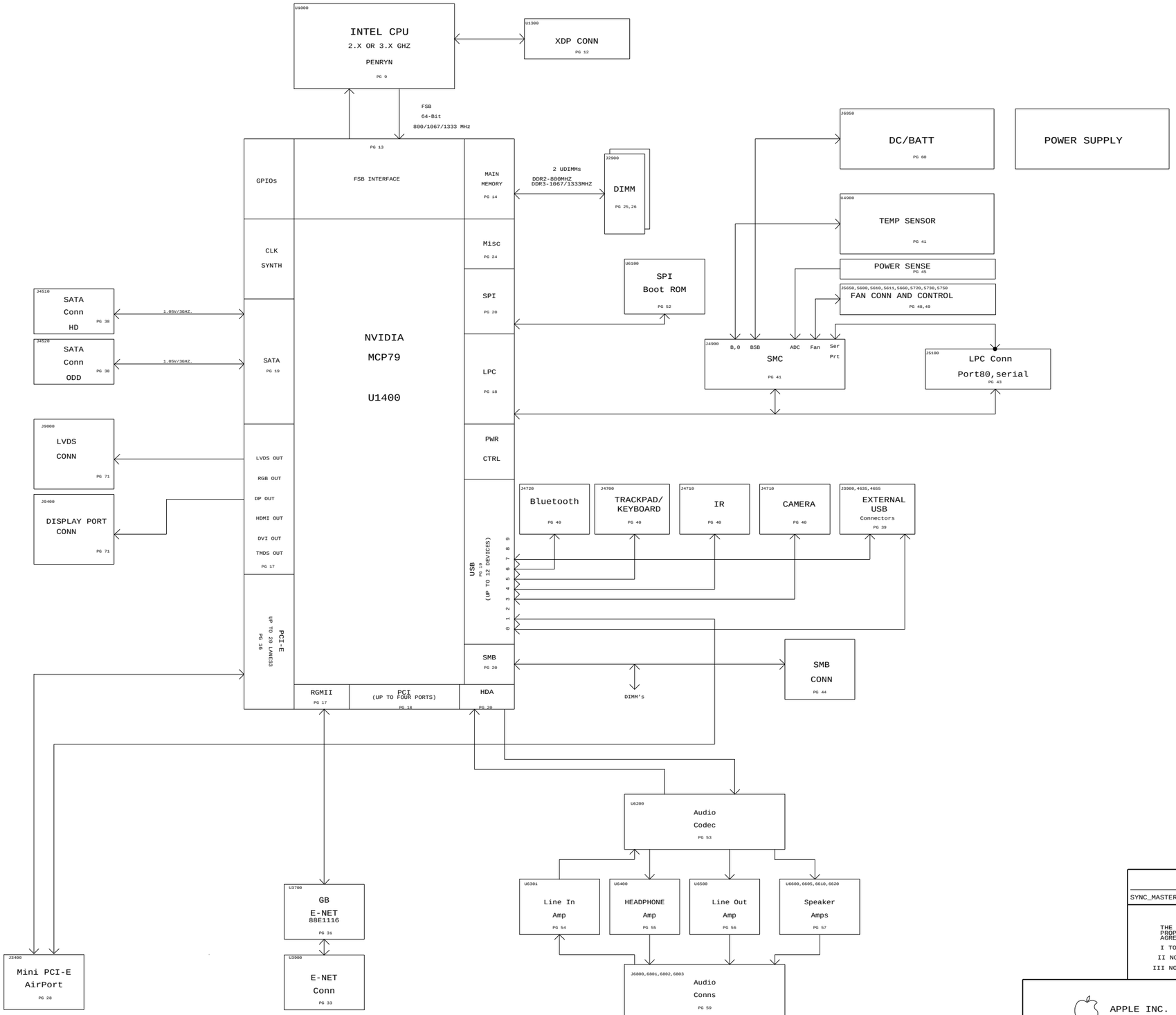
MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

APPLE INC.

TITLE
SCHEM,MBP 15MLB

DRAWING NUMBER 051-7892
REV. A.0.0
SHT 1 OF 97



System Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 2 OF 97	

M98 POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
DCIN(16.5V)
6A FUSE
LIO_DCIN_ISENSE
U5705
ENABLES
VIN
(PAGE 60)
PBUS SUPPLY/
BATTERY CHARGER
ISL6258A
U7000
VOUT
CHGR_EN
(S5)
D6905
D6905
PPVIN_G3H_P3V42G3H
PBUSB_VSENSE
Q5315
ENABLE
3.425V G3HOT
LT3470
U6990
(PAGE 59)
PP3V42_G3H_REG
SMC PWRGD
RN5VD30A-F
U5000
(PAGE 43)
SMC_RESET_L
8A FUSE
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
SMC_GPU_VSENSE
U5715
SMC_BATT_ISENSE
GPU VCORE
VIN
ISL6263B
U8900
EN_PSV
VOUT
PGOOD
(PAGE 78)
PM_GPUVCORE_EN
U5498
GPUVCORE_IOUT
PPVCORE_GPU_REG
(18A MAX CURRENT)
GPUVCORE_PGOOD
CPUVTTS0_EN
VIN
EN_PSV
VOUT
1.05V
TPS51117
U7600
(PAG 66)
PGOOD
PPCPUVTT_S0_REG
(6A MAX CURRENT)
CPUVTTS0_PGOOD
U2830
VR_PWRGD_CLKEN
MCP79
CK_PWRGD
VRMPWRGD
PWROK
CPUPWRGD(GPIO49)
U1400
(PAGE 14~22)
PWRBTN#
PLTRST*
RSMRST*
PLT_RST_L
CPU_PWRGD
MCP_PS_PWRGD
U2850
J6950
3S2P
(9 TO 12.6V)
BATT_POS_F
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R
CPU VCORE
VIN
ISL9504B
U7100
VR_ON
VOUT
PGOOD
(PAGE 61)
IMVP_VR_ON_R
U5400
SMC_CPU_VSENSE
CPUVCORE_IOUT
PPVCORE_CPU_S0
VR_PWRGD_CLKEN_L
VR_PWRGOOD_DELAY
CPU
U1000
(PAGE 10,11)
PWRGOOD
RESET*
PPBUS_G3H
Q7920
PP5V_S0_FET
P5VS0_SS
Q7900
PP5V_S3_FET
P5VS3_SS
P1V1GPU_EN
EN1 VIN
1.103V(L/H)
VOUT1
PP1V1_S0GPU_REG
P1V8FB_EN
EN2
1.8V(R/H)
VOUT2
PP1V8_GPU_REG
TPS51124
U9500
(PAGE 82)
MCP79
SLP_S5#(H17)
SLP_S3#(G17)
U1400
(PAGE 14~22)
P3V3S3_EN
P5VS3_EN
LIO_S3_EN
SMC
U4900
(PAGE 42)
P60
SMC_PM_G2_EN
(S5)
U7859
VIN
5V
(L/H)
3.3V
(R/H)
VOUT1
VOUT2
TPS51125
U7201
(PAGE 62)
EN0
PGOOD1,2
VREG3
PP5V_S5_REG
(8A MAX CURRENT)
PP3V3_S5_REG
(5.5A MAX CURRENT)
PP5V_S3
PP3V3_S5
PP3V3_S3_FET
P3V3S5_EN
P3V5V3_S5_PGOOD
Q7910
P3V3S3_SS
Q7930
PP3V3_S0GPU_FET
P3V3S0_SS
Q7970
PP3V3_S0_FET
P3V3GPU_SS
Q3810
P3V3_ENET_FET
P3V3ENET_EN_L
ISL8009
U7750
(PAGE 66)
V4
PP1V05_S5_MCP
U7400
VIN
EN/PSV
ENL
SC417
(PAGE 64)
VOUT
PGOOD
PP5V_RT_REG
P5V_RT_EN
P5V_RT_PGOOD
Q3805
WOW_EN
PM_WLAN_EN_L
Q3801
PM_ENET_EN
PM_ENET_EN_L
Q3800
WOL_EN
SMC_ADAPTER_EN
PM_ENET_EN_L
RC DELAY
PM_SLP_S3_L
VIN
GOSHAWK6P
U9701
ENA
(PAGE 84)
VOUT
BKLT_EN
PPVOUT_S0_LCDBKLT
VIN LTC3407
RUN2
RUN1
U3850
(PAGE 33)
VOUT1
VOUT2
P1V2ENET_EN
ENETAVDD_EN
PP1V9_ENET_REG
PP1V2_ENET_REG
SMC
RSMRST_OUT(P15)
PWRGD(P12)
99ms DLY
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PWR_BUTTON(P90)
P17(BTN_OUT)
U4900
(PAGE 42)
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
PM_RSMRST_L
IMVP_VR_ON
PLT_RST*
PM_PWRBTN_L
RST*
SMC_RESET_L
P1V05S0_PGOOD
P5VRIGHT_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
P1V8S0_PGOOD
P1V5S0_PGOOD
S0PGOOD_PWROK
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
PPVIN_S0_DDRREG_LDO
DDRREG_EN
DDRVTT_EN
VIN
VLDOIN
S5 1.8V
S3 0.9V
VOUT1
VOUT2
TPS51116
U7300
(PAGE 63)
PPDDR_S3_REG
(12A MAX CURRENT)
PPVTT_S0_DDR_LDO
RST*
PP5V_S0
PP3V3_S0
PP1V5_S0_REG
V1
V2
V3
V4
LTC2900
U7870
(PAGE 68)
RC DELAY
P5VRIGHT_EN
P1V8S0_EN
MCPDDR_EN
CPUVTTS0_EN
MCPCORES0_EN
P5VS0_EN
(S0)
P3V3S0_EN
(S0)
PBUSVSENS_EN
(S0)
PM_SLP_S3_DELAY_L
(S0)
MCP_CORE
EN2
EN1
1.1V
VOUT1
VOUT2
ISL6236
U7500
(PAGE 65)
MCPCORES0_EN
P1V05S0_EN
MCPCPCORE_S0_REG
PP5V_RT_REG
(25A MAX CURRENT)
(5A MAX CURRENT)

Power Block Diagram

SYNC_MASTER=T18_MLB
SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 3 OF 97	

Power Block Diagram

SYNC_MASTER=N/A

SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0

SCALE	SHT	OF
NONE	4	97

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9965	PCBA,2.66GHZ,256SAM_VRAM,HB_AUDIO,K19	K19_COMMON,DEVEL_BOM,EEE_6XN,CPU_2_66GHZ,FB_256_SAMSUNG
630-9966	PCBA,2.66GHZ,256HYN_VRAM,HB_AUDIO,K19	K19_COMMON,DEVEL_BOM,EEE_6XP,CPU_2_66GHZ,FB_256_HYNIX
630-9967	PCBA,2.80GHZ,512SAM_VRAM,HB_AUDIO,K19	K19_COMMON,DEVEL_BOM,EEE_6XQ,CPU_2_80GHZ,FB_512_SAMSUNG
630-9968	PCBA,2.80GHZ,512HYN_VRAM,HB_AUDIO,K19	K19_COMMON,DEVEL_BOM,EEE_6XR,CPU_2_80GHZ,FB_512_HYNIX
630-9969	PCBA,3.06GHZ,512SAM_VRAM,HB_AUDIO,K19	K19_COMMON,DEVEL_BOM,EEE_6XS,CPU_3_06GHZ,FB_512_SAMSUNG
630-9970	PCBA,3.06GHZ,512HYN_VRAM,HB_AUDIO,K19	K19_COMMON,DEVEL_BOM,EEE_6XT,CPU_3_06GHZ,FB_512_HYNIX
085-0736	K19 MLB DEVELOPMENT	K19_DEVEL_PVT

K19 BOM Groups

BOM GROUP	BOM OPTIONS
K19_COMMON	ALTERNATE,COMMON,K19,K19_COMMON1,K19_COMMON2,K19_PROGPARTS
K19_COMMON1	BOOT_MODE_USER,DPMUX_EN_S0,DP_CA_DET_EG_PLD,DP_ESD,EG_PWRSEQ_HW,EXTRACT_BUFF
K19_COMMON2	GMUX_1V8,GPUVID_1P00V,GPU_SS_INT,ISL6258A,MCP_B03,MCPSEQ_SMC,MIKEY,MUXGFX,SMC_DEBUG_YES,XDP
K19_DEVEL_ENG	BMON_ENG,DEBUG_ADC,GMUX_JTAG,LPCPLUS,VREFMRGN,XDP_CONN
K19_DEVEL_PVT	BMON_PROD,LPCPLUS,NO_VREFMRGN,XDP_CONN
K19_PROD	BMON_PROD,LPCPLUS_NOT,NO_VREFMRGN
K19_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4,VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX

Bar Code Labels / EEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XN]	CRITICAL	EEE_6XN
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XP]	CRITICAL	EEE_6XP
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XQ]	CRITICAL	EEE_6XQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XR]	CRITICAL	EEE_6XR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XS]	CRITICAL	EEE_6XS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XT]	CRITICAL	EEE_6XT

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3761	1	IC,PDC,SLGLA,PRQ,2.66G,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3682	1	IC,PDC,SLGEM,PRQ,2.80G,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_80GHZ
337S3744	1	IC,PDC,SLGKH,QS,3.06G,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_3_06GHZ
338S0710	1	IC,MCP79MXT-B3,35X35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0694	1	IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P LQFP	U3700	CRITICAL	
338S0654	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
341S2384	1	IR,ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2462	1	IC,SMC,DEVELOPMENT,K19	U4900	CRITICAL	SMC_PROG
341S2503	1	IC,PSOC +W/USB,56PIN,MLF,K19	U5701	CRITICAL	TPAD_PROG
335S0384	1	IC,32MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2456	1	IC,EFI ROM,DEVELOPMENT,K19	U6100	CRITICAL	BOOTROM_PROG
338S0554	1	IC,GPU,55nm,NV G96-GS,BGA969,LF	U8000	CRITICAL	
333S0507	4	IC,SGRAM,GDDR3,16Mx32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0511	4	IC,SGRAM,GDDR3,32Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0506	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0736	1	K19 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
353S1681	353S1294		ALL	LM4911,QFAMP, GBW
152S0276	152S0683		ALL	Maglayers alt to Dale/Vishay
341S2367	341S2366		ALL	Macronix alt to SST
152S1034	152S0867		ALL	Toko alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0915	152S0796		ALL	Maglayers alt to Cyntec IND
128S0220	128S0262		ALL	KEMET ALT TO SANYO
127S0062	127S0108		ALL	Rdmr ALT TO KEMET
152S0968	152S0966		ALL	Maglayer alt to Delta
311S0447	311S0406		ALL	NXP alt to TI
338S0714	338S0554		ALL	Low Leakage G96 GPU
107S0138	107S0074		ALL	CYNTEC alt to YDS
107S0139	107S0075		ALL	CYNTEC alt to YDS

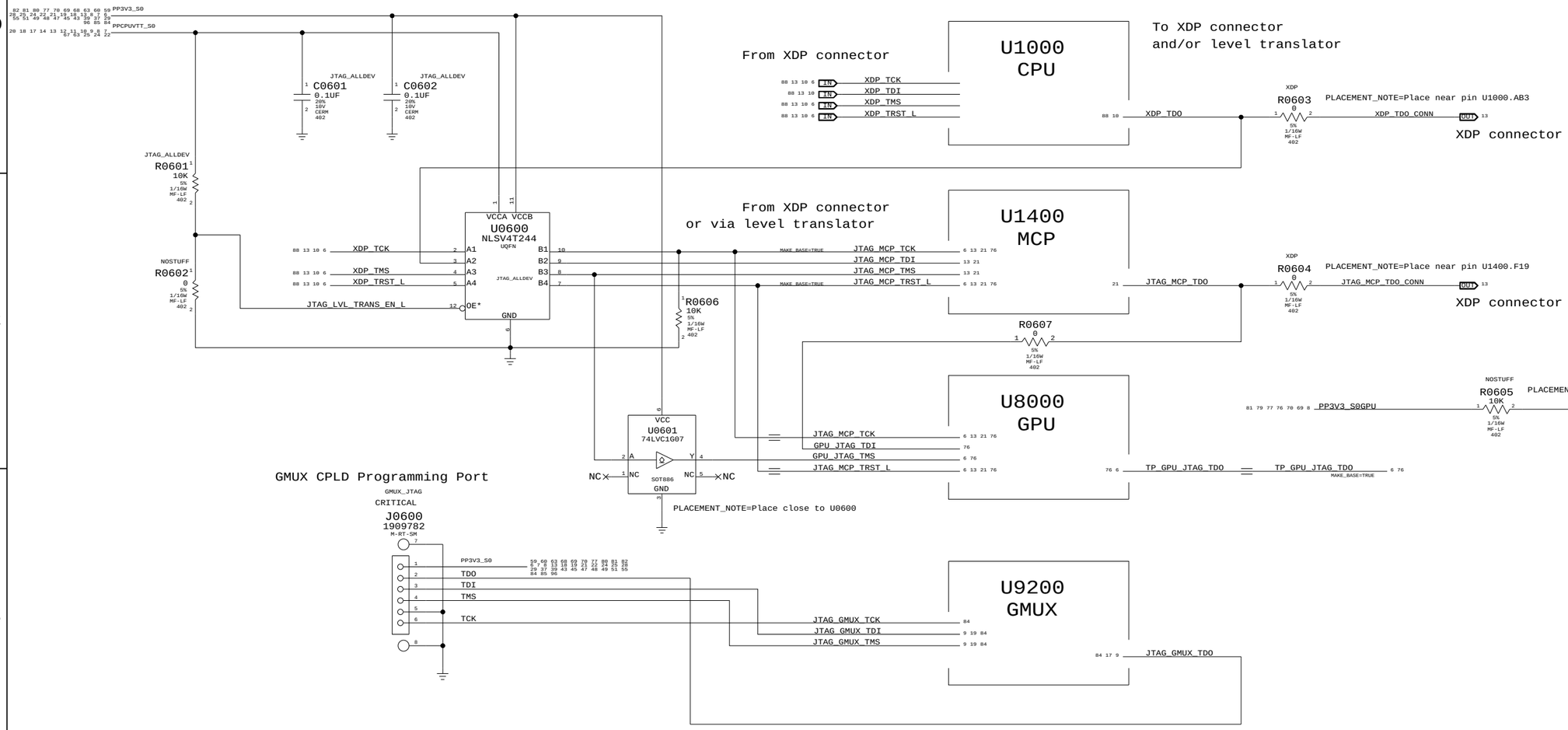
BOM Configuration

SYNC_MASTER=DDR SYNC_DATE=12/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 5 OF 97	

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 6 OF 97	

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	PP5V_S0	66 67 70 41 76 42 43 83 85	3 TPs
TRUE	FAN_LT_PWM	49	
TRUE	FAN_LT_TACH	49	
TRUE	FAN_RT_PWM	49	
TRUE	FAN_RT_TACH	49	
TRUE	GND		5 TPs

LVDS Connector

FUNC_TEST

TRUE	PP3V3_S0	59 60 63 68 69 70 77 80 81 82	
TRUE	PP3V3_SW_LCD	59 67 33 35 36 37 46 48 49 51 55 84 85 96	
TRUE	PPVOUT_S0_LCDBKLT	80 7 53 80 85	
TRUE	LVDS_DDC_CLK	80 81	
TRUE	LVDS_DDC_DATA	80 81	
TRUE	LVDS_CONN_A_DATA_N<0>	80 81 95	
TRUE	LVDS_CONN_A_DATA_P<0>	80 81 95	
TRUE	LVDS_CONN_A_DATA_N<1>	80 81 95	
TRUE	LVDS_CONN_A_DATA_P<1>	80 81 95	
TRUE	LVDS_CONN_A_DATA_N<2>	80 81 95	
TRUE	LVDS_CONN_A_DATA_P<2>	80 81 95	
TRUE	LVDS_CONN_A_CLK_F_N	80 95	
TRUE	LVDS_CONN_A_CLK_F_P	80 95	
TRUE	LVDS_CONN_B_DATA_N<0>	80 81 95	
TRUE	LVDS_CONN_B_DATA_P<0>	80 81 95	
TRUE	LVDS_CONN_B_DATA_N<1>	80 81 95	
TRUE	LVDS_CONN_B_DATA_P<1>	80 81 95	
TRUE	LVDS_CONN_B_DATA_N<2>	80 81 95	
TRUE	LVDS_CONN_B_DATA_P<2>	80 81 95	
TRUE	LVDS_CONN_B_CLK_F_N	80 95	
TRUE	LVDS_CONN_B_CLK_F_P	80 95	
TRUE	LED_RETURN_1	80 85	
TRUE	LED_RETURN_2	80 85	
TRUE	LED_RETURN_3	80 85	
TRUE	LED_RETURN_4	80 85	
TRUE	LED_RETURN_5	80 85	
TRUE	LED_RETURN_6	80 85	
TRUE	BKL_ISEN1	85	
TRUE	BKL_ISEN2	85	
TRUE	BKL_ISEN3	85	
TRUE	BKL_ISEN4	85	
TRUE	BKL_ISEN5	85	
TRUE	BKL_ISEN6	85	
TRUE	GND		5 TPs

IPD Flex Connector

FUNC_TEST

TRUE	PP3V3_S3_LDO	7 51	
TRUE	PP18V5_S3	7 51	
TRUE	Z2_CS_L	50 51	
TRUE	Z2_DEBUG3	50 51	
TRUE	Z2_MOSI	50 51	
TRUE	Z2_MISO	50 51	
TRUE	Z2_SCLK	50 51	
TRUE	Z2_BOOST_EN	51	
TRUE	Z2_HOST_INTN	50 51	
TRUE	Z2_CLKIN	50 51	
TRUE	Z2_KEY_ACT_L	50 51	
TRUE	Z2_RESET	50 51	
TRUE	PSOC_MISO	50 51	
TRUE	PSOC_MOSI	50 51	
TRUE	PSOC_SCLK	50 51	
TRUE	SMBUS_SMC_A_S3_SDA	7 31 42 45 51 94	
TRUE	SMBUS_SMC_A_S3_SCL	7 31 42 45 51 94	
TRUE	PSOC_F_CS_L	50 51	
TRUE	PICKB_L	50 51	
TRUE	GND		2 TPs

SD Card Connector

FUNC_TEST

TRUE	SD_D<7..0>	32 93	
TRUE	SD_CMD	32 93	
TRUE	SD_CLK	32 93	
TRUE	SD_CD_L	32	
TRUE	SD_WP	32	
TRUE	GND		2 TPs

Speaker Connectors

FUNC_TEST

TRUE	BI_MIC_LO	59 60	
TRUE	BI_MIC_SHIELD	59 60	
TRUE	BI_MIC_HI	59 60	
TRUE	SPKRCONN_L_OUT_P	58 59 96	
TRUE	SPKRCONN_L_OUT_N	58 59 96	
TRUE	SPKRCONN_R_OUT_P	58 59 96	
TRUE	SPKRCONN_R_OUT_N	58 59 96	
TRUE	SPKRCONN_S_OUT_P	58 59 96	
TRUE	SPKRCONN_S_OUT_N	58 59 96	
TRUE	GND		6 TPs

SATA ODD Connectors

FUNC_TEST

TRUE	PP5V_SW_ODD	7 39 53	4 TPs
TRUE	SMC_ODD_DETECT	39 42	
TRUE	SATA_ODD_R2D_P	39 90	
TRUE	SATA_ODD_R2D_N	39 90	
TRUE	SATA_ODD_D2R_C_N	39 90	
TRUE	SATA_ODD_D2R_C_P	39 90	
TRUE	GND		3 TPs

Keyboard Connector

FUNC_TEST

TRUE	PP3V3_S3	7 8 21 27 31 32 45 50 52 70	
TRUE	PP3V42_G3H	7 8 21 22 26 40 42 43 44 45 46 50 61 62 64 69	
TRUE	WS_KBD1	50	
TRUE	WS_KBD2	50	
TRUE	WS_KBD3	50	
TRUE	WS_KBD4	50	
TRUE	WS_KBD5	50	
TRUE	WS_KBD6	50	
TRUE	WS_KBD7	50	
TRUE	WS_KBD8	50	
TRUE	WS_KBD9	50	
TRUE	WS_KBD10	50	
TRUE	WS_KBD11	50	
TRUE	WS_KBD12	50	
TRUE	WS_KBD13	50	
TRUE	WS_KBD14	50	
TRUE	WS_KBD15_CAP	50	
TRUE	WS_KBD16_NUM	50	
TRUE	WS_KBD17	50	
TRUE	WS_KBD18	50	
TRUE	WS_KBD19	50	
TRUE	WS_KBD20	50	
TRUE	WS_KBD21	50	
TRUE	WS_KBD22	50	
TRUE	WS_KBD23	50	
TRUE	WS_KBD_ONOFF_L	50	
TRUE	WS_LEFT_SHIFT_KBD	50	
TRUE	WS_LEFT_OPTION_KBD	50	
TRUE	WS_CONTROL_KBD	50	
TRUE	KBDLED_ANODE	7 51	
TRUE	GND		2 TPs

Airport/BT/Camera Conn.

FUNC_TEST

TRUE	PCIE_MINI_D2R_P	17 31 90	
TRUE	PCIE_MINI_D2R_N	17 31 90	
TRUE	PCIE_MINI_R2D_P	31 90 96	
TRUE	PCIE_MINI_R2D_N	31 90 96	
TRUE	PCIE_CLK100M_MINI_CONN_P	31 96	
TRUE	PCIE_CLK100M_MINI_CONN_N	31 96	
TRUE	MINI_CLKREQ_Q_L	31	
TRUE	PCIE_WAKE_L	17 31	
TRUE	MINI_RESET_CONN_L	31	
TRUE	PP5V_WLAN	31	
TRUE	PP3V3_S3_BT_F	31	
TRUE	PP5V_S3_BTCAMERA_F	31	
TRUE	SMBUS_SMC_A_S3_SDA	7 31 42 45 51 94	
TRUE	SMBUS_SMC_A_S3_SCL	7 31 42 45 51 94	
TRUE	USB_CAMERA_CONN_P	31 96	
TRUE	USB_CAMERA_CONN_N	31 96	
TRUE	CONN_USB2_BT_P	31 96	
TRUE	CONN_USB2_BT_N	31 96	
TRUE	GND		10 TPs

SATA HDD Connector

FUNC_TEST

TRUE	PP5V_S0_HDD_FLT	7 39	4 TPs
TRUE	PP5V_S3_IR_R	39	
TRUE	SATA_HDD_R2D_P	39 90	
TRUE	SATA_HDD_R2D_N	39 90	
TRUE	SATA_HDD_D2R_C_P	39 90	
TRUE	SATA_HDD_D2R_C_N	39 90	
TRUE	IR_RX_OUT	39 41	
TRUE	SYS_LED_ANODE_R	39	
TRUE	GND		6 TPs

KBD Backlight Conn.

FUNC_TEST

TRUE	KBDLED_ANODE	7 51	2 TPs
TRUE	SMC_KDBLED_PRESENT_L	51	
TRUE	GND		

DC Power Connector

FUNC_TEST

TRUE	PP18V5_DCIN_FUSE	61	3 TPs
TRUE	ADAPTER_SENSE	61	
TRUE	GND		3 TPs

Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	61 62	3 TPs
TRUE	SMBUS_SMC_BSA_SCL	7 42 45 61 62 94	
TRUE	SMBUS_SMC_BSA_SDA	7 42 45 61 62 94	
TRUE	SYS_DETECT_L	61	
TRUE	GND		6 TPs

Batt Signal Connector

FUNC_TEST

TRUE	PP3V42_G3H	45 46 50 61 62 64 69 44 42 43 21 22 26	3 TPs
TRUE	SMBUS_SMC_BSA_SCL	7 42 45 61 62 94	
TRUE	SMBUS_SMC_BSA_SDA	7 42 45 61 62 94	
TRUE	SMC_BIL_BUTTON_L	42 43 61	
TRUE	SMC_LID_R	61	
TRUE	GND		3 TPs

Power Nets

FUNC_TEST

TRUE	PPVCORE_S0_CPU	8 11 12 46 63	
TRUE	PPVCORE_S0_MCP_REG	8 22 24 46 66	
TRUE	PP0V9R0V75_S0_DDRVTT	8 28 29 65 70	
TRUE	PPCPUVTT_S0	6 8 9 10 11 12 13 14 17 18 20 22 24 25 63 67	
TRUE	PP1V8R1V5_S0_FET	8 11 12 16 24 28 29 39 68 69 70	
TRUE	PP1V8_S0	8 18 25 55 69 70 84 87	
TRUE	PP3V3_S0	59 60 63 68 69 70 77 80 81 82 29 37 38 43 45 47 48 49 51 55 84 85 96	
TRUE	PP1V8R1V5_S3	28 29 39 65 70	
TRUE	PP3V3_S3	7 8 21 27 31 32 45 50 52 70	
TRUE	PP1V2R1V05_S5	8 22 24 34 68	
TRUE	PP3V3_S5	8 18 20 22 24 26 30 34 37 38 44 54 64 68 69 78 82 87 96	
TRUE	PP3V42_G3H	7 8 21 22 26 40 42 43 44 45 46 50 61 62 64 69	
TRUE	PPBUS_G3H	8 37 46 61 62 64 65 66 67 79 83 86	
TRUE	PP3V3_ENET_PHY	8 18 24 33 34	
TRUE	PP1V2R1V05_ENET	8 18 24 33 34 37	
TRUE	PP5V_S3	8 9 31 39 40 41 43 51 53 55 64 65 70 79	
TRUE	PP3V3_S5_AVREF_SMC	42 43	
TRUE	PP18V5_S3	7 51	
TRUE	PP3V3_S3_LDO	7 51	
TRUE	PPVOUT_S0_LCDBKLT	7 53 80 85	
TRUE	PP4V5_AUDIO_ANALOG	55	
TRUE	SMC_PM_G2_EN	42 64 69	
TRUE	PM_SLP_S4_L	21 40 42 43 69 70	
TRUE	PM_SLP_S3_L	21 34 37 42 69 82 84	
TRUE	PP1V05_S0_MCP_PLL_UF	8 24 68	
TRUE	PP5V_SW_ODD	7 39 53	
TRUE	PP5V_S0_HDD_FLT	7 39	
TRUE	BKL_VLDO	85	
TRUE	GND		6 TPs

ICT Test Points

				NO_TEST
55 7	NC_AUD_LO1_N_L	NC_AUD_LO1_N_L		
55 7	NC_AUD_LO1_P_L	NC_AUD_LO1_P_L	MAKE_BASE=TRUE	TRUE 7 55
20 7	NC_USB_10N	NC_USB_10N	MAKE_BASE=TRUE	TRUE 7 20
20 7	NC_USB_10P	NC_USB_10P	MAKE_BASE=TRUE	TRUE 7 20
18 7	NC_ENET_INTR_L	NC_ENET_INTR_L	MAKE_BASE=TRUE	TRUE 7 18
18 7	NC_ENET_PWRDWN_L	NC_ENET_PWRDWN_L	MAKE_BASE=TRUE	TRUE 7 18
19 7	NC_LPC_DRQ0_L	NC_LPC_DRQ0_L	MAKE_BASE=TRUE	TRUE 7 19
	TP_MEM_A_CKE<3..2>	NC_MEM_A_CKE<3..2>		16
15 7	NC_MEM_A_CLK2N	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	TRUE 7 15
16 7	NC_MEM_A_CLK3N	NC_MEM_A_CLK3N	MAKE_BASE=TRUE	TRUE 7 16
16 7	NC_MEM_A_CLK3P	NC_MEM_A_CLK3P	MAKE_BASE=TRUE	TRUE 7 16
16 7	NC_MEM_A_CLK4P	NC_MEM_A_CLK4P	MAKE_BASE=TRUE	TRUE 7 16
16 7	NC_MEM_A_CS_L<3>	NC_MEM_A_CS_L<3>	MAKE_BASE=TRUE	TRUE 7 16
	TP_MEM_A_ODT<3..2>	NC_MEM_A_ODT<3..2>	MAKE_BASE=TRUE	TRUE 16
16 7	NC_MEM_B_CKE<2>	NC_MEM_B_CKE<2>	MAKE_BASE=TRUE	TRUE 7 16
16 7	NC_MEM_B_CLK3P	NC_MEM_B_CLK3P	MAKE_BASE=TRUE	TRUE 7 16
16 7	NC_MEM_B_CLK4N	NC_MEM_B_CLK4N	MAKE_BASE=TRUE	TRUE 7 16
16 7	NC_MEM_B_CLK4P	NC_MEM_B_CLK4P	MAKE_BASE=TRUE	TRUE 7 16
16 7	NC_MEM_B_CLK5N	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	TRUE 7 16
16 7	NC_MEM_B_ODT<2>	NC_MEM_B_ODT<2>	MAKE_BASE=TRUE	TRUE 7 16
21 7	NC_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	TRUE 7 21
50 7	NC_P7_7	NC_P7_7	MAKE_BASE=TRUE	TRUE 7 50
	TP_PCI_AD<31..8>	NC_PCI_AD<31..8>	MAKE_BASE=TRUE	TRUE 19
	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE	TRUE 19
19 7	NC_PCI_CLK0	NC_PCI_CLK0		
19 7	NC_PCI_CLK1	NC_PCI_CLK1	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_DEVSEL_L	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_FRAME_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_GNT0_L	NC_PCI_GNT0_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_GNT1_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_INTW_L	NC_PCI_INTW_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_INTX_L	NC_PCI_INTX_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_INTZ_L	NC_PCI_INTZ_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_IRDY_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_PERR_L	NC_PCI_PERR_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_RESET1_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_SERR_L	NC_PCI_SERR_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_STOP_L	NC_PCI_STOP_L	MAKE_BASE=TRUE	TRUE 7 19
19 7	NC_PCI_TRDY_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE	TRUE 7 19
17 7	NC_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	TRUE 7 17
17 7	NC_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	TRUE 7 17
17 7	NC_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	TRUE 7 17
17 7	NC_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	TRUE 7 17
17 7	NC_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	TRUE 7 17
17 7	NC_PCIE_PE4_D2RN	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE	TRUE 7 17
17 7	NC_PCIE_PE4_R2D_CN	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE	TRUE 7 17
17 7	NC_PE4_PRSNT_L	NC_PE4_PRSNT_L	MAKE_BASE=TRUE	TRUE 7 17
50 7	NC_PSOC_P1_3	NC_PSOC_P1_3	MAKE_BASE=TRUE	TRUE 7 50
50 7	NC_PSOC_SDA	NC_PSOC_SDA	MAKE_BASE=TRUE	TRUE 7 50
20 7	NC_SATA_C_D2RP	NC_SATA_C_D2RP	MAKE_BASE=TRUE	TRUE 7 20
20 7	NC_SATA_C_R2D_CN	NC_SATA_C_R2D_CN	MAKE_BASE=TRUE	TRUE 7 20
20 7	NC_SATA_C_R2D_CP	NC_SATA_C_R2D_CP	MAKE_BASE=TRUE	TRUE 7 20
20 7	NC_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE	TRUE 7 20
20 7	NC_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE	TRUE 7 20
21 7	NC_SB_A20GATE	NC_SB_A20GATE	MAKE_BASE=TRUE	TRUE 7 21

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 88	
TRUE	FSB_ADS_L	10 14 88	
TRUE	FSB_ADSTB_L<1..0>	10 14 88	
TRUE	FSB_D_L<63..0>	10 14 88	
TRUE	FSB_DINV_L<3..0>	10 14 88	
TRUE	FSB_DSTB_L_N<3..0>	10 14 88	
TRUE	FSB_DSTB_L_P<3..0>	10 14 88	
TRUE	FSB_HIT_L	10 14 88	
TRUE	FSB_HITM_L	10 14 88	
TRUE	FSB_LOCK_L	10 14 88	
TRUE	USB_BT_N	20 31 91	
TRUE	USB_BT_P	20 31 91	
TRUE	USB_CAMERA_N	20 31 91	
TRUE	USB_CAMERA_P	20 31 91	
TRUE	SATA_ODD_D2R_UF_N	39 96	
TRUE	SATA_ODD_D2R_UF_P	39 96	
TRUE	DP_ML_C_P<3..0>	82 95	

Note.
NO_TEST properties are also on page9,26,43,50

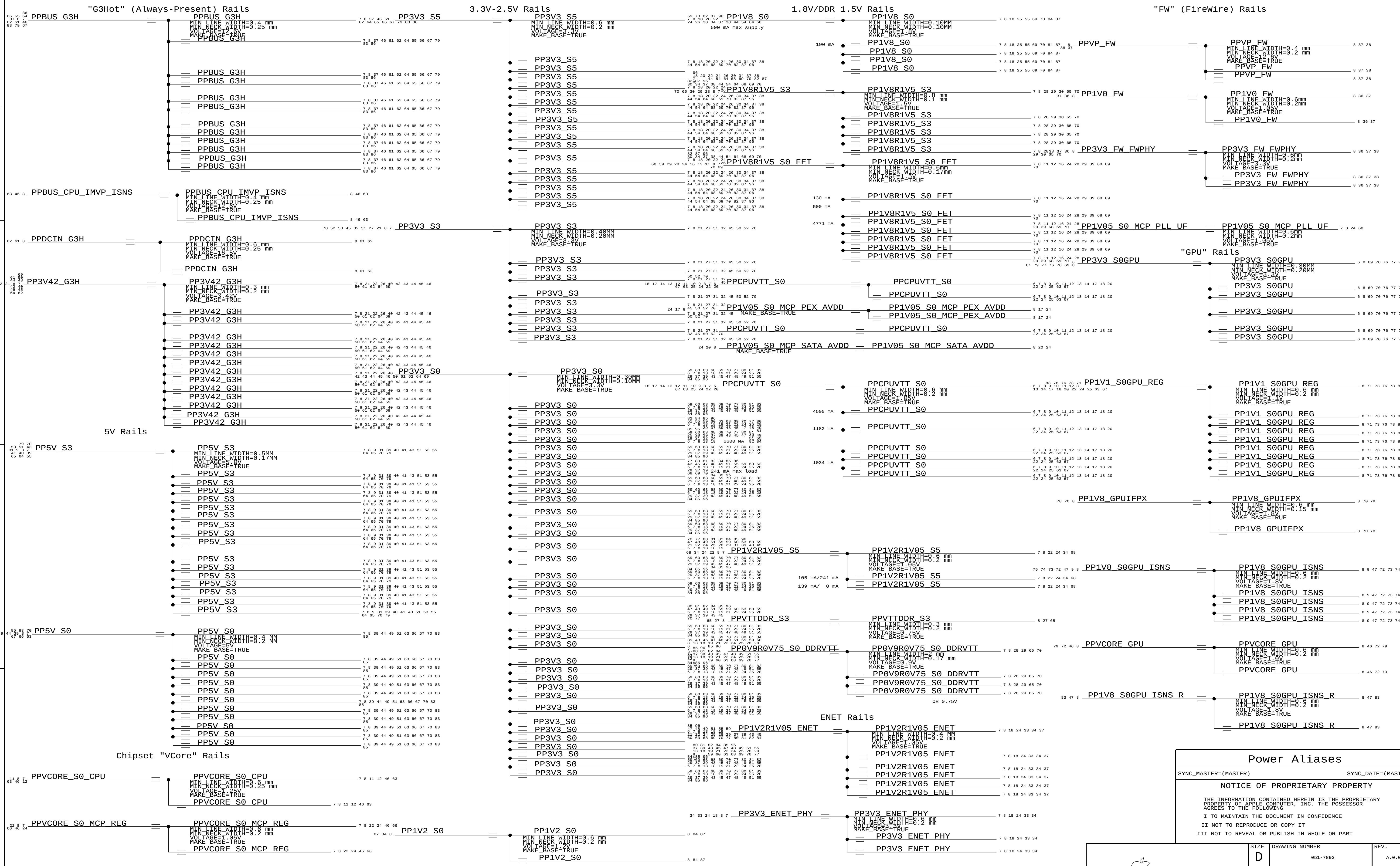
Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0

SCALE	SHT	OF
NONE	7	97



Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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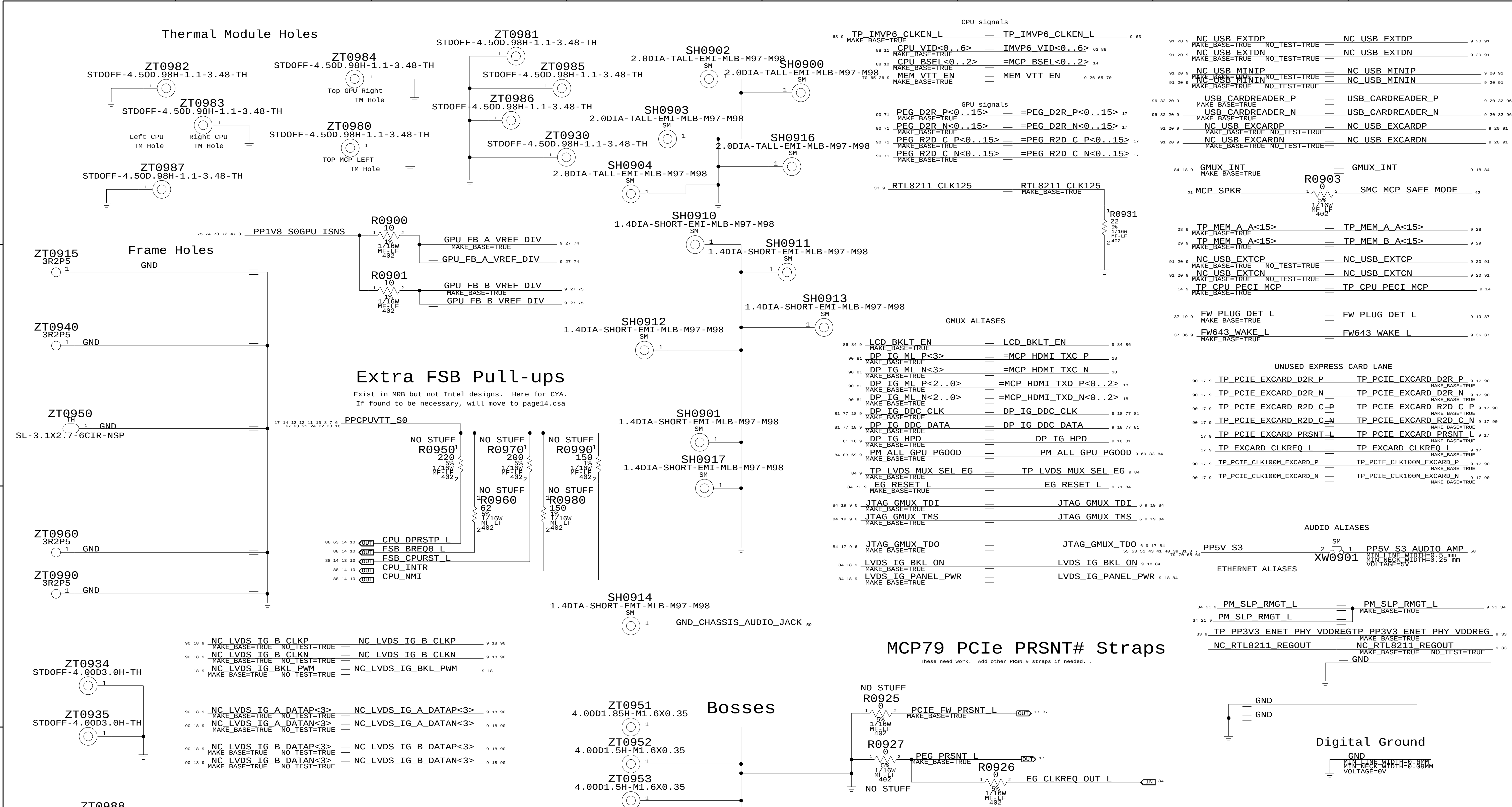
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE NONE	SHT 8	OF 97


Thermal Module Holes
ZT0982 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0983 STDOFF-4.5OD.98H-1.1-3.48-TH
Left CPU TM Hole
Right CPU TM Hole
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
Top GPU Right TM Hole
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
TOP MCP LEFT TM Hole
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0904 2.0DIA-TALL-EMI-MLB-M97-M98
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0901 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0917 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
GND_CHASSIS_AUDIO_JACK
Frame Holes
ZT0915 3R2P5 GND
ZT0940 3R2P5 GND
ZT0950 SL-3.1X2.7-6CIR-NSP GND
ZT0960 3R2P5 GND
ZT0990 3R2P5 GND
PP1V8_S0GPU_ISNS
R0900 10 1% 1/16W MF-LF 402
GPU_FB_A_VREF_DIV
R0901 10 1% 1/16W MF-LF 402
GPU_FB_B_VREF_DIV
Extra FSB Pull-ups
Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa
PPCPUVTT_S0
NO STUFF R0950 220 5% 1/16W MF-LF 402
NO STUFF R0970 200 5% 1/16W MF-LF 402
NO STUFF R0990 150 1% 1/16W MF-LF 402
NO STUFF R0960 62 5% 1/16W MF-LF 402
NO STUFF R0980 150 1% 1/16W MF-LF 402
CPU_DPRSTP_L
FSB_BREQ0_L
FSB_CPURST_L
CPU_INTR
CPU_NMI
NC_LVDS_IG_B_CLKP
NC_LVDS_IG_B_CLKN
NC_LVDS_IG_BKL_PWM
NC_LVDS_IG_A_DATAP<3>
NC_LVDS_IG_A_DATAN<3>
NC_LVDS_IG_B_DATAP<3>
NC_LVDS_IG_B_DATAN<3>
ZT0934 STDOFF-4.0OD3.0H-TH
ZT0935 STDOFF-4.0OD3.0H-TH
ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH
Bosses
ZT0951 4.0OD1.85H-M1.6X0.35
ZT0952 4.0OD1.5H-M1.6X0.35
ZT0953 4.0OD1.5H-M1.6X0.35
ZT0954 4.0OD1.85H-M1.6X0.35
CPU signals
TP_IMVP6_CLKEN_L
CPU_VID<0..6> IMVP6_VID<0..6>
CPU_BSEL<0..2> =MCP_BSEL<0..2>
MEM_VTT_EN
GPU signals
PEG_D2R_P<0..15> =PEG_D2R_P<0..15>
PEG_D2R_N<0..15> =PEG_D2R_N<0..15>
PEG_R2D_C_P<0..15> =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<0..15> =PEG_R2D_C_N<0..15>
RTL8211_CLK125
R0931 22 5% 1/16W MF-LF 402
GMUX ALIASES
LCD_BKLT_EN
DP_IG_ML_P<3> =MCP_HDMI_TXC_P
DP_IG_ML_N<3> =MCP_HDMI_TXC_N
DP_IG_ML_P<2..0> =MCP_HDMI_TXD_P<0..2>
DP_IG_ML_N<2..0> =MCP_HDMI_TXD_N<0..2>
DP_IG_DDC_CLK
DP_IG_DDC_DATA
DP_IG_HPD
PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG
EG_RESET_L
JTAG_GMUX_TDI
JTAG_GMUX_TMS
JTAG_GMUX_TDO
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
MAKE_BASE=TRUE
NO_TEST=TRUE
NC_USB_EXTDP
NC_USB_EXTDN
NC_USB_MINIP
NC_USB_MININ
USB_CARDREADER_P
USB_CARDREADER_N
NC_USB_EXCARDP
NC_USB_EXCARDN
GMUX_INT
R0903 0 5% 1/16W MF-LF 402
MCP_SPKR SMC_MCP_SAFE_MODE
TP_MEM_A_A<15>
TP_MEM_B_A<15>
NC_USB_EXTCP
NC_USB_EXTCN
TP_CPU_PECI_MCP
FW_PLUG_DET_L
FW643_WAKE_L
UNUSED EXPRESS CARD LANE
TP_PCIE_EXCARD_D2R_P
TP_PCIE_EXCARD_D2R_N
TP_PCIE_EXCARD_R2D_C_P
TP_PCIE_EXCARD_R2D_C_N
TP_PCIE_EXCARD_PRSNT_L
TP_EXCARD_CLKREQ_L
TP_PCIE_CLK100M_EXCARD_P
TP_PCIE_CLK100M_EXCARD_N
AUDIO ALIASES
PP5V_S3 XW0901 SM PP5V_S3_AUDIO_AMP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
ETHERNET ALIASES
PM_SLP_RMGT_L
TP_PP3V3_ENET_PHY_VDDREG
NC_RTL8211_REGOUT
GND
MCP79 PCIe PRSNT# Straps
These need work. Add other PRSNT# straps if needed. .
NO STUFF R0925 0 5% 1/16W MF-LF 402
PCIE_FW_PRSNT_L
R0927 0 5% 1/16W MF-LF 402 NO STUFF
PEG_PRSNT_L
R0926 0 5% 1/16W MF-LF 402
EG_CLKREQ_OUT_L
MCP_MII_PD
R0930 47K 5% 1/16W MF-LF 402
Digital Ground
GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.09MM
VOLTAGE=0V

Signal Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE NONE	SHT 9	OF 97

OMIT

U1000
PENRYN
FCBGA
1 OF 4

ADDR GROUP0
FSB_A_L<3> J4 A3*
FSB_A_L<4> L5 A4*
FSB_A_L<5> L4 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M3 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L2 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> M1 ADSTB0*

FSB_REQ_L<0> K3 REQ0*
FSB_REQ_L<1> H2 REQ1*
FSB_REQ_L<2> K2 REQ2*
FSB_REQ_L<3> J3 REQ3*
FSB_REQ_L<4> L1 REQ4*

ADDR GROUP1
FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U1 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W2 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> U2 A30*
FSB_A_L<31> V4 A31*
FSB_A_L<32> W3 A32*
FSB_A_L<33> AA4 A33*
FSB_A_L<34> AB2 A34*
FSB_A_L<35> AA3 A35*
FSB_ADSTB_L<1> V1 ADSTB1*

ICH
CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

RESERVED
TP_CPU_RSVD0 M4 RSVD0
TP_CPU_RSVD1 N5 RSVD1
TP_CPU_RSVD2 T2 RSVD2
TP_CPU_RSVD3 V3 RSVD3
TP_CPU_RSVD4 B2 RSVD4
TP_CPU_RSVD5 F6 RSVD5
TP_CPU_RSVD6 D2 RSVD6
TP_CPU_RSVD7 D22 RSVD7
TP_CPU_RSVD8 D3 RSVD8

CONTROL
ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 CPU_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* C1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

XDP/ITP SIGNALS
BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

THERMAL
PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC B25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

H CLK
BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

PPCPUVTT_S0
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)

R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
NOSTUFF C1000 0.1uF 10% 16V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND

0.5" MAX LENGTH FOR CPU_GTLREF

MISC
CPU_GTLREF AD26 GTLREF
CPU_TEST1 C23 TEST1
CPU_TEST2 D25 TEST2
TP_CPU_TEST3 C24 TEST3
CPU_TEST4 AF26 TEST4
TP_CPU_TEST5 AF1 TEST5
TP_CPU_TEST6 A26 TEST6
TP_CPU_TEST7 C3 TEST7
CPU_BSEL<0> B22 BSEL0
CPU_BSEL<1> B23 BSEL1
CPU_BSEL<2> C21 BSEL2

R1020 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)

XDP_TMS
XDP_TDI
XDP_TDO
XDP_TCK
XDP_TRST_L

NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402

OMIT

U1000
PENRYN
FCBGA
2 OF 4

DATA GRP 0
FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> G22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H22 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H23 D15*
FSB_DSTB_L_N<0> J26 DSTBN0*
FSB_DSTB_L_P<0> H26 DSTBP0*
FSB_DINV_L<0> H25 DINV0*

DATA GRP 1
FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L23 D20*
FSB_D_L<21> M24 D21*
FSB_D_L<22> L22 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P23 D25*
FSB_D_L<26> P22 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L25 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N25 D31*
FSB_DSTB_L_N<1> L26 DSTBN1*
FSB_DSTB_L_P<1> M26 DSTBP1*
FSB_DINV_L<1> N24 DINV1*

DATA GRP 2
D32* Y22 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* V23 FSB_D_L<36>
D37* T22 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U23 FSB_D_L<39>
D40* Y25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* W24 FSB_D_L<43>
D44* W25 FSB_D_L<44>
D45* AA23 FSB_D_L<45>
D46* AA24 FSB_D_L<46>
D47* AB25 FSB_D_L<47>
DSTBN2* Y26 FSB_DSTB_L_N<2>
DSTBP2* AA26 FSB_DSTB_L_P<2>
DINV2* U22 FSB_DINV_L<2>

DATA GRP 3
D48* AE24 FSB_D_L<48>
D49* AD24 FSB_D_L<49>
D50* AA21 FSB_D_L<50>
D51* AB22 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC26 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AC25 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AC22 FSB_D_L<60>
D61* AD23 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AC23 FSB_D_L<63>
DSTBN3* AE25 FSB_DSTB_L_N<3>
DSTBP3* AF24 FSB_DSTB_L_P<3>
DINV3* AC20 FSB_DINV_L<3>

MISC
COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 AA1 CPU_COMP<2>
COMP3 Y1 CPU_COMP<3>
DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_CPUSLP_L
PSI* AE6 CPU_PSI_L

R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB

SYNC_MASTER=M98_MLB SYNC_DATE=11/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 10 OF 97	

(CPU CORE POWER)

PPVCORE_S0_CPU 7 8 11 12 46 63

Standard Voltage:	Low Voltage:	Ultra Low Voltage:
44.0 A (Design Target)	23.0 A (Design Target)	17.0 A (Design Target)
41.0 A (HFM)	21.0 A (HFM)	TBD A (HFM)
30.4 A (LFM)	18.7 A (LFM)	TBD A (LFM)
25.5 A (SuperLFM)	TBD A (SuperLFM)	
27.4 A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)	TBD A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant SuperLFM)	TBD A (Auto-Halt/Stop-Grant LFM)
27.4 A (Sleep HFM)	TBD A (Sleep HFM)	TBD A (Sleep HFM)
16.8 A (Sleep SuperLFM)	TBD A (Sleep SuperLFM)	TBD A (Sleep LFM)
25.0 A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)	TBD A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)	TBD A (Deep Sleep SuperLFM)	TBD A (Deep Sleep LFM)
11.5 A (Deeper Sleep)	TBD A (Deeper Sleep)	TBD A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)	TBD A (Enhanced Deeper Sleep)

OMIT
U1000
PENRYN
FCBGA
3 OF 4

VCC: A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC: AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

(CPU IO POWER 1.05V)

PPCPUVTT_S0 5 7 8 9 10 12 13 14 17 18 20 22 24 25 63 67

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

(CPU INTERNAL PLL POWER 1.5V)

PP1V8R1V5_S0_FET 7 8 12 16 24 28 29 39 68 69 70

130 mA

VCCA: B26 C26

VID0	AD6	CPU_VID<0>	OUT 9 88
VID1	AF5	CPU_VID<1>	OUT 9 88
VID2	AE5	CPU_VID<2>	OUT 9 88
VID3	AF4	CPU_VID<3>	OUT 9 88
VID4	AE3	CPU_VID<4>	OUT 9 88
VID5	AF3	CPU_VID<5>	OUT 9 88
VID6	AE2	CPU_VID<6>	OUT 9 88
VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 63 88
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 63 88

PPVCORE_S0_CPU 7 8 11 12 46 63

R1100 100 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101 100 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
PENRYN
FCBGA
4 OF 4

VSS: A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3 B1

VSS: P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

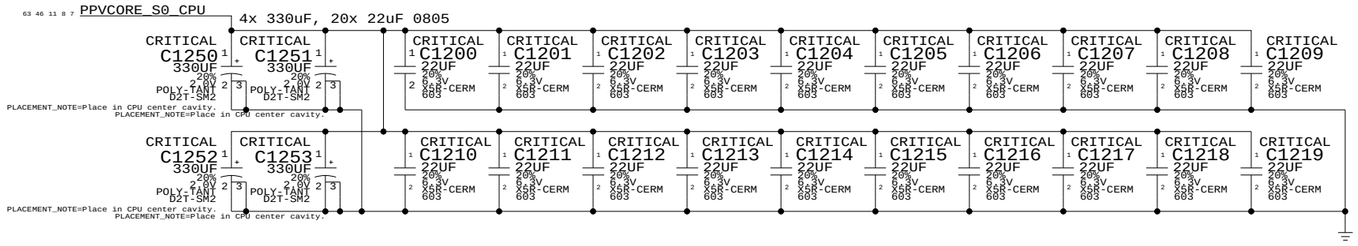
CPU Power & Ground

SYNC_MASTER=M98_MLB SYNC_DATE=11/12/2008

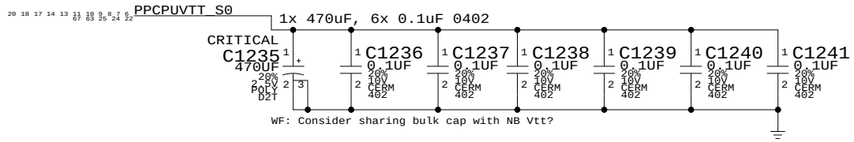
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 11 OF 97	

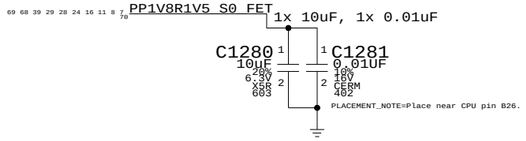
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

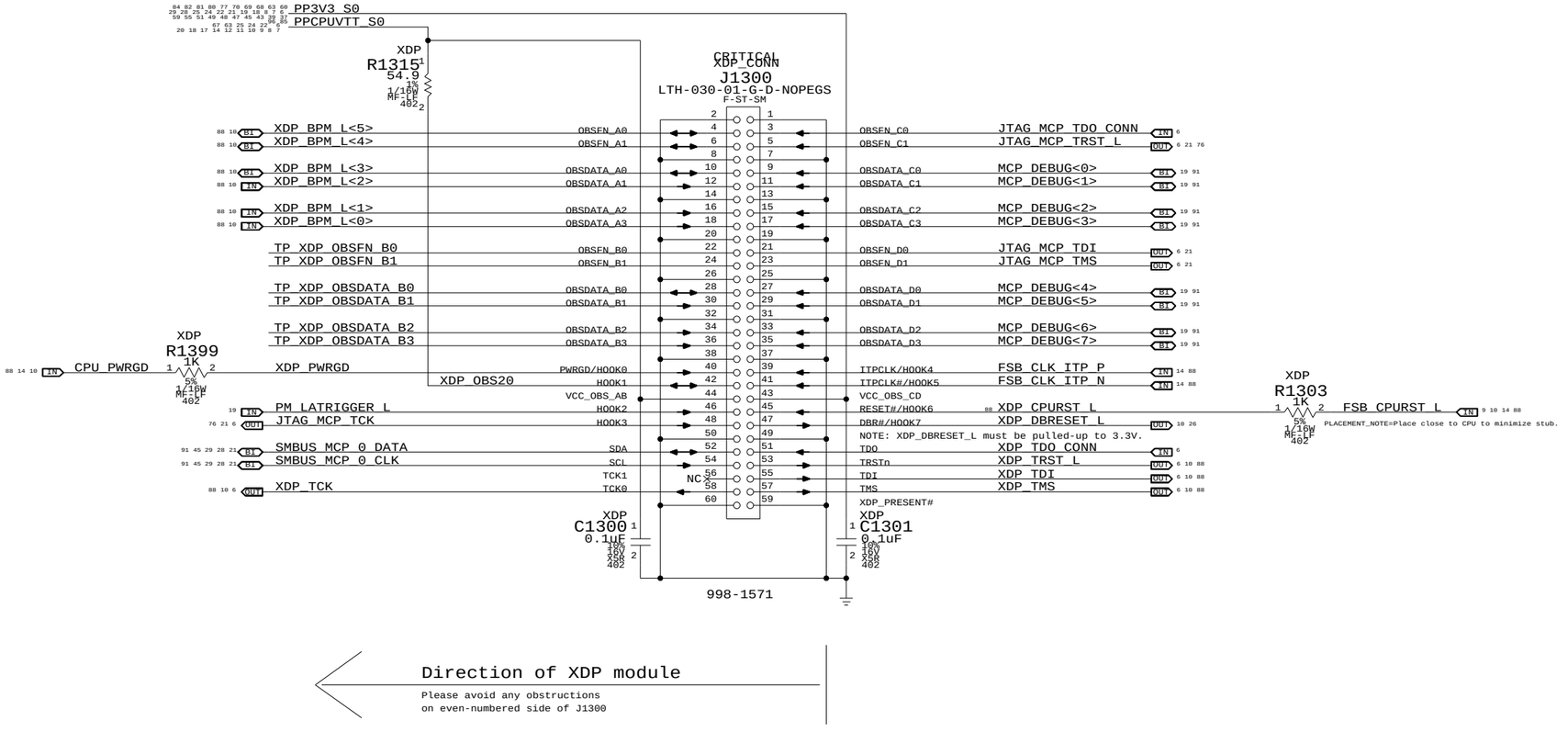
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 12 OF 97	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



eXtended Debug Port(MiniXDP)

SYNC_MASTER=M98_MLB SYNC_DATE=11/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 13 OF 97	

OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	
FSB_DINV_L<0>	V41	CPU_DBI0#	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	
FSB_DINV_L<1>	V35	CPU_DBI1#	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	
FSB_DINV_L<2>	N35	CPU_DBI2#	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	
FSB_DINV_L<3>	J41	CPU_DBI3#	
FSB_A_L<3>	AC34	CPU_A3#	
FSB_A_L<4>	AE38	CPU_A4#	
FSB_A_L<5>	AE34	CPU_A5#	
FSB_A_L<6>	AC37	CPU_A6#	
FSB_A_L<7>	AE37	CPU_A7#	
FSB_A_L<8>	AE35	CPU_A8#	
FSB_A_L<9>	AB35	CPU_A9#	
FSB_A_L<10>	AF35	CPU_A10#	
FSB_A_L<11>	AG35	CPU_A11#	
FSB_A_L<12>	AG39	CPU_A12#	
FSB_A_L<13>	AE33	CPU_A13#	
FSB_A_L<14>	AG37	CPU_A14#	
FSB_A_L<15>	AG38	CPU_A15#	
FSB_A_L<16>	AG34	CPU_A16#	
FSB_A_L<17>	AN38	CPU_A17#	
FSB_A_L<18>	AL39	CPU_A18#	
FSB_A_L<19>	AG33	CPU_A19#	
FSB_A_L<20>	AL33	CPU_A20#	
FSB_A_L<21>	AJ33	CPU_A21#	
FSB_A_L<22>	AN36	CPU_A22#	
FSB_A_L<23>	AJ35	CPU_A23#	
FSB_A_L<24>	AJ37	CPU_A24#	
FSB_A_L<25>	AJ36	CPU_A25#	
FSB_A_L<26>	AJ38	CPU_A26#	
FSB_A_L<27>	AL37	CPU_A27#	
FSB_A_L<28>	AL34	CPU_A28#	
FSB_A_L<29>	AN37	CPU_A29#	
FSB_A_L<30>	AJ34	CPU_A30#	
FSB_A_L<31>	AL38	CPU_A31#	
FSB_A_L<32>	AL35	CPU_A32#	
FSB_A_L<33>	AN34	CPU_A33#	
FSB_A_L<34>	AR39	CPU_A34#	
FSB_A_L<35>	AN35	CPU_A35#	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	
FSB_REQ_L<0>	AC38	CPU_REQ0#	
FSB_REQ_L<1>	AA33	CPU_REQ1#	
FSB_REQ_L<2>	AC39	CPU_REQ2#	
FSB_REQ_L<3>	AC33	CPU_REQ3#	
FSB_REQ_L<4>	AC35	CPU_REQ4#	
FSB_ADS_L	AD42	CPU_ADS#	
FSB_BNR_L	AD43	CPU_BNR#	
FSB_BREQ0_L	AE40	CPU_BR0#	
FSB_BREQ1_L	AL32	CPU_BR1#	
FSB_DBSY_L	AD39	CPU_DBSY#	
FSB_DRDY_L	AD41	CPU_DRDY#	
FSB_HIT_L	AB42	CPU_HIT#	
FSB_HITM_L	AD40	CPU_HITM#	
FSB_LOCK_L	AC43	CPU_LOCK#	
FSB_TRDY_L	AE41	CPU_TRDY#	
TP_CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	
	AG43	CPU_THERMTRIP#	
	AH40	CPU_FERR#	
(MCP_BSEL<2>)	F42	CPU_BSEL2	
(MCP_BSEL<1>)	D42	CPU_BSEL1	
(MCP_BSEL<0>)	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0#	
FSB_RS_L<1>	AB41	CPU_RS1#	
FSB_RS_L<2>	AC42	CPU_RS2#	
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	

CPU_D0#	Y43	FSB_D_L<0>	
CPU_D1#	W42	FSB_D_L<1>	
CPU_D2#	Y40	FSB_D_L<2>	
CPU_D3#	W41	FSB_D_L<3>	
CPU_D4#	Y39	FSB_D_L<4>	
CPU_D5#	V42	FSB_D_L<5>	
CPU_D6#	Y41	FSB_D_L<6>	
CPU_D7#	Y42	FSB_D_L<7>	
CPU_D8#	P42	FSB_D_L<8>	
CPU_D9#	U41	FSB_D_L<9>	
CPU_D10#	R42	FSB_D_L<10>	
CPU_D11#	T39	FSB_D_L<11>	
CPU_D12#	T42	FSB_D_L<12>	
CPU_D13#	T41	FSB_D_L<13>	
CPU_D14#	R41	FSB_D_L<14>	
CPU_D15#	T43	FSB_D_L<15>	
CPU_D16#	W35	FSB_D_L<16>	
CPU_D17#	AA37	FSB_D_L<17>	
CPU_D18#	W33	FSB_D_L<18>	
CPU_D19#	W34	FSB_D_L<19>	
CPU_D20#	AA36	FSB_D_L<20>	
CPU_D21#	AA34	FSB_D_L<21>	
CPU_D22#	AA38	FSB_D_L<22>	
CPU_D23#	AA35	FSB_D_L<23>	
CPU_D24#	U38	FSB_D_L<24>	
CPU_D25#	U36	FSB_D_L<25>	
CPU_D26#	U35	FSB_D_L<26>	
CPU_D27#	U33	FSB_D_L<27>	
CPU_D28#	U34	FSB_D_L<28>	
CPU_D29#	W38	FSB_D_L<29>	
CPU_D30#	R33	FSB_D_L<30>	
CPU_D31#	U37	FSB_D_L<31>	
CPU_D32#	N34	FSB_D_L<32>	
CPU_D33#	N33	FSB_D_L<33>	
CPU_D34#	R34	FSB_D_L<34>	
CPU_D35#	R35	FSB_D_L<35>	
CPU_D36#	P35	FSB_D_L<36>	
CPU_D37#	R39	FSB_D_L<37>	
CPU_D38#	R37	FSB_D_L<38>	
CPU_D39#	R38	FSB_D_L<39>	
CPU_D40#	L37	FSB_D_L<40>	
CPU_D41#	L39	FSB_D_L<41>	
CPU_D42#	L38	FSB_D_L<42>	
CPU_D43#	N36	FSB_D_L<43>	
CPU_D44#	N38	FSB_D_L<44>	
CPU_D45#	J39	FSB_D_L<45>	
CPU_D46#	J38	FSB_D_L<46>	
CPU_D47#	J37	FSB_D_L<47>	
CPU_D48#	L42	FSB_D_L<48>	
CPU_D49#	M42	FSB_D_L<49>	
CPU_D50#	P41	FSB_D_L<50>	
CPU_D51#	N41	FSB_D_L<51>	
CPU_D52#	N40	FSB_D_L<52>	
CPU_D53#	M40	FSB_D_L<53>	
CPU_D54#	H40	FSB_D_L<54>	
CPU_D55#	K42	FSB_D_L<55>	
CPU_D56#	H41	FSB_D_L<56>	
CPU_D57#	L41	FSB_D_L<57>	
CPU_D58#	H43	FSB_D_L<58>	
CPU_D59#	H42	FSB_D_L<59>	
CPU_D60#	K41	FSB_D_L<60>	
CPU_D61#	J40	FSB_D_L<61>	
CPU_D62#	H39	FSB_D_L<62>	
CPU_D63#	M43	FSB_D_L<63>	
CPU_BPRI#	AA41	FSB_BPRI_L	
CPU_DEFER#	AA40	FSB_DEFER_L	
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N	
BCLK_IN_N	AK41		
BCLK_IN_P	AJ40		
CPU_A20M#	AF41	CPU_A20M_L	
CPU_IGNNE#	AH39	CPU_IGNNE_L	
CPU_INIT#	AH42	CPU_INIT_L	
CPU_INTR	AF42	CPU_INTR	
CPU_NMI	AG41	CPU_NMI	
CPU_SMI#	AH41	CPU_SMI_L	
CPU_PWRGD	AH43	CPU_PWRGD	
CPU_RESET#	H38	FSB_CPURST_L	
CPU_SLP#	AM33	FSB_CPUSLP_L	
CPU_DPSLP#	AN33	CPU_DPSLP_L	
CPU_DPWR#	AM32	FSB_DPWR_L	
CPU_STPCLK#	AG42	CPU_STPCLK_L	
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	

PPCPUVTT_S0

R1410 54.9 1% 1/10W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L
CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
R1421 1K 5% 1/16W MF-LF 402
R1422 1K 5% 1/16W MF-LF 402

=MCP_BSEL<2>
=MCP_BSEL<1>
=MCP_BSEL<0>

R1430 49.9 1% 1/10W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/10W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

PP1V05_S0_MCP_PLL_FSB
270 mA (A01)

206 mA	AG27	+V_DLL_DLCELL_AVDD
20 mA	AH27	+V_PLL_MCLK
29 mA	AG28	+V_PLL_FSB
15 mA	AH28	+V_PLL_CPU

Loop-back clock for delay matching.

PPCPUVTT_S0
NO STUFF
R1440 150 5% 1/16W MF-LF 402

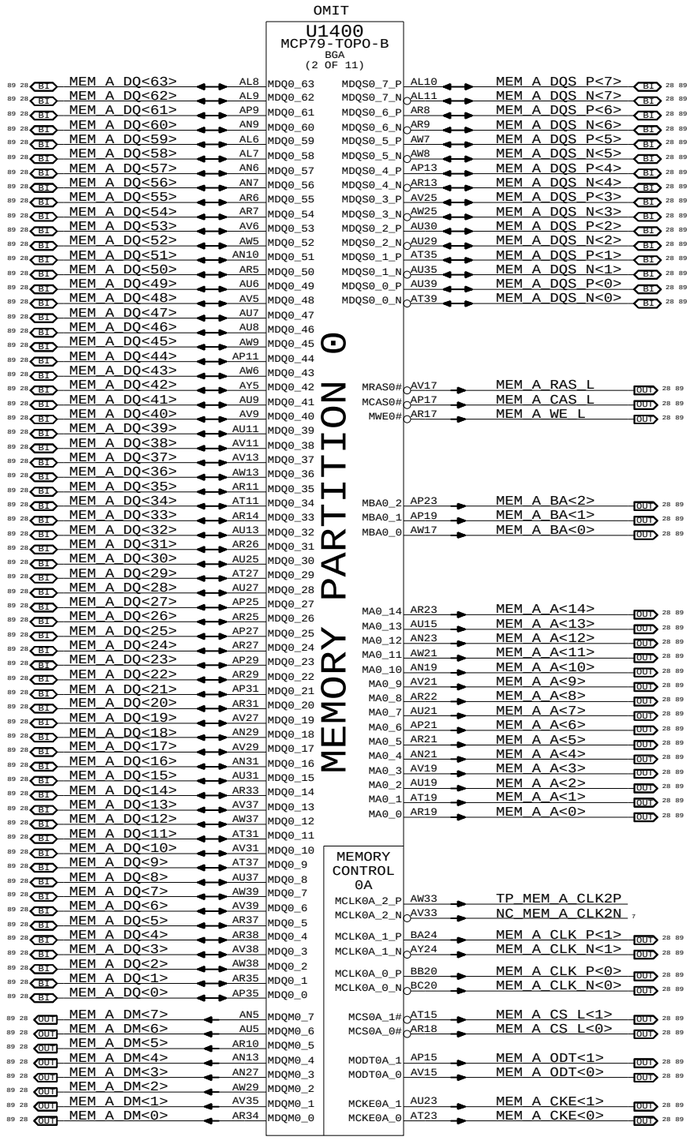
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

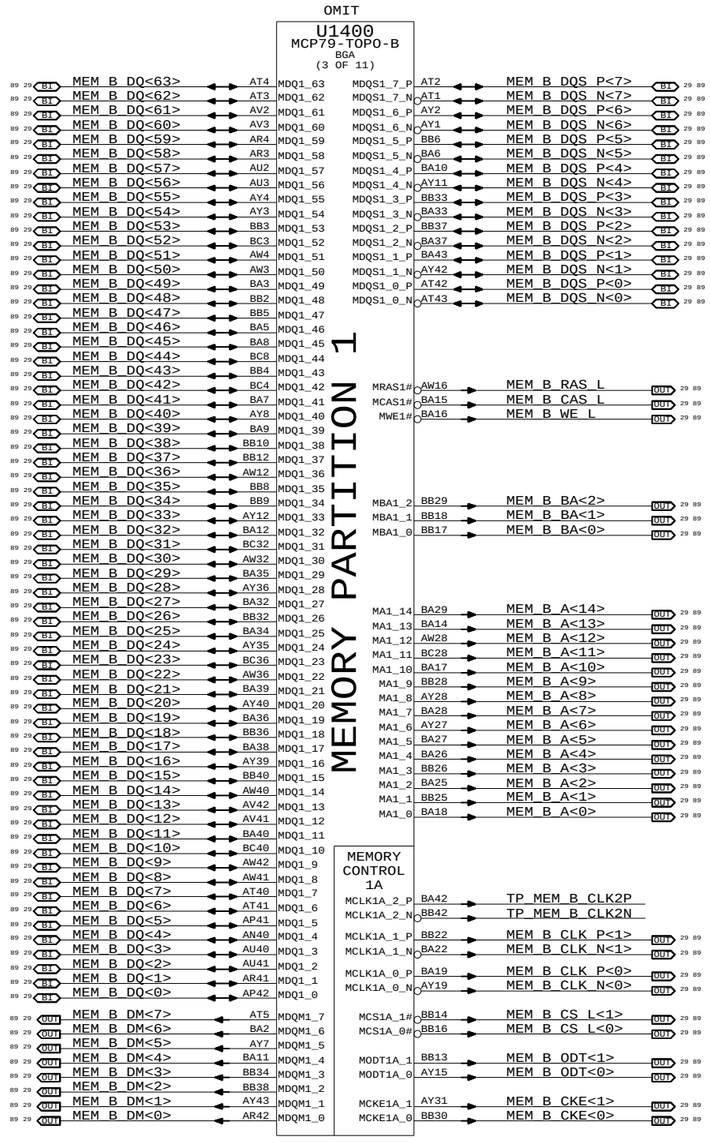
MCP CPU Interface

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 14 OF 97	



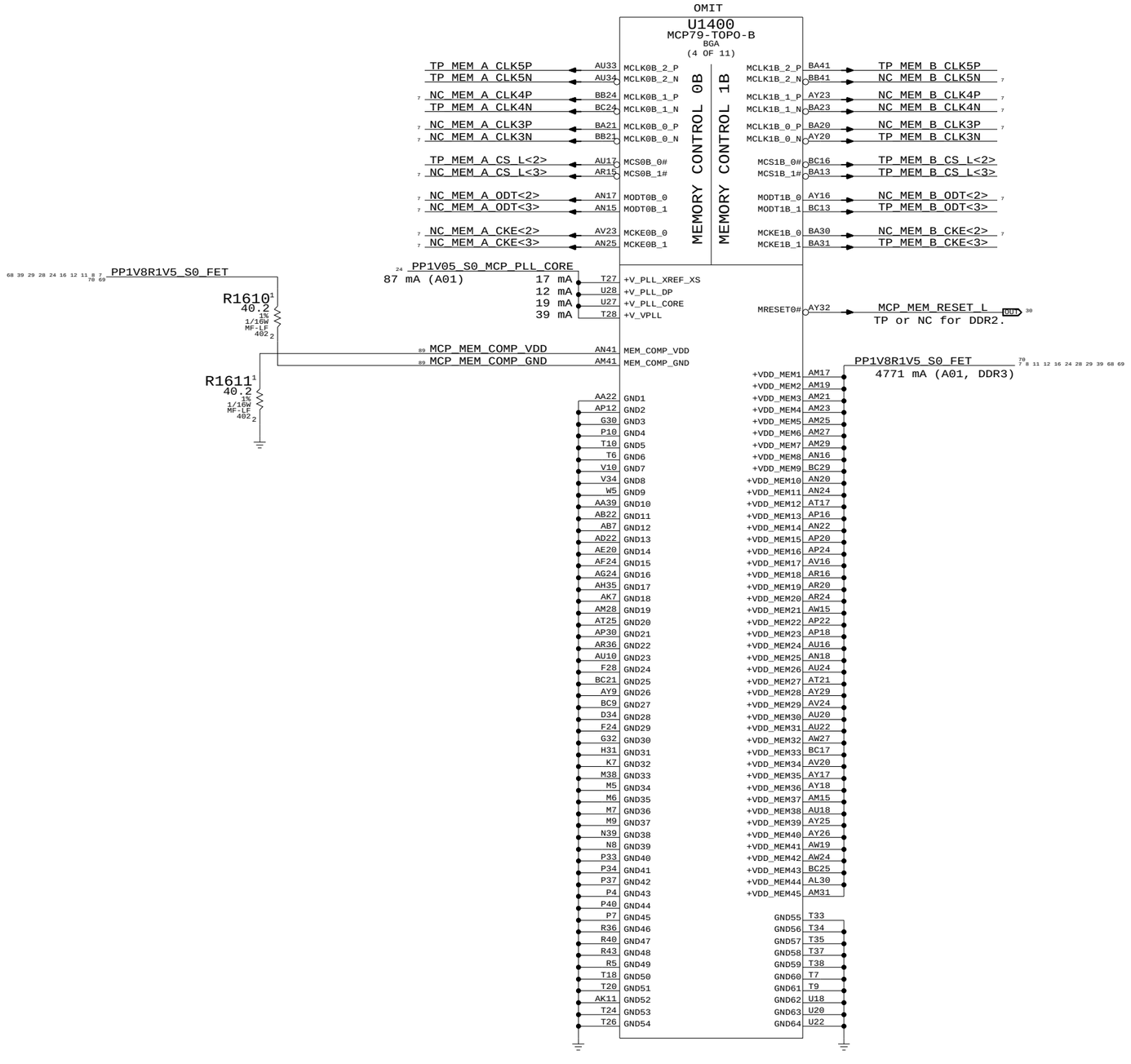


MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 15 OF 97	



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 16 OF 97	

OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

9	IN	=PEG_D2R_P<0>	F7	PE0_RX0_P	PE0_TX0_P	C5	=PEG_R2D_C_P<0>
9	IN	=PEG_D2R_N<0>	E7	PE0_RX0_N	PE0_TX0_N	D4	=PEG_R2D_C_N<0>
9	IN	=PEG_D2R_P<1>	D7	PE0_RX1_P	PE0_TX1_P	C4	=PEG_R2D_C_P<1>
9	IN	=PEG_D2R_N<1>	C7	PE0_RX1_N	PE0_TX1_N	B4	=PEG_R2D_C_N<1>
9	IN	=PEG_D2R_P<2>	E6	PE0_RX2_P	PE0_TX2_P	A4	=PEG_R2D_C_P<2>
9	IN	=PEG_D2R_N<2>	F6	PE0_RX2_N	PE0_TX2_N	A3	=PEG_R2D_C_N<2>
9	IN	=PEG_D2R_P<3>	E5	PE0_RX3_P	PE0_TX3_P	B3	=PEG_R2D_C_P<3>
9	IN	=PEG_D2R_N<3>	F5	PE0_RX3_N	PE0_TX3_N	B2	=PEG_R2D_C_N<3>
9	IN	=PEG_D2R_P<4>	E4	PE0_RX4_P	PE0_TX4_P	C1	=PEG_R2D_C_P<4>
9	IN	=PEG_D2R_N<4>	E3	PE0_RX4_N	PE0_TX4_N	D1	=PEG_R2D_C_N<4>
9	IN	=PEG_D2R_P<5>	C3	PE0_RX5_P	PE0_TX5_P	D2	=PEG_R2D_C_P<5>
9	IN	=PEG_D2R_N<5>	D3	PE0_RX5_N	PE0_TX5_N	E1	=PEG_R2D_C_N<5>
9	IN	=PEG_D2R_P<6>	G5	PE0_RX6_P	PE0_TX6_P	E2	=PEG_R2D_C_P<6>
9	IN	=PEG_D2R_N<6>	H5	PE0_RX6_N	PE0_TX6_N	F2	=PEG_R2D_C_N<6>
9	IN	=PEG_D2R_P<7>	J7	PE0_RX7_P	PE0_TX7_P	F3	=PEG_R2D_C_P<7>
9	IN	=PEG_D2R_N<7>	J6	PE0_RX7_N	PE0_TX7_N	F4	=PEG_R2D_C_N<7>
9	IN	=PEG_D2R_P<8>	J5	PE0_RX8_P	PE0_TX8_P	G3	=PEG_R2D_C_P<8>
9	IN	=PEG_D2R_N<8>	J4	PE0_RX8_N	PE0_TX8_N	H4	=PEG_R2D_C_N<8>
9	IN	=PEG_D2R_P<9>	L11	PE0_RX9_P	PE0_TX9_P	H3	=PEG_R2D_C_P<9>
9	IN	=PEG_D2R_N<9>	L10	PE0_RX9_N	PE0_TX9_N	H2	=PEG_R2D_C_N<9>
9	IN	=PEG_D2R_P<10>	L9	PE0_RX10_P	PE0_TX10_P	H1	=PEG_R2D_C_P<10>
9	IN	=PEG_D2R_N<10>	L8	PE0_RX10_N	PE0_TX10_N	J1	=PEG_R2D_C_N<10>
9	IN	=PEG_D2R_P<11>	L7	PE0_RX11_P	PE0_TX11_P	J2	=PEG_R2D_C_P<11>
9	IN	=PEG_D2R_N<11>	L6	PE0_RX11_N	PE0_TX11_N	J3	=PEG_R2D_C_N<11>
9	IN	=PEG_D2R_P<12>	N11	PE0_RX12_P	PE0_TX12_P	K2	=PEG_R2D_C_P<12>
9	IN	=PEG_D2R_N<12>	N10	PE0_RX12_N	PE0_TX12_N	K3	=PEG_R2D_C_N<12>
9	IN	=PEG_D2R_P<13>	N9	PE0_RX13_P	PE0_TX13_P	L4	=PEG_R2D_C_P<13>
9	IN	=PEG_D2R_N<13>	P9	PE0_RX13_N	PE0_TX13_N	L3	=PEG_R2D_C_N<13>
9	IN	=PEG_D2R_P<14>	N7	PE0_RX14_P	PE0_TX14_P	M4	=PEG_R2D_C_P<14>
9	IN	=PEG_D2R_N<14>	N6	PE0_RX14_N	PE0_TX14_N	M3	=PEG_R2D_C_N<14>
9	IN	=PEG_D2R_P<15>	N5	PE0_RX15_P	PE0_TX15_P	M2	=PEG_R2D_C_P<15>
9	IN	=PEG_D2R_N<15>	N4	PE0_RX15_N	PE0_TX15_N	M1	=PEG_R2D_C_N<15>

					PE0_REFCLK_P	E11	PEG_CLK100M_P
9	IN	PEG_PRSNT_L	C9	Int PU PE0_PRSNT_16#	PE0_REFCLK_N	D11	PEG_CLK100M_N
31	IN	MINI_CLKREQ_L	D5	Int PU PEB_CLKREQ#/GPIO_49	PE1_REFCLK_P	G11	PCIE_CLK100M_MINI_P
31	IN	PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU	PE1_REFCLK_N	F11	PCIE_CLK100M_MINI_N
37	IN	FW_CLKREQ_L	E8	Int PU PEC_CLKREQ#/GPIO_50	PE2_REFCLK_P	J11	PCIE_CLK100M_FW_P
37 9	IN	PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU	PE2_REFCLK_N	J10	PCIE_CLK100M_FW_N
9	IN	TP_EXCARD_CLKREQ_L	M15	Int PU PED_CLKREQ#/GPIO_51	PE3_REFCLK_P	G13	TP_PCIE_CLK100M_EXCARD_P
9	IN	TP_PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU	PE3_REFCLK_N	F13	TP_PCIE_CLK100M_EXCARD_N
		TP_PE4_CLKREQ_L	L16	Int PU PEE_CLKREQ#/GPIO_16	PE4_REFCLK_P	J13	NC_PCIE_CLK100M_PE4P
7		NC_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46	PE4_REFCLK_N	H13	NC_PCIE_CLK100M_PE4N
60		AUD_IP_PERIPHERAL_DET	M16	Int PU PEF_CLKREQ#/GPIO_17	PE5_REFCLK_P	L14	NC_PCIE_CLK100M_PE5P
84	OUT	GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47	PE5_REFCLK_N	K14	NC_PCIE_CLK100M_PE5N
32	OUT	CARDREADER_RESET	M17	Int PU PEG_CLKREQ#/GPIO_18	PE6_REFCLK_P	N14	NC_PCIE_CLK100M_PE6P
84 9 6	IN	JTAG_GMUX_TDO	M19	PEG_PRSNT#/GPIO_48	PE6_REFCLK_N	M14	TP_PCIE_CLK100M_PE6N
31 7	IN	PCIE_WAKE_L	F17	Int PU PE_WAKE# Int PU (S5)	PEX_RST0#	K11	PCIE_RESET_L
90 31 7	IN	PCIE_MINI_D2R_P	K9	PE1_RX0_P	PE1_TX0_P	D8	PCIE_MINI_R2D_C_P
90 31 7	IN	PCIE_MINI_D2R_N	J9	PE1_RX0_N	PE1_TX0_N	C8	PCIE_MINI_R2D_C_N
90 36	IN	PCIE_FW_D2R_P	H9	PE1_RX1_P	PE1_TX1_P	B8	PCIE_FW_R2D_C_P
90 36	IN	PCIE_FW_D2R_N	G9	PE1_RX1_N	PE1_TX1_N	A8	PCIE_FW_R2D_C_N
90 9	IN	TP_PCIE_EXCARD_D2R_P	F9	PE1_RX2_P	PE1_TX2_P	A7	TP_PCIE_EXCARD_R2D_C_P
90 9	IN	TP_PCIE_EXCARD_D2R_N	E9	PE1_RX2_N	PE1_TX2_N	B7	TP_PCIE_EXCARD_R2D_C_N
		TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	PE1_TX3_P	B6	TP_PCIE_PE4_R2D_CP
7		NC_PCIE_PE4_D2RN	G7	PE1_RX3_N	PE1_TX3_N	C6	NC_PCIE_PE4_R2D_CN

18 17 14 13 12 11 10 9 8 7 6 5 67 63 25 24 22 20		PPCPUVTT_S0 57 mA (A01, DVDD0 & 1)	T17	+DVDD0_PEX1	+AVDD0_PEX1	Y12	PP1V05_S0_MCP_PEX_AVDD 206 mA (A01, AVDD0 & 1)
			W19	+DVDD0_PEX2	+AVDD0_PEX2	AA12	
			U17	+DVDD0_PEX3	+AVDD0_PEX3	AB12	
			V19	+DVDD0_PEX4	+AVDD0_PEX4	M12	
			W16	+DVDD0_PEX5	+AVDD0_PEX5	P12	
			W17	+DVDD0_PEX6	+AVDD0_PEX6	R12	
			W18	+DVDD0_PEX7	+AVDD0_PEX7	N12	
			U16	+DVDD0_PEX8	+AVDD0_PEX8	T12	
					+AVDD0_PEX9	U12	
18 17 14 13 12 11 10 9 8 7 6 5 67 63 25 24 22 20		PPCPUVTT_S0	T19	+DVDD1_PEX1	+AVDD0_PEX10	AC12	
			U19	+DVDD1_PEX2	+AVDD0_PEX11	AD12	
					+AVDD0_PEX12	V12	
					+AVDD0_PEX13	W12	
24		PP1V05_S0_MCP_PLL_PEX 84 mA (A01)	T16	+V_PLL_PEX			PP1V05_S0_MCP_PEX_AVDD
					+AVDD1_PEX1	M13	
					+AVDD1_PEX2	N13	
					+AVDD1_PEX3	P13	
50		MCP_PEX_CLK_COMP	A11	PEX_CLK_COMP			

NO STUFF
1 R1710 2.37K 1% 1/16W MF-LF 402 2
PLACEMENT_NOTE=Place within 12.7mm of U1400

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

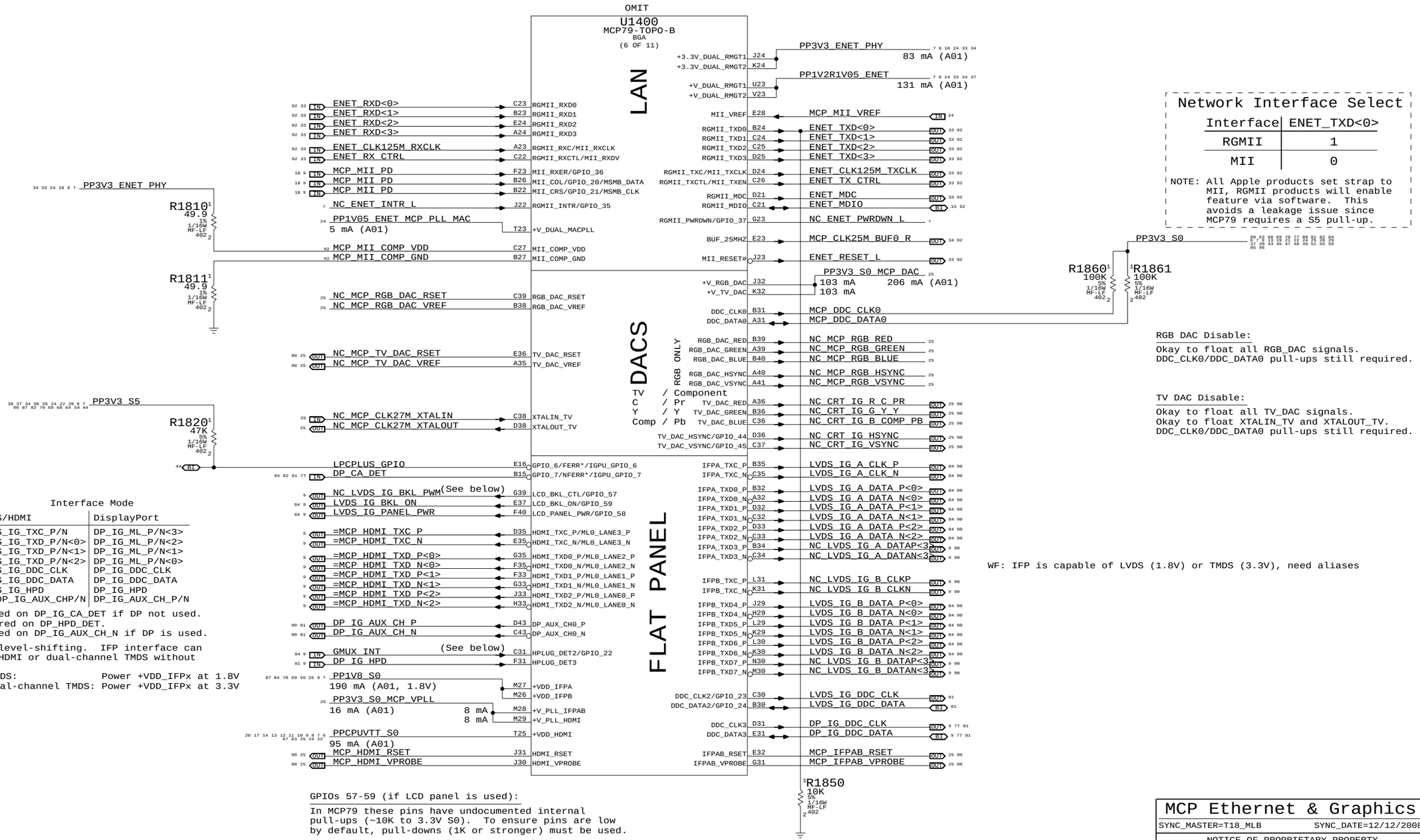
MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 17 OF 97	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 18 OF 97	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI

PCI_REQ0_L	T2	PCI_REQ0#	
PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2	
FW_PWR_EN	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	
AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	
MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	
MCP_DEBUG<0>	AC3	PCI_AD0	
MCP_DEBUG<1>	AE10	PCI_AD1	
MCP_DEBUG<2>	AC4	PCI_AD2	
MCP_DEBUG<3>	AE11	PCI_AD3	
MCP_DEBUG<4>	AB3	PCI_AD4	
MCP_DEBUG<5>	AC6	PCI_AD5	
MCP_DEBUG<6>	AB2	PCI_AD6	
MCP_DEBUG<7>	AC7	PCI_AD7	
NC_PCI_AD<8>	AC8	PCI_AD8	
NC_PCI_AD<9>	AA2	PCI_AD9	
NC_PCI_AD<10>	AC9	PCI_AD10	
NC_PCI_AD<11>	AC10	PCI_AD11	
NC_PCI_AD<12>	AC11	PCI_AD12	
NC_PCI_AD<13>	AA1	PCI_AD13	
NC_PCI_AD<14>	AA5	PCI_AD14	
NC_PCI_AD<15>	Y5	PCI_AD15	
NC_PCI_AD<16>	W3	PCI_AD16	
NC_PCI_AD<17>	W6	PCI_AD17	
NC_PCI_AD<18>	W4	PCI_AD18	
NC_PCI_AD<19>	W7	PCI_AD19	
NC_PCI_AD<20>	V3	PCI_AD20	
NC_PCI_AD<21>	W8	PCI_AD21	
NC_PCI_AD<22>	V2	PCI_AD22	
NC_PCI_AD<23>	W9	PCI_AD23	
NC_PCI_AD<24>	U3	PCI_AD24	
NC_PCI_AD<25>	W11	PCI_AD25	
NC_PCI_AD<26>	U2	PCI_AD26	
NC_PCI_AD<27>	U5	PCI_AD27	
NC_PCI_AD<28>	U1	PCI_AD28	
NC_PCI_AD<29>	U6	PCI_AD29	
NC_PCI_AD<30>	T5	PCI_AD30	
NC_PCI_AD<31>	U7	PCI_AD31	
NC_PCI_INTW_L	P2	PCI_INTW#	
NC_PCI_INTX_L	N3	PCI_INTX#	
TP_PCI_INTY_L	N2	PCI_INTY#	
NC_PCI_INTZ_L	N1	PCI_INTZ#	
NC_PCI_TRDY_L	Y3	PCI_TRDY#	
PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	
FW_PLUG_DET_L	AE2	PCI_DRQ1#/GPIO_19	Int PU
NC_LPC_DRQ0_L	AE1	LPC_DRQ0#	Int PU
LPC_SERIRQ	AE6	LPC_SERIRQ	Int PU

PCI_GNT0#	R3	NC_PCI_GNT0_L	
PCI_GNT1#/FANCTL2	U10	NC_PCI_GNT1_L	
PCI_GNT2#/GPIO_41/RS232_DTR#	R4	JTAG_GMUX_TMS	
PCI_GNT3#/GPIO_39/RS232_RTS#	U11	JTAG_GMUX_TDI	
PCI_GNT4#/GPIO_53/RS232_SOUT#	P3	MCP_RS232_SOUT_L	
PCI_CBE0#	AA3	NC_PCI_C_BE_L<0>	
PCI_CBE1#	AA6	NC_PCI_C_BE_L<1>	
PCI_CBE2#	AA11	NC_PCI_C_BE_L<2>	
PCI_CBE3#	W10	NC_PCI_C_BE_L<3>	
PCI_DEVSEL#	AA9	NC_PCI_DEVSEL_L	
PCI_FRAME#	Y4	NC_PCI_FRAME_L	
PCI_IRDY#	AA10	NC_PCI_IRDY_L	
PCI_PAR	Y1	TP_PCI_PAR	
PCI_PERR#/GPIO_43/RS232_DCD#	AB9	NC_PCI_PERR_L	
PCI_SERR#	AA7	NC_PCI_SERR_L	
PCI_STOP#	Y2	NC_PCI_STOP_L	
PCI_PME#/GPIO_30	T1	PM_LATRIGGER_L	
Int PU (S5)			
PCI_RESET0#	R10	MEM_VTT_EN_R	
PCI_RESET1#	R11	NC_PCI_RESET1_L	
PCI_CLK0	R6	NC_PCI_CLK0	
PCI_CLK1	R7	NC_PCI_CLK1	
PCI_CLK2	R8	PCI_CLK33M_MCP_R	
PCI_CLKIN	R9	PCI_CLK33M_MCP	

R1910
22
5% 1/16W MF-LF
402
PLACEMENT_NOTE=Place close to pin R8

LPC

LPC_FRAME#	AD4	LPC_FRAME_R_L	R1960 22	LPC_FRAME_L
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12	LPC_PWRDWN_L		
LPC_RESET0#	AE5	LPC_RESET_L		
LPC_AD0	AD3	LPC_AD_R<0>	R1950 22	LPC_AD<0>
LPC_AD1	AD2	LPC_AD_R<1>	R1951 22	LPC_AD<1>
LPC_AD2	AD1	LPC_AD_R<2>	R1952 22	LPC_AD<2>
LPC_AD3	AD5	LPC_AD_R<3>	R1953 22	LPC_AD<3>
LPC_CLK0	AE9	LPC_CLK33M_SMC_R		

5% 1/16W MF-LF 402

R1961
10K
5% 1/16W MF-LF
402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

GND65	U24	GND98	Y26
GND66	U26	GND99	Y27
GND67	U39	GND100	AB18
GND68	U4	GND101	H34
GND69	U8	GND102	AB20
GND70	V16	GND103	AB21
GND71	V17	GND104	AB23
GND72	V18	GND105	AB24
GND73	V20	GND106	AB25
GND74	V22	GND107	AB26
GND75	V24	GND108	AB27
GND76	V26	GND109	AB28
GND77	V27	GND110	AB34
GND78	V28	GND111	AB37
GND79	V33	GND112	AB4
GND80	V37	GND113	AB40
GND81	V4	GND114	AC22
GND82	V40	GND115	AC36
GND83	V7	GND116	AC40
GND84	W20	GND117	AB33
GND85	W22	GND118	AC5
GND86	W24	GND119	AD16
GND87	W36	GND120	AD17
GND88	W40	GND121	AD18
GND89	W43	GND122	AD19
GND90	Y16	GND123	AD20
GND91	Y17	GND124	AD24
GND92	Y18	GND125	AD25
GND93	Y19	GND126	AD26
GND94	Y20	GND127	AD27
GND95	Y22	GND128	AD28
GND96	Y24	GND129	AD33
GND97	Y25	GND130	AD34

PP3V3_S0

MCP_RS232_SOUT_L	R1989 8.2K	
PCI_REQ0_L	R1990 8.2K	
PCI_REQ1_L	R1991 8.2K	
FW_PWR_EN	R1992 8.2K	
MCP_RS232_SIN_L	R1994 8.2K	

5% 1/16W MF-LF 402

MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 19 OF 97	

OMIT

U1400
MCP79-TOPO-B
BGA
(8 OF 11)

SATA

90 39 OUT	SATA_HDD_R2D_C_P	AJ7	SATA_A0_TX_P
90 39 OUT	SATA_HDD_R2D_C_N	AJ6	SATA_A0_TX_N
90 39 IN	SATA_HDD_D2R_N	AJ5	SATA_A0_RX_N
90 39 IN	SATA_HDD_D2R_P	AJ4	SATA_A0_RX_P
90 39 OUT	SATA_ODD_R2D_C_P	AJ11	SATA_A1_TX_P
90 39 OUT	SATA_ODD_R2D_C_N	AJ10	SATA_A1_TX_N
90 39 IN	SATA_ODD_D2R_N	AJ9	SATA_A1_RX_N
90 39 IN	SATA_ODD_D2R_P	AK9	SATA_A1_RX_P
7	NC_SATA_C_R2D_CP	AK2	SATA_B0_TX_P
7	NC_SATA_C_R2D_CN	AJ3	SATA_B0_TX_N
	TP_SATA_C_D2RN	AJ2	SATA_B0_RX_N
7	NC_SATA_C_D2RP	AJ1	SATA_B0_RX_P
	TP_SATA_D_R2D_CP	AM4	SATA_B1_TX_P
	TP_SATA_D_R2D_CN	AL3	SATA_B1_TX_N
7	NC_SATA_D_D2RN	AL4	SATA_B1_RX_N
7	NC_SATA_D_D2RP	AK3	SATA_B1_RX_P
	TP_SATA_E_R2D_CP	AN1	SATA_C0_TX_P
	TP_SATA_E_R2D_CN	AM1	SATA_C0_TX_N
	TP_SATA_E_D2RN	AM2	SATA_C0_RX_N
	TP_SATA_E_D2RP	AM3	SATA_C0_RX_P
	TP_SATA_F_R2D_CP	AP3	SATA_C1_TX_P
	TP_SATA_F_R2D_CN	AP2	SATA_C1_TX_N
	TP_SATA_F_D2RN	AN3	SATA_C1_RX_N
	TP_SATA_F_D2RP	AN2	SATA_C1_RX_P
	TP_MCP_SATALED_L	E12	SATA_LED#
24	PP1V05_S0_MCP_PLL_SATA	AE16	+V_PLL_SATA
	84 mA (A01)		
18 17 14 13 12 11 10 9 8 7 6 67 63 25 24 22	PPCPUVTT_S0		
	43 mA (A01, DVDD0 & 1)	AF19	+DVDD0_SATA1
	Minimum 1.025V for Gen2 support	AG16	+DVDD0_SATA2
		AG17	+DVDD0_SATA3
		AG19	+DVDD0_SATA4
	GND	AH17	+DVDD1_SATA1
		AH19	+DVDD1_SATA2
24 8	PP1V05_S0_MCP_SATA_AVDD		
	127 mA (A01, AVDD0 & 1)	AJ12	+AVDD0_SATA1
	Minimum 1.025V for Gen2 support	AN11	+AVDD0_SATA2
		AK12	+AVDD0_SATA3
		AK13	+AVDD0_SATA4
		AL12	+AVDD0_SATA5
		AM11	+AVDD0_SATA6
		AM12	+AVDD0_SATA7
		AN12	+AVDD0_SATA8
		AL13	+AVDD0_SATA9
	GND	AN14	+AVDD1_SATA1
		AL14	+AVDD1_SATA2
		AM13	+AVDD1_SATA3
		AM14	+AVDD1_SATA4
90	MCP_SATA_TERMP	AE3	SATA_TERMP

R2010 2.49K 1% 1/16W MF-LF 402

USB

	External A		
USB0_P	C29	USB_EXTA_P	BI 40 91
USB0_N	D29	USB_EXTA_N	BI 40 91
	AirPort (PCIe Mini-Card)		
USB1_P	C28	NC_USB_MINIP	BI 9 91
USB1_N	D28	NC_USB_MININ	BI 9 91
	External D		
USB2_P	A28	NC_USB_EXTDP	BI 9 91
USB2_N	B28	NC_USB_EXTDN	BI 9 91
	Camera		
USB3_P	F29	USB_CAMERA_P	BI 7 31 91
USB3_N	G29	USB_CAMERA_N	BI 7 31 91
	IR		
USB4_P	K27	USB_IR_P	BI 41 91
USB4_N	L27	USB_IR_N	BI 41 91
	Geyser Trackpad/Keyboard		
USB5_P	J26	USB_TPAD_P	BI 50 91
USB5_N	J27	USB_TPAD_N	BI 50 91
	Bluetooth		
USB6_P	F27	USB_BT_P	BI 7 31 91
USB6_N	G27	USB_BT_N	BI 7 31 91
	External B		
USB7_P	D27	USB_EXTB_P	BI 40 91
USB7_N	E27	USB_EXTB_N	BI 40 91
	ExpressCard		
USB8_P	K25	NC_USB_EXCARDP	BI 9 91
USB8_N	L25	NC_USB_EXCARDN	BI 9 91
	External C		
USB9_P	H25	NC_USB_EXTCP	BI 9 91
USB9_N	J25	NC_USB_EXTCN	BI 9 91
USB10_P	F25	NC_USB_10P	7
USB10_N	G25	NC_USB_10N	7
	SD Card Reader		
USB11_P	K23	USB_CARDREADER_P	BI 9 32 96
USB11_N	L23	USB_CARDREADER_N	BI 9 32 96

USB_OC0#/GPIO_25	L21	USB_EXTA_OC_L 40
USB_OC1#/GPIO_26	K21	USB_EXTB_OC_L 40
USB_OC2#/GPIO_27/MGPIO	J21	USB_EXTC_OC_L
USB_OC3#/GPIO_28/MGPIO	H21	EXCARD_OC_L 43
+V_PLL_USB	L28	PP3V3_S0_MCP_PLL_USB 24
		19 mA (A01)
USB_RBIAS_GND	A27	91 MCP_USB_RBIAS_GND

R2060 806 1% 1/16W MF-LF 402

GND131	AD35
GND132	AD37
GND133	AD38
GND134	AE22
GND135	AE24
GND136	AE39
GND137	AE4
GND138	AD6
GND139	AF16
GND140	AF17
GND141	AF18
GND142	AF20
GND143	AF22
GND144	AF26
GND145	AF27
GND146	AF28
GND147	AF33
GND148	AF34
GND149	AF37
GND150	AF40
GND151	AG18
GND152	AG20
GND153	AG22
GND154	AG26
GND155	AG36
GND156	AG40
GND157	AH18
GND158	AH20
GND159	AH22
GND160	AH24

PP3V3_S5 7 8 18 22 24 26 30 34 37 38 44 54 64 68 69 78 82 87 96

R2051 8.2K 5% 1/16W MF-LF 402
R2053 8.2K 5% 1/16W MF-LF 402
R2050 8.2K 5% 1/16W MF-LF 402
R2052 8.2K 5% 1/16W MF-LF 402

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 20 OF 97	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(9 OF 11)

HDA

MISC

HDA_SDIN0 — G15 HDA_SDATA_IN0 — Int PD
NC_MLB_RAM_SIZE — J14 HDA_SDATA_IN1_GPIO_2/PS2_KB_CLK — Int PD
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems) — J15 HDA_SDATA_IN2_GPIO_3/PS2_KB_DATA — Int PD

PP3V3_S0 — R2110 49.9 1% 1/16W MF-LF 402 — MCP_HDA_PULLDN_COMP — A15 HDA_PULLDN_COMP

PP1V05_S0_MCP_PLL_NV — 37 mA (A01) — 20 mA / 17 mA — AE18 +V_PLL_NV_H, AE17 +V_PLL_SP_SPREF

PP3V42_G3H — R2120 49.9K 1% 1/16W MF-LF 402 — R2121 49.9K 1% 1/16W MF-LF 402

SPIROM_USE_MLB	L24	GPIO_1/PWRDN_OK/SPI_CS1
SMC_ADAPTER_EN	L26	GPIO_12_SUS_STAT_ACCLMTR_EXT_TRIG_L
NC_SB_A20GATE	K13	A20GATE — Int PU
TP_MCP_KBDRSTIN_L	L13	KBRDRSTIN* — Int PU
SMC_WAKE_SCI_L	C19	SIO_PME* — Int PU (S5)
SMC_RUNTIME_SCI_L	C18	EXT_SMI/GPIO_32* — Int PU (S5)
SM_INTRUDER_L	B20	INTRUDER*
TP_MCP_LID_L	M25	LID* — Int PU (S5)
PM_BATLOW_L	M24	LLB* — Int PU (S5)
PM_DPRSLPVR	M22	CPU_DPRSLPVR
PM_PWRBTN_L	C16	PWRBTN* — Int PU (S5)
PM_SYSRST_DEBOUNCE_L	D16	RSTBTN* — Int PU
RTC_RST_L	C20	RTC_RST*
PM_RSMRST_L	D20	PWRGD_SB
MCP_PS_PWRGD	E20	PS_PWRGD
MCP_CPU_VLD	C17	CPU_VLD
JTAG_MCP_TDI	E19	JTAG_TDI — Int PU
JTAG_MCP_TDO	F19	JTAG_TDO
JTAG_MCP_TMS	J19	JTAG_TMS — Int PU
JTAG_MCP_TRST_L	J18	JTAG_TRST*
JTAG_MCP_TCK	G19	JTAG_TCK
MCP_CLK25M_XTALIN	A16	XTALIN
MCP_CLK25M_XTALOUT	B16	XTALOUT
RTC_CLK32K_XTALIN	A19	XTALIN_RTC
RTC_CLK32K_XTALOUT	B19	XTALOUT_RTC

R2150 10K 5% 1/16W MF-LF 402 — R2151 100K 5% 1/16W MF-LF 402

PP3V3_S0 — 7 mA (A01) — R2160 8.2K 5% 1/16W MF-LF 402

+V_DUAL_HDA1 / +V_DUAL_HDA2	J16 / K16	
HDA_SDATA_OUT	F15	HDA_SDOUT_R — R2170 22 5% 1/16W MF-LF 402 — HDA_SDOUT
HDA_BITCLK	E15	HDA_BIT_CLK_R — R2171 22 5% 1/16W MF-LF 402 — HDA_BIT_CLK
HDA_RESET*	K15	HDA_RST_R_L — R2172 22 5% 1/16W MF-LF 402 — HDA_RST_L
HDA_SYNC	L15	HDA_SYNC_R — R2173 22 5% 1/16W MF-LF 402 — HDA_SYNC

HDA_DOCK_EN*_GPIO_4/PS2_MS_CLK	K17	MCP_GPIO_4
HDA_DOCK_RST*_GPIO_5/PS2_MS_DATA	L17	AUD_I2C_INT_L
SLP_S3*	G17	PM_SLP_S3_L
SLP_RMGT*	J17	PM_SLP_RMGT_L
SLP_S5*	H17	PM_SLP_S4_L
THERM_DIODE_P	B11	MCP_THMDIODE_P
THERM_DIODE_N	C11	MCP_THMDIODE_N
MCP_VID0/GPIO_13	L20	MCP_VID<0>
MCP_VID1/GPIO_14	M20	MCP_VID<1>
MCP_VID2/GPIO_15	M21	MCP_VID<2>
SPKR	C13	MCP_SPKR
SMB_CLK0	L19	SMBUS_MCP_0_CLK
SMB_DATA0	K19	SMBUS_MCP_0_DATA
SMB_CLK1/MSMB_CLK	G21	SMBUS_MCP_1_CLK
SMB_DATA1/MSMB_DATA	F21	SMBUS_MCP_1_DATA
SMB_ALERT*/GPIO_64	M23	AP_PWR_EN
(MGPIO2) FANRPM0/GPIO_60	B12	MEM_EVENT_L
FANCTL0/GPIO_61	A12	ODD_PWR_EN_L
(MGPIO3) FANRPM1/GPIO_63	D12	SMC_IG_THROTTLE_L
FANCTL1/GPIO_62	C12	ARB_DETECT
CPUVDD_EN	D17	MCP_CPUVDD_EN
SPI_CS0/GPIO_10	C14	SPI_CS0_R_L
SPI_CLK/GPIO_11	D13	SPI_CLK_R
SPI_DI/GPIO_8	C15	SPI_MISO
SPI_DO/GPIO_9	B14	SPI_MOSI_R
SUS_CLK/GPIO_34	B18	PM_CLK32K_SUSCLK_R
BUF_SIO_CLK	AE7	TP_MCP_BUF_SIO_CLK
TEST_MODE_EN	K22	MCP_TEST_MODE_EN
PKG_TEST	L22	

R2163 10K 5% 1/16W MF-LF 402 — R2190 1K 1% 1/16W MF-LF 402

PP3V3_S0 — BOOT_MODE_SAFE — R2180 10K 5% 1/16W MF-LF 402 — BOOT_MODE_USER — R2181 10K 5% 1/16W MF-LF 402

USER mode: Normal
SAFE mode: For ROMSIP recovery

Connects to SMC for automatic recovery.

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R — HDA_BIT_CLK_R — HDA_RST_R_L — HDA_SYNC_R

C2170 10PF 5% 50V CERM 402 — C2172 10PF 5% 50V CERM 402 — C2171 10PF 5% 50V CERM 402 — C2173 10PF 5% 50V CERM 402

PP3V3_S0 — R2140 10K — R2141 10K — R2142 10K — R2143 10K — MCP_GPIO_4, AUD_I2C_INT_L, MEM_EVENT_L, SMC_IG_THROTTLE_L

ARB_DETECT — R2147 100K

PP3V3_S3 — R2154 100K — AP_PWR_EN

MCP_VID<0>, MCP_VID<1>, MCP_VID<2> — R2155 22K — R2156 22K — R2157 22K

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0

SCALE: NONE — SHT 21 OF 97

OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

PPVCORE_S0_MCP_REG
66 46 24 9 7
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32		
AC23	+VDD_CORE2	+VTT_CPU2	AC32		
U25	+VDD_CORE3	+VTT_CPU3	E40		
AH12	+VDD_CORE4	+VTT_CPU4	J36		
AG10	+VDD_CORE5	+VTT_CPU5	N32		
AG5	+VDD_CORE6	+VTT_CPU6	T32		
Y21	+VDD_CORE7	+VTT_CPU7	U32		
Y23	+VDD_CORE8	+VTT_CPU8	V32		
AA16	+VDD_CORE9	+VTT_CPU9	W32		
AA26	+VDD_CORE10	+VTT_CPU10	P31		
AA27	+VDD_CORE11	+VTT_CPU11	AF32		
AA28	+VDD_CORE12	+VTT_CPU12	AE32		
AC16	+VDD_CORE13	+VTT_CPU13	AH32		
AC17	+VDD_CORE14	+VTT_CPU14	AJ32		
AC18	+VDD_CORE15	+VTT_CPU15	AK31		
AC19	+VDD_CORE16	+VTT_CPU16	AK32		
AC20	+VDD_CORE17	+VTT_CPU17	AD32		
AC21	+VDD_CORE18	+VTT_CPU18	AL31		
AA17	+VDD_CORE19	+VTT_CPU19	AB32		
AC24	+VDD_CORE20	+VTT_CPU20	B41		
AC25	+VDD_CORE21	+VTT_CPU21	B42		
AC26	+VDD_CORE22	+VTT_CPU22	C40		
AC27	+VDD_CORE23	+VTT_CPU23	C41		
AC28	+VDD_CORE24	+VTT_CPU24	C42		
AD21	+VDD_CORE25	+VTT_CPU25	D39		
AD23	+VDD_CORE26	+VTT_CPU26	D40		
W27	+VDD_CORE27	+VTT_CPU27	D41		
V25	+VDD_CORE28	+VTT_CPU28	E38		
AA18	+VDD_CORE29	+VTT_CPU29	E39		
AE19	+VDD_CORE30	+VTT_CPU30	F37		
AE21	+VDD_CORE31	+VTT_CPU31	F38		
AE23	+VDD_CORE32	+VTT_CPU32	F39		
AE25	+VDD_CORE33	+VTT_CPU33	G36		
AE26	+VDD_CORE34	+VTT_CPU34	G37		
AE27	+VDD_CORE35	+VTT_CPU35	G38		
AE28	+VDD_CORE36	+VTT_CPU36	H35		
AF10	+VDD_CORE37	+VTT_CPU37	H37		
AF11	+VDD_CORE38	+VTT_CPU38	J34		
AA19	+VDD_CORE39	+VTT_CPU39	J35		
AF2	+VDD_CORE40	+VTT_CPU40	K33		
AF21	+VDD_CORE41	+VTT_CPU41	K34		
AF23	+VDD_CORE42	+VTT_CPU42	K35		
AF25	+VDD_CORE43	+VTT_CPU43	L32		
AF3	+VDD_CORE44	+VTT_CPU44	L33		
AF4	+VDD_CORE45	+VTT_CPU45	L34		
AF7	+VDD_CORE46	+VTT_CPU46	M31		
AH23	+VDD_CORE47	+VTT_CPU47	M32		
AF9	+VDD_CORE48	+VTT_CPU48	M33		
AA20	+VDD_CORE49	+VTT_CPU49	N31		
AG11	+VDD_CORE50	+VTT_CPU50	P32		
AG12	+VDD_CORE51	+VTT_CPU51	Y32		
AG21	+VDD_CORE52	+VTT_CPU52	AA32		
AG23	+VDD_CORE53				
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32	43 mA	
AG3	+VDD_CORE55				
AG4	+VDD_CORE56				
AA21	+VDD_CORE57				
AG6	+VDD_CORE58				
AG7	+VDD_CORE59	+3.3V_1	AD10	PP3V3_S0	92 84 85 96 47 48 49 51 55 59 60 63 68 69 6 7 8 13 18 19 21 24 25 28 29 76 77 78
AG8	+VDD_CORE60	+3.3V_2	AE8	450 mA (A01)	
AG9	+VDD_CORE61	+3.3V_3	AB10		
AH1	+VDD_CORE62	+3.3V_4	AD9		
AH10	+VDD_CORE63	+3.3V_5	Y10		
AH11	+VDD_CORE64	+3.3V_6	AB11		
W26	+VDD_CORE65	+3.3V_7	AA8		
AH2	+VDD_CORE66	+3.3V_8	Y9		
AA23	+VDD_CORE67				
W28	+VDD_CORE68				
AH25	+VDD_CORE69				
AH21	+VDD_CORE70	+3.3V_DUAL1	G18	PP3V3_S5	79 82 87 90 4 26 30 34 37 38 44 14 17 20 64
AH3	+VDD_CORE71	+3.3V_DUAL2	H19	16 mA	266 mA (A01)
AH4	+VDD_CORE72	+3.3V_DUAL3	J20		
AH5	+VDD_CORE73	+3.3V_DUAL4	K20		
AH6	+VDD_CORE74				
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26	250 mA	
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27		
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28		
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28		
W23	+VDD_CORE79				
W25	+VDD_CORE80				
AF12	+VDD_CORE81				
		+VDD_AUXC1	T21	PP1V2R1V05_S5	7 8 24 34 68
		+VDD_AUXC2	U21	105 mA (A01)	
A20	+VBAT	+VDD_AUXC3	V21		

PP3V42_G3H
46 45 44 43 42 40 26 21 8 7 69 64 62 61 58
10 uA (G3)
80 uA (S0)

PPCPUVTT_S0
6 7 8 9 10 11 12 13 14 17 18 20 24 27 31 32
1139 mA
1182 mA (A01)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 22 OF 97	

MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE	SHT	OF
NONE	23	97

MCP Core Power
PPVCORE_S0_MCP_REG
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)
NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)
C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power
PPCPUVTT_S0
57 mA (A01)
C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power
PPCPUVTT_S0
43 mA (A01)
C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

PPCPUVTT_S0
333 mA (A01)
L2570 30-OHM-5A 0603
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)
C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

MCP 1.05V AUX Power
PP1V2R1V05_S5
105 mA (A01)
C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power
PP1V2R1V05_ENET
131 mA (A01)
C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)
L2575 30-OHM-5A 0603
C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF
PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

MCP FSB (VTT) Power
PPCPUVTT_S0
1182 mA (A01)
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)
C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PLL_UF
562 mA (A01)
L2580 30-OHM-1.7A 0402
C2580 4.7UF 20% 4V X5R 402
C2581 0.1UF 20% 10V CERM 402
PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

MCP Memory Power
PP1V8R1V5_S0_FET
4771 mA (A01, DDR3)
C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

L2582 30-OHM-1.7A 0402
C2582 4.7UF 20% 4V X5R 402
C2583 0.1UF 20% 10V CERM 402
PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

MCP 3.3V Power
PP3V3_S0
450 mA (A01)
NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)
C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

PP3V3_S0
19 mA (A01)
L2555 30-OHM-1.7A 0402
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2555 2.2UF 20% 6.3V CERM 402-LF
PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

L2584 30-OHM-1.7A 0402
C2584 4.7UF 20% 4V X5R 402
C2585 0.1UF 20% 10V CERM 402
PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

MCP 3.3V AUX/USB Power
PP3V3_S5
266 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power
PP3V3_ENET_PHY
83 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2564 2.2UF 20% 6.3V CERM 402-LF

L2586 30-OHM-1.7A 0402
C2586 4.7UF 20% 4V X5R 402
C2587 0.1UF 20% 10V CERM 402
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

MCP 3.3V/1.5V HDA Power
PP3V3_S0
7 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2562 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef
PP3V3_ENET_PHY
R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
C2591 0.1UF 20% 10V CERM 402
MCP_MII_VREF

PP1V2R1V05_ENET
5 mA (A01)
L2595 30-OHM-1.7A 0402
C2595 4.7UF 20% 4V X5R 402
C2596 0.1UF 20% 10V CERM 402
PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

L2588 30-OHM-1.7A 0402
C2588 4.7UF 20% 4V X5R 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402
PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=T18_MLB
SYNC_DATE=06/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 24 OF 97	

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

87 84 70 69 55 18 8 7 PP1V8_S0
190 mA (A01, 1.8V)
C2610 1 2 2.2UF 20% 6.3V X5R CERM 402-LF

18 17 14 13 12 11 10 9 8 7 6 67 63 24 22 20 PPCPUVTT_S0
95 mA (A01)
C2615 4.7UF 20% 6.3V X5R CERM 402
C2616 2.2UF 20% 6.3V X5R CERM 402-LF

90 18 MCP_HDMI_RSET
90 18 MCP_HDMI_VPROBE
NO STUFF
C2620 0.1UF 10% 16V CERM 402
R2620 1K 1% 1/16W MF-LF 402

90 18 MCP_IFPAB_RSET
90 18 MCP_IFPAB_VPROBE
NO STUFF
C2630 0.1UF 10% 16V CERM 402
R2630 1K 1% 1/16W MF-LF 402

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

84 82 81 80 77 70 69 68 63 60 29 28 24 22 21 15 18 13 4 3 0 59 55 51 49 48 47 45 42 39 37 32 33
PP3V3_S0
16 mA (A01)
L2640 30-OHM-1.7A 0402
C2640 4.7UF 20% 6.3V CERM 603
C2641 0.1UF 20% 10V CERM 402
PP3V3_S0_MCP_VPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18 16 mA (A01)

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)
PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18 206 mA (A01)
R2651 0 5% 1/16W MF-LF 402

25 18 NC_MCP_RGB_RED — NC_MCP_RGB_RED 18 25
25 18 NC_MCP_RGB_GREEN — NC_MCP_RGB_GREEN 18 25
25 18 NC_MCP_RGB_BLUE — NC_MCP_RGB_BLUE 18 25
25 18 NC_MCP_RGB_HSYNC — NC_MCP_RGB_HSYNC 18 25
25 18 NC_MCP_RGB_VSYNC — NC_MCP_RGB_VSYNC 18 25
90 25 18 NC_CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR 18 25 90
90 25 18 NC_CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y 18 25 90
90 25 18 NC_CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB 18 25 90
90 25 18 NC_CRT_IG_HSYNC — NC_CRT_IG_HSYNC 18 25 90
90 25 18 NC_CRT_IG_VSYNC — NC_CRT_IG_VSYNC 18 25 90
25 18 NC_MCP_RGB_DAC_RSET — NC_MCP_RGB_DAC_RSET 18 25
25 18 NC_MCP_RGB_DAC_VREF — NC_MCP_RGB_DAC_VREF 18 25
90 25 18 NC_MCP_TV_DAC_RSET — NC_MCP_TV_DAC_RSET 18 25 90
90 25 18 NC_MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF 18 25 90
25 18 NC_MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN 18 25
25 18 NC_MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT 18 25
MAKE_BASE=TRUE NO_TEST=TRUE

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

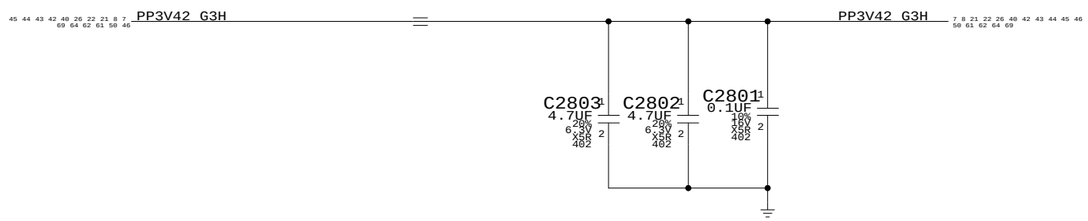
MCP Graphics Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

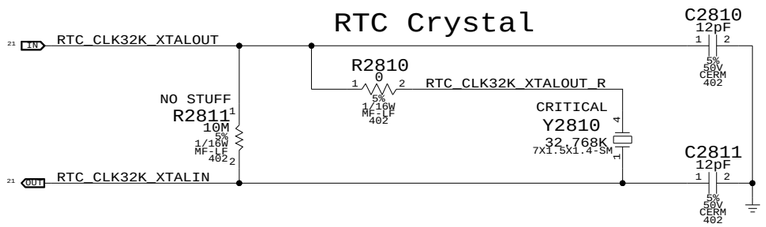
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 25 OF 97	

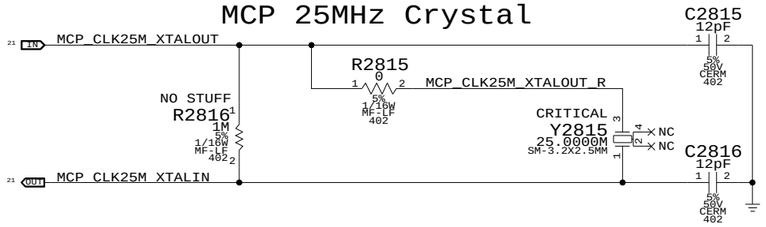
RTC Power Sources



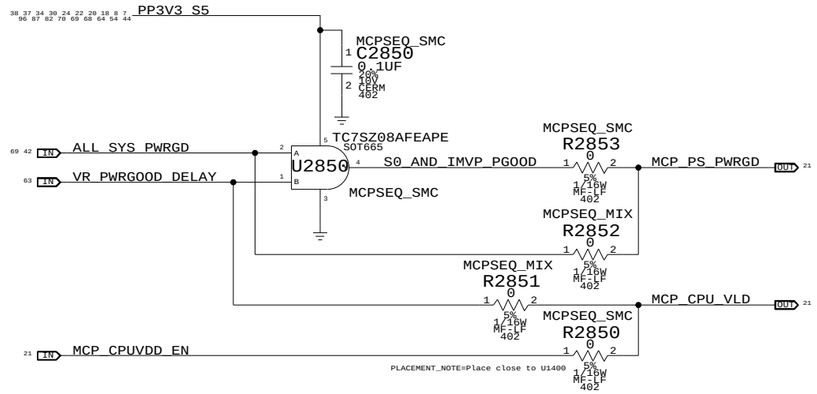
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

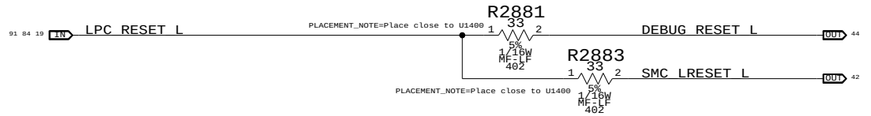
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

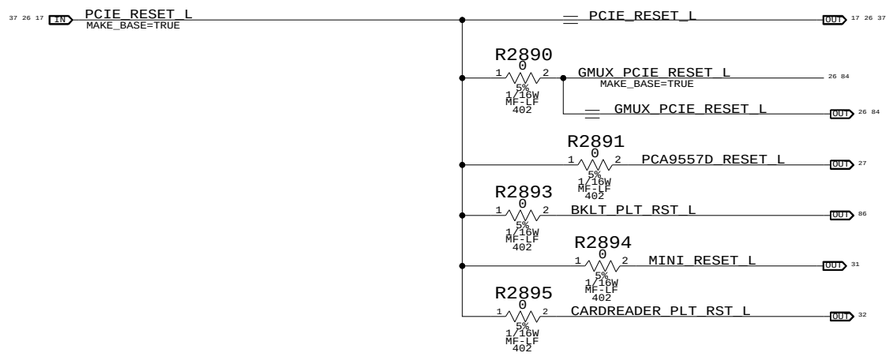
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

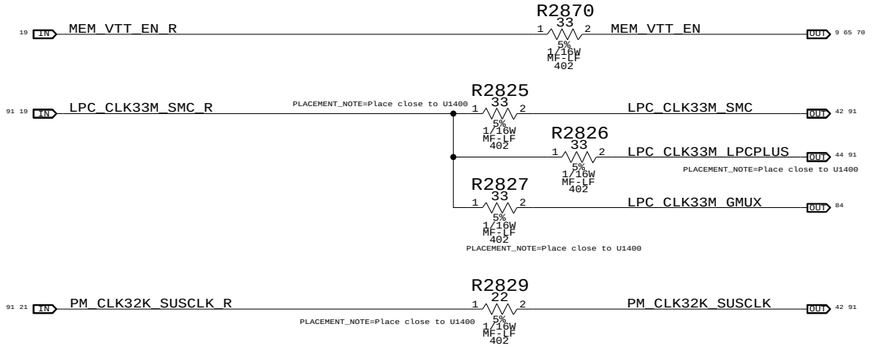
Platform Reset Connections

LPC Reset (Unbuffered)

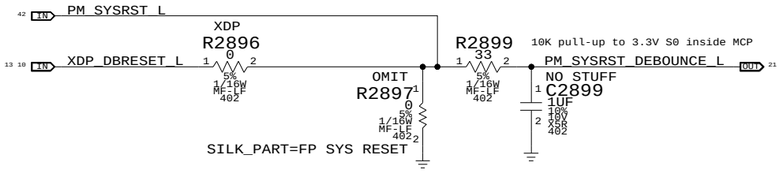


PCIE Reset (Unbuffered)





Reset Button



SB Misc		
SYNC_MASTER=DDR		SYNC_DATE=12/15/2008

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
	SCALE: NONE	SHT 26 OF 97	

Page Notes

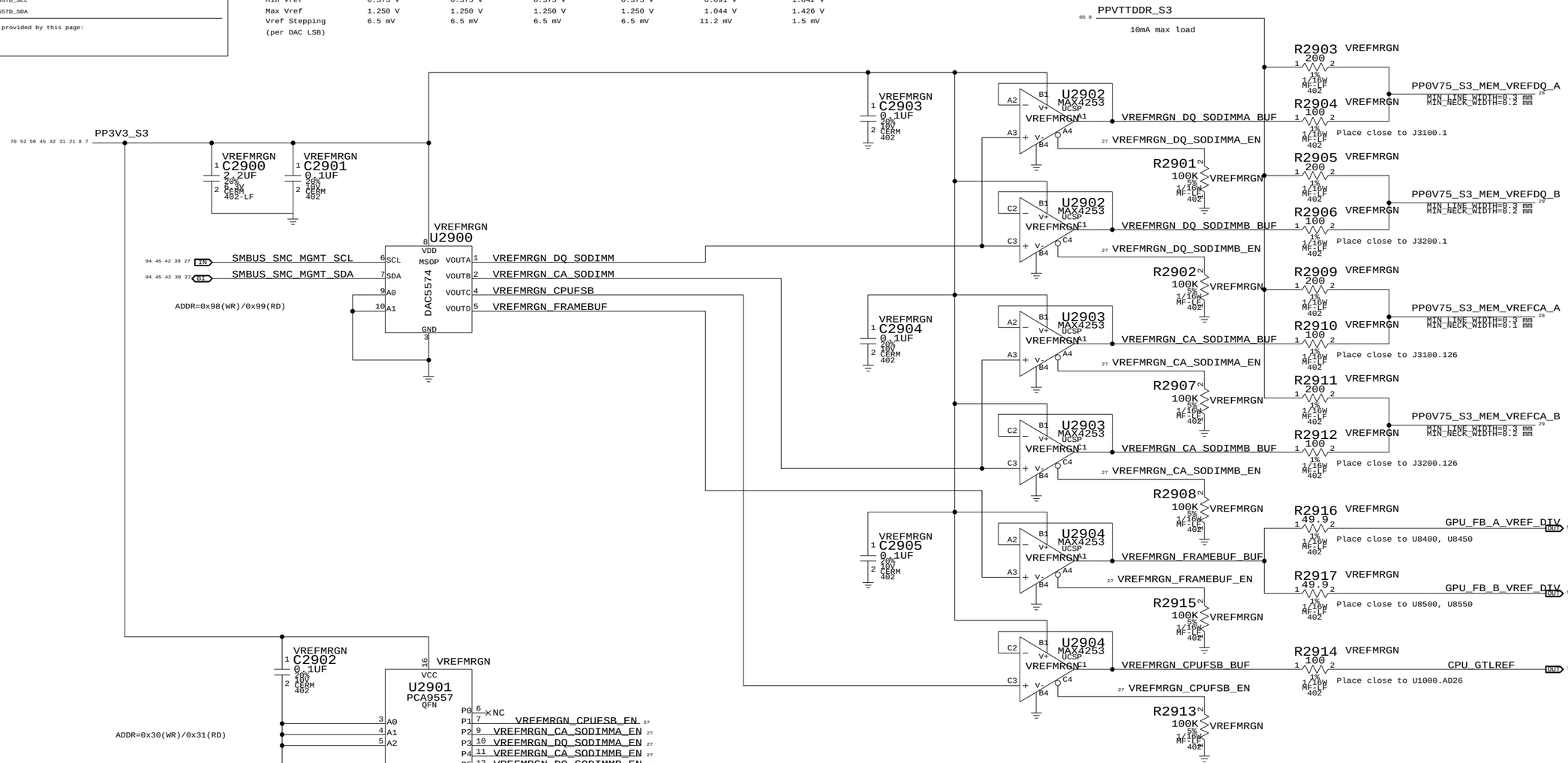
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C	FRAME BUFFER VREF D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=DDR SYNC_DATE=12/05/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 27 OF 97	

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

69 68 39 29 24 16 12 11 8 7 PP1V8R1V5_S0_FET

70 65 30 29 8 7 PP1V8R1V5_S3

C3100 10UF 20% 6.3V X6S 603
C3101 10UF 20% 6.3V X6S 603
C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

27 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

89 15 IN	MEM_A_CKE<0>	73	CKE0	CKE1	74	MEM_A_CKE<1>	IN 15 89
		75	VDD	VDD	76		
		77	NC	A15	78	TP_MEM_A_A<15>	IN 9
89 15 IN	MEM_A_BA<2>	79	BA2	A14	80	MEM_A_A<14>	IN 15 89
		81	VDD	VDD	82		
89 15 IN	MEM_A_A<12>	83	A12/BC*	A11	84	MEM_A_A<11>	IN 15 89
89 15 IN	MEM_A_A<9>	85	A9	A7	86	MEM_A_A<7>	IN 15 89
		87	VDD	VDD	88		
89 15 IN	MEM_A_A<8>	89	A8	A6	90	MEM_A_A<6>	IN 15 89
89 15 IN	MEM_A_A<5>	91	A5	A4	92	MEM_A_A<4>	IN 15 89
		93	VDD	VDD	94		
89 15 IN	MEM_A_A<3>	95	A3	A2	96	MEM_A_A<2>	IN 15 89
89 15 IN	MEM_A_A<1>	97	A1	A0	98	MEM_A_A<0>	IN 15 89
		99	VDD	VDD	100		
89 15 IN	MEM_A_CLK_P<0>	101	CK0	CK1	102	MEM_A_CLK_P<1>	IN 15 89
89 15 IN	MEM_A_CLK_N<0>	103	CK0*	CK1*	104	MEM_A_CLK_N<1>	IN 15 89
		105	VDD	VDD	106		
89 15 IN	MEM_A_A<10>	107	A10/AP	BA1	108	MEM_A_BA<1>	IN 15 89
89 15 IN	MEM_A_BA<0>	109	BA0	RAS*	110	MEM_A_RAS_L	IN 15 89
		111	VDD	VDD	112		
89 15 IN	MEM_A_WE_L	113	WE*	S0*	114	MEM_A_CS_L<0>	IN 15 89
89 15 IN	MEM_A_CAS_L	115	CAS*	ODT0	116	MEM_A_ODT<0>	IN 15 89
		117	VDD	VDD	118		
89 15 IN	MEM_A_A<13>	119	A13	ODT1	120	MEM_A_ODT<1>	IN 15 89
89 15 IN	MEM_A_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
89 15 BI	MEM_A_DQ<33>	129	DQ32	DQ36	130	MEM_A_DQ<36>	BI 15 89
89 15 BI	MEM_A_DQ<32>	131	DQ33	DQ37	132	MEM_A_DQ<37>	BI 15 89
		133	VSS	VSS	134		
89 15 BI	MEM_A_DQS_N<4>	135	DQS4*	DM4	136	MEM_A_DM<4>	IN 15 89
89 15 BI	MEM_A_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_A_DQ<38>	BI 15 89
89 15 BI	MEM_A_DQ<34>	141	DQ34	DQ39	142	MEM_A_DQ<39>	BI 15 89
89 15 BI	MEM_A_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_A_DQ<47>	BI 15 89
89 15 BI	MEM_A_DQ<44>	147	DQ40	DQ45	148	MEM_A_DQ<40>	BI 15 89
89 15 BI	MEM_A_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_A_DQS_N<5>	BI 15 89
89 15 IN	MEM_A_DM<5>	153	DM5	DQS5	154	MEM_A_DQS_P<5>	BI 15 89
		155	VSS	VSS	156		
89 15 BI	MEM_A_DQ<45>	157	DQ42	DQ46	158	MEM_A_DQ<46>	BI 15 89
89 15 BI	MEM_A_DQ<42>	159	DQ43	DQ47	160	MEM_A_DQ<43>	BI 15 89
		161	VSS	VSS	162		
89 15 BI	MEM_A_DQ<52>	163	DQ48	DQ52	164	MEM_A_DQ<48>	BI 15 89
89 15 BI	MEM_A_DQ<51>	165	DQ49	DQ53	166	MEM_A_DQ<53>	BI 15 89
		167	VSS	VSS	168		
89 15 BI	MEM_A_DQS_N<6>	169	DQS6*	DM6	170	MEM_A_DM<6>	IN 15 89
89 15 BI	MEM_A_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_A_DQ<50>	BI 15 89
89 15 BI	MEM_A_DQ<55>	175	DQ50	DQ55	176	MEM_A_DQ<49>	BI 15 89
89 15 BI	MEM_A_DQ<54>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_A_DQ<57>	BI 15 89
89 15 BI	MEM_A_DQ<61>	181	DQ56	DQ61	182	MEM_A_DQ<56>	BI 15 89
89 15 BI	MEM_A_DQ<60>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_A_DQS_N<7>	BI 15 89
89 15 IN	MEM_A_DM<7>	187	DM7	DQS7	188	MEM_A_DQS_P<7>	BI 15 89
		189	VSS	VSS	190		
89 15 BI	MEM_A_DQ<58>	191	DQ58	DQ62	192	MEM_A_DQ<62>	BI 15 89
89 15 BI	MEM_A_DQ<59>	193	DQ59	DQ63	194	MEM_A_DQ<63>	BI 15 89
		195	VSS	VSS	196		
	MEM_A_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT 21 29 42
		199	VDDSPD	SDA	200	SMBUS_MCP_0_DATA	BI 13 21 29 45 91
	MEM_A_SA<1>	201	SA1	SCL	202	SMBUS_MCP_0_CLK	IN 13 21 29 45 91
		203	VTT	VTT	204	PP0V9R0V75_S0_DDRVTT	7 8 29 65 70

516-0196
SPD ADDR=0xA0(WR)/0xA1(RD)

89 84 82 81 80 61 49 47 46 19 18 13 8 7 6 43 32 27 26 25 24 22 21 77 76 65 58 53 50 49 66

PP3V3_S0

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

PP0V75_S3_MEM_VREFCA_A 27

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)
CRITICAL

		1	VREFDQ	VSS	2		
		3	VSS	DQ4	4	MEM_A_DQ<4>	BI 15 89
89 15 BI	MEM_A_DQ<0>	5	DQ0	DQ5	6	MEM_A_DQ<5>	BI 15 89
89 15 BI	MEM_A_DQ<1>	7	DQ1	VSS	8		
		9	VSS	DQS0*	10	MEM_A_DQS_N<0>	BI 15 89
89 15 IN	MEM_A_DM<0>	11	DM0	DQS0	12	MEM_A_DQS_P<0>	BI 15 89
		13	VSS	VSS	14		
89 15 BI	MEM_A_DQ<3>	15	DQ2	DQ6	16	MEM_A_DQ<6>	BI 15 89
89 15 BI	MEM_A_DQ<2>	17	DQ3	DQ7	18	MEM_A_DQ<7>	BI 15 89
		19	VSS	VSS	20		
89 15 BI	MEM_A_DQ<9>	21	DQ8	DQ12	22	MEM_A_DQ<8>	BI 15 89
89 15 BI	MEM_A_DQ<13>	23	DQ9	DQ13	24	MEM_A_DQ<12>	BI 15 89
		25	VSS	VSS	26		
89 15 BI	MEM_A_DQS_N<1>	27	DQS1*	DM1	28	MEM_A_DM<1>	IN 15 89
89 15 BI	MEM_A_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 29 30
		31	VSS	VSS	32		
89 15 BI	MEM_A_DQ<11>	33	DQ10	DQ14	34	MEM_A_DQ<15>	BI 15 89
89 15 BI	MEM_A_DQ<14>	35	DQ11	DQ15	36	MEM_A_DQ<10>	BI 15 89
		37	VSS	VSS	38		
89 15 BI	MEM_A_DQ<16>	39	DQ16	DQ20	40	MEM_A_DQ<21>	BI 15 89
89 15 BI	MEM_A_DQ<18>	41	DQ17	DQ21	42	MEM_A_DQ<20>	BI 15 89
		43	VSS	VSS	44		
89 15 BI	MEM_A_DQS_N<2>	45	DQS2*	DM2	46	MEM_A_DM<2>	IN 15 89
89 15 BI	MEM_A_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_A_DQ<17>	BI 15 89
89 15 BI	MEM_A_DQ<23>	51	DQ18	DQ23	52	MEM_A_DQ<22>	BI 15 89
89 15 BI	MEM_A_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_A_DQ<29>	BI 15 89
89 15 BI	MEM_A_DQ<24>	57	DQ24	DQ29	58	MEM_A_DQ<28>	BI 15 89
89 15 BI	MEM_A_DQ<30>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_A_DQS_N<3>	BI 15 89
89 15 IN	MEM_A_DM<3>	63	DM3	DQS3	64	MEM_A_DQS_P<3>	BI 15 89
		65	VSS	VSS	66		
89 15 BI	MEM_A_DQ<27>	67	DQ26	DQ30	68	MEM_A_DQ<26>	BI 15 89
89 15 BI	MEM_A_DQ<25>	69	DQ27	DQ31	70	MEM_A_DQ<31>	BI 15 89
		71	VSS	VSS	72		

KEY
516-0196

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 28 OF 97	

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM0_SCL
- =I2C_SODIMM0_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

69 68 39 28 24 16 12 11 8 7 PP1V8R1V5_S0_FET

70 65 30 28 8 7 PP1V8R1V5_S3

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X6S 603
C3201 10UF 20% 6.3V X6S 603

27 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 DDR3-SODIMM (2 OF 2) F-RT-BGA3

KEY

89 15 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 15 89
		75	VDD	VDD	76		
		77	NC	A15	78	TP_MEM_B_A<15>	IN 9
89 15 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 15 89
		81	VDD	VDD	82		
89 15 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 15 89
89 15 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 15 89
		87	VDD	VDD	88		
89 15 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 15 89
89 15 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 15 89
		93	VDD	VDD	94		
89 15 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 15 89
89 15 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 15 89
		99	VDD	VDD	100		
89 15 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 15 89
89 15 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 15 89
		105	VDD	VDD	106		
89 15 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 15 89
89 15 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 15 89
		111	VDD	VDD	112		
89 15 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 15 89
89 15 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 15 89
		117	VDD	VDD	118		
89 15 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 15 89
89 15 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
89 15 BI	MEM_B_DQ<32>	129	DQ32	DQ36	130	MEM_B_DQ<33>	BI 15 89
89 15 BI	MEM_B_DQ<37>	131	DQ33	DQ37	132	MEM_B_DQ<36>	BI 15 89
		133	VSS	VSS	134		
89 15 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 15 89
89 15 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	BI 15 89
89 15 BI	MEM_B_DQ<34>	141	DQ34	DQ39	142	MEM_B_DQ<39>	BI 15 89
89 15 BI	MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<44>	BI 15 89
89 15 BI	MEM_B_DQ<41>	147	DQ40	DQ45	148	MEM_B_DQ<45>	BI 15 89
89 15 BI	MEM_B_DQ<40>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 15 89
89 15 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 15 89
		155	VSS	VSS	156		
89 15 BI	MEM_B_DQ<43>	157	DQ42	DQ46	158	MEM_B_DQ<47>	BI 15 89
89 15 BI	MEM_B_DQ<42>	159	DQ43	DQ47	160	MEM_B_DQ<46>	BI 15 89
		161	VSS	VSS	162		
89 15 BI	MEM_B_DQ<55>	163	DQ48	DQ52	164	MEM_B_DQ<48>	BI 15 89
89 15 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<54>	BI 15 89
		167	VSS	VSS	168		
89 15 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 15 89
89 15 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<53>	BI 15 89
89 15 BI	MEM_B_DQ<52>	175	DQ50	DQ55	176	MEM_B_DQ<50>	BI 15 89
89 15 BI	MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<60>	BI 15 89
89 15 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<61>	BI 15 89
89 15 BI	MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 15 89
89 15 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 15 89
		189	VSS	VSS	190		
89 15 BI	MEM_B_DQ<63>	191	DQ58	DQ62	192	MEM_B_DQ<58>	BI 15 89
89 15 BI	MEM_B_DQ<59>	193	DQ59	DQ63	194	MEM_B_DQ<62>	BI 15 89
		195	VSS	VSS	196		
MEM_B_SA<0>		197	SA0	EVENT*	198	MEM_EVENT_L	OUT 21 28 42
		199	VDDSPD	SDA	200	SMBUS_MCP_0_DATA	BI 13 21 28 45 91
MEM_B_SA<1>		201	SA1	SCL	202	SMBUS_MCP_0_CLK	IN 13 21 28 45 91
		203	VTT	VTT	204	PP0V9R0V75_S0_DDRVTT	7 8 28 65 70
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

MTG PINS

516s0704

SPD ADDR=0xA2(WR)/0xA3(RD)

R3240 10K 5% 1/16W MF-LF 402

60 59 55 51 49 46 PP3V3_S0
47 45 43 39 37 34
84 82 81 80 77 76 69 66 63

C3240 2.2UF 20% 6.3V CERM 402-LF

R3241 10K 5% 1/16W MF-LF 402

J3200 DDR3-SODIMM (1 OF 2) F-RT-BGA3

CRITICAL

KEY

	1	VREFDQ	VSS	2	
89 15 BI	MEM_B_DQ<0>	3	VSS	DQ4	4	MEM_B_DQ<4>	BI 15 89
89 15 BI	MEM_B_DQ<1>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 15 89
		7	DQ1	VSS	8		
89 15 IN	MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 15 89
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 15 89
		13	VSS	VSS	14		
89 15 BI	MEM_B_DQ<2>	15	DQ2	DQ6	16	MEM_B_DQ<6>	BI 15 89
89 15 BI	MEM_B_DQ<3>	17	DQ3	DQ7	18	MEM_B_DQ<7>	BI 15 89
		19	VSS	VSS	20		
89 15 BI	MEM_B_DQ<28>	21	DQ8	DQ12	22	MEM_B_DQ<29>	BI 15 89
89 15 BI	MEM_B_DQ<24>	23	DQ9	DQ13	24	MEM_B_DQ<25>	BI 15 89
		25	VSS	VSS	26		
89 15 BI	MEM_B_DQS_N<3>	27	DQS1*	DM1	28	MEM_B_DM<3>	IN 15 89
89 15 BI	MEM_B_DQS_P<3>	29	DQS1	RESET*	30	MEM_RESET_L	IN 28 30
		31	VSS	VSS	32		
89 15 BI	MEM_B_DQ<31>	33	DQ10	DQ14	34	MEM_B_DQ<26>	BI 15 89
89 15 BI	MEM_B_DQ<30>	35	DQ11	DQ15	36	MEM_B_DQ<27>	BI 15 89
		37	VSS	VSS	38		
89 15 BI	MEM_B_DQ<9>	39	DQ16	DQ20	40	MEM_B_DQ<13>	BI 15 89
89 15 BI	MEM_B_DQ<8>	41	DQ17	DQ21	42	MEM_B_DQ<12>	BI 15 89
		43	VSS	VSS	44		
89 15 BI	MEM_B_DQS_N<1>	45	DQS2*	DM2	46	MEM_B_DM<1>	IN 15 89
89 15 BI	MEM_B_DQS_P<1>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<14>	BI 15 89
89 15 BI	MEM_B_DQ<15>	51	DQ18	DQ23	52	MEM_B_DQ<11>	BI 15 89
89 15 BI	MEM_B_DQ<10>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<20>	BI 15 89
89 15 BI	MEM_B_DQ<21>	57	DQ24	DQ29	58	MEM_B_DQ<16>	BI 15 89
89 15 BI	MEM_B_DQ<17>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<2>	BI 15 89
89 15 IN	MEM_B_DM<2>	63	DM3	DQS3	64	MEM_B_DQS_P<2>	BI 15 89
		65	VSS	VSS	66		
89 15 BI	MEM_B_DQ<18>	67	DQ26	DQ30	68	MEM_B_DQ<19>	BI 15 89
89 15 BI	MEM_B_DQ<22>	69	DQ27	DQ31	70	MEM_B_DQ<23>	BI 15 89
		71	VSS	VSS	72		

516s0704

PP0V75_S3_MEM_VREFCA_B 27

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC_MASTER=ODR SYNC_DATE=07/22/2008

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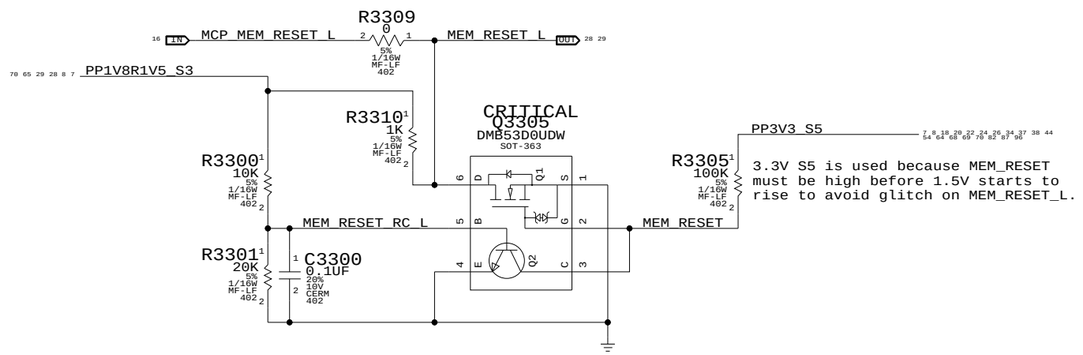
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 29 OF 97	

DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.

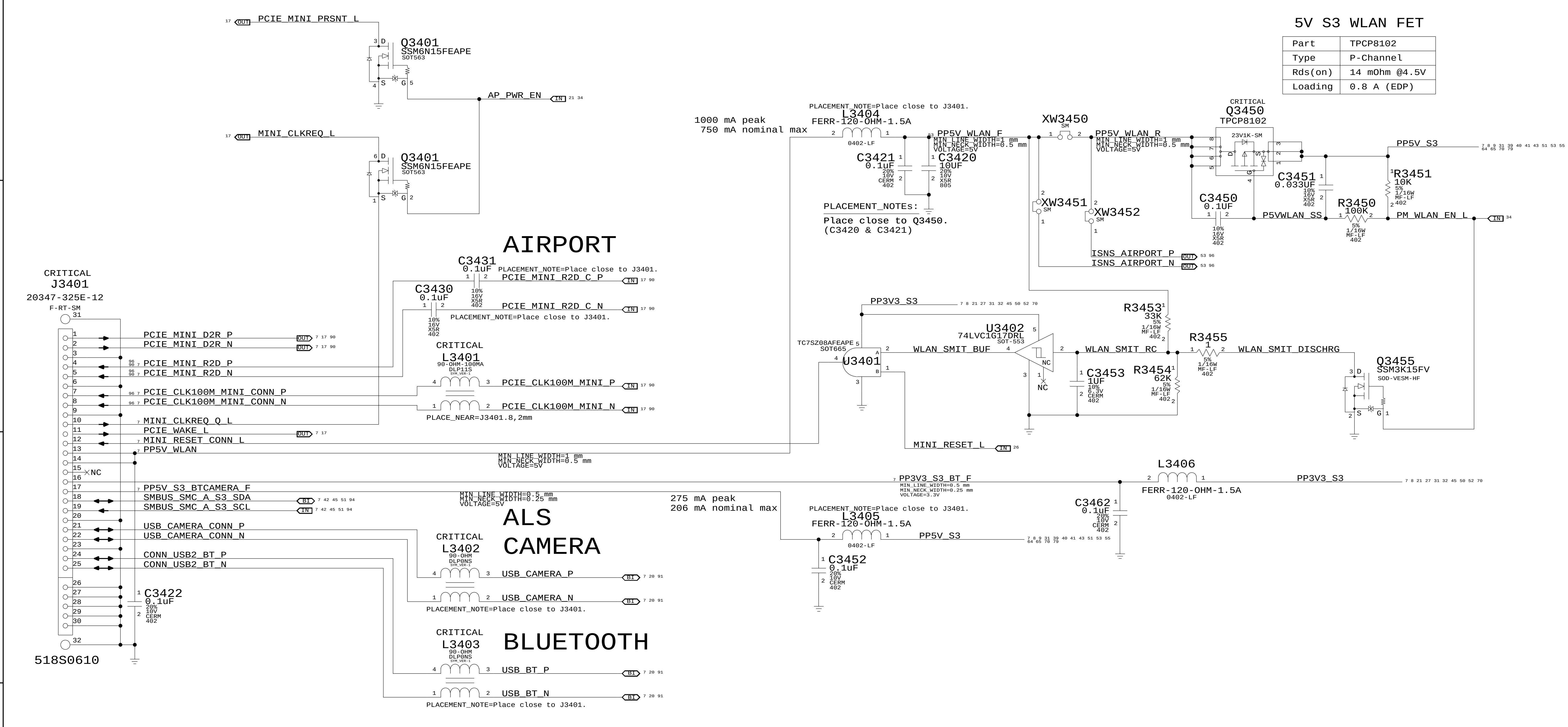


DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 30 OF 97	


AIRPORT
ALS
CAMERA
BLUETOOTH
CRITICAL
J3401
20347-325E-12
F-RT-SM
518S0610
Q3401
SSM6N15FEAPE
SOT563
PCIE_MINI_PRSNT_L
MINI_CLKREQ_L
AP_PWR_EN
C3431
0.1uF
C3430
0.1uF
PLACEMENT_NOTE=Place close to J3401.
PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_C_N
PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_Q_L
PCIE_WAKE_L
MINI_RESET_CONN_L
PP5V_WLAN
PP5V_S3_BTCAMERA_F
SMBUS_SMC_A_S3_SDA
SMBUS_SMC_A_S3_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
CONN_USB2_BT_P
CONN_USB2_BT_N
L3401
90-OHM-100MA
DLP11S
PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N
PLACE_NEAR=J3401.8,2mm
L3402
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
L3403
90-OHM
DLP0NS
USB_BT_P
USB_BT_N
C3422
0.1uF
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
1000 mA peak
750 mA nominal max
L3404
FERR-120-OHM-1.5A
0402-LF
C3421
0.1uF
C3420
10UF
PP5V_WLAN_F
PLACEMENT_NOTES:
Place close to Q3450.
(C3420 & C3421)
XW3450
XW3451
XW3452
PP5V_WLAN_R
ISNS_AIRPORT_P
ISNS_AIRPORT_N
CRITICAL
Q3450
TPCP8102
C3450
0.1UF
C3451
0.033UF
R3450
100K
R3451
10K
P5VWLAN_SS
PM_WLAN_EN_L
PP5V_S3
PP3V3_S3
U3401
TC7SZ08AFEAPE
SOT665
U3402
74LVC1G17DRL
SOT-553
WLAN_SMIT_BUF
WLAN_SMIT_RC
WLAN_SMIT_DISCHRG
R3453
33K
R3454
62K
R3455
1
C3453
1UF
Q3455
SSM3K15FV
SOD-VESM-HF
MINI_RESET_L
L3406
FERR-120-OHM-1.5A
PP3V3_S3_BT_F
C3462
0.1uF
275 mA peak
206 mA nominal max
L3405
FERR-120-OHM-1.5A
C3452
0.1uF

5V S3 WLAN FET

Part	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
Loading	0.8 A (EDP)

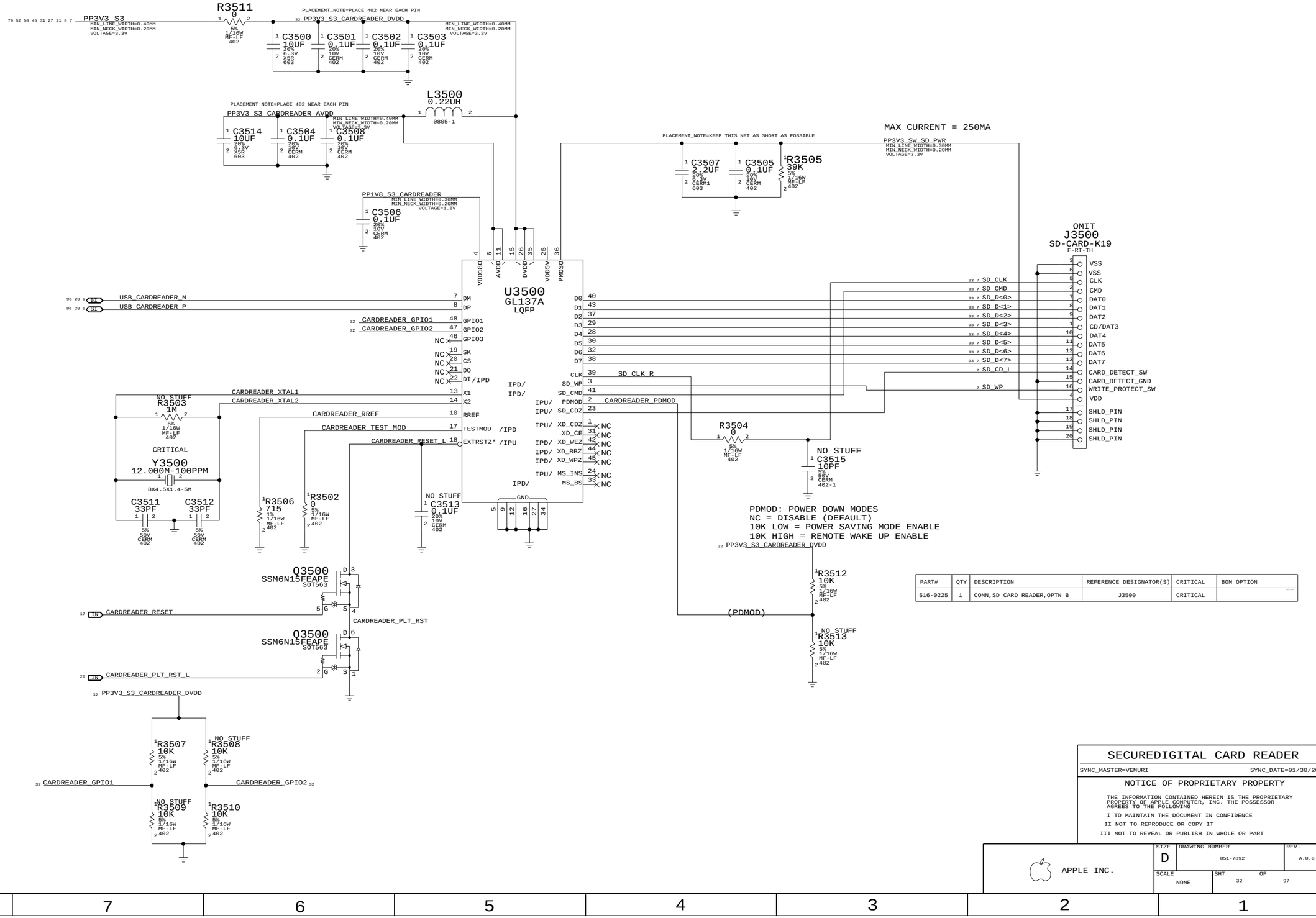
Right Clutch Connector

SYNC_MASTER=MUXGFX SYNC_DATE=12/08/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE NONE	SHT 31	OF 97



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B	J3500	CRITICAL	

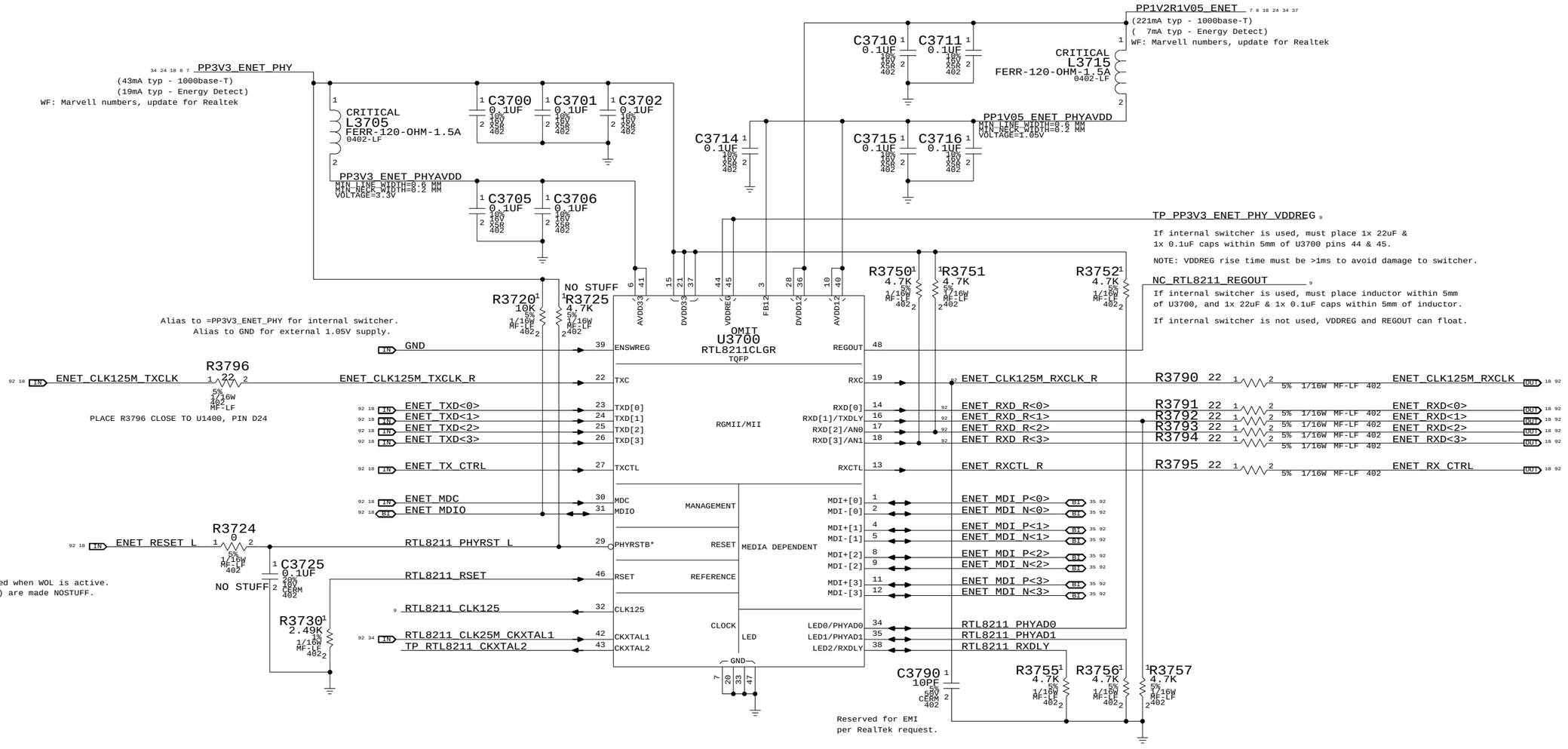
SECUREDIGITAL CARD READER

SYNC_MASTER=VEMURI SYNC_DATE=01/30/2009

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 32 OF 97	


PP3V3_ENET_PHY
(43mA typ - 1000base-T)
(19mA typ - Energy Detect)
WF: Marvell numbers, update for Realtek
CRITICAL
L3705
FERR-120-OHM-1.5A
0402-LF
C3700 0.1UF
C3701 0.1UF
C3702 0.1UF
PP3V3_ENET_PHYAVDD
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C3705 0.1UF
C3706 0.1UF
PP1V2R1V05_ENET
(221mA typ - 1000base-T)
(7mA typ - Energy Detect)
WF: Marvell numbers, update for Realtek
C3710 0.1UF
C3711 0.1UF
CRITICAL
L3715
FERR-120-OHM-1.5A
0402-LF
PP1V05_ENET_PHYAVDD
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
C3714 0.1UF
C3715 0.1UF
C3716 0.1UF
TP_PP3V3_ENET_PHY_VDDREG
If internal switcher is used, must place 1x 22uF &
1x 0.1uF caps within 5mm of U3700 pins 44 & 45.
NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.
NC_RTL8211_REGOUT
If internal switcher is used, must place inductor within 5mm
of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.
If internal switcher is not used, VDDREG and REGOUT can float.
R3720 10K
R3725 4.7K
R3750 4.7K
R3751 4.7K
R3752 4.7K
NO STUFF
Alias to =PP3V3_ENET_PHY for internal switcher.
Alias to GND for external 1.05V supply.
OMIT
U3700
RTL8211CLGR
TQFP
AVDD33
DVDD33
VDDREG
FB12
DVDD12
AVDD12
GND
ENSWREG
REGOUT
R3796 22
PLACE R3796 CLOSE TO U1400, PIN D24
ENET_CLK125M_TXCLK
ENET_CLK125M_TXCLK_R
TXC
RXC
ENET_CLK125M_RXCLK_R
R3790 22
ENET_CLK125M_RXCLK
ENET_TXD<0>
ENET_TXD<1>
ENET_TXD<2>
ENET_TXD<3>
TXD[0]
TXD[1]
TXD[2]
TXD[3]
RGMII/MII
RXD[0]
RXD[1]/TXDLY
RXD[2]/AN0
RXD[3]/AN1
ENET_RXD_R<0>
ENET_RXD_R<1>
ENET_RXD_R<2>
ENET_RXD_R<3>
R3791 22
R3792 22
R3793 22
R3794 22
ENET_RXD<0>
ENET_RXD<1>
ENET_RXD<2>
ENET_RXD<3>
ENET_TX_CTRL
TXCTL
RXCTL
ENET_RXCTL_R
R3795 22
ENET_RX_CTRL
ENET_MDC
ENET_MDIO
MDC
MDIO
MANAGEMENT
MDI+[0]
MDI-[0]
MDI+[1]
MDI-[1]
MDI+[2]
MDI-[2]
MDI+[3]
MDI-[3]
ENET_MDI P<0>
ENET_MDI N<0>
ENET_MDI P<1>
ENET_MDI N<1>
ENET_MDI P<2>
ENET_MDI N<2>
ENET_MDI P<3>
ENET_MDI N<3>
ENET_RESET_L
R3724 0
C3725 0.1UF
NO STUFF
RTL8211_PHYRST_L
PHYRSTB*
RESET
MEDIA DEPENDENT
RTL8211_RSET
RSET
REFERENCE
R3730 2.49K
RTL8211_CLK125
CLK125
RTL8211_CLK25M_CKXTAL1
TP_RTL8211_CKXTAL2
CKXTAL1
CKXTAL2
CLOCK
LED
LED0/PHYAD0
LED1/PHYAD1
LED2/RXDLY
RTL8211_PHYAD0
RTL8211_PHYAD1
RTL8211_RXDLY
C3790 10PF
R3755 4.7K
R3756 4.7K
R3757 4.7K
Reserved for EMI
per RealTek request.
ENET_RESET_L is not asserted when WOL is active.
Hence, RC (R3725 and C3725) are made NOSTUFF.
Configuration Settings:
PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)
Ethernet PHY (RTL8211CL)
SYNC_MASTER=SUMA_M98_MLB
SYNC_DATE=07/01/2008
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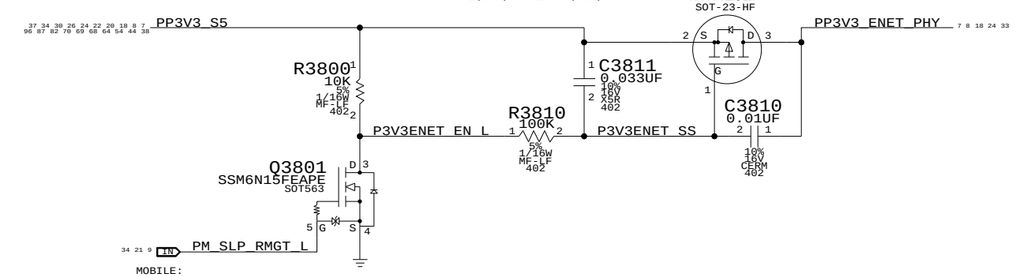
APPLE INC.
SIZE D
DRAWING NUMBER 051-7892
REV. A.0.0
SCALE NONE
SHT 33 OF 97

3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL
Q3810
NTR4101P
SOT-23-HF



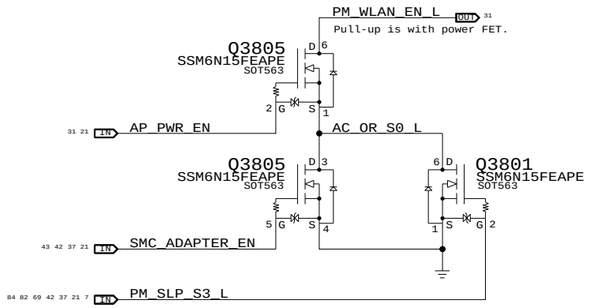
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

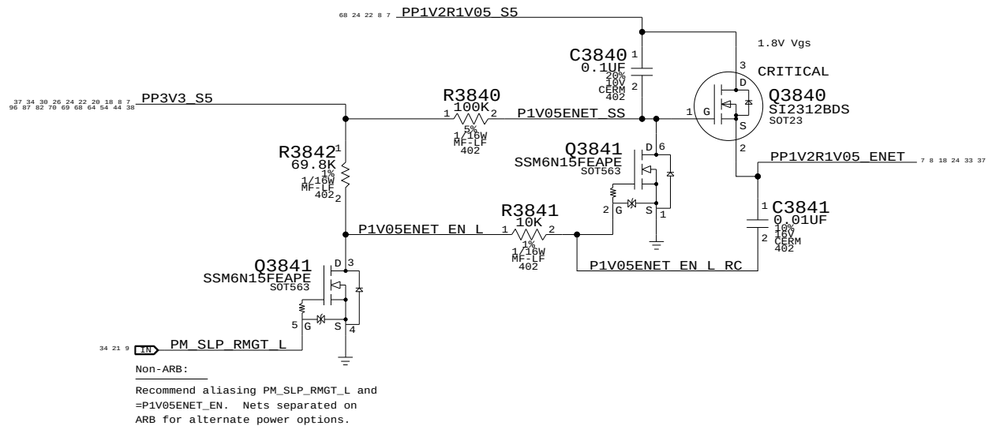
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET

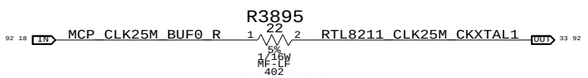


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

APPLE INC.

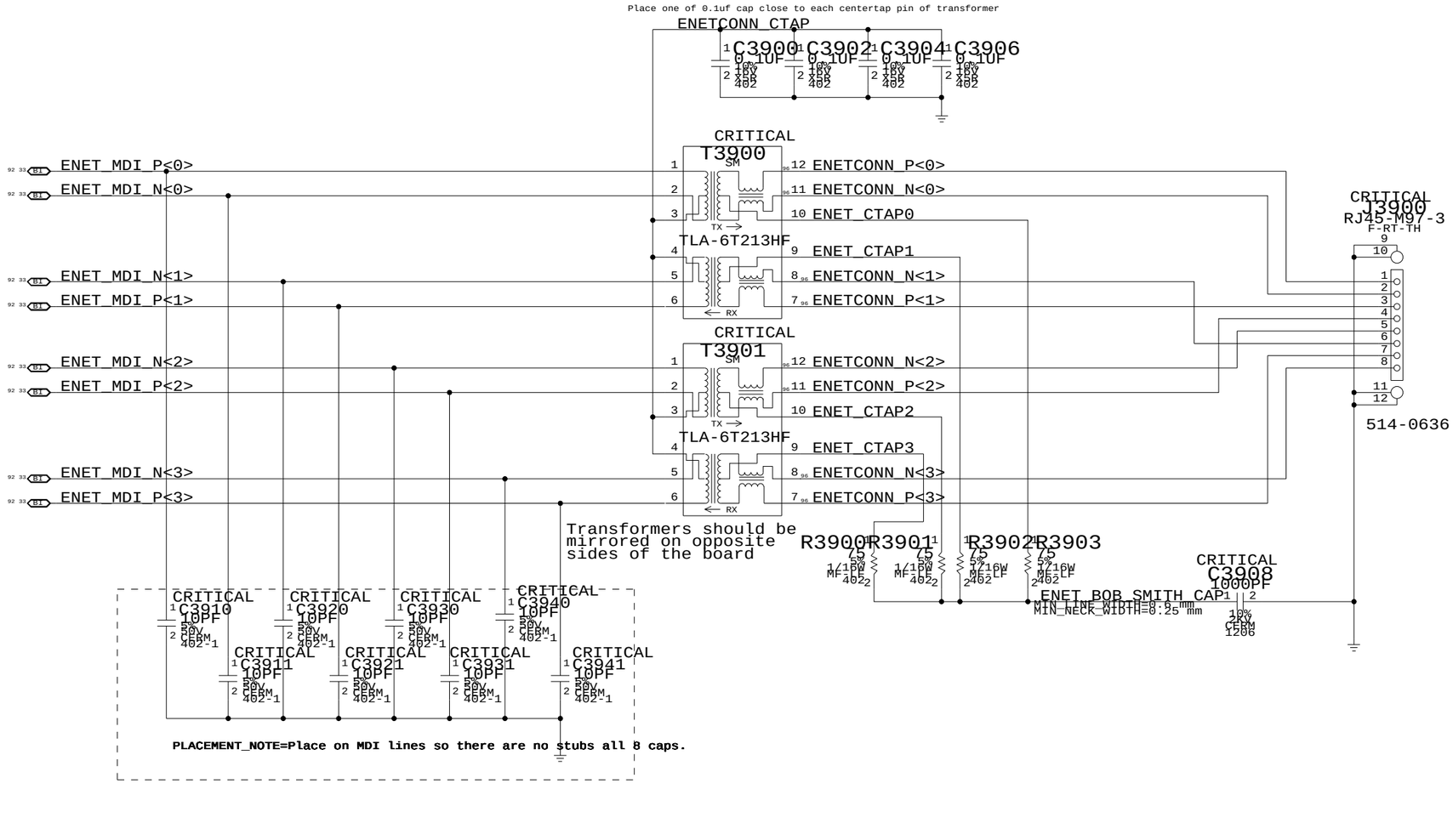
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 34 OF 97	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Ethernet Connector

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=12/16/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 35 OF 97	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0557	1	RES,0.475 ohm,1%,1/16W,0402	R4100	CRITICAL	

PP1V0_FW 135 mA

OMIT R4100 0.2 1% 1/10W MF-LF 402

PP1V0_FW_R MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.0V

L4110 120-OHM-0.3A-EMI 0402-LF

PP1V0_FW_FWPHY_AVDD MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.0V

25 mA PCIe SerDes

C4110 1UF 10% 6.3V CERM 402

C4111 1UF 10% 6.3V CERM 402

110 mA Digital Core

C4100 1UF 10% 6.3V CERM 402

C4101 1UF 10% 6.3V CERM 402

C4102 1UF 10% 6.3V CERM 402

C4103 1UF 10% 6.3V CERM 402

C4104 1UF 10% 6.3V CERM 402

C4105 1UF 10% 6.3V CERM 402

C4106 1UF 10% 6.3V CERM 402

7 mA I/O

C4120 1UF 10% 6.3V CERM 402

C4121 1UF 10% 6.3V CERM 402

C4122 1UF 10% 6.3V CERM 402

C4123 1UF 10% 6.3V CERM 402

C4124 1UF 10% 6.3V CERM 402

PP3V3_FW_FWPHY 8 36 37 38

138 mA

L4130 120-OHM-0.3A-EMI

114 mA FireWire PHY

PP3V3_FW_FWPHY_VDDA MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V 0402-LF

C4130 1UF 10% 6.3V CERM 402

C4131 1UF 10% 6.3V CERM 402

C4132 1UF 10% 6.3V CERM 402

L4135 120-OHM-0.3A-EMI

17 mA PCIe SerDes

PP3V3_FW_FWPHY_VP25 MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V 0402-LF

C4135 1UF 10% 6.3V CERM 402

C4136 1UF 10% 6.3V CERM 402

0 mA VReg PWR

C4141 0.1UF 20% 10V CERM 402

C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

OMIT CRITICAL U4100 FW643 BGA

PCI EXPRESS PHY

TEST CONTROLLER

1394 PHY

POWER MANAGEMENT

SCIF

SERIAL EEPROM CONTROLLER

MISCELLANEOUS

CHIP RESET

NOTE: NT-xx notes show NAND tree order.

NC	B13	ATBUSB	
NC	A13	ATBUSH	
NC	A11	ATBUSN	
FWPHY_DS0	F12	DS0 (IPD) NT-19	
FWPHY_DS1	E12	DS1 (IPD) NT-20	
FWPHY_DS2	E13	DS2 (IPD) NT-21	
NC_FW0_TPAN	B8	TPA0N	
NC_FW0_TPAP	A8	TPA0P	
FW_PORT1_TPA_N	B5	TPA1N	
FW_PORT1_TPA_P	A5	TPA1P	
NC_FW2_TPAN	B3	TPA2N	
NC_FW2_TPAP	A3	TPA2P	
NC_FW0_TPBN	B9	TPB0N	
NC_FW0_TPBP	A9	TPB0P	
FW_PORT1_TPB_N	B6	TPB1N	
FW_PORT1_TPB_P	A6	TPB1P	
NC_FW2_TPBN	B4	TPB2N	
NC_FW2_TPBP	A4	TPB2P	
NC_FW0_TPBIAS	B7	TPBIAS0	
FW_P1_TPBIAS	C3	TPBIAS1	
NC_FW2_TPBIAS	A2	TPBIAS2	
FW643_R0	B11	R0	
FW643_TPCPS	B10	TPCPS	
TP_FW643_NAND_TREE	K1	NAND_TREE NT-OUT	
FW643_REXT	L8	REXT	
FW_CLK24P576M_XO_R	F13	XO	
FW_CLK24P576M_XI	G13	XI NT-9	
TP_FW643_SE	M13	SE (IPD)	
TP_FW643_SM	N13	SM (IPD)	
TP_FW643_MODE_A	J2	MODE_A (IPD) NT-18	
TP_FW643_CE	L13	CE (IPD)	
TP_FW643_FW620_L	D12	FW620* (IPU)	
TP_FW643_JASI_EN	D1	JASI_EN (IPD) NT-11	
TP_FW643_AVREG	A10	AVREG	
TP_FW643_VBUF	H13	VBUF	
FW643_PU_RST_L	K13	FW_RESET* (IPU) NT-8	
TP_FW643_OCR10_CTL	J12	OCR_CTL_V10	
NC	J13	OCR_CTL_V12 (Reserved)	

PCIE_RXD0N	N8	PCIE_FW_R2D_N	
PCIE_RXD0P	N7	PCIE_FW_R2D_P	
PCIE_TXD0N	N5	PCIE_FW_D2R_C_N	
PCIE_TXD0P	N6	PCIE_FW_D2R_C_P	
REFCLKN	N9	PCIE_CLK100M_FW_N	
REFCLKP	N10	PCIE_CLK100M_FW_P	
NT-4 (IPU) TCK	M4	TP_FW643_TCK	
NT-3 (IPU) TDI	N2	TP_FW643_TDI	
(IPU) TDO	M1	TP_FW643_TDO	
NT-1 (IPU) TMS	M3	TP_FW643_TMS	
NT-2 (IPU) TRST*	N1	FW643_TRST_L	
NT-10 (IPD) WAKE*	C2	FW643_WAKE_L	OUT
REGCLT	D13	FW643_REGCTL	
VAUX_DETECT	E1	FW643_VAUX_DETECT	
VAUX_DISABLE	D2	TP_FW643_VAUX_ENABLE	
(OD) CLKREQN	L2	FW_CLKREQ_PHY_L	OUT
NT-16 (IPD) SCIFCLK	G2	TP_FW643_SCIFCLK	
NT-14 (IPD) SCIFDAIN	G1	TP_FW643_SCIFDAIN	
NT-17 SCIFDOUT	H1	TP_FW643_SCIFDOUT	
NT-15 (IPD) SCIFMC	F2	TP_FW643_SCIFMC	
NT-7 SCL	N12	FW643_SCL	
NT-6 SDA	M11	TP_FW643_SDA	
NT-5 PERST*	N4	FW_RESET_L	IN

FIXME!!! - TYPO IN SYMBOL REGCTL

PPVP_FW_CPS

R4160 200K 1% 1/16W MF-LF 402

C4150 22PF 5% 50V CERM 402

C4151 22PF 5% 50V CERM 402

FW_CLK24P576M_XO CRITICAL Y4150 24.576MHZ SM-3.2X2.5MM

R4150 412 1% 1/16W MF-LF 402

R4161 2.94K 1% 1/16W MF-LF 402

R4170 191 1% 1/16W MF-LF 402

R4162 470K 5% 1/16W MF-LF 402

C4162 0.33UF 10% 6.3V CERM-X5R 402

C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N

C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P

C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N

C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P

PLACEMENT_NOTE=Place C4170 close to U1400
PLACEMENT_NOTE=Place C4171 close to U1400
PLACEMENT_NOTE=Place C4175 close to U4000
PLACEMENT_NOTE=Place C4176 close to U4000

PP3V3_FW_FWPHY 8 36 37 38

FW643_LDO

R4165 10K 5% 1/16W MF-LF 402

R4166 10K 5% 1/16W MF-LF 402

R4164 10K 5% 1/16W MF-LF 402

R4163 10K 5% 1/16W MF-LF 402

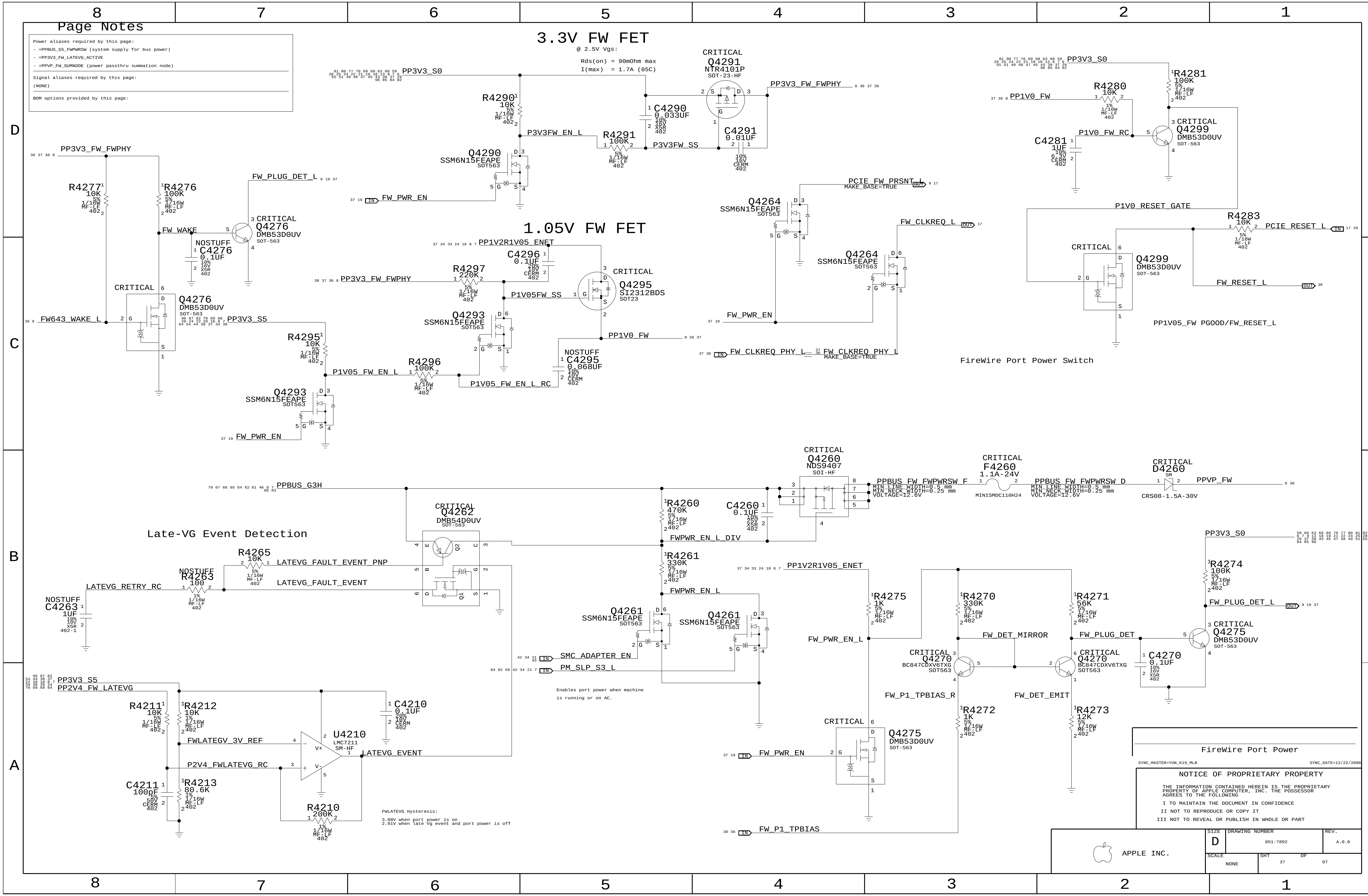
VSS VREG_VSS

FireWire LLC/PHY (FW643)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	4.12.0
SCALE: NONE	SHT: 36	OF: 97



Page Notes
Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
3.3V FW FET
@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)
1.05V FW FET
Late-VG Event Detection
FireWire Port Power Switch
PP1V05_FW PGOOD/FW_RESET_L
Enables port power when machine is running or on AC.
FWLATEVG Hysteresis:
3.08V when port power is on
2.91V when late Vg event and port power is off
PP3V3_S0
PP3V3_FW_FWPHY
PP1V0_FW
PPBUS_G3H
PPBUS_FW_FWPWRSW_F
PPBUS_FW_FWPWRSW_D
PPVP_FW
PP2V4_FW_LATEVG
PP1V2R1V05_ENET
FW_PLUG_DET_L
FW_PWR_EN
FW_WAKE
FW643_WAKE_L
PCIE_FW_PRSNT_L
FW_CLKREQ_L
FW_CLKREQ_PHY_L
PCIE_RESET_L
FW_RESET_L
P1V0_RESET_GATE
SMC_ADAPTER_EN
PM_SLP_S3_L
LATEVG_EVENT
LATEVG_RETRY_RC
LATEVG_FAULT_EVENT
LATEVG_FAULT_EVENT_PNP
FWPWR_EN_L_DIV
FWPWR_EN_L
FW_PWR_EN_L
FW_DET_MIRROR
FW_PLUG_DET
FW_DET_EMIT
FW_P1_TPBIAS_R
FW_P1_TPBIAS
CRITICAL
Q4291 NTR4101P SOT-23-HF
Q4295 SI2312BDS SOT23
Q4290 SSM6N15FEAPE SOT563
Q4293 SSM6N15FEAPE SOT563
Q4264 SSM6N15FEAPE SOT563
Q4261 SSM6N15FEAPE SOT563
Q4276 DMB53D0UV SOT-563
Q4299 DMB53D0UV SOT-563
Q4275 DMB53D0UV SOT-563
Q4262 DMB54D0UV SOT-563
Q4260 NDS9407 SOI-HF
Q4270 BC847CDXV6TXG SOT563
F4260 1.1A-24V MINISMDC110H24
D4260 CRS08-1.5A-30V
U4210 LMC7211 SM-HF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
NOSTUFF
FireWire Port Power
SYNC_MASTER=YUN_K19_MLB
SYNC_DATE=12/22/2008
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SIZE D
DRAWING NUMBER 051-7892
REV. A.0.0
SCALE NONE
SHT 37 OF 97

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain
the necessary aliases to map the
FireWire TPA/TPB pairs to their
appropriate connectors and/or to
properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT
constrained on this page. It is
assumed that FireWire PHY page will
provide the appropriate constraints
to apply to entire TPA/TPB XNets.

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

38 37 36 8 PP3V3_FW_FWPHY

R4382 10K 1% 1/10W MF-LF 402

R4380 10K 1% 1/10W MF-LF 402

38 36 FWPHY_DS0 — FWPHY_DS0 36 38 MAKE_BASE=TRUE

38 36 FWPHY_DS2 — FWPHY_DS2 36 38 MAKE_BASE=TRUE

38 36 FWPHY_DS1 — FWPHY_DS1 36 38 MAKE_BASE=TRUE

R4381 10K 1% 1/10W MF-LF 402

38 36 NC_FW0_TPBIAS — NC_FW0_TPBIAS MAKE_BASE=TRUE 36 38

38 36 NC_FW2_TPBIAS — NC_FW2_TPBIAS MAKE_BASE=TRUE 36 38

93 38 36 NC_FW0_TPAN — NC_FW0_TPAN MAKE_BASE=TRUE 36 38 93

93 38 36 NC_FW0_TPAP — NC_FW0_TPAP MAKE_BASE=TRUE 36 38 93

38 36 NC_FW2_TPAN — NC_FW2_TPAN MAKE_BASE=TRUE 36 38

38 36 NC_FW2_TPAP — NC_FW2_TPAP MAKE_BASE=TRUE 36 38

93 38 36 NC_FW0_TPBN — NC_FW0_TPBN MAKE_BASE=TRUE 36 38 93

93 38 36 NC_FW0_TPBP — NC_FW0_TPBP MAKE_BASE=TRUE 36 38 93

38 36 NC_FW2_TPBN — NC_FW2_TPBN MAKE_BASE=TRUE 36 38

38 36 NC_FW2_TPBP — NC_FW2_TPBP MAKE_BASE=TRUE 36 38

Termination

Place close to FireWire PHY

37 36 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

93 38 36 FW_PORT1_TPA_P — FW_PORT1_TPA_P 36 38 93 MAKE_BASE=TRUE

93 38 36 FW_PORT1_TPA_N — FW_PORT1_TPA_N 36 38 93 MAKE_BASE=TRUE

93 38 36 FW_PORT1_TPB_P — FW_PORT1_TPB_P 36 38 93 MAKE_BASE=TRUE

93 38 36 FW_PORT1_TPB_N — FW_PORT1_TPB_N 36 38 93 MAKE_BASE=TRUE

SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

38 37 8 PPVP_FW

R4311 470K 5% 1/10W MF-LF 402

Q4300 BSS8402DW SOT-363 (SYM-VER1)

38 36 PPVP_FW_CPS MAKE_BASE=TRUE — PPVP_FW_CPS 36 38

MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

CPS_EN_L_DIV

R4312 330K 5% 1/10W MF-LF 402

CPS_EN_L

38 37 36 8 PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

"Snapback" & "Late VG" Protection

38 37 PP2V4_FW_LATEVG

C4311 0.01uF 10% 50V X7R 402

C4310 0.01uF 10% 50V X7R 402

C4312 0.01uF 10% 50V X7R 402

C4313 0.01uF 10% 50V X7R 402

CRITICAL DP4310 BAV99DW-X-G SOT-363

CRITICAL DP4311 BAV99DW-X-G SOT-363

93 38 36 FW_PORT1_TPB_N

93 38 36 FW_PORT1_TPB_P

93 38 36 FW_PORT1_TPA_N

93 38 36 FW_PORT1_TPA_P

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

(GND_FW_PORT1_VG)

FW_PORT1_AREF

(FW_PORT1_BREF)

Cable Power

38 37 8 PPVP_FW

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

1	TPB-	TPB(R) TPB-	OUTPUT
9		TPB<R>	
2	TPB+	TPB+ VP	
8		VP	
7	NC	VBC/NC	
6		VG	
3	TPA-	TPA- VG	INPUT
5		TPA<R>	
4	TPA+	TPA(R) TPA+	
10			
11	CHASSIS GND		
12			
13			

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

Late-VG Protection Power

37 34 30 26 24 22 20 18 8 | 98 87 82 76 69 68 61 54 44

PP3V3_S5

R4390 332 1% 1/16W MF-LF 402

PP2V4_FW_LATEVG 37 38

MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.4V

CRITICAL D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

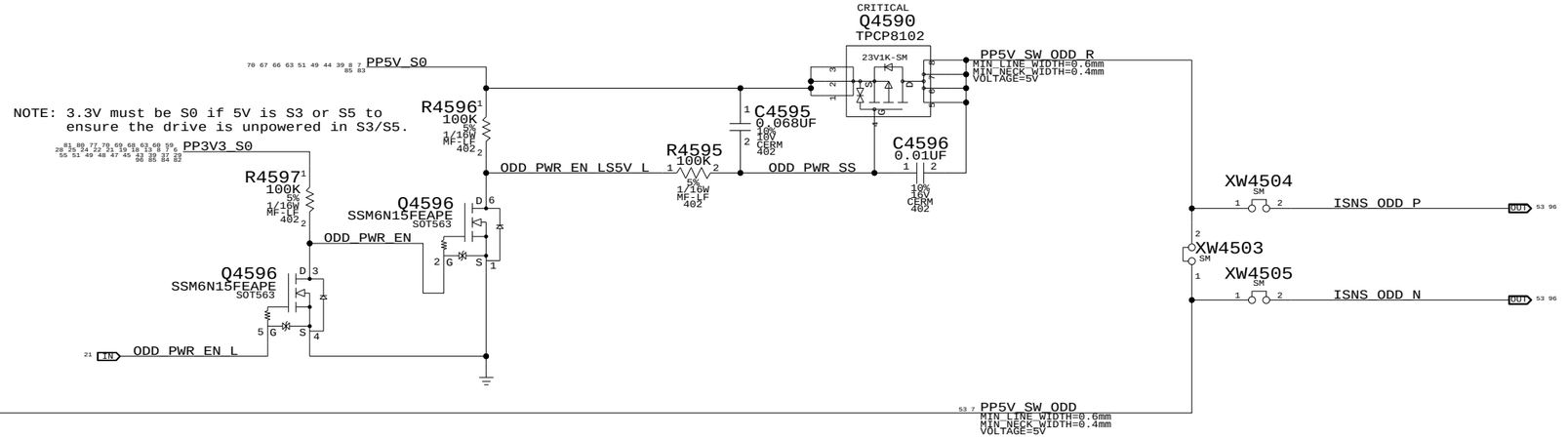
FireWire Ports

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

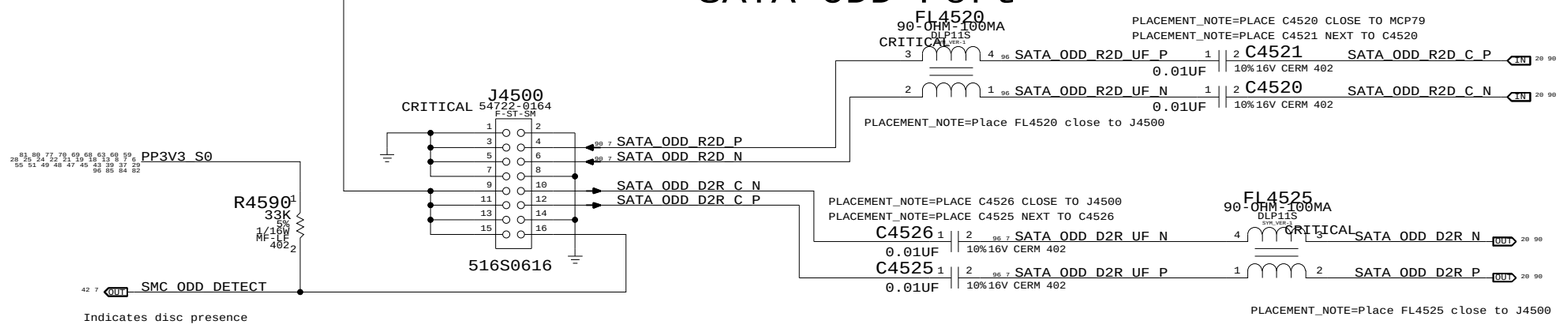
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 38 OF 97	

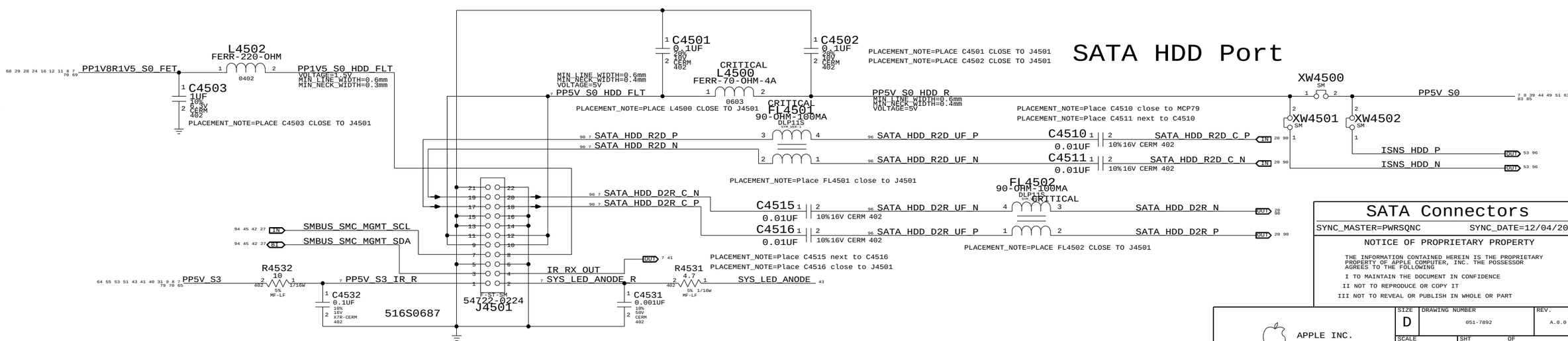
ODD Power Control



SATA ODD Port



SATA HDD Port



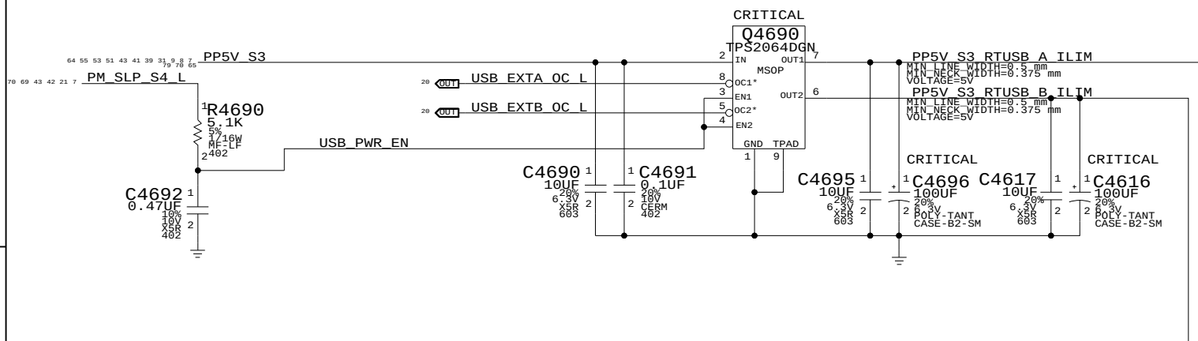
SATA Connectors

SYNC_MASTER=PWRSQNC SYNC_DATE=12/04/2008

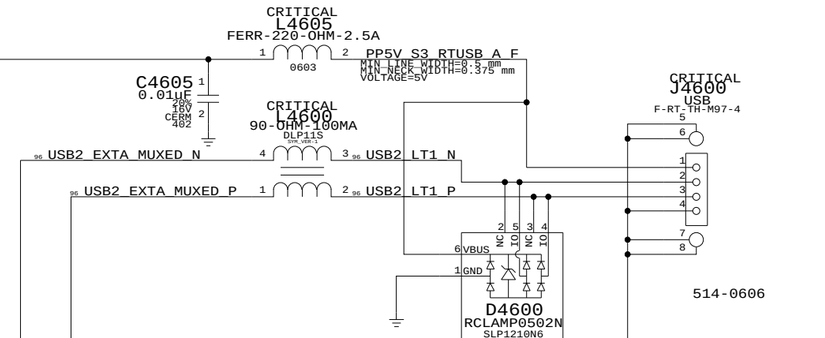
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 39 OF 97	

Port Power Switch



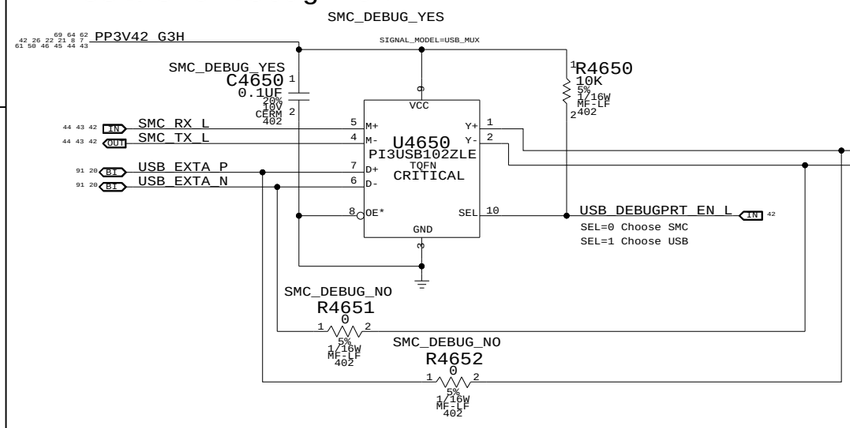
Left USB Port A



We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin

USB/SMC Debug Mux



Left USB Port B

External USB Connectors		
SYNC_MASTER=M98_MLB	SYNC_DATE=11/14/2008	

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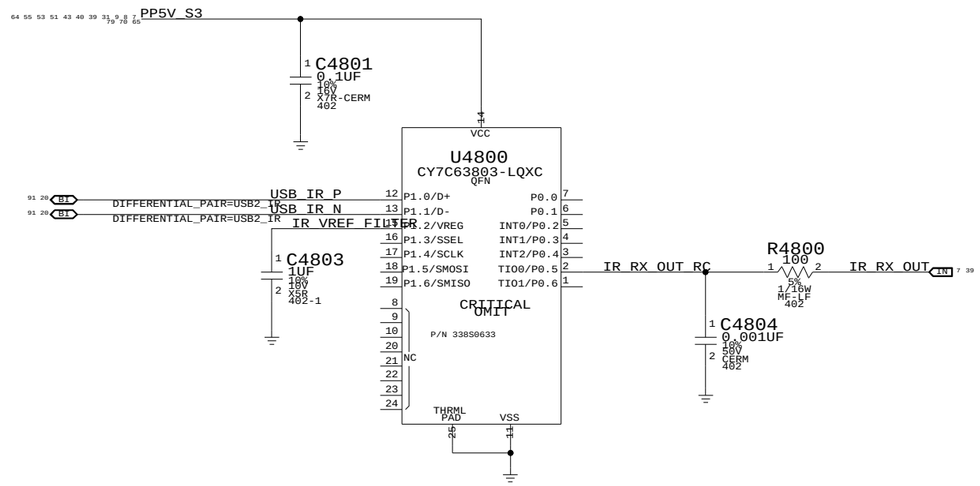
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
	SCALE: NONE	SHT 40 OF 97	

IR SUPPORT



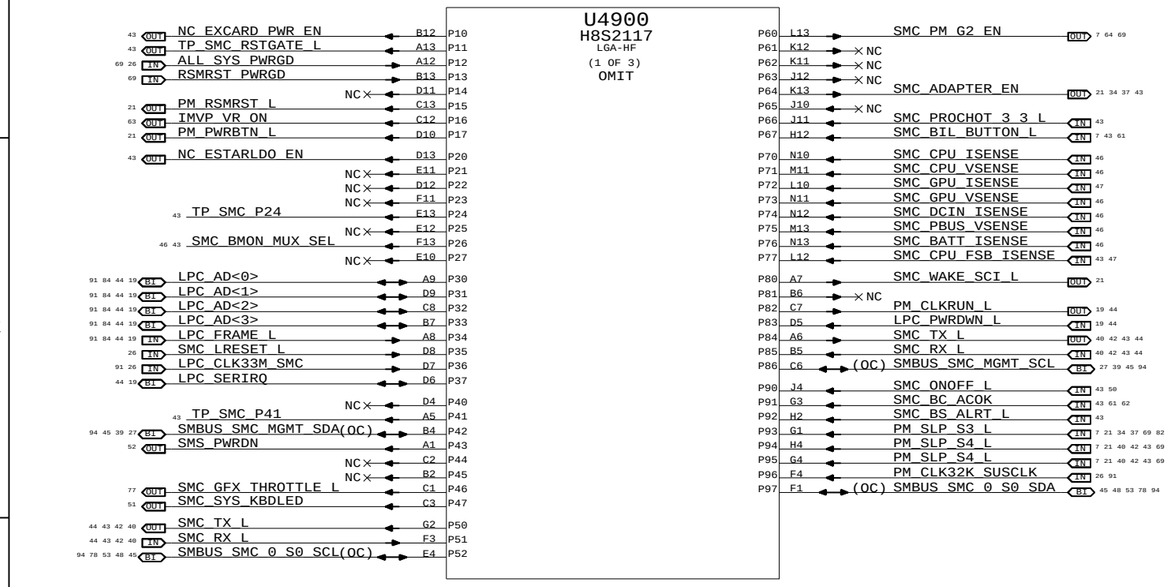
Front Flex Support

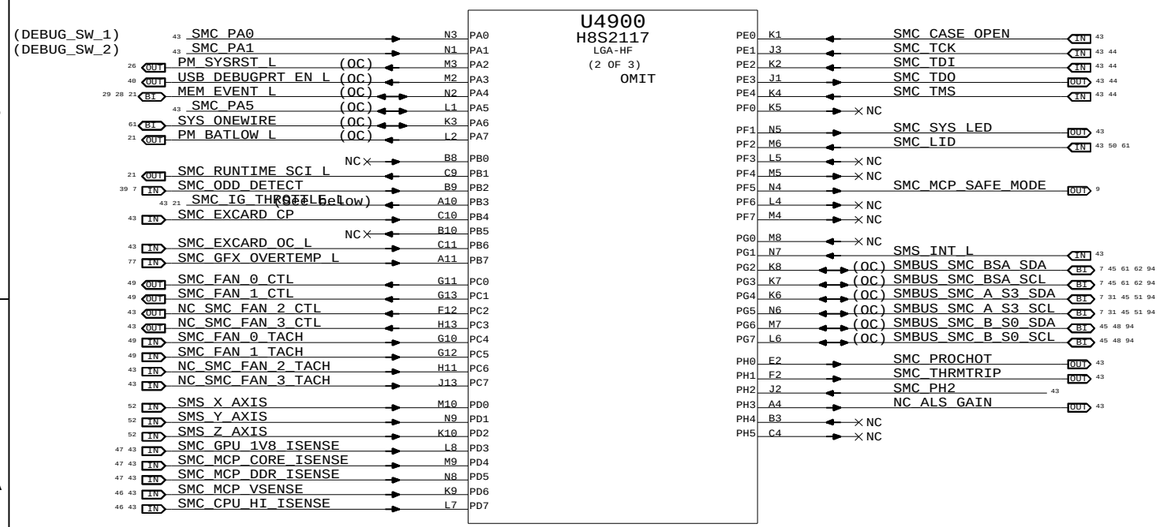
SYNC_MASTER=PWRSQNC SYNC_DATE=12/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 41 OF 97	

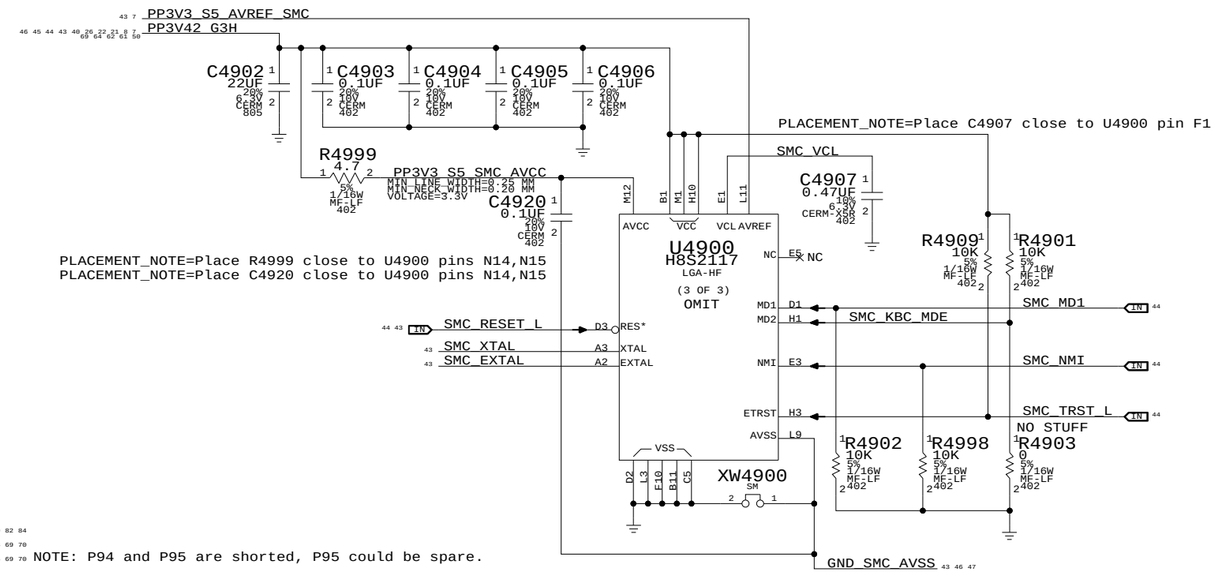
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

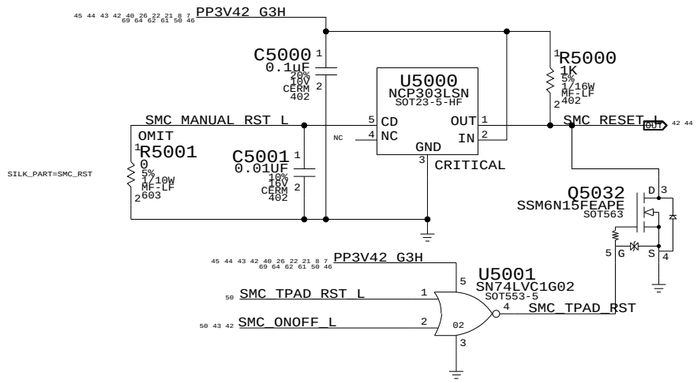
SMC

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

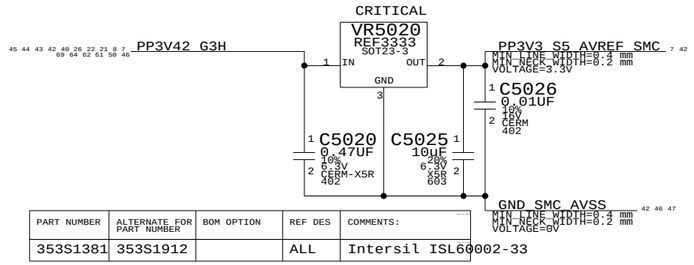
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 42 OF 97	

SMC Reset "Button" / Brownout Detect

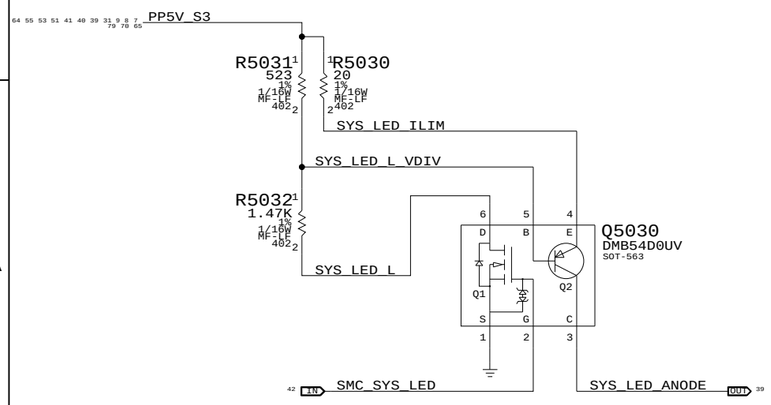


SMC AVREF Supply

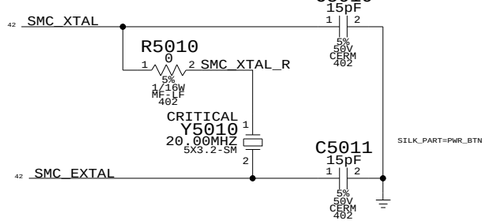


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

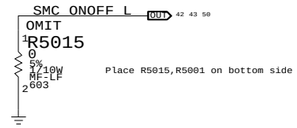
System (Sleep) LED Circuit

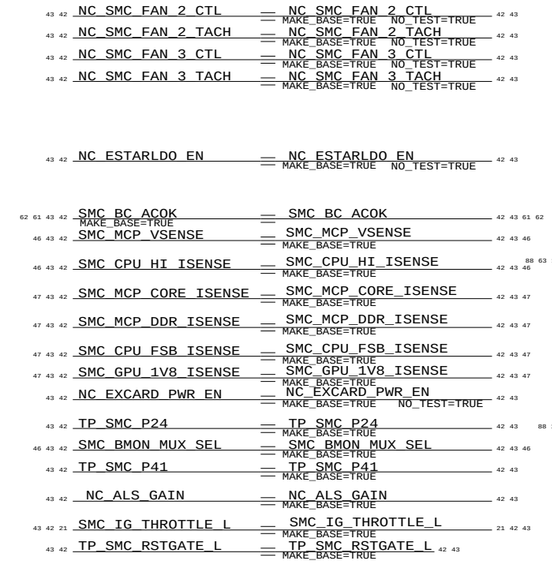


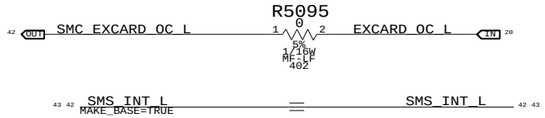
SMC Crystal Circuit



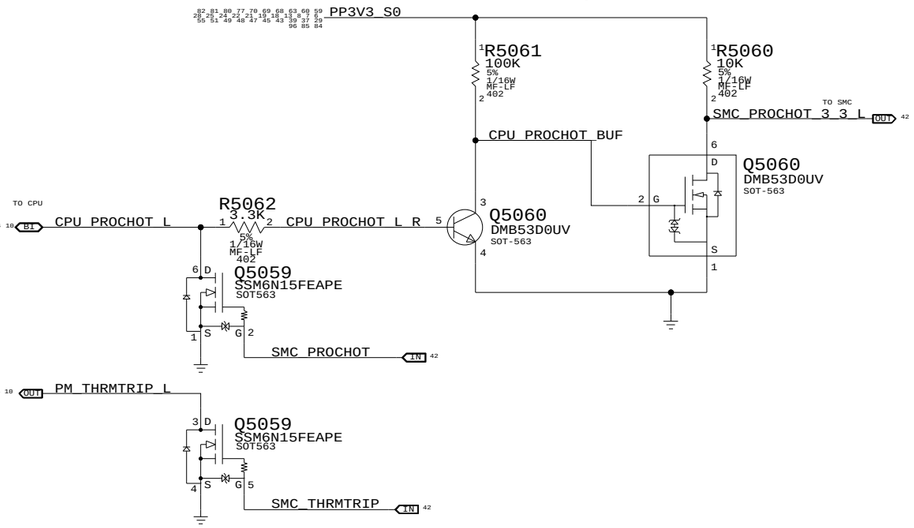
Debug Power "Button"

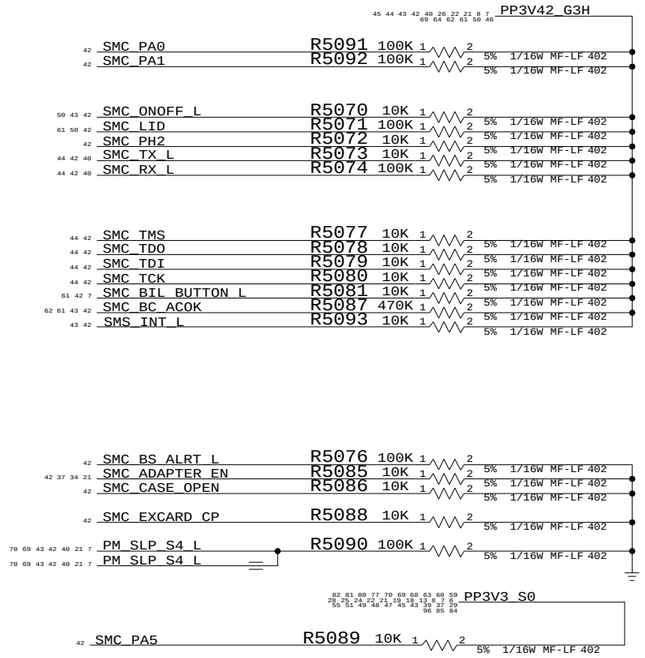






SMC FSB to 3.3V Level Shifting





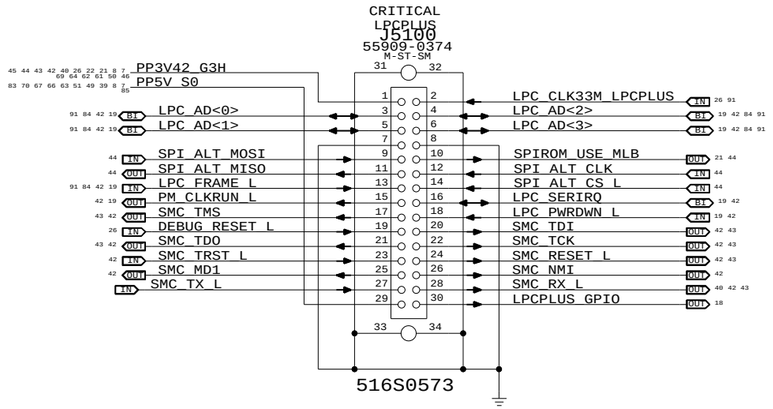
SMC Support

SYNC_MASTER=DDR SYNC_DATE=12/19/2008

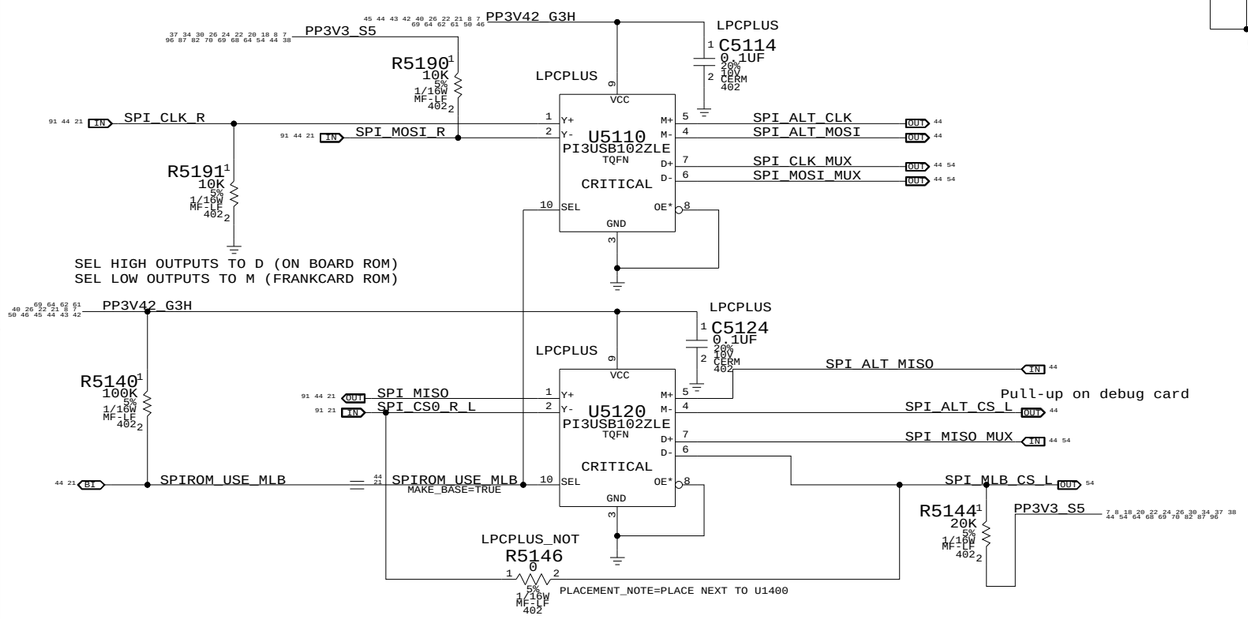
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 43 OF 97	

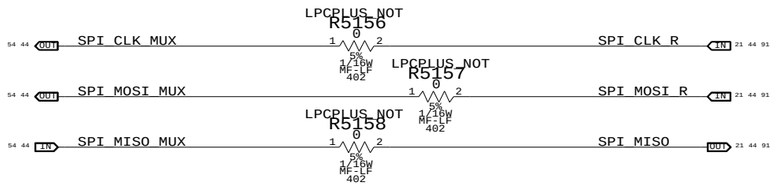
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



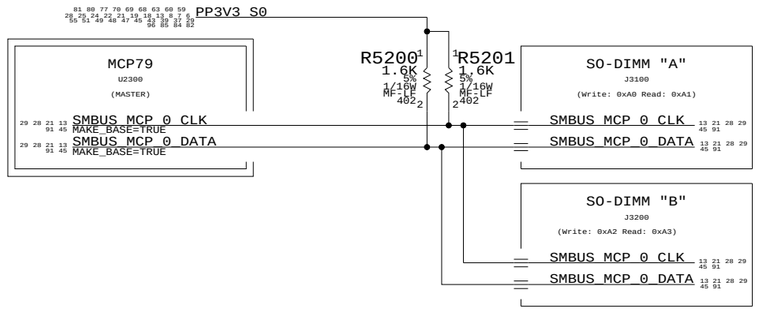
LPC+SPI Debug Connector

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

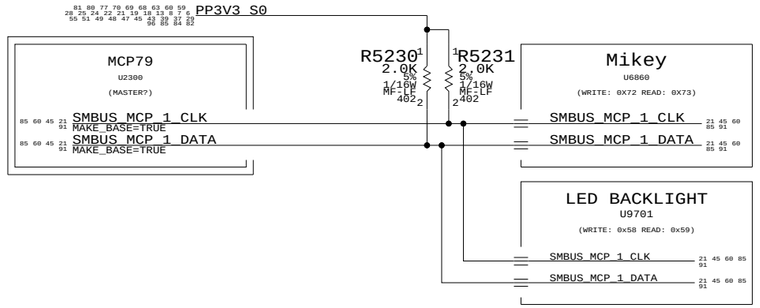
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 44 OF 97	

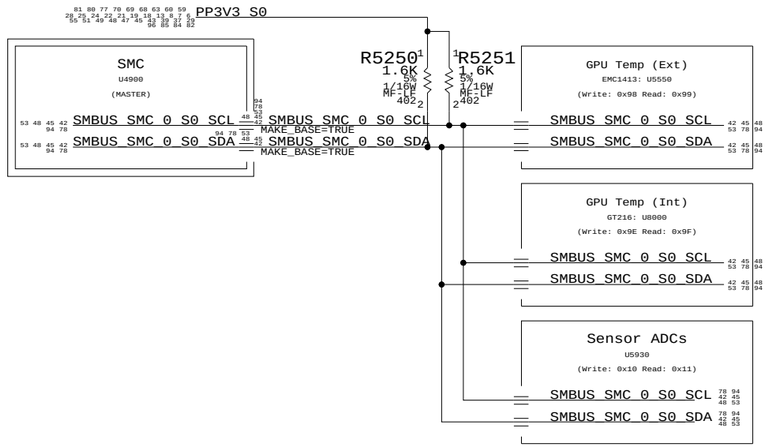
MCP79 SMBus "0" Connections



MCP79 SMBus "1" Connections

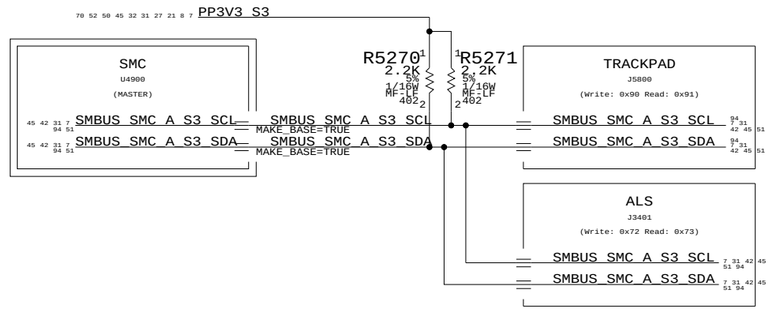


SMC "0" SMBus Connections

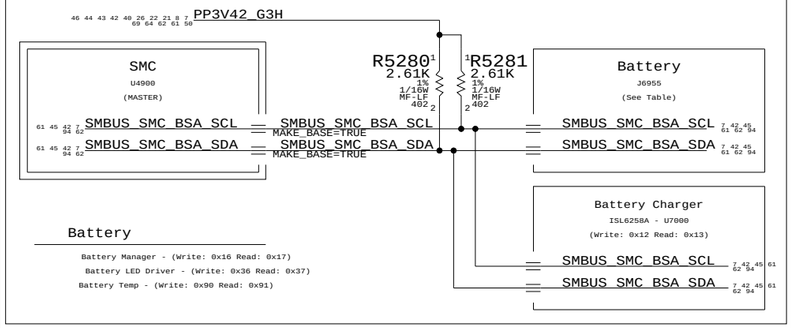


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



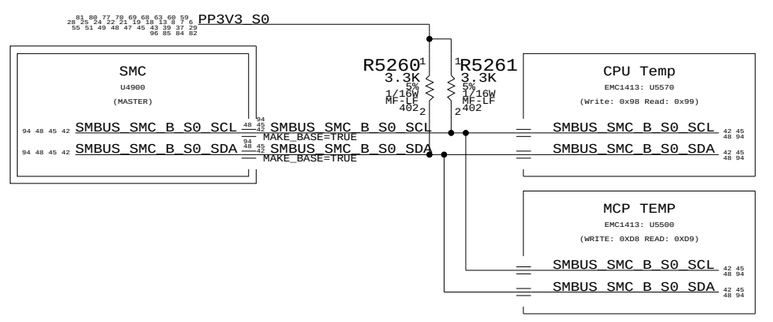
SMC "Battery A" SMBus Connections



Battery

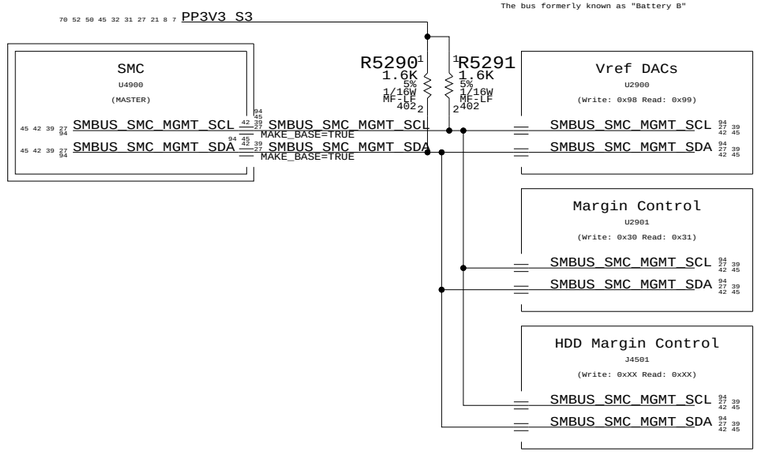
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "B" SMBus Connections



SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



K19 SMBUS CONNECTIONS

SYNC_MASTER=DDR SYNC_DATE=12/19/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 45 OF 97	

CPU Voltage Sense / Filter

63 12 11 8 7 PPVCORE_S0_CPU — XW5309 SM 1 2 — CPUVSENSE_IN — R5309 4.53K 1% 1/10W MF-LF 402 1 2 — SMC_CPU_VSENSE OUT 42

Place short near U1000 center

C5309 0.22UF 20% 6.3V X5R 402 (1 2 GND_SMC_AVSS 42 43 46 47)

Place RC close to SMC

GPU Voltage Sense / Filter

79 72 8 PPVCORE_GPU — XW5359 SM 1 2 — GPUVSENSE_IN — R5359 4.53K 1% 1/10W MF-LF 402 1 2 — SMC_GPU_VSENSE OUT 42

Place short near U8000 center

C5359 0.22UF 20% 6.3V X5R 402 (1 2 GND_SMC_AVSS 42 43 46 47)

Place RC close to SMC

MCP Voltage Sense / Filter

66 24 22 8 7 PPVCORE_S0_MCP_REG — XW5399 SM 1 2 — MCPVSENSE_IN — R5399 4.53K 1% 1/10W MF-LF 402 1 2 — SMC_MCP_VSENSE OUT 42 43

PLACEMENT_NOTE=Place near U1400 center

C5399 0.22UF 20% 6.3V X5R 402 (1 2 GND_SMC_AVSS 42 43 46 47)

Place RC close to SMC

PBUS Voltage Sense & Filter

67 66 65 64 62 61 46 37 8 7 86 83 79 PPBUS_G3H — R5315 100K 5% 1/10W MF-LF 402 — Q5315 FDG6332CG SC70-6 P-CHN (4 S, 3 D, G, 5) — PPBUS_G3H_VSENSE — MIN_LINE_WIDTH=0.20 mm MIN_NECK_WIDTH=0.20 mm VOLTAGE=18.5V

PBUSVSENS_EN_DIV — R5316 100K 5% 1/10W MF-LF 402

PBUSVSENS_EN_L

70 69 PM_SLP_S3_L_R — Q5315 FDG6332CG SC70-6 N-CHN (2 G, 1 S, 6 D)

Enables PBUS VSense divider when high.

R5385 27.4K 1% 1/10W MF-LF 402 — Rthevanin = 4573 ohms — SMC_PBUS_VSENSE OUT 42

R5386 5.49K 1% 1/10W MF-LF 402 — C5385 0.22UF 20% 6.3V X5R 402 (GND_SMC_AVSS 42 43 46 47)

Place RC close to SMC

BMON Current Sense - Entire circuit must be near SMC (U4900)

45 44 43 42 40 26 22 21 8 7 69 64 62 61 50 46 PP3V42_G3H

BMON_ENG C5318 0.1uF 20% 10V CERM 402 (3 V+)

REGULATOR SIDE:

U5303 INA213 SC70 — 96 62 CHGR_CSO_R_P (OUT) → 5 IN- — 96 62 CHGR_CSO_R_N (IN) → 4 IN+ — OUT 6 — REF 1 — GND 2

LOAD SIDE:

Monitors battery discharge current from battery to PBUS

BMON_INA_OUT

U5313 NC7SB3157P6XG SC70 — 1 B1 — 2 GND — 3 B0 — 4 A — 5 VCC — 6 SEL — 1 / 0 — VER 1

SMC_BMON_MUX_SEL IN 42 43

62 CHGR_BMON (IN)

BMON_PROD R5330 0 5% 1/10W MF-LF 402

BMON_ENG R5371 100K 5% 1/10W MF-LF 402

BMON_AMUX_OUT — R5391 4.53K 1% 1/10W MF-LF 402 — SMC_BATT_ISENSE OUT 42

C5390 0.22UF 20% 6.3V X5R 402 (GND_SMC_AVSS 42 43 46 47)

BMON_ENG C5369 0.1uF 20% 10V CERM 402

INA213 has gain of 50V/V

DCIN Current Sense Filter

Place RC close to SMC

62 CHGR_AMON (IN) — R5380 4.53K 1% 1/10W MF-LF 402 — SMC_DCIN_ISENSE OUT 42

C5380 0.22UF 20% 6.3V X5R 402 (GND_SMC_AVSS 42 43 46 47)

CPU VCore High Side Current Sensor

69 64 62 61 50 46 45 44 43 42 40 26 22 21 8 7 PP3V42_G3H

C5388 0.1UF 20% 10V CERM 402 (3 V+)

63 8 PPBUS_CPU_IMVP_ISNS (OUT)

CRITICAL R5388 0.001 1% 0.5W MF 1206 (1 3 — 2 4)

96 ISNS_CPU_N — 96 ISNS_CPU_P

U5388 INA210 SC70 — 5 IN- — 4 IN+ — OUT 6 — REF 1 — GND 2

CPUVCORE_HISIDE_IOUT

R5335 4.53K 1% 1/10W MF-LF 402 — SMC_CPU_HI_ISENSE OUT 42 43

C5335 0.22UF 20% 6.3V X5R 402 (GND_SMC_AVSS 42 43 46 47)

Place RC close to SMC

62 61 46 37 8 7 79 67 66 65 64 PPBUS_G3H (IN)

Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

CPU VCore Load Side Current Sense / Filter

Place RC close to SMC

63 IMVP6_IMON (IN) — R5331 6.19K 1% 1/10W MF-LF 402 — SMC_CPU_ISENSE OUT 42

R5332 17.4K 1% 1/10W MF-LF 402 — C5330 0.22UF 20% 6.3V X5R 402 (GND_SMC_AVSS 42 43 46 47)

Current & Voltage Sensing

SYNC_MASTER=SENSOR — SYNC_DATE=08/14/2008

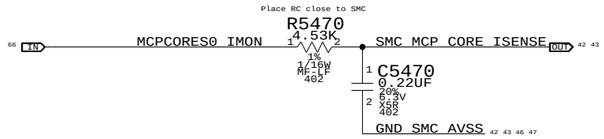
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 46 OF 97	

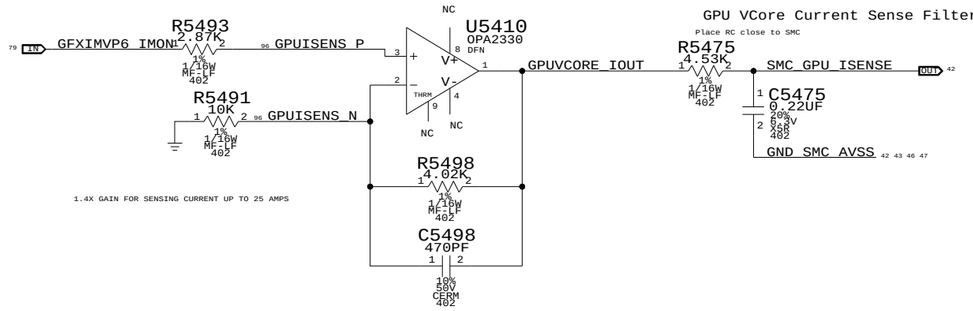
MCP VCore Current Sense

MCP VCore Current Sense Filter

Place RC close to SMC



GPU VCore Current Sense



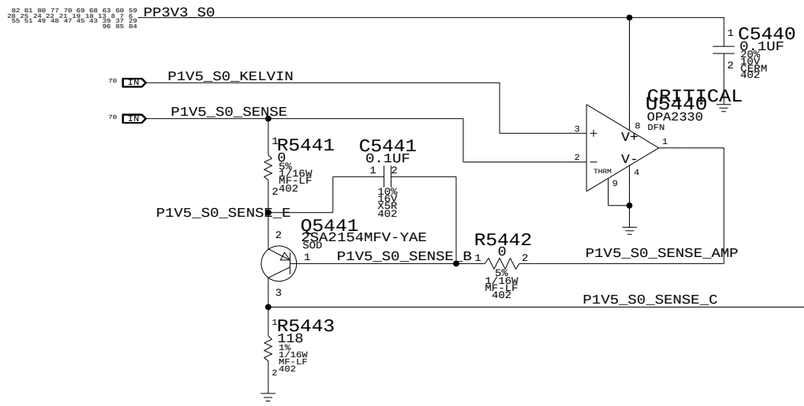
1.4X GAIN FOR SENSING CURRENT UP TO 25 AMPS

GPU VCore Current Sense Filter

Place RC close to SMC

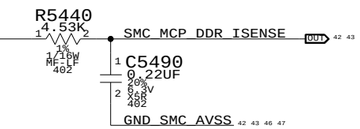
GPU VCore Current Sense and GPU 1.8V Current Sense share
dual package opamp U5410

MCP MEM VDD Current Sense

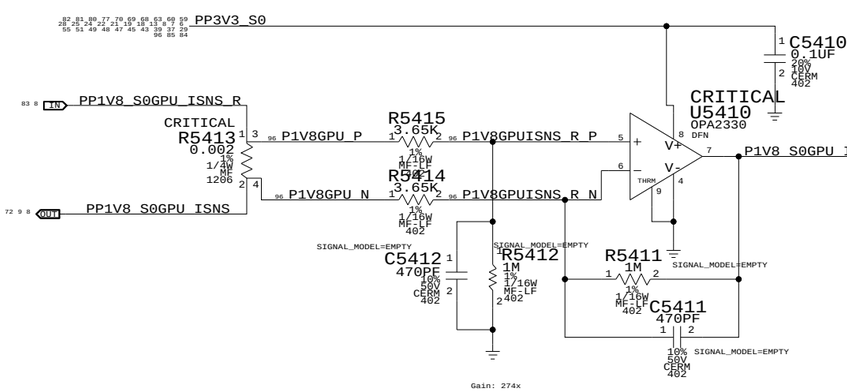


MCP MEM VDD Current Sense Filter

Place RC close to SMC



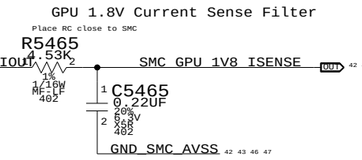
GPU 1.8V Current Sense



Gain: 274x

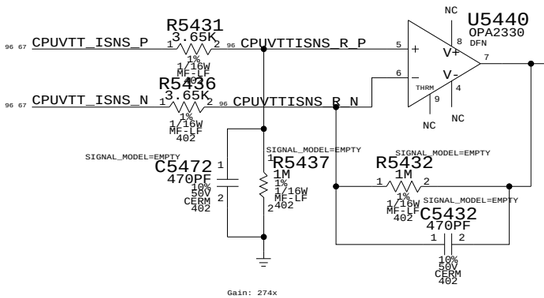
GPU 1.8V Current Sense Filter

Place RC close to SMC



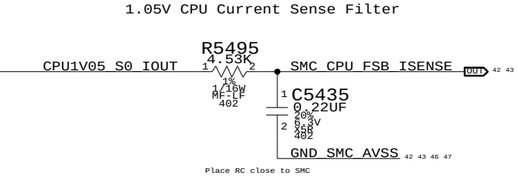
MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

CPU FSB 1.05V Current Sense



Gain: 274x

1.05V CPU Current Sense Filter



Place RC close to SMC

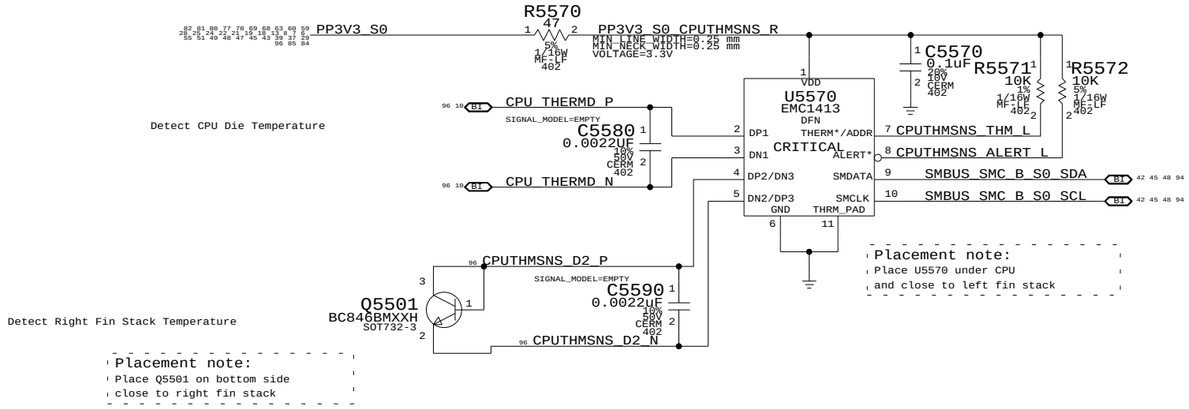
Current Sensing

SYNC_MASTER=YUN_K19_MLB SYNC_DATE=12/10/2008

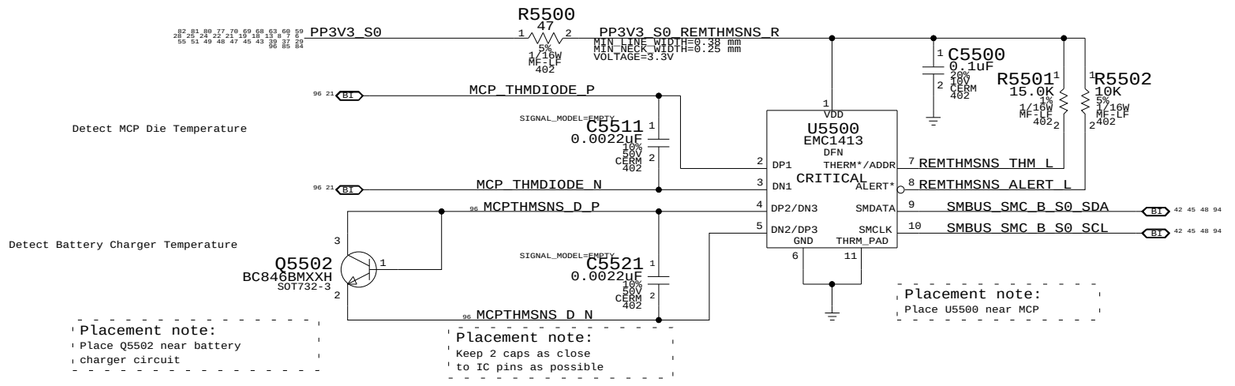
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 47 OF 97	

CPU Proximity/CPU Die/Right Fin Stack

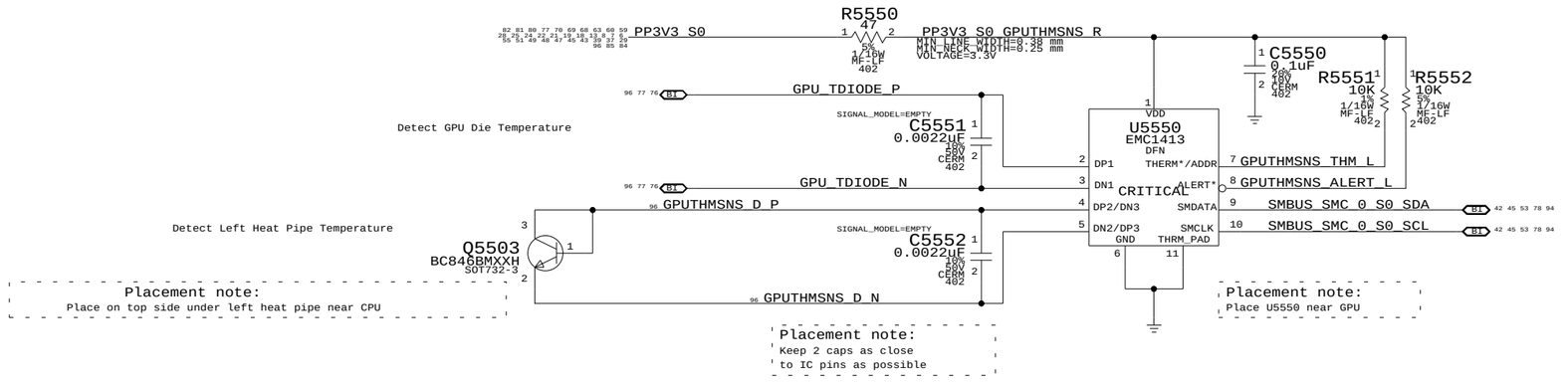


MCP Proximity/MCP Die/Battery Charger Proximity



Note: EMC1413 can perform Beta
Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe



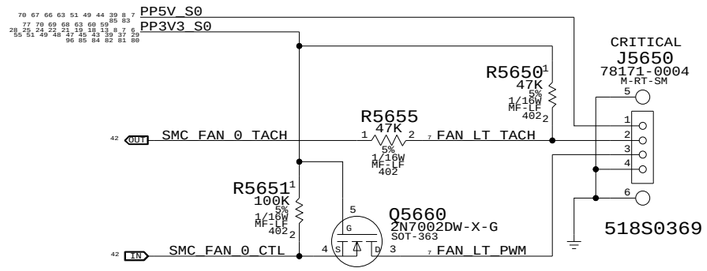
Thermal Sensors

SYNC_MASTER=YUN_K19_MLB SYNC_DATE=12/22/2008

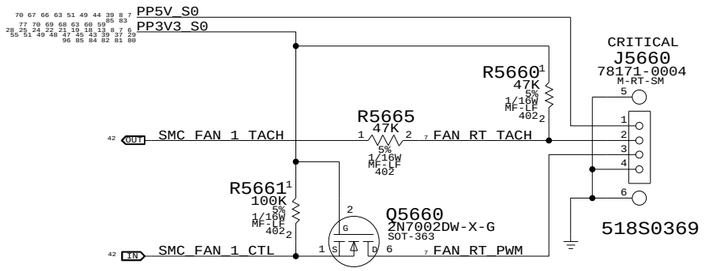
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 48 OF 97	

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

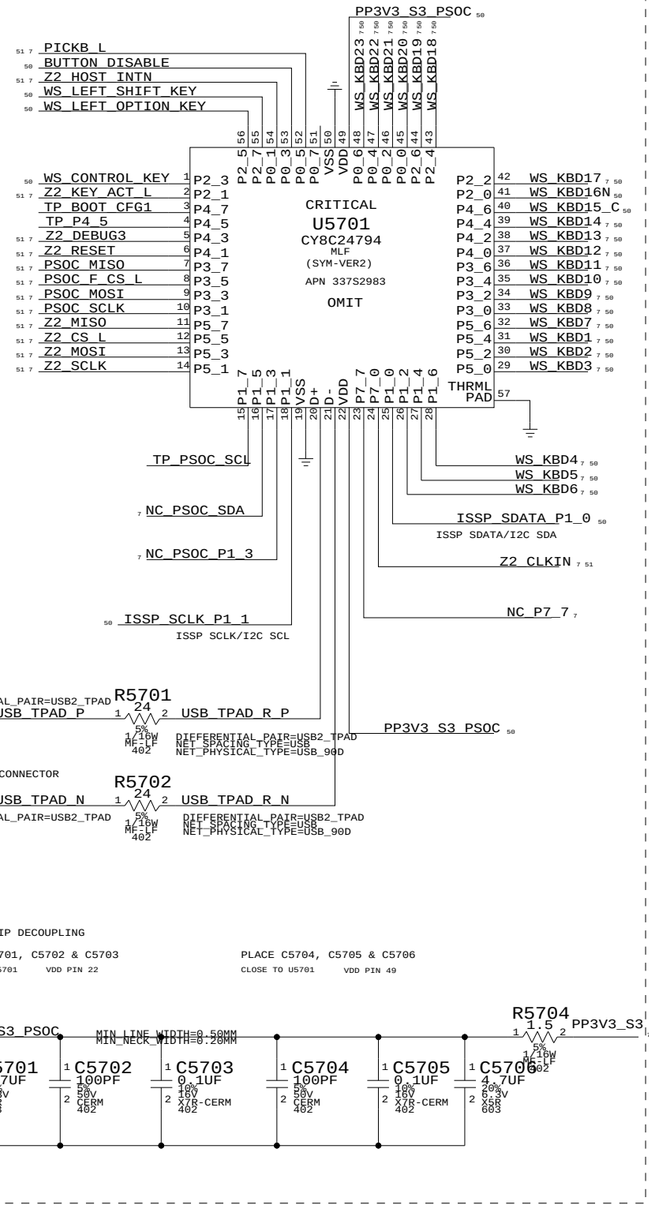
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 49 OF 97	

PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



U5701 CHIP DECOUPLING

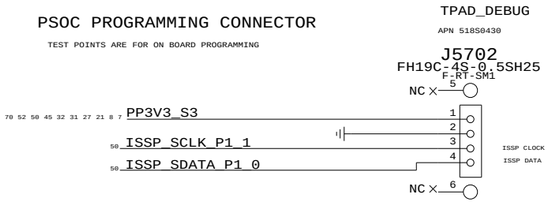
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

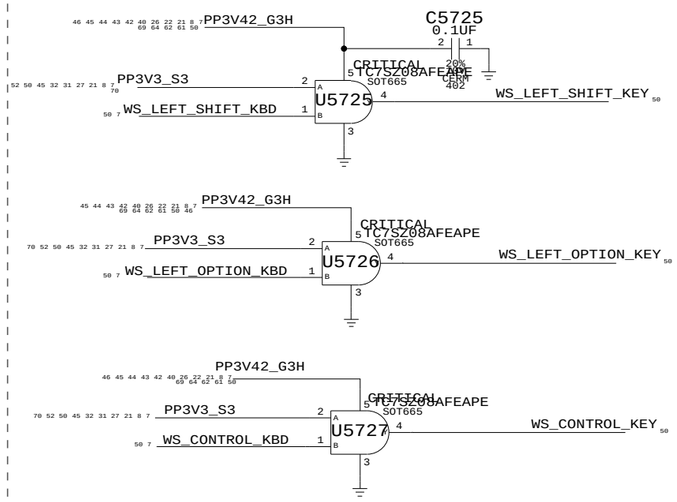
TEST POINTS ARE FOR ON BOARD PROGRAMMING



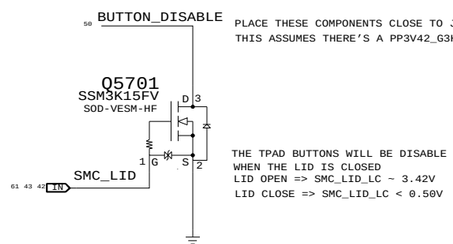
TPAD_DEBUG

APN 518S0430

ISOLATION CIRCUIT



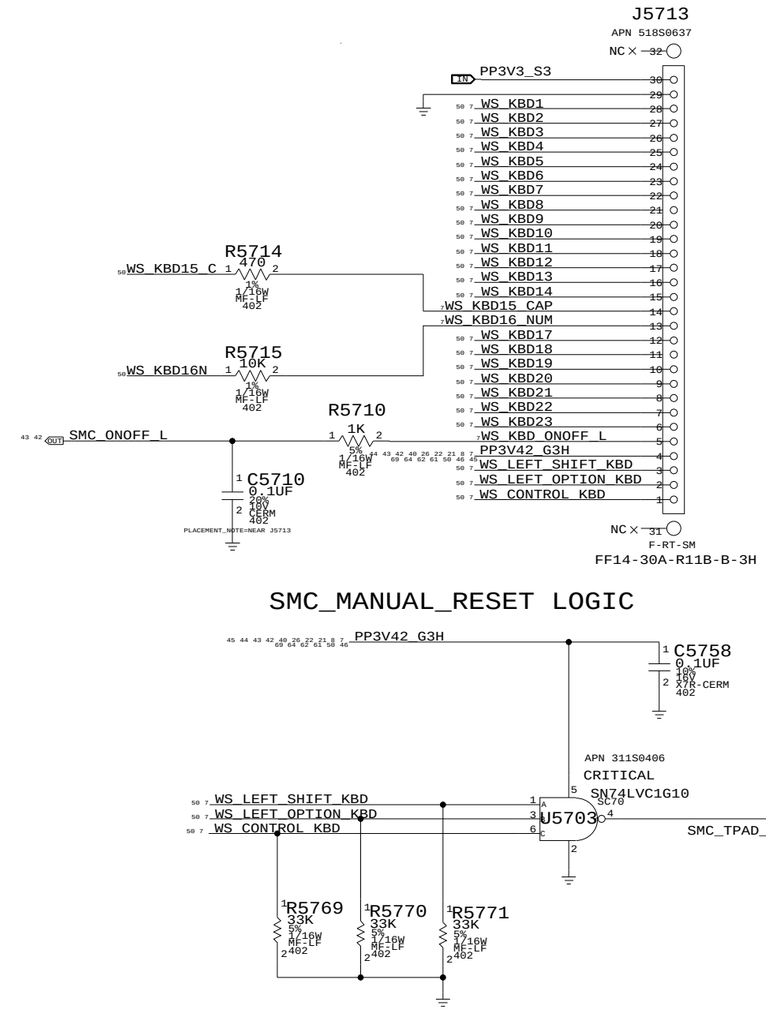
TPAD BUTTONS DISABLE



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



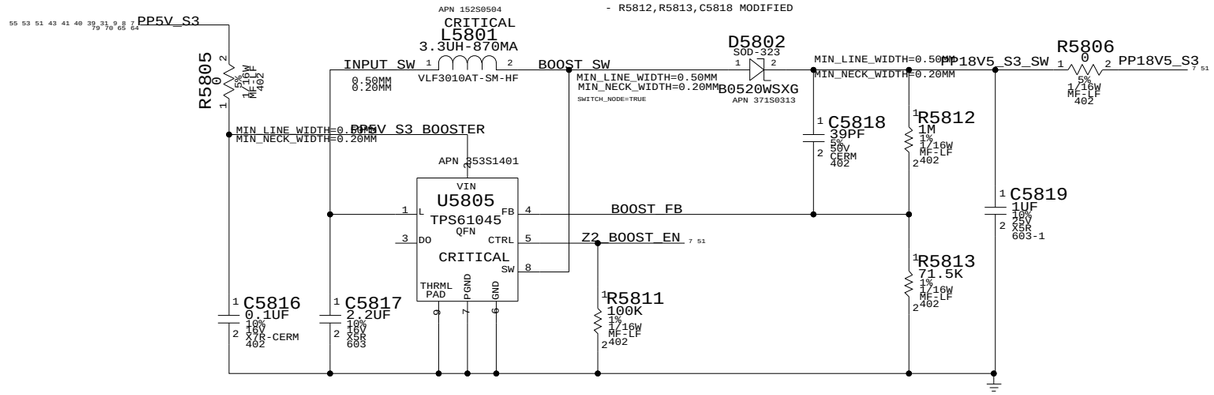
SMC_MANUAL_RESET LOGIC

APPLE INC.

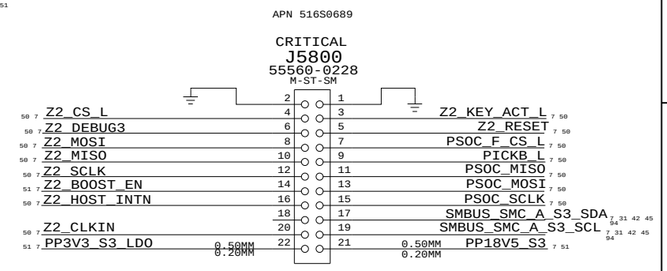
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 50 OF 97	

BOOSTER +18.5VDC FOR SENSORS

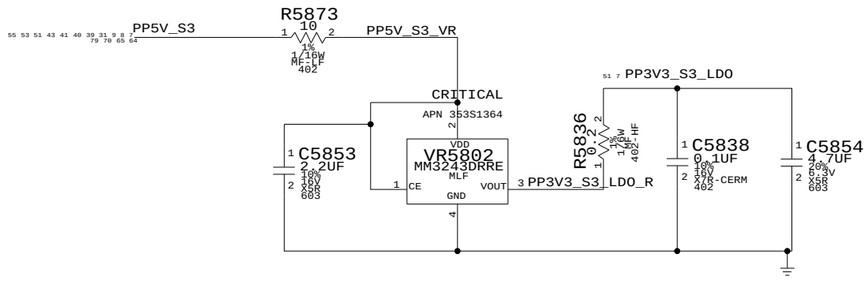
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



Keyboard LED Driver

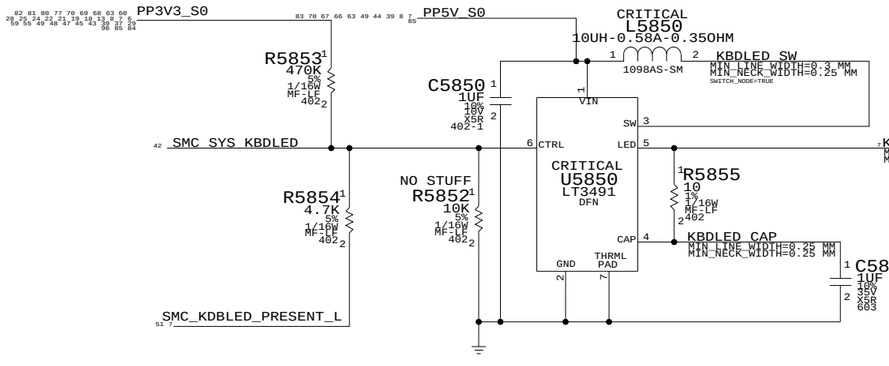
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

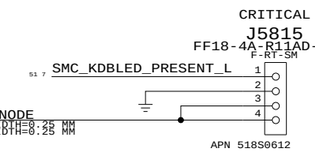
HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT



J5815 pin 1 is grounded on keyboard backlight flex



KBD BACKLIGHT CONNECTOR

WELLSPRING 2

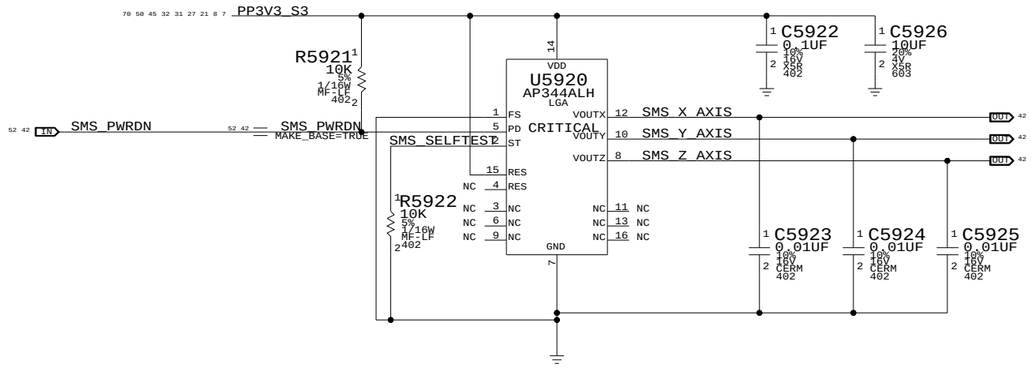
SYNC_MASTER=PWRSQNC SYNC_DATE=01/05/2009

APPLE INC.

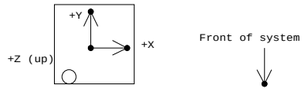
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 51 OF 97	

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when
placed on board top-side:



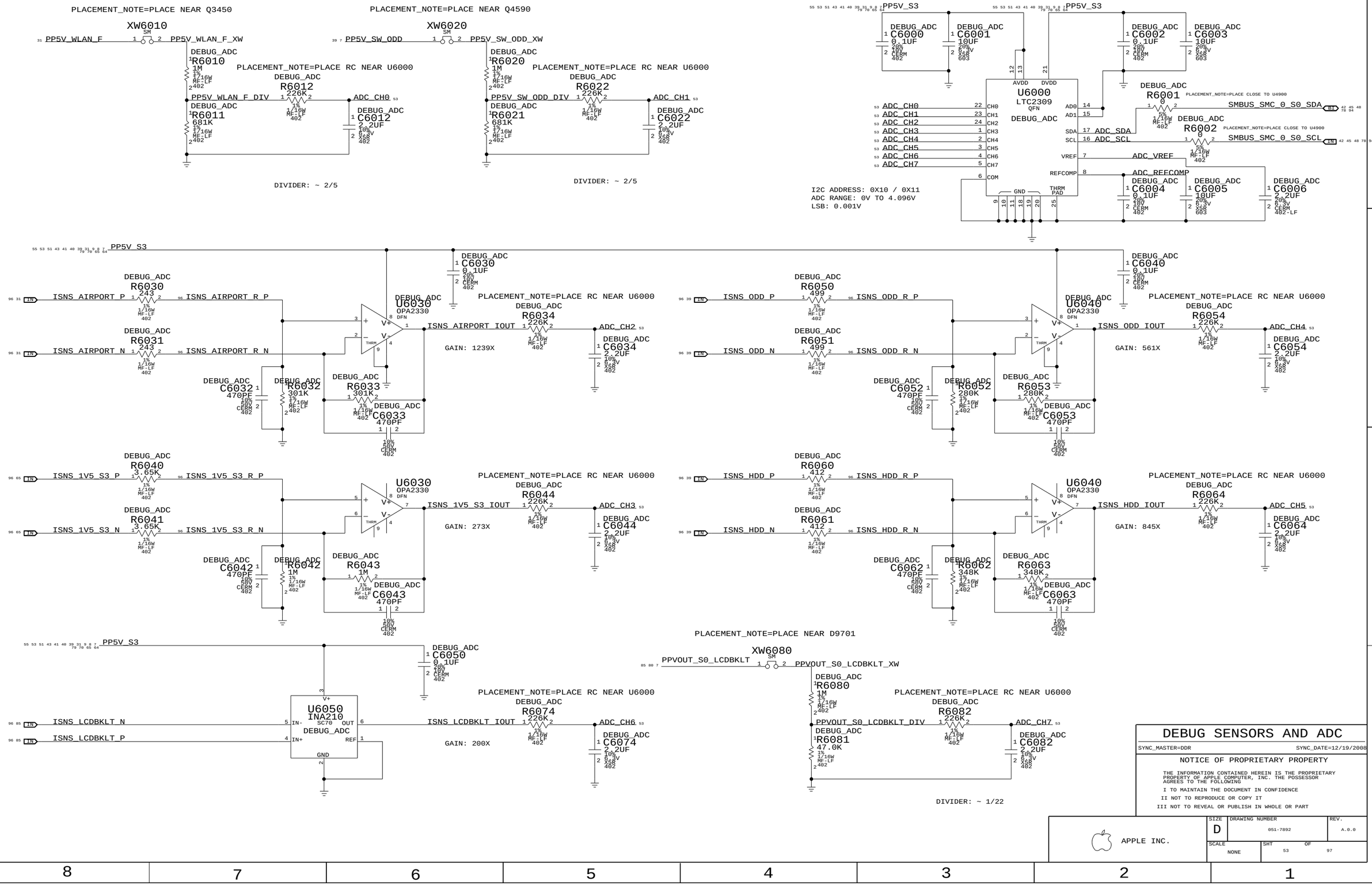
Circle indicates pin 1 location when placed
in correct orientation

Sudden Motion Sensor (SMS)

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 52 OF 97	


PLACEMENT_NOTE=PLACE NEAR Q3450
XW6010
PP5V_WLAN_F
PP5V_WLAN_F_XW
R6010 1M
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6012 226K
PP5V_WLAN_F_DIV
ADC_CH0
R6011 681K
C6012 2.2UF
DIVIDER: ~ 2/5
PLACEMENT_NOTE=PLACE NEAR Q4590
XW6020
PP5V_SW_ODD
PP5V_SW_ODD_XW
R6020 1M
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6022 226K
PP5V_SW_ODD_DIV
ADC_CH1
R6021 681K
C6022 2.2UF
DIVIDER: ~ 2/5
PP5V_S3
C6000 0.1UF
C6001 10UF
C6002 0.1UF
C6003 10UF
U6000 LTC2309 QFN
AVDD
DVDD
GND
THRM PAD
ADC_CH0
ADC_CH1
ADC_CH2
ADC_CH3
ADC_CH4
ADC_CH5
ADC_CH6
ADC_CH7
COM
R6001 0
PLACEMENT_NOTE=PLACE CLOSE TO U4900
SMBUS_SMC_0_S0_SDA
R6002 0
SMBUS_SMC_0_S0_SCL
ADC_SDA
ADC_SCL
ADC_VREF
ADC_REFCOMP
C6004 0.1UF
C6005 10UF
C6006 2.2UF
I2C ADDRESS: 0X10 / 0X11
ADC RANGE: 0V TO 4.096V
LSB: 0.001V
PP5V_S3
C6030 0.1UF
R6030 243
ISNS_AIRPORT_P
ISNS_AIRPORT_R_P
R6031 243
ISNS_AIRPORT_N
ISNS_AIRPORT_R_N
U6030 OPA2330 DFN
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6034 226K
ISNS_AIRPORT_IOUT
ADC_CH2
GAIN: 1239X
C6034 2.2UF
C6032 470PF
R6032 301K
R6033 301K
C6033 470PF
C6040 0.1UF
R6050 499
ISNS_ODD_P
ISNS_ODD_R_P
R6051 499
ISNS_ODD_N
ISNS_ODD_R_N
U6040 OPA2330 DFN
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6054 226K
ISNS_ODD_IOUT
ADC_CH4
GAIN: 561X
C6054 2.2UF
C6052 470PF
R6052 280K
R6053 280K
C6053 470PF
R6040 3.65K
ISNS_1V5_S3_P
ISNS_1V5_S3_R_P
R6041 3.65K
ISNS_1V5_S3_N
ISNS_1V5_S3_R_N
U6030 OPA2330 DFN
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6044 226K
ISNS_1V5_S3_IOUT
ADC_CH3
GAIN: 273X
C6044 2.2UF
C6042 470PF
R6042 1M
R6043 1M
C6043 470PF
R6060 412
ISNS_HDD_P
ISNS_HDD_R_P
R6061 412
ISNS_HDD_N
ISNS_HDD_R_N
U6040 OPA2330 DFN
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6064 226K
ISNS_HDD_IOUT
ADC_CH5
GAIN: 845X
C6064 2.2UF
C6062 470PF
R6062 348K
R6063 348K
C6063 470PF
PP5V_S3
C6050 0.1UF
U6050 INA210 SC70
ISNS_LCDBKLT_N
ISNS_LCDBKLT_P
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6074 226K
ISNS_LCDBKLT_IOUT
ADC_CH6
GAIN: 200X
C6074 2.2UF
PLACEMENT_NOTE=PLACE NEAR D9701
XW6080
PPVOUT_S0_LCDBKLT
PPVOUT_S0_LCDBKLT_XW
R6080 1M
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6082 226K
PPVOUT_S0_LCDBKLT_DIV
ADC_CH7
R6081 47.0K
C6082 2.2UF
DIVIDER: ~ 1/22
DEBUG SENSORS AND ADC
SYNC_MASTER=DDR
SYNC_DATE=12/19/2008
NOTICE OF PROPRIETARY PROPERTY
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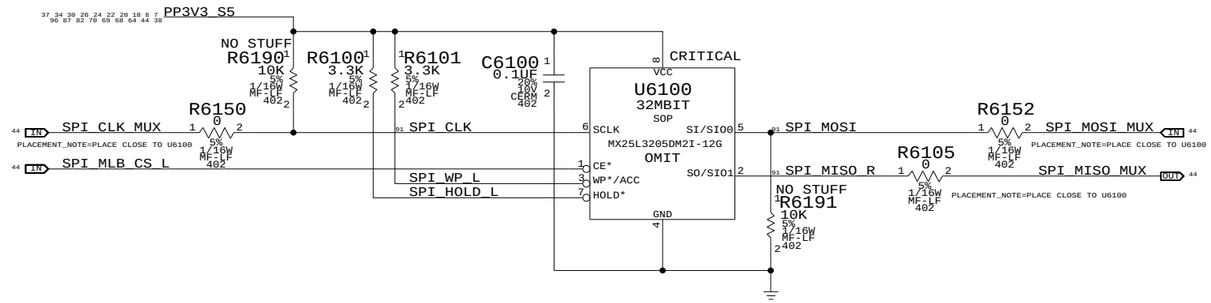
APPLE INC.
SIZE D
DRAWING NUMBER 051-7892
REV. A.0.0
SCALE NONE
SHT 53 OF 97



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

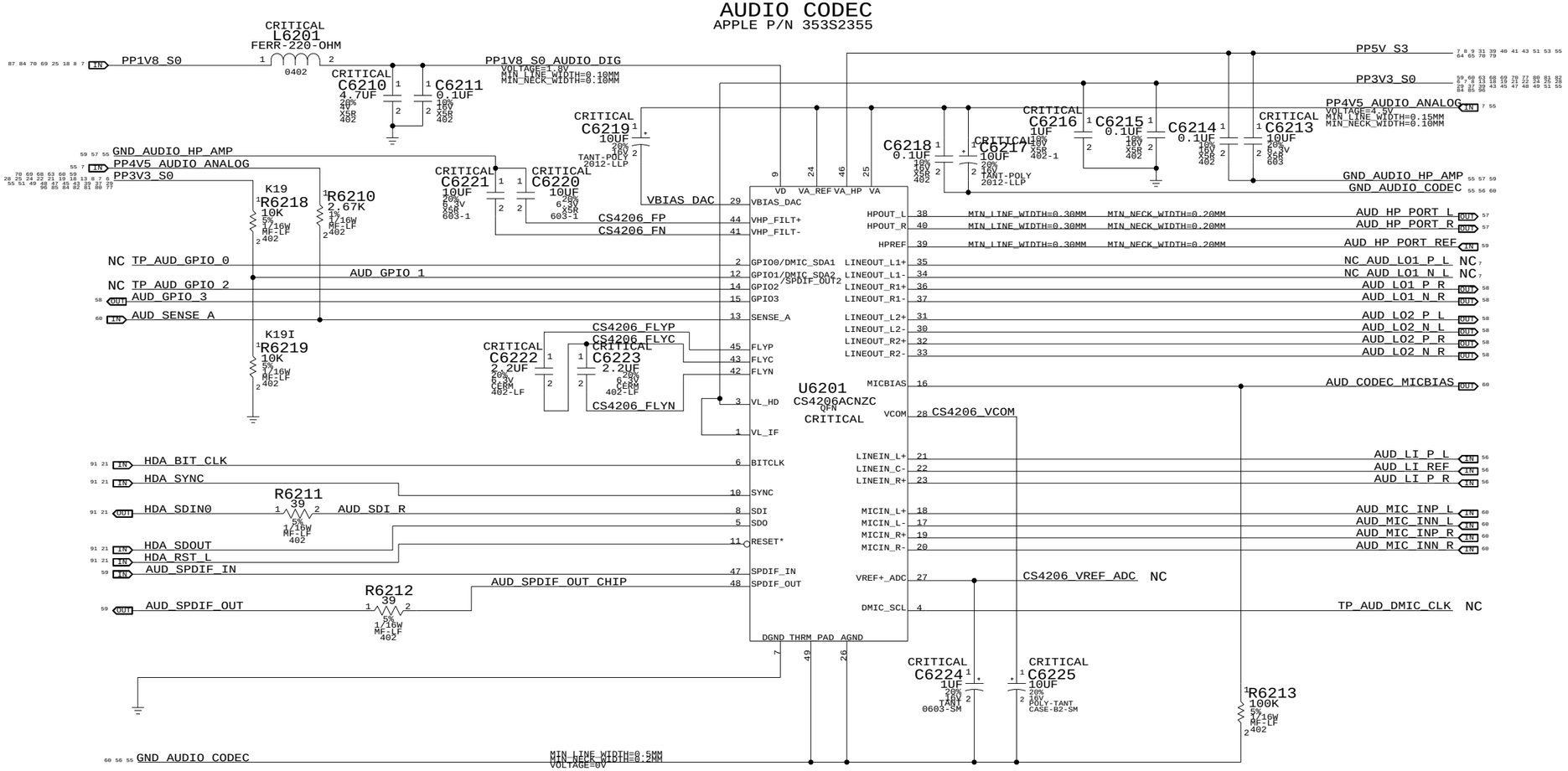
SPI ROM

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

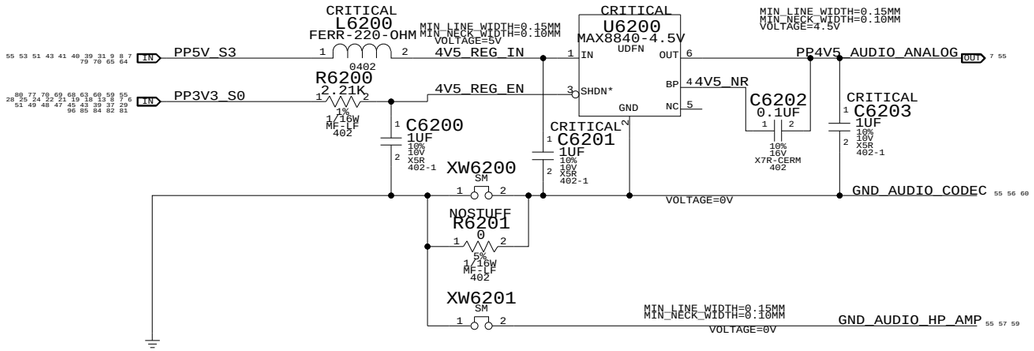
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 54 OF 97	

AUDIO CODEC
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

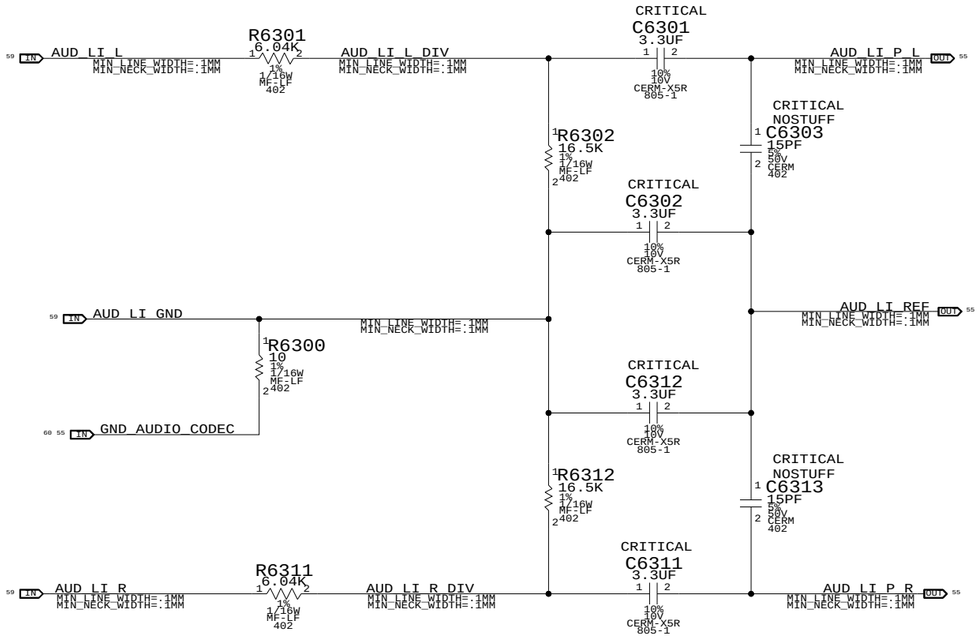
AUDIO: CODEC/REGULATOR

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 55 OF 97	

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 20K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.21 VRMS

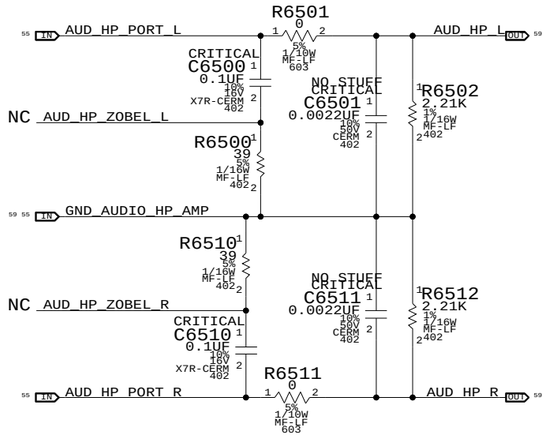


AUDIO: LINE INPUT FILTER

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 56 OF 97	

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



AUDIO: HEADPHONE FILTER

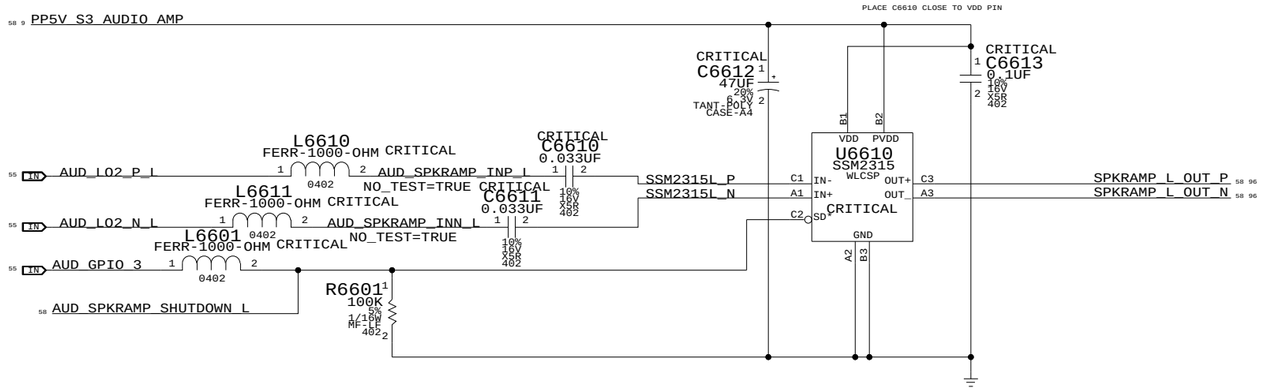
SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009

APPLE INC.

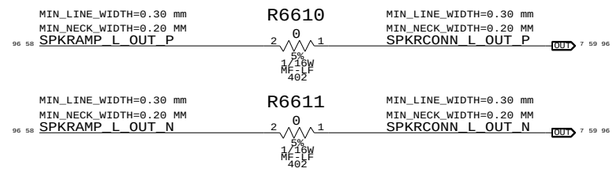
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 57 OF 97	

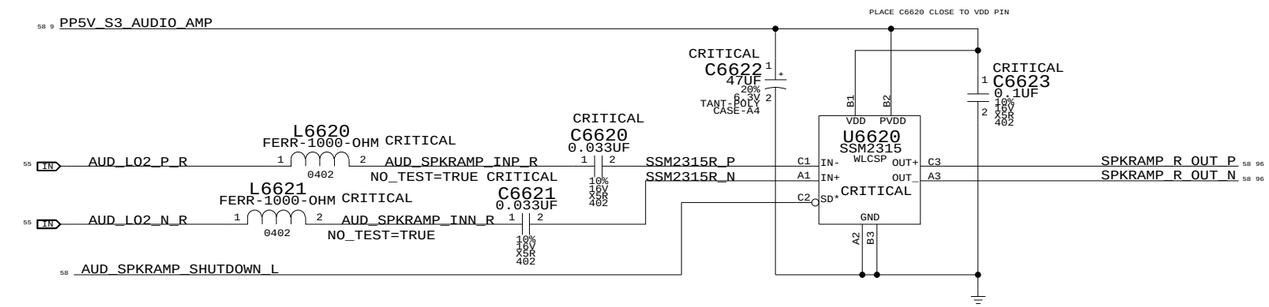
3X MONO SPEAKER AMPLIFIERS (SSM2315)
APN: 353S2500

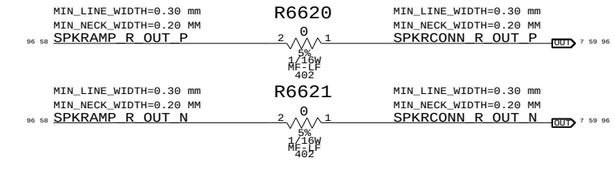
GAIN = 6DB
1ST ORDER FC (L&R) = 120 HZ +/- 30%
1ST ORDER FC (SUB) = 58HZ +/- 30%

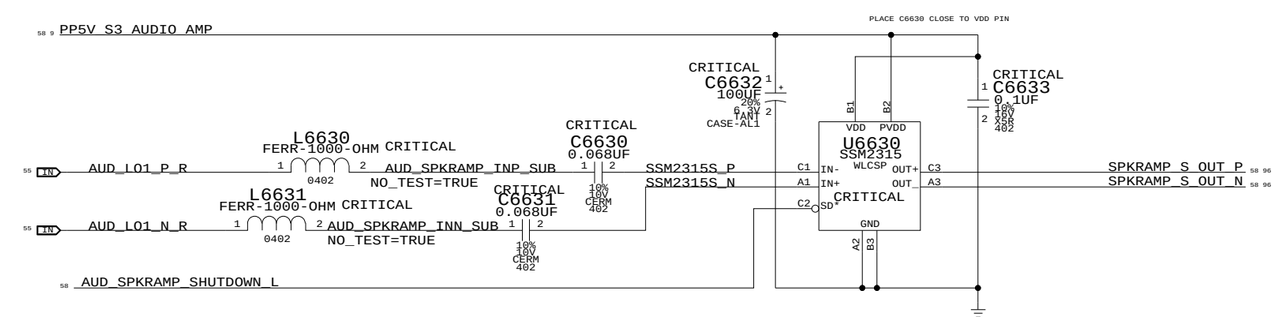


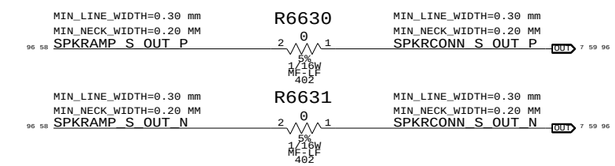
SPEAKER CHECKPOINTS











AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 58 OF 97	

AUDIO JACK 1 LO/HP JACK, SPDIF TX

PP3V3_S0
APN: 514-0671
J6700
SPDIF-TXRX-K24
F-RT-TH
MIC
DETECT
SWITCH
LEFT
RIGHT
GND
AUDIO
A - VIN
B - VCC
C - GND
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
AUD_CONNJ1_SLEEVE2
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING
AUD_CONNJ1_SLEEVE
C6700 0.1UF 10% 10V X5R 402
C6701 2.2UF 20% 6.3V CERM 402-LF
AUD_SPDIF_OUT
L6703 FERR-1000-OHM CRITICAL 0402
HS_MIC_HI
L6702 FERR-1000-OHM CRITICAL 0402
HS_MIC_LO
L6707 CRITICAL FERR-220-OHM 0402
AUD_HP_PORT_REF
L6701 CRITICAL FERR-220-OHM-2.5A 0603
GND_AUDIO_HP_AMP
L6704 CRITICAL FERR-220-OHM 0402
AUD_HP_R
L6706 CRITICAL FERR-220-OHM 0402
AUD_HP_L
R6700 10K 5% 1/16W MF-LF 402
AUD_J1_SLEEVEDET_R
L6705 FERR-1000-OHM CRITICAL 0402
AUD_J1_TIPDET_R
DZ6703 CRITICAL 6.8V-100PF 402
DZ6704 CRITICAL 6.8V-100PF 402
DZ6700 CRITICAL 6.8V-100PF 402
DZ6706 CRITICAL 6.8V-100PF 402
DZ6701 CRITICAL 6.8V-100PF 402
C6705 100PF 5% 50V CERM 402
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.10 MM
VOLTAGE=0V
GND_CHASSIS_AUDIO_JACK
XW6701 SM
XW6702 SM
GND PATCH
R6701 0 5% 1/10W MF-LF 402
GND_CHASSIS_AUDIO_JACK

MIC CONNECTOR

APN: 518S0520
CRITICAL
J6780
78171-0003
M-RT-SM
BI_MIC_LO
BI_MIC_SHIELD
BI_MIC_HI

SPEAKER CONNECTOR

APN: 518S0519
CRITICAL
J6781
78171-0002
M-RT-SM
SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N

APN: 518S0521
CRITICAL
J6782
78171-0004
M-RT-SM
SPKRCONN_S_OUT_P
SPKRCONN_S_OUT_N
SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
NOSTUFF CRITICAL C6781 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6782 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6783 33PF 5% 50V CERM 402
NOSTUFF CRITICAL C6784 33PF 5% 50V CERM 402

AUDIO JACK 2 LINE IN JACK, SPDIF RX

PP3V3_S0
APN: 514-0635
J6750
AUDIO-RCVR-M97
F-RT-TH5
DETECT_FOR_PLUG_TYPE
SWITCH
LEFT
RIGHT
GROUND
AUDIO
A - VDD
B - GND
C - VOUT
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
C6750 1UF 10% 10V X5R 402-1
AUD_J2_OPT_OUT
R6749 4.7 5% 1/10W MF-LF 402
AUD_SPDIF_IN
AUD_CONNJ2_SLEEVE
AUD_CONNJ2_TIPDET
AUD_CONNJ2_RING
AUD_CONNJ2_TIP
AUD_CONNJ2_SLEEVEDET
L6751 FERR-220-OHM CRITICAL 0402
L6754 CRITICAL FERR-1000-OHM 0402
AUD_LI_R
L6756 CRITICAL FERR-1000-OHM 0402
AUD_LI_L
L6758 CRITICAL FERR-220-OHM 0402
AUD_LI_GND
L6752 CRITICAL FERR-1000-OHM 0402
AUD_J2_TIPDET_R
DZ6754 CRITICAL 6.8V-100PF 402
DZ6756 CRITICAL 6.8V-100PF 402
DZ6758 CRITICAL 6.8V-100PF 402
DZ6751 CRITICAL 6.8V-100PF 402
C6756 100PF 5% 50V CERM 402
GND_CHASSIS_AUDIO_JACK

AUDIO: JACKS

SYNC_MASTER=AUDIO
SYNC_DATE=03/16/2009

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 59 OF 97	

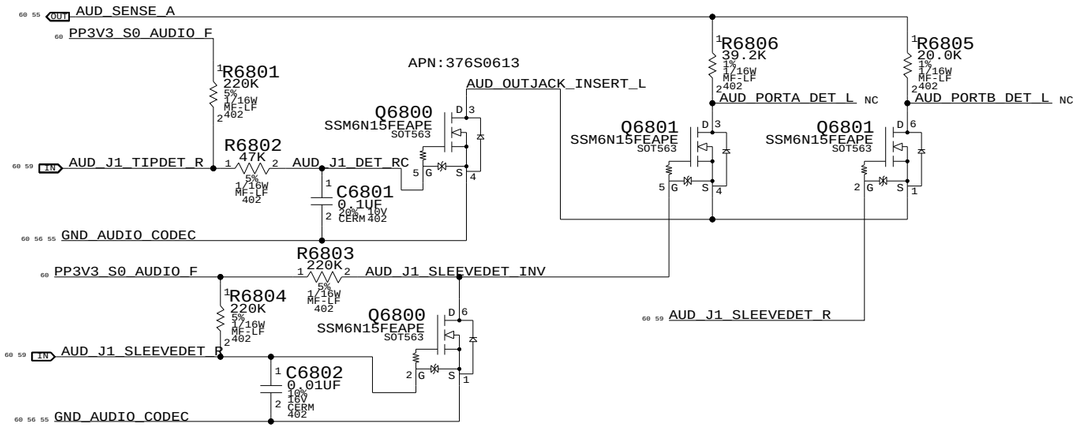
CODEC OUTPUT SIGNAL PATHS

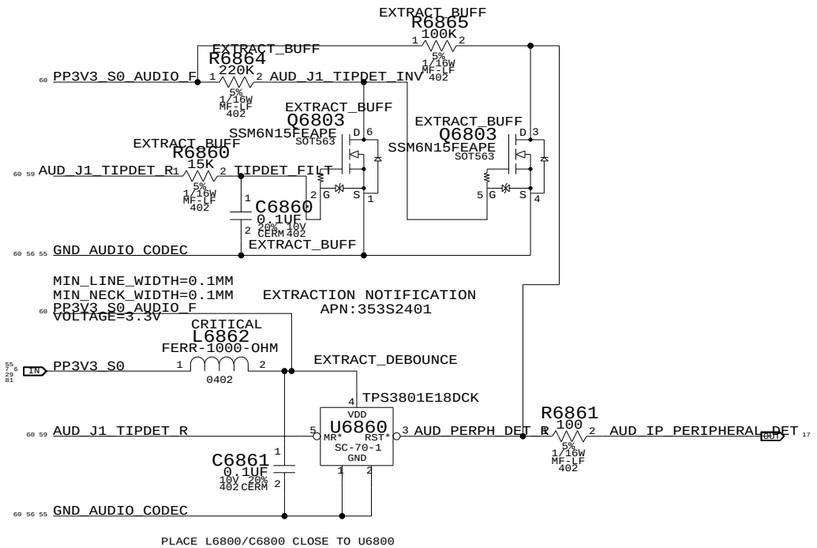
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

CODEC INPUT SIGNAL PATHS

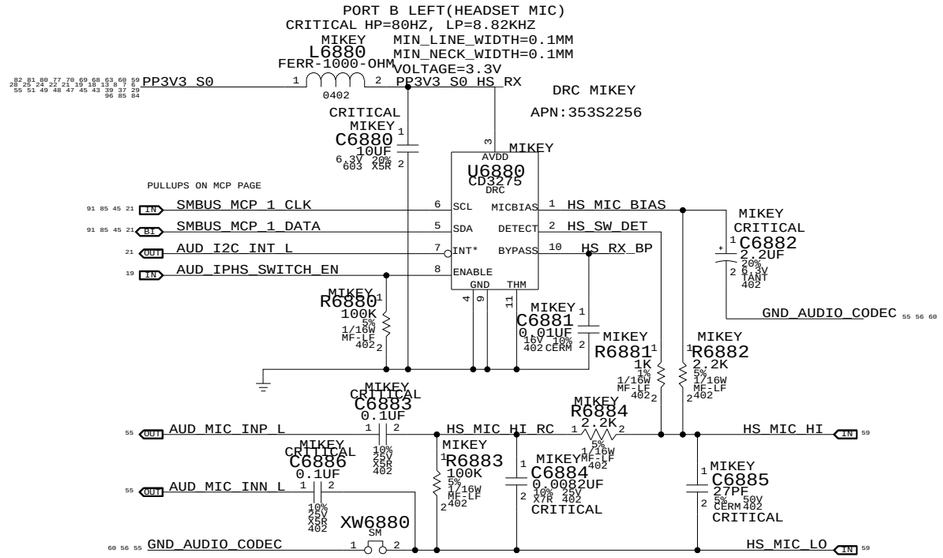
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)

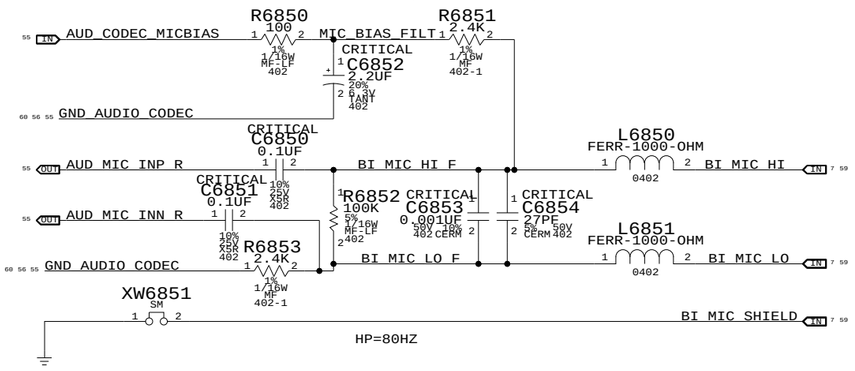




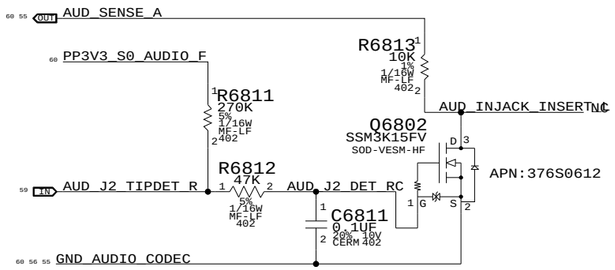
PORT B LEFT(HEADSET MIC)
CRITICAL HP=80HZ, LP=8.82KHZ
MIN_LINE_WIDTH=0.1MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=3.3V



PORT B RIGHT(BUILT-IN MIC)



PORT C DETECT (LINE-IN)



AUDIO: JACK TRANSLATORS		
SYNC_MASTER=AUDIO	SYNC_DATE=03/16/2009	

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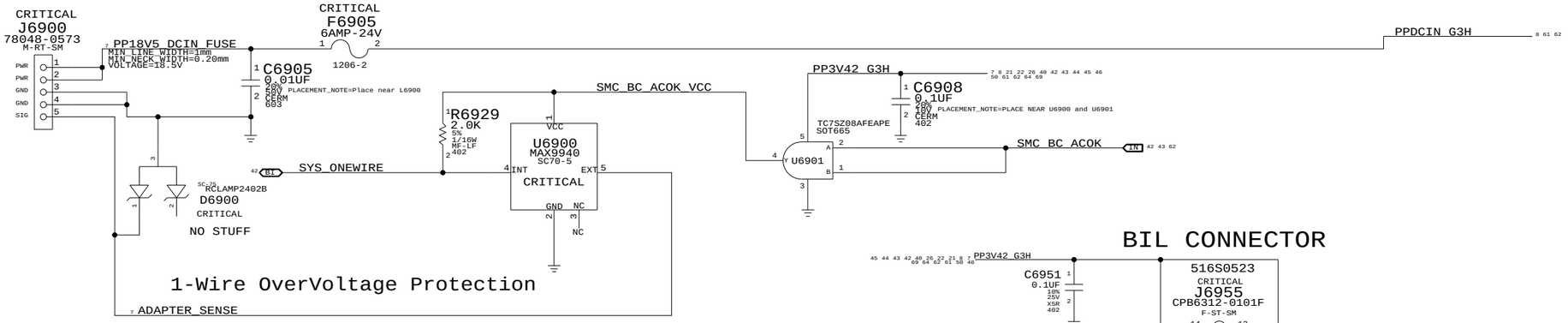
APPLE INC.

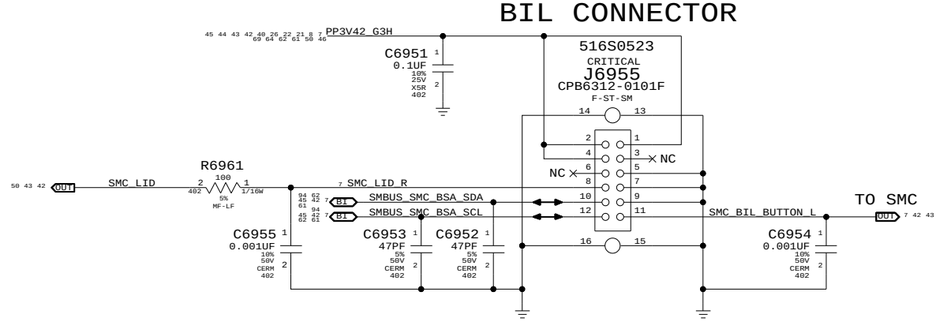
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 60 OF 97	

MagSafe DC Power Jack



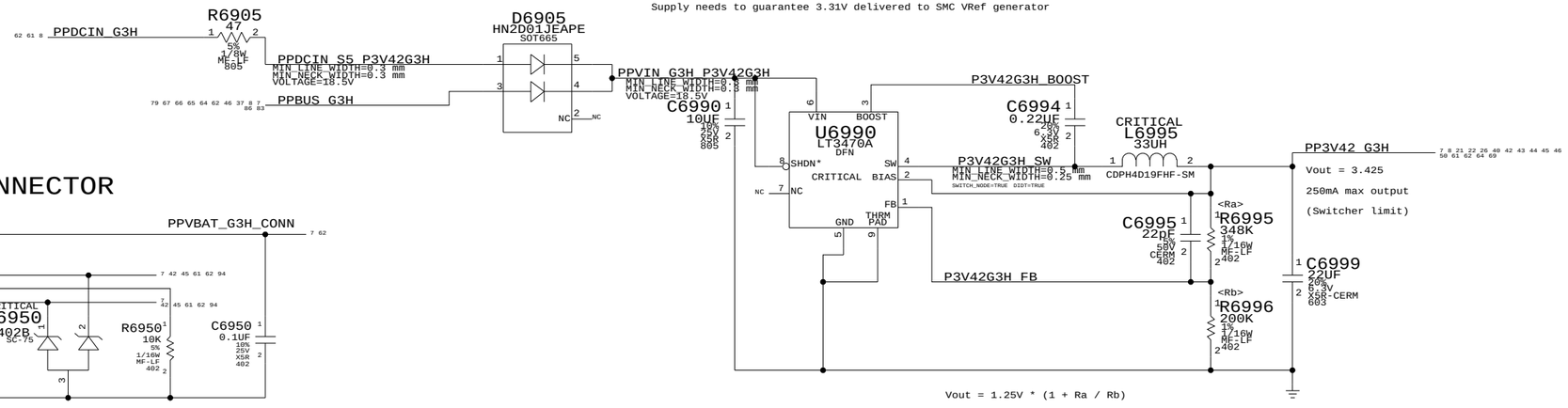
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR

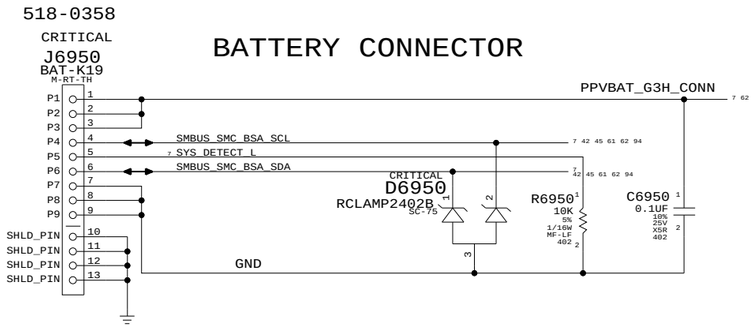


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



DC-In & Battery Connectors			
SYNC_MASTER=YUN_K19_MLB	SYNC_DATE=12/16/2008		
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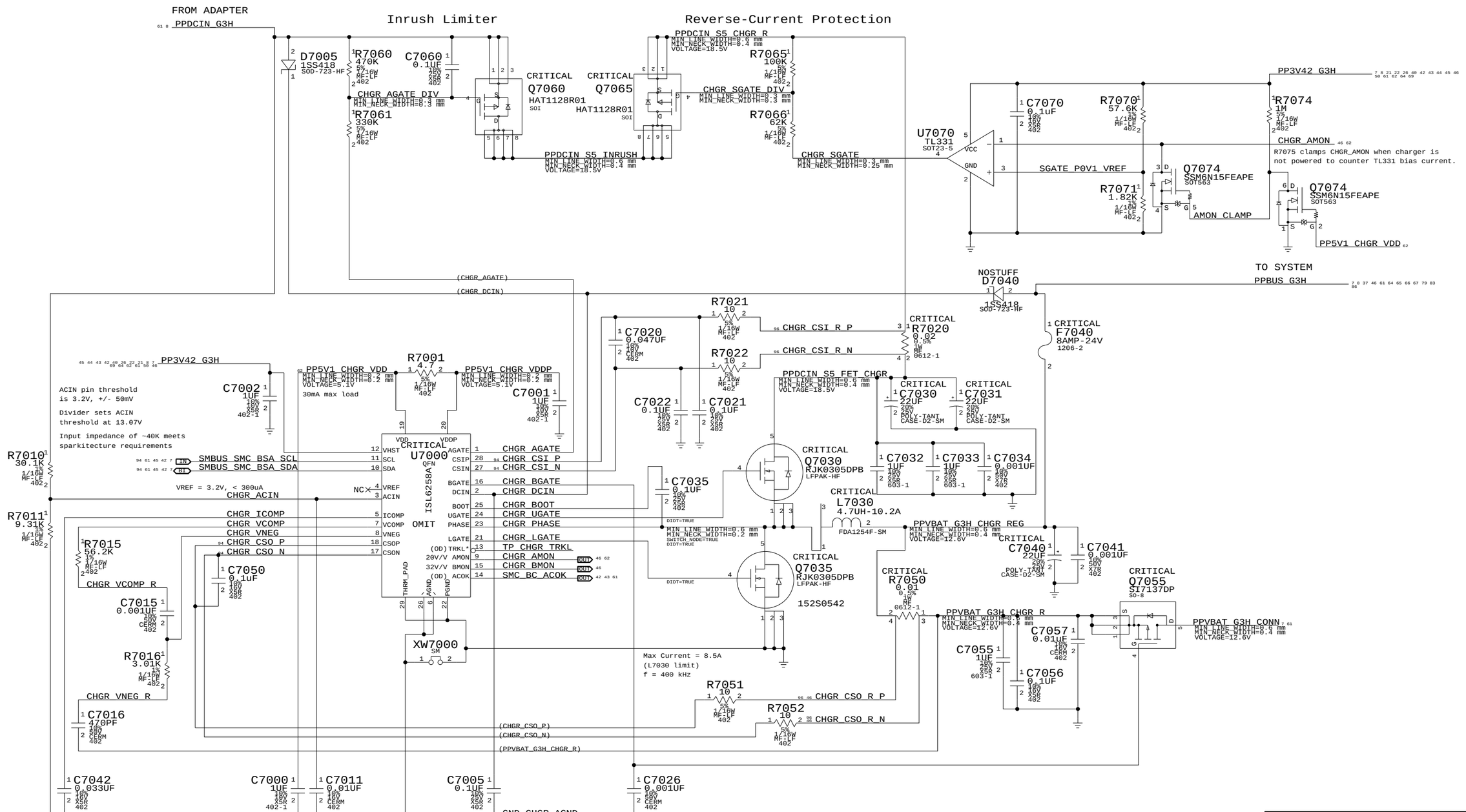
APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7892	REV: A.0.0
	SCALE: NONE	SHT: 61	OF: 97



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1811	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

PBus Supply & Battery Charger

SYNC_MASTER=M99_MLB SYNC_DATE=12/10/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT: 62	OF: 97

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

Place R7131 Between L7100,L7101 and CPU

IMVP6_PHASE1	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		

IMVP6_PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		

IMVP_VR_ON	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_OCSET	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_VO	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_DROOP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_DFB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_SOFT	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_RBIAS	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_VDIFF	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_FB2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_FB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_COMP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_VW	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		

IMVP6 CPU VCore Regulator

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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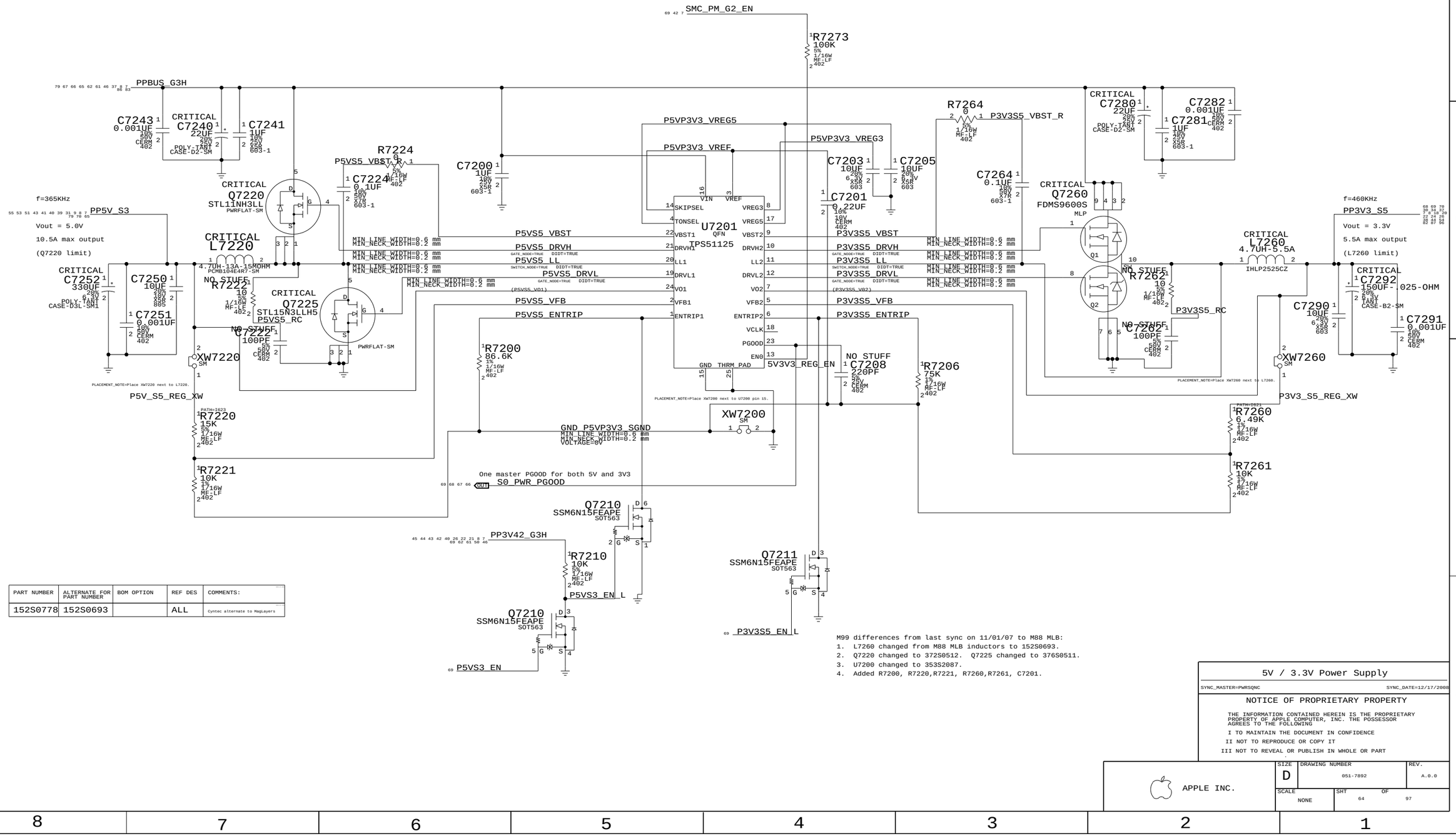
SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT: 63	OF: 97



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	Cyntec alternate to MagLayers

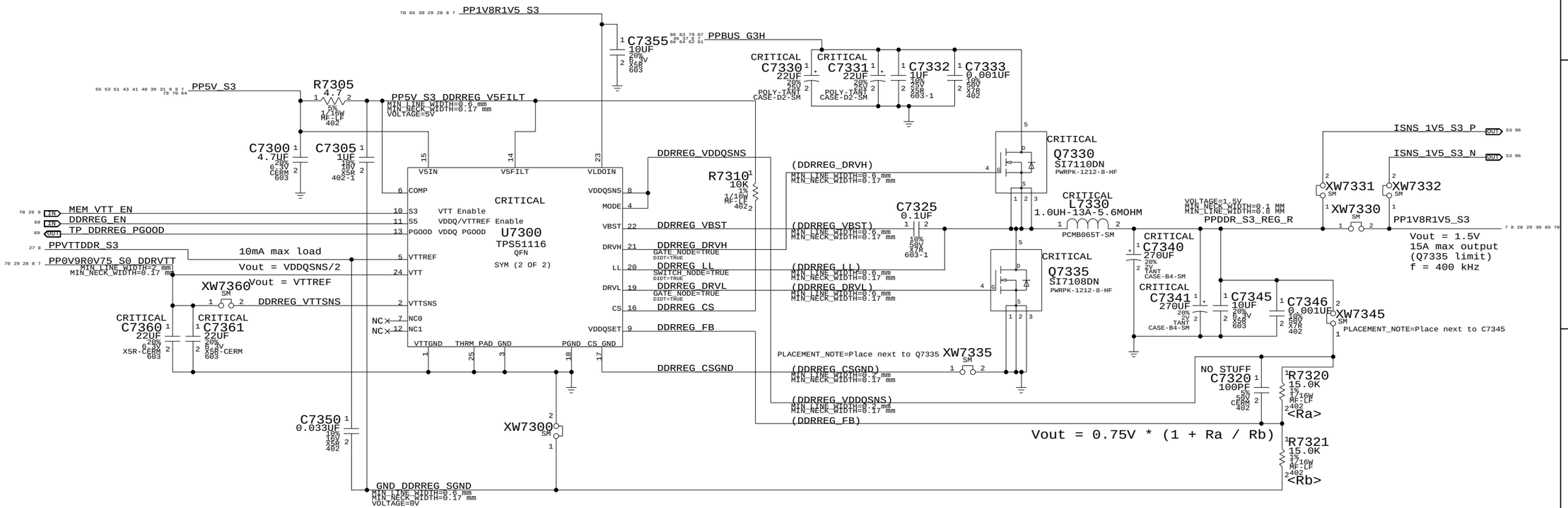
M99 differences from last sync on 11/01/07 to M88 MLB:
1. L7260 changed from M88 MLB inductors to 152S0693.
2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
3. U7200 changed to 353S2087.
4. Added R7200, R7220,R7221, R7260,R7261, C7201.

5V / 3.3V Power Supply

SYNC_MASTER=PWRSQNC SYNC_DATE=12/17/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 64	OF 97

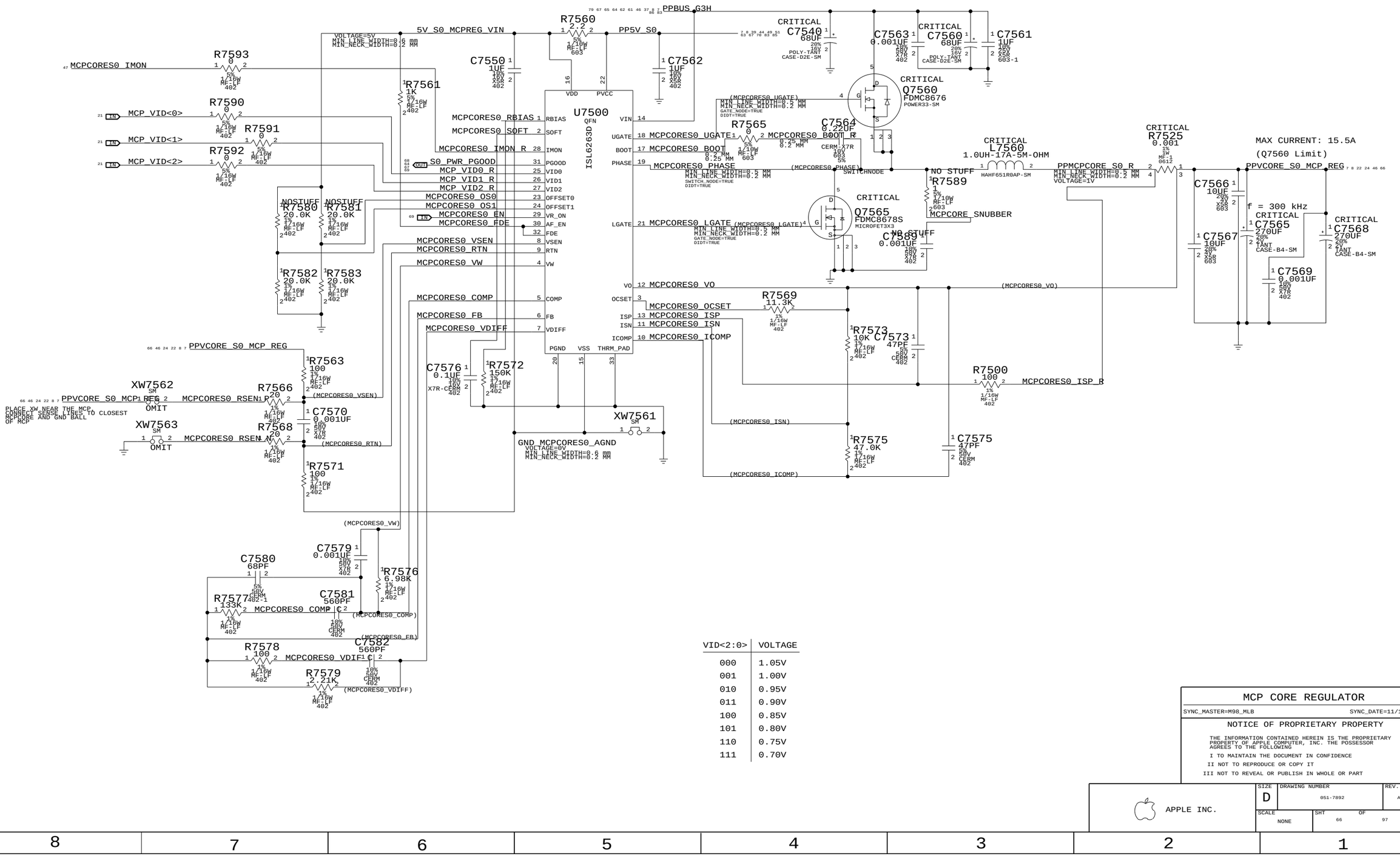


1.5V DDR3 Supply

SYNC_MASTER=DDR SYNC_DATE=12/05/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 65 OF 97	


U7500
ISL6263D
QFN
R7560 2.2
PPBUS_G3H
5V_S0_MCPREG_VIN
PP5V_S0
MCPCORES0_IMON
MCP_VID<0>
MCP_VID<1>
MCP_VID<2>
S0_PWR_PGOOD
MCPCORES0_RBIAS
MCPCORES0_SOFT
MCPCORES0_IMON_R
MCP_VID0_R
MCP_VID1_R
MCP_VID2_R
MCPCORES0_OS0
MCPCORES0_OS1
MCPCORES0_EN
MCPCORES0_FDE
MCPCORES0_VSEN
MCPCORES0_RTN
MCPCORES0_VW
MCPCORES0_COMP
MCPCORES0_FB
MCPCORES0_VDIFF
MCPCORES0_PHASE
MCPCORES0_UGATE
MCPCORES0_BOOT_R
MCPCORES0_LGATE
MCPCORES0_VO
MCPCORES0_OCSET
MCPCORES0_ISP
MCPCORES0_ISN
MCPCORES0_ICOMP
MCPCORES0_ISP_R
PPVCORE_S0_MCP_REG
MCPCORES0_RSEN
GND_MCPCORES0_AGND
CRITICAL
NO STUFF
MCPCORE_SNUBBER
MAX CURRENT: 15.5A
(Q7560 Limit)
f = 300 kHz
PLACE XW NEAR THE MCP
CONNECT SENSE LINES TO CLOSEST
MCPCORE AND GND BALL
OF MCP
VID<2:0>
VOLTAGE
000 1.05V
001 1.00V
010 0.95V
011 0.90V
100 0.85V
101 0.80V
110 0.75V
111 0.70V
MCP CORE REGULATOR
SYNC_MASTER=M98_MLB
SYNC_DATE=11/14/2008
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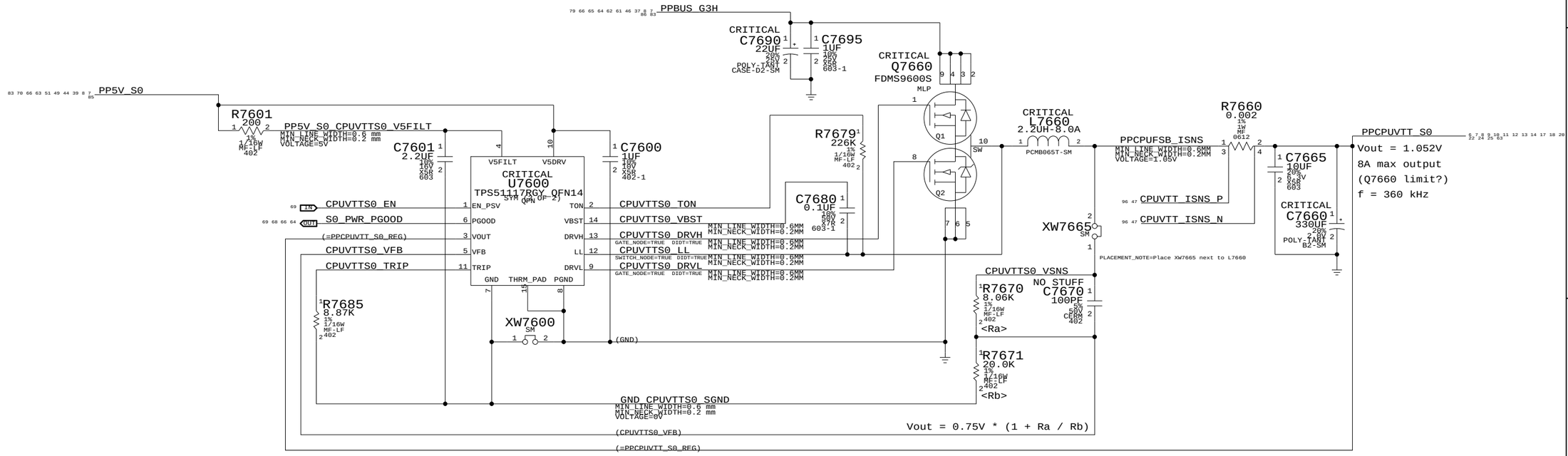
APPLE INC.
SIZE D
DRAWING NUMBER 051-7892
REV. A.0.0
SCALE NONE
SHT 66 OF 97



M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

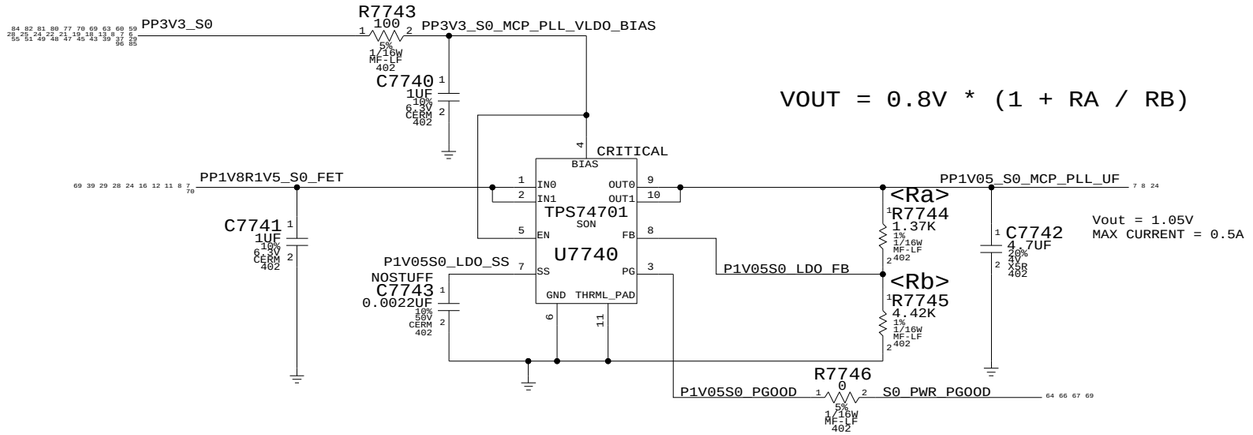
CPU VTT / 1V05 S0 Power Supply

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

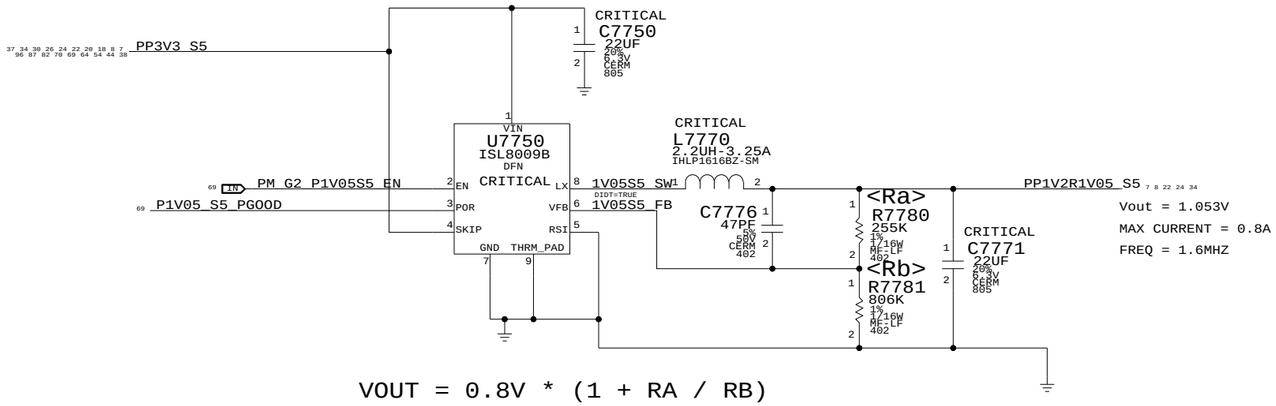
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 67 OF 97	

1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY



VOUT = 0.8V * (1 + RA / RB)

Misc Power Supplies

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 68 OF 97	

3.3V 1,05V S5 ENABLE

R7802 100K 5% 1/16W MF-LF 402 — PP3V42_G3H — P3V3S5_EN_L (OUT)

NO STUFF C7802 0.068UF 10% 16V CERM 402

Q7800 SSM3K15FV SOD-VESM-HF

SMC_PM_G2_EN (IN) — R7858 100K 5% 1/16W MF-LF 402

R7801 5.1K 5% 1/16W MF-LF 402 — PM_G2_P1V05S5_EN — PM_G2_P1V05S5_EN (OUT) MAKE_BASE=TRUE

C7801 0.47UF 10% 6.3V CERM-X5R 402

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

S5 rail PWRGD

PP3V42_G3H — C7840 0.1UF 20% 16V CERM 402 — R7840 100K 5% 1/16W MF-LF 402

PP3V3_S5

U7840 TPS3808G33DBVRG4 SOT23-6 (VDD, SENSE, CT, GND, RESET*, MR*)

CT — C7841 0.001UF 20% 25V CERM 402

RSMRST_PWRGD (42)

P1V05_S5_PGOOD (68)

TPS3808 MR* HAS INTERNAL PULLUP

3.3V,5V S3 ENABLE

PM_SLP_S4_L (IN) MAKE_BASE=TRUE — R7810 100K 5% 1/16W MF-LF 402

(PM_S4_STATE_L) — PM_SLP_S4_L (OUT)

R7811 5.1K 5% 1/16W MF-LF 402 — R7812 0 5% 1/16W MF-LF 402

P5VS3_EN — P5VS3_EN (OUT) MAKE_BASE=TRUE

DDRREG_EN — DDRREG_EN (OUT) MAKE_BASE=TRUE

C7810 0.47UF 10% 6.3V CERM-X5R 402

NO STUFF C7812 0.47UF 10% 6.3V CERM-X5R 402

S0 ENABLE

(PM_SLP_S3_L)

PM_SLP_S3_L (IN) — R7878 100 5% 1/16W MF-LF 402

R7879 100K 5% 1/16W MF-LF 402

PM_SLP_S3_L_R — MAKE_BASE=TRUE

R7880 22K 5% 1/16W MF-LF 402 — R7881 33K 5% 1/16W MF-LF 402 — R7882 0 5% 1/16W MF-LF 402 — R7883 10K 5% 1/16W MF-LF 402 — R7884 0 5% 1/16W MF-LF 402

PM_SLP_S3_L_R (OUT)

P3V3S0_EN — MAKE_BASE=TRUE — P3V3S0_EN (OUT)

P1V2R1V8S0_EN — MAKE_BASE=TRUE — P1V2R1V8S0_EN (OUT)

MCPDDR_EN — MAKE_BASE=TRUE — MCPDDR_EN (OUT)

CPUVTTS0_EN — MAKE_BASE=TRUE — CPUVTTS0_EN (OUT)

MCPCORES0_EN — MAKE_BASE=TRUE — MCPCORES0_EN (OUT)

C7880 0.47UF 10% 6.3V CERM-X5R 402 — C7881 0.47UF — NO STUFF C7882 0.47UF — C7883 0.47UF — NO STUFF C7884 0.47UF

Other S0 RAILS

	PM_ALL_GFX_PGOOD
IG	high
EG	PM_ALL_GPU_PGOOD

PP3V3_S0 — R7892 10K 5% 1/16W MF-LF 402

S0_PWR_PGOOD — MAKE_BASE=TRUE

R7894 0 5% 1/16W MF-LF 402 — C7889 0.1UF 20% 16V CERM 402

PP3V3_S5

NO STUFF R7891 0 5% 1/16W MF-LF 402

PM_ALL_GPU_PGOOD — ALL_GFX_PGOOD_R

U7880 TC7SZ08AFEAPE SOT665 — ALL_SYS_PWRGD (OUT)

Unused PGOOD signal

TP_DDRREG_PGOOD — TP_DDRREG_PGOOD MAKE_BASE=TRUE

1.1V GPU ENABLE

EG_PWRSEQ_HW R7851 10K 5% 1/16W MF-LF 402 — PP3V3_S0 — P1V1_GPU_EN_RC

EG_PWRSEQ_HW R7850 100K 5% 1/16W MF-LF 402 — PP3V3_S5

EG_PWRSEQ_HW Q7850 SSM6N15FEAPE SOT563

EXTGPU_PWR_EN (IN) — R7853 100K 5% 1/16W MF-LF 402

EG_PWRSEQ_HW Q7850 SSM6N15FEAPE SOT563

R7852 0 5% 1/16W MF-LF 402 — P1V1_GPU_EN — P1V1_GPU_EN (OUT) MAKE_BASE=TRUE

NO STUFF C7859 0.022UF 20% 16V CERM 402

GPU_S0_EN_L — MAKE_BASE=TRUE — GPU_S0_EN_L

Graphic MEM ENABLE

EG_PWRSEQ_HW R7868 100K 5% 1/16W MF-LF 402 — PP3V3_S0GPU — P1V8_S0GPU_EN_RC

EG_PWRSEQ_HW R7869 0 5% 1/16W MF-LF 402 — P1V8_S0GPU_EN — MAKE_BASE=TRUE — P1V8_S0GPU_EN (OUT)

GPUVCORE_PGOOD

EG_PWRSEQ_HW Q7861 SSM6N15FEAPE SOT563

NO STUFF C7869 0.022UF 20% 16V CERM 402

G96 GPU requires rails to come up in the following order:
1) 1.1V
2) GPU_3.3V
3) GPUvcore
4) GDDR3 1.8V
BOMOPTION: EG

3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

place XW0402 if needed to save trace space for pin 7,8

PP3V3_S0 — C7870 0.1UF 20% 16V CERM 402

APN: 353S2310

U7870 ISL88042IRTEZ TDFN (VDD, V2MON, V3MON, V4MON, MR*, RST*, GND, THRM_PAD, NC)

PP1V8R1V5_S0_FET

PP1V8_S0

S0_PWR_PGOOD

V2MON THRESHOLD IS 2.866V
V3MON THRESHOLD IS 0.6V
V4MON THRESHOLD IS 0.6V

GPUVCORE ENABLE

EG_PWRSEQ_HW R7863 100K 5% 1/16W MF-LF 402 — PP3V3_S0GPU — GPUVCORE_EN_RC

EG_PWRSEQ_HW R7864 0 5% 1/16W MF-LF — GPUVCORE_EN — GPUVCORE_EN (OUT) MAKE_BASE=TRUE

EG_PWRSEQ_HW Q7861 SSM6N15FEAPE SOT563

GPU_S0_EN_L

C7861 0.01UF 10% 16V CERM 402

EXT GPU PWRGD Pullup

PP3V3_S0

EG_PWRSEQ_HW R7889 100K 5% 1/16W MF-LF 402

P1V1GPU_PGOOD — EG_PWRSEQ_HW R7888 0 5% 1/16W MF-LF 402 — P3V3GPU_EN (OUT)

R7890 100K 5% 1/16W MF-LF 402

PM_ALL_GPU_PGOOD — ALL_GPU_PGOOD — MAKE_BASE=TRUE (OUT)

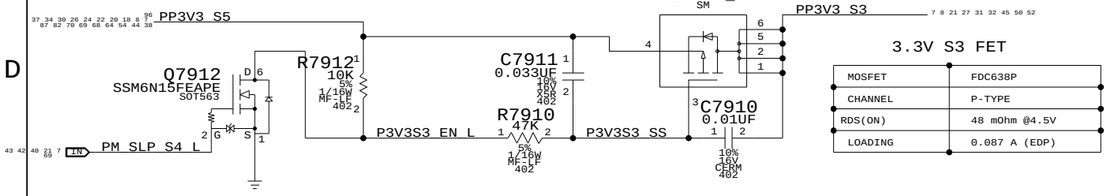
Power Control

SYNC_MASTER=PWRSQNC SYNC_DATE=12/17/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT: 69	OF: 97

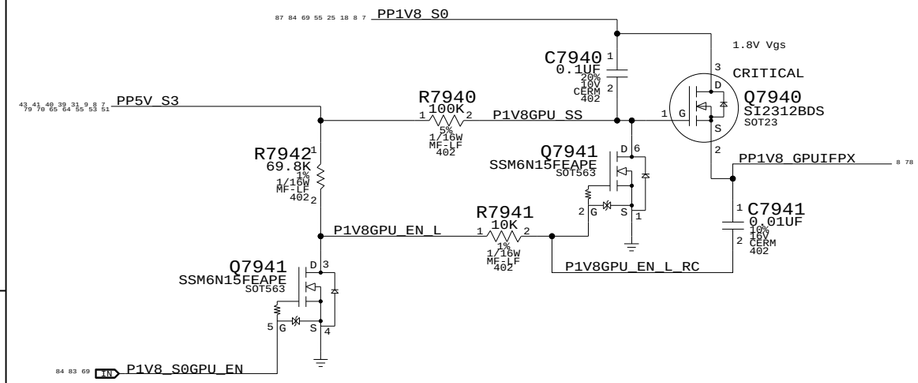
3.3V S3 FET



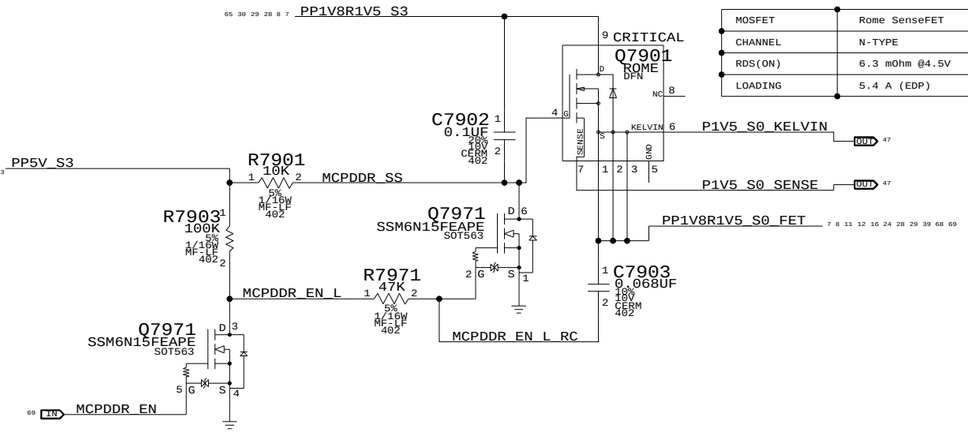
3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

1.8V GPU FET



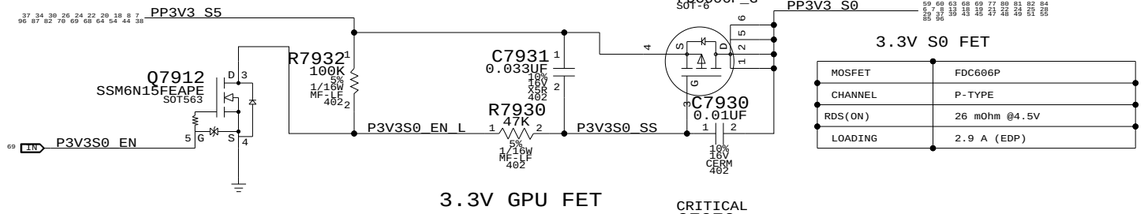
1.5V S0 FET



1.5V S0 FET

MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOhm @4.5V
LOADING	5.4 A (EDP)

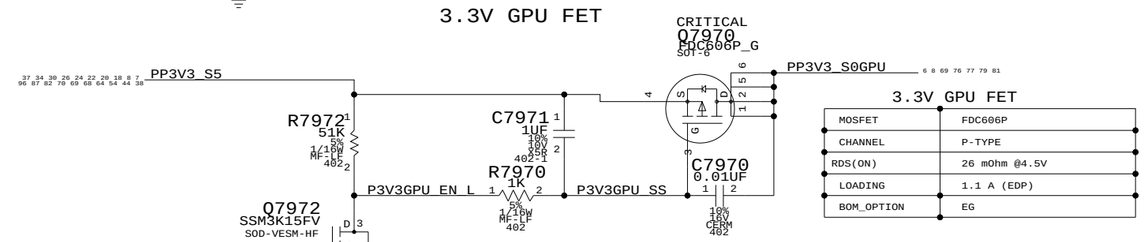
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

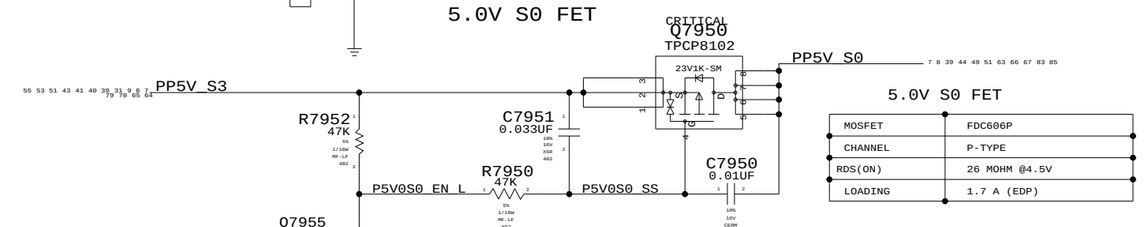
3.3V GPU FET



3.3V GPU FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)
BOM_OPTION	EG

5.0V S0 FET

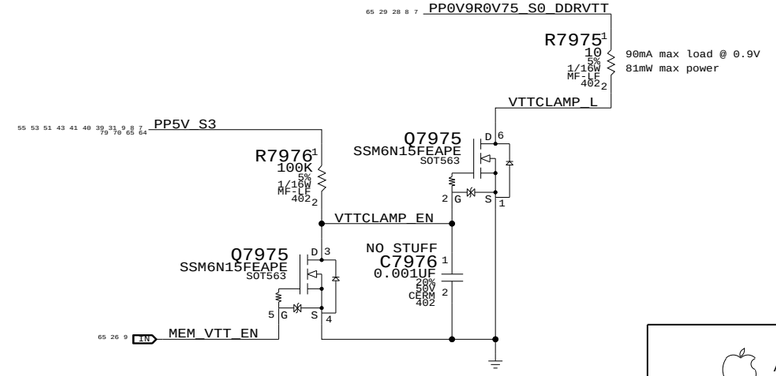


5.0V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.7 A (EDP)

MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.



Power FETs

SYNC_MASTER=DDR SYNC_DATE=12/05/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 70 OF 97	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PEX 1.1V Current = 2A

PP1V1_S0GPU_REG
PP1V1_S0GPU_REG
PP1V1_S0GPU_REG

250mA

C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805
C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA

C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8009 1UF 10% 6.3V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

180mA

L8015 10NH-600MA 0603

PP1V1_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V

C8017 0.1UF 20% 10V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

NC_GPU_DFM
NO_TEST=TRUE

OMIT

U8000
NB9P-GS
BGA
SYMBOL 2 OF 9

H32	PEX_IOVDD1	AK16
M7	PEX_IOVDD2	AK17
P6	PEX_IOVDD3	AK21
P7	PEX_IOVDD4	AK24
R7	PEX_IOVDD5	AK27
U7		
V6		
AB7		
AD6	PEX_IOVDDQ1	AG11
AF6	PEX_IOVDDQ2	AG12
AG6	PEX_IOVDDQ3	AG13
AJ5	PEX_IOVDDQ4	AG15
D35	PEX_IOVDDQ5	AG16
AK15	PEX_IOVDDQ6	AG17
AL7	PEX_IOVDDQ7	AG18
E7	PEX_IOVDDQ8	AG22
E35	PEX_IOVDDQ9	AG23
F7	PEX_IOVDDQ10	AG24
A2	PEX_IOVDDQ11	AG25
	PEX_IOVDDQ12	AG26
	PEX_IOVDDQ13	AJ14
	PEX_IOVDDQ14	AJ15
	PEX_IOVDDQ15	AJ19
	PEX_IOVDDQ16	AJ21
	PEX_IOVDDQ17	AJ22
	PEX_IOVDDQ18	AJ24
	PEX_IOVDDQ19	AJ25
	PEX_IOVDDQ20	AJ27
	PEX_IOVDDQ21	AK18
	PEX_IOVDDQ22	AK20
	PEX_IOVDDQ23	AK23
	PEX_IOVDDQ24	AK26
	PEX_IOVDDQ25	AL16
	PEX_PLLVDD	AG14
	VDD_SENSE	AD20
	GND_SENSE	AD19

NC

VDD_SENSE → GPU_VDD_SENSE (79)
GND_SENSE → GPU_GND_SENSE (79)

OMIT

U8000
NB9P-GS
BGA
SYMBOL 1 OF 9

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AP17	PEX_RX0	PEX_TX0 AL17 → PEG_D2R_C_P<0> C8055 0.1uF → PEG_D2R_P<0>
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AN17	PEX_RX0*	PEX_TX0* AM17 → PEG_D2R_C_N<0> C8056 0.1uF → PEG_D2R_N<0>
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AN19	PEX_RX1	PEX_TX1 AM18 → PEG_D2R_C_P<1> C8057 0.1uF → PEG_D2R_P<1>
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AP19	PEX_RX1*	PEX_TX1* AM19 → PEG_D2R_C_N<1> C8058 0.1uF → PEG_D2R_N<1>
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AR19	PEX_RX2	PEX_TX2 AL19 → PEG_D2R_C_P<2> C8059 0.1uF → PEG_D2R_P<2>
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AR20	PEX_RX2*	PEX_TX2* AK19 → PEG_D2R_C_N<2> C8060 0.1uF → PEG_D2R_N<2>
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AP20	PEX_RX3	PEX_TX3 AL20 → PEG_D2R_C_P<3> C8061 0.1uF → PEG_D2R_P<3>
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AN20	PEX_RX3*	PEX_TX3* AM20 → PEG_D2R_C_N<3> C8062 0.1uF → PEG_D2R_N<3>
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AN22	PEX_RX4	PEX_TX4 AM21 → PEG_D2R_C_P<4> C8063 0.1uF → PEG_D2R_P<4>
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AP22	PEX_RX4*	PEX_TX4* AM22 → PEG_D2R_C_N<4> C8064 0.1uF → PEG_D2R_N<4>
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AR22	PEX_RX5	PEX_TX5 AL22 → PEG_D2R_C_P<5> C8065 0.1uF → PEG_D2R_P<5>
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AR23	PEX_RX5*	PEX_TX5* AK22 → PEG_D2R_C_N<5> C8066 0.1uF → PEG_D2R_N<5>
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AP23	PEX_RX6	PEX_TX6 AL23 → PEG_D2R_C_P<6> C8067 0.1uF → PEG_D2R_P<6>
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AN23	PEX_RX6*	PEX_TX6* AM23 → PEG_D2R_C_N<6> C8068 0.1uF → PEG_D2R_N<6>
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AN25	PEX_RX7	PEX_TX7 AM24 → PEG_D2R_C_P<7> C8069 0.1uF → PEG_D2R_P<7>
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AP25	PEX_RX7*	PEX_TX7* AM25 → PEG_D2R_C_N<7> C8070 0.1uF → PEG_D2R_N<7>
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AR25	PEX_RX8	PEX_TX8 AL25 → PEG_D2R_C_P<8> C8071 0.1uF → PEG_D2R_P<8>
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AR26	PEX_RX8*	PEX_TX8* AK25 → PEG_D2R_C_N<8> C8072 0.1uF → PEG_D2R_N<8>
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AP26	PEX_RX9	PEX_TX9 AL26 → PEG_D2R_C_P<9> C8073 0.1uF → PEG_D2R_P<9>
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AN26	PEX_RX9*	PEX_TX9* AM26 → PEG_D2R_C_N<9> C8074 0.1uF → PEG_D2R_N<9>
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AN28	PEX_RX10	PEX_TX10 AM27 → PEG_D2R_C_P<10> C8075 0.1uF → PEG_D2R_P<10>
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AP28	PEX_RX10*	PEX_TX10* AM28 → PEG_D2R_C_N<10> C8076 0.1uF → PEG_D2R_N<10>
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AR28	PEX_RX11	PEX_TX11 AL28 → PEG_D2R_C_P<11> C8077 0.1uF → PEG_D2R_P<11>
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AR29	PEX_RX11*	PEX_TX11* AK28 → PEG_D2R_C_N<11> C8078 0.1uF → PEG_D2R_N<11>
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AP29	PEX_RX12	PEX_TX12 AK29 → PEG_D2R_C_P<12> C8079 0.1uF → PEG_D2R_P<12>
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AN29	PEX_RX12*	PEX_TX12* AL29 → PEG_D2R_C_N<12> C8080 0.1uF → PEG_D2R_N<12>
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AN31	PEX_RX13	PEX_TX13 AM29 → PEG_D2R_C_P<13> C8081 0.1uF → PEG_D2R_P<13>
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AP31	PEX_RX13*	PEX_TX13* AM30 → PEG_D2R_C_N<13> C8082 0.1uF → PEG_D2R_N<13>
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AR31	PEX_RX14	PEX_TX14 AM31 → PEG_D2R_C_P<14> C8083 0.1uF → PEG_D2R_P<14>
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AR32	PEX_RX14*	PEX_TX14* AM32 → PEG_D2R_C_N<14> C8084 0.1uF → PEG_D2R_N<14>
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AR34	PEX_RX15	PEX_TX15 AN32 → PEG_D2R_C_P<15> C8085 0.1uF → PEG_D2R_P<15>
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AP34	PEX_RX15*	PEX_TX15* AP32 → PEG_D2R_C_N<15> C8086 0.1uF → PEG_D2R_N<15>
PEG_CLK100M_P			AR16	PEX_REFCLK	PEX_TSTCLK_OUT AJ17 → PEX_TSTCLK_P → R8060 200 1% 1/10W MF-LF 402
PEG_CLK100M_N			AR17	PEX_REFCLK*	PEX_TSTCLK_OUT* AJ18 → PEX_TSTCLK_N
EG_RESET_L	R8020 0 5% 1/10W MF-LF 402	GPU_RESET_R_L	AM16	PEX_RST*	PEX_TERMP AG21 → PEX_TERMP_PD → R8050 2.49K 1% 1/10W MF-LF 402
		TP_PEX_CLKREQ_L	AR13	PEX_CLKREQ*	
				PEX_RFU1	AG19 NC
				PEX_RFU2	AG20 NC

All C8xxx capacitors: 10% 16V X5R 402

NV G96 PCI-E		
SYNC_MASTER=MUXGFX	SYNC_DATE=07/10/2008	

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7892	A.0.0
	SCALE: NONE	SHT 71 OF 97	

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

79 8 46 PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 4.7UF 20% 6.3V X5R-CERM 402
C8101 4.7UF 20% 6.3V X5R-CERM 402
C8102 4.7UF 20% 6.3V X5R-CERM 402

C8103 0.47UF 10% 6.3V CERM-X5R 402
C8104 0.47UF 10% 6.3V CERM-X5R 402
C8105 0.47UF 10% 6.3V CERM-X5R 402
C8106 0.47UF 10% 6.3V CERM-X5R 402
C8107 0.47UF 10% 6.3V CERM-X5R 402

C8108 0.47UF 10% 6.3V CERM-X5R 402
C8109 0.47UF 10% 6.3V CERM-X5R 402
C8110 0.47UF 10% 6.3V CERM-X5R 402
C8111 0.47UF 10% 6.3V CERM-X5R 402
C8112 0.47UF 10% 6.3V CERM-X5R 402

C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402

C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 9 OF 9

L11			V19
L12			V21
L13			V23
L14			V25
L15			W11
L16			W12
L17			W13
L18			W14
L19			W15
L20			W16
L21			W17
L22			W18
L23			W19
L24			AD24
L25			W21
M12			W22
M14			W23
M16			W24
M18			W25
M20			Y12
M22			Y14
M24			Y16
P11			Y18
P13			Y20
P15			Y22
P17			Y24
P19			AB11
P21			AB13
P23	VDD	VDD	AB15
P25			AB17
R11			AB19
R12			AB21
R13			AB23
R14			AB25
R15			AC11
R16			AC12
R17			AC13
R18			AC14
R19			AC15
R20			AC16
R21			AC17
R22			AC18
R23			AC19
R24			AC20
R25			AC21
T12			AC22
T14			AC23
T16			AC24
T18			AC25
T20			AD12
T22			AD14
T24			AD16
V11			AD18
V13			AD22
V15			W20
V17			

75 74 73 47 9 8 PP1V8_S0GPU_ISNS

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603

C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402

C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402

C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

OMIT

U8000
NB9P-GS
BGA
SYMBOL 7 OF 9

B18			J20
J17			J21
U27			J22
AB27			J23
AB29			J24
AC27			J29
AD27			N27
AE27			P27
AJ28			R27
E21	FBVDDQ	FBVDDQ	T27
G8			U29
G9			V27
G17			V29
G18			V34
G22			W27
H29			Y27
J14			AA27
J15			AA29
J16			AA31

U8000
NB9P-GS
BGA
SYMBOL 8 OF 9

B3			V18
B6			V20
B9			V22
B12			V24
B15			V31
B21			Y11
B24			Y13
B27			Y15
B30			Y17
B33			Y19
C2			Y21
C34			Y23
E6			Y25
E9			AA2
E12			AA5
E15			AA11
E18			AA12
E24			AA13
E27			AA14
E30			AA15
F2			AA16
F5			AA17
F31			AA18
F34			AA19
J2			AA20
J5			AA21
J31			AA22
J34			AA23
L9			AA24
M2			AA25
M5			AA34
M11			AB12
M13			AB14
M15			AB16
M17			AB18
M19			AB20
M21			AB22
M23			AB24
M25			AC9
M31			AD2
M34			AD5
N11			AD11
N12			AD13
N13			AD15
N14			AD17
N15			AD21
N16			AD23
N17	GND	GND	AD25
N18			AD31
N19			AD34
N20			AE11
N21			AE12
N22			AE13
N23			AE14
N24			AE15
N25			AE16
P12			AE17
P14			AE18
P16			AE19
P18			AE20
P20			AE21
P22			AE22
P24			AE23
R2			AE24
R5			AE25
R31			AG2
R34			AG5
T11			AG31
T13			AG34
T15			AK2
T17			AK5
T19			AP33
T21			AK31
T23			AK34
T25			AL6
U11			AL9
U12			AL12
U13			AL15
U14			AL18
U15			AL21
U16			AL24
U17			AL27
U18			AL30
U19			AN2
U20			AN34
U21			AP3
U22			AP6
U23			AP9
U24			AP12
U25			AP15
V2			AP18
V5			AP21
V9			AP24
V12			AP27
V14			AP30
V16			

NV G96 Core/FB Power

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 72 OF 97	

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8000
NB9P-GS
BGA
SYMBOL 3 OF 9

OMIT
U8000
NB9P-GS
BGA
SYMBOL 4 OF 9

FB_A_DQ<0> R30
FB_A_DQ<1> R32
FB_A_DQ<2> P31
FB_A_DQ<3> N30
FB_A_DQ<4> L31
FB_A_DQ<5> M32
FB_A_DQ<6> M30
FB_A_DQ<7> L30
FB_A_DQ<8> P33
FB_A_DQ<9> P34
FB_A_DQ<10> N35
FB_A_DQ<11> P35
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FB_A_DQ<13> L33
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FB_A_DQ<25> K35
FB_A_DQ<26> K33
FB_A_DQ<27> G34
FB_A_DQ<28> K34
FB_A_DQ<29> E33
FB_A_DQ<30> E34
FB_A_DQ<31> G33
FB_A_DQ<32> AG30
FB_A_DQ<33> AH31
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FB_A_DQ<53> AK30
FB_A_DQ<54> AJ30
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FBA_D2 U31 FB_A_LMA<5>
FBA_D3 Y32 FB_A_BA<1>
FBA_D4 AB35 FB_A_UMA<2>
FBA_D5 AB34 FB_A_UMA<4>
FBA_D6 W35 FB_A_UMA<3>
FBA_D7 W33 NC_FB_A_CS1_L
FBA_D8 W30 FB_A_CS0_L
FBA_D9 T34 FB_A_MA<11>
FBA_D10 T35 FB_A_CAS_L
FBA_D11 AB31 FB_A_WE_L
FBA_D12 Y30 FB_A_BA<0>
FBA_D13 Y34 FB_A_UMA<5>
FBA_D14 W32 FB_A_MA<12>
FBA_D15 AA30 FB_A_DRAM_RST
FBA_D16 AA32 FB_A_MA<7>
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FBA_D23 V30 FB_A_MA<8>
FBA_D24 U35 FB_A_LMA<3>
FBA_D25 U30 FB_A_MA<1>
FBA_D26 U33 NC_FBA_MA<13>
FBA_D27 AB30 FB_A_BA<2>
FBA_D28 AB33 NC_FBA_CMD28
FBA_D29 T33 NC_FBA_CMD29
FBA_D30 W29 NC_FBA_CMD30
FBA_D31

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FBA_CLK0* T31 FB_A_CLK_N<0>
FBA_CLK1 AC31 FB_A_CLK_P<1>
FBA_CLK1* AC30 FB_A_CLK_N<1>

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FBA_DQM1 P32 FB_A_DQM_L<1>
FBA_DQM2 J30 FB_A_DQM_L<2>
FBA_DQM3 H34 FB_A_DQM_L<3>
FBA_DQM4 AF32 FB_A_DQM_L<4>
FBA_DQM5 AF35 FB_A_DQM_L<5>
FBA_DQM6 AL32 FB_A_DQM_L<6>
FBA_DQM7 AL34 FB_A_DQM_L<7>

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FBA_DQS_WP1 L34 FB_A_WDQS<1>
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FBA_DQS_WP5 AC33 FB_A_WDQS<5>
FBA_DQS_WP6 AJ32 FB_A_WDQS<6>
FBA_DQS_WP7 AJ34 FB_A_WDQS<7>

FB_DLLAVDD0 AG27
FB_PLLAVDD0 AF27

FBA_DEBUG T30 FBA_DEBUG

FB_CAL_PD_VDDQ K27 FBCAL_PD_VDDQ
FB_CAL_PU_GND L27 FBCAL_PU_GND
FB_CAL_TERM_GND M27 FBCAL_TERM_GND

FBA_RFU0 P29 NC
FBA_RFU1* N29 NC
FBA_RFU2 L29 NC
FBA_RFU3* M29 NC
FBA_RFU4 AD29 NC
FBA_RFU5* AE29 NC
FBA_RFU6 AG29 NC
FBA_RFU7* AH29 NC

R8200 10K 5% 1/16W MF-LF 402
R8201 10K 5% 1/16W MF-LF 402
R8292 40.2 1% 1/16W MF-LF 402
R8291 33.2 1% 1/16W MF-LF 402
R8293 60.4 1% 1/16W MF-LF 402
R8290 48.7 1% 1/16W MF-LF 402

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PLACEMENT_NOTE=Place close to U8000.
PLACEMENT_NOTE=Place close to U8000.

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L8200 FERR-220-OHM 0402
PP1V1_GPU_FBPLLAVDD0_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V
C8202 0.1UF 20% 10V CERM 402
C8201 0.1UF 20% 10V CERM 402
C8200 1UF 10% 6.3V CERM 402
PP1V8_S0GPU_ISNS

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FBC_D1 E11 FB_B_DQ<1>
FBC_D2 F10 FB_B_DQ<2>
FBC_D3 D8 FB_B_DQ<3>
FBC_D4 F8 FB_B_DQ<4>
FBC_D5 F9 FB_B_DQ<5>
FBC_D6 E8 FB_B_DQ<6>
FBC_D7 F12 FB_B_DQ<7>
FBC_D8 B11 FB_B_DQ<8>
FBC_D9 C13 FB_B_DQ<9>
FBC_D10 A11 FB_B_DQ<10>
FBC_D11 B8 FB_B_DQ<11>
FBC_D12 A8 FB_B_DQ<12>
FBC_D13 C8 FB_B_DQ<13>
FBC_D14 C11 FB_B_DQ<14>
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FBC_D20 F16 FB_B_DQ<20>
FBC_D21 E16 FB_B_DQ<21>
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FBC_D34 E25 FB_B_DQ<34>
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FBC_CMD8 G21 FB_B_CS0_L
FBC_CMD9 F20 FB_B_MA<11>
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FBC_CMD11 F23 FB_B_WE_L
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FBC_CMD16 C25 FB_B_MA<7>
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FBC_CMD19 B22 FB_B_MA<0>
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FBC_CMD21 D22 FB_B_MA<6>
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FBC_CMD23 E19 FB_B_MA<8>
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FBC_CMD26 C19 NC_FBB_MA<13>
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FBC_CMD29 B20 NC_FBC_CMD29
FBC_CMD30 A20 NC_FBC_CMD30
FBC_D31

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FBC_DQM2 D15 FB_B_DQM_L<2>
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FBC_DQM4 D27 FB_B_DQM_L<4>
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FBC_DQS_WP4 E26 FB_B_WDQS<4>
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FB_DLLAVDD1 J19
FB_PLLAVDD1 J18

FBC_DEBUG G19 FBC_DEBUG
FB_VREF J27 GPU_FB_VREF

FBC_RFU0 G11 NC
FBC_RFU1* G12 NC
FBC_RFU2 G14 NC
FBC_RFU3* G15 NC
FBC_RFU4 G24 NC
FBC_RFU5* G25 NC
FBC_RFU6 G27 NC
FBC_RFU7* G28 NC

R8250 10K 5% 1/16W MF-LF 402
R8251 10K 5% 1/16W MF-LF 402
R8294 60.4 1% 1/16W MF-LF 402
R8295 1.07K 1% 1/16W MF-LF 402
R8296 2.49K 1% 1/16W MF-LF 402
R8297 1.02K 1% 1/16W MF-LF 402

PP1V1_S0GPU_REG
L8290 FERR-220-OHM 0402
PP1V1_GPU_FBPLLAVDD1_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V
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C8291 0.1UF 20% 10V CERM 402
C8292 1UF 10% 6.3V CERM 402
PP1V8_S0GPU_ISNS

NO STUFF
C8296 0.1UF 10% 16V X5R 402

GPU_FB_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

NO STUFF
Q8295 SSM6N15FEAPE SOT563

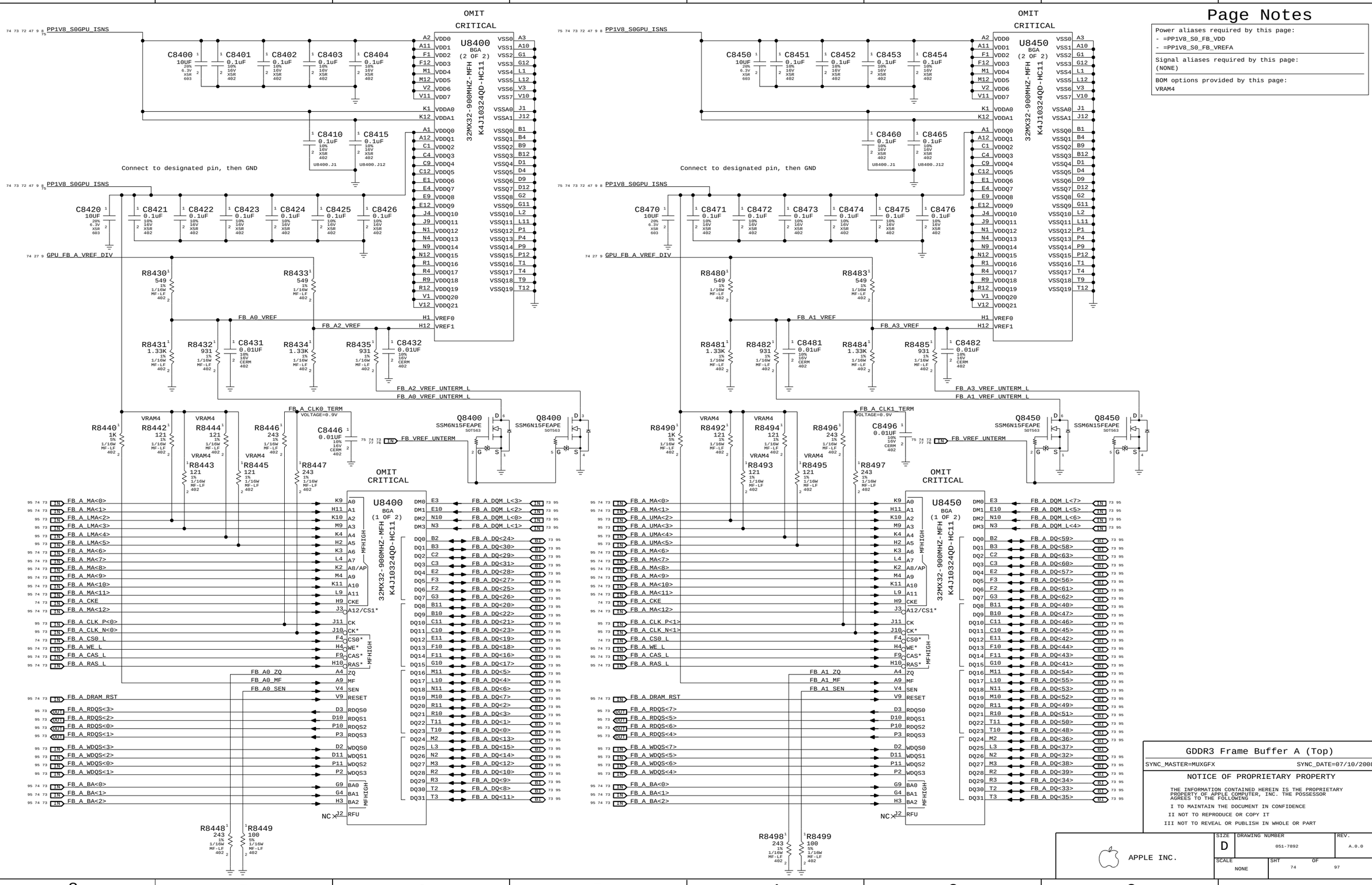
FB_VREF_UNTERM

NV G96 Frame Buffer I/F

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 73 OF 97	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U8400
BGA
(2 OF 2)
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K4J10324QD-HC11
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C8401 0.1uF
C8402 0.1uF
C8403 0.1uF
C8404 0.1uF
C8410 0.1uF
C8415 0.1uF
Connect to designated pin, then GND
C8420 10UF
C8421 0.1uF
C8422 0.1uF
C8423 0.1uF
C8424 0.1uF
C8425 0.1uF
C8426 0.1uF
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R8433 549
FB_A0_VREF
FB_A2_VREF
R8431 1.33K
R8432 931
C8431 0.01UF
R8434 1.33K
R8435 931
C8432 0.01UF
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FB_A0_VREF_UNTERM_L
FB_A_CLK0_TERM
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R8444 121
R8446 243
R8443 121
R8445 121
R8447 243
C8446 0.01UF
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Q8400 SSM6N15FEAPE
OMIT
CRITICAL
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FB_A0_SEN
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R8449 100
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OMIT
CRITICAL
U8450
BGA
(2 OF 2)
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K4J10324QD-HC11
PP1V8_S0GPU_ISNS
C8450 10UF
C8451 0.1uF
C8452 0.1uF
C8453 0.1uF
C8454 0.1uF
C8460 0.1uF
C8465 0.1uF
Connect to designated pin, then GND
C8470 10UF
C8471 0.1uF
C8472 0.1uF
C8473 0.1uF
C8474 0.1uF
C8475 0.1uF
C8476 0.1uF
GPU_FB_A_VREF_DIV
R8480 549
R8483 549
FB_A1_VREF
FB_A3_VREF
R8481 1.33K
R8482 931
C8481 0.01UF
R8484 1.33K
R8485 931
C8482 0.01UF
FB_A3_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L
FB_A_CLK1_TERM
VOLTAGE=0.9V
R8490 1K
R8492 121
R8494 121
R8496 243
R8493 121
R8495 121
R8497 243
C8496 0.01UF
FB_VREF_UNTERM
Q8450 SSM6N15FEAPE
OMIT
CRITICAL
FB_A_MA<0>
FB_A_MA<1>
FB_A_UMA<2>
FB_A_UMA<3>
FB_A_UMA<4>
FB_A_UMA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE
FB_A_MA<12>
FB_A_CLK_P<1>
FB_A_CLK_N<1>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L
FB_A_DRAM_RST
FB_A_RDQS<7>
FB_A_RDQS<5>
FB_A_RDQS<6>
FB_A_RDQS<4>
FB_A_WDQS<7>
FB_A_WDQS<5>
FB_A_WDQS<6>
FB_A_WDQS<4>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN
R8498 243
R8499 100
FB_A_DQM_L<7>
FB_A_DQM_L<5>
FB_A_DQM_L<6>
FB_A_DQM_L<4>
FB_A_DQ<59>
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FB_A_DQ<33>
FB_A_DQ<35>
Page Notes
Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
VRAM4
GDDR3 Frame Buffer A (Top)
SYNC_MASTER=MUXGFX
SYNC_DATE=07/10/2008
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SIZE D
DRAWING NUMBER 051-7892
REV. A.0.0
SCALE NONE
SHT 74 OF 97

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

OMIT
CRITICAL

U8500
BGA
(2 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11

U8550
BGA
(2 OF 2)
32MX32-900MHZ-MFH
K4J10324QD-HC11

Connect to designated pin, then GND

PP1V8_S0GPU_ISNS

GPU_FB_B_VREF_DIV

FB_B0_VREF
FB_B2_VREF
FB_B2_VREF_UNTERM_L
FB_B0_VREF_UNTERM_L

FB_B1_VREF
FB_B3_VREF
FB_B3_VREF_UNTERM_L
FB_B1_VREF_UNTERM_L

FB_B_CLK0_TERM
VOLTAGE=0.9V

FB_B_CLK1_TERM
VOLTAGE=0.9V

FB_VREF_UNTERM

Q8500
SSM6N15FEAPE
SOT563

Q8550
SSM6N15FEAPE
SOT563

MFHIGH

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FB_B_CKE
FB_B_MA<12>
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FB_B_CLK_N<0>
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FB_B_WE_L
FB_B_CAS_L
FB_B_RAS_L
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FB_B_WDQS<3>
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FB_B_BA<2>

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FB_B0_MF
FB_B0_SEN

FB_B1_ZQ
FB_B1_MF
FB_B1_SEN

FB_B_DQM_L<1>
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FB_B_DQM_L<2>
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FB_B_DQ<58>
FB_B_DQ<62>
FB_B_DQ<61>
FB_B_DQ<60>

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE D | DRAWING NUMBER 051-7892 | REV. A.0.0

SCALE NONE | SHT 75 OF 97

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

110mA
81 79 77 76 70 69 8 6 PP3V3_S0GPU

C8690 0.022UF 10% 16V CERM-X5R 402
C8692 0.022UF 10% 16V CERM-X5R 402
C8694 0.1UF 20% 10V CERM 402
C8696 0.47UF 10% 6.3V CERM-X5R 402
C8698 1UF 10% 6.3V CERM 402
C8691 0.022UF 10% 16V CERM-X5R 402
C8693 0.022UF 10% 16V CERM-X5R 402
C8695 0.1UF 20% 10V CERM 402
C8697 0.47UF 10% 6.3V CERM-X5R 402

76 70 69 8 6 81 79 77 PP3V3_S0GPU
Typically <??mA
C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

81 79 77 76 70 69 8 6 PP3V3_S0GPU

R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ 76
GPU_MIOB_PD_VDDQ 76
GPU_MIOA_PU_GND 76
GPU_MIOB_PU_GND 76
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1UF 10% 16V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1UF 10% 16V X5R 402
R8660 10K 5% 1/16W MF-LF 402

C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

83 78 76 73 71 8 PP1V1_S0GPU_REG
L8630 FERR-220-OHM 0402
PP1V1_GPU_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
65mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1UF 10% 16V X5R 402

83 78 76 73 71 8 PP1V1_S0GPU_REG
L8635 FERR-220-OHM 0402
PP1V1_GPU_H_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
25mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1UF 10% 16V X5R 402

83 78 76 73 71 8 PP1V1_S0GPU_REG
L8640 FERR-220-OHM 0402
PP1V1_GPU_VID_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
50mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1UF 10% 16V X5R 402

OMIT
U8000
NB9P-GS
BGA
SYMBOL 6 OF 9

J9	VDD33_1		
J10	VDD33_2		
J11	VDD33_3		
J12	VDD33_4		
J13	VDD33_5		
J25	RFU0	NC	
J26	RFU1	NC	
AK14	RFU0_GND		
K9	RFU1_GND		
C3	ROM_CS*	77	NC_GPU_ROM_CS_L
D4	ROM_SCLK	77	GPU_ROM_SCLK
D3	ROM_SI	77	GPU_ROM_SI
C4	ROM_SO	77	GPU_ROM_SO
N9	STRAP_REF_3V3		GPU_STRAP_REF_3V3_PD
M9	STRAP_REF_MIOB		GPU_STRAP_REF_MIOB_PD (IPD)
P9	MIOA_VDDQ_1		
R9	MIOA_VDDQ_2		
T9	MIOA_VDDQ_3		
U9	MIOA_VDDQ_4		
AA9	MIOB_VDDQ_1		
AB9	MIOB_VDDQ_2		
W9	MIOB_VDDQ_3		
Y9	MIOB_VDDQ_4		
AP35	TESTMODE		GPU_TESTMODE_PD
N5	MIOA_VREF		GPU_MIOA_VREF
AF1	MIOB_VREF		GPU_MIOB_VREF
U5	MIOA_CAL_PD_VDDQ	76	GPU_MIOA_PD_VDDQ
T5	MIOA_CAL_PU_GND	76	GPU_MIOA_PU_GND
AA7	MIOB_CAL_PD_VDDQ	76	GPU_MIOB_PD_VDDQ
AA6	MIOB_CAL_PU_GND	76	GPU_MIOB_PU_GND
AF9	SP_PLLVDD		
AE9	PLLVDD		
AD9	VID_PLLVDD		
B1	XTAL_IN	95 77 IN	GPU_CLK27M
B2	XTAL_OUT	77 OUT	GPU_XTALOUT
D1	XTAL_OUTBUFF	77 OUT	GPU_XTALOUTBUFF
D2	XTAL_SSIN	95 77 IN	GPU_CLK27M_SS

K1	GPIO0		NC_GPU_GPIO_0 B1 77
K2	GPIO1		DP_EG_HPD B1 77 81
K3	GPIO2		TP_LVDS_EG_BKL_PWM B1 77
H3	GPIO3		EG_LCD_PWR_EN B1 77 84
H2	GPIO4		EG_BKLT_EN B1 77 84
H1	GPIO5		TP_GPU_GSTATE<0> B1 77
H4	GPIO6		GPU_GPIO_6 B1 77
H5	GPIO7		GPIO7_FBVDD_ALTVQ B1 77 83
H6	GPIO8		SMC_GFX_OVERTEMP_R_L B1 77
J7	GPIO9		SMC_GFX_THROTTLE_R_L B1 77
K4	GPIO10		FB_VREF_UNTERM B1 73 74 75 77
K5	GPIO11		GPU_VCORE_VID0 B1 77 79
H7	GPIO12		GPU_VCORE_VID1 B1 77 79
J4	GPIO13		GPU_VCORE_VID2 B1 77 79
J6	GPIO14		TP_GPU_VCORE_VID3 B1 77
L1	GPIO15		NC_GPU_GPIO_15 B1 77
L2	GPIO16		GPU_GPIO_16 B1 77
L4	GPIO17		NC_GPU_GPIO_17 B1 77
M4	GPIO18		NC_GPU_GPIO_18 B1 77
L7	GPIO19		NC_GPU_GPIO_19 B1 77
L5	GPIO20		NC_GPU_GPIO_20 B1 77
K6	GPIO21		NC_GPU_GPIO_21 B1 77
L6	GPIO22		NC_GPU_GPIO_22 B1 77
M6	GPIO23		NC_GPU_GPIO_23 B1 77
C7	HDA_SDI		NC_CPU_HDA_SDI OUT 77
B7	HDA_SDO		NC_CPU_HDA_SDO OUT 77
A7	HDA_SYNC		NC_CPU_HDA_SYNC OUT 77
D7	HDA_BCLK		NC_CPU_HDA_BCLK OUT 77
D6	HDA_RST*		NC_CPU_HDA_RST_L OUT 77
A5	SPDIF		NC_GPU_SPDIF IN 77
A4	BUFRST*		TP_GPU_BUFRST_L OUT
AP14	JTAG_TCK		JTAG_MCP_TCK IN 6 13 21
AN14	JTAG_TDI		GPU_JTAG_TDI IN 6
AN16	JTAG_TDO		TP_GPU_JTAG_TDO OUT 6
AR14	JTAG_TMS		GPU_JTAG_TMS IN 6
AP16	JTAG_TRST*		JTAG_MCP_TRST_L IN 6 13 21
N4	MIOA_CLKIN		NC_GPU_MIOA_CLKIN IN 77
R4	MIOA_CLKOUT		NC_GPU_MIOA_CLKOUT_P B1 77
T4	MIOA_CLKOUT*		NC_GPU_MIOA_CLKOUT_N B1 77
P5	MIOA_CTL3		NC_GPU_MIOA_CTL3 B1 77
N2	MIOA_DE		TP_GPU_MIOA_DE B1 77
N1	MIOA_D0		TP_GPU_MIOA_D<0> B1 77
P4	MIOA_D1		TP_GPU_MIOA_D<1> B1 77
P1	MIOA_D2		TP_GPU_MIOA_D<2> B1 77
P2	MIOA_D3		TP_GPU_MIOA_D<3> B1 77
P3	MIOA_D4		TP_GPU_MIOA_D<4> B1 77
T3	MIOA_D5		TP_GPU_MIOA_D<5> B1 77
T2	MIOA_D6		TP_GPU_MIOA_D<6> B1 77
T1	MIOA_D7		TP_GPU_MIOA_D<7> B1 77
U4	MIOA_D8		TP_GPU_MIOA_D<8> B1 77
U1	MIOA_D9		TP_GPU_MIOA_D<9> B1 77
U2	MIOA_D10		NC_GPU_MIOA_D<10> B1 77
U3	MIOA_D11		NC_GPU_MIOA_D<11> B1 77
R6	MIOA_D12		NC_GPU_MIOA_D<12> B1 77
T6	MIOA_D13		NC_GPU_MIOA_D<13> B1 77
N6	MIOA_D14		NC_GPU_MIOA_D<14> B1 77
N3	MIOA_HSYNC		NC_GPU_MIOA_HSYNC B1 77
L3	MIOA_VSYNC		NC_GPU_MIOA_VSYNC B1 77
AE1	MIOB_CLKIN		NC_GPU_MIOB_CLKIN IN 77
V4	MIOB_CLKOUT		NC_GPU_MIOB_CLKOUT_P B1 77
W4	MIOB_CLKOUT*		NC_GPU_MIOB_CLKOUT_N B1 77
W3	MIOB_CTL3		NC_GPU_MIOB_CTL3 B1 77
Y5	MIOB_DE		NC_GPU_MIOB_DE B1 77
Y1	MIOB_D0		NC_GPU_MIOB_D<0> B1 77
Y2	MIOB_D1		NC_GPU_MIOB_D<1> B1 77
Y3	MIOB_D2		NC_GPU_MIOB_D<2> B1 77
AB3	MIOB_D3		NC_GPU_MIOB_D<3> B1 77
AB2	MIOB_D4		NC_GPU_MIOB_D<4> B1 77
AB1	MIOB_D5		NC_GPU_MIOB_D<5> B1 77
AC4	MIOB_D6		NC_GPU_MIOB_D<6> B1 77
AC1	MIOB_D7		NC_GPU_MIOB_D<7> B1 77
AC2	MIOB_D8		NC_GPU_MIOB_D<8> B1 77
AC3	MIOB_D9		NC_GPU_MIOB_D<9> B1 77
AE3	MIOB_D10		NC_GPU_MIOB_D<10> B1 77
AE2	MIOB_D11		NC_GPU_MIOB_D<11> B1 77
U6	MIOB_D12		NC_GPU_MIOB_D<12> B1 77
W6	MIOB_D13		NC_GPU_MIOB_D<13> B1 77
Y6	MIOB_D14		NC_GPU_MIOB_D<14> B1 77
W5	MIOB_D15		GPU_STRAP<0> B1 77
W7	MIOB_D16		GPU_STRAP<1> B1 77
V7	MIOB_D17		GPU_STRAP<2> B1 77
W1	MIOB_HSYNC		NC_GPU_MIOB_HSYNC B1 77
W2	MIOB_VSYNC		NC_GPU_MIOB_VSYNC B1 77
B5	THERMDP		GPU_TDIODE_P IN 48 77 96
B4	THERMDN		GPU_TDIODE_N OUT 48 77 96
C5	PGOOD_OUT*		TP_GPU_PGOOD_OUT_L OUT

NV G96 GPIO/MIO/Misc

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 76 OF 97	

GPIOs

	Native Func	
NC_GPU_GPIO_0	GP	NC_GPU_GPIO_0
DP_EG_HPD	HPDC	DP_EG_HPD
TP_LVDS_EG_BKL_PWM	LCD0_BL_PWM	TP_LVDS_EG_BKL_PWM
EG_LCD_PWR_EN	LCD0_VDD	EG_LCD_PWR_EN
EG_BKLT_EN	LCD0_BL_EN	EG_BKLT_EN
TP_GPU_GSTATE<0>	VID0	TP_GPU_GSTATE<0>
GPU_GPIO_6	VID1	TP_GPU_GSTATE<1>
GPIO7_FBVDD_ALTVO	VID2/MEM_VID	GPIO7_FBVDD_ALTVO
SMC_GFX_OVERTEMP_R_L	THERM	SMC_GFX_OVERTEMP_R_L
SMC_GFX_THROTTLE_R_L	FAN_PWM	SMC_GFX_THROTTLE_R_L
FB_VREF_UNTERM	MEM_VREF	FB_VREF_UNTERM
GPU_VCORE_VID0	SLI_SYNC	GPU_VCORE_VID0
GPU_VCORE_VID1	AC_DET	GPU_VCORE_VID1
GPU_VCORE_VID2	PWR_CTL0	GPU_VCORE_VID2
TP_GPU_VCORE_VID3	PWR_CTL1	TP_GPU_VCORE_VID3

GPIOs

	Native Func	
NC_GPU_GPIO_15	HPDE	NC_GPU_GPIO_15
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET
NC_GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17
NC_GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18
NC_GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19
NC_GPU_GPIO_20	HPDD	NC_GPU_GPIO_20
NC_GPU_GPIO_21	HPDF	NC_GPU_GPIO_21
NC_GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22
NC_GPU_GPIO_23	GP	NC_GPU_GPIO_23

Renamed signals

GPU_XTALOUT	GPU_XTALOUT
GPU_CLK27M	GPU_CLK27M
GPU_CLK27M_SS	GPU_CLK27M_SS
GPU_TDIODE_P	GPU_TDIODE_P
GPU_TDIODE_N	GPU_TDIODE_N
LVDS_EG_DDC_CLK	LVDS_EG_DDC_CLK
LVDS_EG_DDC_DATA	LVDS_EG_DDC_DATA
DP_EG_DDC_CLK	DP_EG_DDC_CLK
DP_EG_DDC_DATA	DP_EG_DDC_DATA

Unused signals

NC_GPU_SPDIF	NC_GPU_SPDIF
NC_CPU_HDA_SDI	NC_CPU_HDA_SDI
NC_CPU_HDA_SD0	NC_CPU_HDA_SD0
NC_CPU_HDA_SYNC	NC_CPU_HDA_SYNC
NC_CPU_HDA_BCLK	NC_CPU_HDA_BCLK
NC_CPU_HDA_RST_L	NC_CPU_HDA_RST_L
NC_FBA_MA<13>	NC_FBA_MA<13>
NC_FBB_MA<13>	NC_FBB_MA<13>
NC_FBA_CMD28	NC_FBA_CMD28
NC_FBC_CMD28	NC_FBC_CMD28
NC_FBA_CMD29	NC_FBA_CMD29
NC_FBC_CMD29	NC_FBC_CMD29
NC_FBA_CMD30	NC_FBA_CMD30
NC_FBC_CMD30	NC_FBC_CMD30
NC_GPU_ROM_CS_L	NC_GPU_ROM_CS_L
NC_FB_A_CS1_L	NC_FB_A_CS1_L
NC_FB_B_CS1_L	NC_FB_B_CS1_L

Unused I2C Buses

NC_GPU_I2CC_SCL	NC_GPU_I2CC_SCL
NC_GPU_I2CC_SDA	NC_GPU_I2CC_SDA
NC_GPU_I2CD_SCL	NC_GPU_I2CD_SCL
NC_GPU_I2CD_SDA	NC_GPU_I2CD_SDA
NC_GPU_I2CE_SCL	NC_GPU_I2CE_SCL
NC_GPU_I2CE_SDA	NC_GPU_I2CE_SDA
NC_GPU_I2CH_SCL	NC_GPU_I2CH_SCL
NC_GPU_I2CH_SDA	NC_GPU_I2CH_SDA

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

TP_LVDS_EG_B_CLK_P	TP_LVDS_EG_B_CLK_P
TP_LVDS_EG_B_CLK_N	TP_LVDS_EG_B_CLK_N
NC_LVDS_EG_A_DATA_P<3>	NC_LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3>	NC_LVDS_EG_A_DATA_N<3>
NC_LVDS_EG_B_DATA_P<3>	NC_LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3>	NC_LVDS_EG_B_DATA_N<3>

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUT_P	NC_GPU_MIOA_CLKOUT_P
NC_GPU_MIOA_CLKOUT_N	NC_GPU_MIOA_CLKOUT_N
NC_GPU_MIOA_CTL3	NC_GPU_MIOA_CTL3
TP_GPU_MIOA_DE	TP_GPU_MIOA_DE
TP_GPU_MIOA_D<9..0>	GPU_MIOA_D<9..0>
NC_GPU_MIOA_CLKIN	NC_GPU_MIOA_CLKIN
NC_GPU_MIOA_D<14..10>	GPU_MIOA_D<14..10>
NC_GPU_MIOA_HSYNC	NC_GPU_MIOA_HSYNC
NC_GPU_MIOA_VSYNC	NC_GPU_MIOA_VSYNC
NC_GPU_MIOB_CLKIN	NC_GPU_MIOB_CLKIN
NC_GPU_MIOB_CLKOUT_P	NC_GPU_MIOB_CLKOUT_P
NC_GPU_MIOB_CLKOUT_N	NC_GPU_MIOB_CLKOUT_N
NC_GPU_MIOB_CTL3	NC_GPU_MIOB_CTL3
NC_GPU_MIOB_DE	NC_GPU_MIOB_DE
NC_GPU_MIOB_D<14..0>	GPU_MIOB_D<14..0>
NC_GPU_MIOB_VSYNC	NC_GPU_MIOB_VSYNC
NC_GPU_MIOB_HSYNC	NC_GPU_MIOB_HSYNC

Config Straps

PP3V3_S0GPU

R8707[1] 2.0K 5% 1/16W MF-LF 402 — OMIT
R8709[1] 4.99K 1% 1/16W MF-LF 402
R8711[1] 4.99K 1% 1/16W MF-LF 402 — NO STUFF

- GPU_ROM_SI (OUT)
- GPU_ROM_SO (IN)
- GPU_ROM_SCLK (IN)

R8708[1] 45.3K 1% 1/16W MF-LF 402 — OMIT
R8710[1] 2.0K 5% 1/16W MF-LF 402 — NO STUFF
R8712[1] 15.0K 1% 1/16W MF-LF 402

Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

Strap S1/S2 Bit[3:0] PU/PD Rval

0 0000 PD 5k
1 0001 PD 10k
2 0010 PD 15k
3 0011 PD 20k
4 0100 PD 25k
5 0101 PD 30k
6 0110 PD 35k
7 0111 PD 45k

Strap S1/S2 Bit[3:0] PU/PD Rval

8 1000 PU 5k
9 1001 PU 10k
A 1010 PU 15k
B 1011 PU 20k
C 1100 PU 25k
D 1101 PU 30k
E 1110 PU 35k
F 1111 PU 45k

PP3V3_S0GPU

R8701[1] 45.3K 1% 1/16W MF-LF 402 — NO STUFF
R8703[1] 10K 1% 1/16W MF-LF 402
R8705[1] 10K 1% 1/16W MF-LF 402 — NO STUFF

- GPU_STRAP<0> (BI)
- GPU_STRAP<1> (BI)
- GPU_STRAP<2> (BI)

R8702[1] 2.0K 5% 1/16W MF-LF 402 — NO STUFF
R8704[1] 10K 1% 1/16W MF-LF 402
R8706[1] 45.3K 1% 1/16W MF-LF 402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8708		VRAM_512_QIMONDA
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8707		VRAM_1024_QIMONDA

G96 HDCP ROM APN is 341S2272, blank device is 335S0574.

GPU 27MHz Crystal

R8783 0 5% 1/16W MF-LF 402
GPU_CLK27M (IN) — GPU_CLK27M_XTALOUT_R
R8782[1] NO STUFF 10M 5% 1/16W MF-LF 402
GPU_XTALOUT (OUT)

CRITICAL Y8780 27MHz SM-2 — NC, NC

C8780 12pF 5% 50V CERM 402
C8781 12pF 5% 50V CERM 402

Unused Clocks

GPU_CLK27M_SS
GPU_XTALOUTBUFF

R8780[1] 10K 5% 1/16W MF-LF 402 — GPU_SS_INT
R8781[1] 10K 5% 1/16W MF-LF 402

Isolation FETs for DP MUX inputs

PP3V3_S0GPU

R8742[1] 100K 1% 1/16W MF-LF 402
DP_CA_DET_EG_FET — Q8742 SOD-VESM-HF SSM3K15FV
EG_DP_CA_DET — DP_CA_DET (IN)

R8743 0 5% 1/16W MF-LF 402
DP_CA_DET_EG (IN)
DP_CA_DET_EG_PLD

PP3V3_S0
PP3V3_S0GPU

R8750[1] 4.7K 5% 1/16W MF-LF 402
R8751[1] 4.7K 5% 1/16W MF-LF 402
R8752[1] 4.7K 5% 1/16W MF-LF 402
R8753[1] 4.7K 5% 1/16W MF-LF 402

- DP_EG_DDC_CLK (IN)
- DP_EG_DDC_DATA (BI)
- DP_IG_DDC_CLK (IN)
- DP_IG_DDC_DATA (BI)

PP3V3_S0GPU

R8796[1] 2.2K 5% 1/16W MF-LF 402
R8797[1] 2.2K 5% 1/16W MF-LF 402

R8798 0 5% 1/16W MF-LF 402 — SMC_GFX_OVERTEMP_R_L → SMC_GFX_OVERTEMP_L (OUT)
R8799 0 5% 1/16W MF-LF 402 — SMC_GFX_THROTTLE_R_L → SMC_GFX_THROTTLE_L (OUT)

- EG_LCD_PWR_EN (OUT)
- EG_BKLT_EN (OUT)
- GPIO7_FBVDD_ALTVO (OUT)
- FB_VREF_UNTERM (OUT)

R8792[1] 10K 5% 1/16W MF-LF 402
R8793[1] 10K 5% 1/16W MF-LF 402
R8794[1] 10K 5% 1/16W MF-LF 402
R8795[1] NO STUFF 10K 5% 1/16W MF-LF 402

G96 GPIOs & Straps

SYNC_MASTER=MUXGFX SYNC_DATE=07/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 77 OF 97	

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

78 8 PP1V8_GPUIFPX

L8800 FERR-220-OHM 0402
?mA peak per diff pair
?mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
Place at AG9
Place at AG10
PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402
80mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPEF_RSET 78
GPU_IFPCD_RSET 78
GPU_IFPAB_RSET 78

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

L8810 FERR-220-OHM 0402
?mA peak per diff pair
?mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
Place at AJ8
Place at AK8
PP1V1_GPU_IFPCD_IOVDD_F 78
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

83 76 73 71 8 PP1V1_S0GPU_REG

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

L8815 FERR-220-OHM 0402
160mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPCD_PLLVDD_F 78
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F 78
PP1V8_GPU_IFPEF_PLLVDD_F 78

Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

GPU_DACA_VDD
GPU_DACB_VDD
GPU_DACC_VDD

OMIT

U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

AG9	IFPA_IOVDD	IFPA_TXC	AM11
AG10	IFPB_IOVDD	IFPA_TXC*	AM12
AJ8	IFPC_IOVDD	IFPA_TXD0	AM8
AK8	IFPD_IOVDD	IFPA_TXD0*	AL8
AE7	IFPE_IOVDD	IFPA_TXD1	AM10
AD7	IFPF_IOVDD	IFPA_TXD1*	AM9
AK9	IFPAB_PLLVDD	IFPA_TXD2	AK10
AJ11	IFPAB_RSET	IFPA_TXD2*	AL10
AJ9	IFPCD_PLLVDD	IFPA_TXD3	AK11
AK7	IFPCD_RSET	IFPA_TXD3*	AL11
AJ6	IFPEF_PLLVDD	IFPB_TXC	AP13
AL1	IFPEF_RSET	IFPB_TXC*	AN13
G1	I2CA_SCL	IFPB_TXD4	AN8
G4	I2CA_SDA	IFPB_TXD4*	AP8
E3	I2CC_SCL	IFPB_TXD5	AP10
E4	I2CC_SDA	IFPB_TXD5*	AN10
E2	I2CS_SCL	IFPB_TXD6	AR11
E1	I2CS_SDA	IFPB_TXD6*	AR10
F6	I2CH_SCL	IFPB_TXD7	AN11
G6	I2CH_SDA	IFPB_TXD7*	AP11
G3	I2CB_SCL	IFPC_AUX	AP2
G2	I2CB_SDA	IFPC_AUX*	AN3
F4	I2CD_SCL	IFPC_L0	AM7
G5	I2CD_SDA	IFPC_L0*	AM6
D5	I2CE_SCL	IFPC_L1	AL5
E5	I2CE_SDA	IFPC_L1*	AM5
AJ12	DACA_VDD	IFPC_L2	AM3
AK12	DACA_VREF	IFPC_L2*	AM4
AK13	DACA_RSET	IFPC_L3	AP1
AC6	DACB_VDD	IFPC_L3*	AR2
AC5	DACB_VREF	IFPD_AUX	AP4
AB6	DACB_RSET	IFPD_AUX*	AN4
AG7	DACC_VDD	IFPD_L0	AR8
AK6	DACC_VREF	IFPD_L0*	AR7
AK7	DACC_RSET	IFPD_L1	AP7
		IFPD_L1*	AN7
		IFPD_L2	AN5
		IFPD_L2*	AP5
		IFPD_L3	AR5
		IFPD_L3*	AR4
		IFPE_AUX	AE4
		IFPE_AUX*	AD4
		IFPE_L0	AH6
		IFPE_L0*	AH5
		IFPE_L1	AH4
		IFPE_L1*	AG4
		IFPE_L2	AF4
		IFPE_L2*	AF5
		IFPE_L3	AE5
		IFPE_L3*	AE6
		IFPF_AUX	AF3
		IFPF_AUX*	AF2
		IFPF_L0	AL2
		IFPF_L0*	AL3
		IFPF_L1	AJ2
		IFPF_L1*	AJ3
		IFPF_L2	AJ1
		IFPF_L2*	AH1
		IFPF_L3	AH2
		IFPF_L3*	AH3
		DACA_RED	AM15
		DACA_GREEN	AM14
		DACA_BLUE	AL14
		DACA_HSYNC	AM13
		DACA_VSYNC	AL13
		DACB_RED	AA4
		DACB_GREEN	AB4
		DACB_BLUE	Y4
		DACB_CSYNC	AB5
		DACC_RED	AK4
		DACC_GREEN	AL4
		DACC_BLUE	AJ4
		DACC_HSYNC	AN1
		DACC_VSYNC	AM2

NC_GPU_I2CC_SCL
NC_GPU_I2CC_SDA
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
NC_GPU_I2CH_SDA
NC_GPU_I2CH_SCL
DP_EG_DDC_CLK
DP_EG_DDC_DATA
NC_GPU_I2CD_SCL
NC_GPU_I2CD_SDA
NC_GPU_I2CE_SCL
NC_GPU_I2CE_SDA
LVDS_EG_DDC_CLK
LVDS_EG_DDC_DATA

LVDS_EG_A_CLK_P
LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>
LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>
LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>
LVDS_EG_A_DATA_N<2>
NC_LVDS_EG_A_DATA_P<3>
NC_LVDS_EG_A_DATA_N<3>
TP_LVDS_EG_B_CLK_P
TP_LVDS_EG_B_CLK_N
LVDS_EG_B_DATA_P<0>
LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>
LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>
LVDS_EG_B_DATA_N<2>
NC_LVDS_EG_B_DATA_P<3>
NC_LVDS_EG_B_DATA_N<3>
DP_EG_AUX_CH_P
DP_EG_AUX_CH_N
DP_EG_ML_P<0>
DP_EG_ML_N<0>
DP_EG_ML_P<1>
DP_EG_ML_N<1>
DP_EG_ML_P<2>
DP_EG_ML_N<2>
DP_EG_ML_P<3>
DP_EG_ML_N<3>

R8861 1K 5% 1/16W MF-LF 402
R8860 1K 5% 1/16W MF-LF 402 NO STUFF

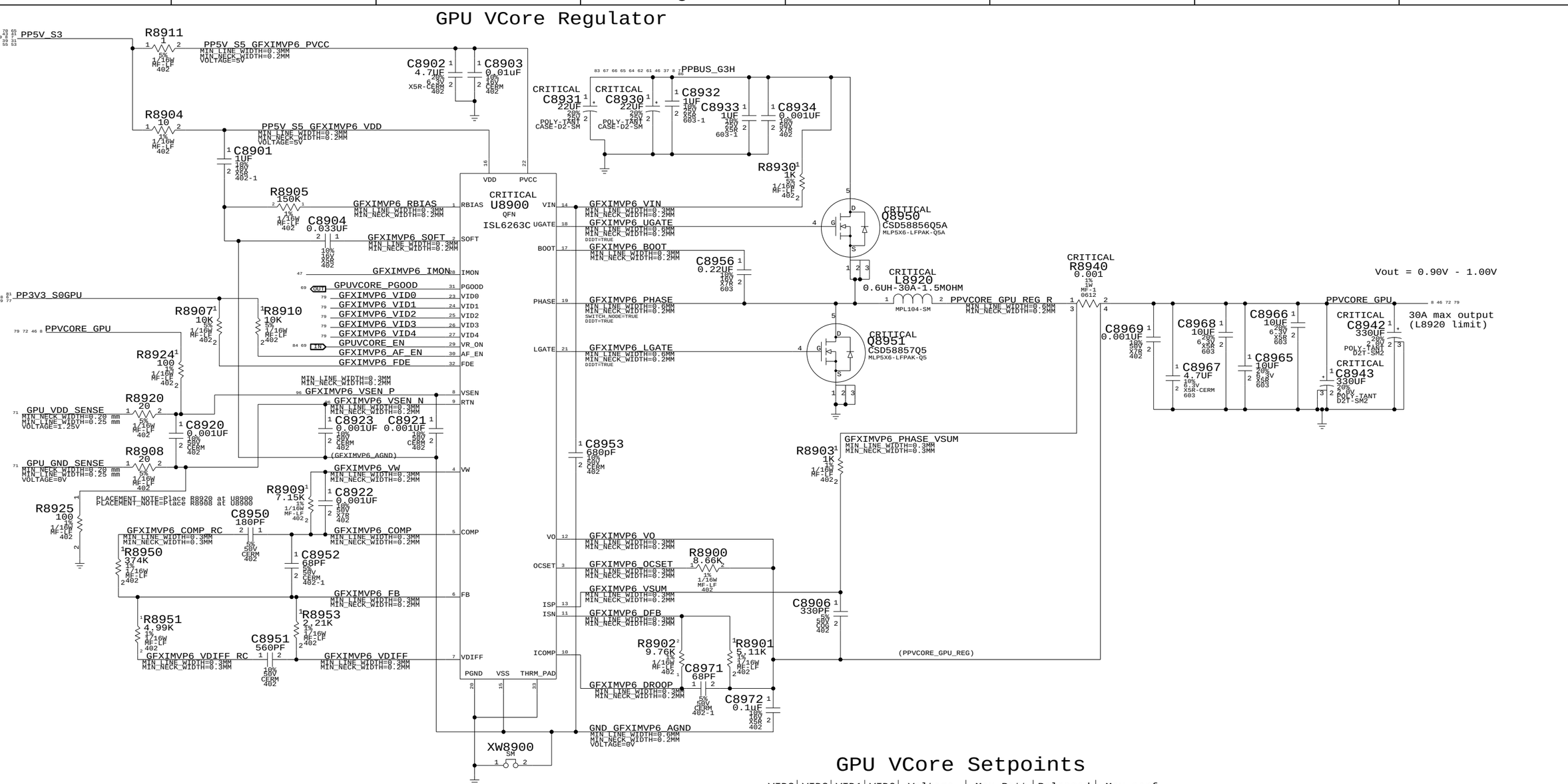
NV G96 Video Interfaces

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 78 OF 97	

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	K19		-
1	1	1	0	0.92700V	-	K19	-
1	0	1	1	1.00425V	-	-	K19

Other VID states may not be valid

K19 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

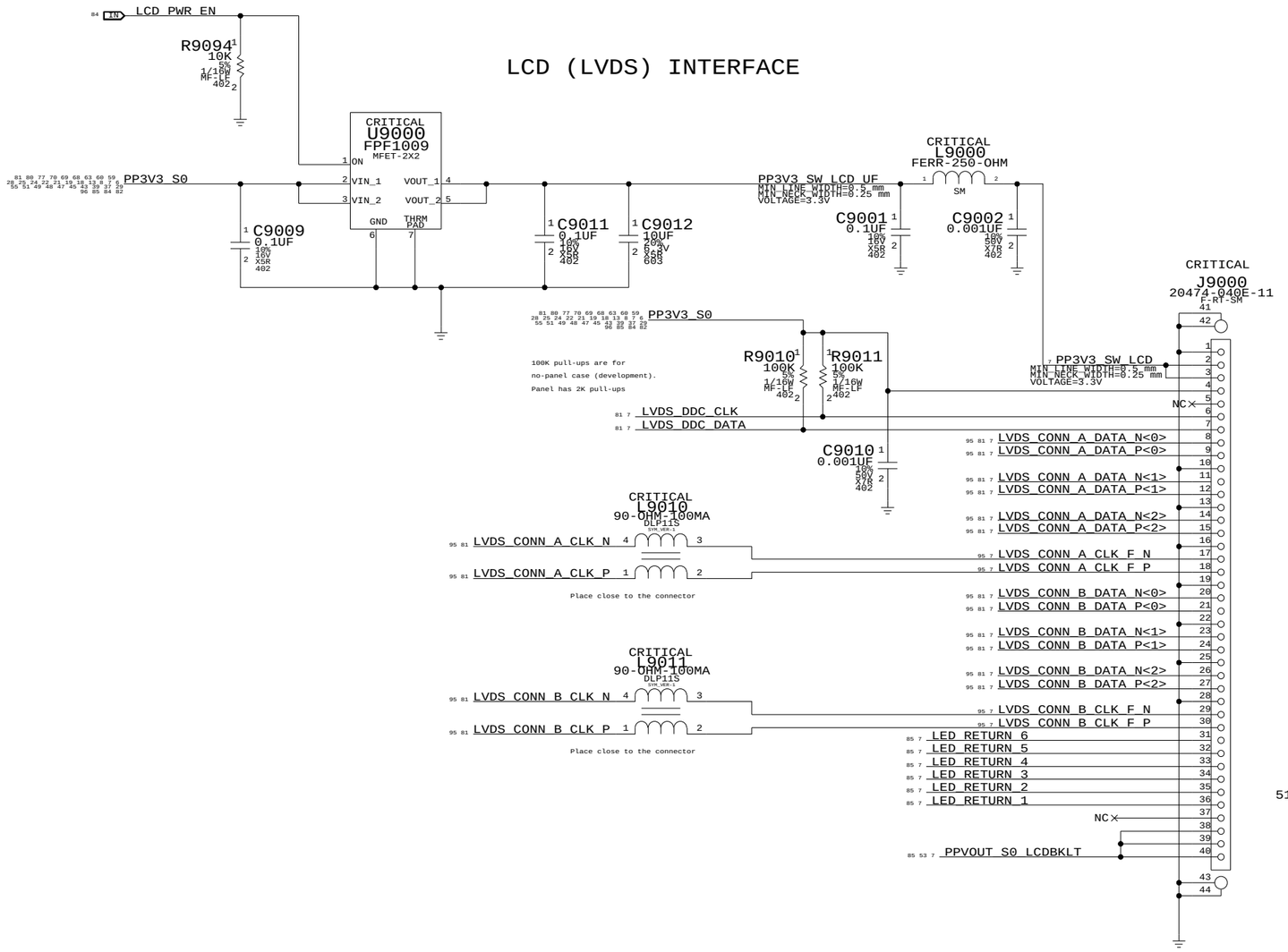
GPU (G96) CORE SUPPLY

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 79 OF 97	

LCD (LVDS) INTERFACE



518S0651

LVDS Display Connector

SYNC_MASTER=DDR SYNC_DATE=12/19/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 80 OF 97	

LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACEMENT_NOTE=Place at U9600 (All 24 resistors)

LVDS_A_CLK_P → OMIT R9320 270 1% 1/10W MF-LF 402 → LVDS_CONN_A_CLK_P
LVDS_A_CLK_N → OMIT R9322 270 1% 1/10W MF-LF 402 → LVDS_CONN_A_CLK_N
LVDS_A_DATA_P<0> → OMIT R9325 270 1% 1/10W MF-LF 402 → LVDS_CONN_A_DATA_P<0>
LVDS_A_DATA_N<0> → OMIT R9327 270 1% 1/10W MF-LF 402 → LVDS_CONN_A_DATA_N<0>
LVDS_A_DATA_P<1> → OMIT R9330 270 1% 1/10W MF-LF 402 → LVDS_CONN_A_DATA_P<1>
LVDS_A_DATA_N<1> → OMIT R9332 270 1% 1/10W MF-LF 402 → LVDS_CONN_A_DATA_N<1>
LVDS_A_DATA_P<2> → OMIT R9335 270 1% 1/10W MF-LF 402 → LVDS_CONN_A_DATA_P<2>
LVDS_A_DATA_N<2> → OMIT R9337 270 1% 1/10W MF-LF 402 → LVDS_CONN_A_DATA_N<2>
LVDS_B_CLK_P → OMIT R9340 270 1% 1/10W MF-LF 402 → LVDS_CONN_B_CLK_P
LVDS_B_CLK_N → OMIT R9342 270 1% 1/10W MF-LF 402 → LVDS_CONN_B_CLK_N
LVDS_B_DATA_P<0> → OMIT R9345 270 1% 1/10W MF-LF 402 → LVDS_CONN_B_DATA_P<0>
LVDS_B_DATA_N<0> → OMIT R9347 270 1% 1/10W MF-LF 402 → LVDS_CONN_B_DATA_N<0>
LVDS_B_DATA_P<1> → OMIT R9350 270 1% 1/10W MF-LF 402 → LVDS_CONN_B_DATA_P<1>
LVDS_B_DATA_N<1> → OMIT R9352 270 1% 1/10W MF-LF 402 → LVDS_CONN_B_DATA_N<1>
LVDS_B_DATA_P<2> → OMIT R9355 270 1% 1/10W MF-LF 402 → LVDS_CONN_B_DATA_P<2>
LVDS_B_DATA_N<2> → OMIT R9357 270 1% 1/10W MF-LF 402 → LVDS_CONN_B_DATA_N<2>

GMUX_2V5 R9321 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
GMUX_2V5 R9326 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
GMUX_2V5 R9331 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
GMUX_2V5 R9336 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
GMUX_2V5 R9341 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
GMUX_2V5 R9346 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
GMUX_2V5 R9351 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
GMUX_2V5 R9356 133 1% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0517	16	RES,MTL FILM,270 OHM,1%,1/16W,0402,SMD,L			GMUX_2V5
114S0174	16	RES,MTL FILM,1/16W,357 OHM,1,0402,SMD,LF			GMUX_1V8

DisplayPort Mux

PP3V3_S0

MUXGFX C9320 0.1UF 20% 16V CERM 402
MUXGFX C9321 0.1UF 20% 16V CERM 402

MUXGFX U9320 CBTL06141EE BGA CRITICAL
SIGNAL_MODEL=DPMUX

DP_IG_ML_P<0>	B4	DIN1_0+	DOUT_0+ B2 → DP_ML_P<0>
DP_IG_ML_N<0>	A4	DIN1_0-	DOUT_0- B1 → DP_ML_N<0>
DP_IG_ML_P<1>	B5	DIN1_1+	DOUT_1+ D2 → DP_ML_P<1>
DP_IG_ML_N<1>	A5	DIN1_1-	DOUT_1- D1 → DP_ML_N<1>
DP_IG_ML_P<2>	B6	DIN1_2+	DOUT_2+ E2 → DP_ML_P<2>
DP_IG_ML_N<2>	A6	DIN1_2-	DOUT_2- E1 → DP_ML_N<2>
DP_IG_ML_P<3>	A8	DIN1_3+	DOUT_3+ F2 → DP_ML_P<3>
DP_IG_ML_N<3>	A9	DIN1_3-	DOUT_3- F1 → DP_ML_N<3>
DP_IG_AUX_CH_P	H9	DAUX1+	AUX+ H2 → DP_AUX_CH_C_P
DP_IG_AUX_CH_N	J9	DAUX1-	AUX- H1 → DP_AUX_CH_C_N
DP_IG_DDC_CLK	H8	DDC_CLK1	
DP_IG_DDC_DATA	J8	DDC_DAT1	
DP_IG_HPD	J2	HPD_1	
DP_EG_ML_P<0>	B8	DIN2_0+	
DP_EG_ML_N<0>	B9	DIN2_0-	
DP_EG_ML_P<1>	D8	DIN2_1+	
DP_EG_ML_N<1>	D9	DIN2_1-	
DP_EG_ML_P<2>	E8	DIN2_2+	
DP_EG_ML_N<2>	E9	DIN2_2-	
DP_EG_ML_P<3>	F8	DIN2_3+	
DP_EG_ML_N<3>	F9	DIN2_3-	
DP_EG_AUX_CH_P	H6	DAUX2+	
DP_EG_AUX_CH_N	J6	DAUX2-	
DP_EG_DDC_CLK	H5	DDC_CLK2	
DP_EG_DDC_DATA	J5	DDC_DAT2	
DP_EG_HPD	H3	HPD_2	
DP_MUX_SEL_EG	A1	GPU_SEL	DDC_AUX_SEL C2 → DP_CA_DET (MAKE_BASE=TRUE)
DP_MUX_XSD_L	B7	XSD*	TST0 G2

LO=PORT1 HI=PORT2
LO=AUX_CH HI=DDC
GND: B3 C8 G8 H4 H7

C9330 0.1uF 10% 16V X5R 402 DP_IG_AUX_CH_C_P
C9331 0.1uF 10% 16V X5R 402 DP_IG_AUX_CH_C_N
C9335 0.1uF 10% 16V X5R 402 DP_EG_AUX_CH_C_P
C9336 0.1uF 10% 16V X5R 402 DP_EG_AUX_CH_C_N

R9304 100K 5% 1/16W MF-LF 402 (DP_IG_HPD)
R9305 100K 5% 1/16W MF-LF 402 (DP_EG_HPD)
R9306 1K 5% 1/16W MF-LF 402
R9307 1K 5% 1/16W MF-LF 402 HPDIN J1 ← DP_HPD_R ← DP_HOTPLUG_DET
R9301 10K 5% 1/16W MF-LF 402 DPMUX_EN_HPD
C9301 1UF 10% 6.3V CERM-X5R 402 DPMUX_EN_HPD
R9302 10K 5% 1/16W MF-LF 402 DPMUX_EN_PLD
R9303 0 5% 1/16W MF-LF 402 DP_MUX_EN ← PP3V3_S0 DPMUX_EN_S0&DPMUX_EN_PLD

DP_HOTPLUG_DET (MAKE_BASE=TRUE)
DP_CA_DET

PLACEMENT_NOTE=Place at U9320
MUXGFX

LVDS DDC MUX

PP3V3_S0GPU
PP3V3_S0

R9370 20K 5% 1/16W MF-LF 402
R9371 20K 5% 1/16W MF-LF 402
R9372 20K 5% 1/16W MF-LF 402
R9373 20K 5% 1/16W MF-LF 402
C9370 0.1UF 20% 10V CERM 402

U9370 SN74LV4066A QFN1

LVDS_DDC_SEL_EG	13	C1	A1 ↔ LVDS_EG_DDC_CLK
LVDS_DDC_SEL_IG	5	C2	A2 ↔ LVDS_IG_DDC_CLK
	6	C3	A3 ↔ LVDS_EG_DDC_DATA
	12	C4	A4 ↔ LVDS_IG_DDC_DATA
			B1 ↔ LVDS_DDC_CLK
			B2 ↔ LVDS_DDC_DATA
	14	VCC	
	7	GND	
	15	THRM	

Muxed Graphics Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=12/05/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 81 OF 97	

Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23
PP3V3_S5
PM_SLP_S3_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
TP_DPPWR_OC_L
C9480 10UF 20% 6.3V X5R 603
C9481 0.1UF 20% 10V CERM 402
C9485 0.1UF 20% 10V CERM 402
CRITICAL
C9486 22UF 20% 6.3V X5R CERM 603
L9400 FERR-120-OHM-3A 0603
C9400 0.01UF 20% 50V CERM 603
PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
R9420 100K 5% 1/10W MF-LF 402

DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8

R9400 NO STUFF 0 5% 1/16W MF-LF 402
R9430 NO STUFF 0 5% 1/16W MF-LF 402
R9401 NO STUFF 0 5% 1/16W MF-LF 402
R9431 NO STUFF 0 5% 1/16W MF-LF 402

HDMI_CEC

R9403 NO STUFF 0 5% 1/16W MF-LF 402
R9413 NO STUFF 0 5% 1/16W MF-LF 402
R9425 1M 5% 1/16W MF-LF 402

CRITICAL
J9400
DSPLYPRT-M97-1
F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
2	HOT_PLUG_DETECT	1 GND
4	CONFIG1	3 ML_LANE0P
6	CONFIG2	5 ML_LANE0N
8	GND	7 GND
10	ML_LANE3P	9 ML_LANE1P
12	ML_LANE3N	11 ML_LANE1N
14	GND	13 GND
16	AUX_CHP	15 ML_LANE2P
18	AUX_CHN	17 ML_LANE2N
20	DP_PWR	19 RETURN
SHIELD PINS		22 21

DP_ML_CONN_P<3>
DP_ML_CONN_N<3>
DP_ML_CONN_P<0>
DP_ML_CONN_N<0>
DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>

DP_ML_P<3> C9414 0.1uF 10% 16V X5R 402 DP_ML_C_P<3>
DP_ML_N<3> C9415 0.1uF 10% 16V X5R 402 DP_ML_C_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N

FL9403 12-OHM-100MA TCM1210-4SM
FL9401 12-OHM-100MA TCM1210-4SM
FL9400 12-OHM-100MA TCM1210-4SM
FL9402 12-OHM-100MA TCM1210-4SM

DP_ML_C_P<0> C9410 0.1uF 10% 16V X5R 402 DP_ML_P<0>
DP_ML_C_N<0> C9411 0.1uF 10% 16V X5R 402 DP_ML_N<0>
DP_ML_C_P<1> C9412 0.1uF 10% 16V X5R 402 DP_ML_P<1>
DP_ML_C_N<1> C9413 0.1uF 10% 16V X5R 402 DP_ML_N<1>
DP_ML_C_P<2> C9416 0.1uF 10% 16V X5R 402 DP_ML_P<2>
DP_ML_C_N<2> C9417 0.1uF 10% 16V X5R 402 DP_ML_N<2>

R9402 NO STUFF 0 5% 1/16W MF-LF 402
R9432 NO STUFF 0 5% 1/16W MF-LF 402

PP3V3_S0
R9443 100K 5% 1/10W MF-LF 402
R9442 100K 5% 1/10W MF-LF 402
DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q

R9421 100K 5% 1/10W MF-LF 402

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1

R9422 1M 5% 1/10W MF-LF 402

DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

PP3V3_S0
R9445 10K 5% 1/10W MF-LF 402
R9444 10K 5% 1/10W MF-LF 402
DP_HOTPLUG_DET
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q

R9423 100K 5% 1/10W MF-LF 402

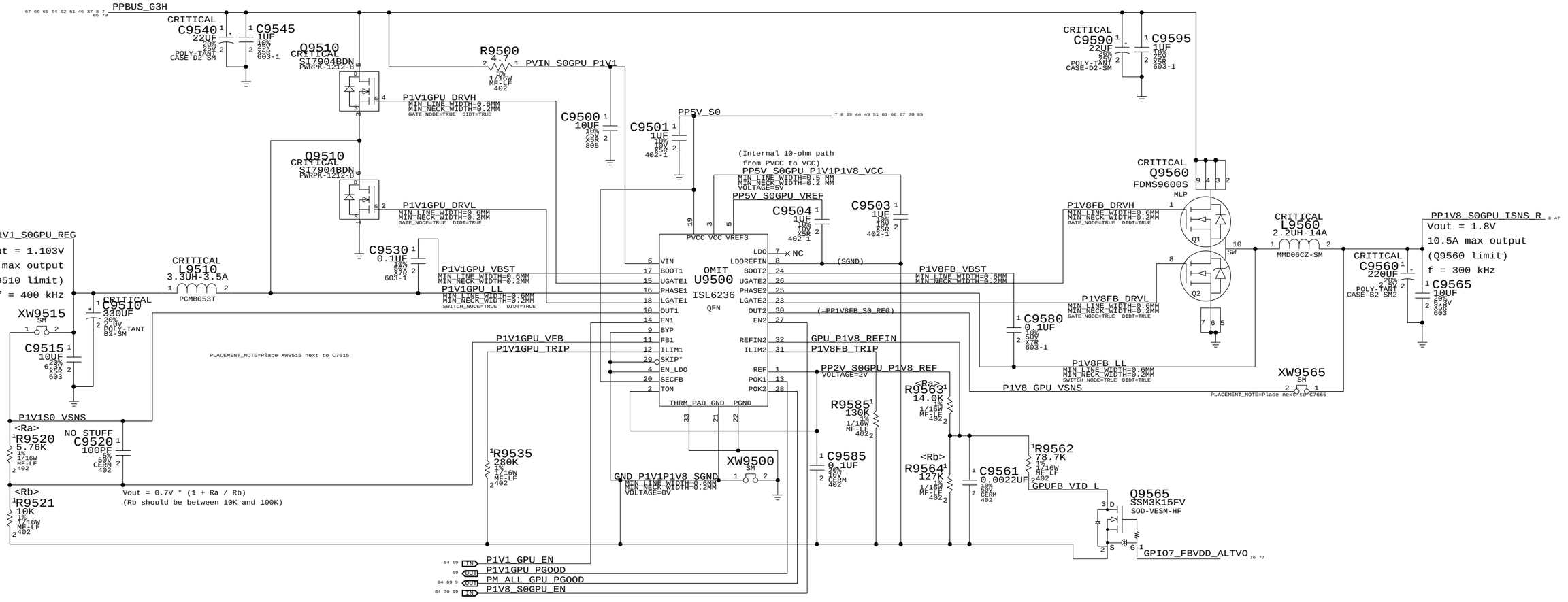
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

DisplayPort Connector

SYNC_MASTER=MUXGFX
SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 82 OF 97	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC,ISL6236,DUAL PWM CTRL,QFN32	U9500	CRITICAL	

1.1V / 1V8 FB Power Supply

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 83 OF 97	

GMUX CPLD

PP3V3_S0
C9610 0.1UF 20% 10V CERM 402
C9621 0.1UF 20% 10V CERM 402
C9622 0.1UF 20% 10V CERM 402
C9623 0.1UF 20% 10V CERM 402
C9624 0.1UF 20% 10V CERM 402
C9625 0.1UF 20% 10V CERM 402
C9626 0.1UF 20% 10V CERM 402
C9628 0.1UF 20% 10V CERM 402
C9629 0.1UF 20% 10V CERM 402
C9630 0.1UF 20% 10V CERM 402

PP1V8_S0
C9611 0.1UF 20% 10V CERM 402
C9612 0.1UF 20% 10V CERM 402
C9613 0.1UF 20% 10V CERM 402
C9614 0.1UF 20% 10V CERM 402
C9615 0.1UF 20% 10V CERM 402
C9616 0.1UF 20% 10V CERM 402
C9617 0.1UF 20% 10V CERM 402

PP1V2_S0
C9600 4.7UF 20% 6.3V X5R 402
C9604 0.1UF 20% 10V CERM 402
C9605 0.1UF 20% 10V CERM 402
C9606 0.1UF 20% 10V CERM 402
C9607 0.1UF 20% 10V CERM 402
C9608 0.1UF 20% 10V CERM 402
C9609 0.1UF 20% 10V CERM 402

PP3V3_S0
L9631 FERR-220-OHM
PP3V3_S0_ULC_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V 0402
C9631 0.1UF 20% 10V CERM 402
L9627 FERR-220-OHM
PP3V3_S0_LRC_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V 0402
C9627 0.1UF 20% 10V CERM 402

R9640 10K 1% 1/16W MF-LF 402
R9645 10K 1% 1/16W MF-LF 402
NO STUFF R9641 10K 1% 1/16W MF-LF 402
NO STUFF R9646 10K 1% 1/16W MF-LF 402
NO STUFF R9647 10K 1% 1/16W MF-LF 402

VCC: B11 C4 J3 J13 N11 P8
VCCAUX: C11 J2 J14 M8
VCCIO0 B5
VCCIO1 B7
VCCIO2 A12 C14 F13
VCCIO3 M12 M9
VCCIO4 M3
VCCIO5 N5
VCCIO6 M1
VCCIO7 C3 F2
VCCJ K12
ULC_VCCPLL A4
LRC_VCCPLL P11

OMIT CRITICAL

U9600
XP28
CSBGA-HF

JTAG_GMUX_TCK	IN	K14	TCK	
JTAG_GMUX_TDI	IN	L13	TDI	
JTAG_GMUX_TDO	OUT	K13	TDO	
JTAG_GMUX_TMS	IN	L12	TMS	
GMUX_TOE		K2	TOE	
GMUX_CFG0		K1	CFG0	
LCD_BKLT_EN	OUT	P2	PB2A	BANK5
LCD_BKLT_PWM	OUT	N2	PB2B	
LVDS_DDC_SEL_EG	OUT	P4	PB14A	
LVDS_DDC_SEL_IG	OUT	N4	PB14B	
DP_MUX_EN	OUT	N3	PB15A (OD)	
DP_MUX_SEL_EG	OUT	M4	PB15B	
EG_RESET_L	OUT	P5	PB16A	
EG_RAIL1_EN	OUT	M5	PB16B	
EG_RAIL2_EN	OUT	P6	PB17A	
EG_RAIL3_EN	OUT	M6	PB17B	
EG_RAIL4_EN	OUT	P7	PB18A	
EG_CLKREQ_OUT_L	OUT	M7	PB18B (OD)	
DP_CA_DET_EG	OUT	N7	PB19A	
LCD_PWR_EN	OUT	N8	PB19B	
LPC_AD<0>	BI	P9	PB20A	BANK4
LPC_AD<1>	BI	N9	PB20B	
LPC_AD<2>	BI	P10	PB30A	
LPC_AD<3>	BI	M10	PB30B	
LPC_FRAME_L	BI	P12	PB31A	
LPC_RESET_L	IN	P13	PB31B	
LPC_CLK33M_GMUX	IN	N12	PB32A	
GMUX_INT	OUT	P14	PB32B	
LVDS_IG_B_DATA_P<2>	IN	B1	PL2A	BANK7
LVDS_IG_B_DATA_N<2>	IN	B2	PL2B	
TP_GMUX_PL10A		C2	PL10A	
TP_GMUX_PL10B		D3	PL10B	
LVDS_IG_A_DATA_P<0>	IN	D1	PL11A	
LVDS_IG_A_DATA_N<0>	IN	E1	PL11B	
LVDS_IG_A_DATA_P<1>	IN	D2	PL12A	
LVDS_IG_A_DATA_N<1>	IN	E3	PL12B	
LVDS_IG_A_DATA_P<2>	IN	F1	PL13A	
LVDS_IG_A_DATA_N<2>	IN	G1	PL13B	
LVDS_IG_B_DATA_P<0>	IN	F3	PL14A	
LVDS_IG_B_DATA_N<0>	IN	G2	PL14B	
LVDS_IG_B_DATA_P<1>	IN	H2	PL15A	
LVDS_IG_B_DATA_N<1>	IN	G3	PL15B	
LVDS_IG_A_CLK_P	IN	H1	PL16A	
LVDS_IG_A_CLK_N	IN	H3	PL16B	
TP_LVDS_MUX_SEL_EG	OUT	L1	PL18A	BANK6
TP_GMUX_PL18B_VSYNC		L3	PL18B	
GMUX_PCIE_RESET_L	IN	K3	PL19A	
GMUX_PM_SLP_S3_L	IN	L2	PL19B	
PM_ALL_GPU_PGOOD	IN	N1	PL32A	
EG_CLKREQ_IN_L	IN	P1	PL32B	

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

GND: J1 B8 C6 C12 C13 E13 M14 N10 N6 P3 M2 C1 E2 B4 M11
GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL

PT2A	A2	LVDS_B_DATA_P<0>	OUT	BANK0
PT2B	A3	LVDS_B_DATA_N<0>	OUT	
PT3A	A1	LVDS_B_DATA_P<1>	OUT	
PT3B	B3	LVDS_B_DATA_N<1>	OUT	
PT4A	C5	LVDS_B_DATA_P<2>	OUT	
PT4B	A5	LVDS_B_DATA_N<2>	OUT	
PT14A	B6	GMUX_PM_SLP_S3_L	IN	
PT14B	C7	GMUX_DEBUG_RESET_L	IN	
PT15A	A6	LVDS_A_CLK_P	OUT	
PT15B	A7	LVDS_A_CLK_N	OUT	
PT16A	C8	LVDS_B_CLK_P	OUT	
PT16B	C9	LVDS_B_CLK_N	OUT	
PT17A	A8	LVDS_A_DATA_P<0>	OUT	
PT17B	B9	LVDS_A_DATA_N<0>	OUT	
PT18A	A9	LVDS_A_DATA_P<1>	OUT	
PT18B	C10	LVDS_A_DATA_N<1>	OUT	
PT19A	B10	LVDS_A_DATA_P<2>	OUT	
PT19B	A10	LVDS_A_DATA_N<2>	OUT	
PT20A	A11	TP_GMUX_PT20A		BANK1
PT20B	B12	TP_GMUX_PT20B		
PT32A	B13	TP_GMUX_PT32A		
PT32B	A13	TP_GMUX_PT32B		
PR2A	A14	DP_CA_DET	IN	BANK2
PR2B	B14	DP_HOTPLUG_DET	IN	
PR10A	D12	LVDS_EG_A_DATA_P<0>	IN	
PR10B	D13	LVDS_EG_A_DATA_N<0>	IN	
PR11A	D14	LVDS_EG_A_DATA_P<1>	IN	
PR11B	E14	LVDS_EG_A_DATA_N<1>	IN	
PR12A	E12	LVDS_EG_A_DATA_P<2>	IN	
PR12B	F12	LVDS_EG_A_DATA_N<2>	IN	
PR13A	F14	LVDS_EG_B_DATA_P<0>	IN	
PR13B	G14	LVDS_EG_B_DATA_N<0>	IN	
PR14A	G12	LVDS_EG_B_DATA_P<1>	IN	
PR14B	G13	LVDS_EG_B_DATA_N<1>	IN	
PR15A	H13	LVDS_EG_B_DATA_P<2>	IN	
PR15B	H12	LVDS_EG_B_DATA_N<2>	IN	
PR16A	H14	LVDS_EG_A_CLK_P	IN	
PR16B	J12	LVDS_EG_A_CLK_N	IN	
PR18A	L14	LVDS_IG_PANEL_PWR	IN	BANK3
PR18B	M13	EG_LCD_PWR_EN	IN	
PR30A	N14	LVDS_IG_BKL_ON	IN	
PR30B	N13	EG_BKLT_EN	IN	

LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9200 (All 14 resistors)

LVDS_IG_A_CLK_P	R9650 100 1% 1/16W MF-LF 402	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA_P<0>	R9651 100 1% 1/16W MF-LF 402	LVDS_IG_A_DATA_N<0>	
LVDS_IG_A_DATA_P<1>	R9652 100 1% 1/16W MF-LF 402	LVDS_IG_A_DATA_N<1>	
LVDS_IG_A_DATA_P<2>	R9653 100 1% 1/16W MF-LF 402	LVDS_IG_A_DATA_N<2>	
LVDS_IG_B_DATA_P<0>	R9654 100 1% 1/16W MF-LF 402	LVDS_IG_B_DATA_N<0>	
LVDS_IG_B_DATA_P<1>	R9655 100 1% 1/16W MF-LF 402	LVDS_IG_B_DATA_N<1>	
LVDS_IG_B_DATA_P<2>	R9656 100 1% 1/16W MF-LF 402	LVDS_IG_B_DATA_N<2>	
LVDS_EG_A_CLK_P	R9660 100 1% 1/16W MF-LF 402	LVDS_EG_A_CLK_N	
LVDS_EG_A_DATA_P<0>	R9661 100 1% 1/16W MF-LF 402	LVDS_EG_A_DATA_N<0>	
LVDS_EG_A_DATA_P<1>	R9662 100 1% 1/16W MF-LF 402	LVDS_EG_A_DATA_N<1>	
LVDS_EG_A_DATA_P<2>	R9663 100 1% 1/16W MF-LF 402	LVDS_EG_A_DATA_N<2>	
LVDS_EG_B_DATA_P<0>	R9664 100 1% 1/16W MF-LF 402	LVDS_EG_B_DATA_N<0>	
LVDS_EG_B_DATA_P<1>	R9665 100 1% 1/16W MF-LF 402	LVDS_EG_B_DATA_N<1>	
LVDS_EG_B_DATA_P<2>	R9666 100 1% 1/16W MF-LF 402	LVDS_EG_B_DATA_N<2>	

SIGNAL_MODEL=EMPTY

Required Pullups

PP3V3_S0
GMUX_DEBUG_RESET_L R9680 1K 5% 1/16W MF-LF 402
JTAG_GMUX_TCK R9690 4.7K 5% 1/16W MF-LF 402
EG_CLKREQ_OUT_L R9695 10K 5% 1/16W MF-LF 402
NO STUFF R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST
PLACEMENT_NOTE=Place on top side at U9200

Required Pulldowns

DP_MUX_SEL_EG	R9681 10K 5% 1/16W MF-LF 402	
LVDS_DDC_SEL_IG	R9682 10K 5% 1/16W MF-LF 402	
LVDS_DDC_SEL_EG	R9683 10K 5% 1/16W MF-LF 402	

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

NO STUFF
EG_RESET_L R9691 100K 5% 1/16W MF-LF 402
GMUX_INT R9692 20K 5% 1/16W MF-LF 402
LCD_BKLT_PWM R9693 100K 5% 1/16W MF-LF 402
EG_CLKREQ_IN_L R9694 100K 5% 1/16W MF-LF 402

EG_PWRSEQ_HW R9630 0 5% 1/16W MF-LF 402 EXTGPU_PWR_EN
EG_RAIL1_EN EG_PWRSEQ_GMUX R9631 0 5% 1/16W MF-LF 402 P1V1_GPU_EN
EG_RAIL2_EN EG_PWRSEQ_GMUX R9632 0 5% 1/16W MF-LF 402 P3V3GPU_EN
EG_RAIL3_EN EG_PWRSEQ_GMUX R9633 0 5% 1/16W MF-LF 402 GPUVCORE_EN
EG_RAIL4_EN EG_PWRSEQ_GMUX R9634 0 5% 1/16W MF-LF 402 P1V8_S0GPU_EN

The MAKE BASE properties for these signals are on the POWER CONTROL page.

NO STUFF C9691 0.1UF 20% 10V CERM 402
NO STUFF C9693 0.1UF 20% 10V CERM 402
NO STUFF C9692 0.1UF 20% 10V CERM 402
NO STUFF C9694 0.1UF 20% 10V CERM 402

PM_SLP_S3_L Isolation

PP3V3_S0
Q9670 SSM6N15FEAPE SOT563
R9670 10K 5% 1/16W MF-LF 402
PM_SLP_S3_L
GMUX_PM_SLP_S3_L
MAKE_BASE=TRUE

GMUX_JTAG_TCK Inversion

JTAG_GMUX_TCK
Q9670 SSM6N15FEAPE SOT563
GMUX_JTAG_TCK_L

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0025	1	IC,XP2-5,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2479	1	IC,CPLD,LATTICE,132CSBGA,K19	U9600	CRITICAL	GMUX_PROG

Graphics MUX (GMUX)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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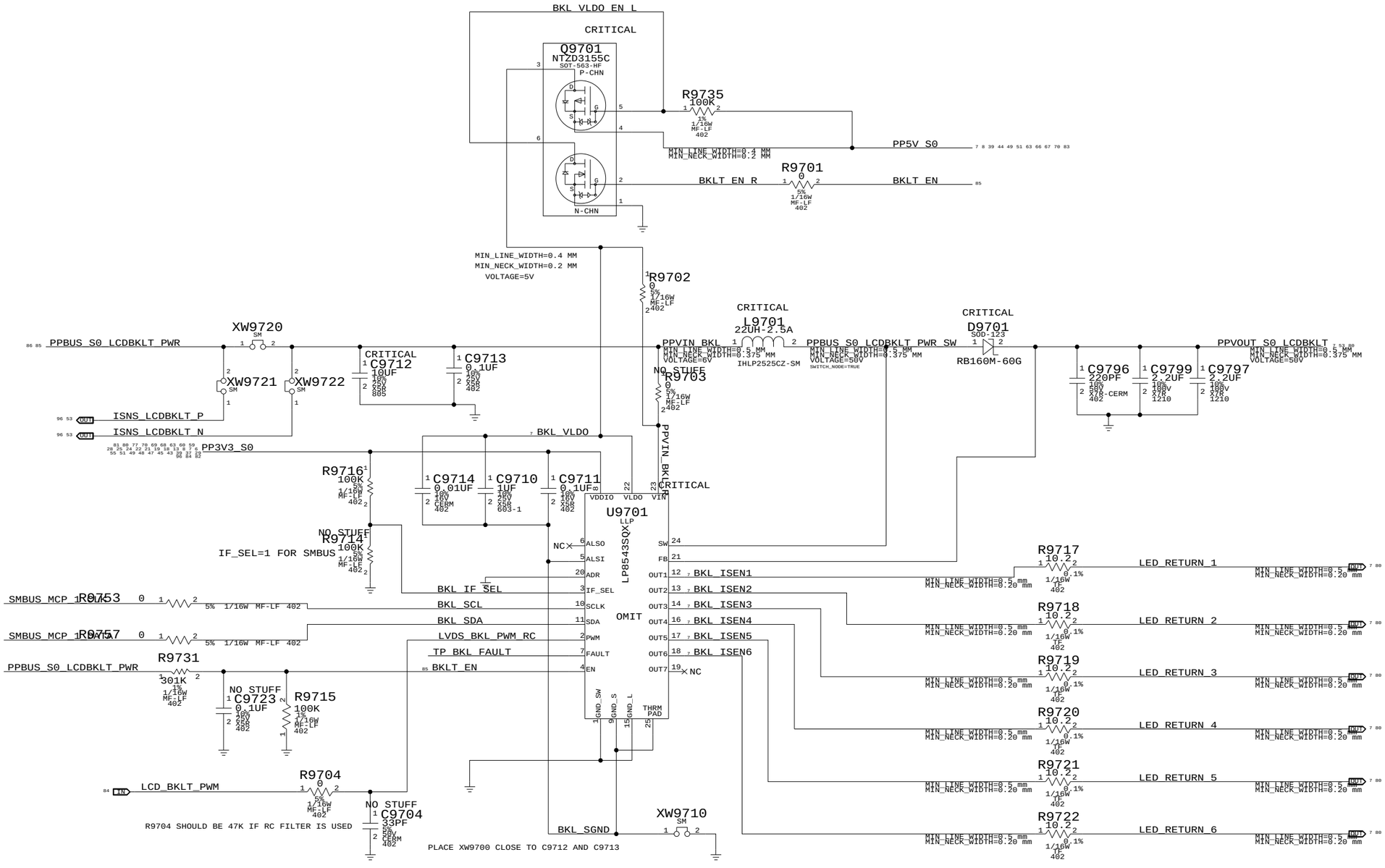
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 84 OF 97	

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



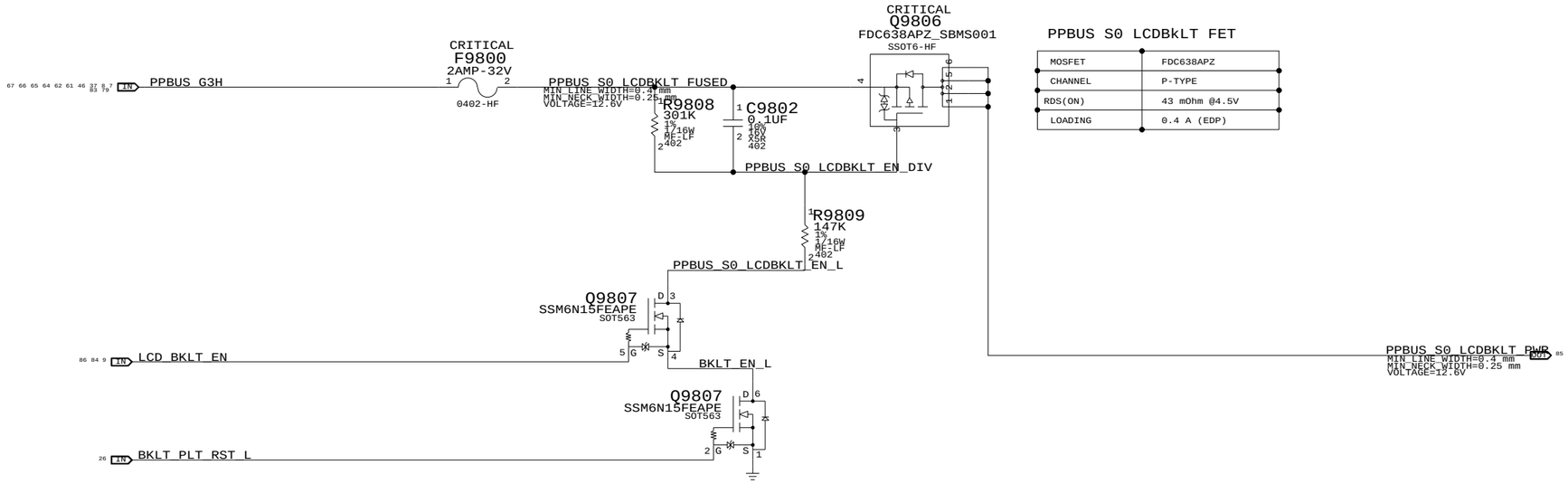
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT,PROD	U9701	CRITICAL	

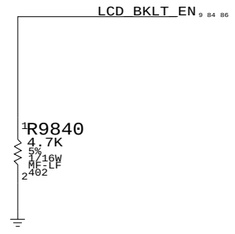
LCD BACKLIGHT DRIVER

SYNC_MASTER=DDR SYNC_DATE=12/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 85 OF 97	





LCD Backlight Support

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

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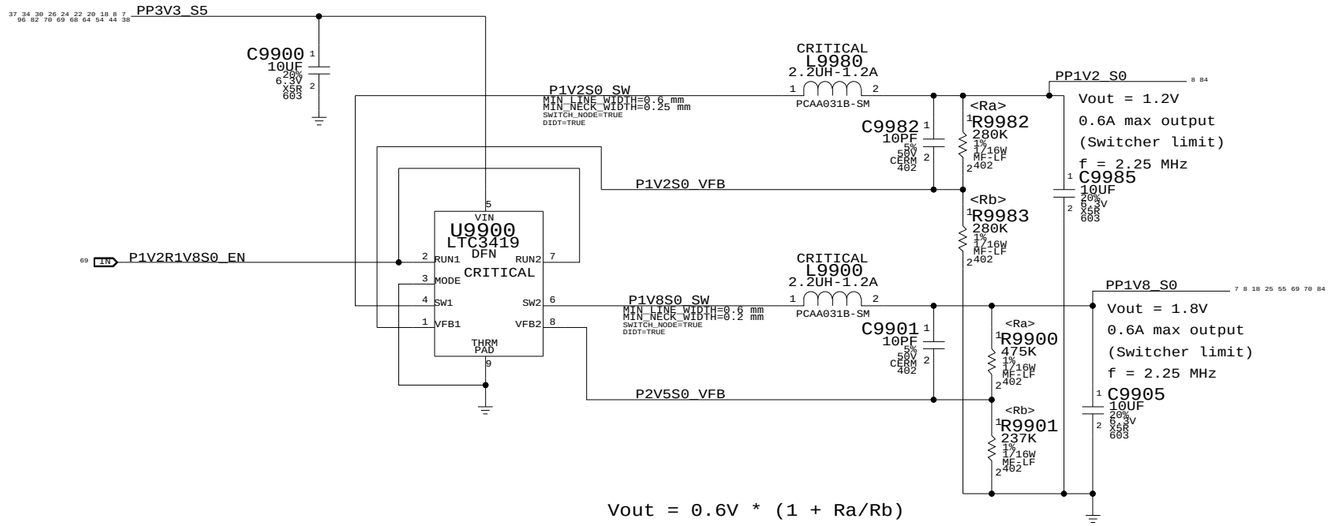
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 86 OF 97	

1.8V/1.2V S0 SWITCHER



Vout = 0.6V * (1 + Ra/Rb)

Misc Power Supplies

SYNC_MASTER=MUXGFX SYNC_DATE=02/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 87 OF 97	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 43 63
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 43
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 63
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 63
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	63
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 27
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 63
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 63
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 63
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	63
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	63

CPU/FSB Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0

SCALE: NONE SHT 88 OF 97

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 89 OF 97	

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	13.1 MM	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	PCIE_90D	PCIE	PEG_R2D_P<15..0> 71
	PCIE_90D	PCIE	PEG_R2D_N<15..0> 71
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0> 9 71
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0> 9 71
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0> 9 71
	PCIE_90D	PCIE	PEG_D2R_N<15..0> 9 71
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0> 71
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0> 71
	PCIE_90D	PCIE	PCIE_MINI_R2D_P 7 31 96
	PCIE_90D	PCIE	PCIE_MINI_R2D_N 7 31 96
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P 17 31
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N 17 31
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P 7 17 31
	PCIE_90D	PCIE	PCIE_MINI_D2R_N 7 17 31
	PCIE_90D	PCIE	PCIE_FW_R2D_P 36
	PCIE_90D	PCIE	PCIE_FW_R2D_N 36
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P 17 36
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N 17 36
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P 17 36
	PCIE_90D	PCIE	PCIE_FW_D2R_N 17 36
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P 36
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N 36
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P 96
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N 96
PCIE_EXCARD_R2D	PCIE_90D	PCIE	TP_PCIE_EXCARD_R2D_C_P 9 17
	PCIE_90D	PCIE	TP_PCIE_EXCARD_R2D_C_N 9 17
PCIE_EXCARD_D2R	PCIE_90D	PCIE	TP_PCIE_EXCARD_D2R_P 9 17
	PCIE_90D	PCIE	TP_PCIE_EXCARD_D2R_N 9 17
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P 17 71
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N 17 71
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P 17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N 17 31
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P 17 36
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N 17 36
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_EXCARD_P 9 17
	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_EXCARD_N 9 17
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP 17
CRT_RED	CRT_50S	CRT	NC_CRT_IG_R_C_PR 18 25
CRT_GREEN	CRT_50S	CRT	NC_CRT_IG_G_Y_Y 18 25
CRT_BLUE	CRT_50S	CRT	NC_CRT_IG_B_COMP_PB 18 25
CRT_SYNC	CRT_50S	CRT_SYNC	NC_CRT_IG_HSYNC 18 25
CRT_SYNC	CRT_50S	CRT_SYNC	NC_CRT_IG_VSYNC 18 25
MCP_DAC_RSET		MCP_DAC_COMP	NC_MCP_TV_DAC_RSET 18 25
MCP_DAC_VREF		MCP_DAC_COMP	NC_MCP_TV_DAC_VREF 18 25
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0> 9 81
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0> 9 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P 18 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N 18 81
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET 18 25
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE 18 25
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P 18 84
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N 18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 84
LVDS_IG_A_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_A_DATAP<3> 9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_A_DATAN<3> 9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	NC_LVDS_IG_B_CLKP 9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	NC_LVDS_IG_B_CLKN 9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 84
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 84
LVDS_IG_B_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_B_DATAP<3> 9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_B_DATAN<3> 9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET 18 25
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE 18 25
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P 20 39
	SATA_100D	SATA	SATA_HDD_R2D_C_N 20 39
	SATA_100D	SATA	SATA_HDD_R2D_P 7 39
	SATA_100D	SATA	SATA_HDD_R2D_N 7 39
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P 20 39
	SATA_100D	SATA	SATA_HDD_D2R_N 20 39
	SATA_100D	SATA	SATA_HDD_D2R_C_P 7 39
	SATA_100D	SATA	SATA_HDD_D2R_C_N 7 39
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P 20 39
	SATA_100D	SATA	SATA_ODD_R2D_C_N 20 39
	SATA_100D	SATA	SATA_ODD_R2D_P 7 39
	SATA_100D	SATA	SATA_ODD_R2D_N 7 39
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P 20 39
	SATA_100D	SATA	SATA_ODD_D2R_N 20 39
	SATA_100D	SATA	SATA_ODD_D2R_C_P 7 39
	SATA_100D	SATA	SATA_ODD_D2R_C_N 7 39
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP 20

MCP Constraints 1

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0

SCALE NONE SHT 90 OF 97

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	19 42 44 84
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19 42 44 84
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 26 84
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 26
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	26 42
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 44
USB_EXTA	USB_90D	USB	USB_EXTA_P	20 40
	USB_90D	USB	USB_EXTA_N	20 40
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	NC_USB_MINIP	9 20
	USB_90D	USB	NC_USB_MININ	9 20
USB_EXTD	USB_90D	USB	NC_USB_EXTDP	9 20
	USB_90D	USB	NC_USB_EXTDN	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 20 31
	USB_90D	USB	USB_CAMERA_N	7 20 31
USB_BT	USB_90D	USB	USB_BT_P	7 20 31
	USB_90D	USB	USB_BT_N	7 20 31
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 50
	USB_90D	USB	USB_TPAD_N	20 50
USB_IR	USB_90D	USB	USB_IR_P	20 41
	USB_90D	USB	USB_IR_N	20 41
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 40
	USB_90D	USB	USB_EXTB_N	20 40
USB_EXCARD	USB_90D	USB	NC_USB_EXCARDP	9 20
	USB_90D	USB	NC_USB_EXCARDN	9 20
USB_EXTC	USB_90D	USB	NC_USB_EXTCP	9 20
	USB_90D	USB	NC_USB_EXTCN	9 20
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	13 21 28 29 45
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	13 21 28 29 45
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 45 60 85
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 45 60 85
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	21 55
	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 55
	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_RST_L	21 55
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 55
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 55
	HDA_55S	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 26
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	26 42
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21 44
	SPI_55S	SPI	SPI_CLK	54
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21 44
	SPI_55S	SPI	SPI_MOSI	54
SPI_MISO	SPI_55S	SPI	SPI_MISO	21 44
	SPI_55S	SPI	SPI_MISO_R	54
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 44
	SPI_55S	SPI	SPI_CS0_L	

MCP Constraints 2

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT: 91	OF: 97

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD 18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND 18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R 18 34
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1 33 34
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO 18 33
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC 18 33
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R 33
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK 18 33
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0> 33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0> 18 33
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1> 18 33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL 18 33
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK 18 33
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0> 18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1> 18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL 18 33
	ENET_MII_55S	ENET_MII	ENET_RESET_L 18 33
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0> 33 35
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0> 33 35

Ethernet Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 92 OF 97	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	36 38
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	36 38
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	36 38
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	36 38
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	36 38
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	36 38
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	36 38
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	36 38
Port 2 Not Used				

SD CARD NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
I32 SD_DATA	SD_55S	SD_INTERFACE	SD_D<0>	7 32
I31 SD_DATA	SD_55S	SD_INTERFACE	SD_D<1>	7 32
I30 SD_DATA	SD_55S	SD_INTERFACE	SD_D<2>	7 32
I29 SD_DATA	SD_55S	SD_INTERFACE	SD_D<3>	7 32
I28 SD_DATA	SD_55S	SD_INTERFACE	SD_D<4>	7 32
I27 SD_DATA	SD_55S	SD_INTERFACE	SD_D<5>	7 32
I26 SD_DATA	SD_55S	SD_INTERFACE	SD_D<6>	7 32
I25 SD_DATA	SD_55S	SD_INTERFACE	SD_D<7>	7 32
I23 SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	7 32
I24 SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	7 32

FireWire Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT 93 OF 97	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	7 31 42 45 51
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	7 31 42 45 51
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	42 45 48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	42 45 48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	42 45 48 53 78
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	42 45 48 53 78
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 42 45 61 62
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 42 45 61 62
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	27 39 42 45
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	27 39 42 45

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	62
	1TO1_DIFFPAIR		CHGR_CSI_N	62
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	62
	1TO1_DIFFPAIR		CHGR_CSO_N	62

SMC Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE NONE	SHT 94 OF 97	

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	81 84
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	81 84
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	81 84
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	81 84
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	81 84
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	81 84
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	81 84
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	81 84
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P	7 80
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N	7 80
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P	7 80
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	7 80
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	80 81
	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	80 81
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>	7 80 81
	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>	7 80 81
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	80 81
	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	80 81
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>	7 80 81
	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>	7 80 81
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	7 82
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	82
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	81 82
	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	81 82
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	82
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	82
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	81 82
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	81 82

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	73 74
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	73 74
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	73 74
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	73 74
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCKE	
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCKE	
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCS0_L	
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	73 74
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	73 74
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	73 74
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	73 74
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	73 74
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	73 74
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	73 74
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	73 74
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	73 74
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	73 74
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	73 74
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	73 74
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	73 74
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	73 74
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	73 74
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	73 74
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	73 74
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	73 74
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	73 74
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	73 74
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	73 74
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	73 74
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	73 74
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	73 74
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	73 74
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	73 74
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	73 74
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	73 74
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	73 74
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	73 74
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	73 74
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	73 74
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	73 74
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	73 74
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	73 74

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
(CK505_OUT36)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	76 77
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	76 77
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	78 84
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	78 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>	78 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>	78 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>	78 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>	78 84
DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_P<3..0>	78 81
DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_N<3..0>	78 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P	78 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N	78 81
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P	81
	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N	81

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	73 75
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	73 75
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	73 75
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	73 75
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCKE	
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCKE	
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCS0_L	
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	73 75
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	73 75
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	73 75
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	73 75
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	73 75
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	73 75
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	73 75
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	73 75
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	73 75
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	73 75
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	73 75
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	73 75
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	73 75
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	73 75
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	73 75
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	73 75
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	73 75
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	73 75
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	73 75
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	73 75
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	73 75
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	73 75
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	73 75
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	73 75
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	73 75
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	73 75
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	73 75
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	73 75
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	73 75
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	73 75
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	73 75
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	73 75
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	73 75
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	73 75
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	73 75

GPU (G96) CONSTRAINTS

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE: NONE	SHT: 95 OF 97	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

PGA CONSTRAINT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PGA_50SE	*	Y	=50_OHM_SE	0.073 MM	=50_OHM_SE	=1:1_DIFFPAIR	0.073 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FSB_50S	PGA	PGA_50SE
FSB_DSTB_50S	PGA	PGA_50SE
CPU_50S	PGA	PGA_50SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_DATA	*	PGA	PGA_CPU
FSB_DSTB	*	PGA	PGA_CPU
FSB_ADDR	*	PGA	PGA_CPU
FSB_ADSTB	*	PGA	PGA_CPU
FSB_1X	*	PGA	PGA_CPU
CPU_AGTL	*	PGA	PGA_CPU
CPU_BMIL	*	PGA	PGA_CPU

K19 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_MDI_100D	ENETCONN	ENETCONN P<3..0>	35
	ENET_MDI_100D	ENETCONN	ENETCONN N<3..0>	35
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	39
U145	SATA_100D	SATA	SATA_ODD_R2D_UF_N	39
U144	SATA_100D	SATA	SATA_ODD_D2R_UF_P	7 39
U142	SATA_100D	SATA	SATA_ODD_D2R_UF_N	7 39
U143	SATA_100D	SATA	SATA_HDD_D2R_UF_P	39
U140	SATA_100D	SATA	SATA_HDD_D2R_UF_N	39
U141	SATA_100D	SATA	SATA_HDD_R2D_UF_P	39
U139	SATA_100D	SATA	SATA_HDD_R2D_UF_N	39
	SENSE_1TO1_55S SENSE		GFXIMVP6_VSEN_P	79
	SENSE_1TO1_55S SENSE		GFXIMVP6_VSEN_N	79
U31	THERM_1TO1_55S THERM		CPUTHMSNS_D2_P	48
U30	THERM_1TO1_55S THERM		CPUTHMSNS_D2_N	48
U27	THERM_1TO1_55S THERM		CPU_THERMD_P	10 48
U26	THERM_1TO1_55S THERM		CPU_THERMD_N	10 48
U29	THERM_1TO1_55S THERM		GPUTHMSNS_D_P	48
U28	THERM_1TO1_55S THERM		GPUTHMSNS_D_N	48
U25	THERM_1TO1_55S THERM		GPU_TDIODE_P	48 76 77
	THERM_1TO1_55S THERM		GPU_TDIODE_N	48 76 77
U138	THERM_1TO1_55S THERM		MCPTHMSNS_D_P	48
U137	THERM_1TO1_55S THERM		MCPTHMSNS_D_N	48
U135	THERM_1TO1_55S THERM		MCP_THMDIODE_P	21 48
U136	THERM_1TO1_55S THERM		MCP_THMDIODE_N	21 48
U158	SENSE_1TO1_55S SENSE		CPUVTTISNS_R_P	47
U157	SENSE_1TO1_55S SENSE		CPUVTTISNS_R_N	47
U153	SENSE_1TO1_55S SENSE		GPUISENS_P	47
U152	SENSE_1TO1_55S SENSE		GPUISENS_N	47
U151	SENSE_1TO1_55S SENSE		CPUVTT_ISNS_P	47 67
U150	SENSE_1TO1_55S SENSE		CPUVTT_ISNS_N	47 67
U158	SENSE_1TO1_55S SENSE		P1V8GPU_P	47
U147	SENSE_1TO1_55S SENSE		P1V8GPU_N	47
U186	SENSE_1TO1_55S SENSE		ISNS_CPU_P	46
U185	SENSE_1TO1_55S SENSE		ISNS_CPU_N	46
		SB_POWER	PP3V3_S5	37 38 44 54 64 68 69 70 7 8 18 20 22 24 26 30 34 82 87
		SB_POWER	PP3V3_S0	48 49 51 55 59 60 63 68 5 7 8 18 20 22 24 26 30 34 37 38 44 54 64 69 70 77 80 81 82 84 85
U34	SENSE_1TO1_55S SENSE		P1V8GPUISNS_R_P	47
U33	SENSE_1TO1_55S SENSE		P1V8GPUISNS_R_N	47
T214	SENSE_1TO1_55S SENSE		ISNS_AIRPORT_P	31 53
T209	SENSE_1TO1_55S SENSE		ISNS_AIRPORT_N	31 53
T215	SENSE_1TO1_55S SENSE		ISNS_AIRPORT_R_P	53
T216	SENSE_1TO1_55S SENSE		ISNS_AIRPORT_R_N	53
T213	SENSE_1TO1_55S SENSE		ISNS_1V5_S3_R_P	53
T211	SENSE_1TO1_55S SENSE		ISNS_1V5_S3_R_N	53
T210	SENSE_1TO1_55S SENSE		ISNS_1V5_S3_P	53 65
T212	SENSE_1TO1_55S SENSE		ISNS_1V5_S3_N	53 65
T219	SENSE_1TO1_55S SENSE		ISNS_LCDBKLT_P	53 85
T218	SENSE_1TO1_55S SENSE		ISNS_LCDBKLT_N	53 85
T217	SENSE_1TO1_55S SENSE		ISNS_LCDBKLT_R_P	53
T220	SENSE_1TO1_55S SENSE		ISNS_LCDBKLT_R_N	53

K19 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T154 (PCIE_EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	90
T152 (PCIE_EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	90
T153	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7 31 90
T151 (PCIE_MINI)	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7 31 90
T150 (PCIE_MINI)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 31
T149	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 31
T189	1TO1_DIFFPAIR		CHGR_CSI_R_P	62
T188	1TO1_DIFFPAIR		CHGR_CSI_R_N	62
T187	1TO1_DIFFPAIR		CHGR_CSO_R_P	46 62
T185	1TO1_DIFFPAIR		CHGR_CSO_R_N	46 62
T192 (USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	40
T191 (USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	40
T172 (USB_EXTA)	USB_90D	USB	USB2_LT1_P	40
T170 (USB_EXTA)	USB_90D	USB	USB2_LT1_N	40
T177 (USB_EXTD)	USB_90D	USB	USB_TPAD_R_P	50
T176 (USB_EXTD)	USB_90D	USB	USB_TPAD_R_N	50
T178 (USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	7 31
T179 (USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	7 31
T174	USB_90D	USB	CONN_USB2_BT_P	7 31
T173	USB_90D	USB	CONN_USB2_BT_N	7 31
T175	USB_90D	USB	USB_LT2_P	40
T171	USB_90D	USB	USB_LT2_N	40
T180 USB_CARDREADER	USB_90D	USB	USB_CARDREADER_P	9 20 32
T181	USB_90D	USB	USB_CARDREADER_N	9 20 32
T193	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P	81
T194	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N	81
T199 SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	7 58 59
T197	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	7 58 59
T201 SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	7 58 59
T200	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	7 58 59
T198 SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	7 58 59
T202	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	7 58 59
T206	DIFFPAIR	AUDIO	SPKRAMP_L_OUT_P	58
T207	DIFFPAIR	AUDIO	SPKRAMP_L_OUT_N	58
T204	DIFFPAIR	AUDIO	SPKRAMP_R_OUT_P	58
T205	DIFFPAIR	AUDIO	SPKRAMP_R_OUT_N	58
T208	DIFFPAIR	AUDIO	SPKRAMP_S_OUT_P	58
T203	DIFFPAIR	AUDIO	SPKRAMP_S_OUT_N	58
T223 SENSE_DIFFPAIR	SENSE_1TO1_55S SENSE		ISNS_ODD_P	39 53
T224	SENSE_1TO1_55S SENSE		ISNS_ODD_N	39 53
T226 SENSE_DIFFPAIR	SENSE_1TO1_55S SENSE		ISNS_ODD_R_P	53
T225	SENSE_1TO1_55S SENSE		ISNS_ODD_R_N	53
T183 SENSE_DIFFPAIR	SENSE_1TO1_55S SENSE		ISNS_HDD_P	39 53
T182	SENSE_1TO1_55S SENSE		ISNS_HDD_N	39 53
T184 SENSE_DIFFPAIR	SENSE_1TO1_55S SENSE		ISNS_HDD_R_P	53
T227	SENSE_1TO1_55S SENSE		ISNS_HDD_R_N	53
	GND		GND	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Project Specific Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/21/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0
SCALE NONE	SHT 96 OF 97	

K19 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,PGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	33.6 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?
PGA_CPU	*	0.073 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M99_MLB SYNC_DATE=01/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7892	A.0.0

SCALE	SHT	OF
NONE	97	97