



Part Number = X76264BOL81
SEYSAM1G@



Part Number = X76264BOL82
SEYHYN1G@



Part Number = X76264BOL55
WHISAM1G@



Part Number = X76264BOL60
WHIHYN1G@



Part Number = X76264BOL61
SAM2G@



Part Number = X76264BOL62
HYN2G@

Compal Confidential

P7YE5/S5 Schematics Document

AMD Sabine

APU Llano / Hudson M2 / Vancouver Whistler_Seymour

DIS only / UMA only / PX Muxless with BACO



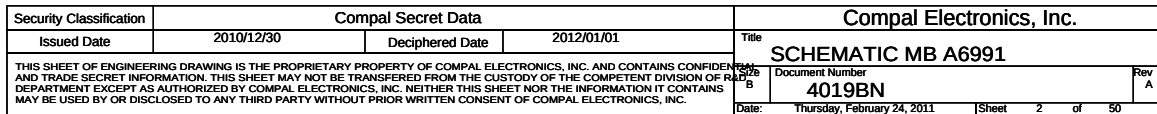
Part Number = DA80000NI00

2011-02-18

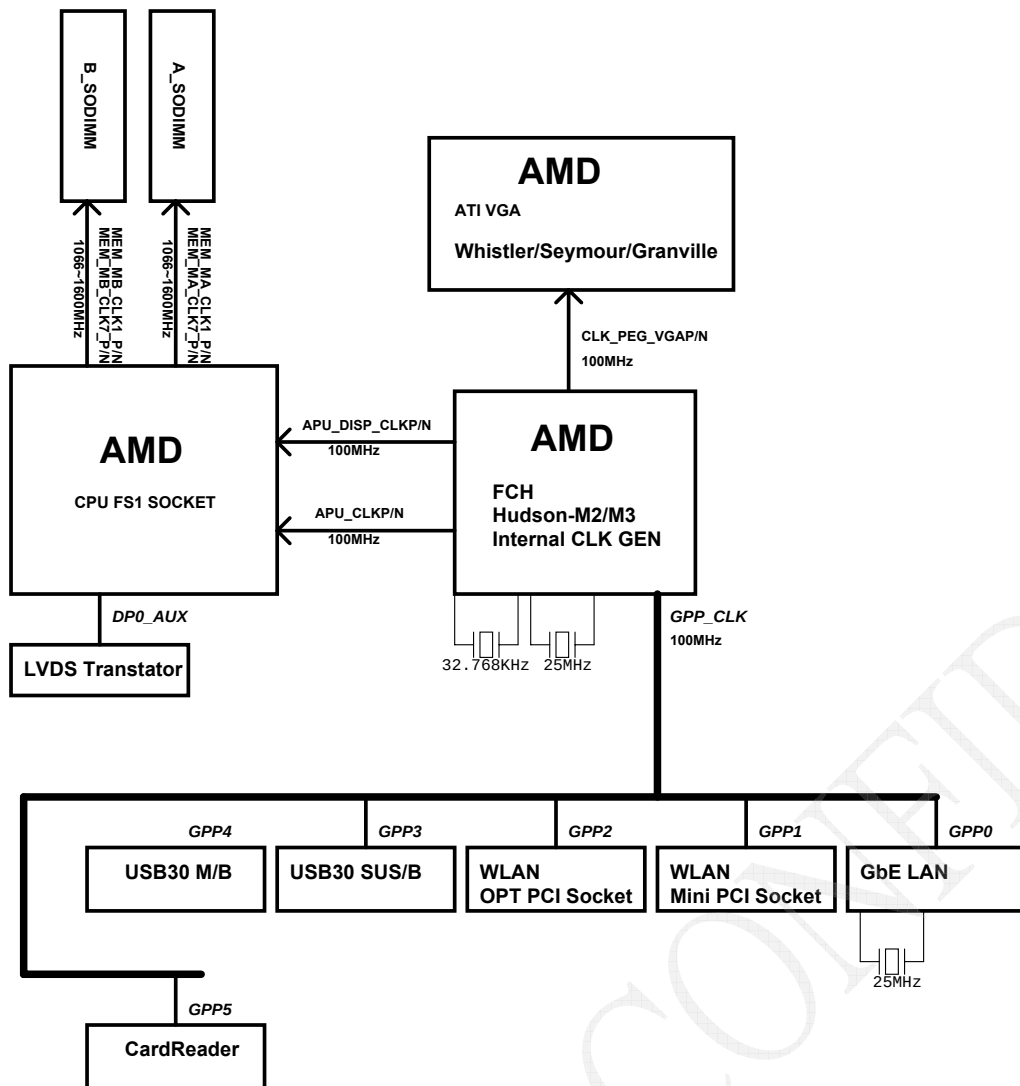
LA-6991P REV: 0.2

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/12/30	Deciphered Date	2012/01/01	Title	
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Date: Thursday, February 24, 2011				Rev A	
Sheet 1 of 50					

Sabine



CLOCK DISTRIBUTION

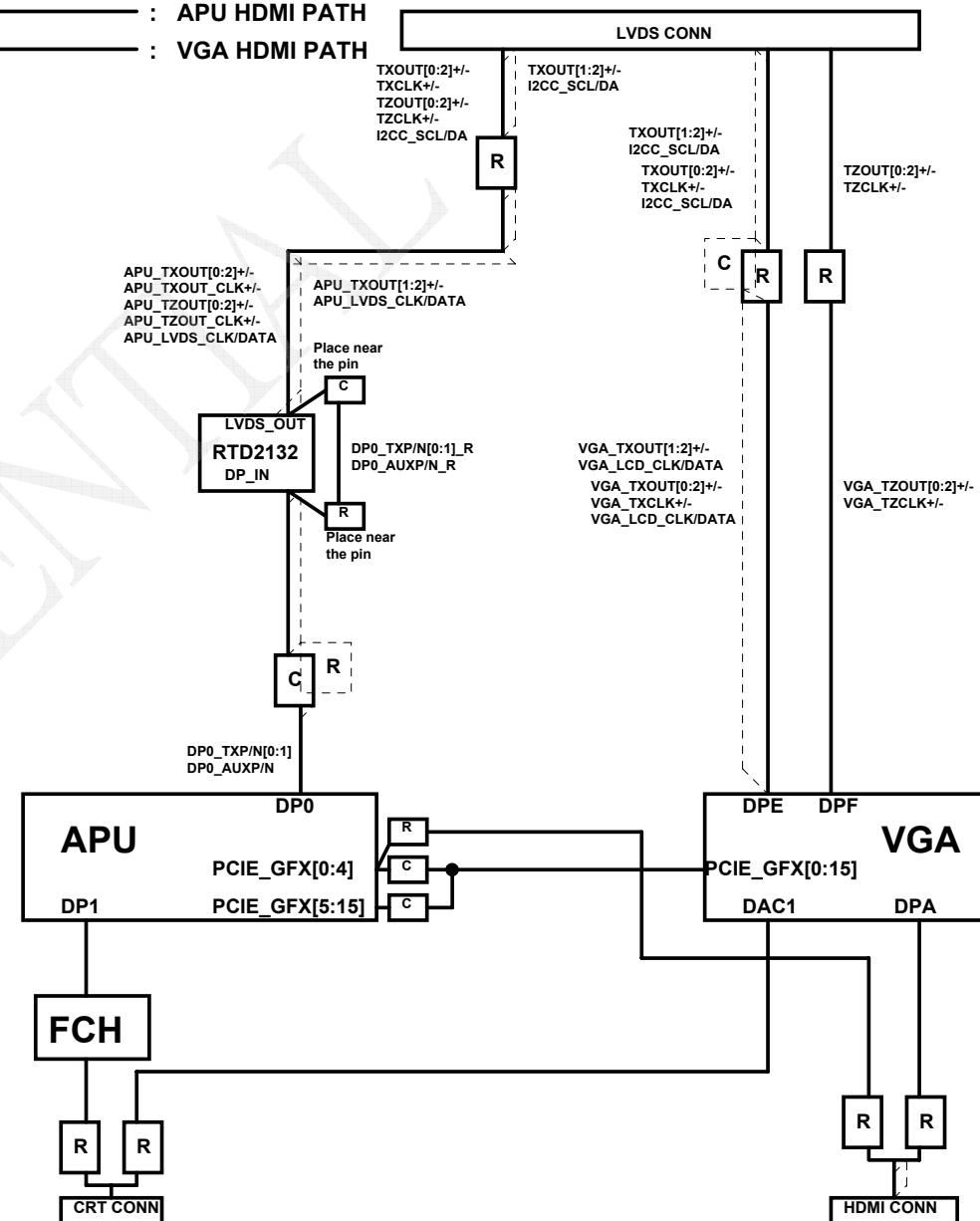


DISPLAY DISTRIBUTION

- ```

_____ : LVDS PATH
_____, --- : eDP PATH
_____ : APU HDMI PATH
_____ : VGA HDMI PATH

```



|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                             |                    |         |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|-----------------------------|--------------------|---------|
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Custom                      | 4019BN             | A       |
| Date                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                    |                 |            | Thursday, February 24, 2011 | Sheet              | 3 of 50 |

Voltage Rails

| Power Plane  | Description                                  | S1  | S3  | S5  |
|--------------|----------------------------------------------|-----|-----|-----|
| VIN          | Adapter power supply (19V)                   | N/A | N/A | N/A |
| B+           | AC or battery power rail for power circuit.  | N/A | N/A | N/A |
| +CPU_CORE    | Core voltage for CPU                         | ON  | OFF | OFF |
| +CPU_CORE_1  | Core voltage for CPU (0.7-1.2V)              | ON  | OFF | OFF |
| +CPU_CORE_NB | Voltage for On-die VGA of APU                | ON  | OFF | OFF |
| +VGA_CORE    | 0.95-1.2V switched power rail                | ON  | OFF | OFF |
| +0.75VS      | 0.75V switched power rail for DDR terminator | ON  | ON  | OFF |
| +1.0VSG      | 1.0V switched power rail for VGA             | ON  | OFF | OFF |
| +1.1ALW      | 1.1V switched power rail for FCH             | ON  | ON  | ON* |
| +1.1VS       | 1.1V switched power rail for FCH             | ON  | OFF | OFF |
| +1.2VS       | 1.2V switched power rail for APU             | ON  | OFF | OFF |
| +1.5V        | 1.5V power rail for CPU VDDIO and DDR        | ON  | ON  | OFF |
| +1.5VS       | 1.5V switched power rail                     | ON  | OFF | OFF |
| +1.8VSG      | 1.8V switched power rail                     | ON  | OFF | OFF |
| +2.5VS       | 2.5V for CPU_VDDA                            | ON  | OFF | OFF |
| +3VALW       | 3.3V always on power rail                    | ON  | ON  | ON* |
| +3V_LAN      | 3.3V power rail for LAN                      | ON  | ON  | ON  |
| +3VS         | 3.3V switched power rail                     | ON  | OFF | OFF |
| +5VALW       | 5V always on power rail                      | ON  | ON  | ON* |
| +5VS         | 5V switched power rail                       | ON  | OFF | OFF |
| +VSB         | VSB always on power rail                     | ON  | ON  | ON* |
| +RTCVCC      | RTC power                                    | ON  | ON  | ON  |

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

| Device | IDSEL# | REQ#/GNT# | Interrupts |
|--------|--------|-----------|------------|
|        |        |           |            |
|        |        |           |            |
|        |        |           |            |
|        |        |           |            |
|        |        |           |            |

EC SM Bus1 address

EC SM Bus2 address

| Device        | Address     | HEX | Device                | Address     | HEX |
|---------------|-------------|-----|-----------------------|-------------|-----|
| Smart Battery | 0001 011X b | 16H | SB-TSI                | 1001 100X b | 98H |
|               |             |     | GMT G781-1 (GPU)      | 1001 101X b | 9AH |
|               |             |     | CAT24C64WJ (RTD2136S) | 1010 100X b | A8H |
|               |             |     | VGA-TSI               | 1000 001X b | 82H |
|               |             |     |                       |             |     |

FCH SM Bus 0 address

FCH SM Bus 1 address

| Device    | Address    | HEX | Device | Address | HEX |
|-----------|------------|-----|--------|---------|-----|
| DDR DIMM1 | 1001 000Xb | 90  |        |         |     |
| DDR DIMM2 | 1001 010Xb | 94  |        |         |     |
|           |            |     |        |         |     |
|           |            |     |        |         |     |
|           |            |     |        |         |     |

| STATE                | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V  | +VS | Clock |
|----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON              |        | HIGH    | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | ON    |
| S1(Power On Suspend) |        | LOW     | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | LOW   |
| S3 (Suspend to RAM)  |        | LOW     | LOW     | HIGH    | HIGH    | ON    | ON  | OFF | OFF   |
| S4 (Suspend to Disk) |        | LOW     | LOW     | LOW     | HIGH    | ON    | OFF | OFF | OFF   |
| S5 (Soft OFF)        |        | LOW     | LOW     | LOW     | LOW     | ON    | OFF | OFF | OFF   |

Board ID / SKU ID Table for AD channel

| Vcc      | 3.3V +/- 5%  |             |             |             |
|----------|--------------|-------------|-------------|-------------|
| Ra/Rc/Re | 100K +/- 5%  |             |             |             |
| Board ID | Rb / Rd / Rf | VAD_BID min | VAD_BID typ | VAD_BID max |
| 0        | 0            | 0 V         | 0 V         | 0 V         |
| 1        | 8.2K +/- 5%  | 0.216 V     | 0.250 V     | 0.289 V     |
| 2        | 18K +/- 5%   | 0.436 V     | 0.503 V     | 0.538 V     |
| 3        | 33K +/- 5%   | 0.712 V     | 0.819 V     | 0.875 V     |
| 4        | 56K +/- 5%   | 1.036 V     | 1.185 V     | 1.264 V     |
| 5        | 100K +/- 5%  | 1.453 V     | 1.650 V     | 1.759 V     |
| 6        | 200K +/- 5%  | 1.935 V     | 2.200 V     | 2.341 V     |
| 7        | NC           | 2.500 V     | 3.300 V     | 3.300 V     |

BTO Option Table

| BOM Structure | BTO Item                                    |
|---------------|---------------------------------------------|
| UMA@          | Display from UMA (PX4.0 or UMA only)        |
| VGA@          | Have VGA chip (Discrete only or PX4.0)      |
| DISO@         | Display from VGA (Discrete only)            |
| SEYM@         | Use Seymour (Discrete only and PX4.0)       |
| WHI@          | Use Whistler (Discrete only and PX4.0)      |
| GRAN@         | Use Granville (Discrete only and PX4.0)     |
| VAN@          | Use Vancouver VGA (Discrete only and PX4.0) |
| RT@           | Use translator RTD2136S                     |
| ANX@          | Use translator ANX3110                      |
| M2@           | Use Hudson-M2                               |
| M3@           | Use Hudson-M3                               |
| 930@          | Use KB930                                   |
| 9012@         | Use KB9012                                  |
| 128@          | Use VRAM channel A                          |
| PX@           | PX4.0                                       |
| BACO@         | Use BACO                                    |
| NOBACO@       | No use BACO                                 |
| APULVDS@      | UMA LVDS path                               |
| APUEDP@       | UMA eDP path                                |
| VGALVDS@      | VGA LVDS path                               |
| VGAEDP@       | VGA eDP path                                |
| EDP@          | eDP path                                    |
| JE@           | ACER                                        |
| SJV@          | PB and GW                                   |
| NOGRAN@       | No Use Granville                            |
|               |                                             |
|               |                                             |
|               |                                             |
|               |                                             |
|               |                                             |

BOM Config

EVT

UMA only:

UMA@, RT@, ANX@, M3@, 930@, APULVDS@, JE@

DISO only:

VGA@, DISO@, VGALVDS@, SEYM@ or WHI@, VAN@, 128@(With WHI@), NOGRAN@, NOBACO@, M3@, 930@, JE@

PX

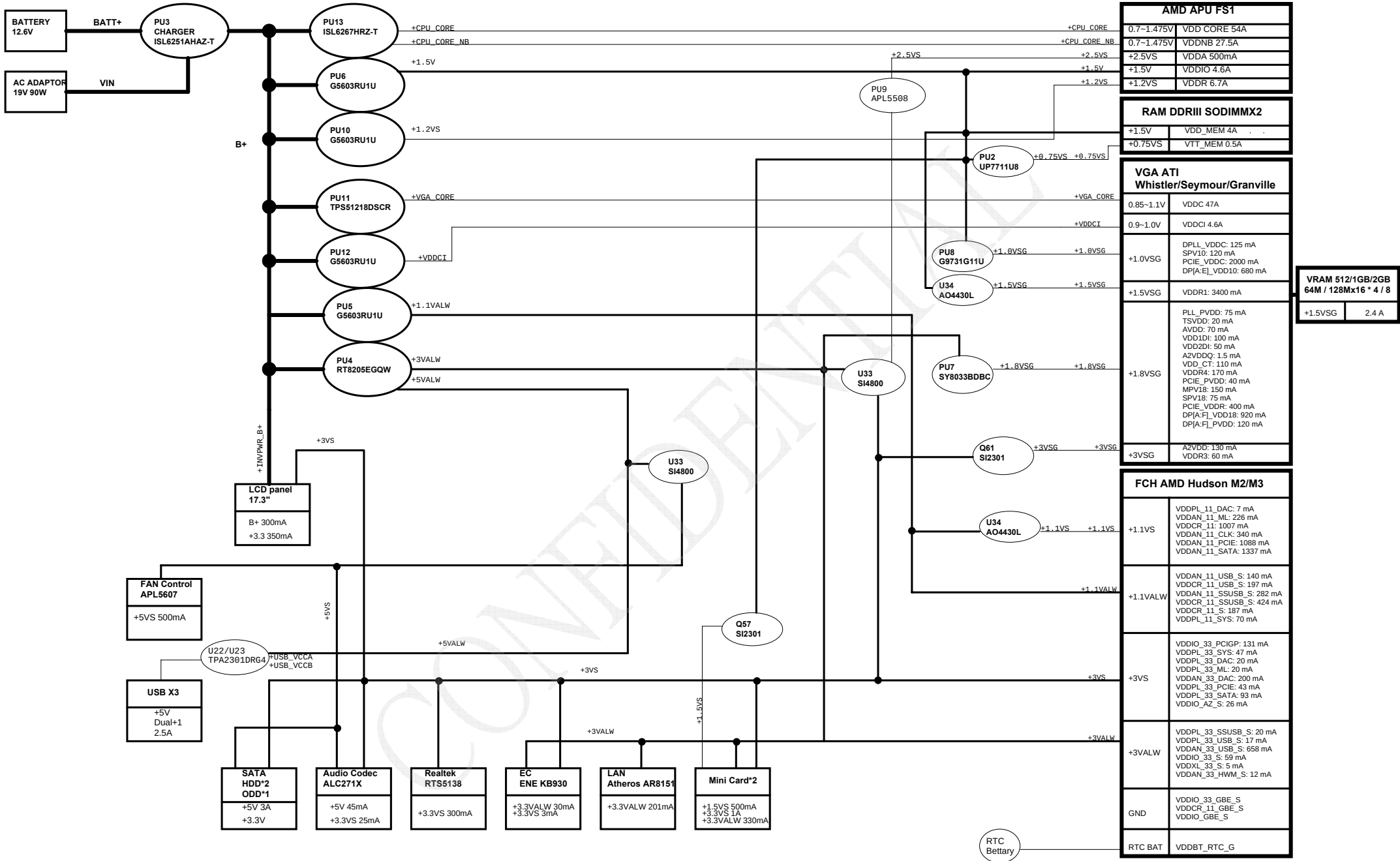
UMA@, VGA@, PX@, SEYM@ or WHI@, VAN@, 128@(With WHI@), NOGRAN@, RT@, ANX@, APULVDS@, BACO@, M3@, 930@, JE@

PROJECT ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 0        |              |
| 1        |              |
| 2        |              |
| 3        |              |
| 4        |              |
| 5        |              |
| 6        |              |
| 7        |              |

BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 0        |              |
| 1        | 0.1(EVT)     |
| 2        | 0.2(DVT)     |
| 3        |              |
| 4        |              |
| 5        |              |
| 6        |              |
| 7        |              |



<13> PCIE\_GTX\_C\_FRX\_P[0..15] <13> PCIE\_GTX\_C\_FRX\_N[0..15]

PCIE\_FTX\_C\_GRX\_P[0..15] <13> PCIE\_FTX\_C\_GRX\_N[0..15] <13>

## APU To HDMI

PCIE\_FTX\_GRX\_P[12..15] <24> PCIE\_FTX\_GRX\_N[12..15] <24>

| JCPU1A             |     | CONN@       |             |
|--------------------|-----|-------------|-------------|
| PCI EXPRESS        |     | PCI EXPRESS |             |
| PCIE_GTX_C_FRX_P0  | AA8 | P_GFX_RXP0  | P_GFX_TXP0  |
| PCIE_GTX_C_FRX_N0  | AA9 | P_GFX_RXN0  | P_GFX_TXN0  |
| PCIE_GTX_C_FRX_P1  | Y7  | P_GFX_RXP1  | P_GFX_TXP1  |
| PCIE_GTX_C_FRX_N1  | Y8  | P_GFX_RXN1  | P_GFX_TXN1  |
| PCIE_GTX_C_FRX_P2  | W5  | P_GFX_RXP2  | P_GFX_TXP2  |
| PCIE_GTX_C_FRX_N2  | W6  | P_GFX_RXN2  | P_GFX_TXN2  |
| PCIE_GTX_C_FRX_P3  | W8  | P_GFX_RXP3  | P_GFX_TXP3  |
| PCIE_GTX_C_FRX_N3  | W9  | P_GFX_RXN3  | P_GFX_TXN3  |
| PCIE_GTX_C_FRX_P4  | V7  | P_GFX_RXP4  | P_GFX_TXP4  |
| PCIE_GTX_C_FRX_N4  | V8  | P_GFX_RXN4  | P_GFX_TXN4  |
| PCIE_GTX_C_FRX_P5  | U5  | P_GFX_RXP5  | P_GFX_TXP5  |
| PCIE_GTX_C_FRX_N5  | U6  | P_GFX_RXN5  | P_GFX_TXN5  |
| PCIE_GTX_C_FRX_P6  | U8  | P_GFX_RXP6  | P_GFX_TXP6  |
| PCIE_GTX_C_FRX_N6  | U9  | P_GFX_RXN6  | P_GFX_TXN6  |
| PCIE_GTX_C_FRX_P7  | T7  | P_GFX_RXP7  | P_GFX_TXP7  |
| PCIE_GTX_C_FRX_N7  | T8  | P_GFX_RXN7  | P_GFX_TXN7  |
| PCIE_GTX_C_FRX_P8  | R5  | P_GFX_RXP8  | P_GFX_TXP8  |
| PCIE_GTX_C_FRX_N8  | R6  | P_GFX_RXN8  | P_GFX_TXN8  |
| PCIE_GTX_C_FRX_P9  | R8  | P_GFX_RXP9  | P_GFX_TXP9  |
| PCIE_GTX_C_FRX_N9  | R9  | P_GFX_RXN9  | P_GFX_TXN9  |
| PCIE_GTX_C_FRX_P10 | P7  | P_GFX_RXP10 | P_GFX_TXP10 |
| PCIE_GTX_C_FRX_N10 | P8  | P_GFX_RXN10 | P_GFX_TXN10 |
| PCIE_GTX_C_FRX_P11 | N5  | P_GFX_RXP11 | P_GFX_TXP11 |
| PCIE_GTX_C_FRX_N11 | N6  | P_GFX_RXN11 | P_GFX_TXN11 |
| PCIE_GTX_C_FRX_P12 | N8  | P_GFX_RXP12 | P_GFX_TXP12 |
| PCIE_GTX_C_FRX_N12 | N9  | P_GFX_RXN12 | P_GFX_TXN12 |
| PCIE_GTX_C_FRX_P13 | M7  | P_GFX_RXP13 | P_GFX_TXP13 |
| PCIE_GTX_C_FRX_N13 | M8  | P_GFX_RXN13 | P_GFX_TXN13 |
| PCIE_GTX_C_FRX_P14 | L5  | P_GFX_RXP14 | P_GFX_TXP14 |
| PCIE_GTX_C_FRX_N14 | L6  | P_GFX_RXN14 | P_GFX_TXN14 |
| PCIE_GTX_C_FRX_P15 | L8  | P_GFX_RXP15 | P_GFX_TXP15 |
| PCIE_GTX_C_FRX_N15 | L9  | P_GFX_RXN15 | P_GFX_TXN15 |

|                        |     |            |            |
|------------------------|-----|------------|------------|
| <34> PCIE_DTX_C_FRX_P0 | AC5 | P_GPP_RXP0 | P_GPP_TXP0 |
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| <33> PCIE_DTX_C_FRX_P1 | AC8 | P_GPP_RXP1 | P_GPP_TXP1 |
| <33> PCIE_DTX_C_FRX_N1 | AC9 | P_GPP_RXN1 | P_GPP_TXN1 |
| <33> PCIE_DTX_C_FRX_P2 | AB7 | P_GPP_RXP2 | P_GPP_TXP2 |
| <33> PCIE_DTX_C_FRX_N2 | AB8 | P_GPP_RXN2 | P_GPP_TXN2 |
|                        | AA5 | P_GPP_RXP3 | P_GPP_TXP3 |
|                        | AA6 | P_GPP_RXN3 | P_GPP_TXN3 |

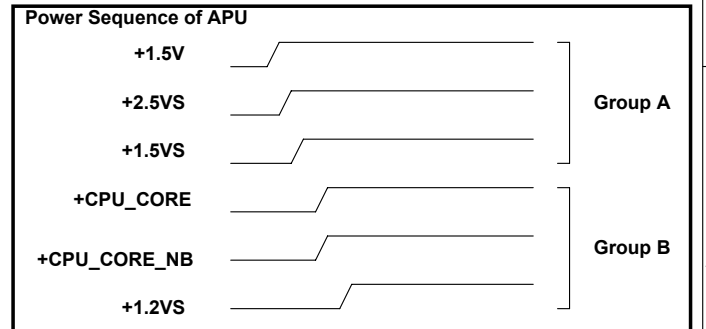
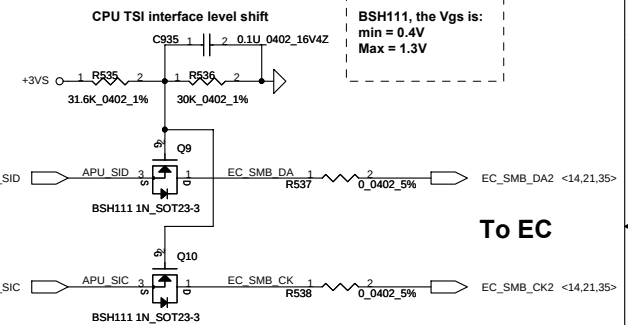
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| <26> UMI_MTX_C_FRX_N0 | AE7 | P_UMI_RXN0 | P_UMI_TXN0 |
| <26> UMI_MTX_C_FRX_P1 | AE6 | P_UMI_RXP1 | P_UMI_TXP1 |
| <26> UMI_MTX_C_FRX_N1 | AE5 | P_UMI_RXN1 | P_UMI_TXN1 |
| <26> UMI_MTX_C_FRX_P2 | AE9 | P_UMI_RXP2 | P_UMI_TXP2 |
| <26> UMI_MTX_C_FRX_N2 | AE8 | P_UMI_RXN2 | P_UMI_TXN2 |
| <26> UMI_MTX_C_FRX_P3 | AD8 | P_UMI_RXP3 | P_UMI_TXP3 |
| <26> UMI_MTX_C_FRX_N3 | AD7 | P_UMI_RXN3 | P_UMI_TXN3 |

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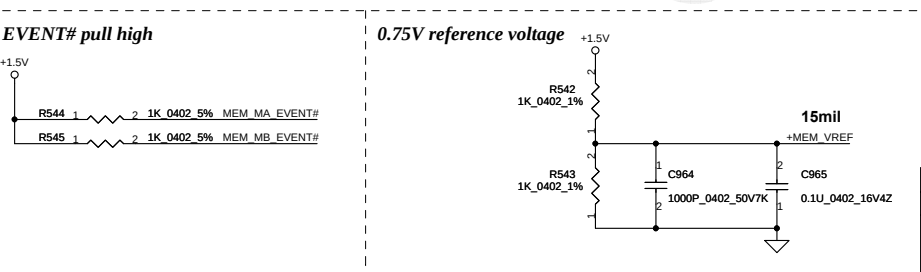
AMD\_TOPEDO\_FS-1

To VGA

2  
1  
0  
To HDMI  
CLK



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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Document Number          | 4019BN                      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Date                     | Thursday, February 24, 2011 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Sheet                    | 6 of 50                     |



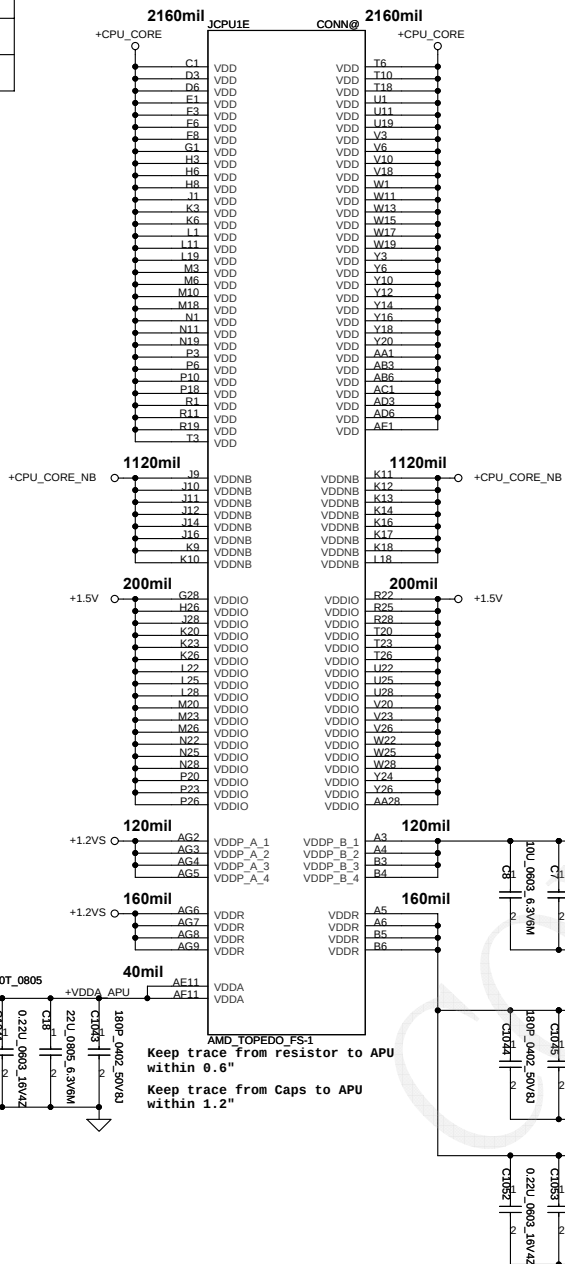
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                             |                    |            | 4019B                    |                    |
| Date:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Thursday, February 24, 2011 | Sheet              | 9          | of                       | 50                 |



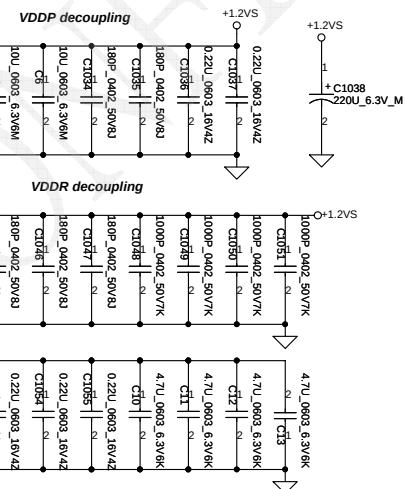
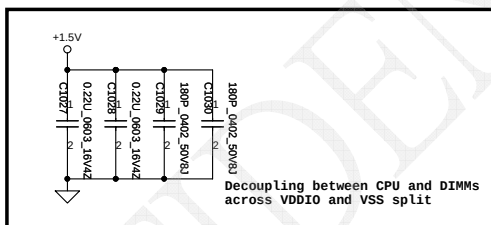
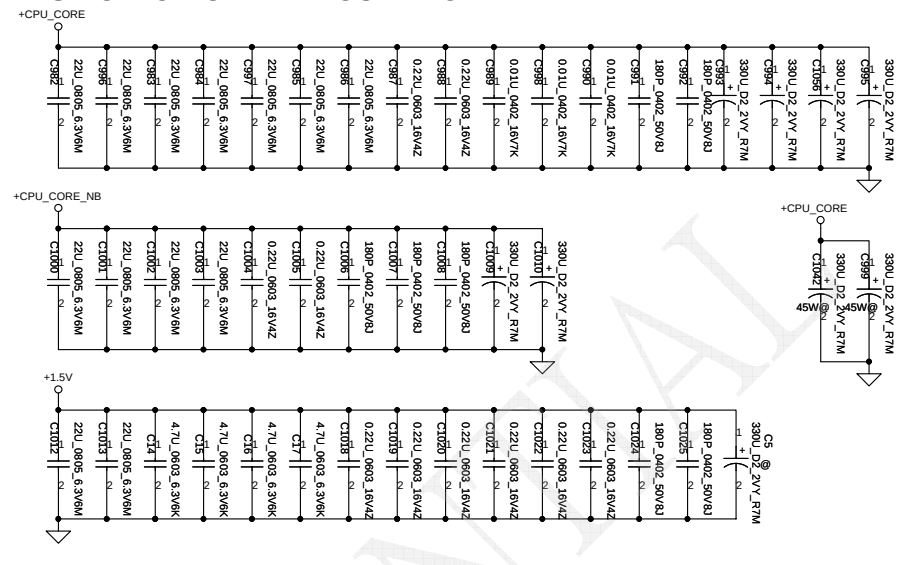


| Power Name            | Consumption      |
|-----------------------|------------------|
| VDD<br>+CPU_CORE      | <b>54A</b>       |
| VDDNB<br>+CPU_CORE_NB | <b>27.5A</b>     |
| VDDIO<br>+1.5V        | <b>4.6A</b>      |
| VDDP / VDDR<br>+1.2VS | <b>3A / 3.7A</b> |
| VDDA<br>+2.5VS        | <b>0.5A</b>      |

|           |           |
|-----------|-----------|
| CORE_NB   | CPU_CORE  |
| 330uF X 2 | 330uF X 4 |
| 22uF X 4  | 22uF X 11 |



## CPU BOTTOM SIDE DECOUPLING



**Demo Board Capacitor (include PWM side)**

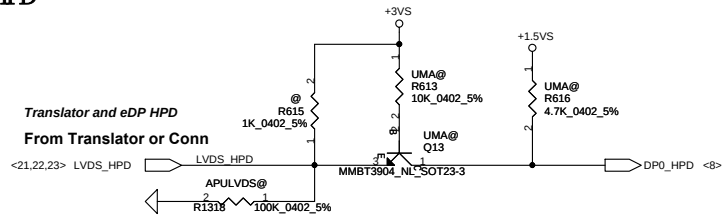
| CPU_CORE   | CORE_NB    | VDDIO_SUS  | VDDIO_SUS | VDDP/R_PWM | VDDP       | VDDR       |
|------------|------------|------------|-----------|------------|------------|------------|
| 470uF x 6  | 470uF x 4  | (CPU side) | (DIMM x2) | 470uF x 2  | 10uF x 3   | 4.7uF x 4  |
| 22uF x 9   | 22uF x 6   | 680uF x 1  | 100uF x 4 | 10uF x 1   | 0.22uF x 2 | 0.22uF x 4 |
| 0.22uF x 2 | 0.22uF x 1 | 330uF x 1  | 0.1uF     |            | 180pF x 2  | 1nF x 4    |
| 180uF x 2  | 180uF x 3  | 22uF x 3   |           |            |            | 180pF x 4  |
| 10nF x 3   |            | 4.7uF x 4  |           |            |            |            |
|            |            | 0.22uF x 6 |           |            |            |            |
|            |            | 180pF x 4  |           |            |            |            |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                             |                    |            |                          |                    |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|--------------------|------------|--------------------------|--------------------|
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| Date:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Thursday, February 24, 2011 | Sheet              | 9          | of                       | 50                 |

# HPD

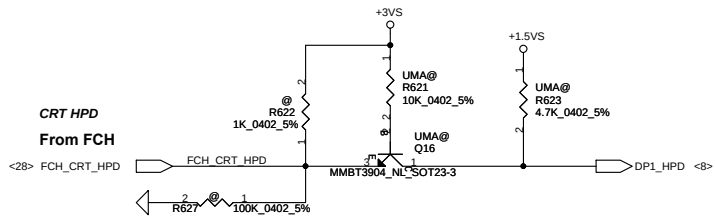
## Translator and eDP HPD

### From Translator or Conn



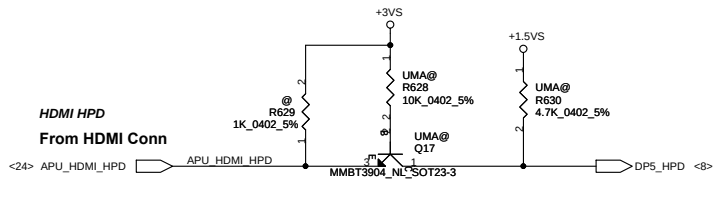
## CRT HPD

### From FCH

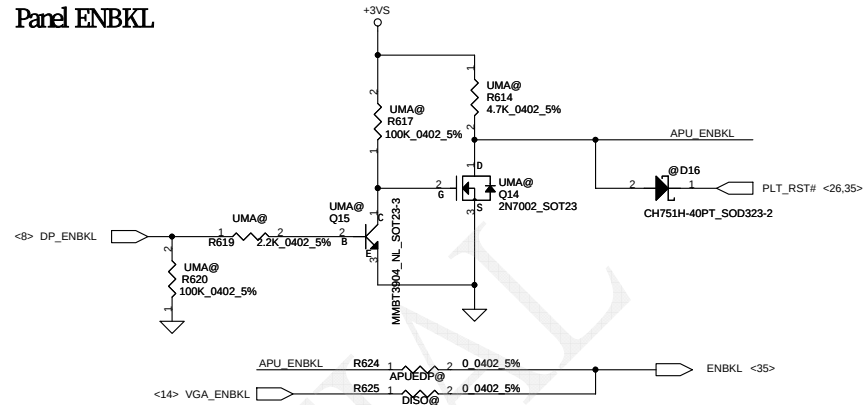


## HDMI HPD

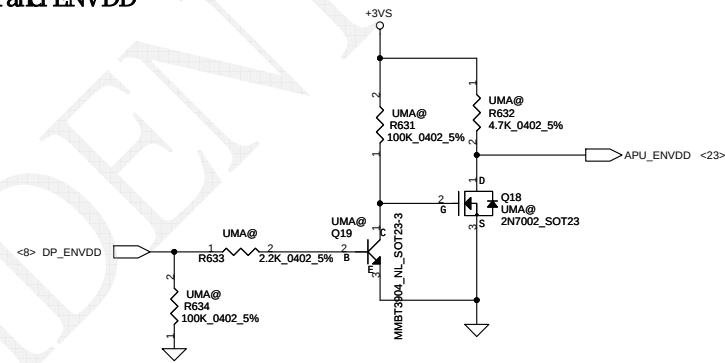
### From HDMI Conn



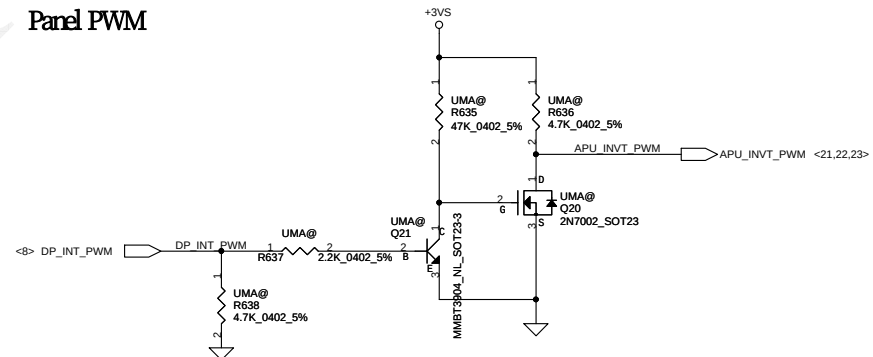
# Panel ENBKL



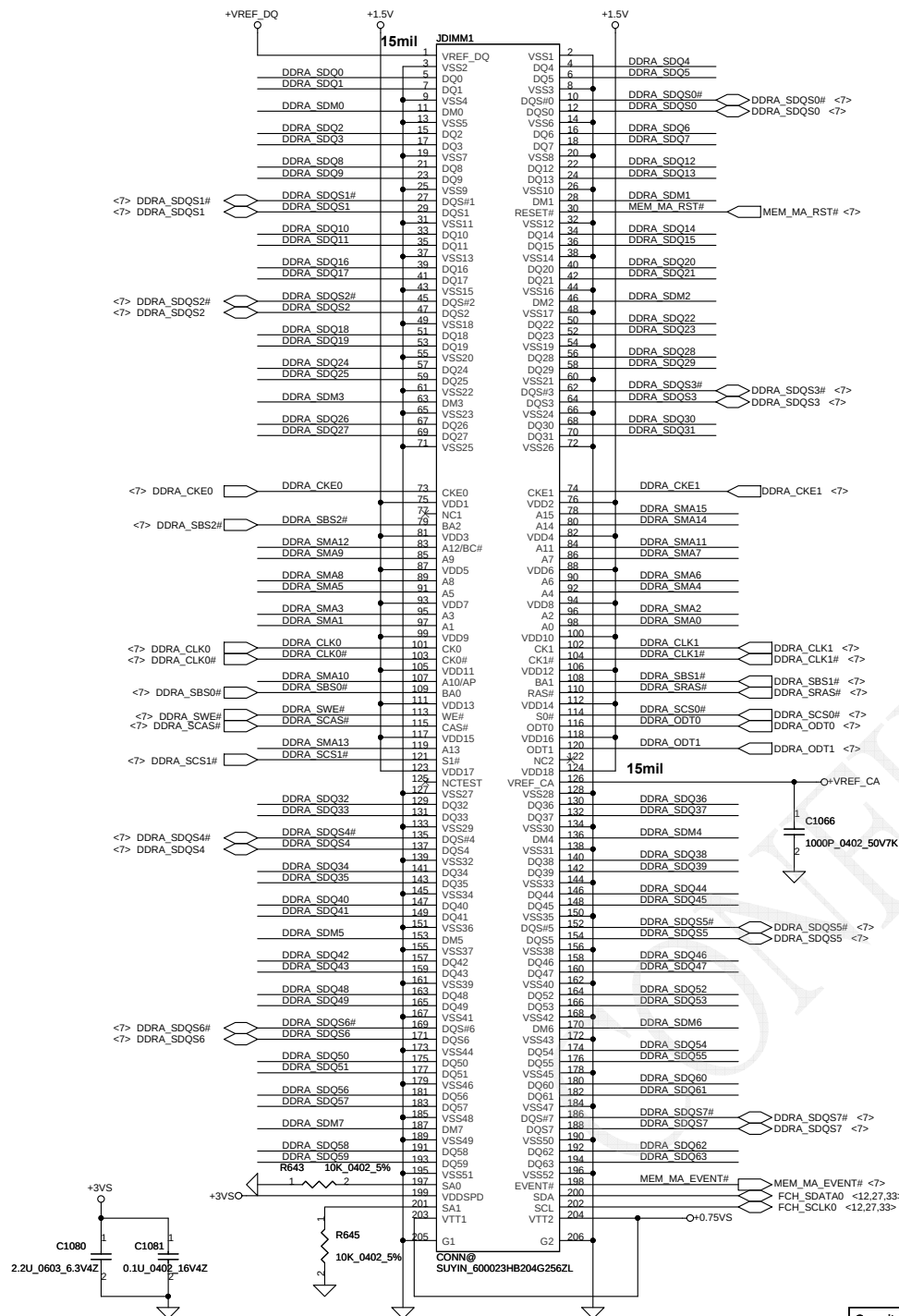
# Panel ENVDD



# Panel PWM



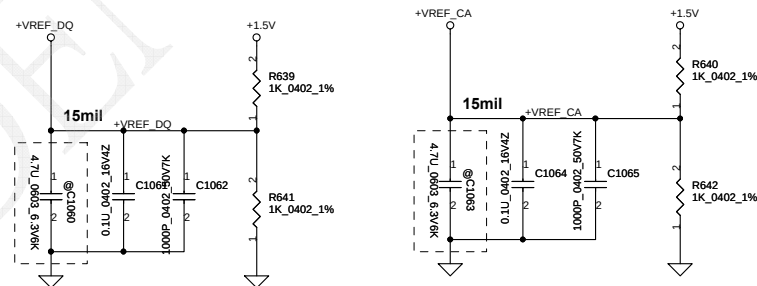
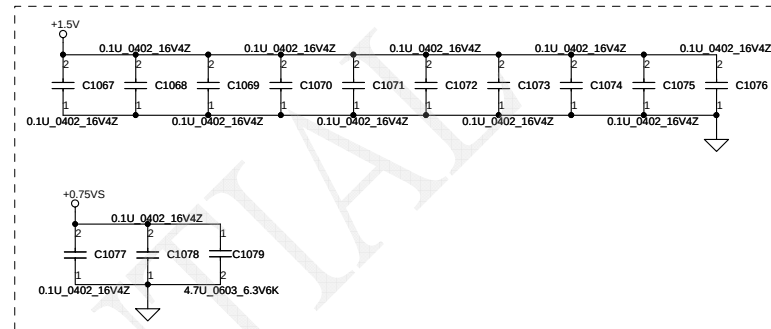
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |            |  |                             |                |
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| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |  | Compal Secret Data |  |                 |  |            |  |                             |                |
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**DIMM\_A STD H:8mm** Change to SUYIN  
 <Address: 00> SP07000N500

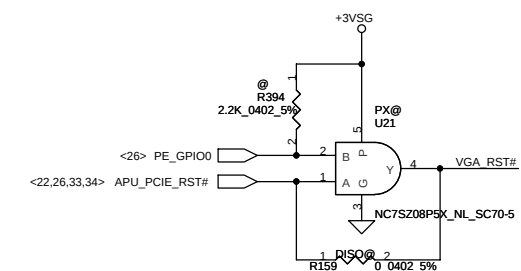
DDR4 SDQ[0.63] <7>  
 DDR4 SDQ[0.7] <7>  
 DDR4 SMA[0.15] <7>

Place near DIMM1



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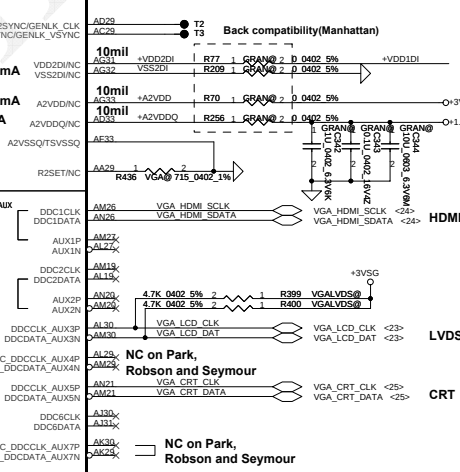
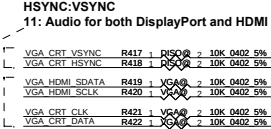
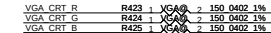
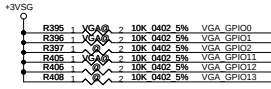
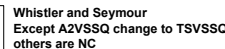
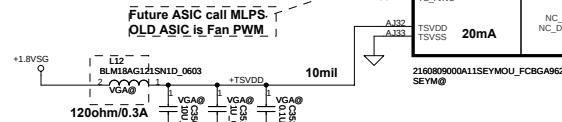
216-0810005 A11  
WHISTLER PRO M2 A11:  
SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |                             |                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|--------------------------|-----------------------------|----------------|
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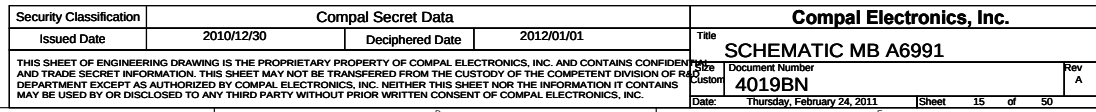
## Global Swap Leverage

**Park 9C pins**

Diagram showing the pinout of the Park 9C connector, including signals like VGA, GPU, and other peripherals. The diagram includes a scale bar indicating 70mm and 100mm.



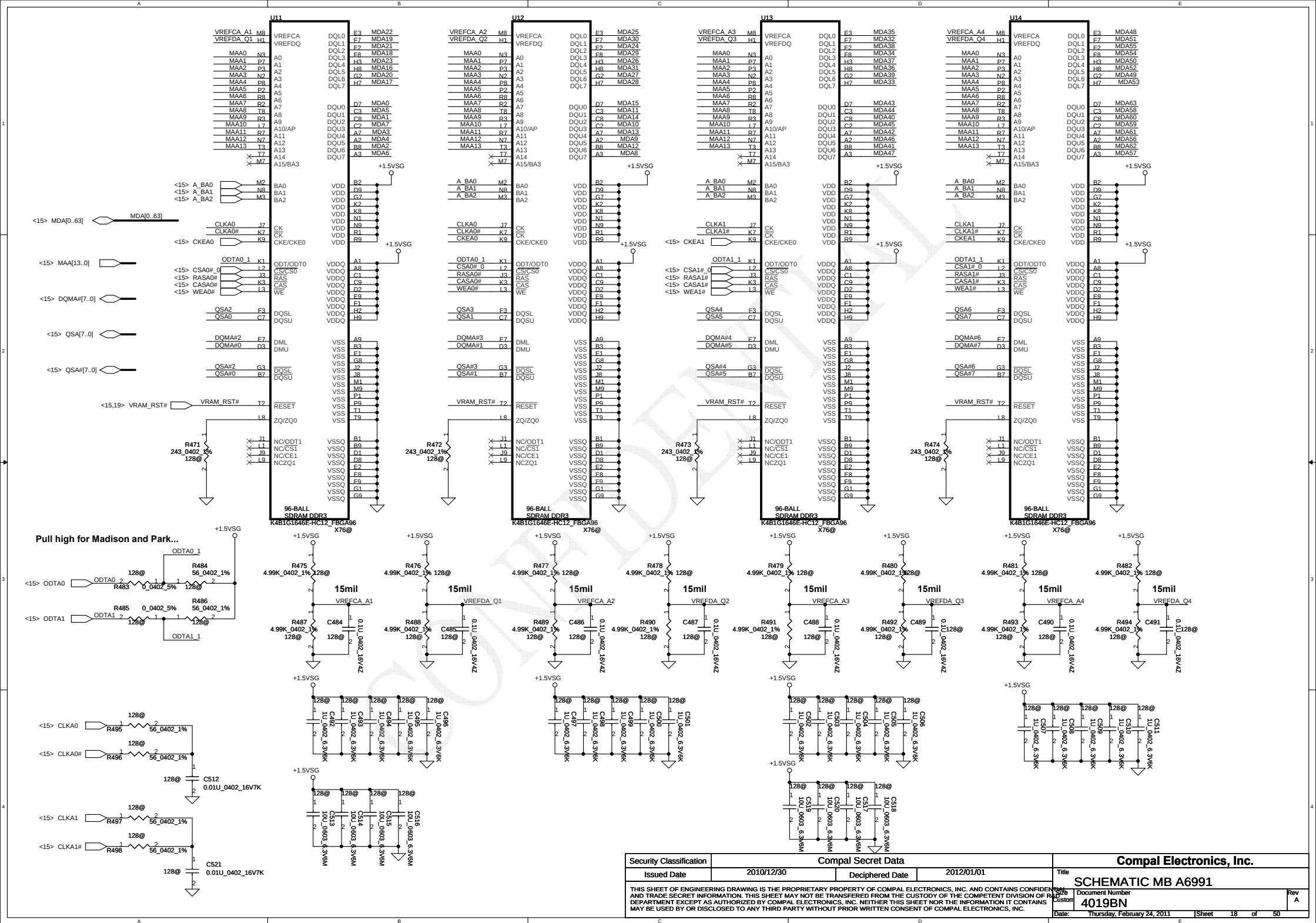
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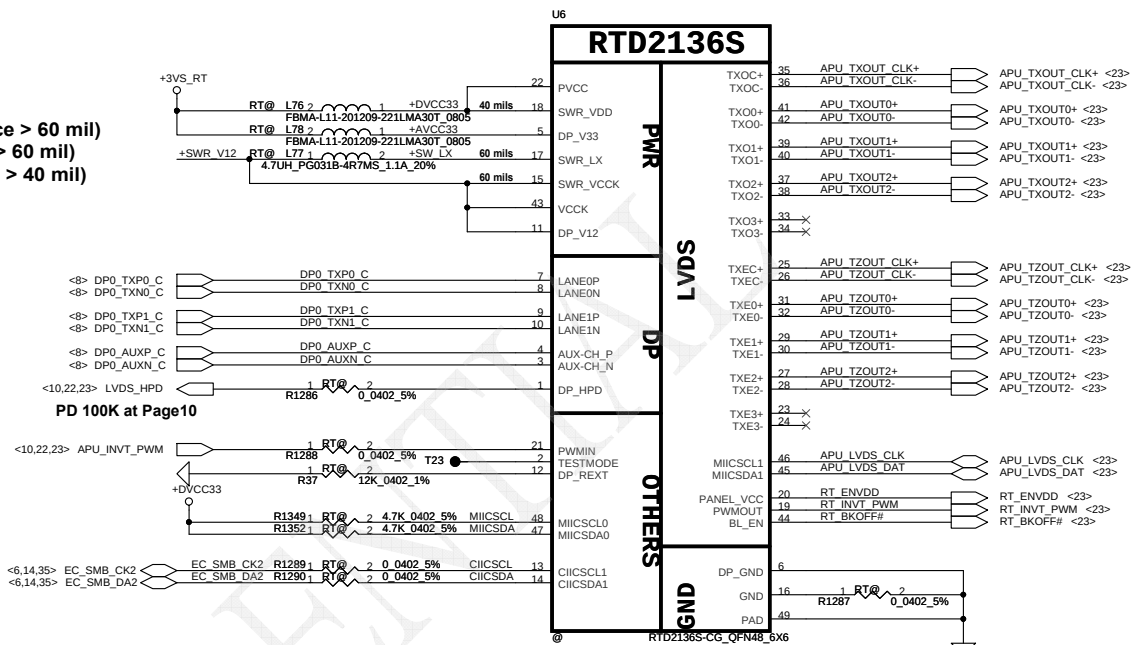
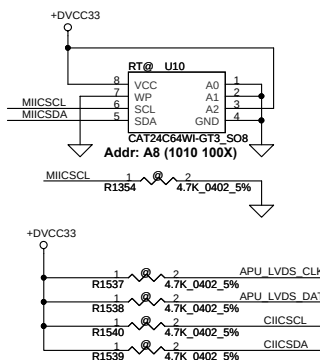
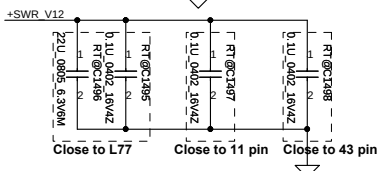
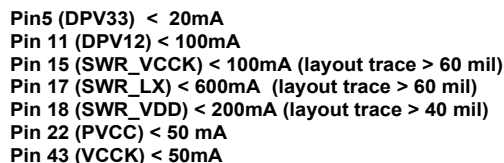






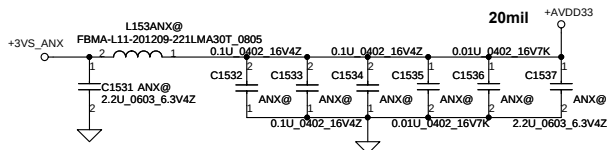






|       |                |   |          |   |   |            |                |
|-------|----------------|---|----------|---|---|------------|----------------|
| <<2>> | ANX LVDS_CLK   | 0 | 0402 596 | 2 | 1 | R1294 ANX@ | APU LVDS CLK   |
| <<2>> | ANX LVDS_DAT   | 0 | 0402 596 | 2 | 1 | R1295 ANX@ | APU LVDS DAT   |
| <<2>> | ANX TXOUT2+    | 0 | 0402 596 | 2 | 1 | R1296 ANX@ | APU TXOUT2+    |
| <<2>> | ANX TXOUT2-    | 0 | 0402 596 | 2 | 1 | R1297 ANX@ | APU TXOUT2-    |
| <<2>> | ANX TXOUT1+    | 0 | 0402 596 | 2 | 1 | R1298 ANX@ | APU TXOUT1+    |
| <<2>> | ANX TXOUT1-    | 0 | 0402 596 | 2 | 1 | R1299 ANX@ | APU TXOUT1-    |
| <<2>> | ANX TXOUT0+    | 0 | 0402 596 | 2 | 1 | R1300 ANX@ | APU TXOUT0+    |
| <<2>> | ANX TXOUT0-    | 0 | 0402 596 | 2 | 1 | R1301 ANX@ | APU TXOUT0-    |
| <<2>> | ANX TXOUT_CLK+ | 0 | 0402 596 | 2 | 1 | R1302 ANX@ | APU TXOUT CLK+ |
| <<2>> | ANX TXOUT_CLK- | 0 | 0402 596 | 2 | 1 | R1303 ANX@ | APU TXOUT CLK- |
| <<2>> | ANX TZOUT0+    | 0 | 0402 596 | 2 | 1 | R1304 ANX@ | APU TZOUT0+    |
| <<2>> | ANX TZOUT0-    | 0 | 0402 596 | 2 | 1 | R1305 ANX@ | APU TZOUT0-    |
| <<2>> | ANX TZOUT1+    | 0 | 0402 596 | 2 | 1 | R1306 ANX@ | APU TZOUT1+    |
| <<2>> | ANX TZOUT1-    | 0 | 0402 596 | 2 | 1 | R1307 ANX@ | APU TZOUT1-    |
| <<2>> | ANX TZOUT2+    | 0 | 0402 596 | 2 | 1 | R1308 ANX@ | APU TZOUT2+    |
| <<2>> | ANX TZOUT2-    | 0 | 0402 596 | 2 | 1 | R1309 ANX@ | APU TZOUT2-    |
| <<2>> | ANX TZOUT_CLK+ | 0 | 0402 596 | 2 | 1 | R1310 ANX@ | APU TZOUT CLK+ |
| <<2>> | ANX TZOUT_CLK- | 0 | 0402 596 | 2 | 1 | R1311 ANX@ | APU TZOUT CLK- |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                 |                    |       |
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| Date: Thursday, February 24, 2011                                                                                                                                                                                                                                                                                                                                                                                                                             |                    |                 |            | Sheet           | 21                 | of 50 |

[illegible]

Place via on each trace bus and let resistor very close the via.

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                             |                    |          |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|-----------------------------|--------------------|----------|
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### Panel LCDVDD Control

The schematic diagram illustrates the Panel LCDVDD Control circuit. It features two MOSFETs, Q140A and Q140B, both of type DMN66D0LDW-7\_SOT363-6. The gates of these MOSFETs are driven by a +3V3 supply through a 60mils trace and a 4.7uF capacitor (C1538 for Q140A and C1542 for Q140B). The gates are also connected to a common node that is further connected to a 10uF capacitor (C1540) and a 0.1uF capacitor (C1543). The drains of both MOSFETs are connected to a common node that is also connected to a 10uF capacitor (C1539) and a 0.1uF capacitor (C1540). The sources of both MOSFETs are connected to ground. The circuit is labeled with component values and part numbers, and includes a note 'Place near LVDS Conn'.

### Panel Backlight Control

<21> RT\_BKOFF# RT\_BKOFF# R1357 1 RT\_Q 2 0 0402 5% DISPOFF#

<22> ANX\_BKOFF# ANX\_BKOFF# R644 1 ANX\_Q 2 0 0402 5%

From EC <35> BKOFF# BKOFF# R1331 1 DIS\_Q 2 0 0402 5%

R1332 1 2 10K 0402 5%

UMA eDP also need to use R1331

C1544 680P\_0402\_50V7K +INVWPR\_B+ 40mils

C1545 68P\_0402\_50V8J

L154 2 1 FBMA-L11-201209-221LMA30T\_0805

L155 2 1 L2UH\_1231AS-H-1R2N-P3\_2.9A\_30%

L156 2 1 FBMA-L11-201209-221LMA30T\_0805

L157 2 1 FBMA-L11-201209-221LMA30T\_0805

B+

### Panel PWM Control

### eDP HDP for APU and VGA

The diagram illustrates the eDP HDP for APU and VGA. It shows two parallel signal paths. The left path is for VGA, featuring a resistor R1342 connected to <14> VGA\_EDP\_HPD and R1343 connected to <10,21,22> LVDS\_HPD. The right path is for eDP, featuring a resistor R1344 connected to EDP\_HPD. Both paths include a 200K\_0402\_5% resistor and a 3V5 supply. The components are labeled with their values and footprints: R1342 (2 0\_0402\_5%), R1343 (2 0\_0402\_5%), R1344 (5 2 200K\_0402\_5%), R1345 EDP@ (200K\_0402\_5%), Q142A EDP@ (2), Q142B EDP@ (2), and R1340 10K\_0402\_5% (2). The components are connected to a 3V5 supply and a ground symbol.

### Translator LVDS Output

| Translator LVDS Output |        |   |                    | BOM Option for APU eDP |         |       |                 |
|------------------------|--------|---|--------------------|------------------------|---------|-------|-----------------|
| TXCLK+                 | 2      | 3 | APULVDS@           | APU_TXOUT_CLK+ <2>     | APUEDP@ | R1409 | 0.1U_0402_16V7K |
| TXCLK-                 | 1      | 4 |                    | APU_TXOUT_CLK- <2>     | APUEDP@ | R1410 | 0.1U_0402_16V7K |
| TXOUT2+                | 2      | 3 | 0.0404 4P2R 5%     | APU_TXOUT2+ <2>        | APUEDP@ | R1411 | 0.1U_0402_16V7K |
| TXOUT2-                | 1      | 4 | 0.0402 5% APULVDS@ | APU_TXOUT2- <2>        | APUEDP@ | R1412 | 0.1U_0402_16V7K |
| TXOUT1+                | 2      | 3 | 0.0402 5% APULVDS@ | APU_TXOUT1+ <2>        | APUEDP@ | R1413 | 0.1U_0402_16V7K |
| TXOUT1-                | 1      | 4 | 0.0402 5% APULVDS@ | APU_TXOUT1- <2>        | APUEDP@ | R1414 | 0.1U_0402_16V7K |
| TXOUT0+                | 2      | 3 | APULVDS@           | APU_TXOUT0+ <2>        | APUEDP@ | R1415 | 0.1U_0402_16V7K |
| TXOUT0-                | 1      | 4 | 0.0404 4P2R 5%     | APU_TXOUT0- <2>        | APUEDP@ | R1416 | 0.1U_0402_16V7K |
| TZCLK+                 | 2      | 3 | APULVDS@           | APU_TZOUT_CLK+ <2>     | APUEDP@ | R1417 | 0.1U_0402_16V7K |
| TZCLK-                 | 1      | 4 | 0.0404 4P2R 5%     | APU_TZOUT_CLK- <2>     | APUEDP@ | R1418 | 0.1U_0402_16V7K |
| TZOUT2+                | 2      | 3 | APULVDS@           | APU_TZOUT2+ <2>        | APUEDP@ | R1419 | 0.1U_0402_16V7K |
| TZOUT2-                | 1      | 4 | 0.0404 4P2R 5%     | APU_TZOUT2- <2>        | APUEDP@ | R1420 | 0.1U_0402_16V7K |
| TZOUT1+                | 2      | 3 | APULVDS@           | APU_TZOUT1+ <2>        | APUEDP@ | R1421 | 0.1U_0402_16V7K |
| TZOUT1-                | 1      | 4 |                    | APU_TZOUT1- <2>        | APUEDP@ | R1422 | 0.1U_0402_16V7K |
| TZOUT0+                | 2      | 3 | 0.0404 4P2R 5%     | APU_TZOUT0+ <2>        | APUEDP@ | R1423 | 0.1U_0402_16V7K |
| TZOUT0-                | 1      | 4 | APULVDS@           | APU_TZOUT0- <2>        | APUEDP@ | R1424 | 0.1U_0402_16V7K |
|                        |        |   | 0.0404 4P2R 5%     |                        |         |       |                 |
| I2CC_SDA               | R14141 | 2 | 0.0402 5% APULVDS@ | APU_LVDS_DAT <2>       |         |       |                 |
| I2CC_SCL               | R14151 | 2 | 0.0402 5% APULVDS@ | APU_LVDS_CLK <2>       |         |       |                 |

**BOM Option for APU eDP**

|        |                 |  |
|--------|-----------------|--|
|        | APUEDP@         |  |
| R1409  | 0.1U_0402_16V7K |  |
| 21> 1> |                 |  |
|        | APUEDP@         |  |
| R1410  | 0.1U_0402_16V7K |  |
|        |                 |  |
|        | APUEDP@         |  |
| R1411  | 0.1U_0402_16V7K |  |
|        |                 |  |
|        | APUEDP@         |  |
| R1412  | 0.1U_0402_16V7K |  |
|        |                 |  |
|        | APUEDP@         |  |
| R1414  | 0.1U_0402_16V7K |  |
|        |                 |  |
| 21> 1> |                 |  |
|        | APUEDP@         |  |
| R1415  | 0.1U_0402_16V7K |  |

## VGA LVDS Output (Reserve eDP)

**BOM Option for VGA eDP**

The diagram illustrates the pin configuration for the VGA LVDS Output (Reserve eDP) option. It shows the connections for various signals and their corresponding pins on the component.

**Pin Connections:**

- R1348:**
  - TXCLK- (Pin 2) to TXCLK+ (Pin 3)
  - TXCLK- (Pin 1) to TXCLK+ (Pin 4)
- R1350:**
  - eDP\_TX0N (Pin 2) to TXOUT2- (Pin 3)
  - eDP\_TX0P (Pin 1) to TXOUT2+ (Pin 4)
- R1351:**
  - eDP\_TX1N (Pin 2) to TXOUT1- (Pin 3)
  - eDP\_TX1P (Pin 1) to TXOUT1+ (Pin 4)
- R1353:**
  - TXOUT0- (Pin 2) to TXOUT0+ (Pin 3)
  - TXOUT0- (Pin 1) to TXOUT0+ (Pin 4)
- R1358:**
  - TZCLK- (Pin 2) to TZCLK+ (Pin 3)
  - TZCLK- (Pin 1) to TZCLK+ (Pin 4)
- R1359:**
  - TZOUT- (Pin 2) to TZOUT+ (Pin 3)
  - TZOUT- (Pin 1) to TZOUT+ (Pin 4)
- R1361:**
  - TZOUT0- (Pin 2) to TZOUT0+ (Pin 3)
  - TZOUT0- (Pin 1) to TZOUT0+ (Pin 4)

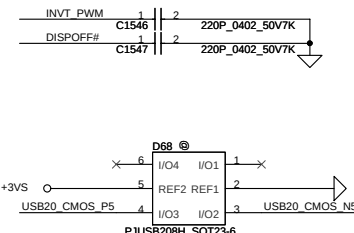
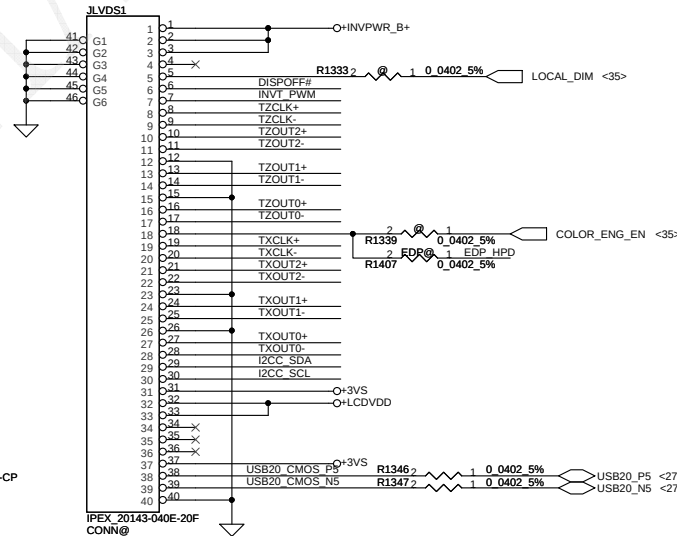
**Signal Connections:**

- VGA\_TXCLK- <13> to TXCLK- (Pin 2)
- VGA\_TXCLK+ <13> to TXCLK+ (Pin 3)
- VGA\_TXOUT2- <13> to TXOUT2- (Pin 2)
- VGA\_TXOUT2+ <13> to TXOUT2+ (Pin 1)
- VGA\_TXOUT1+ <13> to TXOUT1+ (Pin 4)
- VGA\_TXOUT1- <13> to TXOUT1- (Pin 2)
- VGA\_TXOUT0- <13> to TXOUT0- (Pin 2)
- VGA\_TXOUT0+ <13> to TXOUT0+ (Pin 1)
- VGA\_TZCLK- <13> to TZCLK- (Pin 2)
- VGA\_TZCLK+ <13> to TZCLK+ (Pin 3)
- VGA\_TZOUT2- <13> to TZOUT2- (Pin 2)
- VGA\_TZOUT2+ <13> to TZOUT2+ (Pin 1)
- VGA\_TZOUT1+ <13> to TZOUT1+ (Pin 4)
- VGA\_TZOUT1- <13> to TZOUT1- (Pin 2)
- VGA\_TZOUT0+ <13> to TZOUT0+ (Pin 3)
- VGA\_TZOUT0- <13> to TZOUT0- (Pin 1)
- VGA\_LCD\_DAT <14> to R1358 (Pin 2)
- VGA\_LCD\_CLK <14> to R1359 (Pin 2)

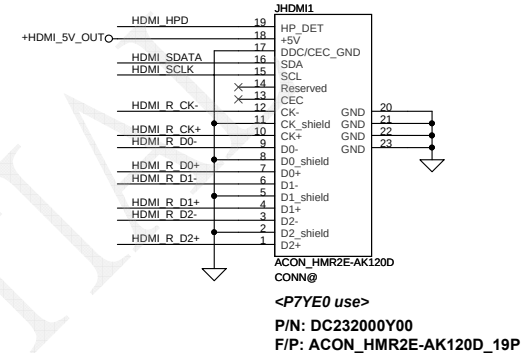
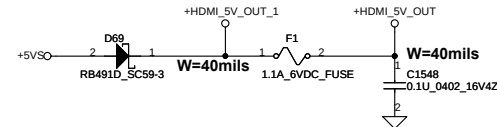
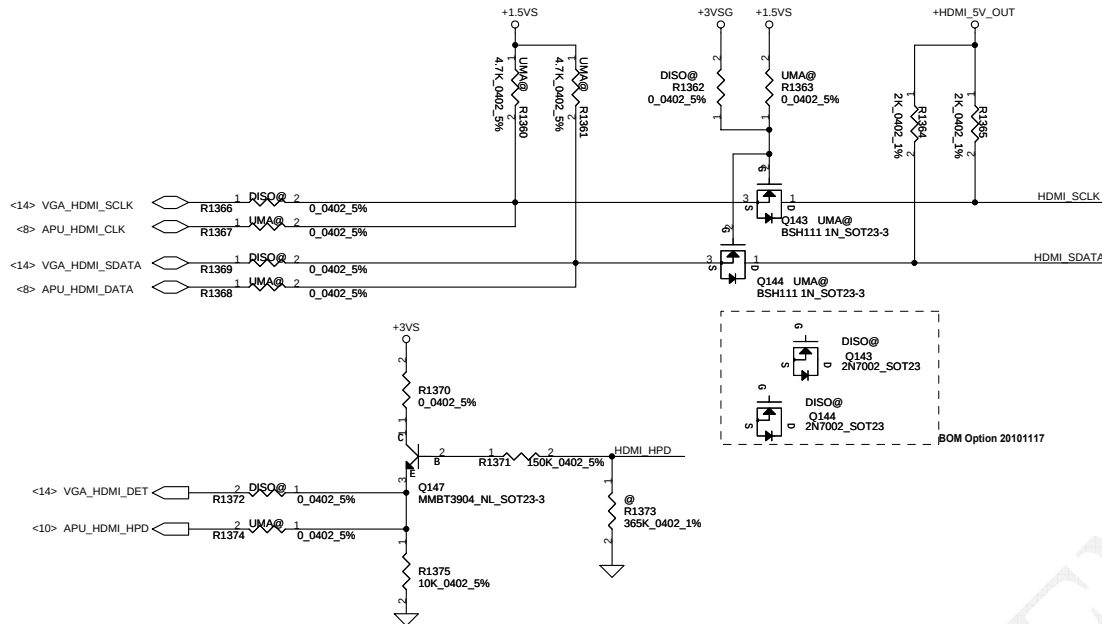
|       |                                  |                      |                    |                            |                   |             |                                                            |                                      |                                      |
|-------|----------------------------------|----------------------|--------------------|----------------------------|-------------------|-------------|------------------------------------------------------------|--------------------------------------|--------------------------------------|
| R1348 | VGAEDP@<br>[N] [I0_U_0402_16V7K] |                      | TXCLK-<br>TXCLK+   | 2<br>1                     | [W]               | 3           | VGALVDS@                                                   |                                      | VGA_TXCLK- <13><br>VGA_TXCLK+ <13>   |
| R1350 | VGAEDP@<br>[N] [I0_U_0402_16V7K] | eDP_TX0N<br>eDP_TX0P | TXOUT2+<br>TXOUT2+ | RP2<br>R1348.1<br>R1350.1  | [W]<br>[W]        | 2<br>2      | 0_0404 4P2R 5%<br>0_0402 5% VGALVDS@                       |                                      | VGA_TXOUT2- <13><br>VGA_TXOUT2+ <13> |
| R1351 | VGAEDP@<br>[N] [I0_U_0402_16V7K] | eDP_TX1P<br>eDP_TX1N | TXOUT1+<br>TXOUT1- | R1351.1<br>R1353.1         | [W]<br>[W]        | 2<br>2      | 0_0402 5% VGALVDS@<br>0_0402 5% VGALVDS@                   |                                      | VGA_TXOUT1+ <13><br>VGA_TXOUT1- <13> |
| R1353 | VGAEDP@<br>[N] [I0_U_0402_16V7K] |                      | TXOUT0-<br>TXOUT0+ | [W]<br>[W]                 | 3<br>4            | VGALVDS@    |                                                            | VGA_TXOUT0- <13><br>VGA_TXOUT0+ <13> |                                      |
| R1358 | VGAEDP@<br>[N] [I0_U_0402_16V7K] |                      | TZCLK-<br>TZCLK+   | RP6                        | [W]<br>[W]        | 2<br>1      | 0_0404 4P2R 5%<br>VGALVDS@                                 |                                      | VGA_TZCLK- <13><br>VGA_TZCLK+ <13>   |
| R1359 | VGAEDP@<br>[N] [I0_U_0402_16V7K] |                      | TZOUT2-<br>TZOUT2+ | RP7                        | [W]<br>[W]        | 2<br>1      | 0_0404 4P2R 5%<br>VGALVDS@                                 |                                      | VGA_TZOUT2- <13><br>VGA_TZOUT2+ <13> |
| R1359 | VGAEDP@<br>[N] [I0_U_0402_16V7K] |                      | TZOUT1-<br>TZOUT1+ | RP10                       | [W]<br>[W]        | 2<br>1      | 0_0404 4P2R 5%<br>VGALVDS@                                 |                                      | VGA_TZOUT1- <13><br>VGA_TZOUT1+ <13> |
|       |                                  |                      | TZOUT0-<br>TZOUT0+ | RP12                       | [W]<br>[W]        | 2<br>1      | 0_0404 4P2R 5%<br>VGALVDS@                                 |                                      | VGA_TZOUT0- <13><br>VGA_TZOUT0+ <13> |
|       | eDP_AUXN<br>eDP_AUXP             | I2CC SDA<br>I2CC_SCL |                    | RP14<br>R1358.1<br>R1359.1 | [W]<br>[W]<br>[W] | 2<br>2<br>2 | 0_0404 4P2R 5%<br>0_0402 5% VGALVDS@<br>0_0402 5% VGALVDS@ |                                      | VGA_LCD_DAT <14><br>VGA_LCD_CLK <14> |

| UMA                              |                          | DIS                         |                      | Panel                |
|----------------------------------|--------------------------|-----------------------------|----------------------|----------------------|
| LVDS                             | eDP                      | LVDS                        | eDP                  | Conn.                |
| APU_TX0UT0+<br>APU_TX0UT0-       |                          | VGA_TX0UT0+<br>VGA_TX0UT0-  |                      | TX0UT0+<br>TX0UT0-   |
| APU_TX0UT1+<br>APU_TX0UT1-       | DP0_TXP1_R<br>DP0_TXN1_R | VGA_TX0UT1+<br>VGA_TX0UT1-  | eDP_TX1P<br>eDP_TX1N | TX0UT1+<br>TX0UT1-   |
| APU_TX0UT2+<br>APU_TX0UT2-       | DP0_TXP0_R<br>DP0_TXN0_R | VGA_TX0UT2+<br>VGA_TX0UT2-  | eDP_TX0P<br>eDP_TX0N | TX0UT2+<br>TX0UT2-   |
| APU_TX0UT_CLK+<br>APU_TX0UT_CLK- |                          | VGA_TXCLK+<br>VGA_TXCLK-    |                      | TXCLK+<br>TXCLK-     |
| APU_TZ0UT0+<br>APU_TZ0UT0-       |                          | VGA_TZ0UT0+<br>VGA_TZ0UT0-  |                      | TZ0UT0+<br>TZ0UT0-   |
| APU_TZ0UT1+<br>APU_TZ0UT1-       |                          | VGA_TZ0UT1+<br>VGA_TZ0UT1-  |                      | TZ0UT1+<br>TZ0UT1-   |
| APU_TZ0UT2+<br>APU_TZ0UT2-       |                          | VGA_TZ0UT2+<br>VGA_TZ0UT2-  |                      | TZ0UT2+<br>TZ0UT2-   |
| APU_TZ0UT_CLK+<br>APU_TZ0UT_CLK- |                          | VGA_TZCLK+<br>VGA_TZCLK-    |                      | TZCLK+<br>TZCLK-     |
| APU_LVDS_CLK<br>APU_LVDS_DAT     | DP0_AUXP_R<br>DP0_AUXN_R | VGA_LCD_CLK<br>VGA_LCD_DATA | eDP_AUXP<br>eDP_AUXN | TZCC_SCL<br>TZCC_SDA |

**LCD/LED PANEL Conn.** P/N: SP010016810  
F/P: IPEX\_20143-040E-20F\_40P



|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |                   |
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| Date: Thursday, February 24, 2011                                                                                                                                                                                                                                                                                                                                                                                                                             |            | Sheet              |            | 23                       | of 50             |



Place near C917~C924 and use common via

From VGA

From APU

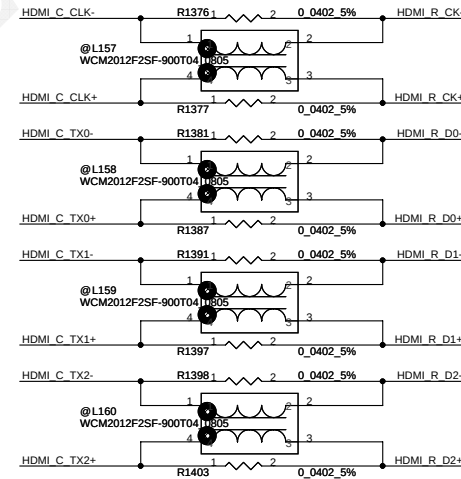
Near the connector

|               |         |                   |               |         |                    |
|---------------|---------|-------------------|---------------|---------|--------------------|
| HDMI C TX2- R | C1549 2 | 1 0.1U 0402 16V7K | HDMI C TX2- R | R1399 1 | 2 DISO@499 0402 1% |
| HDMI C TX2+ R | C1550 2 | 1 0.1U 0402 16V7K | HDMI C TX2+ R | R1400 1 | 2 DISO@499 0402 1% |
| HDMI C TX1- R | C1551 2 | 1 0.1U 0402 16V7K | HDMI C TX1- R | R1401 1 | 2 DISO@499 0402 1% |
| HDMI C TX1+ R | C1552 2 | 1 0.1U 0402 16V7K | HDMI C TX1+ R | R1402 1 | 2 DISO@499 0402 1% |
| HDMI C TX0- R | C1553 2 | 1 0.1U 0402 16V7K | HDMI C TX0- R | R1403 1 | 2 DISO@499 0402 1% |
| HDMI C TX0+ R | C1554 2 | 1 0.1U 0402 16V7K | HDMI C TX0+ R | R1404 1 | 2 DISO@499 0402 1% |
| HDMI C CLK- R | C1555 2 | 1 0.1U 0402 16V7K | HDMI C CLK- R | R1405 1 | 2 DISO@499 0402 1% |
| HDMI C CLK+ R | C1556 2 | 1 0.1U 0402 16V7K | HDMI C CLK+ R | R1406 1 | 2 DISO@499 0402 1% |

UMA use 604 ohm  
VGA use 499 ohm

For UMA HDMI  
termination BOM option

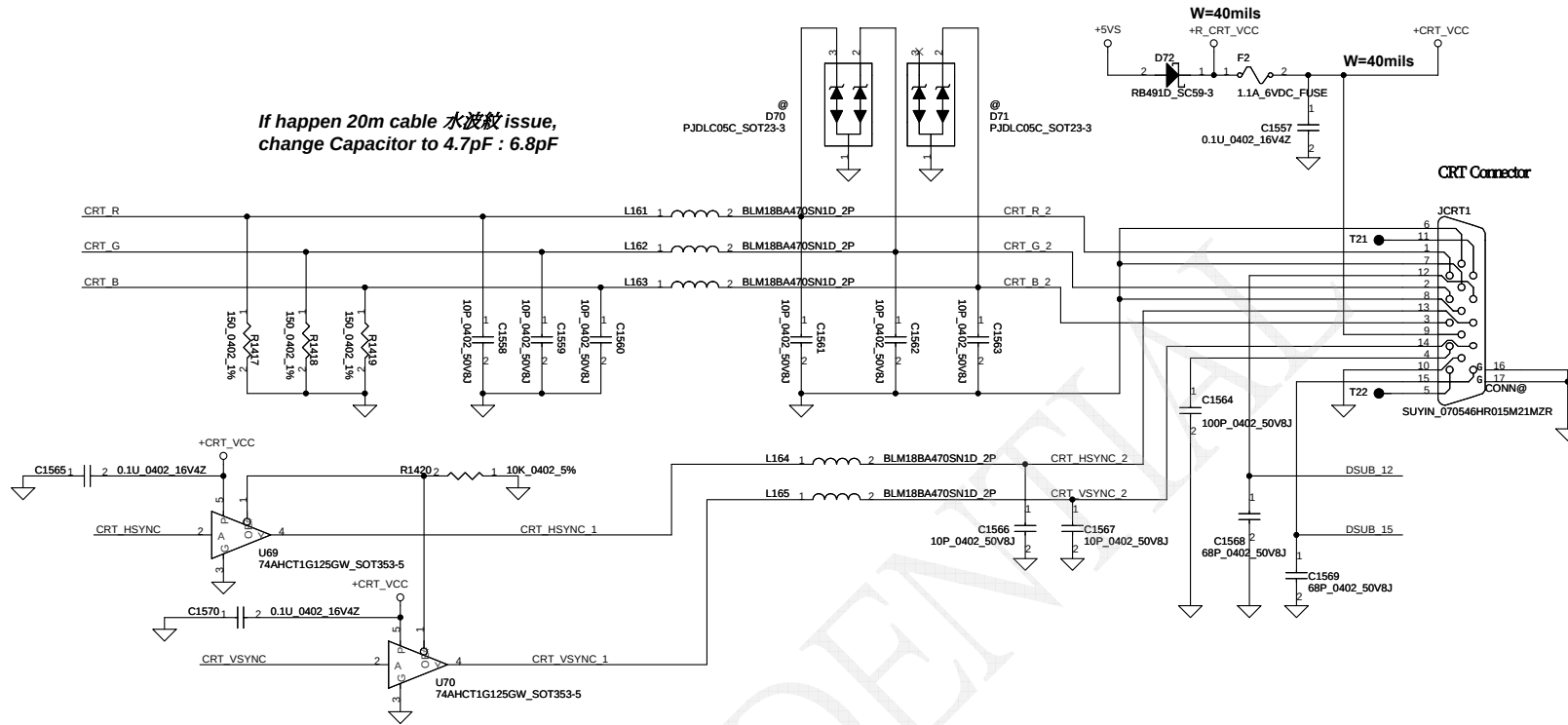
|         |                   |
|---------|-------------------|
| R1399 2 | UMA@1 604 0402 1% |
| R1400 2 | UMA@1 604 0402 1% |
| R1401 2 | UMA@1 604 0402 1% |
| R1402 2 | UMA@1 604 0402 1% |
| R1403 2 | UMA@1 604 0402 1% |
| R1404 2 | UMA@1 604 0402 1% |
| R1405 2 | UMA@1 604 0402 1% |
| R1406 2 | UMA@1 604 0402 1% |
| R1407 2 | UMA@1 604 0402 1% |
| R1408 2 | UMA@1 604 0402 1% |



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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Sheet                    | 24 of 50                    |



If happen 20m cable 水波紋 issue,  
change Capacitor to 4.7pF : 6.8pF



Use common via

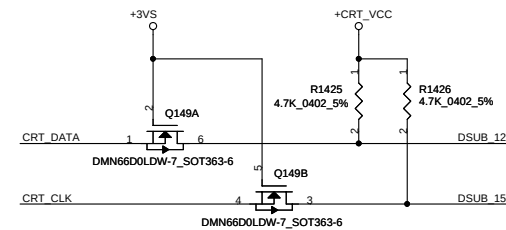
|                      |                 |       |      |   |           |           |
|----------------------|-----------------|-------|------|---|-----------|-----------|
| <28> FCH_CRT_R       | FCH_CRT_R       | R1421 | UMA@ | 1 | 0.0402 5% | CRT_R     |
| <28> FCH_CRT_G       | FCH_CRT_G       | R1422 | UMA@ | 1 | 0.0402 5% | CRT_G     |
| <28> FCH_CRT_B       | FCH_CRT_B       | R1423 | UMA@ | 1 | 0.0402 5% | CRT_B     |
| <28> FCH_CRT_HSYNC   | FCH_CRT_HSYNC   | R1424 | UMA@ | 1 | 0.0402 5% | CRT_HSYNC |
| <28> FCH_CRT_VSYNC   | FCH_CRT_VSYNC   | R1427 | UMA@ | 1 | 0.0402 5% | CRT_VSYNC |
| <28> FCH_CRT_DDC_SDA | FCH_CRT_DDC_SDA | R1428 | UMA@ | 1 | 0.0402 5% | CRT_DATA  |
| <28> FCH_CRT_DDC_SCL | FCH_CRT_DDC_SCL | R1429 | UMA@ | 1 | 0.0402 5% | CRT_CLK   |

From FCH

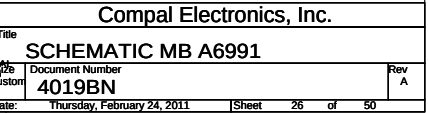
|                    |               |       |       |   |           |           |
|--------------------|---------------|-------|-------|---|-----------|-----------|
| <14> VGA_CRT_R     | VGA_CRT_R     | R1430 | DISO@ | 1 | 0.0402 5% | CRT_R     |
| <14> VGA_CRT_G     | VGA_CRT_G     | R1431 | DISO@ | 1 | 0.0402 5% | CRT_G     |
| <14> VGA_CRT_B     | VGA_CRT_B     | R1432 | DISO@ | 1 | 0.0402 5% | CRT_B     |
| <14> VGA_CRT_HSYNC | VGA_CRT_HSYNC | R1433 | DISO@ | 1 | 0.0402 5% | CRT_HSYNC |
| <14> VGA_CRT_VSYNC | VGA_CRT_VSYNC | R1434 | DISO@ | 1 | 0.0402 5% | CRT_VSYNC |
| <14> VGA_CRT_DATA  | VGA_CRT_DATA  | R1435 | DISO@ | 1 | 0.0402 5% | CRT_DATA  |
| <14> VGA_CRT_CLK   | VGA_CRT_CLK   | R1436 | DISO@ | 1 | 0.0402 5% | CRT_CLK   |

From VGA

Close to Conn side



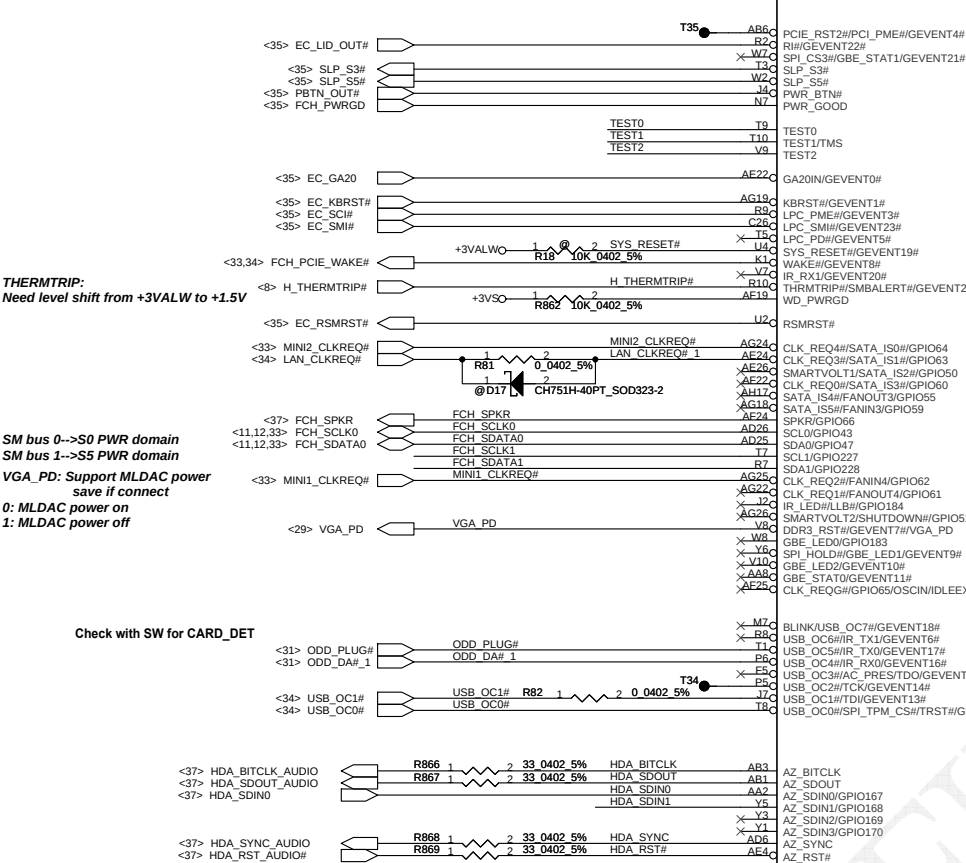
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |            | Compal Secret Data |            | Compal Electronics, Inc. |                             |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Sheet                    | 25 of 50                    |



# PCIE\_RST2 : Reset PCIE device on Hudson2

U2SD

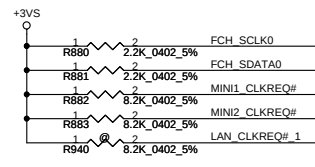
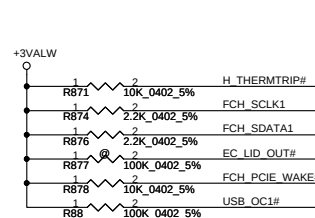
HUDSON-2



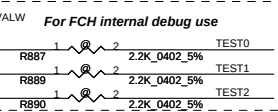
**THERMTRIP:**  
Need level shift from +3VALW to +1.5V

**SM bus 0-->S0 PWR domain**  
**SM bus 1-->S5 PWR domain**  
**VGA\_PD: Support MLDAC power**  
save if connect  
**0: MLDAC power on**  
**1: MLDAC power off**

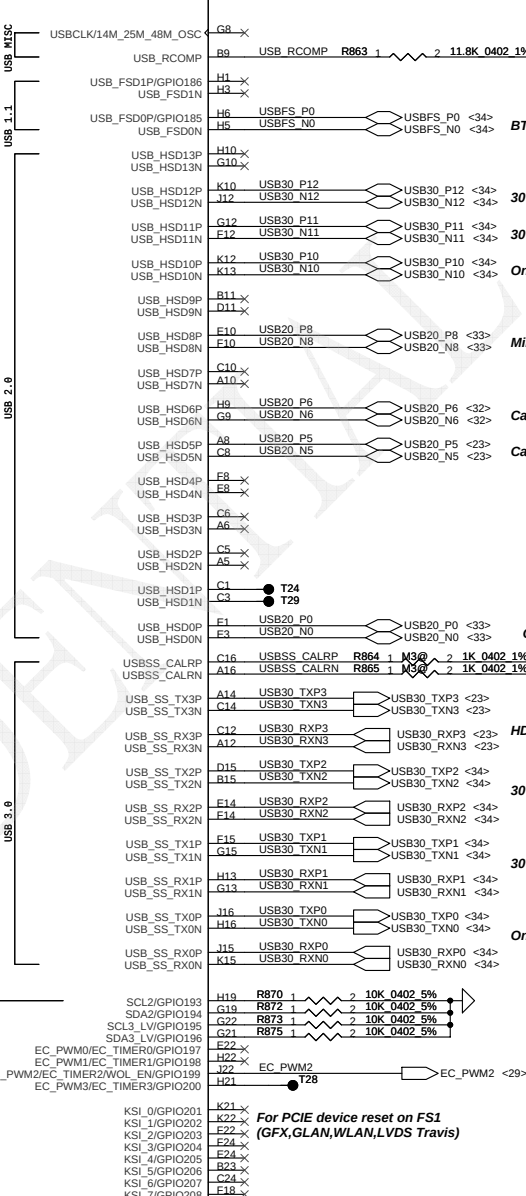
Check with SW for CARD\_DET



| Project SKU ID | HIGH    | LOW     |
|----------------|---------|---------|
| GPIO189        | VGA *   | UMA     |
| GPIO190        | PX *    | NO PX   |
| GPIO191        | 17 *    | 15 *    |
| GPIO192        | Reserve | Reserve |



EMBEDDED CTRL



For PCIE device reset on FS1 (GFX, GLAN, WLAN, LVDS, Travis)

Hudson-M2/M3  
OHCI CTL  
DEV 20, Fn 5  
<Disable CTL>

Hudson-M2  
EHCI CTL  
DEV 22, Fn 2  
<Support Wakeup>

Hudson-M3  
xHCI CTL  
DEV 16, Fn 1

Hudson-M3  
xHCI CTL  
DEV 16, Fn 0  
<Support Wakeup>

Hudson-M2/M3  
EHCI CTL  
DEV 19, Fn 2

Card Reader RTS5138

Camera

Hudson-M2/M3  
EHCI CTL  
DEV 18, Fn 2  
<Disable CTL>

Option Mini2

HD Camera

30 Pin Sub board USB3.0 Conn

30 Pin Sub board USB3.0 Conn

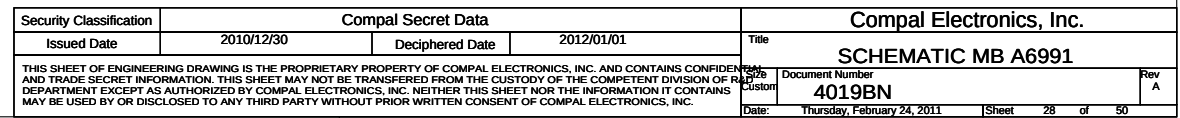
30 Pin Sub board USB3.0 Conn

On board USB Conn

Hudson-M3  
xHCI CTL  
DEV 16, Fn 1

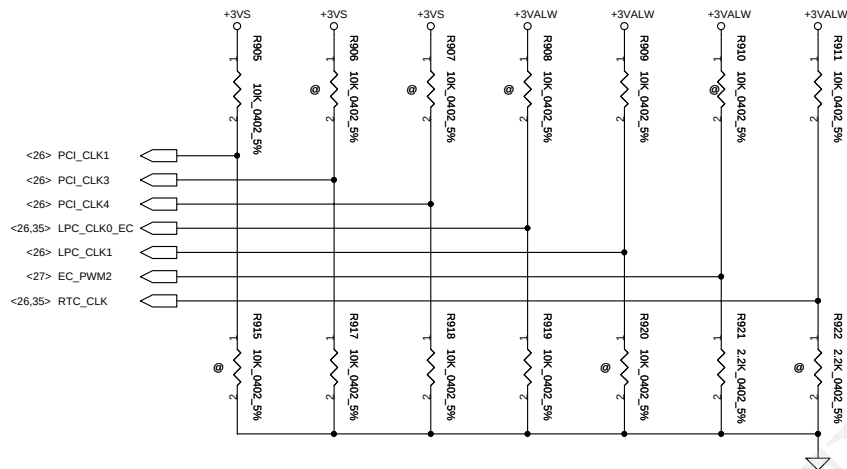
Hudson-M3  
xHCI CTL  
DEV 16, Fn 0

| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                                         |  |  |  | Compal Secret Data |  |  |  | Compal Electronics, Inc. |  |  |  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--------------------|--|--|--|--------------------------|--|--|--|
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |  |  |  | 2010/12/30         |  |  |  | Deciphered Date          |  |  |  |
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## STRAP PINS

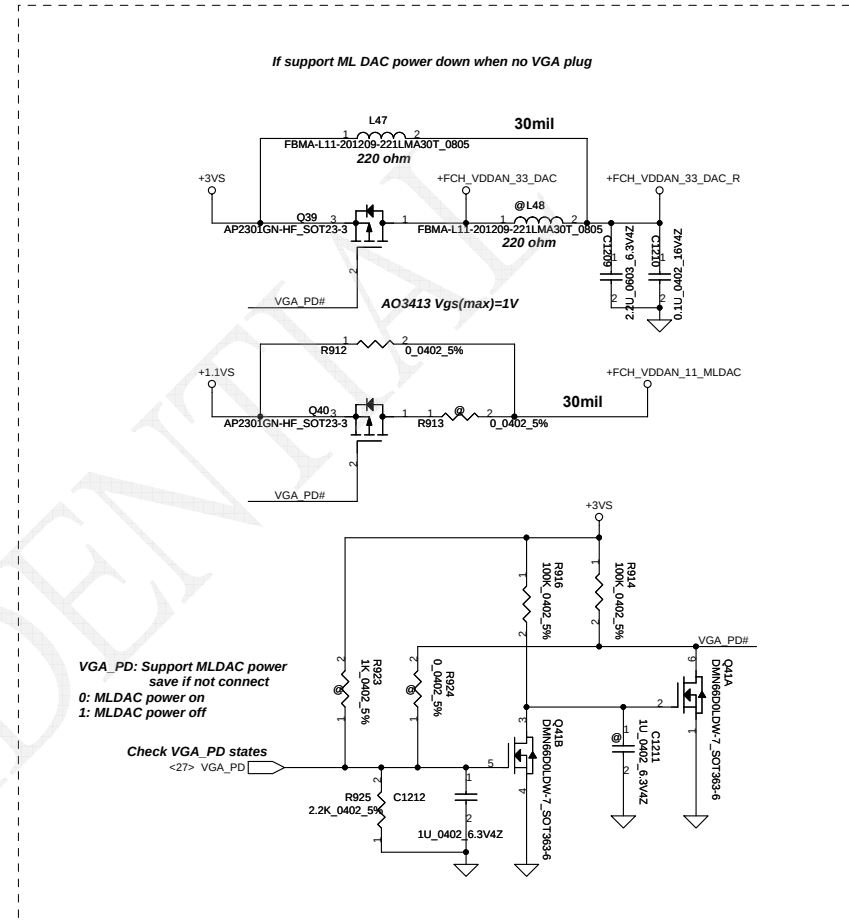
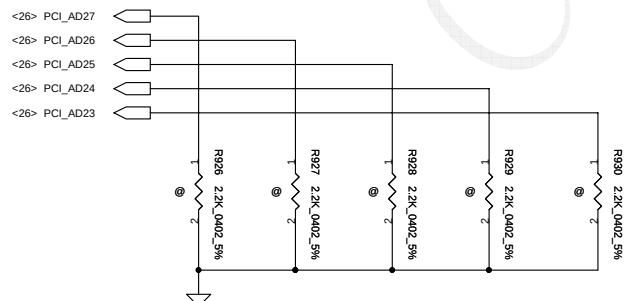
|           | PCI_CLK1                      | PCI_CLK3                            | PCI_CLK4                           | LPC_CLK0                      | LPC_CLK1                         | EC_PWM2                | RTC_CLK                                |
|-----------|-------------------------------|-------------------------------------|------------------------------------|-------------------------------|----------------------------------|------------------------|----------------------------------------|
| PULL HIGH | ALLOW<br>PCIE GEN2<br>DEFAULT | USE<br>DEBUG<br>STRAPS              | NON_FUSION<br>CLOCK MODE           | EC<br>ENABLED                 | CLKGEN<br>ENABLED<br><br>DEFAULT | LPC ROM                | S5 PLUS<br>MODE<br>DISABLED<br>DEFAULT |
| PULL LOW  | FORCE<br>PCIE GEN1            | IGNORE<br>DEBUG<br>STRAP<br>DEFAULT | FUSION<br>CLOCK<br>MODE<br>DEFAULT | EC<br>DISABLED<br><br>DEFAULT | CLKGEN<br>DISABLE                | SPI ROM<br><br>DEFAULT | S5 PLUS<br>MODE<br>ENABLED             |



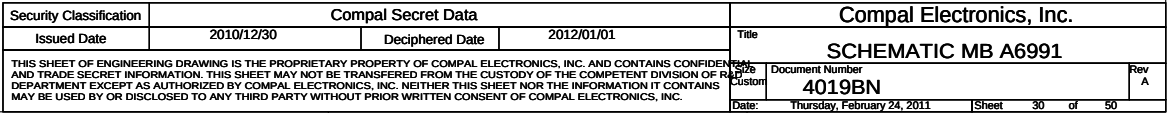
## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

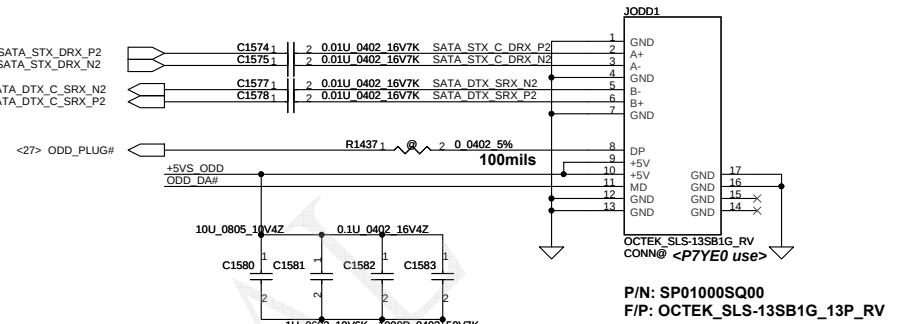
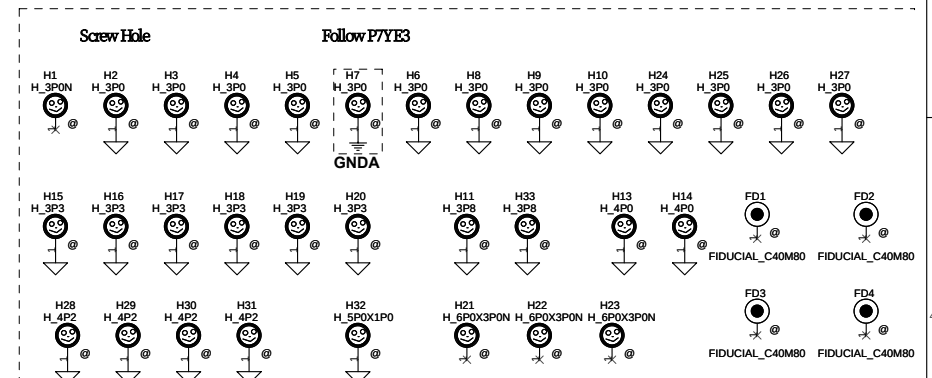
| PCI_AD26  |                        | PCI_AD27                          |  | PCI_AD25              | PCI_AD24                              | PCI_AD23                           |
|-----------|------------------------|-----------------------------------|--|-----------------------|---------------------------------------|------------------------------------|
| PULL HIGH | USE PCI PLL<br>DEFAULT | DISABLE ILA<br>AUTORUN<br>DEFAULT |  | USE FC PLL<br>DEFAULT | USE DEFAULT<br>PCIE STRAPS<br>DEFAULT | DISABLE PCI<br>MEM BOOT<br>DEFAULT |
| PULL LOW  | BYPASS<br>PCI PLL      | ENABLE<br>ILA<br>AUTORUN          |  | BYPASS<br>FC PLL      | USE EEPROM<br>PCIE STRAPS             | ENABLE PCI<br>MEM BOOT             |



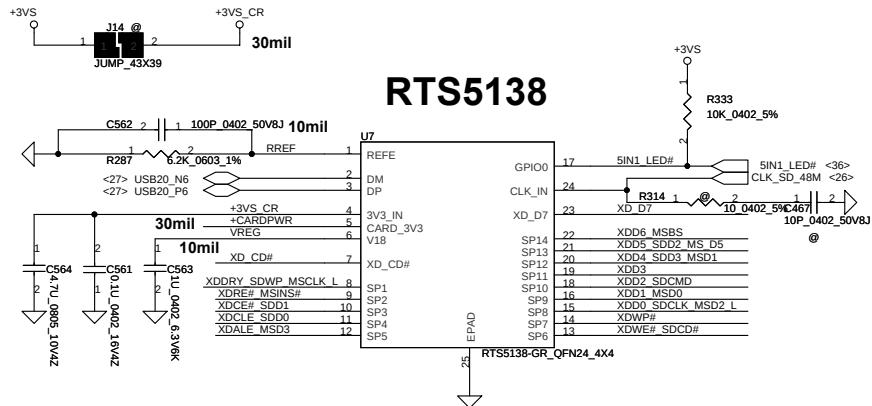
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                    |                 |            |                          |                             |                |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|--------------------------|-----------------------------|----------------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Compal Secret Data |                 |            | Compal Electronics, Inc. |                             |                |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                    |                 |            | Date:                    | Thursday, February 24, 2011 | Sheet 29 of 50 |



**SATA ODD Conn.**

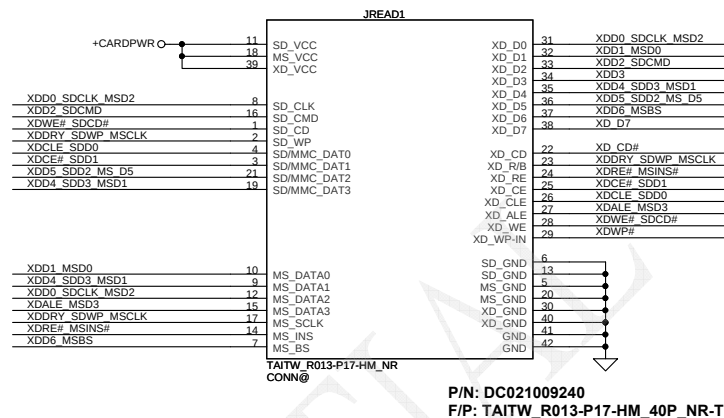
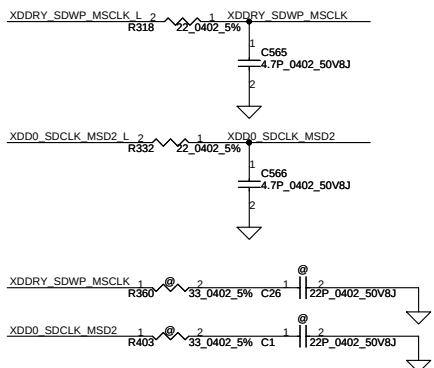
[illegible]

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |                             |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|--------------------------|-----------------------------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |            | Compal Secret Data |            | Compal Electronics, Inc. |                             |
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2010/12/30 | Deciphered Date    | 2012/01/01 | Title                    | SCHEMATIC MB A6991          |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Date                     | Thursday, February 24, 2011 |

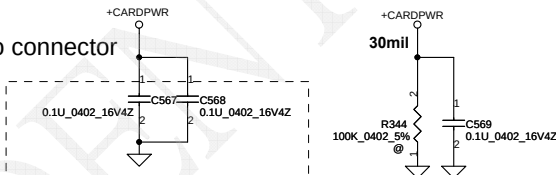


|      | XD     | SD      | MS      |
|------|--------|---------|---------|
| SP1  | XD_RDY | SD_WP   | MS_CLK  |
| SP2  | XD_REF | SD_INS# | MS_INS# |
| SP3  | XD_CEF | SD_D1   | MS_D1   |
| SP4  | XD_CLE | SD_D0   | MS_D0   |
| SP5  | XD_ALE | SD_CD#  | MS_D3   |
| SP6  | XD_WE# | SD_CD#  | MS_D3   |
| SP7  | XD_WP  | SD_CLK  | MS_D2   |
| SP8  | XD_D6  | SD_CLK  | MS_D2   |
| SP9  | XD_D1  | SD_CMD  | MS_D0   |
| SP10 | XD_D2  | SD_CMD  | MS_D0   |
| SP11 | XD_D3  | SD_D3   | MS_D1   |
| SP12 | XD_D4  | SD_D3   | MS_D1   |
| SP13 | XD_D5  | SD_D2   | MS_D1   |
| SP14 | XD_D6  | MS_BS   |         |
| SP15 | XD_D7  |         |         |

Share Pin

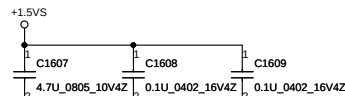
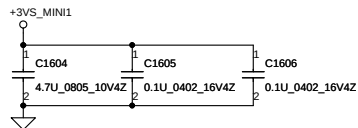
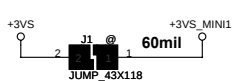


close to connector



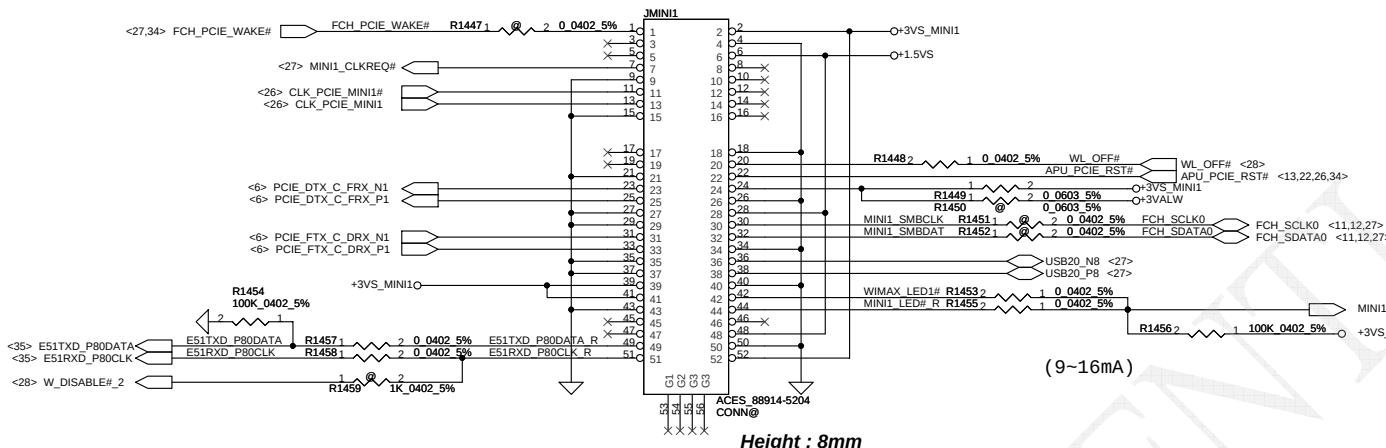


# Mini-Express Card for WLAN



| Mini Card Power Rating |                    |        |                      |
|------------------------|--------------------|--------|----------------------|
| Power                  | Primary Power (mA) |        | Auxiliary Power (mA) |
|                        | Peak               | Normal | Normal               |
| +3VS                   | 1000               | 750    |                      |
| +3V                    | 330                | 250    | 250 (wake enable)    |
| +1.5VS                 | 500                | 375    | 5 (Not wake enable)  |

P/N: SP01000P700  
F/P: ACES\_88914-5204\_52P

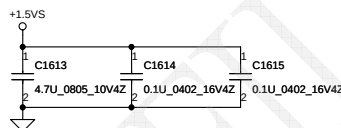
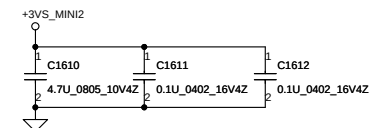
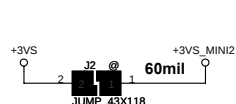


- Note:
1. FCH\_SCLK0 and FCH\_SDAT0 route as daisy chain.  
From FCH->JMINI2->DDR SOCKET->JMINI1
  2. E51RXD\_P80CLK and E51TXD\_P80DATA route as daisy chain.  
From EC->JMINI2->JMINI1

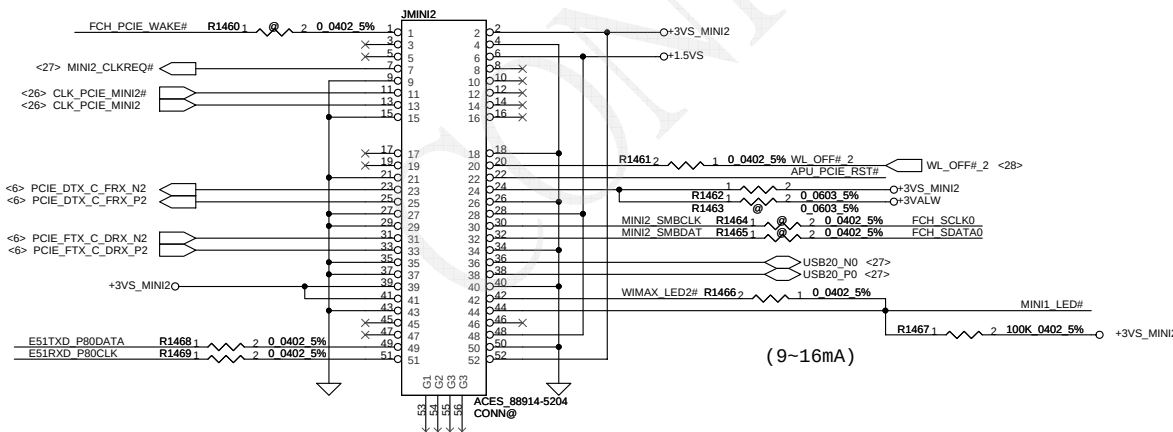
(9~16mA)

Height : 8mm

<P7WE0 use>



P/N: SP01000P700  
F/P: ACES\_88914-5204\_52P



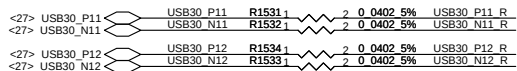
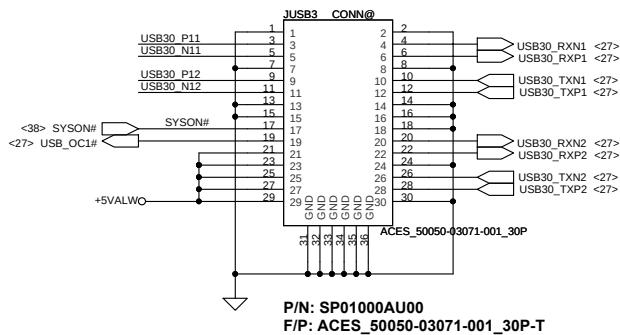
(9~16mA)

Height : 8mm

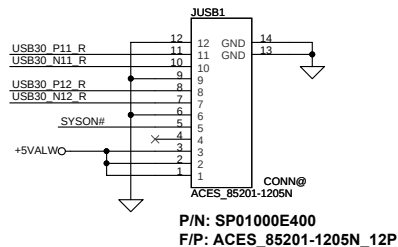
<P7WE0 use>

| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |            | Compal Secret Data |            | Compal Electronics, Inc. |                             |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Date                     | Thursday, February 24, 2011 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Sheet                    | 33 of 50                    |

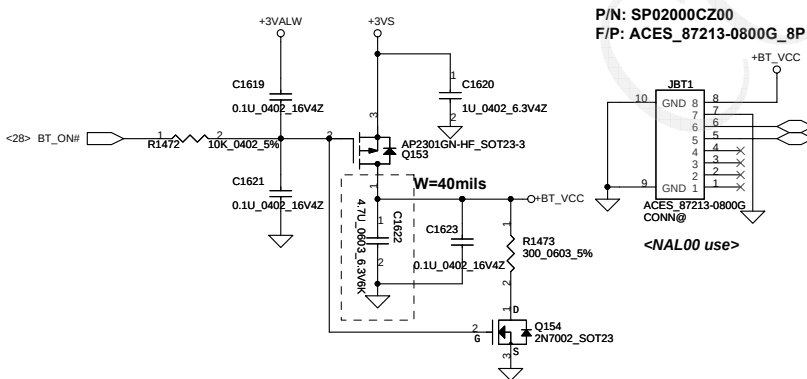
## 30 Pin USB/B Conn.



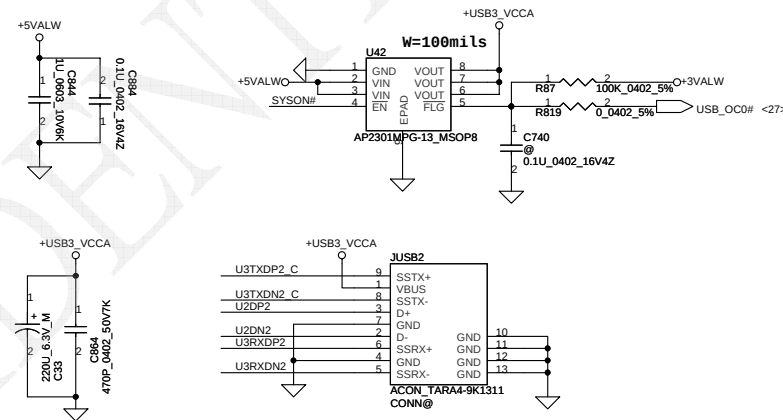
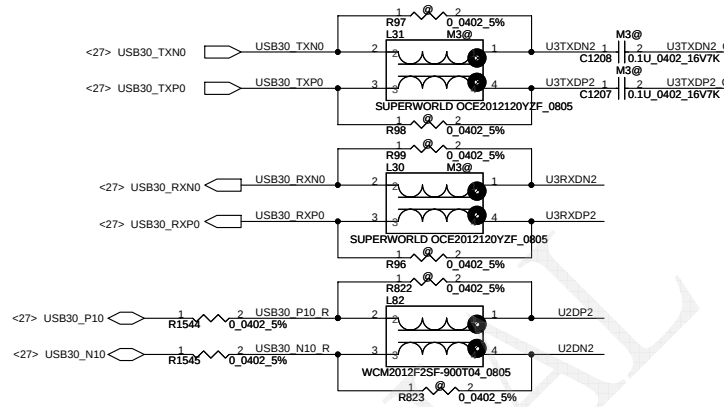
## 12 Pin USB/B Conn.



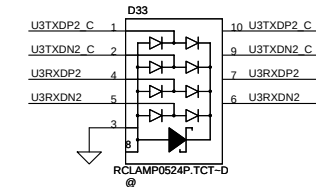
## Bluetooth Conn.



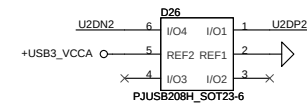
## On Board USB3.0 Conn.



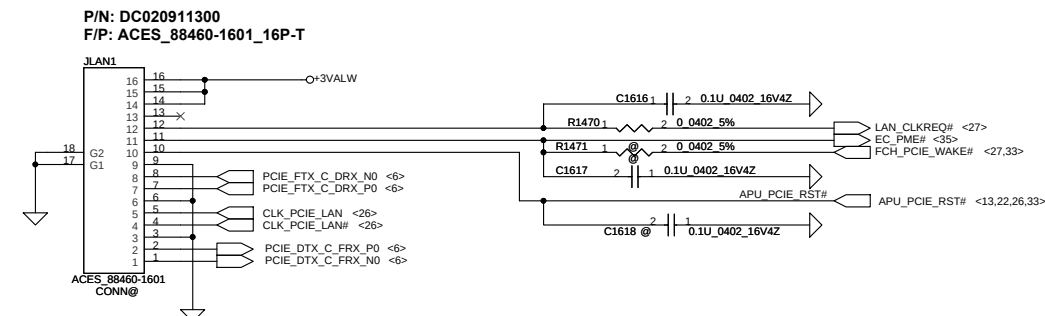
### For USB3.0 ESD diode



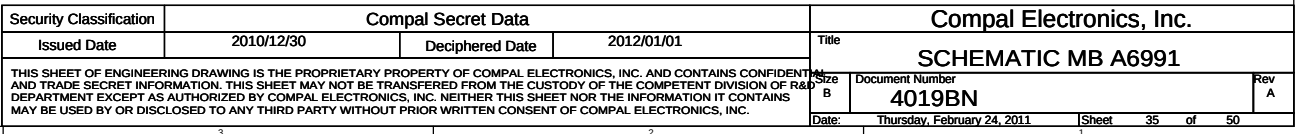
### For USB2.0 ESD diode



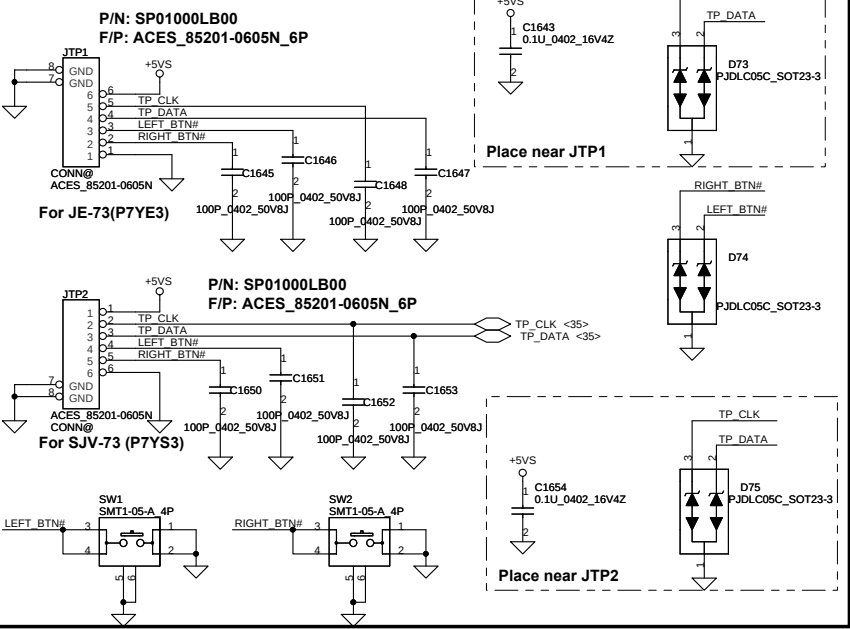
## LAN/B Conn.



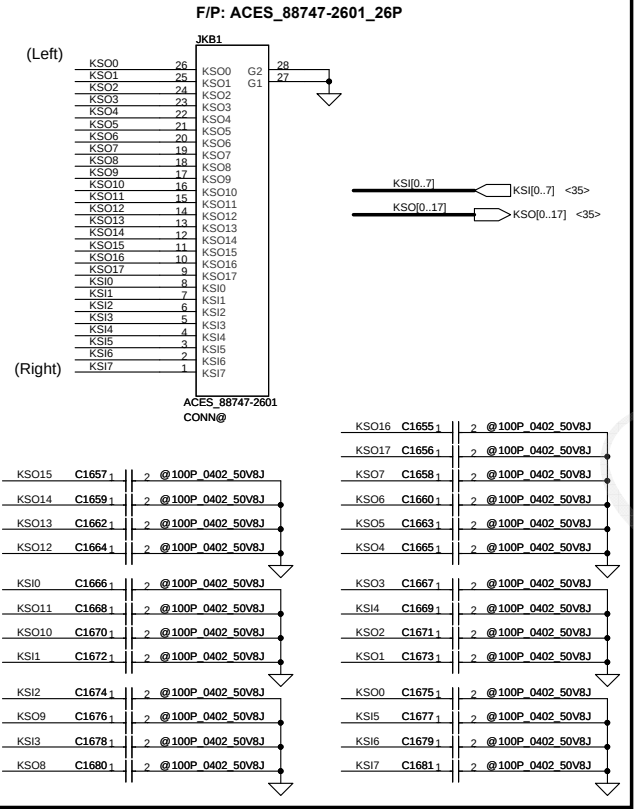
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |                          |  |                             |  |                 |  |       |  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--------------------|--|-----------------|--|--------------------------|--|-----------------------------|--|-----------------|--|-------|--|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |  | Compal Secret Data |  |                 |  | Compal Electronics, Inc. |  |                             |  |                 |  |       |  |
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   |  | 2010/12/30         |  | Deciphered Date |  | 2012/01/01               |  | Title                       |  |                 |  |       |  |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |                          |  | Rev                         |  | Document Number |  | Rev A |  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |                          |  | Date                        |  | 4019BN          |  |       |  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |                          |  | Thursday, February 24, 2011 |  | Sheet 34 of 50  |  |       |  |



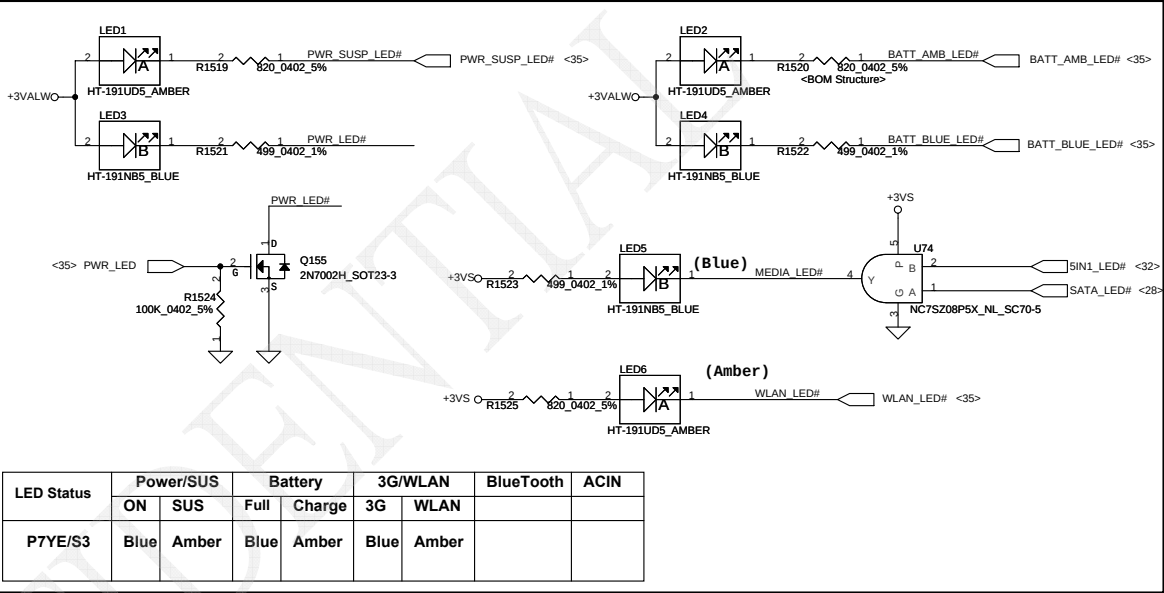
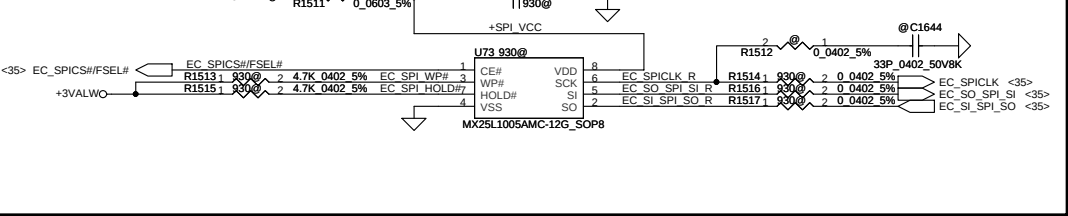
TP Conn.



KB Conn.

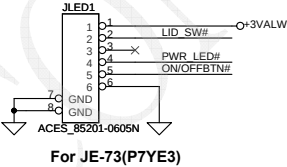


BIOS ROM



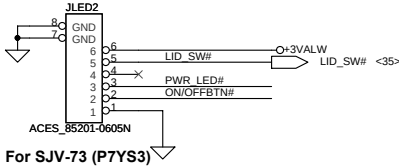
LS-6913P

P/N: SP01000LB00  
F/P: ACES\_85201-0605N\_6P

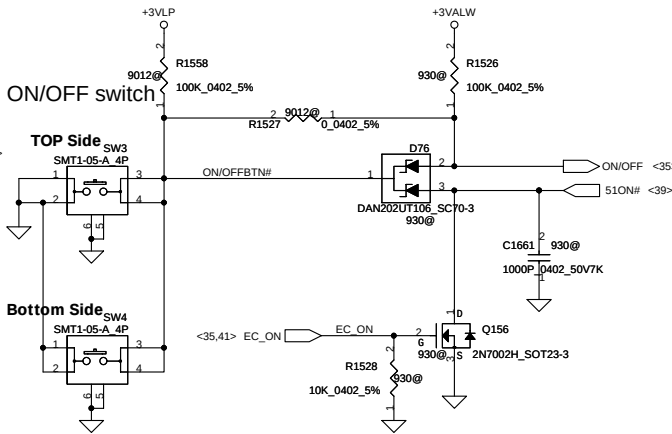


LS-6913P

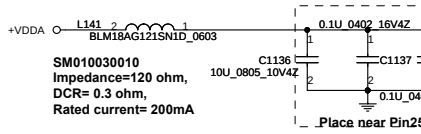
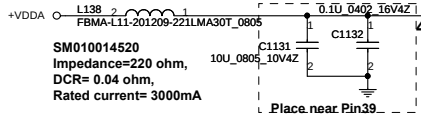
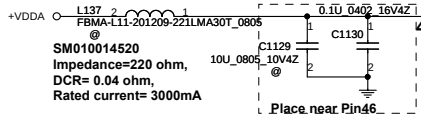
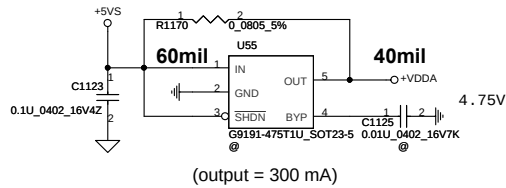
P/N: SP01000LB00  
F/P: ACES\_85201-0605N\_6P



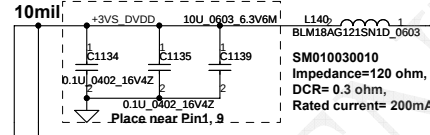
Power Button



|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                                   |                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|-----------------------------------|----------------|
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Date: Thursday, February 24, 2011 | Sheet 36 of 50 |



## HD Audio Codec



35mA

68mA 600mA

SPK\_OUT\_L+

SPK\_OUT\_L-

SPK\_OUT\_R+

SPK\_OUT\_R-

HP\_OUT\_L

HP\_OUT\_R

SDATA\_IN

SDATA\_OUT

SYNC

RESET#

BCLK

GPIO0/DMIC\_DATA

GPIO1/DMIC\_CLK

PD#

PCBEEP

MONO\_OUT

AVSS1

PVSS2

PVSS1

AGND

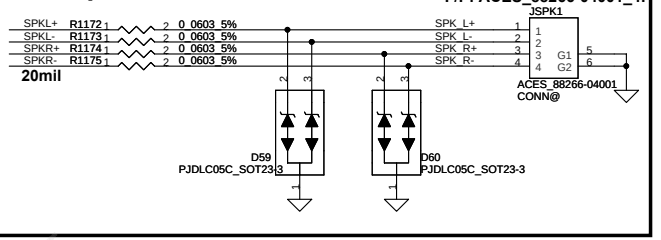
DGND

EC\_MUTE#

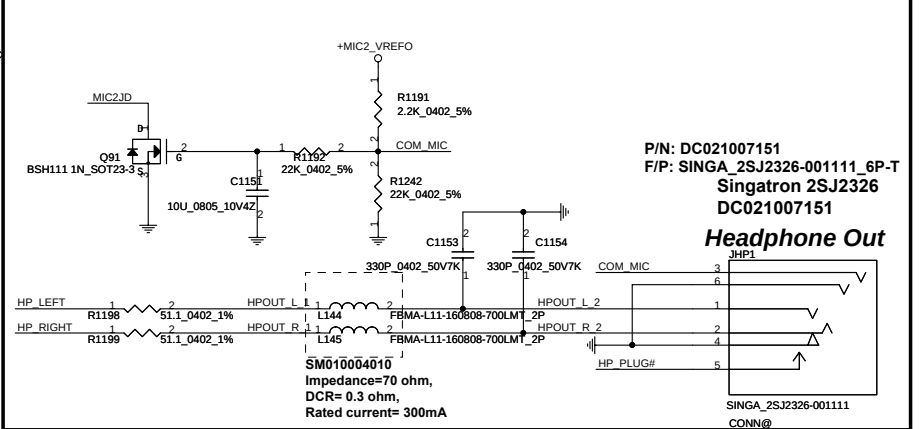
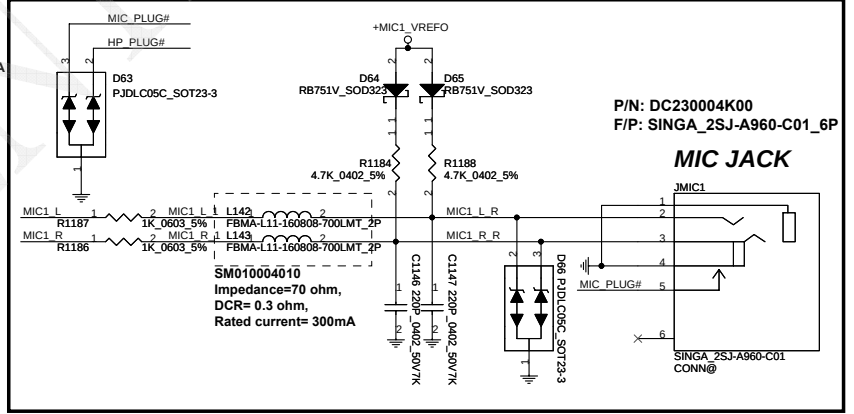
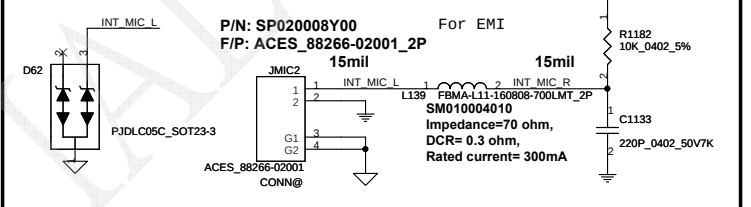
EC\_MUTE# R

EC\_MUTE#

## Int. Speaker Conn.

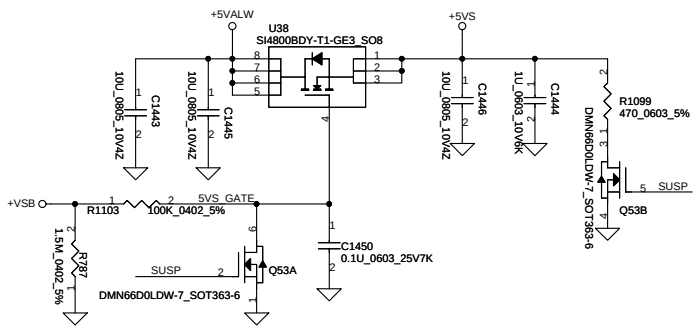


## Int. MIC Conn.

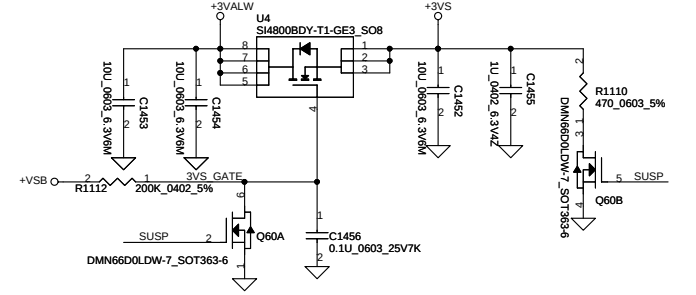


|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |                             |       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|--------------------------|-----------------------------|-------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |            | Compal Secret Data |            | Compal Electronics, Inc. |                             |       |
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2010/12/30 | Deciphered Date    | 2010/08/04 | Title                    | SCHEMATIC MB A6991          |       |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Doc No                   | 4019BN                      | A     |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Date:                    | Thursday, February 24, 2011 | Sheet |

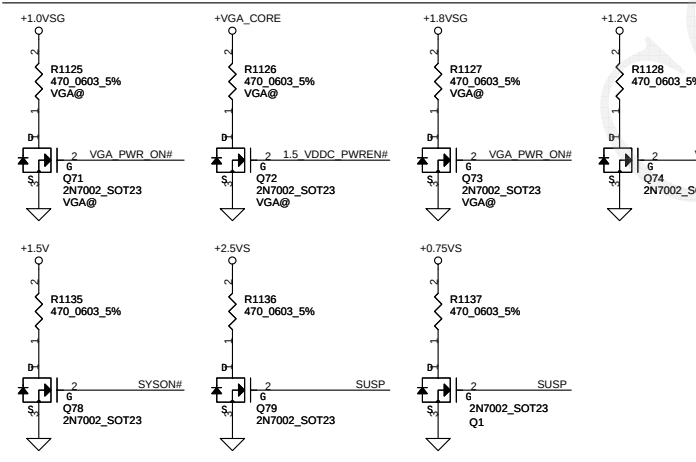
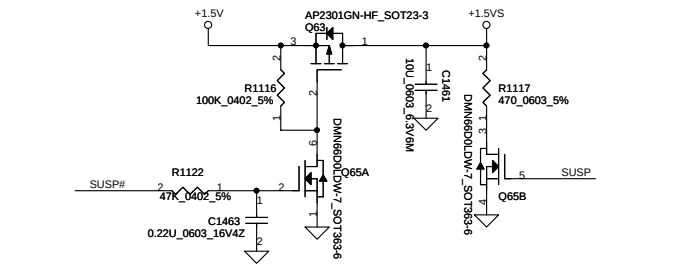
+5VALWTO +5VS



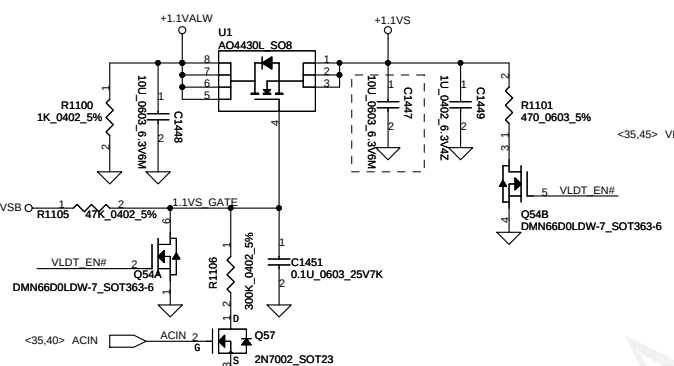
+3VALWTO +3VS



+1.5V TO +1.5VS

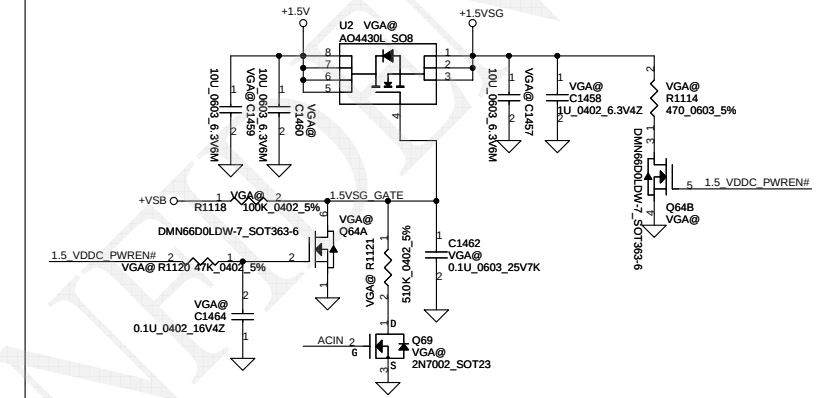


+1.1VALWTO +1.1VS

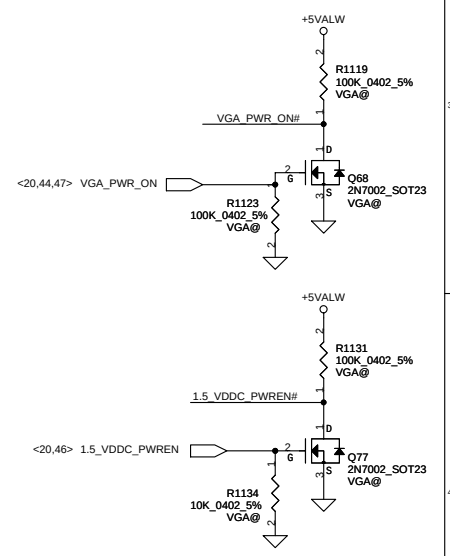
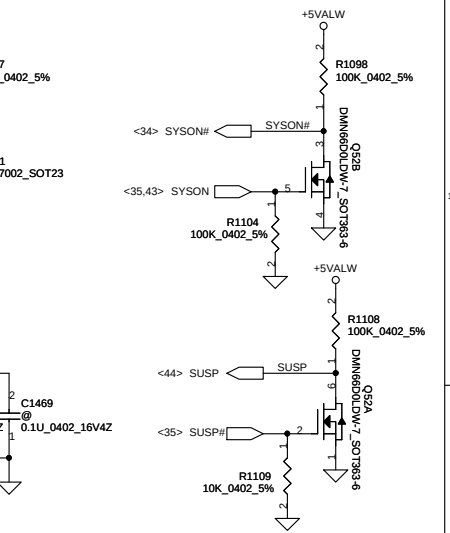
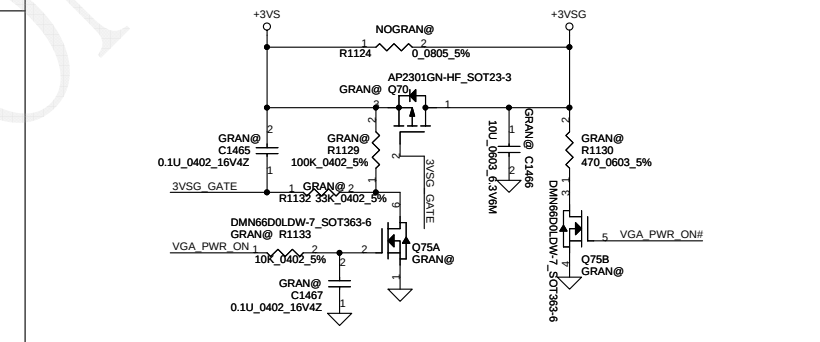


VGA Power

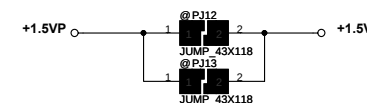
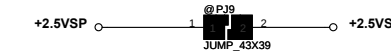
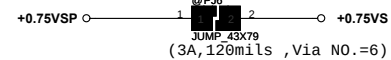
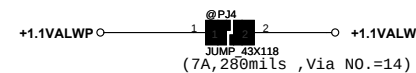
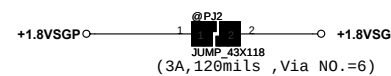
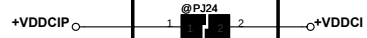
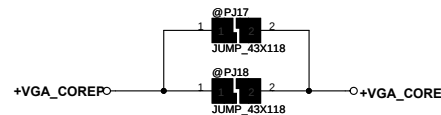
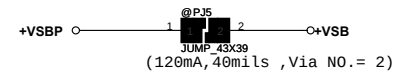
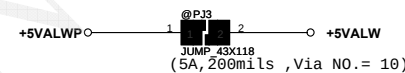
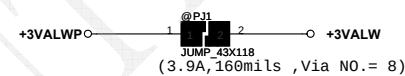
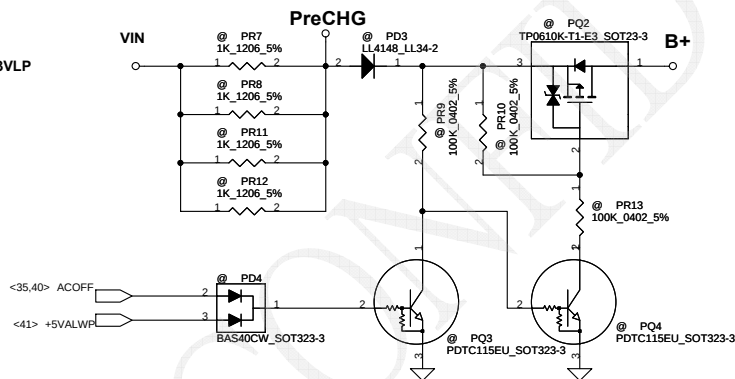
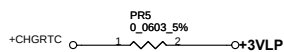
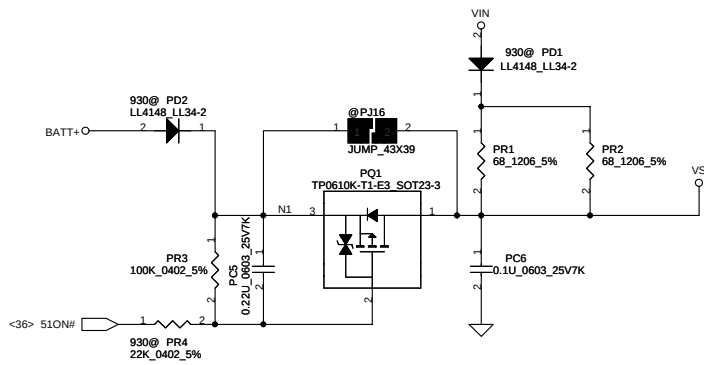
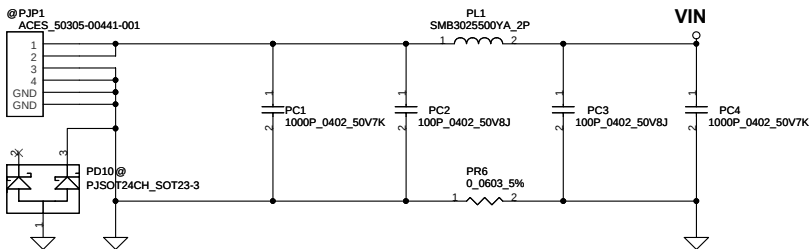
+1.5V to +1.5VSG



+3VS to +3VSG



|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |                          |  |                    |  |                 |  |       |  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--------------------|--|-----------------|--|--------------------------|--|--------------------|--|-----------------|--|-------|--|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |  | Compal Secret Data |  |                 |  | Compal Electronics, Inc. |  |                    |  |                 |  |       |  |
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   |  | 2010/12/30         |  | Deciphered Date |  | 2012/01/01               |  | Title              |  |                 |  |       |  |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |                          |  | Rev B              |  | Document Number |  | Rev A |  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |                          |  | 4019BN             |  |                 |  |       |  |
| Date: Thursday, February 24, 2011                                                                                                                                                                                                                                                                                                                                                                                                                             |  |                    |  | Sheet           |  | 38                       |  | of 50              |  |                 |  |       |  |



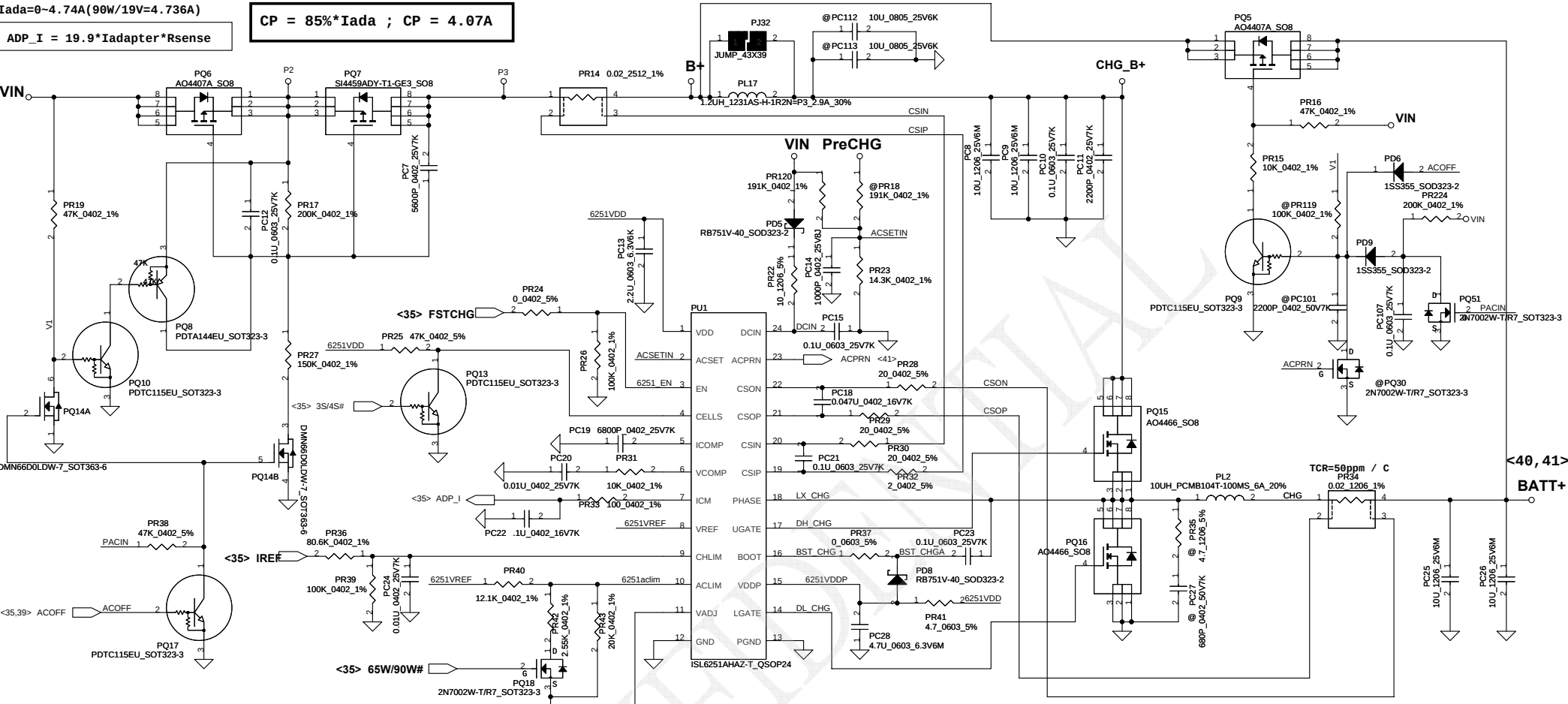
When use Granville, short PJ24

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                                   |                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|-----------------------------------|----------------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |            | Compal Secret Data |            | Title                             |                |
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2010/12/30 | Deciphered Date    | 2011/07/13 | Compal Electronics, Inc.          |                |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | 4019BN                            | A              |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Date: Thursday, February 24, 2011 | Sheet 39 of 50 |

Iada=0~4.74A(90W/19V=4.736A)

ADP\_I = 19.9\*Iadapter\*Rsense

CP = 85%\*Iada ; CP = 4.07A



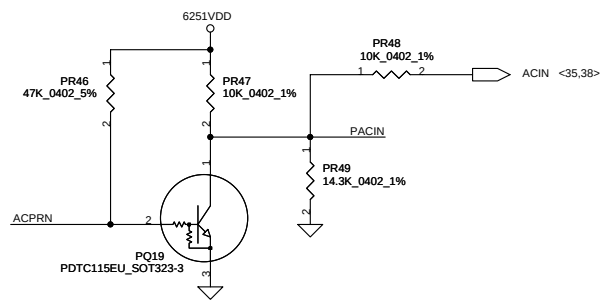
**CP mode**  
 $I_{input} = (1/0.02)(0.05 \cdot V_{ac1m}/2.39 + 0.05)$   
where  $V_{ac1m} = 1.502V$ ,  $I_{input} = 4.07A$

| BATT Type             | Charging Voltage (0x15) | CV mode |
|-----------------------|-------------------------|---------|
| Normal 3S LI-ON Cells | 12600mV                 | 12.60V  |

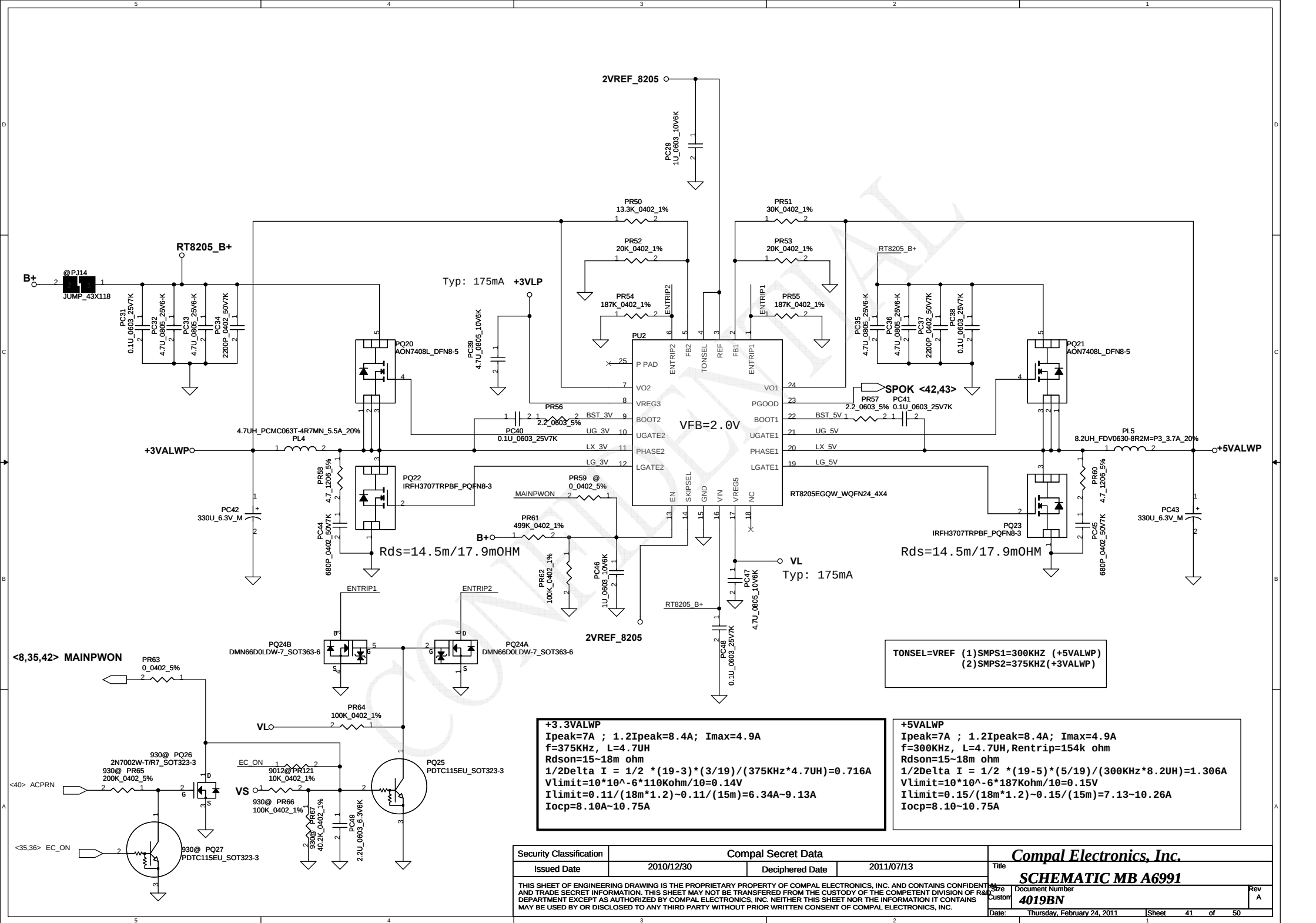
**CC=0.6~4.48A**  
 $I_{REF} = 0.7224 \cdot I_{charge}$   
 $I_{REF} = 0.43V \sim 3.24V$

K1  
 $V_{ch1m} = I_{ref} \cdot (PR39 / (PR36 + PR39))$   
 $= I_{ref} \cdot (100K / (80.6K + 100K))$   
 $= I_{ref} \cdot 0.5537$   
 $I_{charge} = (165mV / PR369) \cdot (V_{ch1m} / 3.3V)$   
 $= (165m / 20m) \cdot (1/3.3V) \cdot I_{ref} \cdot 0.5537$   
 $= 1.3842 \cdot I_{ref}$   
 $I_{ref} = 0.7224 \cdot I_{charge} \Rightarrow K1 = 0.7224$

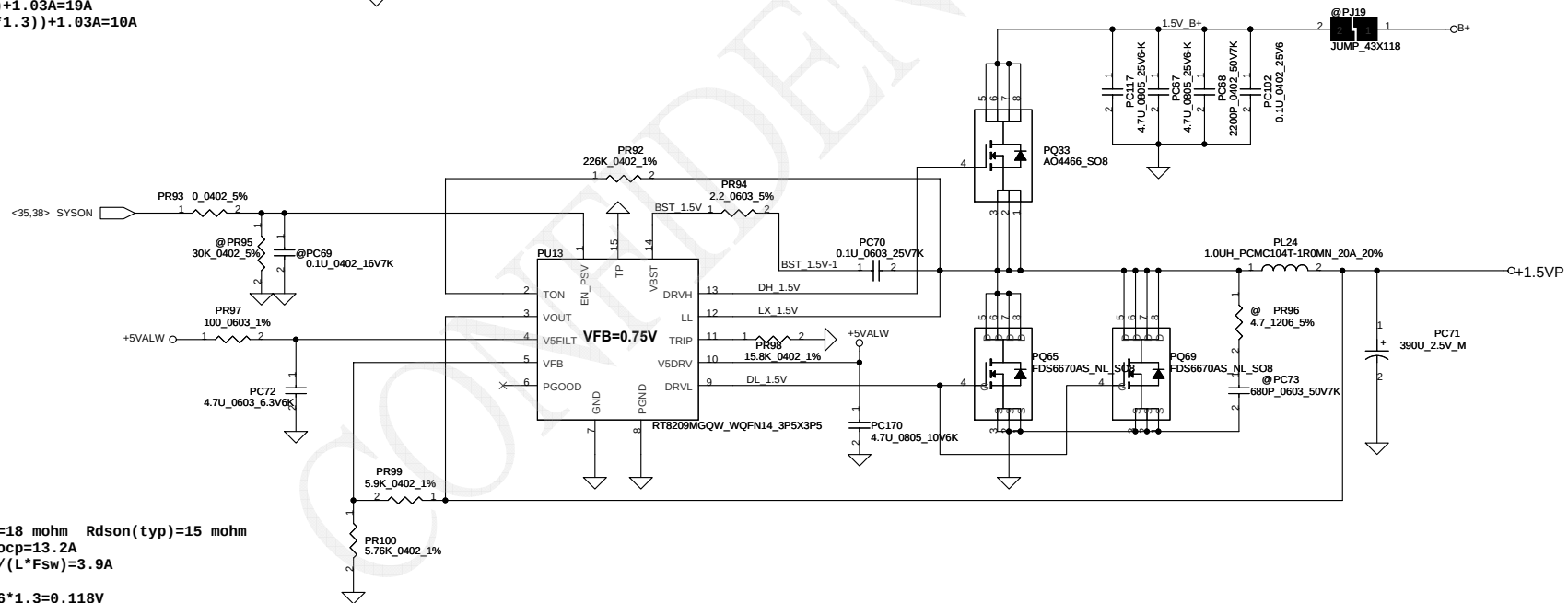
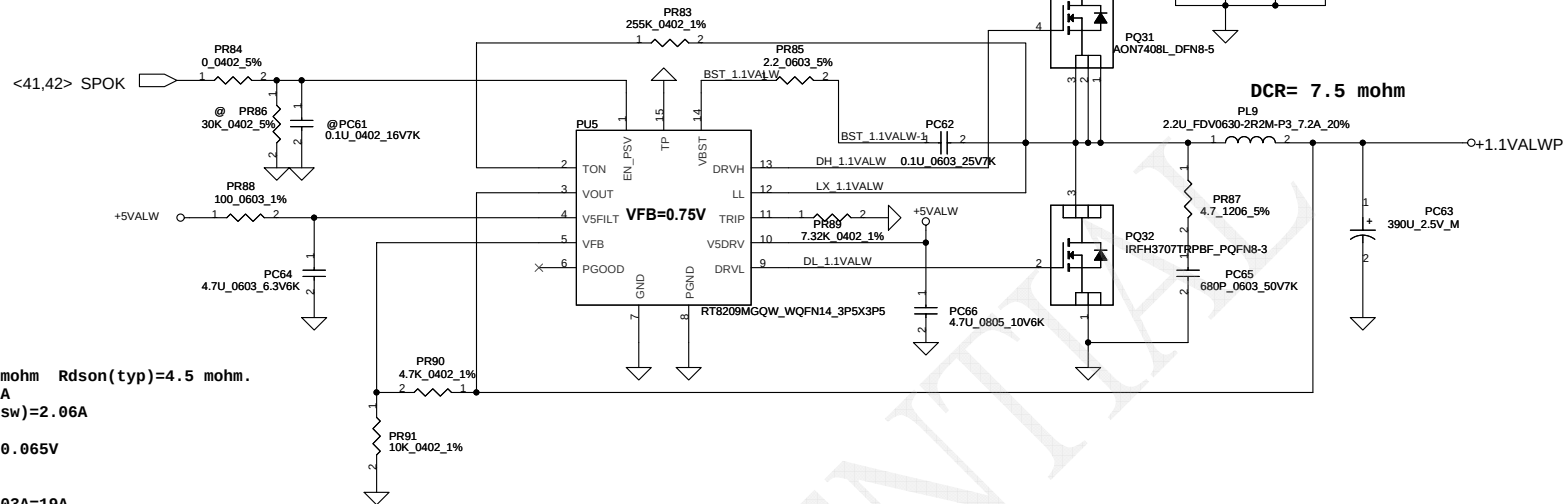
Kv  
 $R_{internal} = 514K$   $R_{ec} = 3K$   $R1 = PR44 = 15.4K$   $R2 = PR45 = 31.6K$   
 $R = 514K / (31.6K / (15.4K + 3K)) = 11.372K$   
 $r = 514K / 514K / (31.6K + 28.14K)$   
 $V_{cell} = 0.175 \cdot V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$   
 $V_{adj} = V_{ref} \cdot (R / (R + 514K)) + CALIBRATE \cdot (r / (r + 514K))$   
 $1.1483 = CALIBRATE \cdot 0.6046 \Rightarrow CALIBRATE = 1.899$   
 $1.899 = (4.2 - (V_{cell} + A \cdot 0.175)) \cdot Kv \Rightarrow (4.2 - (4.2 + A \cdot 0.175)) \cdot Kv$   
 $A = V_{ref} \cdot (R / (R + 514K)) = 0.052$   
 $Kv = 9.451$









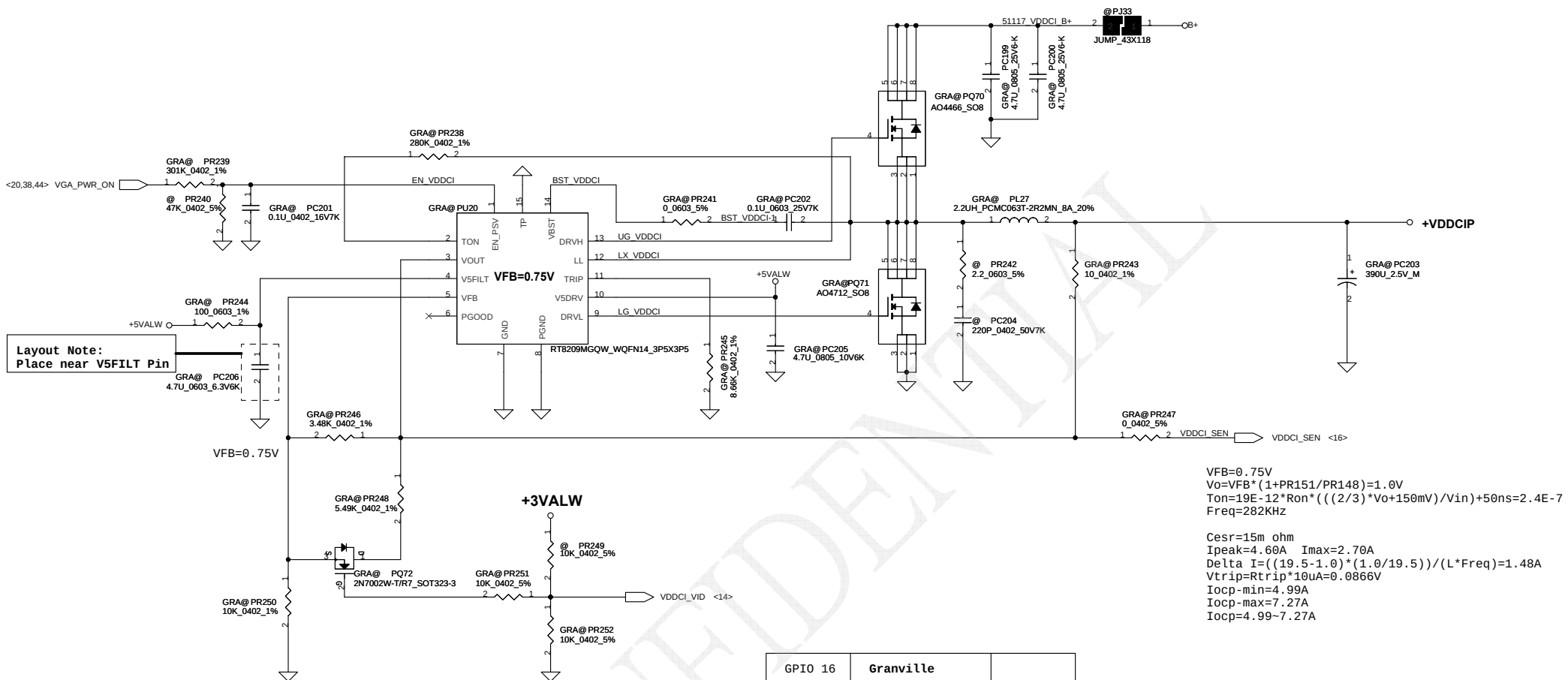


|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |                          |  |                             |  |                |  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--------------------|--|-----------------|--|--------------------------|--|-----------------------------|--|----------------|--|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |  | Compal Secret Data |  |                 |  | Compal Electronics, Inc. |  |                             |  |                |  |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  | Docu<br>Custom           |  | Document Number             |  | Rev A          |  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  | 4019BN                   |  |                             |  |                |  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  | Date:                    |  | Thursday, February 24, 2011 |  | Sheet 43 of 50 |  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |                    |  |                 |  |                          |  |                             |  |                |  |

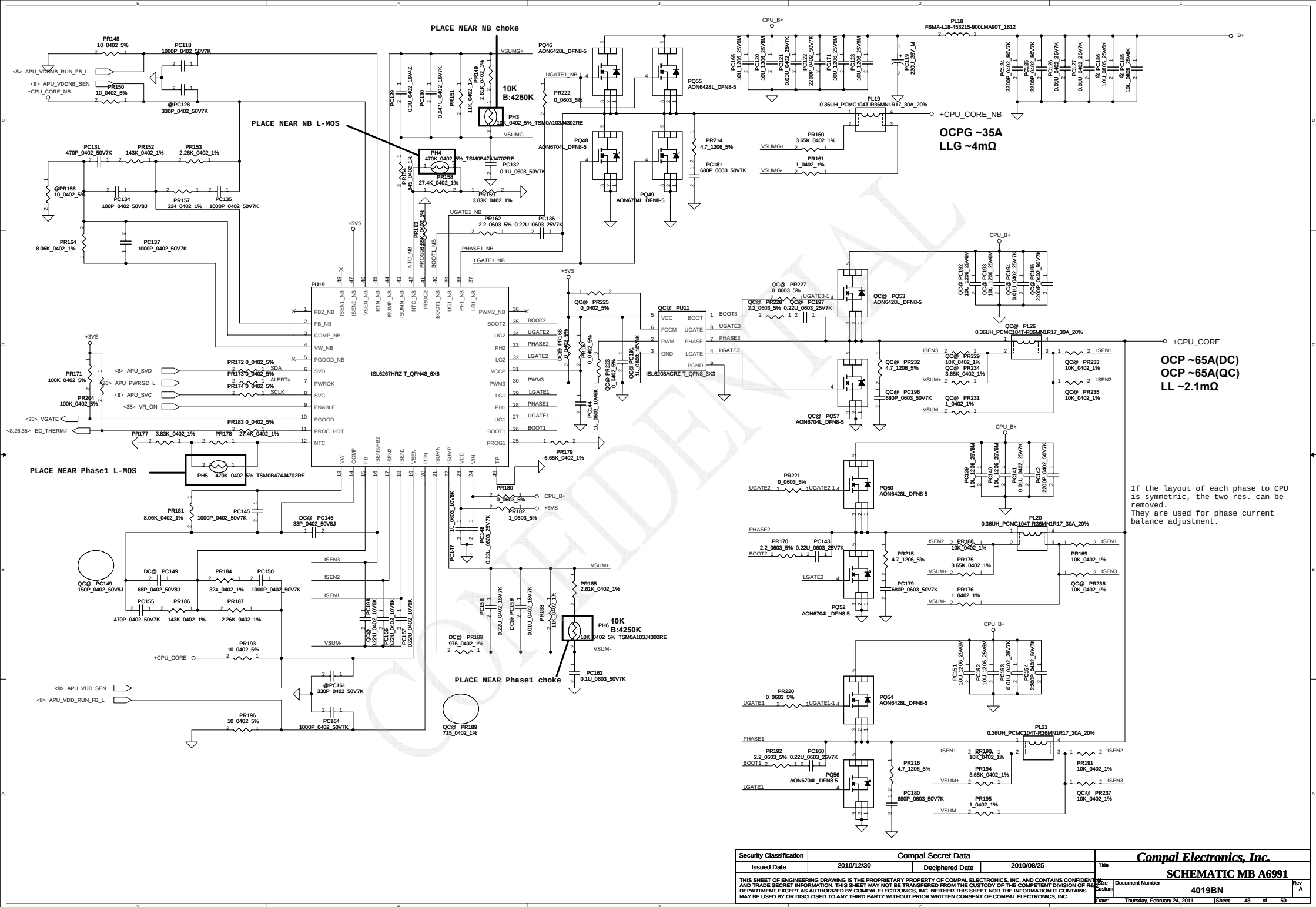








| GPI0 16   | Granville           |         |
|-----------|---------------------|---------|
| VDDCI_VID | VDDCI Voltage Level | Comment |
| 0         | 1.00 V              | Default |
| 1         | 0.90 V              |         |





| Item | Fixed Issue | Reason for change | Rev. | PG # | Modify List                       | Date          | Phase |
|------|-------------|-------------------|------|------|-----------------------------------|---------------|-------|
| 1    |             | Prevent ESD       |      |      | Change SB000006800 to SB000009Q80 | 2011<br>02/09 | DVT   |
| 2    |             |                   |      |      |                                   |               |       |
| 3    |             |                   |      |      |                                   |               |       |
| 4    |             |                   |      |      |                                   |               |       |
| 5    |             |                   |      |      |                                   |               |       |
| 6    |             |                   |      |      |                                   |               |       |
| 7    |             |                   |      |      |                                   |               |       |
| 8    |             |                   |      |      |                                   |               |       |
| 9    |             |                   |      |      |                                   |               |       |
| 10   |             |                   |      |      |                                   |               |       |
| 11   |             |                   |      |      |                                   |               |       |
| 12   |             |                   |      |      |                                   |               |       |
| 13   |             |                   |      |      |                                   |               |       |
| 14   |             |                   |      |      |                                   |               |       |
| 15   |             |                   |      |      |                                   |               |       |
| 16   |             |                   |      |      |                                   |               |       |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |          |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|--------------------------|----------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |            | Compal Secret Data |            | Compal Electronics, Inc. |          |
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2010/12/30 | Deciphered Date    | 2010/10/12 | Title                    |          |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | 4019BN                   |          |
| Date: Thursday, February 24, 2011                                                                                                                                                                                                                                                                                                                                                                                                                             |            |                    |            | Sheet                    | 49 of 50 |

Version change list (P.I.R. List)

- 0.1 ->0.2
1. R1244 change to BACO@; Q136, Q139, R1262, R1259, R1260, R1261 change to @.
  2. Change TEST35 to PU (pop R558; unpopR559).
  3. EC\_PME# PU (Pop R1503).
  4. Change U56 pin 42,43 to DGND.
  5. Change U6, R1537, R1538, R1539, R1540 to @.
  6. ALLOW\_STOP, APU\_SVC, APU\_SVD PU to +1.5V (add R604, R607, R618).
  7. Reserve +1.2VS to replace U6 SW power (add R948 pad).
  8. Unpop R25, add Q145.
  9. Add component for KBC930 and KBC9012 colay:  
R1518 (9012@), R1546 (@), R1547 (930@), R1548 (@), R1549 (930@), R1550 (9012@), R1551 (@), R1552 (9012@), R1553 (9012@), R1556 (930@), R1557 (9012@), R1558 (9012@).
  10. Add Net for KBC930 and KBC9012 colay:  
9012\_PH2, GPX006, GPX007, GPX010, 9012\_PH1, GPXID7, +EC\_VCC.
  11. Reserve R1554, R1555 for FFC USB/B.
  12. Delete RTS5209 PCIE port (del C1376, C1377, C158, C248); delete CLK req (del R55); delete Card det (del R144).
  13. For RTS5138, add USB port 6 and one 48MHz clock from FCH.
  14. Add R88 for USB/B oc pin.
  15. Change D33 to @.
  16. Change R1529, R1530, C1682 to @.
  17. For DVT board ID, change R1475 to 18K.
  18. Change R1526 to 930@.
  19. Change C1486 to PX@.
  20. Reserve R360, R403, C1 and C26 for EMI.
  21. Del R1554, R1555 for FFC USB/B.
  22. Change mini2 USB port from port 9 to port 0 (del R1542, R1543).
  23. Change R1289, R1290 to RT@.
  24. Add C1468, C1469 on SYSON# for ESD reserve.
  25. Change R417, R148 to DISO@.
  26. Add TP on JCRT1.5, JCRT1.11, USB port2.
  27. Add all EMI solution on TP Conn(include JE and SJV).
  28. Change U25 from A12 to A13 (unpop Q145, pop R25).
  29. Change U73, R1513, R1515, R1514, R1516, R1517, R1511, C1642 to 930@.

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                          |                             |                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|--------------------------|-----------------------------|----------------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       | Compal Secret Data |                 |            | Compal Electronics, Inc. |                             |                |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Date:                    | Thursday, February 24, 2011 | Sheet 50 of 50 |