Compal Confidential

JE51/HM51/SJV51_BZ

P5WE7/P5WH7/P5WS7 Schematics Document

AMD Brazos

Brazos with Ontario / Hudson M1 / Robson XT

DIS only / UMA only / PX Muxless / PX Muxless with BACO

2010-11-29

LA-7091P REV: 0.2

ZZZ2

PCB

Part Number = DA60000LQ00

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

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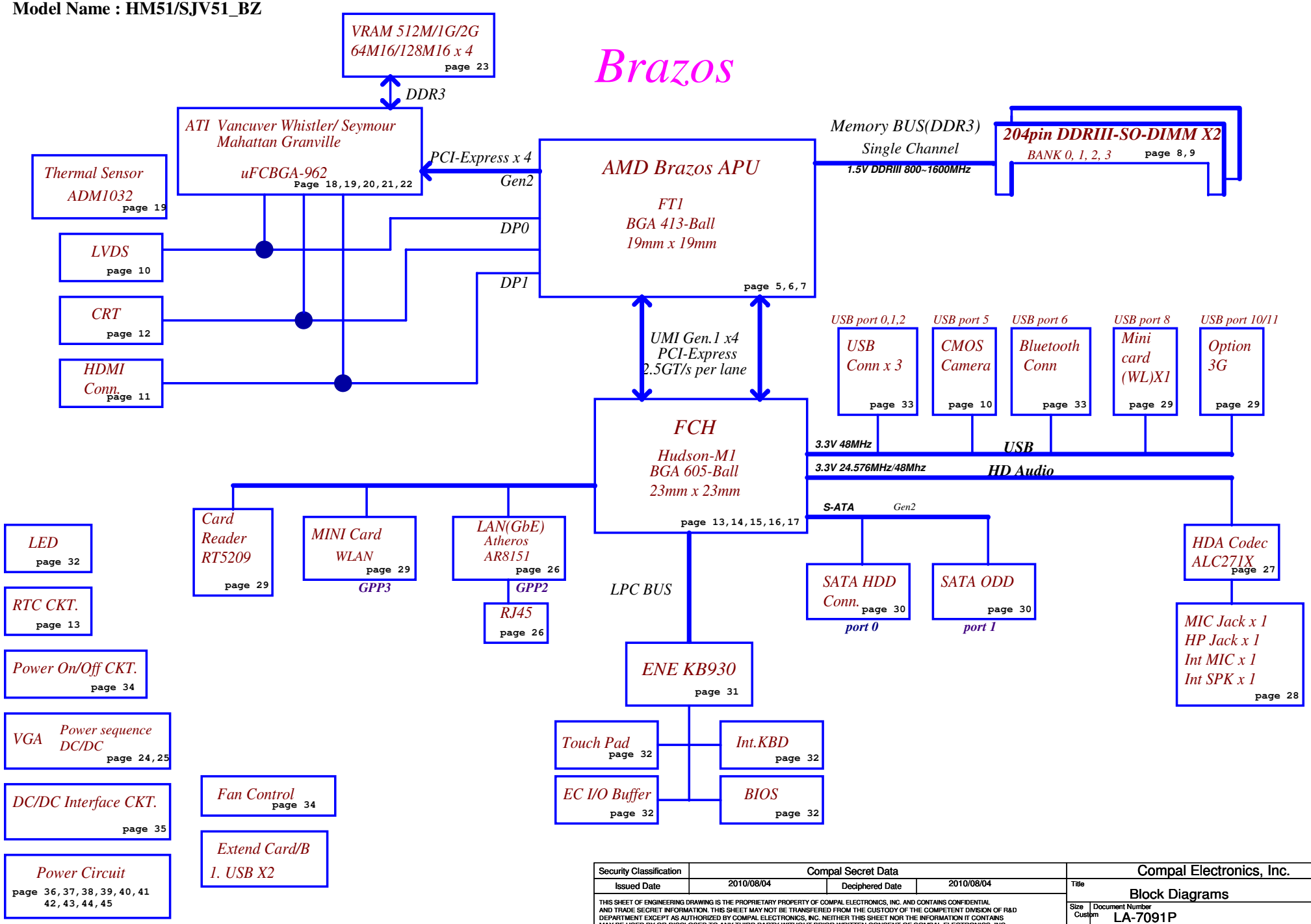
Title: Cover Page

Size	Document Number	Rev
Custom	<Doc>	0.1

Date: Monday, November 29, 2010 Sheet 1 of 48

Compal Confidential

Model Name : HM51/SJV51_BZ



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.			
Title: Block Diagrams			
Size: Custom	Document Number: LA-7091P		Rev: 0.1
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	VSB always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+5VALW	5V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for APU VDD10	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+3VSG	3.3V switched power rail for GPU	ON	OFF	OFF
+1.8VSG	1.8V switched power rail for GPU	ON	OFF	OFF
+1.5VSG	1.5V switched power rail for GPU	ON	OFF	OFF
+1.0VSG	1.0V switched power rail for GPU	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	NA

EC SM Bus2 address

Device	Address	HEX
EMC1403-2(GPU)	1001-101xb	9EH

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	
2	
3	
4	
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Display from APU	UMA@
Display from VGA	DISO@
Use VGA	VGA@
Muxless w/BACO	BACO@
Muxless wo/BACO	WOBACO@
Muxless	PX@
w/Vancouver Serise	VAN@
w/Manhttan Serise	MAN@
Bluetooth	BT@
AR8151	8151@

*UMA only : UMA@ BT@ 8151@
*DIS only : VGA@ DISO@ WOBACO@ VAN@ BT@ 8151@
*Muxless w/BACO : UMA@ VGA@ PX@ BACO@ VAN@ BT@ 8151@
Muxless wo/BACO : UMA@ VGA@ PX@ WOBACO@ VAN@ BT@ 8151@

For Robson:

DIS only : VGA@ DISO@ WOBACO@ MAN@ BT@ 8151@
Muxless w/BACO : UMA@ VGA@ PX@ BACO@ MAN@ BT@ 8151@
Muxless wo/BACO : UMA@ VGA@ PX@ WOBACO@ MAN@ BT@ 8151@

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Title: Notes List

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Power-Up/Down Sequence

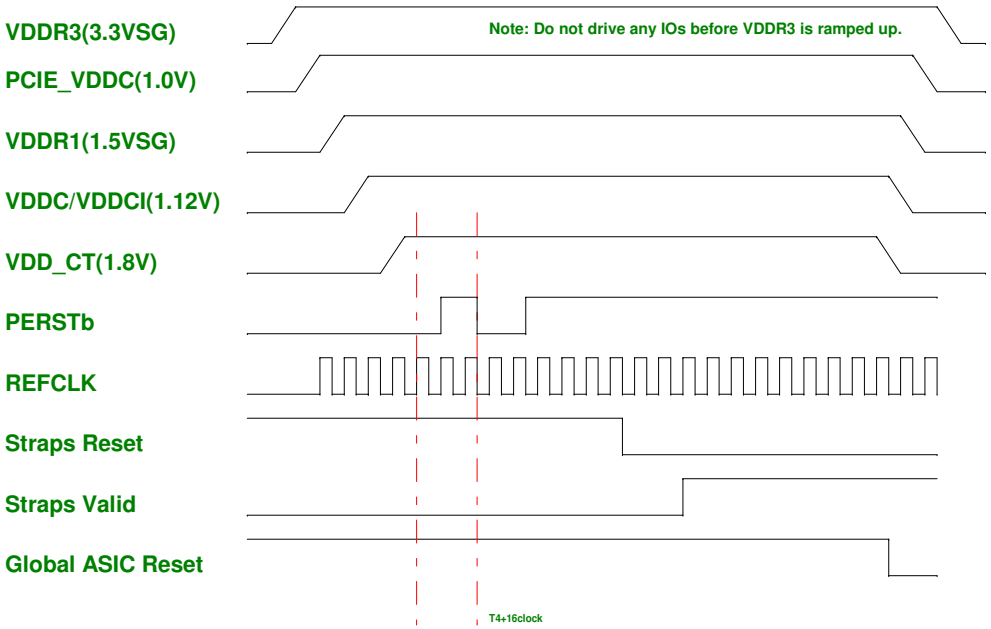
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



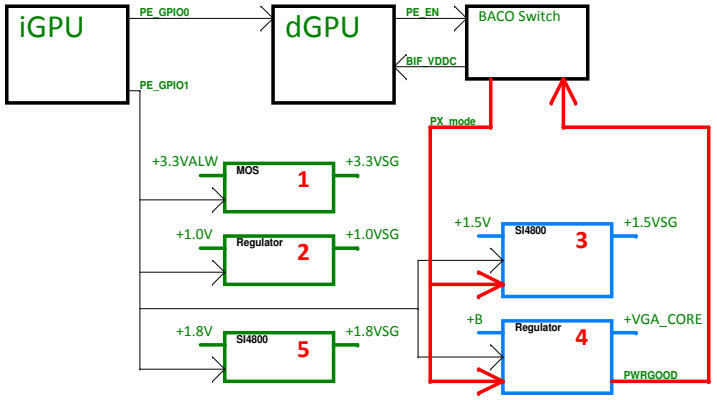
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Compal Electronics, Inc.

Title: dGPU Block Diagram

Size	Document Number	Rev
Custom	LA-7091P	0.1

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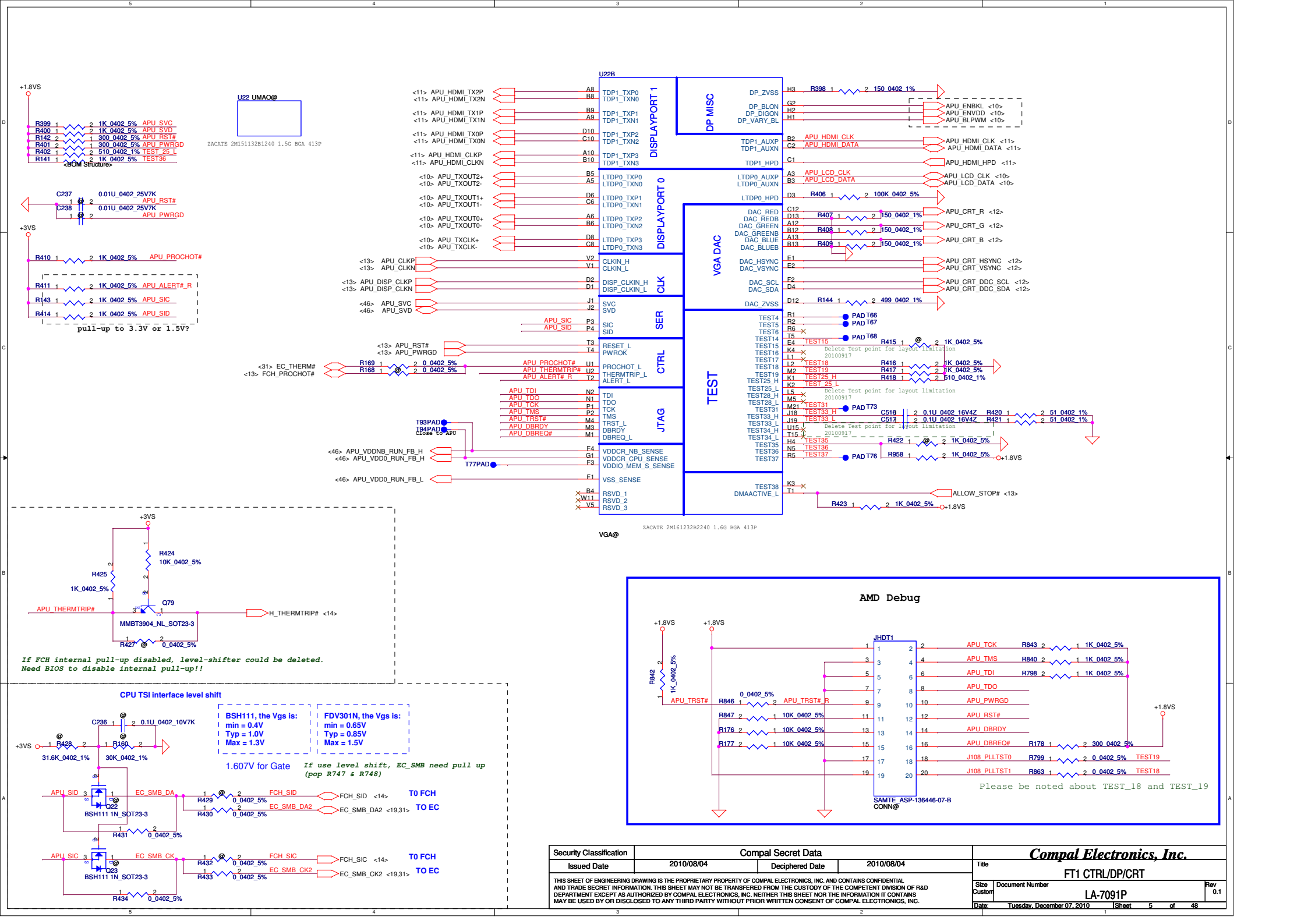

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title	FT1 CTRL/DP/CRT	
Size: Custom	Document Number: LA-7091P	Rev: 0.1
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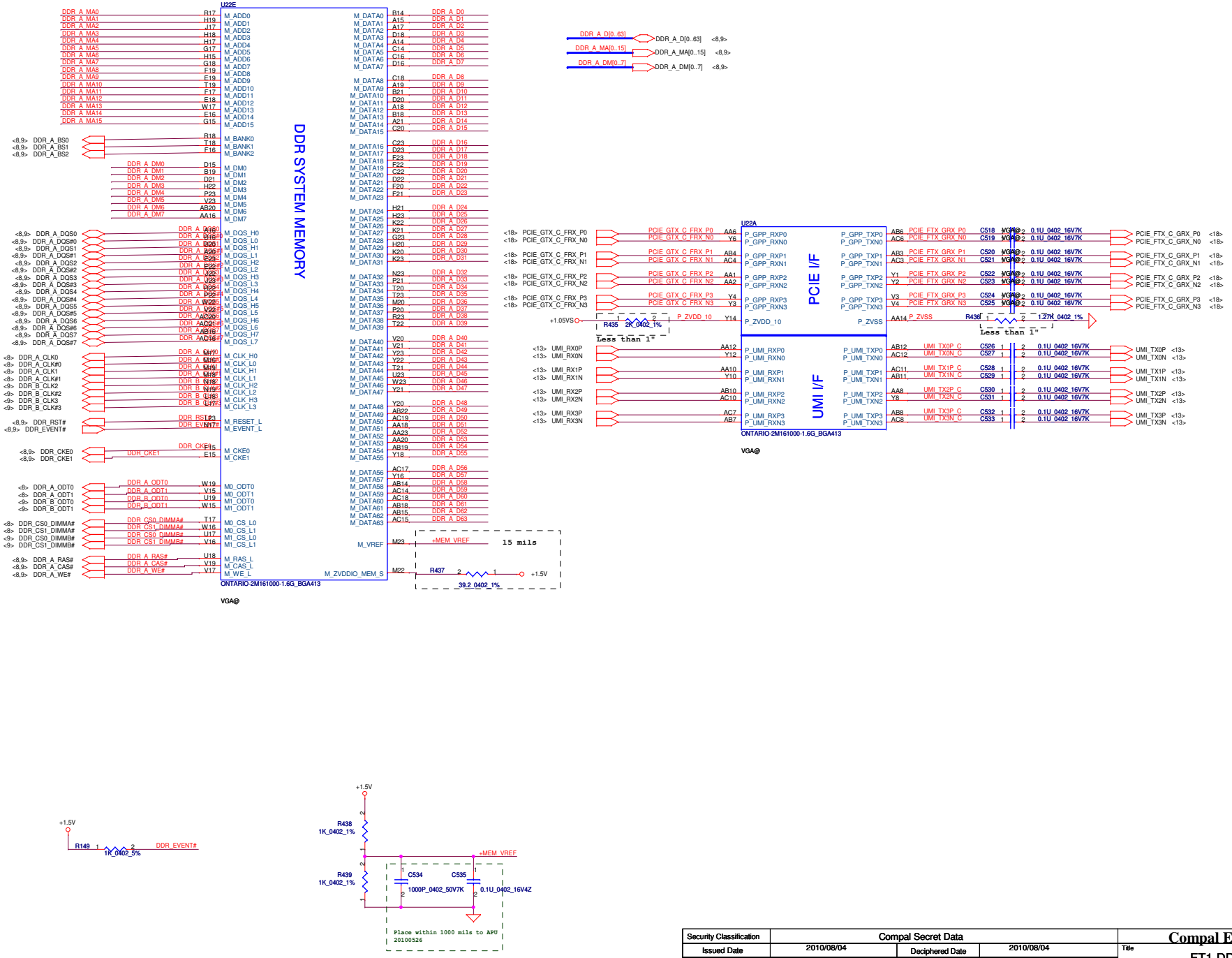


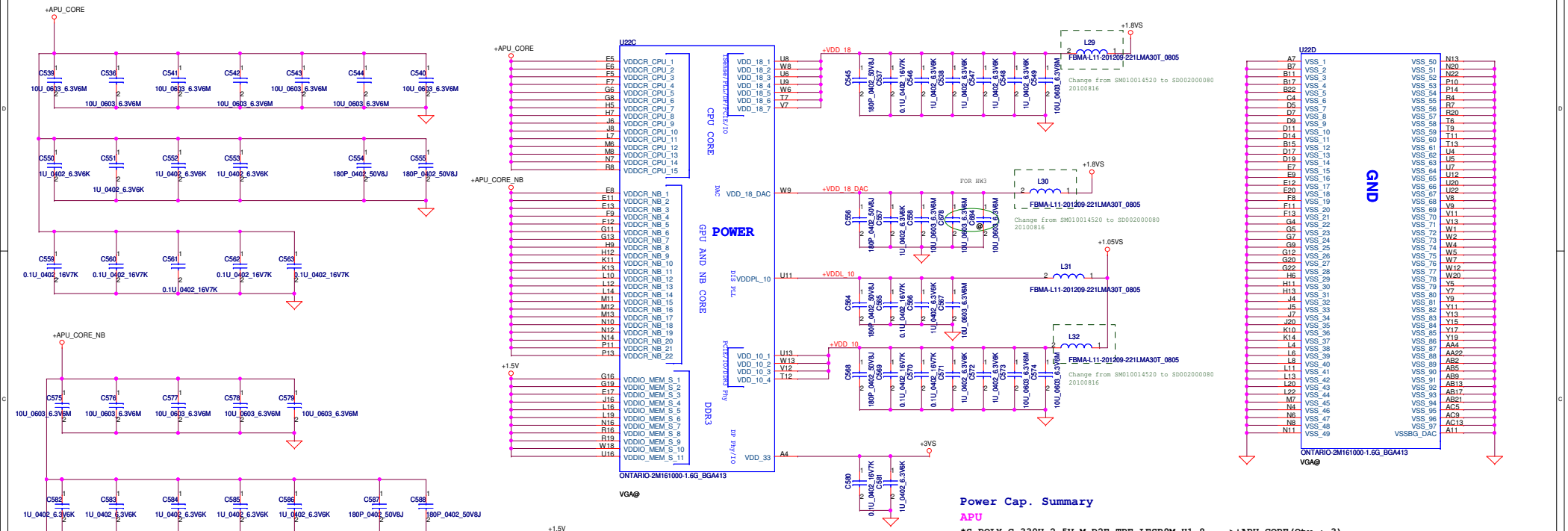
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

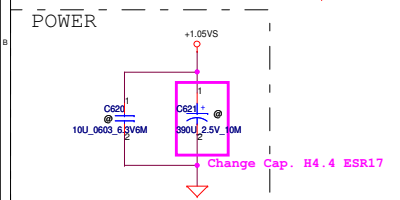
Compal Electronics, Inc.

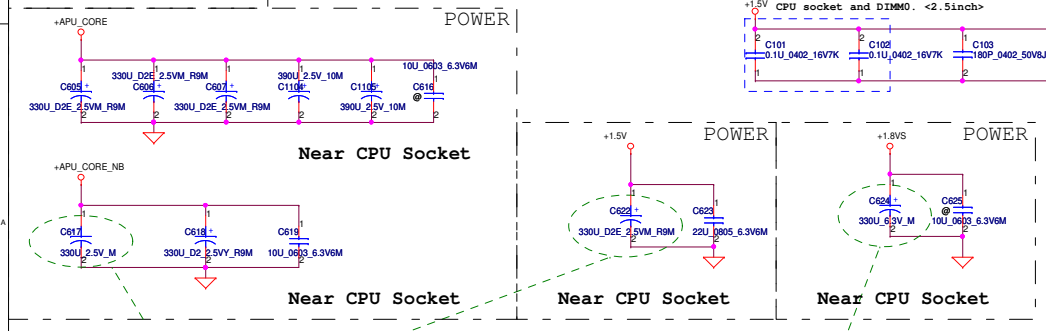
Title: FT1 DDRIII/UMI/PCIE

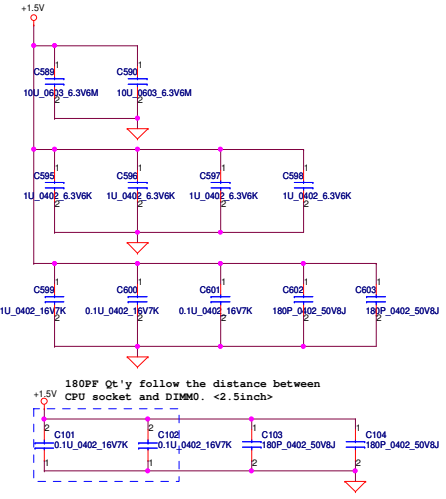
Size	Document Number	Rev
C	LA-7091P	0.1

Date: Tuesday, December 07, 2010 Sheet 6 of 48









Power Cap. Summary

APU

```
*S POLY C 330U 2.5V M D2E TPE LESR9M H1.8 --->+APU_CORE(Qty : 3)
*S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 --->+APU_CORE_NB(Qty : 1)
*S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->1.05VS(Qty : 1)
*S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 --->+1.5V(Qty : 1)
*S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU --->+1.8VS(Qty : 1)
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+APU_CORE(Qty : 2) Reverse
S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLPS --->+APU_CORE_NB(Qty : 1) Reverse
                                           +1.5V(Qty : 1) Reverse
```

DDR3

```
S POLY C 330U 2V M X LESR6M SX H1.9 --->1.5V(Qty : 1) Reserve
```

FCH

```
*S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 --->1.1VS(Qty : 1)
```

GPU

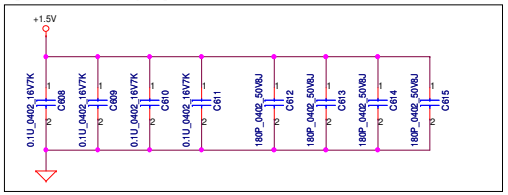
```
*S POLY C 330U 2V M X LESR6M SX H1.9 --->VGA_CORE(Qty : 1)
```
Change as OS_CON Cap. next phase

```
*S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+VGA_CORE(Qty : 1)
S POLY C 330U 2V M X LESR6M SX H1.9 --->VGA_CORE(Qty : 1) Reserve
*S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+1.5VSG(Qty : 1)
```

USB

```
*S_A-P_CAP 220U 6.3V M C45 R17M SVPE H4.4 --->+USB_VCCA(Qty : 1)
```

By case (Along split)



*(330uF_6.3V_4.2L_ESR17m)*1=(SF000002200)*

*(S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU)*1=(SF000002000)*
20100813

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Compal Electronics, Inc.			
Title	P07-FT1 PWR/VSS		
Size C	Document Number LA-7091P		Rev 0.1
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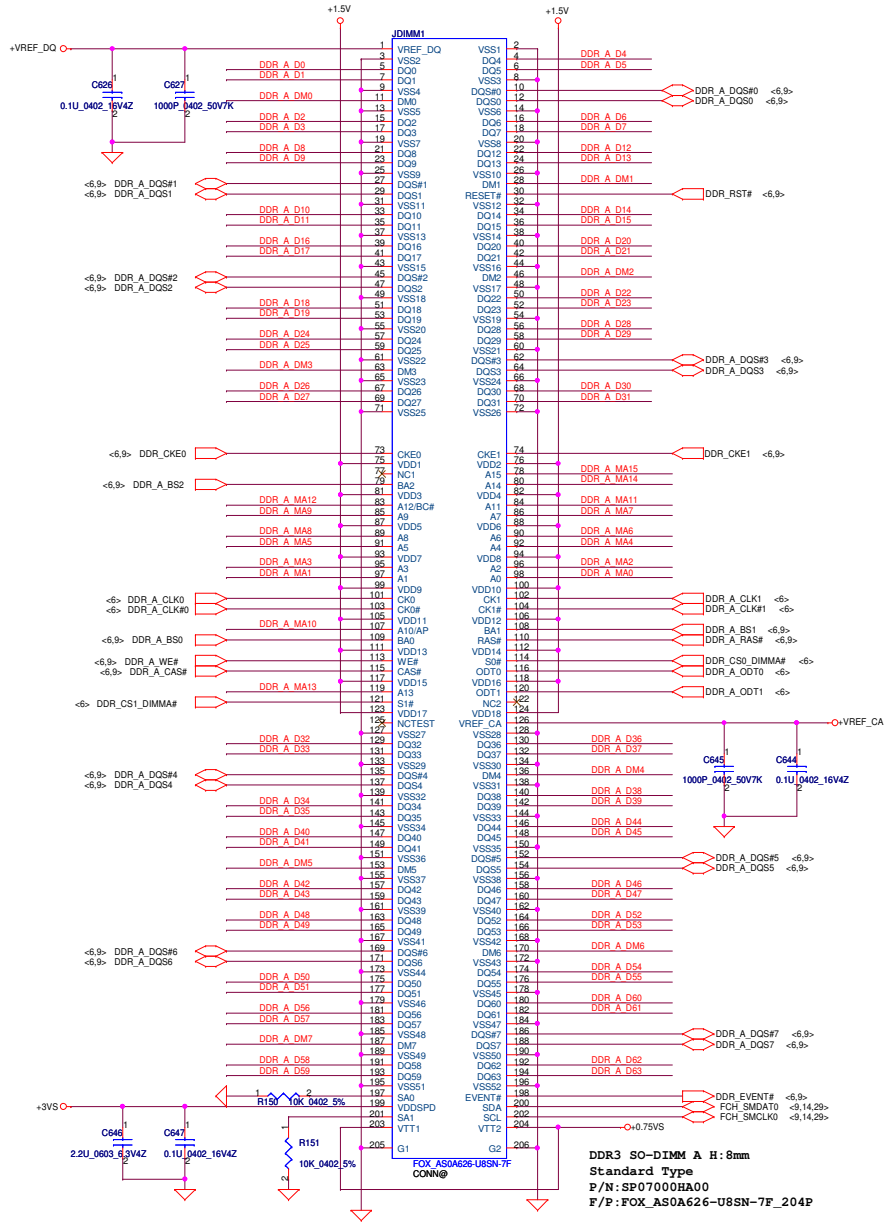

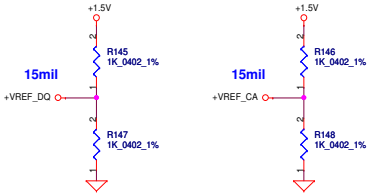

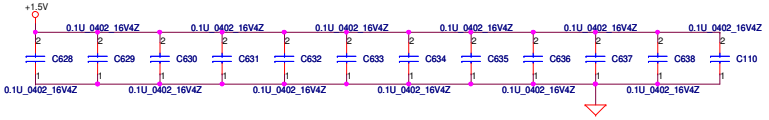

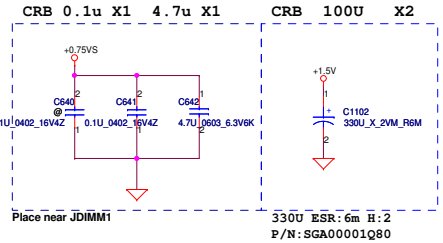

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Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDR3 SODIMM-I Socket

Size	Document Number	Rev
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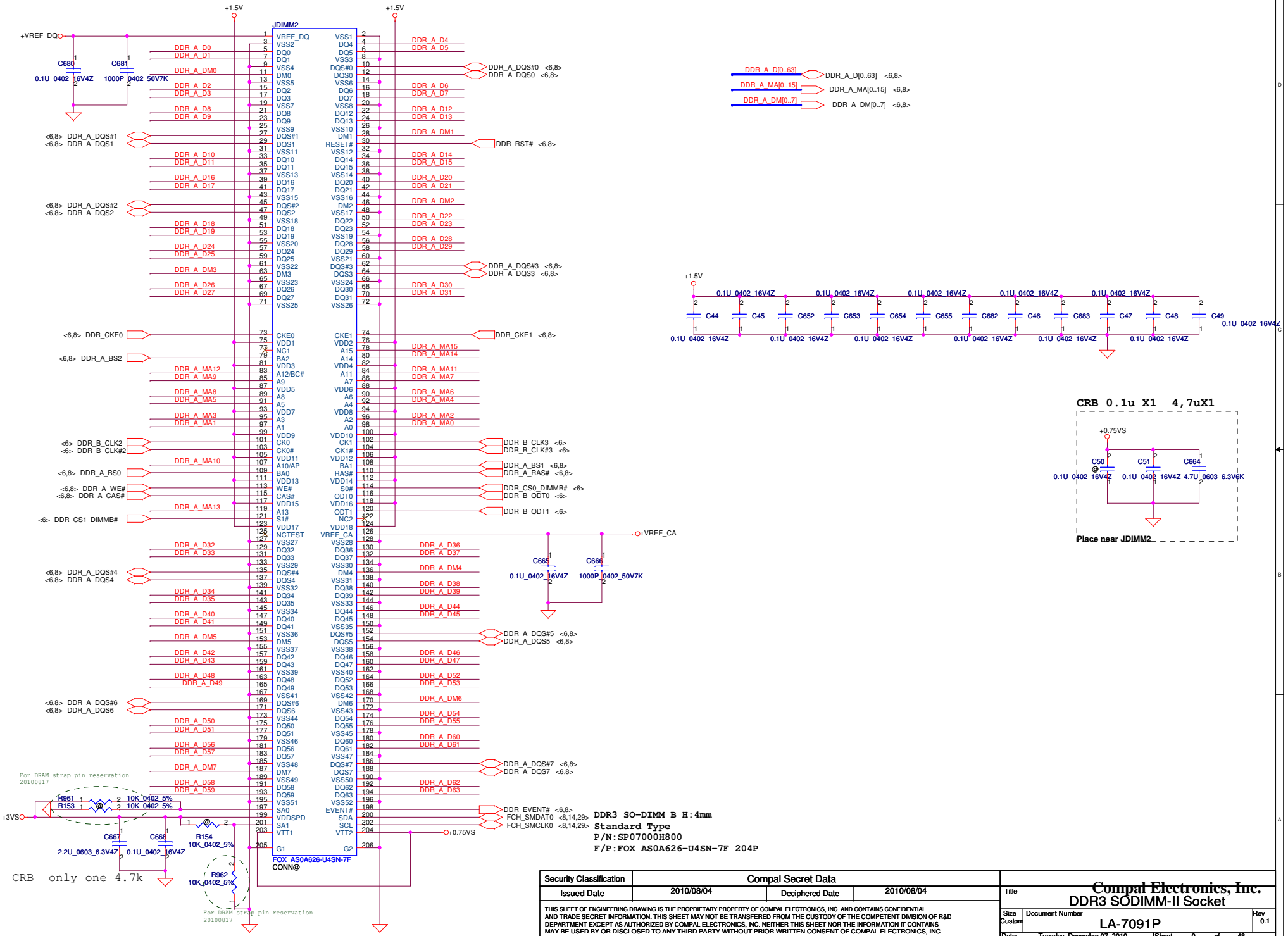

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Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: DDR3 SODIMM-II Socket

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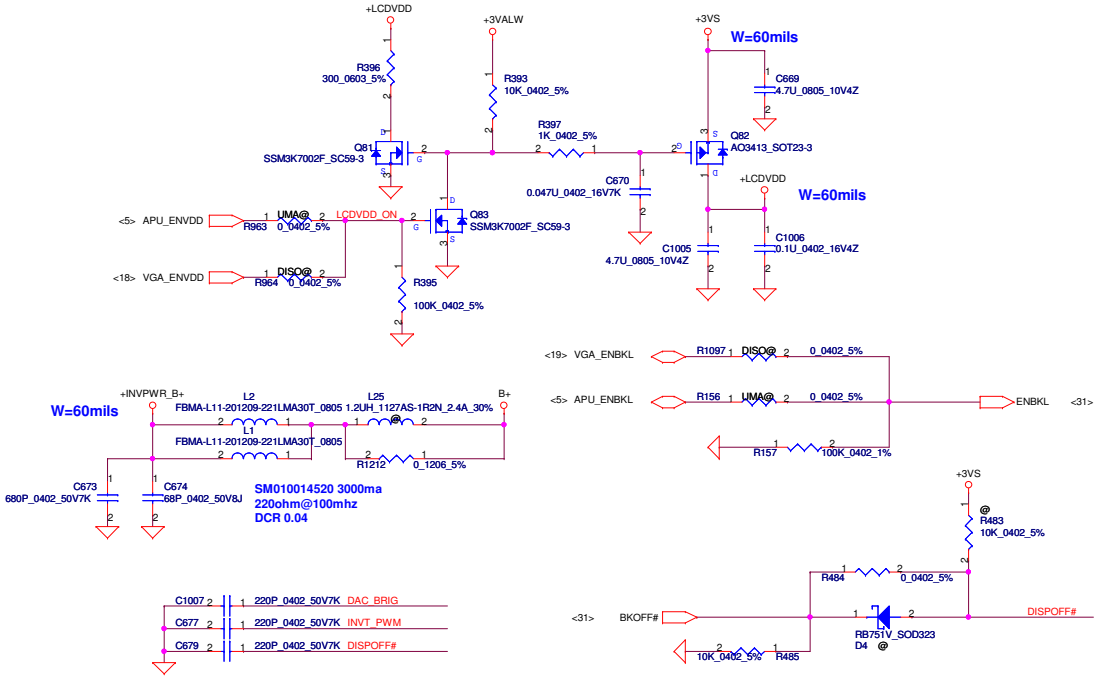
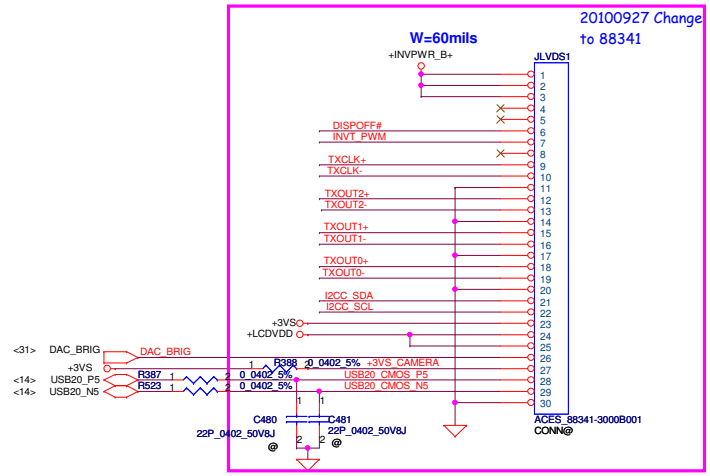
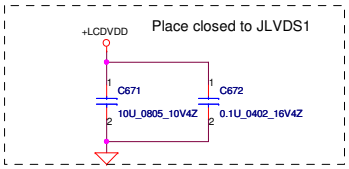
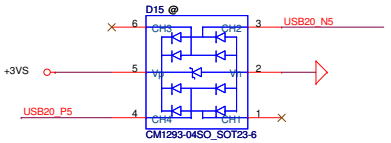
LCD POWER CIRCUIT



LCD/LED PANEL Conn.

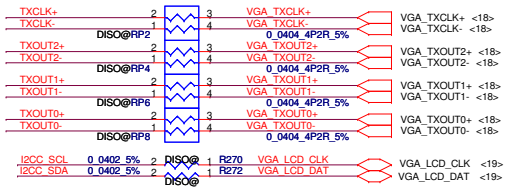




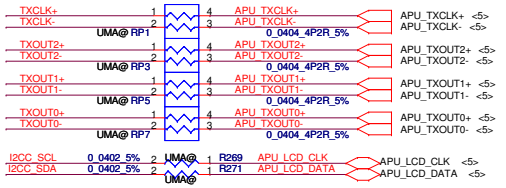


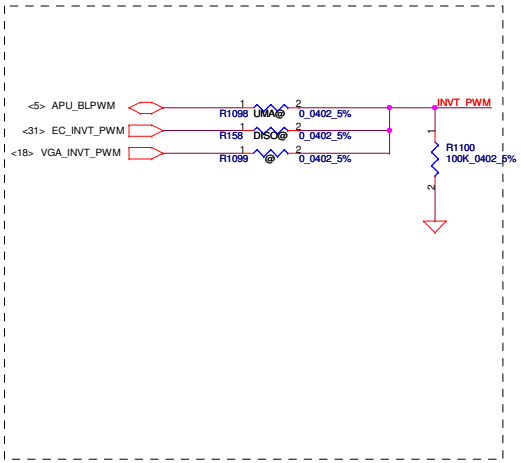
Change P/N as SC300000B00

VGA ONLY



UMA ONLY





LVDS Function Change list For R01

1.Add DISO@ and VGA path connect circuit

2.Remove reserve DMIC circuit

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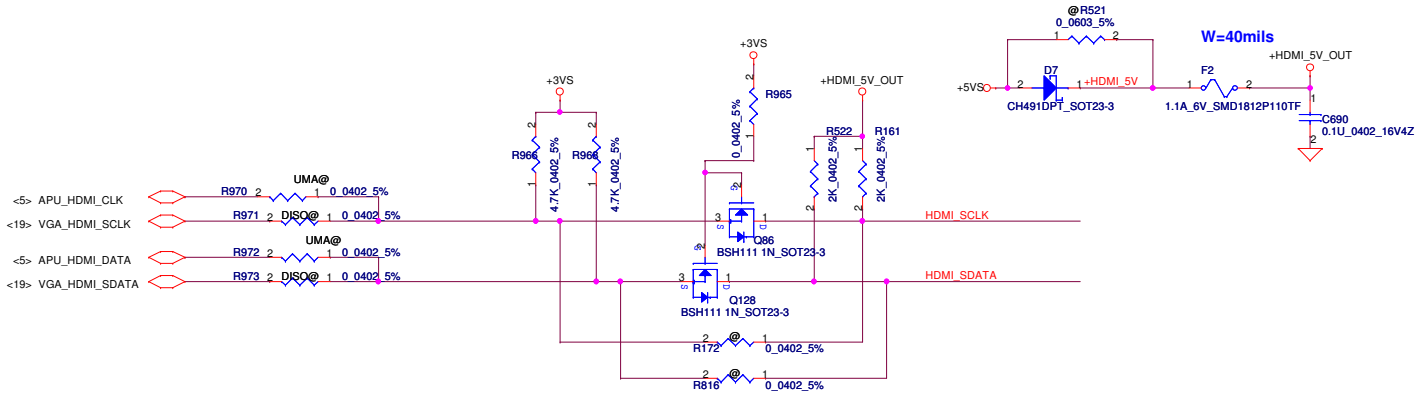
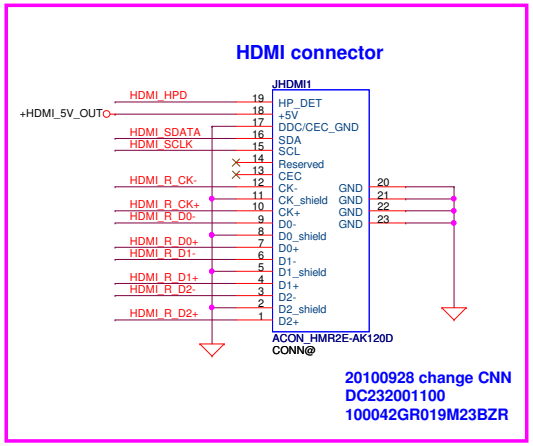
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: Custom	Document Number: LA-7091P		Rev: 0.1
Date: Tuesday, December 07, 2010		Sheet 10 of 48	



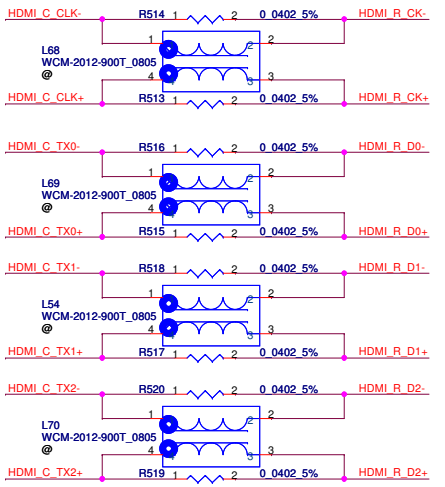


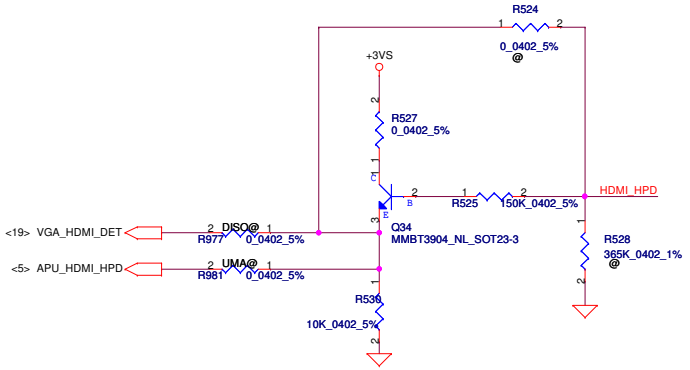
HDMI Function Change list For R01

1.Add DISO@ and VGA path connect circuit
2.Level Shift implement
3.Add termination resistance option

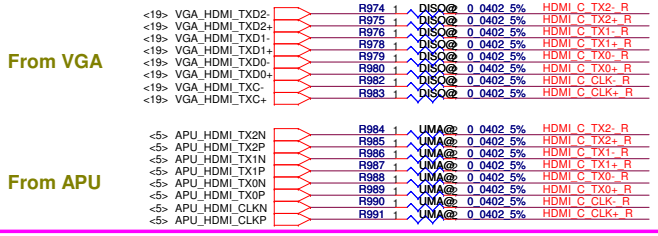
Place closed to JHDMI1

SM070001310 400ma 90ohm@100mhz DCR 0.3

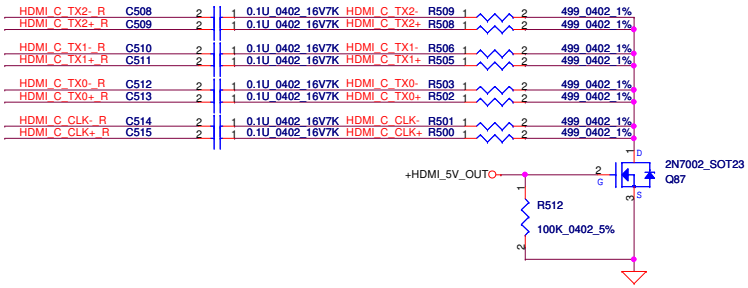




Use common via on related pair



Place closed to JHDMI1



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Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
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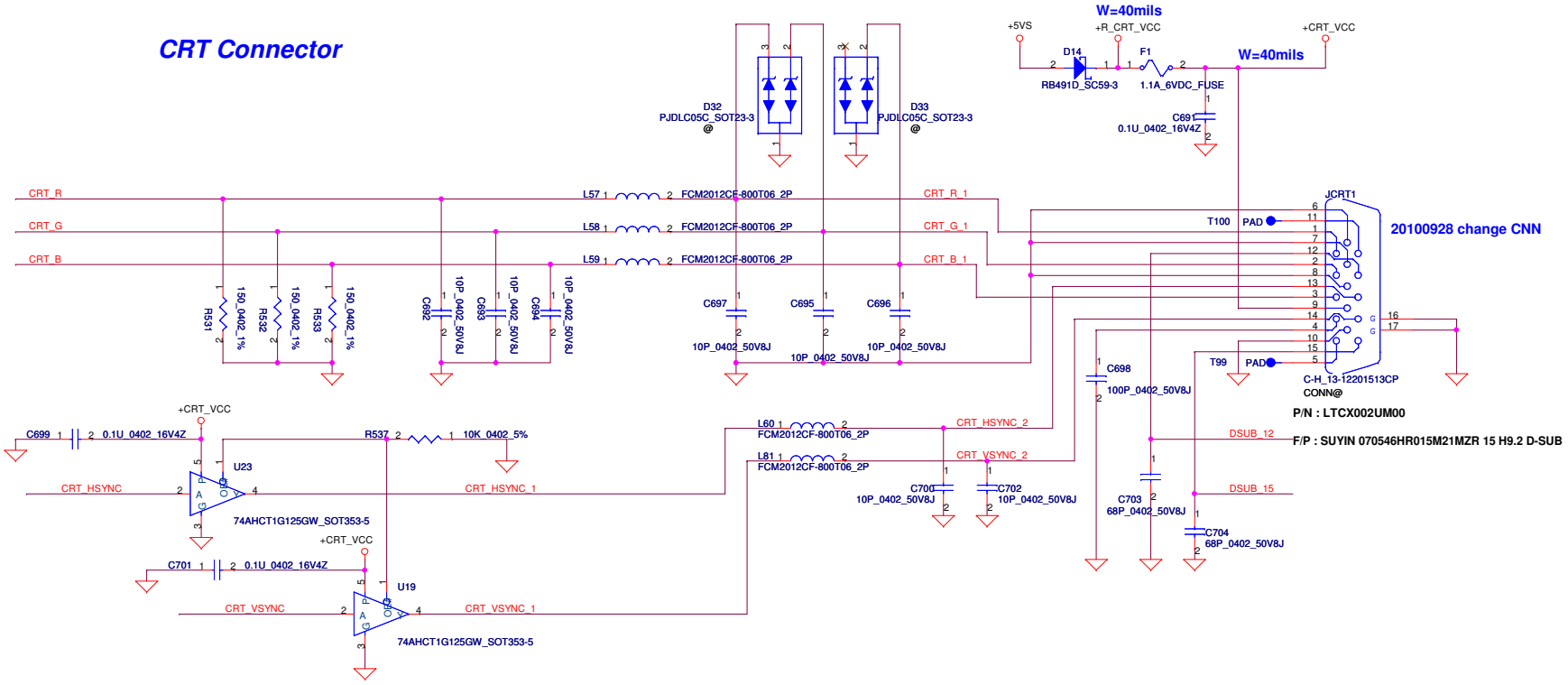
CRT Connector



CRTI Function Change list For R01

1.Add DISO@ and VGA path connect circuit

2.Level Shift implement

Use common via on related pair

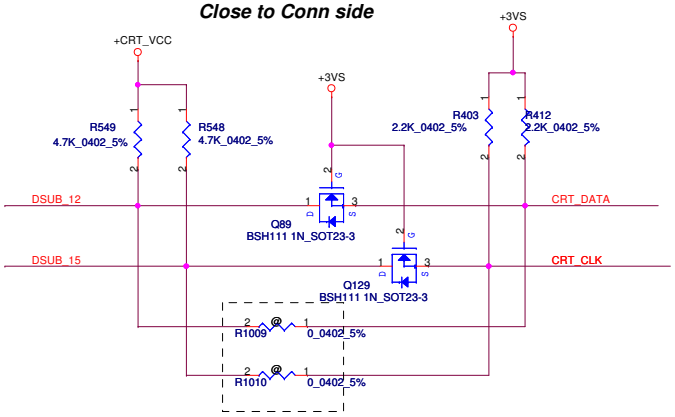
From APU

<5> APU_CRT_R	APU_CRT_R	R995	UMA@	0_0402_5%	CRT_R
<5> APU_CRT_G	APU_CRT_G	R996	UMA@	0_0402_5%	CRT_G
<5> APU_CRT_B	APU_CRT_B	R997	UMA@	0_0402_5%	CRT_B
<5> APU_CRT_HSYNC	APU_CRT_HSYNC	R998	UMA@	0_0402_5%	CRT_HSYNC
<5> APU_CRT_VSYNC	APU_CRT_VSYNC	R999	UMA@	0_0402_5%	CRT_VSYNC
<5> APU_CRT_DDC_SDA	APU_CRT_DDC_SDA	R1000	UMA@	0_0402_5%	CRT_DATA
<5> APU_CRT_DDC_SCL	APU_CRT_DDC_SCL	R1001	UMA@	0_0402_5%	CRT_CLK

From VGA

<19> VGA_CRT_R	VGA_CRT_R	R1002	DISO@	0_0402_5%	CRT_R
<19> VGA_CRT_G	VGA_CRT_G	R1003	DISO@	0_0402_5%	CRT_G
<19> VGA_CRT_B	VGA_CRT_B	R1004	DISO@	0_0402_5%	CRT_B
<19> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R1005	DISO@	0_0402_5%	CRT_HSYNC
<19> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R1006	DISO@	0_0402_5%	CRT_VSYNC
<19> VGA_CRT_DATA	VGA_CRT_DATA	R1007	DISO@	0_0402_5%	CRT_DATA
<19> VGA_CRT_CLK	VGA_CRT_CLK	R1008	DISO@	0_0402_5%	CRT_CLK

Close to Conn side



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title	CRT Connector	
Size: Custom	Document Number: LA-7092P	Rev: 0.1
Date: Tuesday, December 07, 2010	Sheet 12 of 48	

For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

U31E

PCI EXPRESS I/F

JMINI2
Card reader
LAN
WLAN

PCIE_RST_L
A_RST_L
UMI_TX0P
UMI_TX0N
UMI_TX1P
UMI_TX1N
UMI_TX2P
UMI_TX2N
UMI_TX3P
UMI_TX3N
UMI_RX0P
UMI_RX0N
UMI_RX1P
UMI_RX1N
UMI_RX2P
UMI_RX2N
UMI_RX3P
UMI_RX3N
PCIE_CALRP
PCIE_CALRN
GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N
GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N

PCI CLKS

PCICLK0
PCICLK1/GPO36
PCICLK2/GPO37
PCICLK3/GPO38
PCICLK4/14M_OSC/GPO39
PCIRST_L

PCI I/F

AD0/GPIO0 … AD31/GPIO31
CBE0_L … CBE3_L
FRAME_L
DEVSEL_L
IRDY_L
TRDY_L
PAR
STOP_L
PERR_L
SERR_L
REQ0_L
REQ1_L/GPIO40
REQ2_L/CLK_REQ8_L/GPIO41
REQ3_L/CLK_REQ5_L/GPIO42
GNT0_L
GNT1_L/GPO44
GNT2_L/GPO45
GNT3_L/CLK_REQ7_L/GPIO46
CLKRUN_L
LOCK_L
INTE_L/GPIO32
INTF_L/GPIO33
INTG_L/GPIO34
INTH_L/GPIO35

LPC

LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME_L
LDRQ0_L
LDRQ1_L/CLK_REQ6_L/GPIO49
SERIRQ/GPIO48

CPU

ALLOW_LDTSTP/DMA_ACTIVE_L
PROCHOT_L
LDT_PG
LDT_STP_L
LDT_RST_L

RTC

32K_X1
32K_X2
RTCCLK
INTRUDER_ALERT_L
VDDBT_RTC_G

CLOCK GENERATOR

close to FCH within 1"

PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
GPP_CLK4P
GPP_CLK4N
GPP_CLK5P
GPP_CLK5N
GPP_CLK6P
GPP_CLK6N
GPP_CLK7P
GPP_CLK7N
GPP_CLK8P
GPP_CLK8N
14M_25M_48M_OSC
25M_X1
25M_X2

21807-A11-HUDSON-M1_FCBGA605

LAN
WLAN
Mini2

Del 1012

Close to FCH

25MHZ_20PF_7A25000012

32.768KHZ_12.5PF_Q13MC14610050_10PPM

for Clear CMOS

Need to check material?

For DVT 1011

RTC BATT Conn.

P/N: SP07000OU00
F/P: SUYIN_060003HA002G202ZL_2P

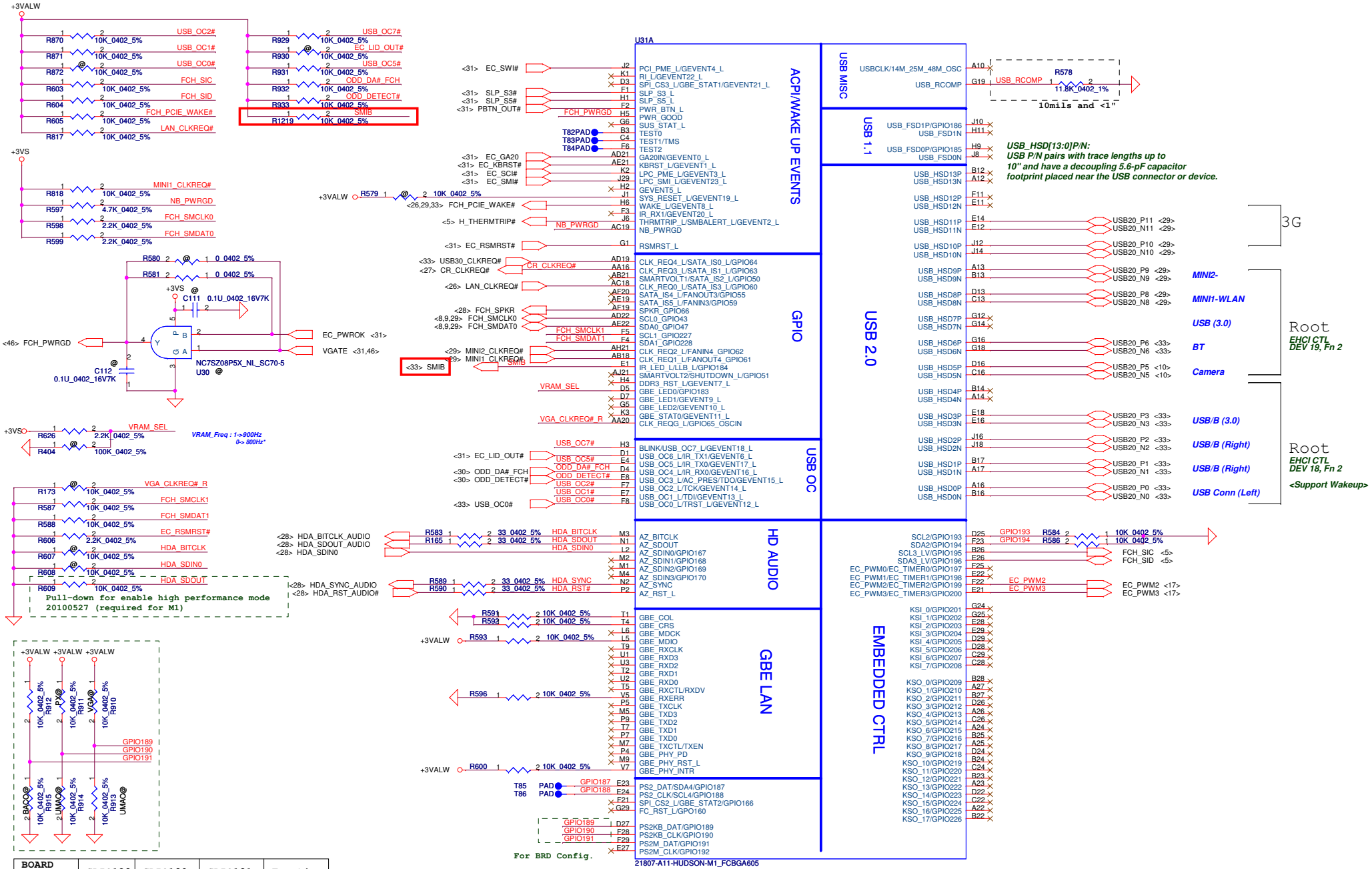
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: FCH PCIE/PCI/ACPI/LPC/RTC

Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 | Sheet 13 of 48



BOARD Config.	GPIO189	GPIO190	GPIO191	Function
	0	0	1	UMA
	1	0	1	DIS
	1	1	1	PX3
	1	1	0	PX4

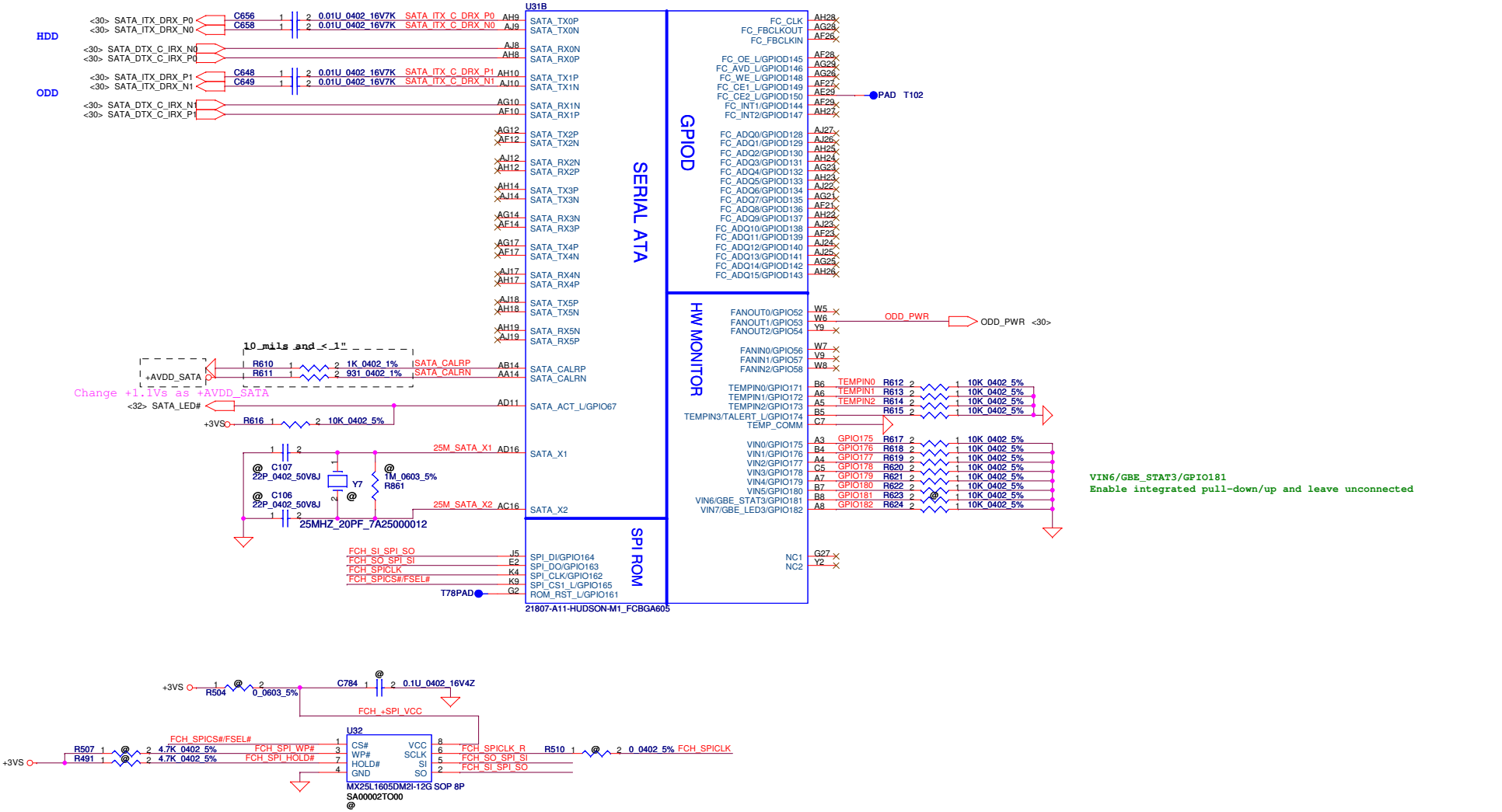
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: FCH HDA/USB/ACPI

Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 | Sheet 14 of 48



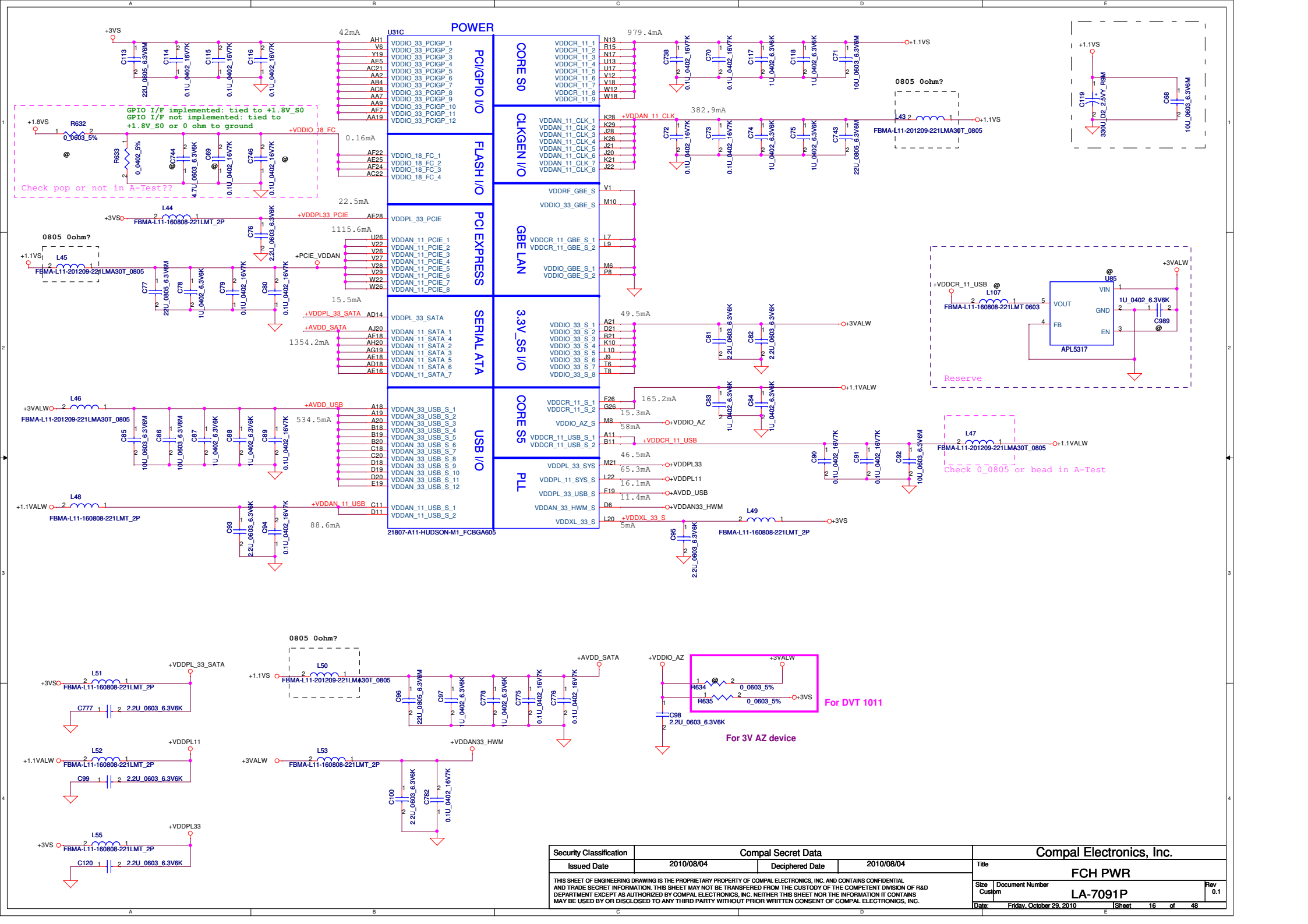
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: FCH-SATA/SPI

Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 | Sheet 15 of 48



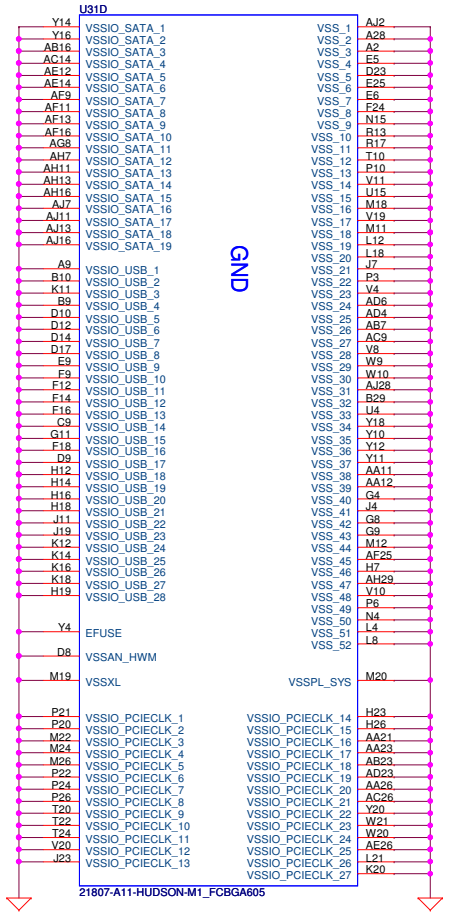
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: FCH PWR

Size: Custom | Document Number: LA-7091P | Rev: 0.1

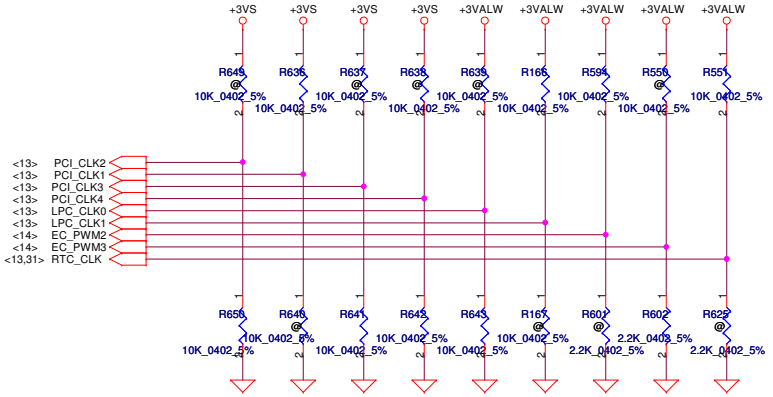
Date: Friday, October 29, 2010 | Sheet 16 of 48



REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
PULL HIGH	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H.L) DEFAULT
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)

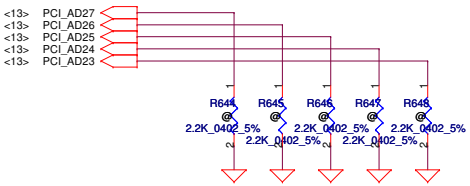


DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH		USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW		BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function check default



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

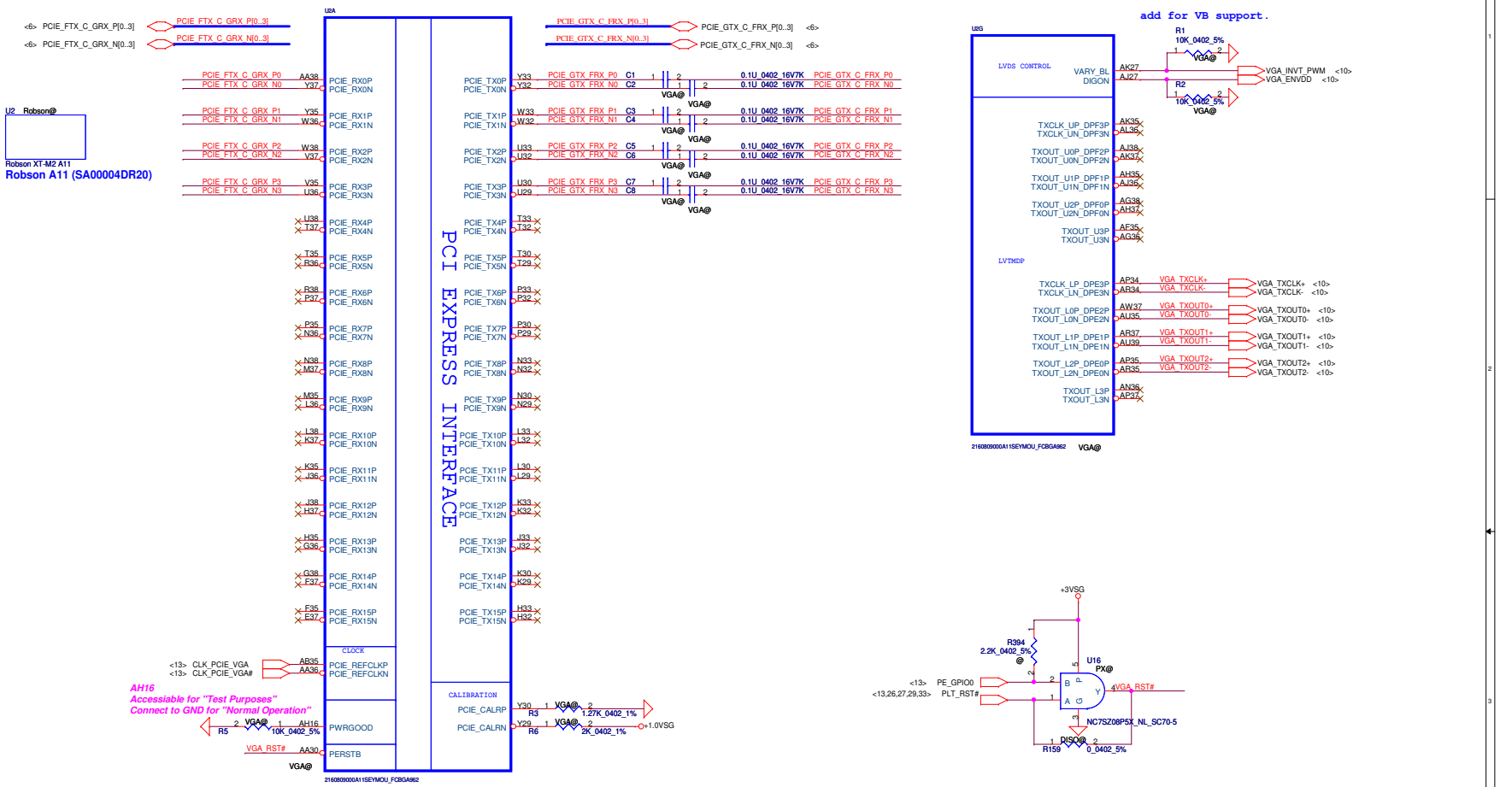
Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size: Custom | Document Number: LA-7091P | Rev: 0.1

Date: Tuesday, December 07, 2010 | Sheet 17 of 48

GFX PCIE LANE REVERSAL



Seymour XT P/N: SA000047H00 (S IC 216-0809000 A11 SEYMOUR XT M2 0FH)

Robson XT P/N: SA00004DR20 (S IC 216-0774211 A11 Robson XT M2)

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Madison_ PCIE / LVDS

Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 | Sheet 18 of 48

Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21 GENERICC GPIO5	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour

NC on Park and Robson

NC on Park, Robson and Seymour

NC on Park, Robson and Seymour

Not share via for other GND

External VGA Thermal Sensor

U4 VGA@ ADM1032ARMZ-2REEL_MSOP8

Address 1001 101X b

Q1A Q1B DMN66D0LDW-7_SOT363-6

Seymour(XT)

VRAM \ Location	VRAM_ID3 <vendor1>	VRAM_ID2	VRAM_ID1	VRAM_ID0
Hynix (512M)	1	1	1	0
Samsung (512M)	0	0	1	1

SA000041S40 Hynix 64MX16 H5TQ1G63DER-11C

SA00004GS10 Samsung 64M16 K4W1G1646G-BC11

Check option2 need to be added or not?

Internal PD

PD-Reset

FLASH ROM

U5 TYPE 1 M25P10-AVMN6P

Y1 VGA@ 27MHZ_16PF_XSH027000FG1H

GPIO_0 will use to control PSI in the future product

NC on Park

AL31 Manhattan/Vancouver is NC, Boardway is ADC input(0-1V) use measure regulator current or temperature

NC on Whistler and Seymour

In Whistler and Seymour, change to GENLK_CLK, GENLK_VSYNC for Global Swap Lock on multiple GPUs

Except A2VSSQ change to TSVSSQ, others are NC on Whistler and Seymour

NC on Park, Robson and Seymour

CRT

NC on Park, Robson and Seymour

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

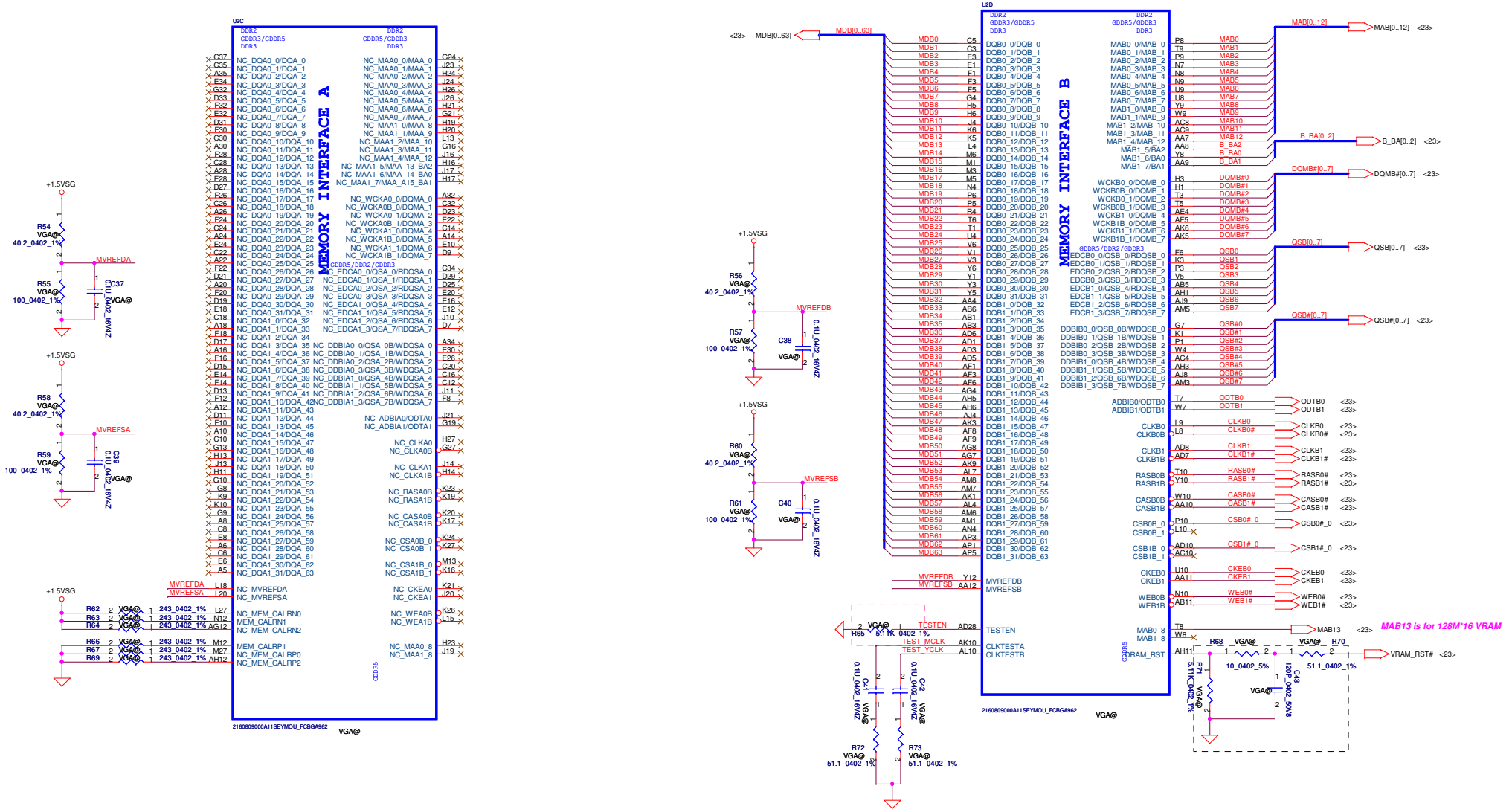
Compal Electronics, Inc.

Title: Madison_Strape/DP/HDMI//CRT

Size: Custom | Document Number: LA-7091P | Rev: 0.1

Date: Tuesday, December 07, 2010 | Sheet 19 of 48

Robson,Seymour only support single channel memory (channel B only)



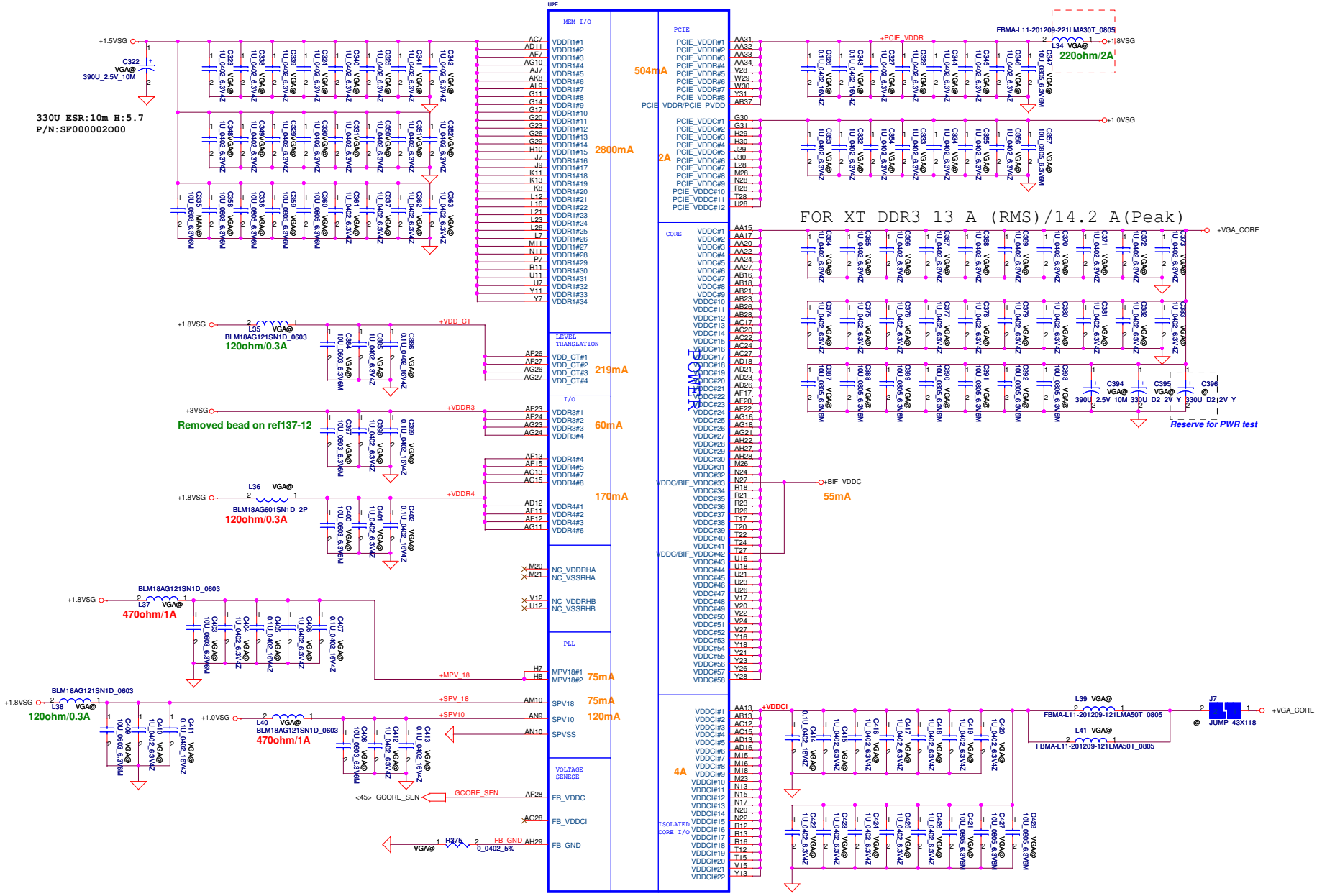
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Memory

Size: Custom | Document Number: LA-7091P | Rev: 0.1

Date: Tuesday, December 07, 2010 | Sheet 20 of 48



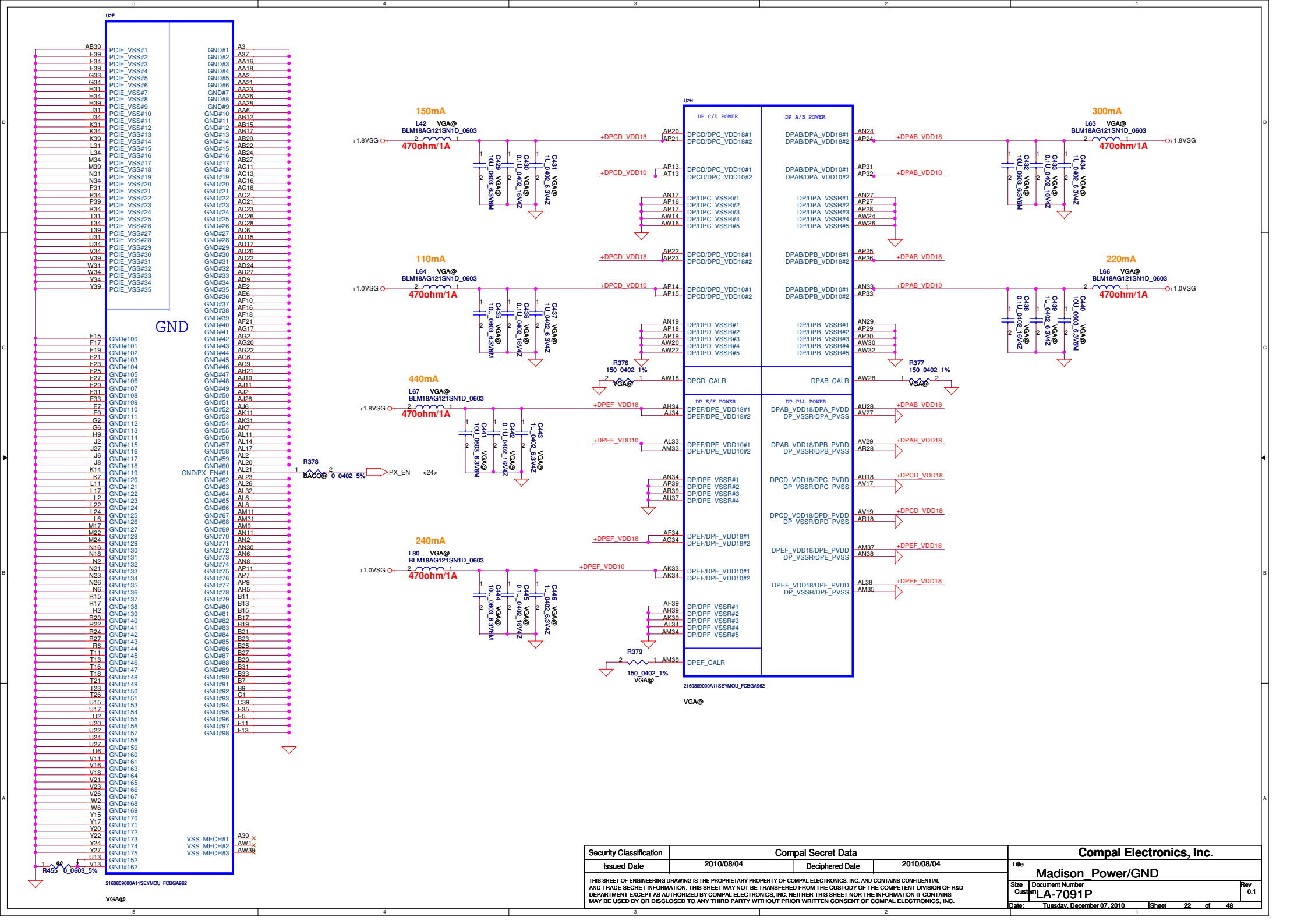
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Madison_Power/GND

Size: Custom | Document Number: LA-7091P | Rev: 0.1

Date: Tuesday, December 07, 2010 | Sheet 21 of 48



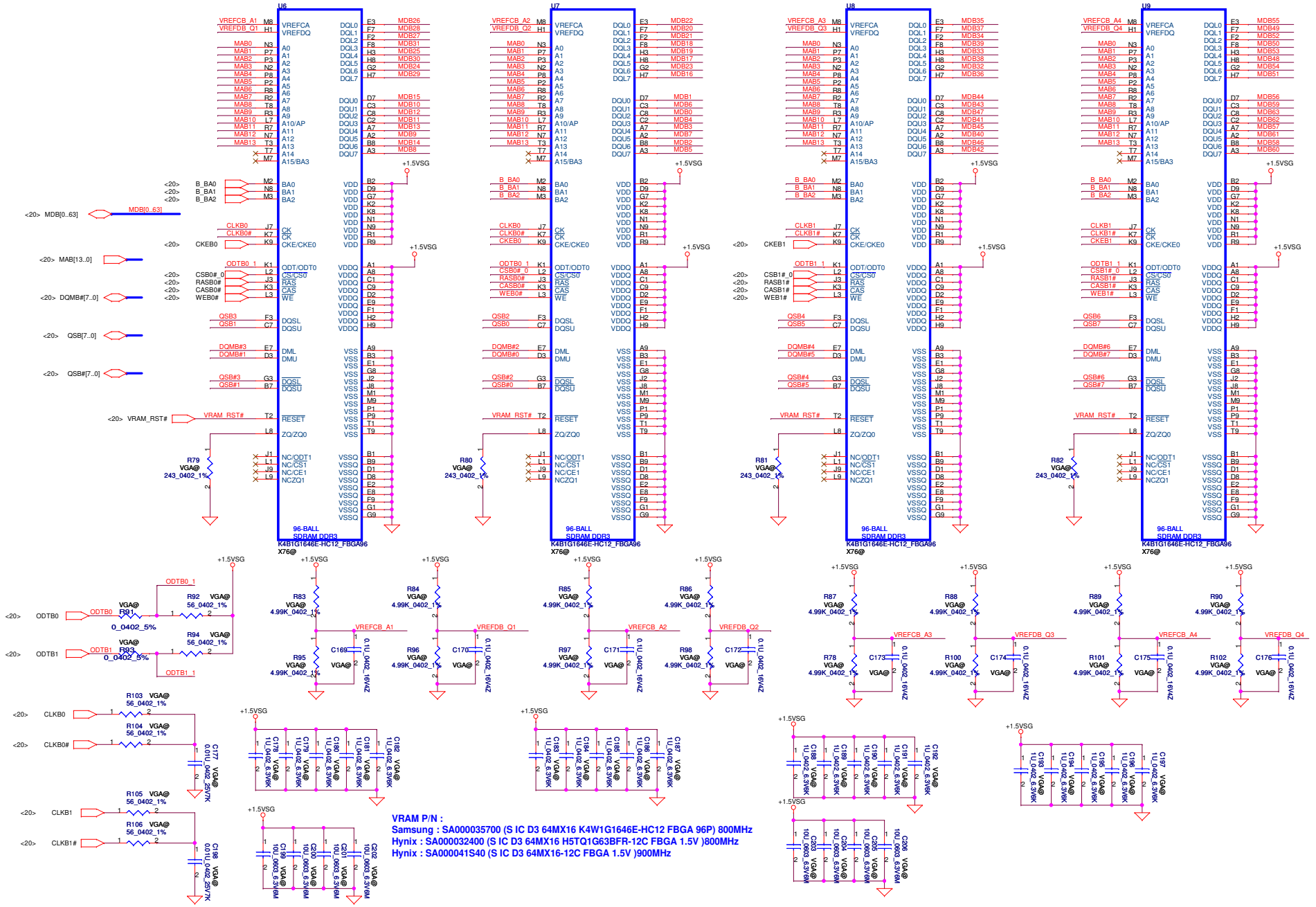
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: Madison_Power/GND

Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 Sheet 22 of 48



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

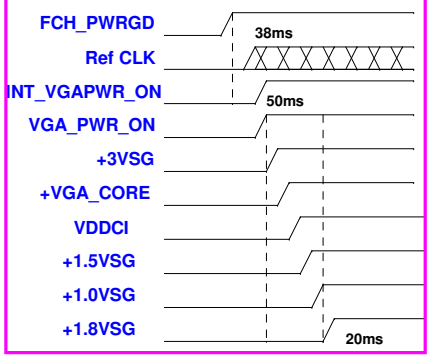
Compal Electronics, Inc.

Title: **VRAM_DDR3 / Channel B**

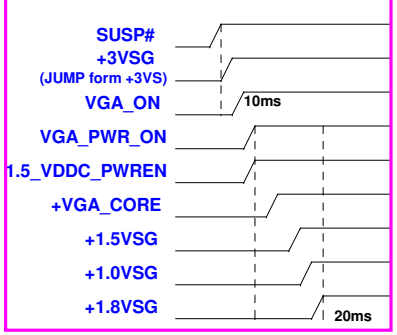
Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 | Sheet 23 of 48

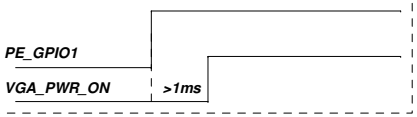
Power Sequence of Granville



Power Sequence of Whistler and Seymour



For PX sequence, >1mS delay is required between PE_GPIO1 and VGA_PWR_ON

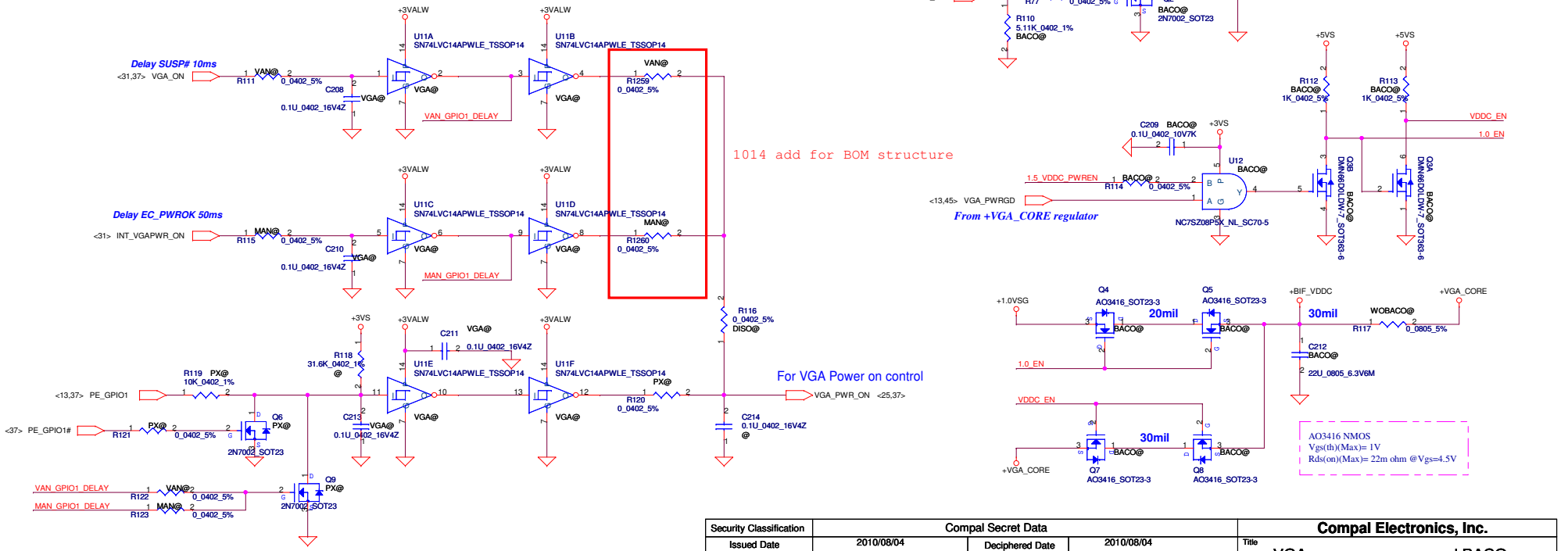


VGA Muxless and Dis only Status Mapping table			
	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

VGA Power ON Circuit



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

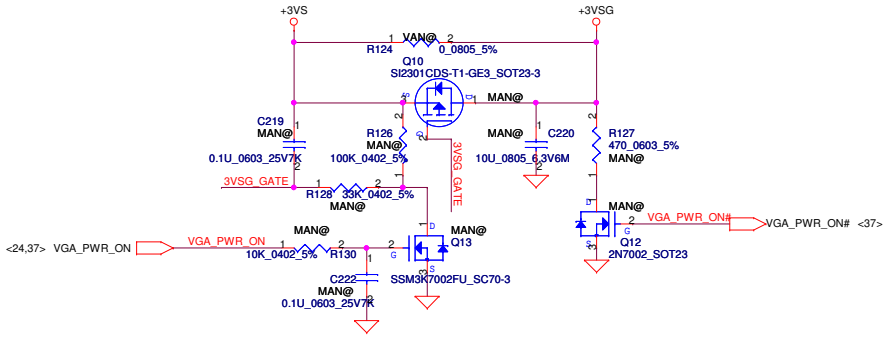
Compal Electronics, Inc.

Title: VGA power sequence and BACO

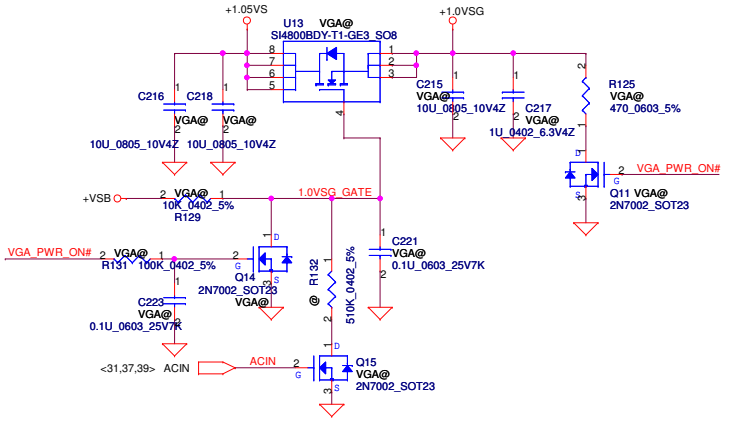
Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 | Sheet 24 of 48

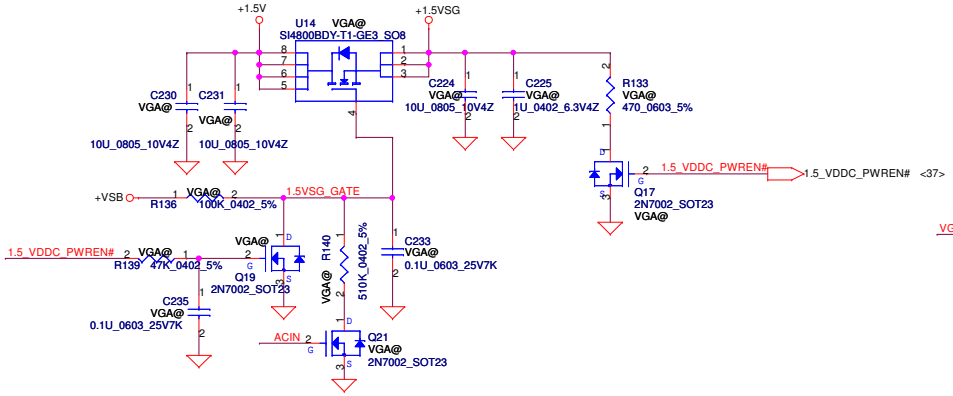
+3.3VS TO +3.3VSG



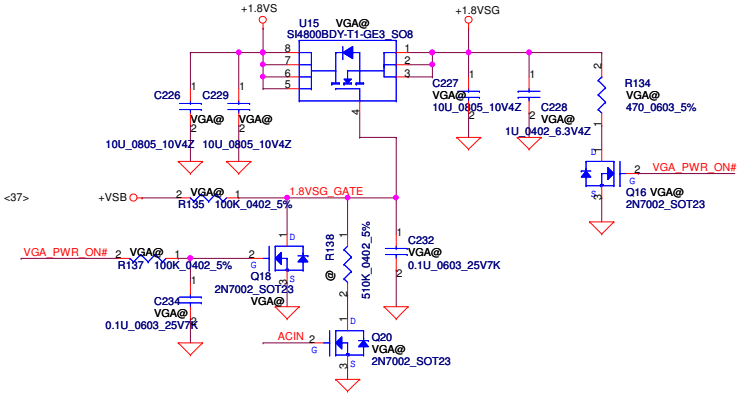
1.05VS TO +1.0VSG



+1.5V TO +1.5VSG

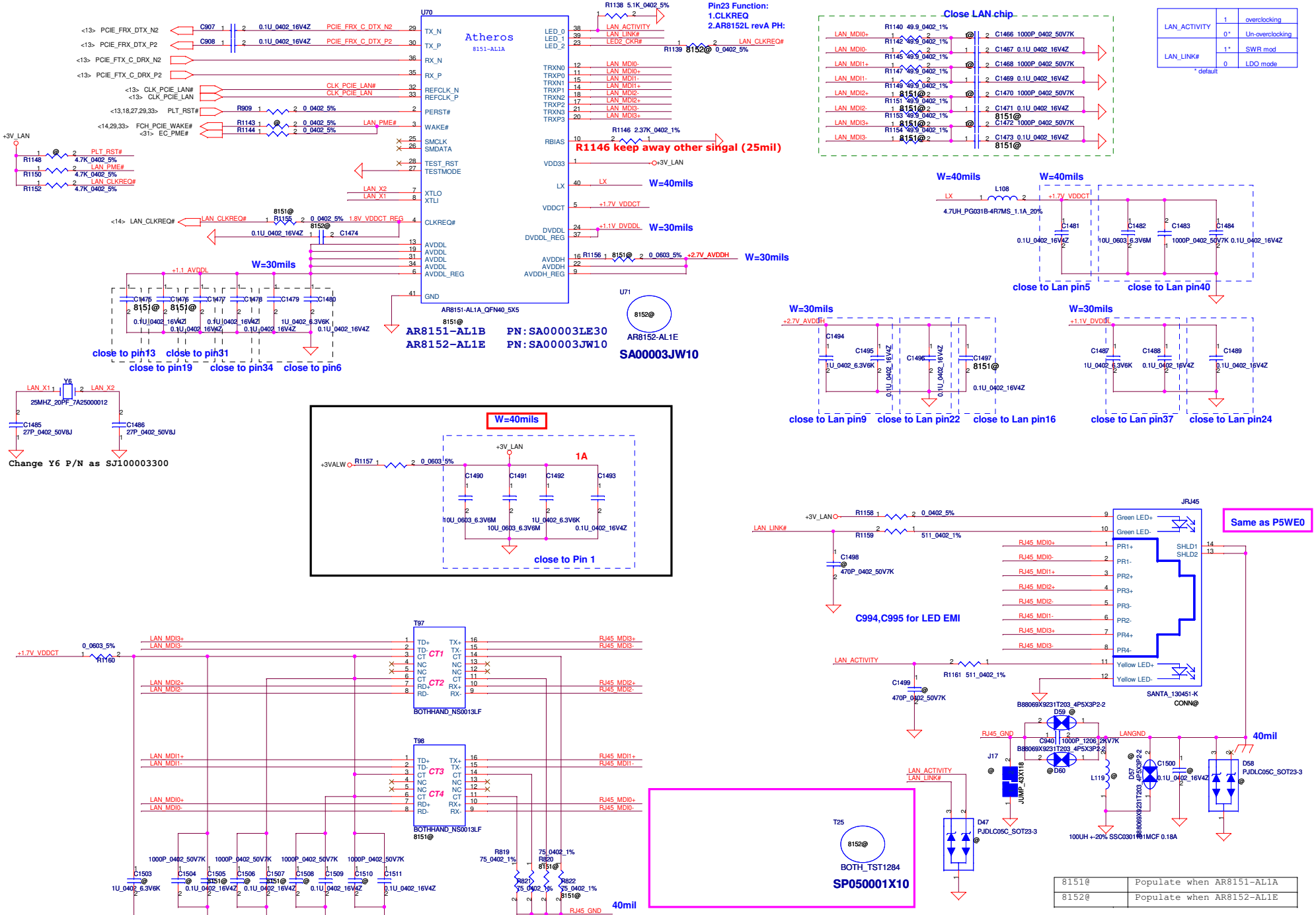


+1.8VS TO +1.8VSG



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.			
Title	RobsonXT-S3 DC Interface		
Size: Custom	Document Number: LA-7091P		Rev: 0.1
Date: Tuesday, December 07, 2010	Sheet 25 of 48		



LAN_ACTIVITY	1	overclocking
	0 *	Un-overclocking
LAN_LINK#	1 *	SWR mod
	0	LDO mode

* default

8151@	Populate when AR8151-AL1A
8152@	Populate when AR8152-AL1E

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/12

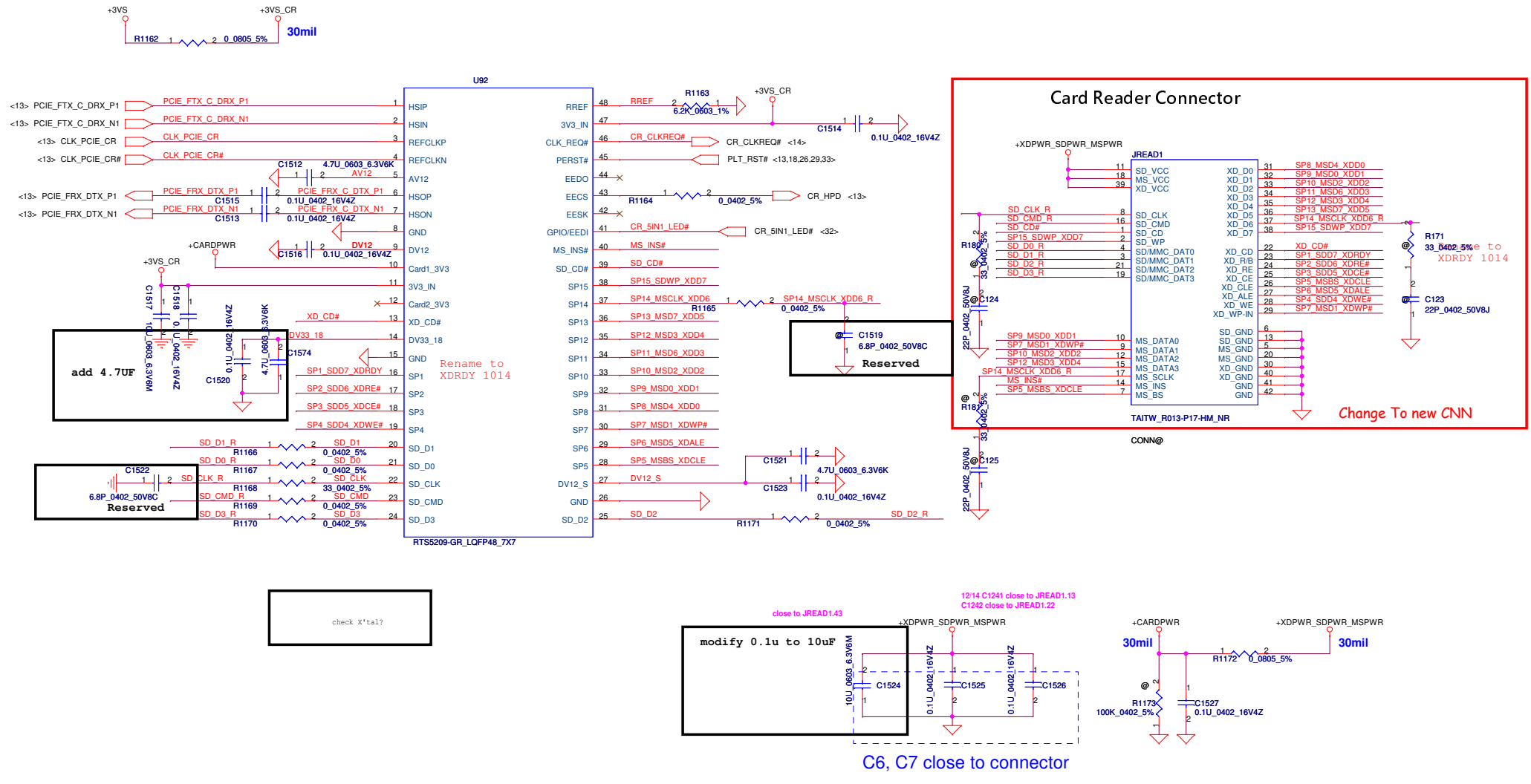
Compal Electronics, Inc.

Title: LAN AR8151 / AR8152

Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 Sheet 26 of 48

RTS5209-GR



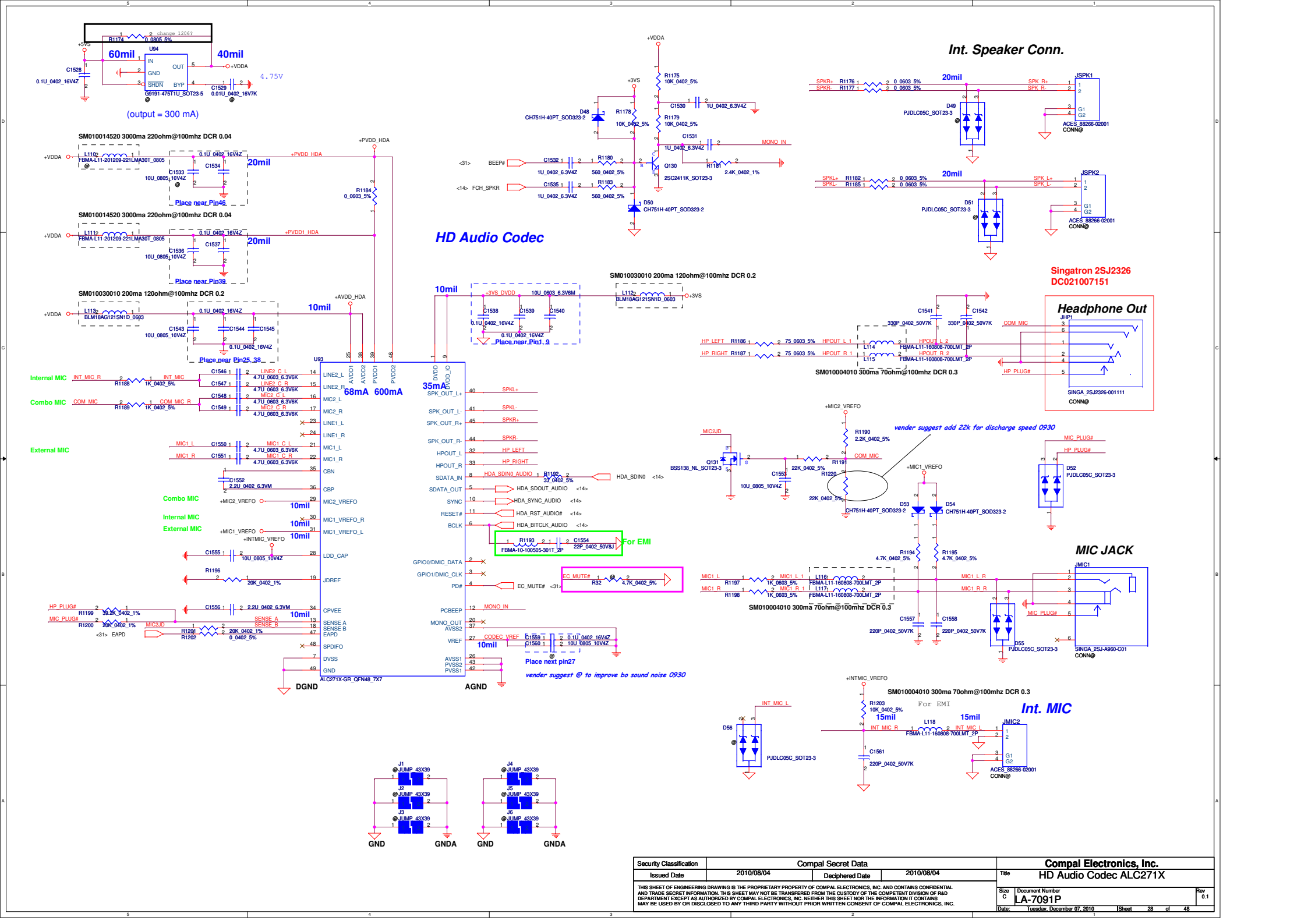
Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/12

Compal Electronics, Inc.

Title: CardReader-RTS5209-GR

Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 Sheet 27 of 48



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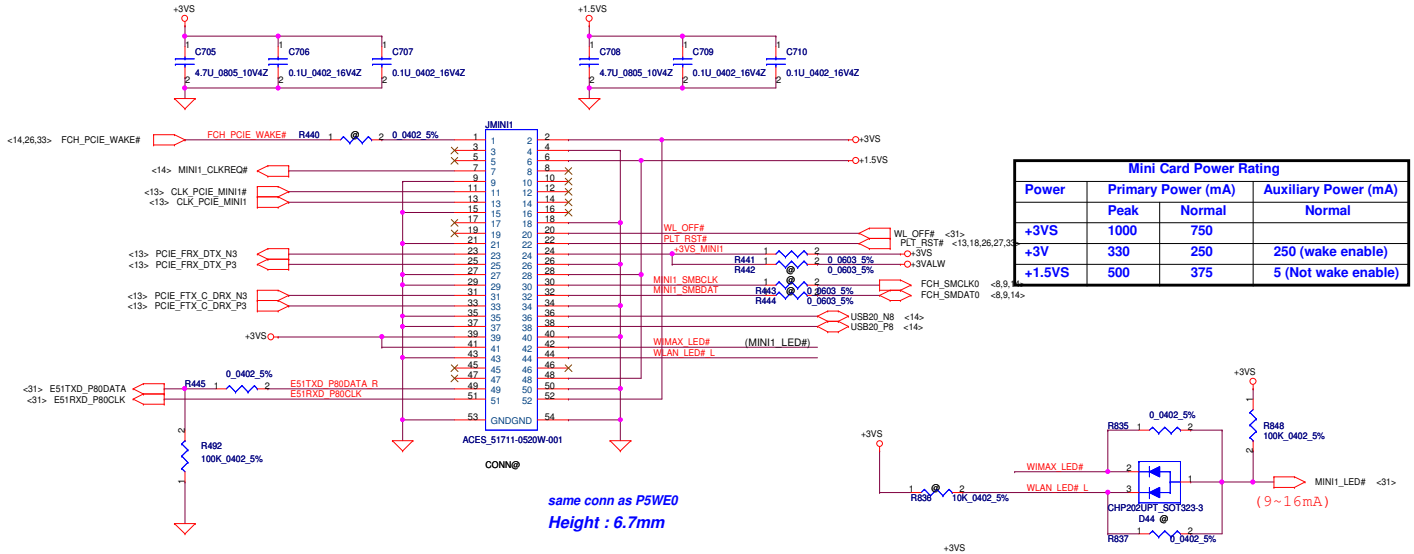
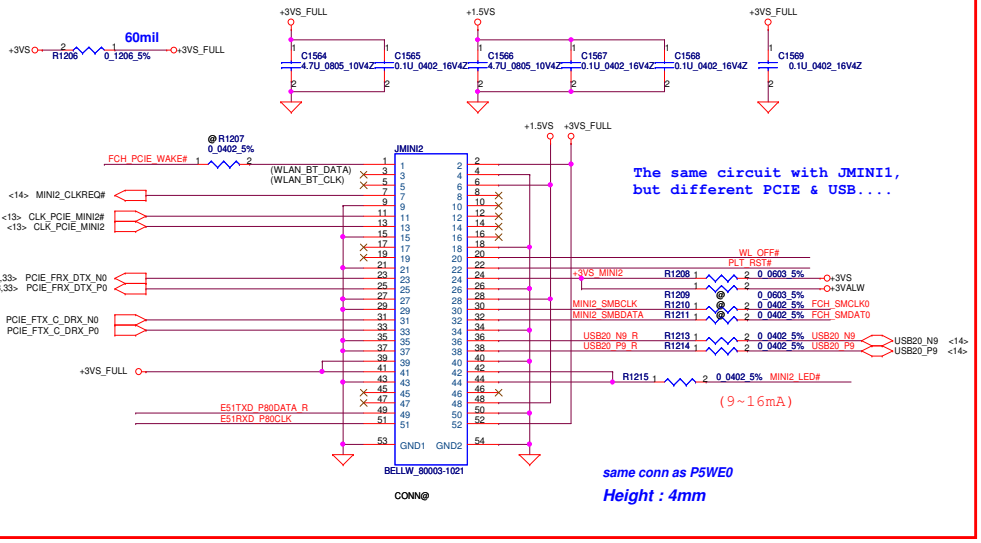
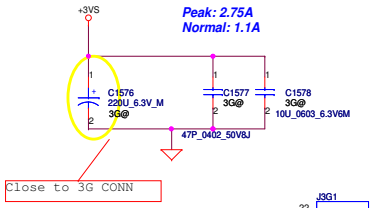
Mini-Express Card for WLAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

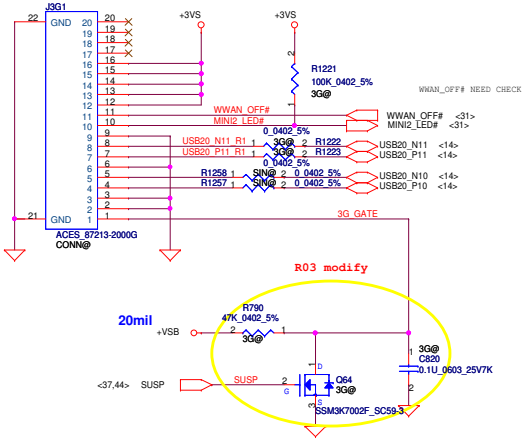
Reserve





For 3G / GPS

To 3G Module Connect



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

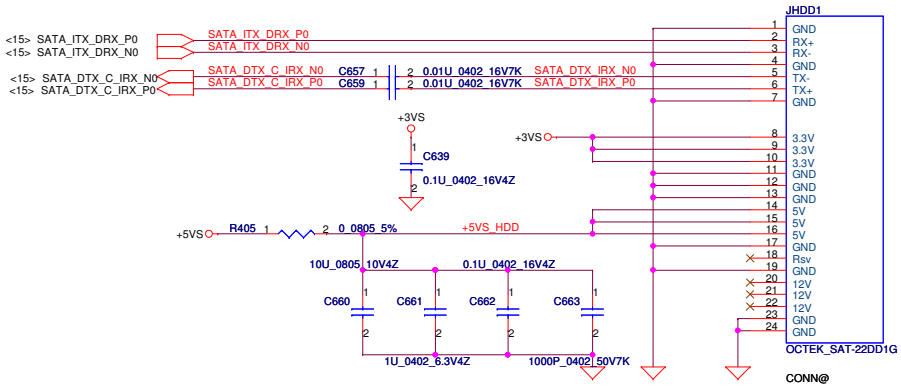
Compal Electronics, Inc.

Title: MINI CARD / CardReader RTS5137

Size	Document Number	Rev
	LA-7091P	0.1

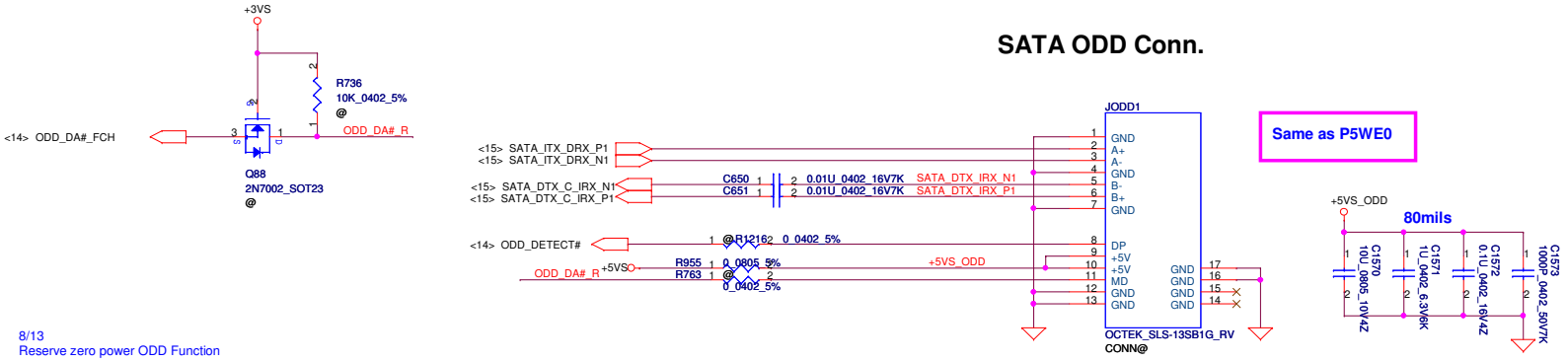
Date: Tuesday, December 07, 2010 Sheet 29 of 48

SATA HDD Conn.

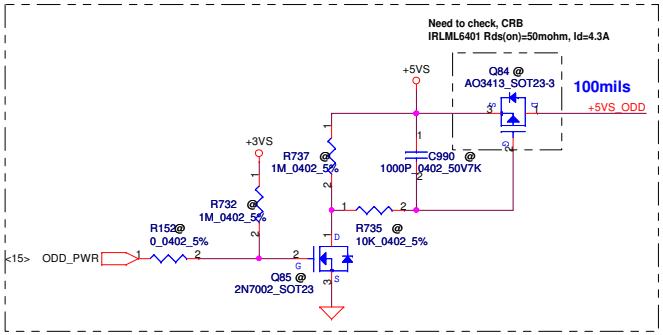


SATA ODD FFC Conn.

SATA ODD Conn.

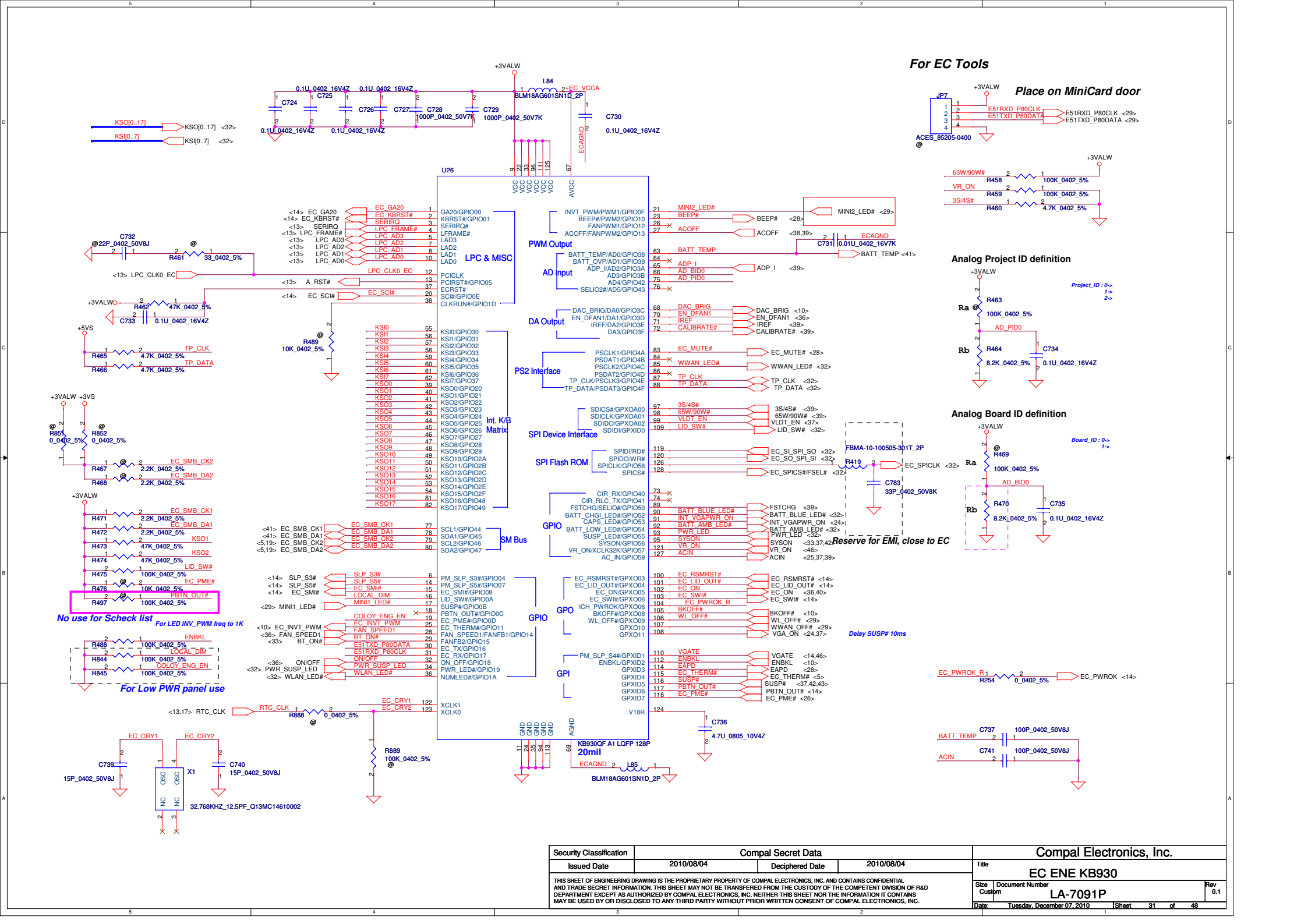


8/13
Reserve zero power ODD Function



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.			
Title: HDD & ODD CONN			
Size: Custom	Document Number: LA-7091P		Rev: 0.1
Date: Tuesday, December 07, 2010	Sheet 30 of 48		


For EC Tools
Place on MiniCard door
JP7
ACES_85205-0400
E51RXD_P80CLK
E51TXD_P80DATA
U26
KB930QF A1 LQFP 128P
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
Analog Project ID definition
Analog Board ID definition
Project_ID : 0->
1->
2->
Board_ID : 0->
1->
FBMA-10-100505-301T_2P
Reserve for EMI, close to EC
No use for Scheck list
For LED INV_PWM freq to 1K
For Low PWR panel use
Delay SUSP# 10ms
X1
32.768KHZ_12.5PF_Q13MC14610002
BLM18AG601SN1D_2P
Security Classification
Compal Secret Data
Issued Date
2010/08/04
Deciphered Date
2010/08/04
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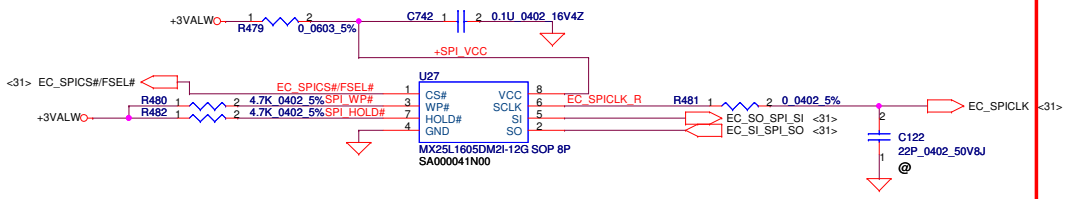
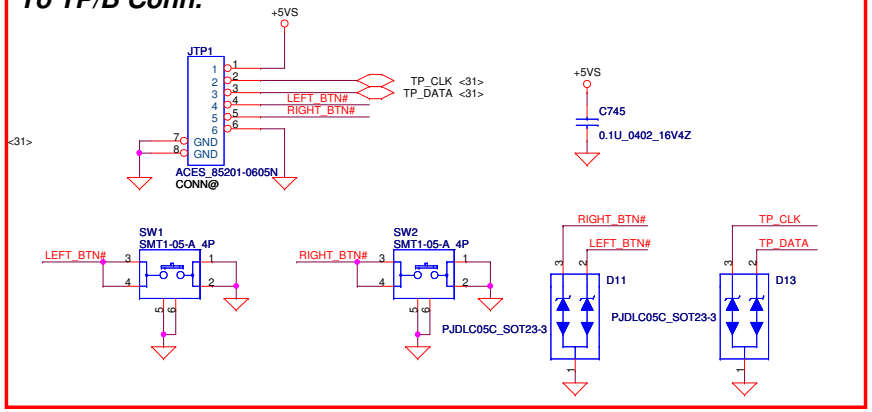
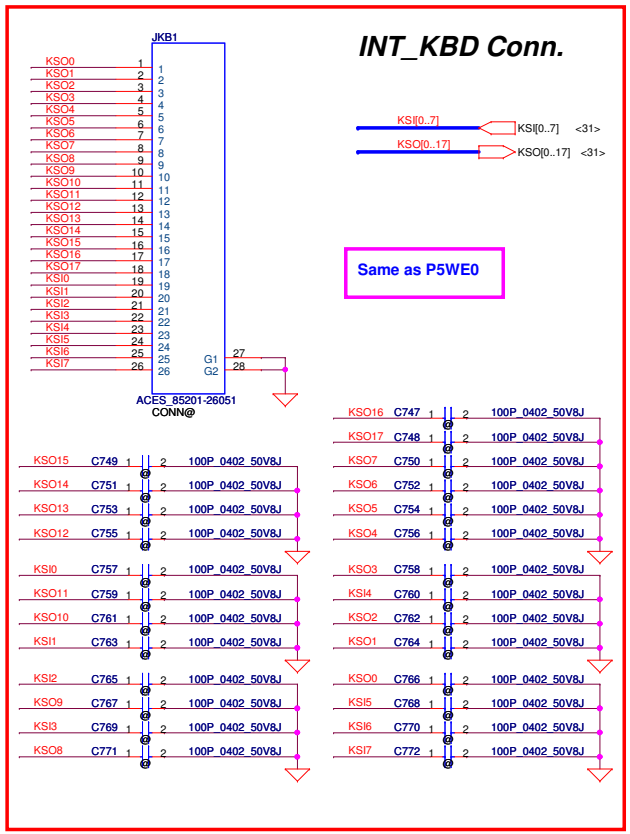
Compal Electronics, Inc.
Title
EC ENE KB930
Size
Custom
Document Number
LA-7091P
Rev
0.1
Date:
Tuesday, December 07, 2010
Sheet
31
of
48

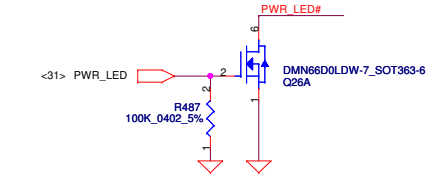


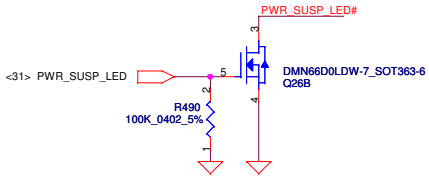
To TP/B Conn.

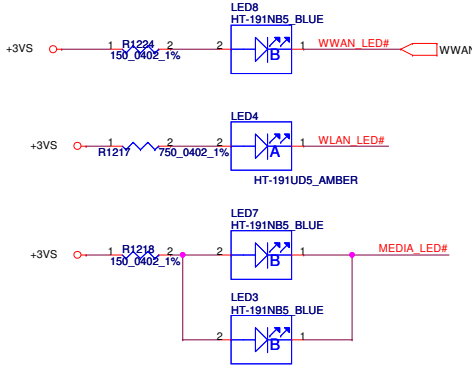


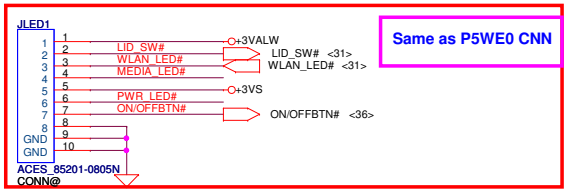
INT_KBD Conn.

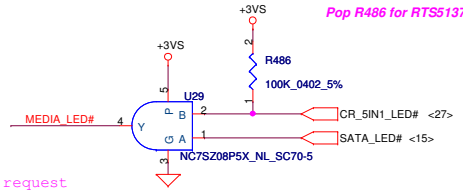


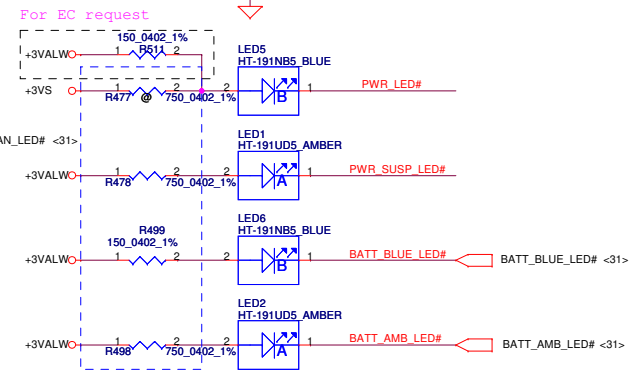








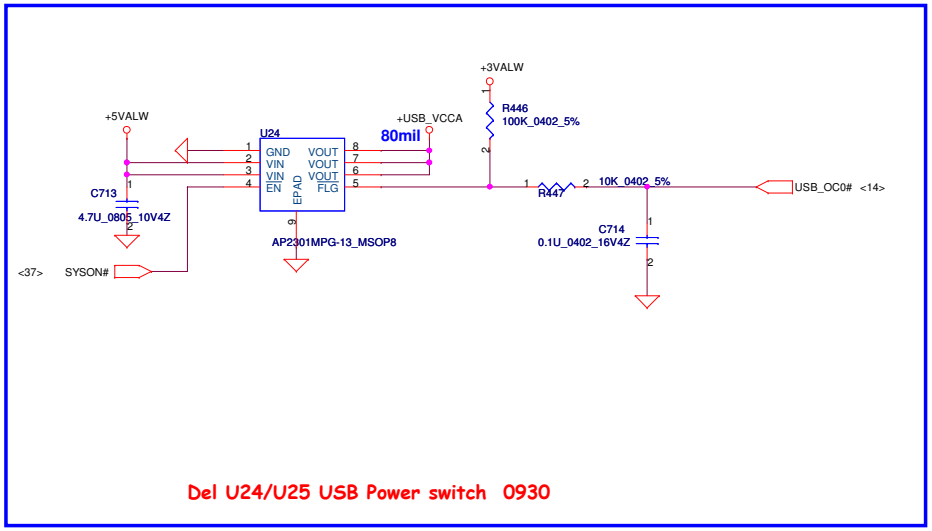


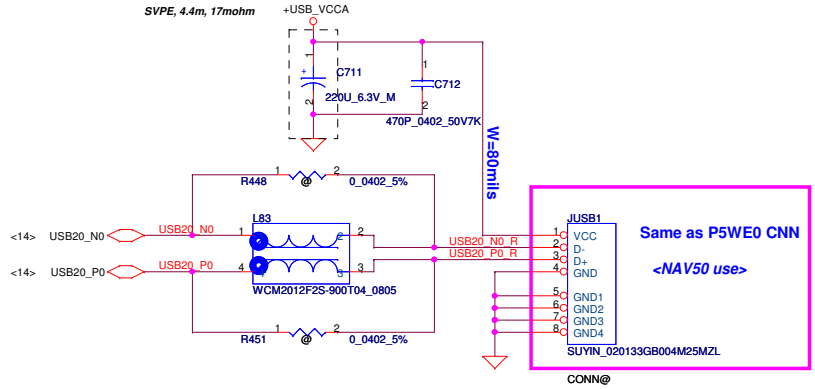


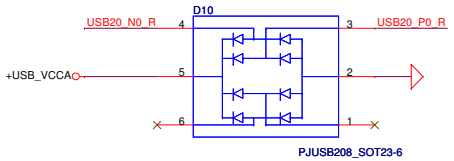
For PEW76/86/96 LED light,
R477, R499 change as 750 ohm
R478 change as 3.01k ohm
R498 change as 3.3k ohm

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

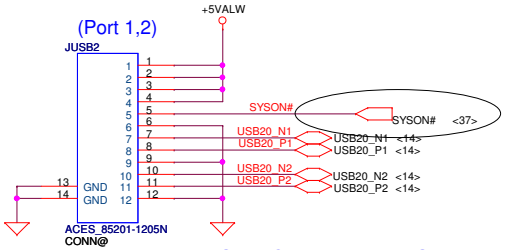
Compal Electronics, Inc.	
Title	KB/TP/LED/SPI ROM/PWRb
Size: Custom	Document Number: LA-7091P
Rev	0.1
Date: Tuesday, December 07, 2010	Sheet 32 of 48





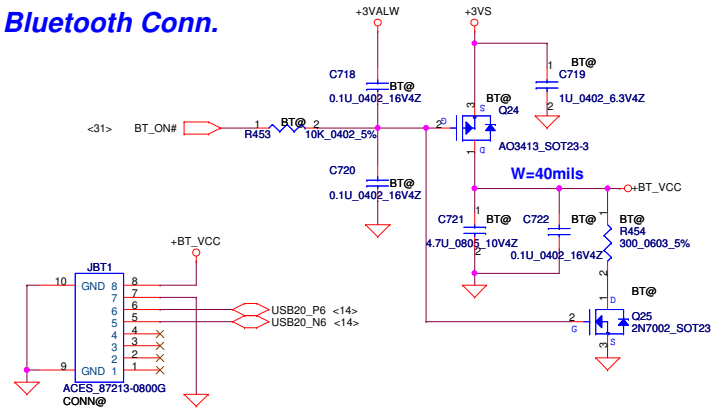


ESD Change P/N SC300000B00 For DVT



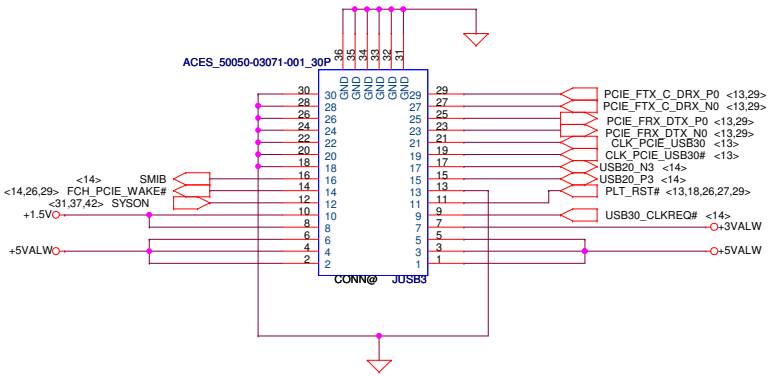
<NAL00 use> To USB/B Connector(for LS-6904P USB2.0 function of USB3.0/20 daughter board)

Bluetooth Conn.



<NAL00 use>

USB3.0 Conn.



OD output

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

Compal Electronics, Inc.

Title: USB/BT/USBsub

Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 | Sheet 33 of 48

Security Classification	Compal Secret Data		
Issued Date	2010/08/27	Deciphered Date	2011/08/27

Title

USB3.0 PD720200

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, October 19, 2010 Sheet 34 of 48

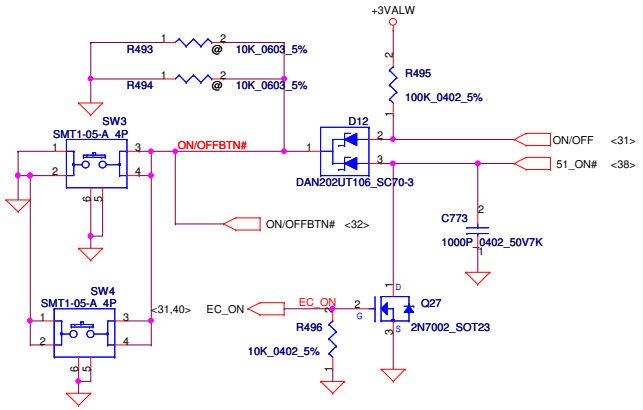
Security Classification	Compal Secret Data		
Issued Date	2010/08/27	Deciphered Date	2011/08/27

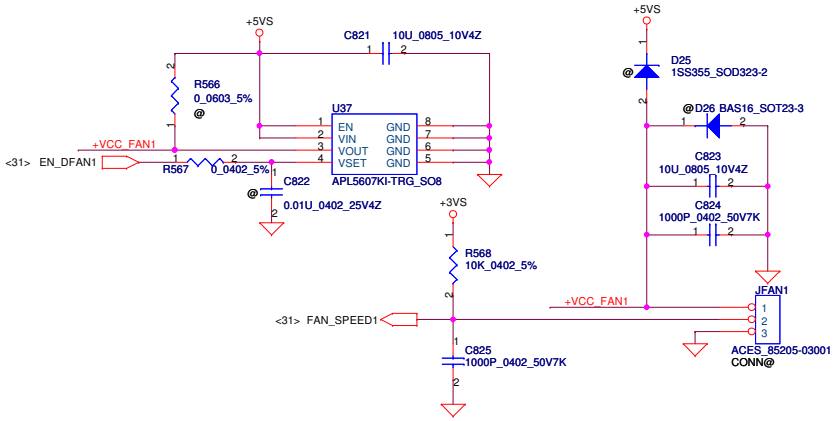
Title

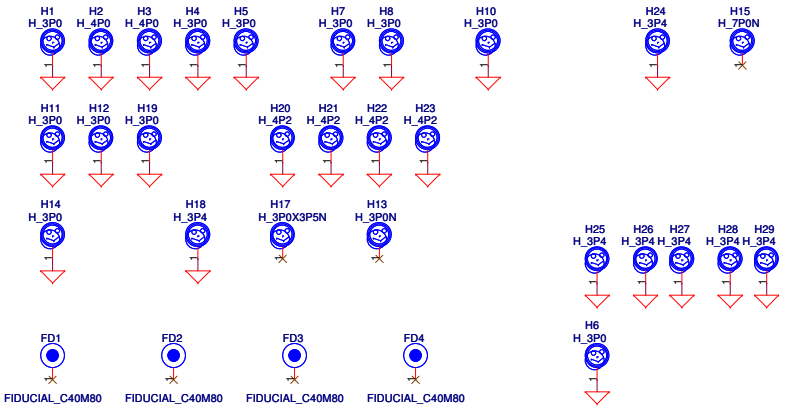
USB3.0 PD720200

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, October 19, 2010 | Sheet 35 of 48







Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

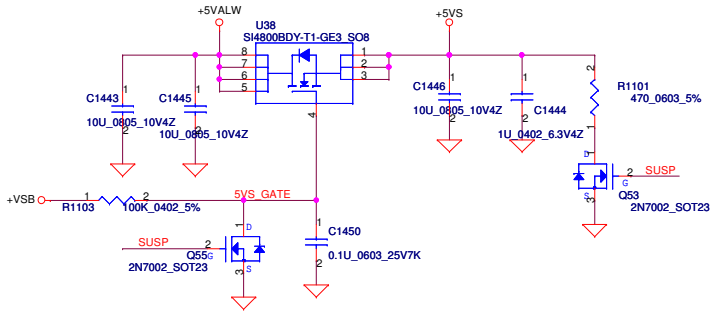
Compal Electronics, Inc.

Title: Other IO/USB (right)

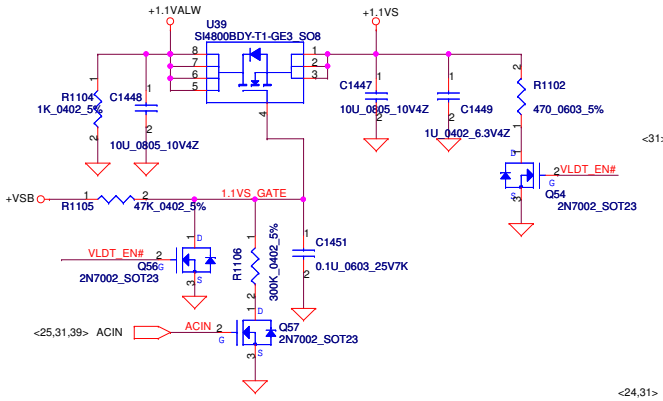
Size	Document Number	Rev
Custom	LA-7091P	0.1

Date: Tuesday, December 07, 2010 | Sheet 36 of 48

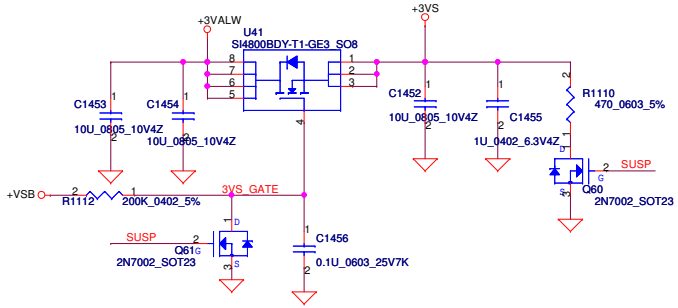
+5VALW TO +5VS

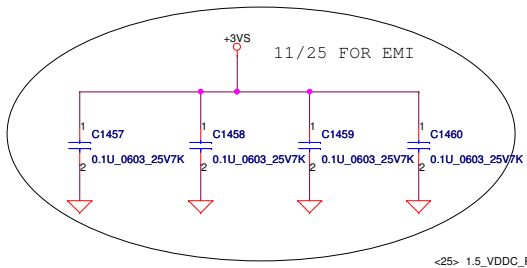


+1.1VALW TO +1.1VS

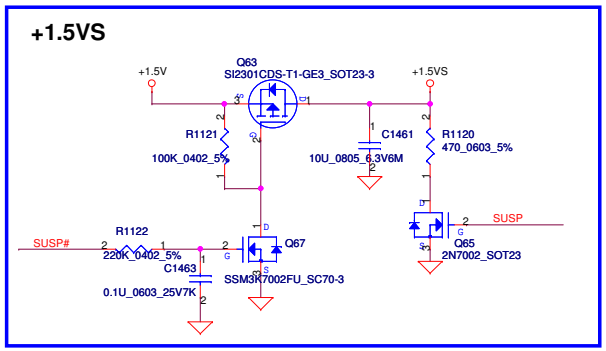


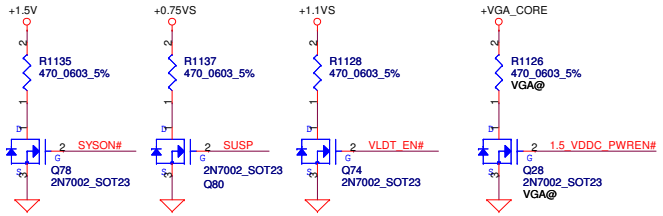
+3VALW TO +3VS

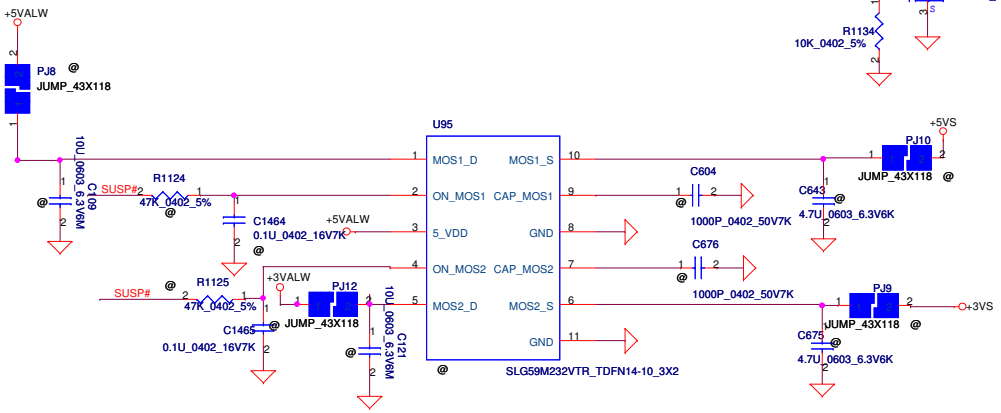


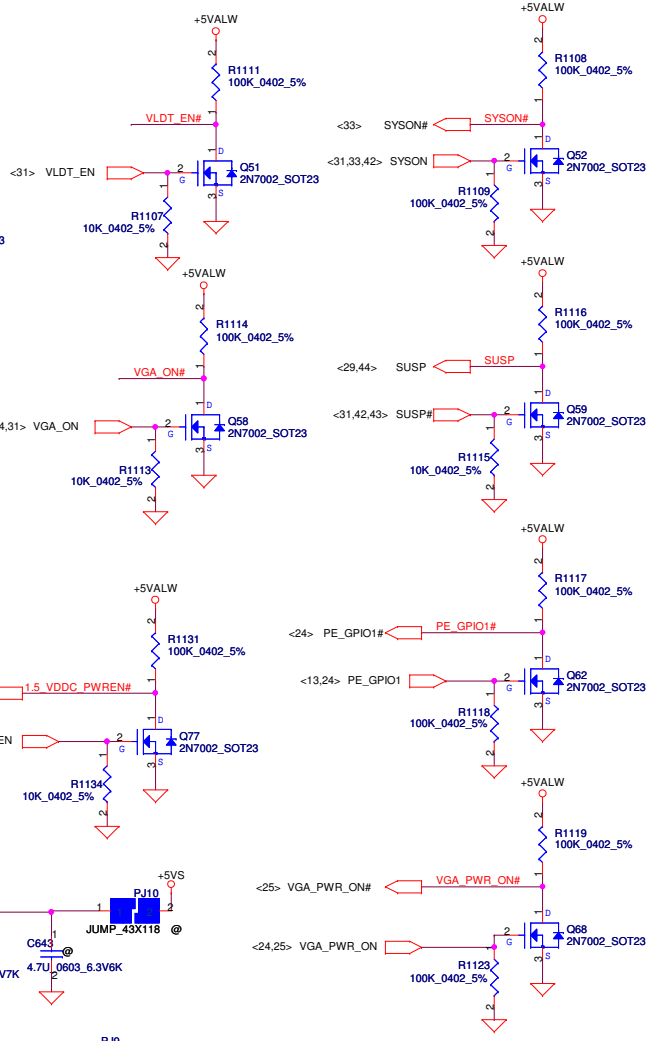


+1.5VS









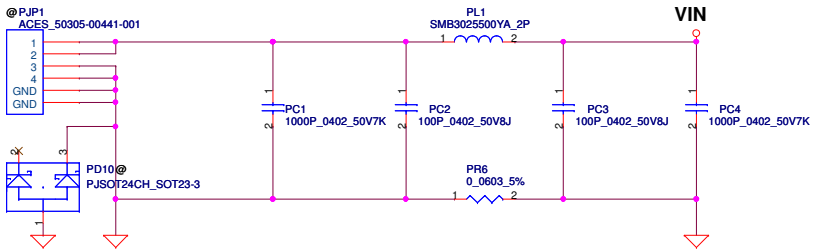
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2010/08/04

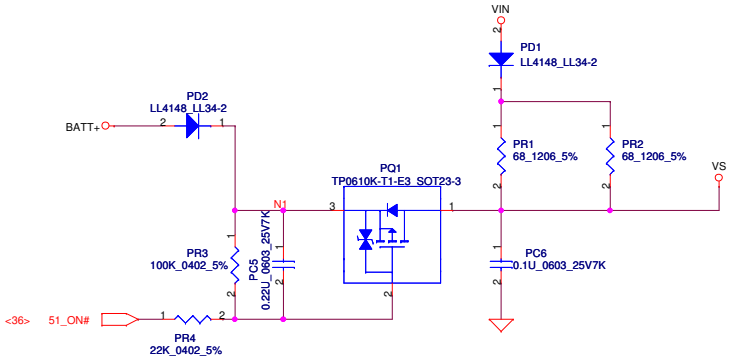
Compal Electronics, Inc.

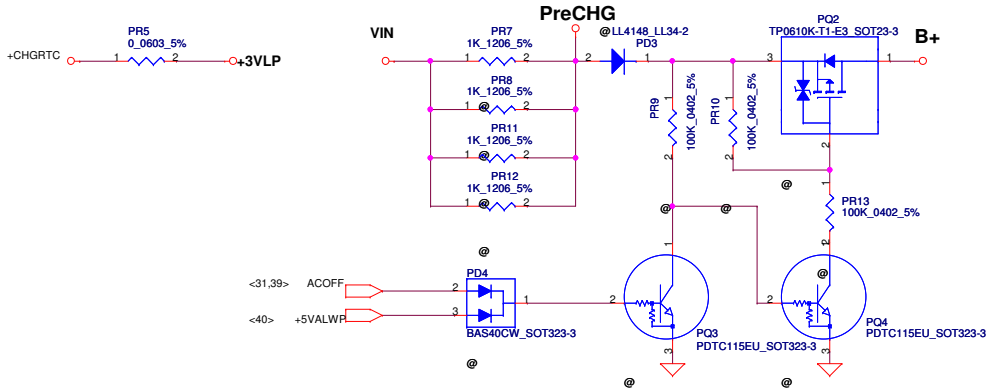
Title: DC Interface

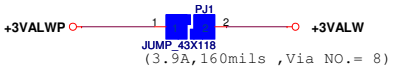
Size: Custom | Document Number: LA-7091P | Rev: 0.1

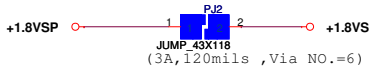
Date: Tuesday, December 07, 2010 | Sheet 37 of 48

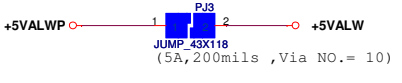


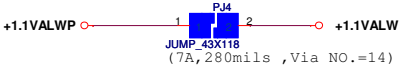


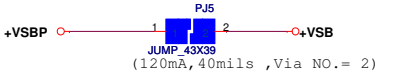


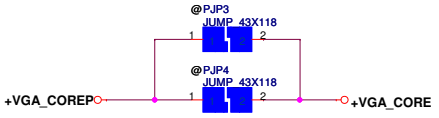


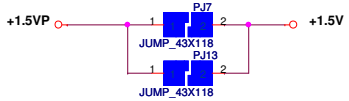


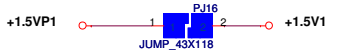












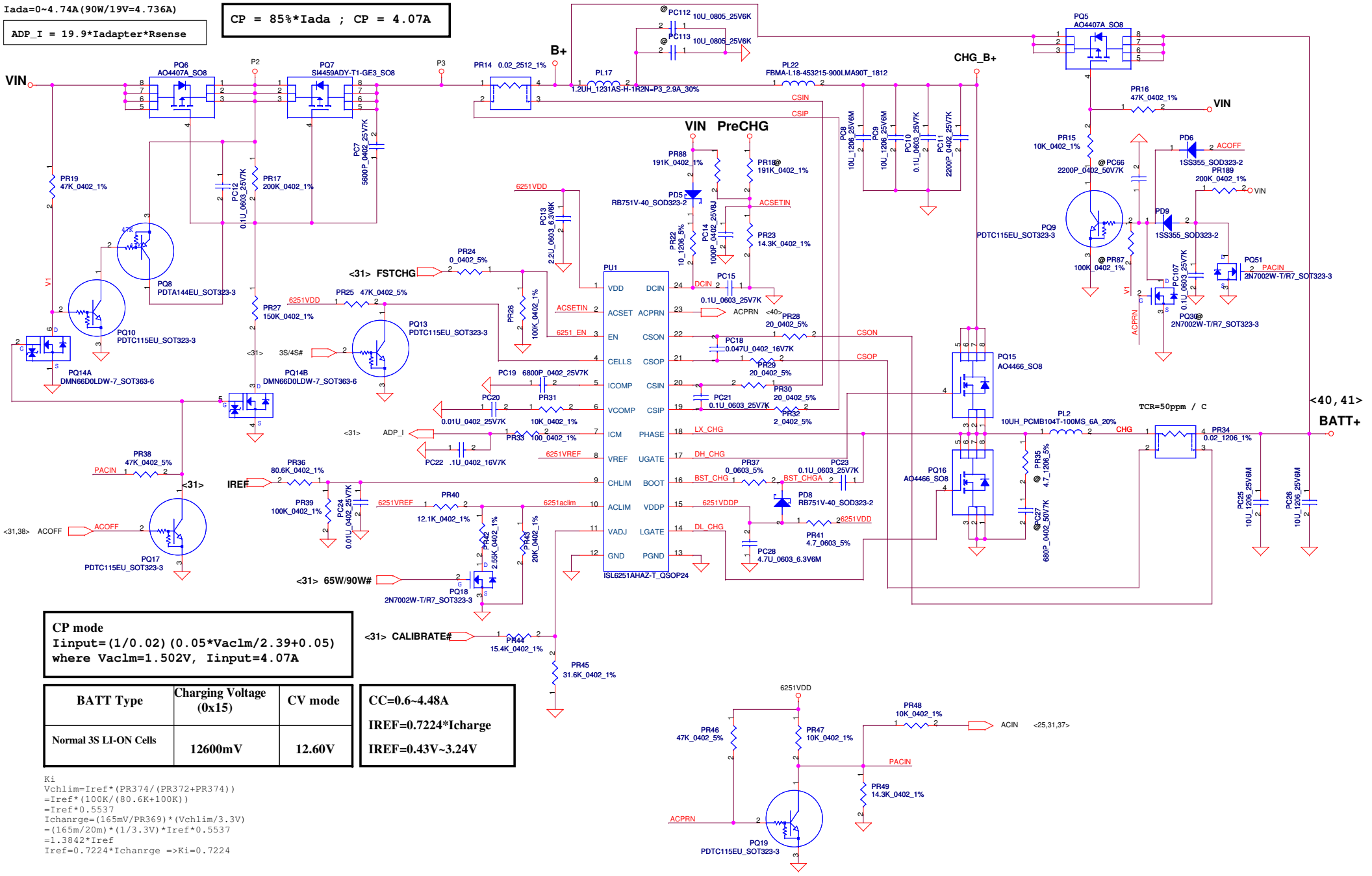
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.			
Title	PWR DCIN / Pre-charge		
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic		Rev: 0.1
Date: Tuesday, December 07, 2010	Sheet 38 of 47		

Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

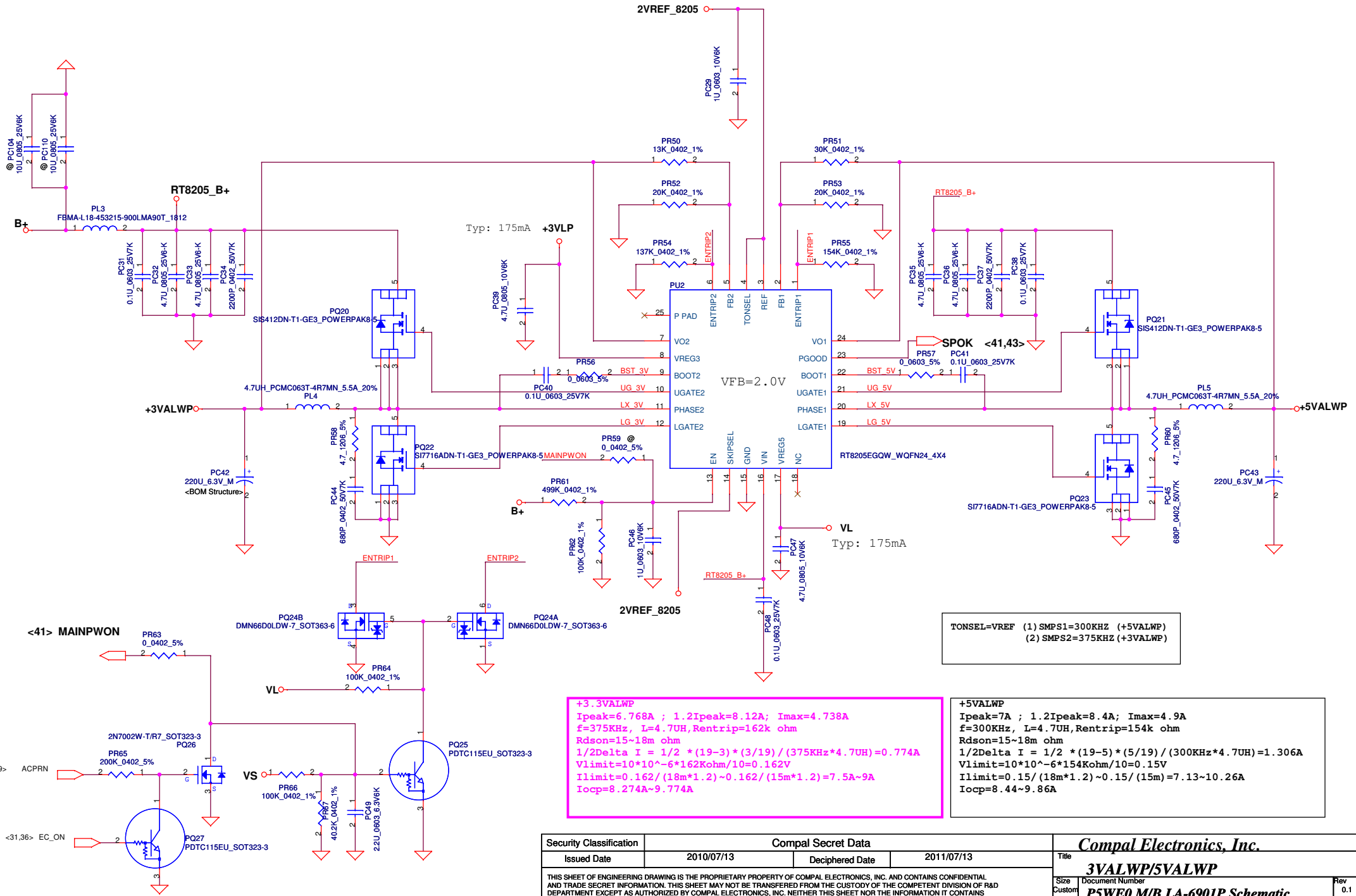
Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Title: Compal Electronics, Inc.
PWR-CHARGER

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Tuesday, December 07, 2010 | Sheet 39 of 47



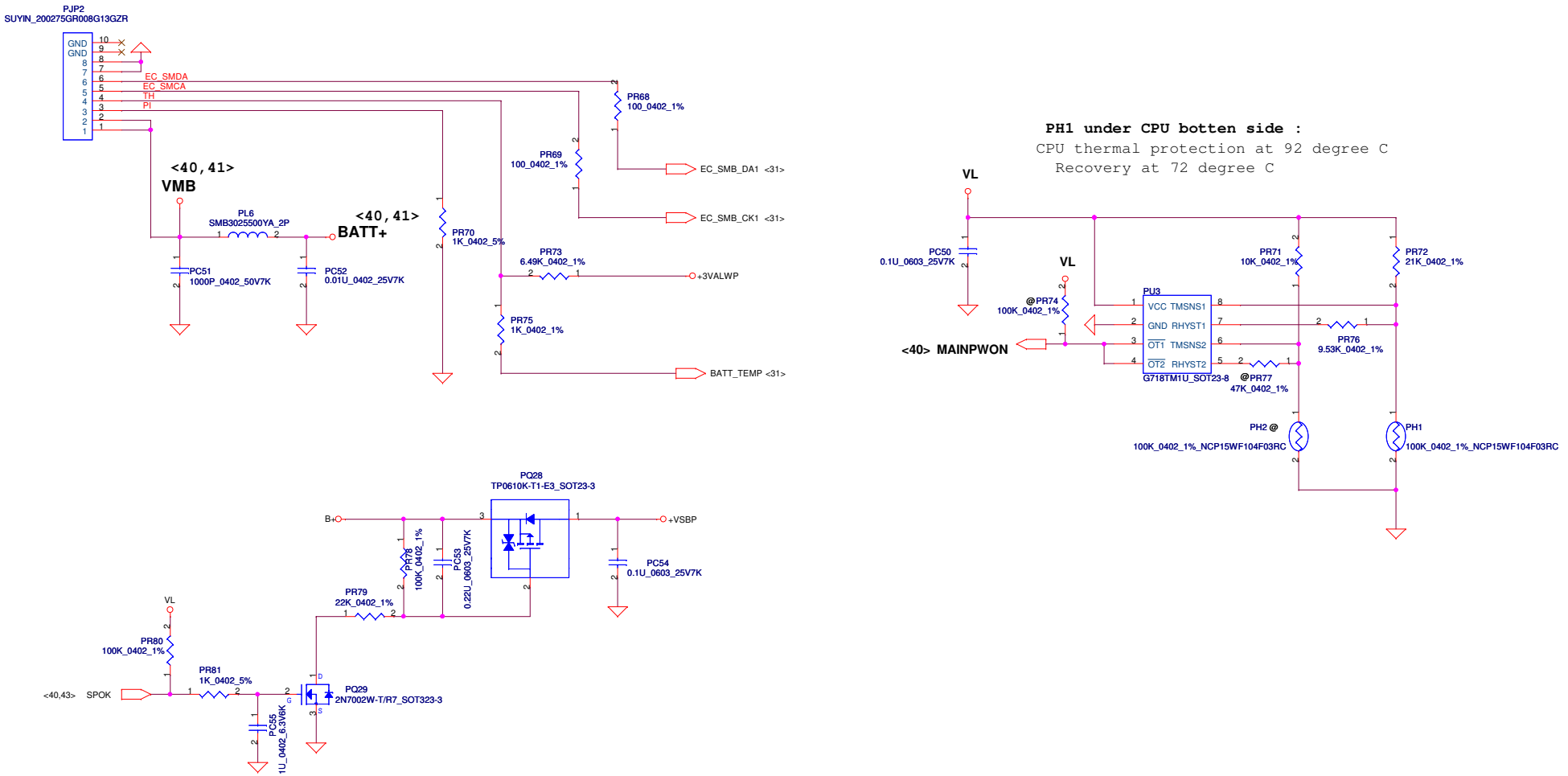
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

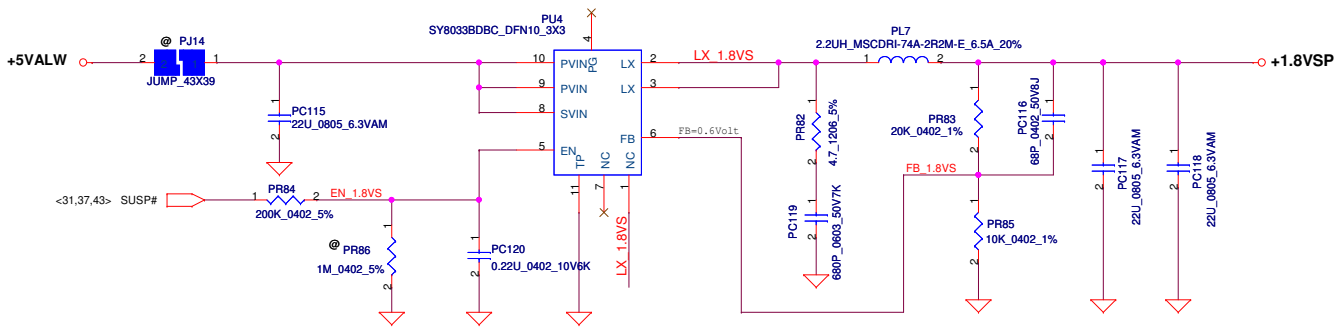
Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

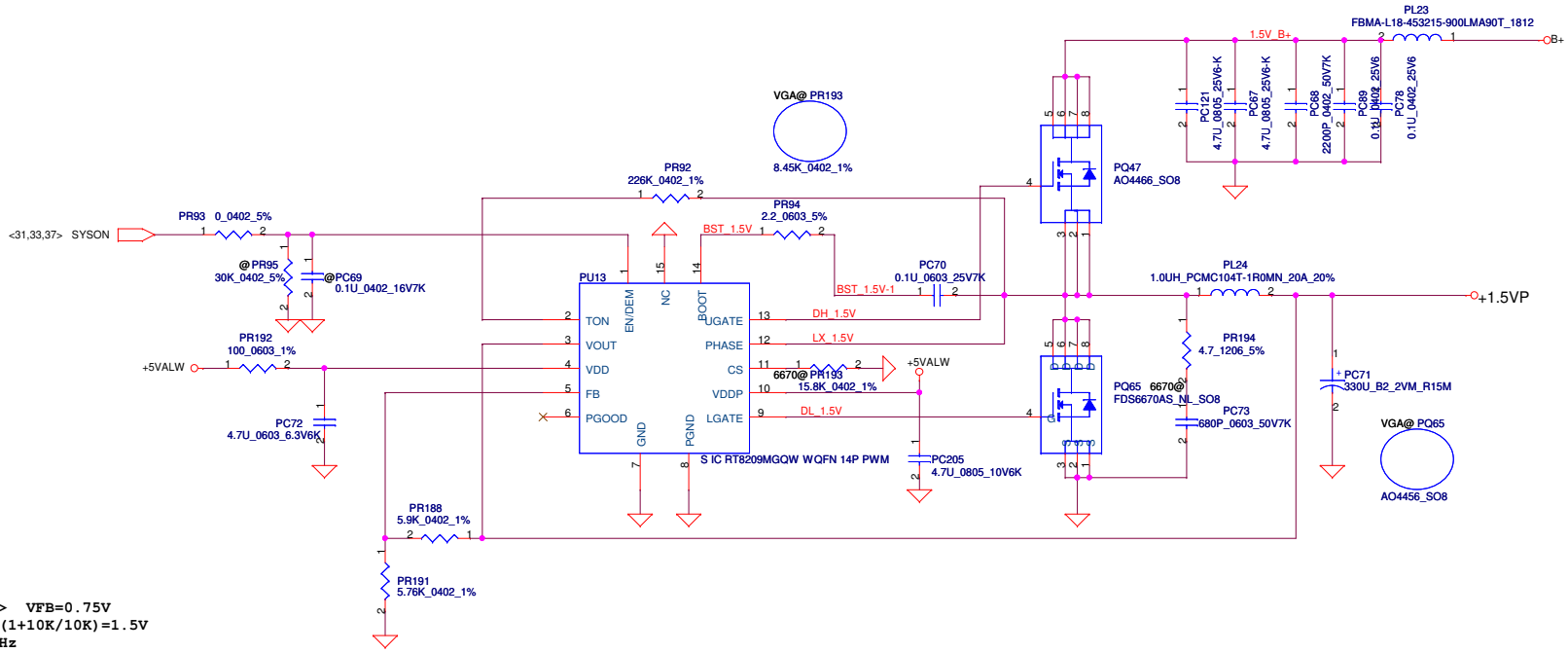
Date: Tuesday, December 07, 2010 | Sheet 40 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic		Rev: 0.1
Date: Tuesday, December 07, 2010	Sheet 41 of 47		





<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+10K/10K)=1.5V
Fsw=280KHz

Cout ESR=17 mohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm
Ipeak=14.4A, Imax=10.08A, Iocp=17.28A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=3.9A
=>1/2Delta I=1.95A
Vtripmax=Iocp*Rdson=16.2*5.6*1.3=0.118V
Rcs=Vtrip/9uA=0.118V/9uA=13.1K
choose Rcs=13K
Iocpmax=((13K*11uA)/0.0045)+1.95A=32A
Iocpmin=((13K*9uA)/(0.0056*1.3))+1.95A=18A
Iocp=18A~32A

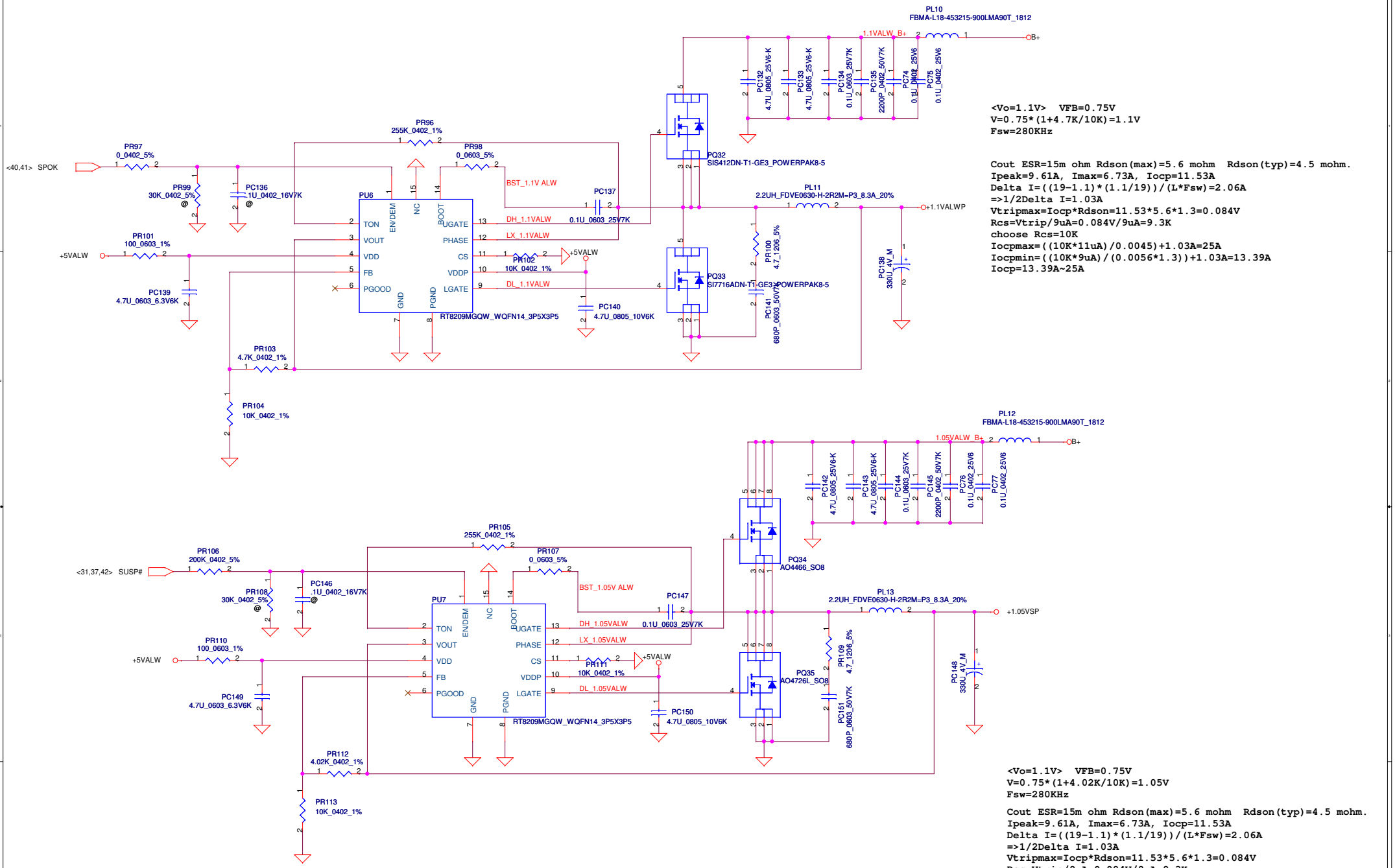
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: 1.8VSP/1.5VP

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, December 07, 2010 | Sheet 42 of 47



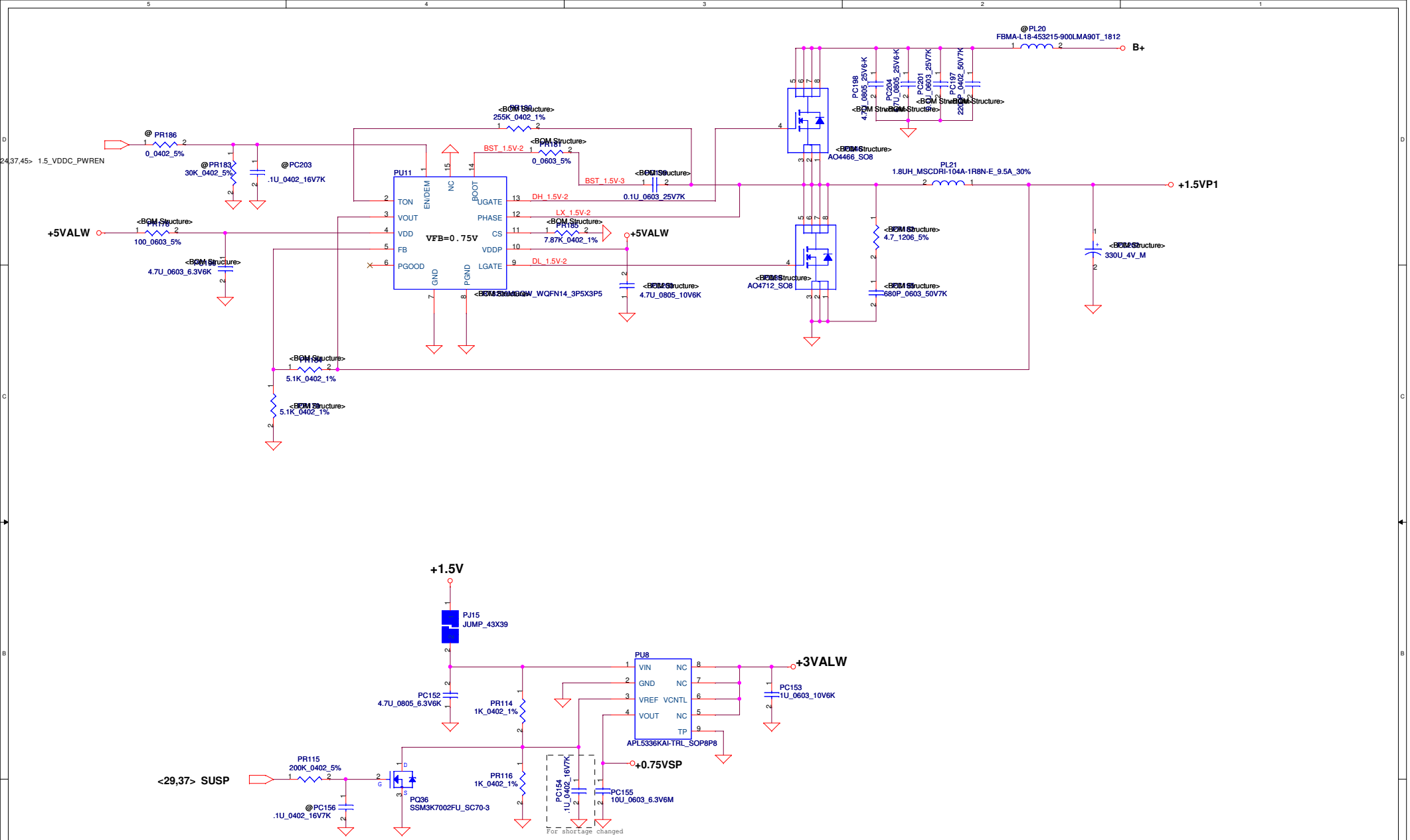
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: 1.1VALWP/1.0VSP

Size: Custom | Document Number | Rev: 0.1

Date: Tuesday, December 07, 2010 | Sheet 43 of 47



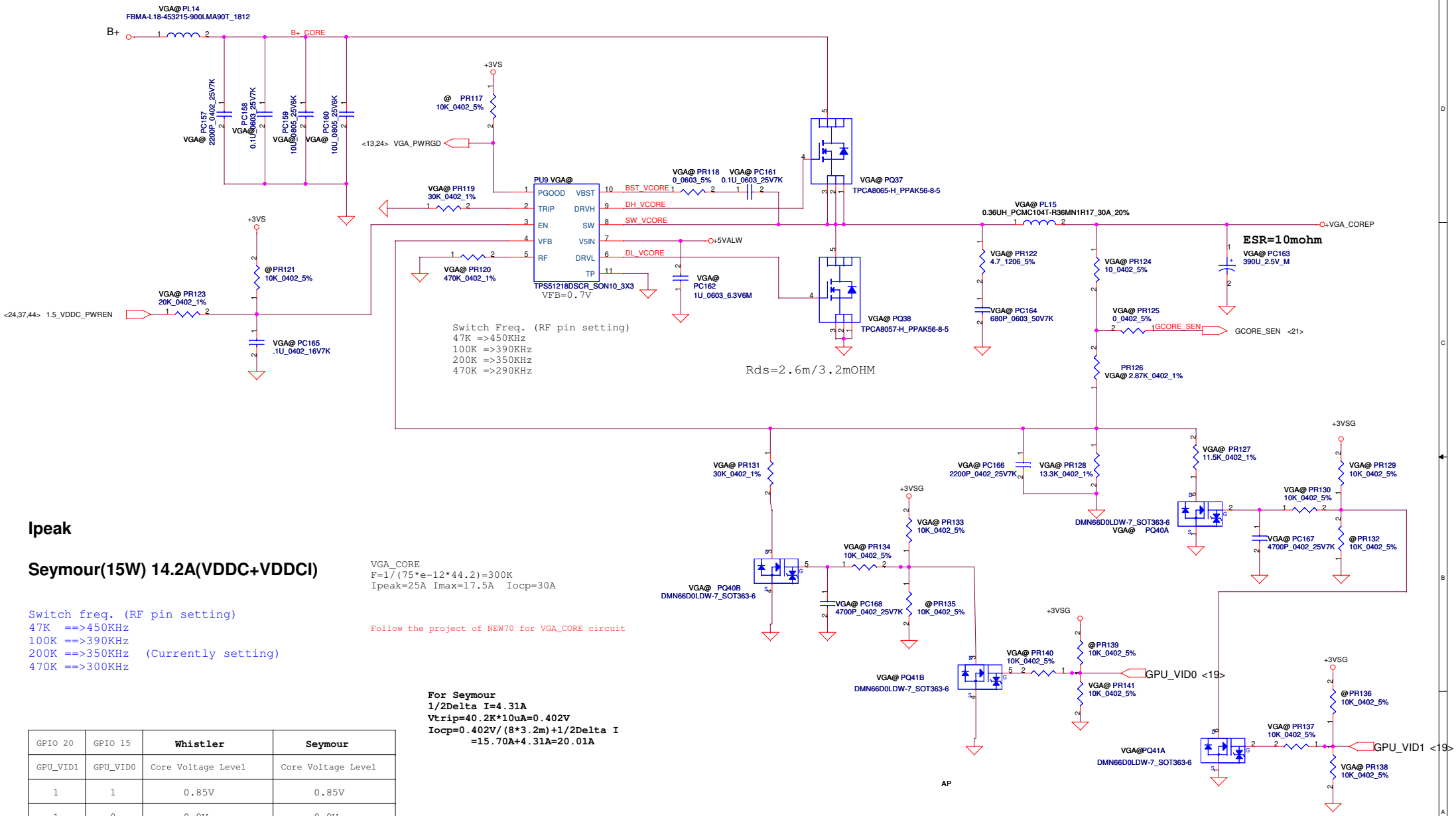
Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: 0.75VSP

Size	Document Number	Rev
		0.3

Date: Tuesday, December 07, 2010 | Sheet 44 of 47



Ipeak

Seymour(15W) 14.2A(VDDC+VDDCI)

Switch freq. (RF pin setting)
47K ==>450KHz
100K ==>390KHz
200K ==>350KHz (Currently setting)
470K ==>300KHz

VGA_CORE
F=1/(75*e-12*44.2)=300K
Ipeak=25A Imax=17.5A Iocp=30A

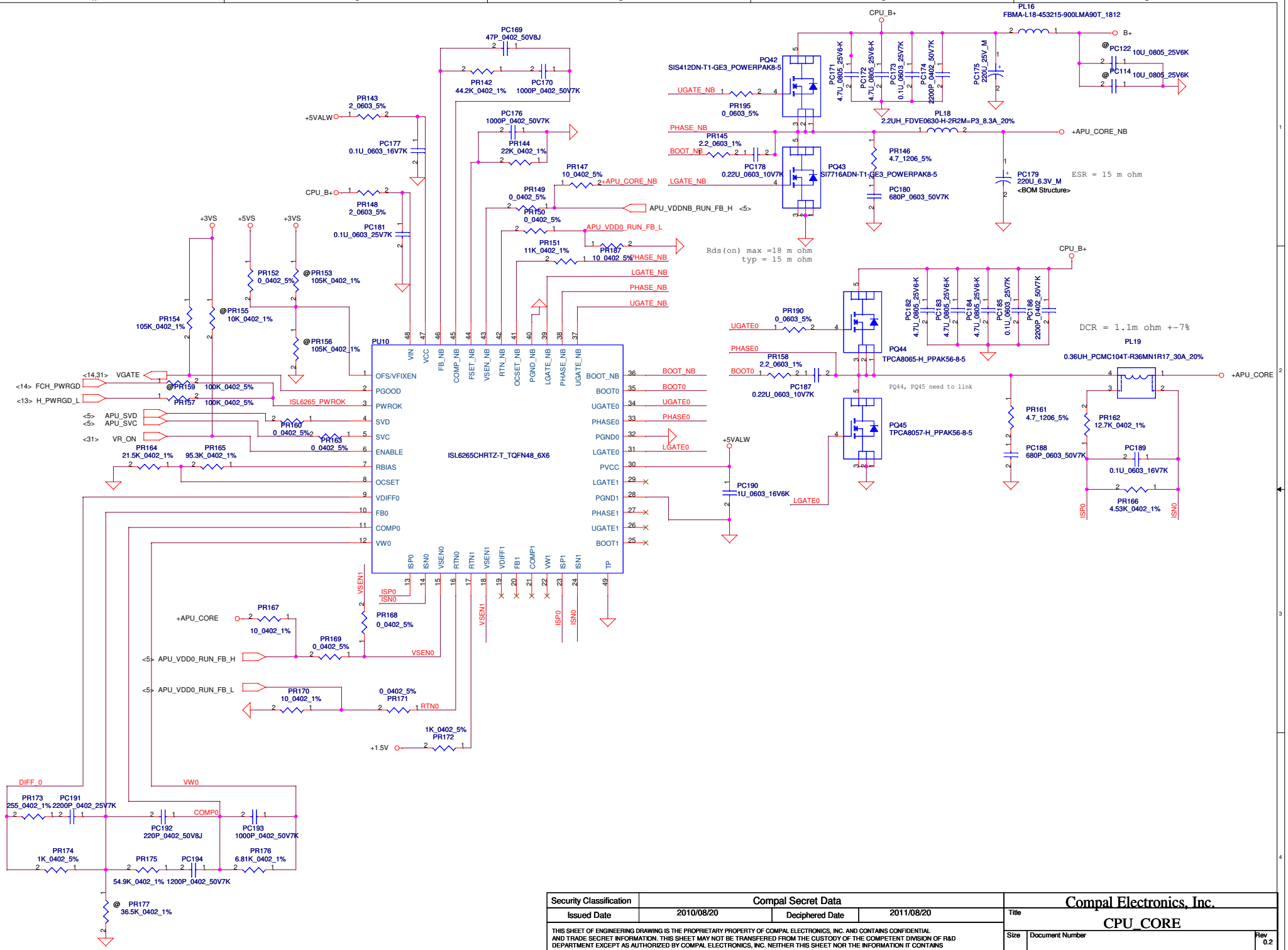
Follow the project of NEW70 for VGA_CORE circuit

For Seymour
1/2Delta I=4.31A
Vtrip=40.2K*10uA=0.402V
Iocp=0.402V/(8*3.2m)+1/2Delta I
=15.70A+4.31A=20.01A

GPIO 20	GPIO 15	Whistler	Seymour
GPU_VID1	GPU_VID0	Core Voltage Level	Core Voltage Level
1	1	0.85V	0.85V
1	0	0.9V	0.9V
0	1	0.95V	1.0V
0	0	1.0V	1.1V

Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

Compal Electronics, Inc.		
Title: +VGA_COREP		
Size: Custom	Document Number: P5WE0	Rev: 0.2
Date: Tuesday, December 07, 2010	Sheet 45 of 47	



Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
		0.2

Date: Tuesday, December 07, 2010 | Sheet 46 of 47

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: PEW96 LA-6552P | Rev: 0.1

Date: Tuesday, December 07, 2010 | Sheet 47 of 47

PHASE	PAGE	Modification list	PURPOSE
0.1	P08	First release	Base on PEW96, change platform (NB,CPU-->APU,SB820-->FCH)
0.1	P10	C669, C671, C1005 change 0603 size P16 C113, C77, C743, C96 change 0603 size	Hight limitation
0.1	P19	C14 change 0603 size P21 C347, C357 change 0603 size P29 C705 change 0603 size	Hight limitation
0.1	P31	C736 change 0603 size P34 C821, C823 change 0603 size P35 C1443, C1445 change 0603 size	Hight limitation
0.1	P33	C711 Change as SF000003I00	Material shortage
0.1	P35	R1122 change as 200k ohm, C1463 change as 0.1UF	Adjust sequence

Change footprint
20100812 : For cost down purpose to change parts

Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

Compal Electronics, Inc.

Title: HW-PIR

Size: B | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 0.2

Date: Tuesday, October 19, 2010 | Sheet 48 of 48