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# Compal confidential

## Schematics Document

## Mobile Yonah uFCPGA with Intel Calistoga_GM/PM+ICH7-M core logic

**2005-12-15**

**REV:1.0**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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Title: *Cover Sheet*

Size: Custom | Document Number: *LA-2841* | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 1 of 60

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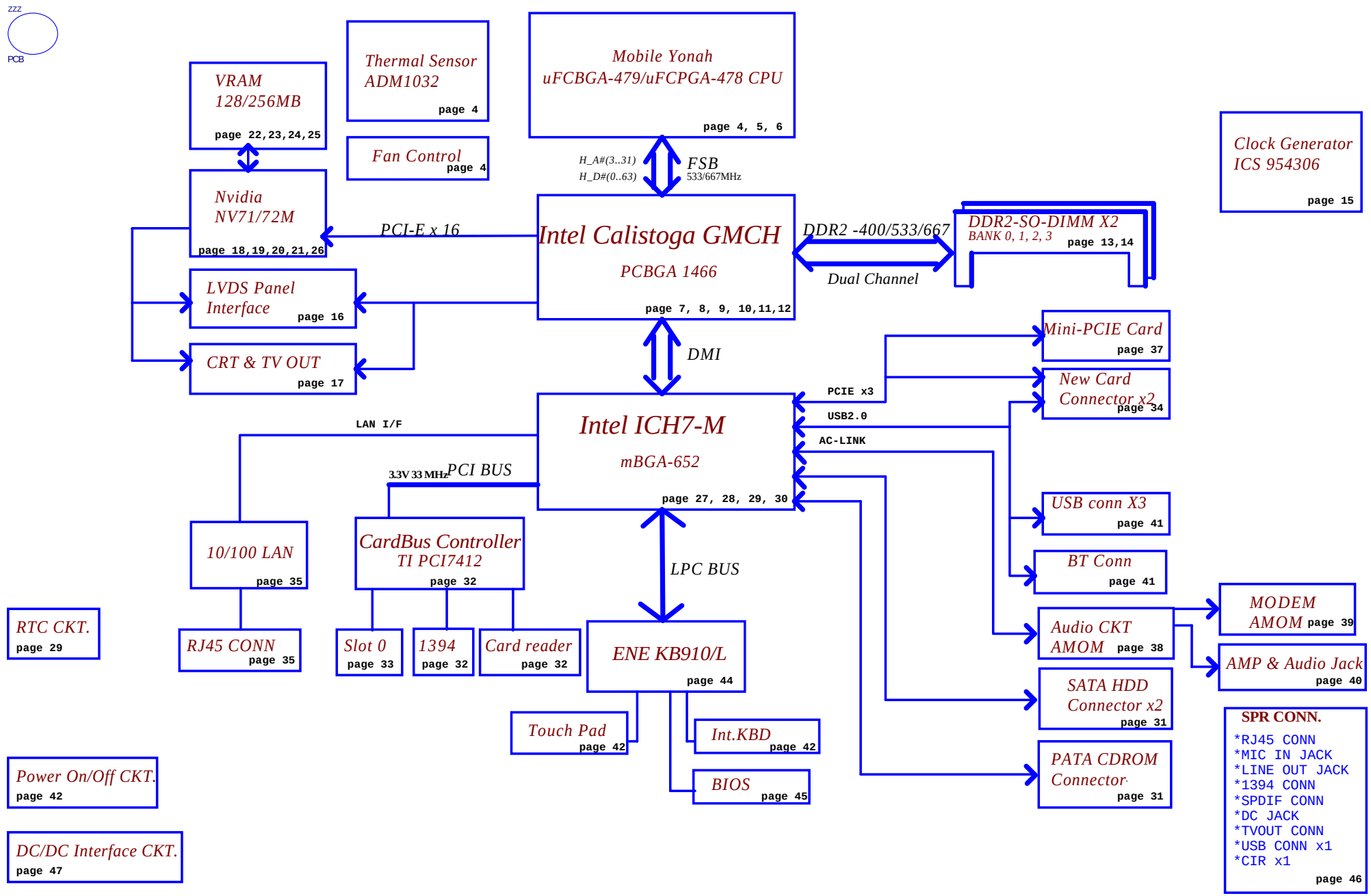
**File Name : LA-2841**

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Title: **Block Diagram**

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## Voltage Rails

| power plane / State | +B<br>LDO3<br>LDO5 | +5VALW<br>+3VALW | +1.8V<br>+5V | +5VS<br>+3VS<br>+2.5VS<br>+1.8VS<br>+1.5VS<br>+1.2VS<br>+VGA_CORE<br>+0.9VS<br>+CPU_CORE<br>+VCCP |
|---|---|---|---|---|
| S0 | O | O | O | O |
| S1 | O | O | O | O |
| S3 | O | O | O | X |
| S5 S4/AC | O | O | X | X |
| S5 S4/ Battery only | O | X | X | X |
| S5 S4/AC & Battery don't exist | X | X | X | X |

O MEANS ON
X MEANS OFF

## PCI Devices

| EXTERNAL | IDSEL# | REQ/GNT# | PIRQ |
|---|---|---|---|
| CARD BUS & 1394 | AD22 | 2 | C,D,E,G |

## Load BOM check item

1.U31 GM/PM/GML part number
2.U6 ICH7 part number
3.VRAM part number and Page26 RAM_CFG[0:3]/PCI_DEVID[0:3] modify check
4.For NV73 R510/R75/R533/R168 change to 499ohm
5.U33 NV7x part number

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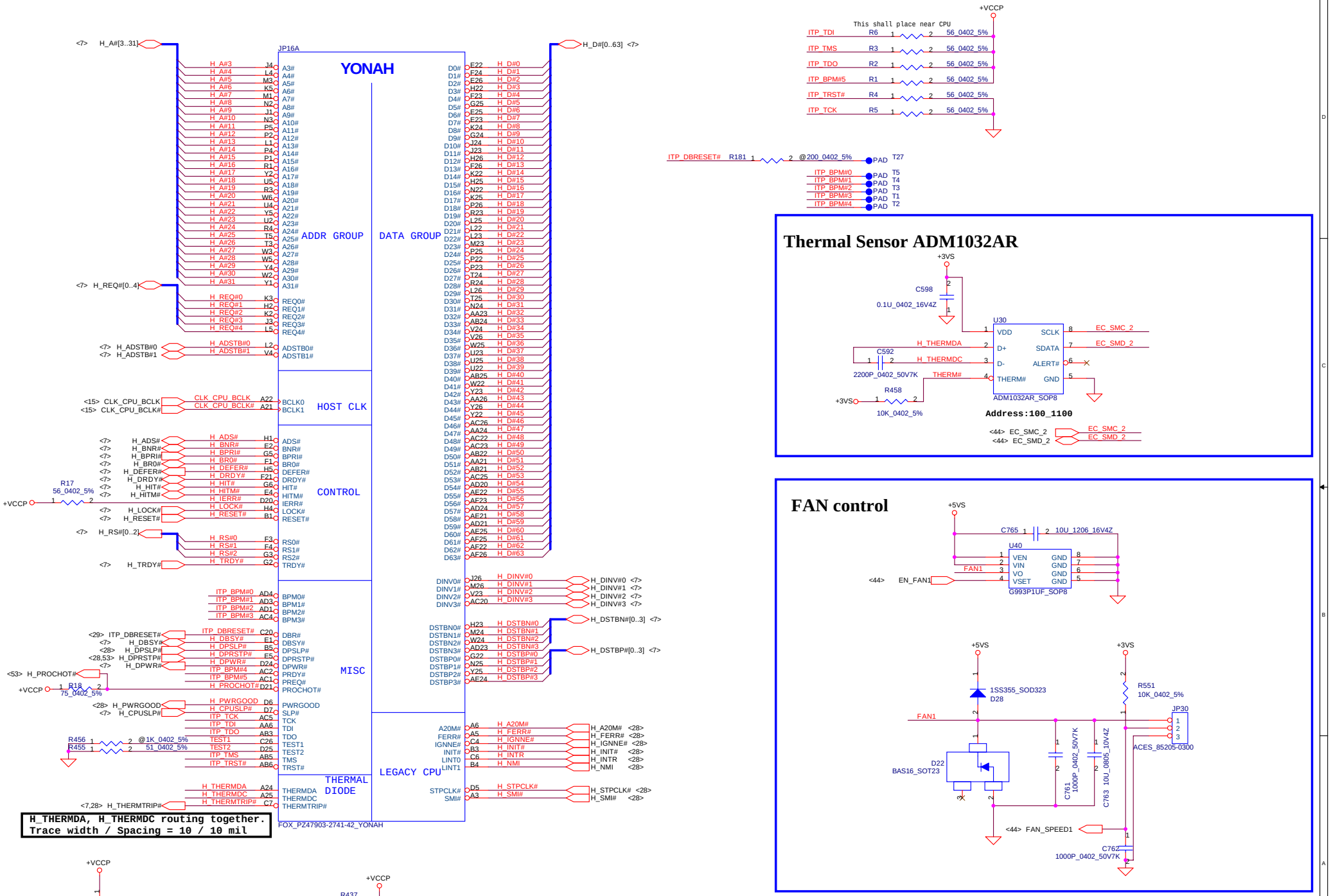


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Title: **Yonah CPU in mFCPGA479**

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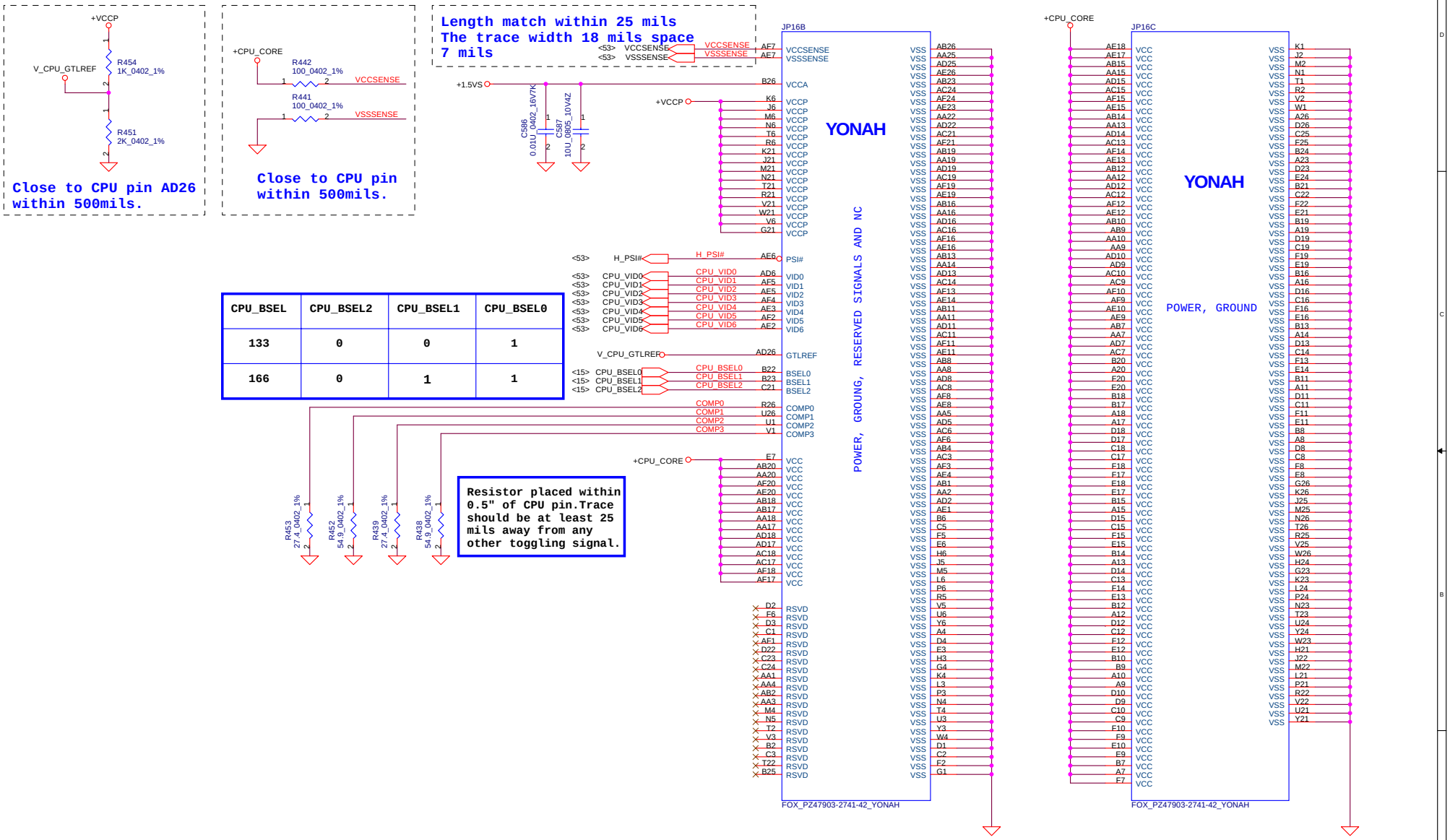


| CPU_BSEL | CPU_BSEL2 | CPU_BSEL1 | CPU_BSEL0 |
|---|---|---|---|
| 133 | 0 | 0 | 1 |
| 166 | 0 | 1 | 1 |

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Compal Electronics, Inc.

Title: Yonah CPU in mFCPGA479

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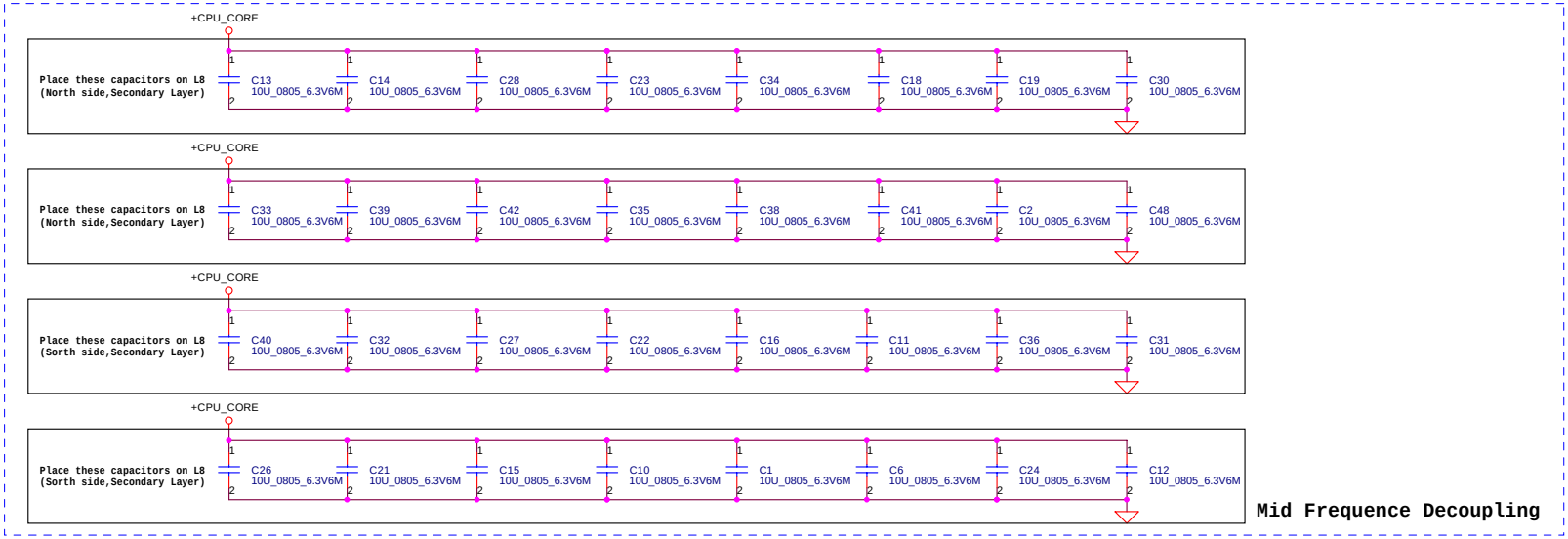
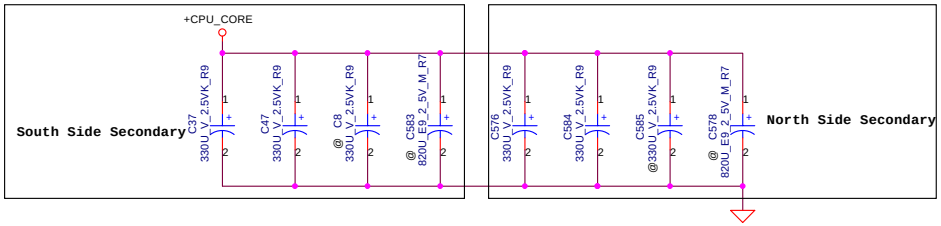
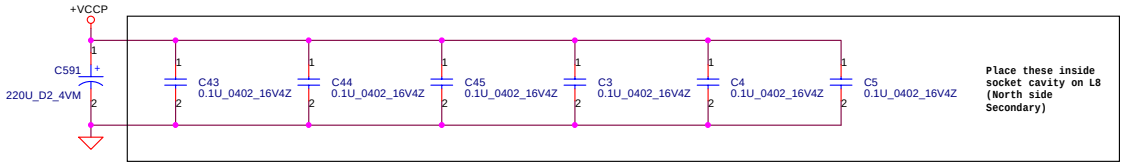



**ESR <= 1.5m ohm**
**Capacitor > 1980uF**

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**Compal Electronics, Inc.**

Title: **CPU Bypass capacitors**

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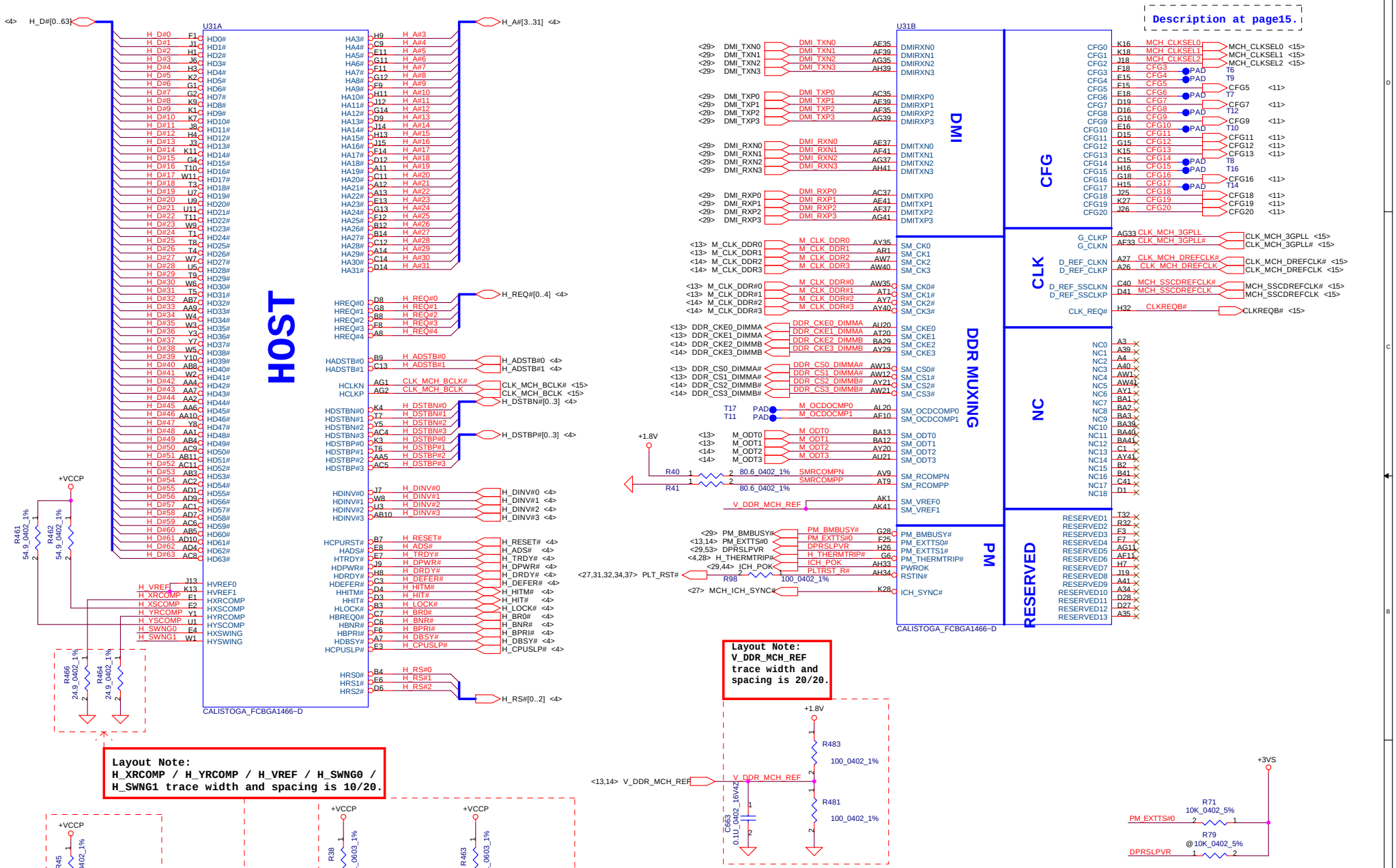


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Title: Calistoga (1/6)

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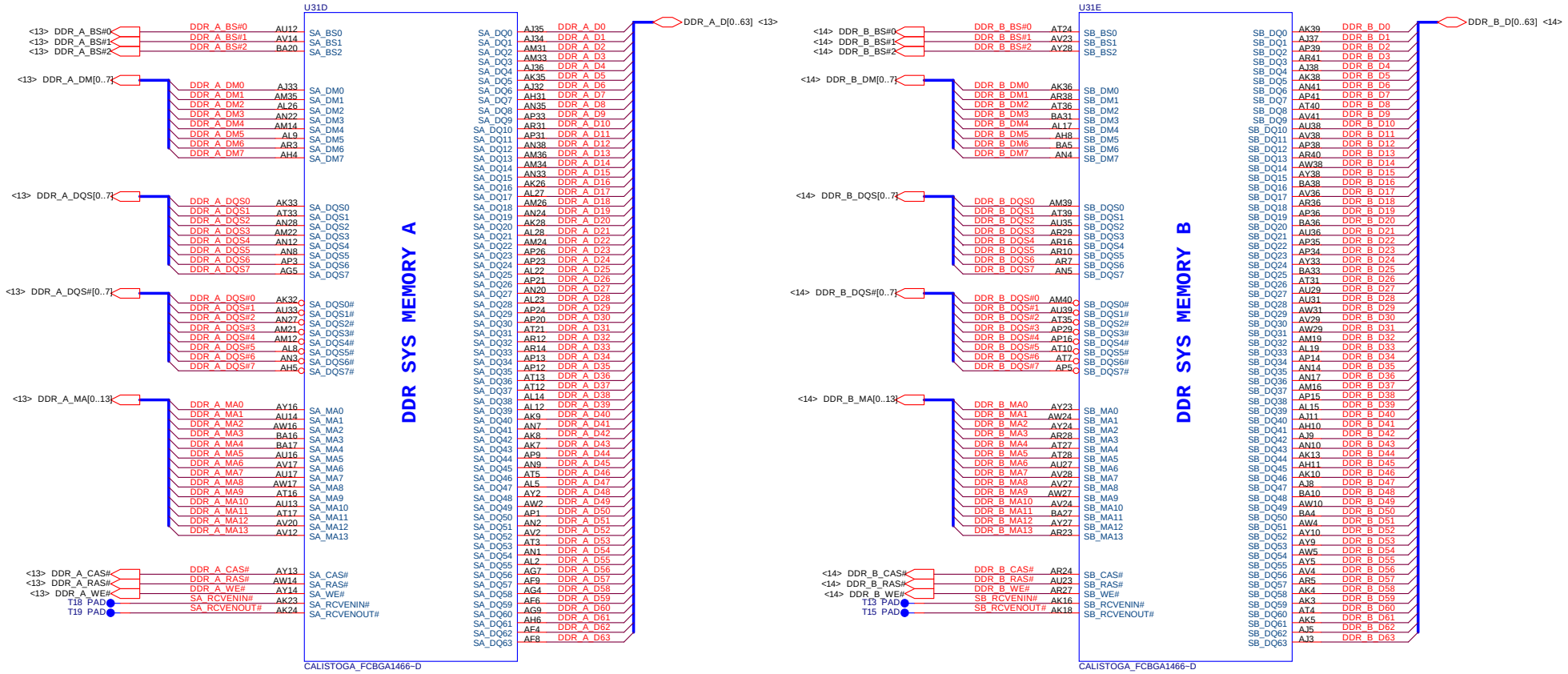


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**Compal Electronics, Inc.**

Title: **Calistoga (2/6)**

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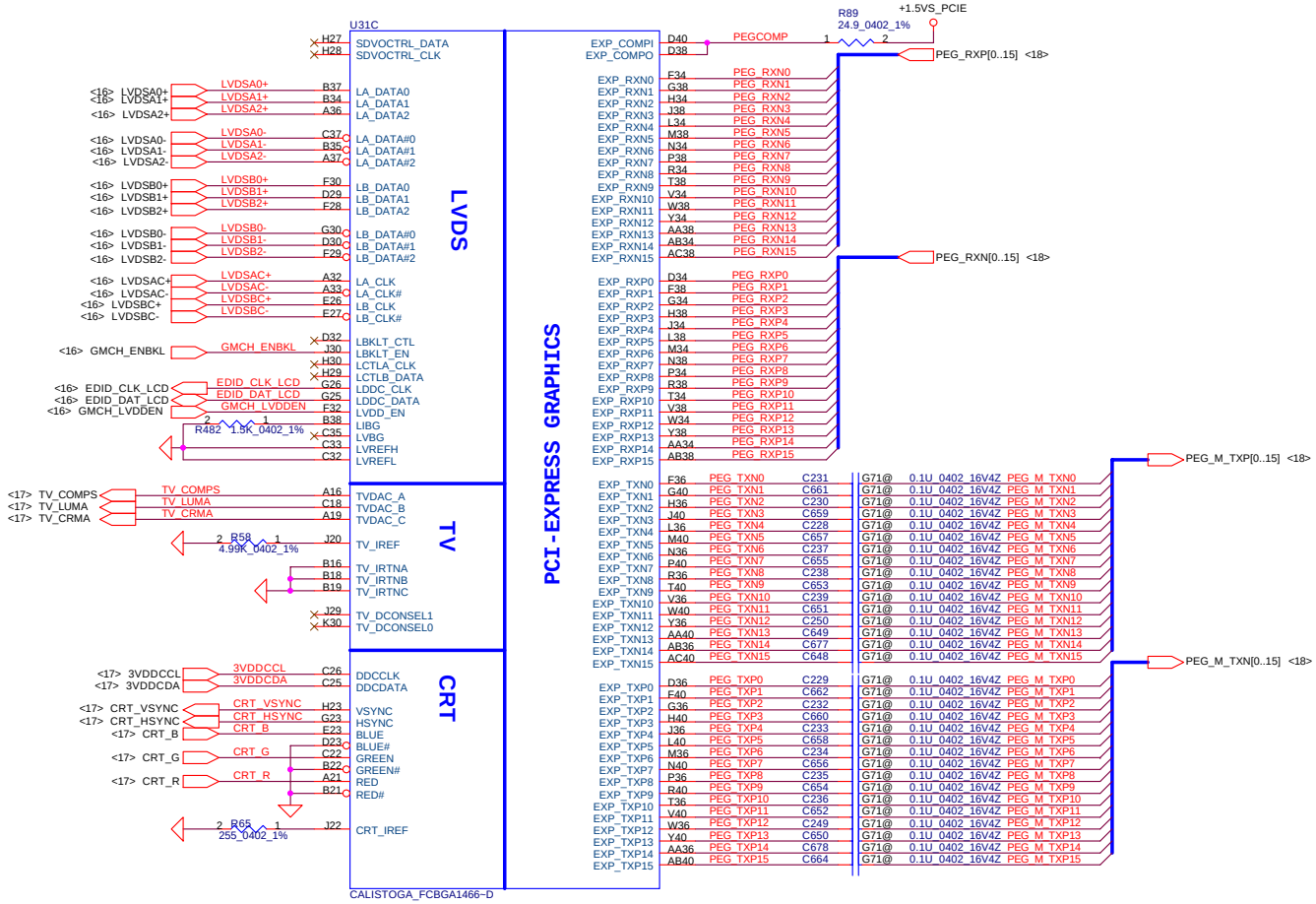


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**Compal Electronics, Inc.**

Title: **Calistoga (3/6)**

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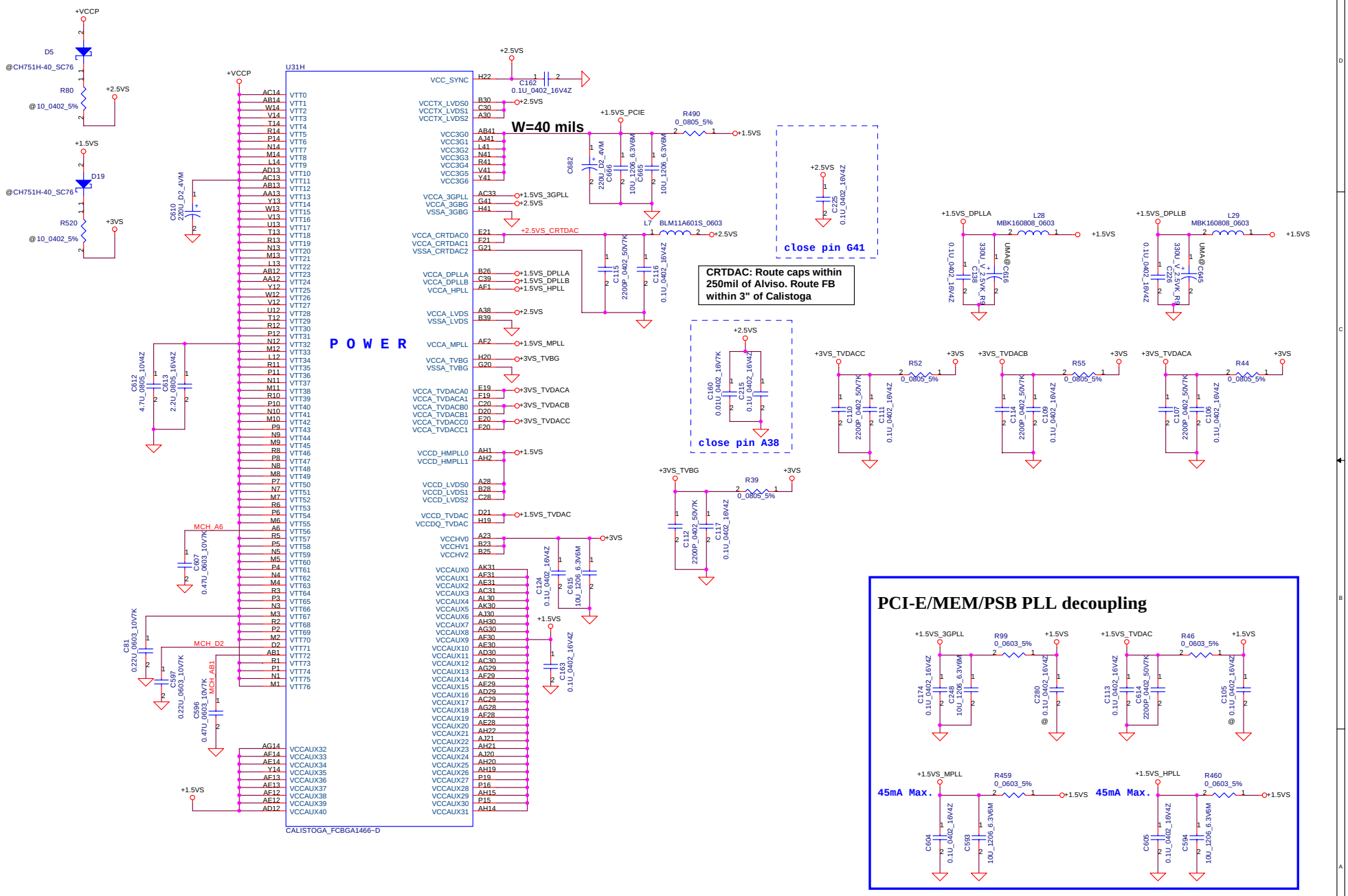


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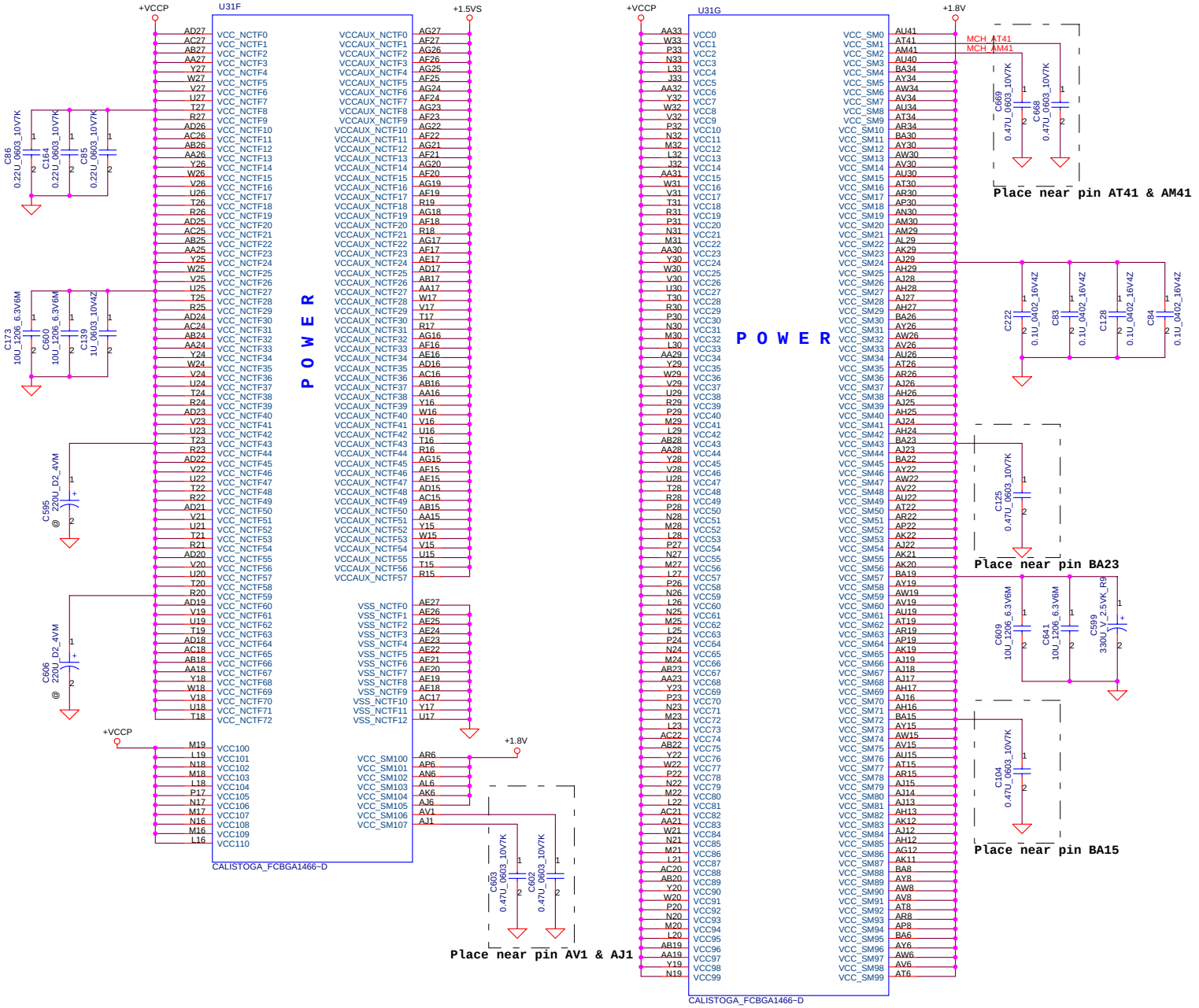
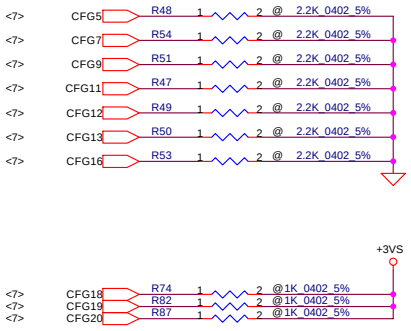



# Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

| | |
|---|---|
| CFG[2:0] | 011 = 667MT/s FSB<br>001 = 533MT/s FSB |
| CFG5 | 0 = DMI x 2<br>1 = DMI x 4*(Default) |
| CFG7 | 0 = Reserved<br>1 = Mobile Yonah CPU*(Default) |
| CFG9 | 0 = Lane Reversal Enable<br>1 = Normal Operation (Default)* |
| CFG6<br>PSB 4X CLK Enable | 0 = Reserved<br>1 = Calistoga * |
| CFG[13:12] | 00 = Reserved<br>01 = XOR Mode Enabled<br>10 = All Z Mode Enabled<br>11 = Normal Operation *(Default) |
| CFG16 | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled *(Default) |
| CFG10 CFG18 | 10 = 1.05V*(Default)<br>01 = 1.5V |
| CFG19 | 0 = Normal Operation * (Default)<br>1 = DMI Lane Reversal Enable |
| SDVO_CTRLDATA | 0 = No SDVO Device Present * (Default)<br>1 = SDVO Device Present |
| CFG20<br>(PCIE/SDVO select) | 0 = Only PCIE or SDVO is operational. *(Default)<br>1 = PCIE/SDVO are operating simu. |




| | | | |
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Title: Calistoga (5/6)

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Date: Friday, December 16, 2005 | Sheet 11 of 60

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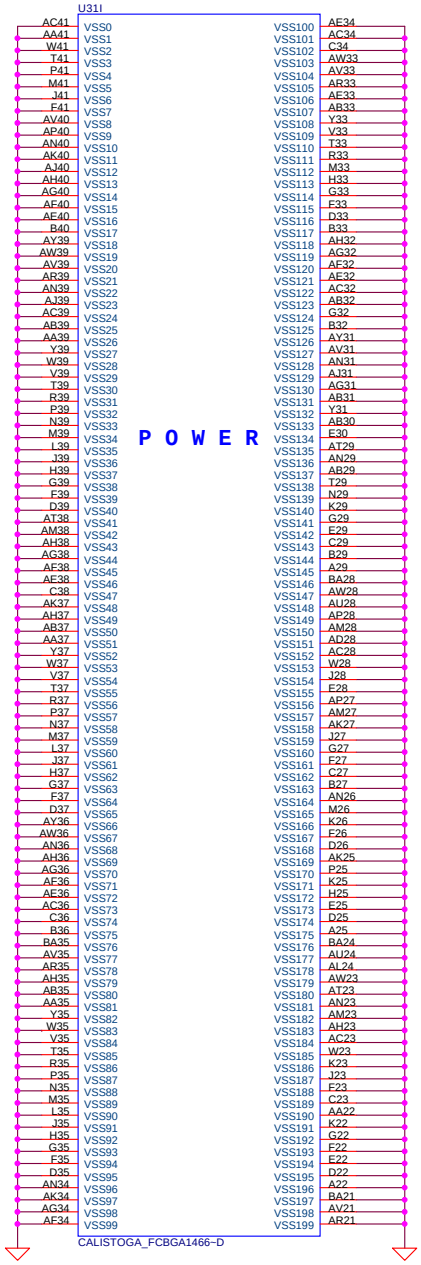


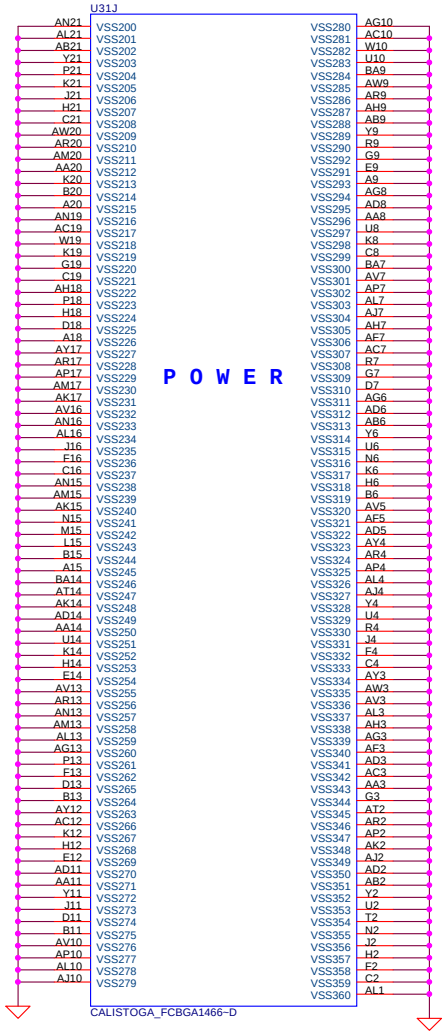


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Title: **Calistoga (6/6)**

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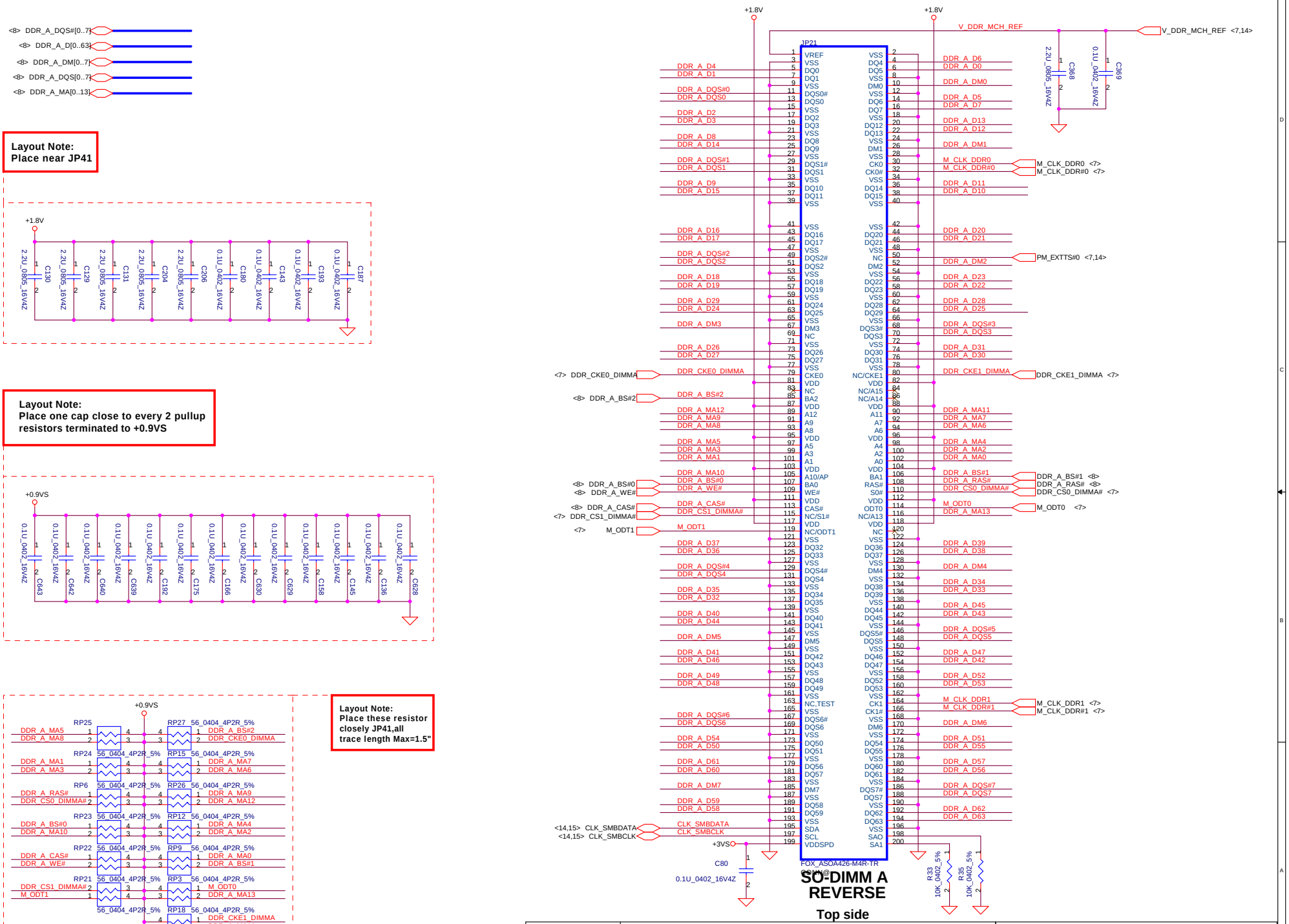


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Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT1

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Date: Thursday, December 15, 2005 | Sheet 13 of 60

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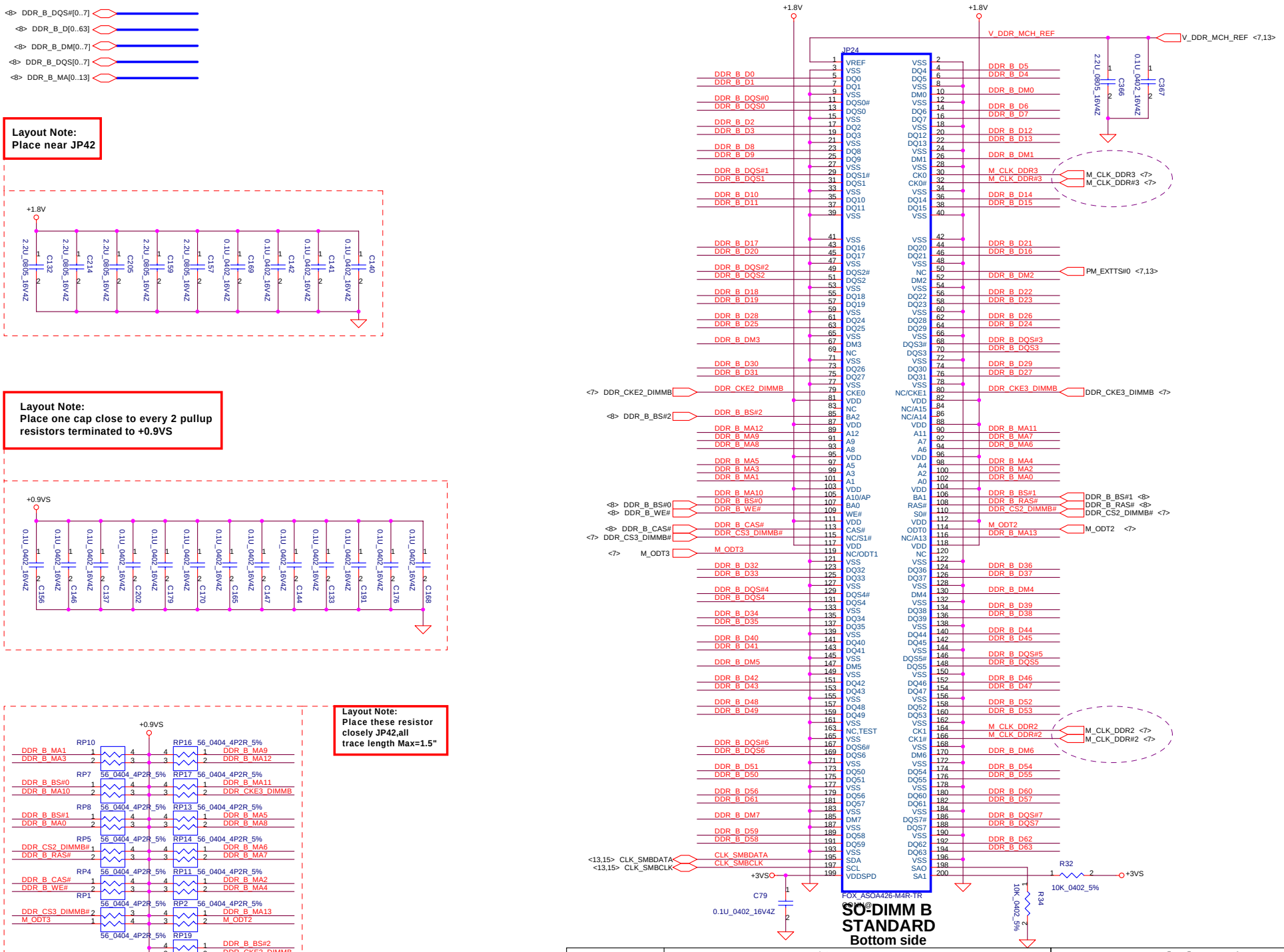


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Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT2

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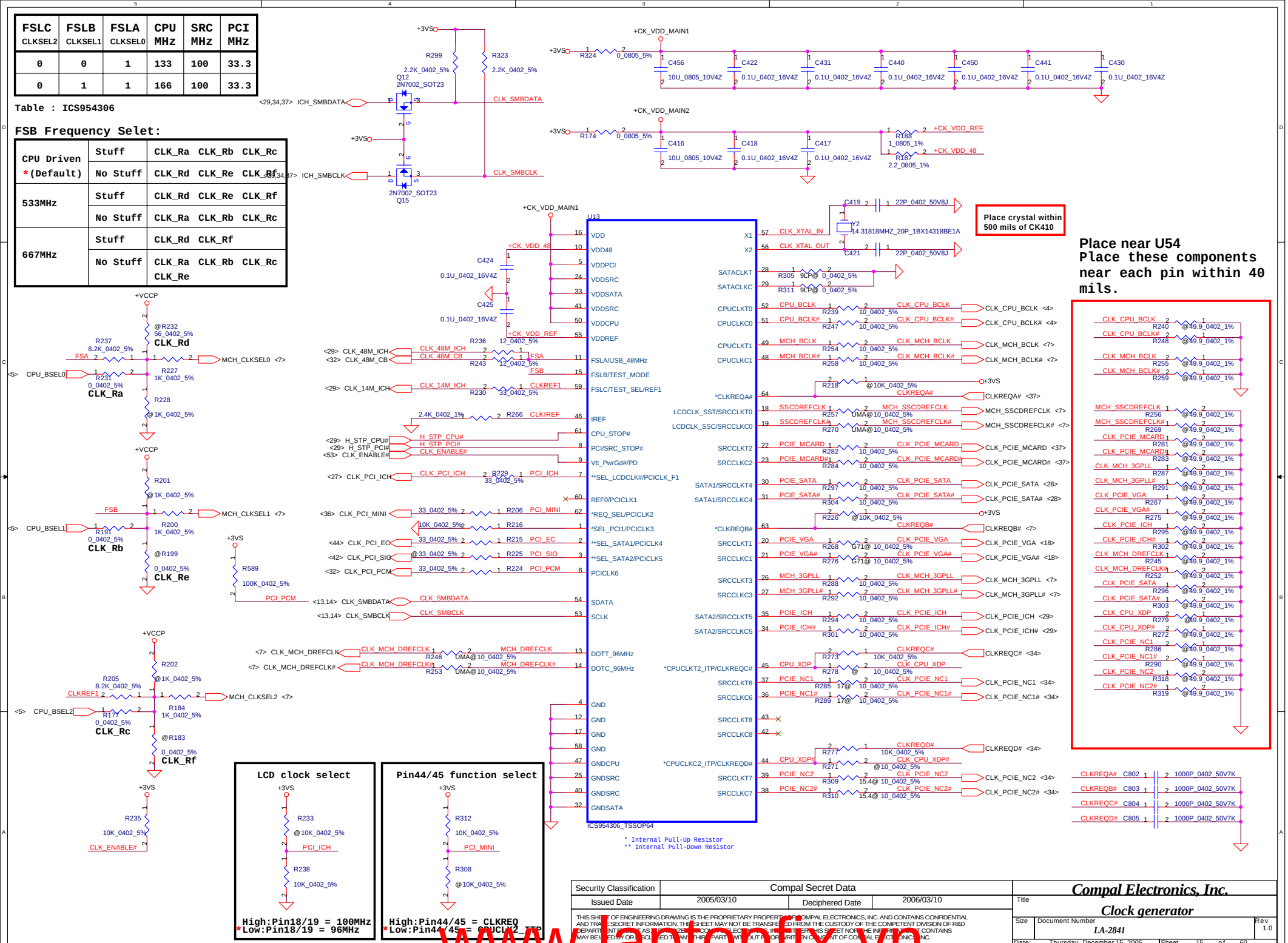
| FSLC CLKSEL2 | FSLB CLKSEL1 | FSLA CLKSEL0 | CPU MHz | SRC MHz | PCI MHz |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 133 | 100 | 33.3 |
| 0 | 1 | 1 | 166 | 100 | 33.3 |

Table : ICS954306

## FSB Frequency Selet:

| | | |
|---|---|---|
| CPU Driven *(Default) | Stuff | CLK_Ra CLK_Rb CLK_Rc |
| | No Stuff | CLK_Rd CLK_Re CLK_Rf |
| 533MHz | Stuff | CLK_Rd CLK_Re CLK_Rf |
| | No Stuff | CLK_Ra CLK_Rb CLK_Rc |
| 667MHz | Stuff | CLK_Rd CLK_Rf |
| | No Stuff | CLK_Ra CLK_Rb CLK_Rc CLK_Re |

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Compal Electronics, Inc.

Title: Clock generator

Size: | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 15 of 60

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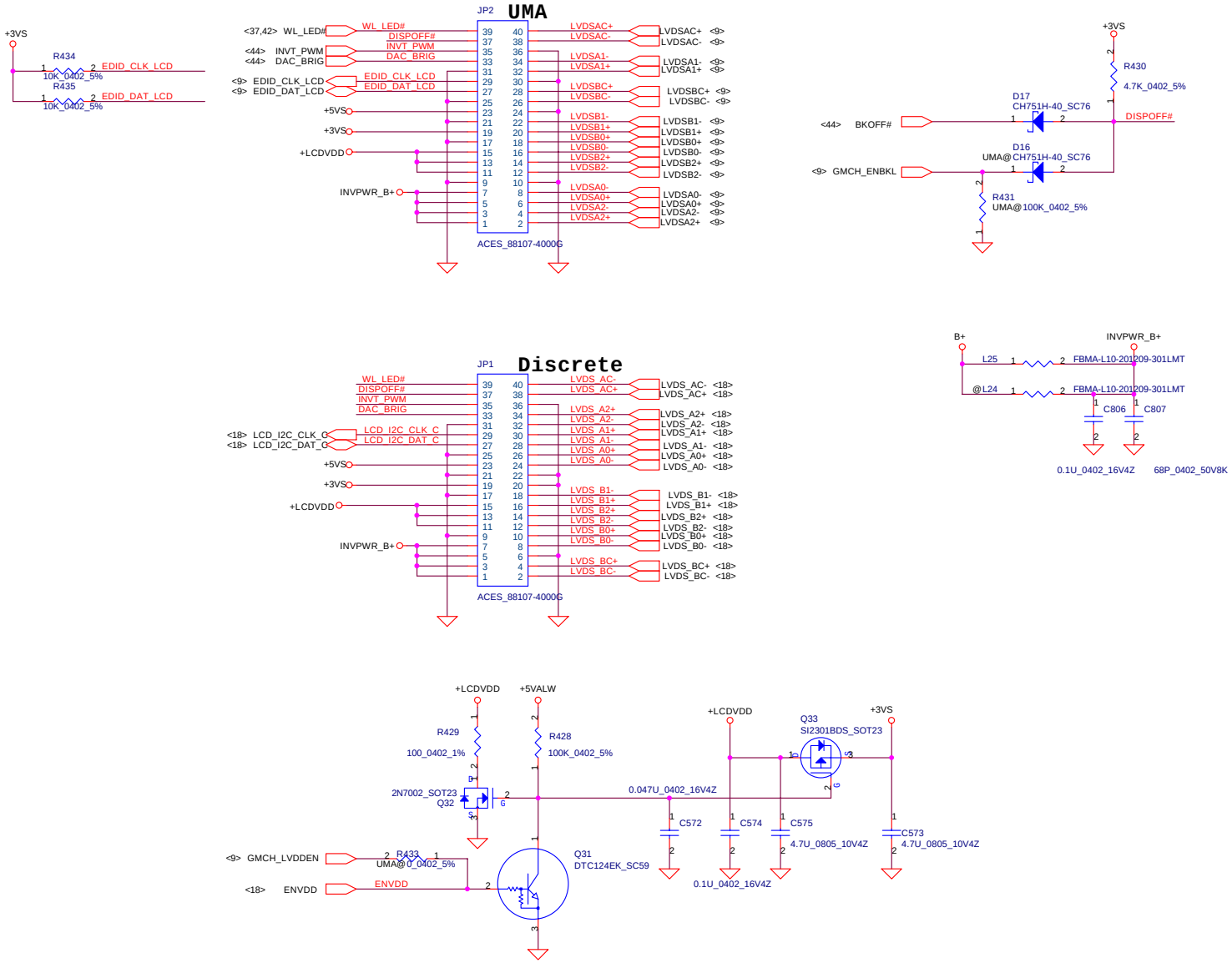
# LCD Panel & inverter Connector

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**Compal Electronics, Inc.**

Title: **LVDS Connector**

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Date: Thursday, December 15, 2005 | Sheet 16 of 60

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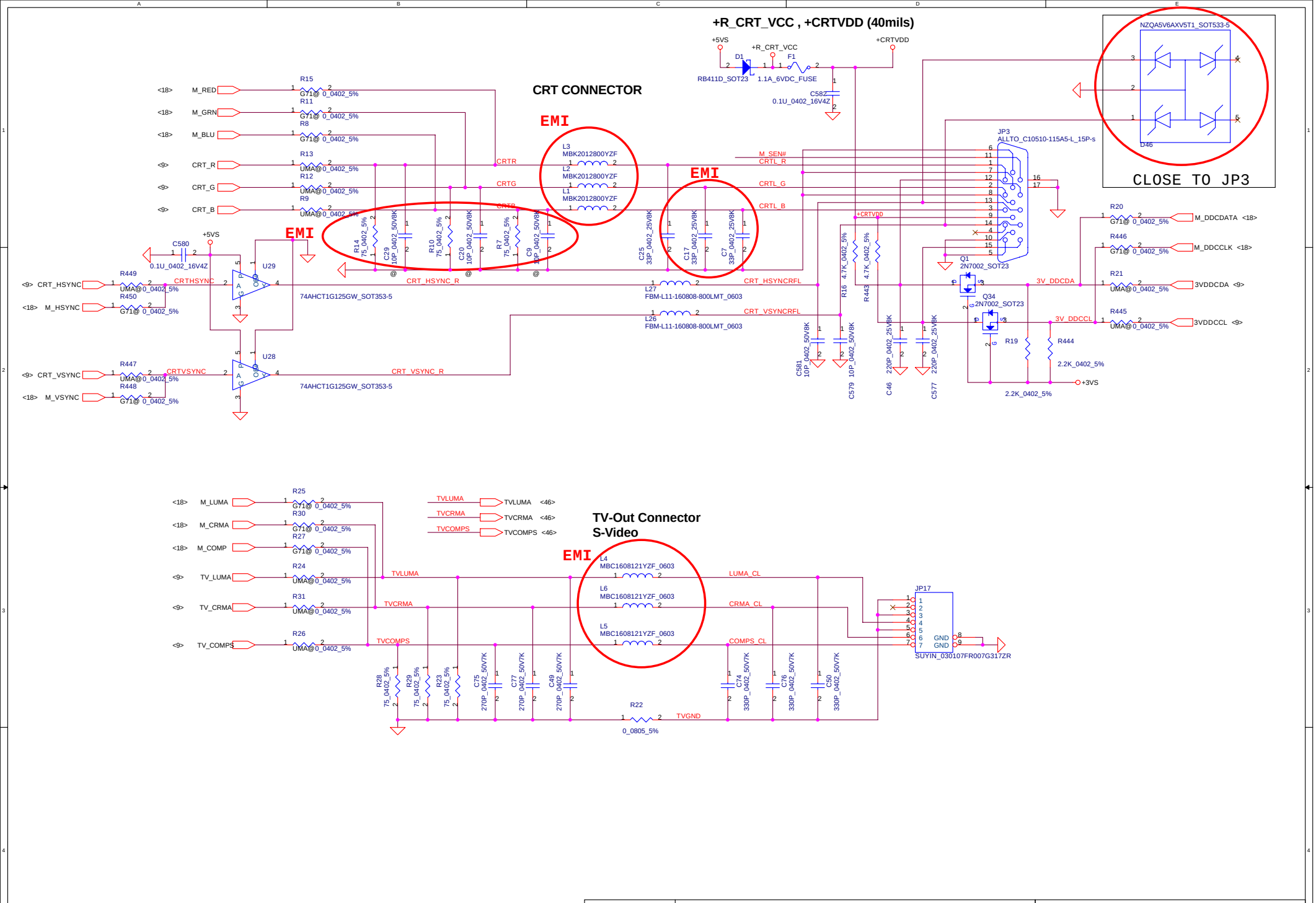


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**Compal Electronics, Inc.**

Title: **CRT & TVout Connector**

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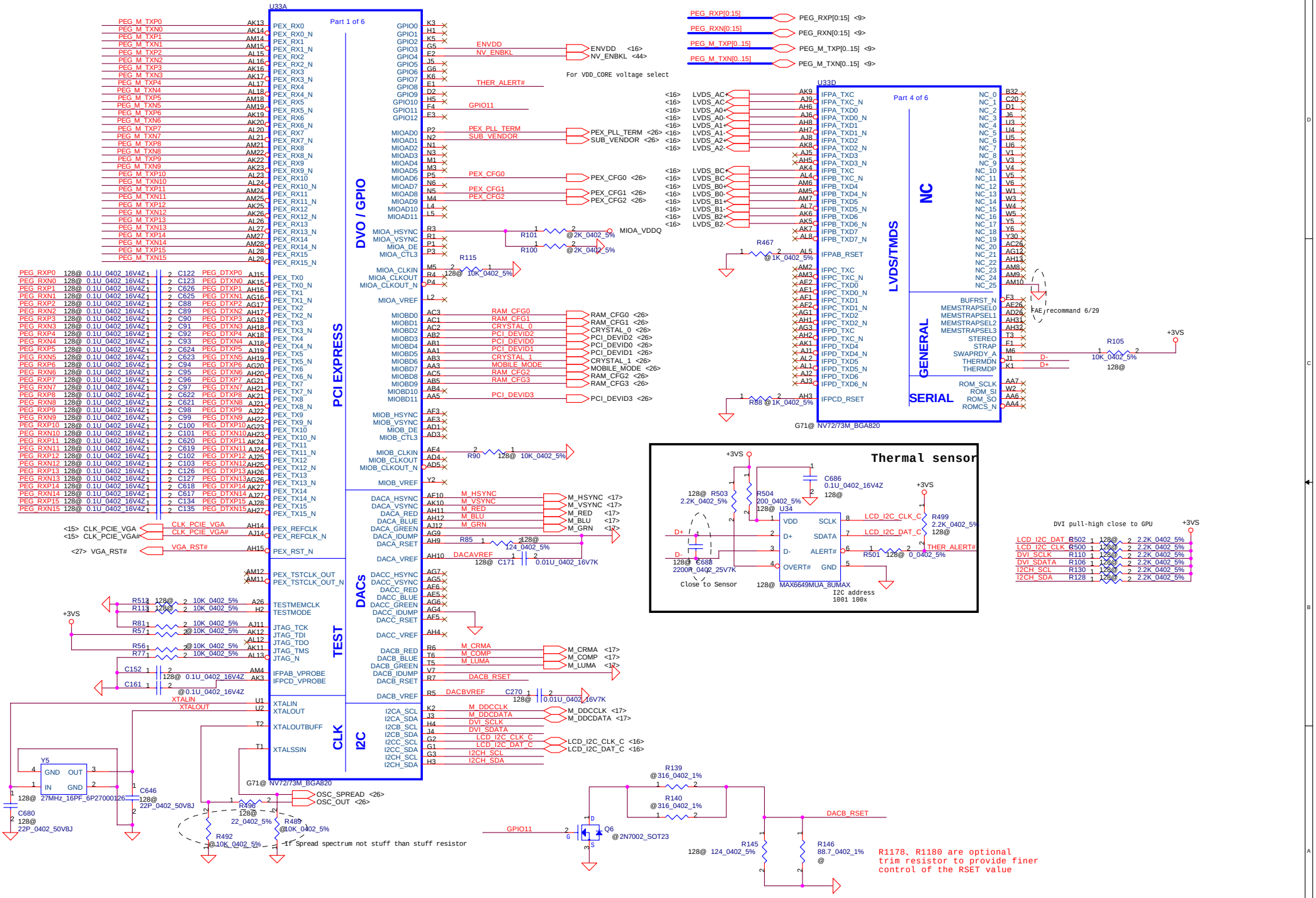


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Compal Electronics, Inc.

Title: G72/73VGA Board

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 18 of 60

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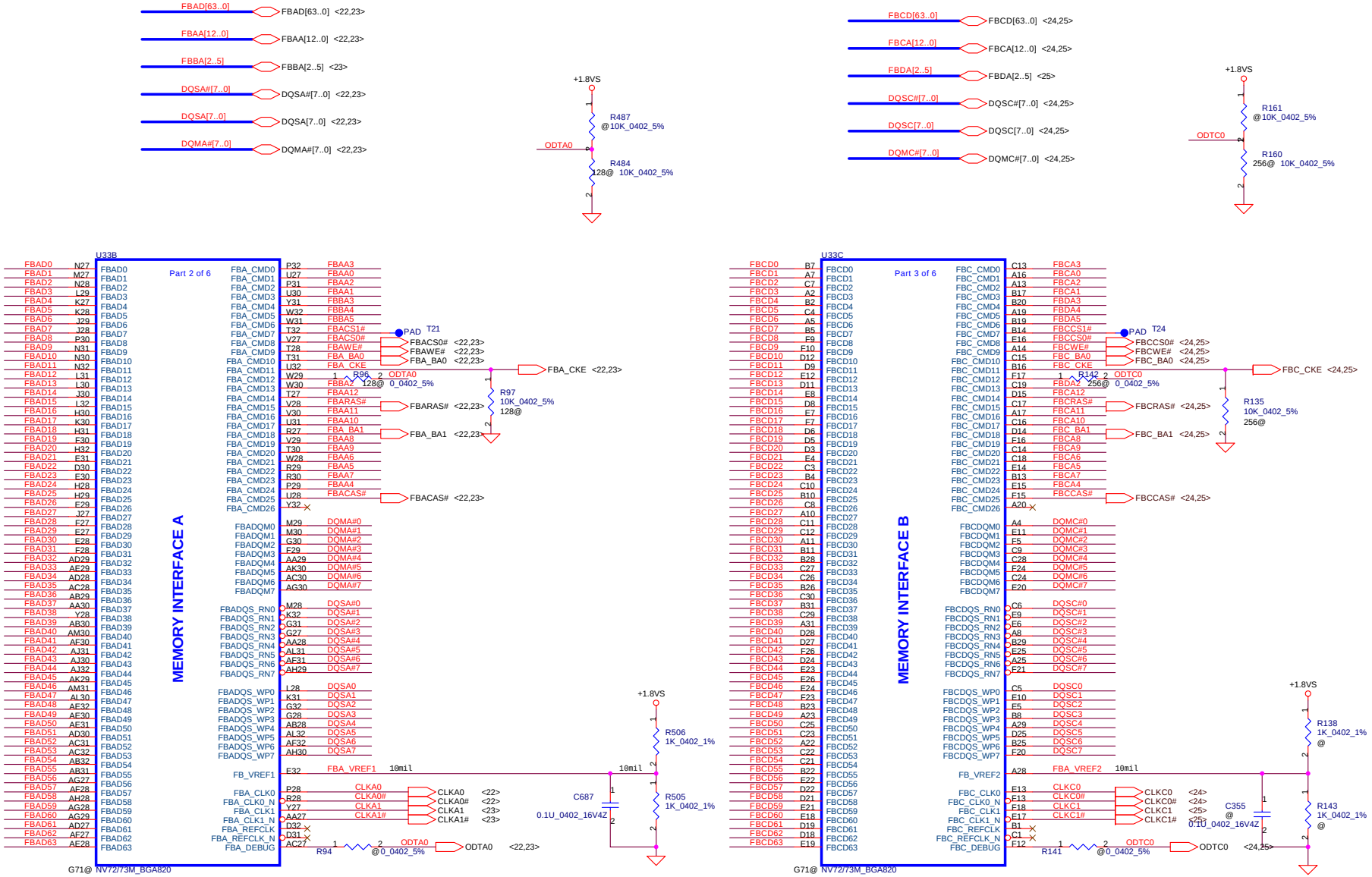


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| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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**Compal Electronics, Inc.**

Title: **G72/73VGA Board**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 19 of 60

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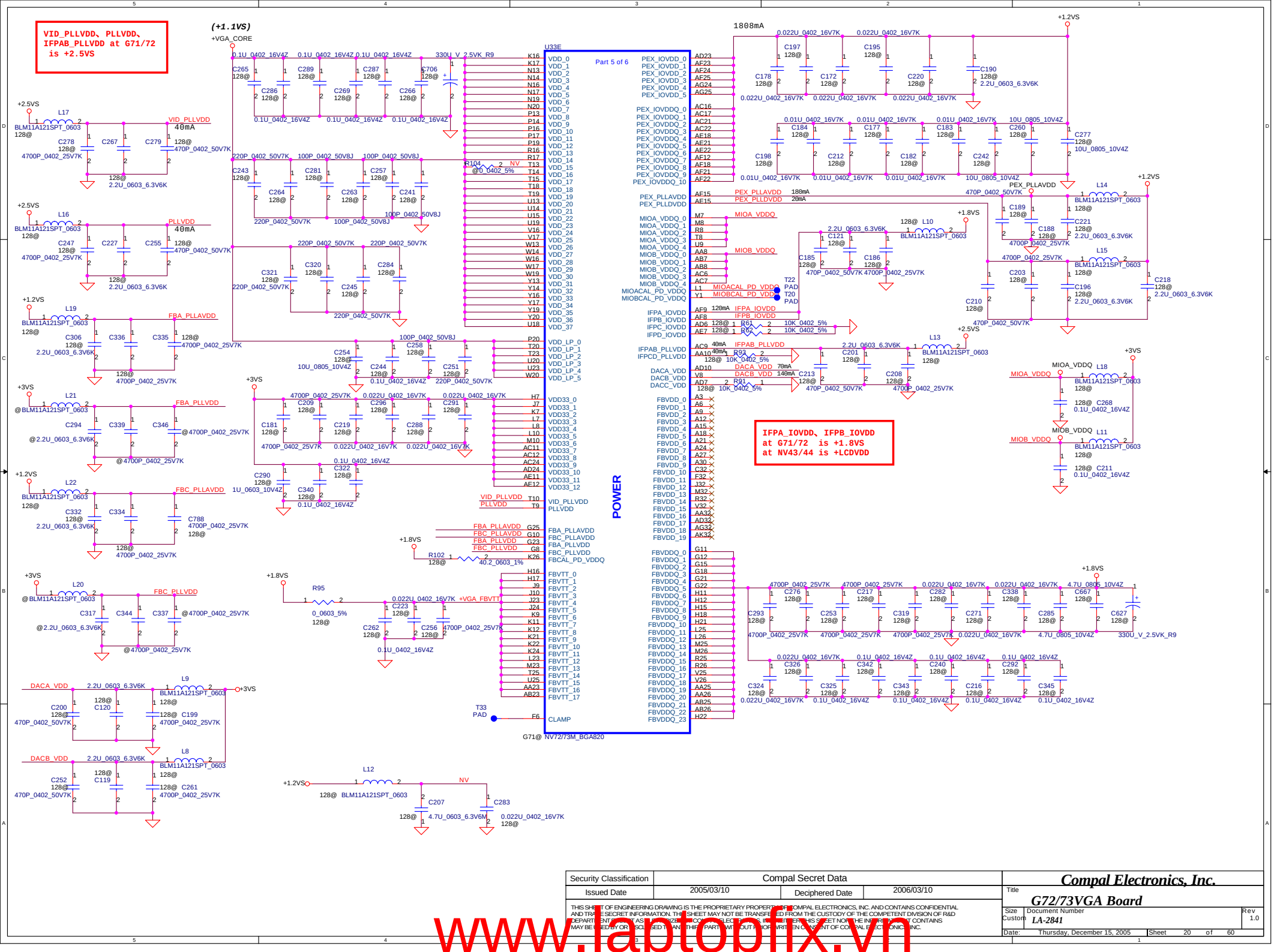


| Security Classification | Compal Secret Data | | |
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| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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Compal Electronics, Inc.

Title: G72/73VGA Board

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 20 of 60

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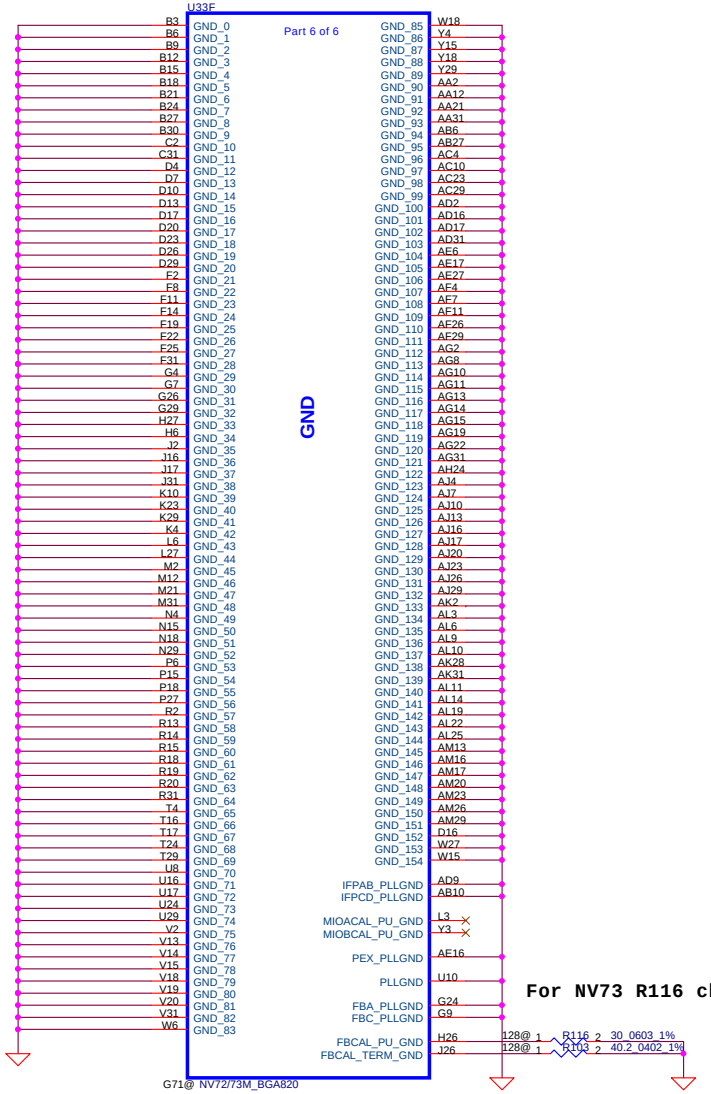


For NV73 R116 change to 40.2_0603_1%(SD014402A80)

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**Compal Electronics, Inc.**

Title: **G72/73VGA Board**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 21 of 60

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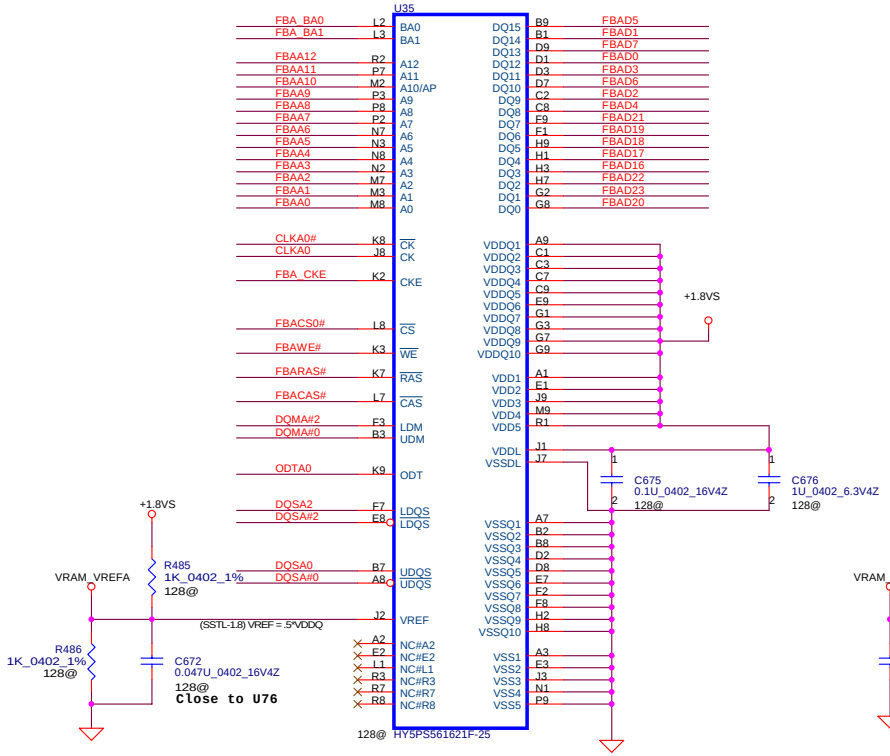
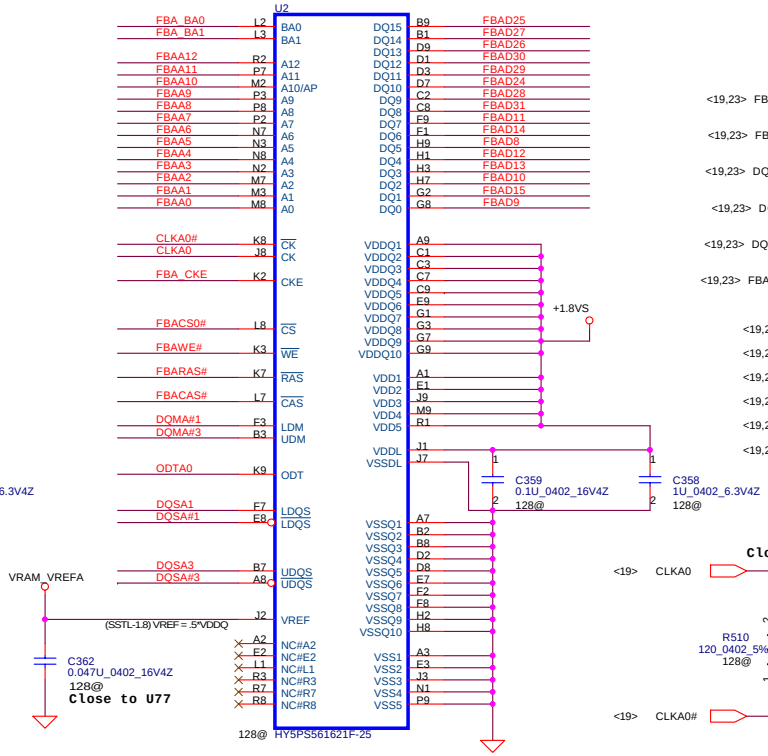
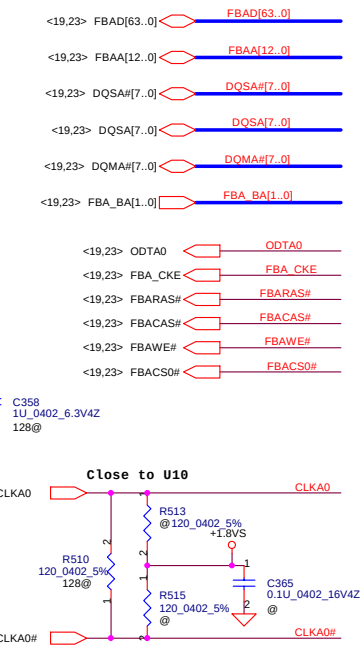


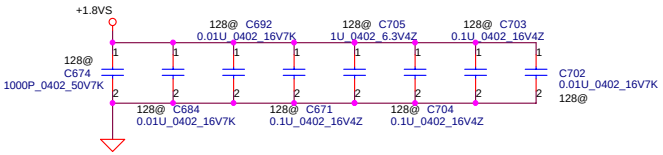

DDR2 BGA MEMORY

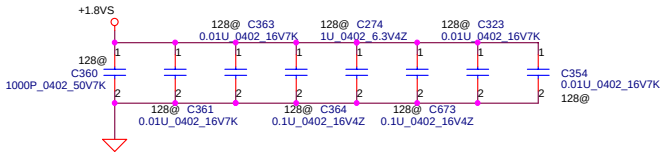



DDR2 BGA MEMORY




**For NV73 R510 change to 481_0402_1%(SD00000CA80)**

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**Compal Electronics, Inc.**

Title: **G72/73VGA Board**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 22 of 60

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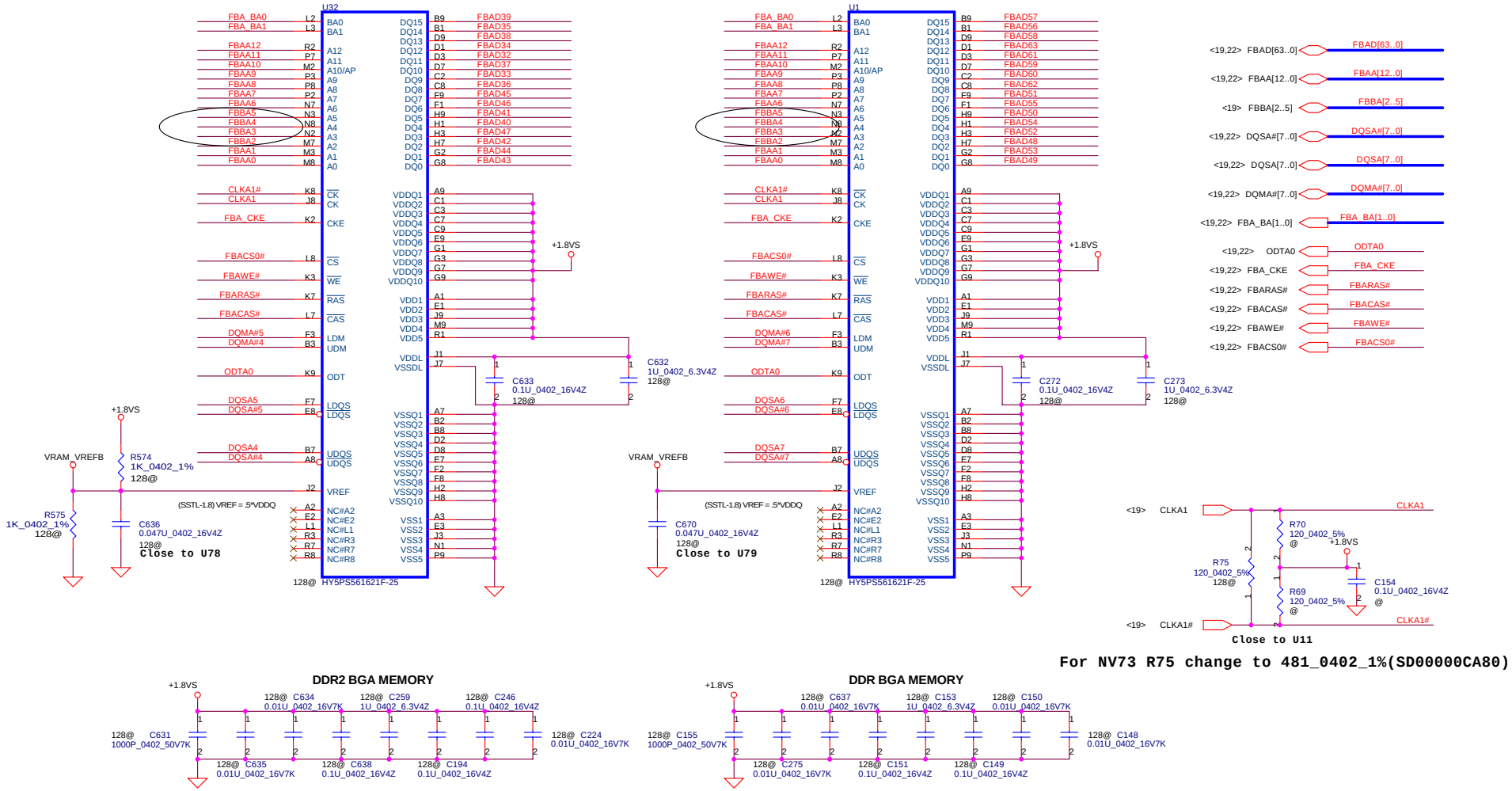


For NV73 R75 change to 481_0402_1%(SD00000CA80)




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| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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**Compal Electronics, Inc.**

Title: **G72/73VGA Board**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 23 of 60

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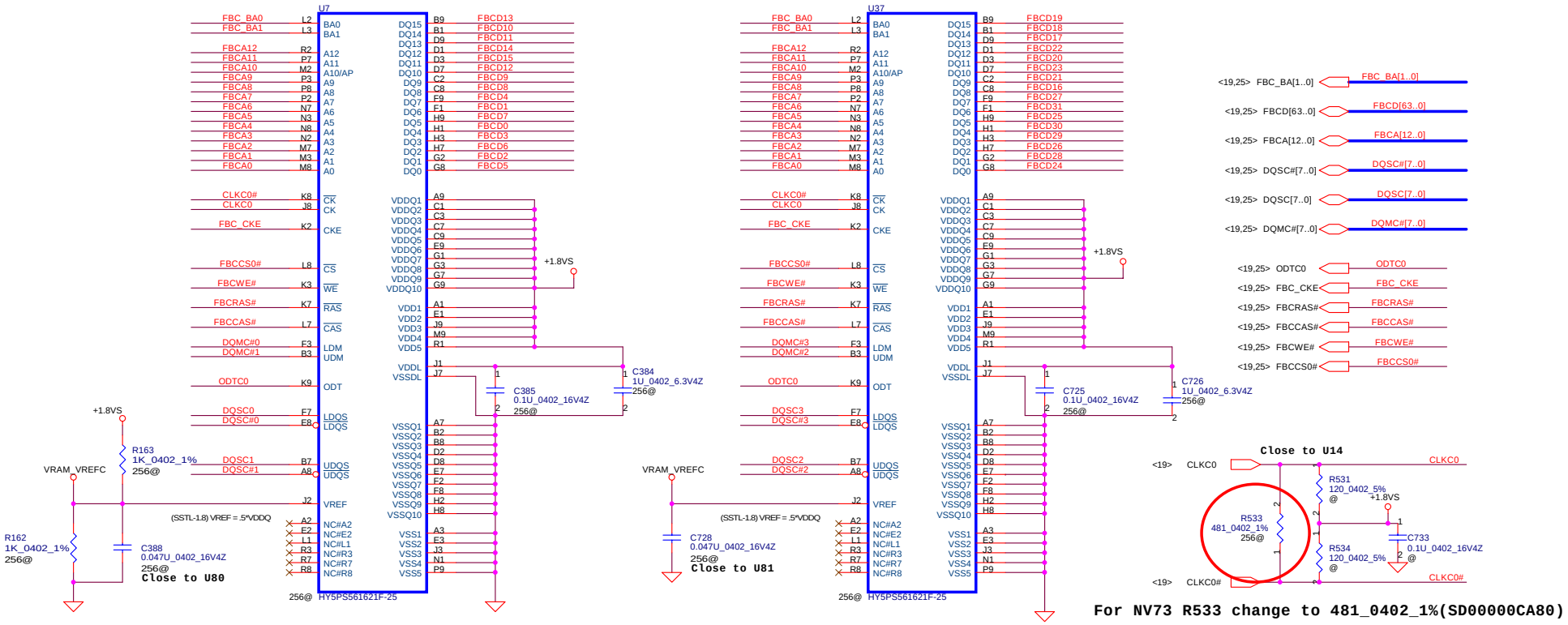
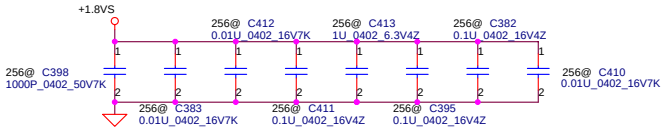
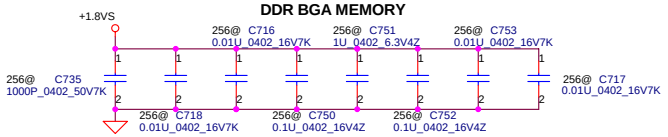



For NV73 R533 change to 481_0402_1%(SD00000CA80)

## DDR2 BGA MEMORY




## DDR BGA MEMORY

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**Compal Electronics, Inc.**

Title: **G71/72VGA Board**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 24 of 60

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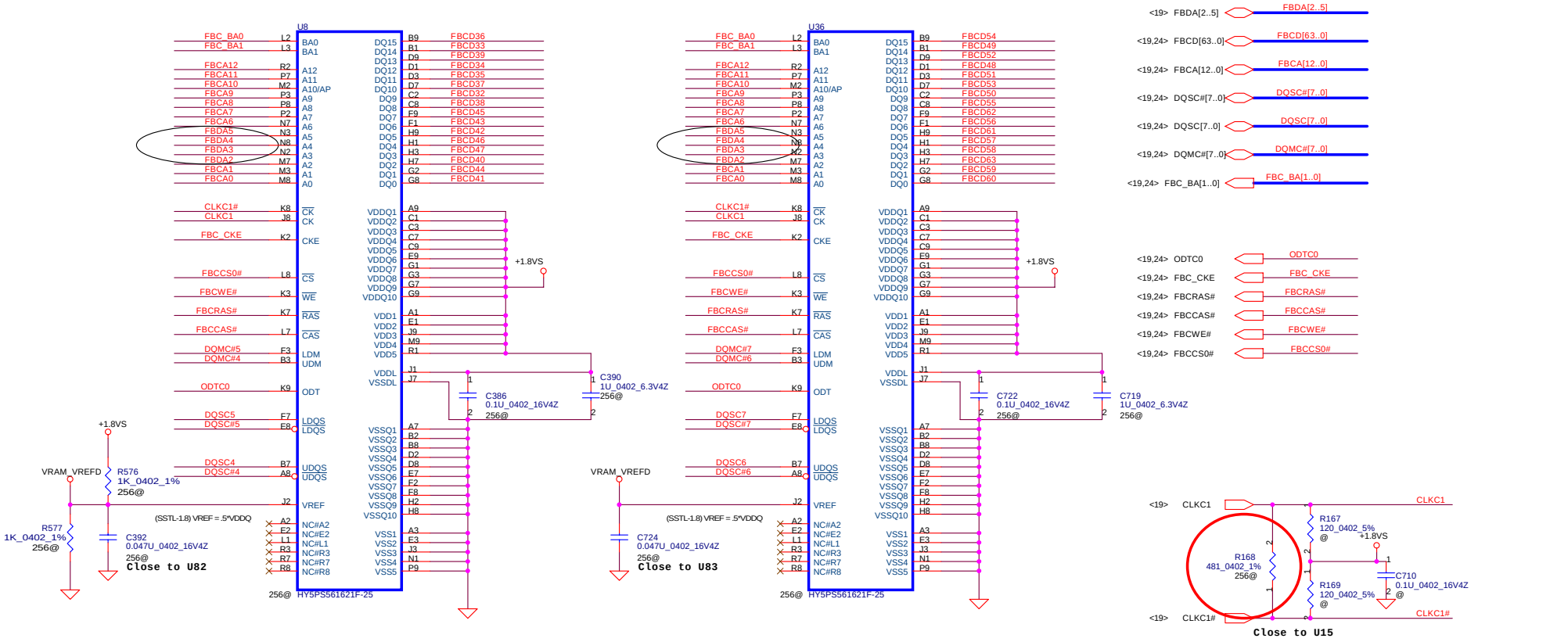


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Compal Electronics, Inc.

Title: G71/72VGA Board

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 25 of 60

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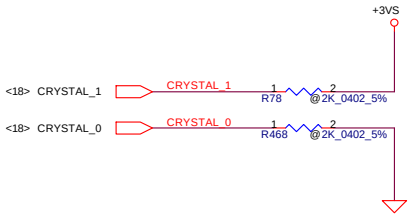
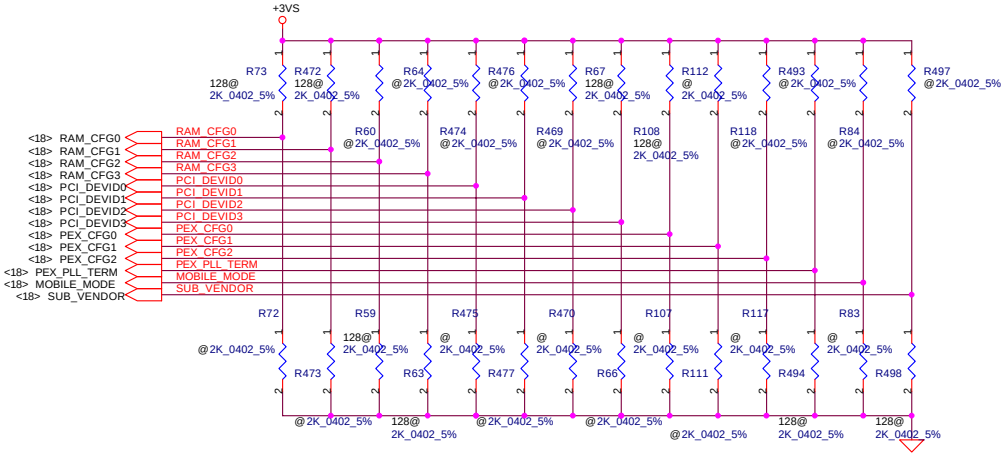
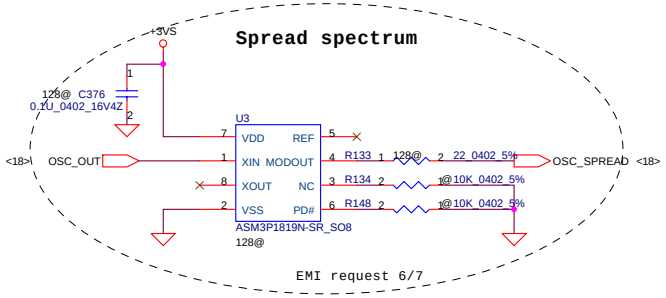
| STRAPS | PIN | DESCRIPTION | Value | |
|---|---|---|---|---|
| CRYSTAL[1:0] | MIOBD[6,2] | 27MHz=10, 14.318MHz=01, 13.5MHz=00 | 10 | |
| ROM_TYPE[1:0] | MIOBD [11:10] | Parallel=00, SERIAL M25P10=01, Serial SST45VF=10 | 01 | |
| SUB_VENDOR | MIOAD1 | VBIOS on card (pull high) VBIOS with system BIOS (pull down) | 0 | |
| PEX_PLL_TERM | MIOAD0 | | 0 | |
| PEX_CFG[2:0] | MIOAD [9,8,6] | Overridden | 001 | |
| RAM_CFG[3:0] | | 16Mx16 (1.8V or 2.5V)Hynix X 4pcs | 0011 | |
| | | 16Mx16 (1.8V or 2.5V)Infineon X 4pcs | 0010 | |
| | | 16Mx16 (1.8V or 2.5V)Samsung X 4pcs | 0001 | |
| | | 16Mx16 (1.8V or 2.5V)Hynix X 8pcs | 1011 | |
| | | 16Mx16 (1.8V or 2.5V)Infineon X 8pcs | 1010 | |
| | | 16Mx16 (1.8V or 2.5V)Samsung X 8pcs | 1001 | |
| PCI_DEVID[3:0] | A01 VIPD[5:3] MIOA_HSYNC | NV72M | 1000 | |
| | | NV73M | 1000 | |

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| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |

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**Compal Electronics, Inc.**

Title: **G71/72 VGA Board**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 26 of 60

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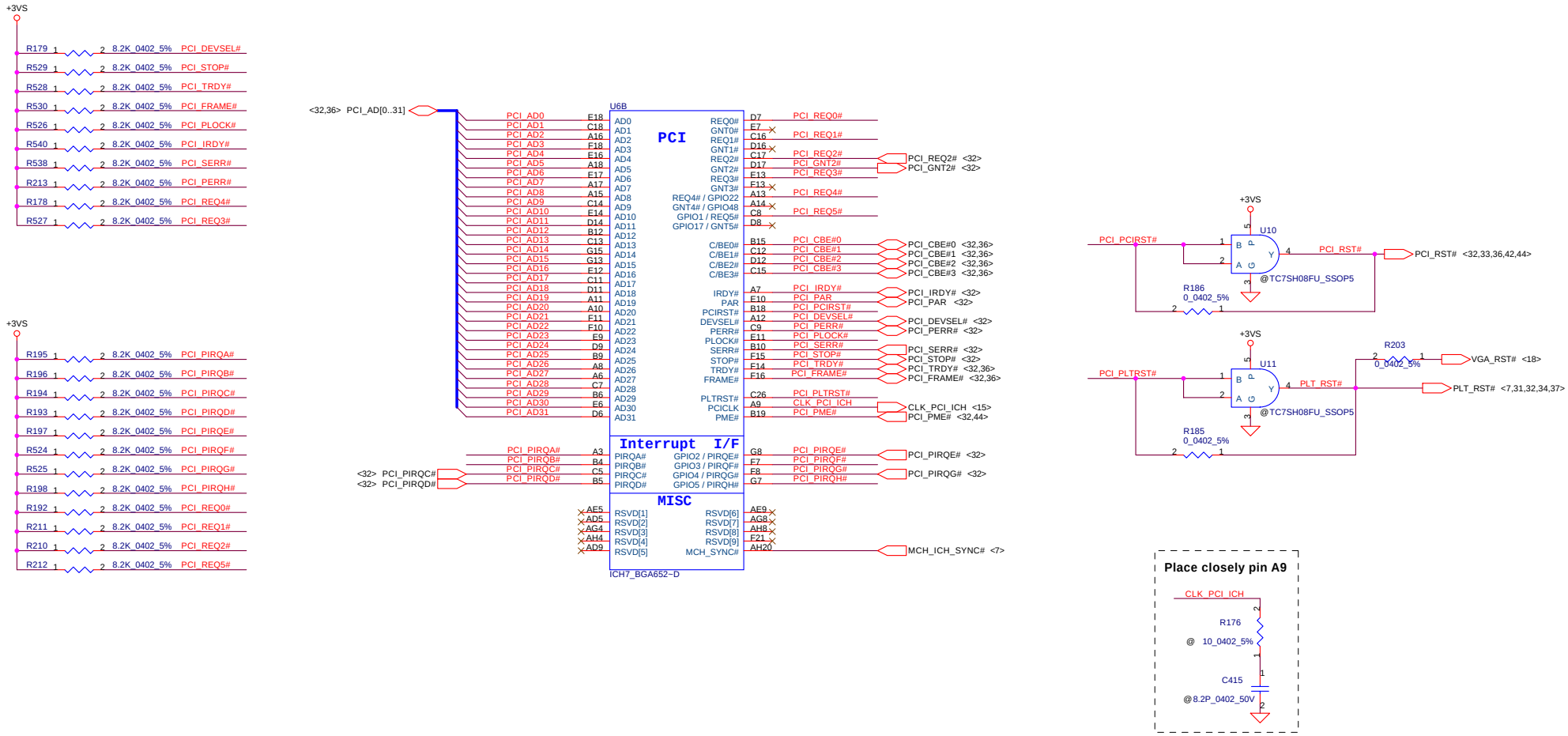


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Compal Electronics, Inc.

Title: ICH7-M(1/4)

Size: | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 27 of 60

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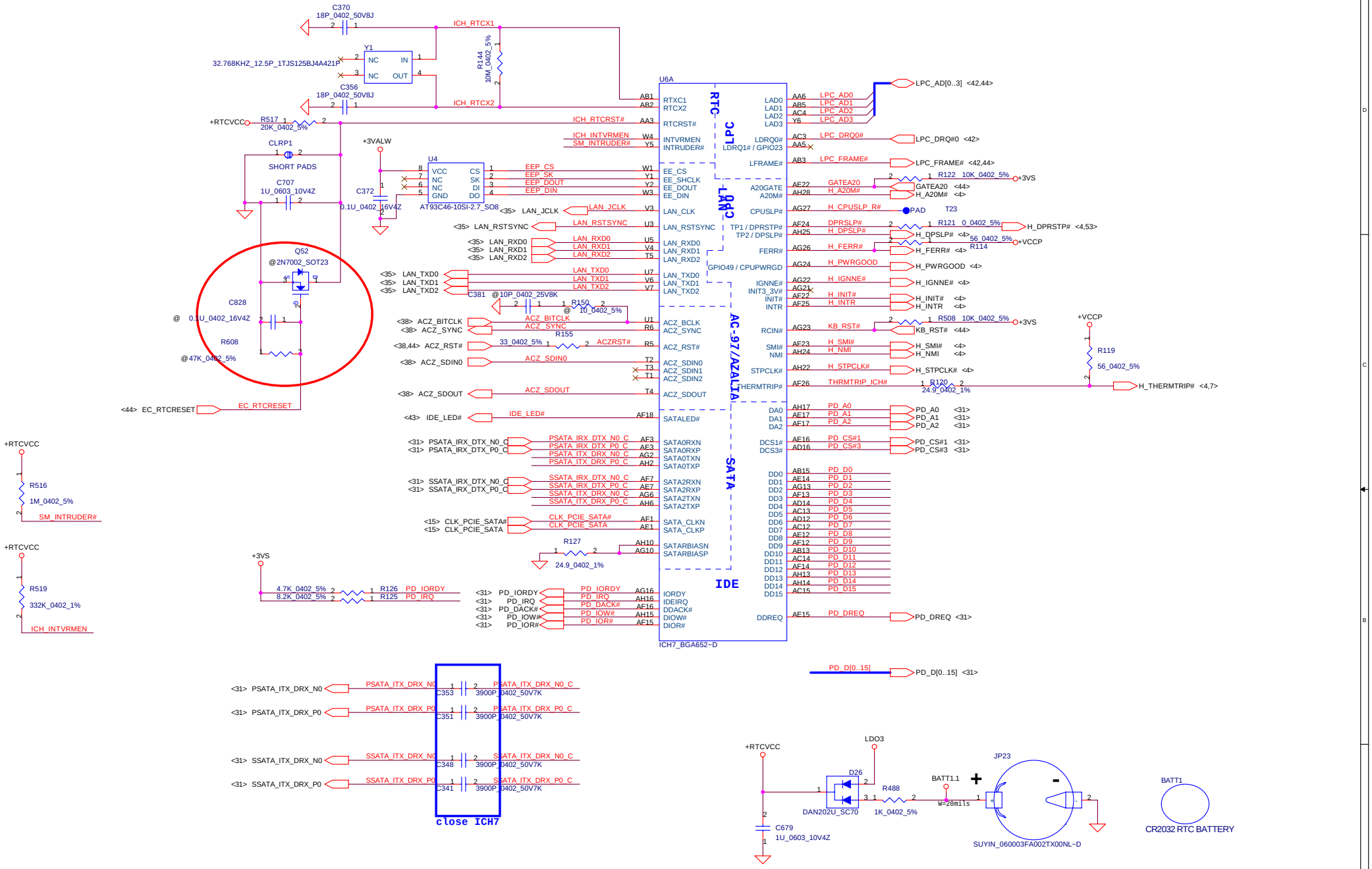


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| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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Compal Electronics, Inc.

Title: ICH7-M(2/4)

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 28 of 60

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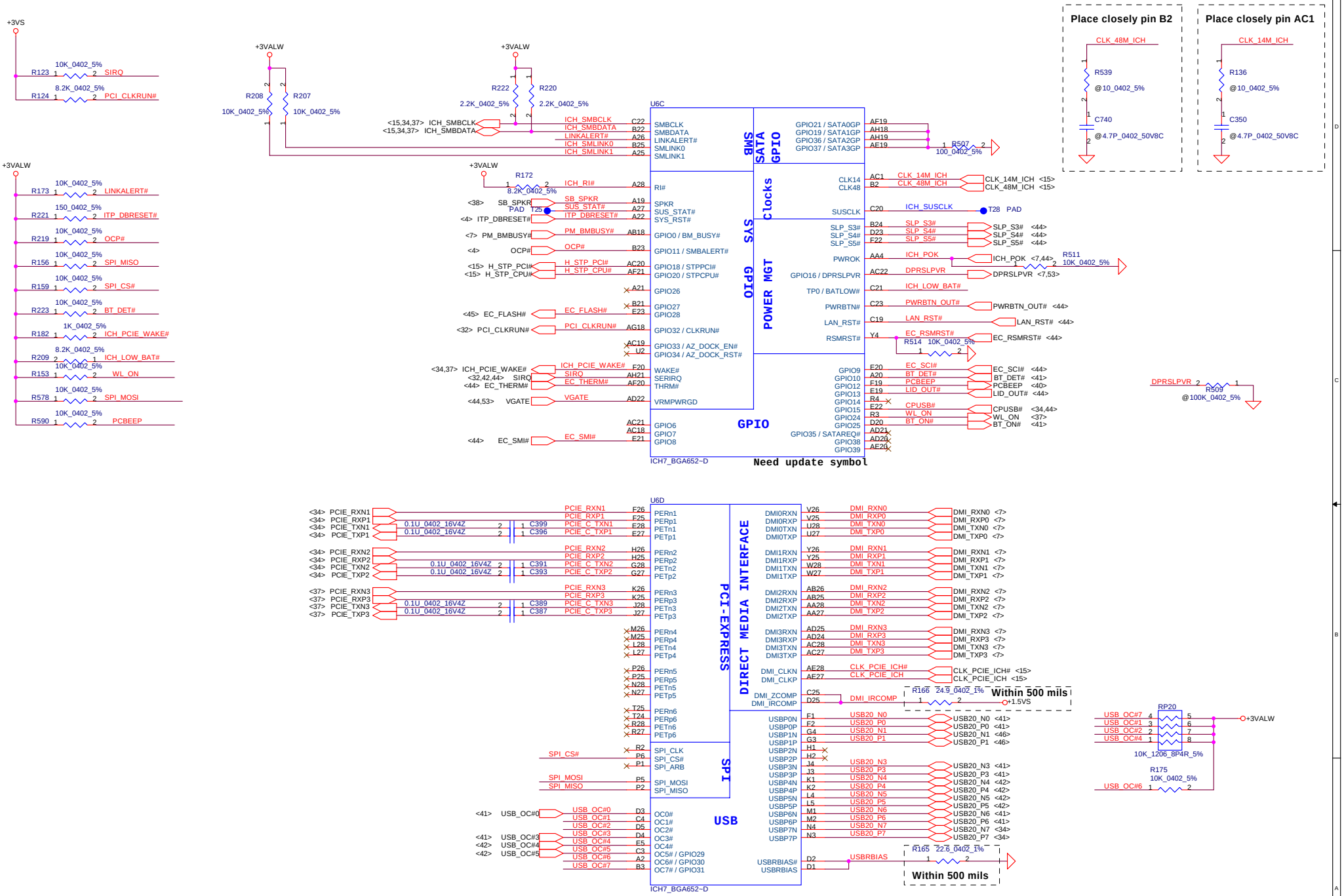


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| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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Compal Electronics, Inc.

Title: ICH7-M(3/4)

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 29 of 60

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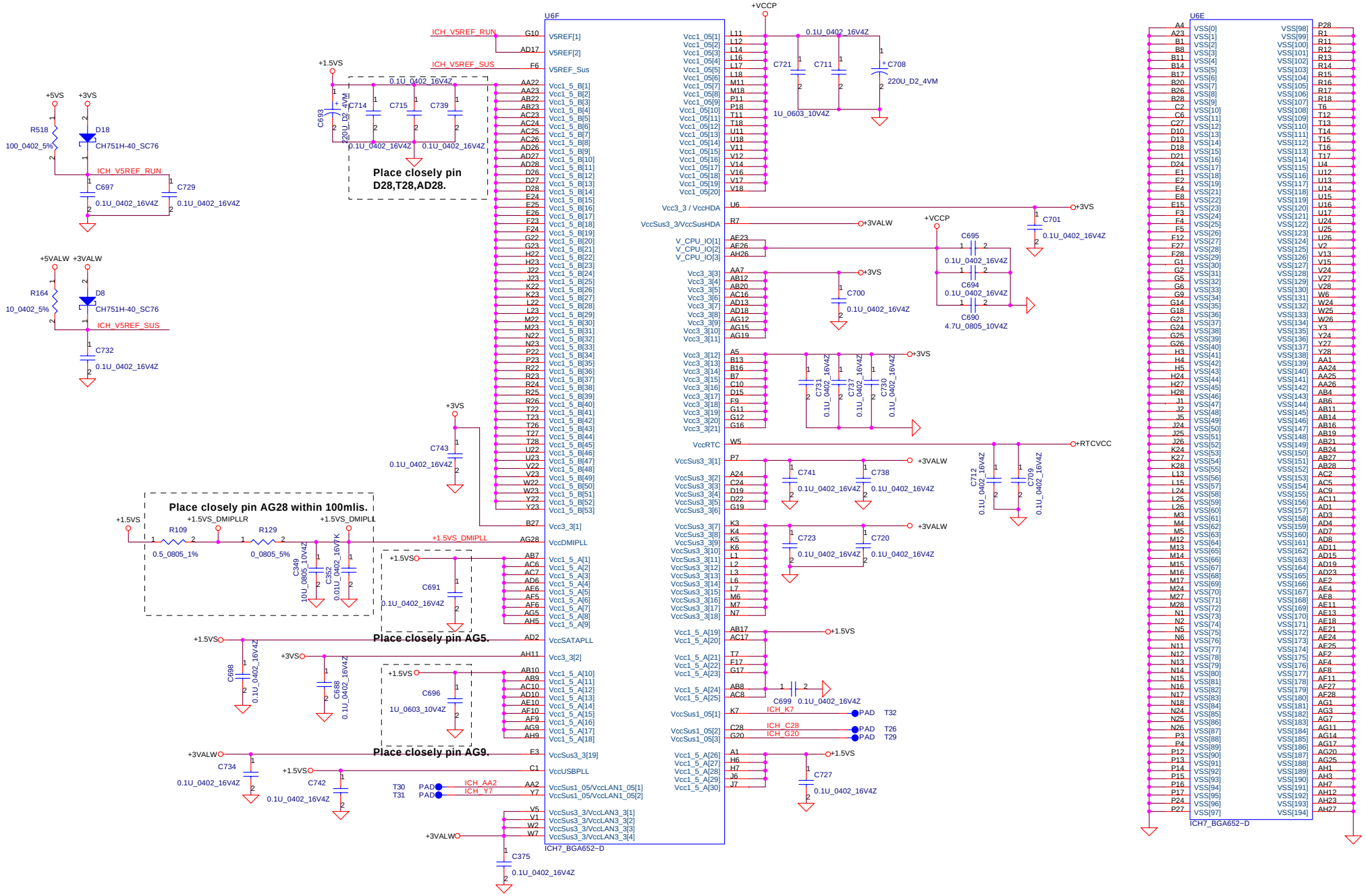


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**Compal Electronics, Inc.**

Title: **ICH7-M(4/4)**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 30 of 60

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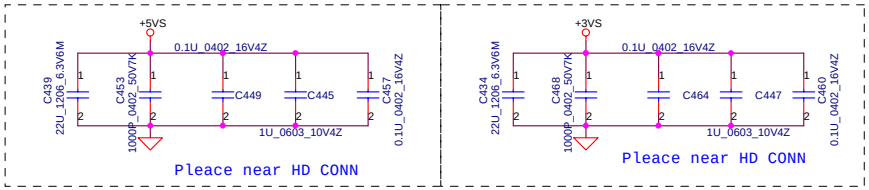
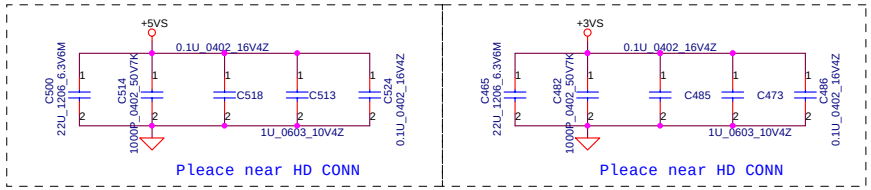
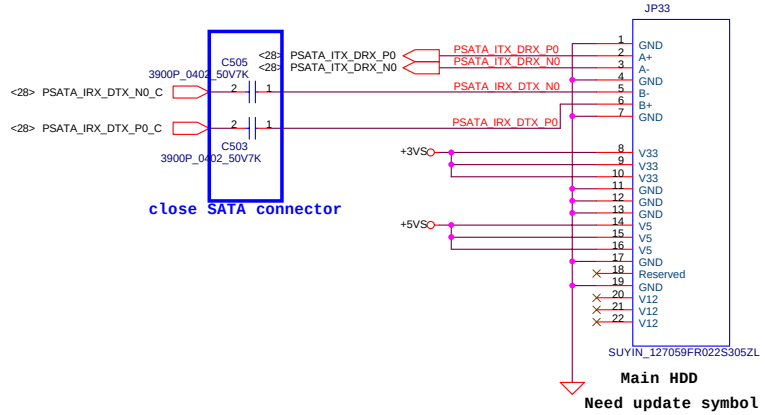


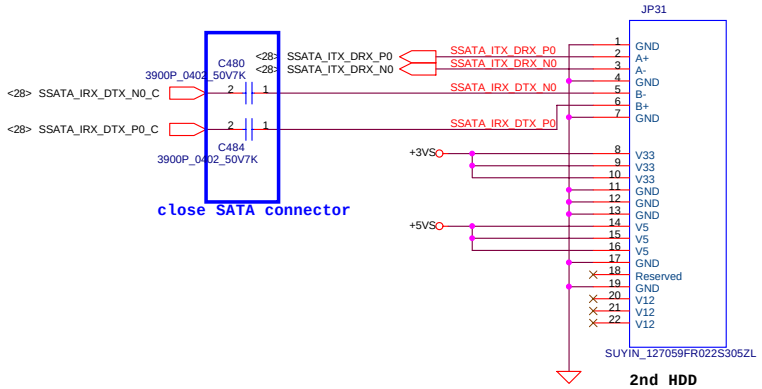




**Main HDD**

**Need update symbol**

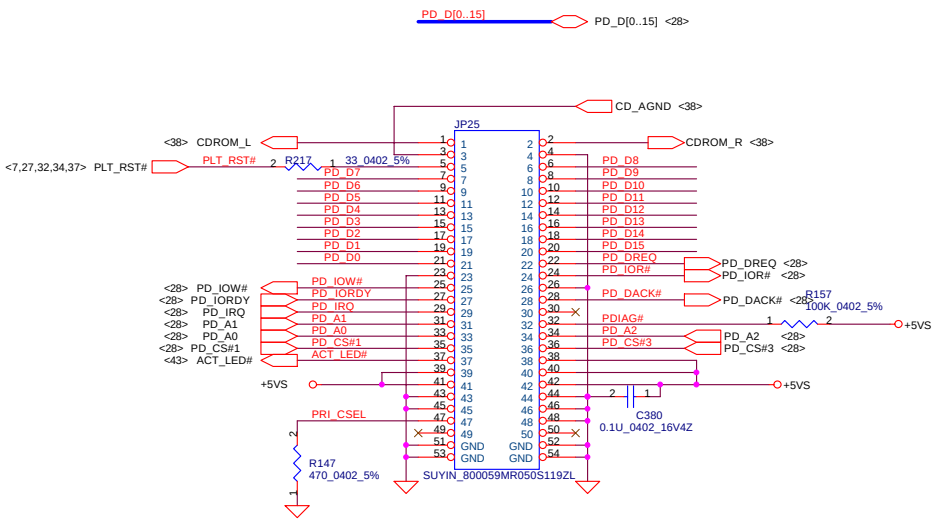
**Main SATA +5V Default**



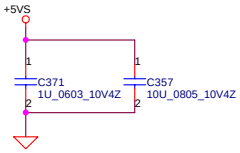

**2nd HDD**

**Need update symbol**

**Main SATA +5V Default**




***CD-ROM Connector***

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**Compal Electronics, Inc.**

Title: **HDD & CDROM**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 31 of 60

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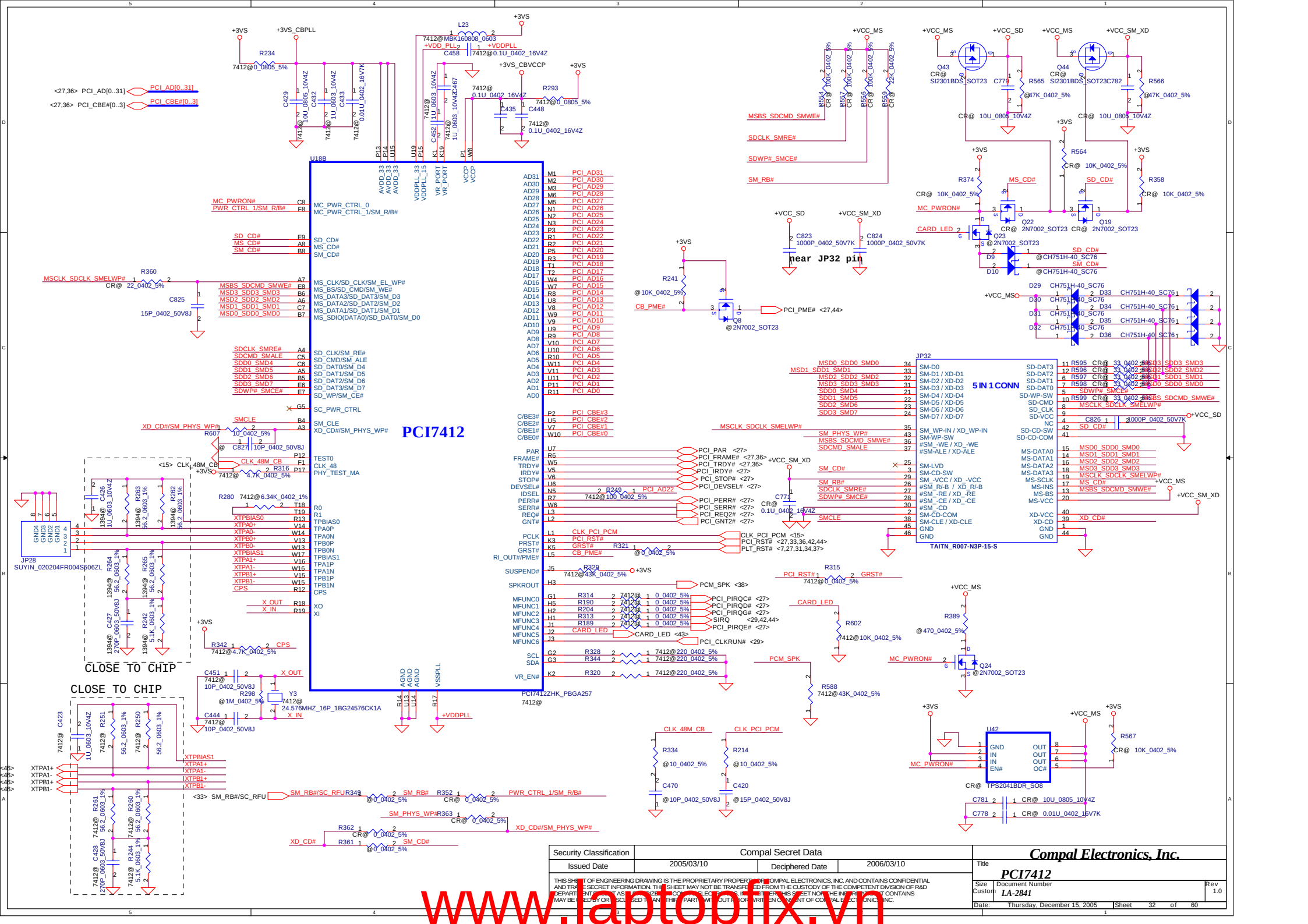


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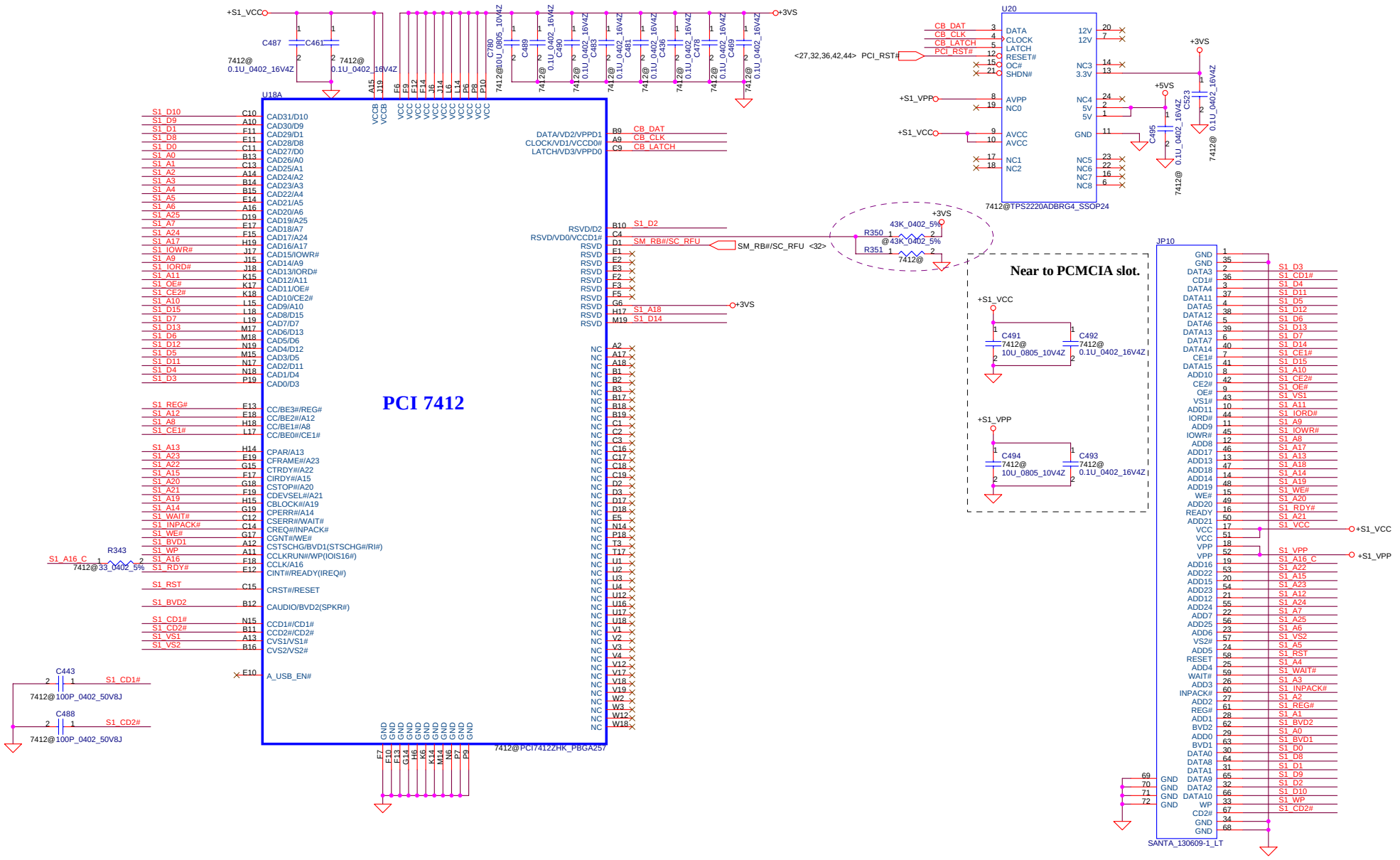
# CardBus Power Switch

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|---|---|---|---|
| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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Compal Electronics, Inc.

Title: PCI7412

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 33 of 60

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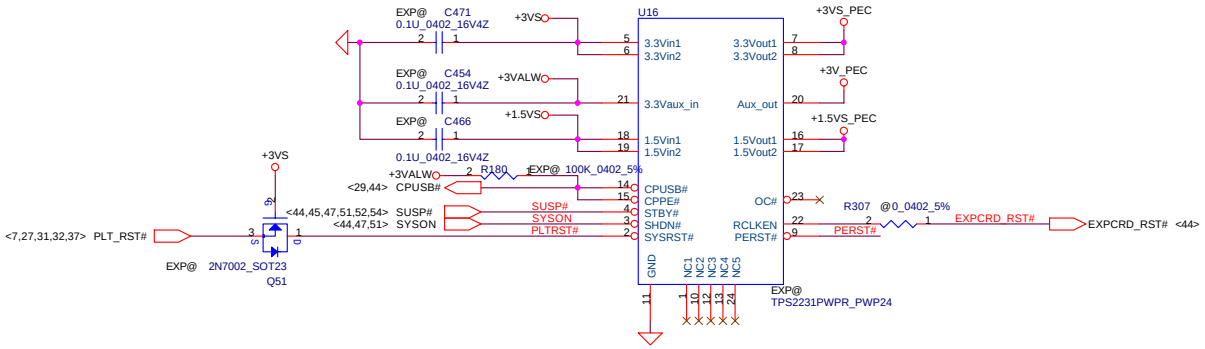
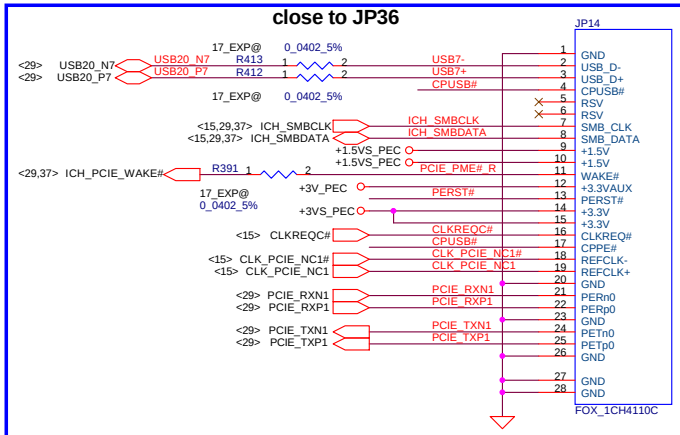
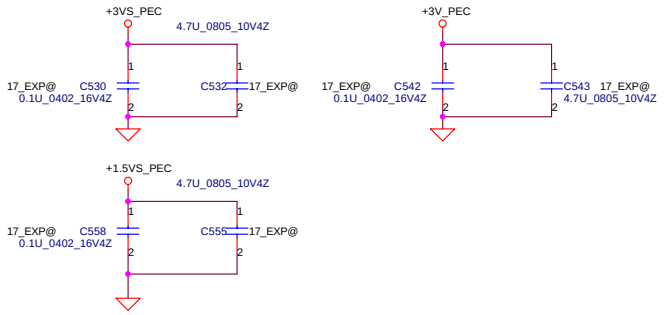
# Express Card Power Switch



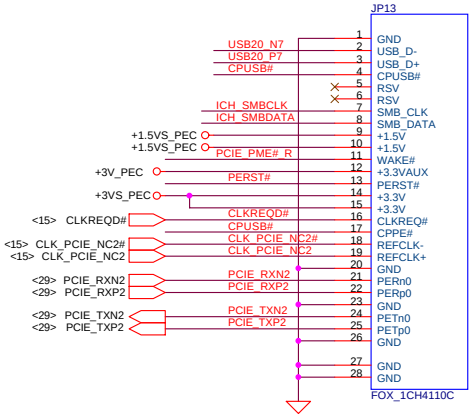

## close to JP36



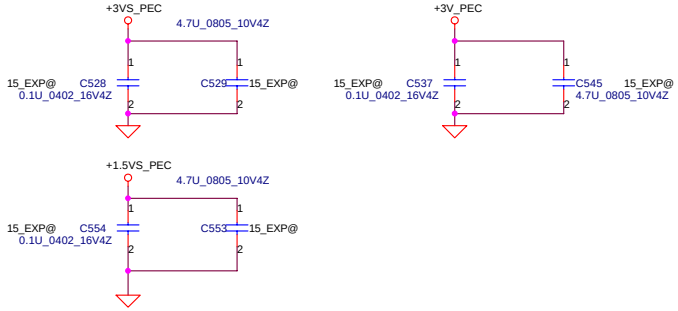

## Near to Express Card slot. 17




## JP13




## Near to Express Card slot. 15.4




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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**Compal Electronics, Inc.**

Title: **Express Card**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 34 of 60

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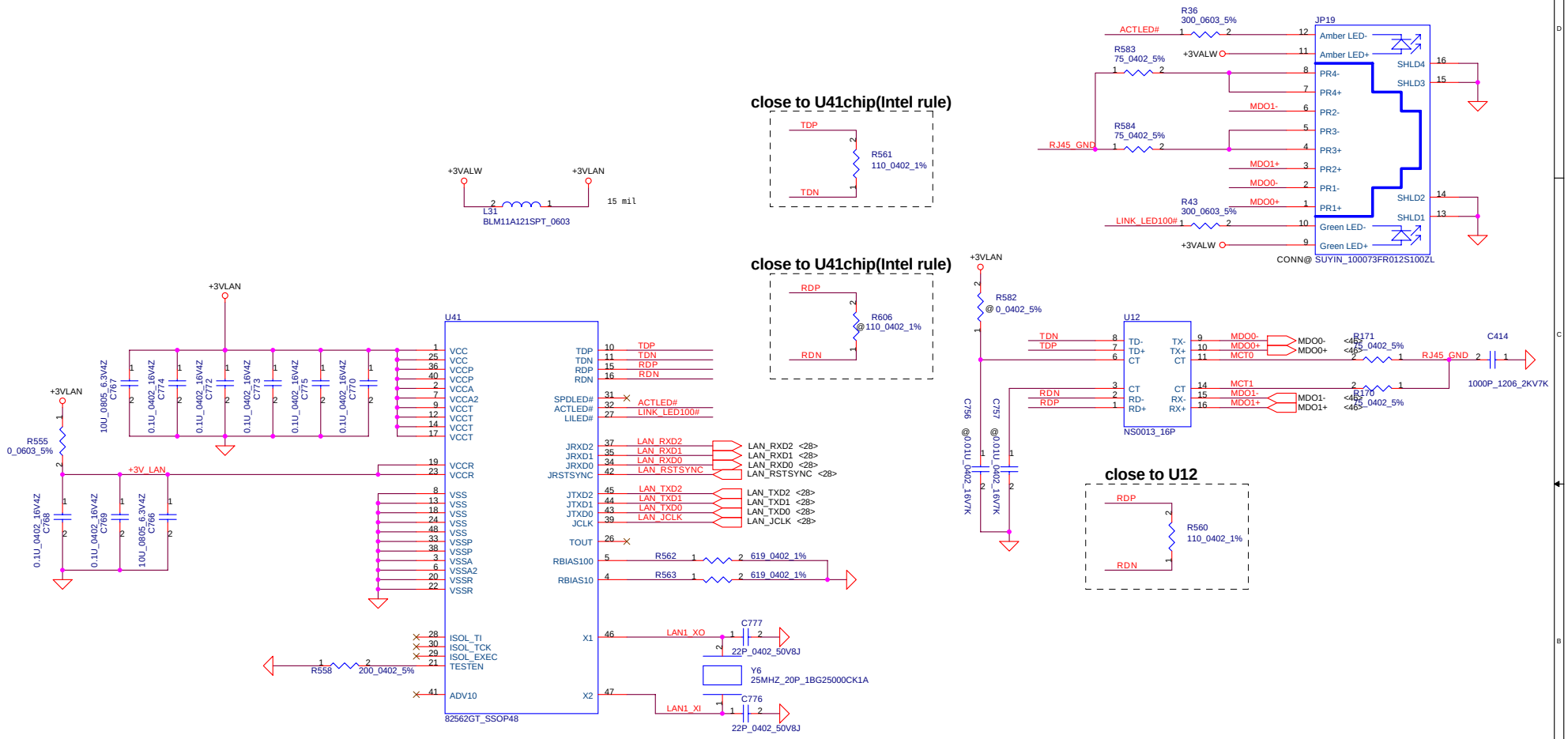


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**Compal Electronics, Inc.**

Title: **82562EZ LAN**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 35 of 60

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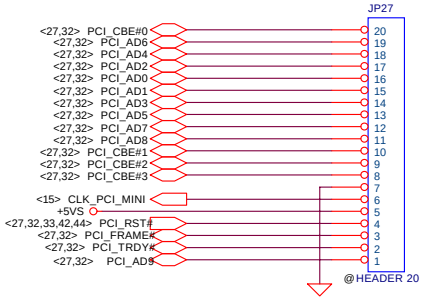
# Port 80 Debug Card Connector

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**Compal Electronics, Inc.**

Title: **Debug port**

Size: Custom | Document Number: *LA-2841* | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 36 of 60

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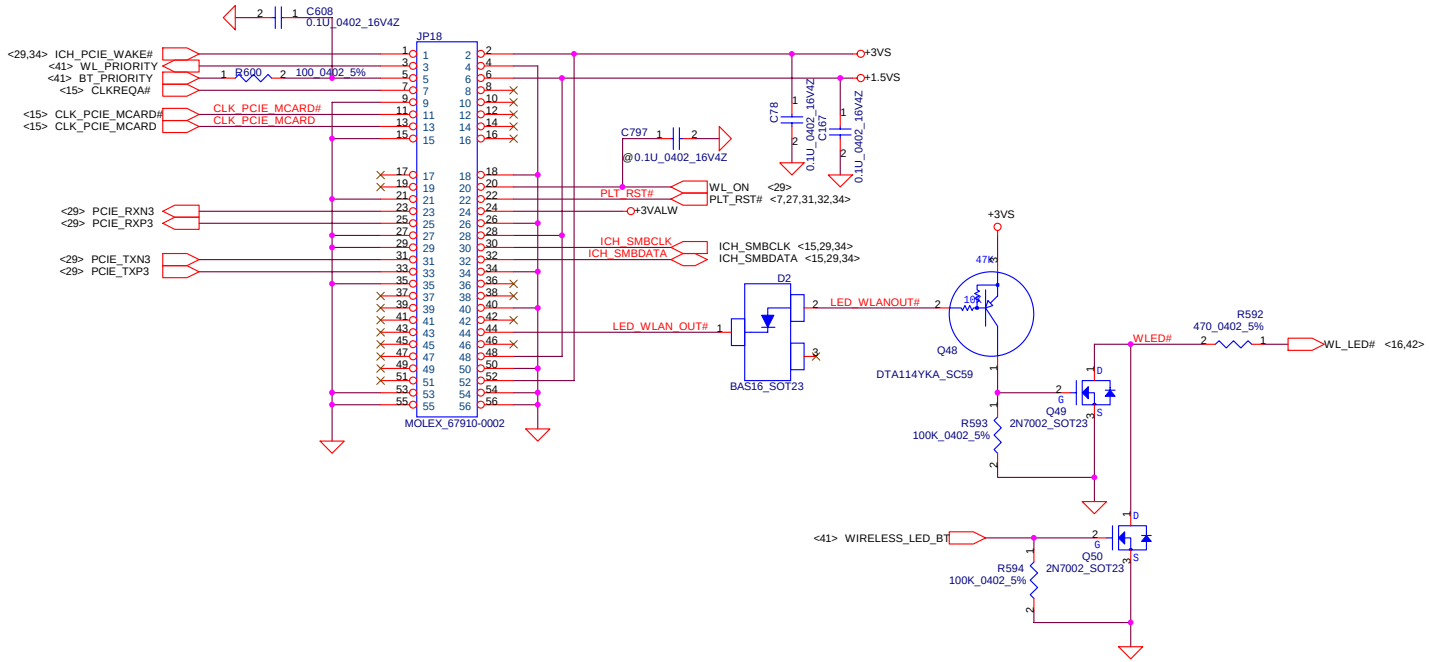
# Mini-Express Card(Slot 1-WLAN)

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|---|---|---|---|
| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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**Compal Electronics, Inc.**

Title: **Mini Card**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 37 of 60

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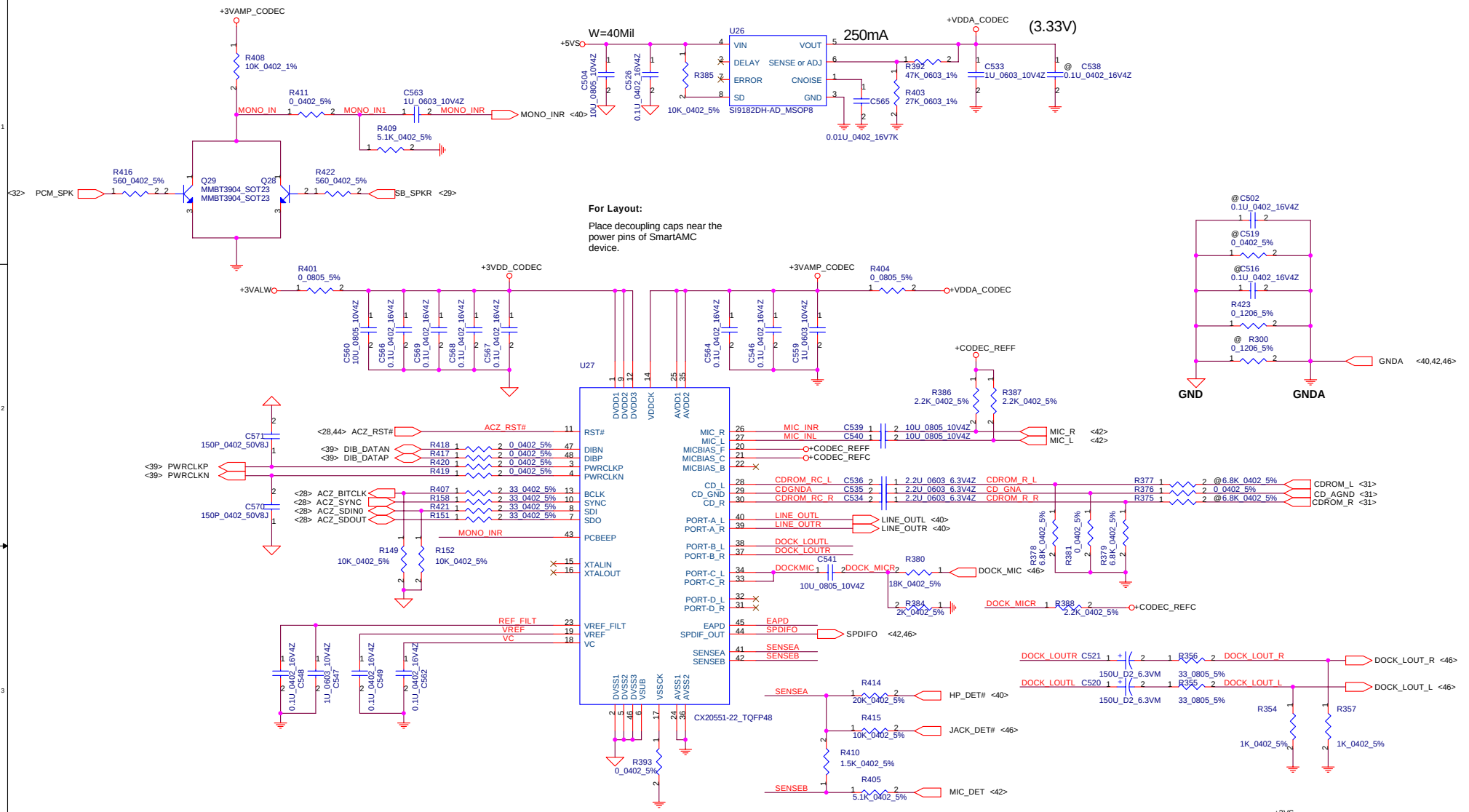


| HP_DET# | JACK_DET# | PORT-A | PORT-B | EQ |
|---|---|---|---|---|
| 0 | 0 | ON | OFF | Disable |
| 0 | NC | ON | OFF | Disable |
| NC | 0 | OFF | ON | Disable |
| NC | NC | ON | OFF | Enable |

| MIC_DET | PORT-C | PORT-F |
|---|---|---|
| 0 | ON | OFF |
| NC | OFF | ON |

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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Compal Electronics, Inc.

Title: AMOM_codec

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 38 of 60

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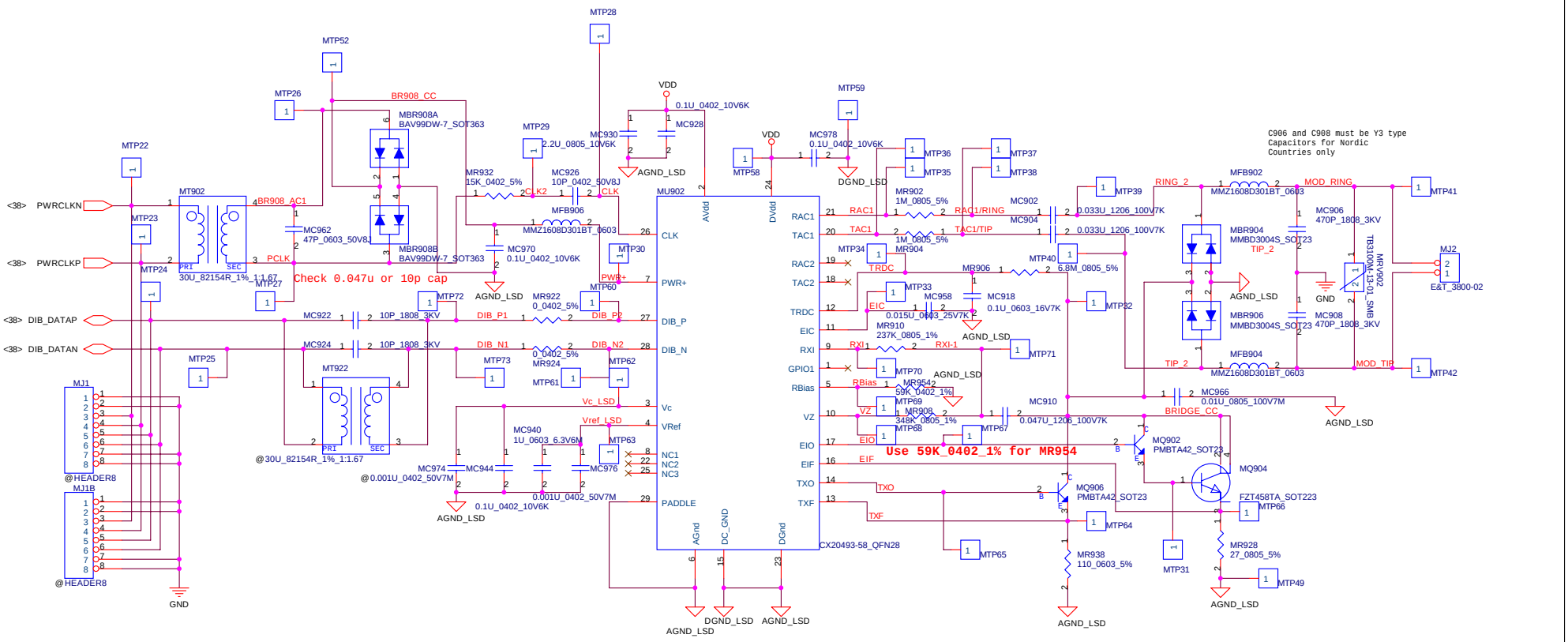


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**Compal Electronics, Inc.**

Title: **AMOM_modem**

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|---|---|---|
| Custom | LA-2841 | 1.0 |

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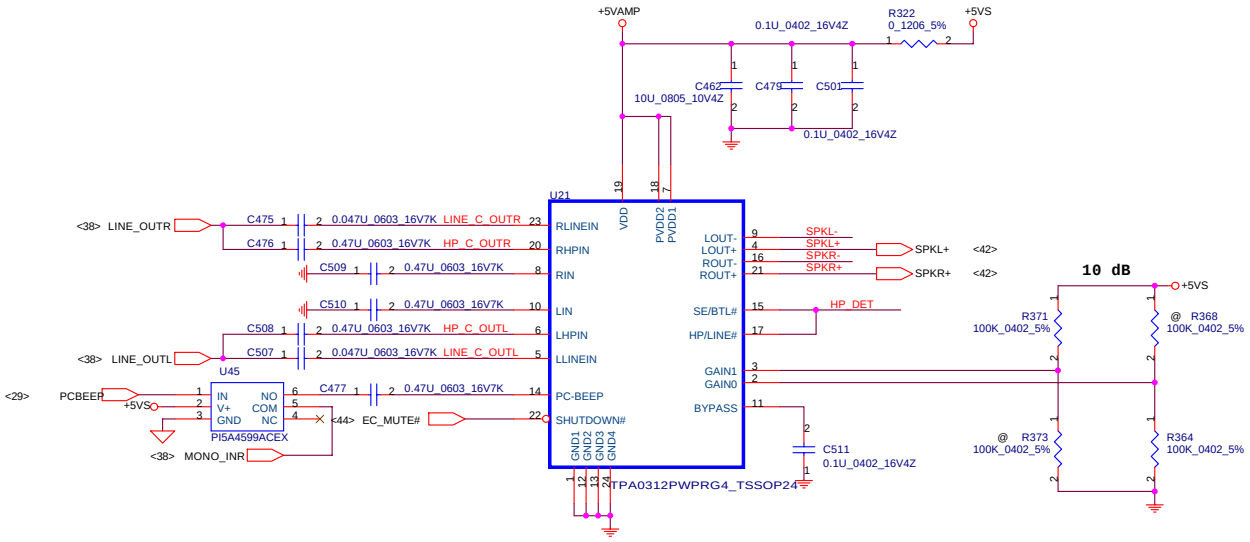
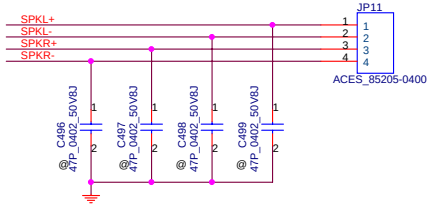
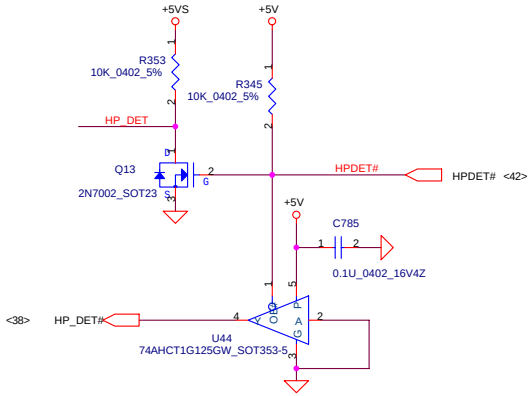



## HEADPHONE OUT/LINE OUT

| Gain Settings | | | |
|---|---|---|---|
| GAIN0 | GAIN1 | SE/BTL# | Av(inv) |
| 0 | 0 | 0 | 6 dB |
| 0 | 1 | 0 | * 10 dB |
| 1 | 0 | 0 | 15.6 dB |
| 1 | 1 | 0 | 21.6 dB |
| X | X | 1 | 4.1 dB |

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**Compal Electronics, Inc.**

Title: **AMP & Audio Jack**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

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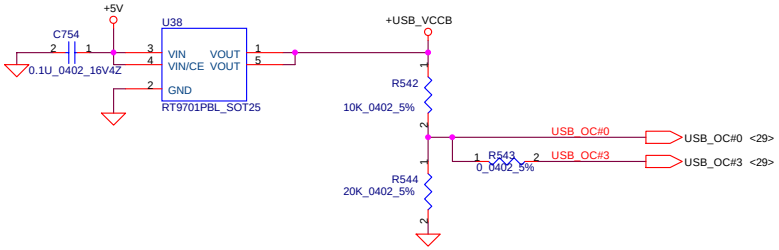
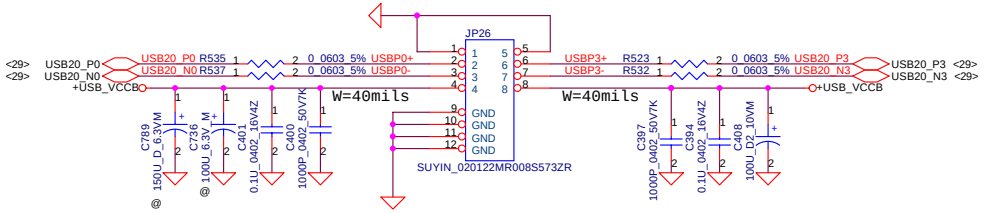
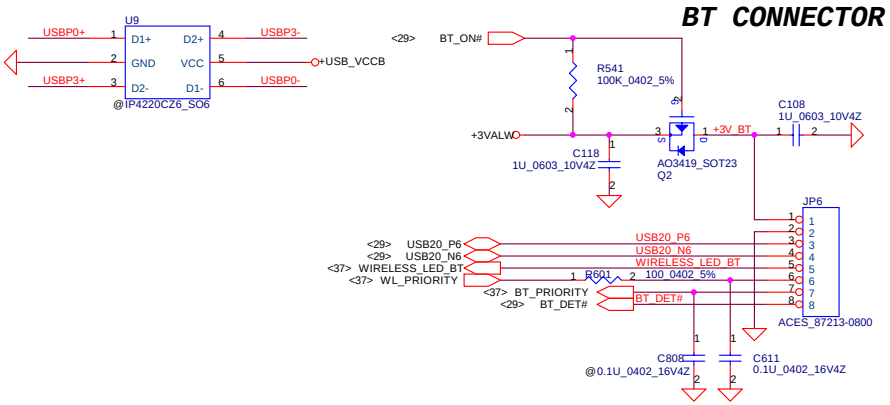



## USB CONNECTOR (Left side)




## BT CONNECTOR

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**Compal Electronics, Inc.**

Title: **Bluetooth & USB CONN.**

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-2841 | 1.0 |

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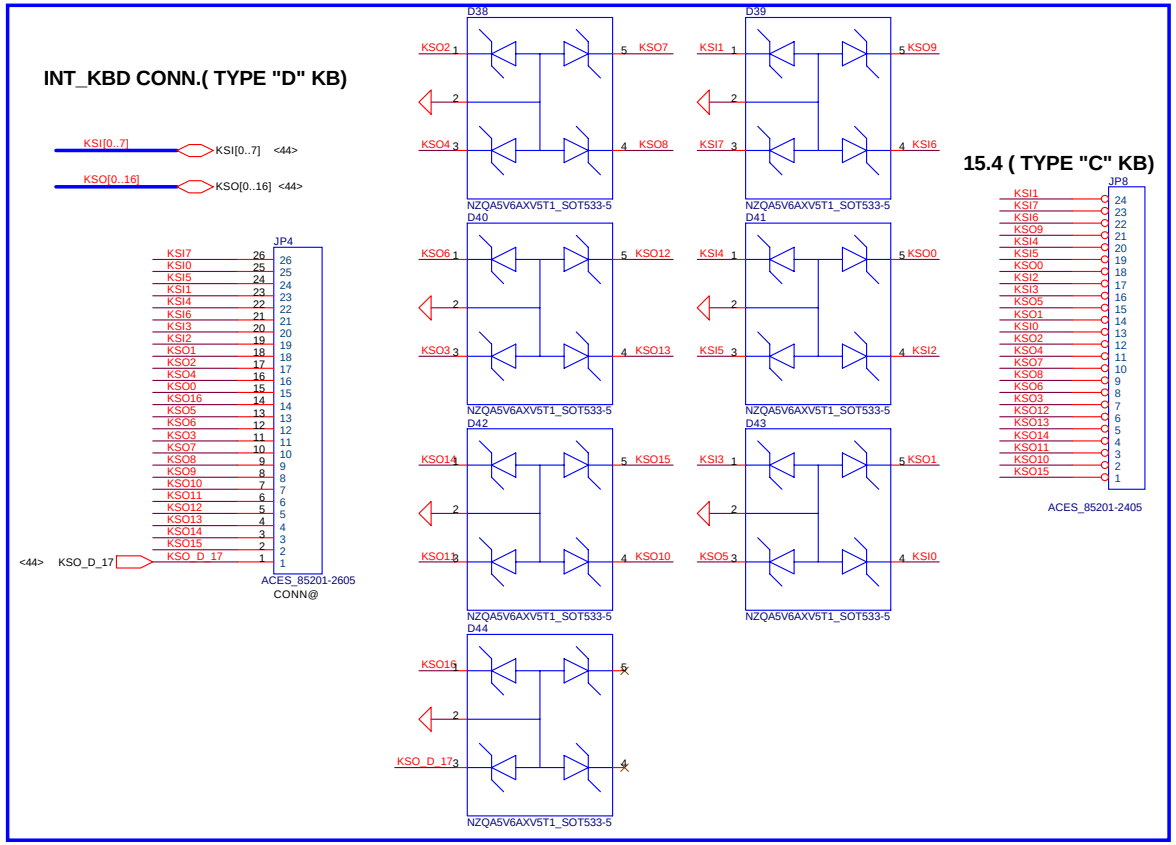


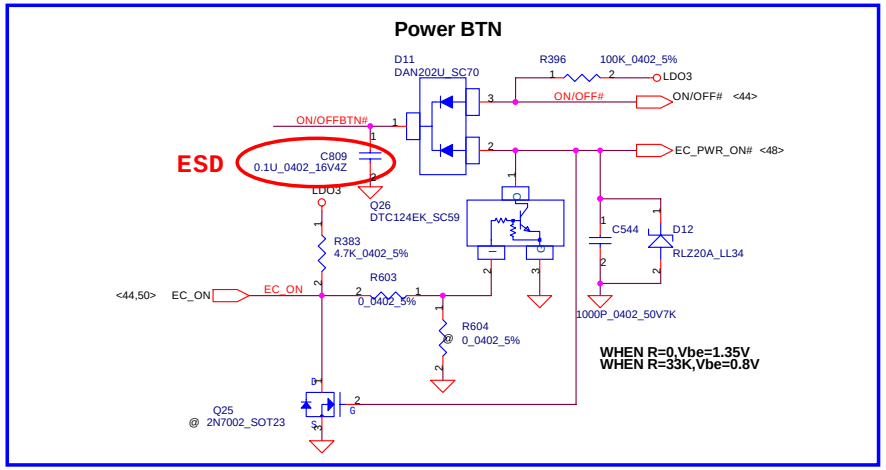


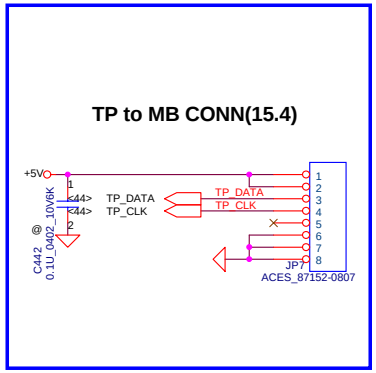


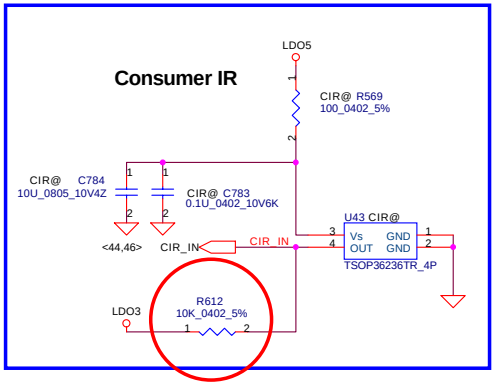


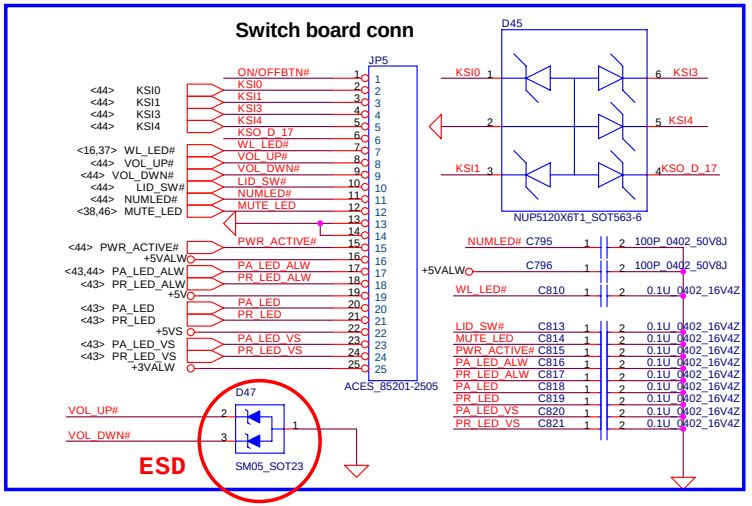


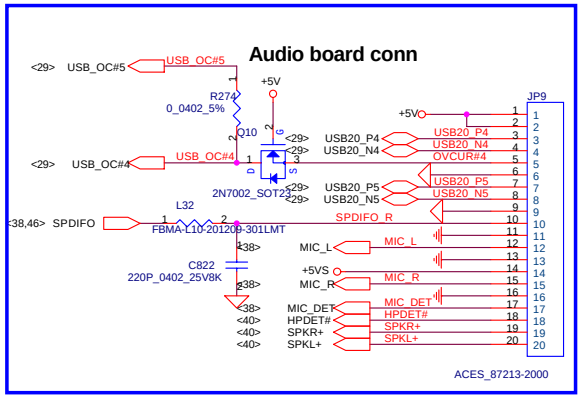


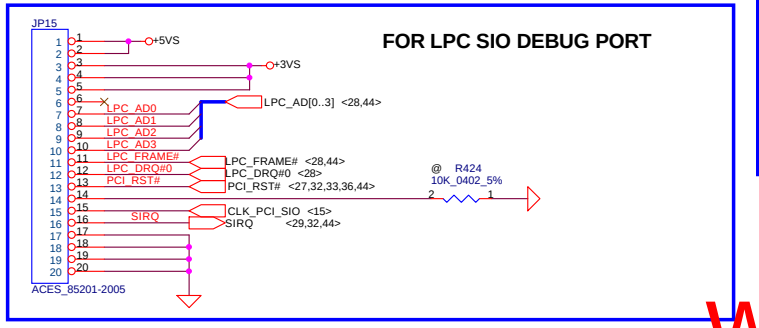


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Compal Electronics, Inc.

Title: KBD,ON/OFF,T/P,LED/B,DEBUG

Size: Custom | Document Number: LA-2841 | Rev: 1.0

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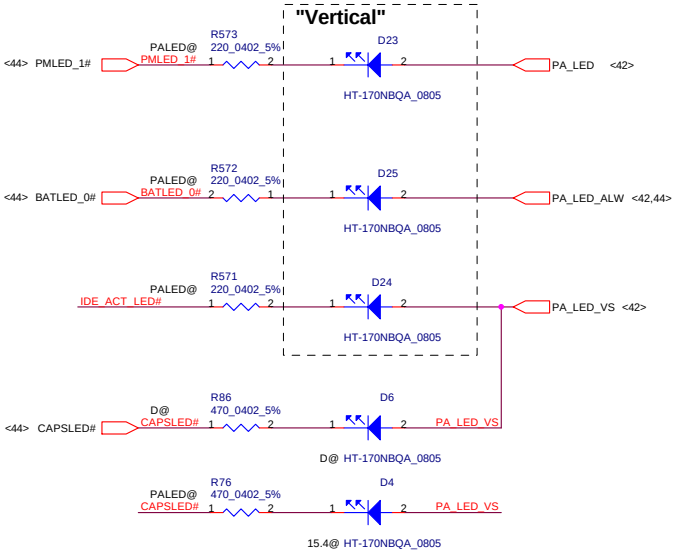
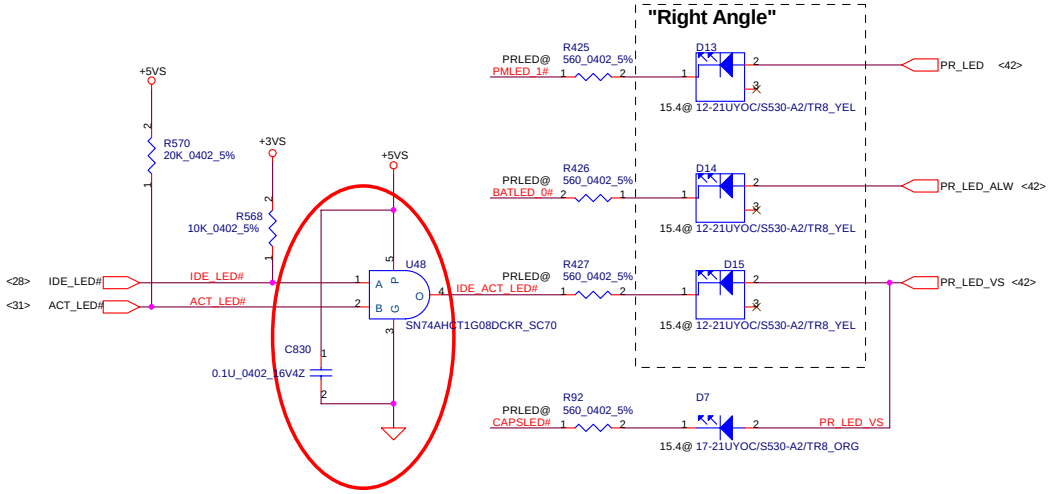
## For PA

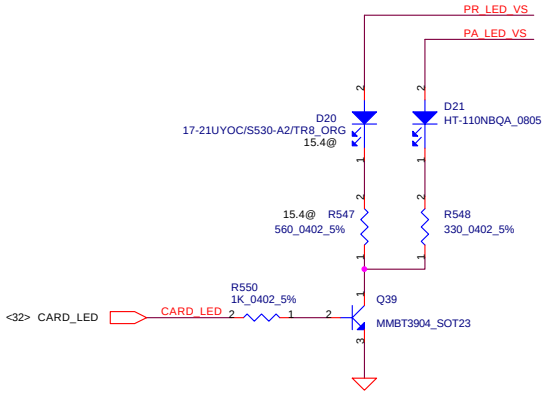
### FOR POWER BUTTON BACKLIGHT SYSTEM POWER




## For PR

### FOR POWER BUTTON BACKLIGHT SYSTEM POWER

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**Compal Electronics, Inc.**

Title: **INDICATE LED**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

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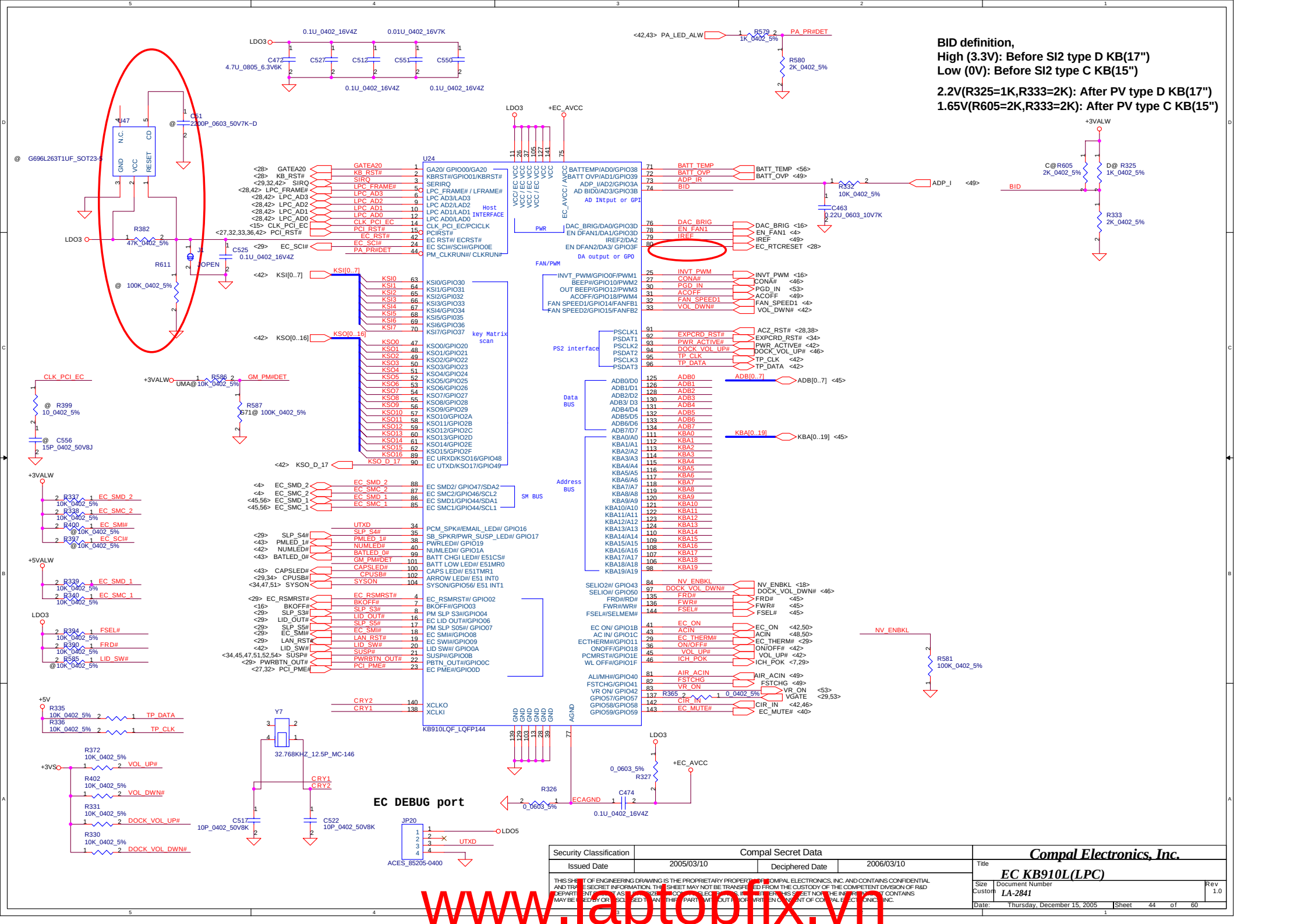
BID definition,
High (3.3V): Before SI2 type D KB(17")
Low (0V): Before SI2 type C KB(15")
2.2V(R325=1K,R333=2K): After PV type D KB(17")
1.65V(R605=2K,R333=2K): After PV type C KB(15")
U24
KB910LQF_LQFP144
G696L263T1UF_SOT23-6
EC DEBUG port
JP20
ACES_85205-0400
Y7
32.768KHZ_12.5P_MC-146
Compal Electronics, Inc.
EC KB910L(LPC)
Security Classification
Compal Secret Data
Issued Date
2005/03/10
Deciphered Date
2006/03/10
Size Custom
Document Number
LA-2841
Rev 1.0
Date: Thursday, December 15, 2005
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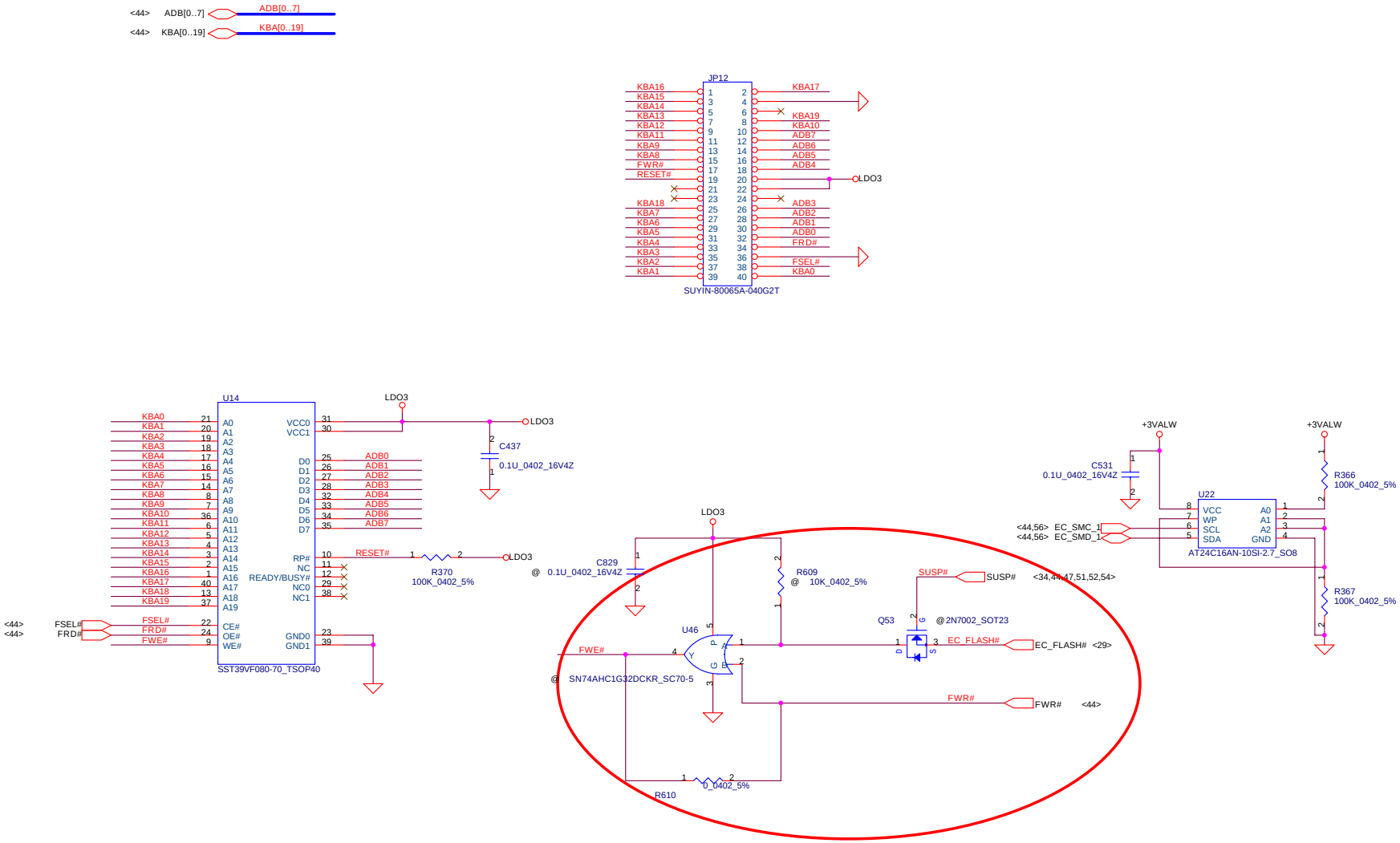


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**Compal Electronics, Inc.**

Title: **BIOS & EC I/O Port**

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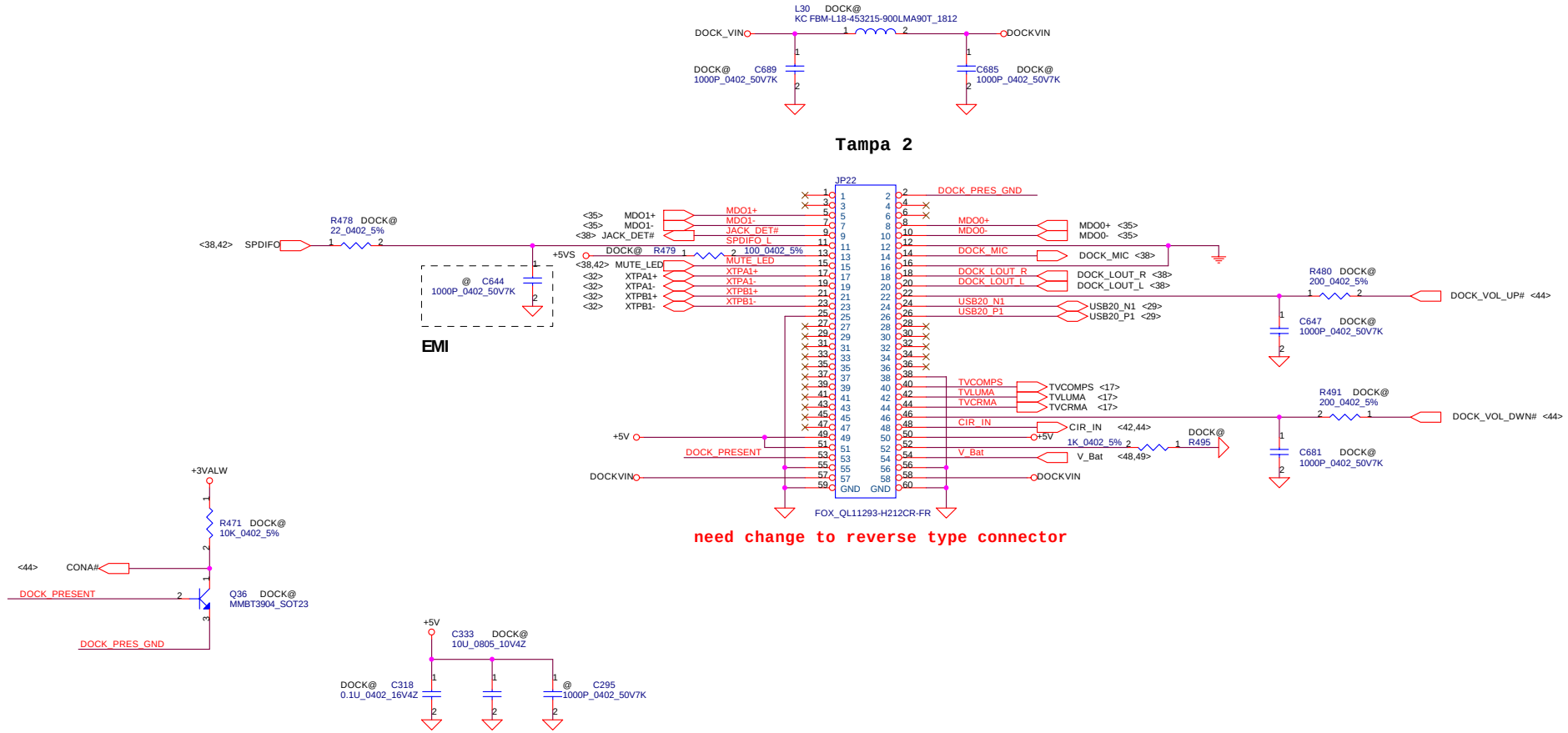


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|---|---|---|---|
| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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**Compal Electronics, Inc.**

Title: **DOCK CONN**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

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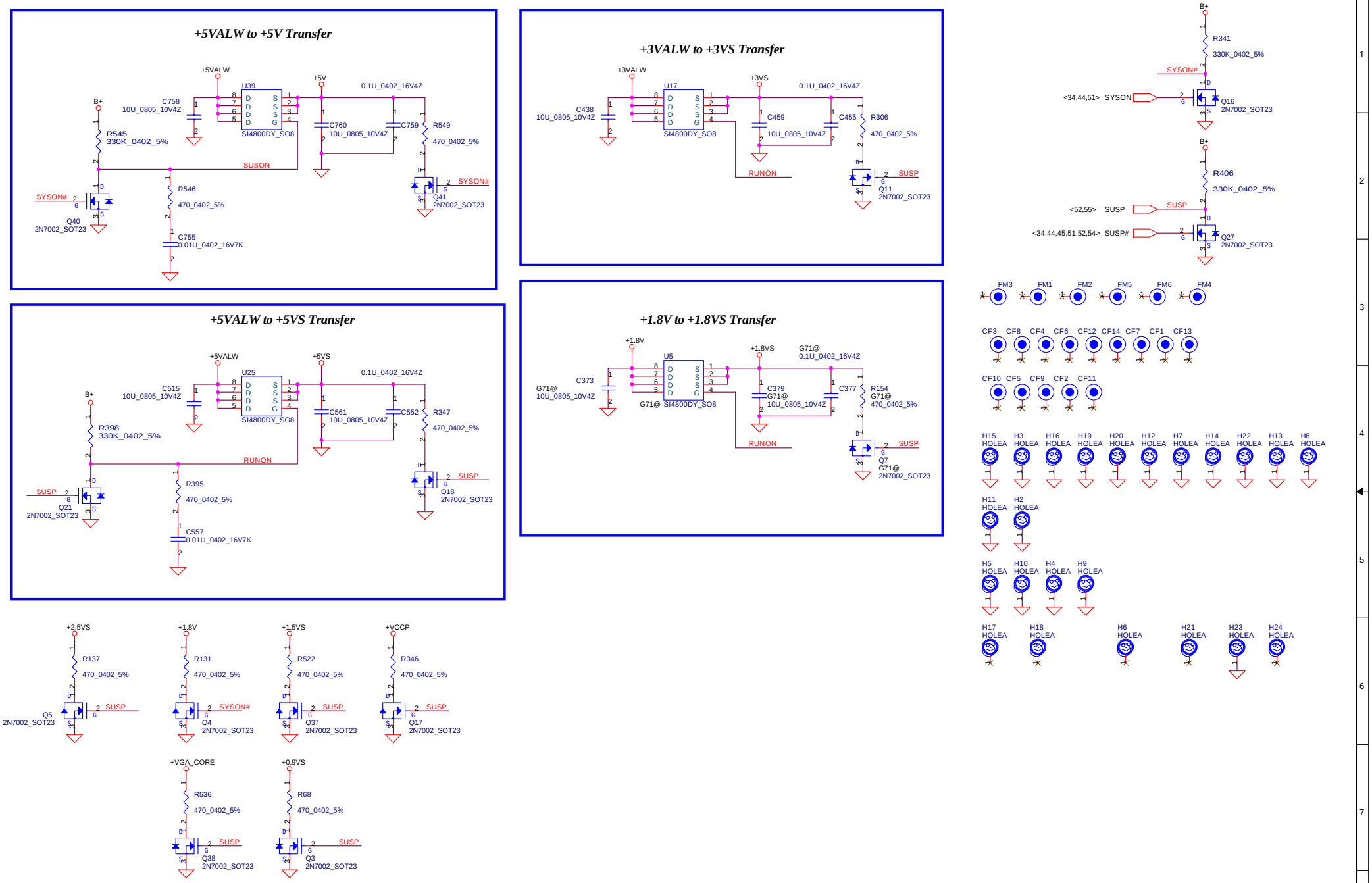


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|---|---|---|---|
| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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**Compal Electronics, Inc.**

Title: **DC/DC Circuit**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 47 of 60

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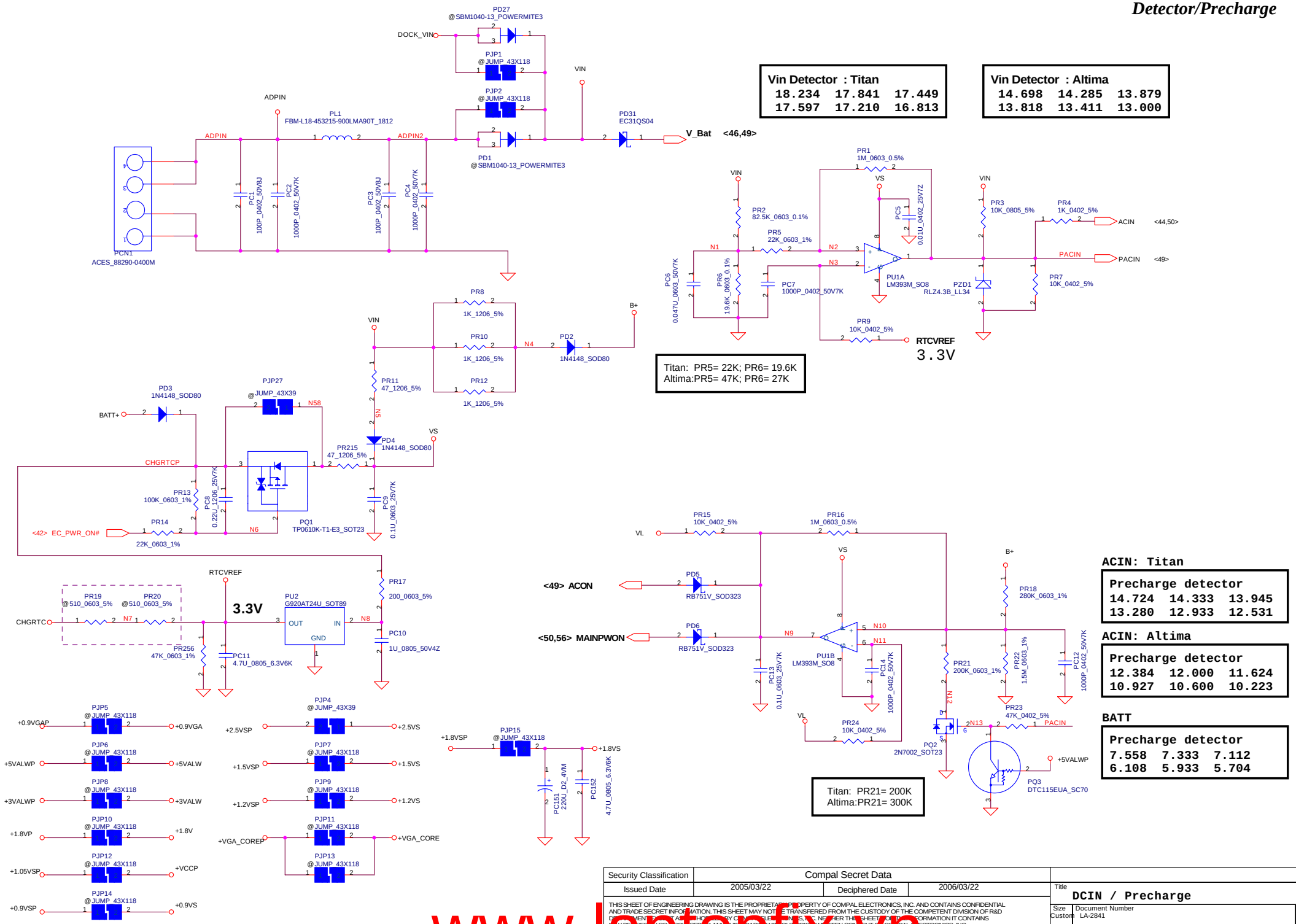
# Detector/Precharge




**Vin Detector : Titan**

| | | |
|---|---|---|
| 18.234 | 17.841 | 17.449 |
| 17.597 | 17.210 | 16.813 |

**Vin Detector : Altima**

| | | |
|---|---|---|
| 14.698 | 14.285 | 13.879 |
| 13.818 | 13.411 | 13.000 |

Titan: PR5= 22K; PR6= 19.6K
Altima:PR5= 47K; PR6= 27K

Titan: PR21= 200K
Altima:PR21= 300K

**ACIN: Titan**

**Precharge detector**

| | | |
|---|---|---|
| 14.724 | 14.333 | 13.945 |
| 13.280 | 12.933 | 12.531 |

**ACIN: Altima**

**Precharge detector**

| | | |
|---|---|---|
| 12.384 | 12.000 | 11.624 |
| 10.927 | 10.600 | 10.223 |

**BATT**

**Precharge detector**

| | | |
|---|---|---|
| 7.558 | 7.333 | 7.112 |
| 6.108 | 5.933 | 5.704 |

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|---|---|---|---|
| Issued Date | 2005/03/22 | Deciphered Date | 2006/03/22 |

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Title: **DCIN / Precharge**

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-2841 | 1.0 |

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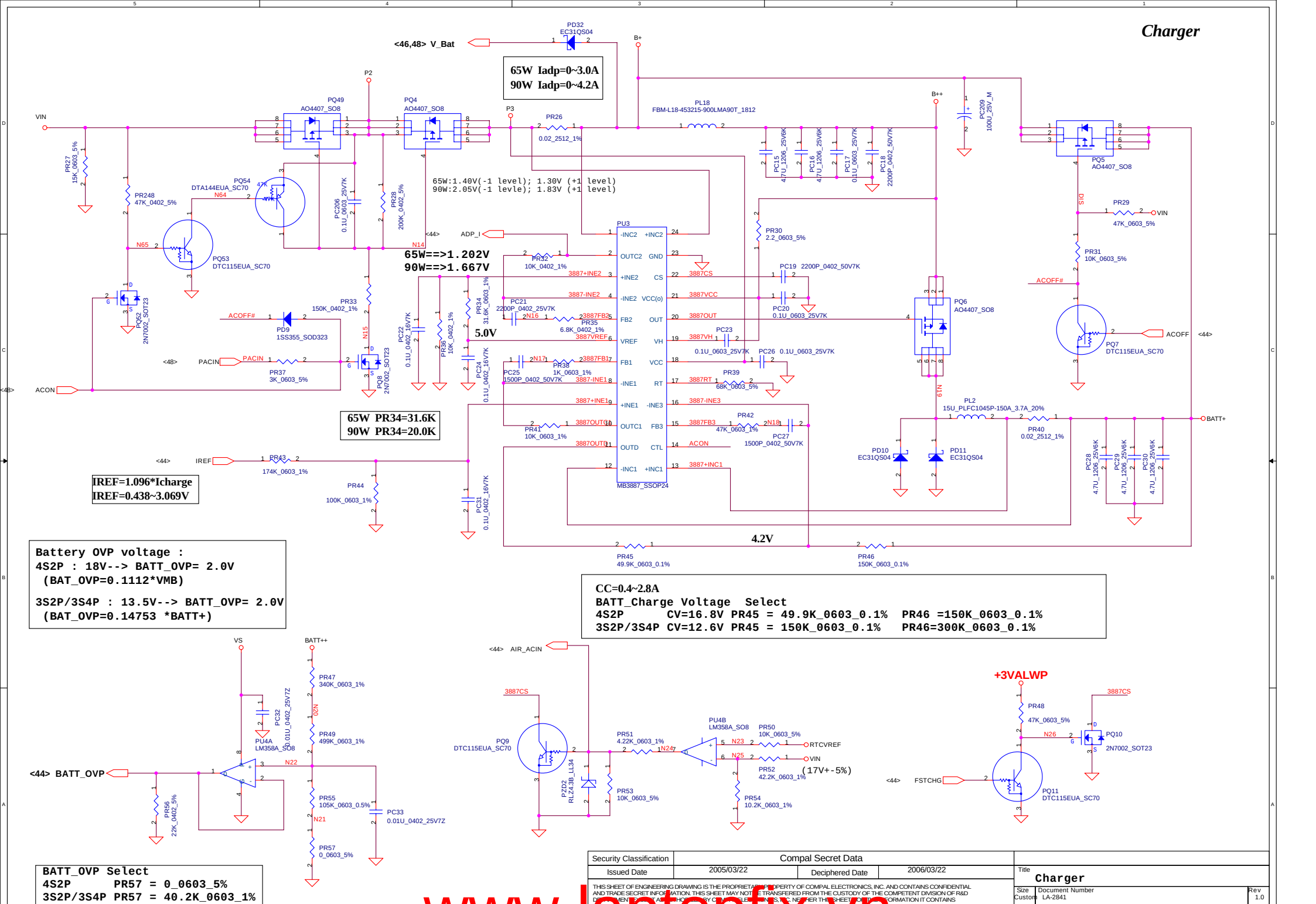
# Charger

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|---|---|---|---|
| Issued Date | 2005/03/22 | Deciphered Date | 2006/03/22 |

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Title: Charger

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 49 of 60

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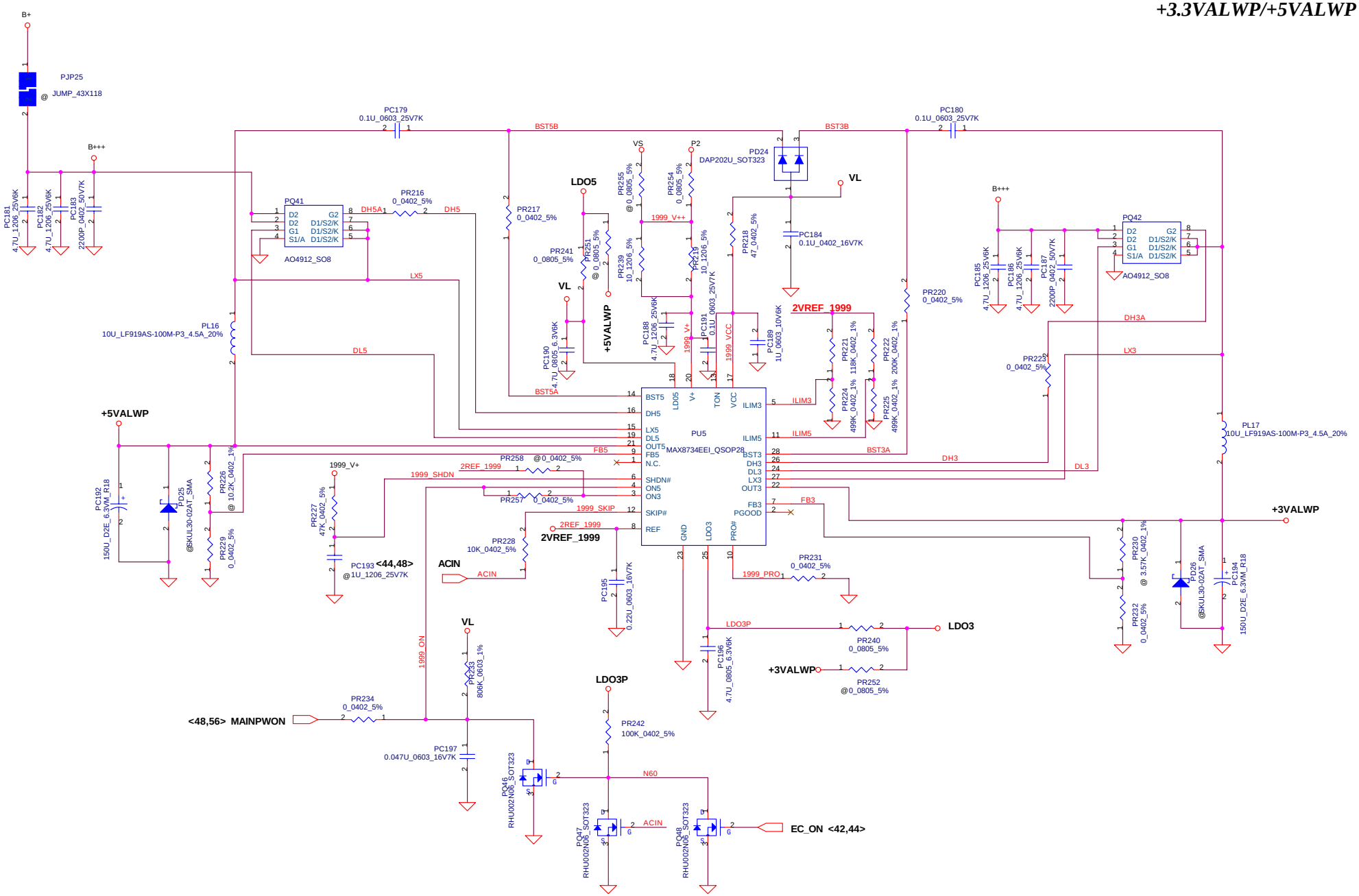
# +3.3VALWP/+5VALWP




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2005/03/22 | Deciphered Date | 2006/03/22 |

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Title: +3V/+5V

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 50 of 60

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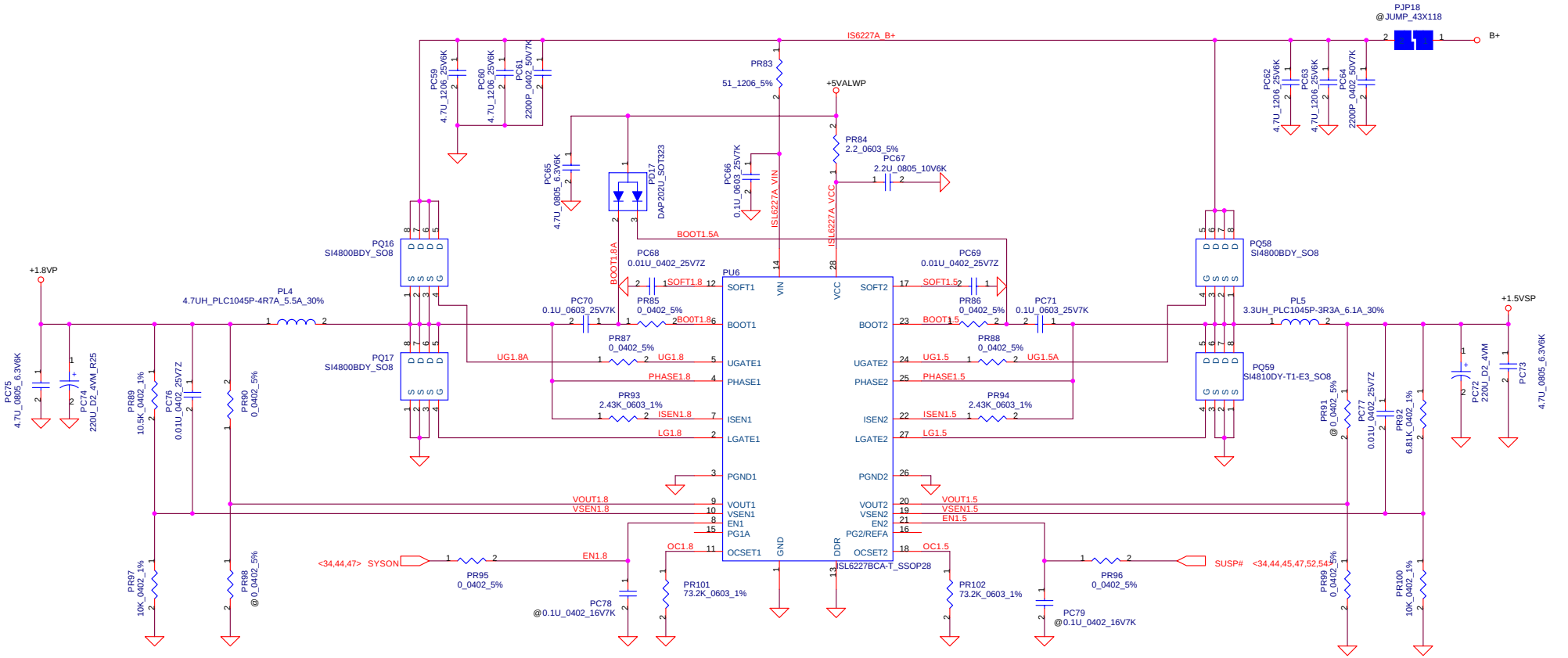
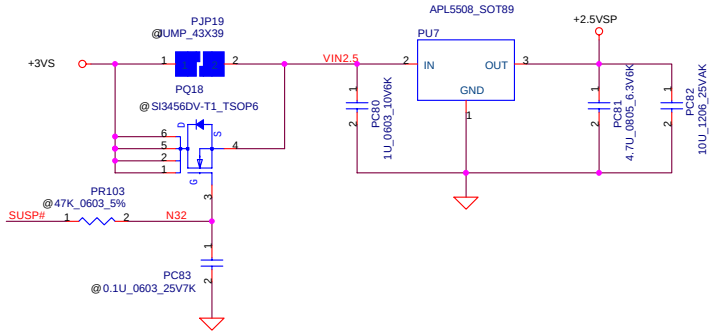
# +1.8VP/+1.5VALWP/+2.5VS




(400mA,40mils ,Via NO.= 1)

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|---|---|---|---|
| Issued Date | 2005/03/22 | Deciphered Date | 2006/03/22 |

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Title: **1.8V/1.5V/2.5V**

Size: Custom | Document Number: LA-2841 | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 51 of 60

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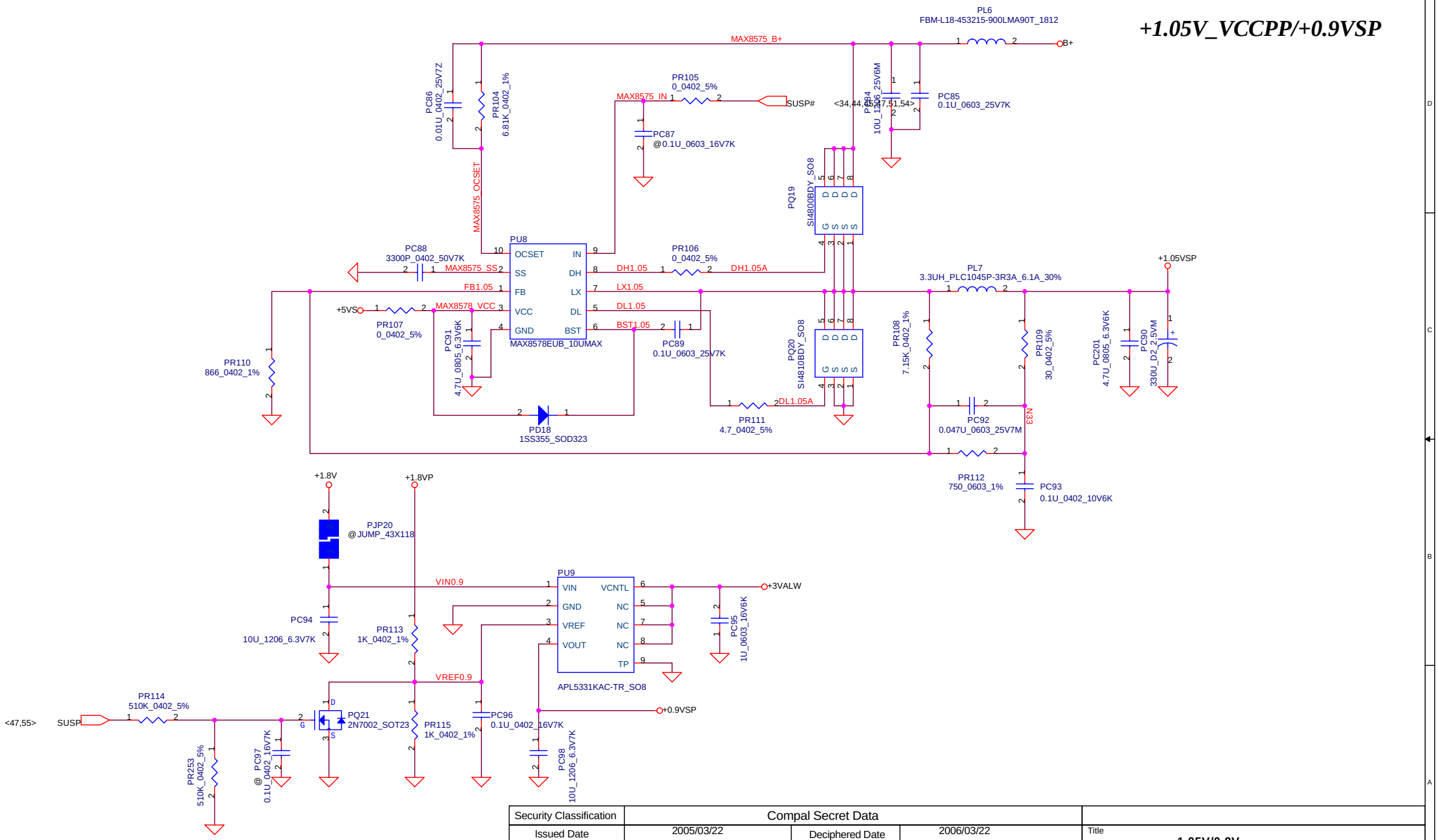
# +1.05V_VCCPP/+0.9VSP




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2005/03/22 | Deciphered Date | 2006/03/22 |

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Title: **1.05V/0.9V**

Size | Document Number | Rev 1.0

Date: Thursday, December 15, 2005 | Sheet 52 of 60

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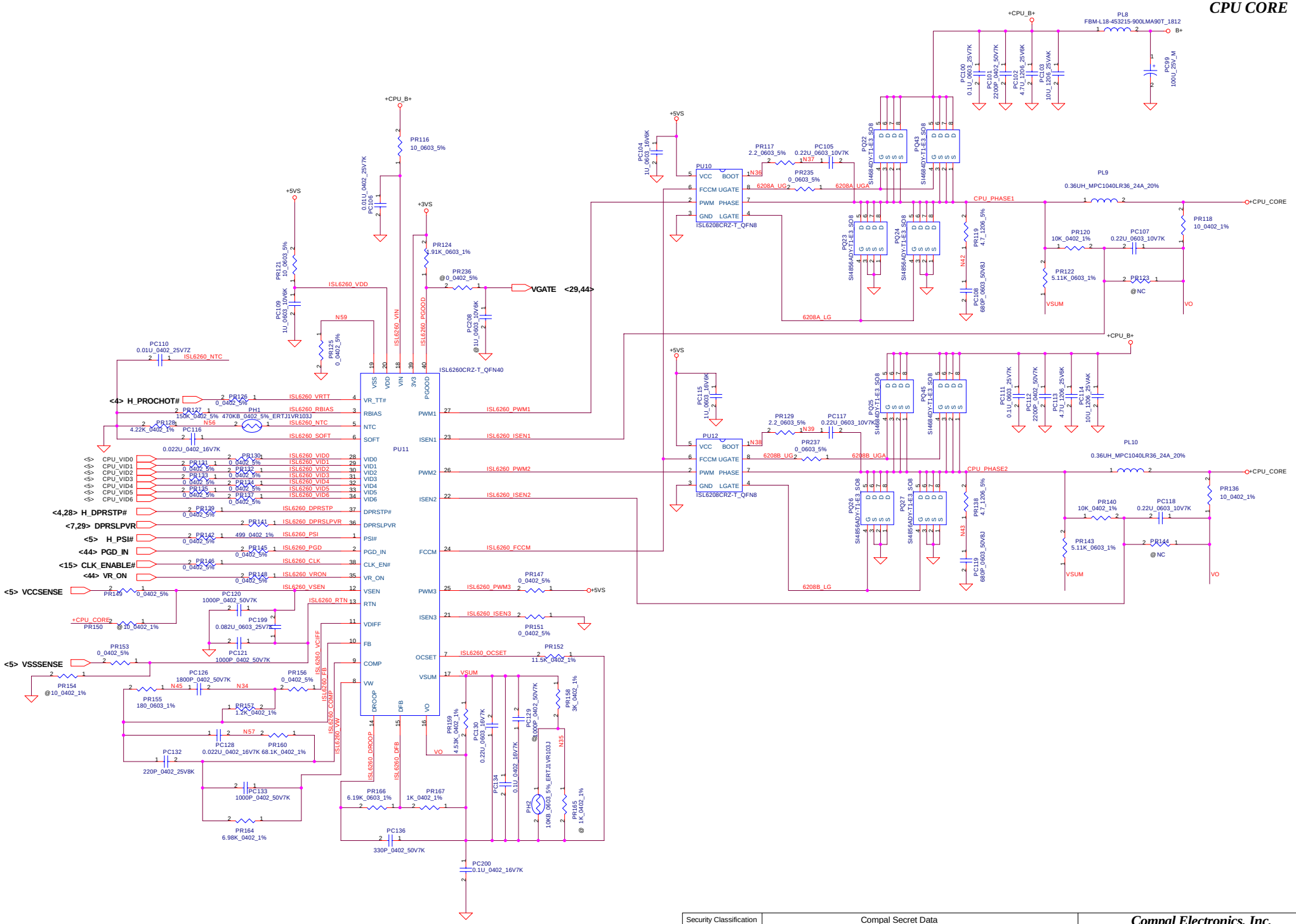
# CPU CORE

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|---|---|---|---|
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**Compal Electronics, Inc.**

Title: CPU_CORE

Size: C | Document Number | Rev: 1.0

Date: Thursday, December 15, 2005 | Sheet 53 of 60

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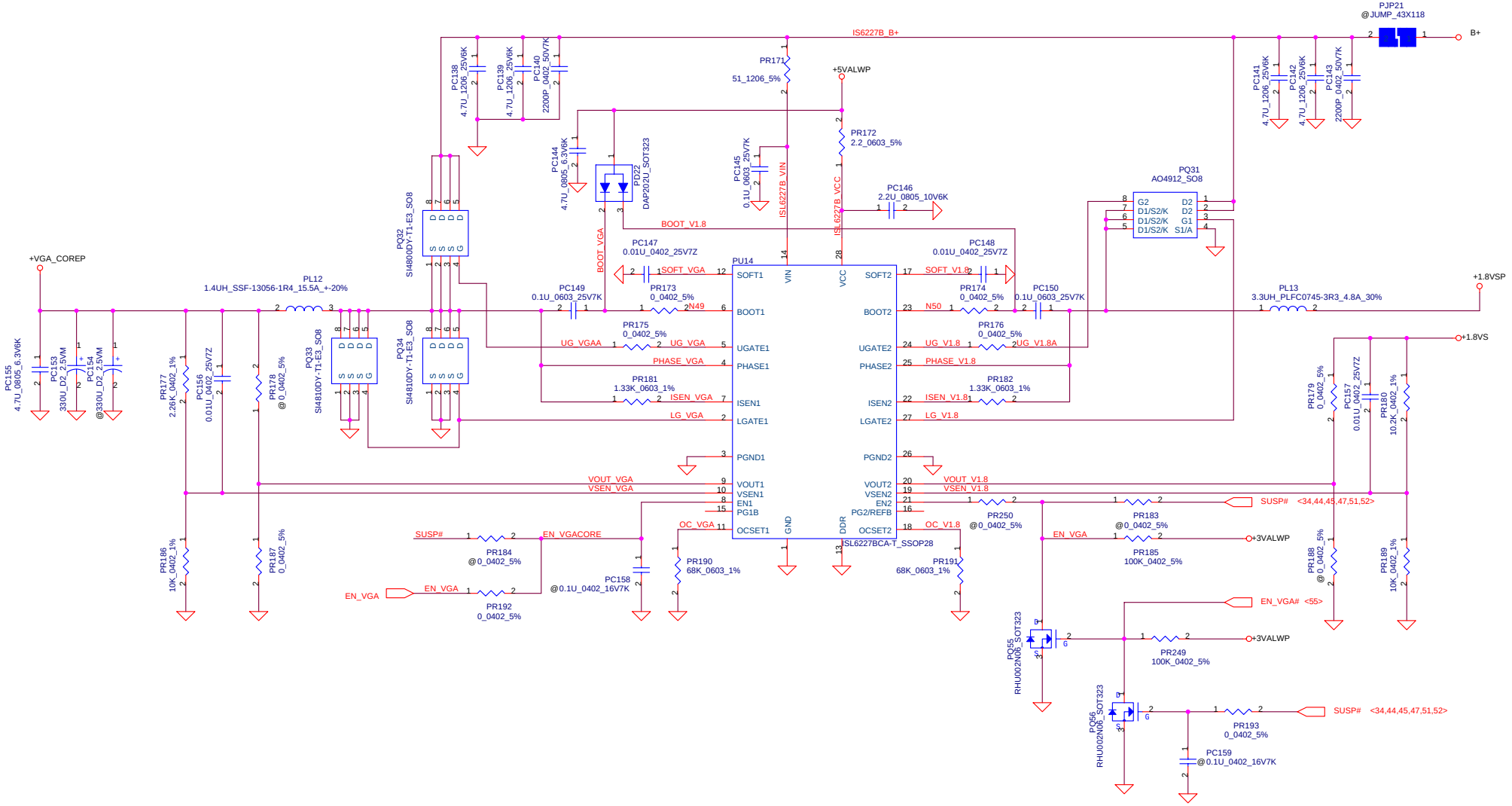
# +VGA_COREP/+1.8VSP

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|---|---|---|---|
| Issued Date | 2005/03/22 | Deciphered Date | 2006/03/22 |

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Title

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-2841 | 1.0 |

Date: Thursday, December 15, 2005 Sheet 54 of 60

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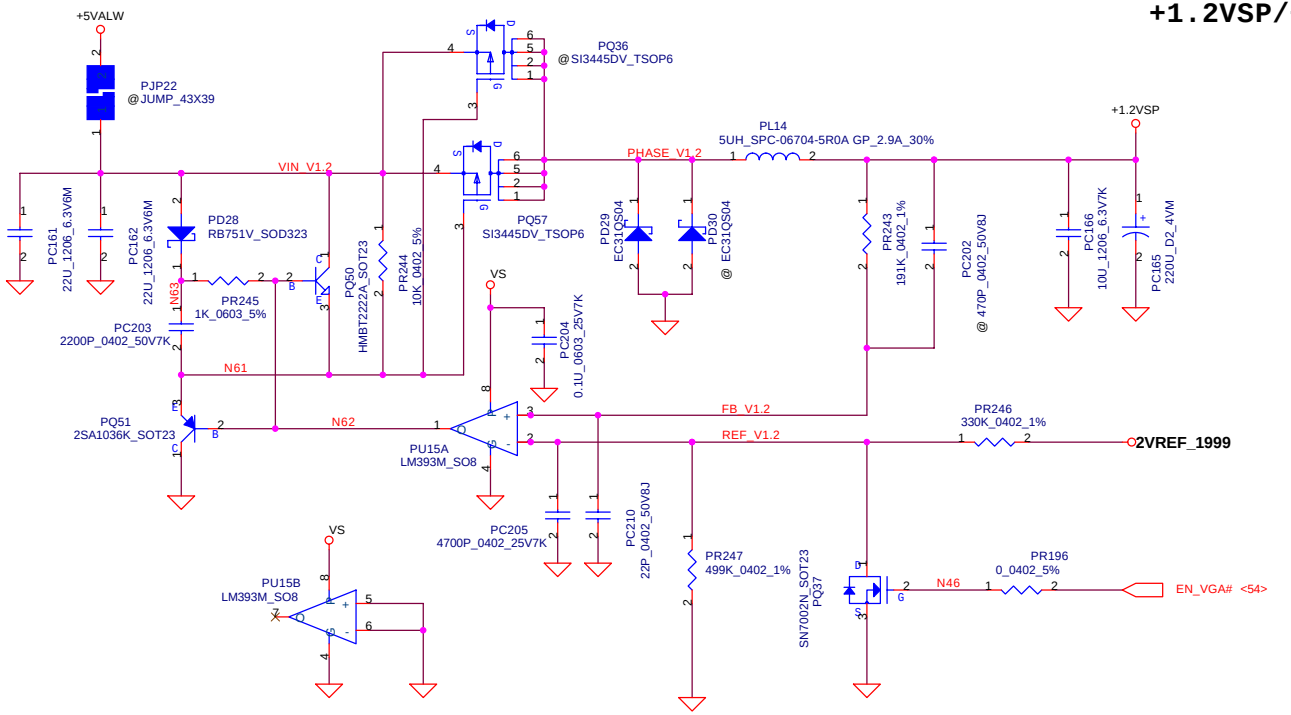
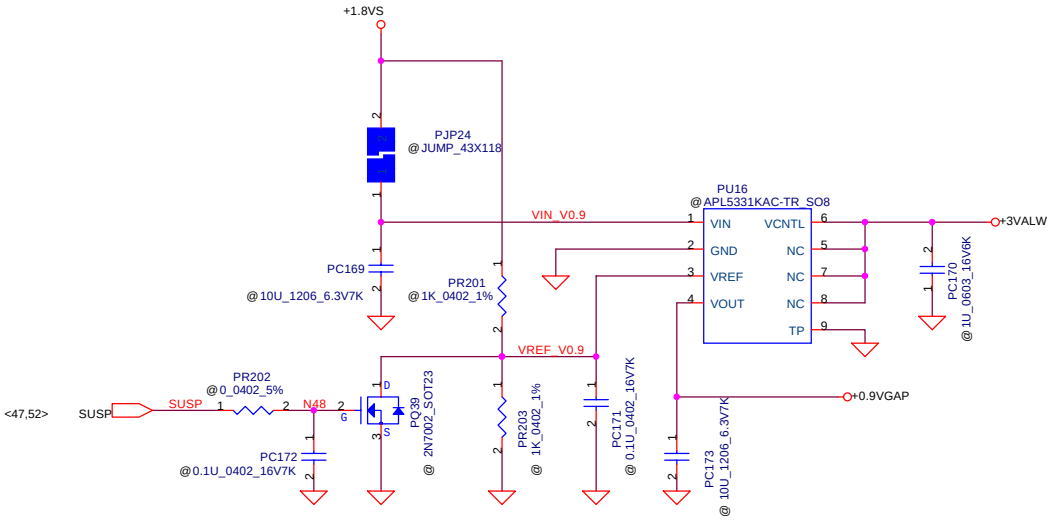
# +1.2VSP/+0.9VSP




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2005/03/2 | Deciphered Date | 2006/03/22 |

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**Compal Electronics, Inc.**

Title: **VGA1.2V/VGA0.9V**

Size: Custom | Document Number | Rev 1.0

Date: Thursday, December 15, 2005 | Sheet 55 of 60

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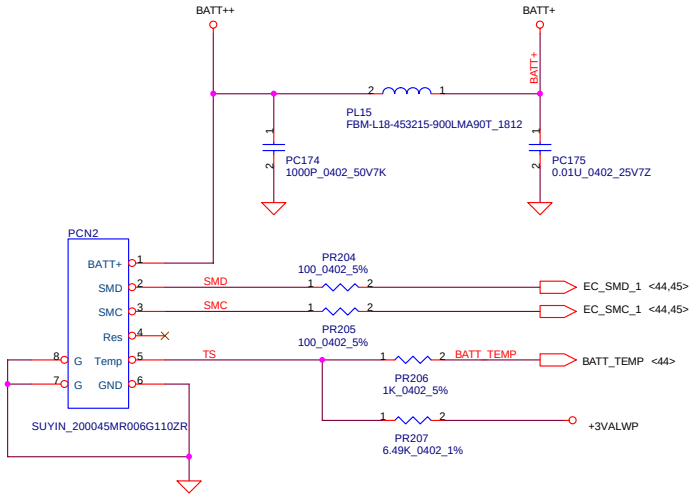
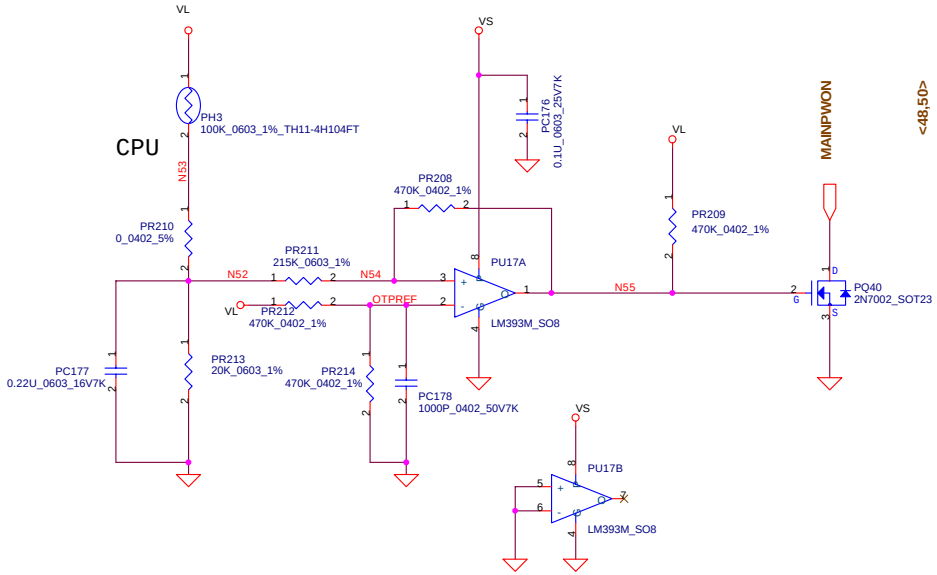
# Battery Connect/OTP




**PJPB1 battery connector**

**SMART Battery:**
**1.BATT+**
**2.SMBD**
**3.SMBC**
**4.Res**
**5.Temp**
**6.GND**

**PH1 under CPU botten side :**
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C

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| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |

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Title: **BATTERY CONN**

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-2841 | 1.0 |

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# Version change list (P.I.R. List)



| Item | Modify list | Reason for change | Rev. | PG# | Modify by |
|---|---|---|---|---|---|
| 1 | Add R579 and R580 for EC PA/PR detec | EC team request | Rev0.2 | P44 | 6/6 '05 |
| 2 | BOM del C591 220U_D2 for +VCCP bypass capacitance | Cost down | Rev0.2 | P6 | 6/6 '05 |
| 3 | U44 pin5 change from +5VAMP to +5V | Design modify | Rev0.2 | P40 | 6/6 '05 |
| 4 | U44 pin3 change from GNDA to GND | Design modify | Rev0.2 | P40 | 6/6 '05 |
| 5 | JP21 50pin contact to U31 F25pin | support system memory throttling | Rev0.2 | P13 | 6/6 '05 |
| 6 | JP24 50pin contact to U31 H26pin | support system memory throttling | Rev0.2 | P14 | 6/6 '05 |
| 7 | Add D26 | Add RTC Battery life | Rev0.2 | P28 | 6/6 '05 |
| 8 | BOM del R51 | Change NB strap pin CFG9 to Normal Operation | Rev0.2 | P11 | 6/6 '05 |
| 9 | Change R562 from 649K_0402 to 649_0402_1% | BOM error fix LAN can't link | Rev0.2 | P35 | 6/6 '05 |
| 10 | Change R558 from3.3K_0402 to 200_0402_5% | BOM error fix LAN can't link | Rev0.2 | P35 | 6/6 '05 |
| 11 | U24 contact to CPUSB# | Reserve new card detect input | Rev0.2 | P44 | 6/6 '05 |
| 12 | BOM del R307 | no need EC control new card reset | Rev0.2 | P44 | 6/6 '05 |
| 13 | Add R582 @0_0402 | Reserve | Rev0.2 | P35 | 6/6 '05 |
| 14 | Cancel U12 pin3 contact to +3VLAN | Design modify for LAN function fix LAN can't link | Rev0.2 | P35 | 6/6 '05 |
| 15 | IFPAB_PLLVDD、PLLVDD、VID_PLLVDD change from 3.3V to 2.5V | G72、G73 power modify | Rev0.2 | P20 | 6/6 '05 |
| 16 | PEX_CFG 0~2 change from 100 to 001 | Overridden CFG modify | Rev0.2 | P26 | 6/6 '05 |
| 17 | Add JP34 for mini-PCIE card | ME update | Rev0.2 | P37 | 6/6 '05 |
| 18 | Del BOM R359,R349,R361,D9,D10,Q23 | For TI 7412 modify request | Rev0.2 | P32 | 6/7 '05 |
| 19 | Change MSBS_SDCMD_SMWE_FIXED# to MSBS_SDCMD_SMWE# | For TI 7412 modify request | Rev0.2 | P32 | 6/7 '05 |
| 20 | Change SDCLK_SMRE_FIXED# to SDCLK_SMRE# | For TI 7412 modify request | Rev0.2 | P32 | 6/7 '05 |
| 21 | Change SDWP#_SMCE_FIXED# to SDWP#_SMCE# | For TI 7412 modify request | Rev0.2 | P32 | 6/7 '05 |
| 22 | Change SM_RB_FIXED# to SM_RB# | For TI 7412 modify request | Rev0.2 | P32 | 6/7 '05 |
| 23 | Change R554,R556,R557,R559 from 10K to 2.2K | For TI 7412 modify request | Rev0.2 | P32 | 6/7 '05 |
| 24 | Del R369,Q20,Q9,C446,JP29,JOPEN1,JOPEN2 | Cancel TV tuner function | Rev0.2 | P41 | 6/7 '05 |
| 25 | Change LINK_LED100# contact to U41 pin27 | Customer request for LAN link LED state | Rev0.2 | P35 | 6/8 '05 |
| 26 | Add R583,R584 75 ohm contact to JP19 and RJ45_GND | LAN modify | Rev0.2 | P35 | 6/8 '05 |
| 27 | Swap DQSA0~7/DQSA#0~7 and DQSC0~7/DQSC#0~7 | Schematic error modify | Rev0.2 | P19 | 6/8 '05 |
| 28 | Add R585 LID_SW# 10K pull-high reserve | LID_SW# floating | Rev0.2 | P44 | 6/13 '05 |
| 29 | U6 pin D23 SLP_S4# contact to U24 pin35 | EC need detect SLP_S4# for S4 state | Rev0.2 | P44 | 6/13 '05 |
| 30 | BOM update add R388 | DOCK_MICR need pull-high to +CODEC_REFC | Rev0.2 | P38 | 6/13 '05 |
| 31 | Change WL_PRIORITY contact to JP18 pin3 and BT_PRIORITY contact to JP18 pin5. | pin define swap | Rev0.2 | P37 | 6/14 '05 |
| 32 | BOM add R587,R588,R589,R590 0 ohm | for NV72 CLK swap pin rework | Rev0.2 | P19 | 6/14 '05 |
| 33 | JP17 footprint update | DB1 footprint error, fix can't TV-out | Rev0.2 | P17 | 6/14 '05 |
| 34 | Del R587,R588,R589,R590 0 ohm | for NV72 chipset modify | Rev0.3 | P19 | 6/17 '05 |
| 35 | Add R586,R587 | UMA or Discrrte PCBA detect | Rev0.3 | P44 | 6/27 '05 |
| 36 | Change R145,R146 from 88.7K to 88.7 ohm | BOM error | Rev0.3 | P18 | 6/28 '05 |
| 37 | Change C419,C421 form 33P to 22P_0402 | improve TV out quility. | Rev0.3 | P15 | 6/28 '05 |
| 38 | Add R588 | TI recommend(It can avoid the small noise form this SPKROUT pin) | Rev0.3 | P32 | 6/30 '05 |
| 39 | JP26 footprint update | ME change new USB connector | Rev0.3 | P41 | 6/30 '05 |
| 40 | JP3 footprint update | ME change new CRT connector | Rev0.3 | P17 | |
| 41 | Add R589 | Dual layout for 9LP306 and SLG8LP462. | Rev0.3 | P15 | 7/05 '05 |
| 42 | BOM add C591 220U_D2 for +VCCP bypass capacitance | change 220U location with C595 | Rev0.3 | P06 | 7/06 '05 |
| 43 | BOM del C595 220U_D2 for +VCCP bypass capacitance | For cost down | Rev0.3 | P11 | 7/06 '05 |
| 44 | U24(EC) pin91 add ACZ_RST# input | fix into xp codec out popo noise | Rev0.3 | P44 | 7/06 '05 |
| 45 | Add C790,C791,C792,C793,C794,C795,C796 100P_0402 | For EMI | Rev0.3 | P42 | 7/06 '05 |
| 46 | Add R590,Q46 | Switch PCBEEP path | Rev0.3 | P29,40 | 7/07 '05 |
| 47 | Add C797 reserve | For EMI | Rev0.3 | P37 | 7/07 '05 |
| 48 | Change R94,R141 to @ and change R96,R142 form @ to 128@ | For NVDIA change request | Rev0.3 | P19 | 7/08 '05 |
| 49 | Change R139,Q6 to @ and change R145 form 87_0402 to 124_0402, R84 from 130_0402 change to 124_0402 | For NVDIA change request | Rev0.3 | P18 | 7/08 '05 |
| 50 | Add screw hold H23, H24 | ME drawing modify | Rev0.3 | P47 | 7/08 '05 |
| 51 | R36 pin1 change contact to ACTLED#,R43 pin1 change contact to LINK_LED100# | Change LAN LED state, Amber LED indicates activity, Green LED indicates the link is present | Rev0.3 | P35 | 7/09 '05 |
| 52 | Add R591 10K_0402 and Q47 | fix mute LED power on turn on | Rev0.3 | P38 | 7/11 '05 |
| 53 | BOM del R383 4.7K pull-high | EC program this pin as push-pull output | Rev0.3 | P42 | 7/13 '05 |

| | | | |
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| Issued Date | 2005/03/10 | Deciphered Date | 2006/03/10 |

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Compal Electronics, Inc.

Title: H/W2 EE Dept. PIR SHEET

Size: | Document Number: LA-2841 | Rev: 1.0

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# Version change list (P.I.R. List)



| Item | Modify list | Reason for change | Rev. | PG# | Modify by |
|---|---|---|---|---|---|
| 54 | BOM del R101,C161,R467,R88 | nvdia recommend | Rev0.3 | P18 | 7/13 '05 |
| 55 | BOM del R78,R468,R111,R117,R63,R475,R477 | nvdia recommend | Rev0.3 | P26 | 7/13 '05 |
| 56 | BOM del R108,add R112 | nvdia recommend(change to PEX_CFG[2..0]=0x010b) | Rev0.3 | P26 | 7/18 '05 |
| 57 | BOM add C599 | add 220U cap for 1.8V power decoupling | Rev0.4 | P11 | 8/18 '05 |
| 58 | BOM add R455 | add 51_0402 resister for intel Yonah B0 sightings update | Rev0.4 | P04 | 8/18 '05 |
| 59 | Add Q48,Q49,Q50,R593,R594 | modify WLED control circuit for OTS:0164892 issue | Rev0.4 | P37 | 8/22 '05 |
| 60 | Del D3 | modify WLED control circuit for OTS:0164892 issue | Rev0.4 | P41 | 8/22 '05 |
| 61 | Del R440,R432,Q30 | modify WLED control circuit for OTS:0164892 issue | Rev0.4 | P16 | 8/22 '05 |
| 62 | Add R592 | add R592 150 ohm for WLED# current limit | Rev0.4 | P37 | 8/22 '05 |
| 63 | JP9 Pin 14 contact to +5VS | change SPDIF LED power from +5V to +5VS | Rev0.4 | P42 | 8/22 '05 |
| 64 | Add Q51 | Prevent TPS2231 pin2 +3VALW leakage to +3VS | Rev0.4 | P34 | 8/29 '05 |
| 65 | JP5 Pin 25 contact to +3VALW | switch board need +3VALW provide lie switch power | Rev0.4 | P42 | 8/23 '05 |
| 66 | BOM change R554/R557/R556 to 100K, change R559 to 22K | TI 7412 pull-high recommend | Rev0.4 | P32 | 8/23 '05 |
| 67 | JP3 change new part | change CRT conn from top side to bottom side for DFX request | Rev0.4 | P17 | 8/24 '05 |
| 68 | Del C764,R552,R553, Add D28,change U40 to G993 fan control | Fan control circuit change to G993 | Rev0.4 | P04 | 8/24 '05 |
| 69 | BOM del R47 | Intel WW31 document update | Rev0.4 | P11 | 8/29 '05 |
| 70 | Add R595/R596/R597/R598/R599 | SD card signal add 33 ohm damping resister | Rev0.4 | P32 | 8/30 '05 |
| 71 | Add R817/R77 10K_0402 | NV72 A1 chip recommend JTAG_TCK pull-high and JTAG_N pull-down | Rev0.4 | P18 | 8/29 '05 |
| 72 | Del clock generators difference clock 49.9ohm termination | ICS9LP306 clock generators update | Rev0.4 | P15 | 8/29 '05 |
| 73 | Change clock generators difference clock 33ohm damping to 10ohm | ICS9LP306 clock generators update | Rev0.4 | P15 | 8/29 '05 |
| 74 | Change R266 from 475 ohm to 2.4K ohm | ICS9LP306 clock generators update | Rev0.4 | P15 | 8/29 '05 |
| 75 | Add D29/D30/D31/D32/D33/D34/D35/D36 | SD card signal add diode for Voltage clamp | Rev0.4 | P32 | 8/30 '05 |
| 76 | Move C87/C11/C10/C3/C4/C5/C2/C13/C14/C34/C35/C1 for layout | ME update limit area for CPU | Rev0.4 | P06 | 8/30 '05 |
| 77 | Change R591 from 10K ohm to 100 ohm | Fix OTS:163350 calgary's mute LED can't display | Rev0.4 | P38 | 8/30 '05 |
| 78 | JP34 pin50 change contact from PM_EXTTS#1 to PM_EXTTS#0 | Intel WW31 document update | Rev0.4 | P14 | 8/30 '05 |
| 79 | U31 pinH6 change contact from PM_EXTTS#1 to DPRSLPVR | Intel WW31 document update | Rev0.4 | P07 | 8/30 '05 |
| 80 | D26 pin2 change contact from +3VALW to LDO3 | Add RTC battery life | Rev0.4 | P28 | 8/30 '05 |
| 81 | BOM change R562 from 649 ohm to 619 ohm and change U12 to new part | LAN performance modify | Rev0.4 | P35 | 8/30 '05 |
| 82 | Add R600 100 ohm and DEL C608 @ | HP recommend | Rev0.4 | P37 | 8/30 '05 |
| 83 | Add R601 100 ohm | HP recommend | Rev0.4 | P41 | 8/30 '05 |
| 84 | Reserve C810~C821 0.1u cap | For EMI | Rev0.4 | P42 | 8/30 '05 |
| 85 | Add L32 and C822 on SPDIF signal | For EMI | Rev0.4 | P42 | 8/30 '05 |
| 86 | Add C802 /C803 /C804 /C805 1000P for CLKREQA#/CLKREQB#/CLKREQC#/CLKREQD# | For EMI | Rev0.4 | P15 | 8/30 '05 |
| 87 | U40 pin5,6,7,8 contact to GND | schematic update for SI2 fan can't full trun on issue | Rev0.5 | P04 | 10/26 '05 |
| 88 | change C599 from 220U to 330U | Steady the 1.8V | Rev0.5 | P11 | 10/26 '05 |
| 89 | Add R103 40.2ohm | nvdia recommend | Rev0.5 | P21 | 10/28 '05 |
| 90 | change R510,R75,R533,R168 from 120ohm to 499ohm for NV73 only | nvdia recommend | Rev0.5 | P22~25 | 10/26 '05 |
| 91 | straps table PEX_CFG[2:0] from 010 to 001 and PCI_DEVID[3:0] NV73M from 1010 to 1011 | nvdia recommend | Rev0.5 | P26 | 10/26 '05 |
| 92 | Add C825 15P_0402 for MSCLK_SDCLK_SMELWP# signal | For EMI | Rev0.5 | P32 | 10/26 '05 |
| 93 | Add C823 1000P_0402 for +VCC_SD | For EMI | Rev0.5 | P32 | 10/26 '05 |
| 94 | Add C824 1000P_0402 for +VCC_SM_XD | For EMI | Rev0.5 | P32 | 10/26 '05 |
| 95 | Add C826 1000P_0402 for JP32 pin4 | For EMI | Rev0.5 | P32 | 10/26 '05 |
| 96 | change PCM_SPK pull down R588 from 43K to 10K | TI recommend | Rev0.5 | P32 | 10/26 '05 |
| 97 | D29,D30,D31,D32 pin1 contact to +VCC_MS | schematic update for SI2 MS card can't work issue | Rev0.5 | P32 | 10/26 '05 |
| 98 | Add R607 22ohm and @ C827 10P | Reserve | Rev0.5 | P32 | 10/26 '05 |
| 99 | U18 pin6 contact to +3VS | TI recommend | Rev0.5 | P33 | 10/26 '05 |
| 100 | Add @ R606 110ohm | Reserve | Rev0.5 | P35 | 10/26 '05 |
| 101 | Change Q46 to U45 analog switch | design change | Rev0.5 | P40 | 10/26 '05 |
| 102 | Change U38 pin3,4 form +5VALW to +5V | design change | Rev0.5 | P41 | 10/26 '05 |
| 103 | Change Q2 from AO3413 to AO3419 | | Rev0.5 | P41 | 10/26 '05 |
| 104 | Add D38~D45 for KB ESD solution | For ESD request | Rev0.5 | P42 | 10/26 '05 |
| 105 | AIR_ACIN change contact to U24 pin81 and add R605 for BID define, add D37. | design change | Rev0.5 | P44 | 10/26 '05 |



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# Version change list (P.I.R. List)

| Item | Modify list | Reason for change | Rev. | PG# | Modify by |
|---|---|---|---|---|---|
| 106 | Add D46 | ESD | Rev1.0 | P17 | 12/08 '05 |
| 107 | RESERVE Q52 / C828 / R608 | CONTROL RTC RESET | Rev1.0 | P28 | 12/08 '05 |
| 108 | ADD R612 | CIR OUTPUT IS OPEN-DRAIN | Rev1.0 | P42 | 12/08 '05 |
| 109 | CANCEL C811 / C812 AND ADD D47 | ESD | Rev1.0 | P42 | 12/08 '05 |
| 110 | CANCEL Q45 AND ADD U48 / C830 | FIX ODD CAUSE BOOT LATE ISSUE | Rev1.0 | P43 | 12/08 '05 |
| 111 | CANCEL D37 AND RESERVE U47 / C51 / R611 | IMPROVE EC RESET SIGNAL | Rev1.0 | P44 | 12/08 '05 |
| 112 | RESERVE U46 / C829 / R609 / Q53 / R610 | CONTROL WRITE SIGNAL OF FLASH ROM | Rev1.0 | P45 | 12/08 '05 |

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# Version change list (P.I.R. List)

## Power section



| Item | Reason for change | PG# | Modify List | Date | B.Ver# |
|---|---|---|---|---|---|
| 1 | Solve the oscillate of +3VALWP when plug adapter. | 48 | Change PC11 from 10U_0805_10V to 0.1U_0603_25V. | 2005.06.01 | |
| 2 | Adjust VGA power rail sequence. | 54 | Add PQ55, PQ56 and PR249 | 2005.06.21 | |
| 3 | To protect PQ21, because SUSP change to 18.5V from 5V. | 52 | Add PR253 and change PR114 to 510K_0402_5%. | 2005.08.10 | |
| 4 | To save S5 power consumption. | 50,48 | Add PR254, PR13, PR14, PQ1 and PC8.<br>Reserve PR255. | 2005.08.15 | |
| 5 | To solve EMI issue. | 53,49 | Add PR117,PR129,PR119,PR138,PC108 and PC119.<br>Change PJP16 to PL18 and PR30 from 0_0402 to 2.2_0603. | 2005.08.15 | |
| 6 | To speed up CP mode response. | 49 | Change PR32 to 10K; PR35 to 6.8K and PC21 to 2200P. | 2005.08.23 | |
| 7 | Reserve capacitor to reduce noise. | 49 | Reserve PC209. | 2005.08.27 | |
| 8 | To speed up C4 return to C0. follow Intel recommend. | 53 | Change PR141 from 0_0402_5% to 499_0402_1%. | 2005.08.29 | |
| 9 | To pull up +1.8V power plan to 1.846V. | 51 | Change PR89 from 10.2K to 10.5K. | 2005.10.01 | |
| 10 | To filter high frequency from AirCard. | 55 | Add PC210 22P_0402_50V. | 2005.11.25 | |

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/03/22 | Deciphered Date | 2006/03/22 |

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