Compal Confidential

Model Name : ZIVY0
File Name : LA-A921PR03
BOM P/N:4319xxxxxx -- ZIVY0

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ZIVY0 M/B Schematics Document

Intel SharyBay ULT Processor

2013-12-01

REV:1.0

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: LA-A921PR01	Rev: 1.0
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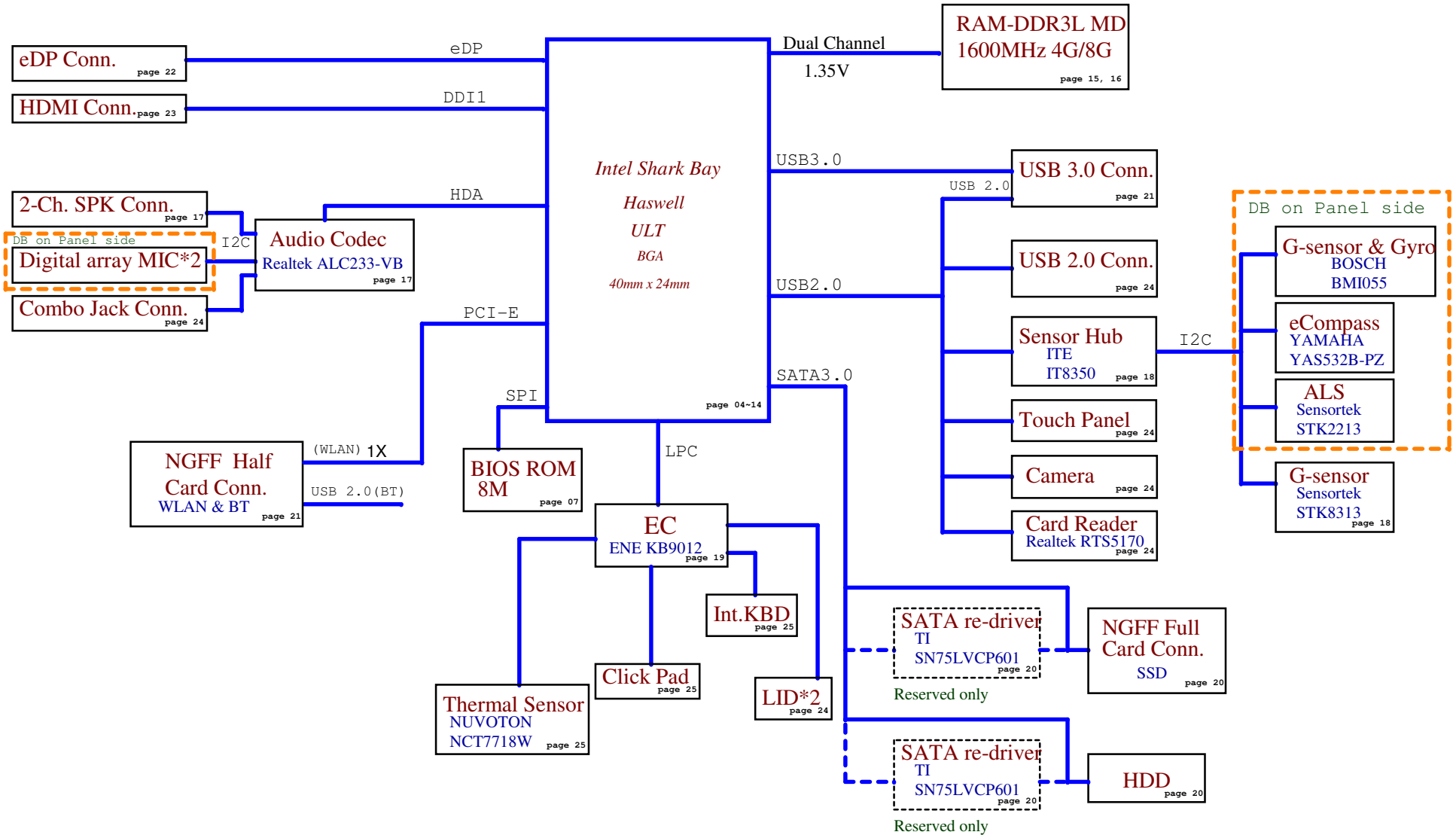
Model Name : ZIVY0
File Name : LA-A921P



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.			
Title: MB Block Diagram			
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Voltage Rails

power plane / State	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
76 LEVEL	X76@
Unpop	@
CPU OPTION	CPU1@ ~ CPU5@
DRAM Option	H4G@ E4G@ S4G@ M4G@ S8G@ E8G@ H8G@ H8G@
KB9012	9012@
KB9022	9022@
No Re-driver	NR@
TI Re-driver	TI@
PARADE Re-driver	8520C@
Segate HDD	HDDSG@
WD HDD	HDDWD@
EMI PART	EMI@
ESD PART	ESD@
SSD-SATA	SSDSATA@

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery Charger Home Key Button	01100000

EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W SharkBay ULT SML1	1001100x

CPU SM Bus address

Device	Address
Touch Pad	

CPU SML0 Bus address

Device	Address

USB 2.0 Port Table

	USB 2.0 Port	2 External USB Port
	0	USB 2.0 Port (I/O Board)
	1	USB 3.0/2.0 Port (MB)
	2	
	3	Card Reader
	4	Touch Screen (reserve)
	5	Camera
	6	Mini Card (WLAN/BT)
	7	Sensor Fusion

USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

SATA Port Table

Port	
3	NGFF SSD(SATA)
2	
1	
0	HDD

PCIE Port Table

Port	Lane	
1		
2		
3		
4		WLAN
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

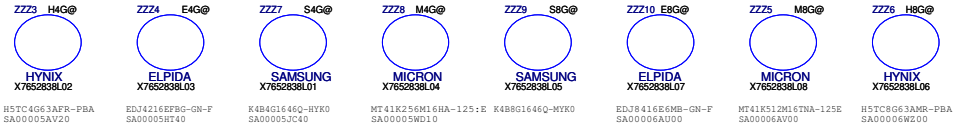
SMBUS Control Table

	HOST	Changer	BATT	KB9022	CPU	HomeKey	Touch Pad	Thermal sensor NCT7718W
EC_SMB_CK1 EC_SMB_DA1	KB9022 +3VLP	V +3VLP	V +3VLP	X	X	V +3VLP	X	X
EC_SMB_CK2 EC_SMB_DA2	KB9022 +3VS	X	X	X	V +3VS	X	X	V +3VS
SMBCLK SMBDATA	CPU +3VALW	X	X	X	X	X	V +3VS	X
SML0CLK SML0DATA	CPU +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	CPU +3VS	X	X	V +3VS	X	X	X	V +3VS

CPU part

PCB part

DRAM



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Compal Electronics, Inc.			
Title: Note List			
Size: Custom	Document Number: LA-A921PR01		Rev: 1.0
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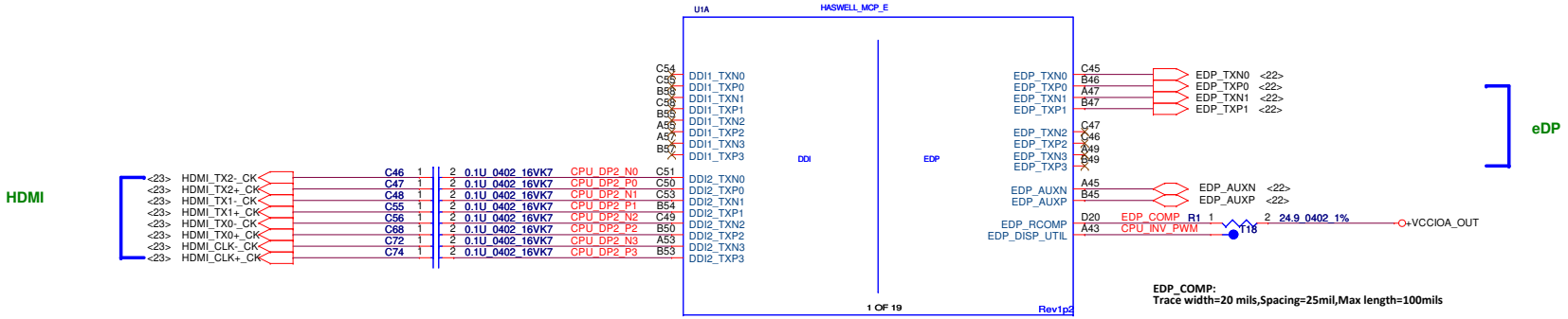
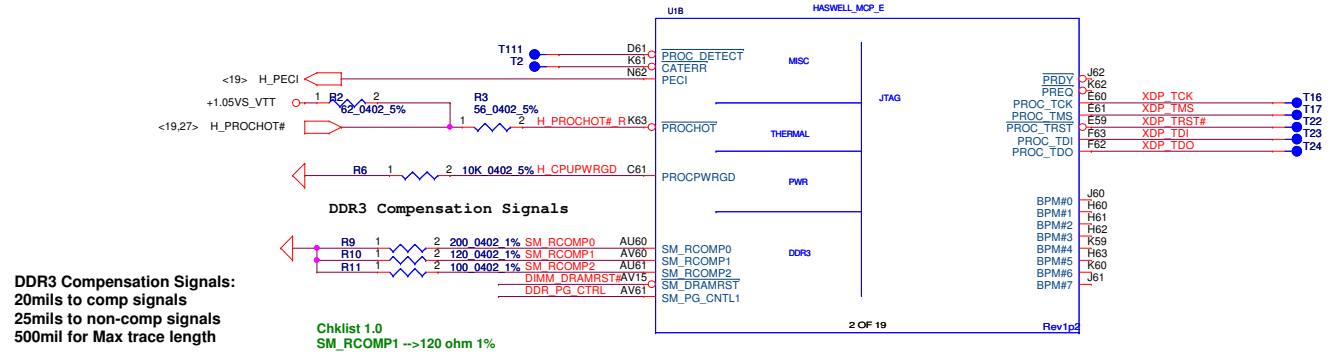
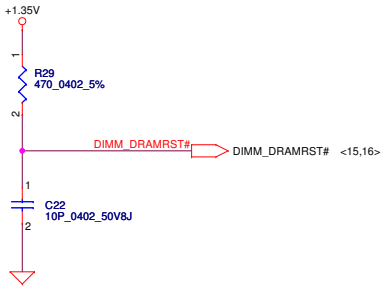
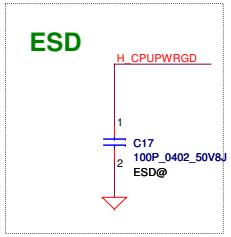


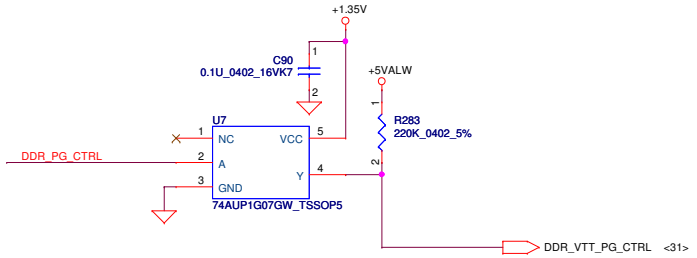


DDR3 Compensation Signals:
20mils to comp signals
25mils to non-comp signals
500mil for Max trace length

Chklist 1.0
SM_RCOMP1 -->120 ohm 1%







Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.			
Title	HSW MCP(1/11) DDI,MSIC,XDP		
Size: Custom	Document Number: LA-A921PR01		Rev: 1.0
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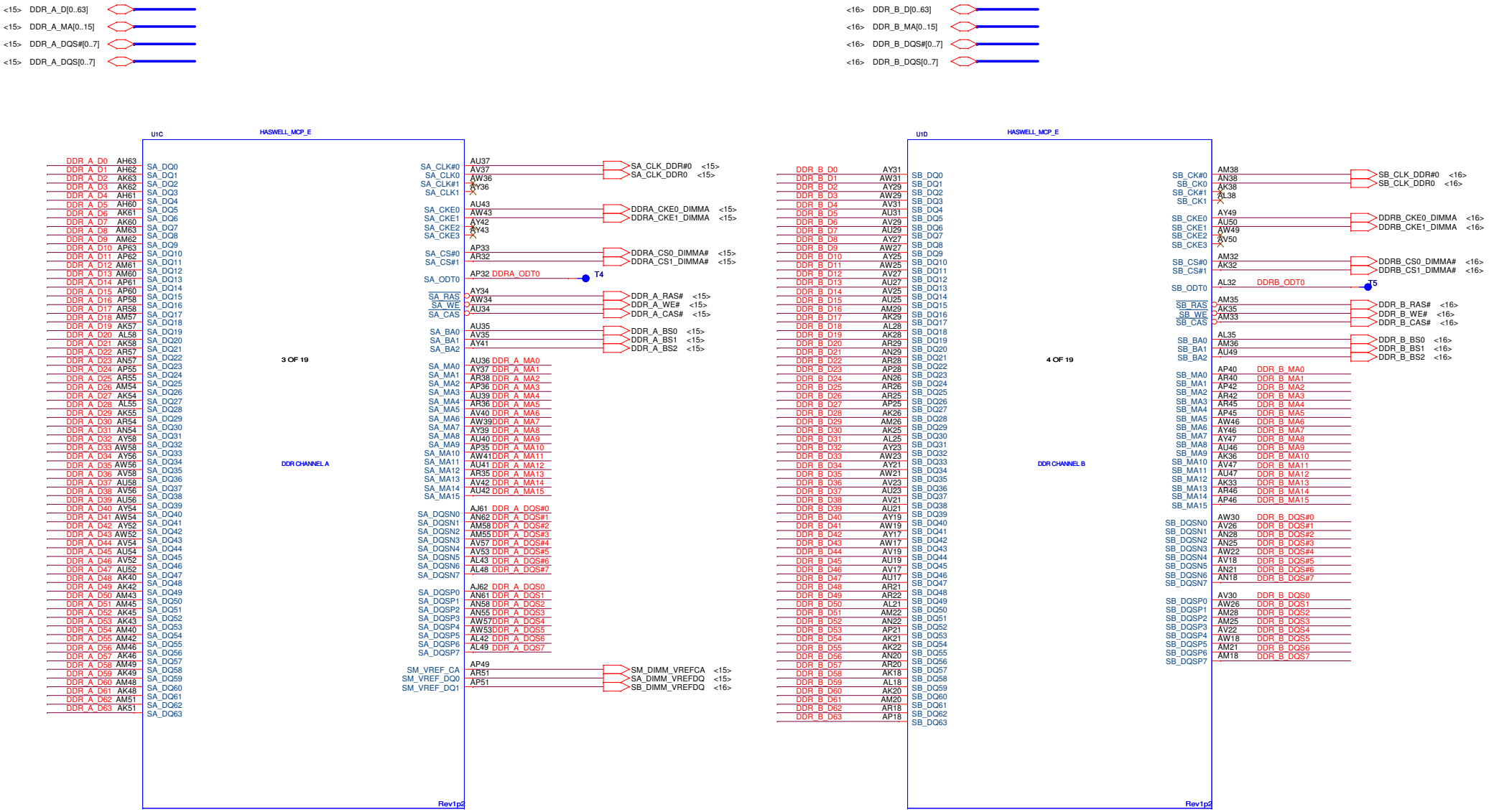
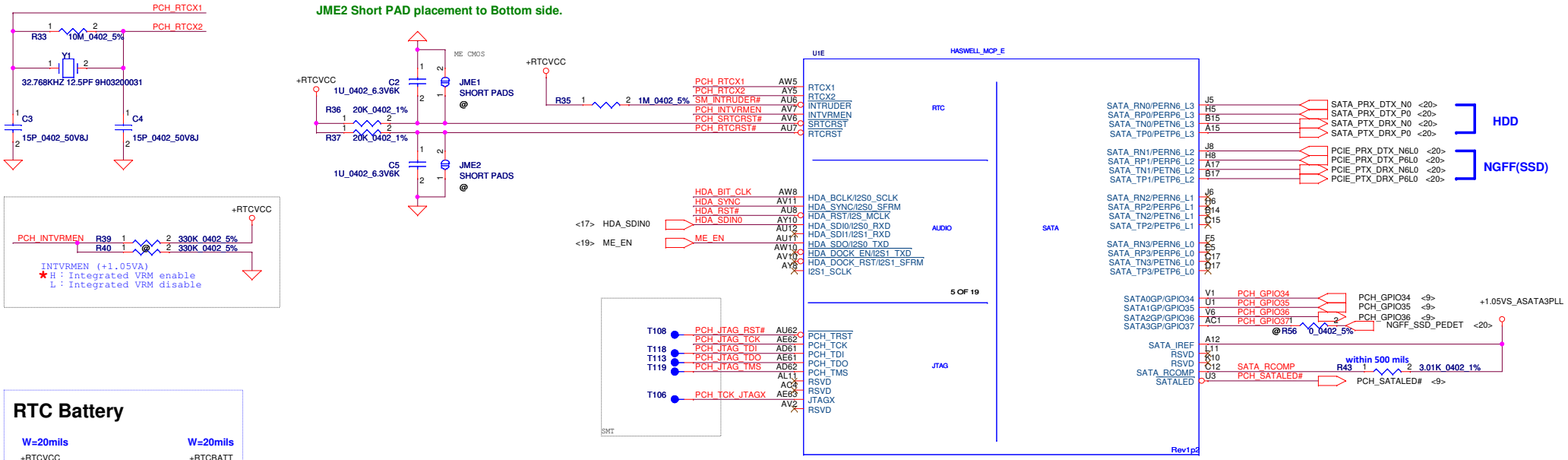


Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.			
Title	HSW MCP(2/11) DDRIII		
Size: Custom	Document Number: LA-A921PR01		Rev: 1.0
Date: Tuesday, December 17, 2013	Sheet 5 of 38		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/24	Deciphered Date 2015/07/24	Title HSW MCP(3/11) RTC,SATA,XDP

Size Custom	Document Number LA-A921PR01		Rev 1.0
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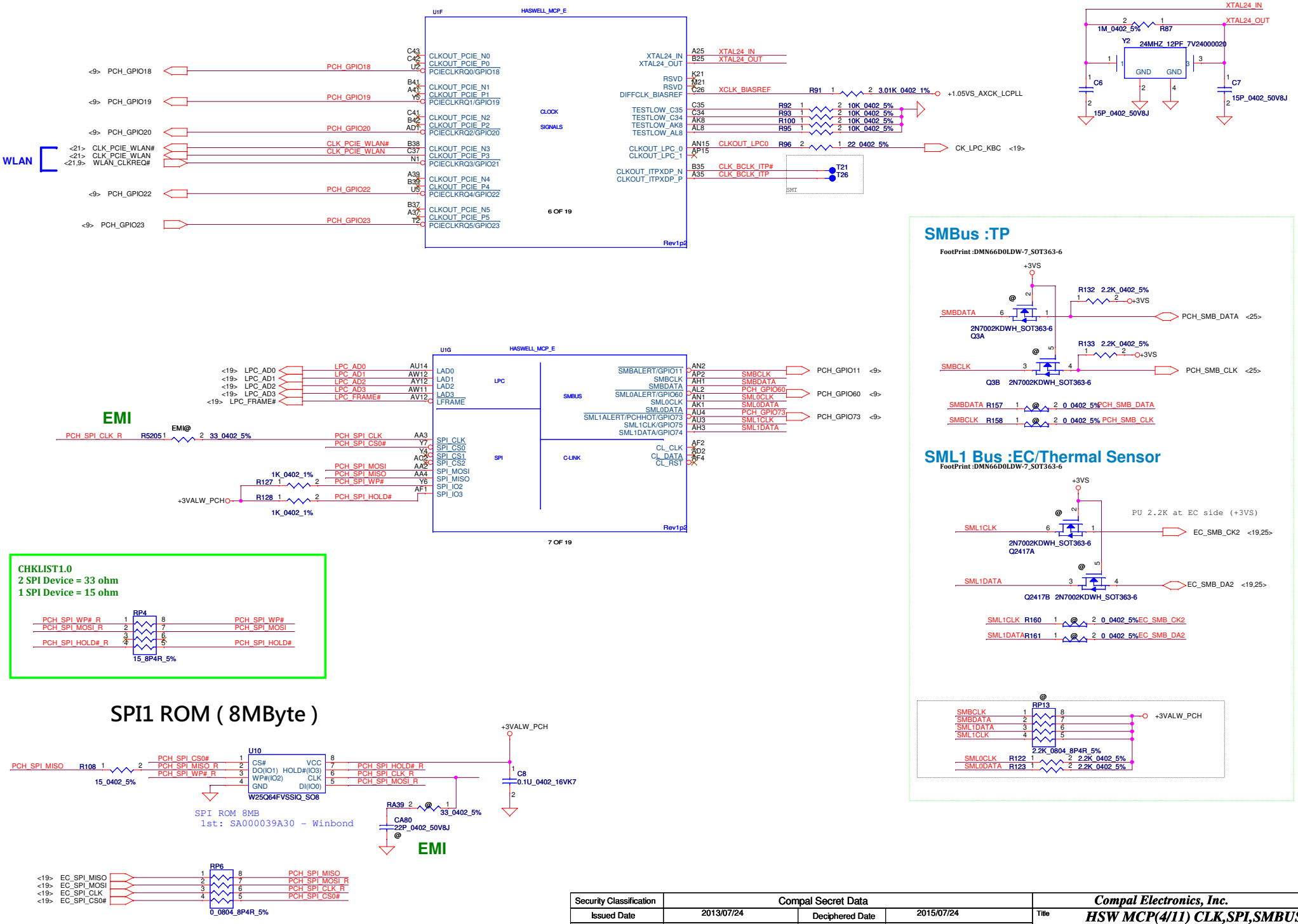

Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.			
Title	HSW MCP(4/11) CLK,SPI,SMBUS		
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Note: SUSACK# and SUSWARN# can be tied together if
EC does not want to involve in the handshake mechanism
for the Deep Sleep state entry and exit

CAN be NC ,if not support Deep Sx

DPWROK: Tired toghter with RSMRST#
that do not support Deep Sx

DSWODVREN - On Die DSW VR Enable
* H : Enable(DEFAULT)
L : Disable

PCH_PWROK R146 1 @ 2 0_0402_5% APWROK_R

+3VALW_PCH
R643 200K_0402_5%
<19> AC_PRESENT AC_PRESENT

U1H HASWELL_MCP_E
SYSTEM POWER MANAGEMENT

T114 SUSACK# R AK2 SUSACK
<9> SYS_RESET# SYS_RESET# AG3 SYS_RESET
<19> SYS_PWROK SYS_PWROK AG2 SYS_PWROK
<19> PCH_PWROK PCH_PWROK AY7 PCH_PWROK
APWROK_R AB5 APWROK
H_PLT_RST# AG7 PLTRST

R149 1 2 10K_0402_5%
<19> EC_RSMRST# EC_RSMRST# AW6 RSMRST
<9> PCH_GPIO30 PCH_GPIO30 AV4 SUSWARN/SUSPWRDNACK/GPIO30
<19> PBTN_OUT# PBTN_OUT# AL7 PWRBTN
AC_PRESENT AJ8 ACPRESENT/GPIO31
<9> PCH_GPIO72 PCH_GPIO72 AN4 BATLOW/GPIO72
T109 AF3 SLP_S0
<9> PCH_GPIO29 PCH_GPIO29 AM5 SLP_WLAN/GPIO29

PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx , connect to VCCSUS3_3)

DSWVRMEN AW7 DSWODVREN
DPWROK AV5 DPWROK
WAKE AJ5 PCH_PCIE_WAKE#
CLKRUN/GPIO32 V5 PCH_GPIO32
SUS_STAT/GPIO61 AG4
SUSCLK/GPIO62 AE6 SUSCLK
SLP_S5/GPIO63 AP5 PM_SLP_S5#
SLP_S4 AJ6 PM_SLP_S4#
SLP_S3 AT4 PM_SLP_S3#
SLP_A AL5 PM_SLP_A#
SLP_SUS AP4
SLP_LAN AJ7

R134 1 2 330K_0402_5%
R139 1 @ 2 330K_0402_5%
+RTCVCC
R148 1 @ 2 0_0402_5% EC_RSMRST#
PCH_PCIE_WAKE# <9>
PCH_GPIO32 <9>
PCH_GPIO61 <9>
R152 1 @ 2 0_0402_5%
SUSCLK_WLAN <21>
PM_SLP_S5# <19>
PM_SLP_S4# <19>
PM_SLP_S3# <19>
T120
T110
T112

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Rev1p2

U11 HASWELL_MCP_E

<22> INVPWM R150 1 @ 2 0_0402_5% EDP_BKCTL B8
<19> ENBKL EDP_BKLCTL A9
<22> PCH_ENVDD EDP_BKLEN C6
EDP_VDDEN
eDP SIDEBAND

DDPB_CTRLCLK B9
DDPB_CTRLDATA C9 DDI1_CTRL_DATA
DDPC_CTRLCLK D9 DDI2_CTRL_CK
DDPC_CTRLDATA D11 DDI2_CTRL_DATA
DDI2_CTRL_CK <23>
DDI2_CTRL_DATA <23>

+3VS
DDI1_CTRL_DATA 1 @ 2 2.2K_0402_5% R310

DDPB_CTRLDATA: Port B Detected
DDPC_CTRLDATA: Port C Detected
* 1: Port B or C is detected
0: Port B or C is not detected
(Have internal PD)

<9> PCH_GPIO77 U6 PIRQA/GPIO77
<9> PCH_GPIO78 PCH_GPIO78 P4 PIRQB/GPIO78
<9> PCH_GPIO79 PCH_GPIO79 N4 PIRQC/GPIO79
<21,9> WLBT_OFF# N2 PIRQD/GPIO80
T27 AD4 PME
GPIO

<9> PCH_GPIO55 U7 GPIO55
<9> PCH_GPIO52 PCH_GPIO52 L1 GPIO52
<9> PCH_GPIO54 PCH_GPIO54 L3 GPIO54
<9> PCH_GPIO51 R5 GPIO51
<9> PCH_GPIO53 PCH_GPIO53 L4 GPIO53

DISPLAY
DDPB_AUXN C5
DDPC_AUXN B6
DDPB_AUXP B5
DDPC_AUXP A6
DDPB_HPD C8
DDPC_HPD A8
EDP_HPD D6
DDI2_HDMI_HPD <23>
EDP_HPD <22>

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Rev1p2

ESD
H_PLT_RST#
C14 100P_0402_50V8J @

R155 1 @ 2 0_0402_5%
+3VS
H_PLT_RST#
U5 @ MC74VHC1G08DFT2G_SC70-5
PLT_RST# <19,21>
R159 100K_0402_5%

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Compal Electronics, Inc.
Title: HSW MCP(5/11) PM,GPIO,DDI
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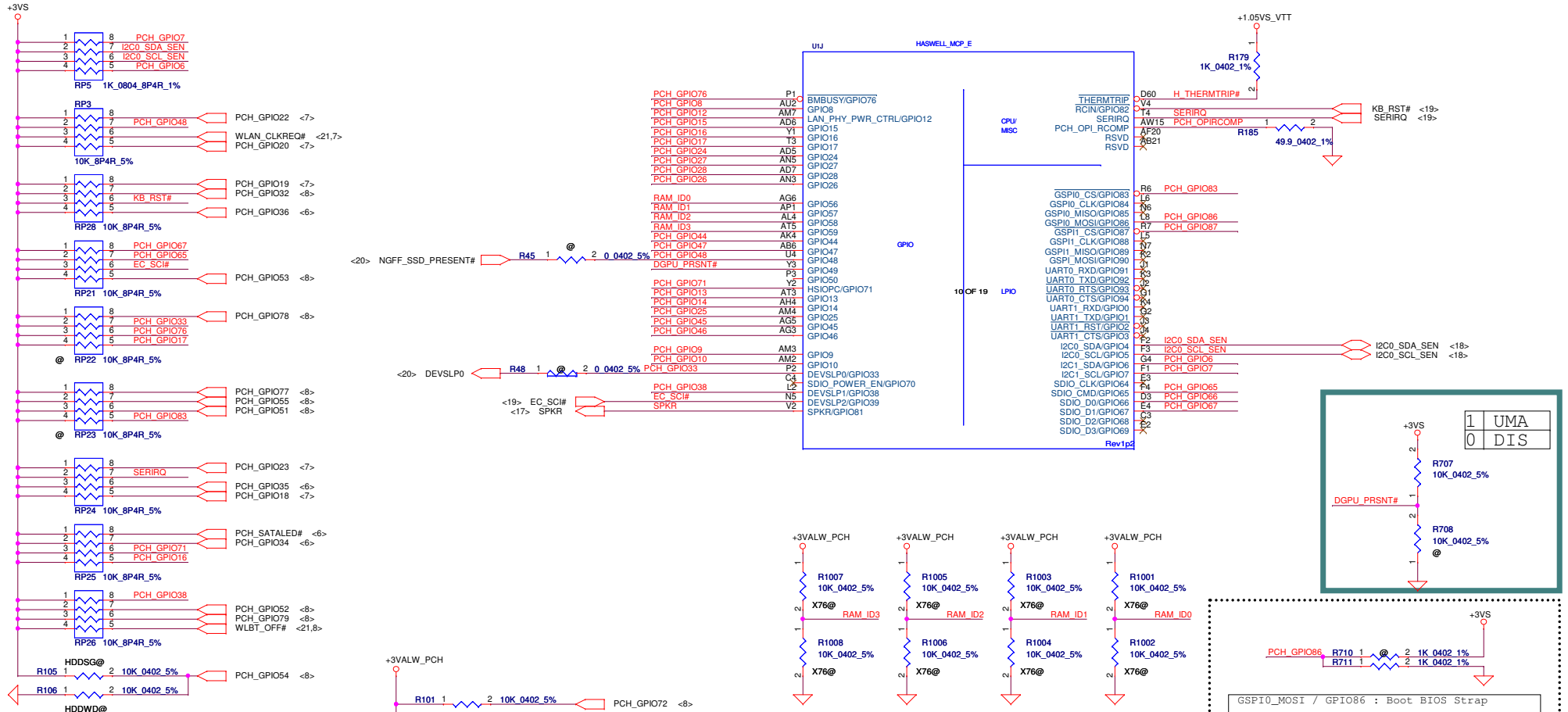

RAM_ID3 GPIO59	RAM_ID2 GPIO58	RAM_ID1 GPIO57	RAM_ID0 GPIO56	RAM P/N
0	0	0	0	HYNIX H5TC4G63AFR-PBA
0	0	0	1	SAMSUNG K4B4G1646Q-HYK0
0	0	1	0	MICRON MT41K256M16HA-125:E
0	0	1	1	ELPIDA EDJ4216EFBG-GN-F
0	1	0	0	SAMSUNG K4B8G1646Q-MYK0
0	1	0	1	ELPIDA EDJ8416E6MB-GN-F
0	1	1	0	MICRON MT41K512M16TNA-125:E
0	1	1	1	HYNIX H5TC8G63AMR-PBA
1	0	0	0	TBD
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD

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Compal Electronics, Inc.	
Title	HSW MCP(6/11) GPIO,LPIO
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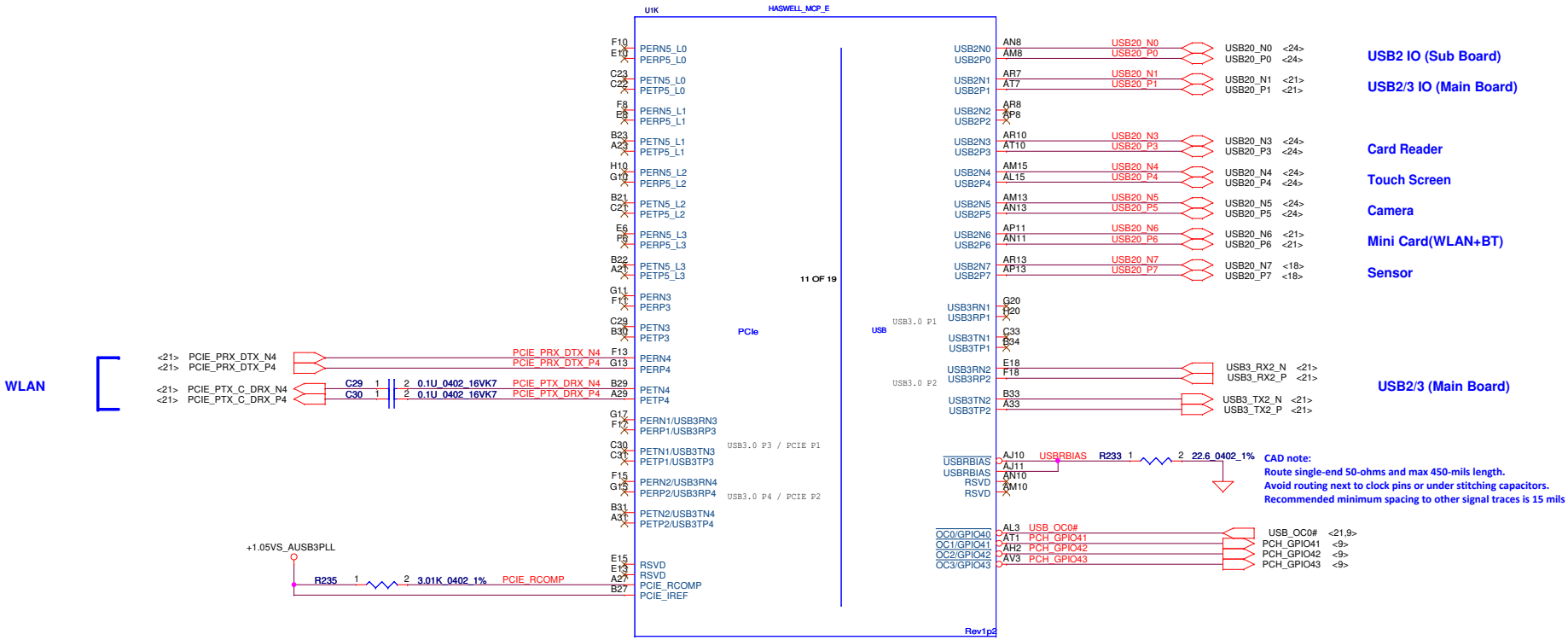

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Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.		
Title	HSW MCP(7/11) PCIE,USB	
Size: Custom	Document Number: LA-A921PR01	Rev: 1.0
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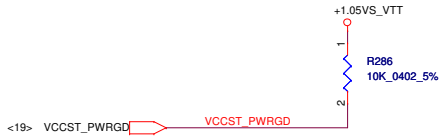
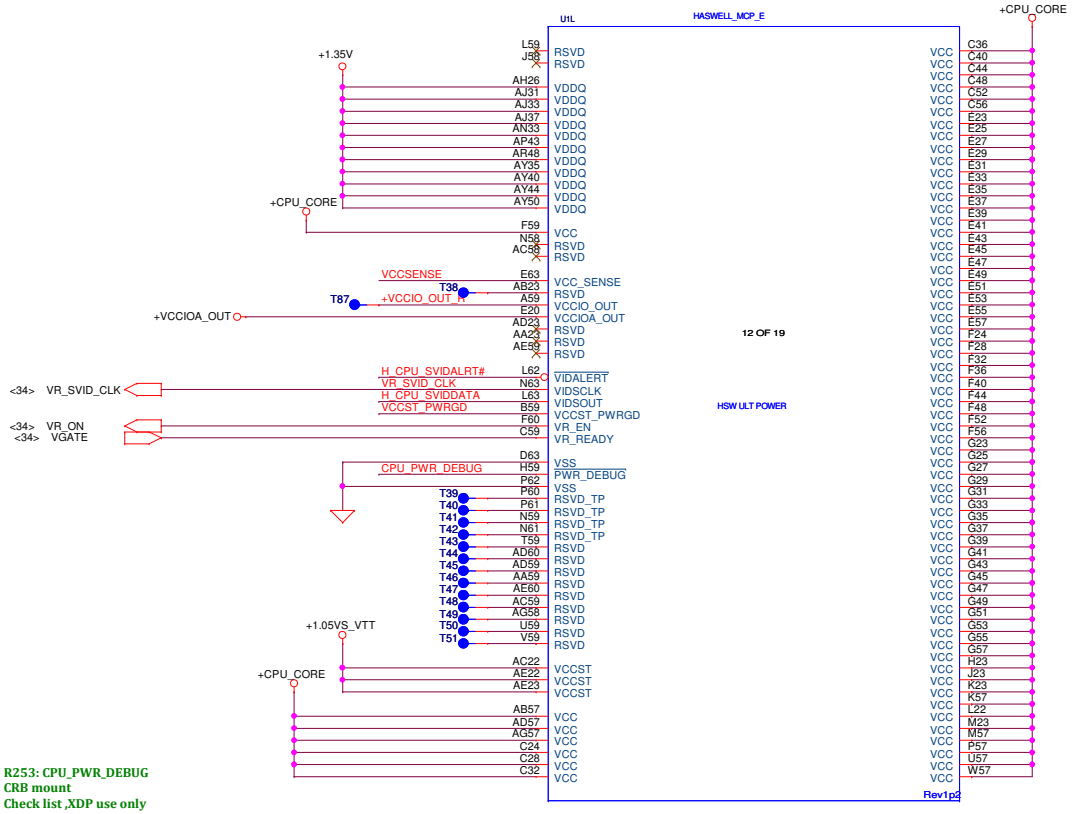
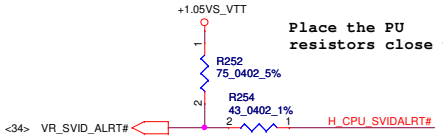


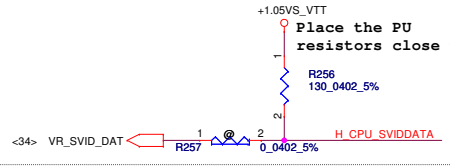
Define EC OD pin, need double confirm.



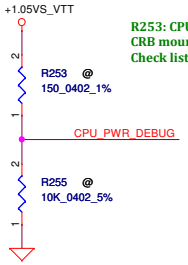
SVID ALERT



SVID DATA

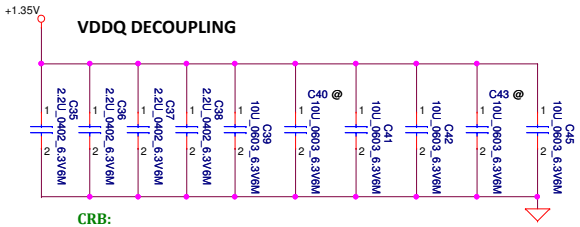


R256:
CRB r0.7 changed from 130 Ohms to 110 Ohms

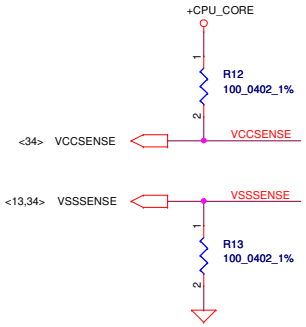


R253: CPU_PWR_DEBUG
CRB mount
Check list ,XDP use only

VDDQ DECOUPLING



CRB:
+1.35V : 470UF/2V/7343 *2 (Un-mount)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4



CAD Note: PU resistor should be close to CPU

CAD Note: PD resistor should be close to CPU

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Compal Electronics, Inc.

Title: HSW MCP(8/11) Power

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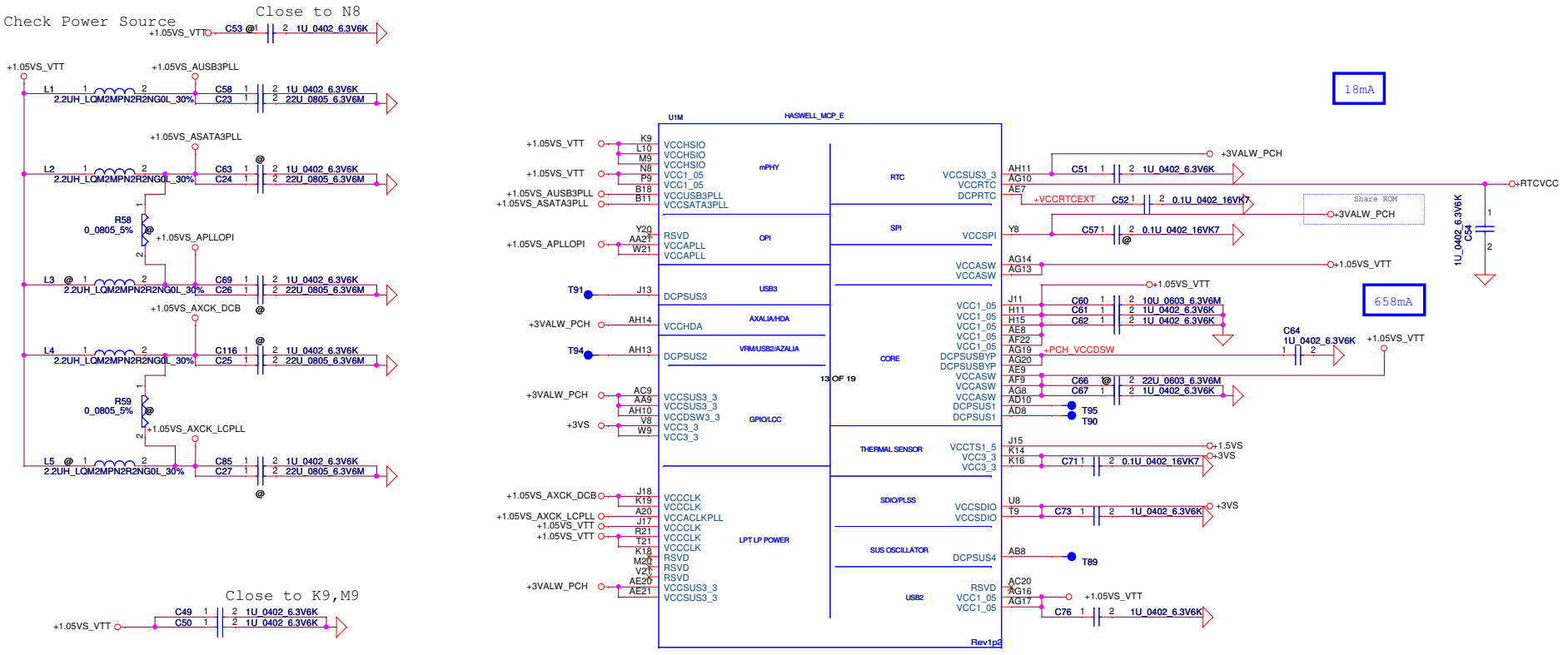

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Compal Electronics, Inc.	
Title	HSW MCP(9/11) Power
Size: Custom	Document Number: LA-A921PR01
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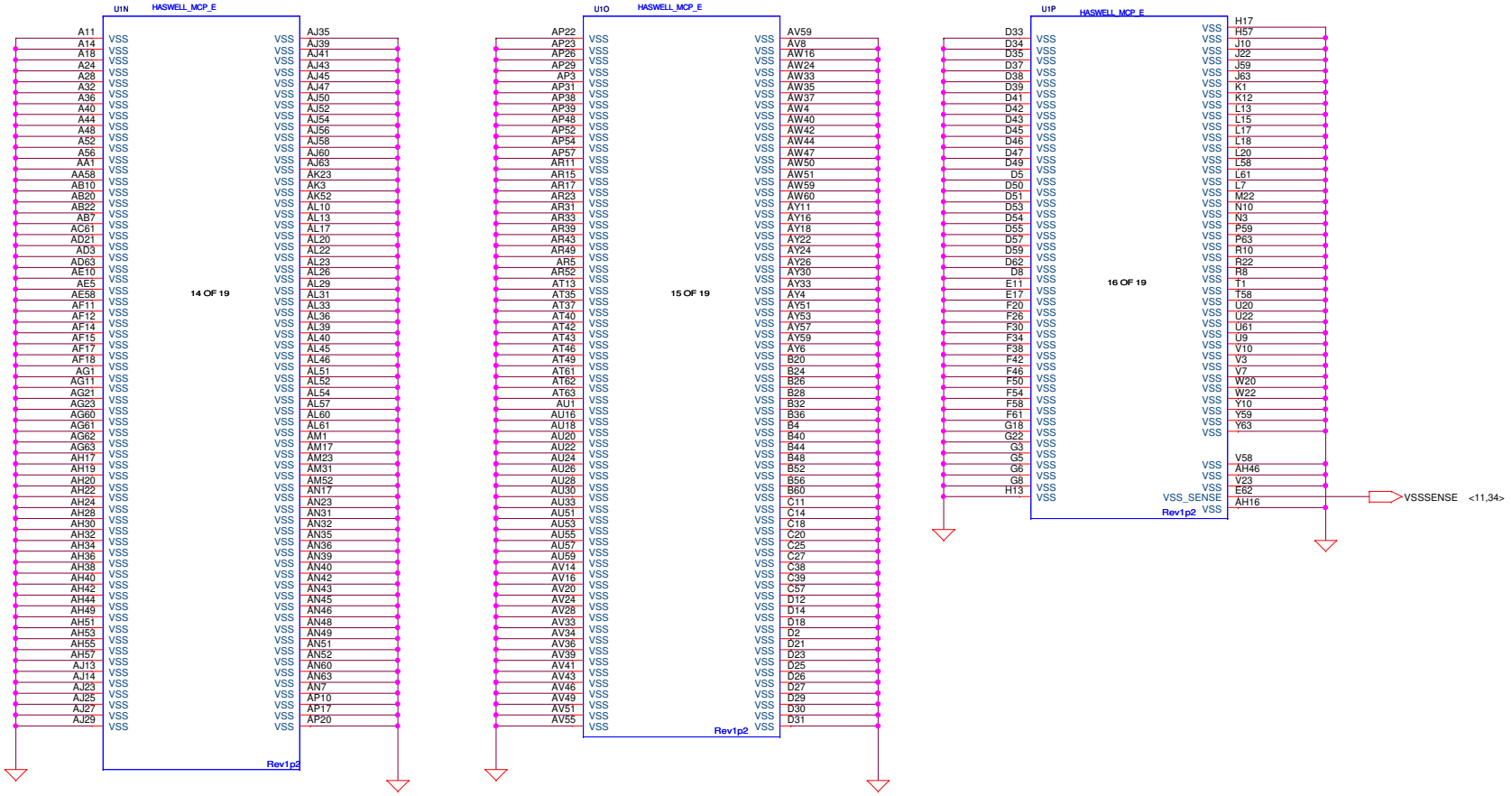

Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.	
Title	HSW MCP(10/11) GND
Size: Custom	Document Number: LA-A921PR01
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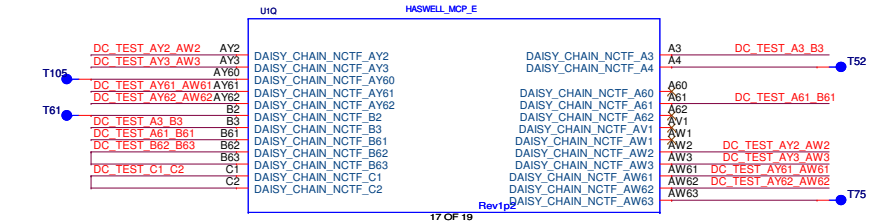
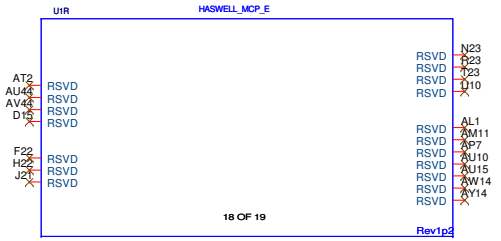
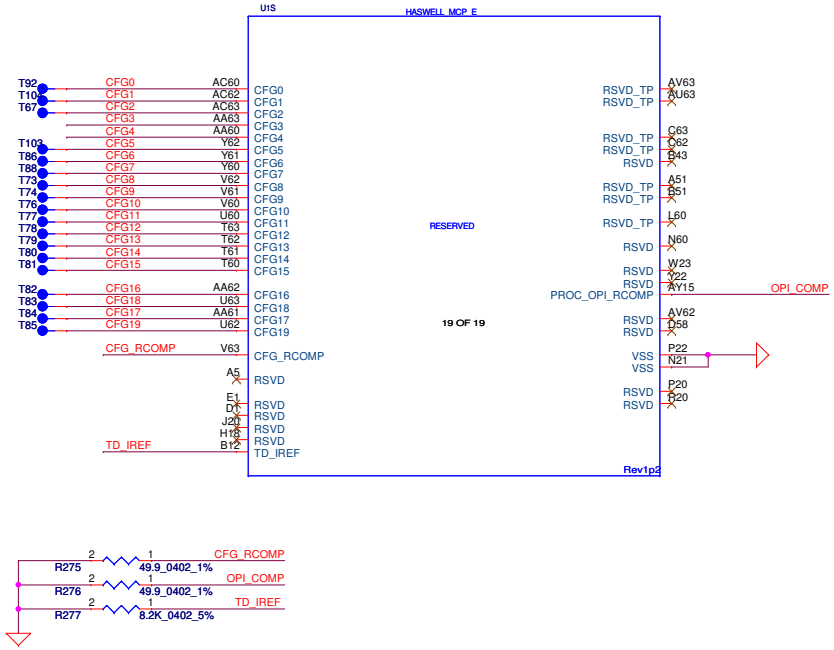
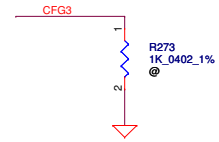


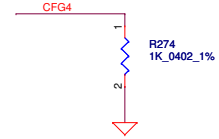




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.			
Title: HSW MCP(11/11) RSVD			
Size: Custom	Document Number: LA-A921PR01		Rev: 1.0
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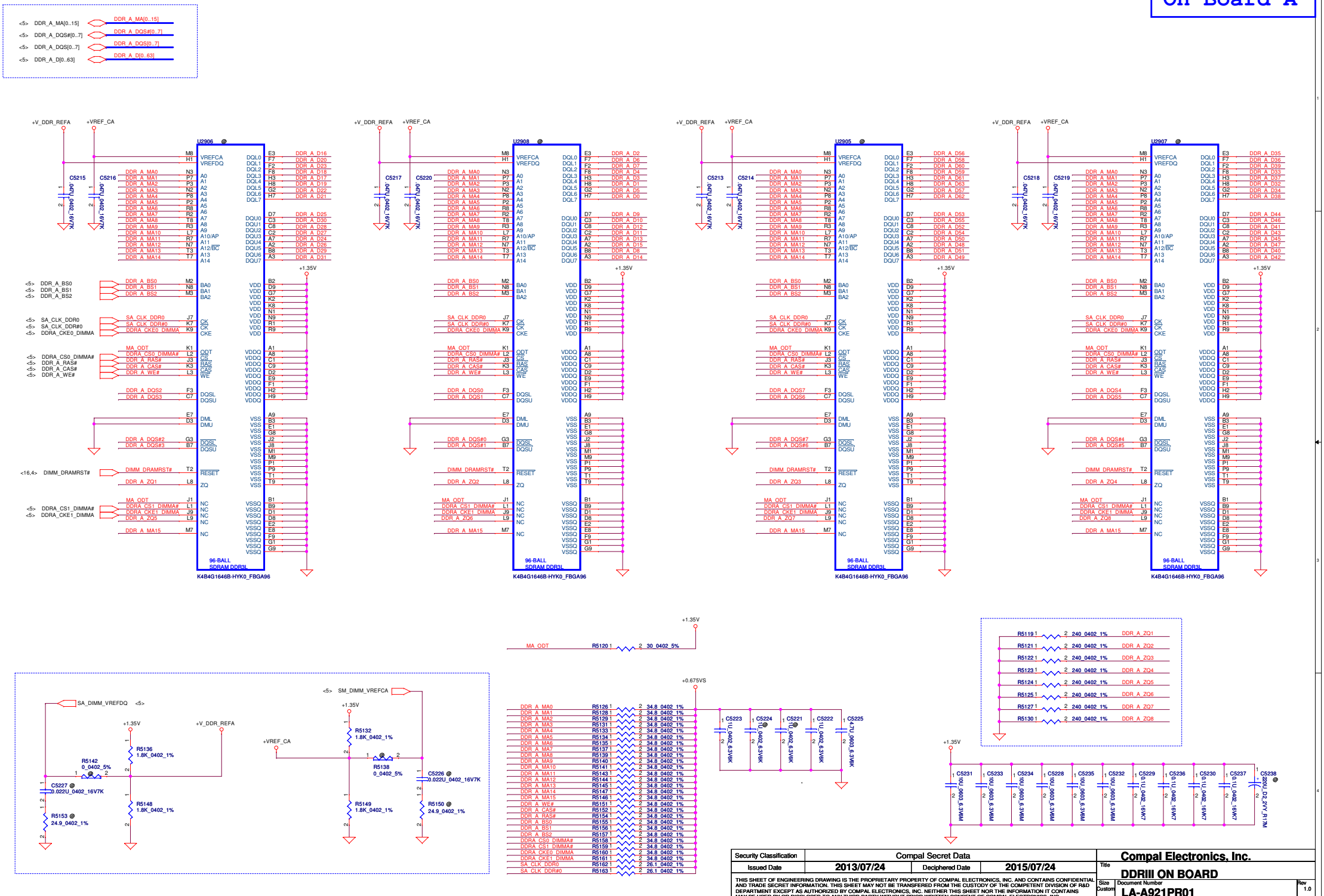
On Board A



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.

Title: **DDRIII ON BOARD**

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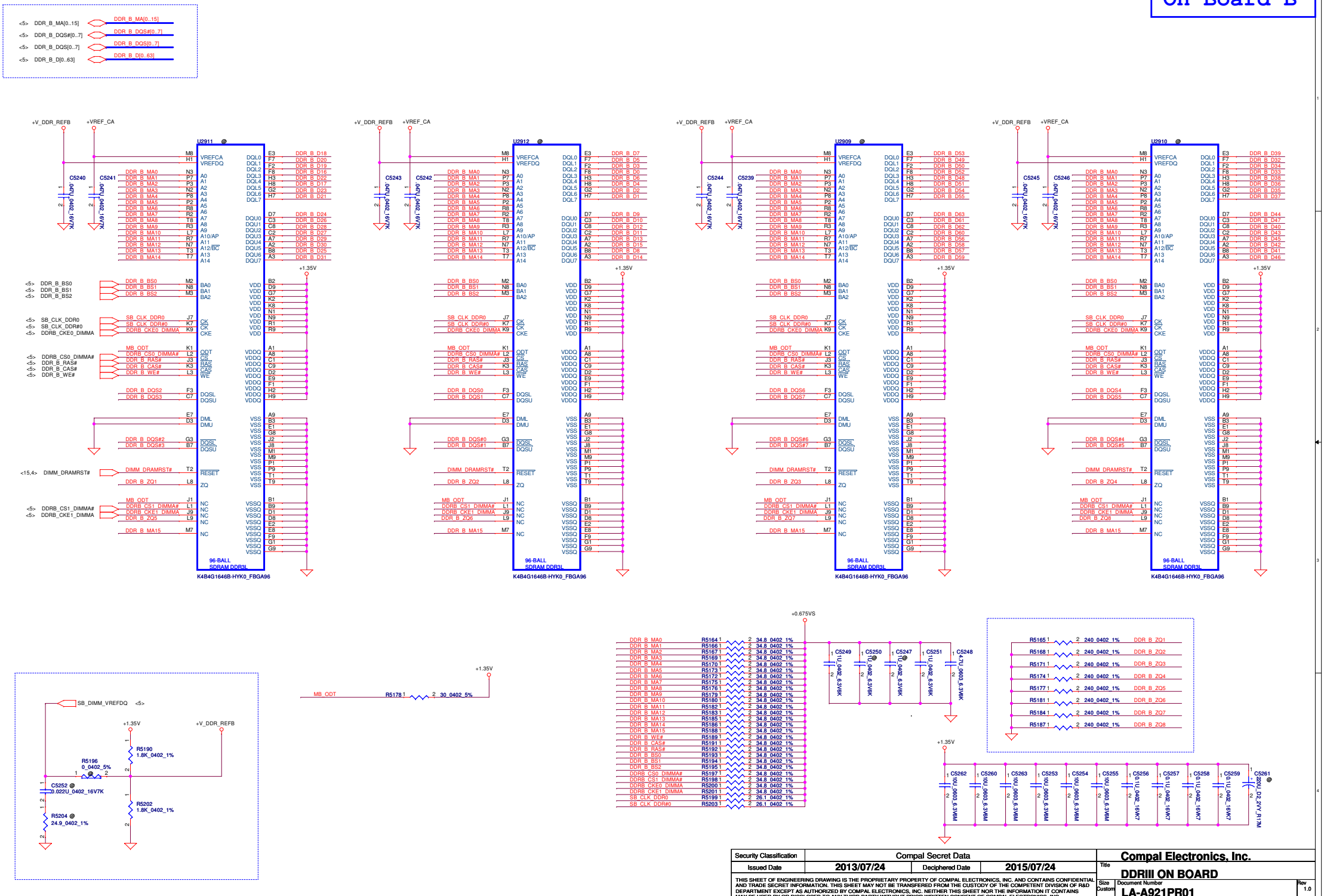
On Board B



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.

Title: **DDRIII ON BOARD**

Size	Document Number	Rev
Custom	LA-A921PR01	1.0

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600ohms @100MHz 2A
P/N: SM01000EE00

Place near Pin41 & 46

+5VS RA1531 2 0 0805 5%
+5VS_PVDD
CA1237 4.7U_0603_6.3V6K
CA1235 4.7U_0603_6.3V6K
CA1236 0.1U_0402_16V7
CA1238 0.1U_0402_16V7

+IOVDD_CODEC
+3VDD_CODEC
+5VDDA_CODEC
+1.5VS
RA1559 0_0402_5%
CA1232 1U_0402_6.3V6K
CA1231 0.1U_0402_16V7
CA1230 1U_0402_6.3V6K
Place near Pin26
+5VS LA41 0_0603_5%
Place LA41 on AGND/DGND moat

+3VS RA1529 0_0603_5%
+3VDD_CODEC CA1226 0.1U_0402_16V7
CA1227 1U_0402_6.3V6K
Place near Pin1
+IOVDD_CODEC CA1228 0.1U_0402_16V7
RA1530 2 0_0603_5%
+3VALW_PCH
Place near Pin9

UA1
DVDD DVDD-IO PVDD1 PVDD2 AVDD1 AVDD2

External MIC
W=40mils
W=40mils
W=40mils
<24> EXT_MIC_RING2
<24> EXT_MIC_SLEEVE
+MIC2-VREFO RA1594 2.2K 0402 5%
RA1595 2.2K 0402 5%
+LINE1-VREFO-R
<22> DMIC_DATA
<22> DMIC_CLK
EMI@ CA3 22P_0402_50V8J
L6 EMI@ BLM15BB221SN1D_2P~D
<19> EC_MUTE#
<6> HDA_RST_AUDIO#
RA15 2 0 0402 5% PDB
+IOVDD_CODEC RA27 100K 0402 5%
<24> PLUG_IN# RA18 200K 0402 1%
For ALC233-VB
CA23 1U 0402 6.3V6K
+3VDD_CODEC CA26 4.7U 0603 6.3V6K
+IOVDD_CODEC RA23 100K 0402 5%
For ALC233-VB
CA29 2.2U 0402 6.3V6M
RA21 2 0 0402 5%
RA21 pop on ALC283, NC on ALC233

LINE1-L
LINE1-R
LINE2-L
LINE2-R
MIC2-L(PORT-F-L) /RING2
MIC2-R(PORT-F-R) /SLEEVE
LINE1-VREFO-L
LINE1-VREFO-R
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
PDB
RESETB
PCBEEP
SENSE A
SENSE B
CBP
CBN
CPVDD
CPVREF
MIC-CAP
DVSS
Thermal PAD

ALC233-CG

SPK-OUT-L-
SPK-OUT-L+
SPK-OUT-R+
SPK-OUT-R-
HPOUT-L(PORT-I-L)
HPOUT-R(PORT-I-R)
SYNC
BCLK
SDATA-OUT
SDATA-IN
SPDIF-OUT/GPIO2
MONO-OUT
MIC2-VREFO
LDO3-CAP
LDO2-CAP
LDO1-CAP
VREF
JDREF
CPVEE
AVSS1
AVSS2

SPK_L1-
SPK_L2+
SPK_R2+
SPK_R1-
HP_OUTL
HP_OUTR
HDA_SYNC_AUDIO <6>
HDA_BITCLK_AUDIO <6>
HDA_SDOUT_AUDIO <6>
HDA_SDIN0 <6>
RA17 22_0402_5%
+MIC2-VREFO
CA22 2.2U 0402 6.3V6M
CA24 2.2U 0402 6.3V6M
CA25 2.2U 0402 6.3V6M
RA26 100K_0402_5%
CA31 1U_0402_6.3V6K
RA20 20K 0402 1%
CA30 1U_0402_6.3V6K
Place colose to UA1

ALC233-VB2_MQFN48_6X6

For EMI
RA1552 27_0402_5%
CA1247 33P_0402_50V8J

For ALC233 only
Place close to connector
+3VS +3VLP +3VALW
RA22 100K_0402_5%
RA24 100K_0402_5%
RA25 100K_0402_5%
EXT_MIC_SLEEVE
HDA_RST_AUDIO#
RA19 10K_0402_5%
CA32 1U_0402_6.3V6K
QA4 2N7002K_SOT23-3
QA5 2N7002K_SOT23-3

RA1549 0_0402_5%
RA1550 0_0402_5%
RA1551 0_0402_5%
RA1563 0_0402_5%
GND
GNDA

Place close to connector
HP_OUTL
HP_OUTR
RA2221 47_0603_5%
RA3331 47_0603_5%
HP_OUTL_R <24>
HP_OUTR_R <24>
LINE1-L CA35 2.2U 0402 6.3V6M
LINE1-R CA36 2.2U 0402 6.3V6M
RA556 4.7K 0402 5%
DA3 CH751H-40PT_SOD323-2
RA1596 4.7K_0402_5%
RA1597 4.7K_0402_5%
DA4 CH751H-40PT_SOD323-2
RA557 4.7K_0402_5%
+LINE1-VREFO-R
RA1561 10K_0402_5%
RA1562 10K_0402_5%
For Universal Audio Jack

PC Beep

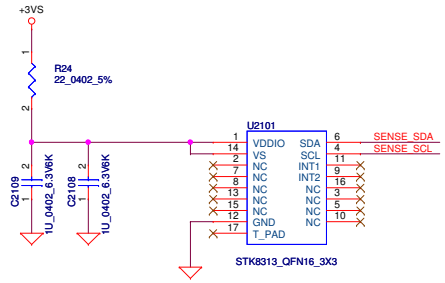
EC Beep <19> BEEP#
ICH Beep <9> SPKR
CA1252 0.1U_0402_16VK7
CA1253 2PC_BEEP1
0.1U_0402_16VK7
RA1557 1K_0402_5%
RA1558 10K_0402_5%
CA4434 PC_BEEP
0.1U_0402_16VK7

W=40mils
Place colose to JSPK1
SPK_R2+ R1357 0_0603_5% SPK_R2+_CONN
SPK_R1- R1356 0_0603_5% SPK_R1-_CONN
SPK_L1- R1358 0_0603_5% SPK_L1-_CONN
SPK_L2+ R1359 0_0603_5% SPK_L2+_CONN
JSPK1
ACES_50278-00401-001
ME@
For EMI
CA38 100P_0402_50V7K
CA39 100P_0402_50V7K
CA40 100P_0402_50V7K
CA43 100P_0402_50V7K
CA44 1000P_0402_50V7K
EMI@
vendor suggest
change to 1000p

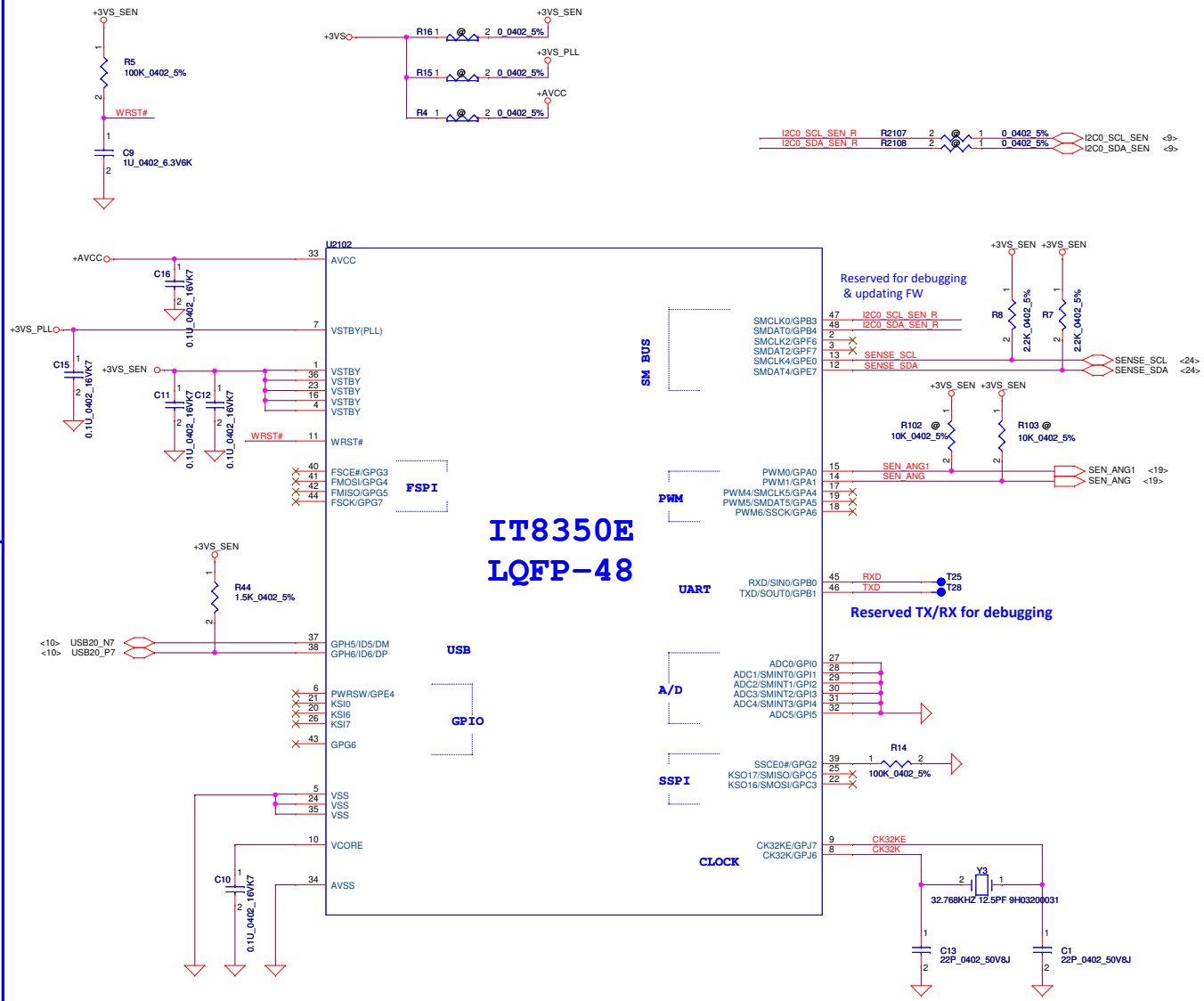
Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.
Title: CODEC ALC233/Speaker CONN
Size: Custom | Document Number: LA-A921PR01 | Rev: 1.0
Date: Tuesday, December 17, 2013 | Sheet 17 of 38

2nd G-sensor



Sensor Hub



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.

Title: Sensor Fusion

Size	Document Number	Rev
Custom	LA-A921PR01	1.0

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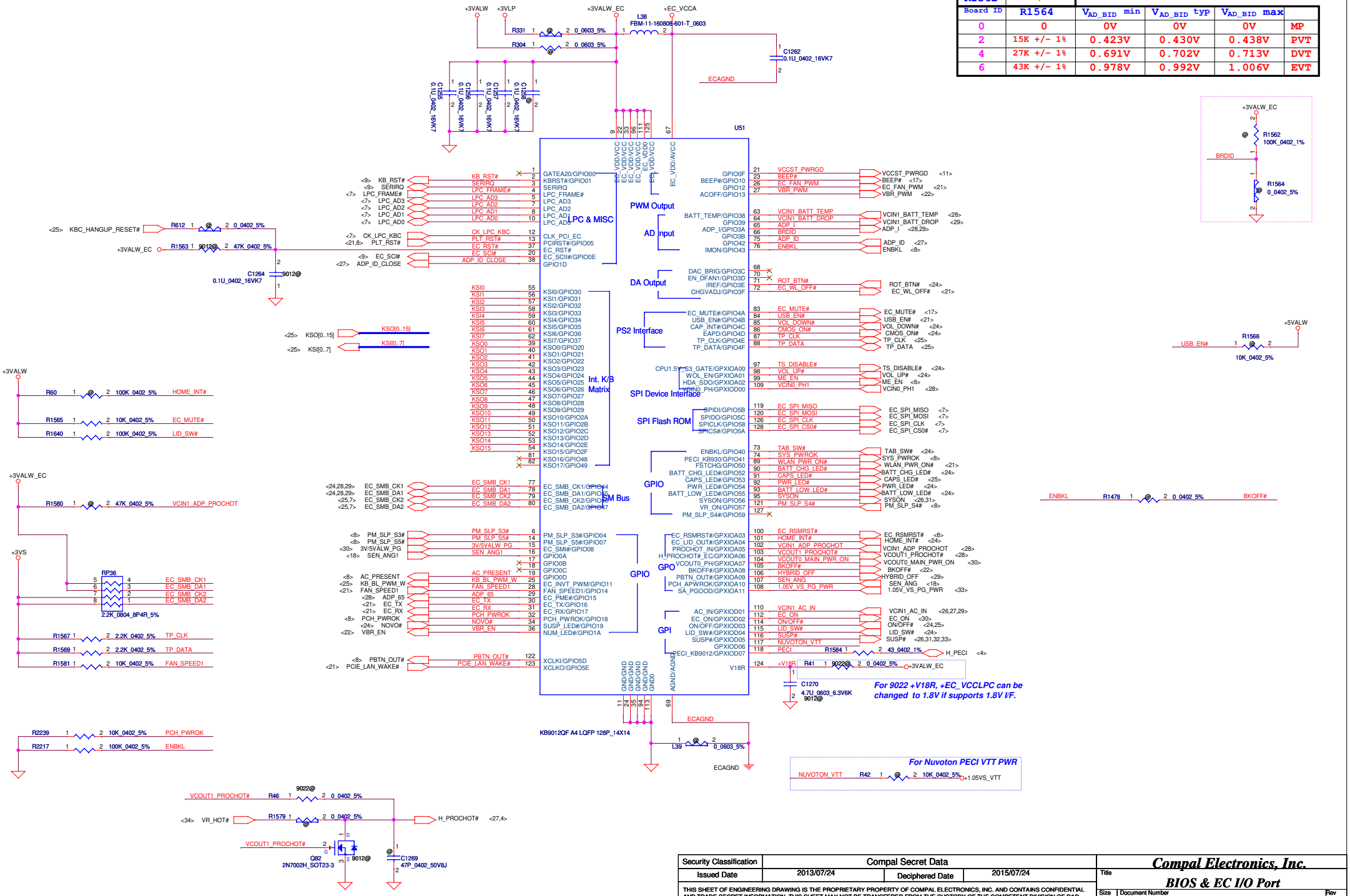
Vcc	3.3V
R1562	100K +/- 1%

Board ID	R1564	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0V	0V	0V	MP
2	15K +/- 1%	0.423V	0.430V	0.438V	PVT
4	27K +/- 1%	0.691V	0.702V	0.713V	DVT
6	43K +/- 1%	0.978V	0.992V	1.006V	EVT



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	LA-A921PR01	1.0

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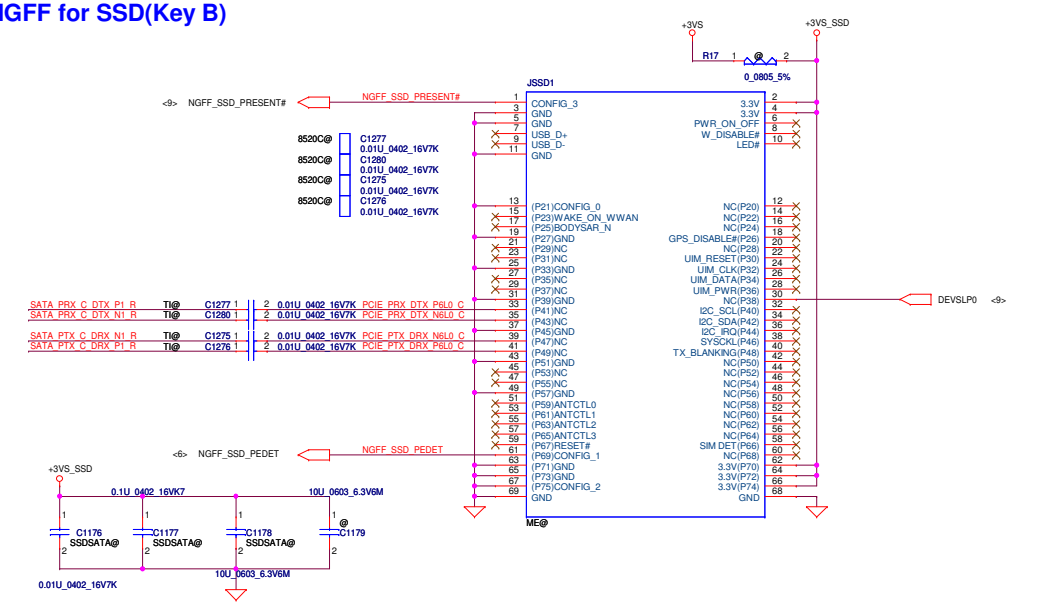
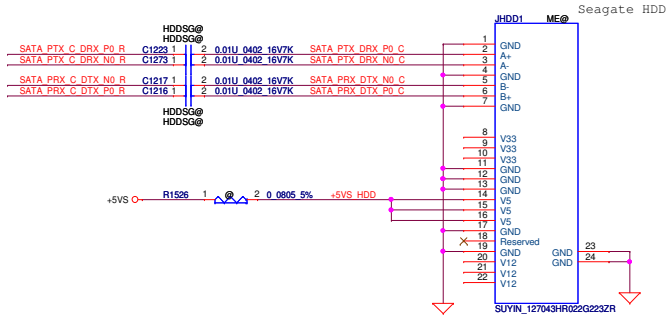
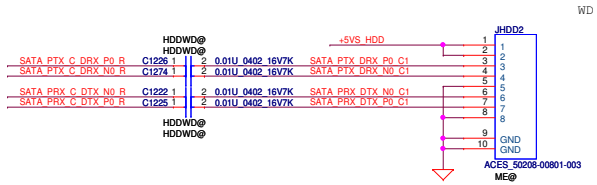
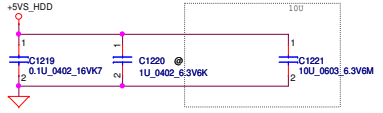
NGFF for SSD(Key B)

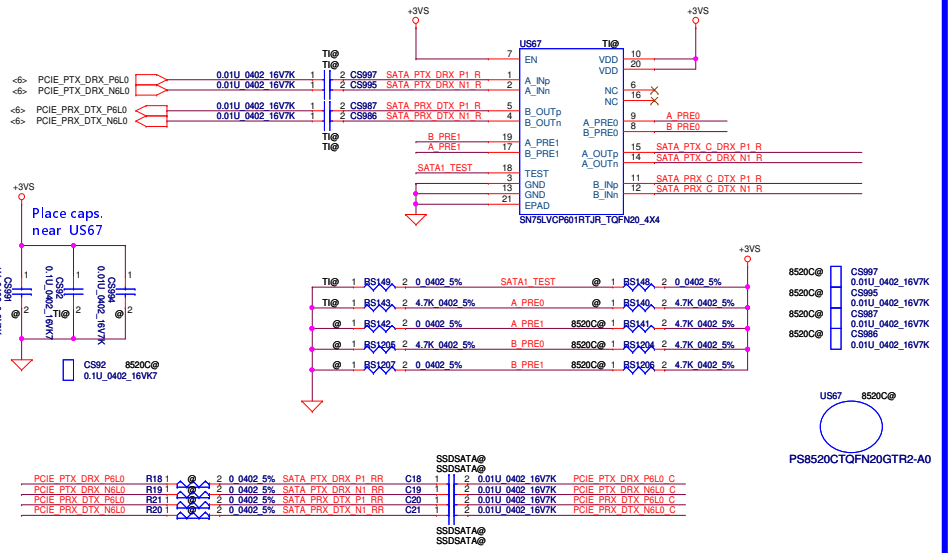


SATA HDD CONN.



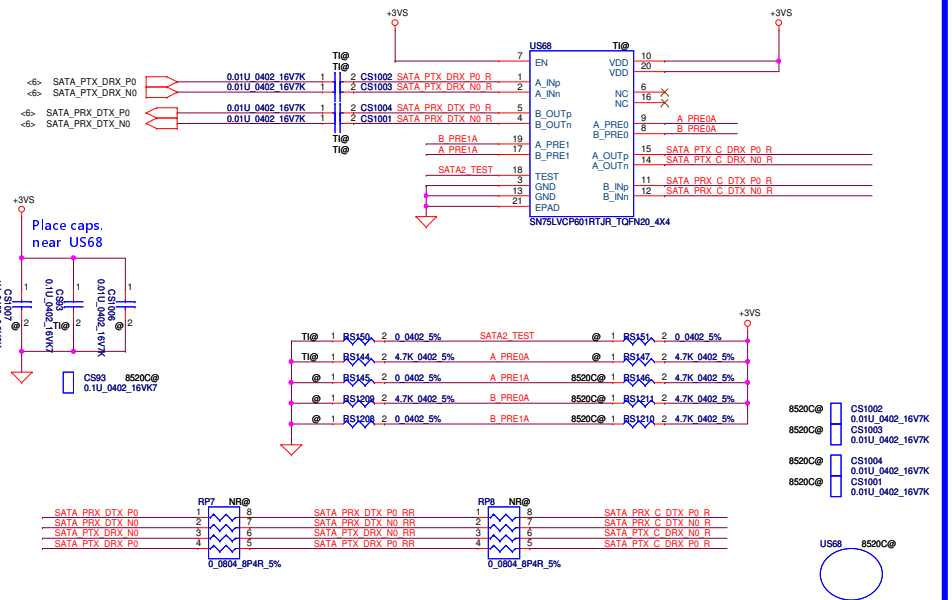






BOM Setting

PARADE 8520C	8520C@
TI	TI@



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.			
Title: HDD/ SSD			
Size: C	Document Number: LA-A921PR01		Rev: 1.0
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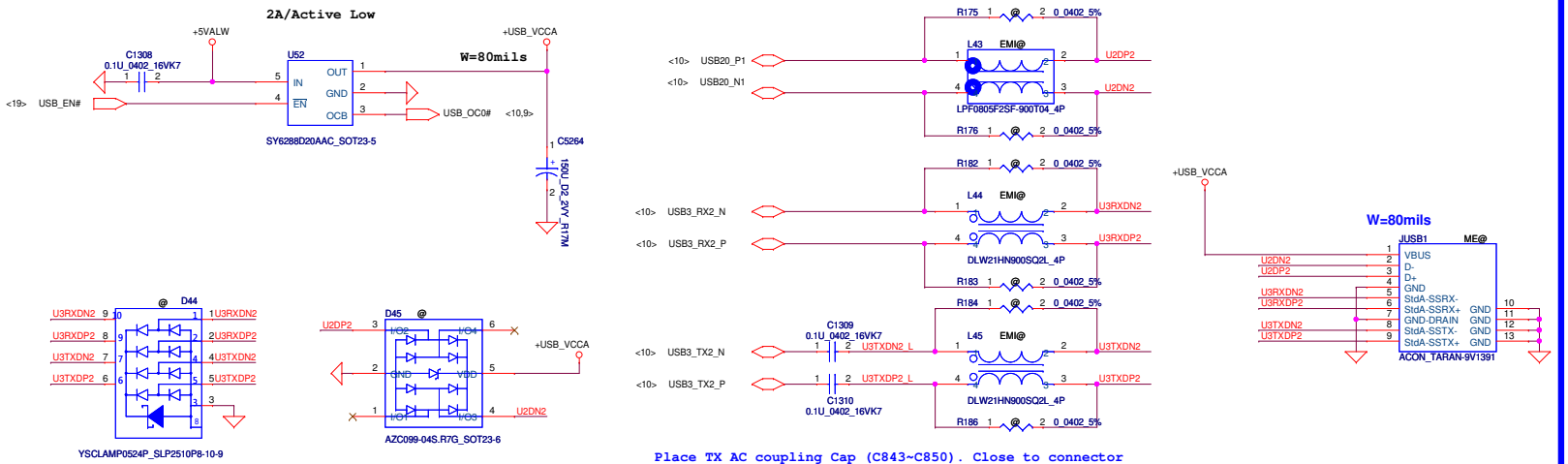
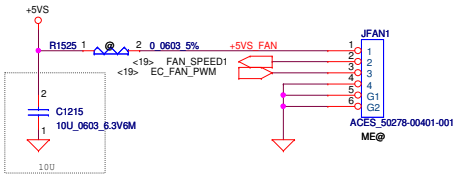
USB 3.0 Conn.



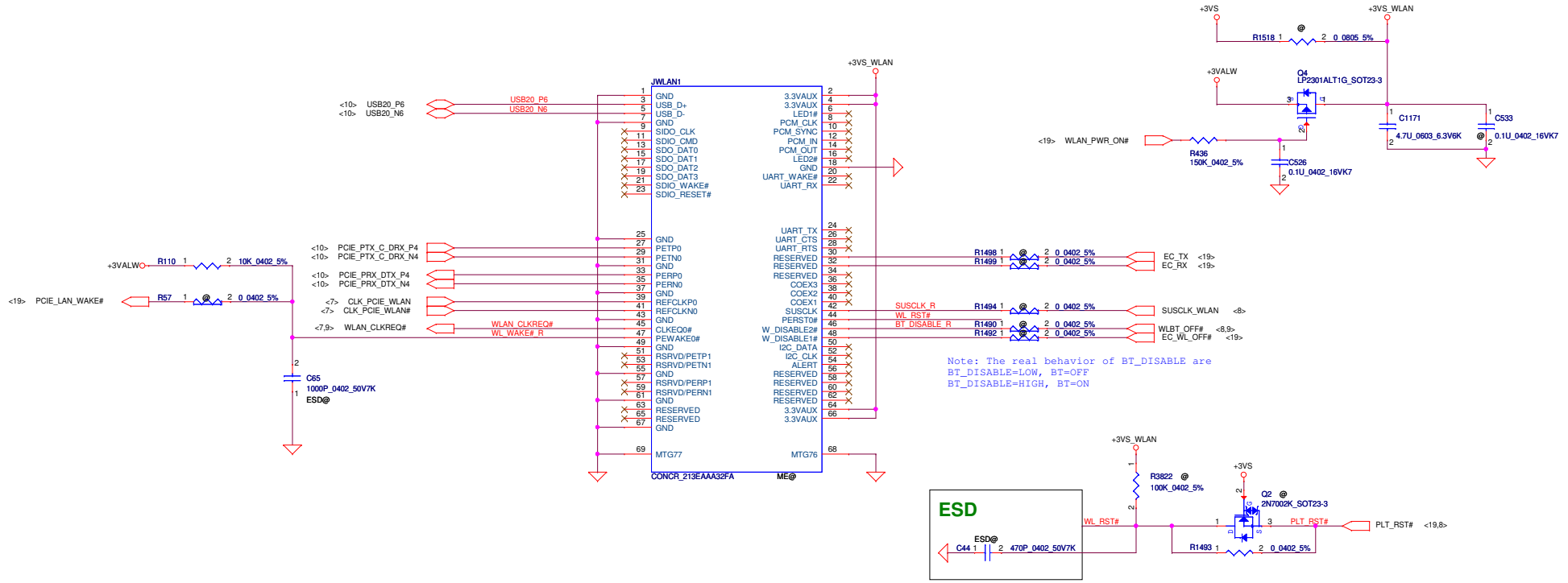
Place TX AC coupling Cap (C843~C850). Close to connector

FAN CONN.

FAN1 Conn



NGFF for WLAN(Key E)



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.			
Title	USB3.0/WLAN/FAN		
Size	Document Number	LA-A921PR01	Rev 1.0
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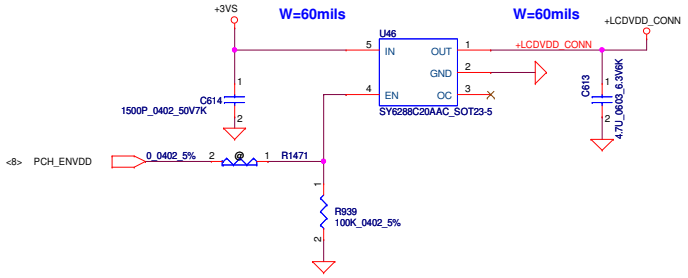
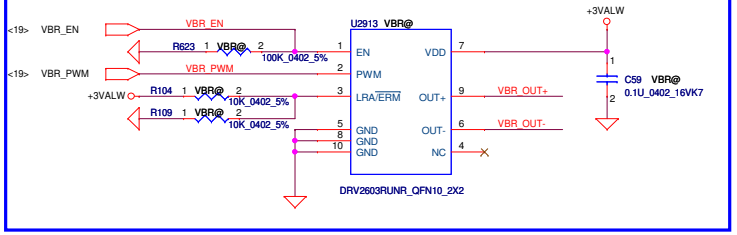
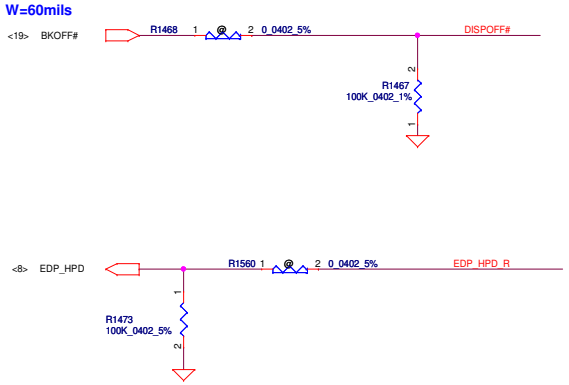
LCD POWER CIRCUIT



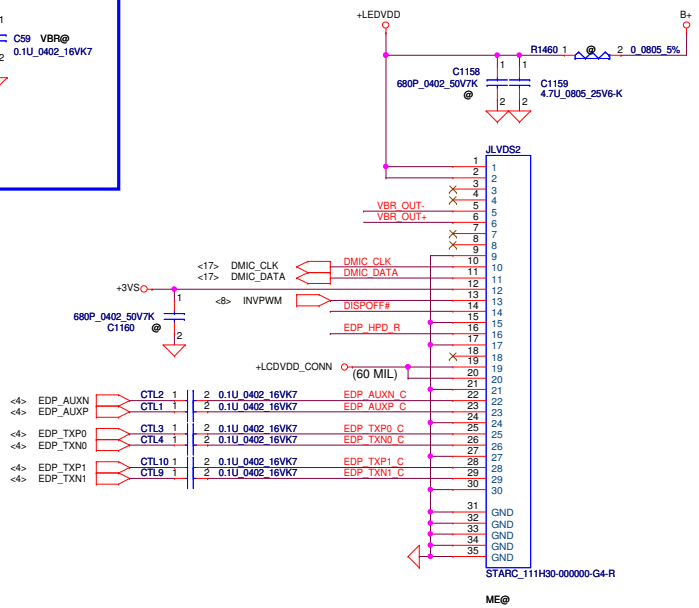
Vibrator drive IC

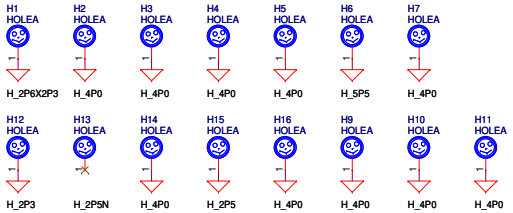


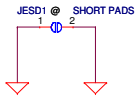
RTD2132R Internal load switch for +LCD_VCC



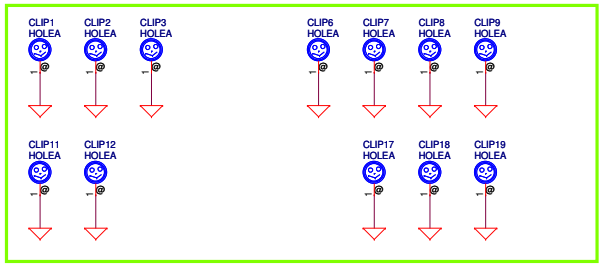
eDP PANEL BD. Conn.







Shielding Clip



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.

Title: eDP /DMIC/ HOLE

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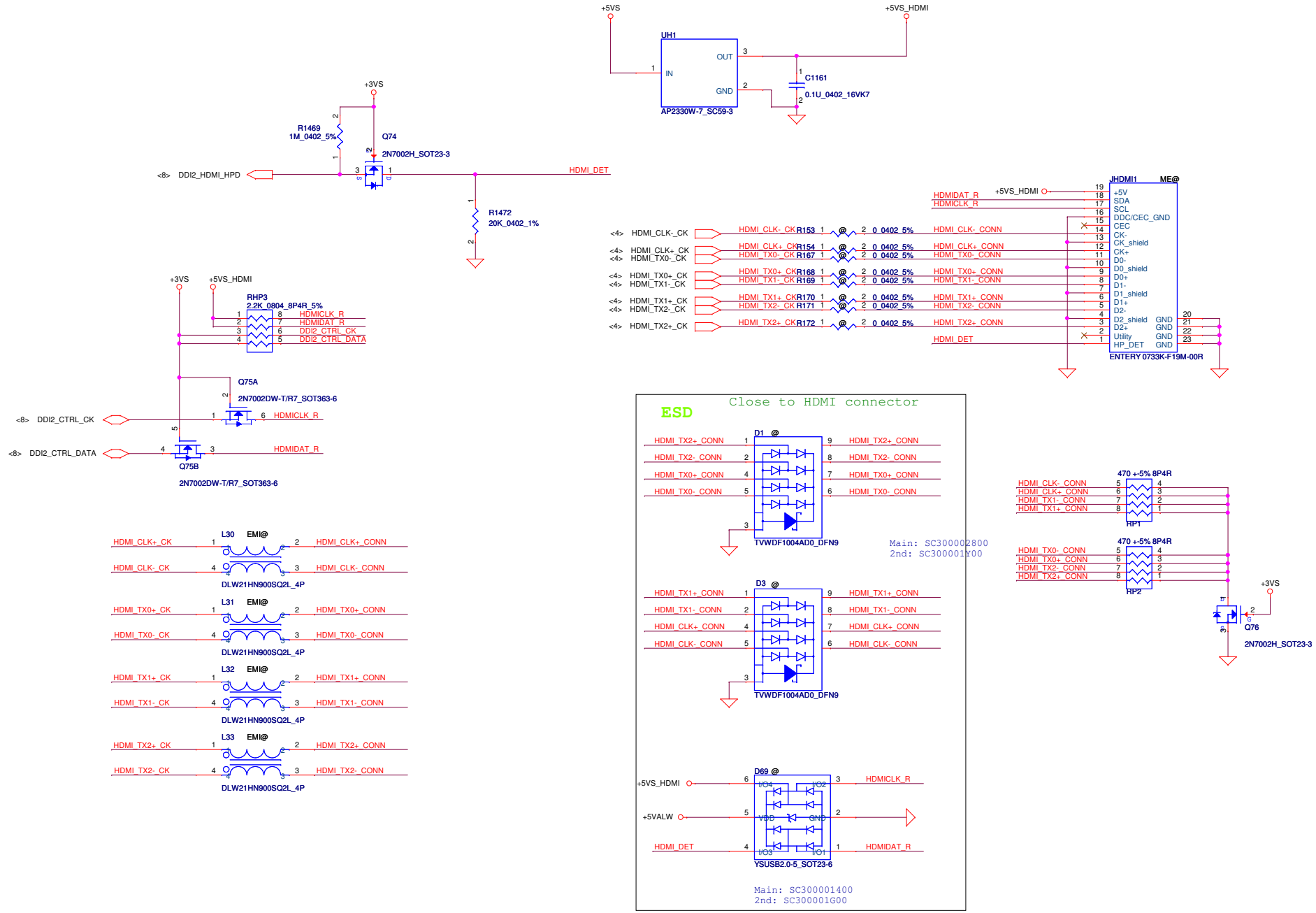

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/07/24	Deciphered Date 2015/07/24	Title: HDMI CONN

Size: Custom	Document Number: LA-A921PR01		Rev: 1.0
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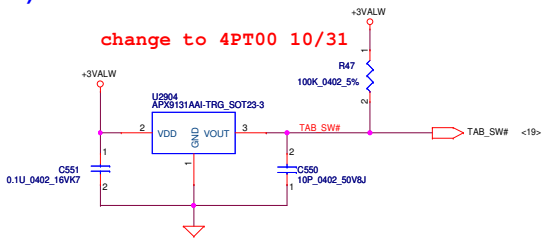
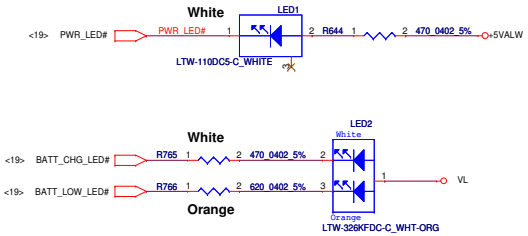
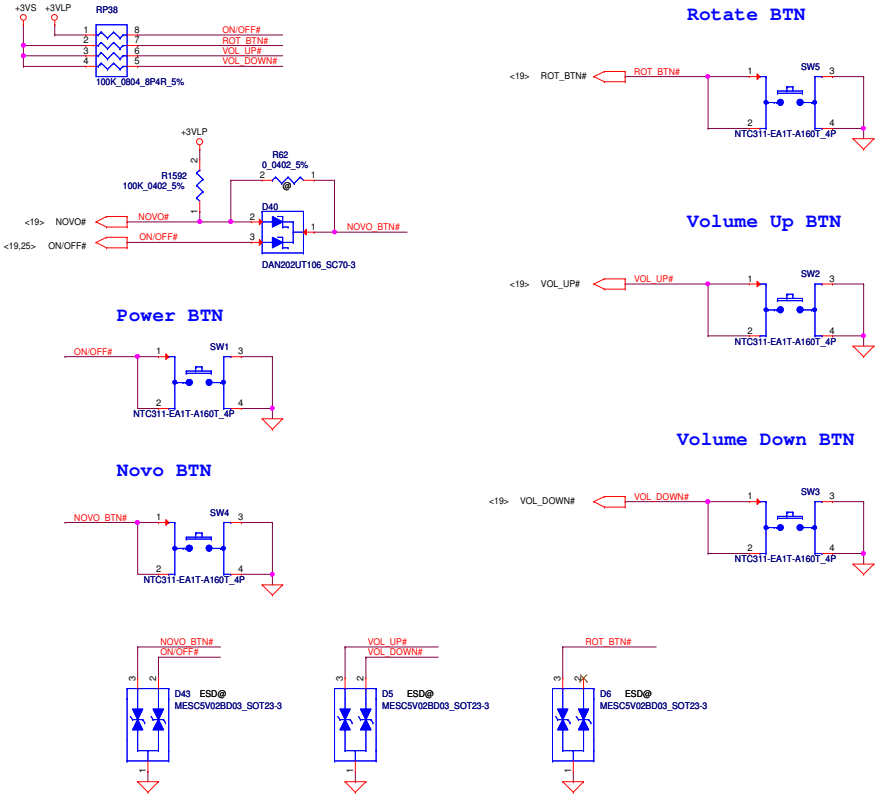
Lid SW(Tablet Mode)



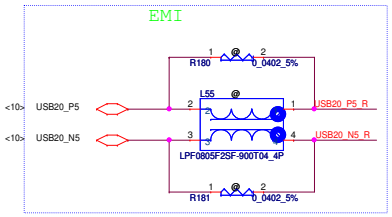
LED

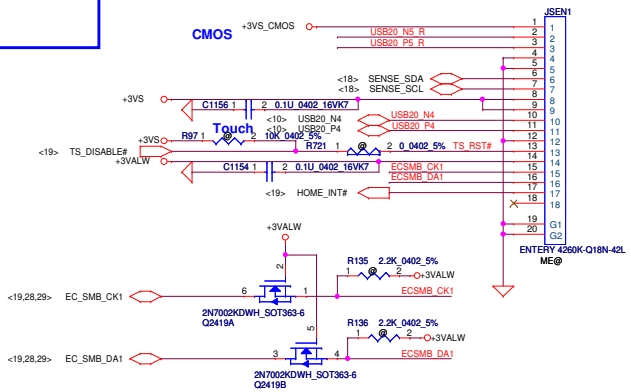


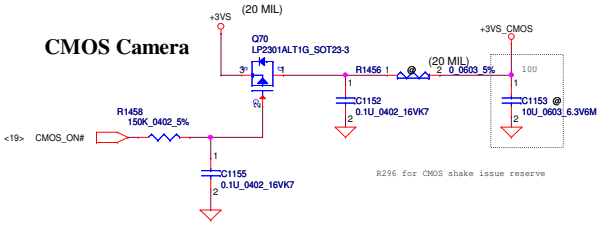
BUTTON



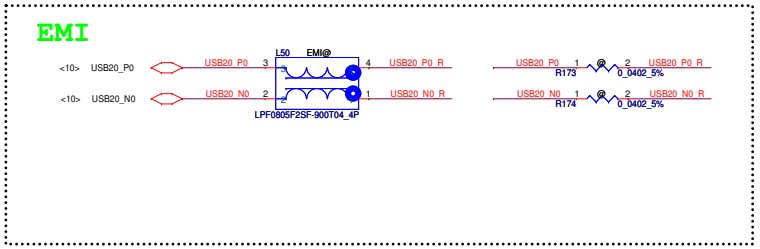
Touch & CMOS Conn

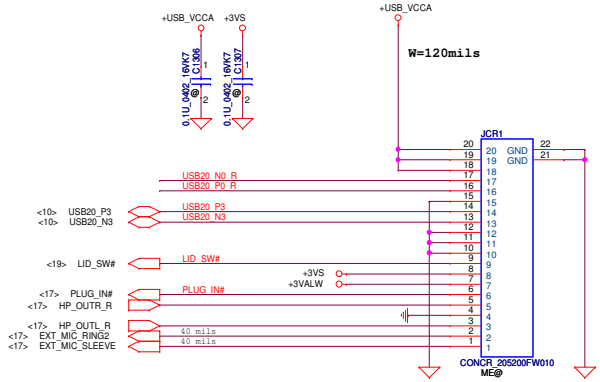






I/O Board





Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.			
Title: Daughter board/LED/BTN/LID			
Size: C	Document Number: LA-A921PR01		Rev: 1.0
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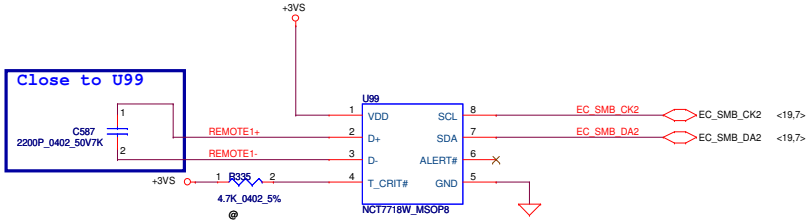
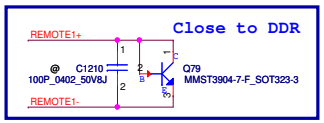
Thermal Sensor

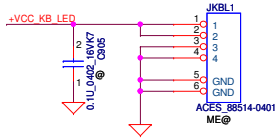


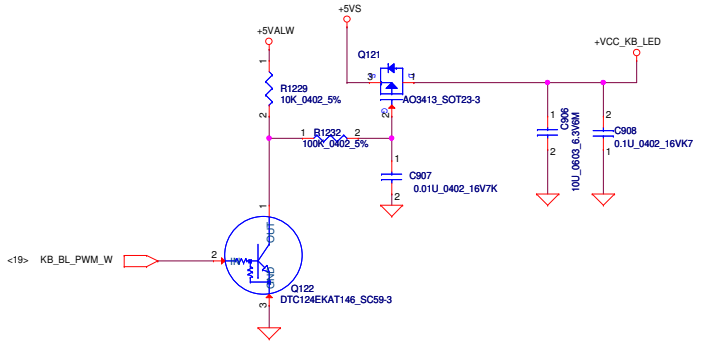
SMBus address: 1001100x

REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

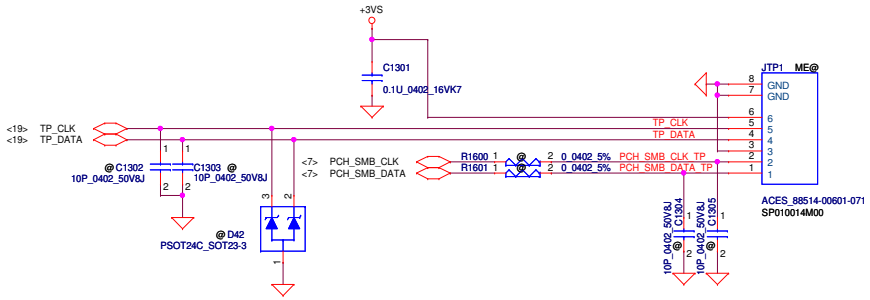


Keyboard Backlight

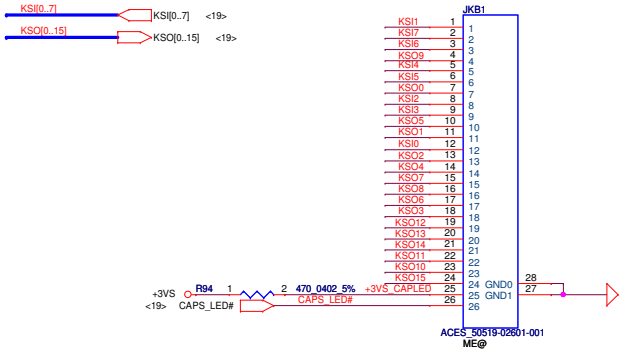




Click Pad

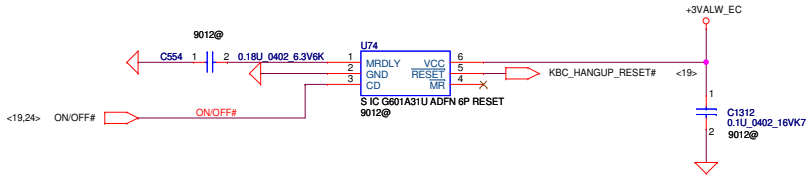


Keyboard



EC Reset IC

EC RESEST function



Compal Electronics, Inc.			
Title: KB/TP/Thermal Sensor			
Size: Custom	Document Number: LA-A921PR01		Rev: 1.0
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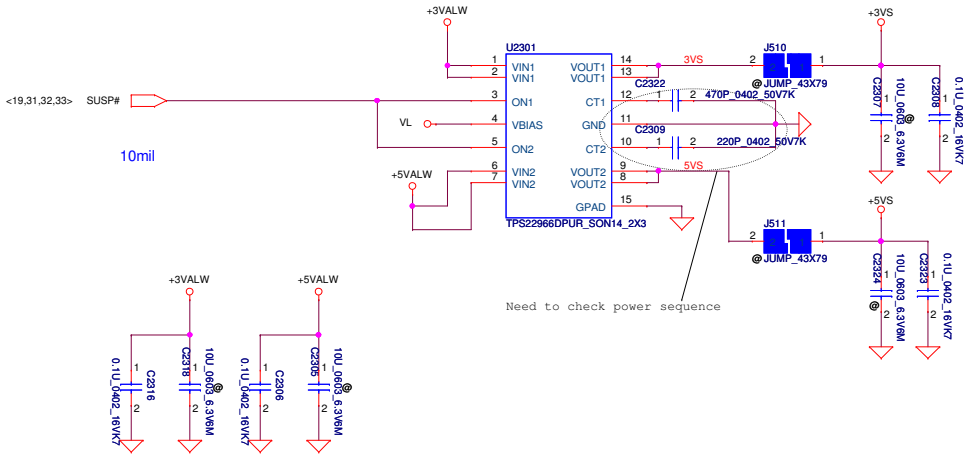
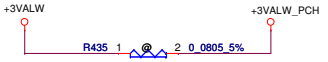
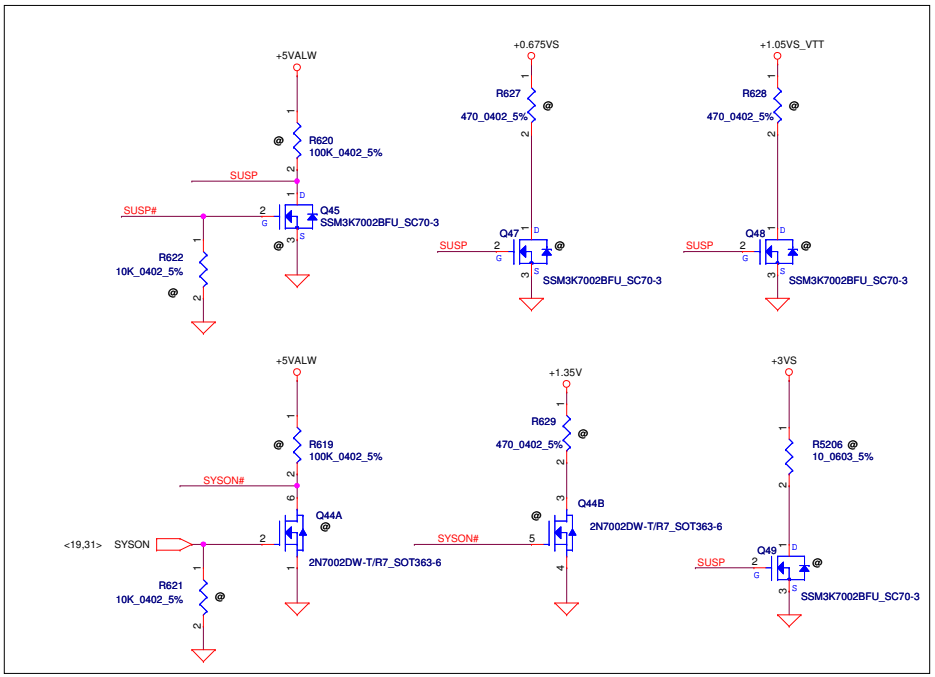
+5VALW TO +5VS
+3VALW TO +3VS

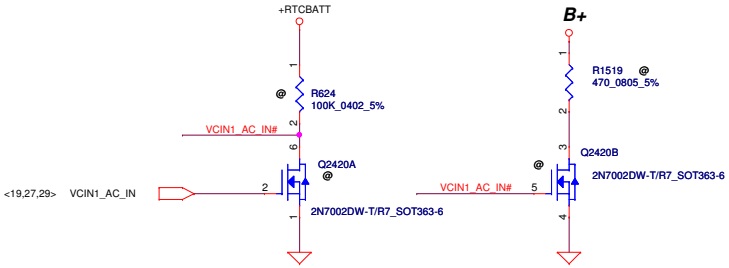


+3VALW TO +3VALW(PCH AUX Power)
+5VALW TO +5VALW(PCH AUX Power)



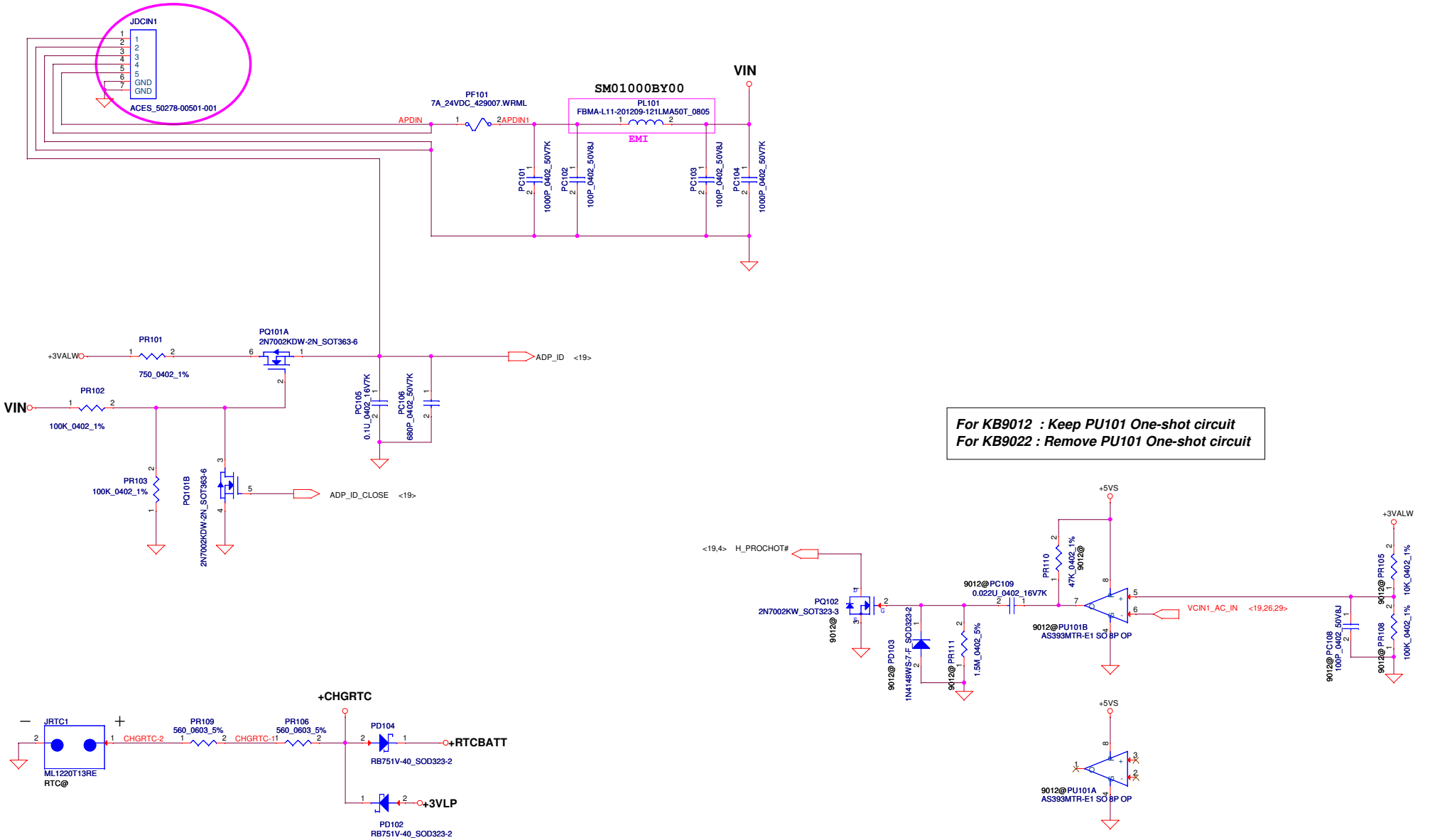


B+ dischager



Security Classification	Compal Secret Data		
Issued Date	2013/07/24	Deciphered Date	2015/07/24

Compal Electronics, Inc.			
Title: DC V TO VS INTERFACE			
Size: Custom	Document Number: LA-A921PR01		Rev: 1.0
Date: Tuesday, December 17, 2013	Sheet 26 of 38		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

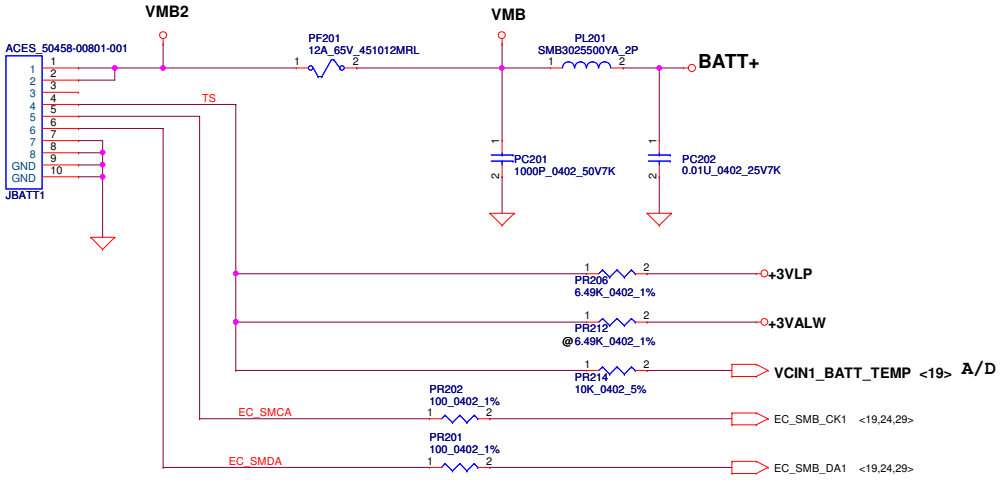
Size	Document Number	Rev
Custom	Gx00	1.0

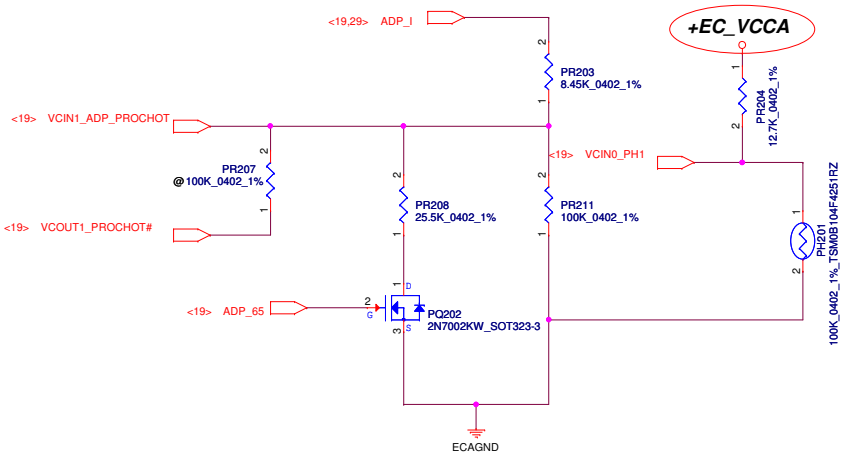
Date: Tuesday, December 17, 2013 Sheet 27 of 38

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

65W(UMA): 85W active W recovery

20120314
Change to +EC_VCCA from +3VLP





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

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Module model information

BQ24715_V2.mdd

65W adapter support NVDC
BQ24715 support 2, 3 cell
BQ24717 for 4 cell

H/MOS
Rds(on)= 24m ohm(typ), 30m ohm(Max.)
power loss= 0.9944W
L/MOS
Rds(on)= 9.9m ohm(typ), 13m ohm(Max.)
power loss= 0.3396W
Pd of Choke = 0.9892W

Cell PIN
Float: 2cell
High: 3cell
GND: disable LEARN

Vin Dectector

	Min.	Typ	Max.
L-->H	17.578V	17.755V	17.933V
H-->L	17.023V	17.349V	17.674V

pacement near EC

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number | Rev 1.0

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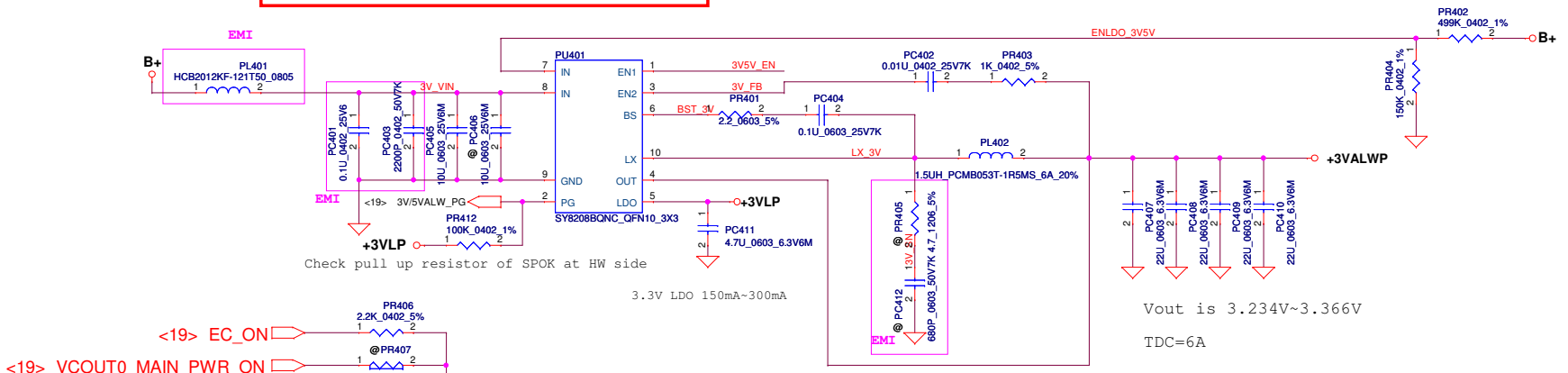
Module model information

SY8208B_V2.mdd

EN1 and EN2 dont't floating

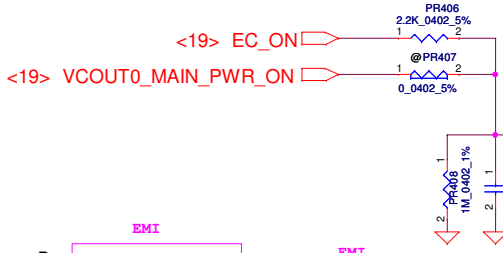


Check pull up resistor of SPOK at HW side

3.3V LDO 150mA~300mA

Vout is 3.234V~3.366V

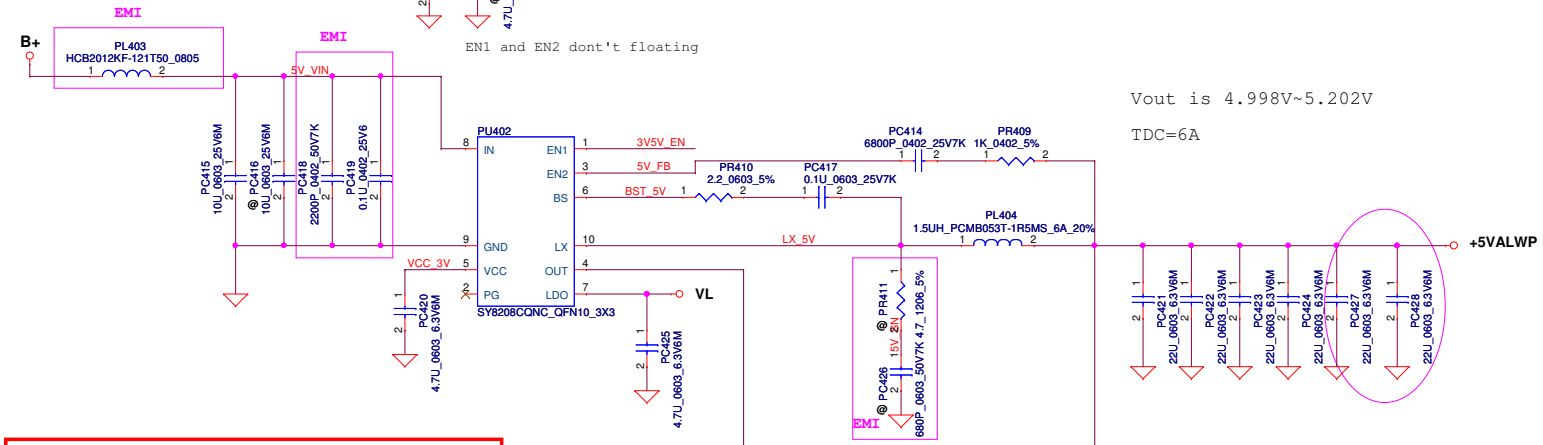
TDC=6A



EC VDD0 is +3VL, PC13 UNPOP

EC VDD0 is +3VALW, PC13 POP

EN1 and EN2 dont't floating



Vout is 4.998V~5.202V

TDC=6A

5V LDO 150mA~300mA

Module model information

SY8208C_V2.mdd

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

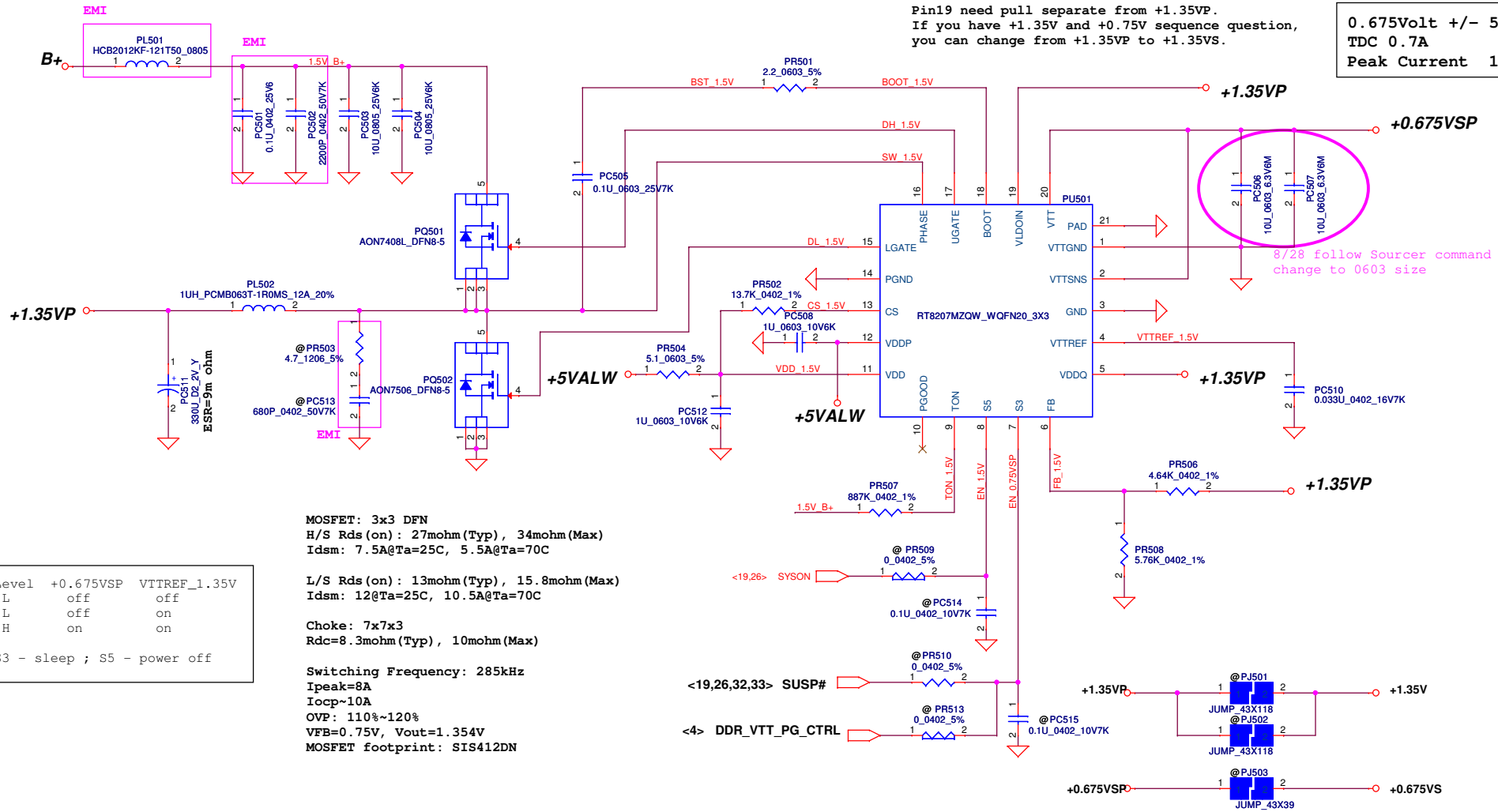
Title: +3VALW/+5VALW

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, December 17, 2013 | Sheet 30 of 38

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 13mohm(Typ), 15.8mohm(Max)
Idsm: 12@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=8A
Iocp~10A
OVP: 110%~120%
VFB=0.75V, Vout=1.354V
MOSFET footprint: SIS412DN

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

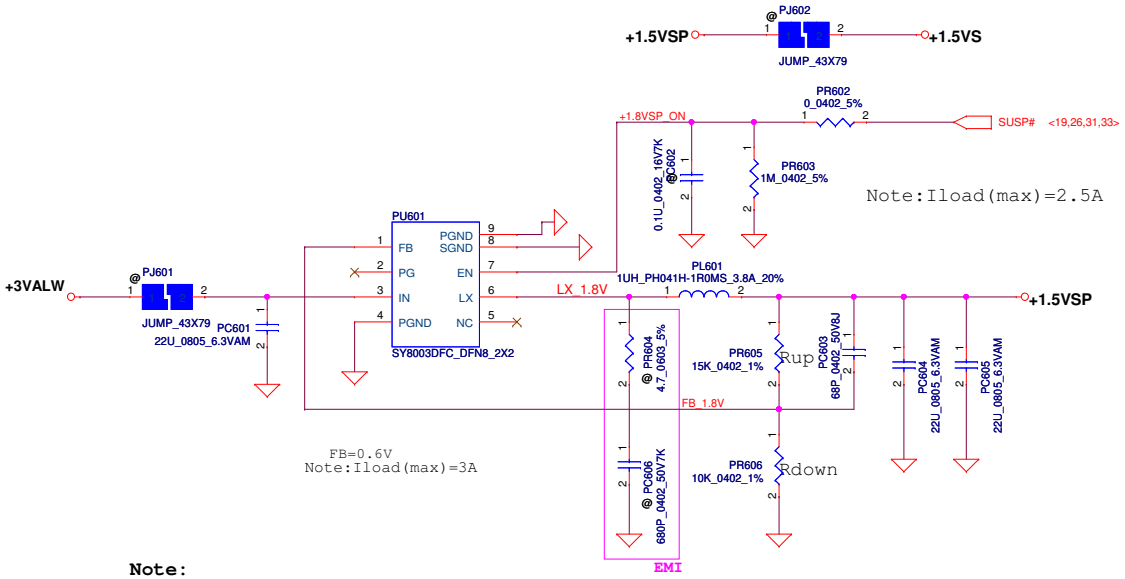
Title: +1.35VP/+0.675VSP

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, December 17, 2013 | Sheet 31 of 38

Module model information

SY8003_V1.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
Vout=1.5V

Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

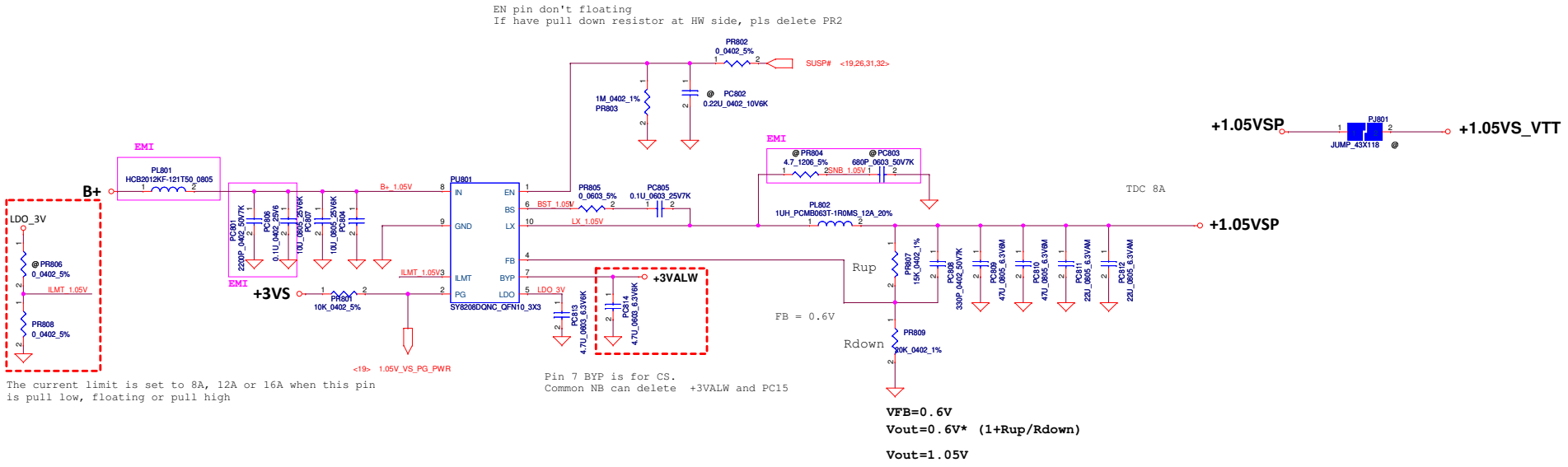
Title: **+1.5VSP**

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, December 17, 2013 | Sheet 32 of 38

Module model information

SY8208D_V1.mdd



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +1.05VSP

Size	Document Number	Rev
C		1.0

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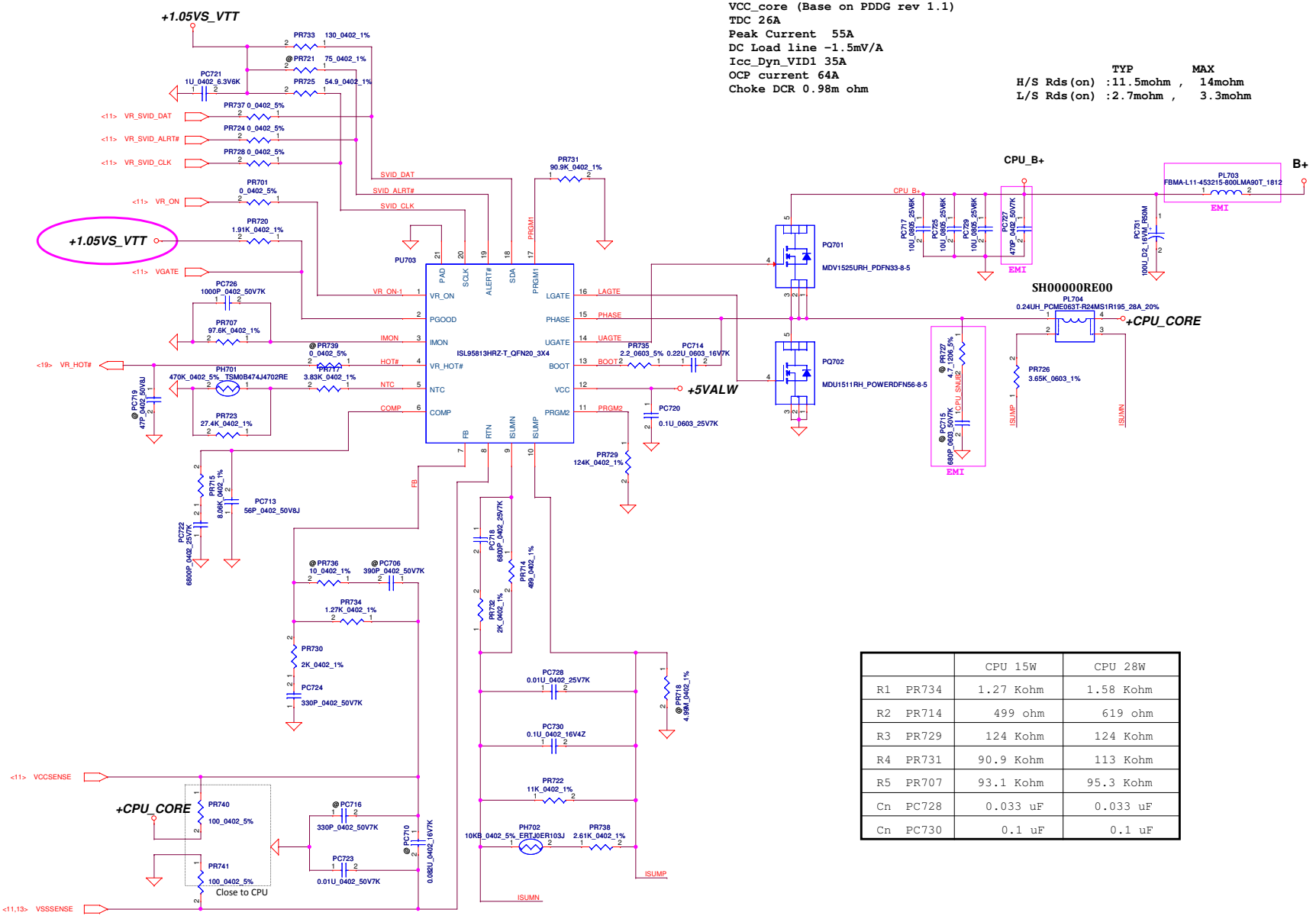
VCC_core (Base on PDDG rev 1.1)
TDC 26A
Peak Current 55A
DC Load line -1.5mV/A
Icc_Dyn_VID1 35A
OCP current 64A
Choke DCR 0.98m ohm

	TYP	MAX
H/S Rds(on)	:11.5mohm ,	14mohm
L/S Rds(on)	:2.7mohm ,	3.3mohm



	CPU 15W	CPU 28W
R1 PR734	1.27 Kohm	1.58 Kohm
R2 PR714	499 ohm	619 ohm
R3 PR729	124 Kohm	124 Kohm
R4 PR731	90.9 Kohm	113 Kohm
R5 PR707	93.1 Kohm	95.3 Kohm
Cn PC728	0.033 uF	0.033 uF
Cn PC730	0.1 uF	0.1 uF

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/08	Deciphered Date 2015/07/08	Title CPU_COREP
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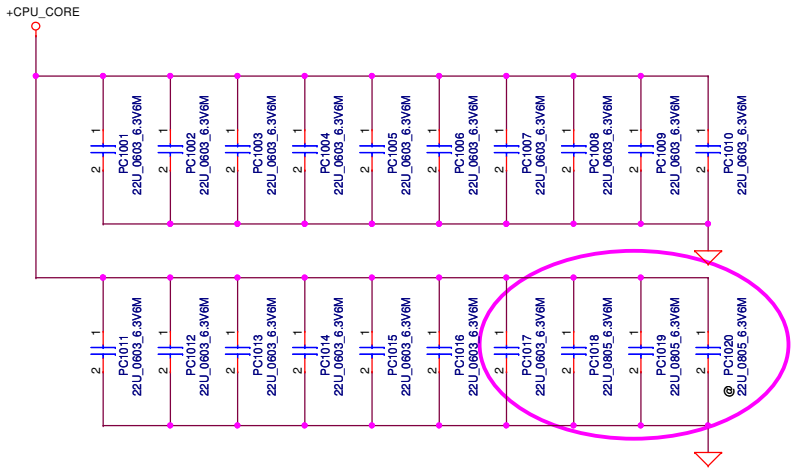
CPU_CORE output cap-->36.4



30 X 22uF 0805
2012/10/23
check the output cap Qty!!!
2012/10/24
23 pcs 22uF and reserve 7 pcs
2013/01/14
22uF*15; reserve 22uF*5

2013/09/6 22U_0603x17 + 22U_0805x2

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

Size | Document Number: **PMIC** | Rev: 1.0

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Phase
1	For ME design change	21,23	JHDMI1,JUSB1 change connector type	EVT
2	For ME design change	24	SW1,SW2,SW3,SW4,SW5 change type	EVT
3	For ME design change	24,25	JCR1,JKB1 change connector type	EVT
4	For EC pin common design	19	EC pin 25,27,38,86,123 control pin change	EVT
5	Follow EC power plane for EC_Reset	25	Change U74 power plan	EVT
6	For DVT phase MB ID	19	R1564 change from 43K to 27K	EVT
7	For BDW HDMI request	23	RP1,RP2 change value from 680ohm to 470ohm	EVT
8	For Audio vender recommend	17	1. Un-mount RA19,RA22 2. Mount RA1551,RA1563 3. Add CA1,CA2	EVT
9	For EMI request	17	R55 change to Bead	EVT
10	For Compal component policy	9,21	U52,U4 change type	EVT
11	For touch vennder recommend	24	1. JSEN1 pin 13 add 10K pull high 2. JSEN1 pin 14 change to +3VALW	EVT
12	For SPEC change	6,20	Delete SSD PCIE interface component	EVT
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Title: PIR (EE)
Size: Custom | Document Number: LA-A321P | Rev: 1.0
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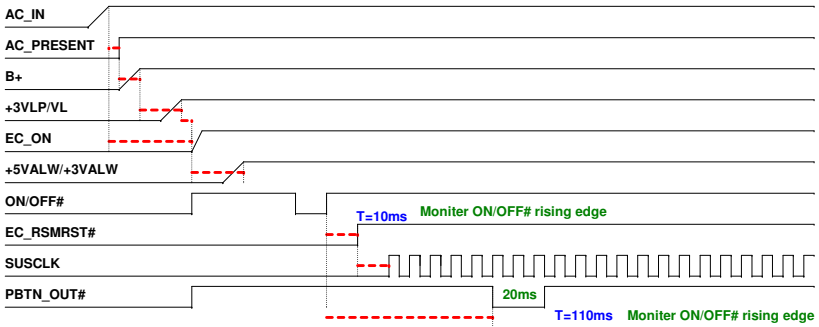
[AC Mode]



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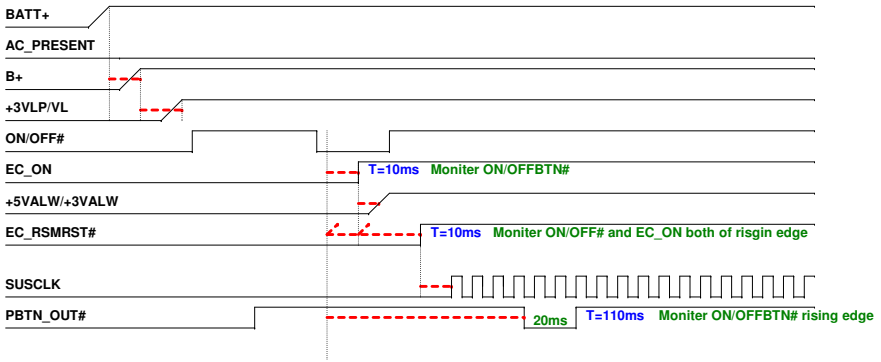

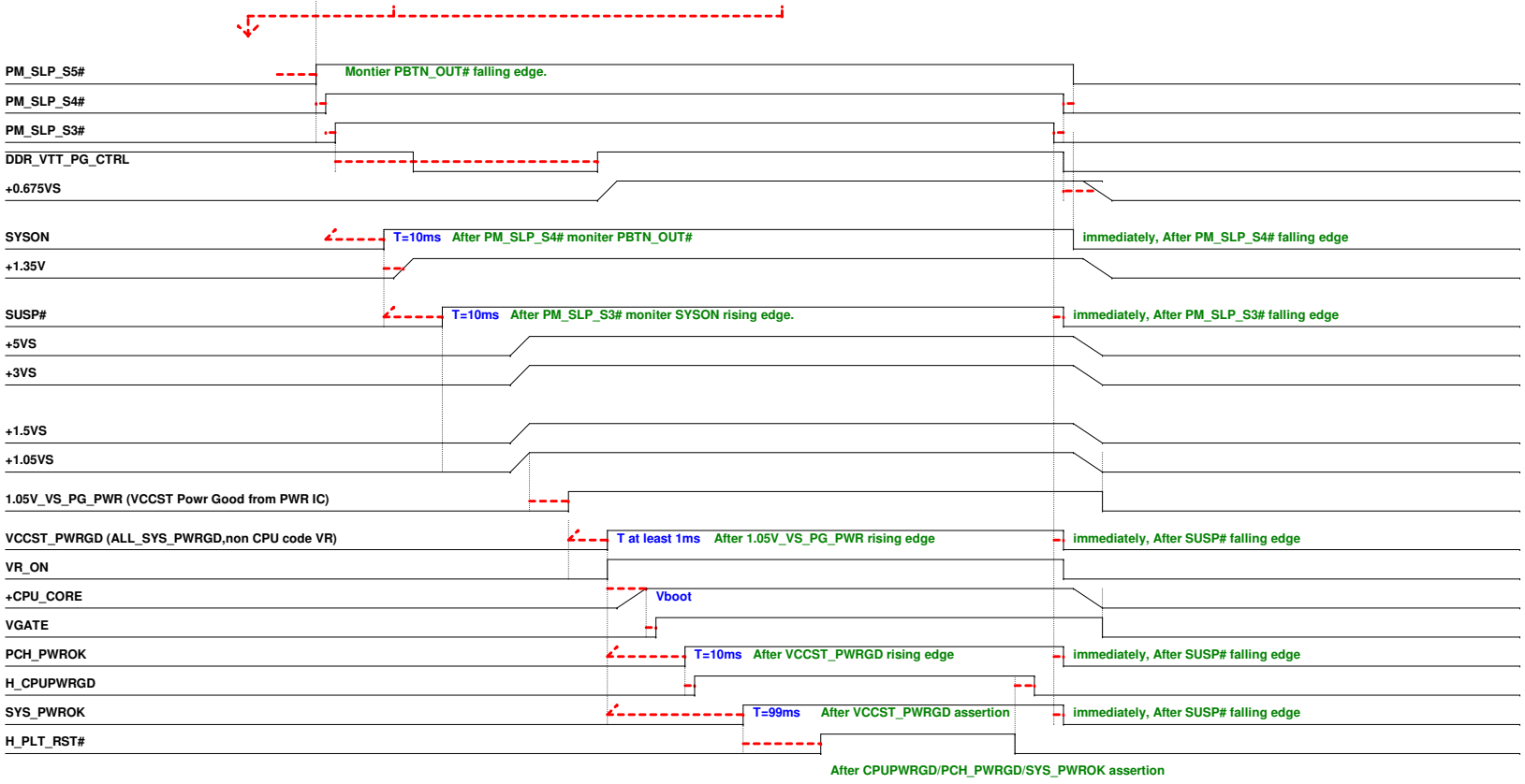

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Title: Power Sequence

Size | Document Number | Rev 1.0

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