

Service Manual



Service Manual

LG-C105



Model : LG-C105

Table Of Contents

1. INTRODUCTION	5	4.12 Microphone Trouble	94
1.1 Purpose.....	5	4.13 SIM Card Interface Trouble.....	96
1.2 Regulatory Information	5	4.14 KEY backlight Trouble	98
1.3 Abbreviations.....	7	4.15 Micro SD (uSD) Trouble.....	100
2. PERFORMANCE.....	9	4.16 Bluetooth Trouble.....	102
2.1 H/W Features.....	9	4.17 FM Radio Trouble	104
2.2 Technical Specification	11	5. DOWNLOAD.....	106
3. TECHNICAL BRIEF	16	6. BLOCK DIAGRAM.....	119
3.1 Digital Main Processor	16	7. CIRCUIT DIAGRAM	121
3.2 Power Management.....	21	8. BGA PIN MAP	127
3.3 FEM with integrated Power Amplifier Module (SKY77547, U400)	33	9. PCB LAYOUT	133
3.4 Crystal(26 MHz, X100).....	35	10. ENGINEERING MODE	137
3.5 RF Subsystem of PMB8810 (U100).....	36	11. STAND ALONE TEST	138
3.6 MEMORY(PF38F5060M0Y0BE, U101).....	41	11.1 Introduction	138
3.7 BT module	43	11.2 Setting Method.....	138
3.8 SIM Card Interface.....	45	11.3 Tx Test.....	141
3.9 LCD Interface.....	46	11.4 Rx Test	142
3.10 Battery Charger Interface	49	12. AUTO CALIBRATION.....	143
3.11 Keypad Interface	50	12.1 Overview	143
3.12 Audio Front-End	52	12.2 Configuration of HotKimchi	143
3.13 Camera Interface(2M Fixed Focus Camera).....	58	12.3 Description of Basic File	144
3.14 KEY BACKLIGHT LED Interface.....	60	12.4 Procedure.....	145
3.15 Vibrator Interface	61	12.5 AGC	148
4. TROUBLE SHOOTING	62	12.6 APC	148
4.1 RF Component.....	62	12.7 ADC.....	148
4.2 RX Trouble	63	12.8 Target Power	148
4.3 TX Trouble	67	13 EXPLODED VIEW & REPLACEMENT PART LIST	149
4.4 Power On Trouble.....	71	13.1 EXPLODED VIEW	149
4.5 Charging Trouble	74	13.2 Replacement Parts.....	151
4.6 Vibrator Trouble.....	76	13.3 Accessory	163
4.7 LCD Trouble.....	79		
4.8 Camera Trouble	83		
4.9 Speaker Trouble	87		
4.10 Earphone Trouble	89		
4.11 Receiver Trouble	92		



1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.

The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

1. INTRODUCTION

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc. Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated by the sign. Following information is ESD handling:



- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current – Constant Voltage
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milli watt
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Interface Bus
GSM	Global System for Mobile Communications
IQUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop

1. INTRODUCTION

PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
PSRAM	Pseudo SRAM
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. PERFORMANCE

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Lithium-Polymer, 3.7V 950mAh	
Stand by TIME	Up to 475 hrs : Paging Period 5, RSSI -85dBm	
Talk time	Up to 253min : GSM Tx Level 5	
Charging time	Approx. 3 hours	
RX Sensitivity	GSM, EGSM: -109dBm, DCS: -109dBm	
TX output power	GSM, EGSM: 32.3dBm(Level 5), DCS , PCS: 29.5dBm(Level 0)	
GPRS compatibility	Class 12	
SIM card type	3V / 1.8V	
Display	MAIN : 2.2" TFT 176 × 220 pixel 262K Color	
Status Indicator	Hard icons. Key Pad 0 ~ 9, #, *, Up/Down Left/Right OK Key Send Key, PWR Key ,Soft Key(Left/Right),	
ANT	Internal	
EAR Phone Jack	Yes	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR	
Data and Fax	Yes	
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	
Microphone	Yes	

2. PERFORMANCE

Item	Feature	Comment
Speaker/Receiver	18x12Φ Speaker/ Receiver	
Travel Adapter	Yes	
MIDI	64 Poly (Mono SPK)	
Camera	1.3M FF	
Bluetooth / FM Radio	Bluetooth version 2.1 / 76~108MHz supported	

2.2 Technical Specification

Item	Description	Specification					
1	Frequency Band	GSM850 TX: 824 ~ 849 MHz RX: 869 ~ 894 MHz DCS TX: 1710 ~ 1785 MHz RX: 1805 ~ 1880 MHz PCS TX: 1850 ~ 1910 MHz RX: 1930 ~ 1990 MHz					
2	Phase Error	RMS < 5 degrees Peak < 20 degrees					
3	Frequency Error	< 0.1 ppm					
4	Power Level	GSM850/EGSM					
		Level	Power	Toler.	Level	Power	Toler.
		5	33dBm	±2dB	13	17dBm	± 3dB
		6	31dBm	±3dB	14	15dBm	± 3dB
		7	29dBm	±3dB	15	13dBm	± 3dB
		8	27dBm	±3dB	16	11dBm	± 5dB
		9	25dBm	±3dB	17	9dBm	± 5dB
		10	23dBm	±3dB	18	7dBm	± 5dB
		11	21dBm	±3dB	19	5dBm	± 5dB
		12	19dBm	±3dB			
		DCS/PCS					
		Level	Power	Toler.	Level	Power	Toler.
		0	30dBm	±2dB	8	14dBm	± 3dB
		1	28dBm	±3dB	9	12dBm	± 4dB
		2	26dBm	±3dB	10	10dBm	± 4dB
		3	24dBm	±3dB	11	8dBm	± 4dB
		4	22dBm	±3dB	12	6dBm	± 4dB
		5	20dBm	±3dB	13	4dBm	± 4dB
		6	18dBm	±3dB	14	2dBm	± 5dB
		7	16dBm	±3dB	15	0dBm	± 5dB

2. PERFORMANCE

Item	Description	Specification	
5	Output RF Spectrum (due to modulation)	GSM850/ EGSM	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-63
		3,000~ <6,000	-65
		6,000	-71
		DCS/PCS	
		Offset from Carrier (kHz).	Max. dBc
		100	+0.5
		200	-30
		250	-33
		400	-60
		600~ <1,200	-60
		1,200~ <1,800	-60
		1,800~ <3,000	-65
		3,000~ <6,000	-65
		6,000	-73
6	Output RF Spectrum (due to switching transient)	GSM850/ EGSM	
		Offset from Carrier (kHz).	Max. dBm
		400	-19
		600	-21
		1,200	-21
		1,800	-24

2. PERFORMANCE

Item	Description	Specification		
6	Output RF Spectrum (due to switching transient)	DCS/PCS		
		Offset from Carrier (kHz).		Max. dBm
		400		-22
		600		-24
		1,200		-24
		1,800		-27
7	Spurious Emissions	Conduction, Emission Status		
8	Bit Error Ratio	GSM850, EGSM BER (Class II) < 2.439% @-102 dBm DCS,PCS BER (Class II) < 2.439% @-100 dBm		
9	RX Level Report Accuracy	±3 dB		
10	SLR	8±3 dB		
11	Sending Response	Frequency (Hz)	Max.(dB)	Min.(dB)
		100	-12	-
		200	0	-
		300	0	-12
		1,000	0	-6
		2,000	4	-6
		3,000	4	-6
		3,400	4	-9
		4,000	0	-
12	RLR	2±3 dB		

2. PERFORMANCE

Item	Description	Specification		
13	Receiving Response	Frequency (Hz)	Max.(dB)	Min.(dB)
		100	-12	-
		200	0	-
		300	2	-7
		500	*	-5
		1,000	0	-5
		3,000	2	-5
		3,400	2	-10
		4,000	2	
		* Mean that Adopt a straight line in between 300 Hz and 1,000 Hz to be Max. level in the range.		
14	STMR	> 17 dB		
15	Stability Margin	> 6 dB		
16	Distortion	dB to ARL (dB)	Level Ratio (dB)	
		-35	17.5	
		-30	22.5	
		-20	30.7	
		-10	33.3	
		0	33.7	
		7	31.7	
		10	25.5	
17	Side Tone Distortion	Three stage distortion < 10%		
18	System frequency (13 MHz) tolerance	≤ 2.5 ppm		
19	32.768KHz tolerance	≤ 30 ppm		
20	Ringer Volume	At least 55 dBspl under below conditions: 1. Ringer set as ringer. 2. Test distance set as 1 m		

2. PERFORMANCE

Item	Description	Specification	
21	Charge Current	Fast Charge : Typ. 400 mA Total Charging Time : average 3 hours	
22	Antenna Display	Bar Number	Power
		7	Over -93
		7 -> 5	-93 $\pm$ 2
		5 -> 4	-98 $\pm$ 2
		4 -> 2	-101 $\pm$ 2
		2 -> 1	-104 $\pm$ 2
		1 -> 0	-106 $\pm$ 2
		0 -> OFF	Under -106
23	Battery Indicator	Battery Bar Number	Voltage
		3	$\geq 3.73 \pm 0.05$ V
		3 -> 2	3.72 $\pm$ 0.05 V
		2 -> 1	3.58 $\pm$ 0.05 V
		1 -> 0	3.42 $\pm$ 0.05 V
24	Low Voltage Warning (Blinking Bar)	$\leq 3.42 \pm 0.05$ V (Call), 1 time per 1 minute (Receiver)	
		$\leq 3.42 \pm 0.05$ V (Standby), 1 time per 3 minutes(Speaker)	
25	Forced shut down Voltage	3.35 $\pm$ 0.05V	
26	Sustain RTC without battery	220 min	
27	Battery Type	Lithium-Polymer Battery Standard Voltage = 3.7 V Battery full charge voltage = 4.2 V Capacity: 950mAh	
28	Travel Charger	Switching-mode charger Input: 100 ~ 240V, 50/60 Hz Output: 4.8V, 400mA	

3. TECHNICAL BRIEF

The diagram illustrates the system architecture of the ARM1176, organized into several functional blocks:

- Top Section (Yellow):** Contains the ARM1176 processor, External Memory-IF, SD/MMC, SIM, CIF, Keypad, Measurement IF(A/D), and Digital-Microphone. These are connected via a 64-bit bus and a 32-bit bus.
- Bottom Section (Blue):** Includes cache, RAM, and ROM.
- Right Section (Green):** Features GSM, USIF, USB 2.0 FS, DCC, FM-radio, GSM Cipher, IR-Memory, GPTU, TEAKLite, RF Control, and FS/DAI.
- Left Section (Purple):** Includes DAC, GM6K, Mic, SD PLL, ADC, DSP, IF, Low-Power DCXO, 32 kHz XO, and RF PMU.
- Bottom Section (Red):** Contains LRTC, LPMU, VANA, LSIM, LAUX, VMMC, Vcore, Vibrator, VUSB, Back-light, DC/DC Buck, and Charge.
- Right Section (Green):** Includes Stereo Headset, Earpiece, Loud-speaker, Mic MUX, MicSupply generation, and Charge Pump (negative voltage for bipolar audio out).
- Bottom Section (White):** Shows the DC/DC converter circuit with components like capacitors, resistors, and a ZXTF 25020 for example.

LGE Internal Use Only

3.1.1 General

- Technology:
 - SoC, Monolithic, 65 nm CMOS
- Package:
 - eWLB, 8x8x0.8 mm
 - 0.5 mm pitch
 - 217 balls / 8-layer PCB

3.1.2 RF Transceiver

- Dual-band direct conversion receiver
- Tri/Quad-band possible with external circuitry
- Fully integrated digital controlled XO
- Additional buffer for 2 external system clocks
- Fully digital RF-Synthesizer incl. $\Sigma\Delta$ -Transmitter

3.1.3 Baseband

- DSP:
 - 156 MHz TeakLite™
- MCU:
 - ARM1176® @ 208 MHz
- MCU RAM:
 - 3.00Mbit
- Memory I/F:
 - 512 Mbit
- Modem:
 - GPRS class 12, (RX/TX CS1-CS4)
 - EGPRS class 12, (RX MCS1-MCS9, TX MCS1-MCS4)
- Cipher Units:
 - A51/2/3
 - GEA-1/2/3
- Security:
 - OMTP TR0
 - Secure Boot
 - RSA(ROM)/SHA-1(HW accel.)
 - OCDS disabling
 - Certificate Management

3. TECHNICAL BRIEF

- Speech Codec:
 - FR / HR / EFR / NB-AMR
- Audio Codec (running on ARM1176):
 - SP-MIDI
 - SB-ADPCM
 - MP3
 - WB-AMR
 - AAC/AAC+/eAAC+
- Others:
 - DARP (SAIC)
 - TTY
- Customization:
 - E-Fuses

3.1.4 External Memory

- External Bus Unit
 - 25-bit address bus (512 Mbit)
 - 16-bit data bus
 - 1.8V & 2.8V support
- Flash / RAM
 - NOR Type
 - Serial Flash SPI and SPI-4
 - Parallel Flash (Page & Burst Mode)
 - 16-bit Demultiplexed
 - 16-bit AD-multiplexed
 - 16-bit AAD-multiplexed
 - iNAND Type e.g. oneNAND
- Memory card
 - SD/MMC card interface with 1 or 4 data lines

3.1.5 Connectivity

- 3xUSIF (configurable either as SPI or UART), I2C, I2S; Interfaces @ 1.8V
- Direct (U)SIM 1.8/3V
- USB2.0 up to 480 Mbit/s (High Speed) w/ external USB Phy over ULPI interface
- Stereo Headset (Amplifier integrated)
- 3 external analog measurement PIN's
- Bluetooth

3.1.6 Mixed Signal

- Improved audio performance
- Loudspeaker Audio Class D Amplifier, 700 mW@8 Ω mono for hands-free and ringing
- Stereo Headset 2x30 mW@16 Ω w/o coupling C
- Mono Earpiece 100 mW@16 Ω
- Digital microphone supported
- Differential microphone inputs

3.1.7 FM Radio

- Integrated FM radio
 - FM Stereo RDS Receiver
 - Sensitivity 2 μ V EMF
 - Support for US & EU bands
 - Stereo recording

3.1.8 Power Management

- Direct-to-Battery Connection
 - LDOs (incl. capless)
 - DC/DC step-down converter
 - DC/DC step-up for white LED supply
- Battery Type
 - Li-Polymer
- Charging control
 - Battery temperature
 - Watchdog protection
 - Start-up on flat battery
- External Charger
 - Switch mode
- USB battery charging
 - USB charging spec 1.0 compliant
- Backlight
 - Up to 4 serial white LEDs (integrated LDO)

3.1.9 Sub Display

- LED Module Display
 - 115 LEDs (5x23 LEDs)
 - RED Color
 - Display Surface : 7.5 mm x 27.9 mm

3. TECHNICAL BRIEF

3.1.10 Main LCD Display

- Type
 - 176*220, QCIF, 262k color (parallel)
- Interface
 - Parallel 8bit
 - Interf. voltage at 1.8V or 2.8V
- gRacr - Display Controller (Hardware)
 - 30 fps Display update without DMA (up to 60 fps) (full or partial)
 - Video post processing Scaling, Rotation (90° steps), Mirroring
 - Overlay with alpha blending
 - Color conversion YUV -> RGB
 - 2D vector graphics (Lines, filled rectangles, Bit block transfer (e.g. sprites, scrolling, antialiased bitmap fonts)

3.1.11 Camera

- 1.3 M pixel, FF
- Frame Rate : 15fps@VGA
- 13 MHz Pixel Rate
- ADC resolution : 10 bit

3.1.12 Video Capabilities

- Video Decoding MPEG-4/H.263
 - QCIF@30 fps
 - QVGA@15fps
- Video Encoding MPEG-4/H.263
 - QCIF@15 fps

3.1.13 Audio Capabilities

- Polyphonic ring tones
 - 64 voices MIDI, SP-MIDI
 - FM synthesizer
- AMR-WB
- True ring tones (MP3)
- MP3, eAAC+
- G.722 SB-ADPCM encoding/decoding

A mobile platform requires power supplies for different functions. These power supplies are generated in the integrated power management Unit (PMU). The PMU is designed to deliver the power for a typical standard phone.



The DC/DC converter generates a 1.8V supply rail. This voltage rail is used to supply main parts of the system, like the digital core of the chip (via LDO LCORE), some parts of the mixed signal macro, parts of the RF macro and the external memory if a 1.8V memory is used. The efficiency of the DC/DC converter is optimized for an average load current of 100mA. That is the load current estimated for the GSM talk mode.

3. TECHNICAL BRIEF

▪ Linear voltage Regulators (low dropout) LDOs

The LDOs are used to generate the supply for the different supply domains not directly supplied out of the DC/DC converter.

The VSIM output current is high enough to drive USB SIM cards.

▪ LCORE

The LCORE LDO provides the VCORE supply used for most of the digital parts of the chip

▪ LPMU

The LPMU provides VPMU supply for the PMU supply, e.g. for the startup state machine and analog parts like ADC, sense amplifier etc.

▪ LUSB

The LUSB LDO generates the supply for the USB transceiver (output driver and input). If no USB interface is required, LUSB can be used as general purpose LDO.

▪ LAUX

The LAUX generates VAUX. It is a general purpose LDO and can be used for different functions depending on the phone application, e.g. for the display or Camera.

▪ LMMC

The LMMC generates VMMC. It is a general purpose LDO and can be used e.g. for memory cards

▪ LSIM

The LSIM LDO generates the VSIM supply for the SIM card and interface. It is designed to supply Standard SIM cards.

▪ Other LDOs

The RF module has implemented several LDO's for different RF Power domain.

The mixed signal module has some LDO's for the audio driver and microphone supply.

Supply Domain LDO Name	Voltage	Max. Current	Output Cap	Input Domain	Comment
VBAT	0 ... 6.0 V				Operating range is 3.05 V ... 5.5 V, system emergency switch off voltage is about 2.8 V
VDD1V8	1.8 V	450 mA	22 μ F	VBAT	This voltage is generated by the DC/DC converter with 3.3 μ H inductor, The voltage is used for: Memory supply, and via LDO's for digital core supply, mixed signal supply and RF supply.
LCORE	1.2 V	300 mA	2x100 nF	VDD1V8	
LANA	1.3 V	10 mA	No	VDD1V8	No ball
LRTC	2.3 V	2 mA	≥ 100 nF	VBAT	This supply is only used for the HPBG, the 32.768 kHz oscillator and the real-time clock counter required during the sleep- and low-power mode.
LPMU	1.2 V	15 mA	100 nF	VBAT	Supply for the digital part of the PMU including digital control of DC/DC converter. This voltage is also used for the N-DEMOS driver of DC/DC converter and the class-D amplifier and the core PLL.
LUSB	3.1 V	40 mA	100 nF	VBAT	Used for the USB driver supply or as general purpose LDO with programmable output voltages (2.5 V, 2.85 V, 3.1 V)
LAUX	1.5 V ... 2.85 V	150 mA	470 nF	VBAT	General purpose LDO for e.g. Display, Bluetooth, Camera etc. Programmable output voltages are (1.5 V, 1.8 V, 2.5 V, 2.85 V)
LSIM	1.8 V / 2.85 V	30 mA	≥ 100 nF	VBAT	LDO dedicated to the SIM-Card supply. It is chip internal connected to the SIM interface driver.
LMMC	1.5 V ... 2.85 V	150 mA	≥ 470 nF	VBAT	General purpose LDO, targeted for MMC/SD card supply.
VDDNEG	-1.3 V	100 mA	100 nF	VDD1V8	Negative voltage for the bipolar headset audio driver. Generated by a charge pump.

Table. 3-2-1 Power supply Domains (without RF)

3. TECHNICAL BRIEF

3.2.1 Power on and startup

▪ Analog startup Circuit

Because the POR circuit and the LPBG are directly connected to the battery, it is not possible to switch them off. If the battery voltage exceeded the power on reset threshold (2.5V), the power on reset is released, the LPMU regulator and the LRTC voltage regulator are switched on. The LPMU regulator starts in its ultra-low power mode.

The LPMU regulator generates a control signal (lpmu_OK) that enables the 50KHZ PMU oscillator. The output clock of the oscillator is checked with a fully coded counter. A counter overflow releases the reset (vpmu_rst_n) signal for the small PMU state-machine.

▪ Small first digital State-Machine

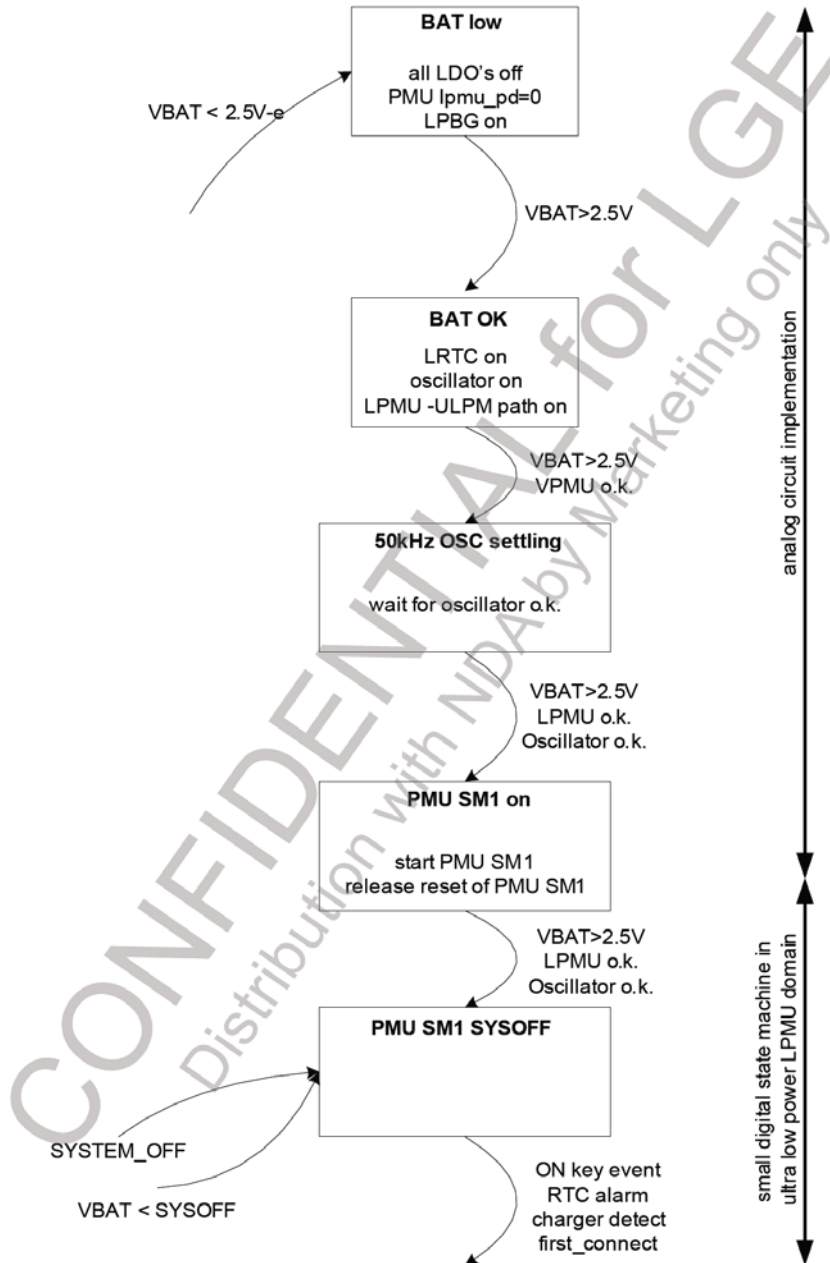
The small PMU state-machine is always connected to VPMU. After starting from reset the small startup state machine enters the SYSTEM OFF state and only continues the startup procedure if a switch on event like first connect, on-key, wake up or charge detect occurs.

▪ PMU-main State-Machine

The main PMU state-machine is always connected to VPMU also. The power up sequence driven by the PMU state-machine can be seen in Figure 18. After enabling the reference (HPGB) and waiting for the settling time, the battery voltage is measured and compared with the power on threshold. If the battery voltage is high enough, the SD1 DC/DC converter and the LDCORE LDO are started. A timer ensures that the supply voltage will be stable before the DCXO is enabled. The DCXO settling time is ensured using a fixed timer. After an overflow of this timer, the reset is released for the rest of the system. The PMU state machine remains in this System-ON state until the system is switched into the OFF state. For example the system sleep mode is completely configured by software (for example switching off the LDO's, switching of the DCXO etc.) and controlled by the VCXO_enable signal. The reason for the startup is stored in the ResetSourceRead register.

▪ Battery Measurement

The ADC and the oscillator for the ADC need the VDD_ADC supply voltage from the LADC LDO. LADC uses either the charger voltage VDD_CHARGE or VDDRTC as input voltage. The input voltage is selected automatically by a bulk switch circuit. LADC, the ADC and the oscillator are enabled on request for every battery measurement if the charger unit is not running. This is handled by an ADC control block in one of the state-machines. If the charger unit is running the ADC is controlled by the charger state-machine.



**Figure.3.2.1 First Part of the State Machine,
Running in Different Power Domains than the Second Part**

3. TECHNICAL BRIEF

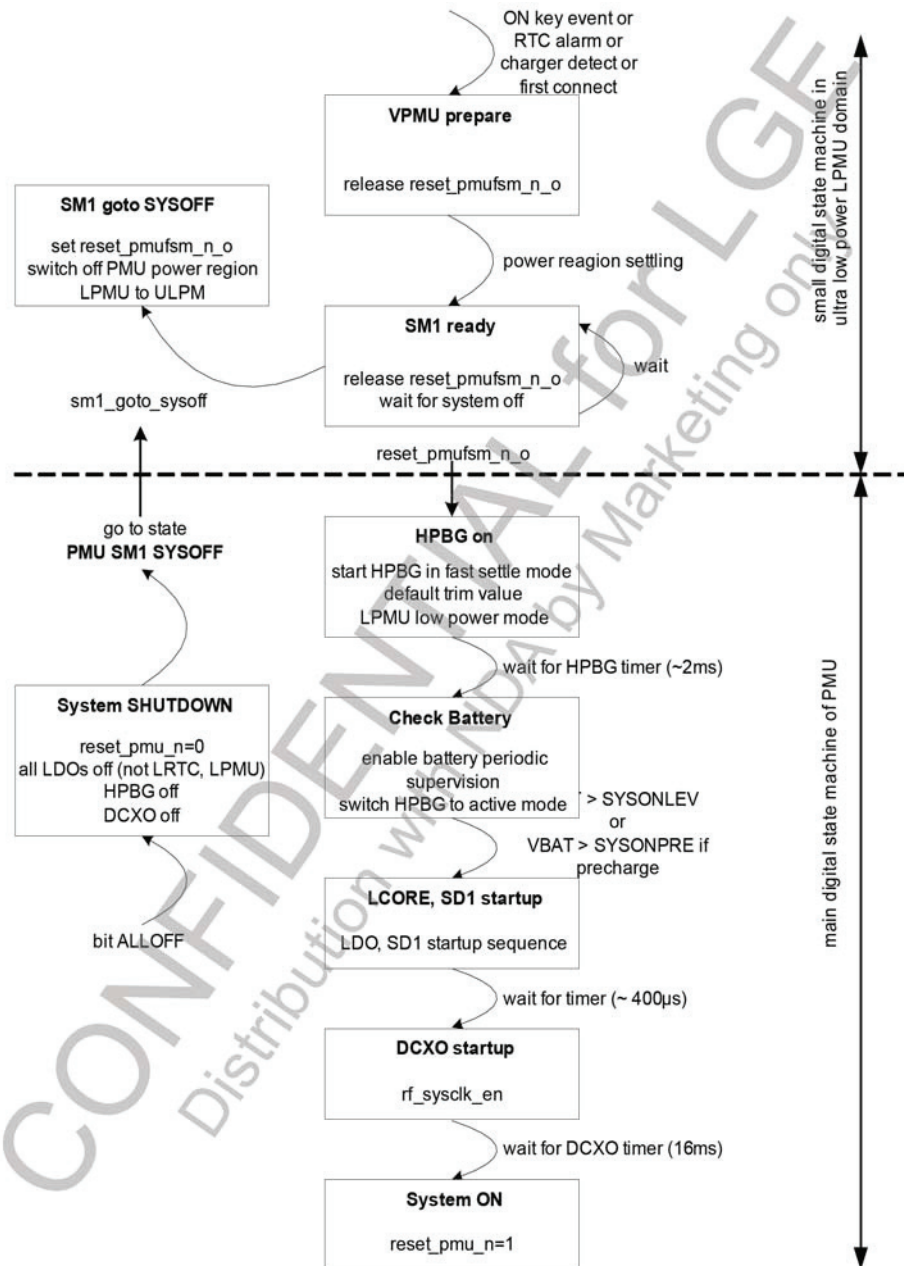


Figure 3.2.2 Second (Main) Part of the Startup State Machine in the VPMU Domain

3.2.2 Switching on due to first connect

If the battery voltage is connected the first time, that means the system enters the first time the SYSOFF state, this is stored in a first connect flag. If the first connect flag is set, the system will start immediately and not wait for any other system on event in the SYSOFF state.

3.2.3 Switching on due to on-Key event

The on key is connected to the ONKEY pad. The ESD protection and the input structure of this pad are connected to VRTC. If the ONKEY pad is forced to VRTC by an external key or similar circuit, the system starts. The ONKEY is sampled with the PMU clock. It has to be sampled four times high before a valid on event is generated. The status of the ON key can be read in the PMU registers, so it can be used as a functional key during phone operation also.

3.2.4 Switching on due to RTC alarm

The real time clock can generate a wakeup signal called RTC alarm. This signal is sampled from the state-machine and after successfully detecting a high, the system is switched on.

3.2.5 Switching on due to charging

When a battery with a voltage below the SSONLEV level is inserted, the state machine will not start the system. As long as the battery voltage stays lower than SYSONLEV the system will stay off. The only possibility to start up the system is due to an external charger.

If an external charger is connected and detected and the battery is charged above the SYSONPRE voltage level the system will start up.

The PMU main state machine waits in the Check battery state until the battery voltage condition is fulfilled. The charger state machine provides the necessary pre-charge indication signal. This pre-charge signal is denounced in a small counter to have a stable signal. This is important, especially in half/full-wave charging where the charger detection is switching between charger detected/not detected according to the AC supply frequency. Reasons.

For details on pre-charging see the charger chapter. The charger is controlled by an independent state machine. The pre-charge signal is used to trigger the pre-charge signal is used to trigger the pre-charge functionality. The charger state machine fully control the pre-charge, the PMU-state machine now changes to state HPBG on state and the system starts. This state change is indicated to the charger state-machine to enable the charger watchdog for safety.

3.2.6 Power Supply Start-up sequence

In order to avoid an excessive drop on the battery voltage caused by in-rush current during system power-on, possibly leading to system instability and "hick-ups" a staggered turn-on approach for the regulators is implemented. The regulators are turned on in a well defined sequence, thus spreading the in-rush current transients over time.

The IO's of X-GOLD TM 213 are isolated in OFF mode (core supply is off). The isolation signal is controlled by the PMU state machine. This ensures that the PADs are in a well defined state during core supply settling. This allows to power up the LCORE core regulator and wait for the core to reach reset state before powering up the I/O supply regulators.

3. TECHNICAL BRIEF

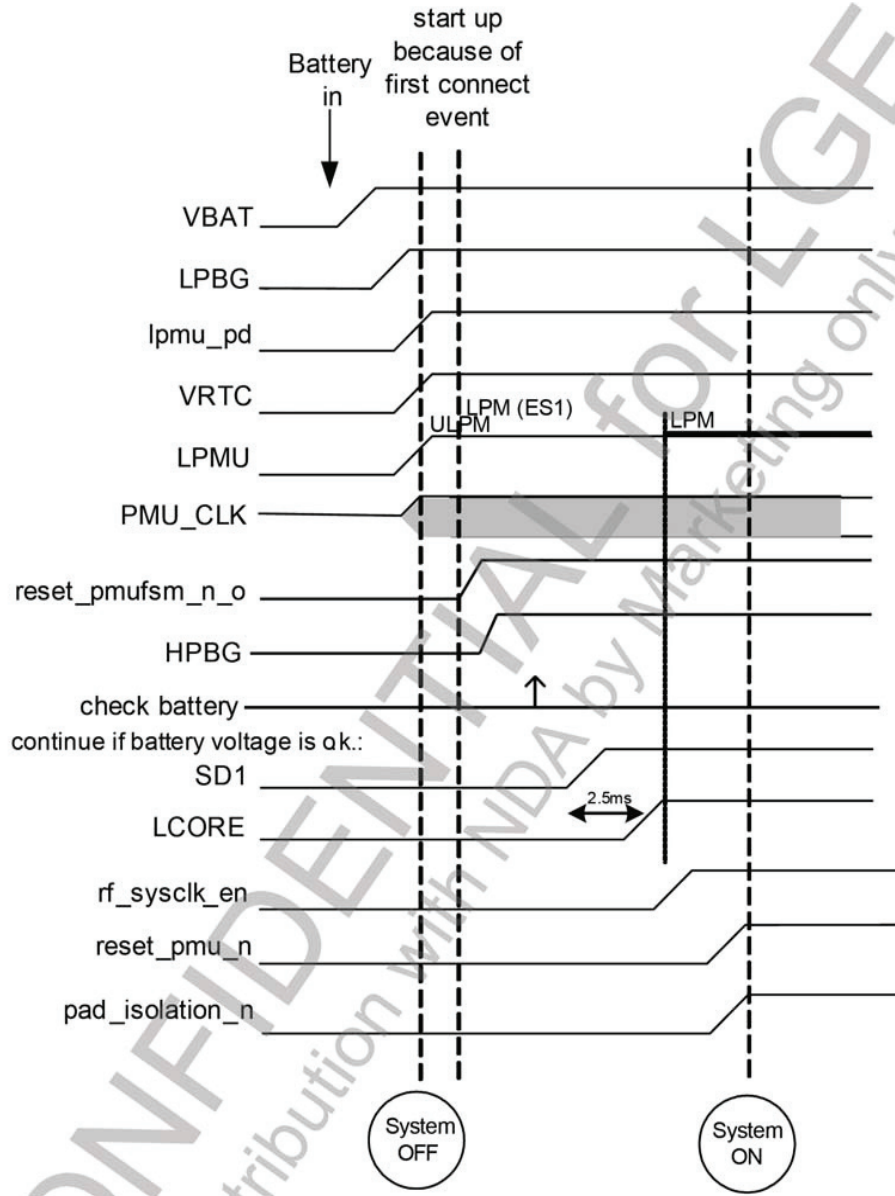


Figure 3.2.3 Start Up Sequence (triggered by First Connect Event)

3.2.7 External Reset Handling

The chip reset can be controlled by an external RESET_N ball. If this ball is pulled low, the chip will be reset.

All PMU registers are reset during the external reset including LSIM control bits. The PMU statemachines are also not reset from the external reset. An SW or watchdog reset will not reset the PMU registers.

A SW and Watchdog reset is seen on the reset_n pad to allow the reset of external devices. Basically there are three reset sources, first the reset signal controlled by the PMU (reset_pmu_n_o), second the reset signal controlled by the SCU (resetout_o) and third the external reset (RESET_N). The SCU reset is triggered by SW (for example due to a SW reset or watchdog reset). The PMU reset is controlled by the PMU state machine.

The output of the reset handling block is the reset_postscu_n_o signal. This signal controls for example the μ C subsystem and releases reset for the controller. During normal start up, the PMU releases the reset_pmu_n_o signal after entering the SYSTEM ON state. At this time the resetout_o signal is high, the RESET_N pad is not pulled low and therefore the reset_postscu_n_o signal follows the reset_pmu_n_o signal.

That means the μ C reset will be released and the μ C starts operation. If the SW triggers an external reset via the SCU, signal resetout_o will be forced to low for a certain time and RESET_N will be forced to low by the open drain driver. At the same time the feedback to the SCU will be masked to not reset the baseband.

The RESET_N pad is in the VDDRTC domain but the internal pull up is connected to the VDD_VDIG1 (1.8V) domain. That allows the pad to be used as reset for external devices running in the VDD1V8 domain. The RESET_N pad can also be used to monitor the chip internal reset condition during startup.

The open drain driver is a weak driver, that means it can be forced to high during debug from external pushing some current into the pad. In testmode signal reset_pmu_n_o is high, that means the chip reset is fully controlled from external.

3. TECHNICAL BRIEF

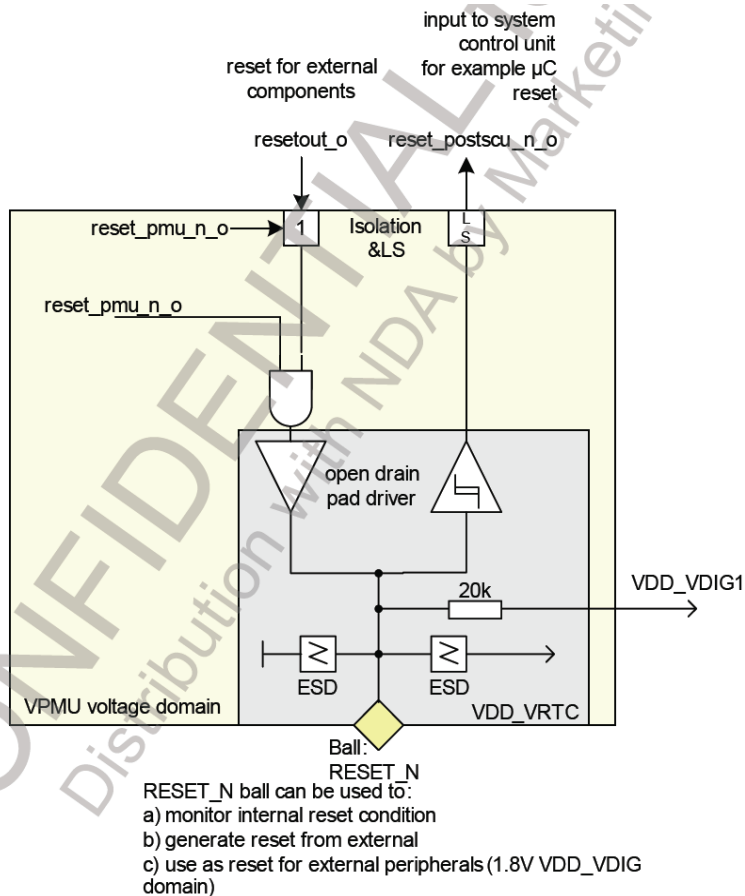


Figure 3.2.4 PMU, CGU and External Reset

3.2.8 Sysclock Switching

The PMU controls the `rf_sysclk_en` signal of the DCXO in the RF macro. During startup the PMU enables the DCXO. After the system is running the DCXO is controlled by the SCU of the baseband by using the `vcxo_enable` signal. This is handled by a dedicated logic in the PMU, see **Figure 21**. As long as `rf_sysclk_en_pmu`, the output of the PMU state-machine is high, `vcxo_enable` controls the `rf_sysclk_en` signal to the RF. If `rf_sysclk_en_pmu` is low, the DXCO is switched off, independent from `vcxo_enable`.

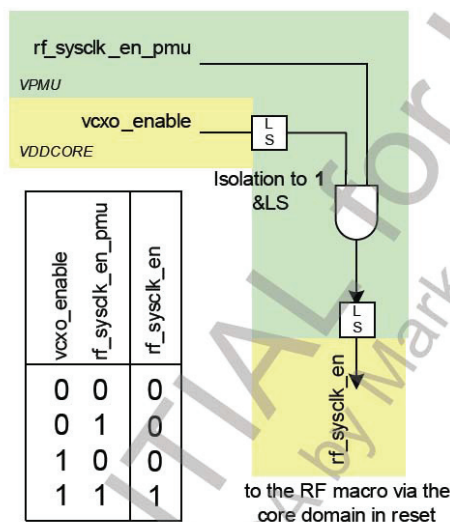


Figure 3.4.2 How sysclock Enable is Routed in the PMU

3.2.9 Undervoltage Shutdown

In active mode the PMU periodically measures the battery voltage using the ADC from the charger unit. If the battery is measured to be below the programmable shut-down level (called SYSOFF), the system changes to OFF mode. This is done via the SHUTDOWN state of the PMU state machine. (see chapter switch OFF)

3.2.10 Software Reset

A software reset does not affect any PMU register. The PMU register are reset with the `reset_pmufsm_n_o` signal. That means all PMU register are reset in OFF state. For details about the SW reset see chapter **External Reset Handling**.

3. TECHNICAL BRIEF

3.2.11 PMU Clock

During the first startup (for example plugging in a battery) a PMU internal oscillator is used for generation of the PMU clock (pmu_clock). The frequency is slightly above 32 kHz (typ. 50 kHz) to be out of the audio band also for worst case devices. After first startup the software shall enable the 32 kHz crystal oscillator. It is not possible to use the 32 kHz oscillator during first startup, because the settling time of the oscillator can be quite long. After the 32 kHz oscillator is running and settled the software shall switch the PMU clock to the 32 kHz clock and disable the internal PMU oscillator for power saving reasons. The 32 kHz oscillator shall never be disabled after the PMU clock has been switched. The ADC in the charger unit has its own oscillator generating a frequency of about 10 MHz. This oscillator is running during charging and during battery measurements triggered by the PMU. It is off otherwise.

3.2.12 System Sleep Mode

The sleep mode is controlled by using the VCXO_enable signal. This signal is used to switch the LDO's and the DC/DC converter SD1 in a programmable way into its low power mode (PFM). In addition DC/DC converter SD1 can be configured to change the output voltage to a lower value for additional power saving. VCXO_enable is also used to deactivate the HPBG and setting LDO LPMU in the ultra-low-power mode. In addition the DCXO is switched off by the VCXO_enable signal. The VCXO_enable signal is also used to switch some LDO's (software configured) to sleep and/or off mode or to change the output voltages of said LDO's. The state of the main PMU state machine is not changed due to VCXO_enable.

3.2.13 DC/DC Pre-Load Register Handling

The DC/DC converter works in different modes. If the mode is switched from PFM to PWM the pulse-width of the DC/DC converter depends on the current battery voltage (and on the output voltage). The PMU state-machine knows the battery voltage because of the battery supervision function. Depending on this value it selects a startup pulse-width for the DC/DC converter out of a register table. (4-values)

3.2.14 Power Down Sequence

Setting bit OFF in the GeneralControl register switches the system into OFF mode. After the turn off event, the state-machine switches to the SHUTDOWN state. The reset_pmu_n_o signal changes to low, the I/O pads are isolated using the padisolation_n signal, the LCORE LDO and the SD1 DC/DC converter are switched off, the LPMU LDO is switched to ultra-low power mode, the DCXO is turned off and the bandgap buffer is disabled. Before switching OFF the software shall have enabled the 32 kHz oscillator and has switched the PMU clock to the 32 kHz clock to archive the target OFF current .

3.3 FEM with integrated Power Amplifier Module (SKY77547, U400)

3.3.1 Internal Block Diagram

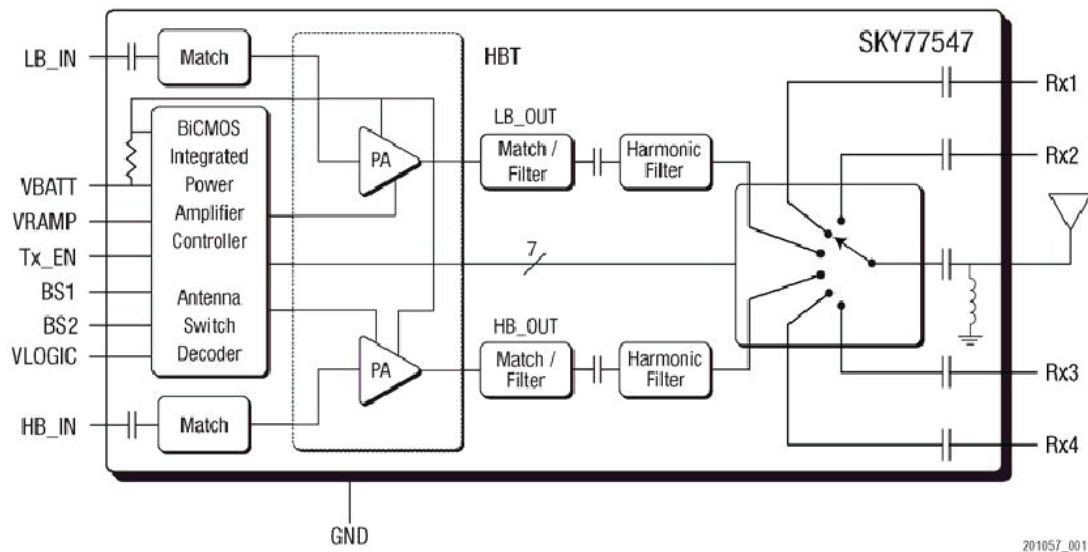


Figure. 3-3-1 SKY77547 FUNCTIONAL BLOCK DIAGRAM

3.3.2 General Description

The RF7161 is a quad-band (GSM850/EGSM900/DCS1800/PCS1900) GSM/GPRS, Class 12 compliant transmit module with four interchangeable receive ports. This transmit module builds upon RFMD's leading power amplifier with PowerStar® integrated power control technology, pHEMT switch technology, and integrated transmit filtering for best-in-class harmonic performance.

The results are high performance, reduced solution size, and ease of implementation. The device is designed for use as the final portion of the transmitter section in a GSM850/EGSM900/DCS1800/PCS1900 handset and eliminates the need for a PA-to antenna switch module matching network.

The RF7161 features RFMD's latest integrated power-flattening circuit which significantly reduces current and power variation into load mismatch. Additionally, a VBATT tracking feature is incorporated to maintain switching performance as supply voltage decreases.

3. TECHNICAL BRIEF

Mode	VLOGIC	Input Control Bits		
		TX_EN	BS1	BS2
STANDBY	0	X	X	X
RX1	1	0	0	0
RX2	1	0	0	1
RX3	1	0	1	1
RX4	1	0	1	0
LB_TX	1	1	0	X
HB_TX	1	1	1	X

1. X = DON'T CARE

2. RX1, RX2, RX3, and RX4 are broadband receive ports and each supports the GSM850, GSM900, DCS, and PCS bands.

Figure 3.3.2 Band SW Logic Table

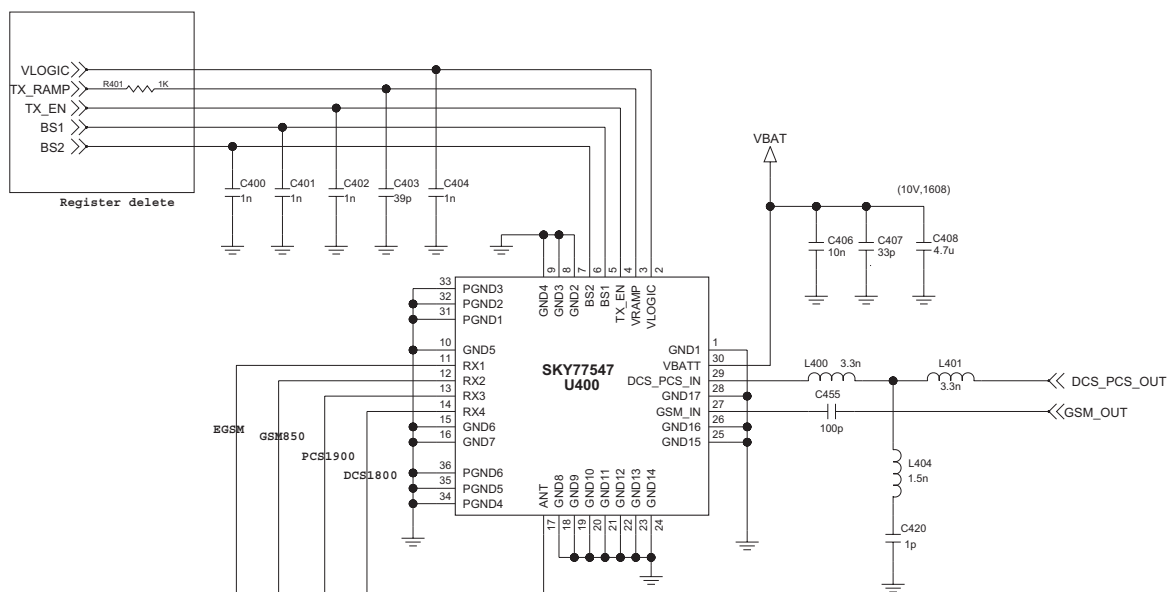
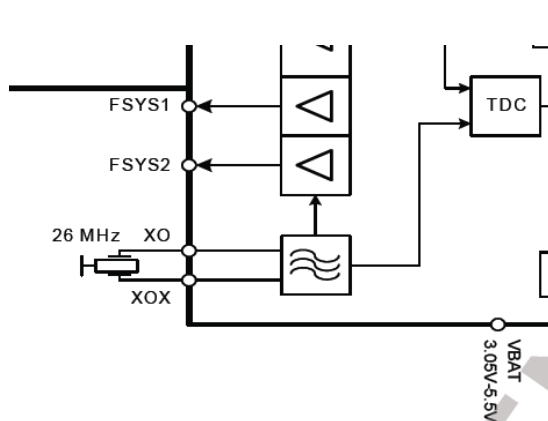


Figure 3.3.3 FEM CIRCUIT DIAGRAM

3.4 Crystal(26 MHz, X100)



The X-GOLDTM213 RF-Subsystem contains a fully integrated 26 MHz digitally controlled crystal oscillator, designed for 8 pF crystals. The only external part of the oscillator is the crystal itself. Overall pulling range of the DCXO is approximately ± 55 ppm, controllable by a 13-bit tuning word.

This frequency serves as comparison frequency within the RF-PLL and as clock frequency for the digital circuitry.

The 26 MHz reference clock can also be applied to external components like Bluetooth or GPS, via the two buffered output signals FSYS1 and FSYS2

Figure. 3.4.1 Crystal Oscillator External Connection

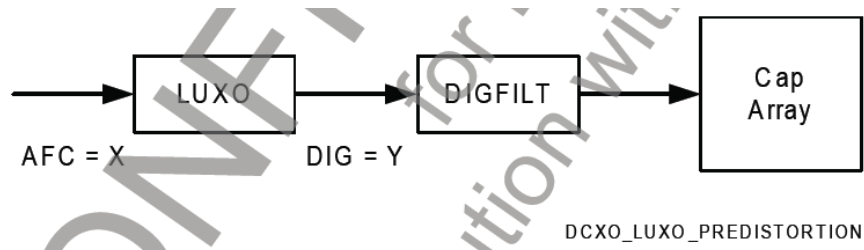


Figure. 3.4.2 Digital PREDISTORTION with LUXO

The DCXO tuning characteristic should be a first order linear function of the programming word AFC. The variable capacitance array is a first order linear function of the digital word DIG, which leads to a nonlinear curve ppm vs. DIG (and also a nonlinear ppm vs. AFC for DIG=AFC). In order to linearize the ppm vs. AFC curve the implementation of a predistortion is necessary.

To get the wanted linear ppm vs. AFC tuning curve some digital predistortion of the AFC word is required. This predistortion is performed by the linearization unit for crystal oscillator (LUXO). The LUXO calculates the corresponding DIG value according to the given AFC value.

3. TECHNICAL BRIEF

3.5 RF Subsystem of PMB8810 (U100)

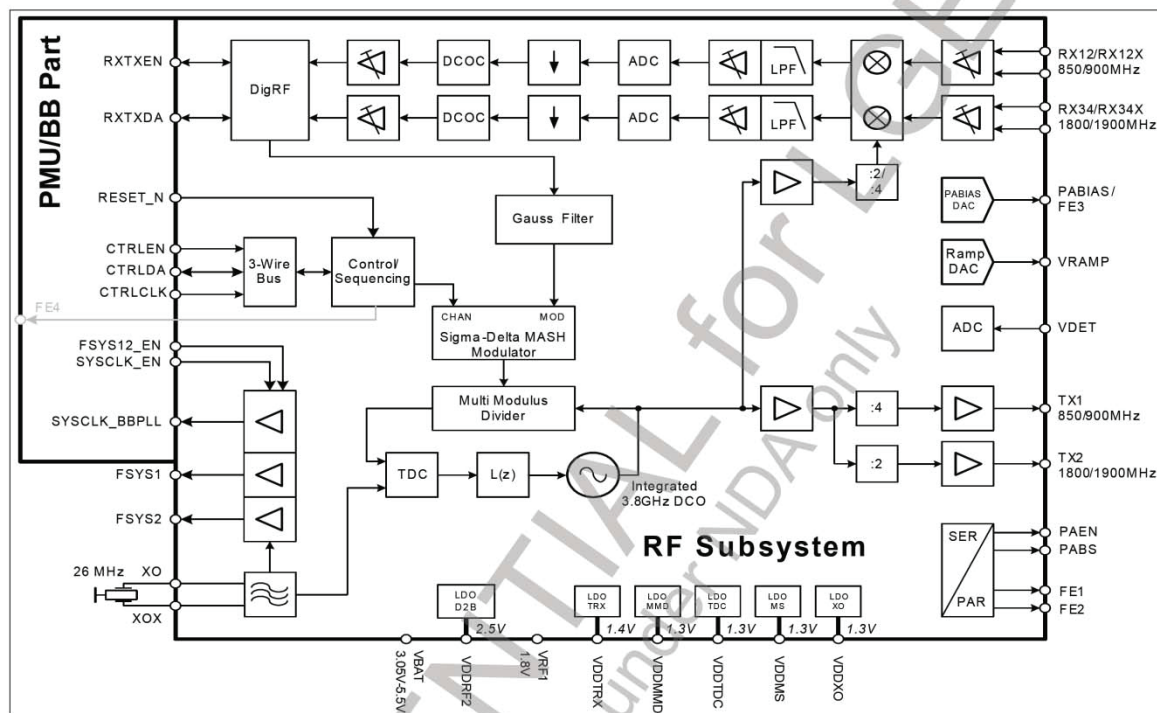


Figure. 3-5-1 Block DIAGRAM of RF Subsystem

3.5.1 GENERAL DESCRIPTION

The PMB8810 RF subsystem is designed for dual-band GSM voice and data applications (GPRS class 12). The system can be configured to support one low band, GSM850 or EGSM900, and one high band, DCS1800 or PCS1900. A block diagram of the RF subsystem is given in Figure 3-4-1.

3.5.2 FUNCTIONAL DESCRIPTION

3.5.2.1 Receiver

The X-GOLD™213 dual-band receiver is based on a Direct Conversion Receiver (DCR) architecture. Input impedance of the LNAs is optimized to achieve a matching without (external) high quality inductors. By use of frequency dividers (by 2/4) the LO frequency is derived from the RF frequency synthesizer. The receive path is fully differential to suppress the on-chip interferences and reduce DC-offsets. The analog chain of the receiver contains two LNAs (low/high band), a quadrature mixer followed by an analog baseband filter and 14-bit continuous-time delta-sigma analog-to-digital converter. The filtered and digitized signal is fed into the digital signal processing chain, which provides decimation, DC offset removal and programmable gain control.

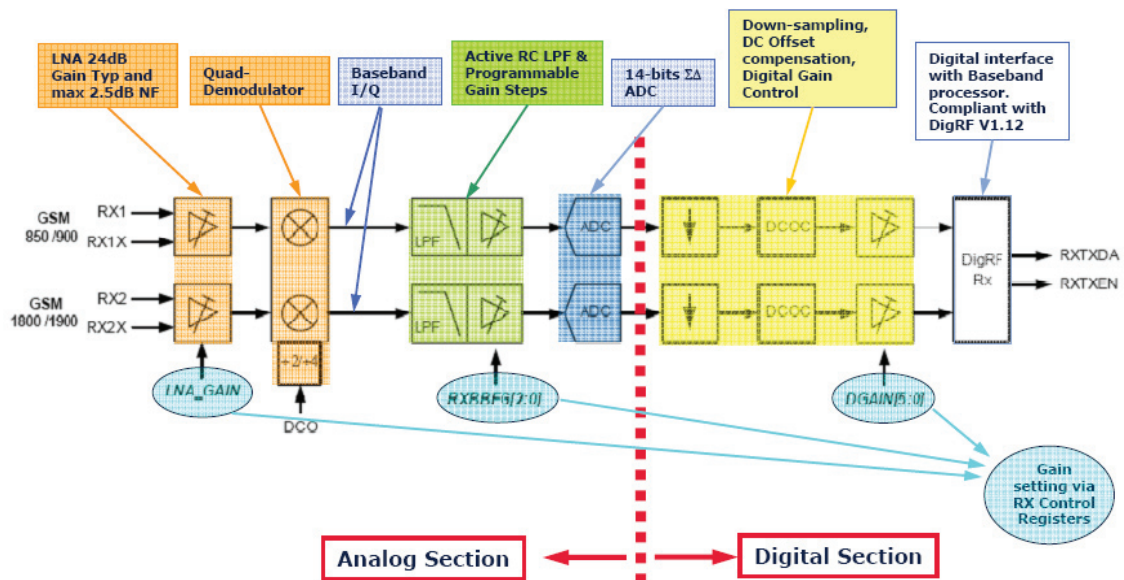


Figure. 3.5.2 RECEIVER CHAIN BLOCK DIAGRAM

3. TECHNICAL BRIEF

3.5.2.2 Transmitter

The GMSK transmitter supports power class 4 for GSM850 or GSM900 as well as power class 1 for DCS1800 or PCS1900. The digital transmitter architecture is based on a fractional-N sigma-delta synthesizer for constant envelope GMSK modulation. This configuration allows a very low power design without any external components.

Up- and down-ramping is performed via the ramping DAC connected to VRAMP.

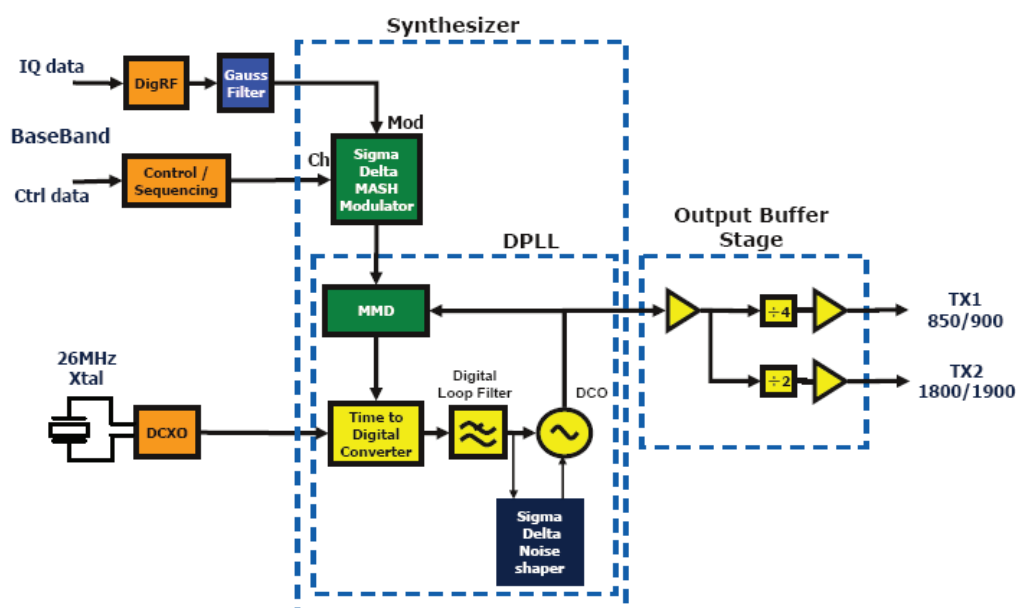


Figure. 3.5.3 TRANSMITTER CHAIN BLOCK DIAGRAM

RF synthesizer

The RF subsystem contains a fractional-N sigma-delta synthesizer for the frequency synthesis. Respective to the chosen band of operation the phase locked loop (PLL) operates at twice or forth of the target signal frequency. In receive operation mode the divided output signal of the digital controlled oscillator output (DCO) serves as local oscillator signal for the balanced mixer. For transmit operation the fractional-N sigma-delta synthesizer is used as modulation loop to process the phase/frequency signal. The 26 MHz reference signal of the phase detector incorporated in the PLL is provided by the reference oscillator.

3.5.2.3 Front-end/PA Control Interface

Two outputs (FE1, FE2) for direct control of antenna switch modules enable to select RX- and TX-mode as well as low- and high-band operation.

An extra band select signal PABS for the power amplifier is used, to support discrete PA and switching modules. Time accurate power dissipation of the PA is achieved by the control signal PAEN.

A minor set of power amplifiers require a bias voltage to enhance power efficiency. Support of this power amplifiers is achieved by the implemented bias DAC.

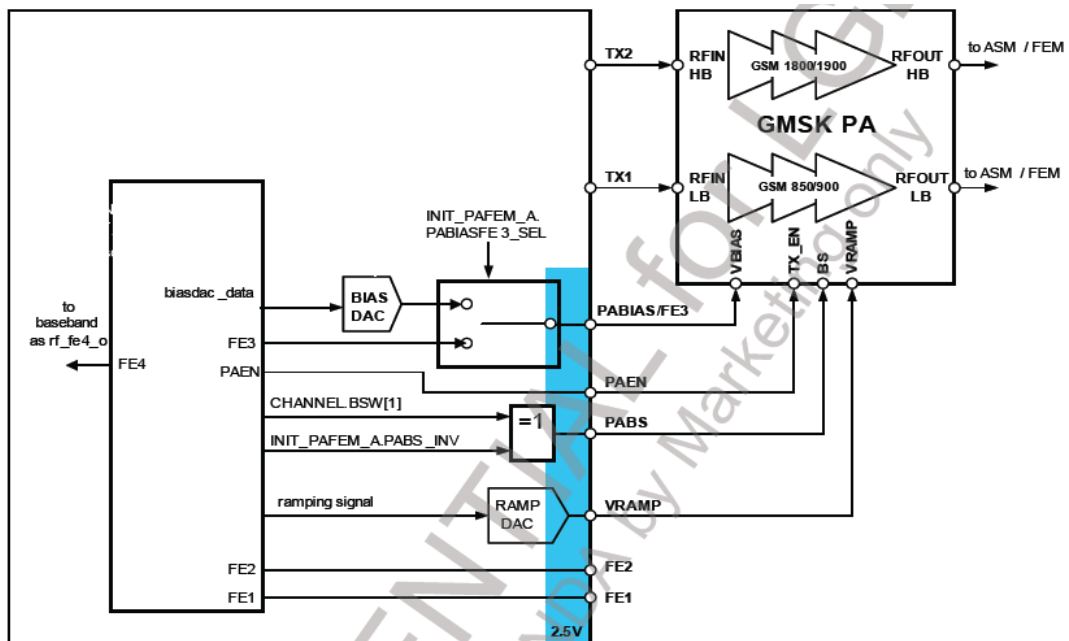


Figure. 3.5.4 PA AND FEM CONTROL BLOCK DIAGRAM

3. TECHNICAL BRIEF

3.5.2.4 Power Supply

To increase power efficiency most parts of the RF subsystem are supplied by the DCDC converter situated in the PMU subsystem. Conversion of the 1.8 V output voltage of the DCDC to the 1.3 V/1.4 V circuit supply voltages is achieved by several Low-DropOut regulators (LDO). One embedded direct-to-battery LDO provides the 2.5 V supply voltage for the remaining circuits.

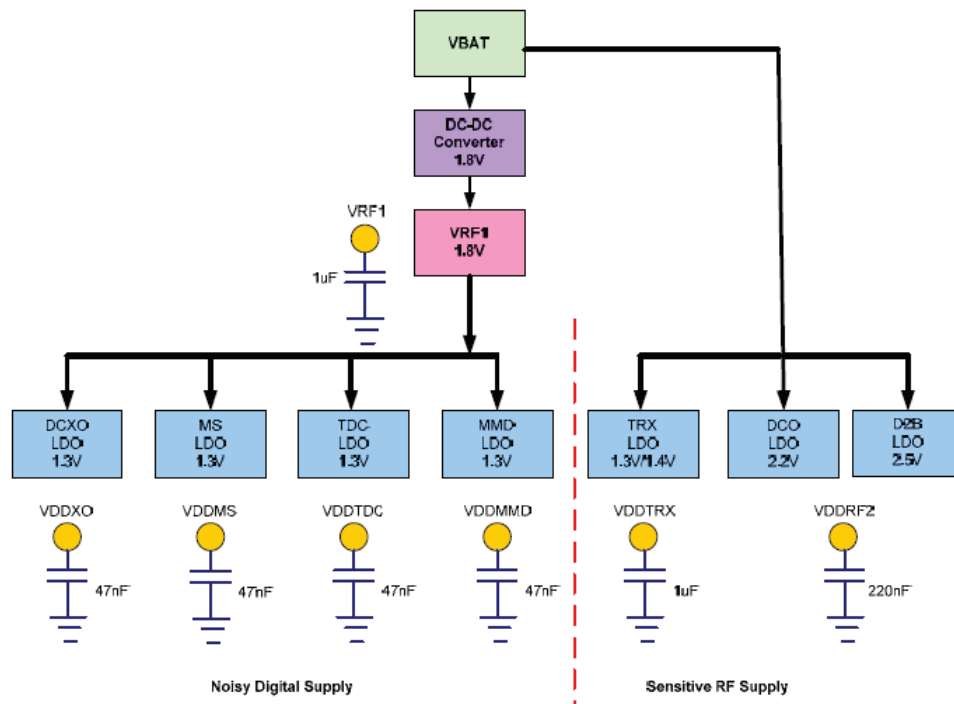


Figure. 3.5.5 POWER SUPPLY BLOCK DIAGRAM

3.6 MEMORY(PF38F5060M0Y0BE, U101)

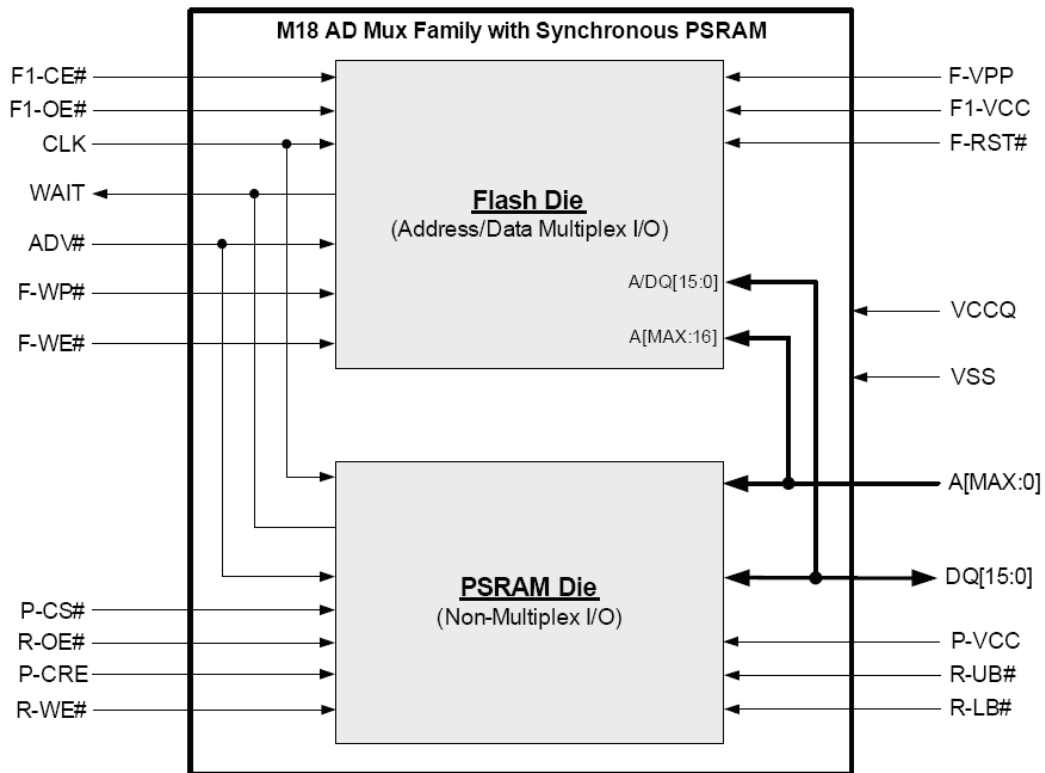


Figure. 3.6.1 MEMORY BLOCK DIAGRAM

The Numonyx™ StrataFlash® Cellular Memory (M18) device provides high read and write performance at low voltage on a 16-bit data bus.

The flash memory device has a multi-partition architecture with read-while-program and read-while-erase capability.

The device supports synchronous burst reads up to 108 MHz using ADV# and CLK address-latching (legacy-latching) on some litho/density combinations and up to 133 MHz using CLK address-latching only on some litho/density combinations. It is listed below in the following table.

3. TECHNICAL BRIEF

Litho (nm)	Density (Mbit)	Supports frequency up to (MHz)	Sync read address-latching
90	256	133	CLK-latching
	512	108	Legacy-latching
65	128	133	CLK-latching
	256	133	CLK-latching
	512	108	Legacy-latching
	512	133	CLK-latching
	1024	108	Legacy-latching
	1024	133	CLK-latching

Table 3_6_1 M18 Frequency combinations

In continuous-burst mode, a data Read can traverse partition boundaries.

Upon initial power-up or return from reset, the device defaults to asynchronous arrayread mode.

Synchronous burst-mode reads are enabled by programming the Read configuration Register. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

Designed for low-voltage applications, the device supports read operations with VCC at 1.8 V, and erase and program operations with VPP at 1.8 V or 9.0 V. VCC and VPP can be tied together for a simple, ultra-low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when VPP is less than VPPLK.

A Status Register provides status and error conditions of erase and program operations.

One-Time-Programmable (OTP) registers allow unique flash device identification that can be used to increase flash content security. Also, the individual block-lock feature provides zero-latency block locking and unlocking to protect against unwanted program or erase of the array.

The flash memory device offers three power savings features:

- Automatic Power Savings (APS) mode: The device automatically enters APS following a read-cycle completion.
- Standby mode: Standby is initiated when the system deselects the device by deasserting CE#.
- Deep Power-Down (DPD) mode: DPD provides the lowest power consumption and is enabled by programming in the Enhanced Configuration Register. DPD is initiated by asserting the DPD pin.

3.7 BT module

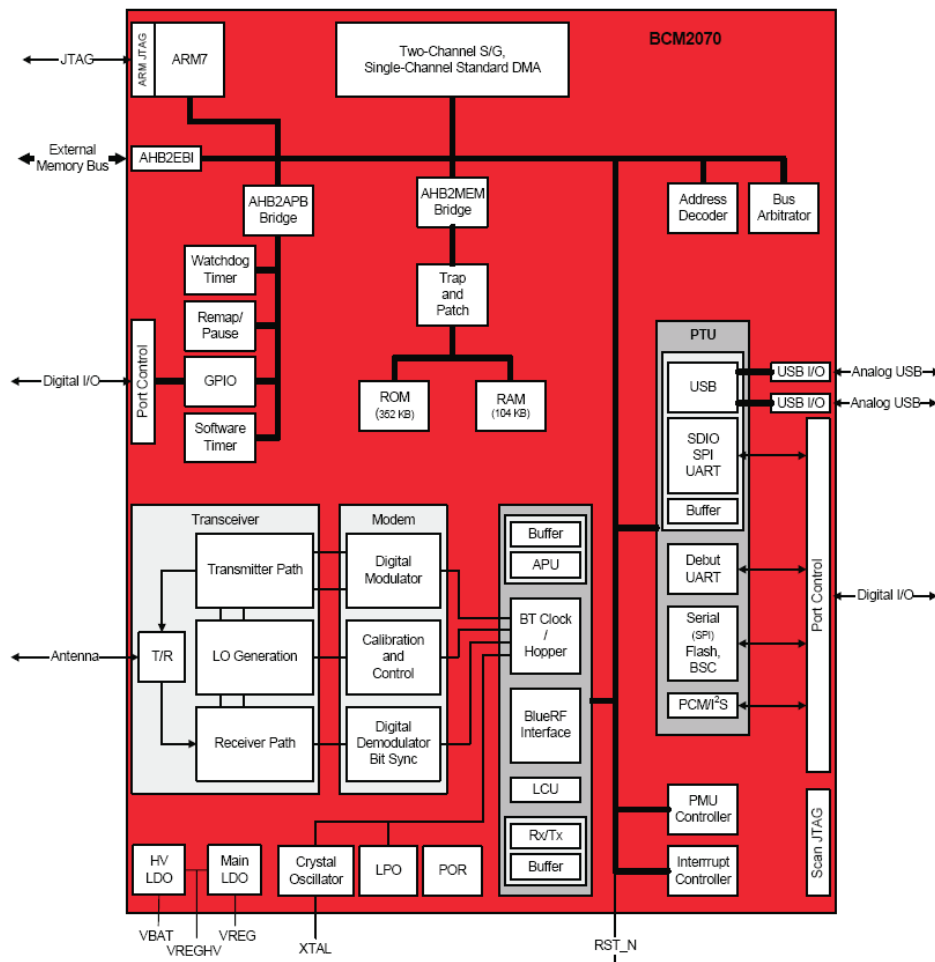


Figure 3_7_1. BT BLOCK DIAGRAM

This module has an integrated radio transceiver that has been optimized for use in 2.4GHz Bluetooth Wireless systems. It has been designed to provide low-power, robust communications for applications Operating in the globally available 2.4GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and enhanced data rate specification and meets or exceed the requirement to provide the highest communication link quality of service.

3. TECHNICAL BRIEF

3.7.1 Transmitter path

This module features a fully integrated zero IF transmitter. The baseband transmitted data is digitally modulated in the modem block and up-converted to the 2.4GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q up-conversion, high-output power amplifier (PA), and RF filtering. It also incorporates modulation schemes: P/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support enhanced data rate.

• Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK, B/4DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

• Power Amplifier

The integrated PA for the BCM2070 is configurable for Class 2 operation, transmitting up to +4 dBm as well as Class 1 operation and transmit power up to +12 dBm at the chip, GFSK, >2.5V supply. Due to the linear nature of the PA, combined with some integrated filtering, no external filters are required for meeting Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications, where Bluetooth is integrated next to the cellular radio, minimal external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. Using a highly linearized, temperature compensated design the PA can transmit +12 dBm for basic rate and +10 dBm for enhanced data rates (2 to 3 Mbps). A flexible supply voltage range allows the PA to operate from 1.2V to 3.0V. The minimum supply voltage at VDDTF is 1.8V to achieve +10dBm of transmit power.

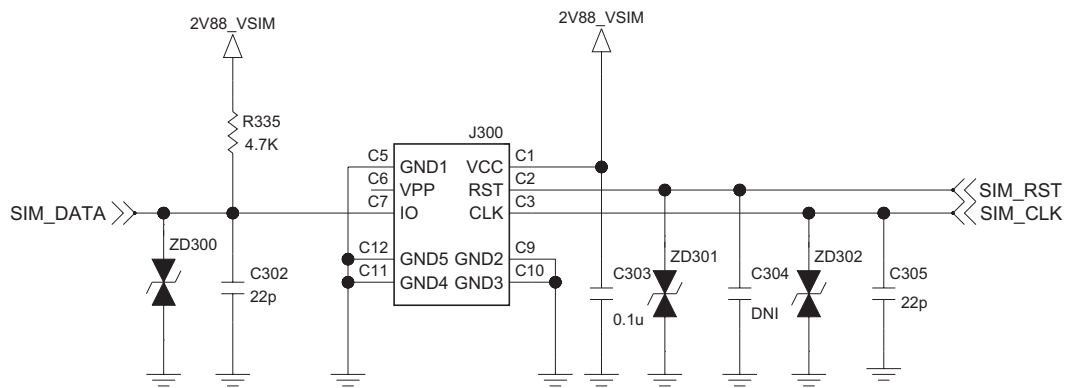
3.7.2 Receiver path

The receiver path uses a low IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the device to be used in most applications with no off-chip filtering.

For integrated handset operation where the Bluetooth function is integrated close to the cellular transmitter, minimal external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

3.8 SIM Card Interface

SIM_SOCKET



These are added for CMCC ESD test

Figure 3-8-1. SIM CARD Interface

The Main Base Band Processor(PMB8810) provides SIM Interface Module.

The PMB8810 checks status Periodically During established call mode whether SIM card is inserted or not, but it doesn't check during deep sleep mode. In order to communicate with SIM card, 3 signals SIM_DATA, SIM_CLK, SIM_RST.

And This model supports 1.8/2.88V SIM Card.

Signal	Description
SIM_RST	This signal makes SIM card to HW default status.
SIM_CLK	This signal is transferred to SIM card.
SIM_DATA	This signal is interface datum.

3. TECHNICAL BRIEF

3.9 LCD Interface

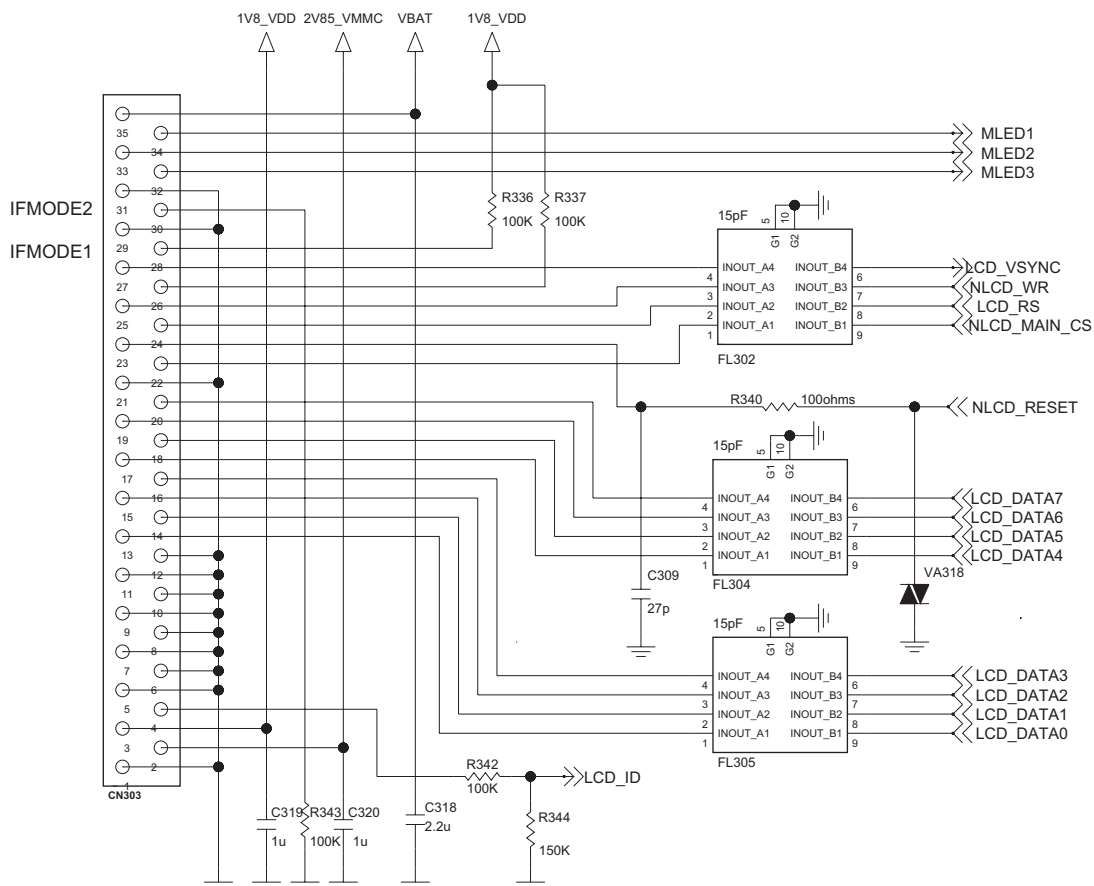


Figure 3-9-1. LCD Interface of LCD FPCB

IM220CBNFA is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 176RGBx220 dots, comprising a 528-channel source driver, a 220-channel gate driver, 87120 bytes RAM for graphic data of 176RGBx220 dots, and power supply circuit.

ILI9225 can operate with low I/O interface power supply up to 1.65V, with an incorporated voltage follower circuit to generate voltage levels for driving an LCD.

The IM220CBNFA also supports a function to display in 8 colors and a standby mode, allowing for precise power control by software. These features make the IM220CBNFA an ideal LCD driver for medium or small size portable products such as digital cellular phones or small PDA, where long battery life is a major concern.

LCD BLU Driver

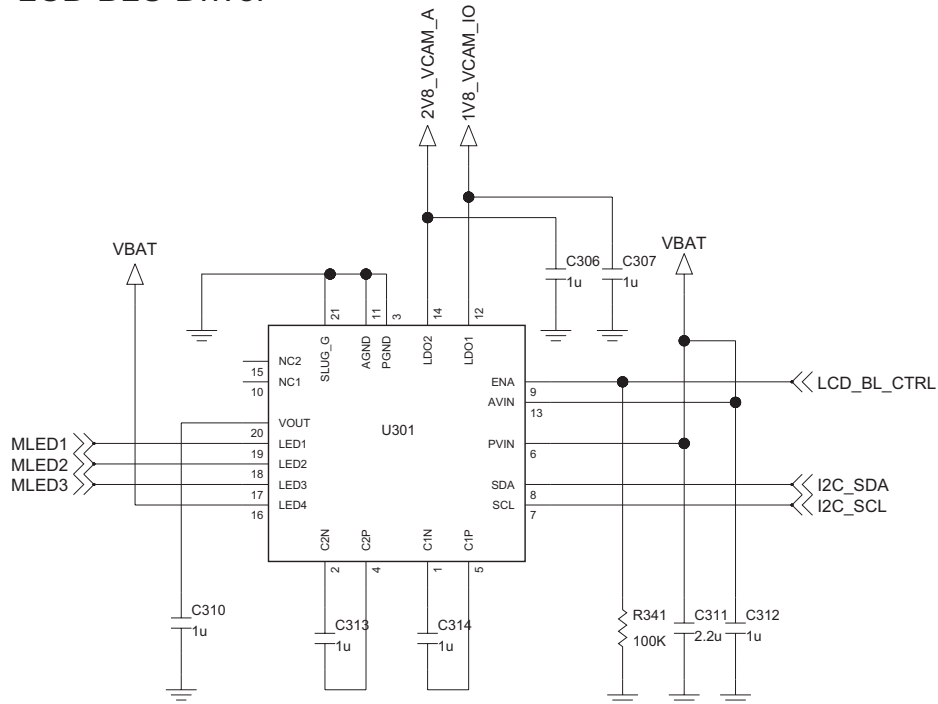


Figure 3-9-2. RT9367C CIRCUIT DIAGRAM

The RT9367 is a high efficiency charge pump LED driver using Richtech's proprietary technology. Performance is optimized for use in single-cell Li-ion battery applications.

The charge pump provides backlight current in conjunction with four matched current sinks. The load and supply conditions determine whether the charge pump operates in 1x, 1.5x, or 2x mode. An optional fading feature that gradually adjusts the backlight current is provided to simplify control software. The RT9367 also provides two low-dropout, low-noise linear regulators for powering a camera module or other peripheral circuits.

The RT9367 uses the I2C interface. The interface controls all functions of the device, including backlight current and two LDO voltage outputs. The single wire implementation minimizes microcontroller and interface pin counts.

In sleep mode, the device reduces quiescent current to 60μA while continuing to monitor the serial interface. The two LDOs can be enabled when the device is in sleep mode. Total current reduces to 1μA in shutdown.



3.10 Battery Charger Interface

CHARGING IC

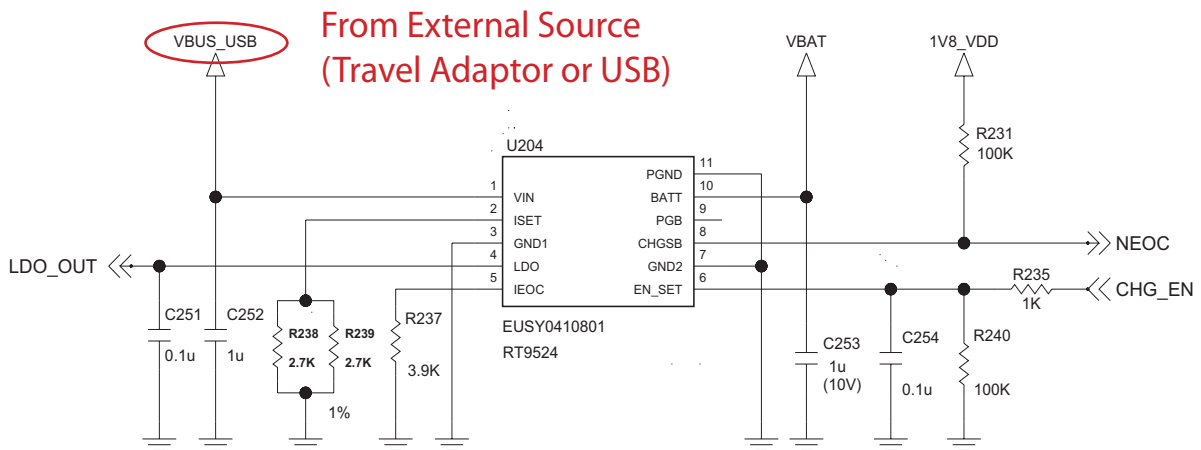


Figure 3-10-1 BATTERY CHARGER BLOCK

The RT9524 is a fully integrated single-cell Li-Ion battery charger IC ideal for portable applications. The RT 9524 optimizes the charging task by using a control algorithm including pre-charge mode, fast charge mode and constant voltage mode. The input voltage range of the VIN pin can be as high as 30V. When the input voltage exceeds the OVP threshold, it will turn off the charging MOSFET to avoid overheating of the chip.

In RT9524, the maximum charging current can be programmed with an external resistor. For the USB application, user can set the current to 100mA/500mA through EN/SET pin. For the factory mode, the RT9524 can allow 4.2V/2.3V power pass through to support system operation. It also provides a 50mA LDO to support the power of peripheral circuit. The internal thermal feedback circuit regulates the die temperature to optimize the charge rate for all ambient temperatures. The RT9524 provides protection functions such as under voltage protection, over voltage protection for VIN supply and thermal protection for battery temperature.

The RT9524 is available in a WDFN-10L 2x3 package to achieve optimized solution for PCB space and thermal considerations.

3. TECHNICAL BRIEF

3.11 Keypad Interface

KEY MATRIX

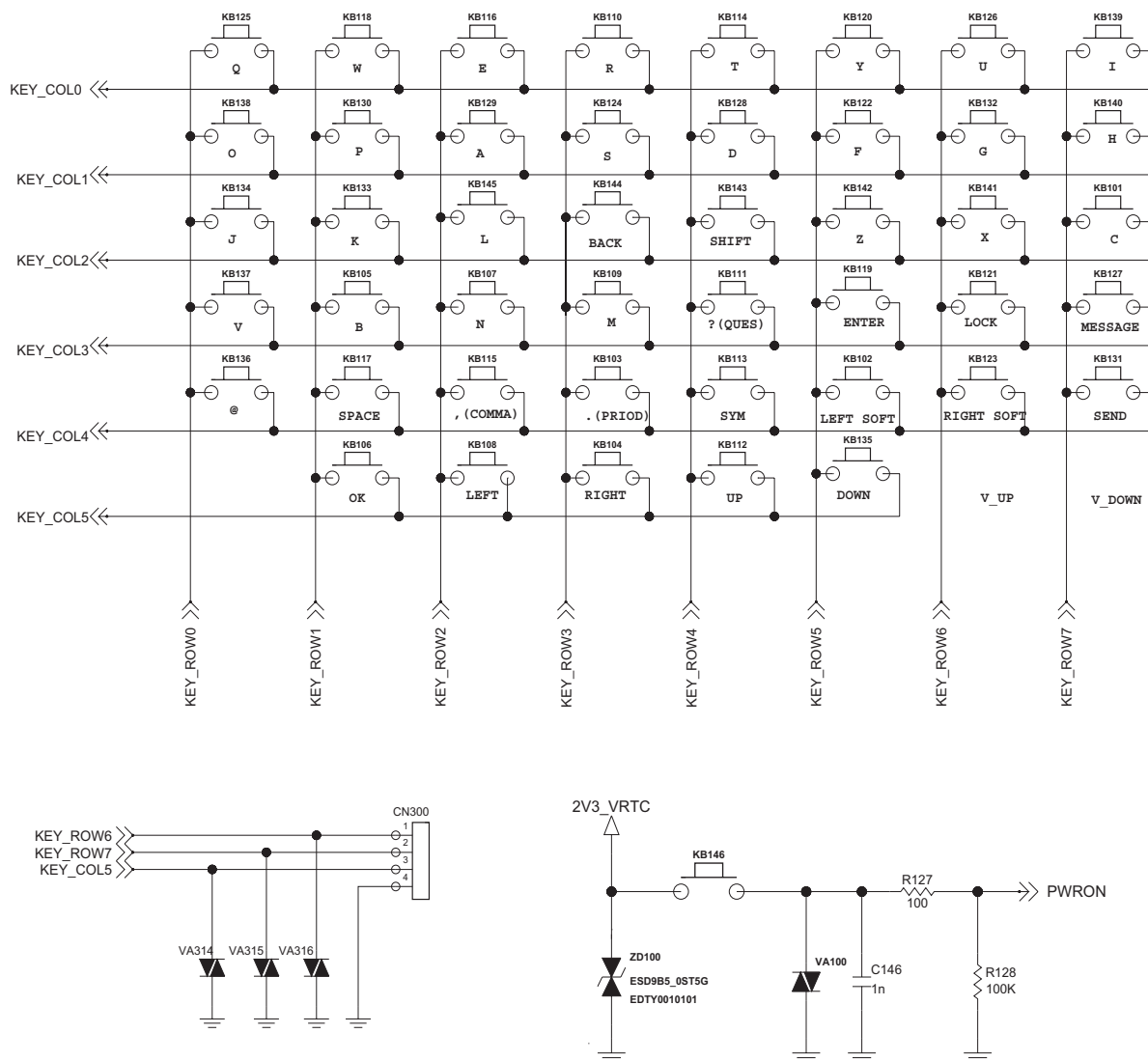
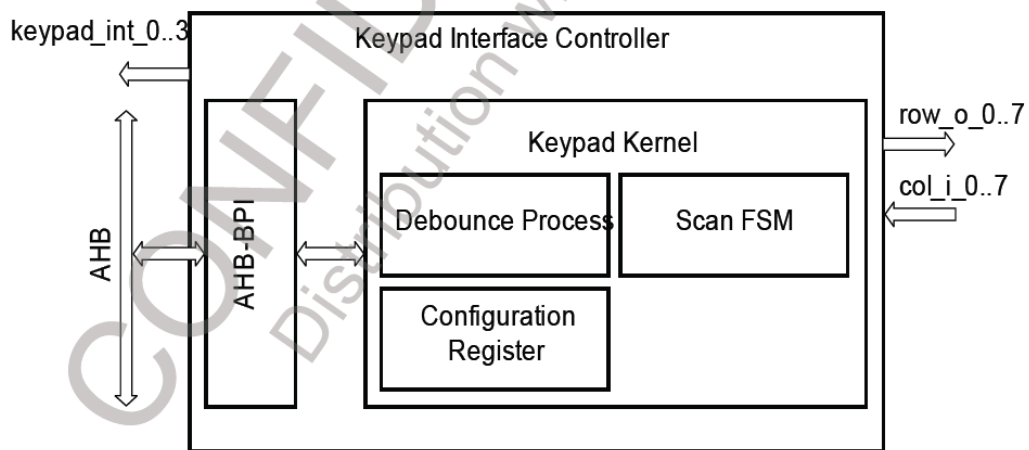


Figure 3-11-1 MAIN KEY STRUCTURE

The Keypad Interface is a peripheral controller, which can be used for scanning external keypad matrices with up to 8 rows and 8 columns (that is 64 standard keys). By adding an additional row of keys connected to ground the number of keys can be extended by up to 8 keys. This results in a maximum number of 72 keys to be identified by the Keypad Interface Controller.

The Keypad Scan Module reduces the number of interrupts and polling through the processor and therefore reduces the power consumption. The module is able to debounce and scan the external keypad matrix automatically without any software intervention. After debouncing it generates an interrupt. The interface controller contains information about the key (or key combination) that was pressed and how long it was pressed.



KEYPAD_1_OVW

Figure 3-11-3 Block Diagram and System Integration of the KPD

3. TECHNICAL BRIEF

3.12 Audio Front-End

3.12.1 Functional Overview

The audio front-end of X-GOLD™213 offers the digital and analog circuit blocks for both receive and transmit audio operation, from a mobile phone perspective (called audio-in and audio-out subsequently). It features a high-quality, stereo digital-to-analog path with amplifier stages for connecting acoustic transducers to X-GOLD™213. In audio-in path the supply voltage generation for electret microphones, a low-noise amplifier and analog to digital conversion are integrated in X-GOLD™213. A more detailed functional description will be given in the following sections.

The audio front-end itself can be considered to be organized in three sub-blocks:

- Interface to processor cores (TEAKLite® and - indirectly - ARM)
- Digital filters
- Analog part

The following figure shows an architecture overview of the Audio section.

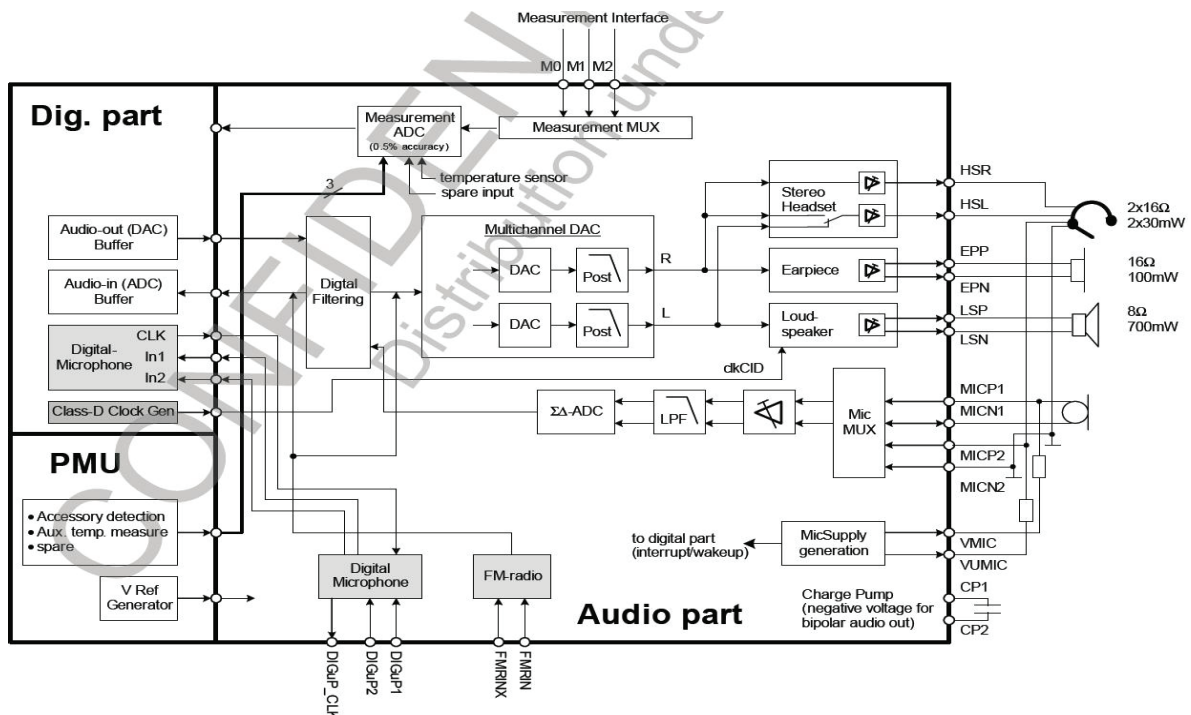


Figure 3.12.1 Audio Section Overview

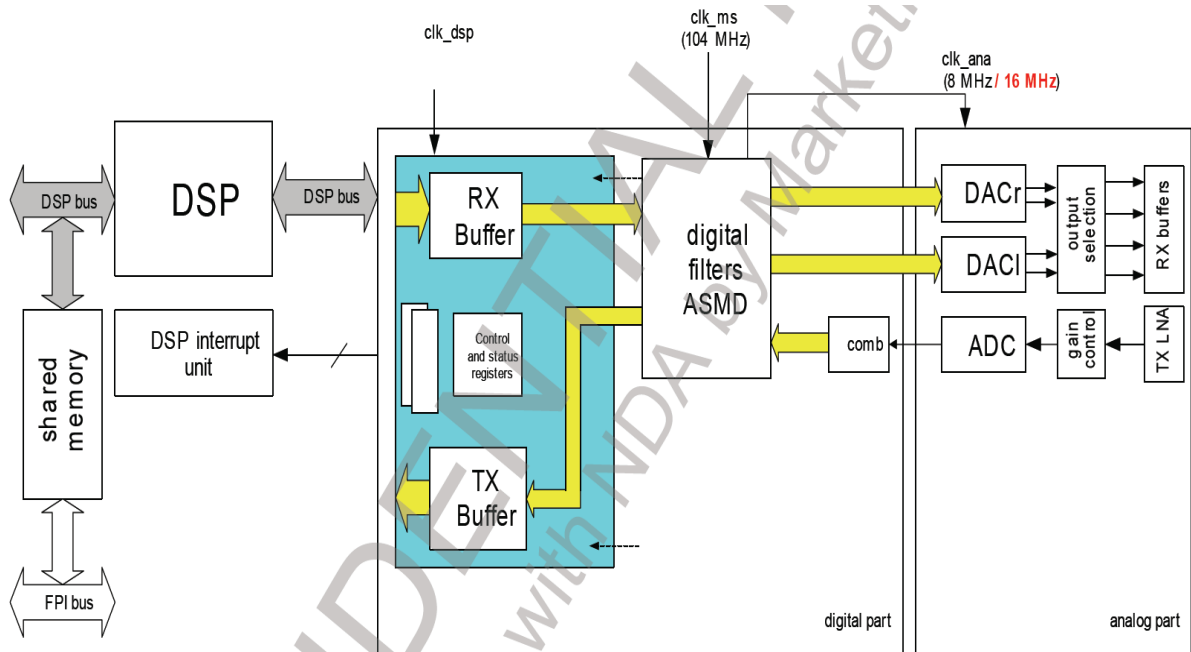


Figure 3.12.2 Overview of Clocking and Interfaces of Audio Front End

The audio front-end of X-GOLD™213 has the following major operation modes:

- Power-down: All analog parts are in power down and all clocks of the digital part are switched off.
- Audio mode: Digital decimation/interpolation filters are connected to the interface buffers and the analog part is enabled.

These major modes can be modified by certain control register settings.

- Due to the new gain settings in the TX path, the maximum input voltage is limited to 0.8 Vpp.
- In both voiceband paths, the value range for voice samples is confined to 97.5%, i.e. to [-31948, 31947] or [8334H, 7CCBH] in X-GOLD™213.
- On the TX path, 83% "1"s on the VTPDM line correspond to a 16-bit value of 7CCBH and 17% "1"s correspond to a 16-bit value of 8334H at the digital filter output. Thus the usable range is 66%. This range can be scaled to 100% by Firmware.
- The high-pass functions of the voiceband filters have to be implemented in firmware on TEAKLite®.

3. TECHNICAL BRIEF

3.12.2 Digital Part

The digital part of the X-GOLD™213 audio front-end comprises an interface to the TEAKLite® bus, interfaces to the interrupt units of TEAKLite®, digital interpolation filters for oversampling digital-to-analog conversion, digital decimation filters for analog-to-digital conversion and an interface to the analog part of the audio front-end. For the digital microphone all the filtering is done in a dedicated hardware. The output sample stream is then fed in a duplicated ring buffer structure like the data from the analog microphone path (after A/D conversion and subsequent digital filtering).

▪ Interpolation Filter

The interpolation path of the X-GOLD™213 audio front-end increases the sampling rate of the audio samples to the rate of the digital-to-analog converter. Because the input sampling rates can vary between 8 kHz and 47.619 kHz the filter characteristic and oversampling ratio can be adjusted to the respective sampling rate. The requirements for the interpolation filters depend on the sampling rate, because a sufficient out-of-band discrimination in the audio frequency band (20 Hz,...,20 kHz) has to be ensured.

▪ Decimation Filter

The digital decimation filter on X-GOLD™213 has two operating modes: 8 kHz output sampling rate and 16 kHz output sampling rate (or 16 kHz output sample rate and 16kHz bandwidth in case of doubled ASMD clock).

3.12.3 Analog Part

The analog part of the X-GOLD™213 audio front-end in audio-out direction consists of a stereo digital to analog converter (multi-bit oversampling converter) which transforms the output of the digital interpolation filter into analog signals. It is followed by the gain control/amplifier section. The DAC outputs can be switched to several output buffers. In audio-in section there is an input multiplexer which selects either one of two differential microphone inputs to be connected to the low-noise amplifier and analog pre-filter. The signals from the analog pre-filter are input to a second-order sigma-delta analog-to-digital converter. In addition there is a connection for FM-radio playing.

▪ Audio-out Part

The analog audio-out part consists of two multi-bit digital-to-analogue converters (DAC) and an output stage. The signal sources are switched to the output drivers in the output stage. The output drivers consist of: a) one mono, differential class-D Loudspeaker driver, b) one mono, differential Earpiece driver and c) one stereo, single-ended (with uni- or bipolar signals), Headset driver.

▪ Digital-to-analog converters

The multi-bit oversampling DACs of the X-GOLD™213 audio front-end convert the 16-bit data words coming from the digital interpolation filters to analogue signals.

▪ Output Amplifier

The different output buffers in X-GOLD™213 are driven by the outputs of the selection block. The differential earpiece driver can be used to drive a 16 Ω earpiece and works in differential. The two single ended headset drivers can be used to drive a 16 Ω headset. They can work unipolar mode, where an AC coupling of the headset might be needed, or can work also in bipolar mode. The differential loudspeaker driver can be used to drive a 8 Ω loudspeaker. As it is a class-D amplifier the needed suppression of the higher harmonics of the switching signals has to be achieved by the external circuitry. The buffers are designed to be short circuit protected.

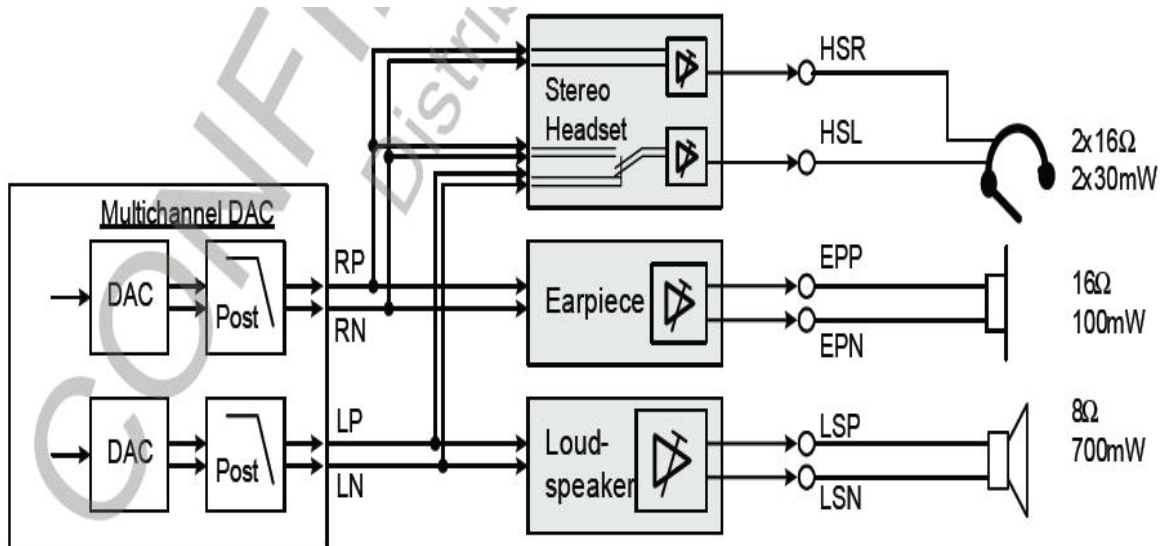


Figure 3.12.3 Switching for R/L DACs onto Buffers

3. TECHNICAL BRIEF

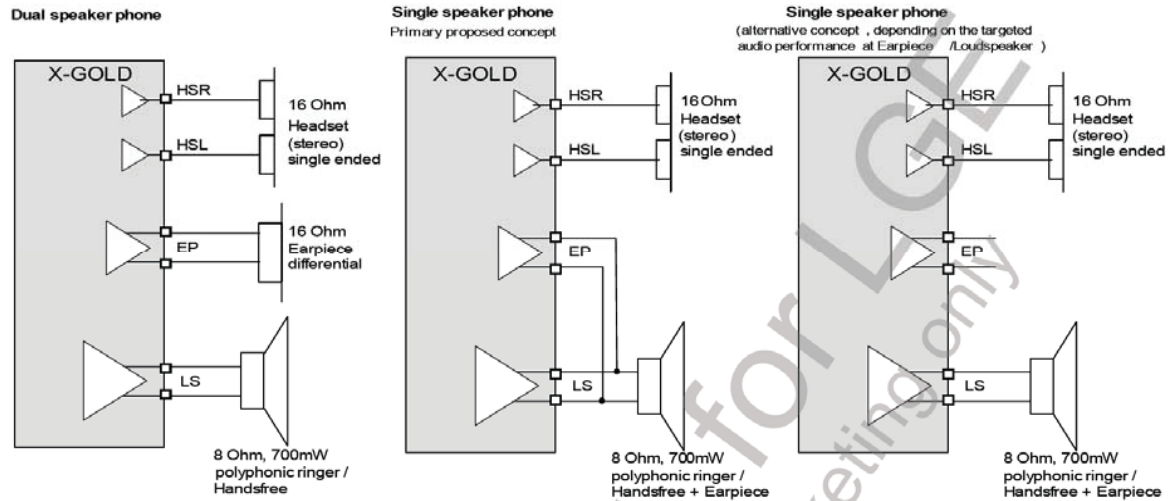


Figure 3.12.4 Different Application Scenarios

In order to achieve the single-speaker concept by parallel connection of Earpiece and Headset amplifier the Earpiece amplifier have to sustain the up to 5 V voltage of the class-D amplifier.

▪ Audio-in Path

The audio-in path of X-GOLD™213 provides two differential microphone input sources, MIC1 and MIC2.

- The inputs for microphone MIC1 are MICP1 and MICN1.
- The inputs for microphone MIC2 are MICP2 and MICN2.

The audio-in path consists of an input selector, a low noise amplifier and following pre-filter with gain control, a second order $\Sigma\Delta$ -converter and a digital decimation filter. It supports both standard GSM (bandwidth 3.5 kHz) and wideband (bandwidth 7 kHz) speech bands.

The differential input signal from the microphone first passes a low noise amplifier and following pre-filter and an anti-aliasing pre-filtering stage achieving an overall variable gain ranging from 0 dB to +39 dB. The signal is then modulated by a second order $\Sigma\Delta$ -converter which is clocked with the same clock rate as the digital to analog converters. The $\Sigma\Delta$ -converter delivers a 1-bit pulse density modulated data stream at a rate of 2 MHz to the digital decimation filter which reduces the rate to 8 kHz or 16 kHz, depending on the current mode.

To improve SNR the sample frequency can be doubled in dedicated modes and the modulated data stream is 4MHz instead of 2 MHz.

▪ Microphone Supply

X-GOLD™213 has a single ended power-supply concept for electret microphones:

For both modes a minimal load capacitance of t.b.d. nF is necessary to guarantee stable operation of the buffer.

The maximal load capacitance must not exceed t.b.d. nF.

2 microphone supplies VMIC and VUMIC are available. The supply VUMIC has a ultra-low-power mode, where the current consumption is minimum, whilst at the same time the noise performance is reduced.

For this purpose the VUMIC is directly supplied out of the VMIC regulator, the Mic-Buffer can be switched off and only the quiescent current of the VMIC regulator is present. This mode can be used to supply a headset and allow accessory detection with highly reduced current consumption For normal operation the supply can be switched to normal operation mode with improved noise performance. In case of an digital microphone VMIC can be used for supplying this microphone.

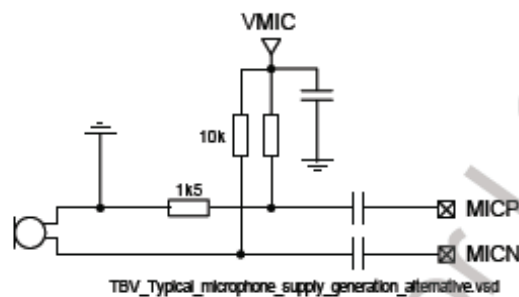


Figure 3.12.5 Typical Microphone Supply Generation (alternative)

3. TECHNICAL BRIEF

3.13 Camera Interface(2M Fixed Focus Camera)

3.13.1 PMB8810 Camera Interface

The Camera Interface (CIF) represents a complete video and still picture input interface (see Figure 3.13.1).

The CIF contains image processing, scaling, and compression functions. The integrated image processing unit supports image sensors with integrated $YCbCr$ processing.

Scaling is used for downsizing the sensor data for either displaying them on the LCD, or for generating data streams for MPEG-4 compression. In general, $YCbCr$ 4:2:2 JPEG compressed images should use the full sensor resolution, but they can also be downscaled to a lower resolution for smaller JPEG files. Scaling also can be used for digital zoom effects, because the scalers are capable of up-scaling as well.

CIF

All data is transmitted via the memory interface to an AHB bus system using a bus master interface.

Programming is done by register read/write transactions using an AHB slave interface.

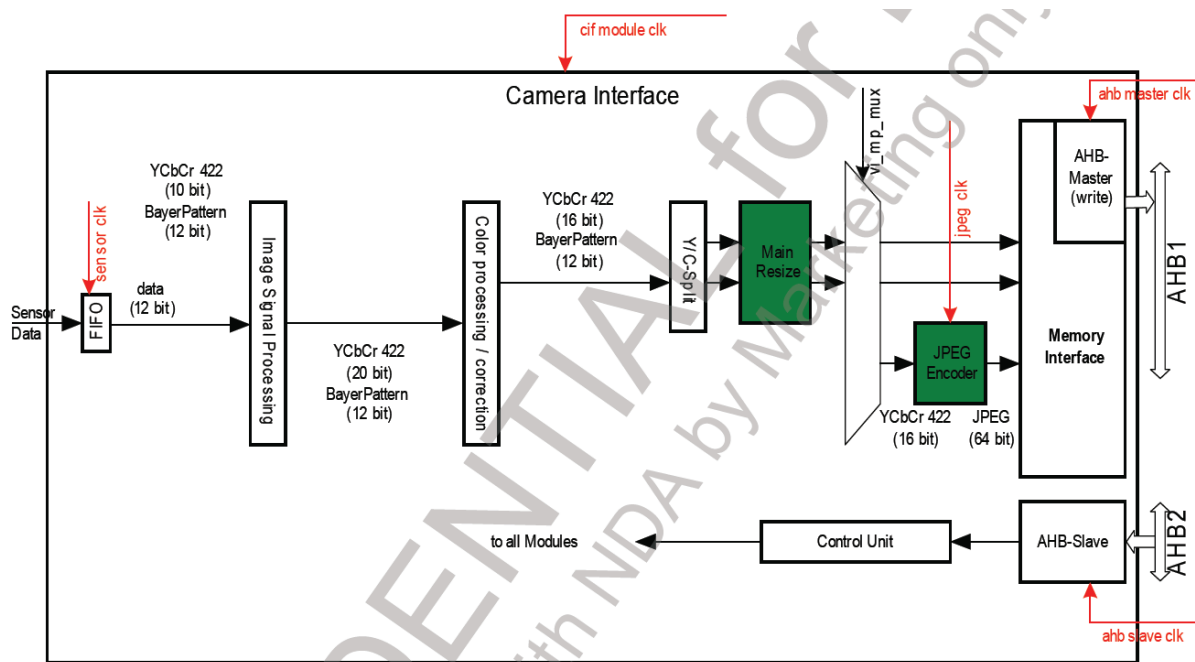


Figure 3.13.1 Block Diagram of Camera Interface

Functional Overview of CIF

The following list gives an overview over the CIF's functionality:

- 78 MHz system clock
- 78 MHz sensor clock
- 78 MHz JPEG encoder clock
- 32-bit AHB slave programming interface
- ITU-R BT 601 compliant video interface supporting YC_bC_r
- ITU-R BT 656 compliant video interface supporting YC_bC_r data
- 8-bit camera interface
- 12-bit resolution per color component internally
- YC_bC_r 4:2:2 processing
- Hardware JPEG encoder incl. JFIF1.02 stream generator and programmable quantization and Huffman tables
- Windowing and frame synchronization
- Continuous resize support
- Frame skip support for video (e.g. MPEG-4) encoding
- Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
- Programmable polarity for synchronization signals
- Luminance/chrominance and chrominance blue/red swapping for YUV input signals
- Maximum input resolution of 3 Mpixels (2048x1536 pixels)
- Main scaler with pixel-accurate up- and down-scaling to any resolution between 3 MP (2048x1536) and 32x16
- pixel in processing mode
- Buffer in system memory organized as ring-buffer
- Buffer overflow protection for raw data and JPEG files
- Asynchronous reset input, software reset for the entire IP and separate software resets for all sub-modules
- Interconnect test support
- Semi planar storage format
- Color processing (contrast, saturation, brightness, hue)
- Power management by software controlled clock disabling of currently not needed sub-modules

3. TECHNICAL BRIEF

3.14 KEY BACKLIGHT LED Interface

Key Backlight LED is controlled by switch (Q200). If KEY_BL_EN is high, Current is flowing from VBAT to LED. Then Light emitted from The LED.

KEY_BL_EN is operating PWM. It is reducing current consumption.

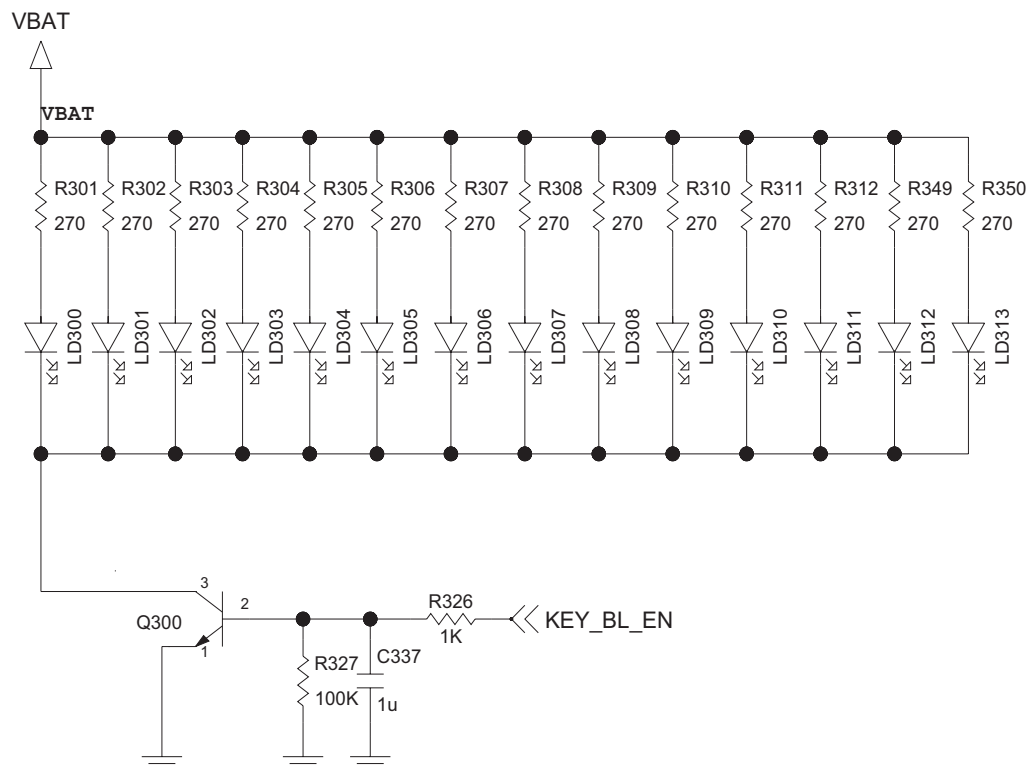


Figure 3-14-1 Key Backlight Block

3.15 Vibrator Interface

Support PWM signal which generated by hardware itself via register control
 Direct connect to the VIB and VSSVIB pin from XMM2130 without any external component required.
 It is capable to driver the vibrator motor up to 150mA.

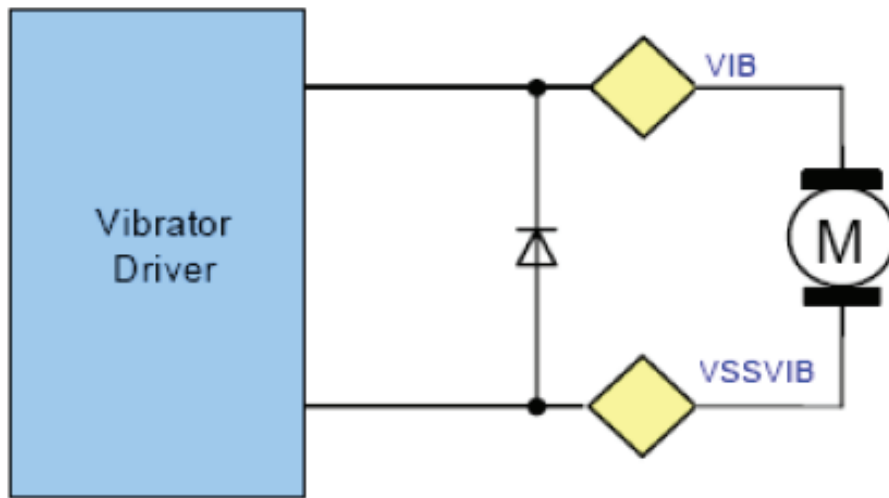


Figure 3-15-1 Vibrator Driver Block Diagram

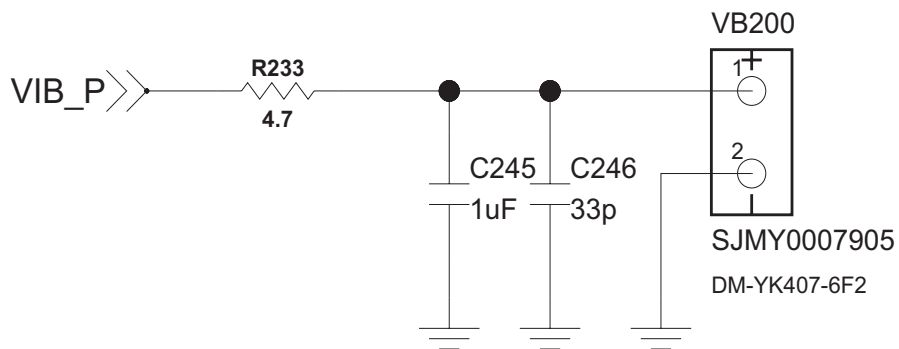


Figure 3-15-2 Vibrator Driver Block

4. TROUBLE SHOOTING

4.1 RF Component

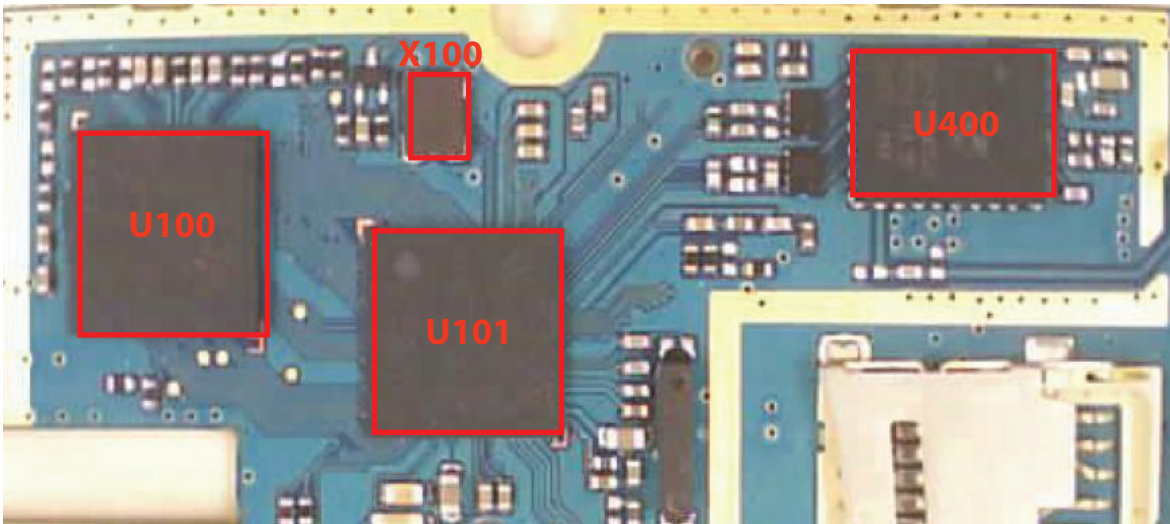
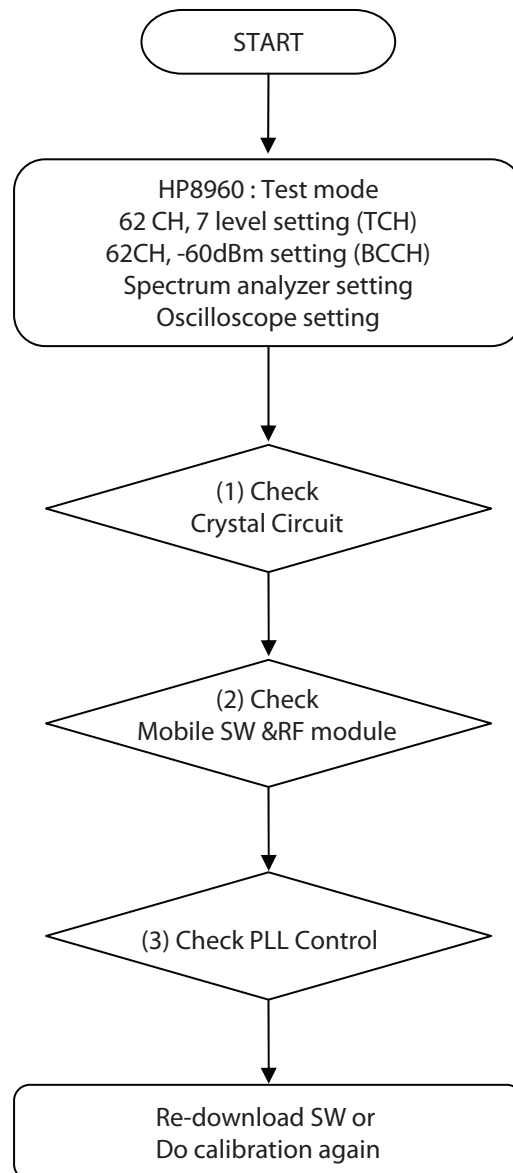


Figure 4.1

U100	Memory(512NOR/128pSDRAM)
U101 (PMB8810)	Main Chip (A-GOLDRADIO+)
U400	RF Module
X100	Crystal, 26MHz Clock

4.2 RX Trouble

CHECKING FLOW



4. TROUBLE SHOOTING

(1) Checking Crystal Circuit

TEST POINT

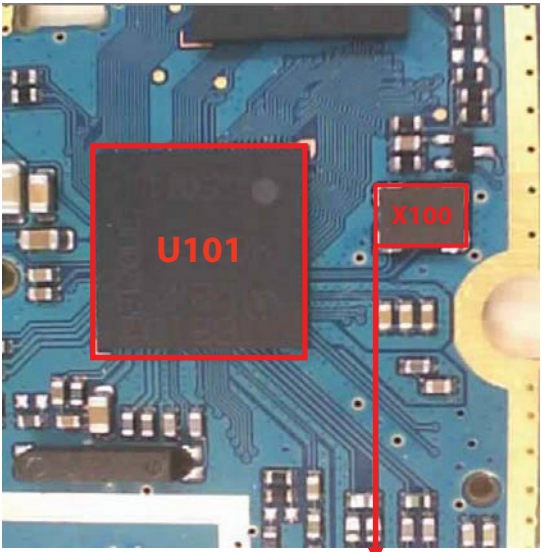
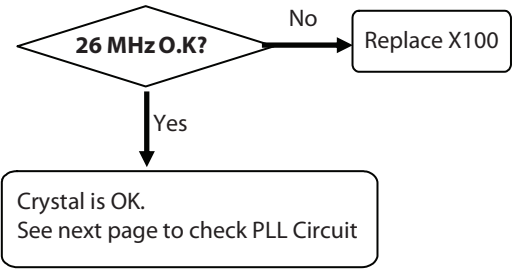


Figure 4.2.1 1 pin : 26MHz

CHECKING FLOW



CIRCUIT

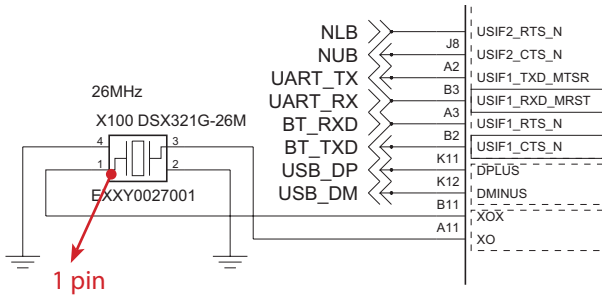


Figure 4.2.2

WAVEFORM

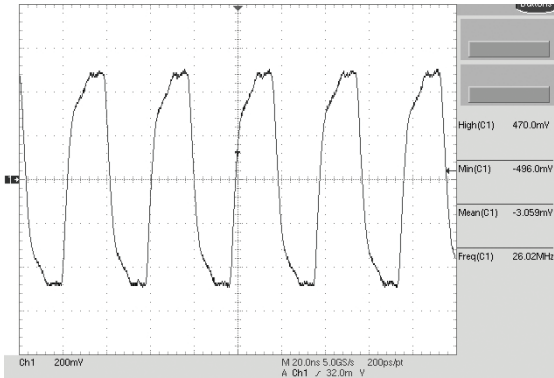


Figure 4.2.3

(2) Checking Mobile SW &FEM

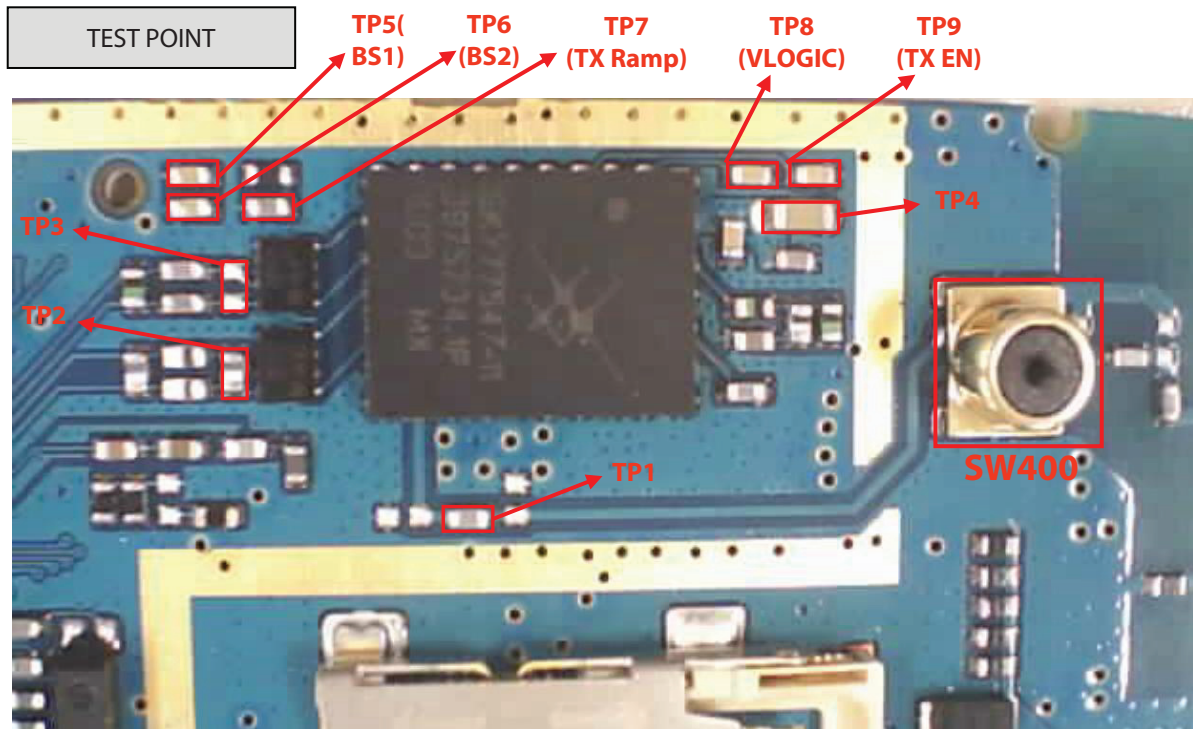
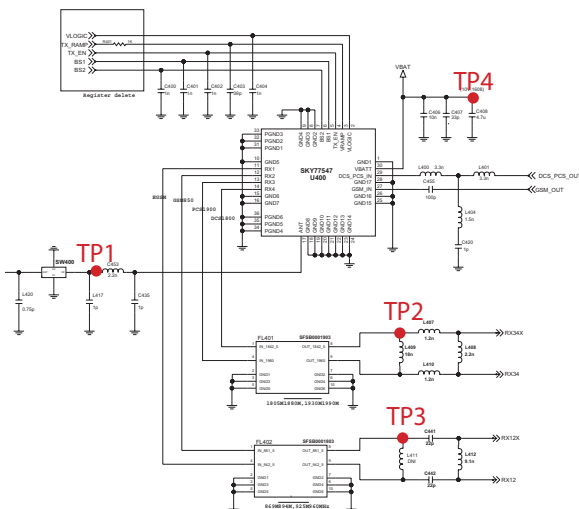


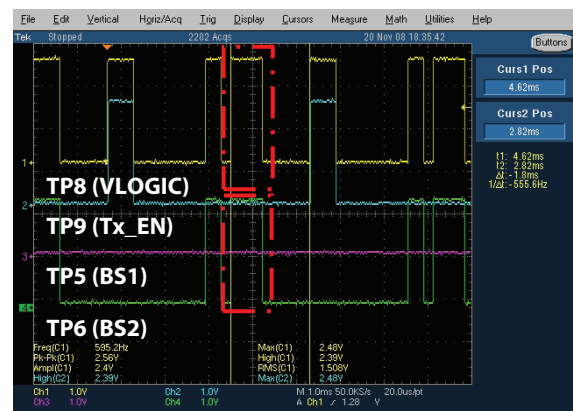
Figure 4.2.4

CIRCUIT

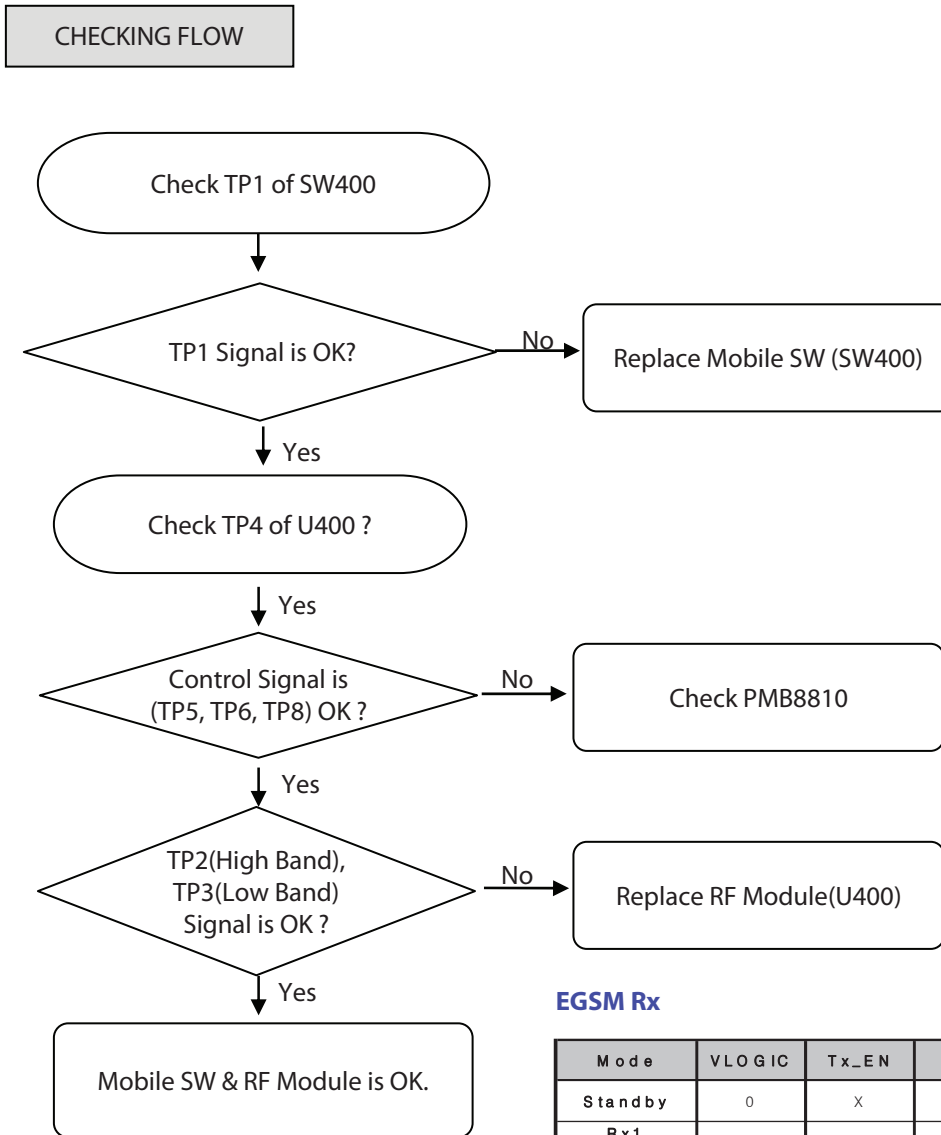


CONTROL LOGIC

EGSM Rx



4. TROUBLE SHOOTING

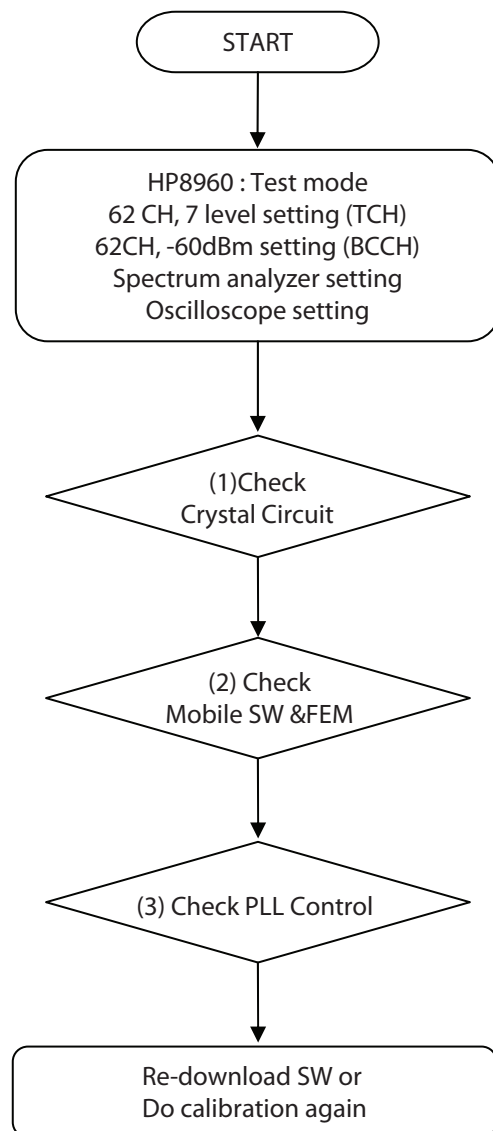


EGSM Rx

Mode	VLOGIC	Tx_EN	BS1	BS2
Standby	0	X	X	X
Rx1 (GSM850)	1	0	0	0
Rx2 (EGSM)	1	0	0	1
Rx3 (DCS)	1	0	1	1
Rx4 (PCS)	1	0	1	0
LB_Tx	1	1	0	X
HB_Tx	1	1	1	X

4.3 TX Trouble

CHECKING FLOW



4. TROUBLE SHOOTING

(1) Checking Crystal Circuit

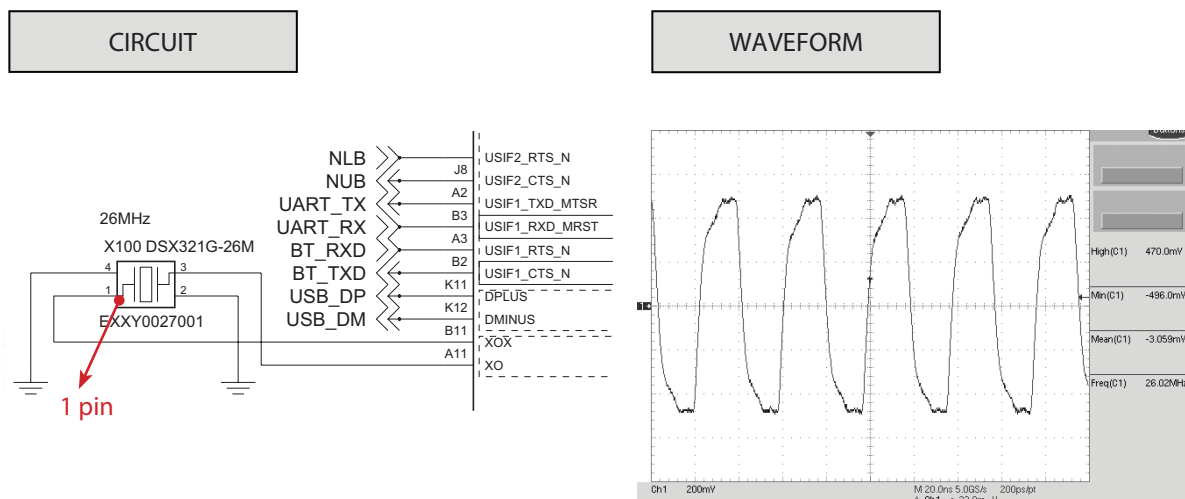
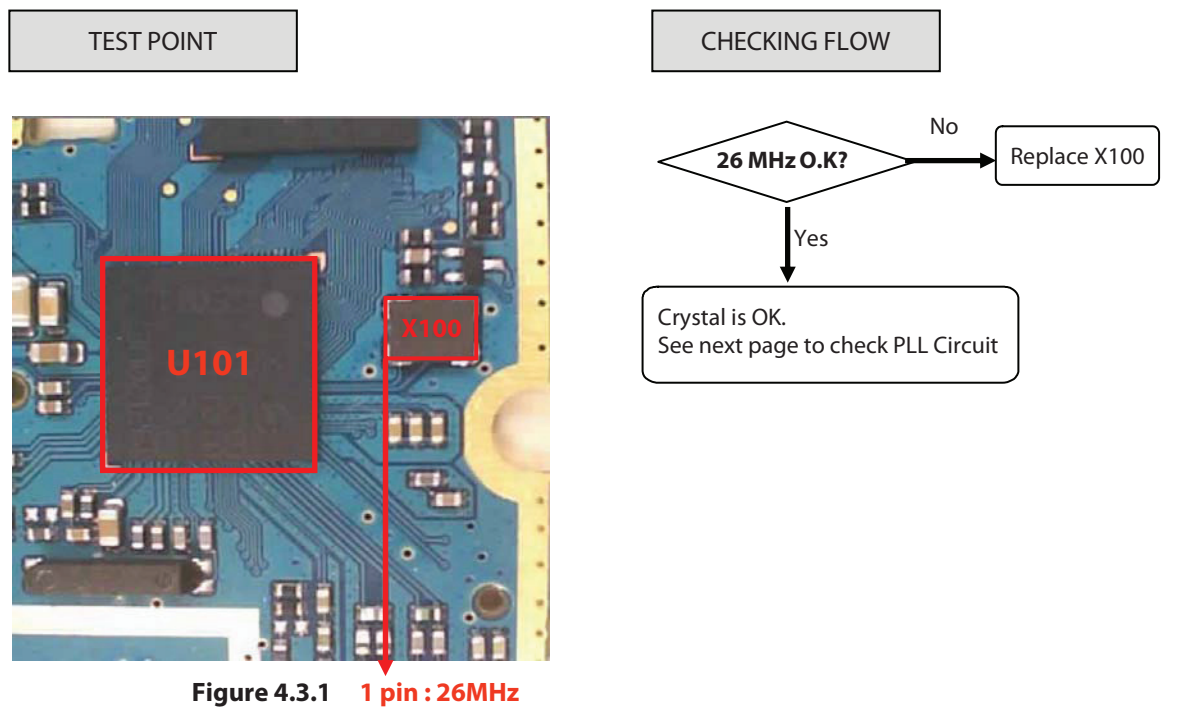


Figure 4.3.2

Figure 4.3.3

(2) Checking Mobile SW & TX Module

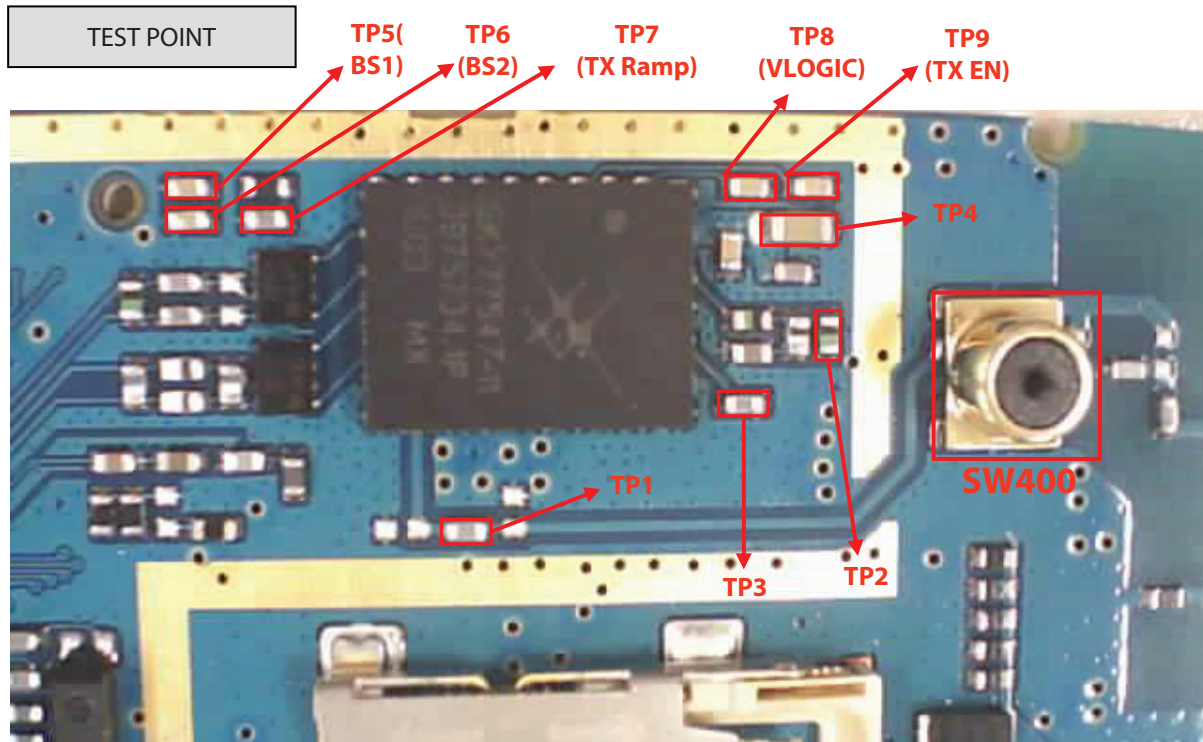
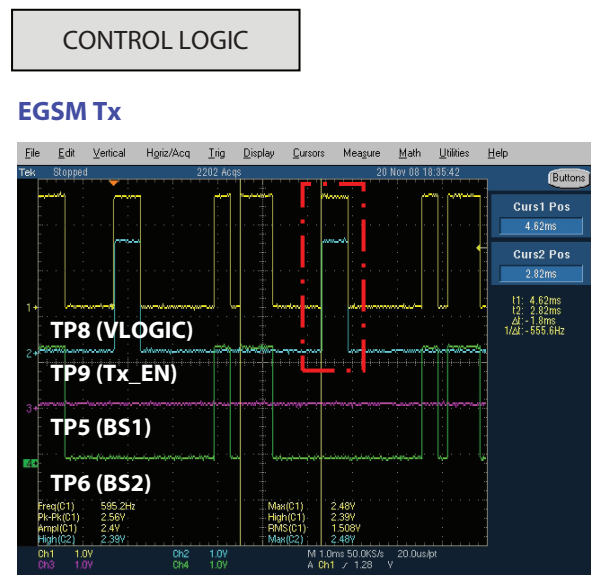
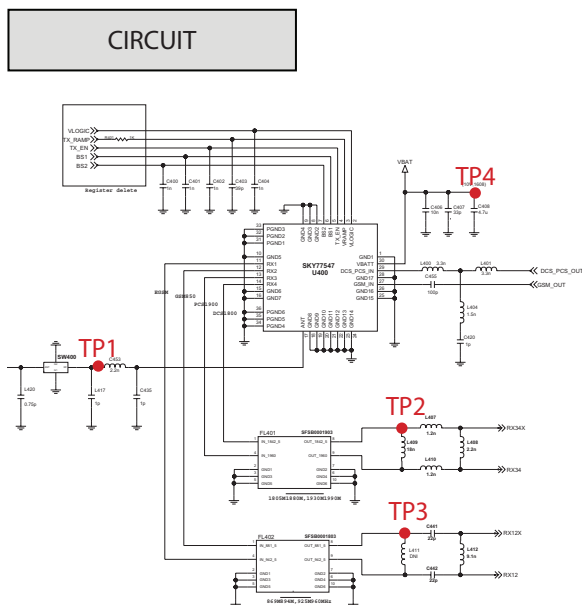
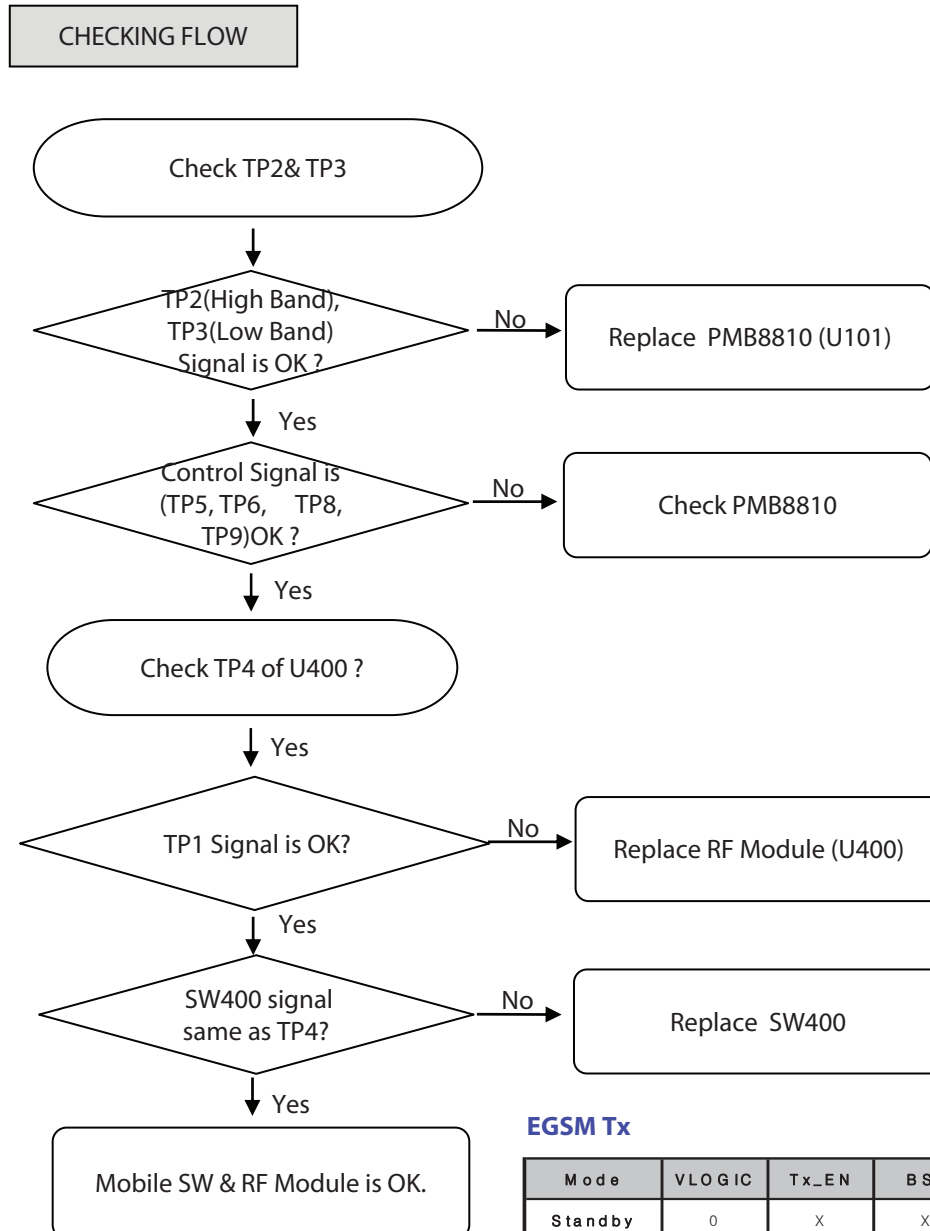


Figure 4.3.4



4. TROUBLE SHOOTING



EGSM Tx

Mode	VLOGIC	Tx_EN	BS1	BS2
Standby	0	X	X	X
Rx1 (GSM850)	1	0	0	0
Rx2 (EGSM)	1	0	0	1
Rx3 (DCS)	1	0	1	1
Rx4 (PCS)	1	0	1	0
LB_Tx	1	1	0	X
HB_Tx	1	1	1	X

4.4 Power On Trouble

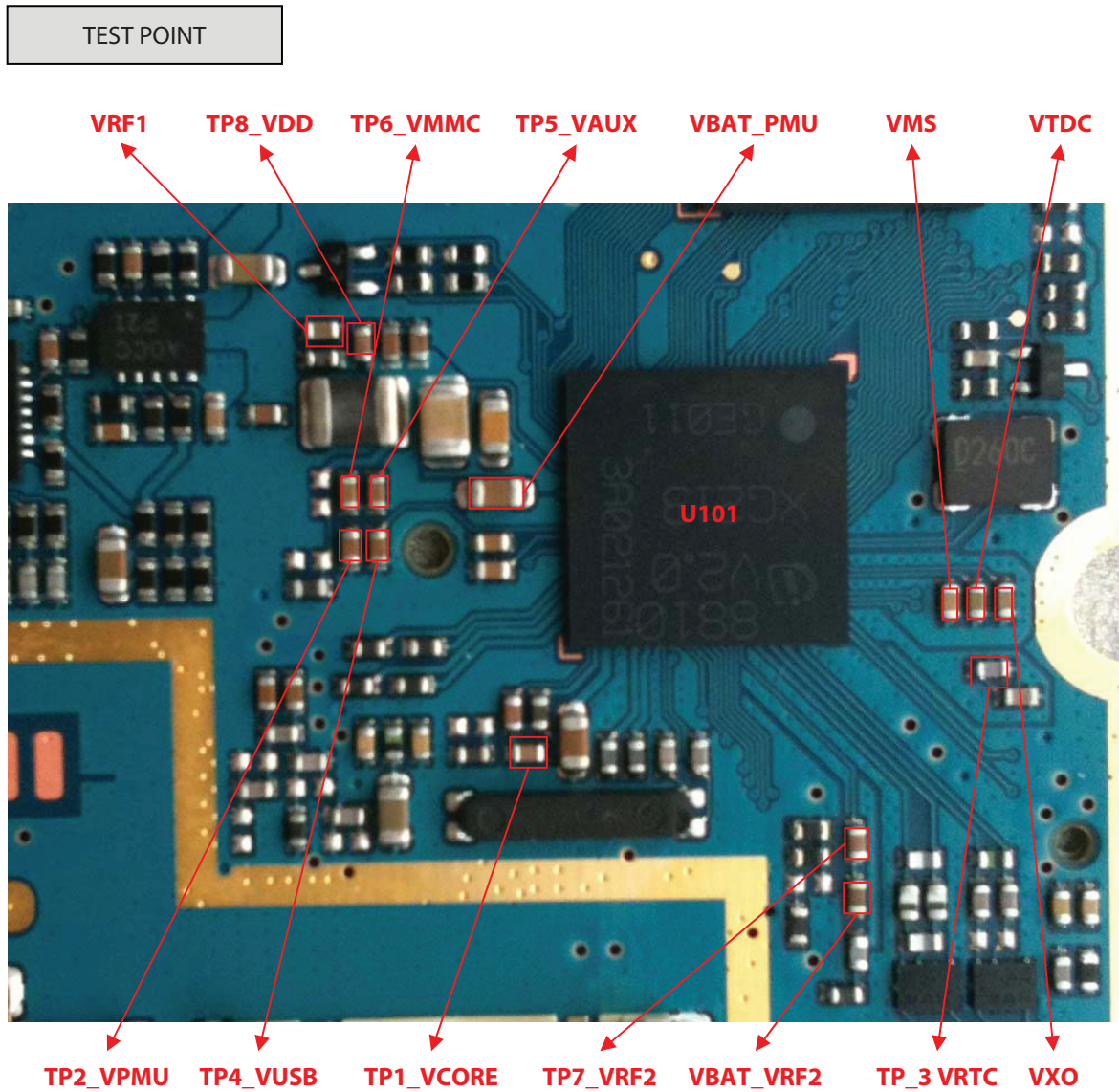
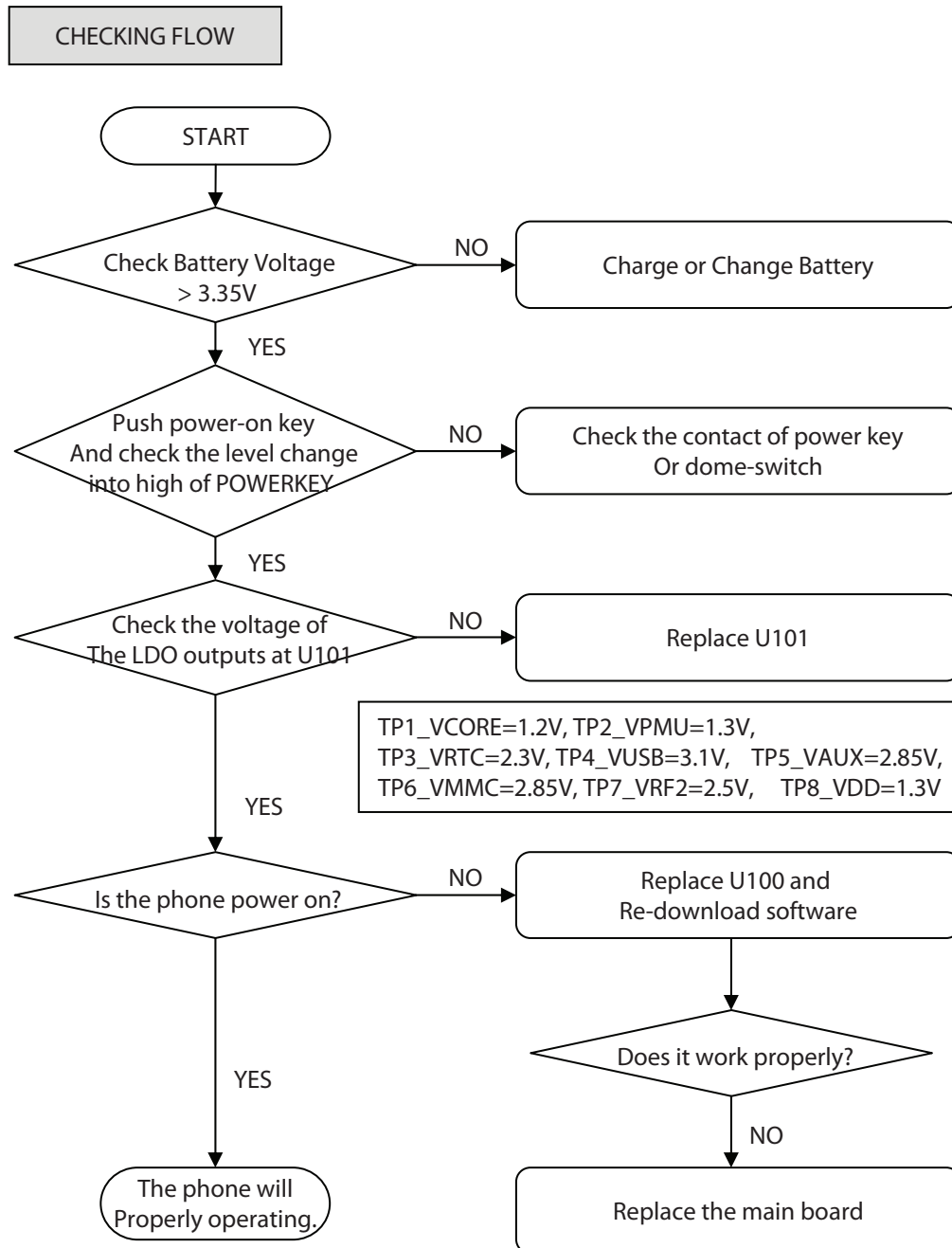


Figure 4.1

CIRCUIT





4.5 Charging Trouble

TEST POINT

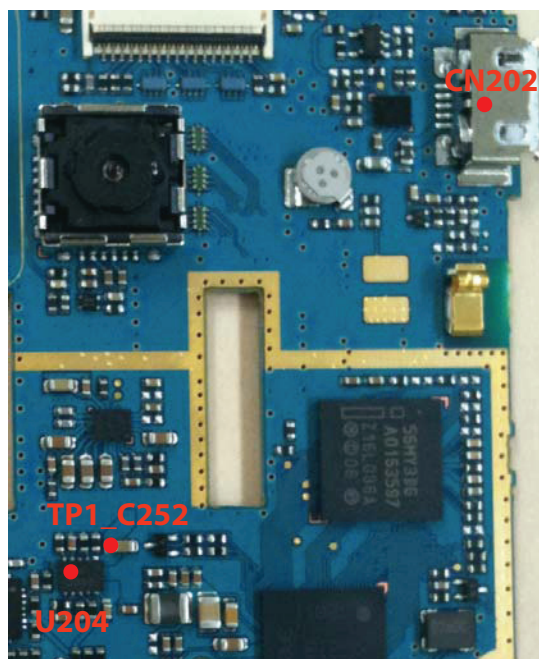
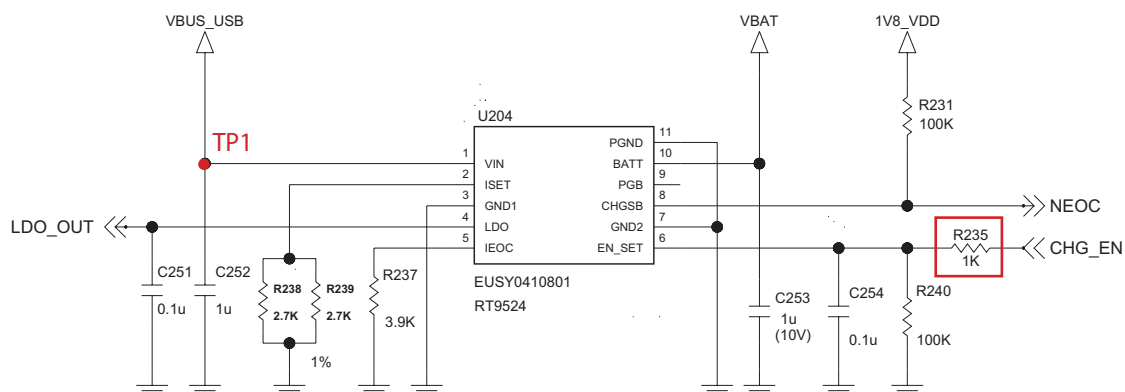


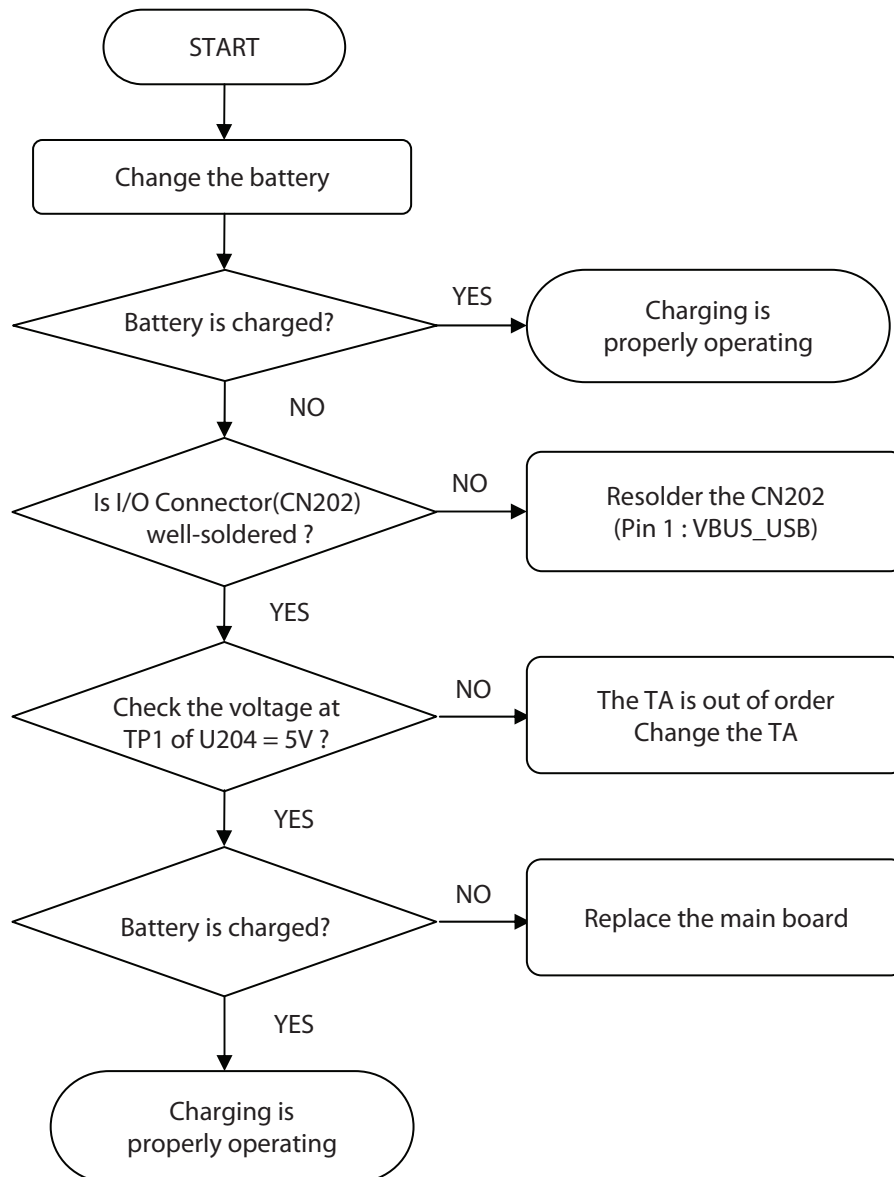
Figure 4.5

CIRCUIT

CHARGING IC



CHECKING FLOW



4. TROUBLE SHOOTING

4.6 Vibrator Trouble

TEST POINT

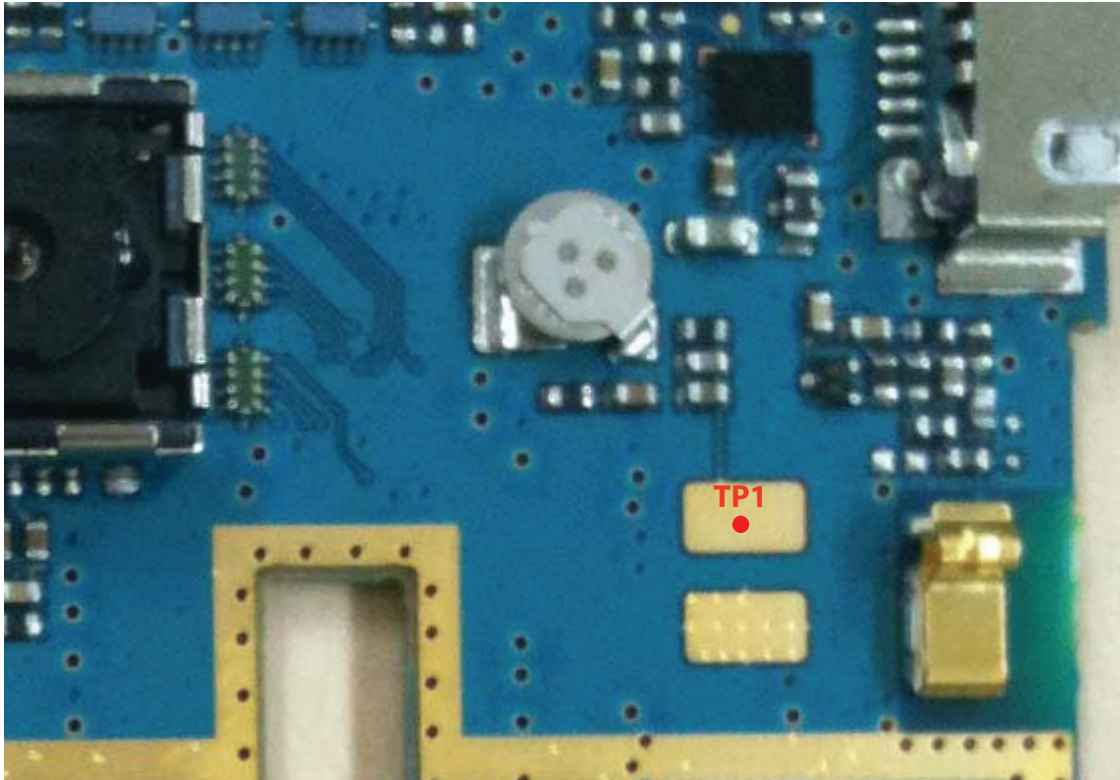
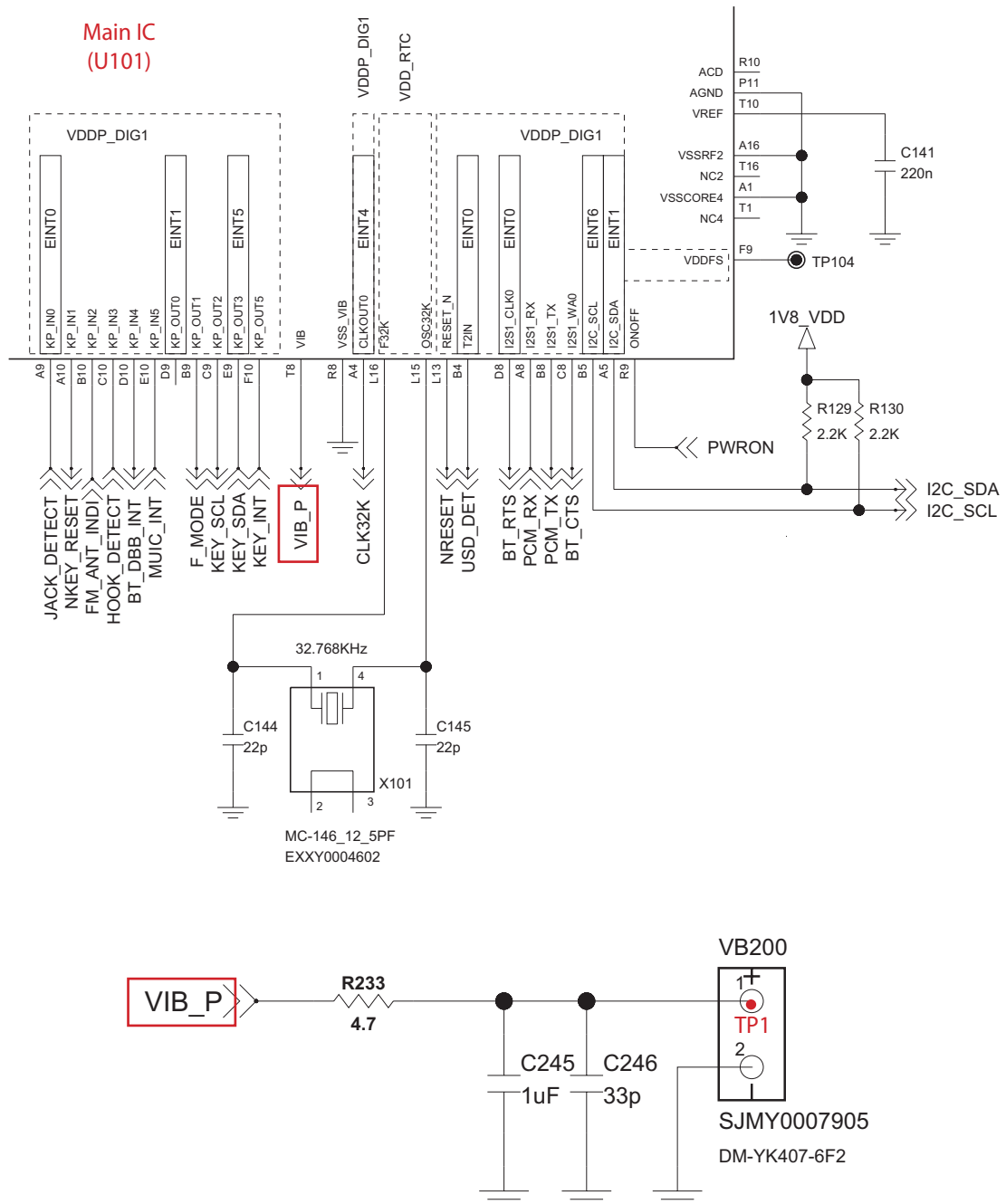


Figure 4.6

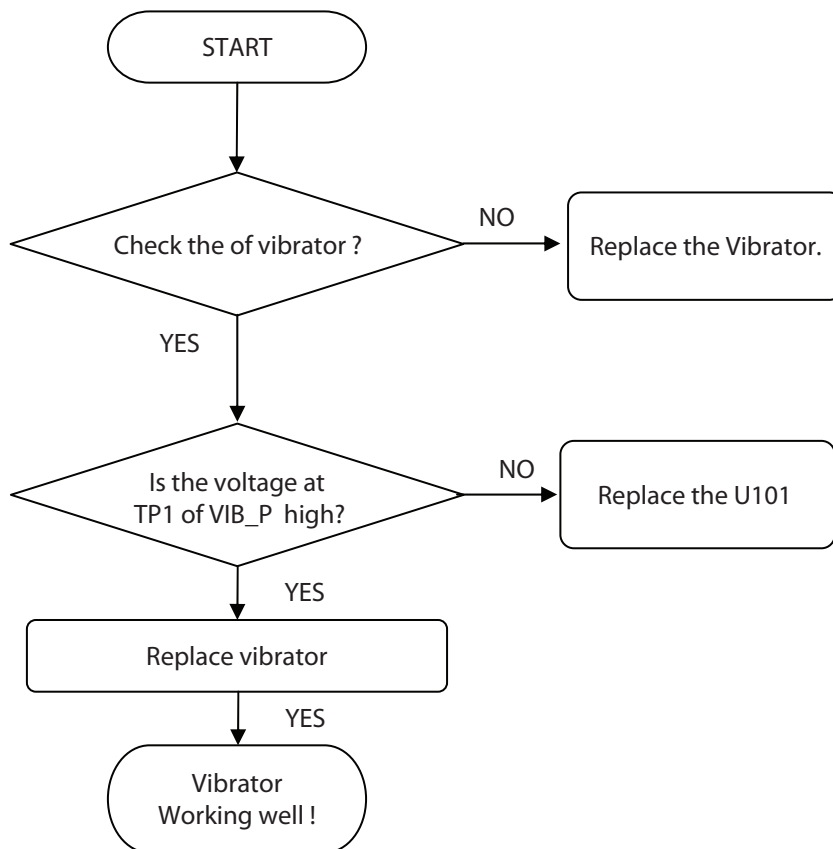
CIRCUIT



4. TROUBLE SHOOTING

CHECKING FLOW

SETTING : Enter the engineering mode, and set vibrator on at vibration of BB test menu



4.7 LCD Trouble

TEST POINT

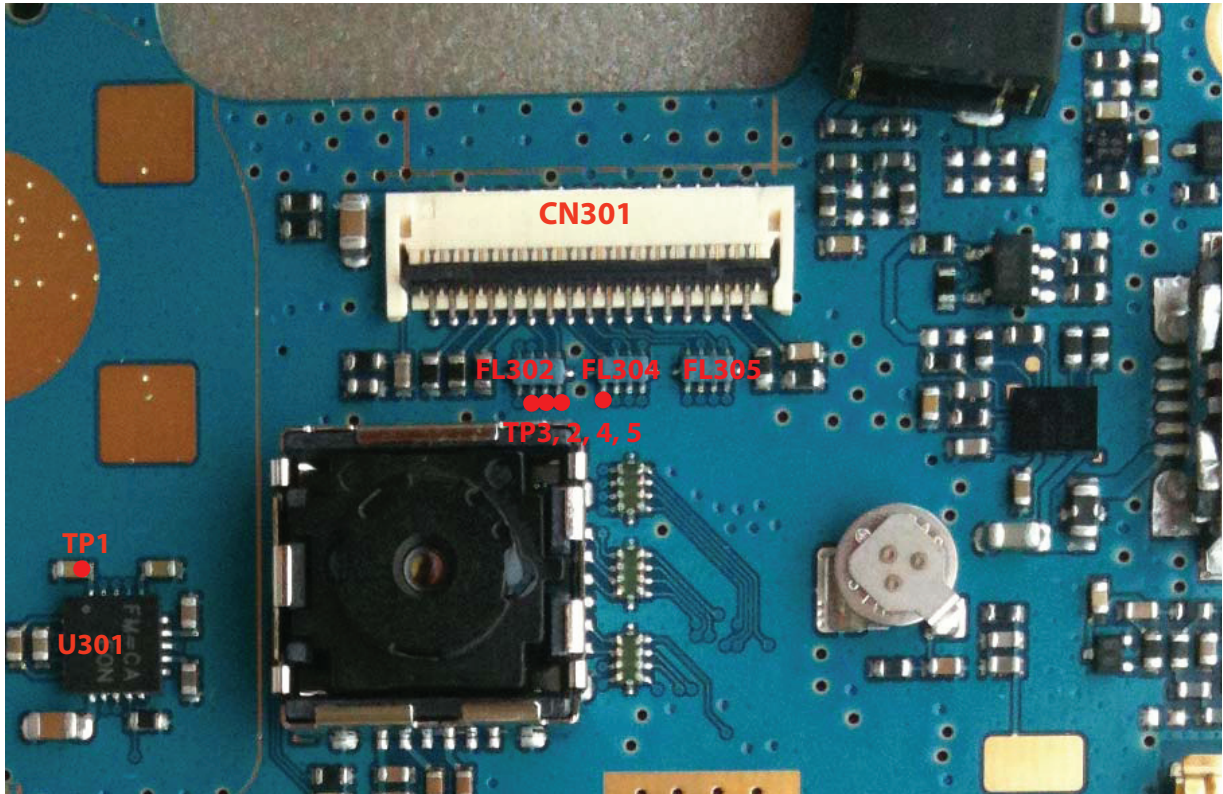
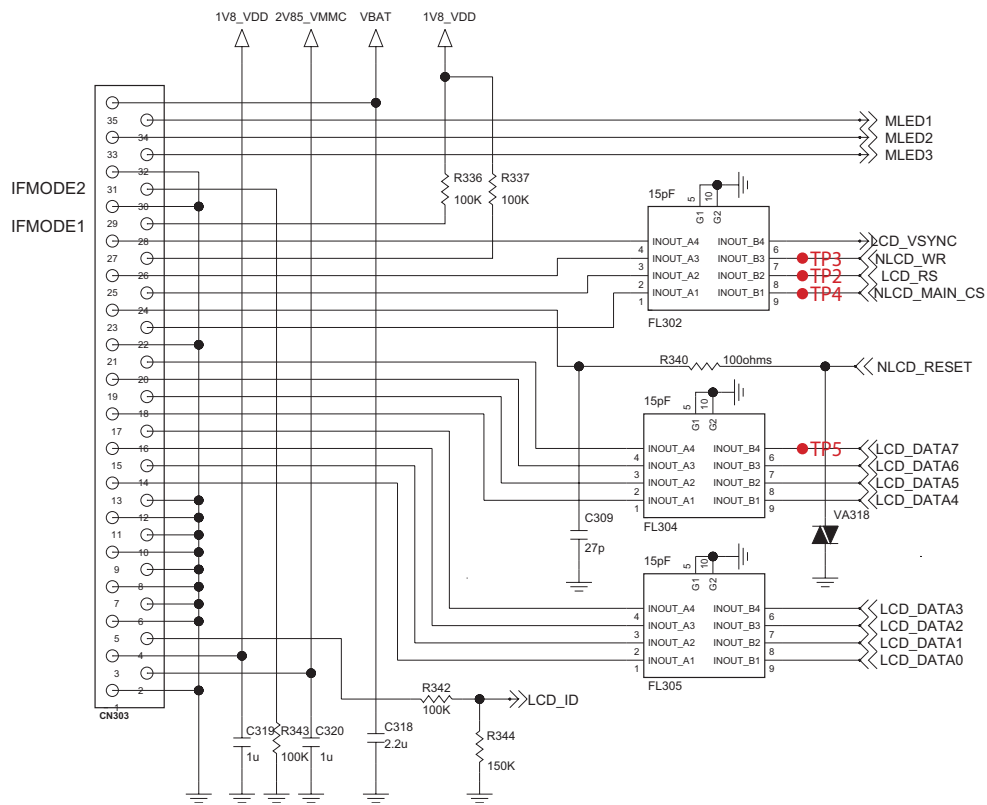


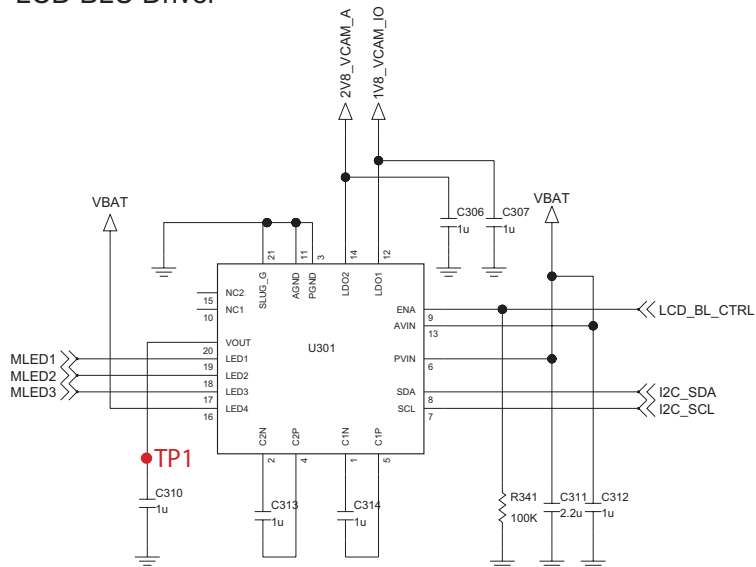
Figure 4.7

4. TROUBLE SHOOTING

CIRCUIT

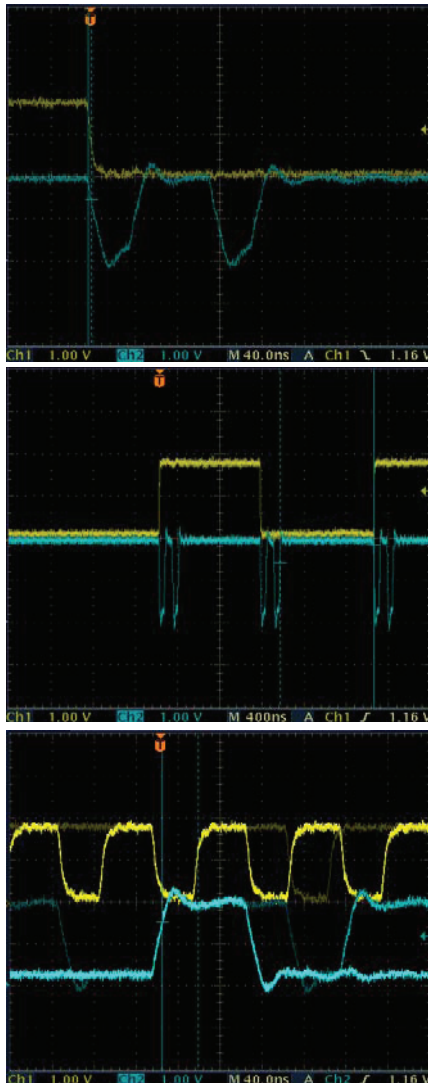


LCD BLU Driver



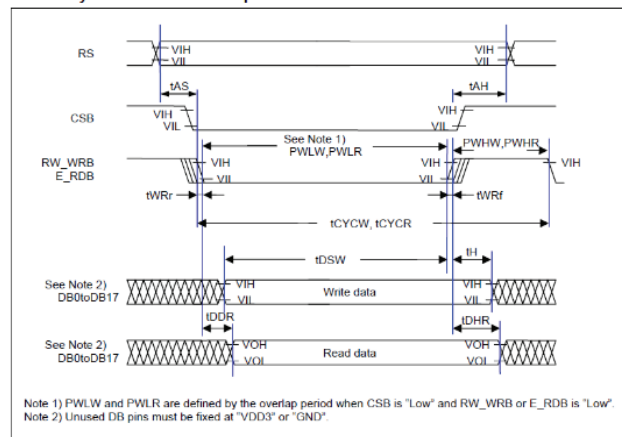
Waveform

Bus Interface Operation



15. Timing characteristics

15.1. 80-system bus interface operation



15.2. Timing Characteristics

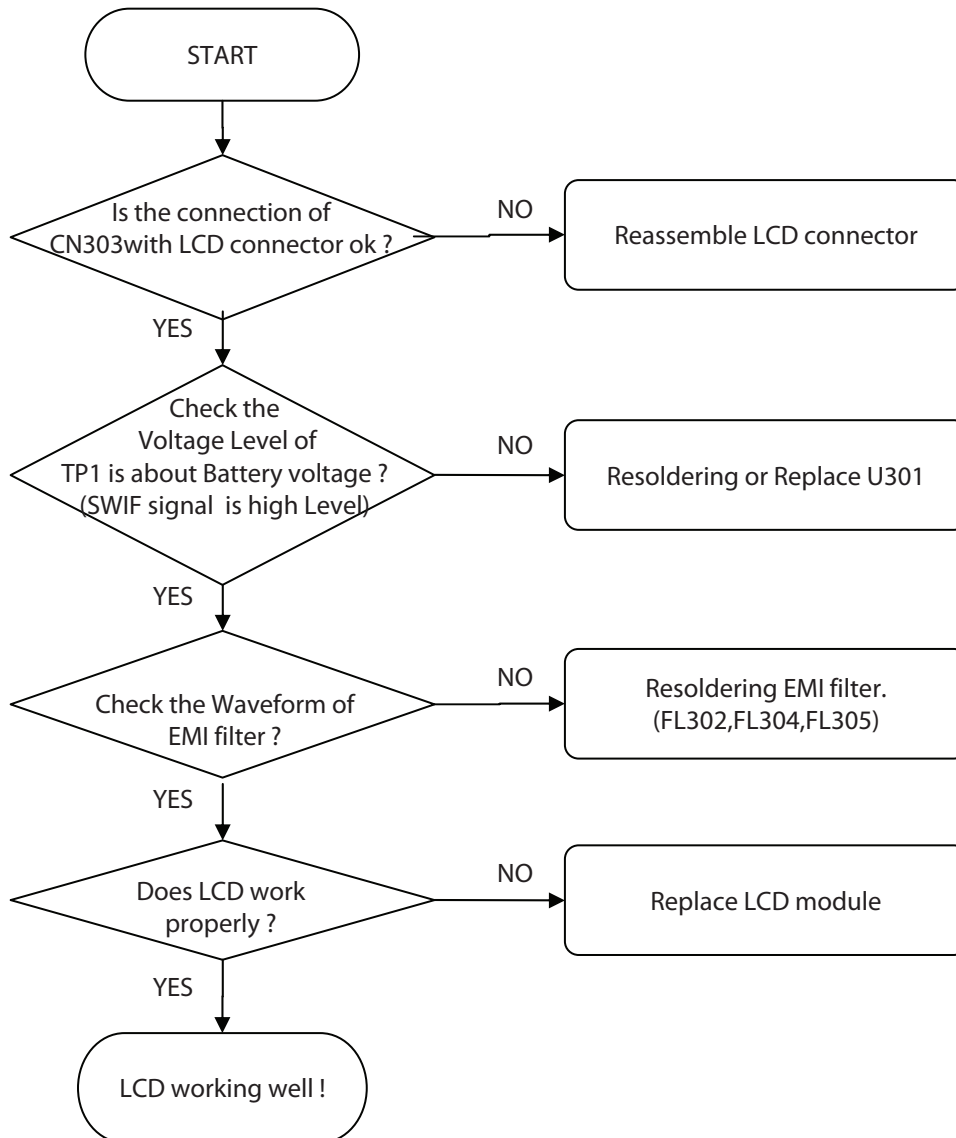
Normal Write Mode (HWM=0) (IOVcc=1.65~3.3V, Vcc=Vcl=2.5~3.3V, Ta=25°C)

Item	Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	tcycw	ns	80	-
	Read	tcycr	ns	350	-
Write "Low" level pulse width	Write	PWLW	ns	15	-
Read "Low" level pulse width	Read	PWLR	ns	200	-
Write "High" level pulse width	Write	PWHW	ns	15	-
Read "High" level pulse width	Read	PWHR	ns	150	-
Write/Read rise/fall time	tWrr, tWrf	ns	-	-	25
Setup time	Write(RS-CS/, WR/)	tAS	ns	0	-
	Read(RS-CS/, WR/)	tAH	ns	10	-
Address hold time	tAH	ns	2	-	-
Write data setup time	tDSW	ns	25	-	-
Write data hold time	tH	ns	5	-	-
Read data delay time	tDDR	ns	-	-	20
Read data hold time	tDHR	ns	5	-	-

Graph 4.7.2. LCD Data Waveform

4. TROUBLE SHOOTING

CHECKING FLOW



4.8 Camera Trouble

TEST POINT

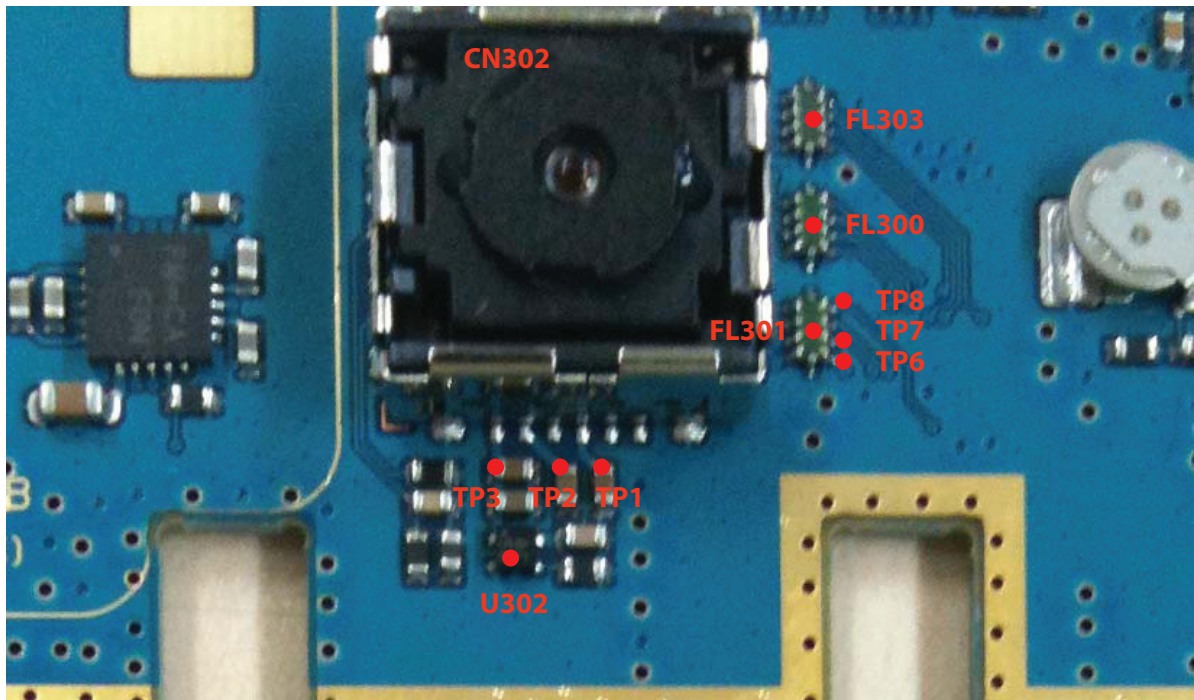


Figure 4.8

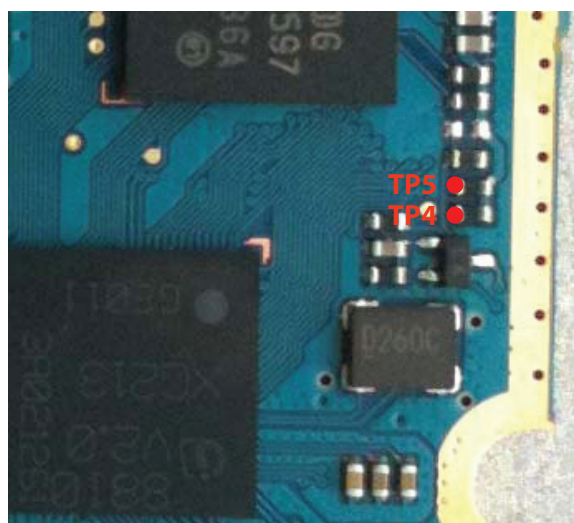
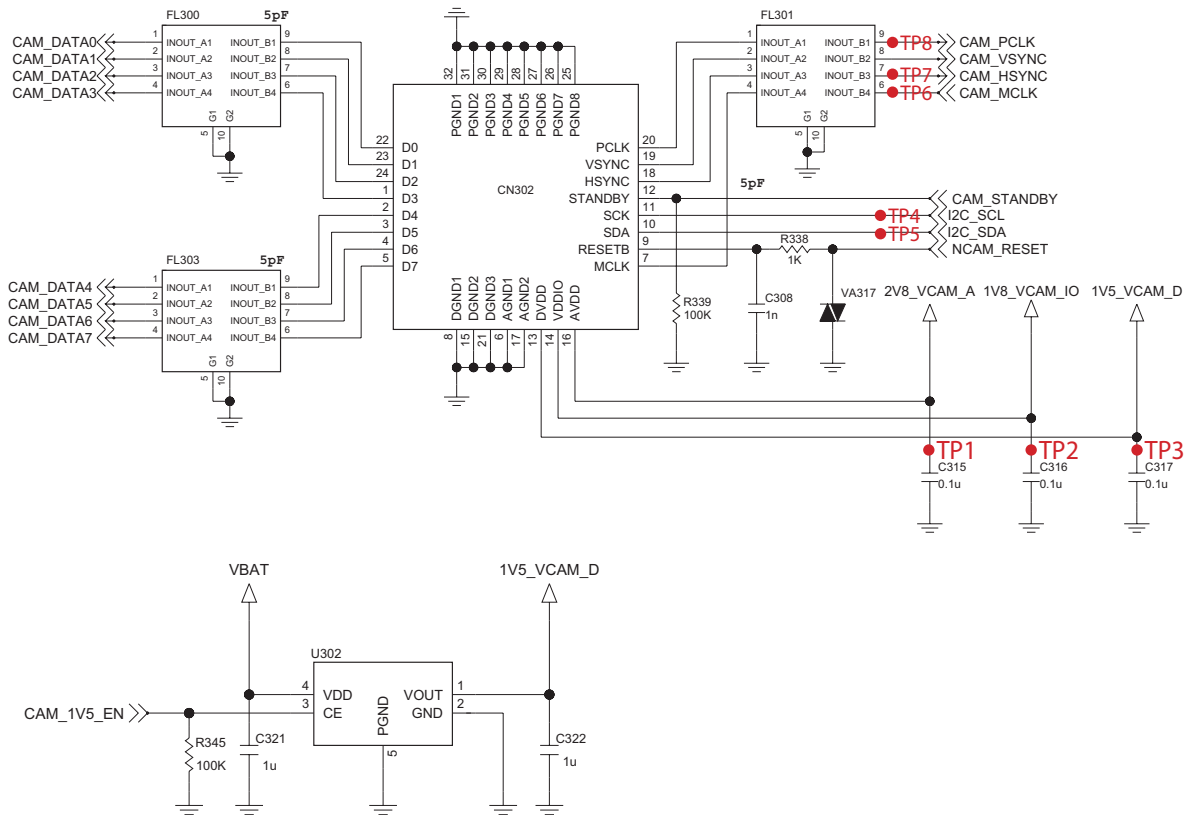


Figure 4.8.1

4. TROUBLE SHOOTING

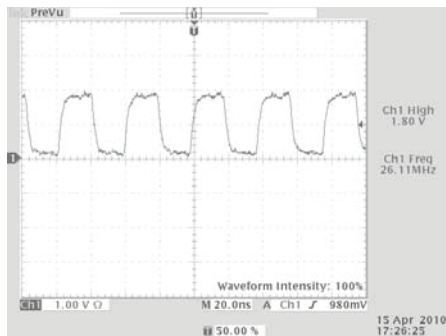
CIRCUIT



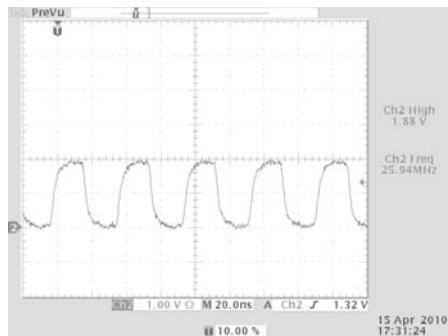
4. TROUBLE SHOOTING

Waveform

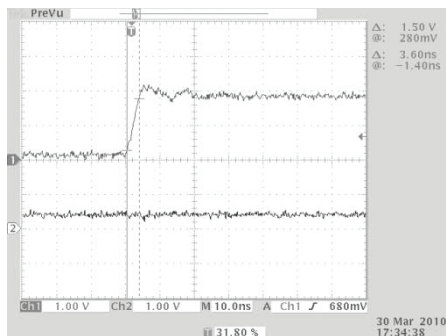
AC Characteristic



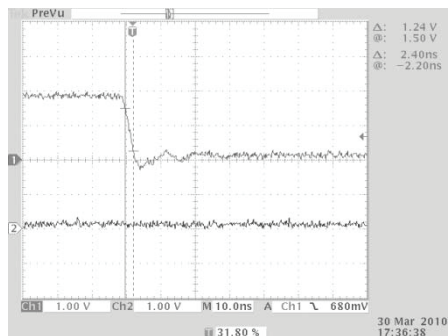
TP6→MCLK 26MHz



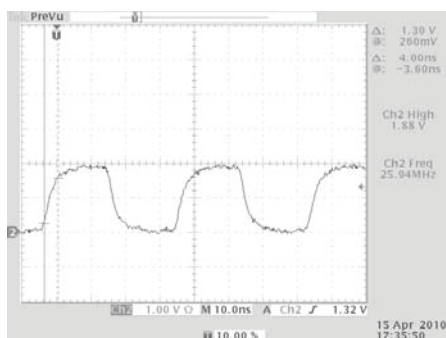
TP8→PCLK 26MHz



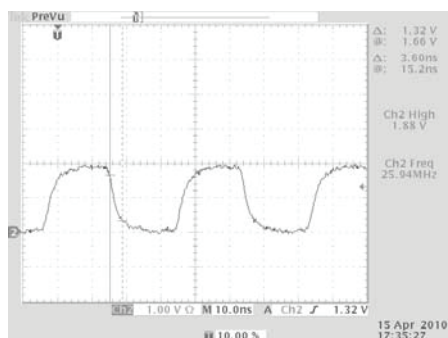
TP7→HSYNC rising time = 3.6ns



TP7→HSYNC falling time = 2.4ns

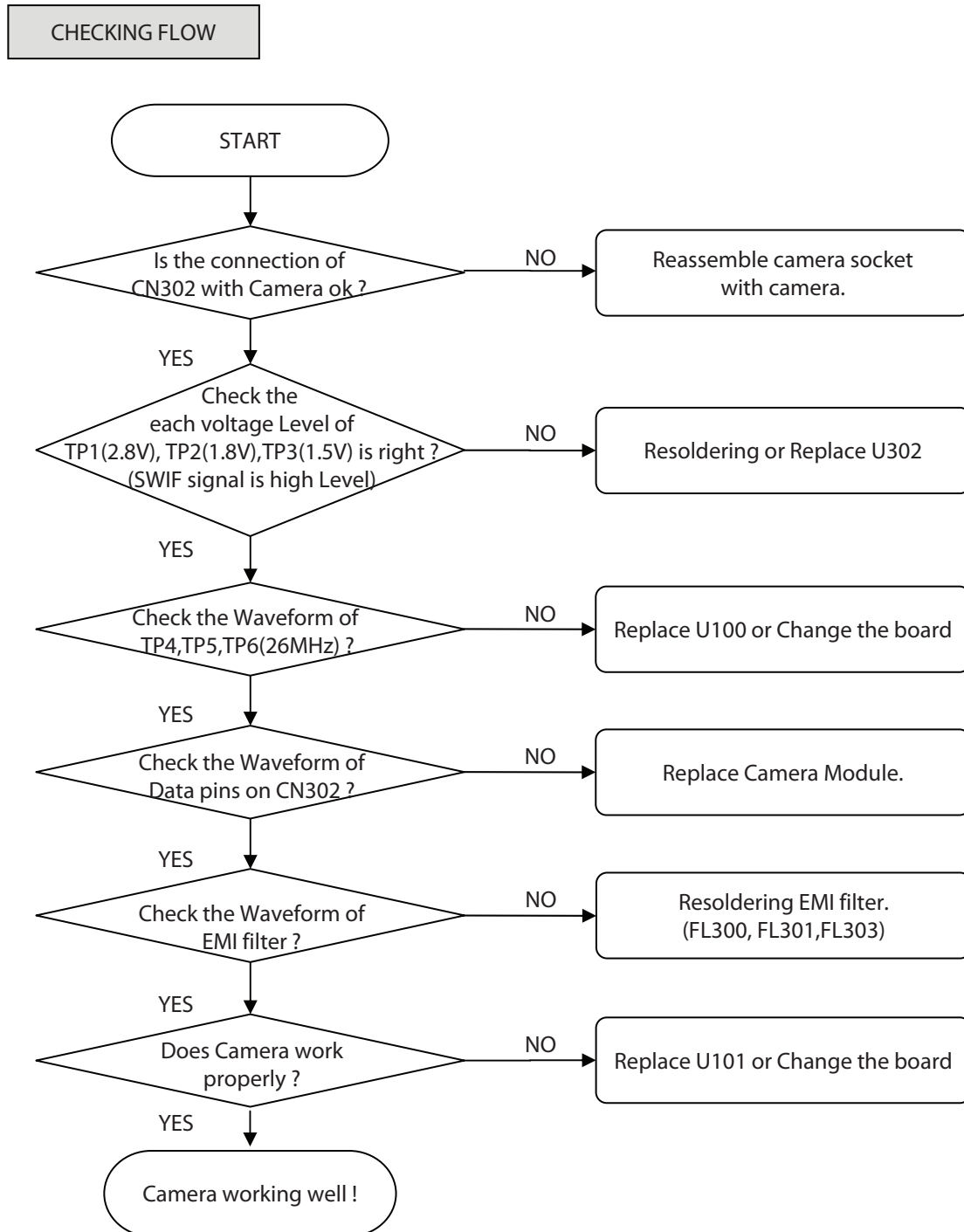


TP8→PCLK rising time = 3.6ns



TP8→PCLK falling time = 3.6ns

4. TROUBLE SHOOTING



4.9 Speaker Trouble

TEST POINT

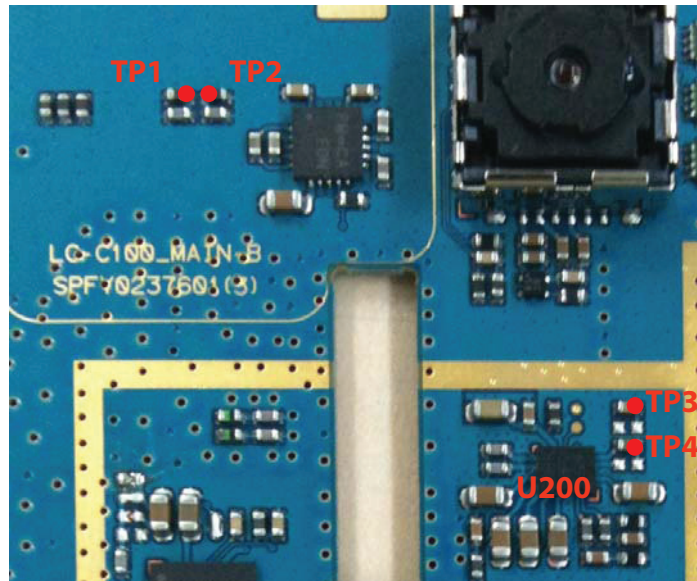
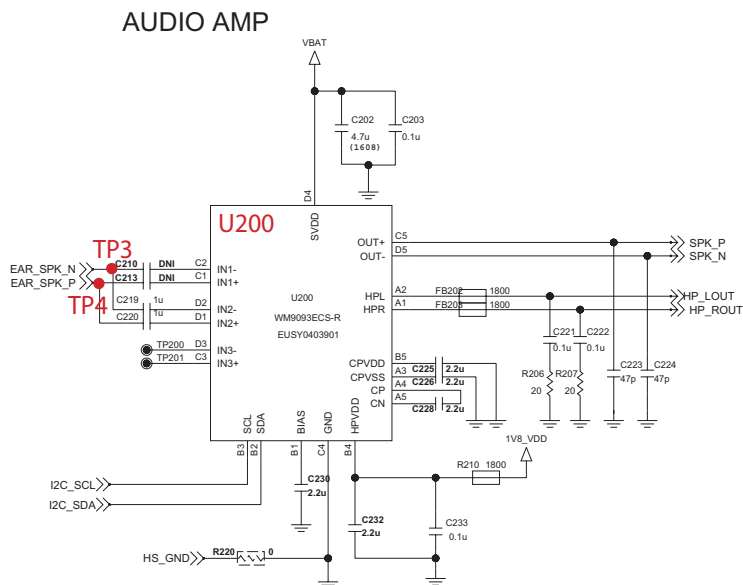
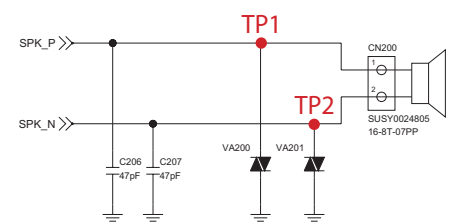


Figure 4.9

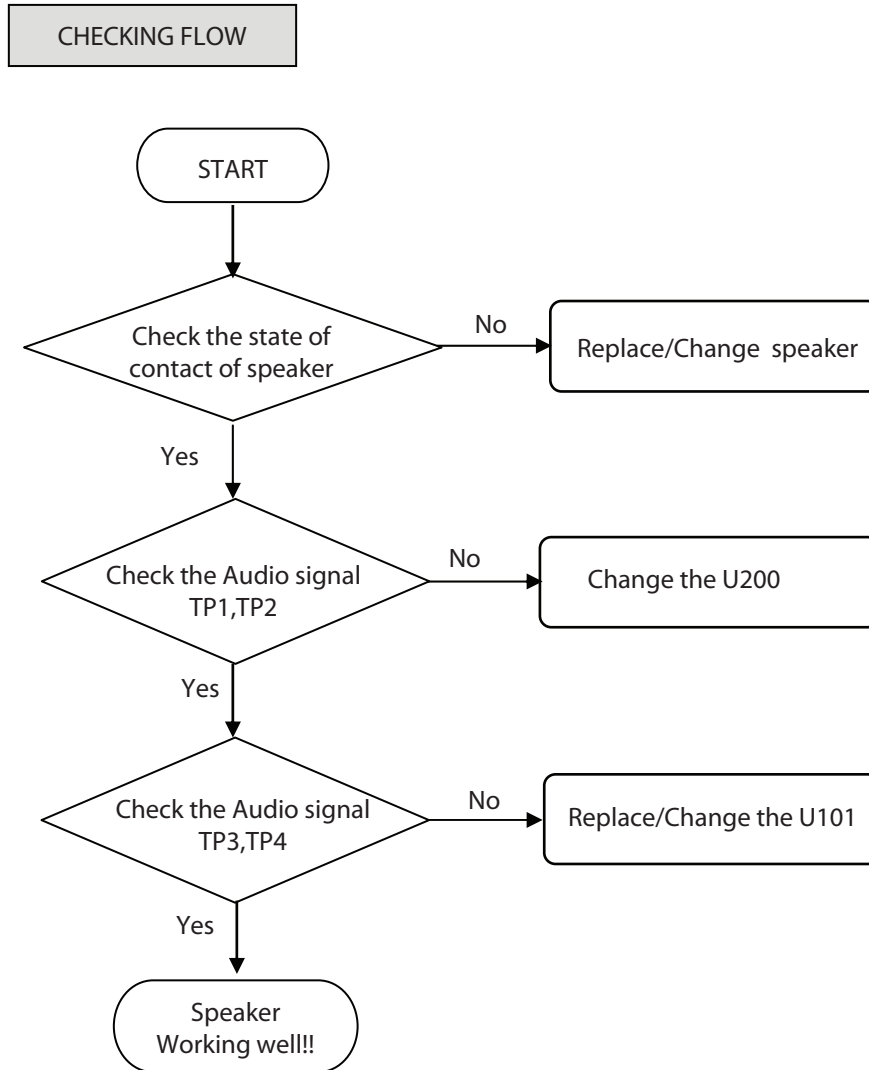
CIRCUIT



LOUD SPEAKER



4. TROUBLE SHOOTING



4.10 Earphone Trouble

TEST POINT

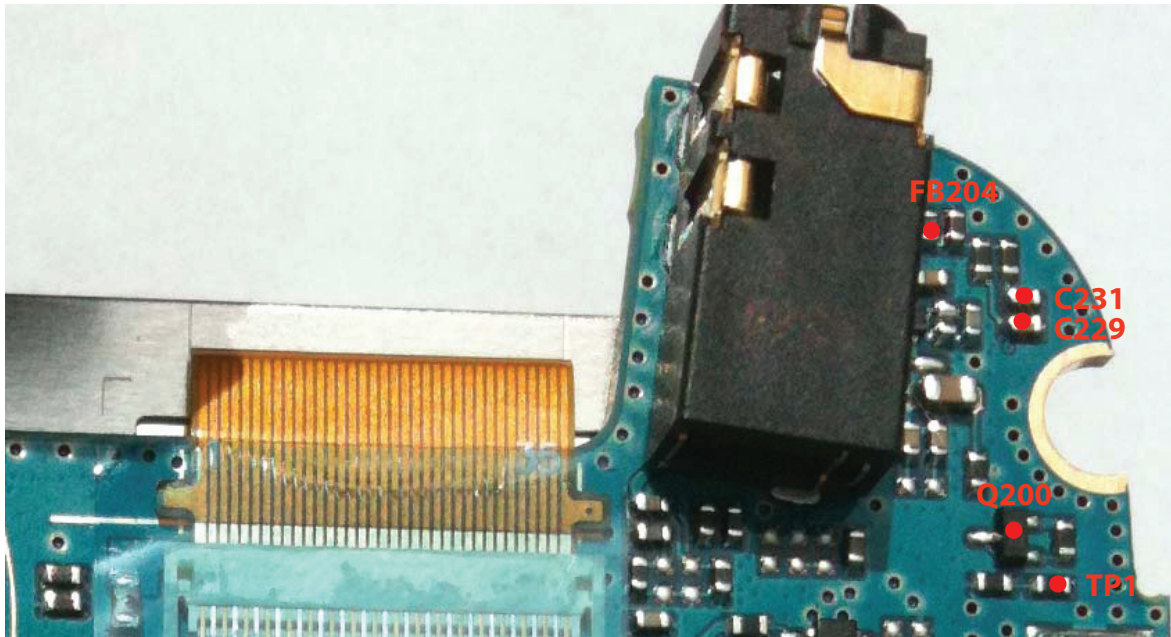


Figure 4.10

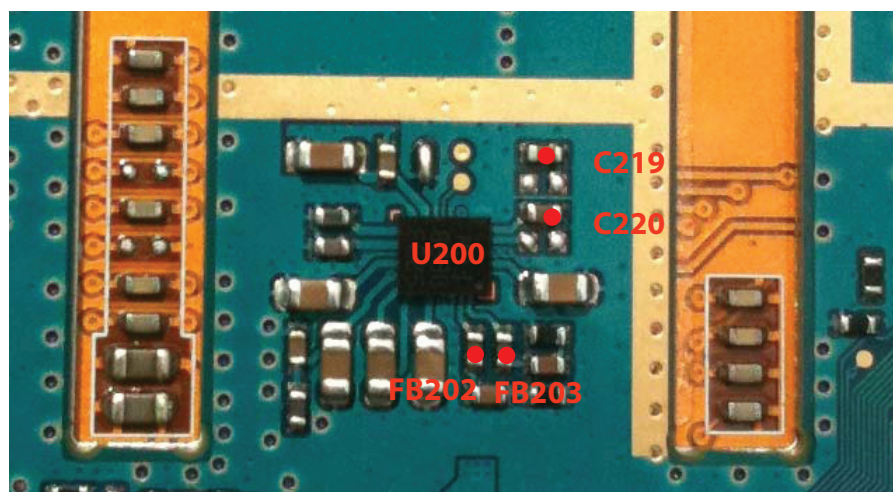
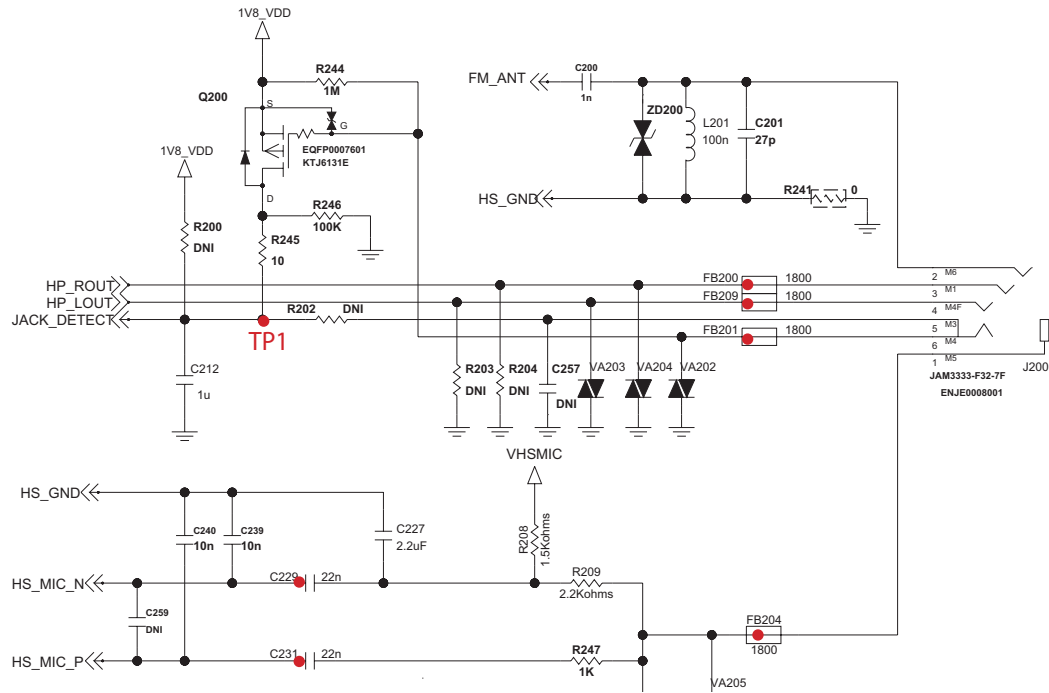


Figure 4.10.1

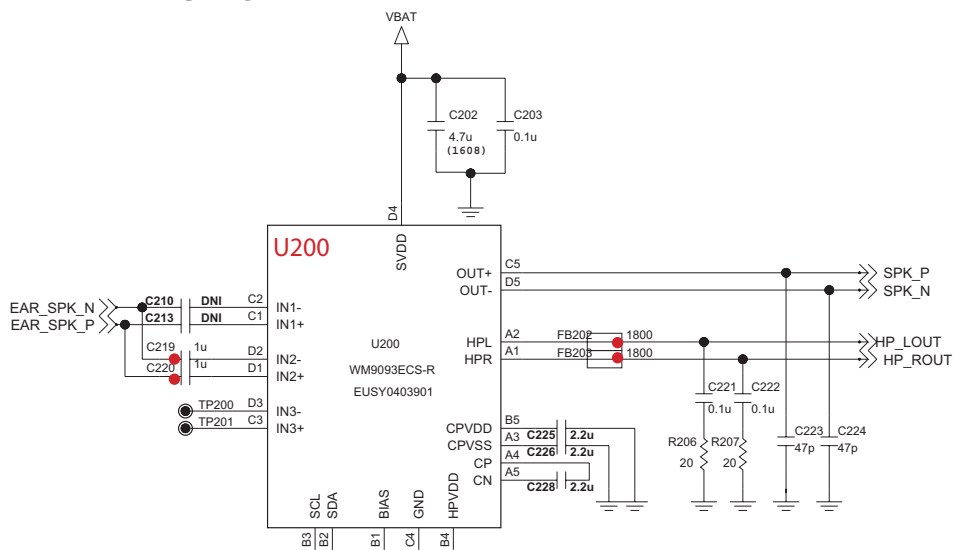
4. TROUBLE SHOOTING

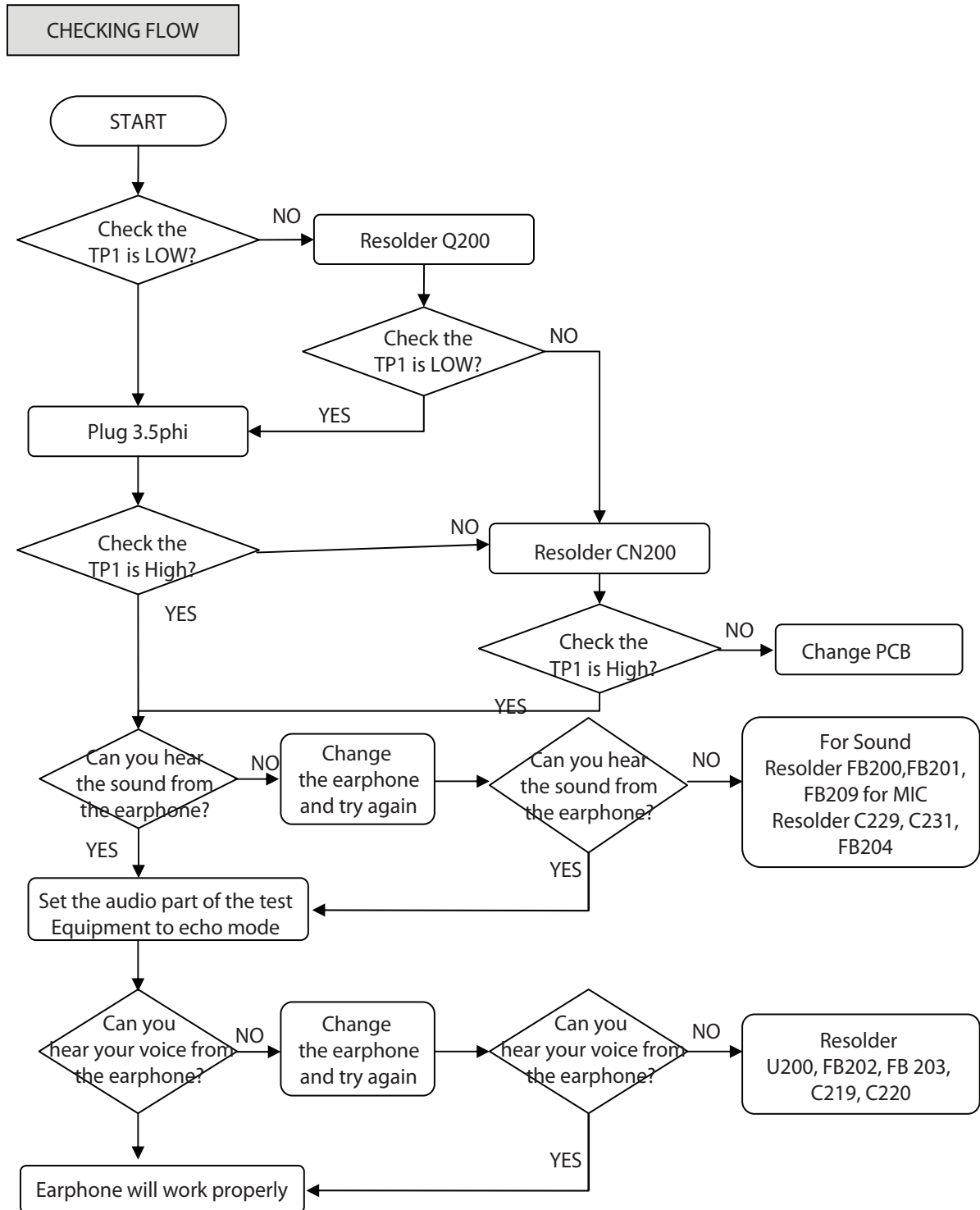
CIRCUIT

3.5phi JACK



AUDIO AMP





4. TROUBLE SHOOTING

4.11 Receiver Trouble

TEST POINT

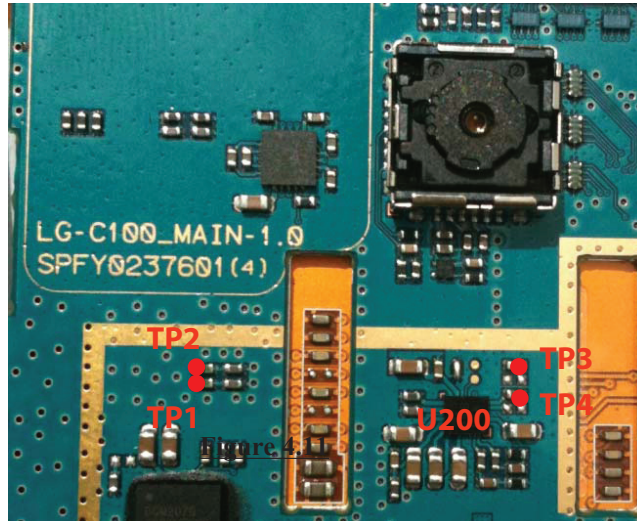
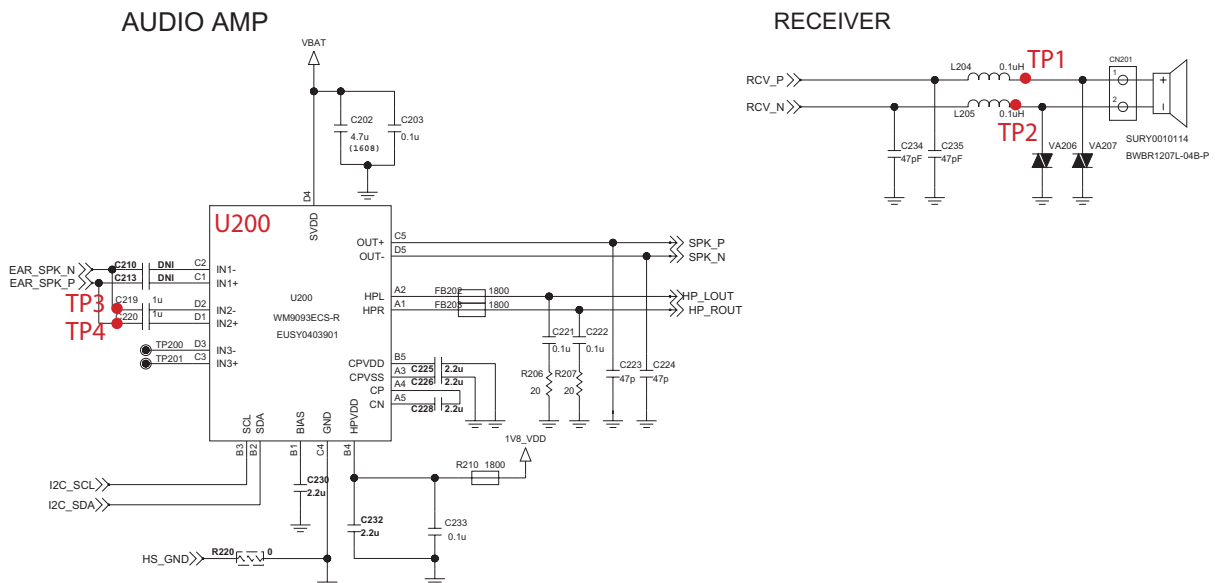


Figure 4.11

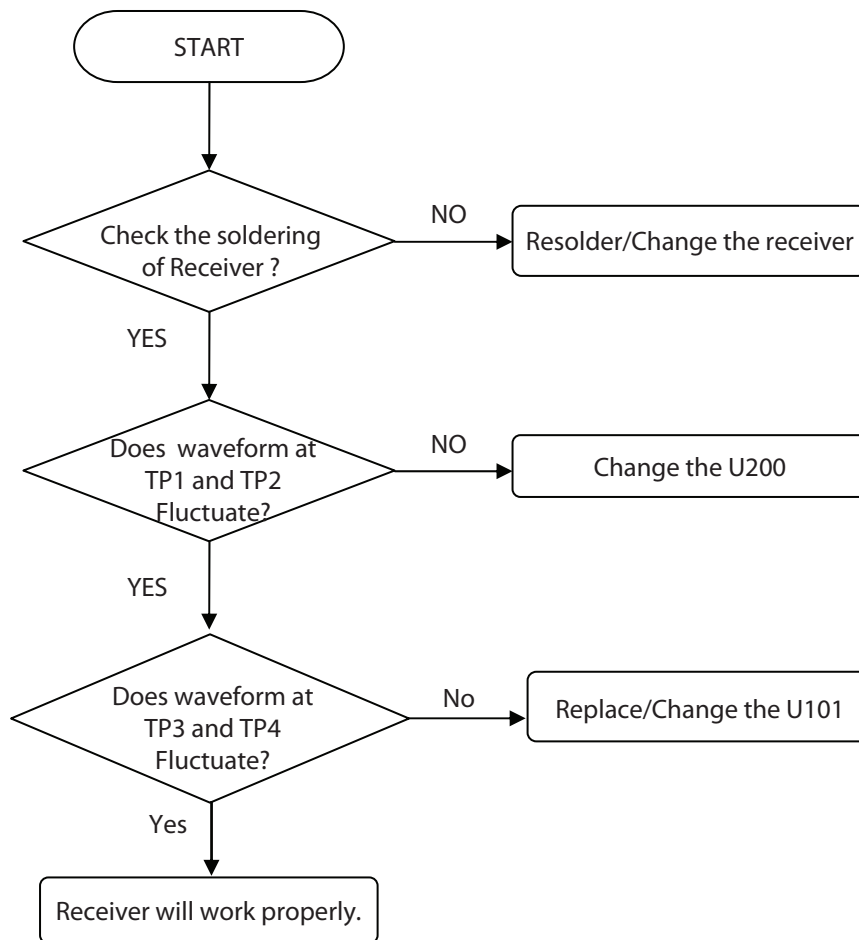
CIRCUIT



4. TROUBLE SHOOTING

CHECKING FLOW

SETTING : After initialize Agilent 8960, Test EGSM900, DCS mode (or GSM850, PCS mode)
Set the property of audio as PRBS or continuous wave. Set the receiving volume of mobile as Max.



4. TROUBLE SHOOTING

4.12 Microphone Trouble

TEST POINT

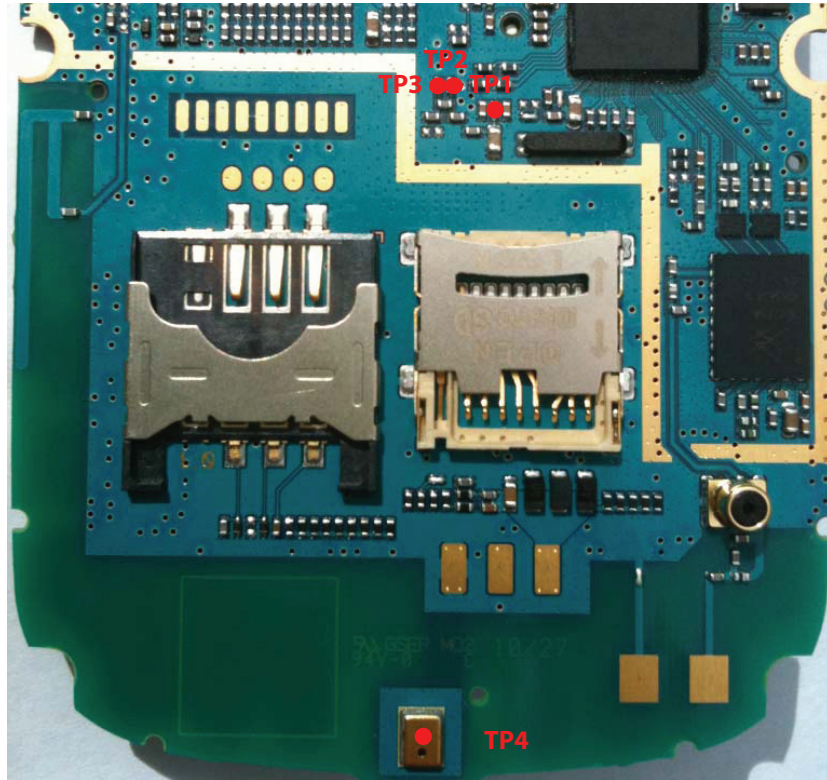
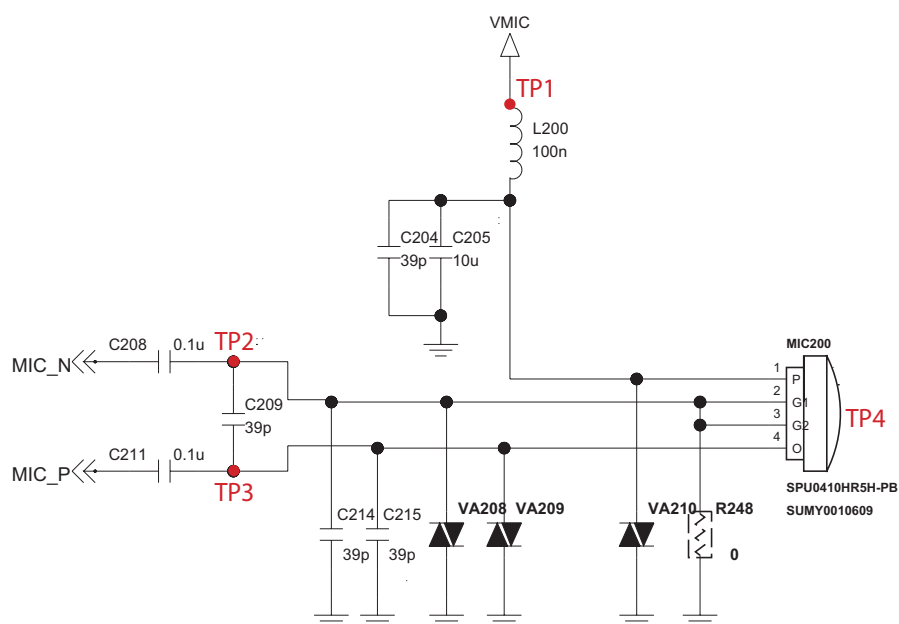


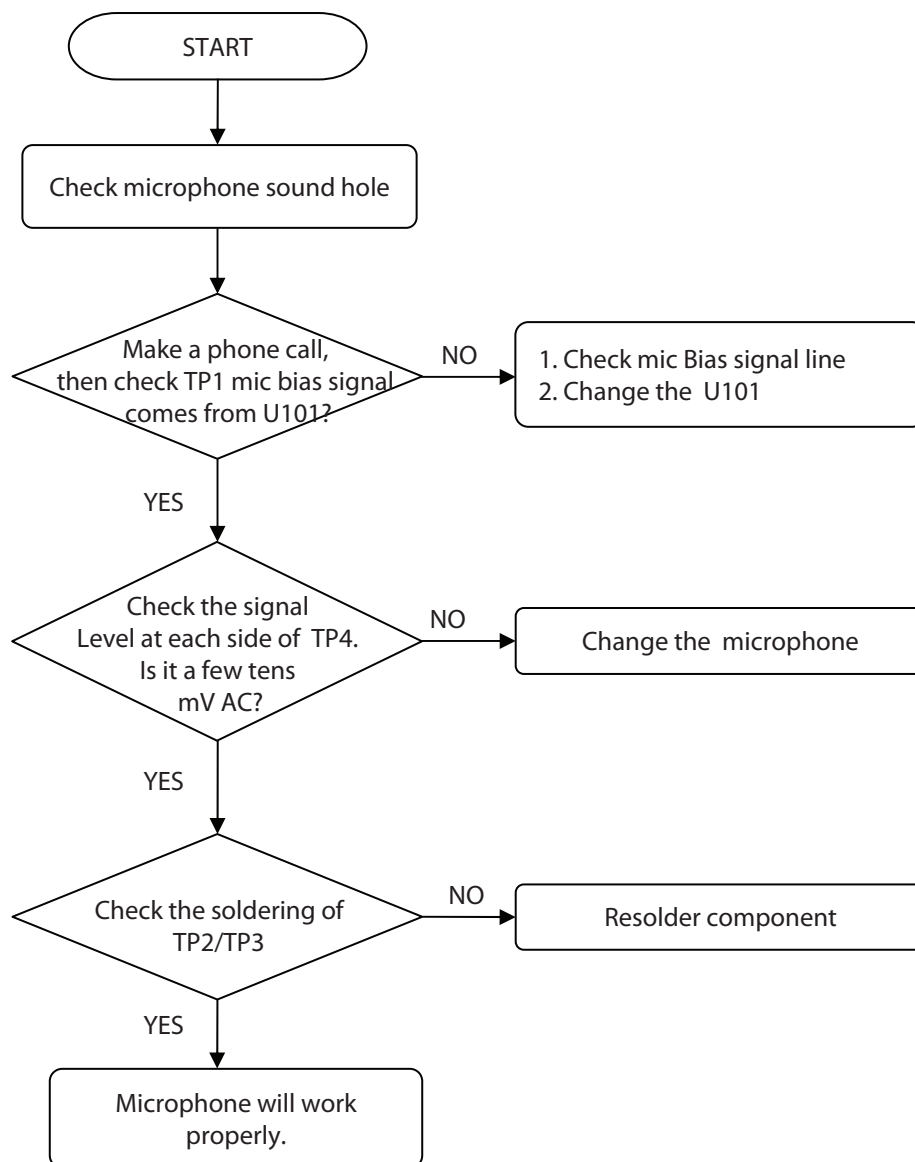
Figure 4.12

CIRCUIT



CHECKING FLOW

SETTING : After initialize Agilent 8960, Test EGSM900, DCS mode (or GSM850, PCS mode)



4. TROUBLE SHOOTING

4.13 SIM Card Interface Trouble

TEST POINT

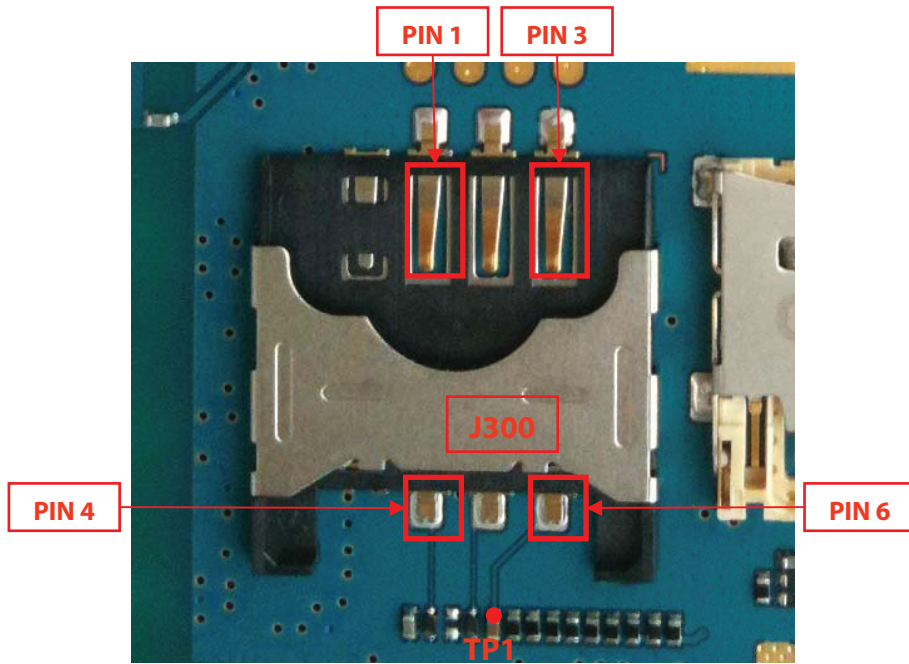
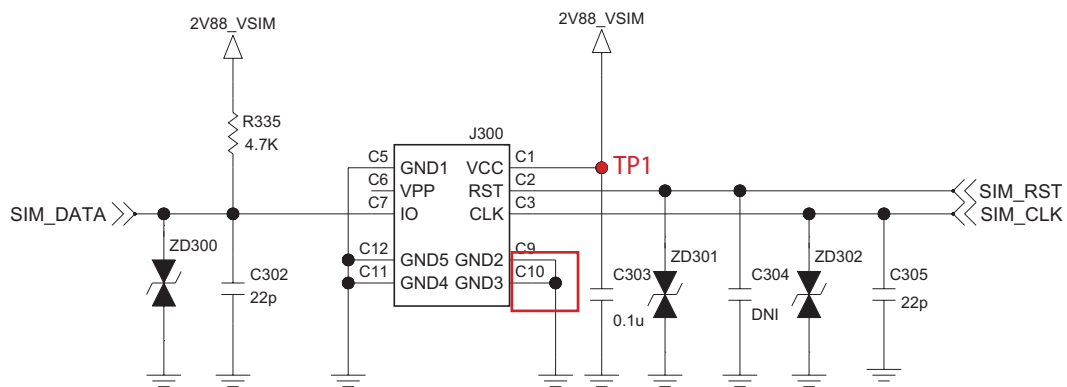


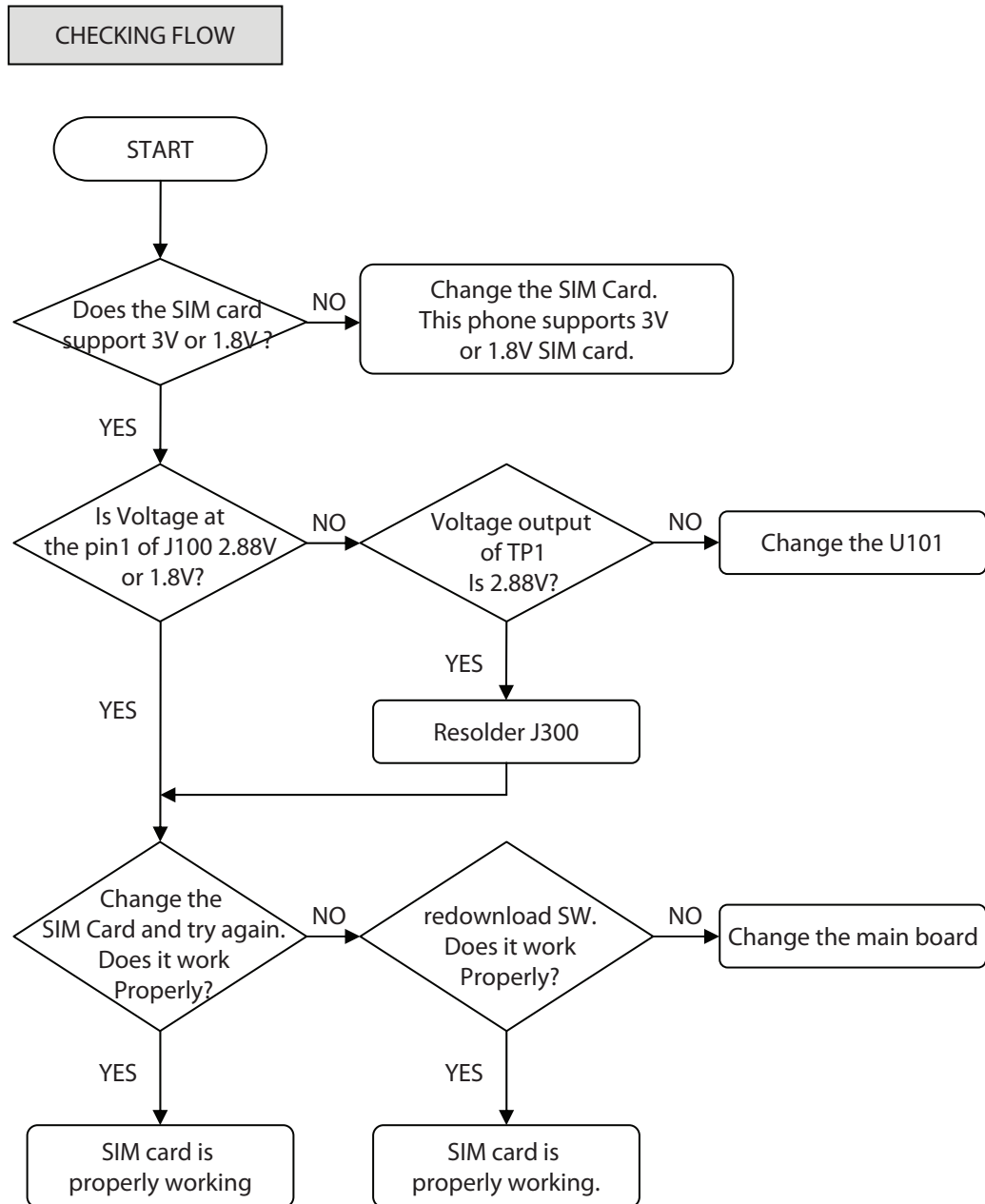
Figure 4.13

CIRCUIT

SIM_SOCKET



These are added for CMCC ESD test



4. TROUBLE SHOOTING

4.14 KEY backlight Trouble

TEST POINT

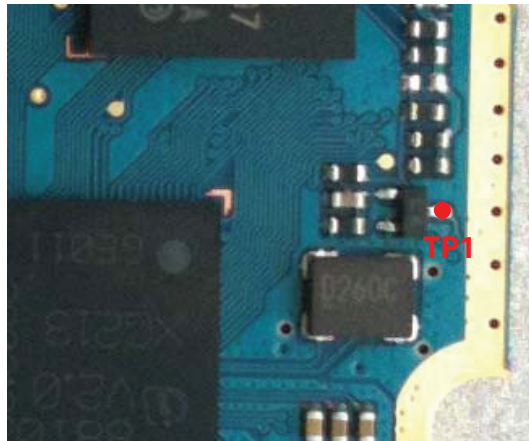


Figure 4.14

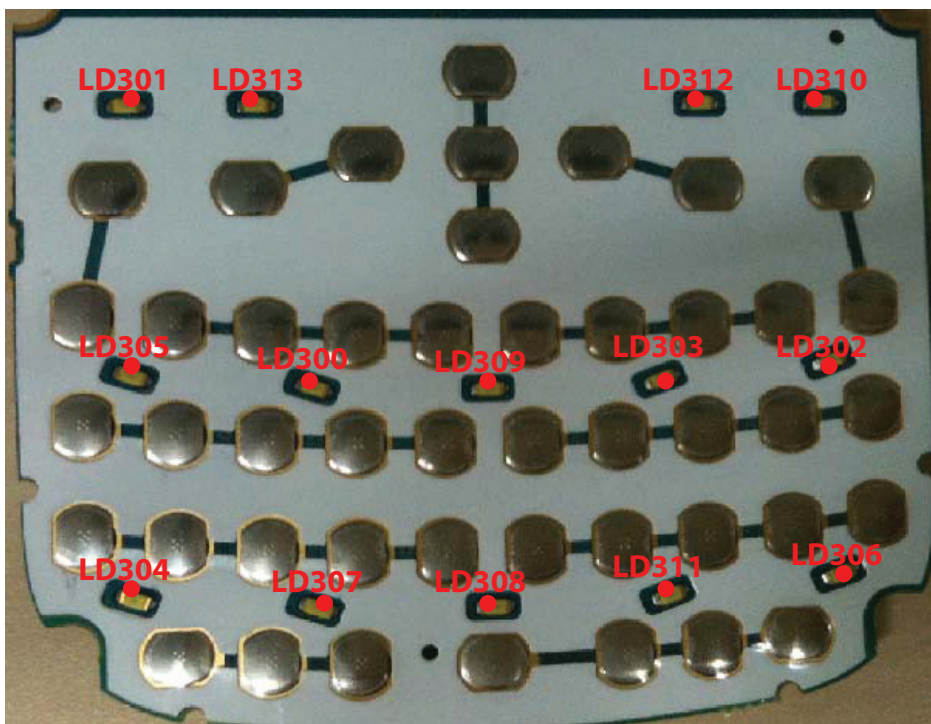
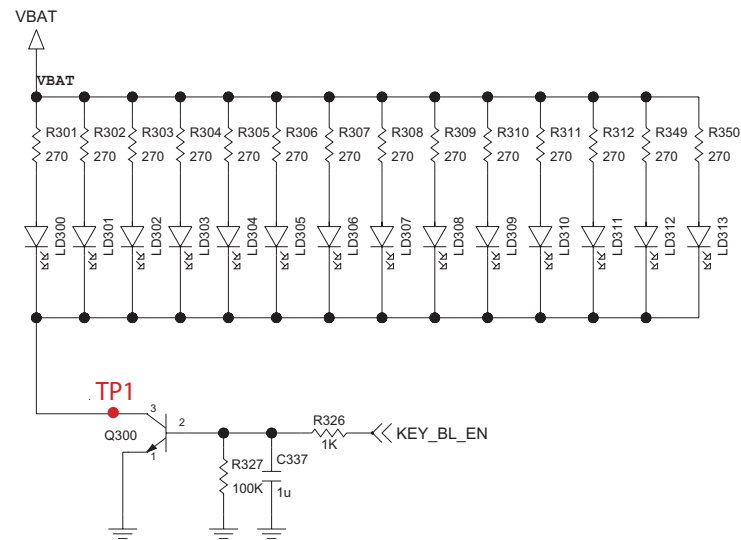
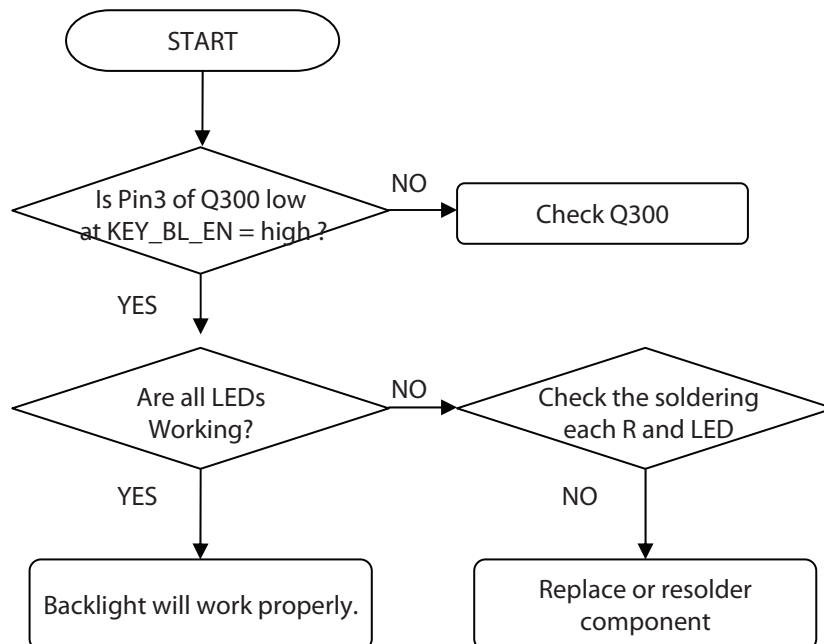


Figure 4.14.1

CIRCUIT



CHECKING FLOW



4. TROUBLE SHOOTING

4.15 Micro SD (uSD) Trouble

TEST POINT

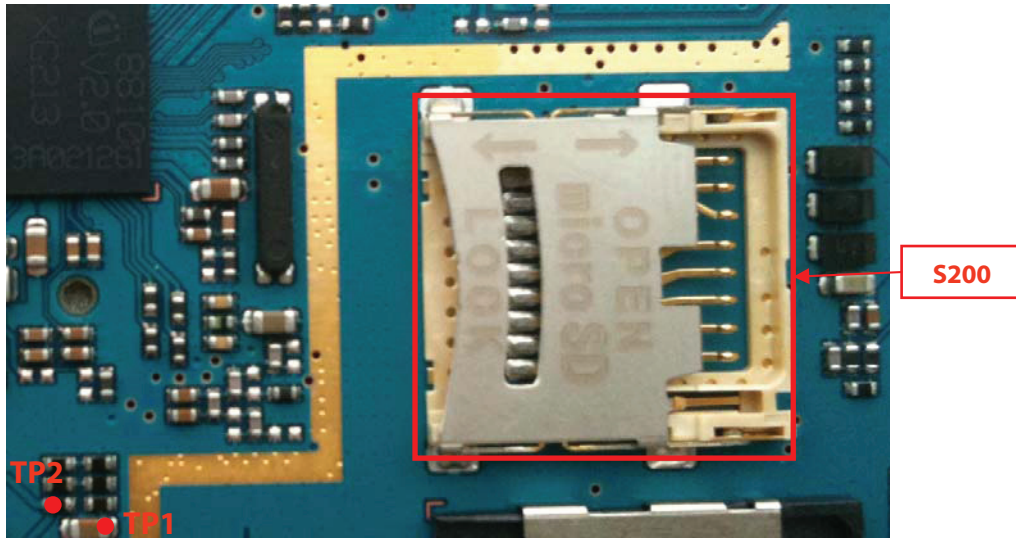
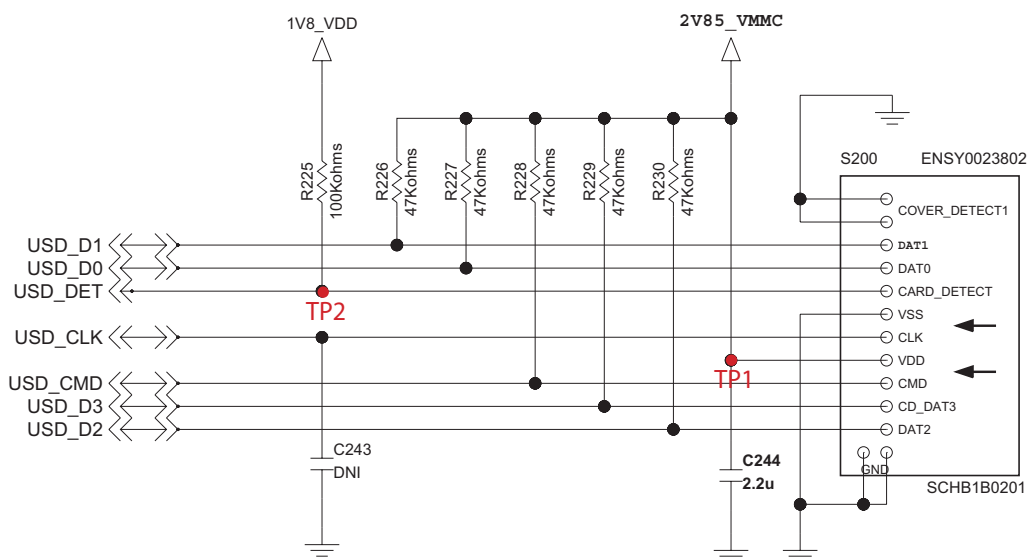
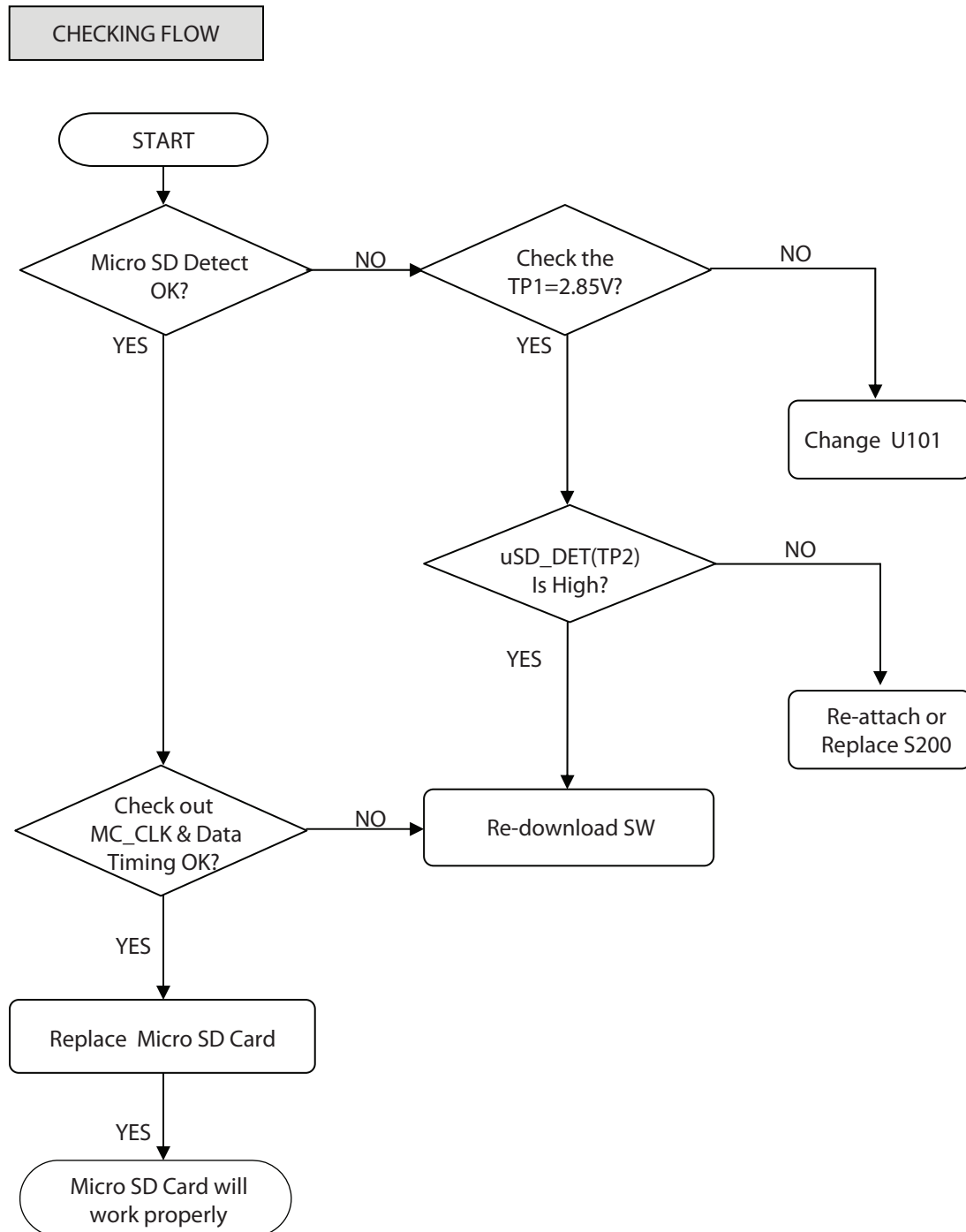


Figure 4.15

CIRCUIT

MICRO SD SOCKET





4. TROUBLE SHOOTING

4.16 Bluetooth Trouble

TEST POINT

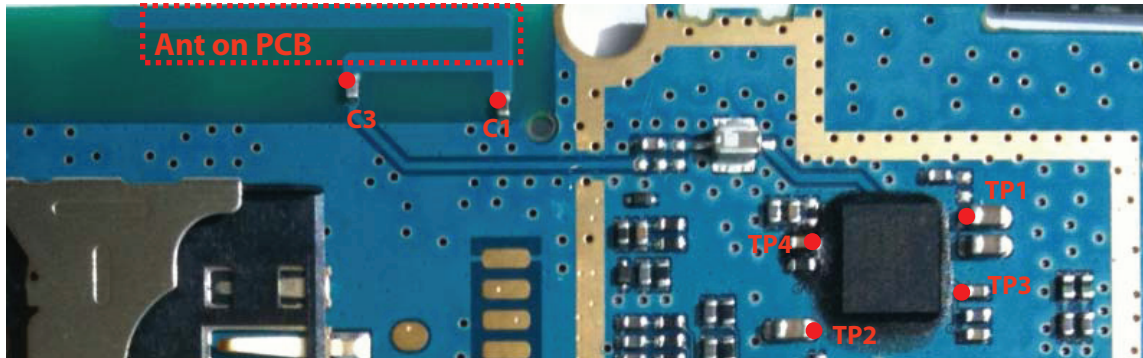
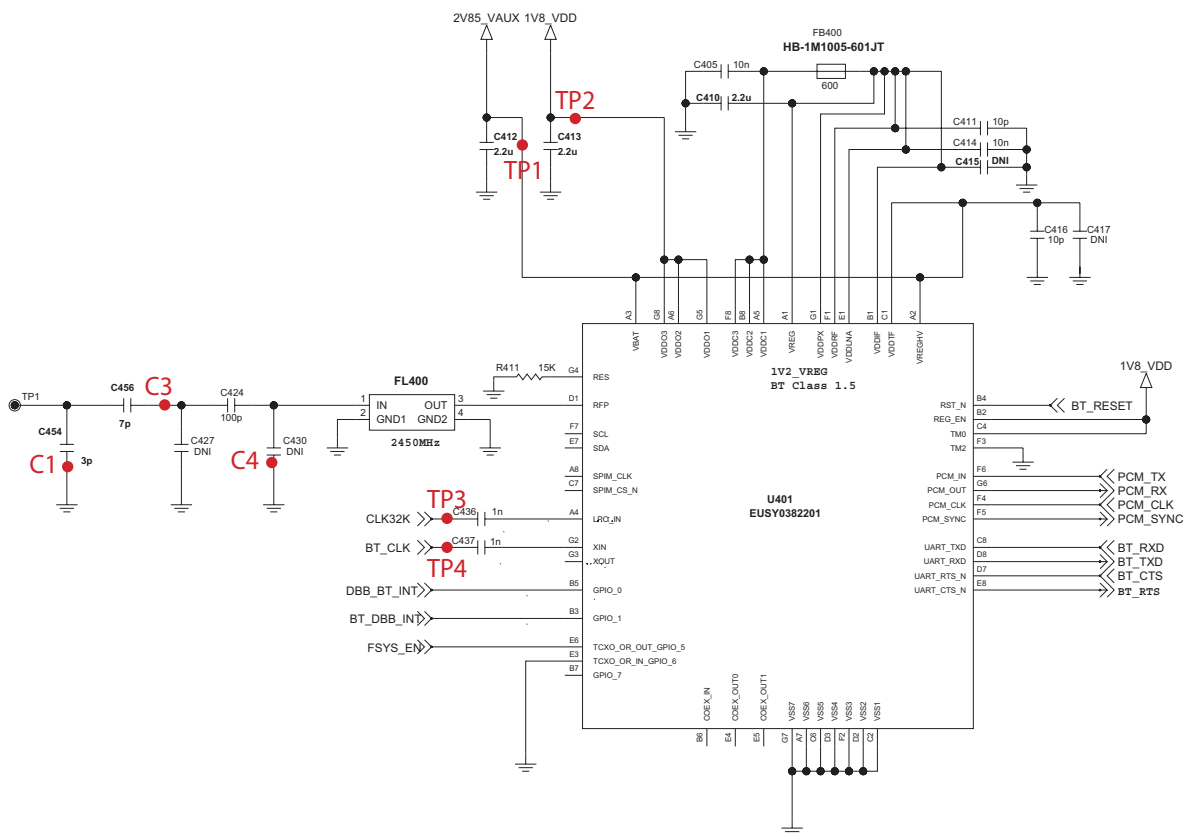
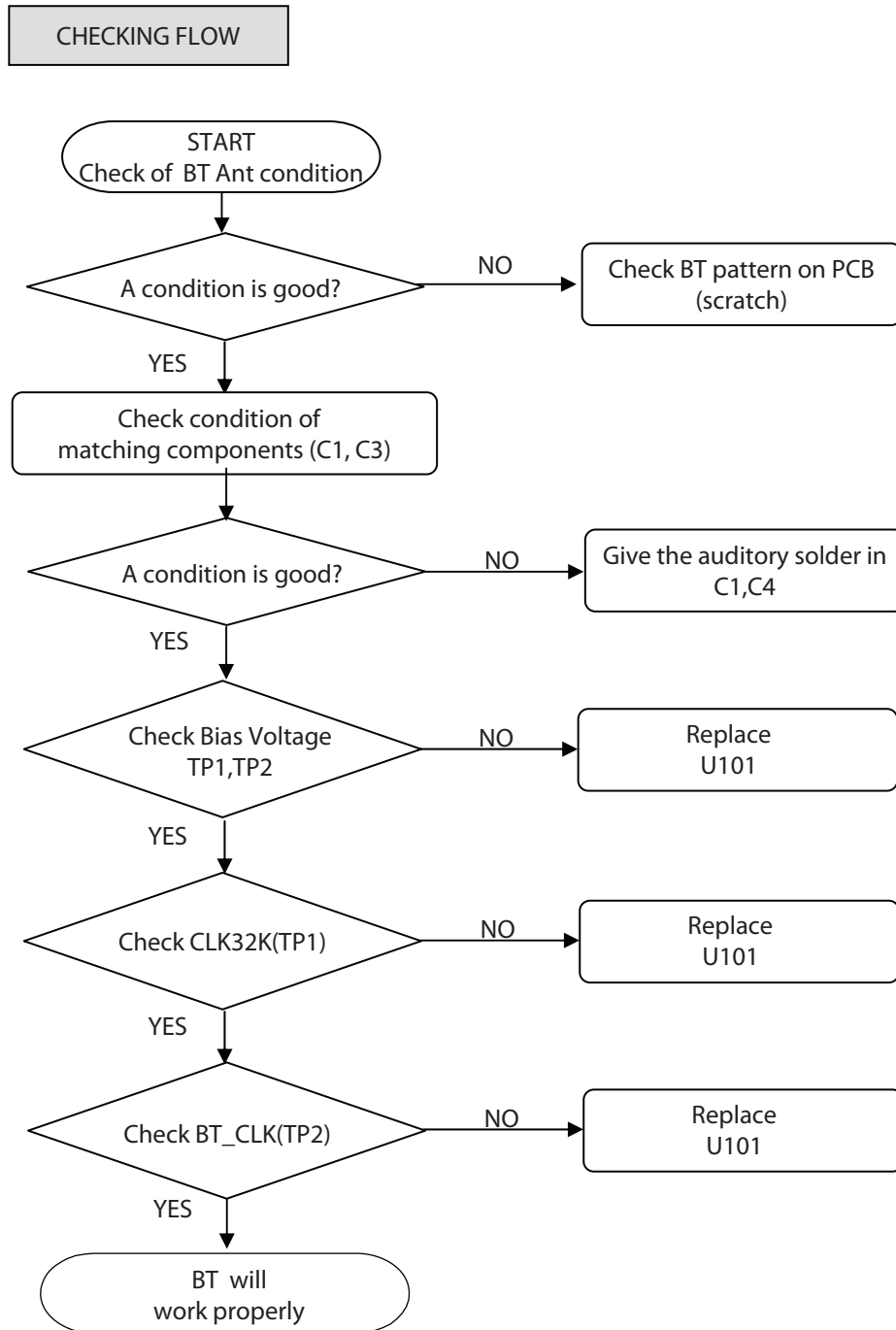


Figure 4.16

CIRCUIT





4. TROUBLE SHOOTING

4.17 FM Radio Trouble

TEST POINT

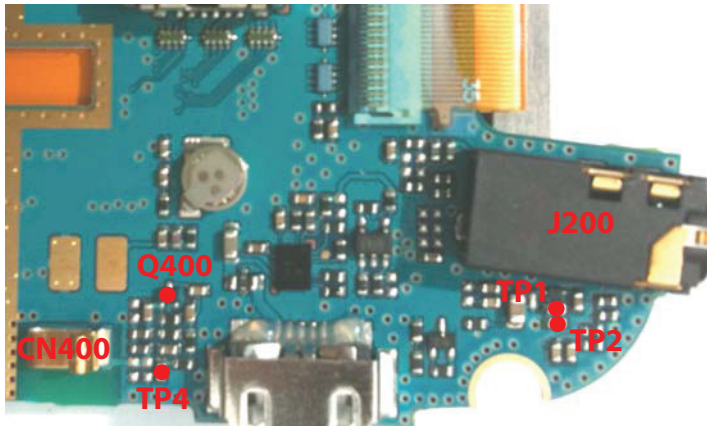


Figure 4.17

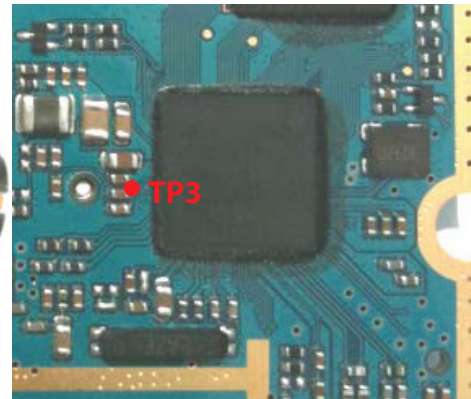
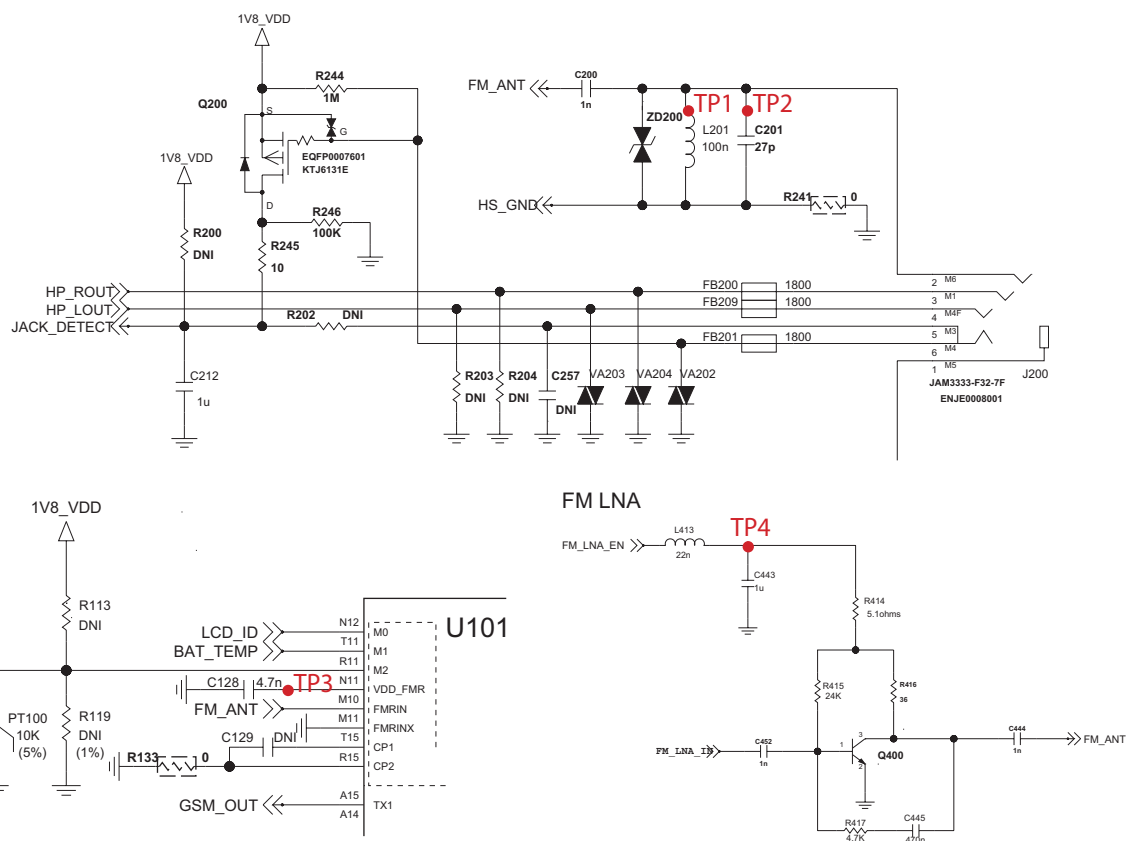
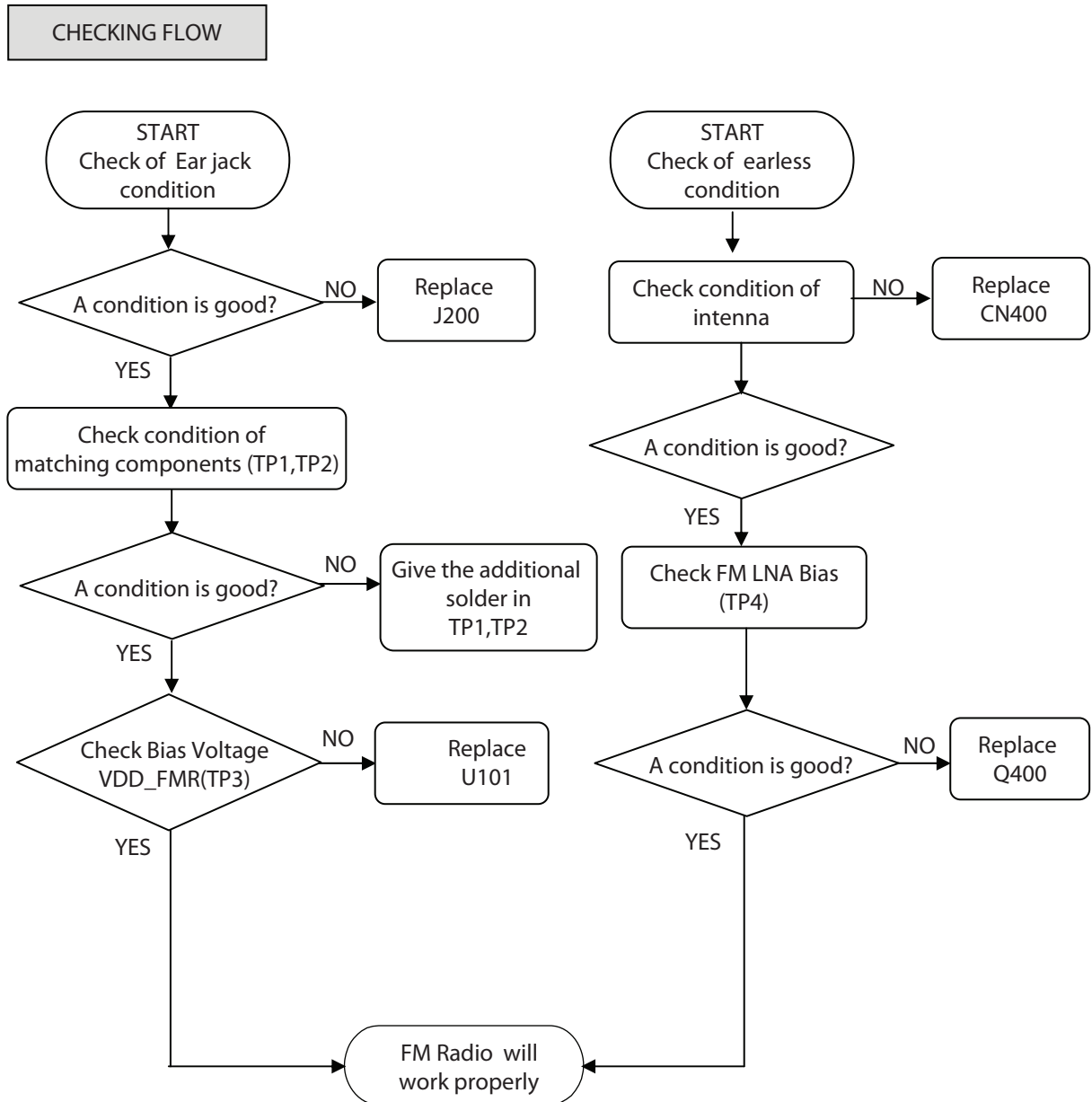


Figure 4.17.1

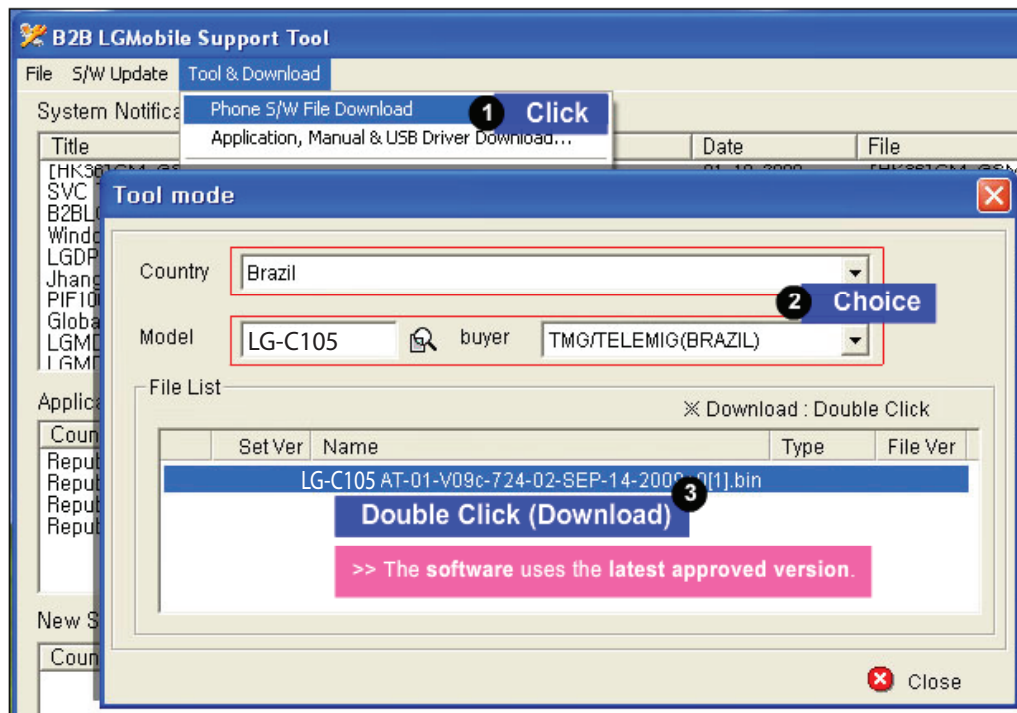
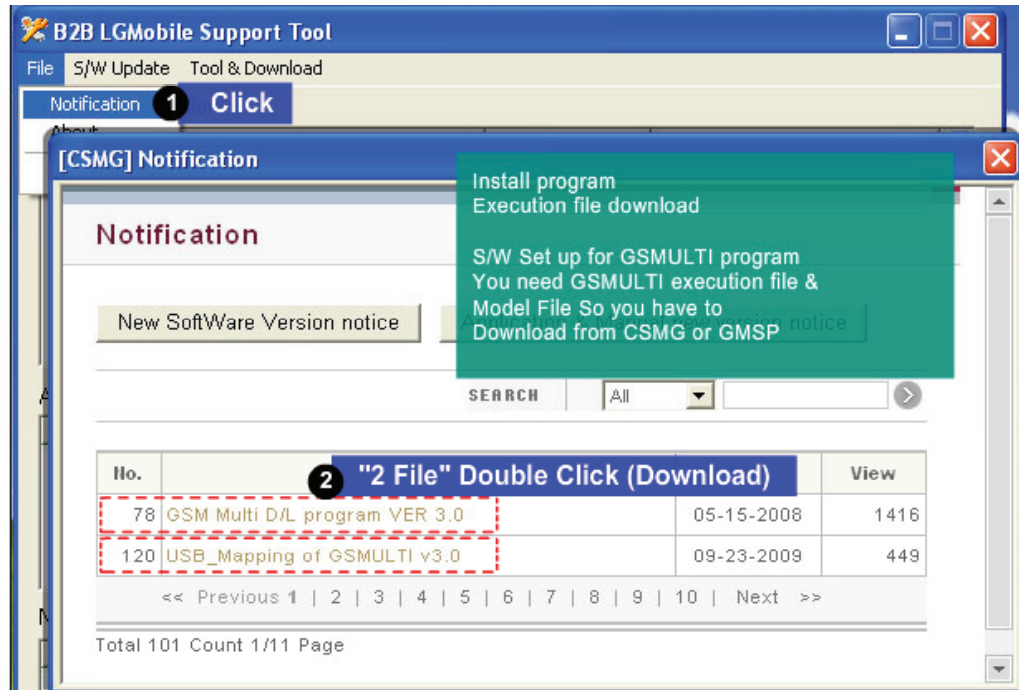
CIRCUIT



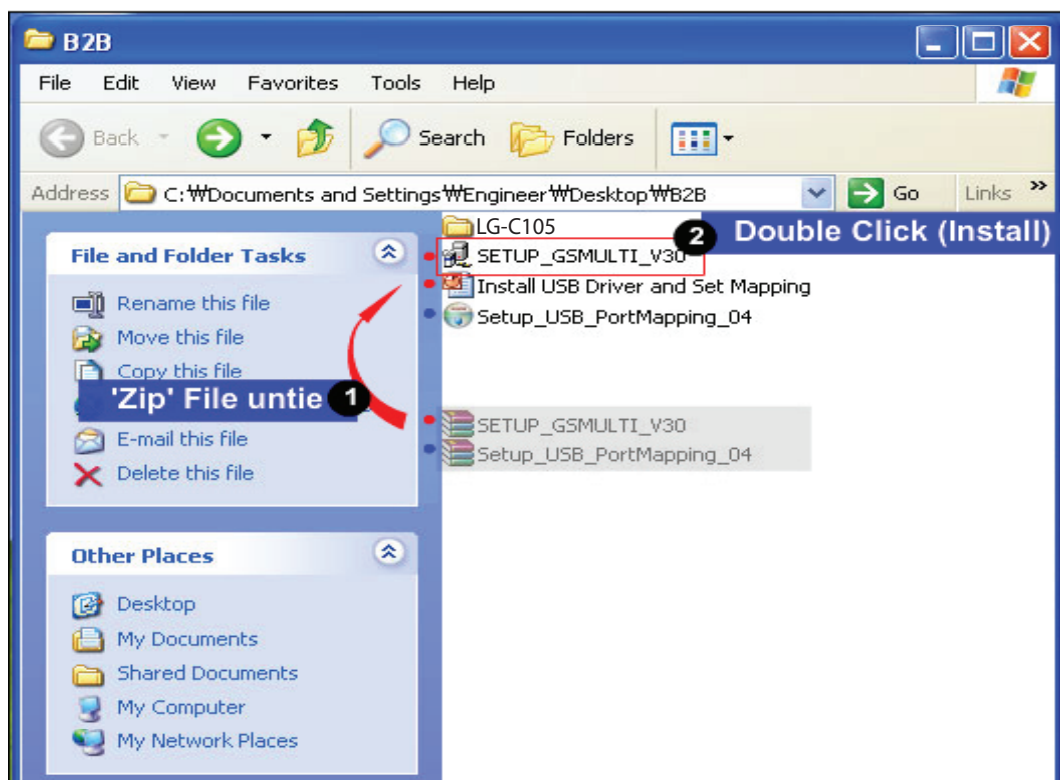
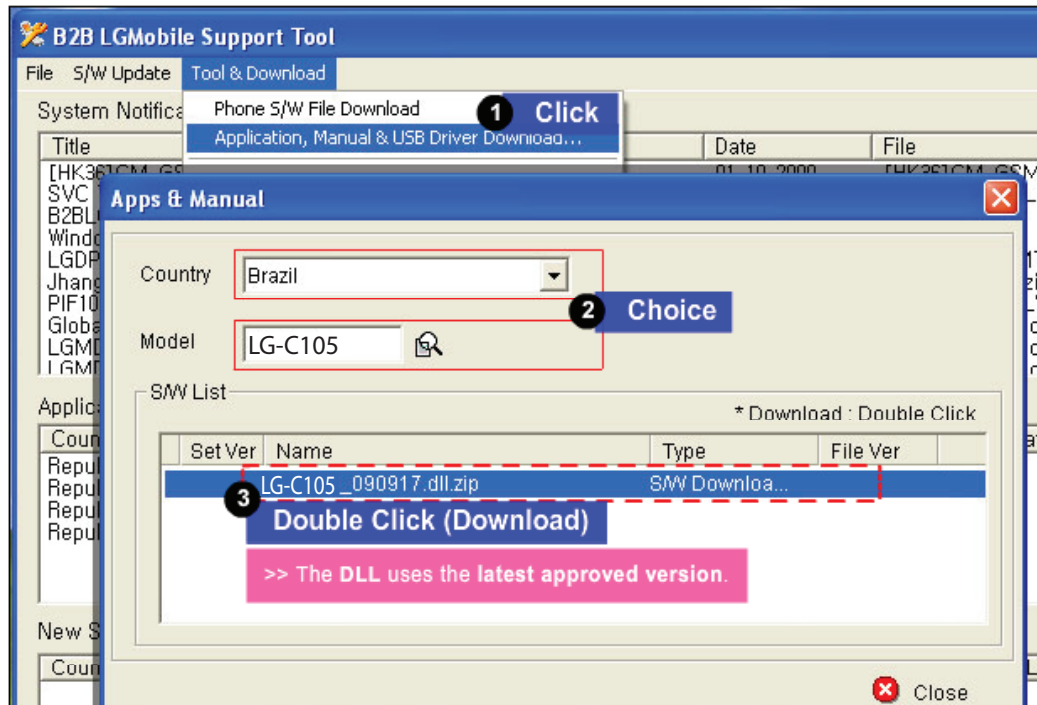


5. DOWNLOAD

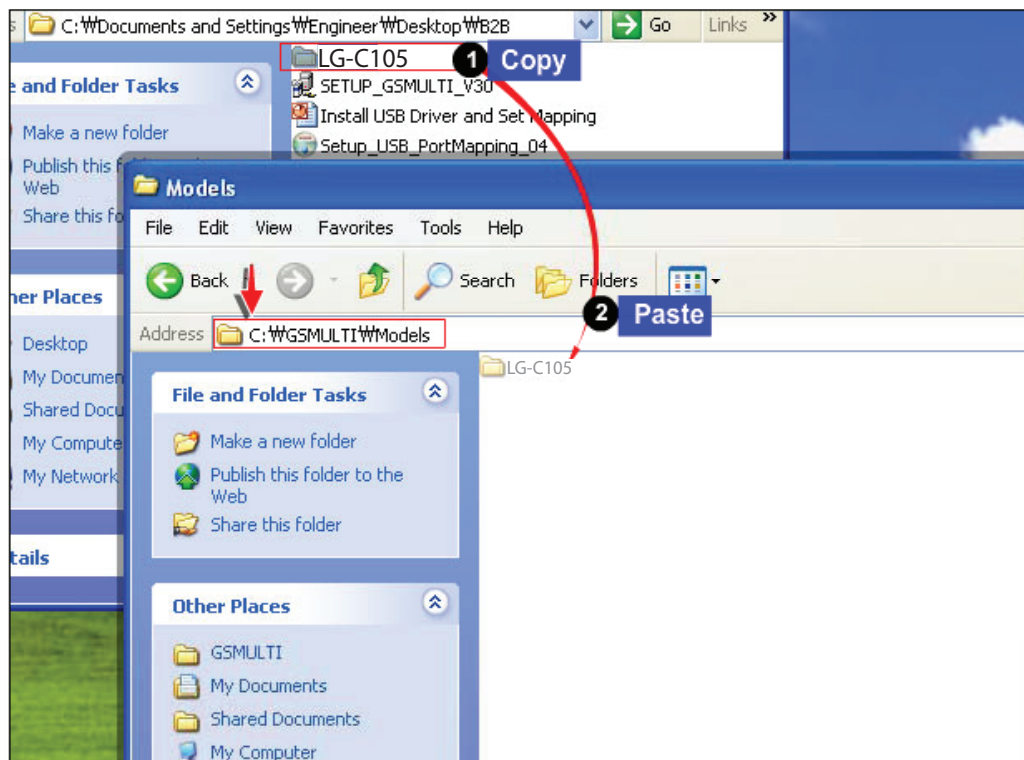
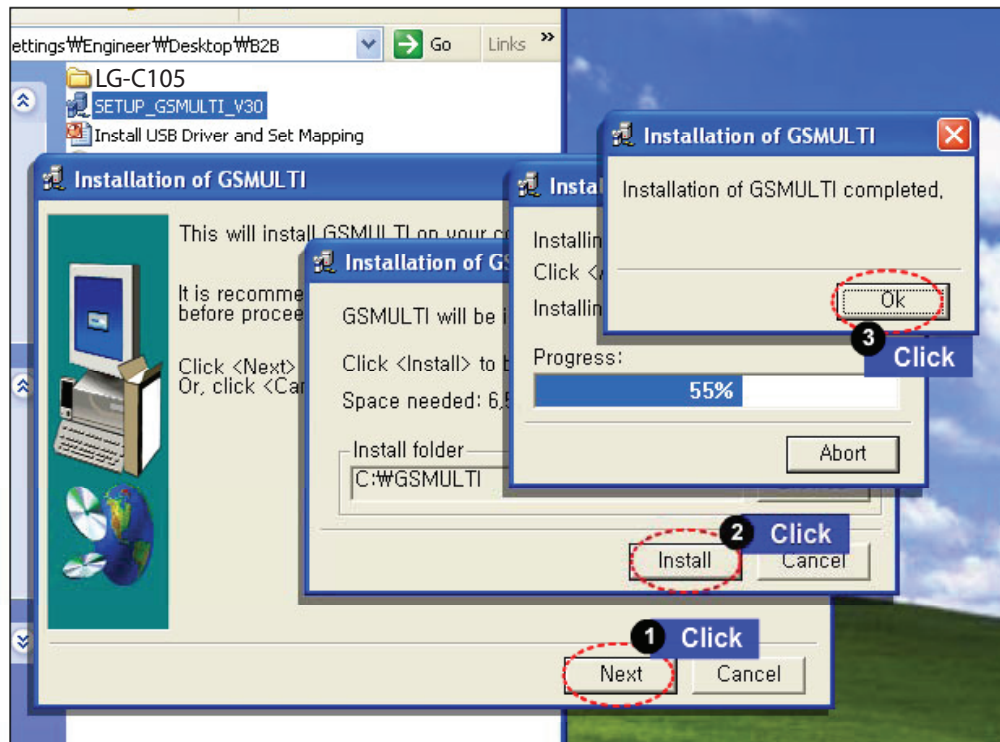
5. DOWNLOAD



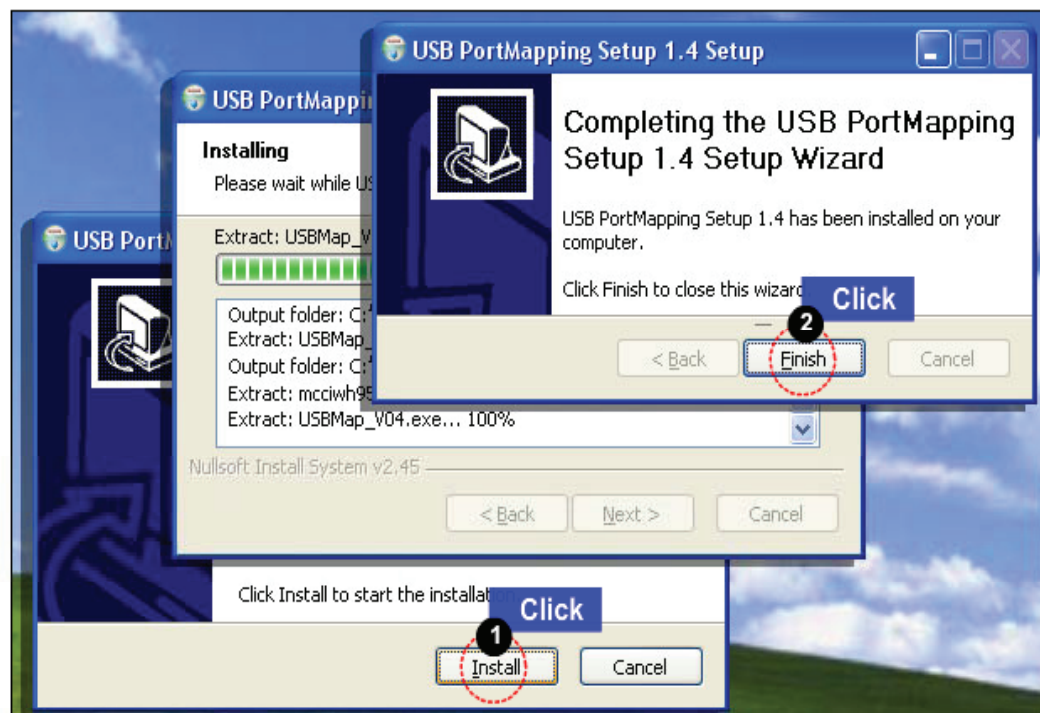
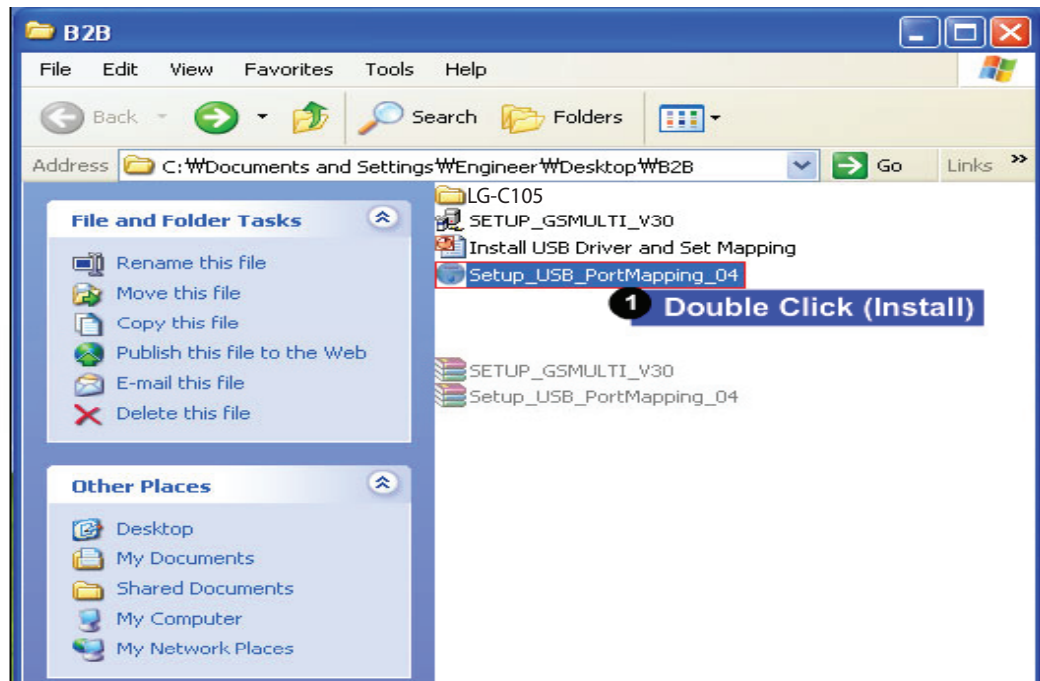
5. DOWNLOAD



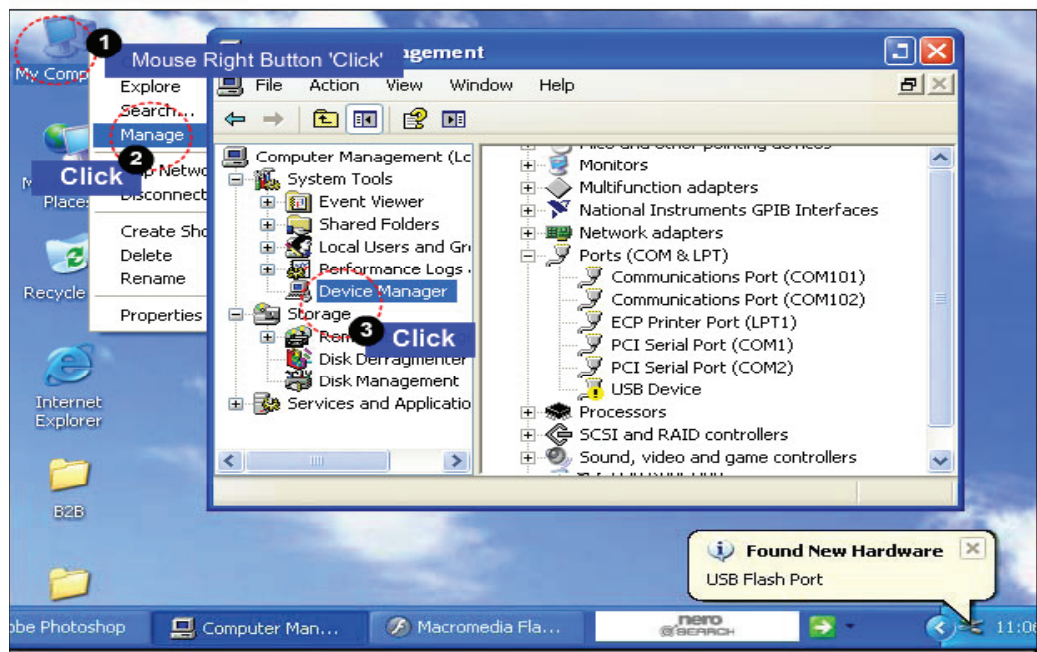
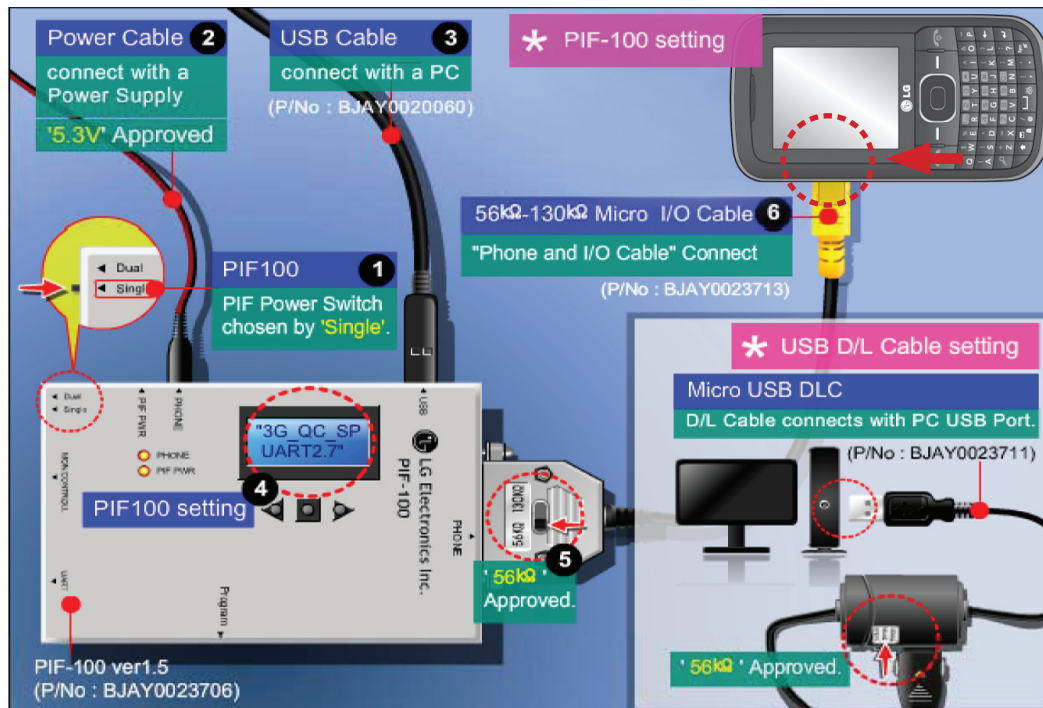
5. DOWNLOAD

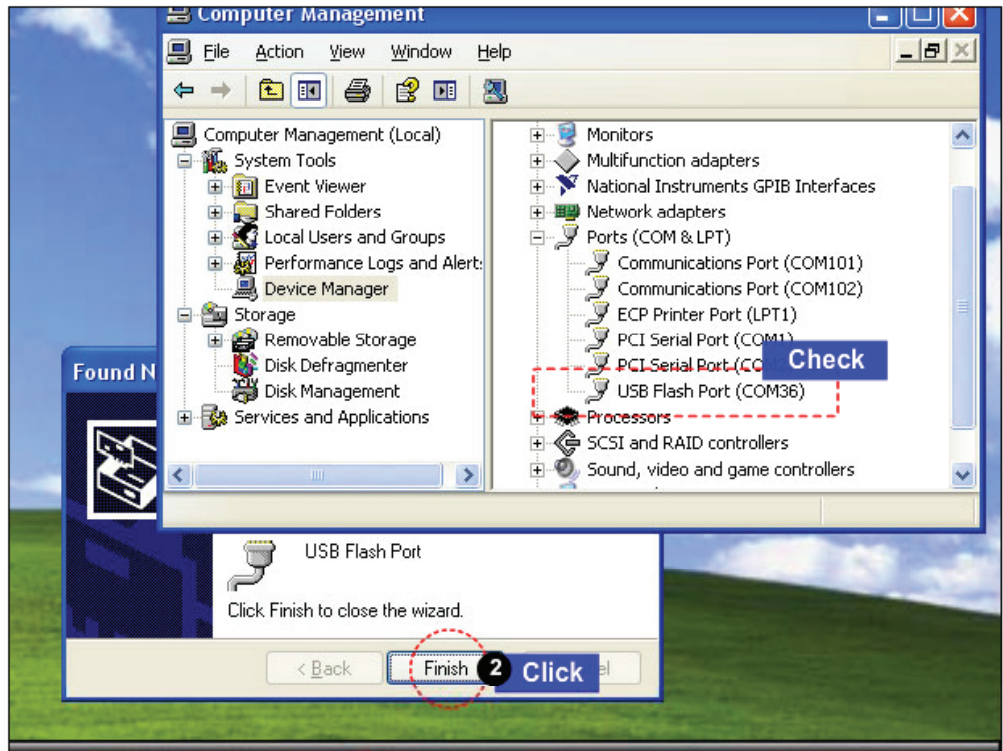
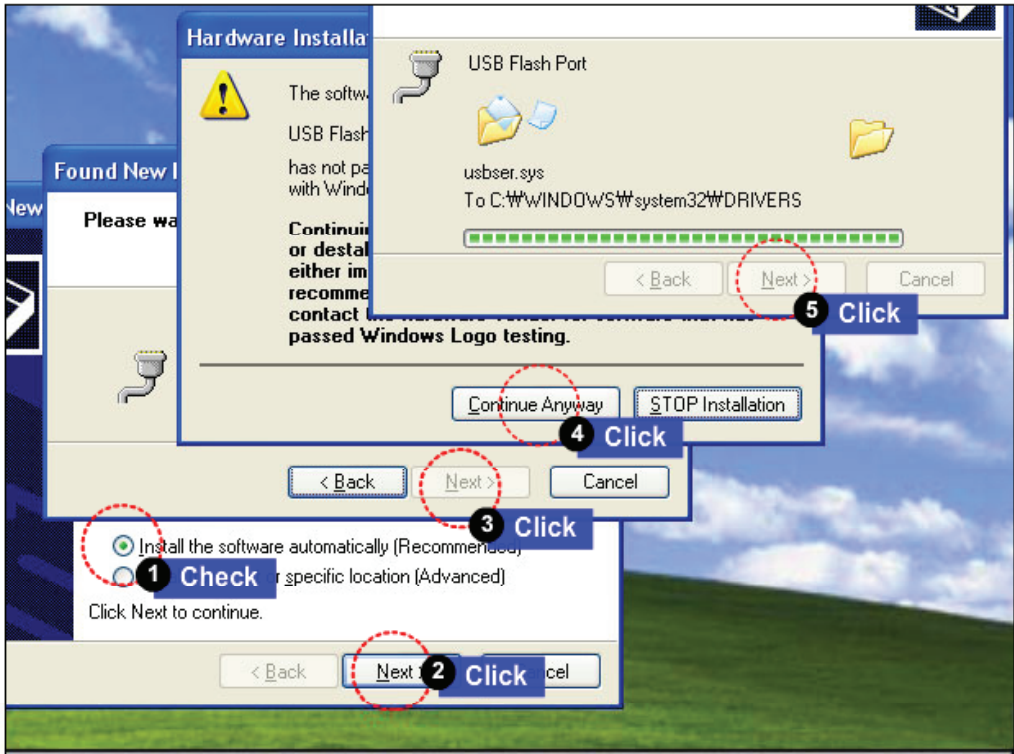


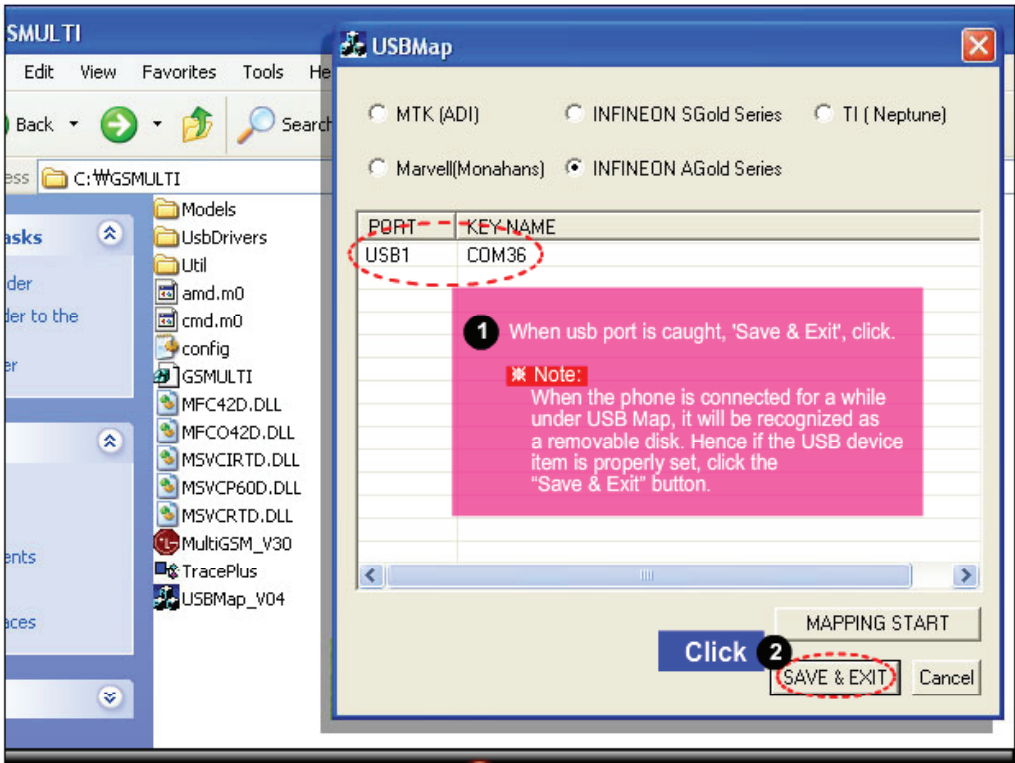
5. DOWNLOAD



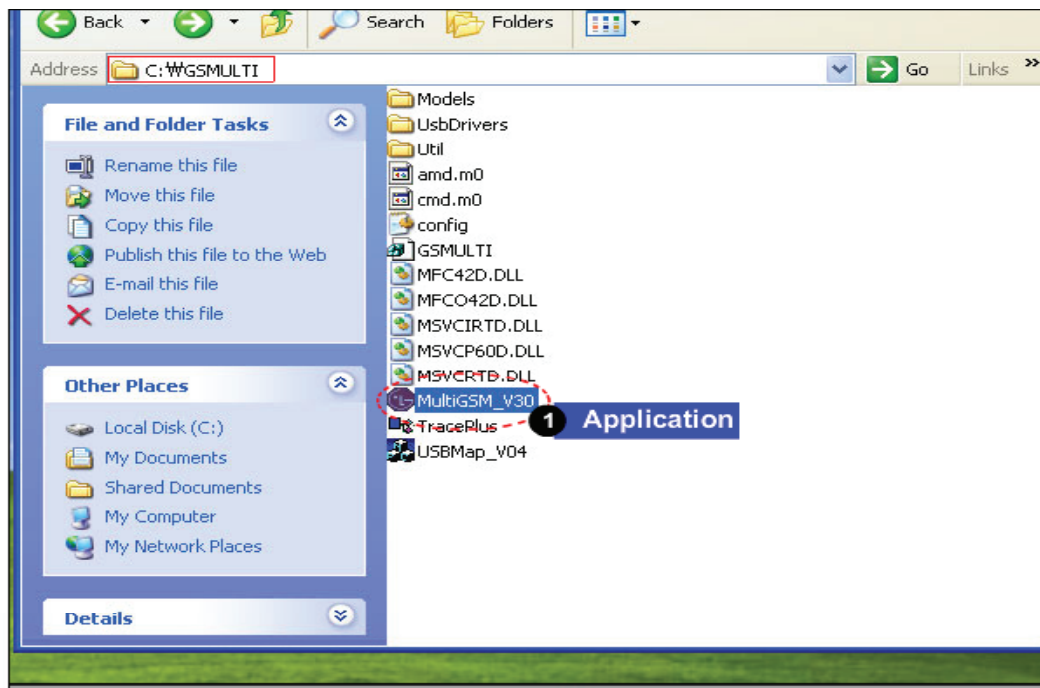
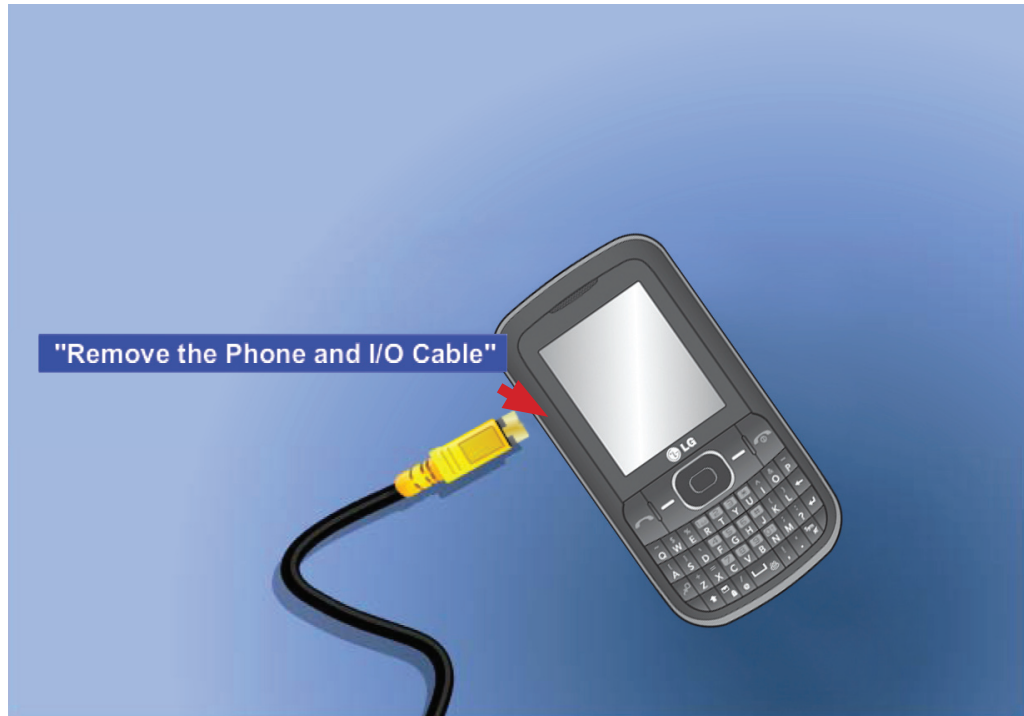
5. DOWNLOAD



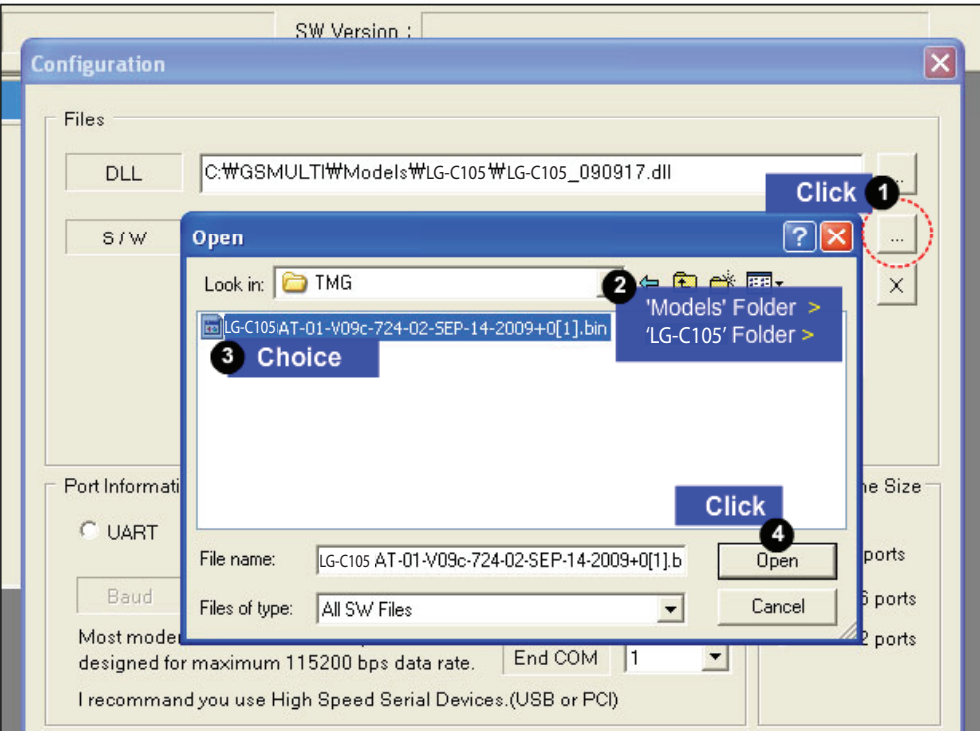
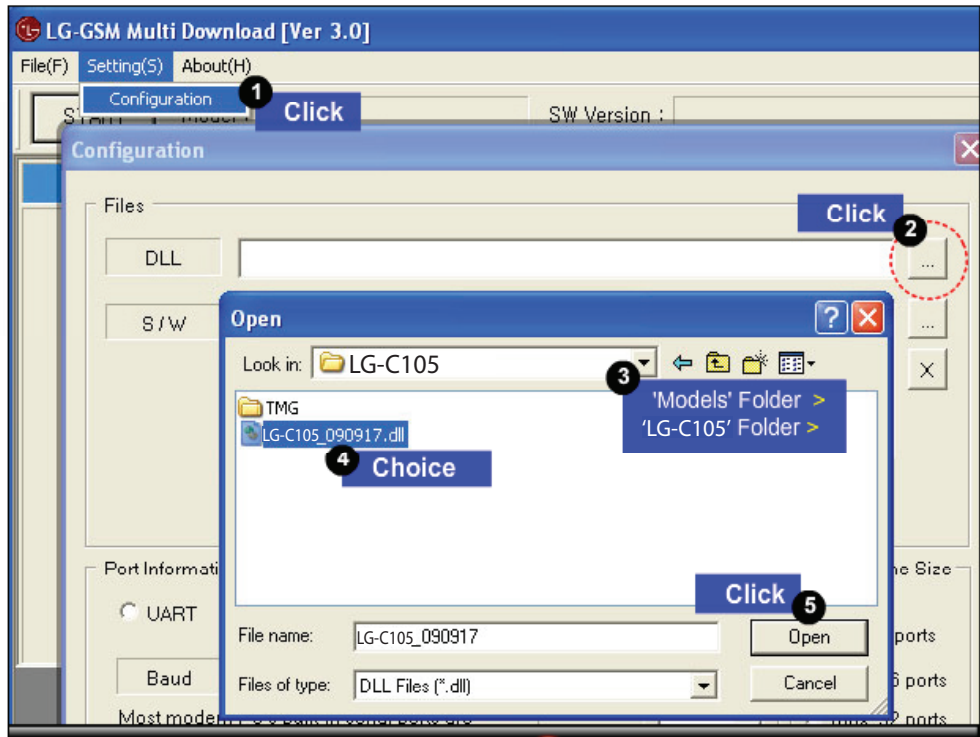




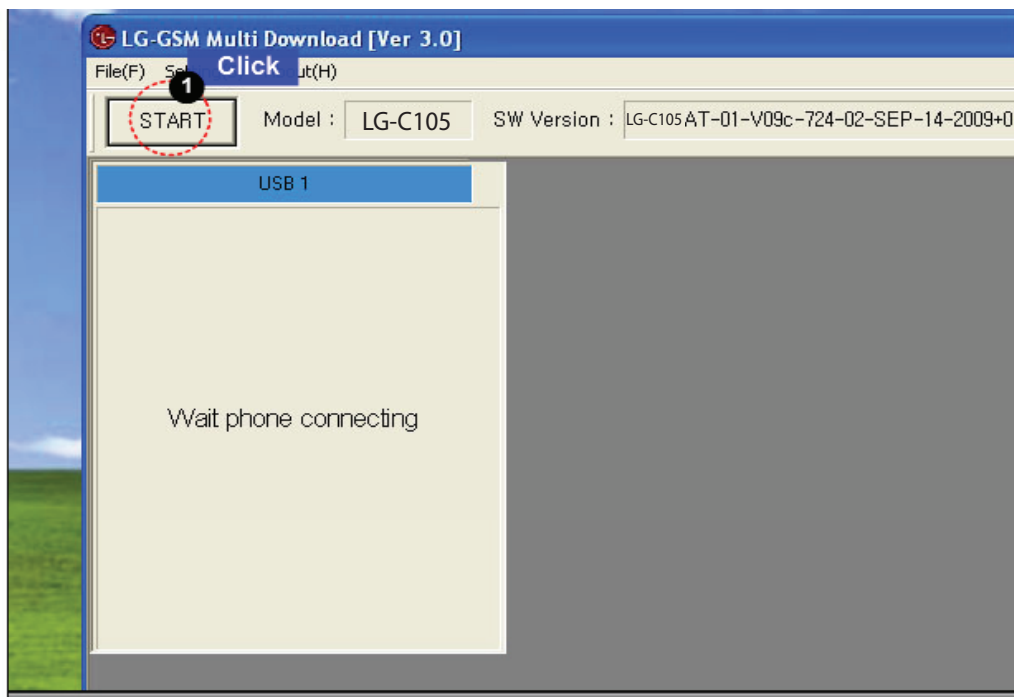
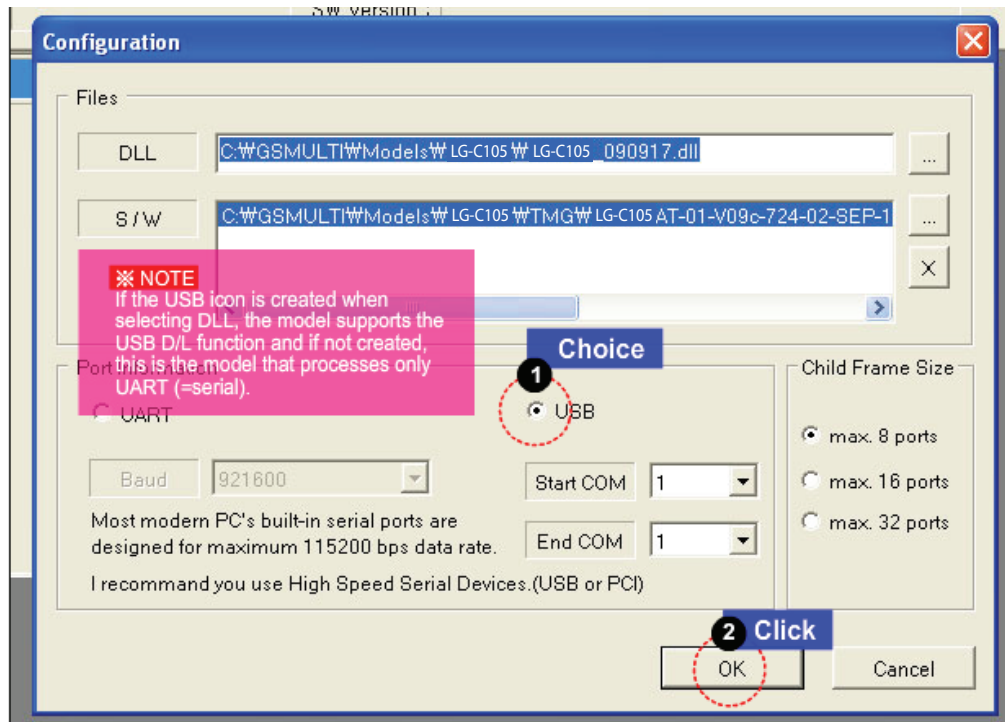
5. DOWNLOAD



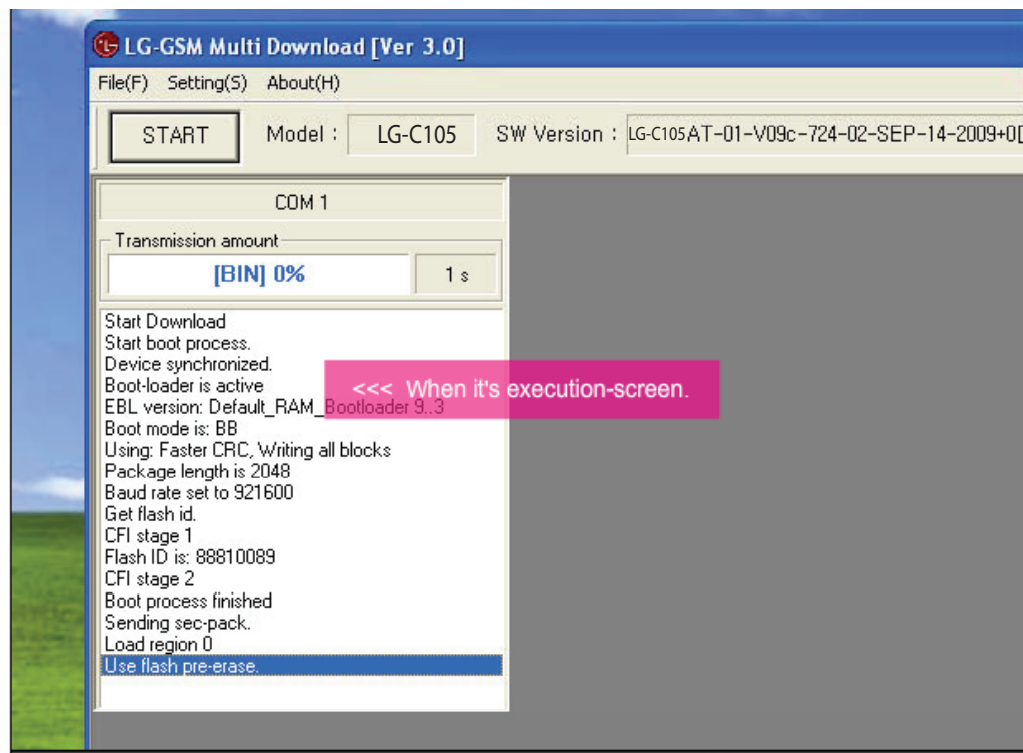
5. DOWNLOAD



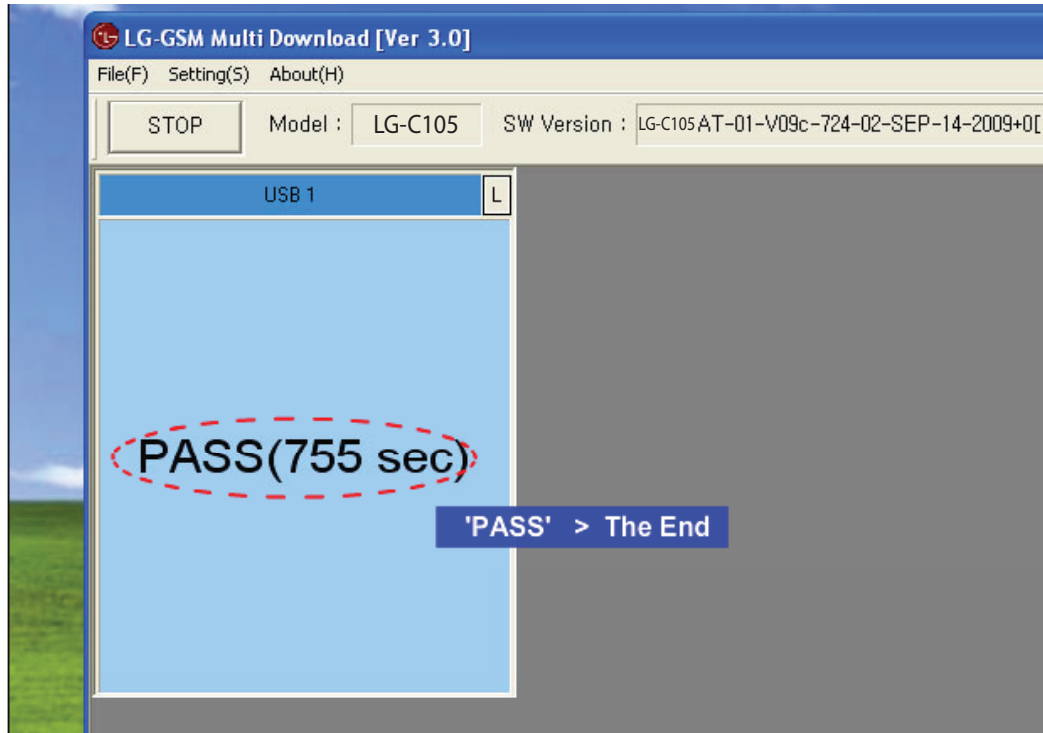
5. DOWNLOAD



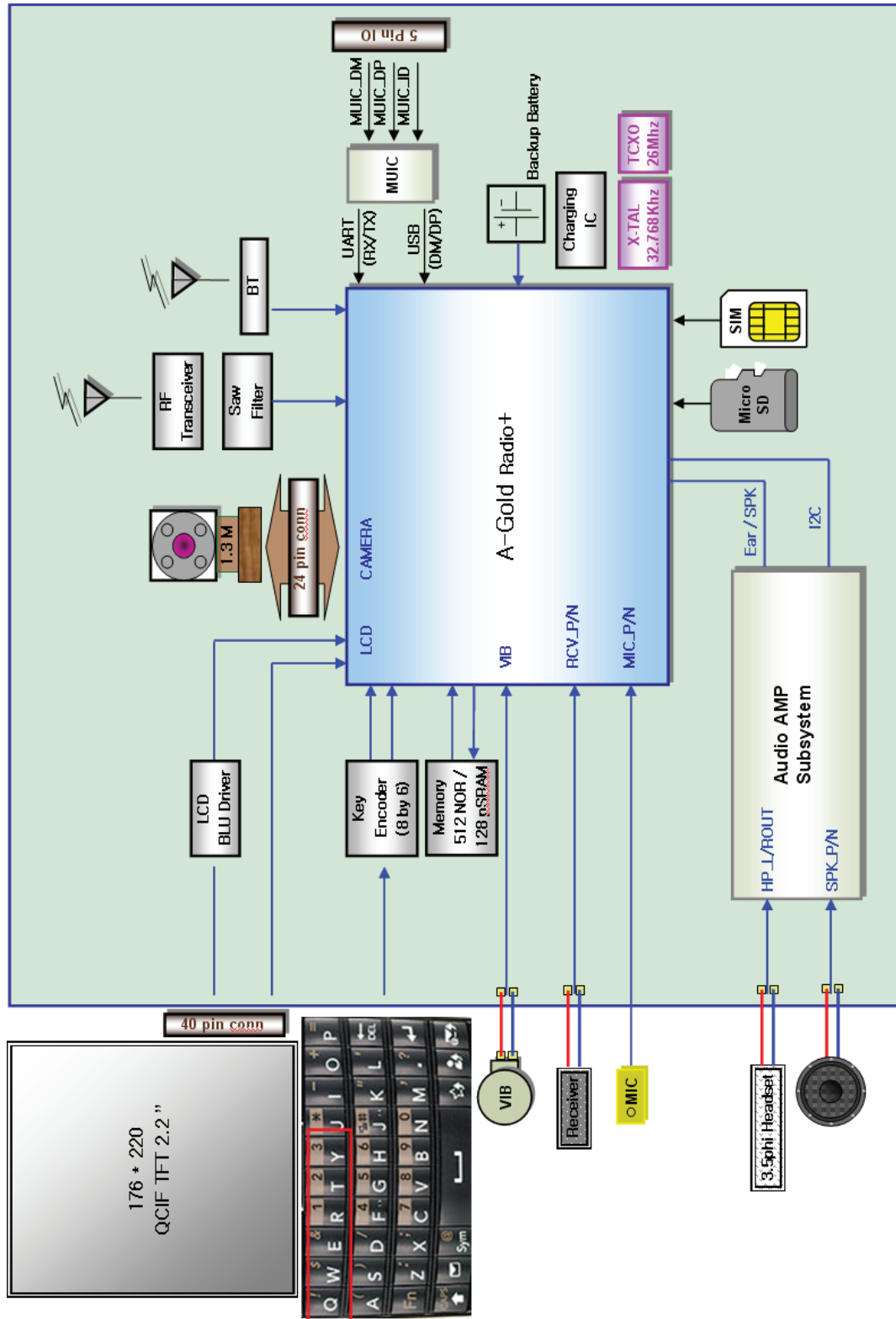
5. DOWNLOAD



5. DOWNLOAD

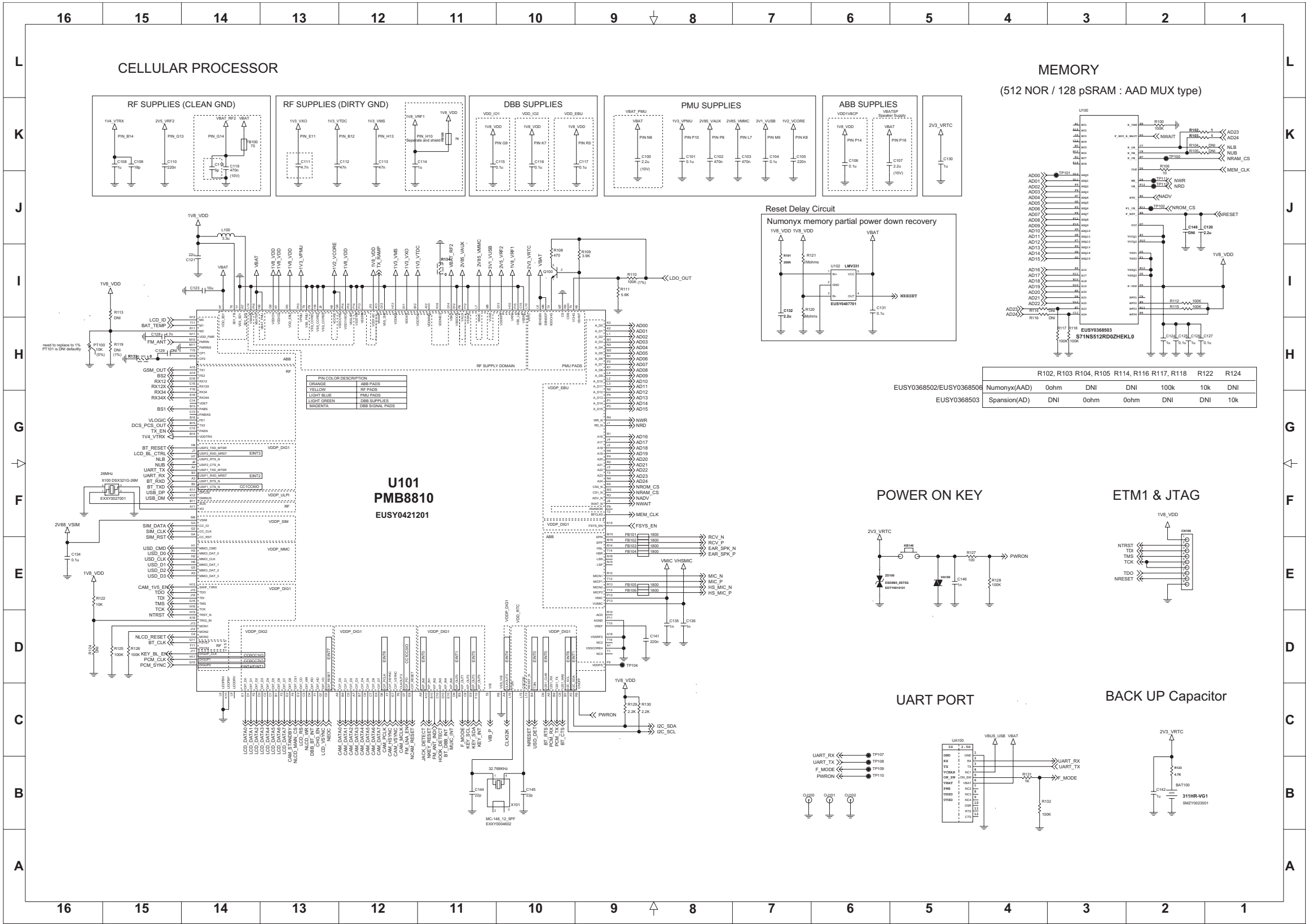


6. BLOCK DIAGRAM

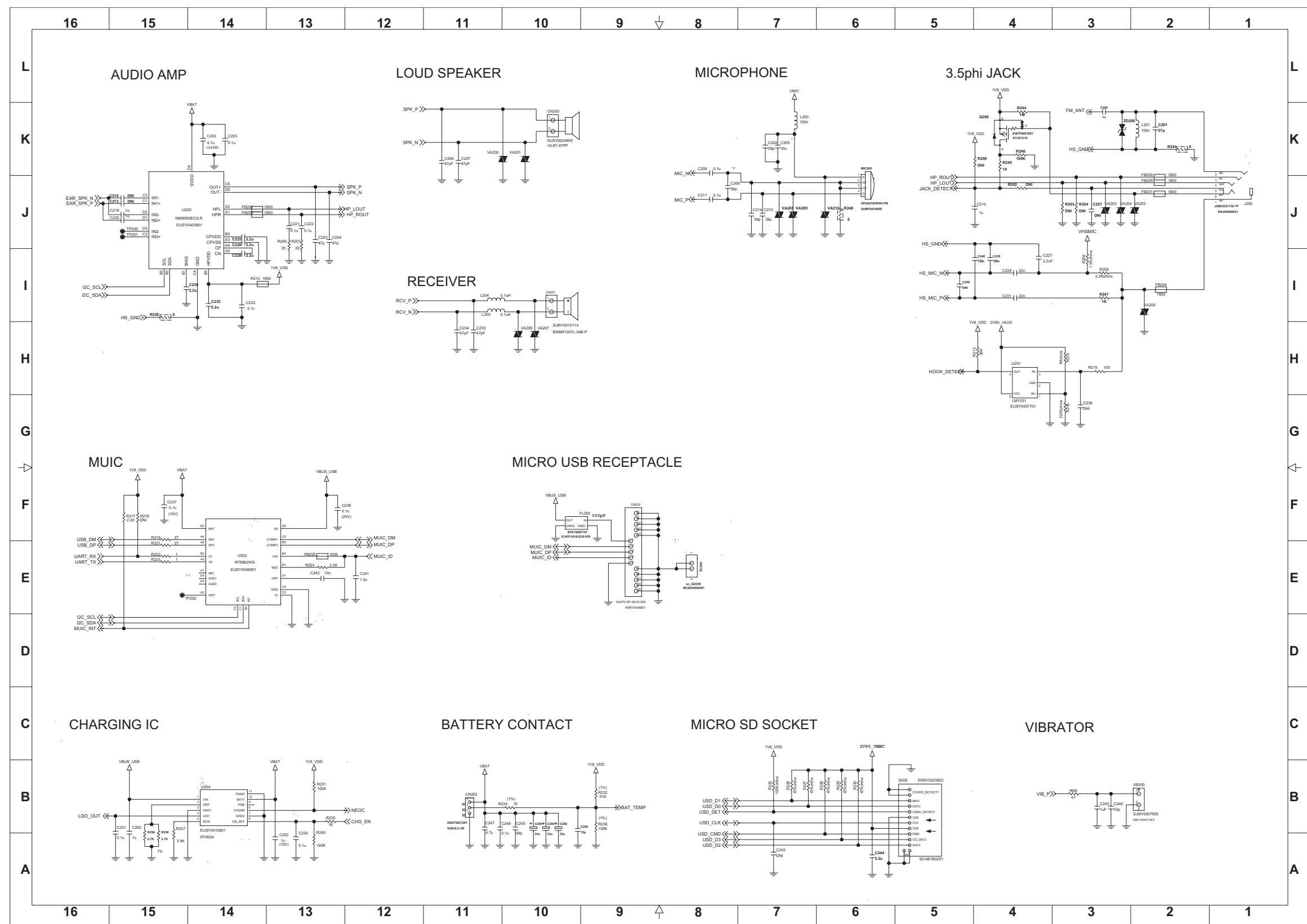




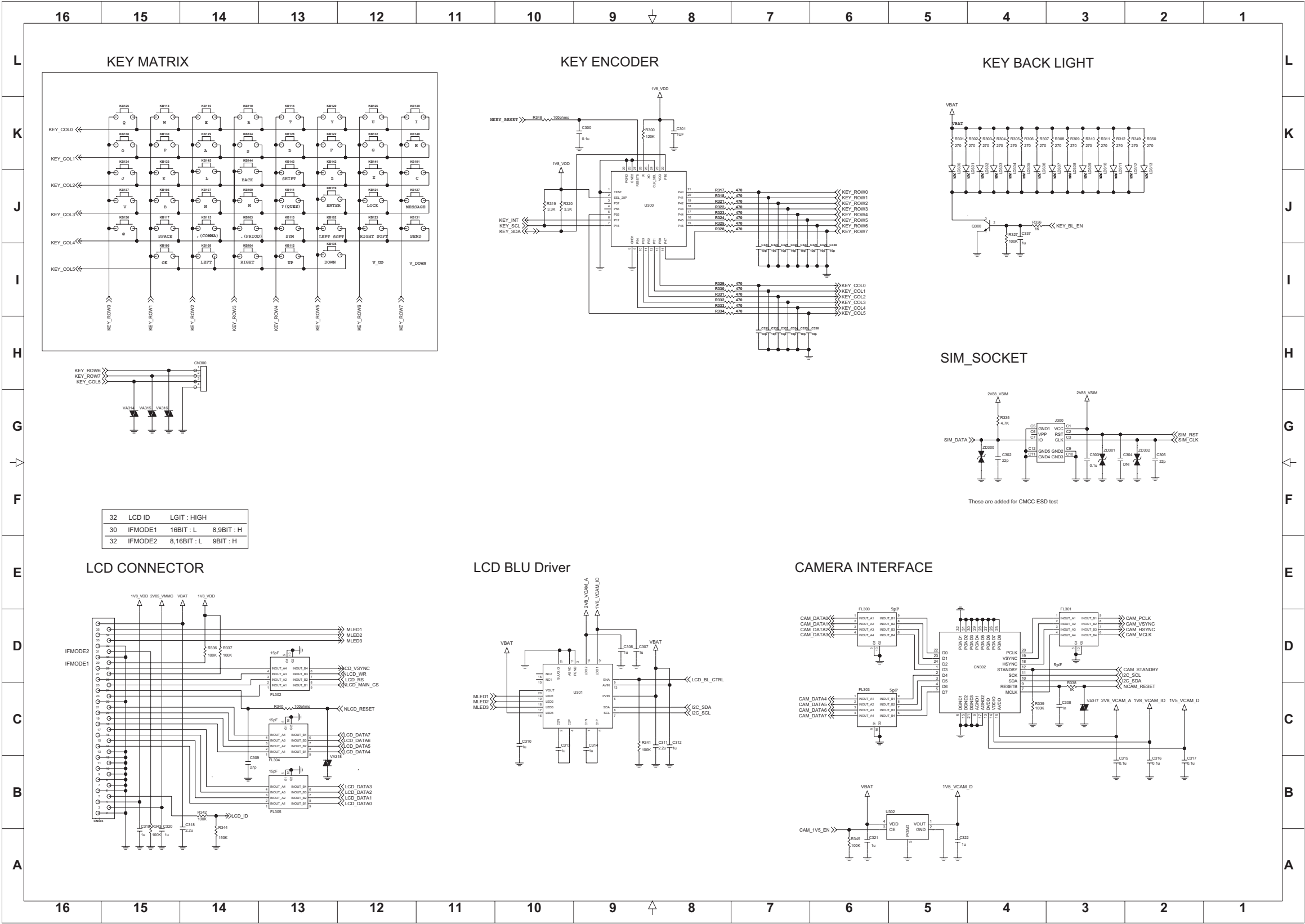
7. CIRCUIT DIAGRAM



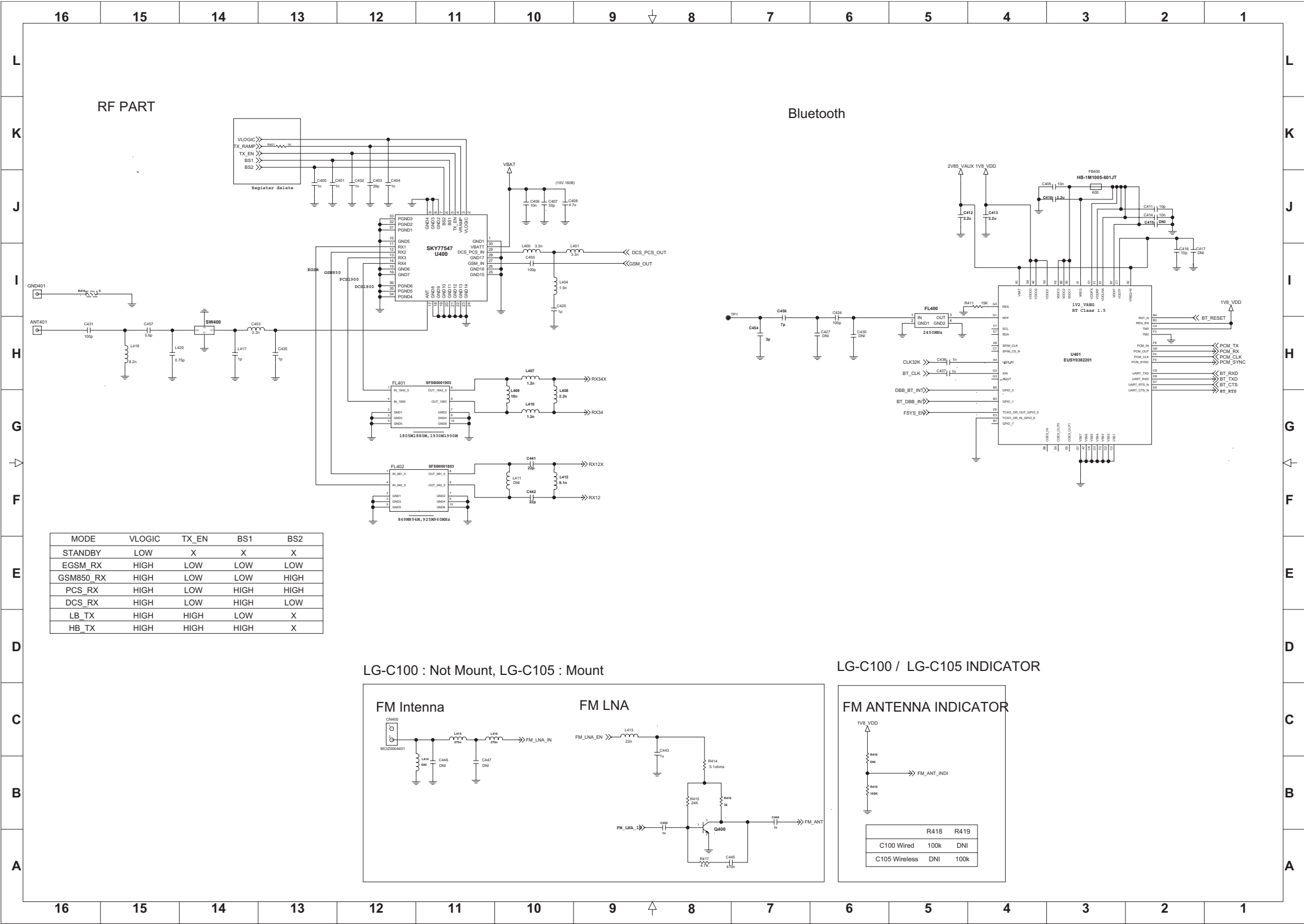
7. CIRCUIT DIAGRAM



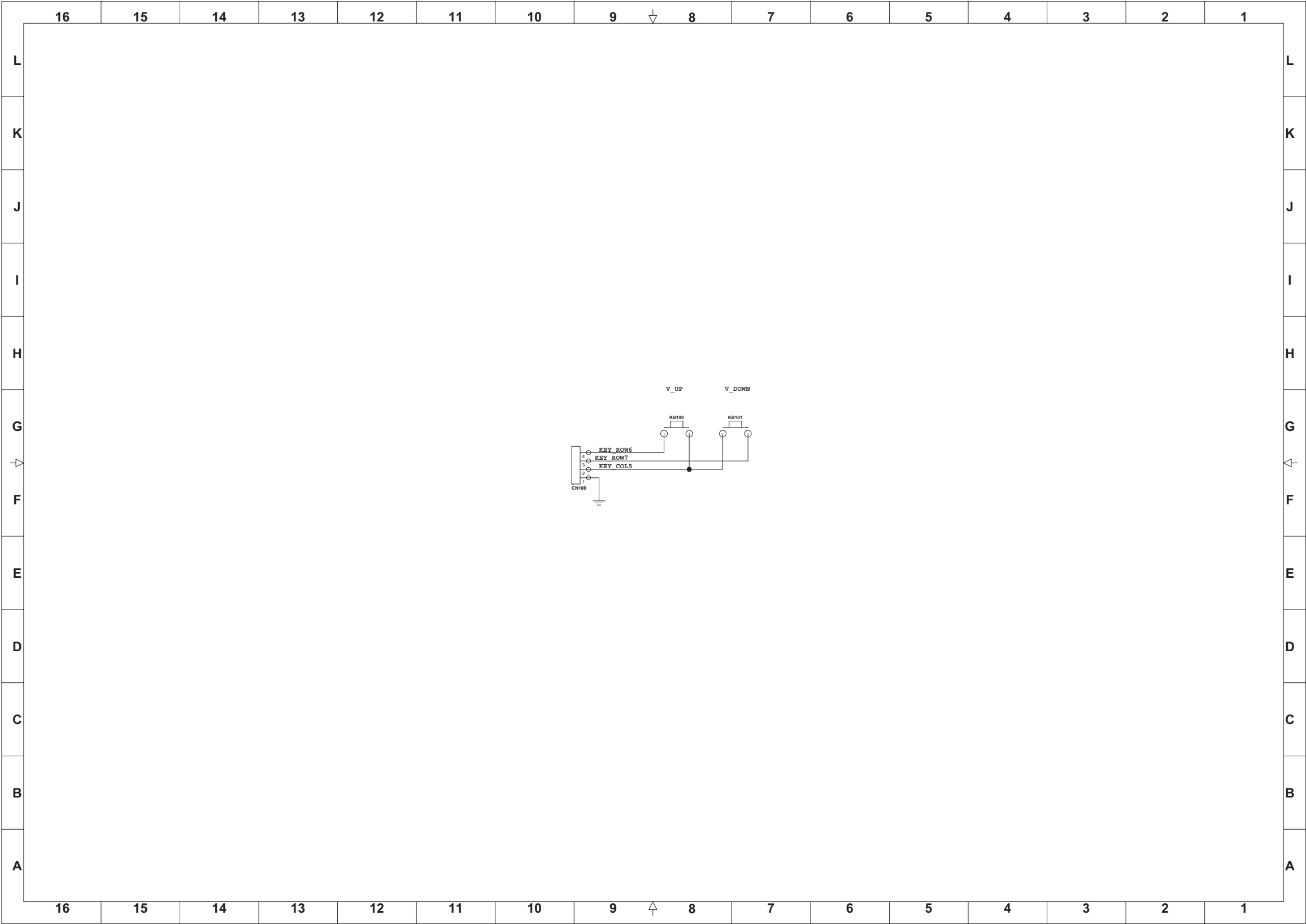
7. CIRCUIT DIAGRAM



7. CIRCUIT DIAGRAM

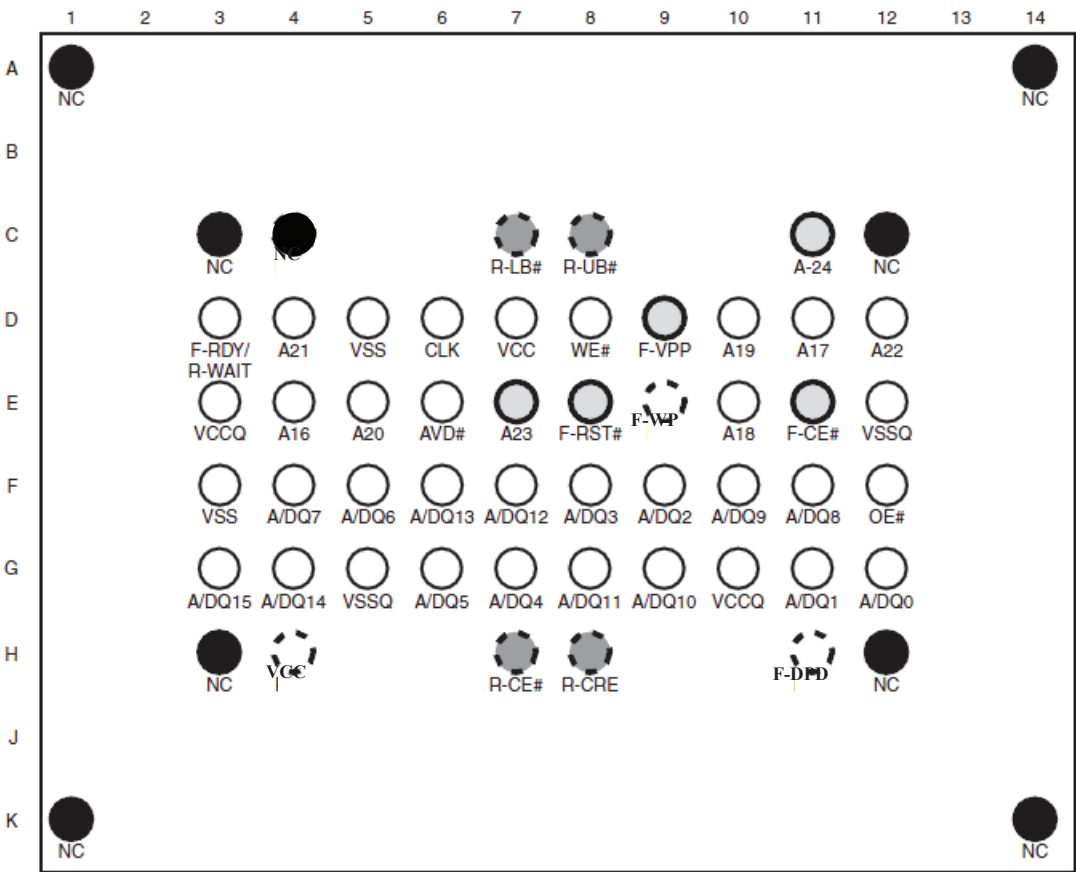


7. CIRCUIT DIAGRAM



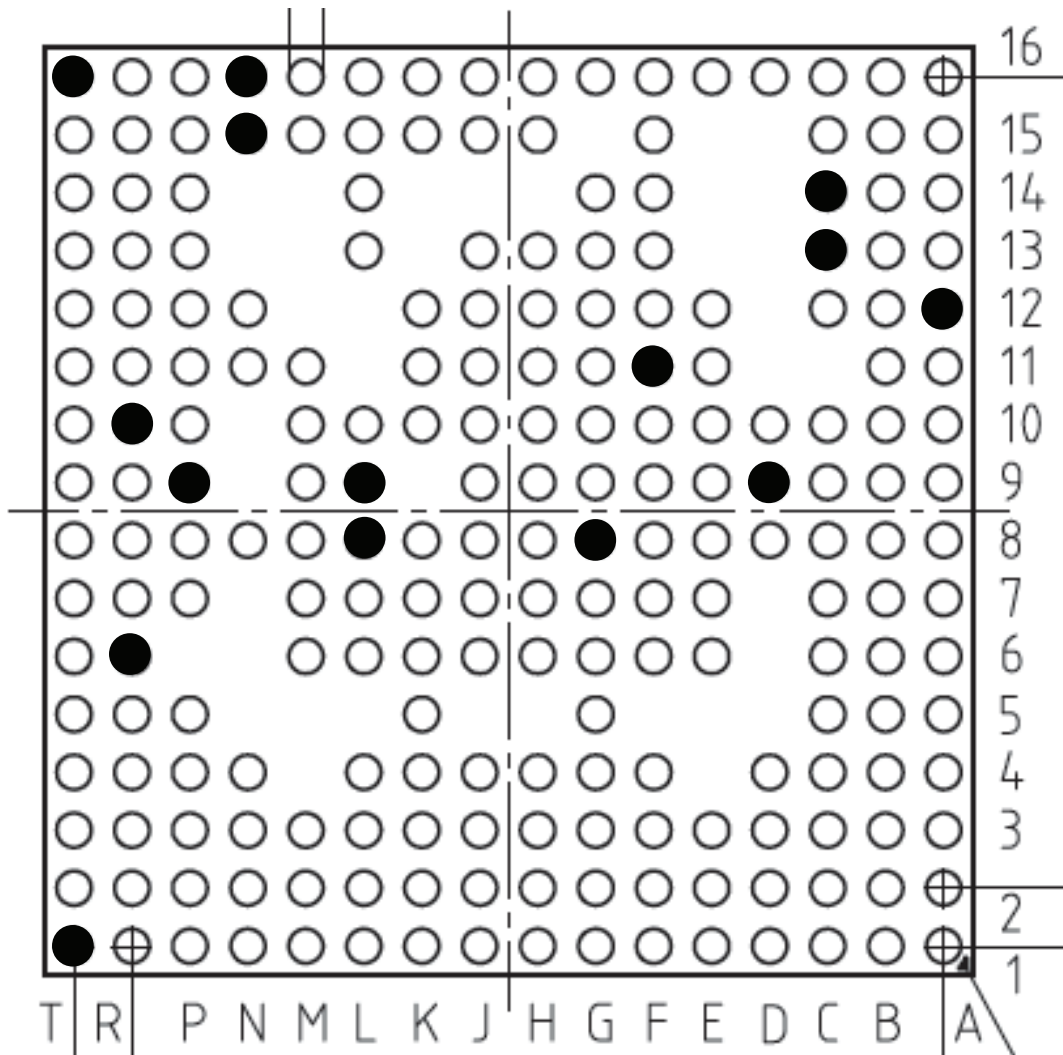
8. BGA PIN MAP

U100 (EUSY0368503, S71NS512RD0ZHEKL0)



8. BGA PIN MAP

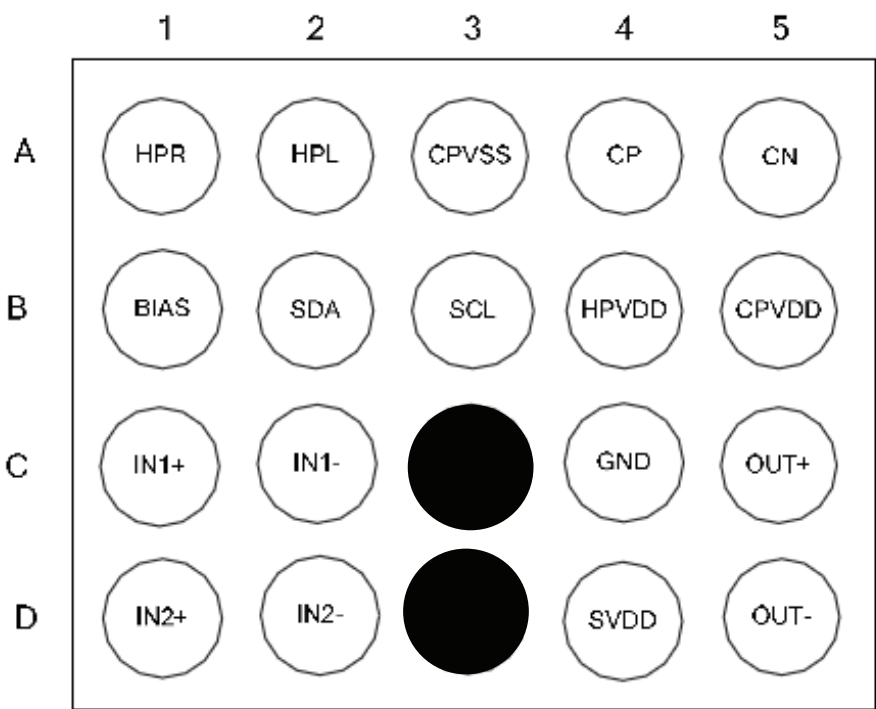
U101 (EUSY0421201, PMB8810)



○: Use

●: Not Use

U200 (EUSY0403901, WM9093ECS-R)

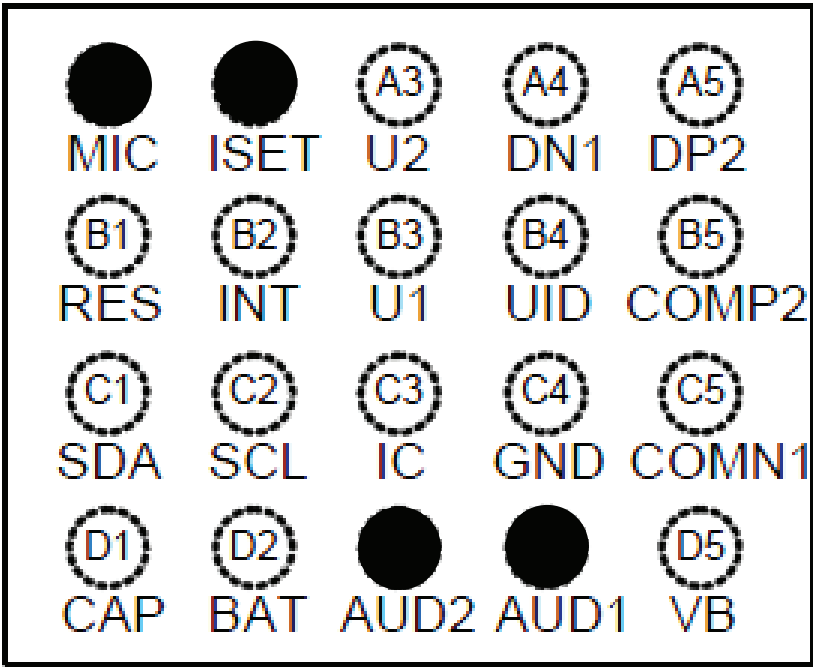


○ : Use

● : Not Use

8. BGA PIN MAP

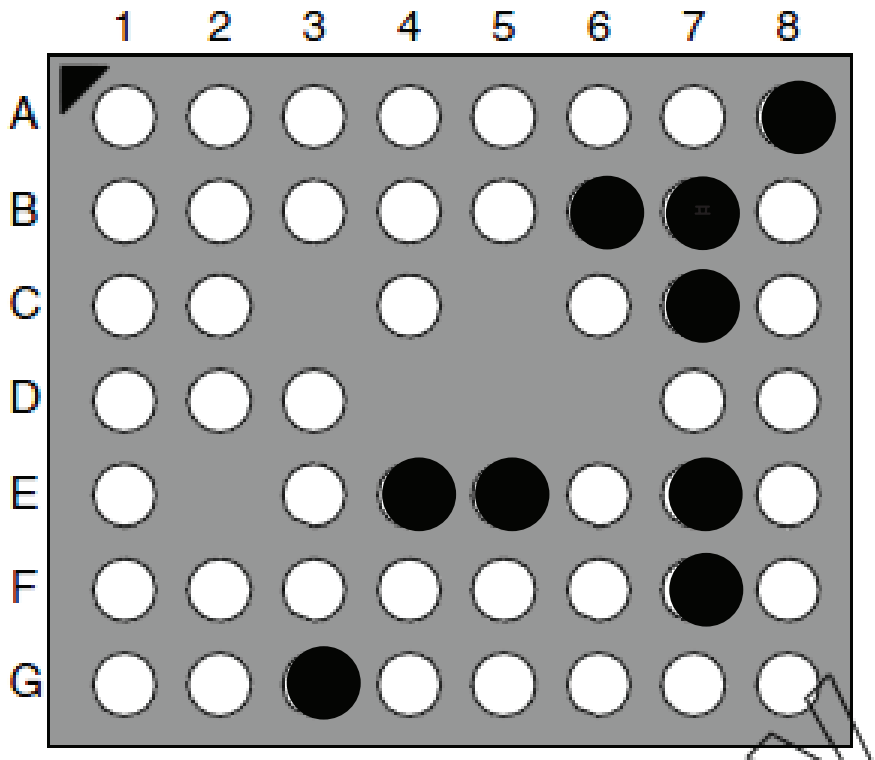
U202 (EUSY0406901, RT8962WS)



○: Use

●: Not Use

U401(EUSY0382201, BCM2070CB0KUFBXG)

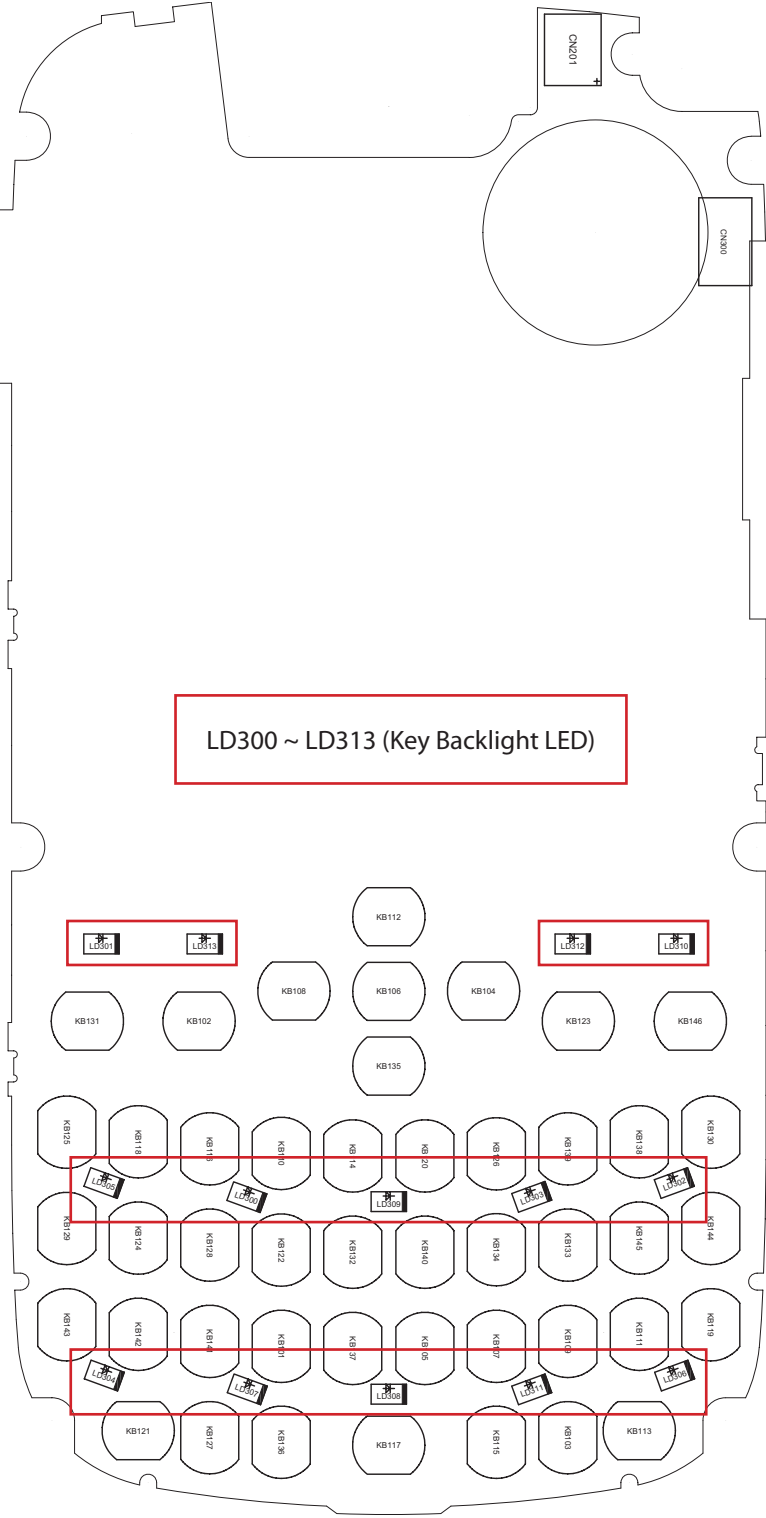


○: Use

●: Not Use



9. PCB LAYOUT



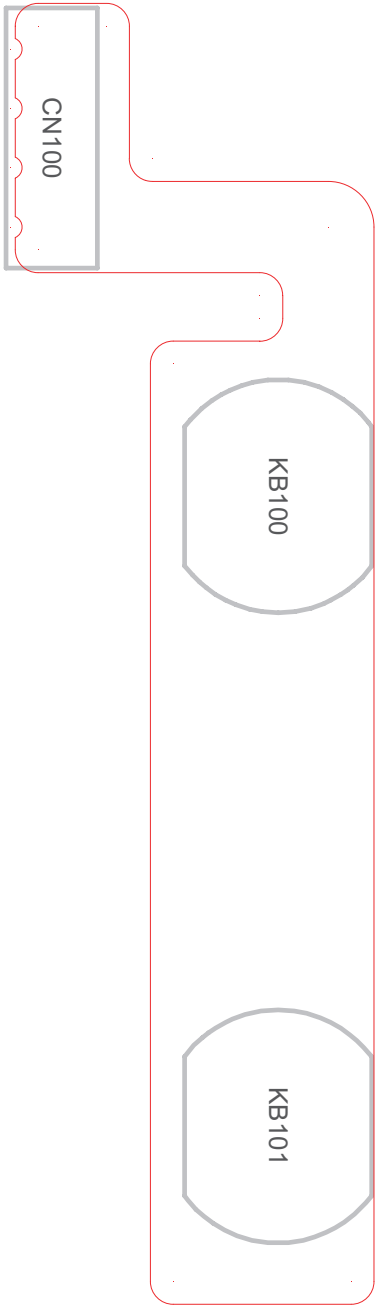
LG-C105_MAIN_SPFY0237601-1.0-TOP

9. PCB LAYOUT



LG-C105_MAIN_SPFY0237601-1.0-BOT

9. PCB LAYOUT



10.ENGINEERING MODE

Engineering mode is designed to allow a service man/engineer to view and test the basic functions provided by a handset. The key sequence for switching the engineering mode on is "1809#*350#" Select. Pressing END will switch back to non-engineering mode operation. Use Up and Down key to select a menu and press 'select' key to progress the test. Pressing 'back key will switch back to the original test menu.

[1] BB TEST

[1-1] Battery Info

[1-1-1] BattInfo

[1-2] Bluetooth Test

[1-2-1] Enter Test Mode

[1-2-2] OnOff Test

[1-2-3] Headset Test

[1-2-4] BT Test1

[1-2-5] BT Test2

[1-2-6] Xhtml Compose Print

[1-2-7] Xhtml Print Test

[2] Model Version

[2-1] Version

[3] Eng Mode

[3-1] Cell environ.

[3-2] PS Layer Info

[3-2-1] Mobility

[3-2-2] RadioRes

[3-2-1] Gprs

[3-3] Layer1 Info

[3-4] Reset Information

[3-5] Memory Configurarion

[3-6] MemGenConf

[3-7] MemAllUse

[3-8] MemDetUse

[3-9] MemDump

[3-10] Change Frequency Band

[4] Call Timer

[5] Factory Reset

[6] MF TEST

[6-1] All Auto Test

[6-2] Backlight

[6-2-1] BacklightOn

[6-2-2] BacklightOff

[6-3] Audio

[6-3-1] Audio Test

[6-4] Vibrator

[6-4-1] VibratorOn

[6-4-2] VibratorOff

[6-5] LCD

[6-5-1] Auto LCD

[6-6] Key pad

[6-7] Mic Speaker

[6-8] Camera

[6-8-1] Camera Main Preview

[6-8-2] FlashOn

[6-8-3] FlashOff

[6-8-4] CameraFlashBunning

[6-9] FM Radio

[6-9-1] FM Radio Test

[7] Network selection

[7-1] Automatic

[7-2] GSM850

[7-3] EGSM

[7-4] DCS

[7-5] PCS

11. STAND ALONE TEST

11. STAND ALONE TEST

11.1 Introduction

This manual explains how to examine the status of RX and TX of the model.

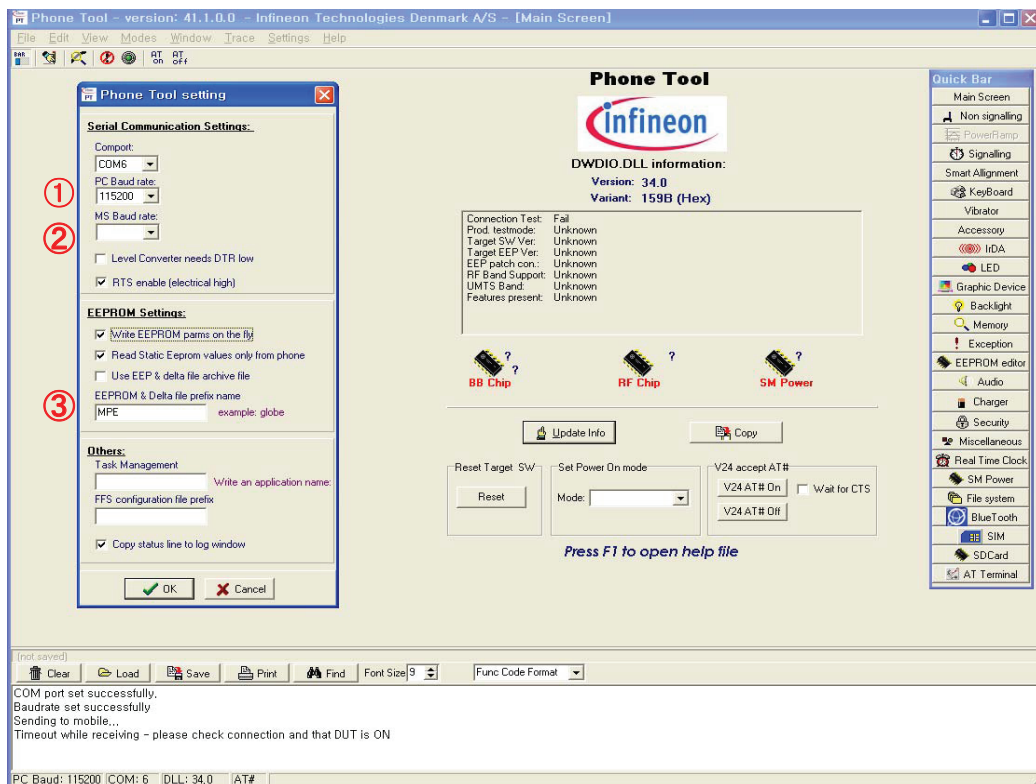
A. Tx Test

TX test - this is to see if the transmitter of the phones is activating normally.

B. Rx Test

RX test - this is to see if the receiver of the phones is activating normally.

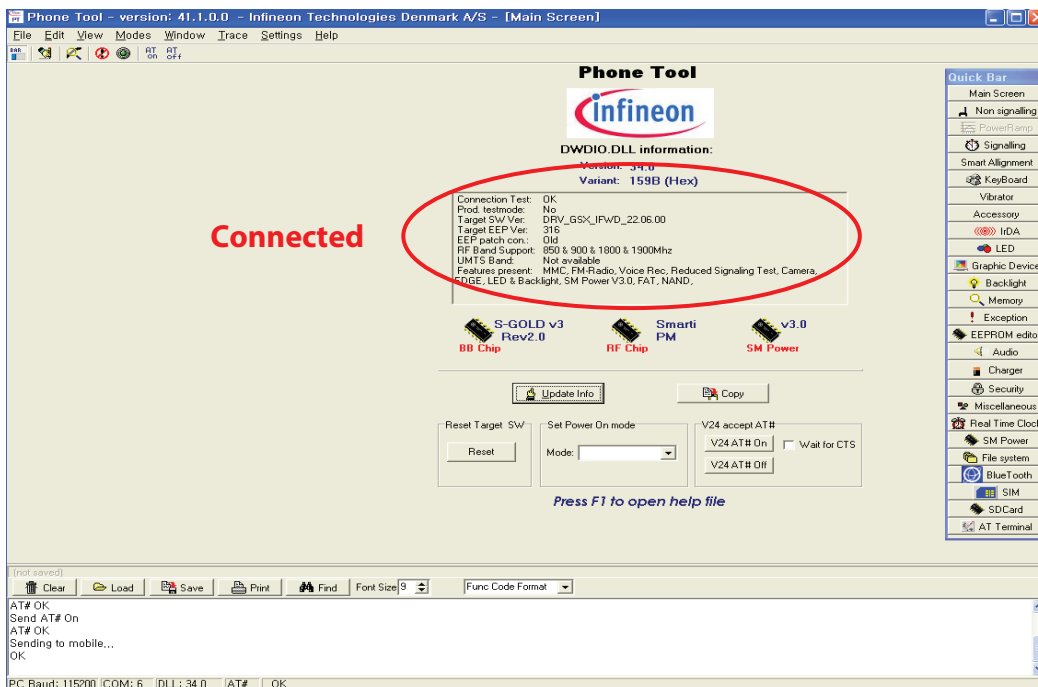
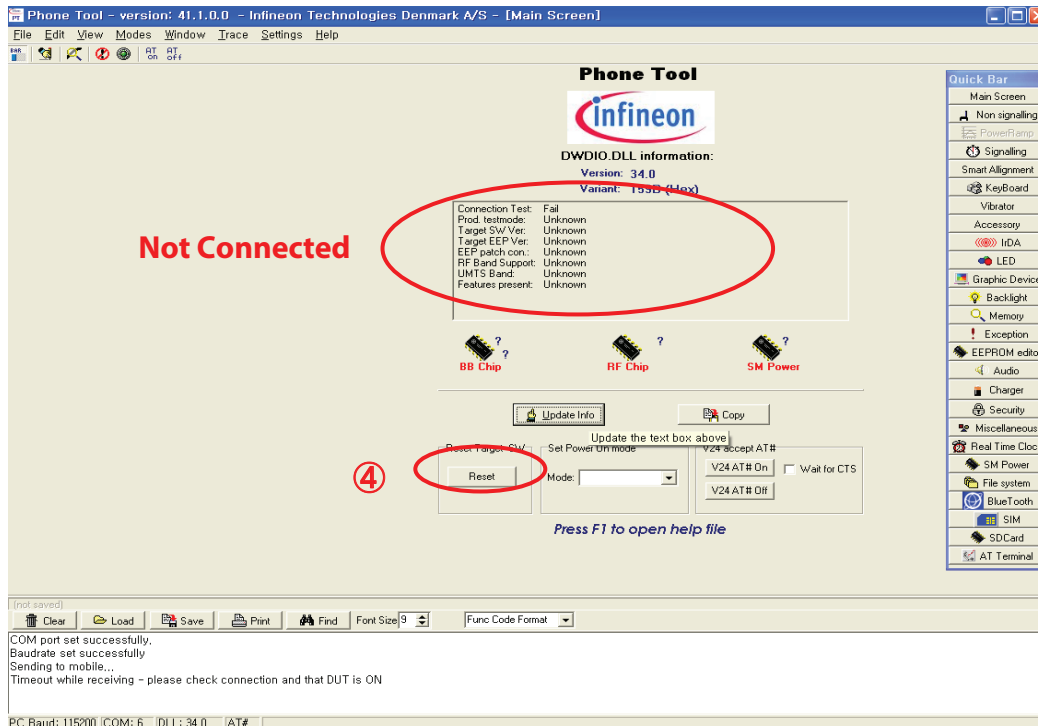
11.2 Setting Method



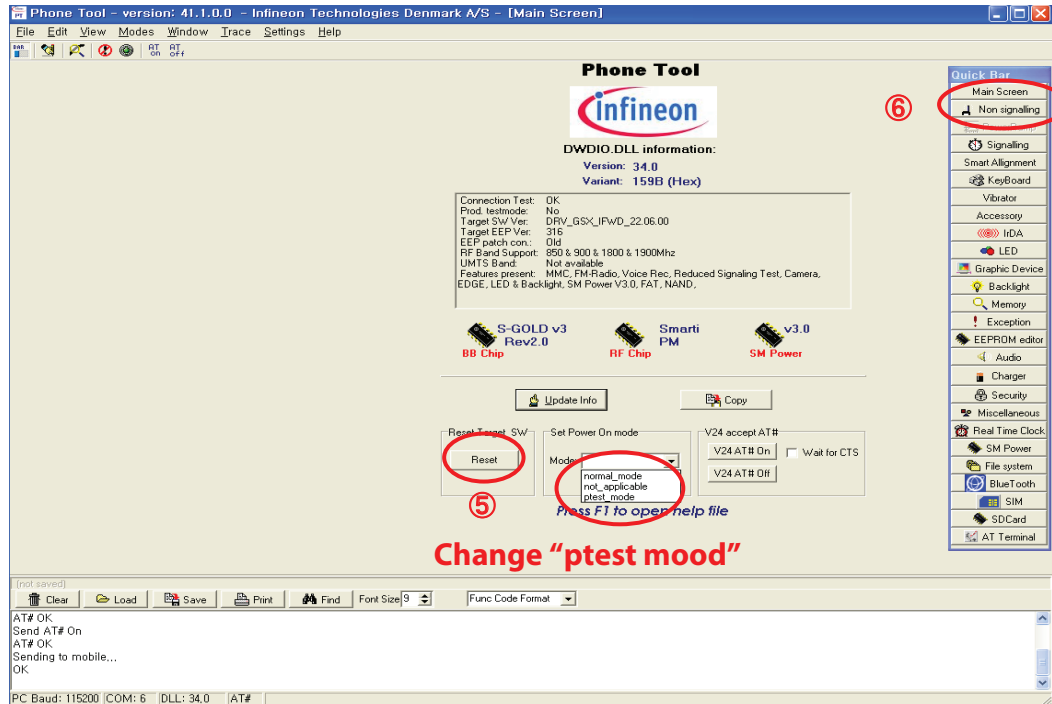
1. Set COM Port
2. Check PC Bau Rate
3. Confirm EEPROM & Delta file prefix name

11. STAND ALONE TEST

4. Click "Update Info" for communicating Phone and Test-Program

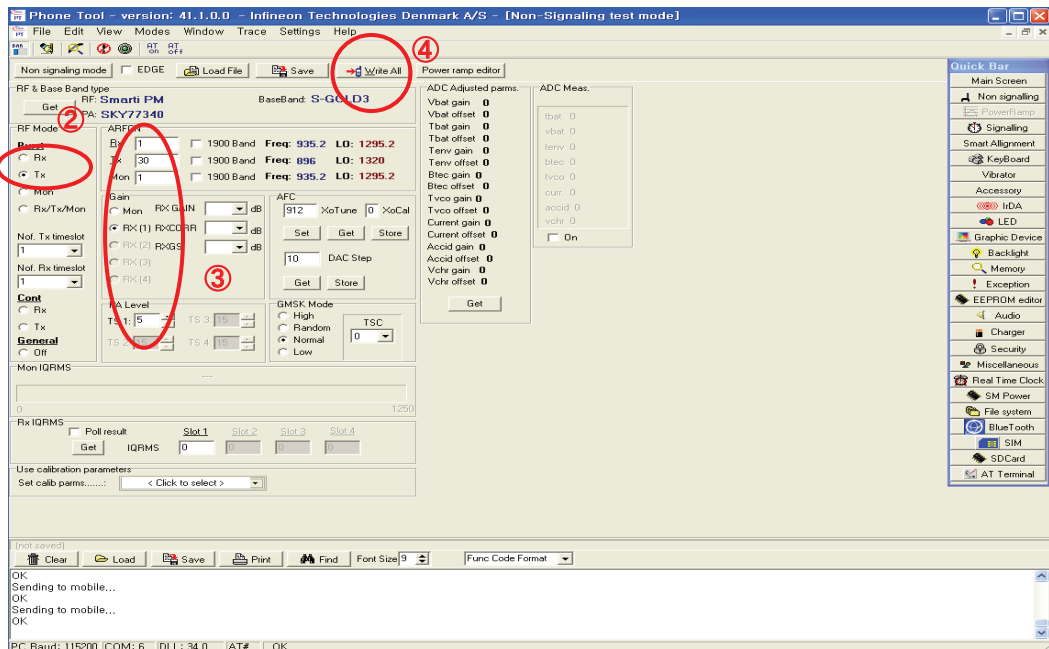
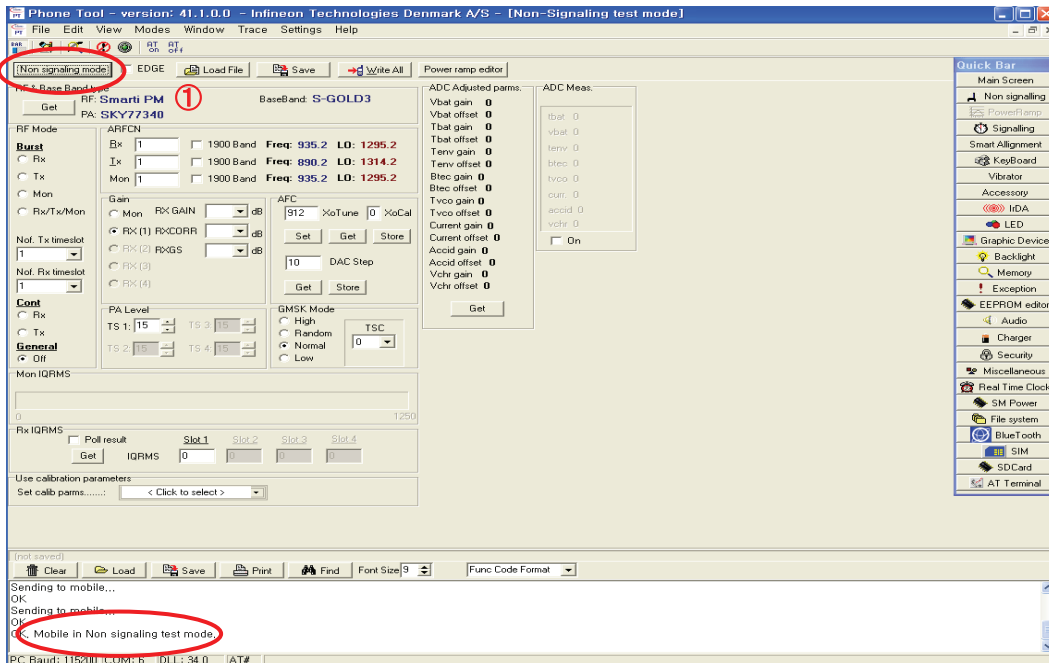


11. STAND ALONE TEST



5. For the purpose of the Standalone Test, Change the Phone to "ptest mode" and then Click the "Reset" bar.
6. Select "Non signaling" in the Quick Bar menu. Then Standalone Test setup is finished.

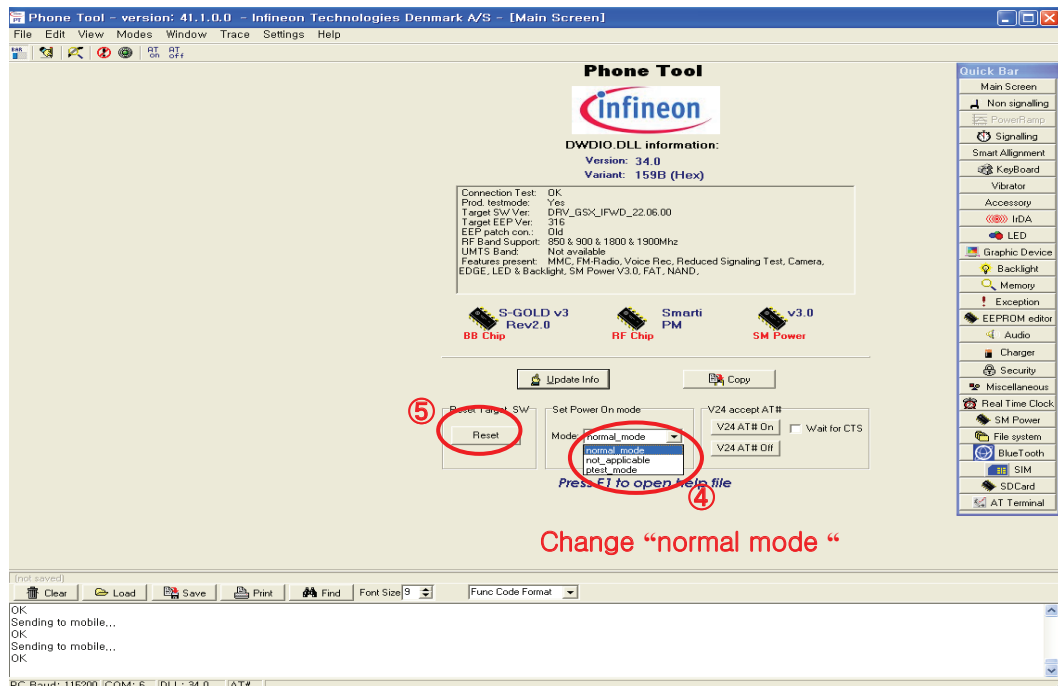
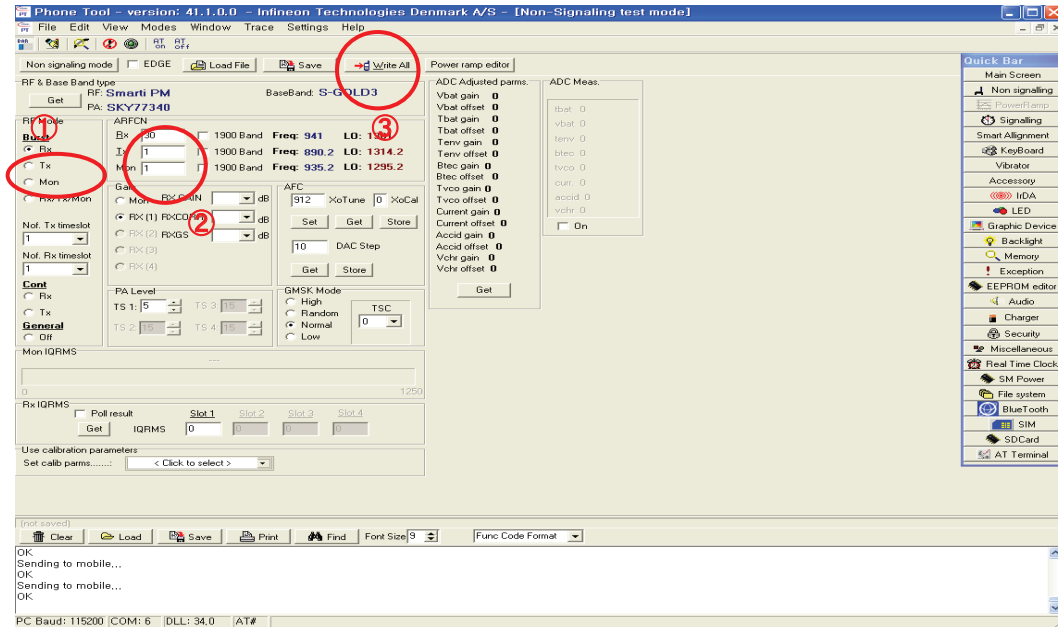
11.3 Tx Test



1. "Non signaling mode" bar and then confirm "OK" text in the command line.
2. Put the number of TX Channel in the ARFCN
3. Select "Tx" in the RF mode menu and "PCL" in the PA Level menu.
4. Finally, Click "Write All" bar and try the efficiency test of Phone.

11. STAND ALONE TEST

11.4 Rx Test



1. Put the number of RX Channel in the ARFCN.
2. Select "Rx" in the RF mode menu.
3. Finally, Click "Write All" bar and try the efficiency test of Phone.
4. The Phone must be changed "normal mode" after finishing Test.
5. Change the Phone to "normal mode" and then Click the "Reset" bar.

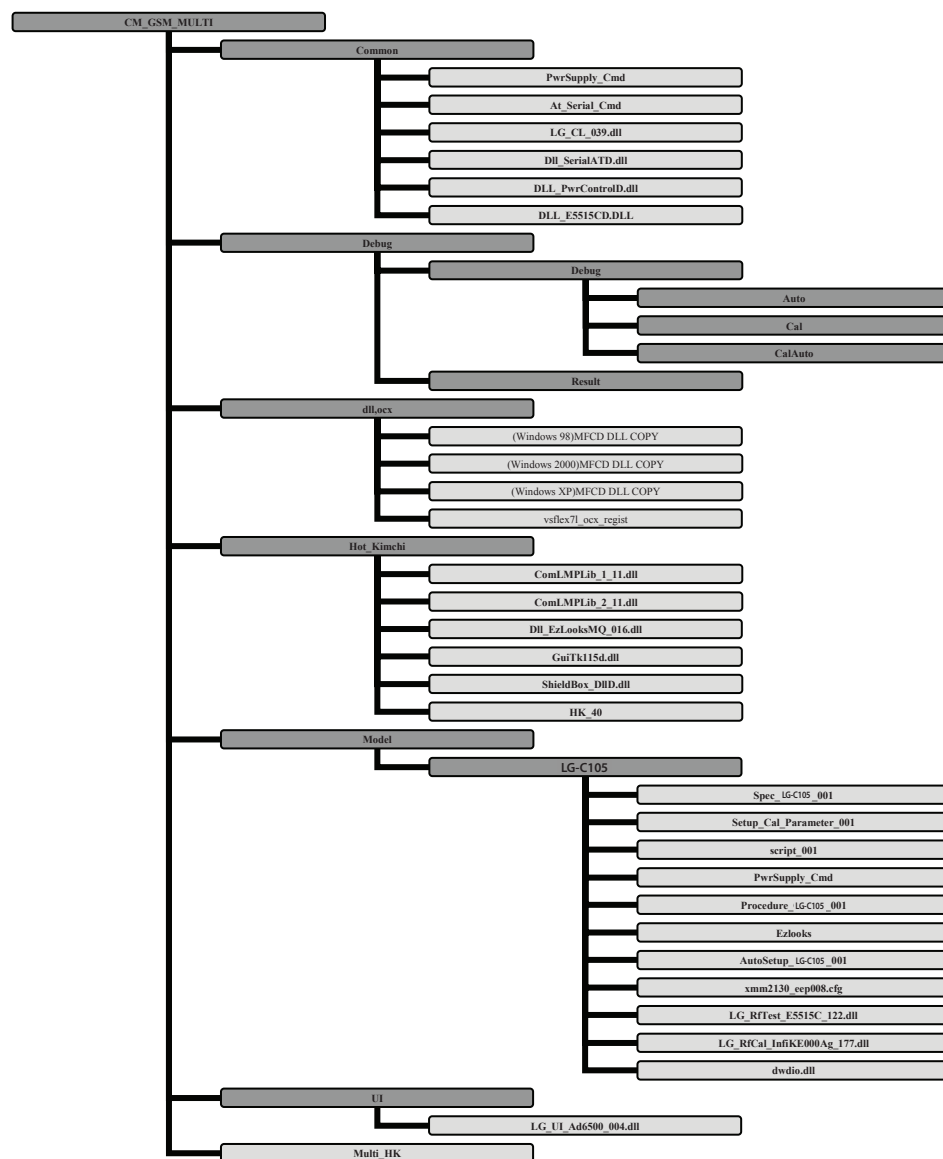
12.AUTO CALIBRATION

12.1 Overview

Auto-cal (Auto Calibration) is the PC side Calibration tool that perform Tx, Rx and Battery Calibration with Agilent 8960(GSM call setting instrument) and Tektronix PS2521G(Programmable Power supply).

Auto-cal generates calibration data by communicating with phone and measuring equipment then write it into calibration data block of flash memory in GSM phone.

12.2 Configuration of HotKimchi



12.AUTO CALIBRATION

12.3 Description of Basic File

12.3.1 Common

- **LG_CL_039.dll** : Common logic dll, Module In Charge of Reading PID & S/W Version, Booting.
- **Dll_SerialATD.dll** : Serial Communication Module From Phone by AT Command.
- **DLL_PwrControlD.dll** : Communication Module From Power supply.
- **DLL_E5515CD.DLL** : Communication Module From Agilent 8960(Test Set).
- **At_Serial_Cmd.xml** : Definition File of AT Command.
- **PwrSupply_Cmd.xml** : Definition File of Power supply command.

12.3.2 Debug

- **Debug** - Cal : Result File of Calibration.
Auto : Result File of Auto Test.
CalAuto : Result File of Cal & Auto Test.

12.3.3 dll, ocx

- **vsflex7l_ocx_regist** : Registration File for System use
- **Windows XXX)MFCD DLL** : Registration File for System use

12.3.4 HotKimchi

- **HK_40.exe** : Execute File, HK_XX → XX is File Version.
- **ComLMPLib_1_11.dll** : Communication Module With PLC or Shield Box In Automation Rack.
Support to J&S Shield Box and Tescom TC-5981A.
- **ComLMPLib_2_11.dll** : Communication Module With PLC or Shield Box In Automation Rack.
Support to J&S Shield Box and Tescom TC-5981A.
- **Dll_EzLooksMQ_005.dll** : Communication Module with ezTray Installed In Local PC.
- **GuiTk115d.dll** : control library
- **ShieldBox_DIID.dll** : Communication with Shield Box. Support to Tescom TC-5952B.

12.3.5 Model

- **LG_RfCal_InfiKE000Ag_177.dll** : Main Module of Calibration
- **LG_RfTest_E5515C_122.dll** : Main Module of Auto Test
- **Xmm2130_eep008.cfg** : Cal Data Save binary Module.
- **AutoSetup_LG-C105_100.xml** : RF TEST Setup Module.
- **Ezlooks.xml** : Calibration ezLooks Item & Cal Spec Definition Module.
- **Procedure_LG-C105_001.xml** : RF TEST Procedure Definition Module.
- **Script_001.xml** : RF TEST Setup & calibration Setup Module.
- **Spec_LG-C105_001.xml** : Definition Module of Auto Test Spec
- **Setup_Cal_Parameter_001.xml** : Calibration Definition Module.

12.3.6 UI

-. **LG_UI_Ad6500_002.dll** : ADI Model UI DLL.

12.3.7 Multi_HK

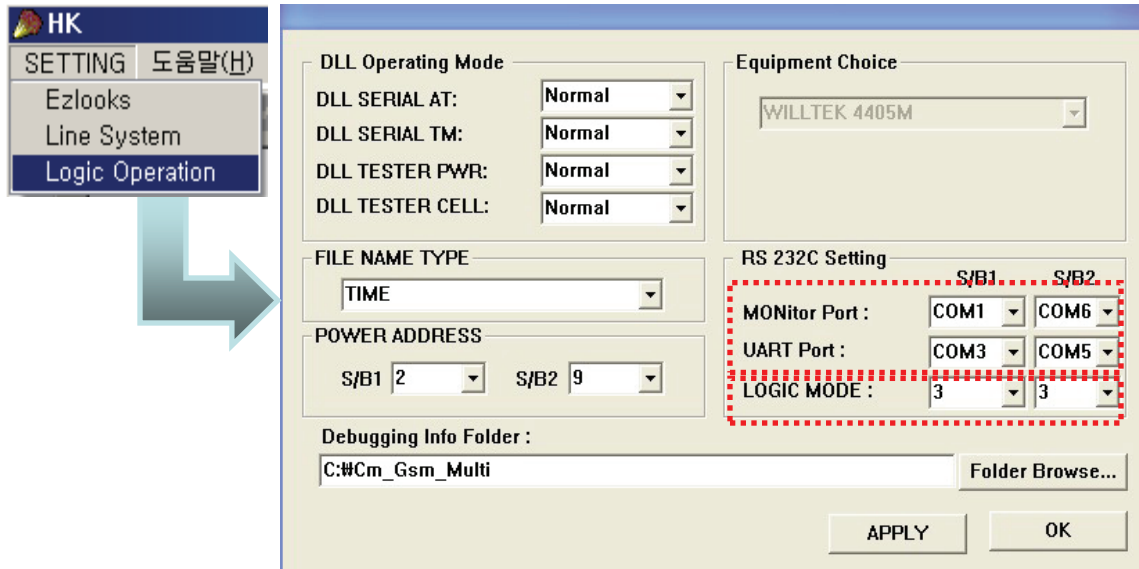
-. Registration File For System Setting.

1. Connect as Fig 6-2(RS232 serial cable is connected between COM port of PC and MON port of TEST JIG, in general)
2. Set the Power Supply 4.0V
3. Set the 3rd, 4th of DIP SW ON state always
4. Press the Phone power key, if the Remote ON is used, 1st ON state

12.4 Procedure

1. Copy the file to C:\Cm_Gsm_Multi
2. Copy the files of((Windows XXX)MFCD DLL, vsflex7l_ocx_regist to C:\Cm_Gsm_Multi\dll,ocx
3. Select MFCD DLL of your computer OS
4. Click on "vsflex7l_ocx_regist"
5. Click on "Multi_HK reg"
6. Connect as Fig 11-2 (RS232 serial cable is connected between COM port of PC, in general.)
7. . Run HK_40exe to start calibration.
8. Click " Logic Operation" of "SETTING" menu bar

12.AUTO CALIBRATION

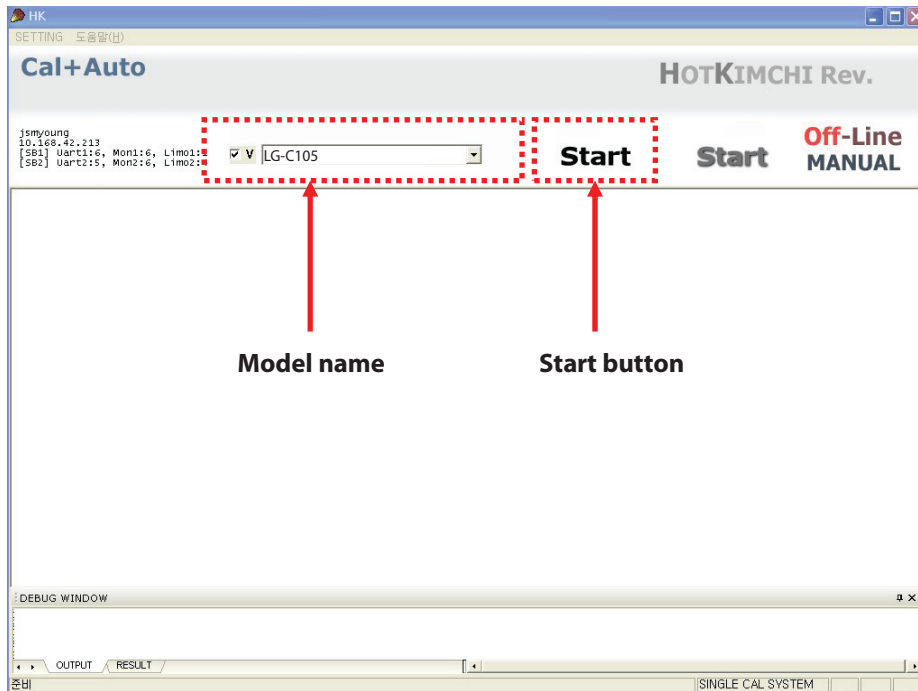


9. Set PORT (using RS232 cable) that PC can communicate with the phone

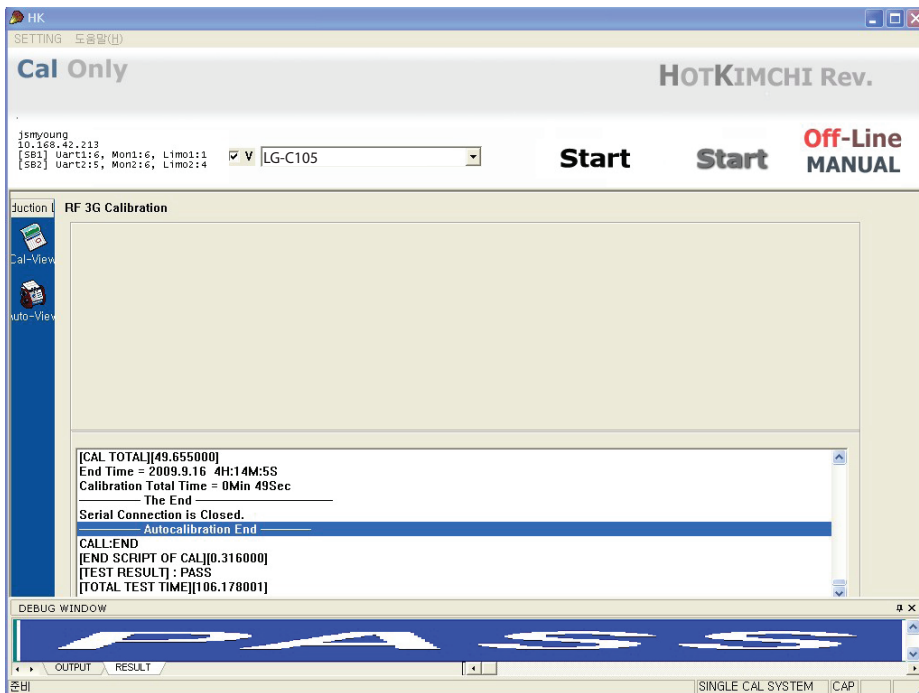
10. Select " LOGIC MODE" that you want

- Logic mode: 1-> Calibration only
- 2-> Auto test only
- 3-> Cal & Auto

11. Select the model name "LG-C105"



12. Click "start" button



12.AUTO CALIBRATION

12.5 AGC

This procedure is for Rx calibration.

In this procedure, We can get RSSI correction value. Set band EGSM and press Start button the result window will show correction values per every power level and gain code and the same measure is performed per every frequency.

12.6 APC

This procedure is for Tx calibration.

In this procedure you can get proper scale factor value and measured power level.

12.7 ADC

This procedure is for battery calibration.

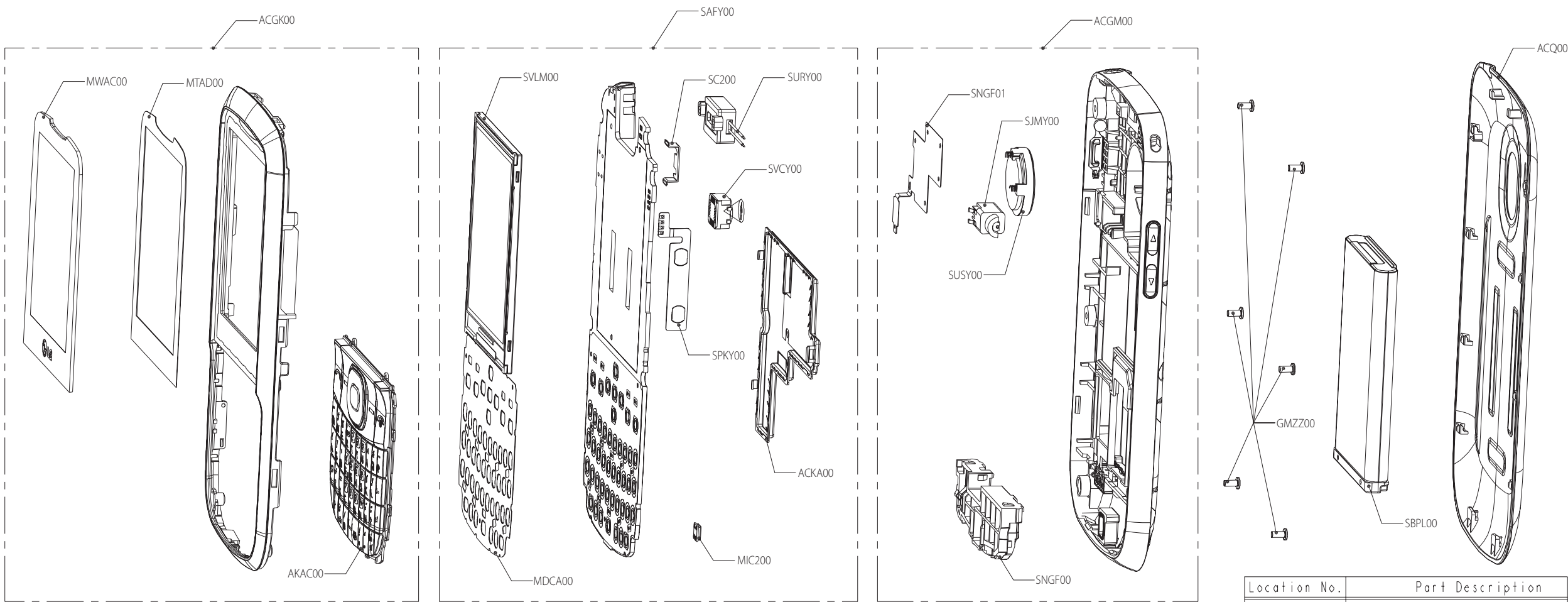
You can get main Battery Config Table and temperature Config Table will be reset.

12.8 Target Power

BAND	Description	Low	Middle	High
GSM 850	Channel	128	191	251
	Frequency	824.2 MHz	836.8 MHz	848.8 MHz
	Max power	32.5 dBm	32.5 dBm	32.5 dBm
EGSM 900	Channel	975	37	124
	Frequency	880.2 MHz	897.4 MHz	914.8 MHz
	Max power	32.5 dBm	32.5 dBm	32.5 dBm
DCS1800	Channel	512	699	885
	Frequency	1710.2 MHz	1747.6 MHz	1784.8 MHz
	Max power	29.5 dBm	29.5 dBm	29.5 dBm
PCS 1900	Channel	512	661	810
	Frequency	1850.2 MHz	1880 MHz	1909.8 MHz
	Max power	29.5 dBm	29.5 dBm	29.5 dBm

13. EXPLODED VIEW & REPLACEMENT PART LIST

13.1 EXPLODED VIEW



Location No.	Part Description
ACQ00	Cover Assembly,Battery
SBPL00	Rechargeable Battery,Lithium Ion
ACGK00	Cover Assembly,Front
AKAC00	Keypad Assembly,Main
MTAD00	Tape,Window
MWAC00	Window, LCD
ACGM00	Cover Assembly,Rear
SJMY00	Motor, DC
SNGF00	Antenna,Helical
SNGF01	Antenna,Helical
SUSY00	Speaker, Module
GMZZ00	Screw, Machine
SAFY00	PCB Assembly, Main
SURY00	Receiver
ACKA00	Can Assembly, Shield
ADCA00	Dome Assembly, Metal
SPKY00	PCB,Sidekey
SVCY00	Camera Module
SVLM00	LCD, Module-TFT
SC200	Can, Shield
MIC200	Microphone, Condenser

13. EXPLODED VIEW & REPLACEMENT PART LIST

13.2 Replacement Parts <Mechanic component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
1	AAD000000	Addition Assembly	AAAY0523504-8	LGC105.ACLRRDRD:Red-	
2	ACQ004100	Cover Assembly, Battery	ACQ85291501-2	LGC100.AIDNRDZZ:WithoutColor-	
3	MCK004100	Cover, Battery	MCJA0120901	COMPLEXLG-C100IDNRDRD:RedMOLD,PCLUPOYSC-1004A,,,,,	
3	MJN061100	Tape, Protect	MJN67688001	COMPLEXLGC100.AIDNRDZZ:WithoutColor-	
2	MFL053800	Manual, Operation	MMBB0392812	COMPLEXLGC105.ACLRRDZZ:WithoutColorLGC105manual forCLR	
1	AGF000000	Package Assembly	APAY0151205	LGC105.ABRABKZZ:WithoutColorLG-C105BrazilPacking	
1	AGQ000000	Phone Assembly	APEY0952711-2	LGC105.ACLRRDRD:RedUADSRef.APEY0952701	
2	ACQ100400	Cover Assembly, EMS	ACGY0087507-4	LGC105.ACLRRDRD:Red-	
3	ACGK00	Cover Assembly, Front	ACGK0171701-9	LG-C100IDNRDRD:Red-	
4	AKAC00	Keypad Assembly, Main	AKAC0019701	LG-C100IDNRDZZ:WithoutColor-	
4	MCJK00	Cover, Front	MCJK0135801-2	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
5	MBFZ00	Bracket	MBFZ0055901	COMPLEXLG-C100IDNRDZZ:WithoutColorPRESS,STS,,,,,	
5	MICE00	Insert, Nut	MICE0016903	COMPLEXMECH_COMMONZZ:WithoutColor-	
4	MFBZ00	Filter	MFBZ0026701	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MPBG00	Damper, LCD	MPBG0113901	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAB00	Tape, Protect	MTAB0445801	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAB01	Tape, Protect	MTAB0445901	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAB02	Tape, Protect	MTAB0450201	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAD00	Tape, Window	MTAD0134601	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MWAC00	Window, LCD	MWAC0153001	COMPLEXLG-C100IDNRDZZ:WithoutColorCUTTING,PMMAMR200,,,,,	
3	ACGM00	Cover Assembly, Rear	ACGM0175301-22	LG-C105ZAFDRD:RedC105RearAssy,Red	
4	MBJZ00	Button	MBJZ0043101	COMPLEXLG-C100IDNRDRD:RedCOMPLEX,(empty),,,,,	
4	MCCZ01	Cap	MCCZ0045301	COMPLEXLG-C100IDNRDRD:RedCOMPLEX,(empty),,,,,	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
4	MCCZ00	Cap	MCCZ0045501	COMPLEXLG-C100IDNRDZZ:WithoutColorMOLD,UrethaneRubberS190A,, ,,	
4	MCCZ02	Cap	MCCZ0045901	COMPLEXLG-C100IDNRDZZ:WithoutColorMOLD,UrethaneRubberS190A,, ,,	
4	MCCZ03	Cap	MCCZ0046001	COMPLEXLG-C100IDNRDRD:RedCOMPLEX,(empty),,,,,	
4	MCJN00	Cover,Rear	MCJN0128201	COMPLEXLG-C100IDNRDRD:RedMOLD,PCLUPOYSC-1004A,,,,,	
4	MFBZ00	Filter	MFBZ0029701	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MJN061101	Tape,Protect	MJN67687901	COMPLEXLGC100.AIDNRDZZ:WithoutColor-	
4	MLAB	Label,AfterService	MLAB0001102	COMPLEXC2000CGRSVWA:WhiteC2000USASVDIA4.0PRINTING,	
4	MPBN00	Damper,Speaker	MPBN0092201	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MPBZ00	Damper	MPBZ0326401	COMPLEXLG-C100IDNRDZZ:WithoutColorMOLD,UrethaneRubberS190A,, ,,	
4	MPBZ01	Damper	MPBZ0329901	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MPBZ02	Damper	MPBZ0337501	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAB00	Tape,Protect	MTAB0427601	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MTAD00	Tape,Window	MTAD0134701	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MJN000000	Tape	MTAZ0352901	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
4	MWAE00	Window,Camera	MWAE0065801	COMPLEXLG-C100IDNRDZZ:WithoutColorCUTTING,PMMAMR200,,,,,	
3	GMZZ00	Screw,Machine	GMZZ0017701	GMZZ0017701BH+1.4mM3mMMSWRNIPLTN-ASIABOLT	
5	ACKA00	CanAssembly,Shield	ACKA0033301	LG-C100IDNRDZZ:WithoutColor-	
6	MCBA00	Can,Shield	MCBA0097701	COMPLEXLG-C100IDNRDZZ:WithoutColorPRESS,STS,,,,,	
6	MTAB00	Tape,Protect	MTAB0439401	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
5	ADCA00	DomeAssembly,Metal	ADCA0119101	LG-C100IDNRDZZ:WithoutColor-	
5	MEZ000900	Label,AfterService	MLAB0000601	COMPLEXKE520ORFBKZZ:WithoutColorPRINTING,PPRIPRINTING	
5	MTAZ00	Tape	MTAZ0358301	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
5	MTAZ01	Tape	MTAZ0358401	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
5	MTAZ02	Tape	MTAZ0377101	COMPLEXLG-C100IDNRDZZ:WithoutColorCOMPLEX,(empty),,,,,	
5	MLAZ00	Label	MLAZ0038301	COMPLEXLG-VX6000ZZ:WithoutColorPIDLabel4ArrayPRINTING,	
6	SC200	Can,Shield	MCBA0059201	COMPLEXGD350CLPZZ:WithoutColor-	
6	CN400	Contact	MCIZ0004401	COMPLEXLG-C300FRAZZ:WithoutColor-	
2	MLAA00	Label,Approval	MLAA0062320	COMPLEXGU280OREBKZZ:WithoutColorCOMPLEX,(empty) ,,,,,	

13. EXPLODED VIEW & REPLACEMENT PART LIST

13.2 Replacement Parts <Main component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
4	ENZY00	Connector, TerminalBlock	ENZY0019901	HSBC-3P-583P3.00MMSTRAIGHTSMDR/TP-HANSHINTERMINALCO.,LTD.	
4	SJMY00	Motor,DC	SJMY0007905	DM-YK407-6F23V80mA0A11KRPM0RPM0SEC0GF.CM0OHMDONGYANGCHENGJICO.	
4	SNGF00	Antenna,Helical	SNGF0064402	HIR-02A37-0000AA3.0,-2dBd,GSMQuad,CarrierType,QUAD,-2.0,50,3.0E.M.WCO.,LTD.	
4	SNGF01	Antenna,Helical	SNGF0064502	HIR-02A48-0000AA3.0,-5dBd,FMintenna,FPCBtype,SINGLE,-5.0,50,3.0E.M.WCO.,LTD.	
4	SUSY00	SpeakerModule	SUSY0024805	16-8T-07PP16-8T-07PP,PIN,8ohm,91dB,16mm,3.4Tspring0.9WKIRYNTELECOMCO.,LTD	
3	SAFY00	PCBAssembly,Main	SAFY0389207 2	LGC105.ACLRRDMAIN1.0	
4	EBR071500	PCBAssembly,Main,Insert	SAFB0126701 10	LG-C100IDNRDMAIN1.1	
5	SPKY00	PCB,Sidekey	SPKY0095101	SPKY0095101LG-C100IDNRD,SIDEKEY,C,POLYI,0.2mm,DOUBLE,LG-C100SIDEKEYLGInnotek.com	
5	EAB010400	Receiver	SURY0015701	BWBR1207L-04C-PASSY,dB,32ohm,13.2*8.2*5.4,RubberUnifiedTypeRCV,WIRE,BUJEONELECTRONICSCO.,LTD	
5	SVCY00	CameraModule	SVCY0022901	C1FK-Z238AC1FK-Z238A1.3M,Siliconfile(1/5"),7x7x4.1t,SocketLGINNOTEKCO.,LTD	
5	SVLM00	LCD,Module-TFT	SVLM0036102	GPM1031A0Main,2.2",176*220,39.848*52.95*1.9t,262K,TFT,TM,ILI9225B,GIANTPLUSTECHNOLOGYCO.,LTD.	
4	SAFF00	PCBAssembly,Main,SMT	SAFF0289311 4	LGC105.ACLRRDMAIN1.0	
5	SAFC00	PCBAssembly,Main,SMTBottom	SAFC0162001 126	LG-C105MAIN1.0	
6	C454	Capacitor,Ceramic,Chip	ECCH0000104	MCH155A030C3pF0.25PF50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C456	Capacitor,Ceramic,Chip	ECCH0000108	MCH155A070DK7pF0.25PF50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C323,C324,C325,C326,C327,C328,C329,C330,C331,C332,C333,C334,C335,C336,C411,C416	Capacitor,Ceramic,Chip	ECCH0000110	MCH155A100D10pF0.25PF50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C258	Capacitor,Ceramic, Chip	ECCH0000112	MCH155C150J15pF5%50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C109	Capacitor,Ceramic, Chip	ECCH0000113	MCH155A180J18pF5%50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C144,C145, C302,C305, C441,C442	Capacitor,Ceramic, Chip	ECCH0000115	MCH155A220JK22pF5%50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C201,C309	Capacitor,Ceramic, Chip	ECCH0000117	CL05C270JB5NNNC27pF5%50VNP0-55TO+125C1005R/TP0.5SAMSUNGELECTRO-MECHANISCO.,LTD.	
6	C204,C209, C214,C215, C249,C403	Capacitor,Ceramic, Chip	ECCH0000120	MCH155A390J39pF5%50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C206,C207, C223,C224, C234,C235	Capacitor,Ceramic, Chip	ECCH0000122	MCH155A470JK47pF5%50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C135,C136, C146,C200, C308,C400, C401,C402, C404,C436, C437,C444, C452	Capacitor,Ceramic, Chip	ECCH0000143	MCH155CN102KK1nF10%50VX7R-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C241	Capacitor,Ceramic, Chip	ECCH0000145	MCH155CN152KK1.5nF10%50VX7R-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C111,C128	Capacitor,Ceramic, Chip	ECCH0000151	CL05B472KB5NNNC4.7nF10%25VX7R-55TO+125C1005R/TP-SAMSUNGELECTRO-MECHANISCO.,LTD.	
6	C239,C240, C242,C405, C406,C414	Capacitor,Ceramic, Chip	ECCH0000155	MCH153CN103KK10nF10%16VX7R-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C229,C231	Capacitor,Ceramic, Chip	ECCH0000179	GRM155R71C223K22nF10%16VX7R-55TO+85C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C203,C233, C254	Capacitor,Ceramic, Chip	ECCH0000182	GRM155R61A104K0.1uF10%10VX5R-55TO+85C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C457	Capacitor,Ceramic, Chip	ECCH0000185	GRM1555C1H5R6C5.6pF0.25PF50VNP0-55TO+125C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	L420	Capacitor,Ceramic, Chip	ECCH0000196	MCH155A0R75C0.75pF0.25PF50VNP0-55TO+125C1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	C120,C132	Capacitor,Ceramic, Chip	ECCH0000198	CL05A225MQ5NSNC2.2uF20%6.3VX5R-55TO+85C1005R/TP.SAMSUNGELECTRO-MECHANISCO.,LTD.	
6	C125,C127, C221,C222	Capacitor,Ceramic, Chip	ECCH0002001	C1005JB0J104KT000F0.1uF10%6.3VY5P-30TO+85C1005R/TP-TDKCORPORATION	
6	C112,C113	Capacitor,Ceramic, Chip	ECCH0002002	C1005X7R1A473KT000F47000pF10%10VY5P-30TO+85C1005R/TP-TDKCORPORATION	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C108,C114, C124,C126, C130,C142, C245,C306, C307,C313, C314,C337, C443	Capacitor,Ceramic, Chip	ECCH0004904	GRM155R60J105K1uF10%6.3VX5R-55TO+85C1005R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C100,C107, C225,C226, C227,C228, C230,C232, C244,C311, C318,C410, C412,C413	Capacitor,Ceramic, Chip	ECCH0005603	GRM188R61A225K2.2uF10%10VX5R-55TO+85C1608R/TP-MURATAMANUFACTURINGCO.,LTD.	
6	C205	Capacitor,Ceramic, Chip	ECCH0005604	GRM188R60J106M10000000pF,6.3V,M,X5R,TC,1608,R/TP,0.8mmMURATAMANUFACTURINGCO.,LTD.	
6	C202,C247, C408	Capacitor,Ceramic, Chip	ECCH0007802	CV105X5R475M10AT4.7uF20%10VX5R-55TO+85C1608R/TP-KYOCERACORP.	
6	C123	Capacitor,Ceramic, Chip	ECCH0007803	CL10A106MP8NNNC10uF20%10VX5R-55TO+85C1608R/TP0.8MMSAMSUNG-ELECTRO-MECHANISCO.,LTD.	
6	C250,C255, C256	Capacitor,TA, Conformal	ECTH0002002	F981A336MSA33F20%10V3.3A-55TO+85C60HM2.2X1.1X1.1MM-SMDR/TPNICHICONCORPORATION,EASTJAPANSALESO FFICE	
6	C420,C435, L417	Capacitor,Ceramic, Chip	ECZH0000802	C1005C0G1H010CT1pF0.25PF50VNP0-55TO+125C1005R/TP-TDKKOREACOOOPERATION	
6	C118	Capacitor,Ceramic, Chip	ECZH0000806	C1005C0G1H050CT000F5pF0.25PF50VNP0-55TO+125C1005R/TP-TDKKOREACOOOPERATION	
6	C424,C431, C455	Capacitor,Ceramic, Chip	ECZH0000813	C1005C0G1H101JT100pF5%50VNP0-55TO+125C1005R/TP-TDKKOREACOOOPERATION	
6	C246,C407	Capacitor,Ceramic, Chip	ECZH0000830	C1005C0G1H330JT000F33pF5%50VNP0-55TO+125C1005R/TP-TDKKOREACOOOPERATION	
6	C119	Capacitor,Ceramic, Chip	ECZH0001210	C1005Y5V1A474ZT000F470nF-20TO+80%10VY5V-30TO+85C1005R/TP-TDKKOREACOOOPERATION	
6	C212,C219, C220,C253, C301,C310, C312,C319, C320,C321, C322	Capacitor,Ceramic, Chip	ECZH0001215	C1005X5R1A105KT000F1uF10%10VX5R-55TO+85C1005R/TP-TDKKOREACOOOPERATION	
6	C105,C110, C141	Capacitor,Ceramic, Chip	ECZH0001216	C1005X5R1A224KT000E220nF10%10VX5R-55TO+85C1005R/TP-TDKKOREACOOOPERATION	
6	C102,C103, C445	Capacitor,Ceramic, Chip	ECZH0001217	GRM155R60J474K470nF10%6.3VX5R-25TO+70C1005BK-DUP-MURATAMANUFACTURINGCO.,LTD.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	C101,C104, C106,C115, C116,C117, C131,C134, C208,C211, C237,C248, C251,C300, C303,C315, C316,C317	Capacitor,Ceramic, Chip	ECZH0003103	GRM36X7R104K10PT100nF10%10VX7R- 55TO+125C1005R/TP- MURATAMANUFACTURINGCO.,LTD.	
6	C252	Capacitor,Ceramic, Chip	ECZH0003503	GRM188R61E105K1uF10%25VX5R-55TO+85C1608R/TP- MURATAMANUFACTURINGCO.,LTD.	
6	C238	Capacitor,Ceramic, Chip	ECZH0003504	GRM188R71E104K100nF10%25VX7R- 55TO+125C1608R/TP- MURATAMANUFACTURINGCO.,LTD.	
6	C121	Capacitor,Ceramic, Chip	ECZH0025502	GRM219R60J226M0.000022F20%6.3VX5R- 55TO+85C2012R/TP0.85MMMURATAMANUFACTURINGCO.,LTD.	
6	ZD100, ZD200, ZD300, ZD301, ZD302	Diode,TVS	EDTY0010101	ESD9B5.0ST5GESD9B5.0ST5G,SOD- 923,5V,300mW,R/TP,15pFSCGHONGKONGSARLTD.	
6	L409	Inductor,Multilayer, Chip	ELCH0001032	HK100518NJ- T18NH5%0V8A3.1GOHM350mHZ300mNONSHIELD11.0X0.5X0.5MMR/TPTAIYOYUDENCO.,LTD	
6	L404	Inductor,Multilayer, Chip	ELCH0001404	LL1005- FHL1N5S_1.5NH0.3NH0V500mA0.13OHM12GHZ8NONSHIELD11.0X0.5X0.5MMR/TPTOKO,INC.	
6	L419	Inductor,Multilayer, Chip	ELCH0001426	LL1005- FHL8N2J8.2NH5%0V400mA0.25OHM4GHZ9NONSHIELD11.0X0.5X0.5MMR/TPTOKO,INC.	
6	L201	Inductor,Multilayer, Chip	ELCH0001430	LL1005- FHLR10J100NH5%0V200mA2.2OHM870MHZ10NONSHIELD11.0X0.5X0.5MMR/TPTOKO,INC.	
6	L412	Inductor,Multilayer, Chip	ELCH0003818	LQG15HS9N1J02D9.1NH5%0V300mA0.26OHM3.4GHZ8NONSHIELD11.0X0.5X0.5MMR/TPMURATAMANUFACTURINGCO.,LTD.	
6	L400,L401	Inductor,Multilayer, Chip	ELCH0003826	LQG15HS3N3S02D3.3NH0.3NH0V300mA0.17OHM6GHZ8NONSHIELD11.0X0.5X0.5MMR/TPMURATAMANUFACTURINGCO.,LTD.	
6	L200,L204, L205	Inductor,Multilayer, Chip	ELCH0003842	LQG15HSR10J02100NH5%- 150mA1.25OHM600HZ8SHIELD11.0X0.5X0.55MMR/TPMURATAMANUFACTURINGCO.,LTD.	
6	L407,L410	Inductor,Multilayer, Chip	ELCH0004720	1005GC2T1N2S001.2NH0.3NH0V300mA0.12OHM9GHZ8NONSHIELD11.0X0.5X0.5MMR/TPPILKORELECTRONICSLTD.	
6	C453,L408	Inductor,Multilayer, Chip	ELCH0005001	HK10052N2S2.2NH0.3NH0V8A10GOHM70mHZ300mNONSHIELD11.0X0.5X0.5MMR/TPTAIYOYUDENCO.,LTD	
6	L413	Inductor,Multilayer, Chip	ELCH0005004	HK100522NJ22NH5%0V8A2.8GOHM420mHZ300mNONSHIELD11.0X0.5X0.5MMR/TPTAIYOYUDENCO.,LTD	
6	L415,L416	Inductor,Multilayer, Chip	ELCH0010402	LK1005R27-TLK1005R27- T,270nH,M,1005,R/TP,CHIPTAIYOYUDENCO.,LTD	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	L100	Inductor,WireWound,chip	ELCP0009410	LQM2HPN3R3MG0LQM2HPN3R3MG0,3.3uH,N,2x2.5x1.0,R/TP,chippowerMURATAMANUFACTURINGCO.,LTD.	
6	J200	Jack,Phone	ENJE0008001	JAM3333-F32-7F1P4PANGLER/TP4mMBLACK6P-HONHAIPRECISIONINDUSTRYCO.,LTD.	
6	CN303	Connector,FFC/FPC/PIC	ENQY0013901	04-6293-635-005-829+35P0.30MMFPCANGLEBOTHSMR/TPLOCKINGFLIPTYPEKYOCERAELCOKOREASALESCO.,LTD.	
6	CN202	connector,I/O	ENRY0008801	GU073-5P-SD-E1500GU073-5P-SD-E1500,5,mm,ANGLELSMtronLtd.	
6	J300	CardSocket	ENSY0022102	GCA26A-6S-H16-M-E1000SIM6PANGLESMDR/TP-LSMtronLtd.	
6	CN302	CardSocket	ENSY0023701	SD-105076-001Camera24PSTRAIGHTSMR/TP-HANKOOKMOLEX	
6	S200	Socket,Card	ENSY0023802	SCHB1B0201Micro-SD8PANGLESMDR/TP-ALPSELECTRICKOREACO.,LTD.	
6	SW400	connector,RF	ENWY0007601	NMS-306NMS-306,SMD,dBNAMAELECTRONICSINC	
6	Q400	TR,Bipolar	EQBN0019201	KTC3770VVSMD,0.1W,R/TP,1.2*1.2*0.5Vcbo=20,Vceo=12,Vebo=2V,Ic=100mAKECCORPORATION	
6	Q100,Q300	TR,Bipolar	EQBN0020501	KTC4075ENPN5V60V50V150mA100NA700100mWESMR/TP3PKECCORPORATION	
6	Q200	FET	EQFP0007601	KTJ6131EP-CHANNELMOSFET-30V+-20-0.05A200HM100mWESMR/TP3PKECCORPORATION	
6	R213	Resistor,Chip	ERHY0000140	MCR01MZIP5F360236KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R131,R235, R247,R326, R338,R401	Resistor,Chip	ERHY0000241	MCR01MZIP5J1021KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R123	Resistor,Chip	ERHY0000254	MCR01MZIP5J4724.7KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R127,R215, R340,R348	Resistor,Chip	ERHY0003301	MCR01MZIP5J101100OHM5%1/16W1005R/TP-ROHM.	
6	R238,R239	Resistor,Chip	ERHY0003601	MCR01MZIP5J2722.7KOHM5%1/16W1005R/TP-ROHM.	
6	R100,R110, R112,R115, R117,R118, R236,R341, R342,R345	Resistor,Chip	ERHZ0000204	MCR01MZIP5F1003100KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R106,R234	Resistor,Chip	ERHZ0000206	MCR01MZIP5F10R010OHM0.1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R300	Resistor,Chip	ERHZ0000213	MCR01MZIP5F1203120KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R206,R207	Resistor,Chip	ERHZ0000240	MCR01MZIP5F20R020OHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R237	Resistor,Chip	ERHZ0000278	MCR01MZIP5F39013.9KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R232	Resistor,Chip	ERHZ0000295	MCR01MZIP5F510251KOHM1%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	R245	Resistor,Chip	ERHZ0000402	MCR01MZIP5J10010OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R122	Resistor,Chip	ERHZ0000405	MCR01MZIP5J10310KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R125,R126, R128,R132, R225,R231, R240,R246, R327,R336, R337,R339, R343,R419	Resistor,Chip	ERHZ0000406	MCR01MZIP5J104100KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R120,R121, R214,R244	Resistor,Chip	ERHZ0000407	MCR01MZIP5J1051MOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R411	Resistor,Chip	ERHZ0000422	MCR01MZIP5J15315KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R344	Resistor,Chip	ERHZ0000423	MCR01MZIP5J154150KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R102,R103, R222,R223	Resistor,Chip	ERHZ0000434	MCR01MZIP5J1R01OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R101	Resistor,Chip	ERHZ0000439	MCR01MZIP5J204200KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R129,R130, R209,R217, R224	Resistor,Chip	ERHZ0000443	MCR01MZIP5J2222.2KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R216	Resistor,Chip	ERHZ0000445	MCR01MZIP5J224220KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R415	Resistor,Chip	ERHZ0000449	MCR01MZIP5J24324KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R219,R221	Resistor,Chip	ERHZ0000451	MCR01MZIP5J27027OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R319,R320	Resistor,Chip	ERHZ0000465	MCR01MZIP5J3323.3KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R416	Resistor,Chip	ERHZ0000469	MCR01MZIP5J36036OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R109	Resistor,Chip	ERHZ0000475	MCR01MZIP5J3923.9KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R108,R317, R318,R321, R322,R323, R324,R325, R328,R329, R330,R331, R332,R333, R334	Resistor,Chip	ERHZ0000484	MCR01MZIP5J471470OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R335,R417	Resistor,Chip	ERHZ0000485	MCR01MZIP5J4724.7KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R226,R227, R228,R229, R230	Resistor,Chip	ERHZ0000486	MCR01MZIP5J47347KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R233	Resistor,Chip	ERHZ0000488	MCR01MZIP5J4R74.7OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	R111	Resistor,Chip	ERHZ0000499	MCR01MZIP5J5625.6KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R208	Resistor,Chip	ERHZ0000529	MCR01MZIP5J1521.5KOHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R301,R302, R303,R304, R305,R306, R307,R308, R309,R310, R311,R312, R349,R350	Resistor,Chip	ERHZ0000531	MCR01MZIP5J271270OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	R414	Resistor,Chip	ERHZ0003801	MCR01MZIP5J5R15.1OHM5%1/16W1005R/TP-ROHMSemiconductorKOREACORPORATION	
6	U300	IC,BusController	EUSY0300008	PP2106M31.8/2.6V1mA-MLFR/TP28P-G5CORPORATION	
6	U301	IC,ChargePump	EUSY0344402	RT9367CQFN,20,R/TP,4CH,2LDO,3X3,IC,SubPMICIC,SubPMICRICHEKTEKTECHNOLOGYCORP.	
6	U100	IC,MCP,NOR	EUSY0368502	PF38F5060M0Y3DFNOR/512PSRAM/1281.7VTO1.95V8x8x1TR56PNOR+PSRAMFBGA-NumonyxAsiaPacificPteLtd.	
6	U302	IC,LDOVoltageRegulator	EUSY0369401	RP103K151DRP103K151D,PLP1010,4,R/TP,150mALDORIC OHCOMPANY,LTD.	
6	U401	IC,Bluetooth	EUSY0382201	BCM2070CB0KUFGBXGBCM2070CB0KUFGBXG,FPBGA,50,R/TP,4.5x4.0x0.6,BT2.1BROADCOMASIA DISTRIBUTIONPTE LTD	
6	U200	IC,AudioSubSystem	EUSY0403901	WM9093ECS/R1.71~5.5V0WWLCSPR/TP20P-WOLFSONMICROELECTRONICSPLC	
6	U202	IC,AnalogMultiplexer	EUSY0406901	RT8962WSWLCSP,20,R/TP,MUIC-Basic,2X2.5,IC,AnalogSwitchIC,AnalogSwitchRICHEKTEKTECHNOLOGYCORP.	
6	U102,U201	IC,TTL	EUSY0407701	LMV3312.7~5.5V-COMPARATORSC70R/TP5P-TEXASINSTRUMENTSKOREALTD,HONGKONGBRANCH.	
6	U204	IC,VoltageReference	EUSY0410801	RT9524DFN,10,R/TP,DFNCalTestModeSingleChargerICforMicroUSB,IC,ChargerIC,ChargerRICHEKTEKTECHNOLOGYCORP.	
6	U101	IC,DigitalSignalProcessors	EUSY0421201	PMB8810000NONENONEBGAR/TP217P-INFINEONTECHNOLOGIES(ASIAPACIFIC)PTELTD.	
6	X101	Crystal	EXXY0004602	MC-146(12.5PF,+/-20PPM)32.768KHZ20PPM12.5PF69*14SMDR/TPSEIKOEPS ONCORP	
6	X100	Crystal	EXXY0027001	DSX321G-26M(8PF)26MHZ10PPM0FNONESMDR/TPDAISHINKUCORPORATION.	
6	R133,R134, R220,R241, R248,R410	WirePad,Short	SAFP0000501	LG-VS760VRZ	
6	PT100	Thermistor,NTC	SETY0006301	NCP15XH103J03RC10KOHM5%0V0A3.35KKSMDP/TP1005sizeMURATAMANUFACTURINGCO.,LTD.	
6	VA206, VA207	Varistor	SEVY0003601	ICVL0505101V150FR5.6V0%60F1.0*0.5*0.55NONESMDR/T PINNOCHIPTECHNOLOGY	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	VA100, VA200, VA201, VA202, VA203, VA204, VA205, VA208, VA209, VA210, VA314, VA315, VA316, VA317, VA318	Varistor	SEVY0004301	ICVL0518100Y500FR18V0%10F1.0*0.5*0.55NONESMDR/T PINNOCHIPSTECHNOLOGY	
6	FB400	Filter,Bead	SFBH0000903	HB-1M1005- 601JT600ohm1.0*0.5*0.5SMDR/TP2PCERATECHCORPOR ATION	
6	FB205	Filter,Bead	SFBH0000912	HB-1M1005- 102JT1000ohm1.0*0.5*0.5SMDR/TP2PCERATECHCORPO RATION	
6	FB100, FB109	Filter,Bead	SFBH0007103	BLM15BB750SN1J75ohm1.0x0.5x0.55SMDR/TP2PMURATA MANUFACTURINGCO.,LTD.	
6	FB101, FB102, FB103, FB104, FB105, FB106, FB200, FB201, FB202, FB203, FB204, FB209, R210	Filter,Bead	SFBH0008105	BLM15BD182SN1D1800ohm;1.0x0.5x0.55SMDR/TP2PMUR ATAMANUFACTURINGCO.,LTD.	
6	FL400	Filter,Dielectric	SFDY0003001	DEA202450BT-1275A1DEA202450BT- 1275A1,2450MHz,2.0*1.25*1.05,SMD,2400M~2500M,IL1.6,4 pin,U-U,50-50,BTBPFTDKCORPORATION	
6	FL200	Filter,EMI/Power	SFEY0007101	ICVFP10181E301FRES/EMI0HZ300pF0HSMDR/TPINNOC HIPSTECHNOLOGY	
6	FL302, FL304, FL305	Filter,EMI/Power	SFEY0013201	EVRC14S03Q030100RES/EMI0HZ15pF0HSMDR/TPAMO TECHCO.,LTD.	
6	FL300, FL301, FL303	Filter,EMI/Power	SFEY0015501	ICVE10184E050R101FRES/EMI550HZ10F0HSMDR/TPIN NOCHIPSTECHNOLOGY	
6	FL402	Filter,Saw,Dual	SFSB0001803	SAWEN881MBK0F00881.5MHz,942.5MHz1.8*1.4*0.5SMDR /TP10PMURATAMANUFACTURINGCO.,LTD.	
6	FL401	Filter,Saw,Dual	SFSB0001903	SAWEN1G84BK0F001842.5MHz,1960MHz1.8*1.4*0.5SMD R/TP10PMURATAMANUFACTURINGCO.,LTD.	
6	U400	RFModule	SMRH0005601	SKY77547MHz,MHz,GSMQuadTxModule6x8,SKYWORKSS OLUTIONSINC.	

13. EXPLODED VIEW & REPLACEMENT PART LIST

Level	LocationNo.	Description	PartNumber	Spec	Remark
6	BAT100	CapacitorAssembly	SMZY0023501	PAS311HR-VG13.8BackupCapacitor0.03F,ModuleAssembly,KOREATAIYOYUDEN.CO.,LTD.	
6	MIC200	Microphone, Condenser	SUMY0010609	SPU0410HR5H-PBSPU0410HR5H-PB,UNIT,42dB,3.76*2.95*1.1,memssmdmicKNOWLESACOUSTICS	
5	EBR071700	PCBAsembly, Main,SMTTop	SAFD0153601 2	LG-C100IDNRDMAIN,1.0	
6	LD300, LD301, LD302, LD303, LD304, LD305, LD306, LD307, LD308, LD309, LD310, LD311, LD312, LD313	LED,Chip	EDLH0011901	SSC-TWH104-HLWHITE2.7~3.120mA100~220mcdX(0.24~0.34)Y(0.25~0.34)66mW1608R/TP2P-SEOULSEMICONDUCTORCO.,LTD	
6	SPFY00	PCB,Main	SPFY0237601	SPFY0237601LG-C100IDNRD,MAIN,D,FR-4,1mm,BUILD-UP6,C100MAINLGInnotek.com	

13. EXPLODED VIEW & REPLACEMENT PART LIST

13.3 Accessory

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	LocationNo.	Description	PartNumber	Spec	Remark
2	SBPL00	Rechargeable Battery, Lithium Ion	SBPL0091404	LGIP-531A-LA-SANYO LGIP-531A-LA-SANYO, 3.7V, 950mAh, 1CELL, PRISMATIC, 553450 Latin America TOCADDONGHWA	
2	SGDY00	Accessory, Data Cable	SGDY0018001	LG0029 LG0029 Micro USB, 0.8M Ningbo broad telecommunications co., Ltd	
2	SGEY00	Earphone, Stereo	SGEY0003219	EMB-LGE001STKE, BLACK, 4POLE PLUG, 3.54, Earphone, Stereo C RESYNCO., LTD	
2	EAY060000	Adapters	SSAD0037101	STA-U35BR100-240V, 5060Hz, 4.8V, .4A, ANATEL, AC-DC ADAPTOR, 90Vac~264Vac, 4.8Vdc, 400mA, 5060, WALL2P, USB, -, 90Vac~264Vac, 4.8Vdc, 400mA, 5060, WALL2P, USB, - SUNLINE ELECTRONICSCO., LTD	
2	EAY060000	Adapters	*S*SSAD0037102	STA-U35BS100-240V, 5060Hz, 4.8V, .4A, ANATEL, AC-DC ADAPTOR, 90Vac~264Vac, 4.8Vdc, 400mA, 5060, WALL2P, USB, -, 90Vac~264Vac, 4.8Vdc, 400mA, 5060, WALL2P, USB, - SALCOMPOY	
2	EAY060000	Adapters	*S*SSAD0037103	STA-U35BD100-240V, 5060Hz, 4.8V, .4A, ANATEL, AC-DC ADAPTOR, 90Vac~264Vac, 4.8Vdc, 400mA, 5060, WALL2P, USB, -, 90Vac~264Vac, 4.8Vdc, 400mA, 5060, WALL2P, USB, - DONGDO ELECTRONICSCO., LTD	