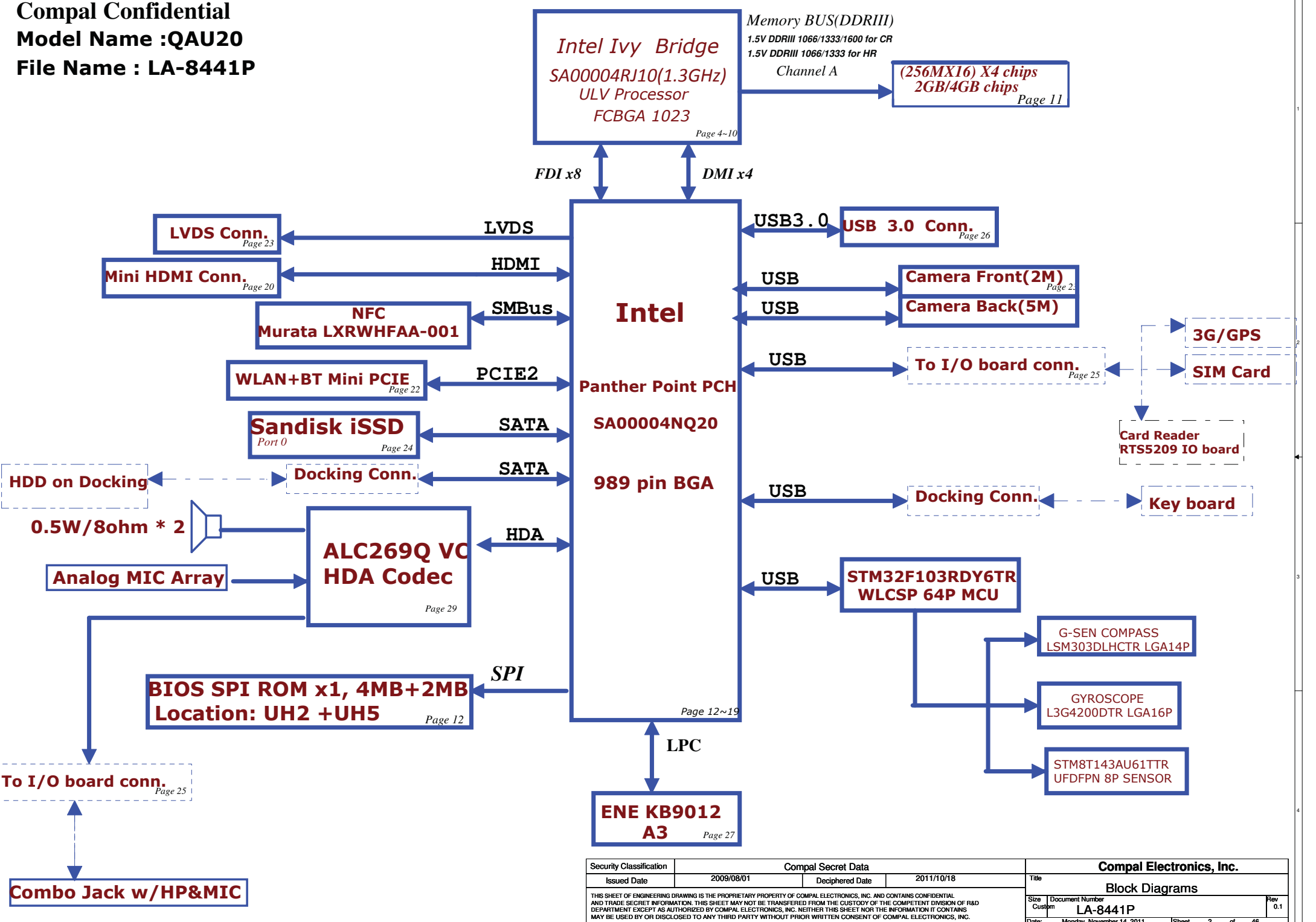


# Compal Confidential

## QAU20 M/B Schematics Document

Date : 2011/11/08

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# QAZ50 (LA-8101P Ver:0.1)

## Voltage Rails 2011/08/19 Modify

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (7.2V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCSA	Voltage for CPU SA RALL	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+CHGRTC	BATT+ or Vin to +CHGRTC always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VCCP	+VCCP (1.05V ) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+LG_OUT	Voltage for LCD Panel Backlight LED Power	ON	OFF	OFF
+1.8VS	(+5VALW ) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	ClOCK
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

### EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

SMBUS Control Table

## 2011/07/28 Modify

	SOURCE	BATT	MINI1 (mSATA)	MINI2 (Wlan1)		EC_SMB_CK2 EC_SMB_DA2	PCH_SMBCLK PCH_SMBDATA
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	X	X		X	X
EC_SMB_CK2 EC_SMB_DA2	KB9012	X	X	X		O	V
PCH_SMBCLK PCH_SMBDATA	PCH	X	V	V		V	O
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X		X	X



CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	m-SATA,JSSD1
SATA1	None
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table 2011/07/12 Check

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	
		1	USB/B ( External)
	UHCI1	2	USB/B ( External)
		3	
	UHCI2	4	Mini Card(WLAN)
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	Test Point (RH274,RH310)
	UHCI5	10	
		11	
		12	
UHCI6	13		

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

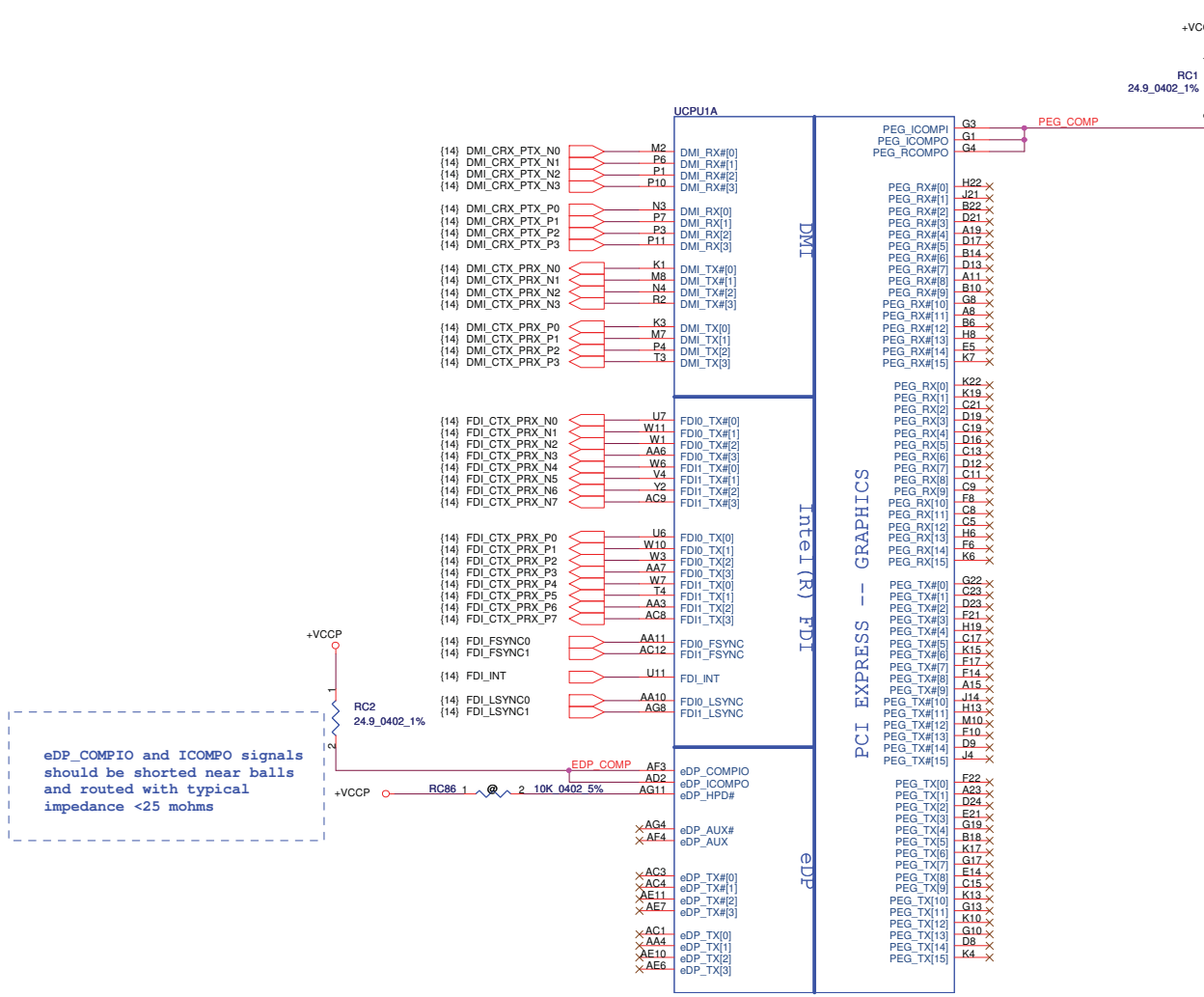
Symbol Note :  
 : means Digital Ground  
 : means Analog Ground

### 2011/08/19 Modify

Option	@	CONN@		
CR UMA	X	X		

USB 3.0	Port	2 External USB Port
	1	
	2	USB/B ( External)
	3	USB/B ( External)
	4	

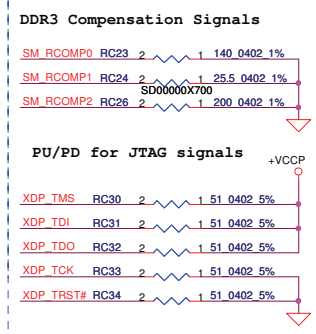
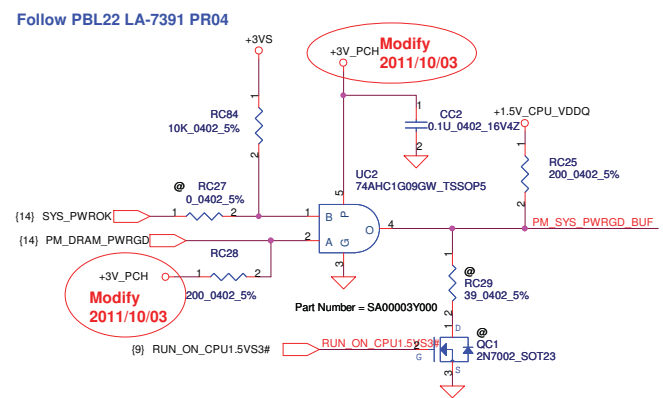
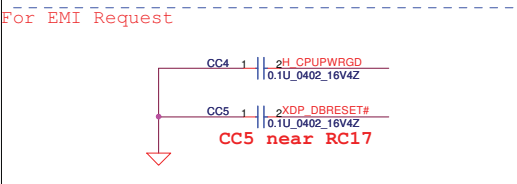
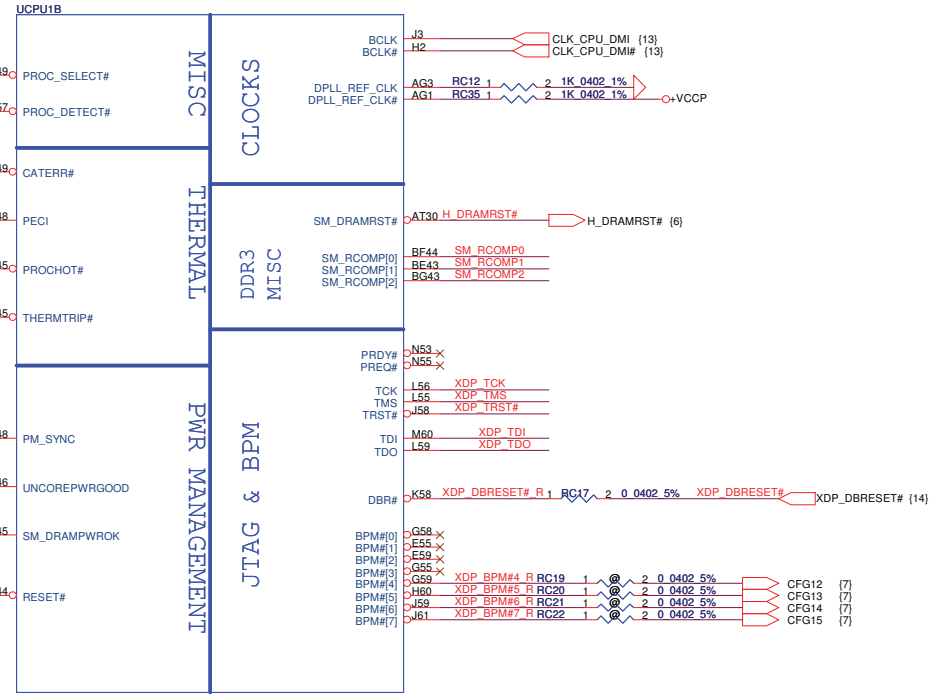
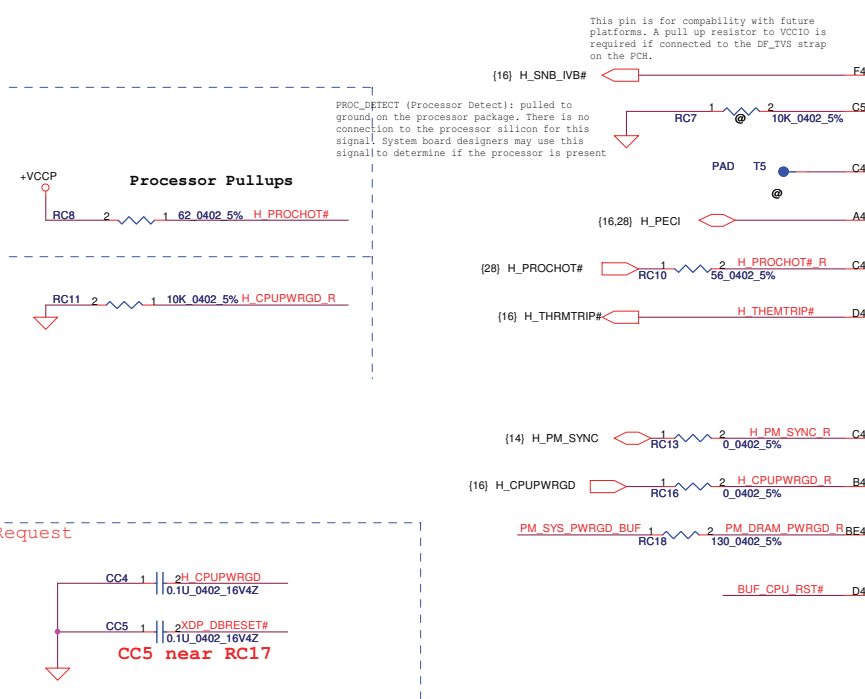
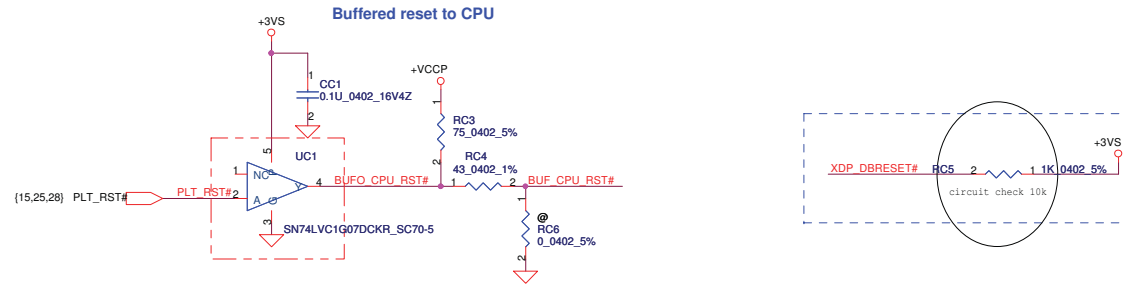
USB/B ( External)



PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

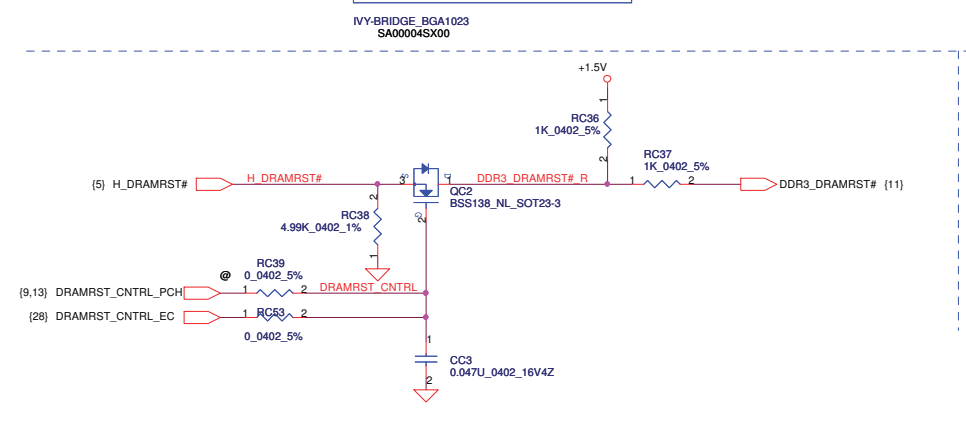
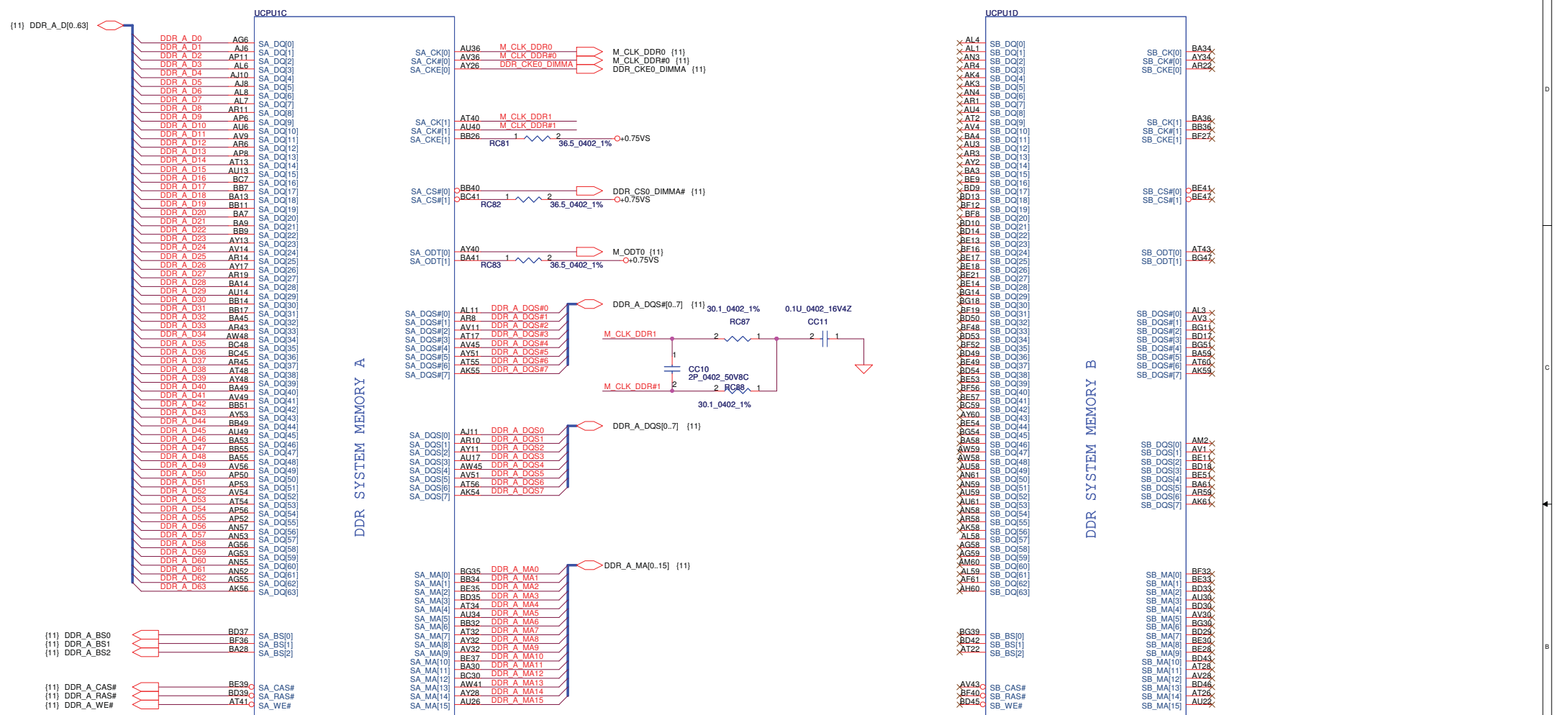
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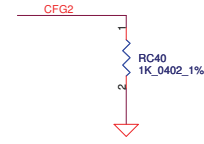
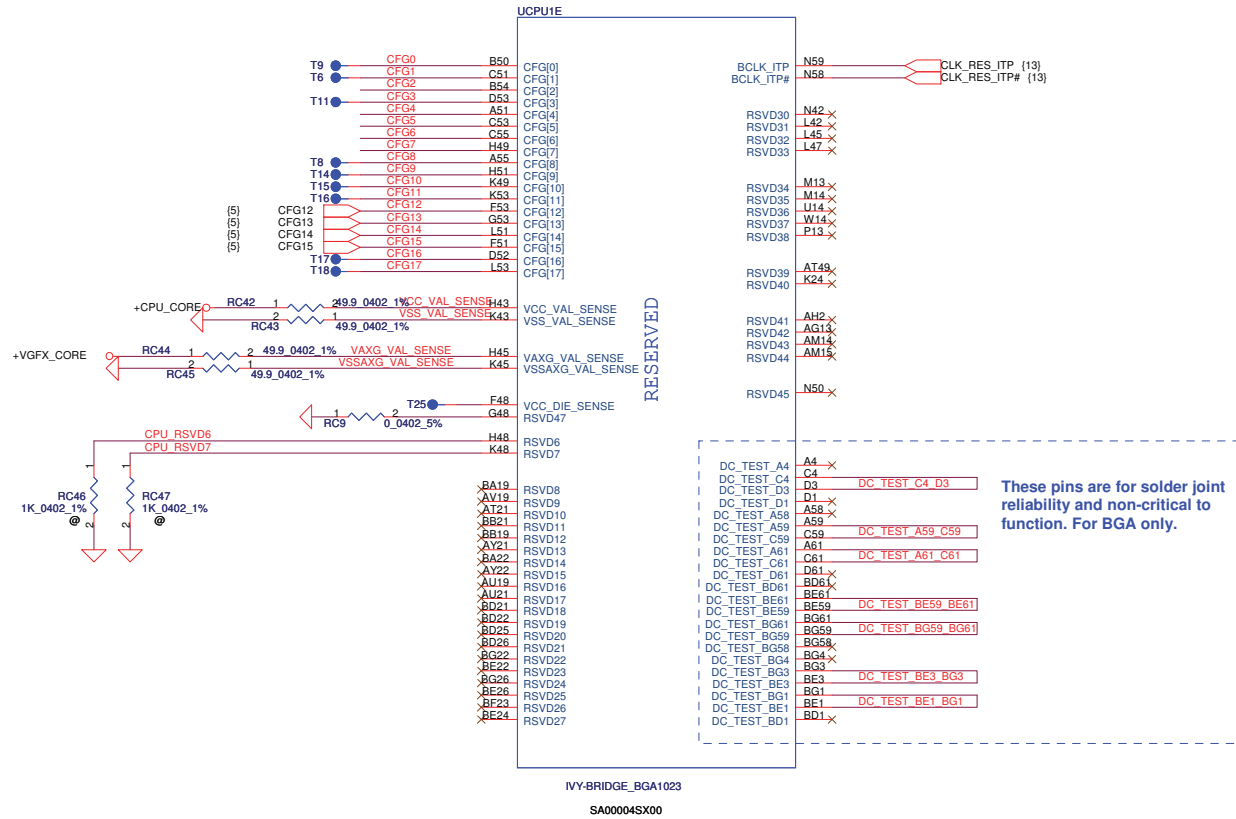
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<b>Compal Electronics, Inc.</b>		
<b>PROCESSOR(2/7) PM,XDP,CLK</b>		
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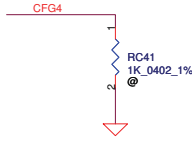


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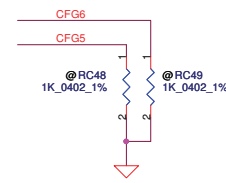
# CFG Straps for Processor



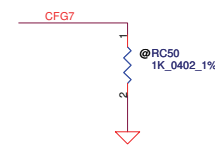
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

ULV type CPU

- CPU\_CORE 28A
- A26 VCC[1]
- A29 VCC[2]
- A31 VCC[3]
- A34 VCC[4]
- A35 VCC[5]
- A38 VCC[6]
- A39 VCC[7]
- A42 VCC[8]
- C26 VCC[9]
- C27 VCC[10]
- C32 VCC[11]
- C34 VCC[12]
- C37 VCC[13]
- C38 VCC[14]
- C42 VCC[15]
- D27 VCC[16]
- D32 VCC[17]
- D34 VCC[18]
- D37 VCC[19]
- D39 VCC[20]
- D42 VCC[21]
- E28 VCC[22]
- E28 VCC[23]
- E32 VCC[24]
- E34 VCC[25]
- E37 VCC[26]
- E38 VCC[27]
- F25 VCC[28]
- F26 VCC[29]
- F28 VCC[30]
- F32 VCC[31]
- F34 VCC[32]
- F37 VCC[33]
- F38 VCC[34]
- F42 VCC[35]
- G42 VCC[36]
- H25 VCC[37]
- H28 VCC[38]
- H28 VCC[39]
- H32 VCC[40]
- H32 VCC[41]
- H34 VCC[42]
- H35 VCC[43]
- H37 VCC[44]
- H38 VCC[45]
- H40 VCC[46]
- J25 VCC[47]
- J26 VCC[48]
- J28 VCC[49]
- J29 VCC[50]
- J32 VCC[51]
- J34 VCC[52]
- J35 VCC[53]
- J37 VCC[54]
- J38 VCC[55]
- J40 VCC[56]
- J42 VCC[57]
- K26 VCC[58]
- K27 VCC[59]
- K29 VCC[60]
- K32 VCC[61]
- K34 VCC[62]
- K35 VCC[63]
- K37 VCC[64]
- K39 VCC[65]
- K42 VCC[66]
- L25 VCC[67]
- L28 VCC[68]
- L33 VCC[69]
- L36 VCC[70]
- L40 VCC[71]
- N26 VCC[72]
- N30 VCC[73]
- N34 VCC[74]
- N38 VCC[75]
- N38 VCC[76]

# POWER

UCPU1F

CORE SUPPLY

PEG IO AND DDR IO

QUIET PULLS

SVID

SENSE LINES

- VCCIO[1] AF46
- VCCIO[3] AG48
- VCCIO[4] AG50
- VCCIO[5] AG51
- VCCIO[6] AJ17
- VCCIO[7] AJ21
- VCCIO[8] AJ25
- VCCIO[9] AJ43
- VCCIO[10] AJ47
- VCCIO[11] AK50
- VCCIO[12] AK51
- VCCIO[13] AL14
- VCCIO[14] AL15
- VCCIO[15] AL16
- VCCIO[16] AL20
- VCCIO[17] AL26
- VCCIO[18] AL45
- VCCIO[19] AL48
- VCCIO[20] AM16
- VCCIO[21] AM17
- VCCIO[22] AM21
- VCCIO[23] AM43
- VCCIO[24] AM47
- VCCIO[25] AN20
- VCCIO[26] AN42
- VCCIO[28] AN45
- VCCIO[29] AN48
- VCCIO[30] AA14
- VCCIO[31] AA15
- VCCIO[32] AB17
- VCCIO[33] AB20
- VCCIO[34] AC13
- VCCIO[35] AD18
- VCCIO[36] AD21
- VCCIO[37] AE14
- VCCIO[38] AE15
- VCCIO[39] AE16
- VCCIO[40] AF18
- VCCIO[41] AF20
- VCCIO[42] AG15
- VCCIO[43] AG16
- VCCIO[44] AG17
- VCCIO[45] AG20
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- VCCIO[48] AJ14
- VCCIO[49] AJ15

+VCCP  
18A

- VCCIO50 W16
- VCCIO51 W17

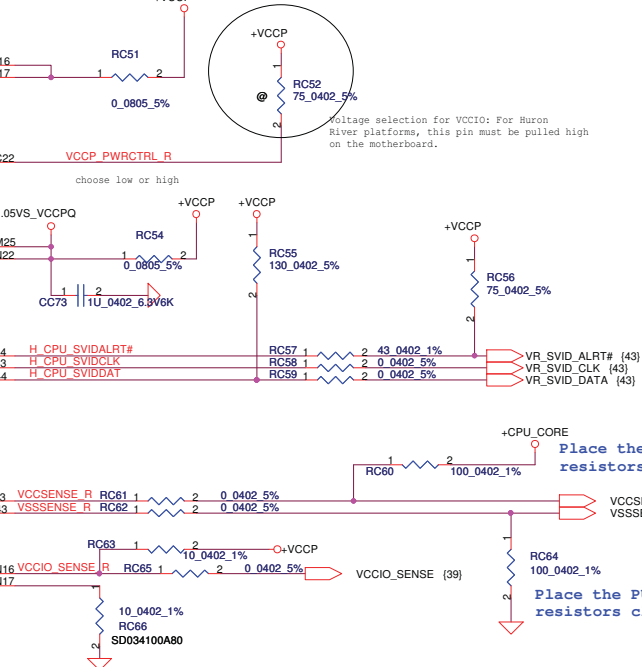
VCCIO\_SEL BC22

- VCCPQE[1] AM25
- VCCPQE[2] AN22

- VIDALERT# A44
- VIDSCLK B43
- VIDSOUT C44

- VCC\_SENSE F43
- VSS\_SENSE G43

- VCCIO\_SENSE AN16
- VSS\_SENSE\_VCCIO AN17



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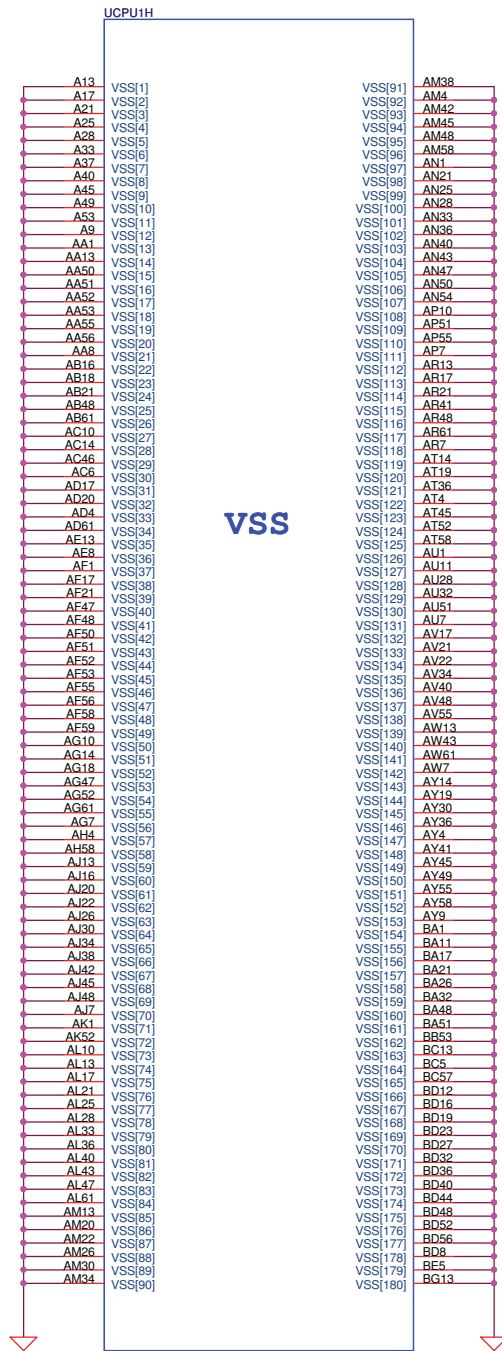
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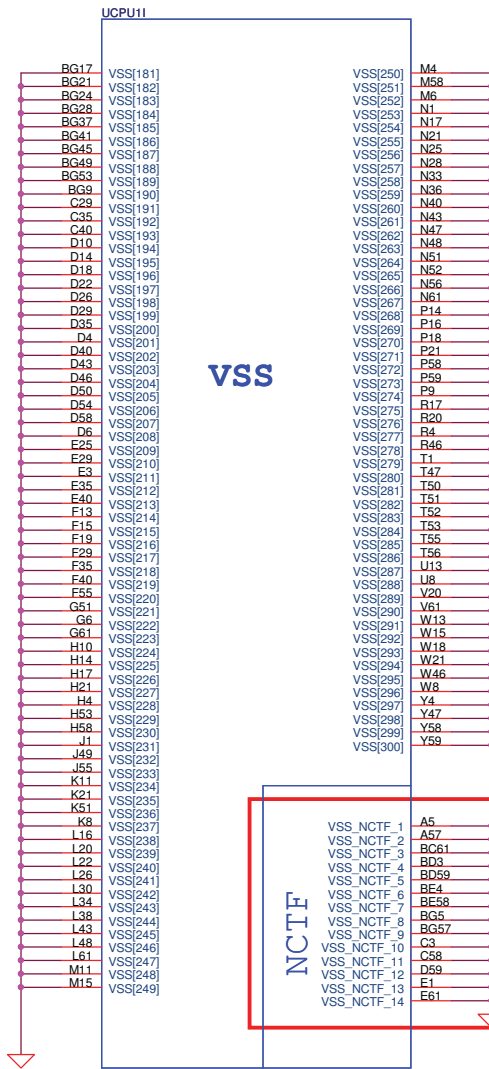
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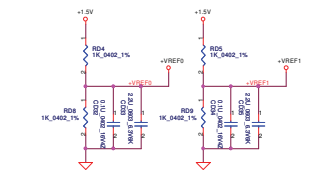
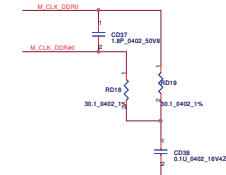
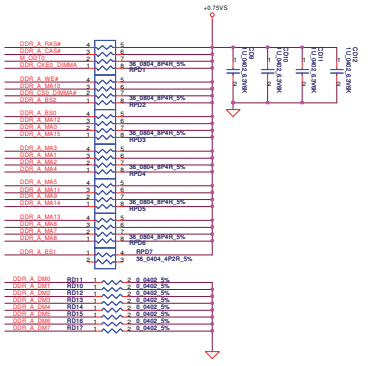
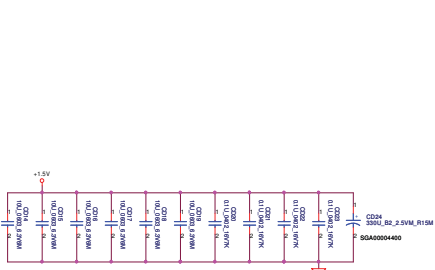
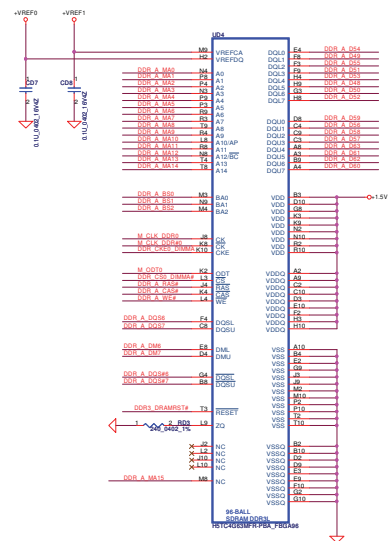
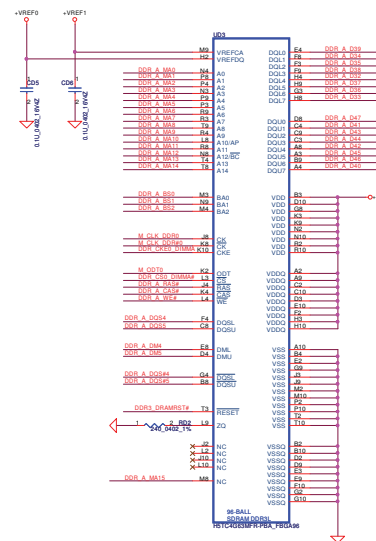
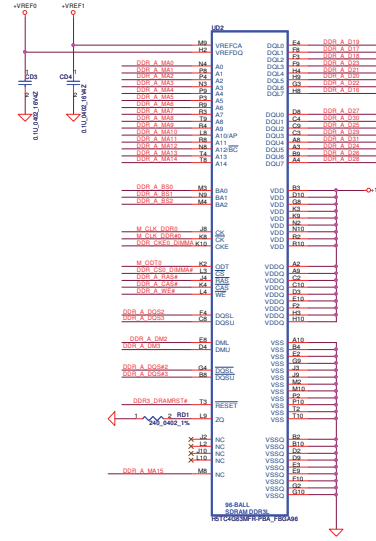
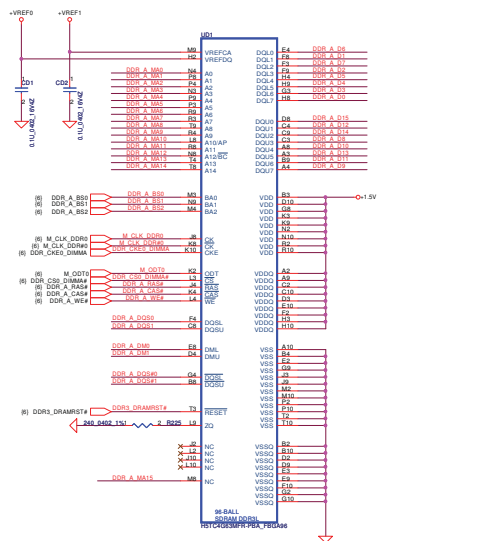
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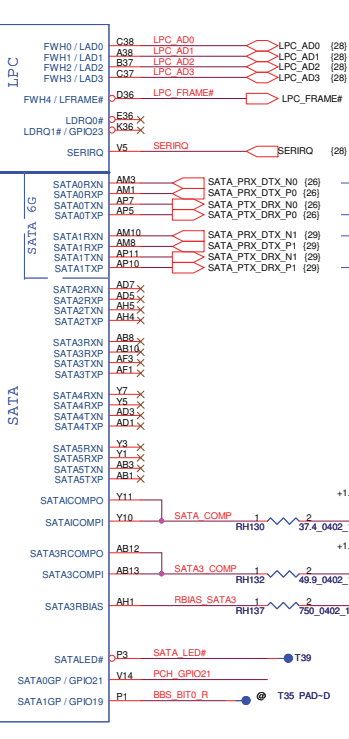
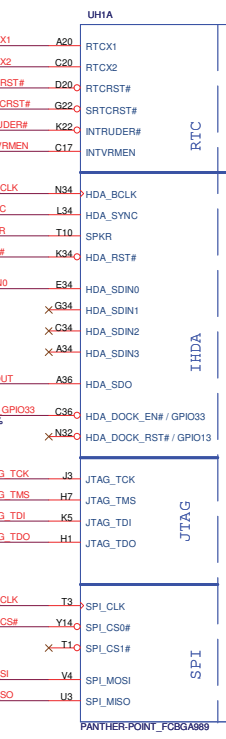
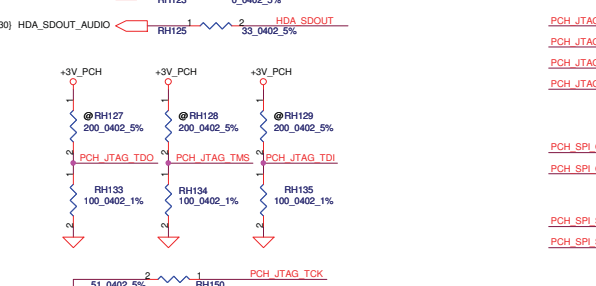
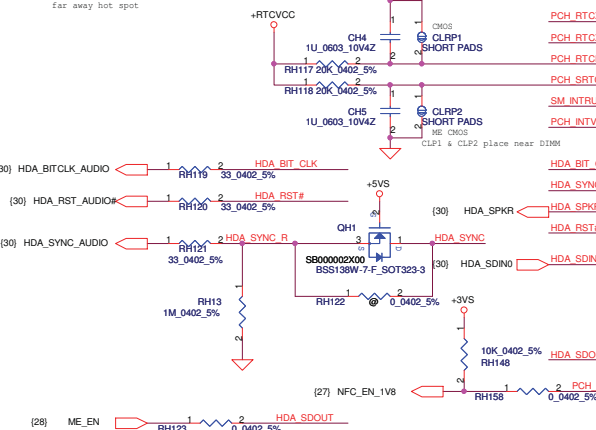
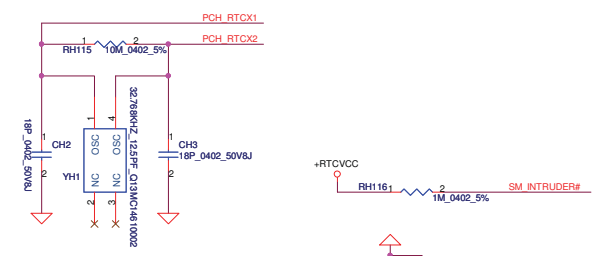
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A3	LA-8101P	Date:		Monday, November 14, 2011
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- (R) DDR\_A\_M0-15 DDR\_A\_M0-15
- (R) DDR\_A\_D049-71 DDR\_A\_D049-71
- (R) DDR\_A\_D058-71 DDR\_A\_D058-71
- (R) DDR\_A\_D01-43 DDR\_A\_D01-43

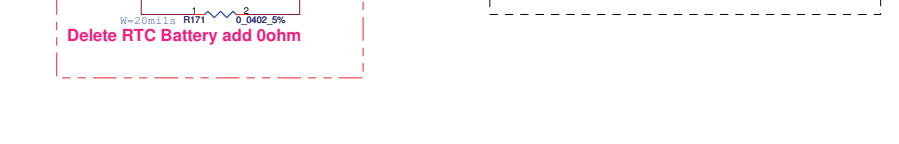
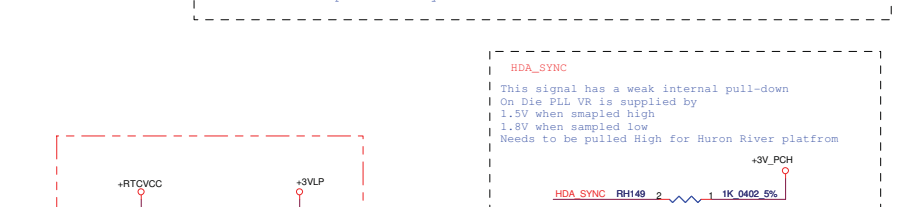
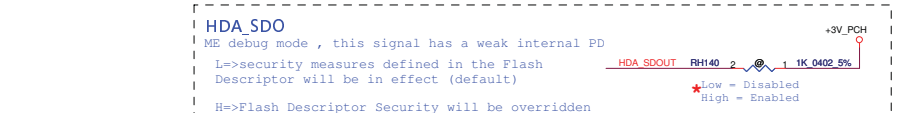
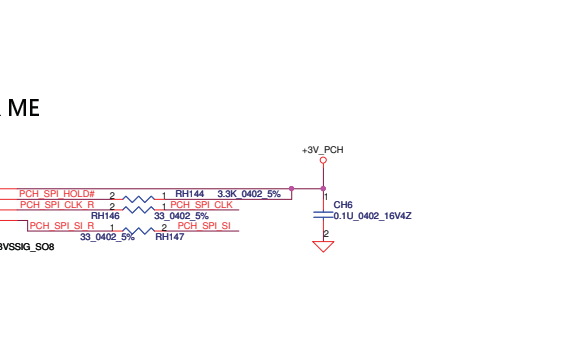
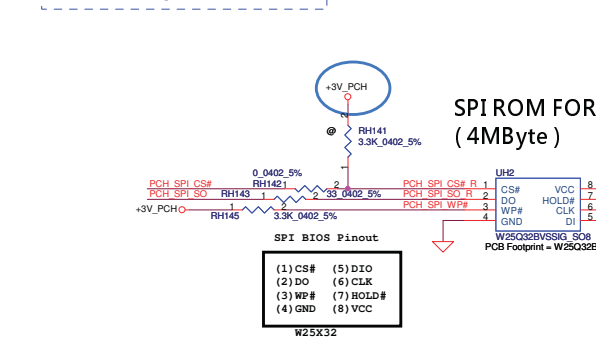


Classification	Confidential		File
Issued Date	2010/04/26	Disciplined Date	2011/07/16
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Doc No.	Doc Number	Rev	6.1
Monday, November 14, 2011			Page 11 of 18

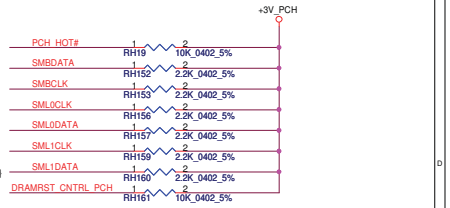
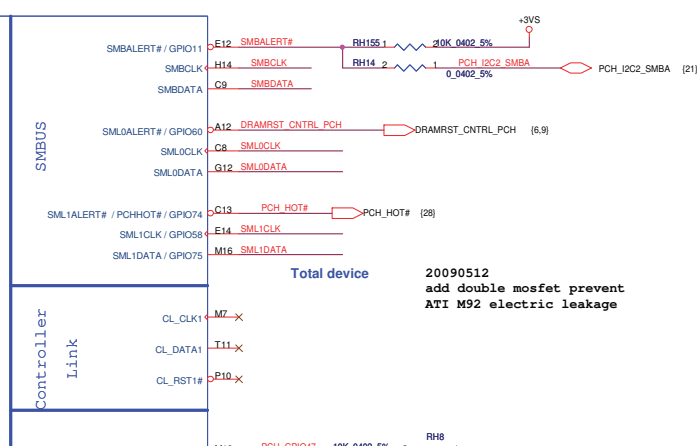
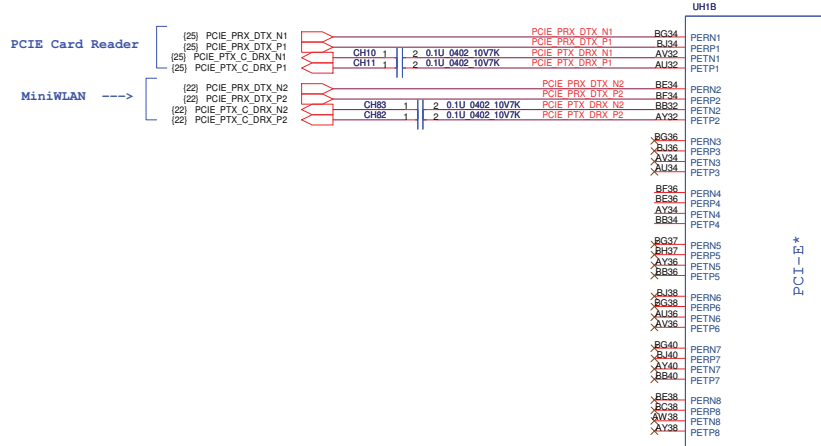


PANTHER-POINT\_FCBGA869  
Part Number = SA00004N020

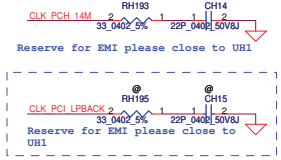
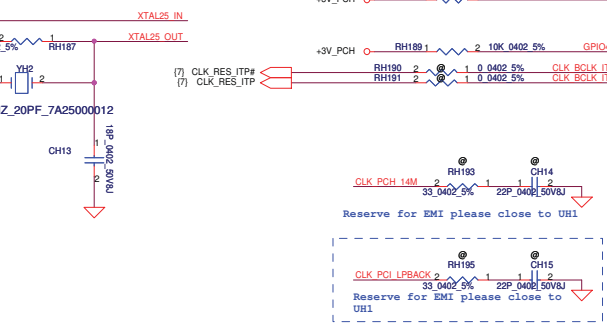
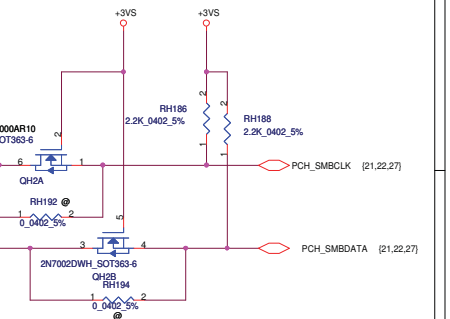
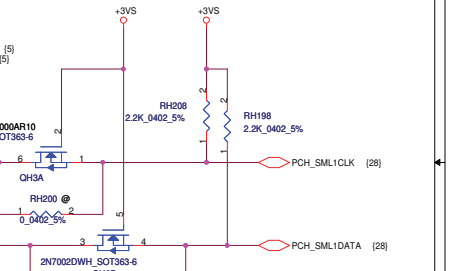
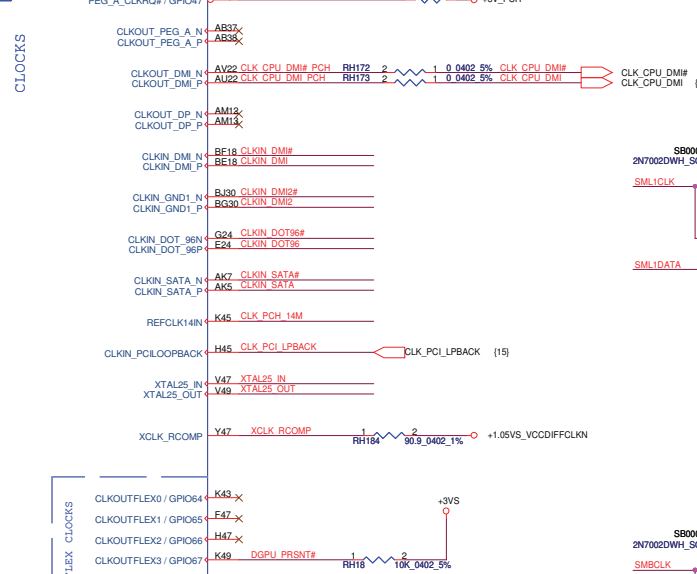
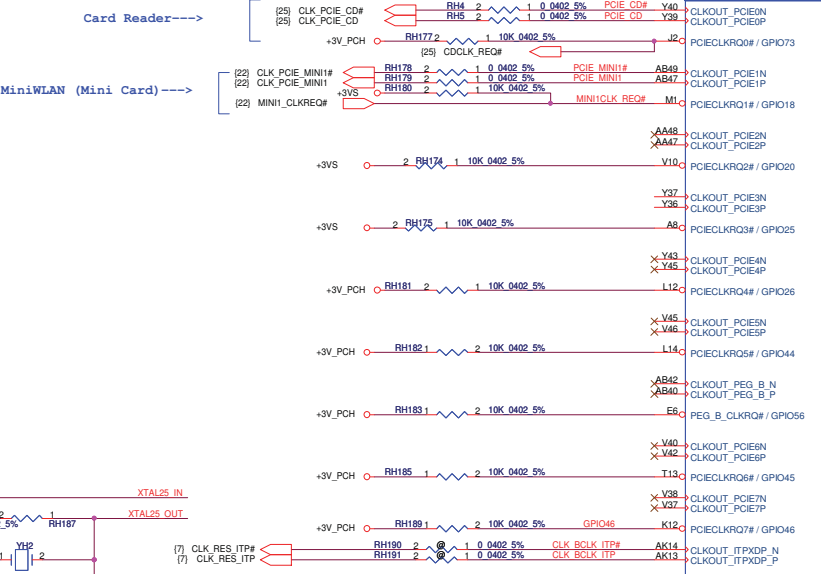
### SPI ROM FOR ME (4MByte)



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				1A-841P	Rev 0.1
				Date:	Monday, November 14, 2011
				Sheet	12 of 46



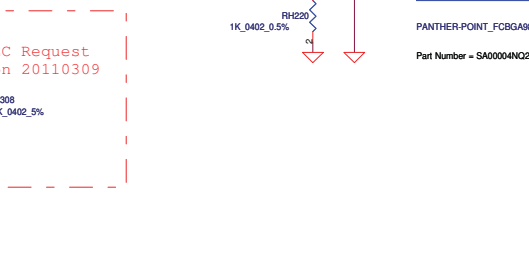
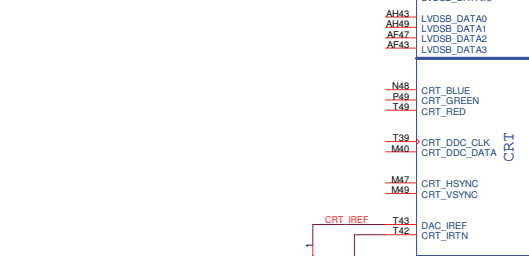
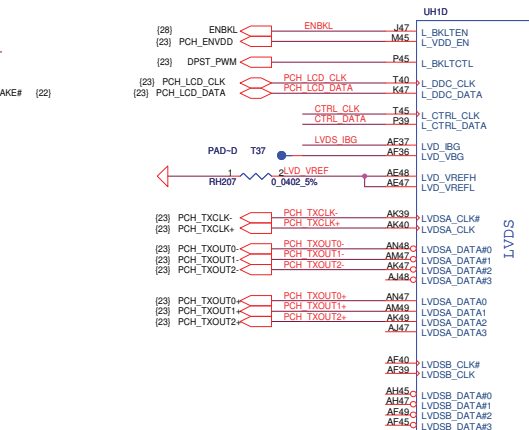
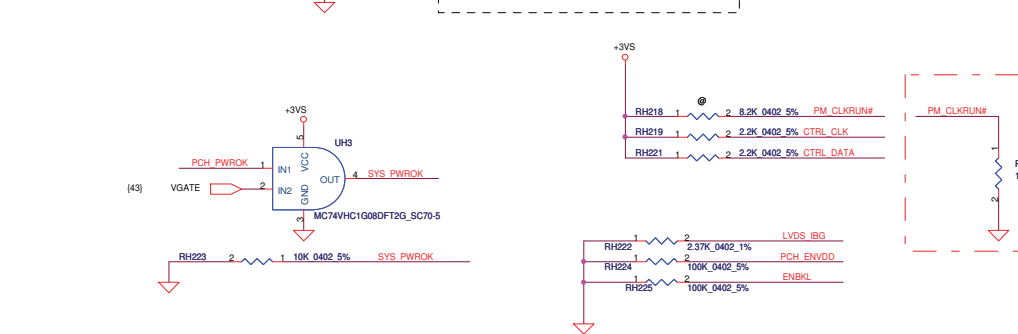
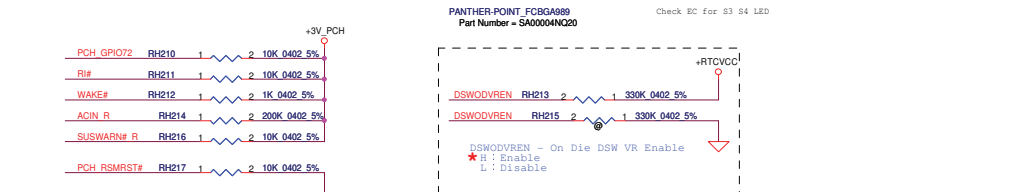
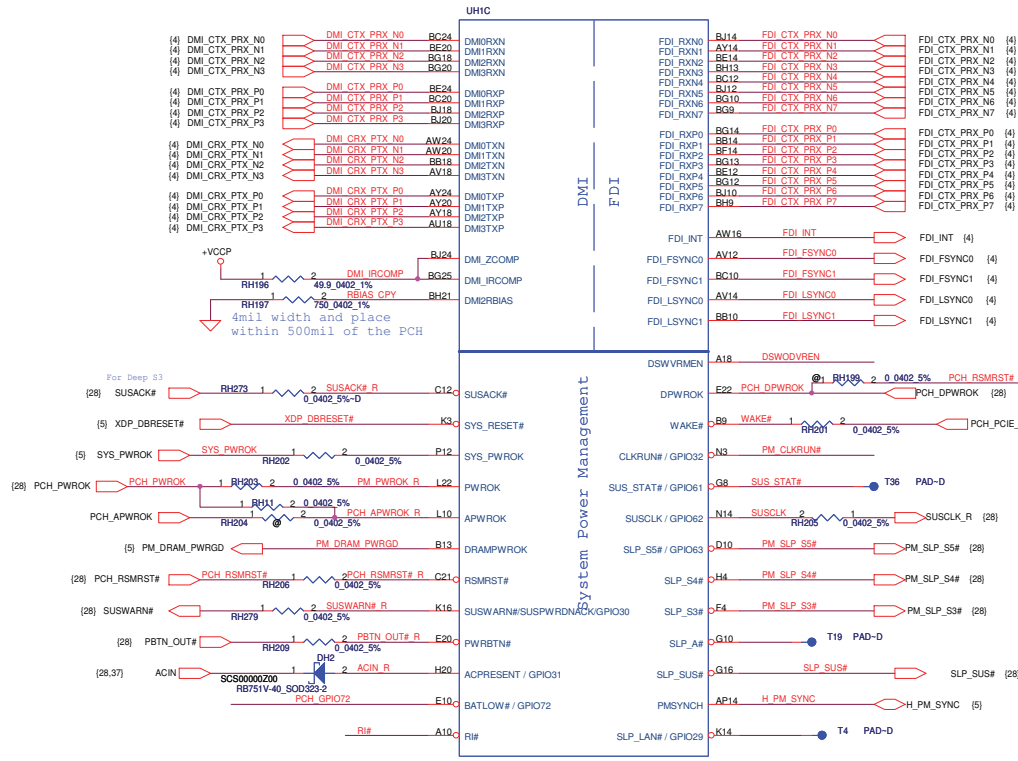
Total device 20090512  
add double mosfet prevent  
ATI M92 electric leakage

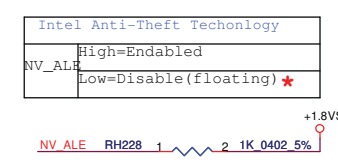
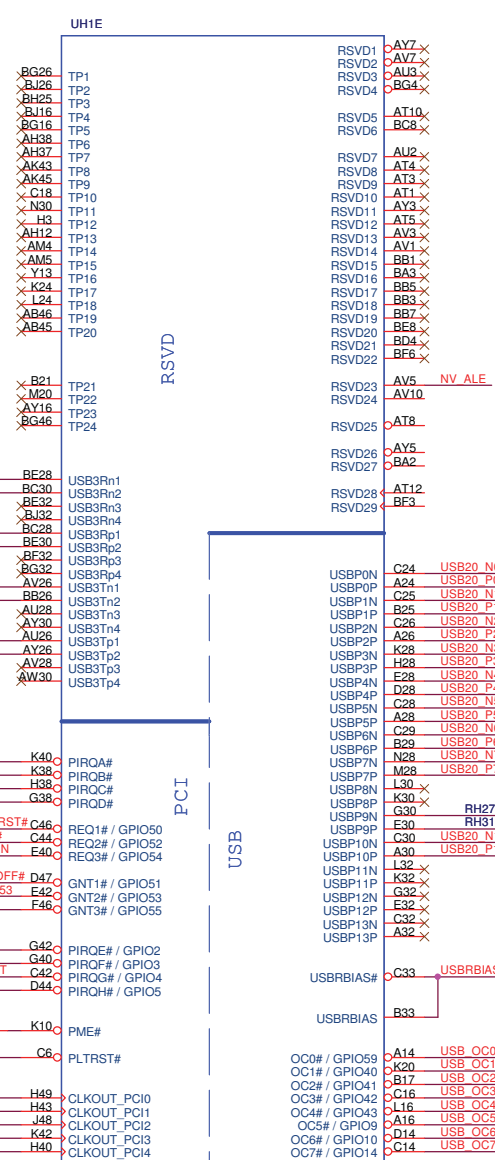
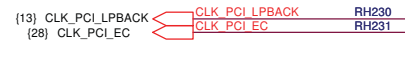
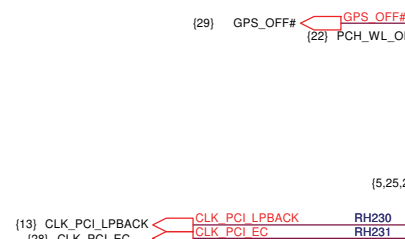
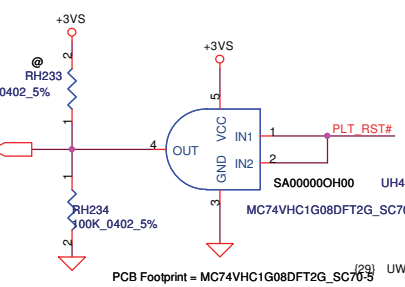
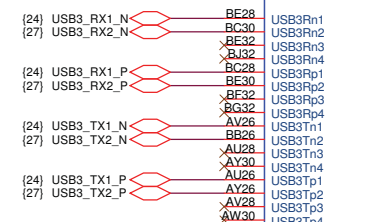
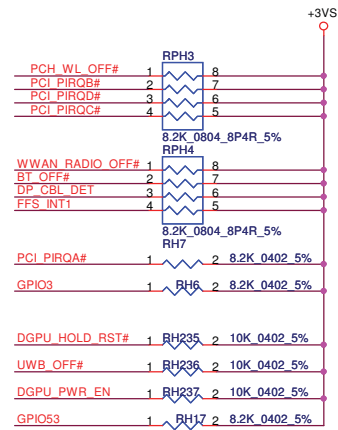


PANTHER-POINT\_FCBGA989  
Part Number = SA0004NC20

Pull High to UMA Mode

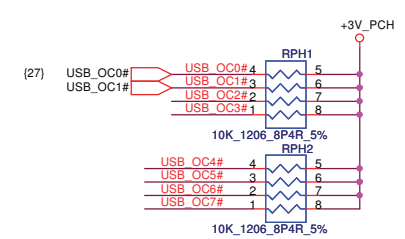
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Issued Date	2010/07/06	Deciphered Date	2011/10/18
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Size	Document Number <b>LA-8441P</b>	Revision 0.1	Date: Monday, November 14, 2011   Sheet 13 of 46





To Cradle for Display link  
 External USB  
 Touch Sensor  
 Sensor  
 MPCIE-WLAN  
 Mini PCIE 3G  
 CAM1 >>1.3M  
 CAM2 >> 2M

To Cradle USB HUB



PANTHER-POINT\_FCBGA989 Part Number = SA00004N020

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			Rev	0.1

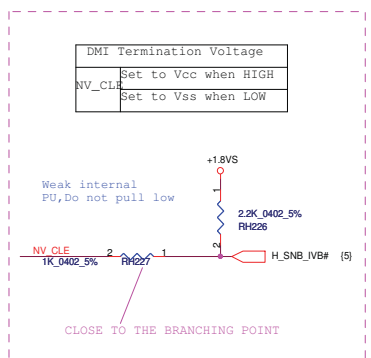
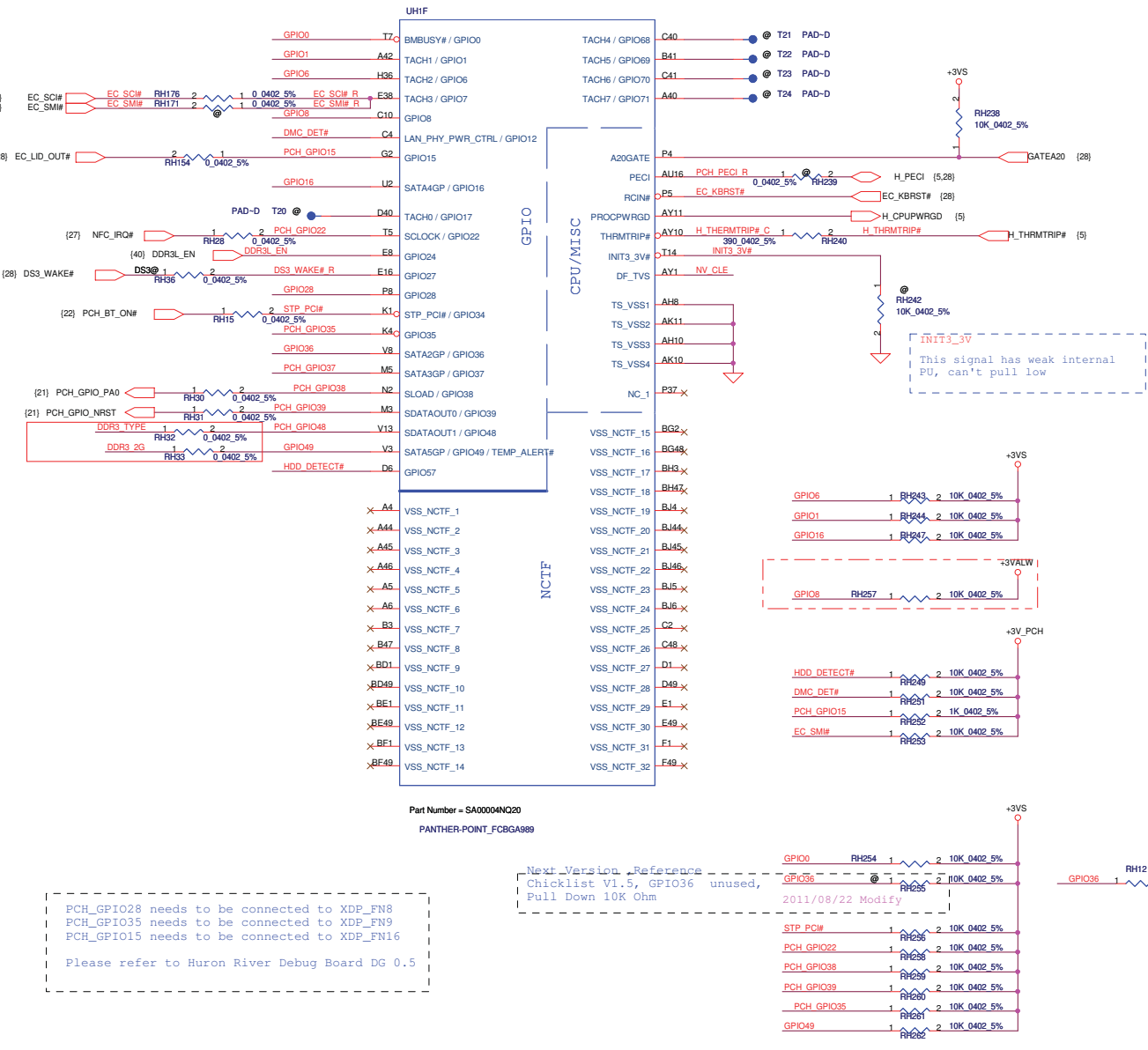
**UFI023**  
 On-Die PLL Voltage Regulator  
 This signal has a weak internal pull up  
 \* H: On-Die voltage regulator enable  
 L: On-Die PLL Voltage Regulator disable

**PCH\_GPIO37**  
 FDI TERMINATION VOLTAGE OVERRIDE  
 \* LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

**For DDR3 need check**

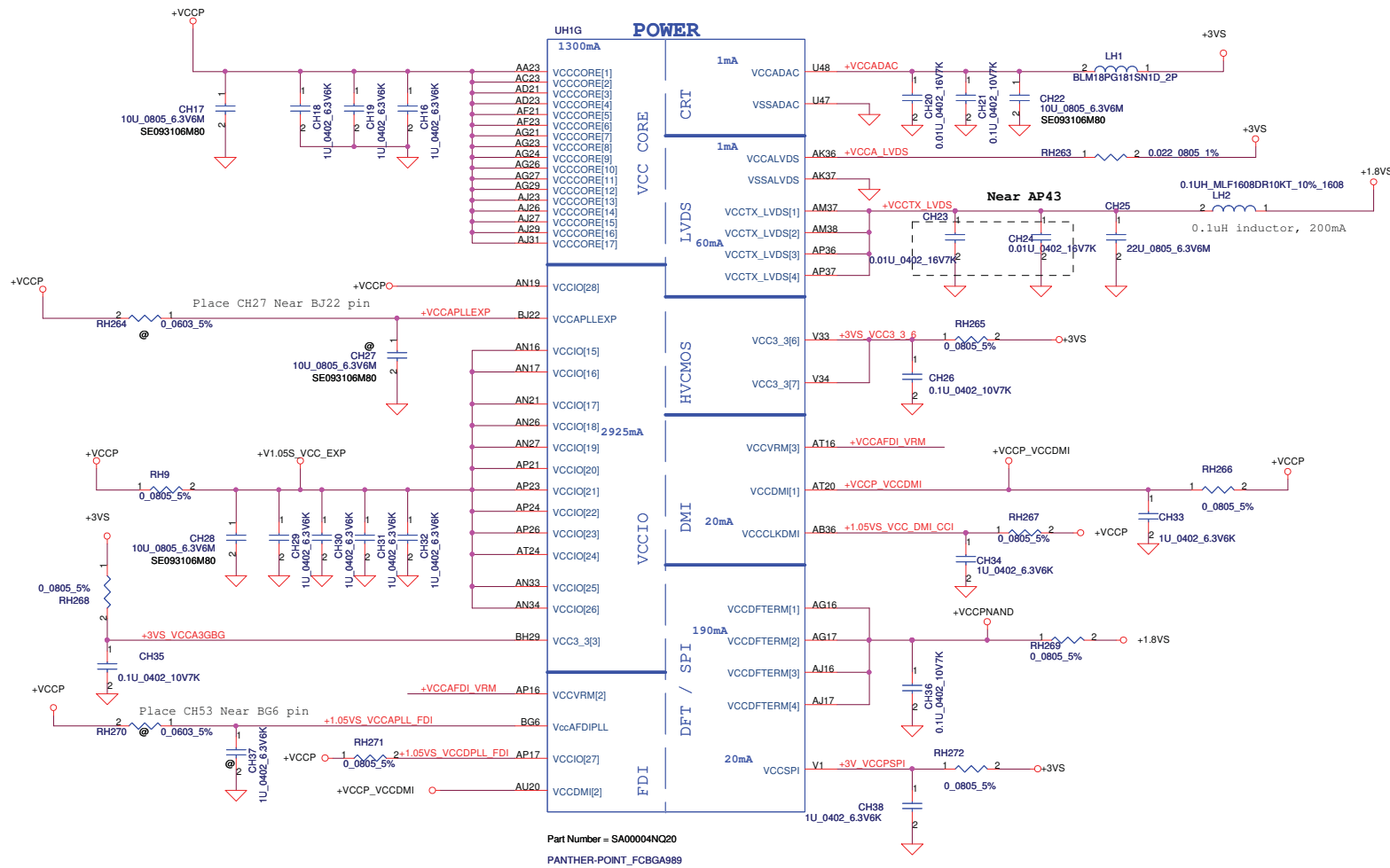
PCH\_GPIO28 needs to be connected to XDP\_FN8  
 PCH\_GPIO35 needs to be connected to XDP\_FN9  
 PCH\_GPIO15 needs to be connected to XDP\_FN16  
 Please refer to Huron River Debug Board DG 0.5

Next Version Reference  
 Checklist V1.5, GPIO36 unused,  
 Pull Down 10K Ohm



Security Classification	Compal Secret Data		Title	
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Compal Electronics, Inc.			PCH (5/8) GPIO, CPU, MISC	
Size	Document Number	Rev		0.1
LA-3441P		Date:		Monday, November 14, 2011
Date:		Sheet		16 of 46

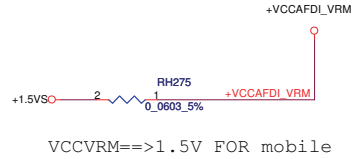




Part Number = SA00004NQ20  
 PANTHER-POINT\_FCBGA989

PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc_3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus_3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detail waiting for newest spec

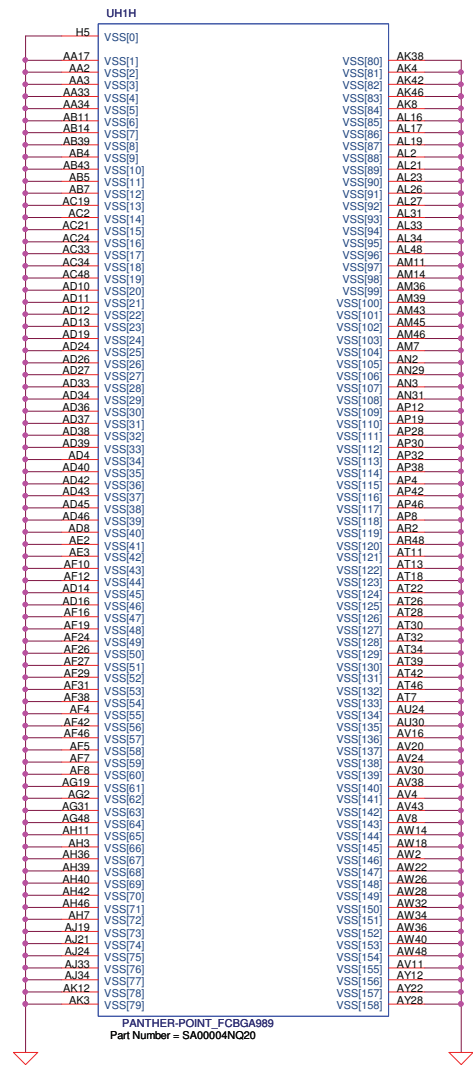
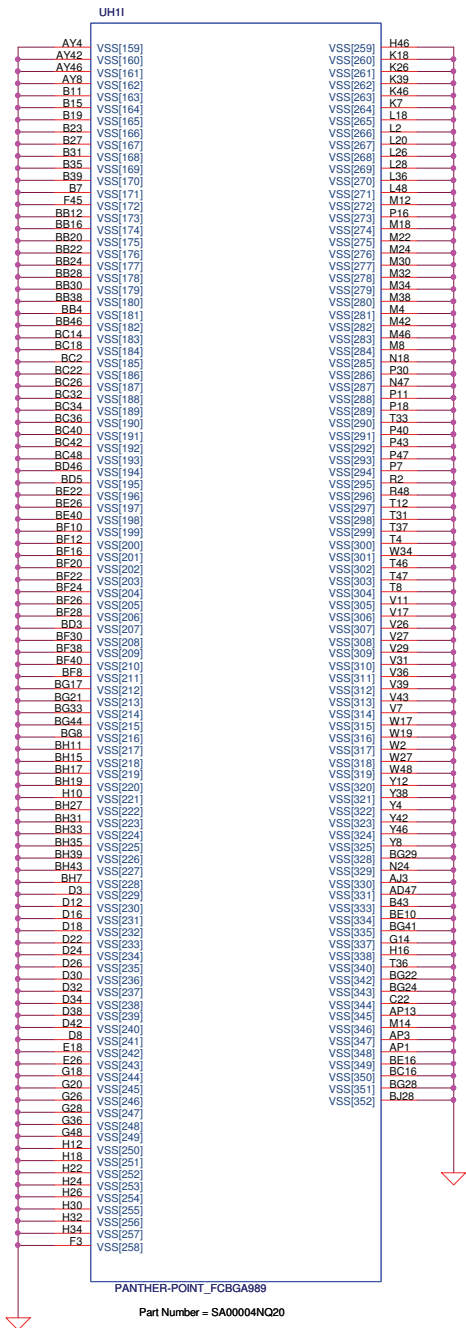


VCCVRM==>1.5V FOR mobile

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Issued Date	2010/07/06	Deciphered Date
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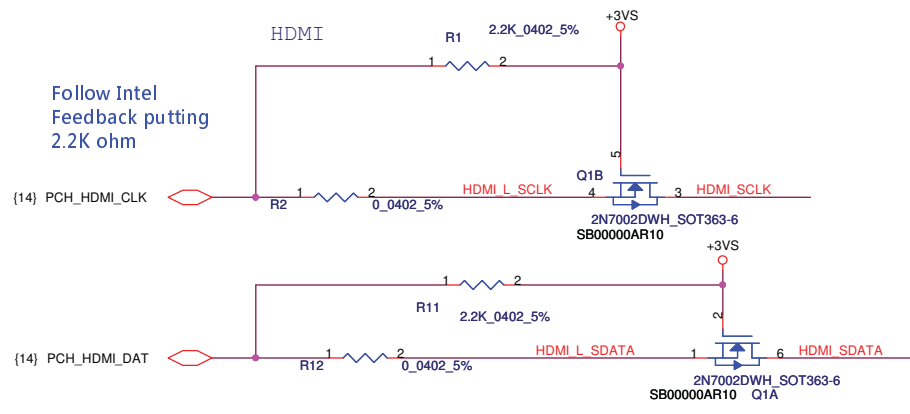
Compal Electronics, Inc.		
Title	PCH (6/8) PWR	
Size	Document Number	Rev
	LA-8441P	0.1
Date:	Monday, November 14, 2011	Sheet 17 of 46



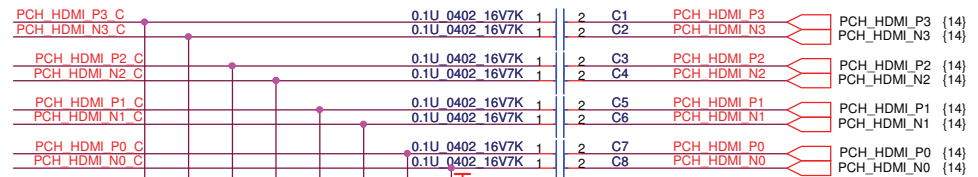


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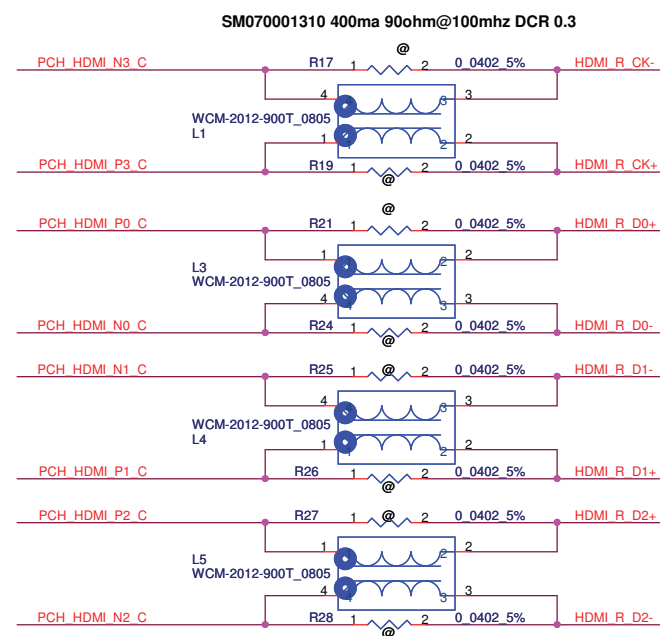
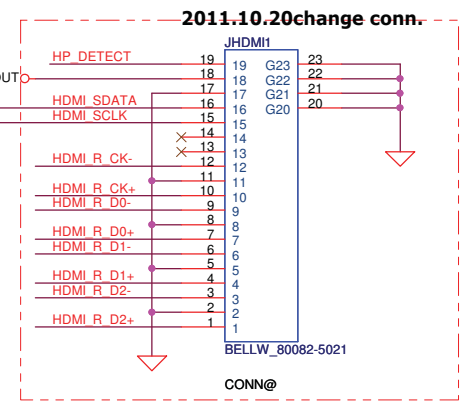
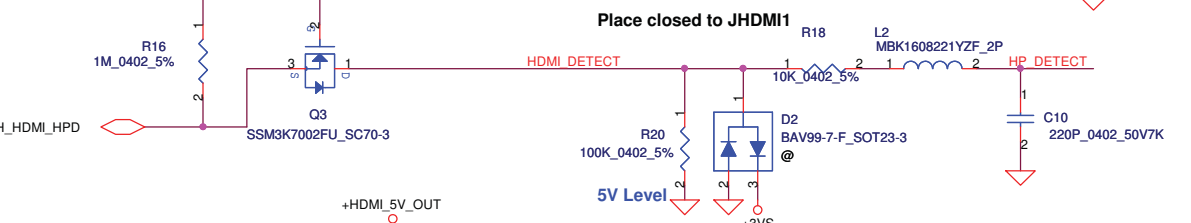
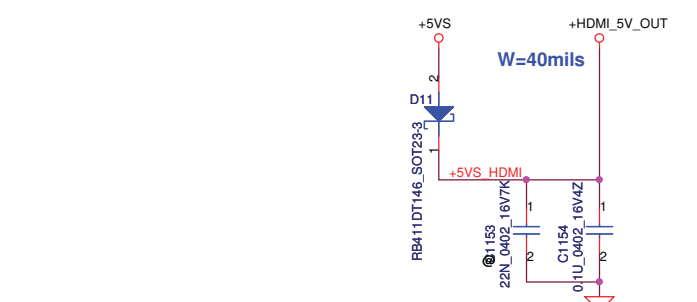
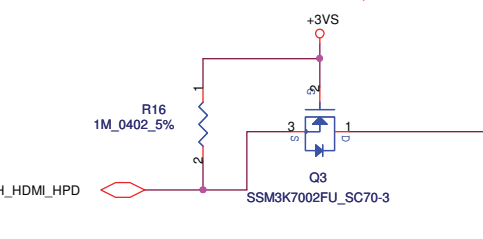
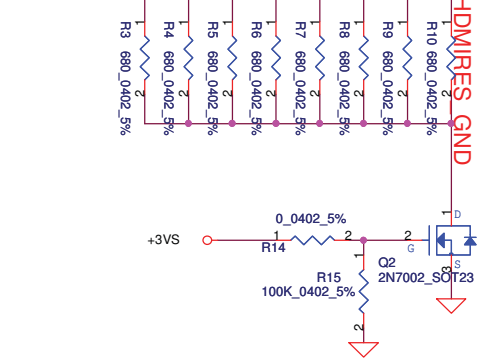
Compal Electronics, Inc.		
Title	<b>PCH (8/8) VSS</b>	
Size	Document Number	Rev
	<b>LA-8441P</b>	0.1
Date:	Monday, November 14, 2011	Sheet 19 of 46



5V PULL UP IN CONNECTER SIDE



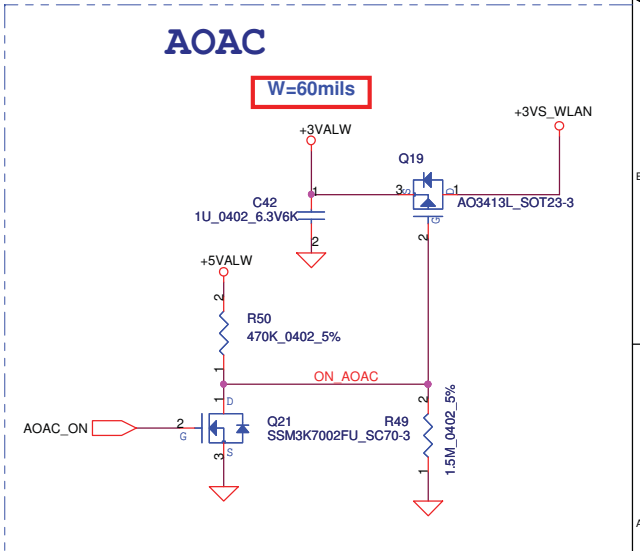
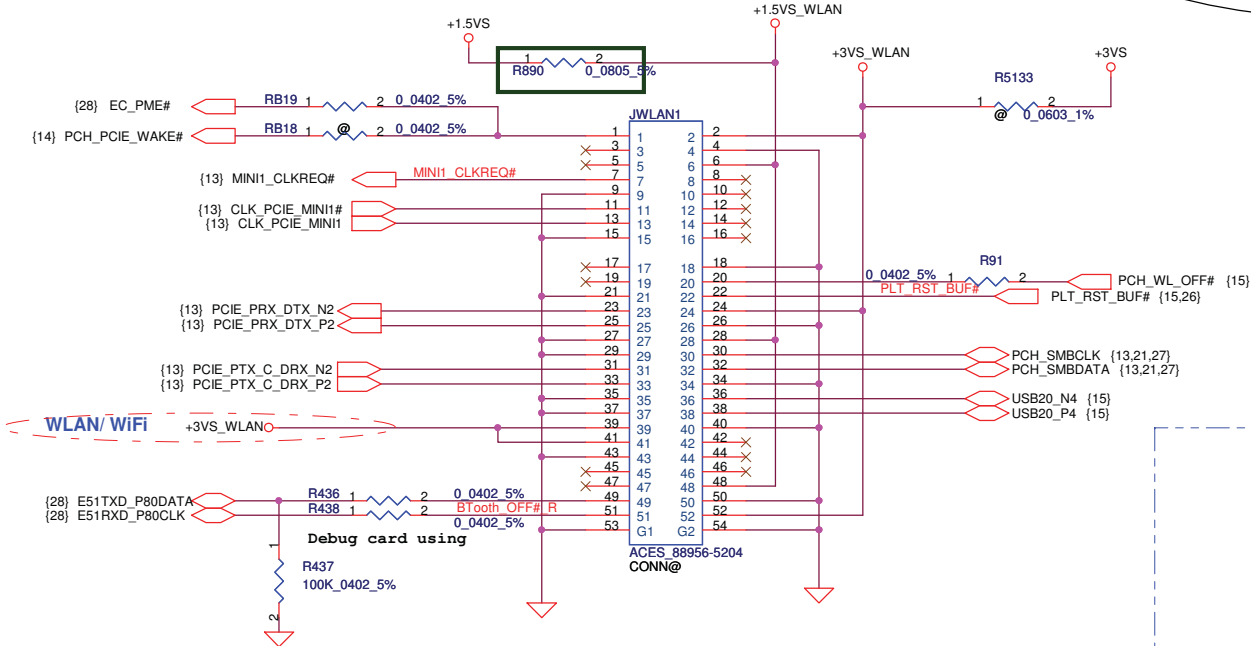
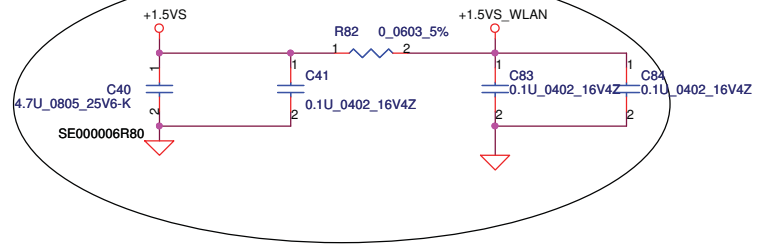
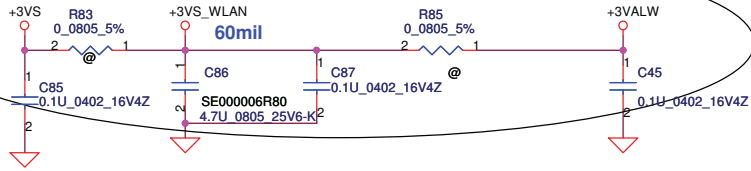
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WIDTH>20 mils



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					<b>LA-8441P</b>	0.1
				Date:	Monday, November 14, 2011	Sheet 20 of 46



# For Wireless LAN

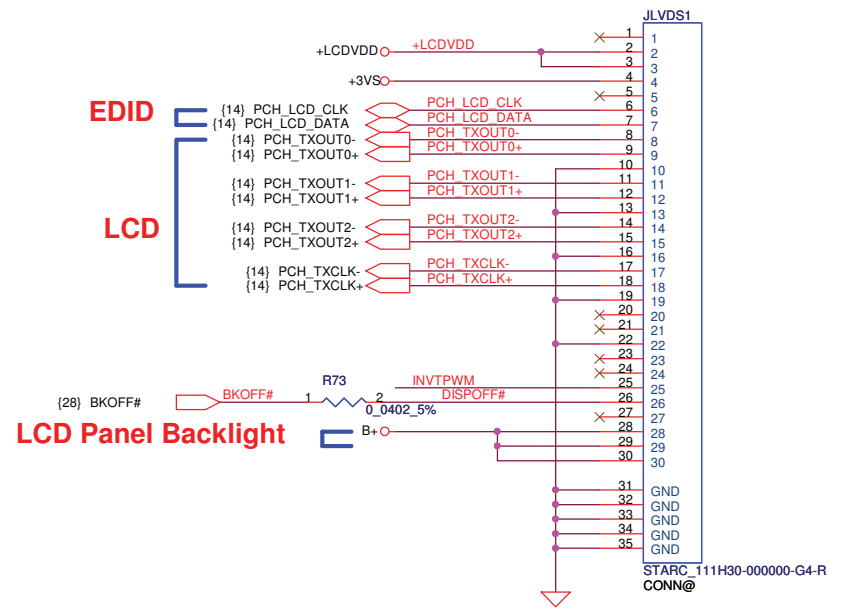
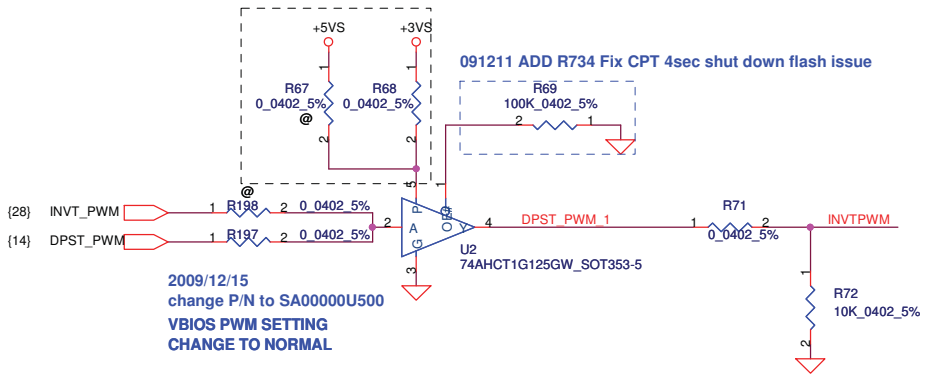
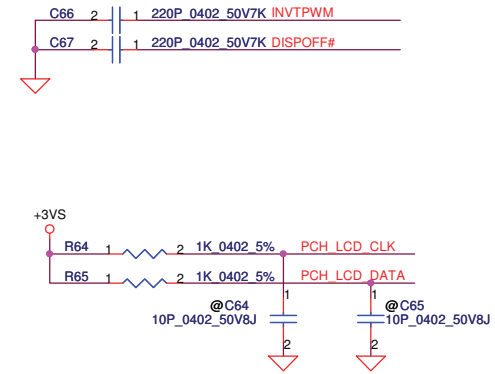
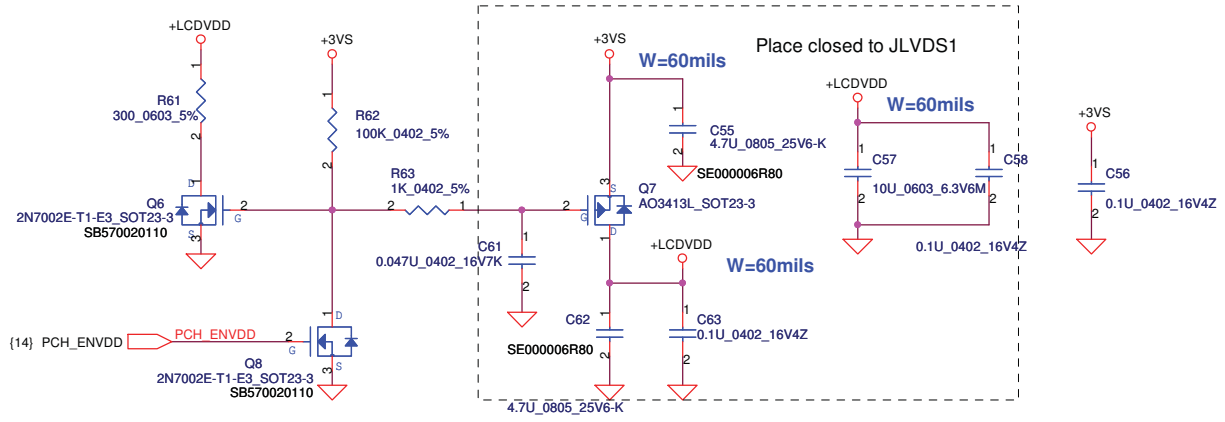


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/07/06	Deciphered Date	2011/10/18	Title		
				MiniCard Wlan Conn		
				Size	Document Number	Rev
				LA-8441P		0.1
				Date:	Monday, November 14, 2011	Sheet 22 of 46

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# LCD POWER CIRCUIT



## LCD Panel Backlight

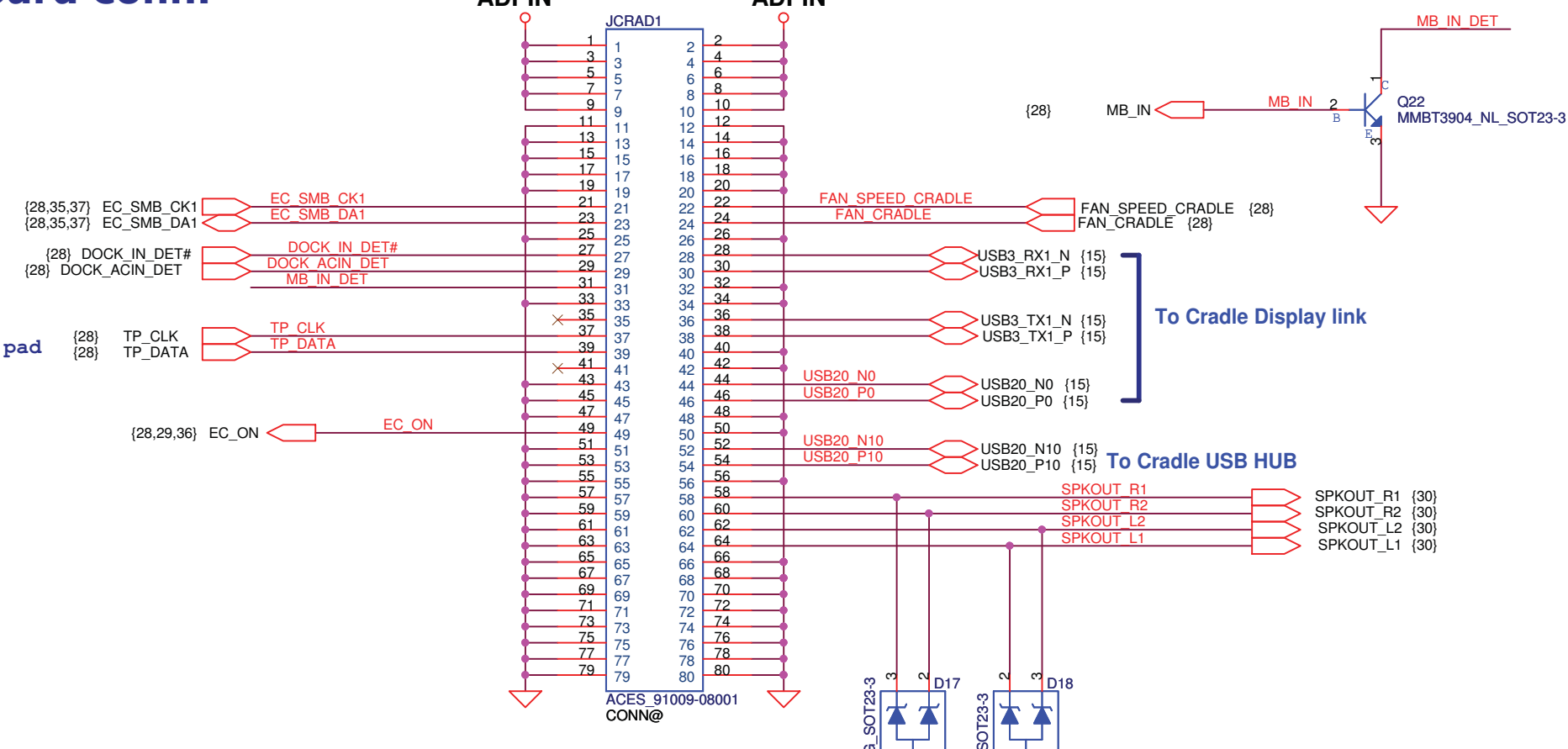
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/06	Deciphered Date	2011/10/18	Title <b>LVDS Connector</b>	
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Date:	Monday, November 14, 2011	Sheet	23	of	46
Rev	0.1				

# To Cradle board conn.

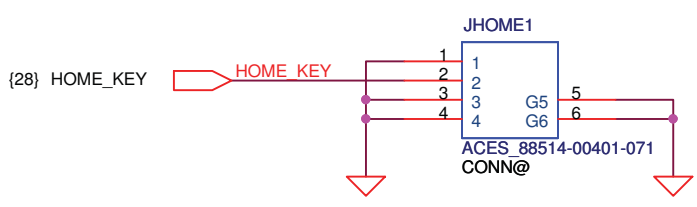
ADPIN ADPIN

For cradle BATT

Touch pad

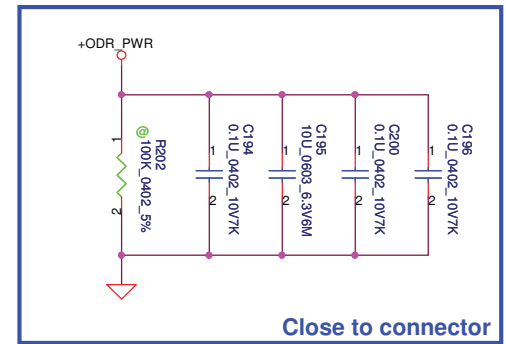
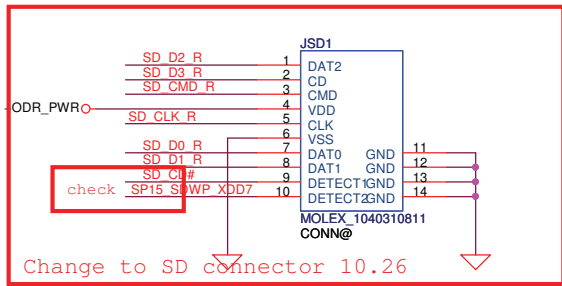
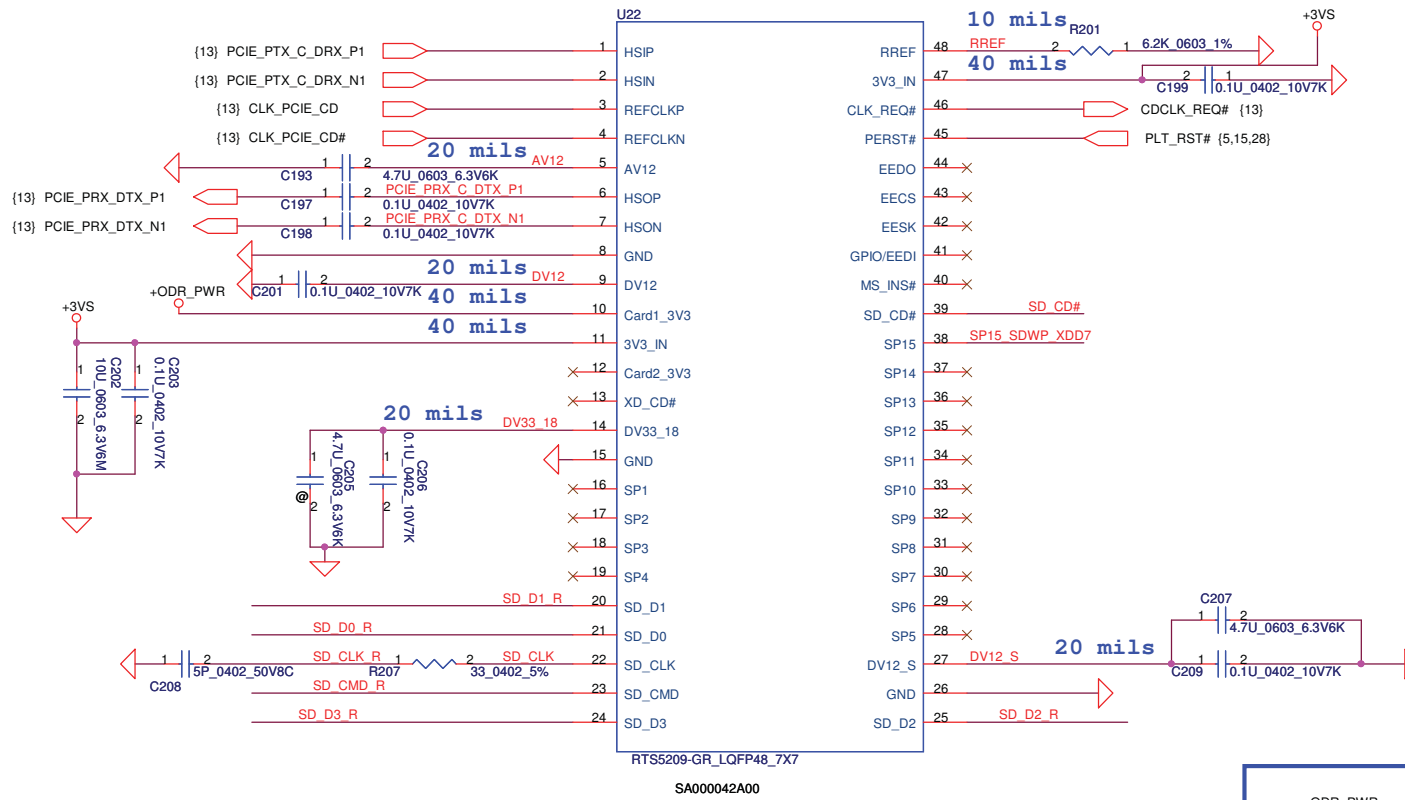


# To home key conn.

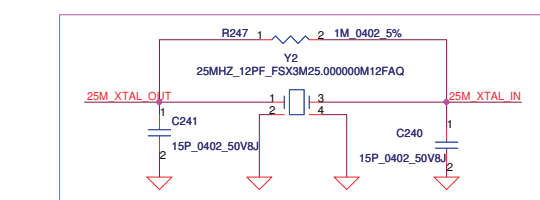
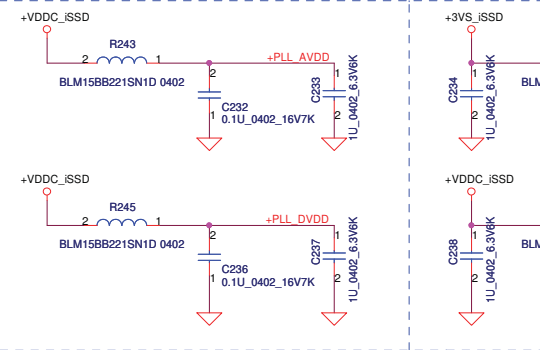
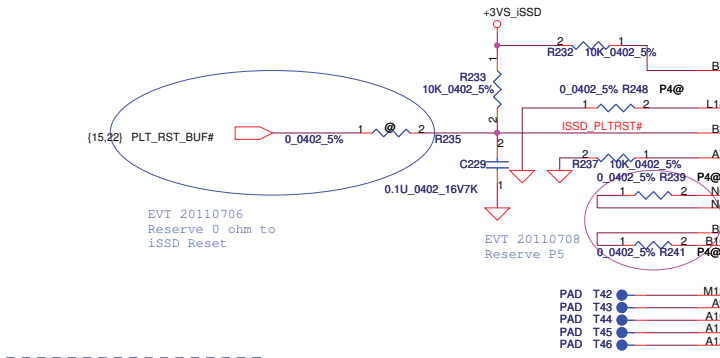
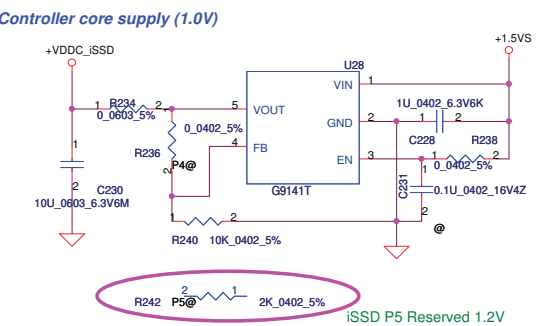
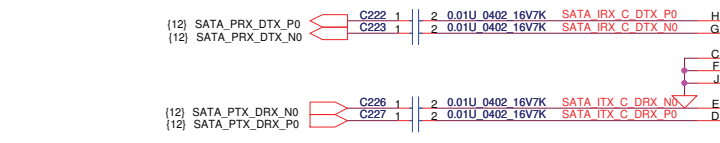
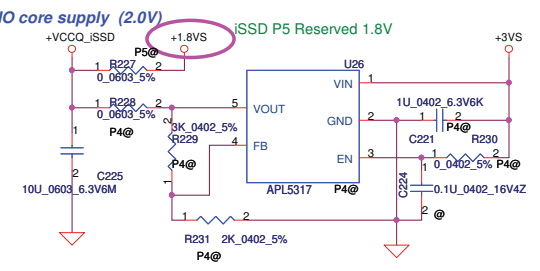
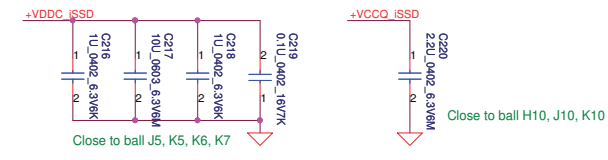
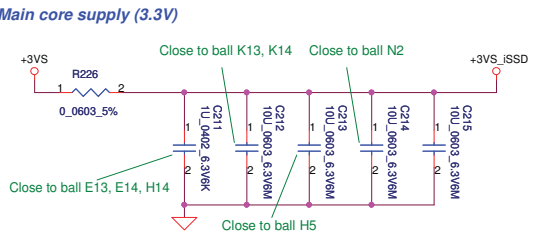


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				Date: Monday, November 14, 2011		Sheet 24 of 46	



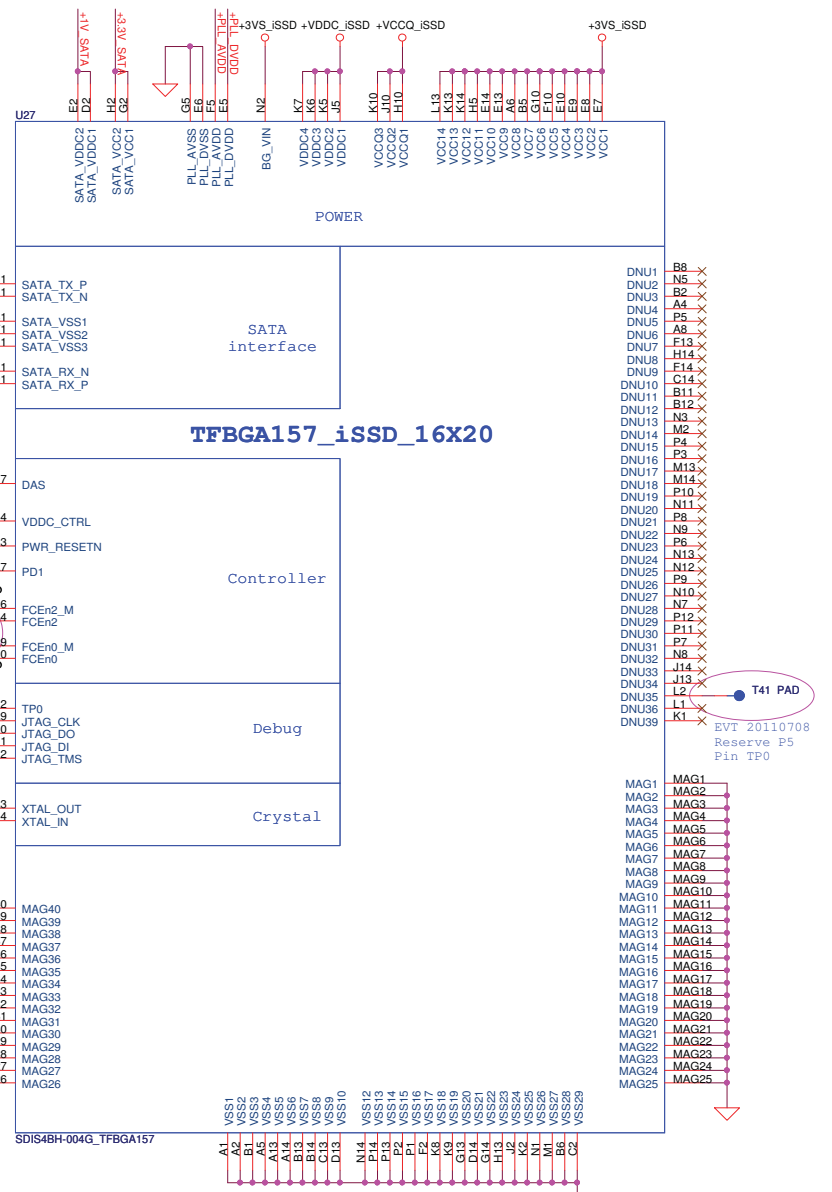


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Size B	Document Number	LA-8101P		Rev	0.1
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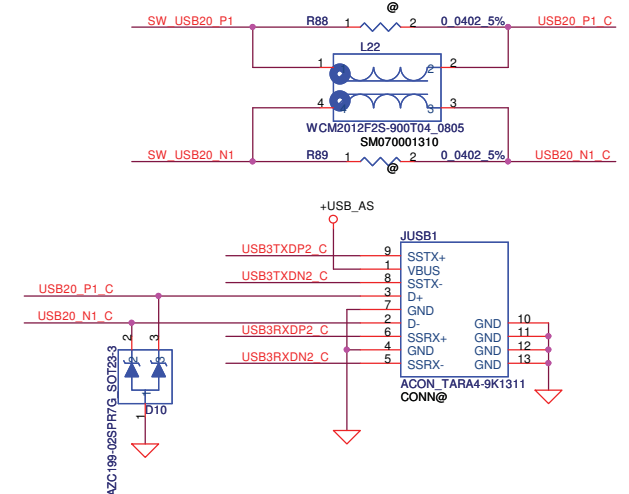
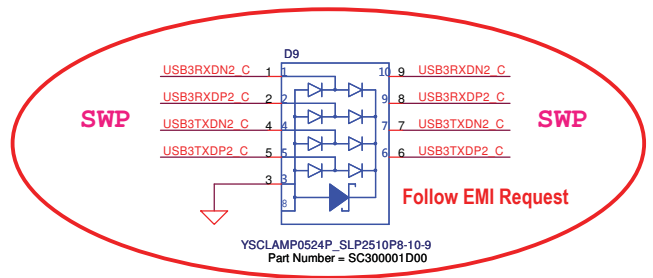
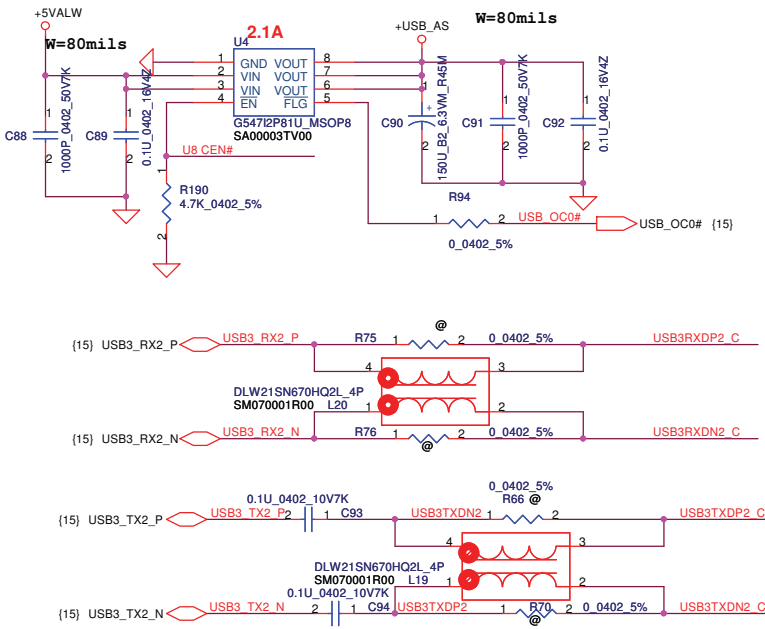
EVT 20110708  
 Change to Seam type Crystal  
 25 MHz, 12pF, 30 ppm

Sandisk suggest Crystal is Seam type

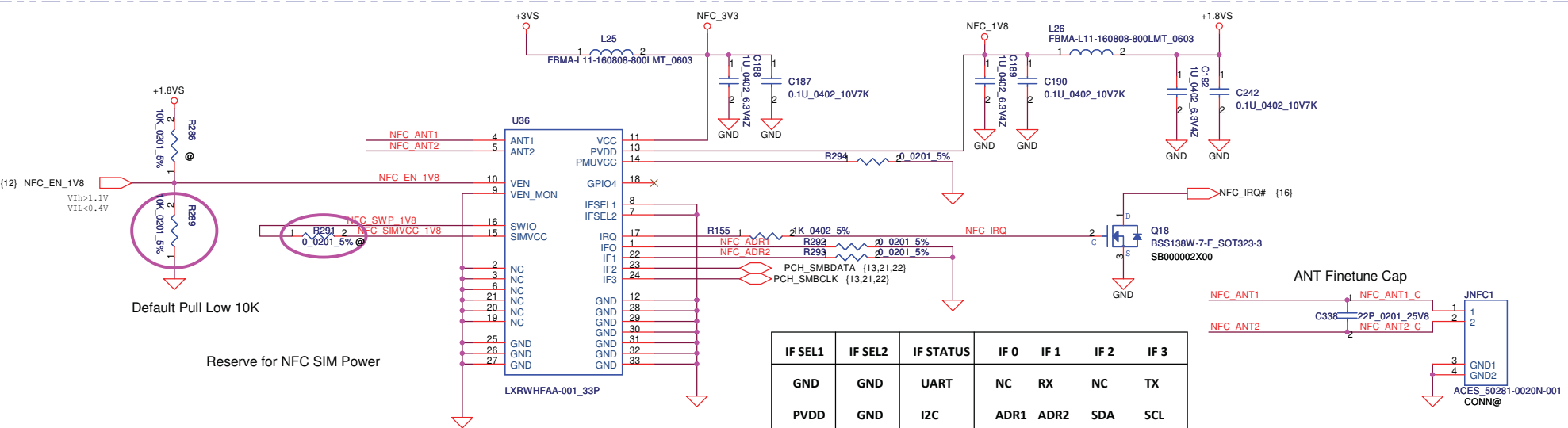


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Date: Monday, November 14, 2011		Sheet 26 of 46		Rev 0.3	

# USB3.0



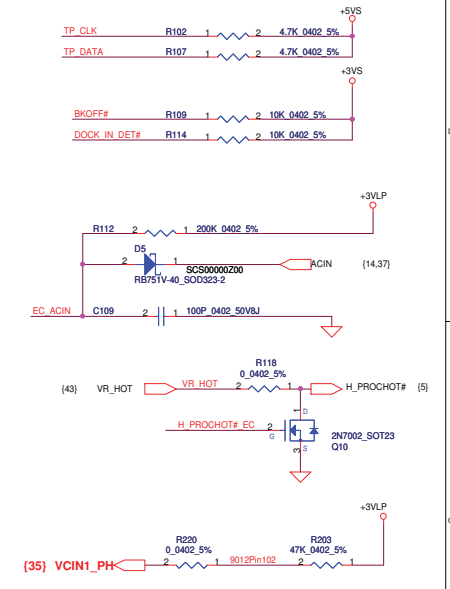
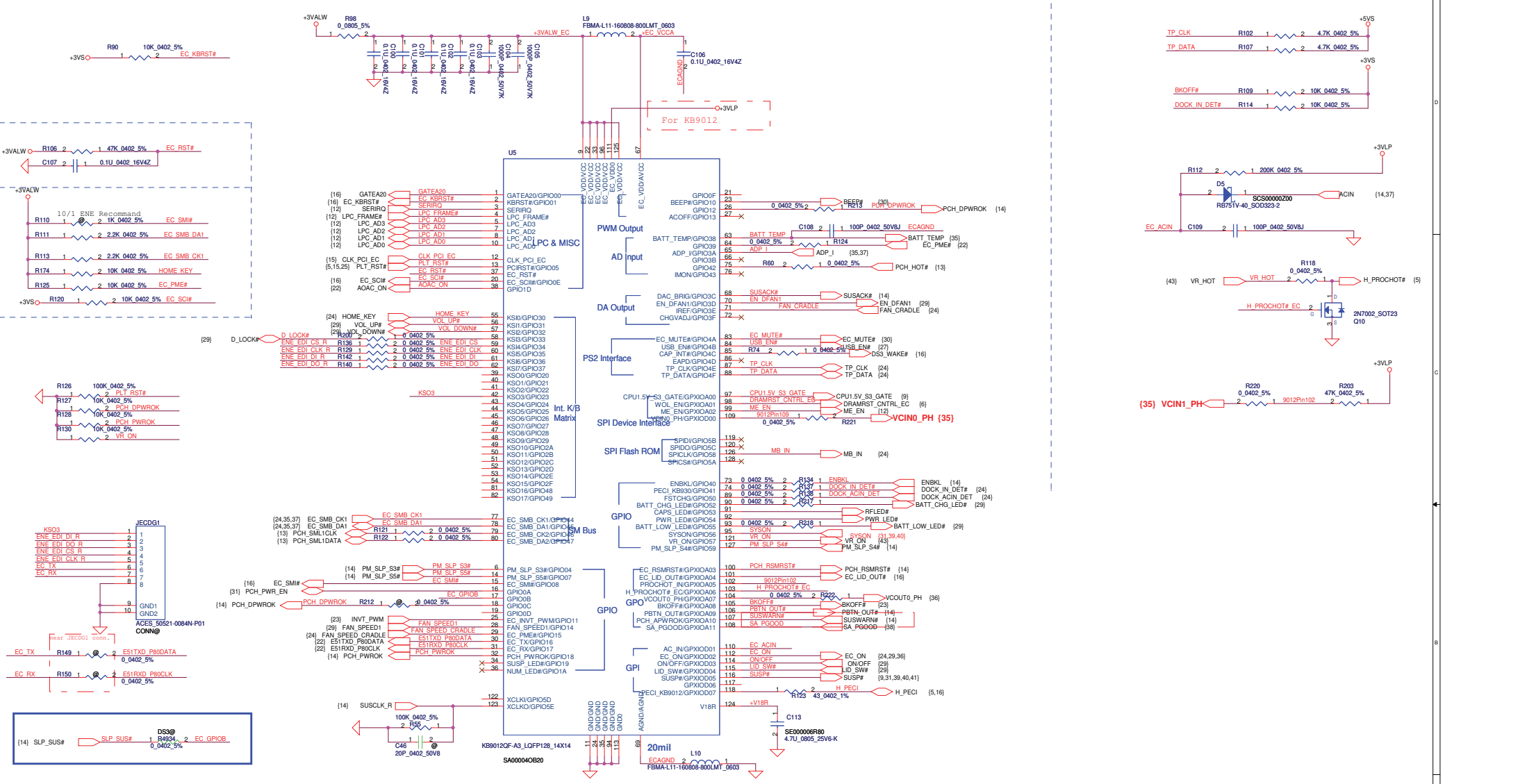
# NFC



IF SEL1	IF SEL2	IF STATUS	IF 0	IF 1	IF 2	IF 3
GND	GND	UART	NC	RX	NC	TX
PVDD	GND	I2C	ADR1	ADR2	SDA	SCL
GND	PVDD	SPI	NSS	MOSI	SCK	MISO
PVDD	PVDD	SPI	NSS	MOSI	SCK	MISO

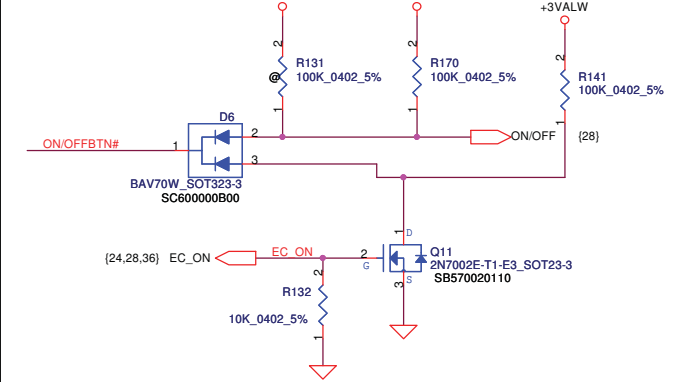
NFC_IRQ	NFC_IRQ#	Function
High	Low	NFC Transfer Data to PCH
Low	High	NFC No Data to PCH

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/26	Deciphered Date	2011/10/18	Title
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Size A3	Document Number	LA-8101P		Rev 0.1
Date:	Monday, November 14, 2011	Sheet	27	of 46

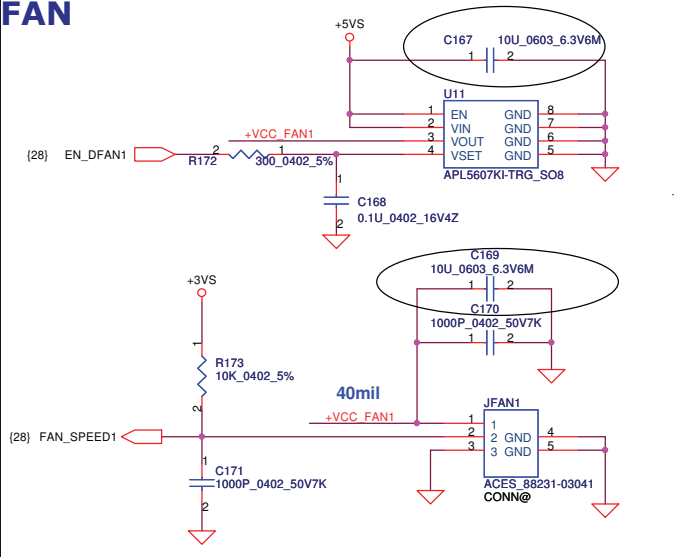


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Title	EC ENE-KB930 & 9012		Size	0.1
Document Number	LA-8101P		Date	Monday, November 14, 2011
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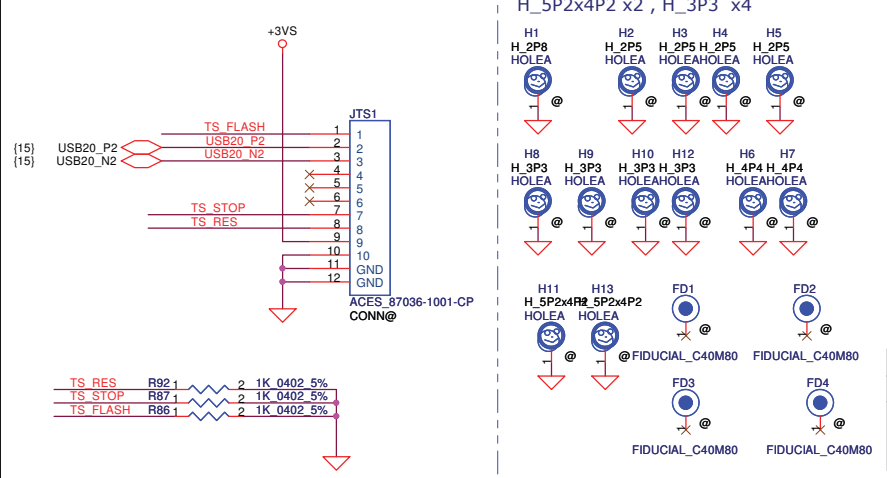
# ON/OFF BTN



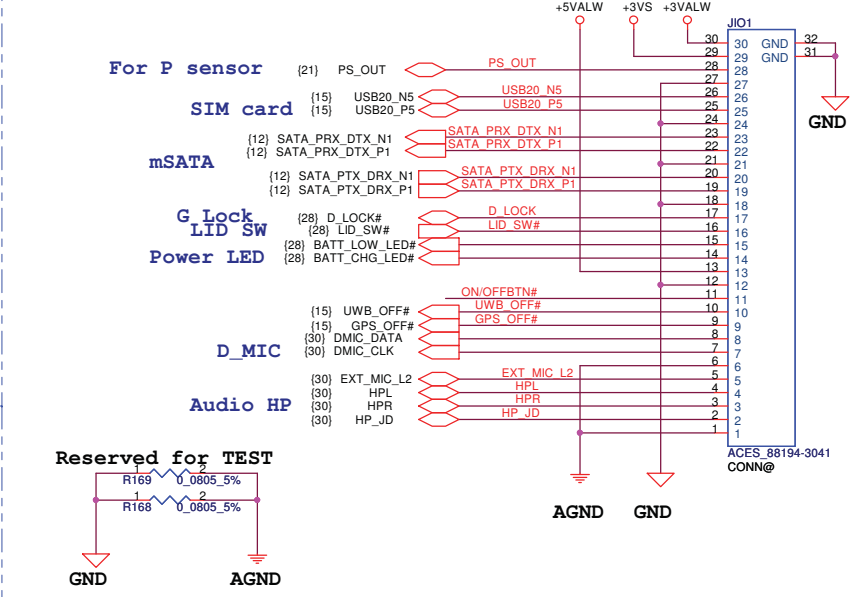
# FAN



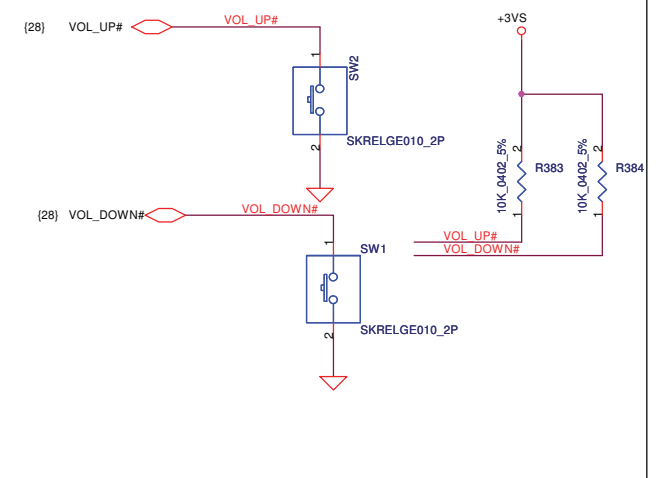
# Touch Screen CONN



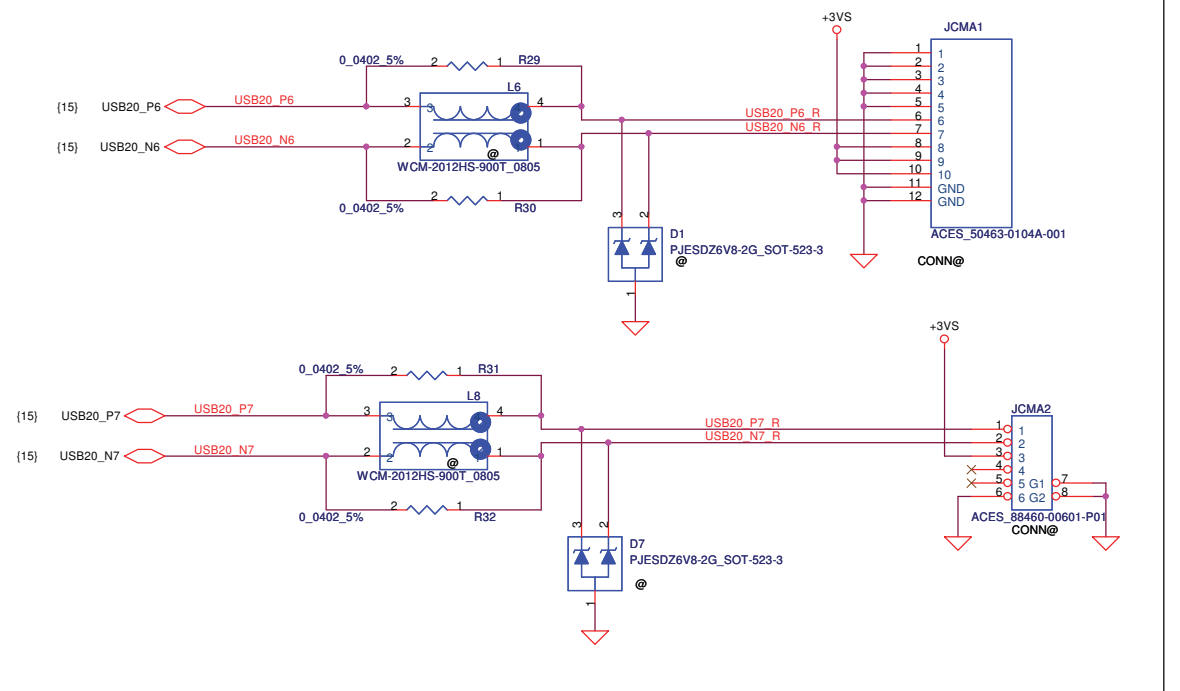
# To IO Board conn.



# VOLUME SW

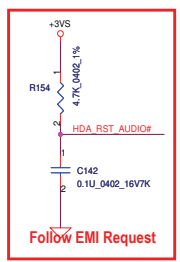
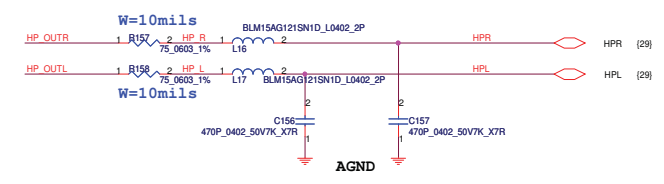
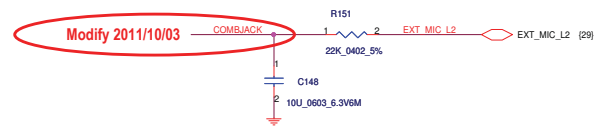
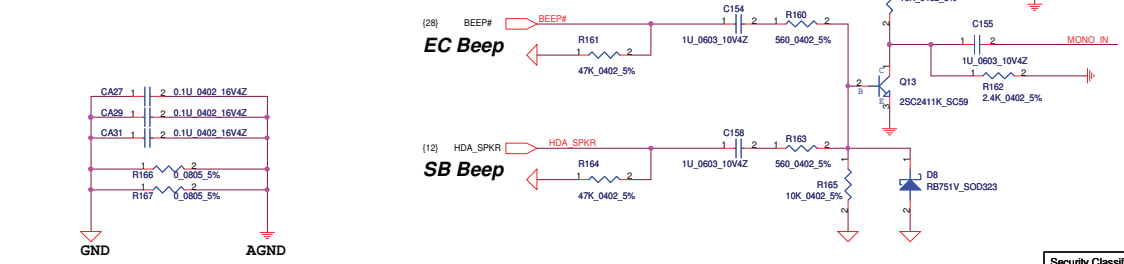
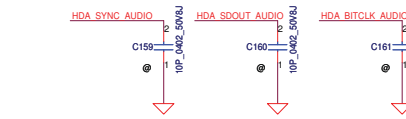
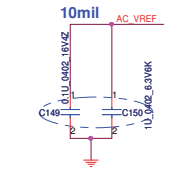
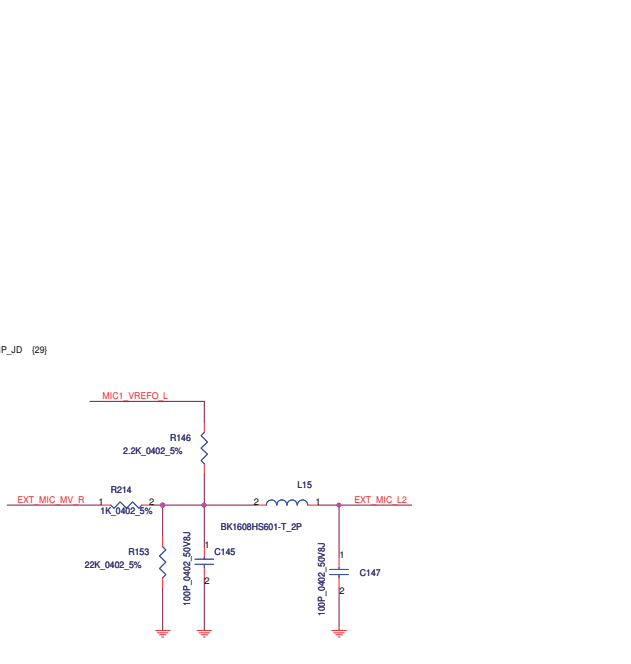
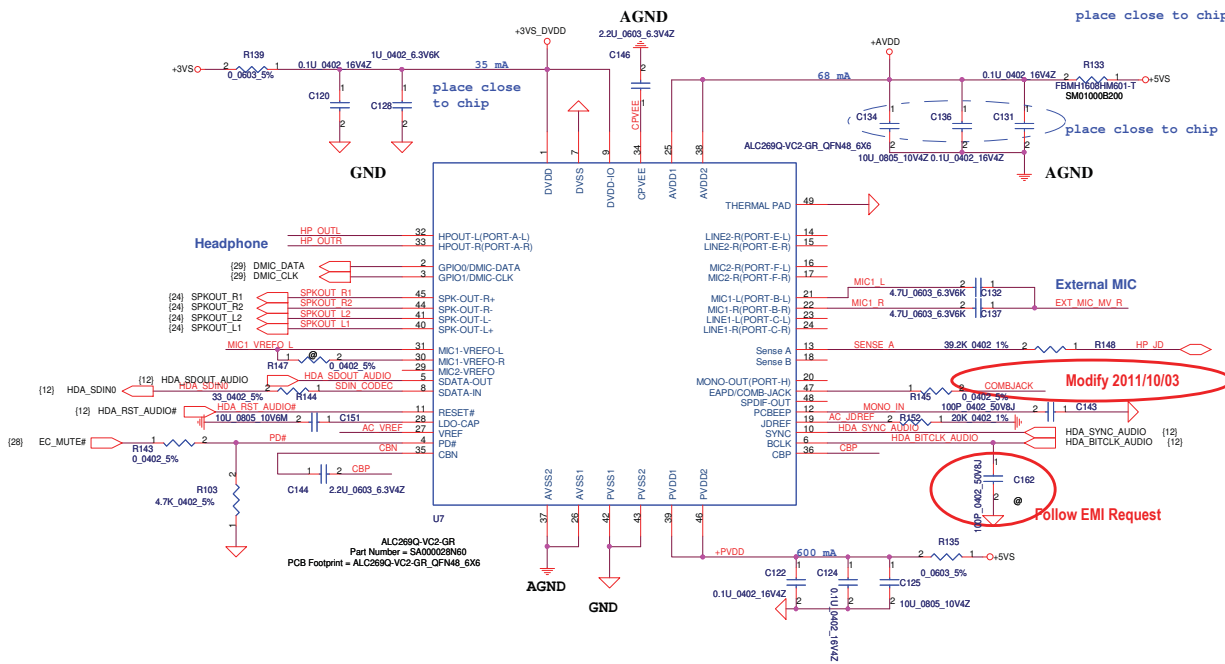


# CMA conn.



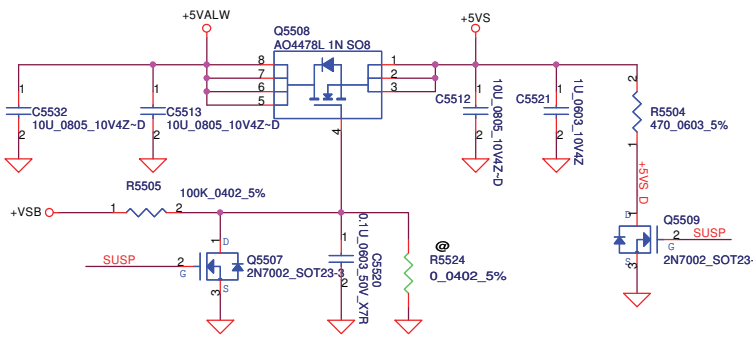
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/26	Deciphered Date	2011/10/18	Title	
				I/O Port / CMA / FAN	
Size	Document Number	Rev			
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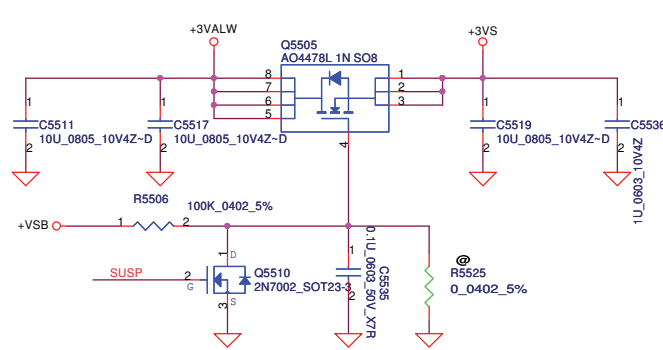


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Size	C	Document Number	LA-8101P	Rev 0.1
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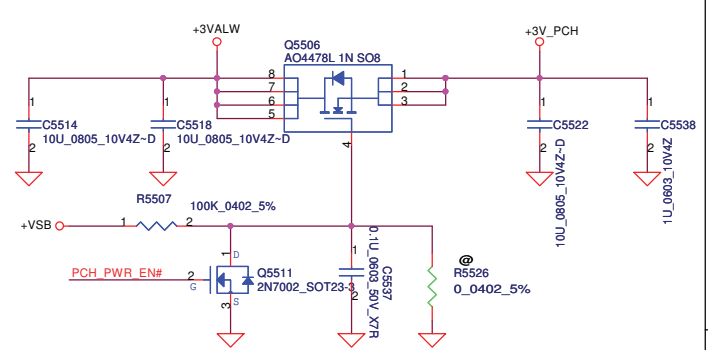
**+5VALW to +5VS**



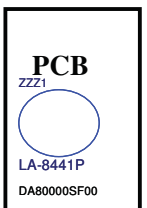
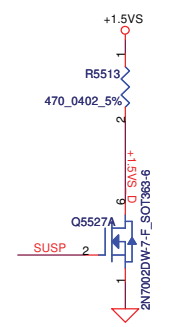
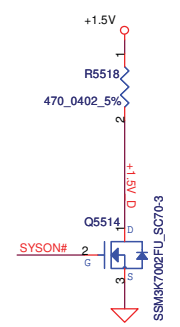
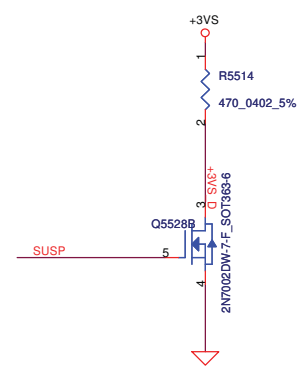
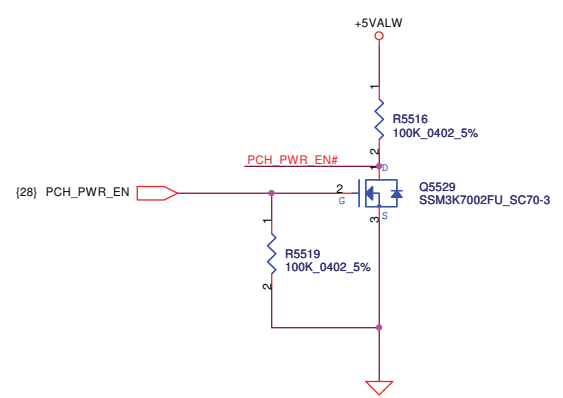
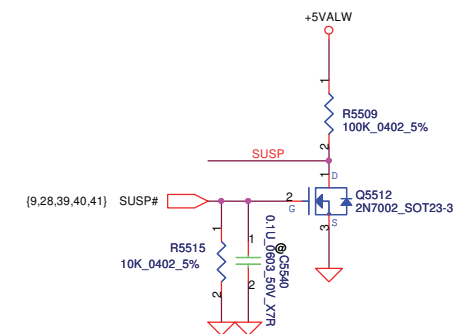
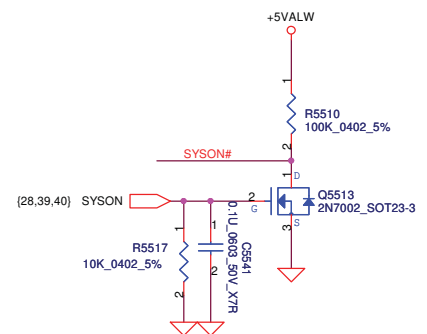
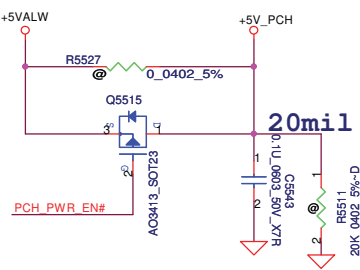
**+3VALW to +3VS**



**+3VALW to +3V\_PCH**



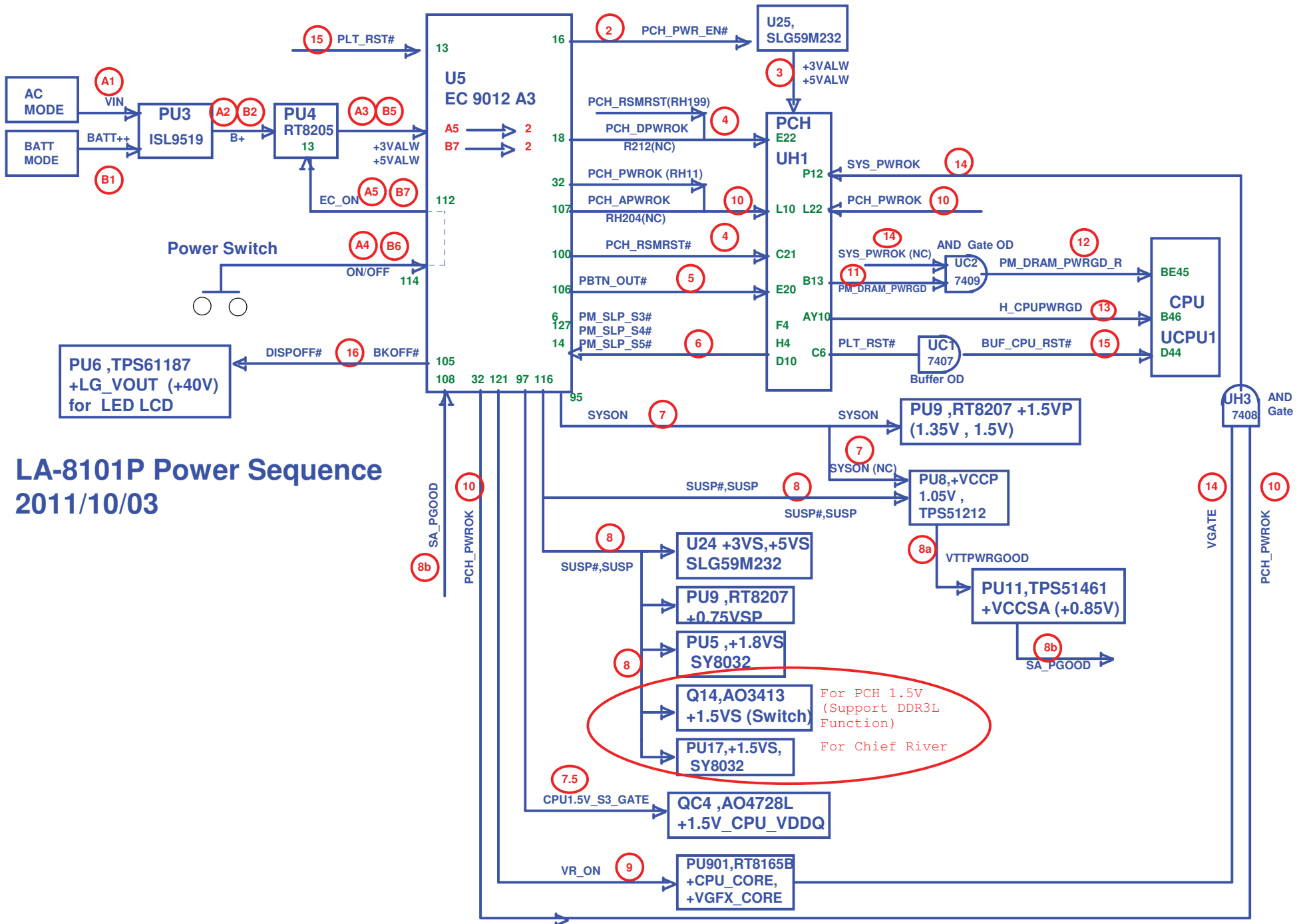
**+5VALW to +5V\_PCH**



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Size	Document Number	LA-8101P		Rev
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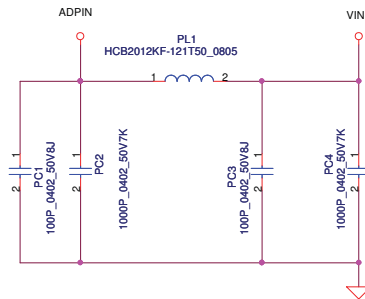




# LA-8101P Power Sequence

2011/10/03

LA-8101P Security Classification		Compal Secret Data		Title <b>EE PIR</b>	
Issued Date	2010/04/26	Deciphered Date	2011/10/18	Size A3	Document Number LA-8101P
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2011/07/12  
 deletet pre-charge circuit

2011/10/17  
 change to DCIN connector  
 2011/10/21  
 delete the DCIN connector for QAU20

2011/07/06  
 for KB9012 only, delete the 51\_ON# circuit

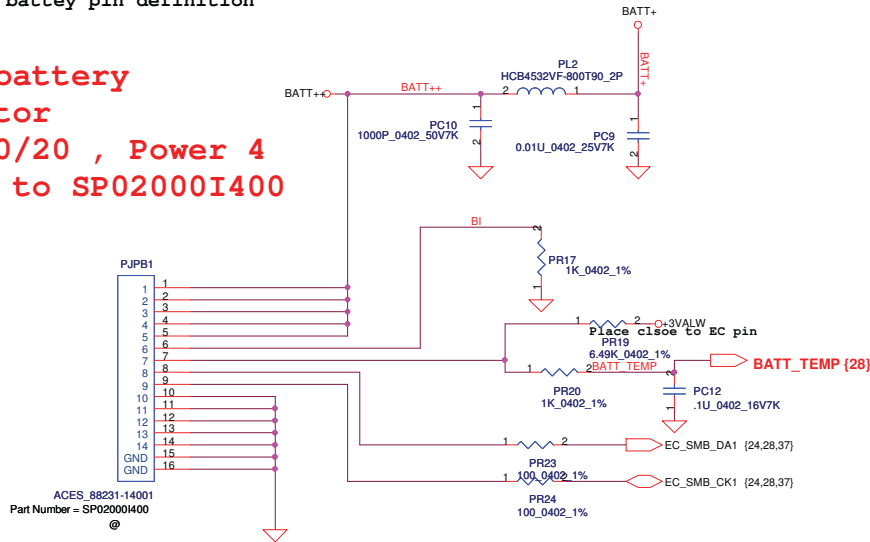
2011/06/27  
 change PU1 from SOT89-3 to SOT23-5  
 2011/10/26  
 delete the RTC battery and the +CHGRTC circuit

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				Size Custom	Document Number
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PJPB1 battery connector  
 2011/07/06  
 change 14 pin to 12pin  
 2011/07/12  
 swap the BATT+ and GND  
 change 12 pin to 14 pin  
 2011/07/20  
 change the battey pin definition

2011/10/20  
 change to PL2 Bead  
 2011/11/08  
 change to SM01000JR00

PJPB1 battery  
 connector  
 2011/10/20 , Power 4  
 modify to SP02000I400

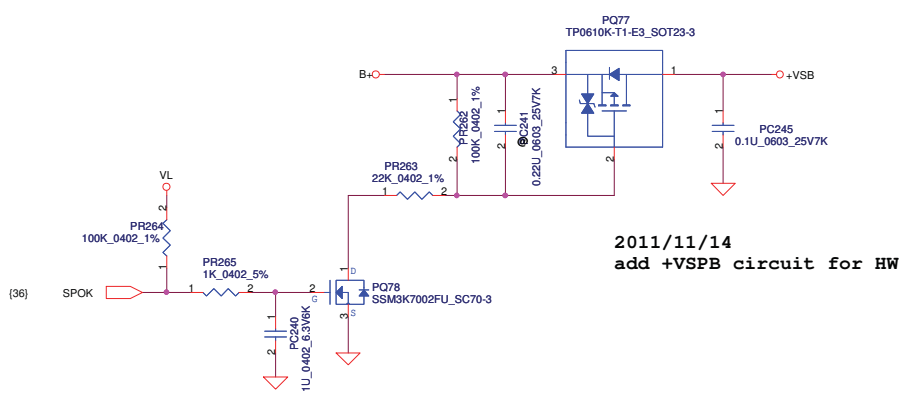
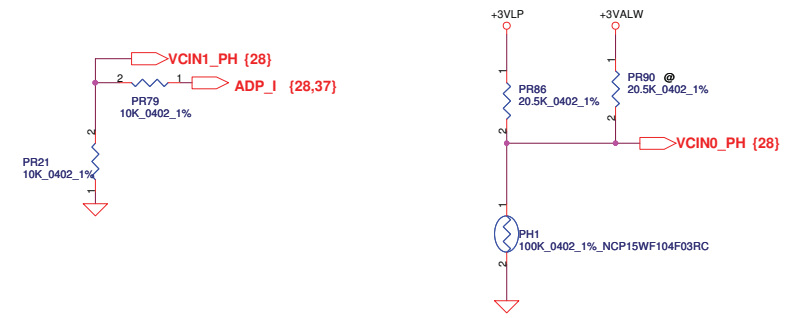


PH1 under CPU botten side :  
 CPU thermal protection at 93 +-3 degree C  
 Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit  
 (Vth = 0.825V)

For KB912 --> Remove PU1 circuit, but keep PR18  
 PH1, PR79, PQ19, PR21, PR88, PR87  
 VCIN0\_PH-->NTC\_V  
 VCIN1\_PH-->Turbo\_V

2011/10/24  
 delete G718 circuit for EN9012



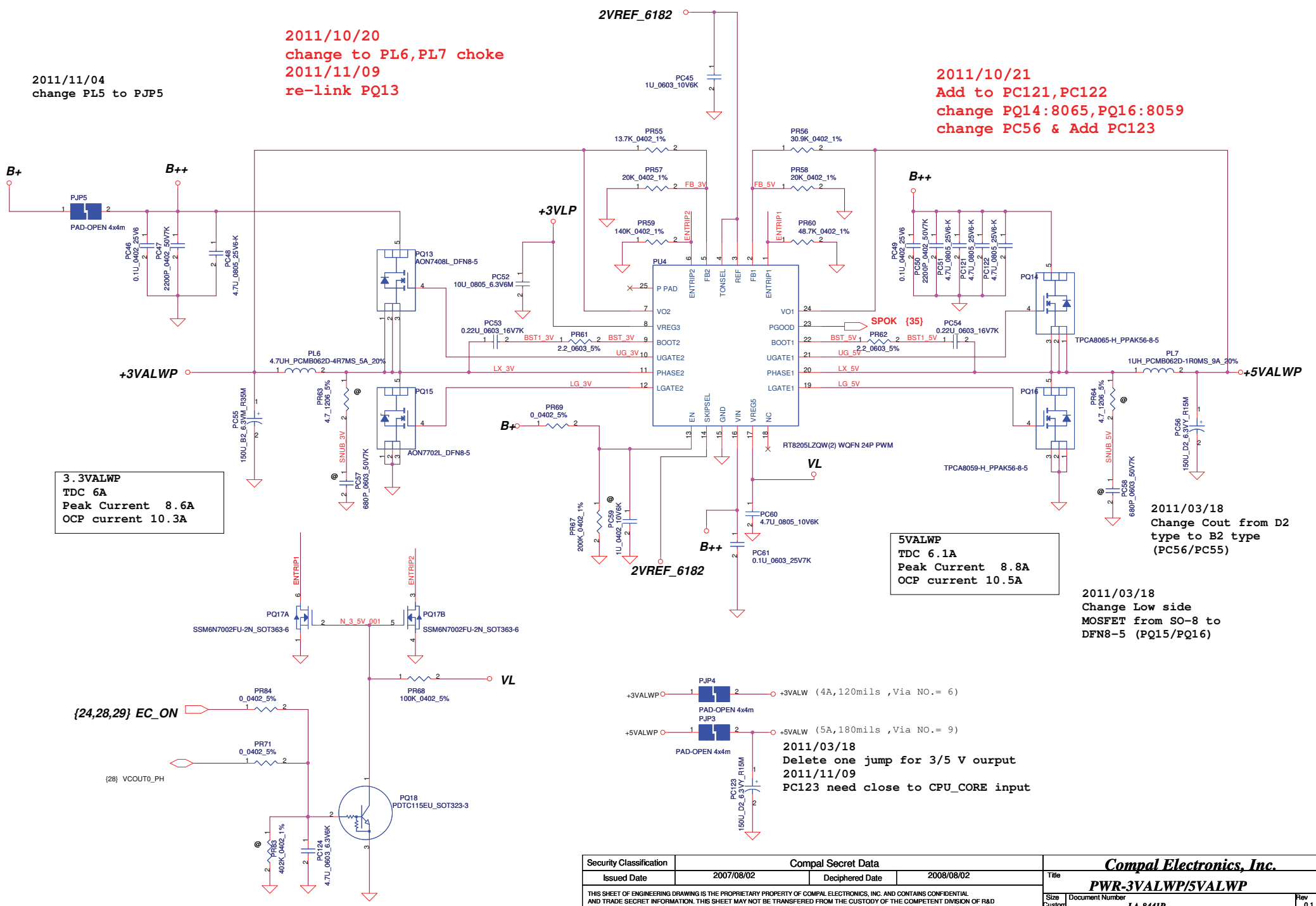
2011/11/14  
 add +VSPB circuit for HW

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2011/10/20  
change to PL6, PL7 choke  
2011/11/09  
re-link PQ13

2011/11/04  
change PL5 to PJP5

2011/10/21  
Add to PC121, PC122  
change PQ14:8065, PQ16:8059  
change PC56 & Add PC123



3.3VALWP  
TDC 6A  
Peak Current 8.6A  
OCP current 10.3A

5VALWP  
TDC 6.1A  
Peak Current 8.8A  
OCP current 10.5A

2011/03/18  
Change Cout from D2  
type to B2 type  
(PC56/PC55)

2011/03/18  
Change Low side  
MOSFET from SO-8 to  
DFN8-5 (PQ15/PQ16)

2011/03/18  
Delete one jump for 3/5 V output  
2011/11/09  
PC123 need close to CPU\_CORE input

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Size	Document Number	Rev		Date	
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				Sheet	36 of 46

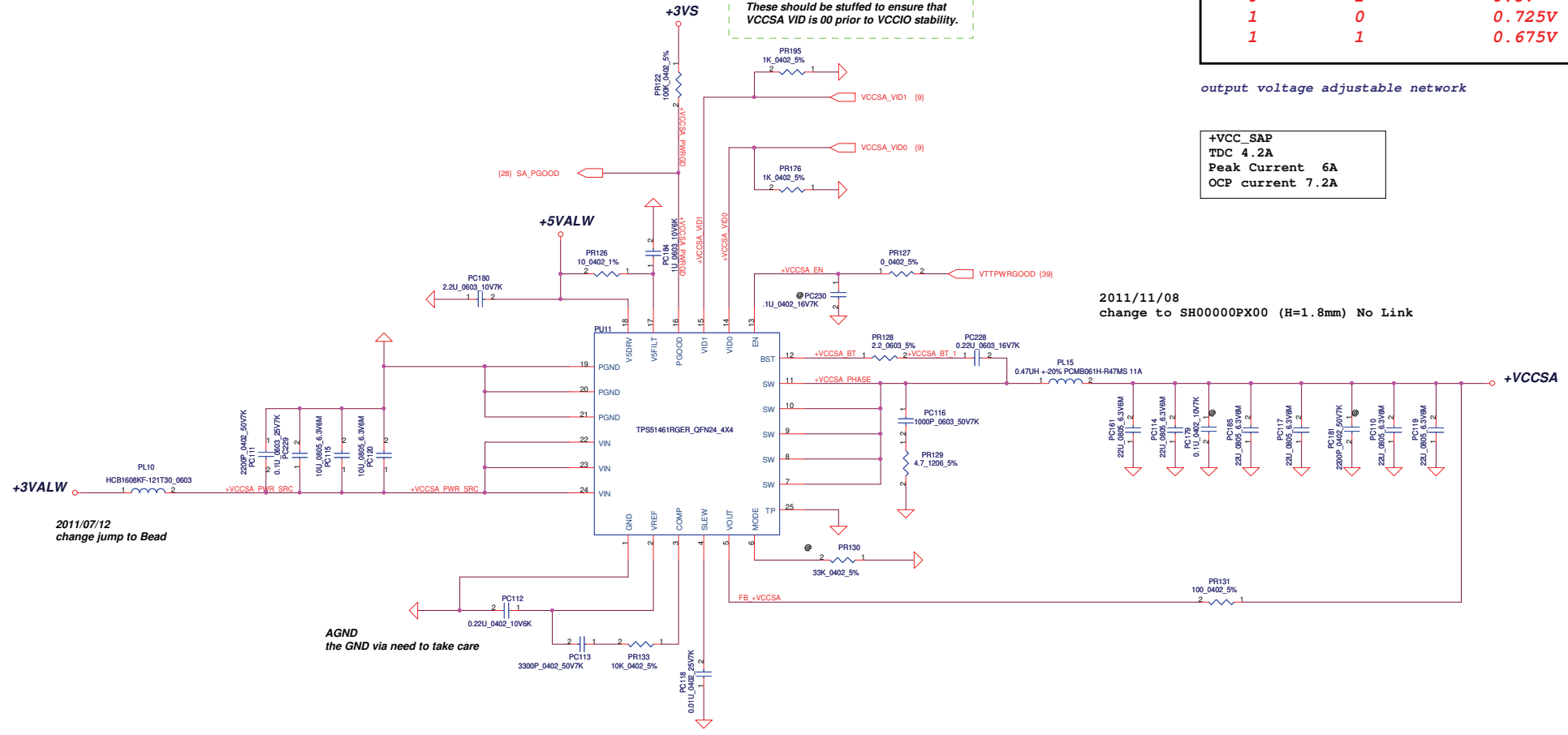


VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC\_SAP  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



2011/07/12  
change jump to Bead

AGND  
the GND via need to take care

2011/11/08  
change to SH00000PX00 (H=1.8mm) No Link

2011/07/12  
delete output jump  
delete AGND jump

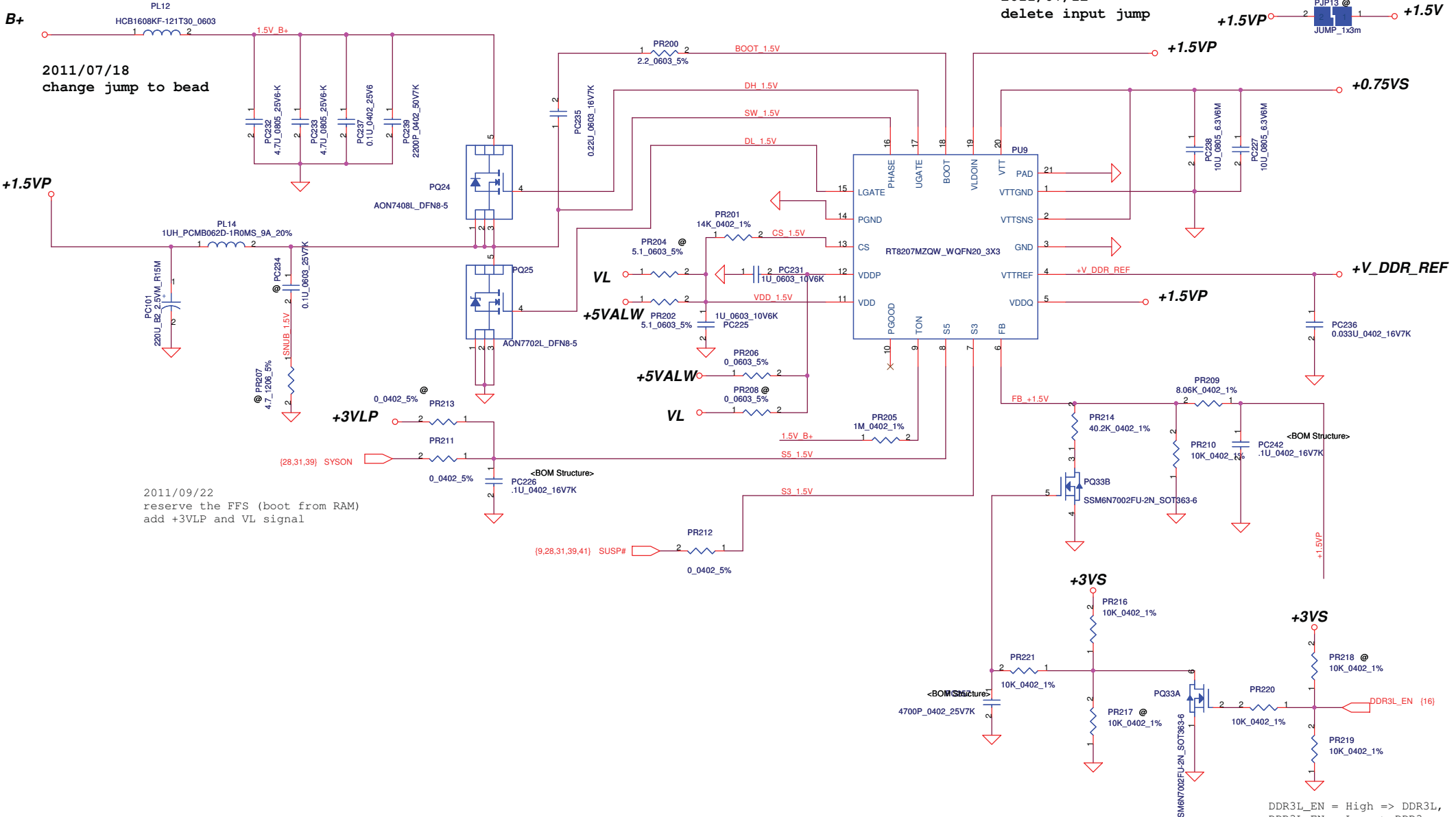


1.5Volt +/- 5%  
 TDC 4.48A  
 Peak Current 6.4A  
 OCP current 7.68A

Mode SYSON SUSP# +0.75V\_P +V\_DDR\_REF  
 S5 L L off off  
 S3 H L off on  
 S0 H H on on  
 Note: S3 - sleep ; S5 - power off

0.75Volt +/- 5%  
 TDC 0.525A  
 Peak Current 0.75A  
 OCP Current 0.9A

2011/07/12  
 delete input jump



2011/07/18  
 change jump to bead

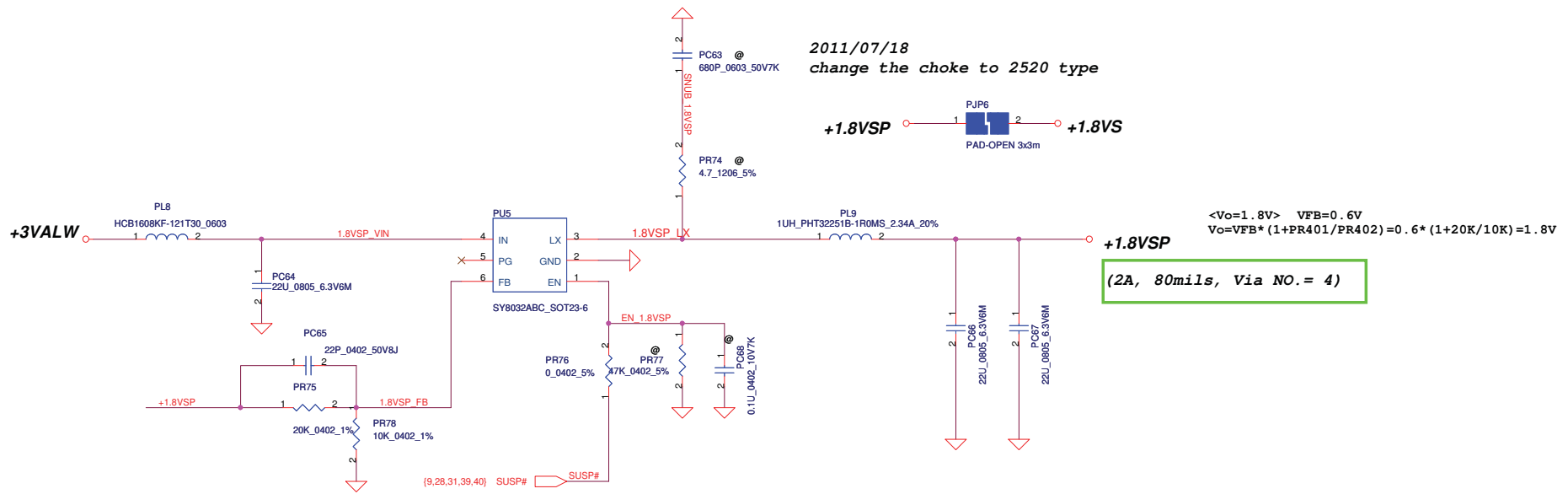
2011/09/22  
 reserve the FFS (boot from RAM)  
 add +3VLP and VL signal

DDR3L\_EN = High => DDR3L,  
 DDR3L\_EN = Low => DDR3

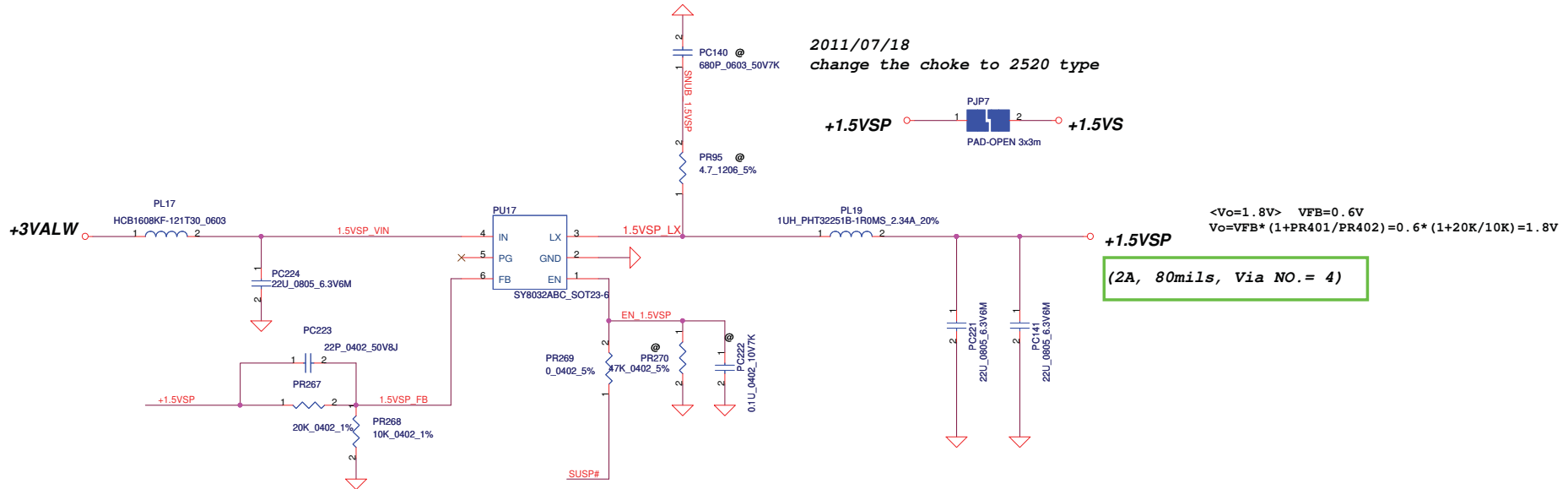
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Date			Monday, November 14, 2011	Sheet	40 of 46



2011/07/18  
change the choke to 2520 type



2011/07/18  
change the choke to 2520 type

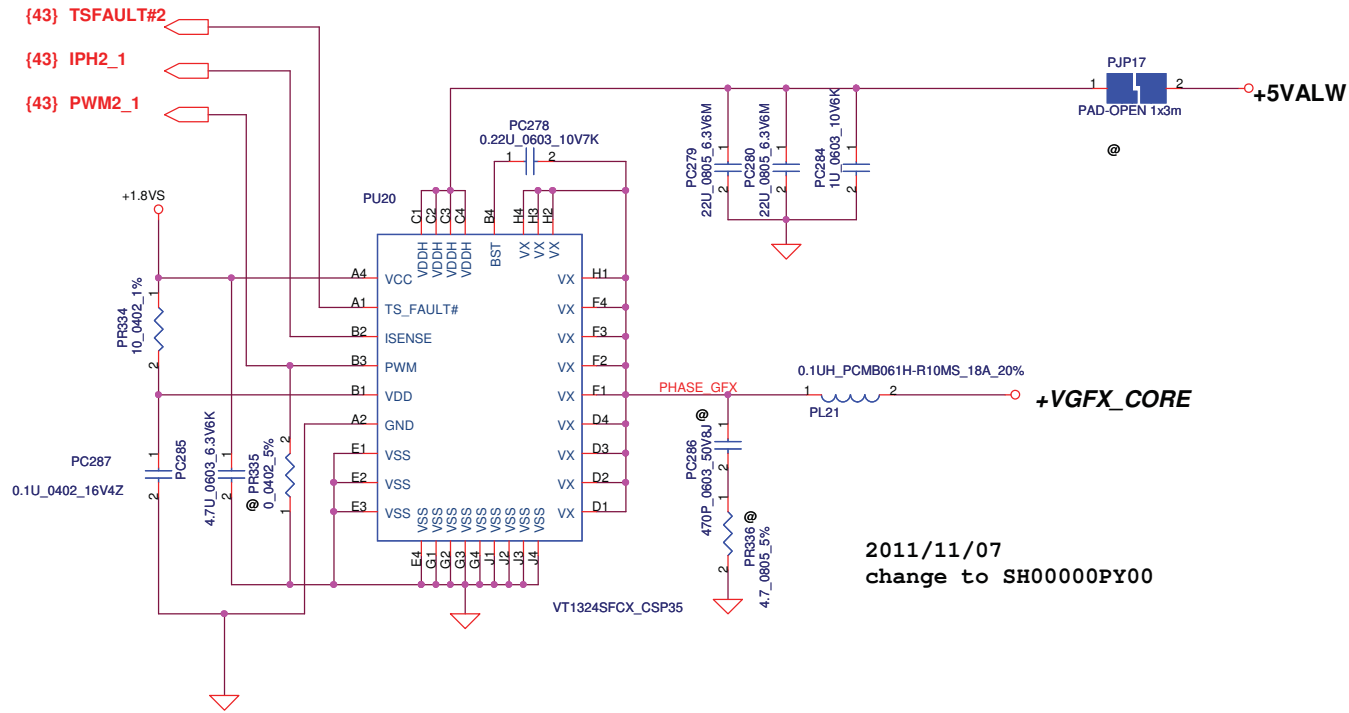


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2011/10/24  
 delete the panel power circuit

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VCC\_GFXCORE  
 TDC 38A  
 Peak Current 46A  
 OCP current 57.18A  
 Load line -3.9mV/A

2011/11/07  
 change to SH00000PY00

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