Compal Confidential

ZIVY2/ZIVY3 M/B Schematics Document

Intel Shark Bay + N15P-GX
(Crescent Bay + N15P-GX)

LA-B111P

2014-02-25

REV:1.0

Security Classification	Compal Secret Data		
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Title: Cover Sheet			
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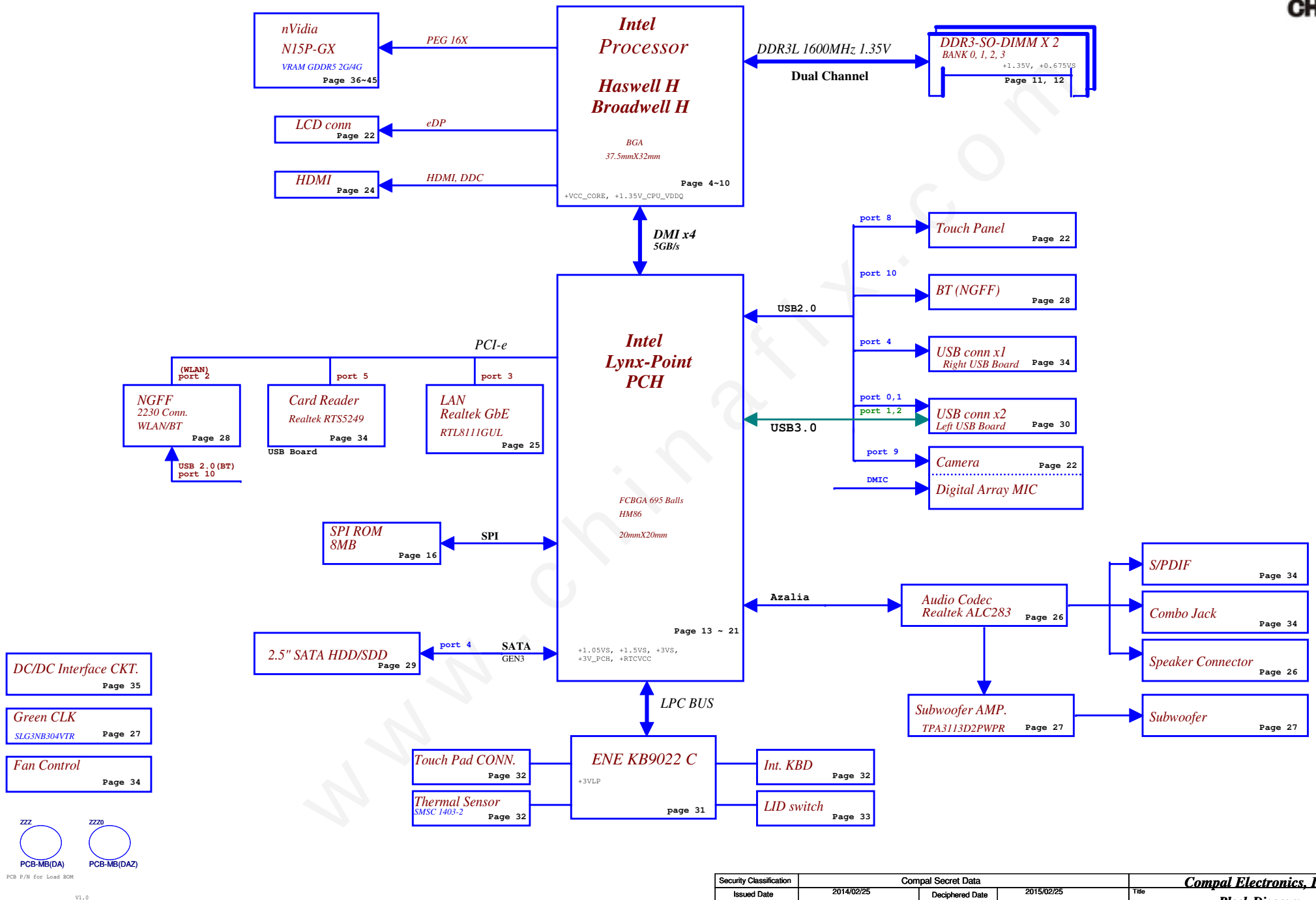
Shark Bay/Crescent Bay



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Title: **Block Diagram**

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	B+	+5VALW +3VALW +12VS_PANEL	+3V_PCH	+1.35V	+5VS +3VS +1.5VS +1.05VS +VCC_CORE +0.675VS +12VS
S0	O	O	O	O	O
S3	O	O	O	O	X
DeepS3	O	O	X	O	X
S5 S4/AC	O	O	X	X	X
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

USB Port Table

	USB 2.0	Port	USB 3.0	Port	5 External USB Port
EHCI1	UHCI0	0	XHCI	1	Left USB3.0
		1	XHCI	2	Left USB3.0
	UHCI1	2			
		3			
	UHCI2	4			Right USB2.0
		5			
	UHCI3	6			
		7			
EHCI2	UHCI4	8			Touch screen
		9			Camera
	UHCI5	10			WLAN
		11			
	UHCI6	12			
		13			

Board ID Table for AD channel

Vcc	3.3V
Ra / Rc	100K +/- 1%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	12K +/- 1%	0.347 V	0.354 V	0.360 V
2	15K +/- 1%	0.423 V	0.430 V	0.438 V
3	20K +/- 1%	0.541 V	0.550 V	0.559 V
4	27K +/- 1%	0.691 V	0.702 V	0.713 V
5	33K +/- 1%	0.807 V	0.819 V	0.831 V
6	43K +/- 1%	0.978 V	0.992 V	1.006 V
7				

BOM Structure Table

BTO Item	BOM Structure
45 LEVEL	45@
Connector	CONN@
KB ZIVY2 (15")	KB15@
KB ZIVY3 (17")	KB17@
ZIVY2 (15")	15@
ZIVY3 (17")	17@
Subwoofer	WF@
DIS SKU	DIS@
Nvidia GC6 state	SW@
Haswell	HW@
Broadwell	BW@
Deep S3	DS3@
NO Deep S3	NODS3@
Green clk support	GCLK@
No Green clk support	NOGCLK@
Unpop	CMOS@/NCMOS@
Unpop	@
EMI Pop	EMI@
EMI unpop	@EMI@
ESD Pop	ESD@
ESD unpop	@ESD@
SATA re-driver	TI@/Parade@

EC SM Bus1 address

Device	Address
Smart Battery Charger	0b 0001 0010 (0x12H)

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2-AIZL-TR	1001_101xb
PCH SML1 Bus address	
nVidia N15P-GX	0x9E

PCH SM Bus address

Device	Address
DDR DIMM0	1010 000x A0h
DDR DIMM1	1010 010x A4h
Click Pad	

PCH SML0 Bus address

Device	Address

Symbol Note :

: means Digital Ground : means Analog Ground

Install below 43 level BOM structure for ver. 0.1

CPU part

CPU1@ U1 R3 — I5_4200H 2.8G SA000071N20

CPU3@ U1 R1 — I7_4750HQ 2G SA00007A900 — 4319S138L03 V2G

CPU4@ U1 R3 — I7_4702HQ 2.2G SA00006TQ20 — 4319S138L04 V4G

CPU5@ U1 R3 — I7_4700HQ 2.4G SA00006TP20 — 4319S138L05 V4G

CPU6@ U1 — I7_4850HQ 3.5G SA00007J710

CPU7@ U1 — I7_4950HQ 3.6G SA00007A800

SMBUS Control Table

	SOURCE	BATT	KB9022	SODIMM	Touch Pad	Thermal sensor	VGA
SMB_EC_CK1 SMB_EC_DA1	KB9022 +3VLP_EC	V	X	X	X	X	X
SMBCLK SMBDATA	PCH +3V_PCH	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3V_PCH	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3V_PCH	X	V +3VS	X	X	V +3VS	V +3VS_DGPU

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Title: Notes List

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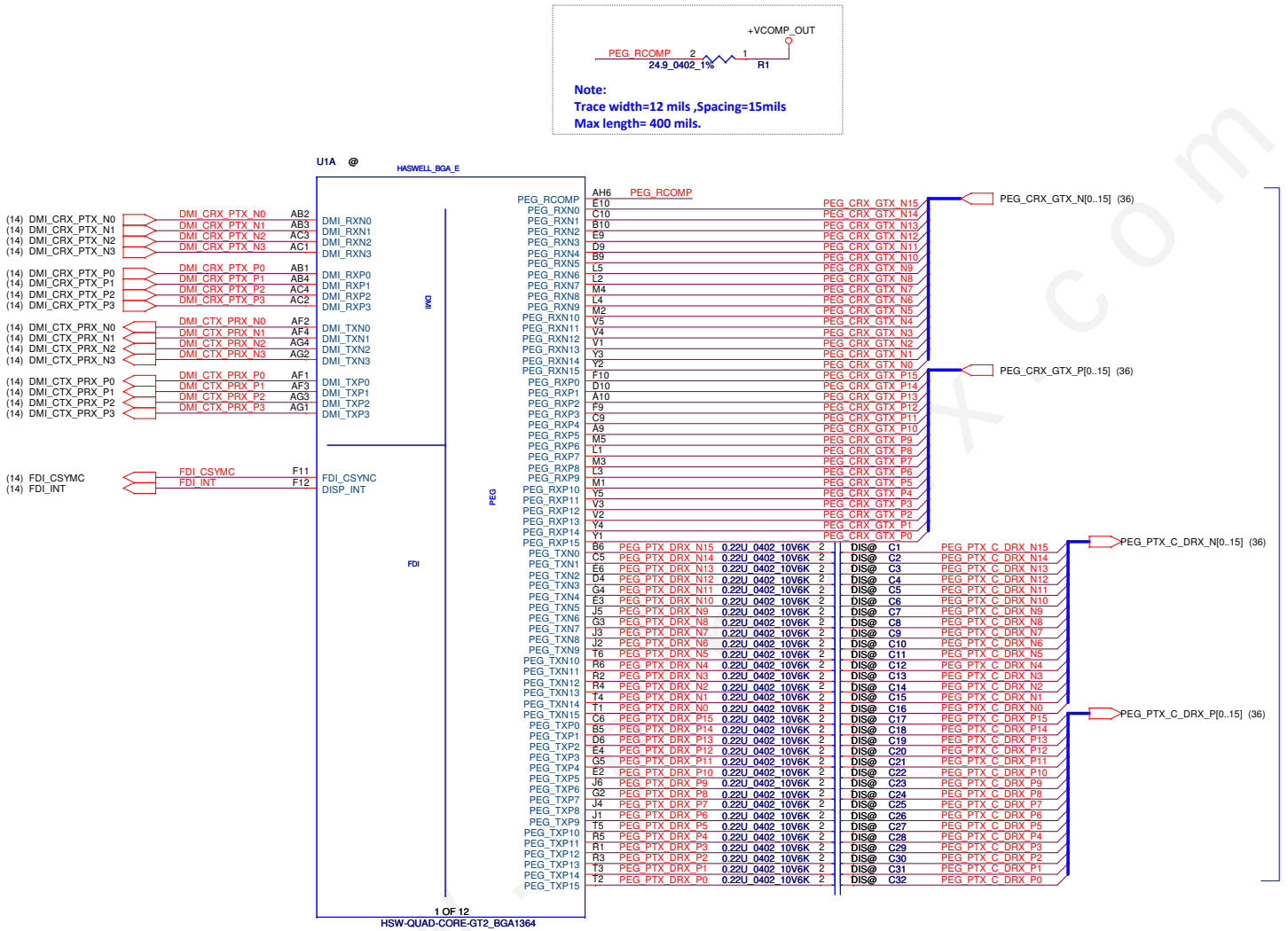

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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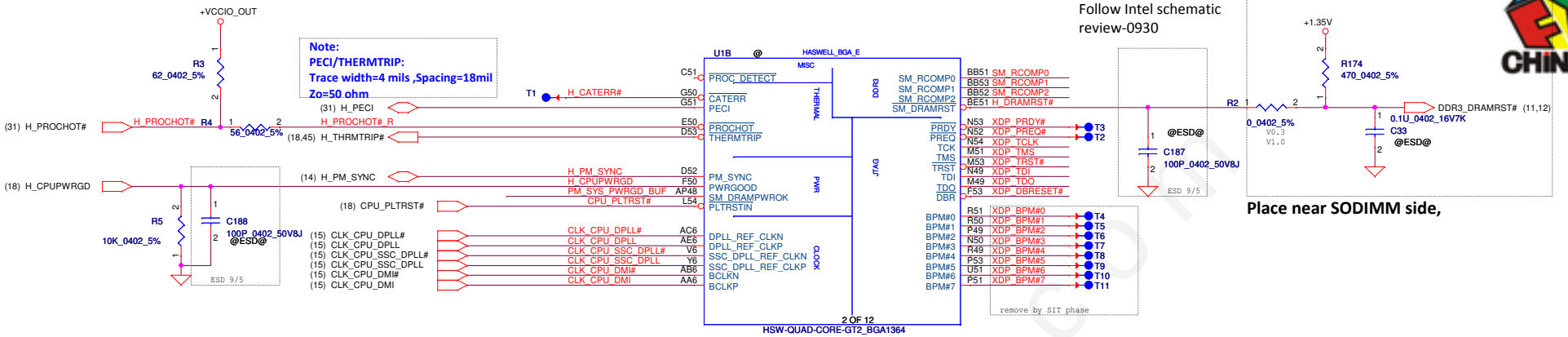
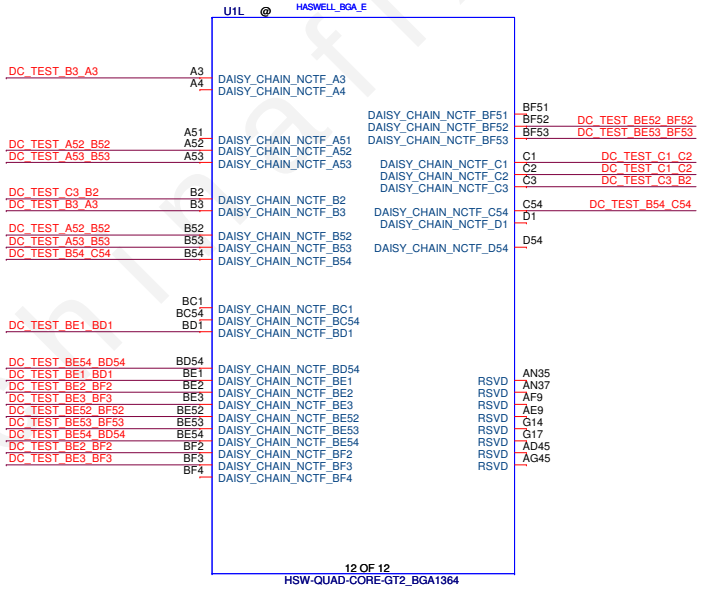
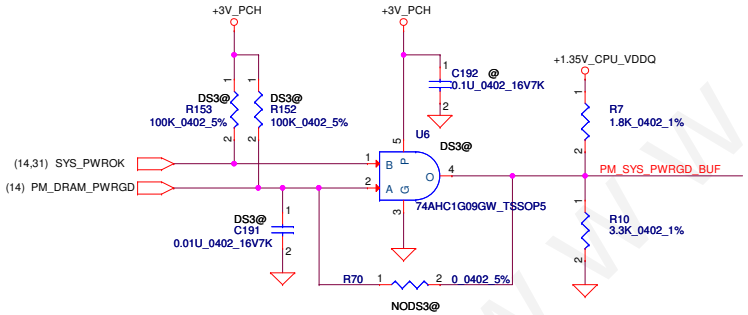
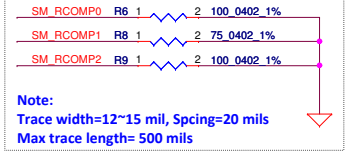




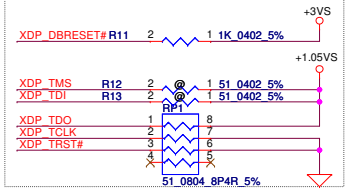
SM_DRAMPWROK with DDR Power Gating Topology



DDR3 COMPENSATION SIGNALS



PU/PD for JTAG signals



TMS/TDI no require pull high on Check list

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Title: PROCESSOR(2/7) PM,XDP,CLK

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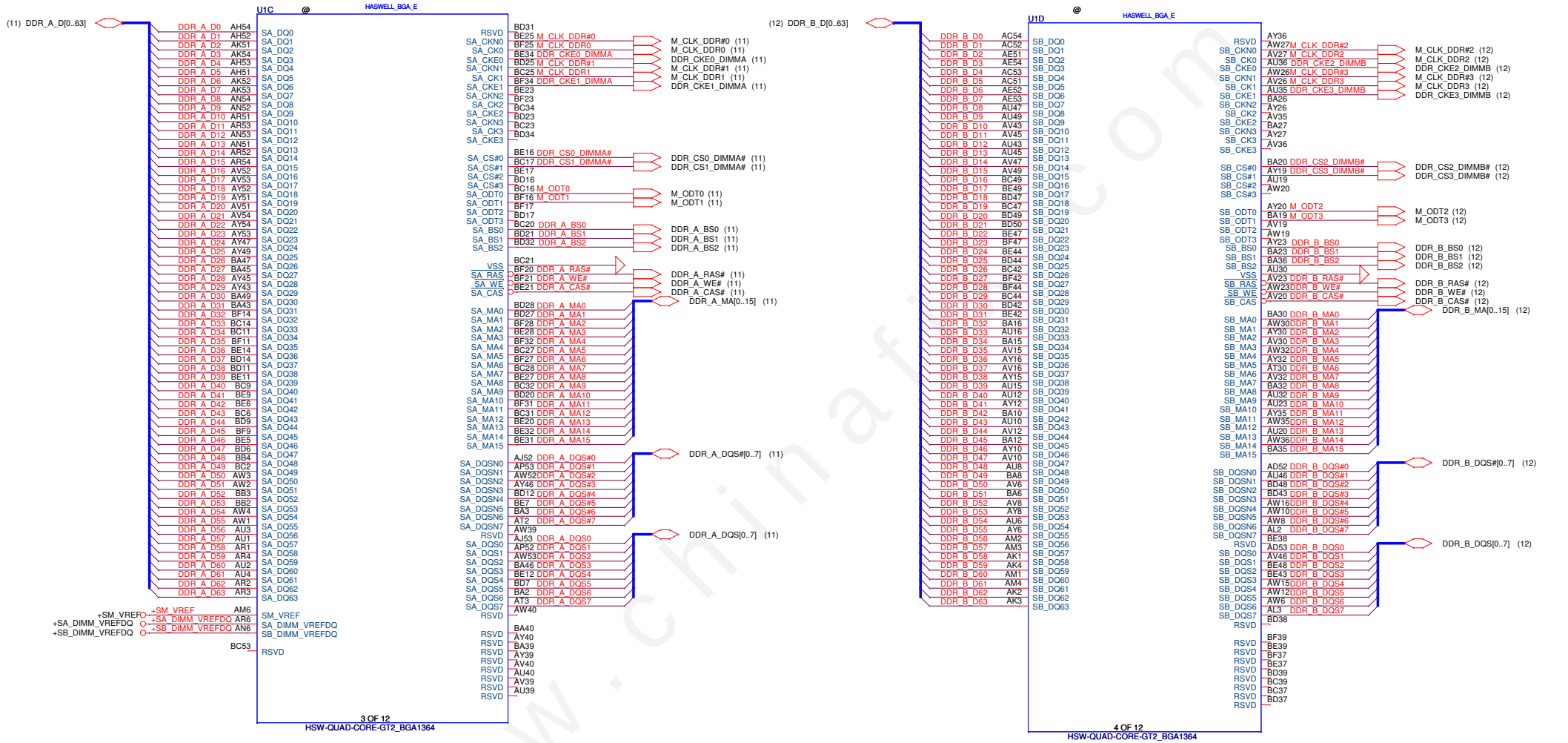

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Title: **PROCESSOR(3/7) DDRIII**

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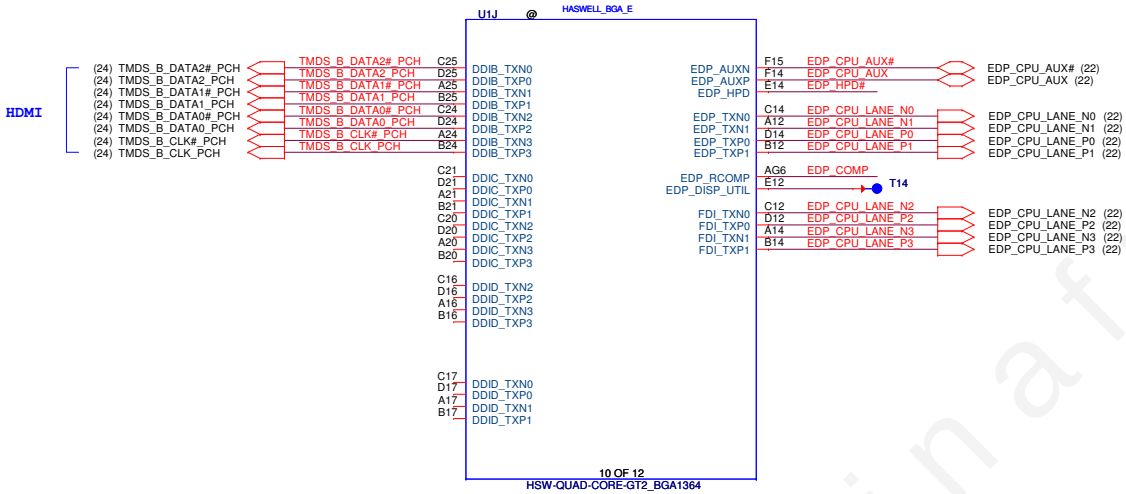
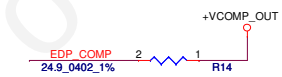
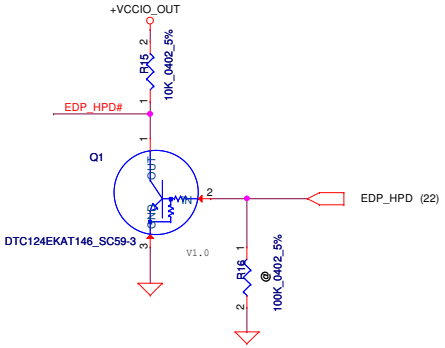


COMPENSATION PU FOR eDP



Note:
Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

HPD INVERSION FOR EDP



HPD is a active-high signal from device.
The HPD processor input is
active-low signal.

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Title: PROCESSOR(4/7) eDP,DP and HDMI

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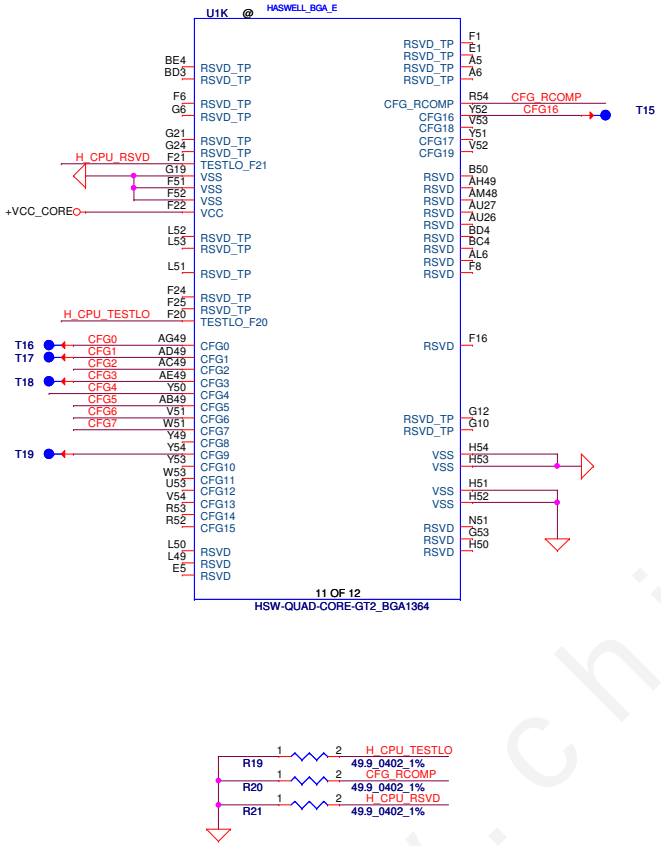
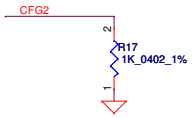
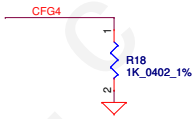
CFG Straps for Processor

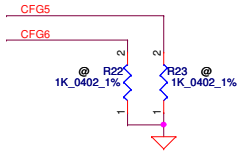




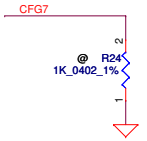
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(5/7) RSVD,CFG

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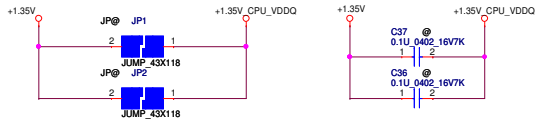
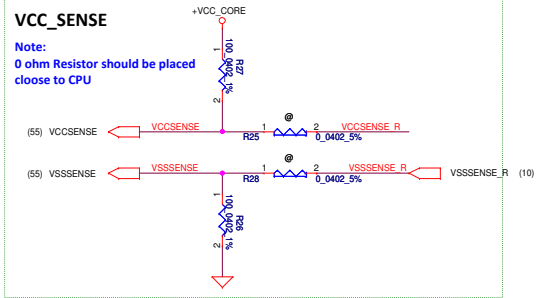
+1.35V_CPU_VDDQ Source

Note:
Intel Shark Bay
Removed the S3 power reduction circuit.

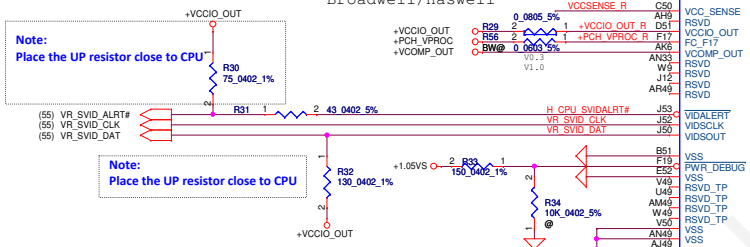


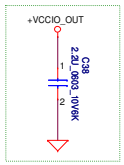
VCC_SENSE

Note:
0 ohm Resistor should be placed cloose to CPU

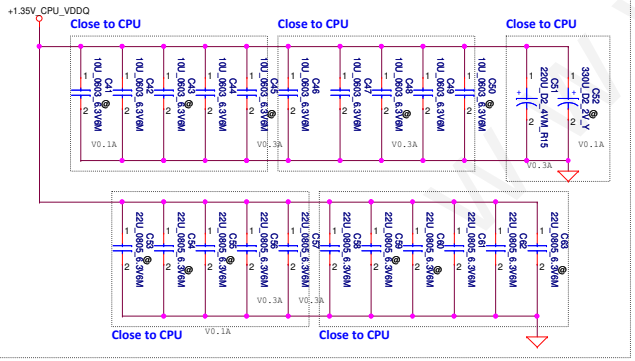


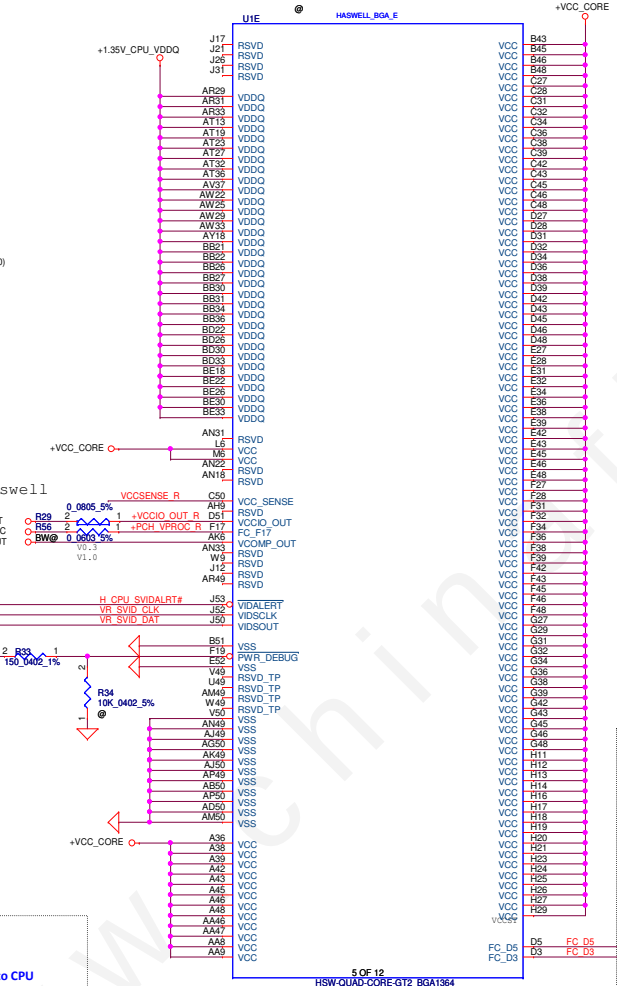
Broadwell/Haswell

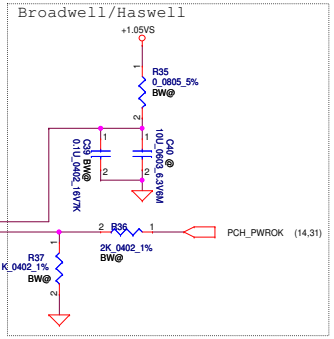


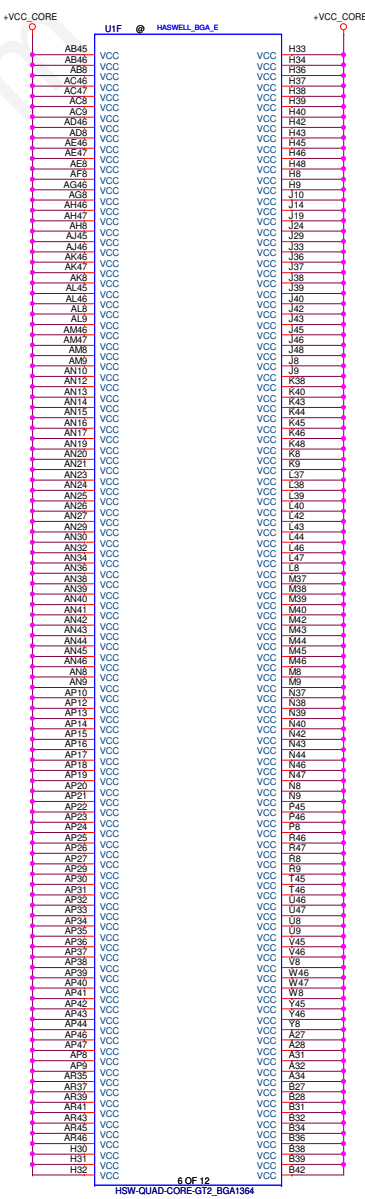


VDDQ DECOUPLING (Follow INTEL DG)









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Title	PROCESSOR(6/7) PWR		
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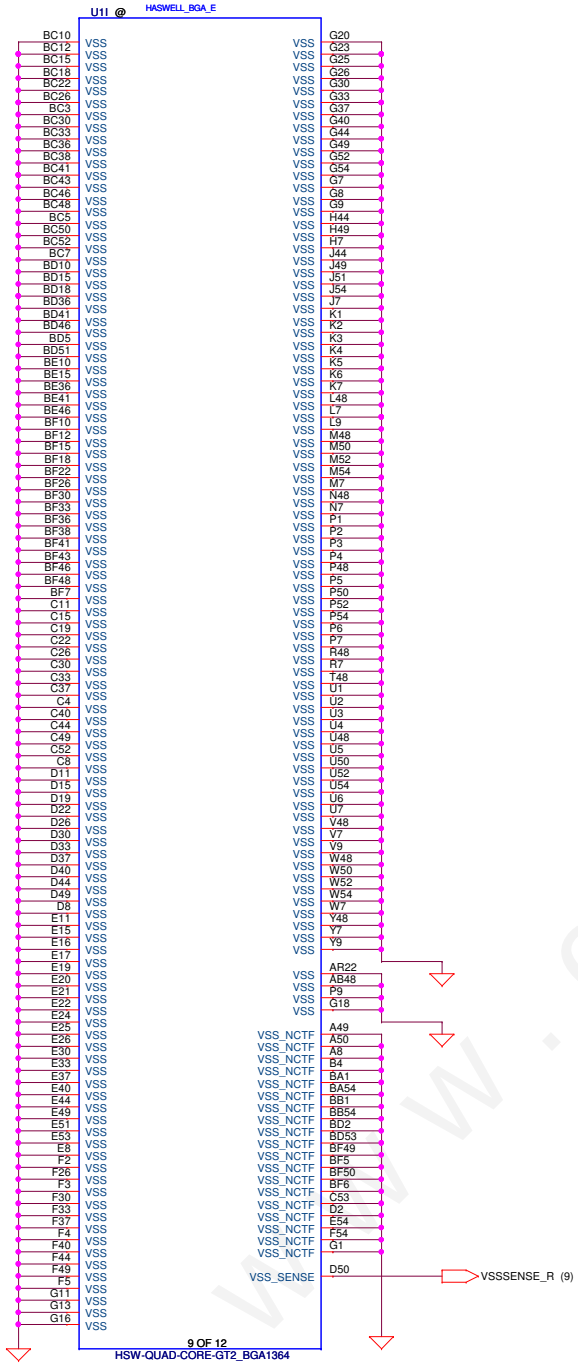

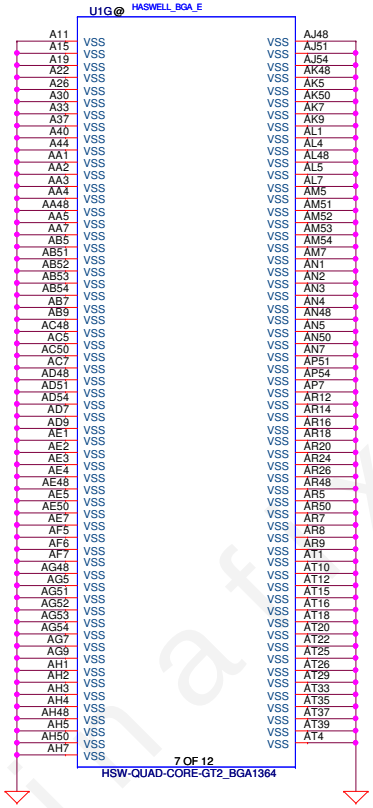

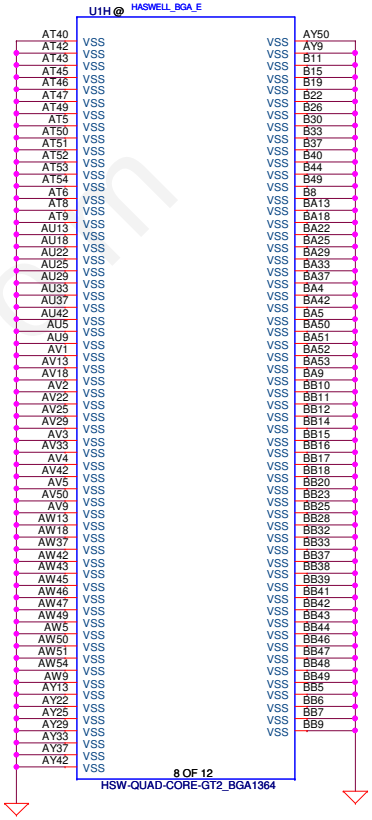

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Title: PROCESSOR(7/7) VSS

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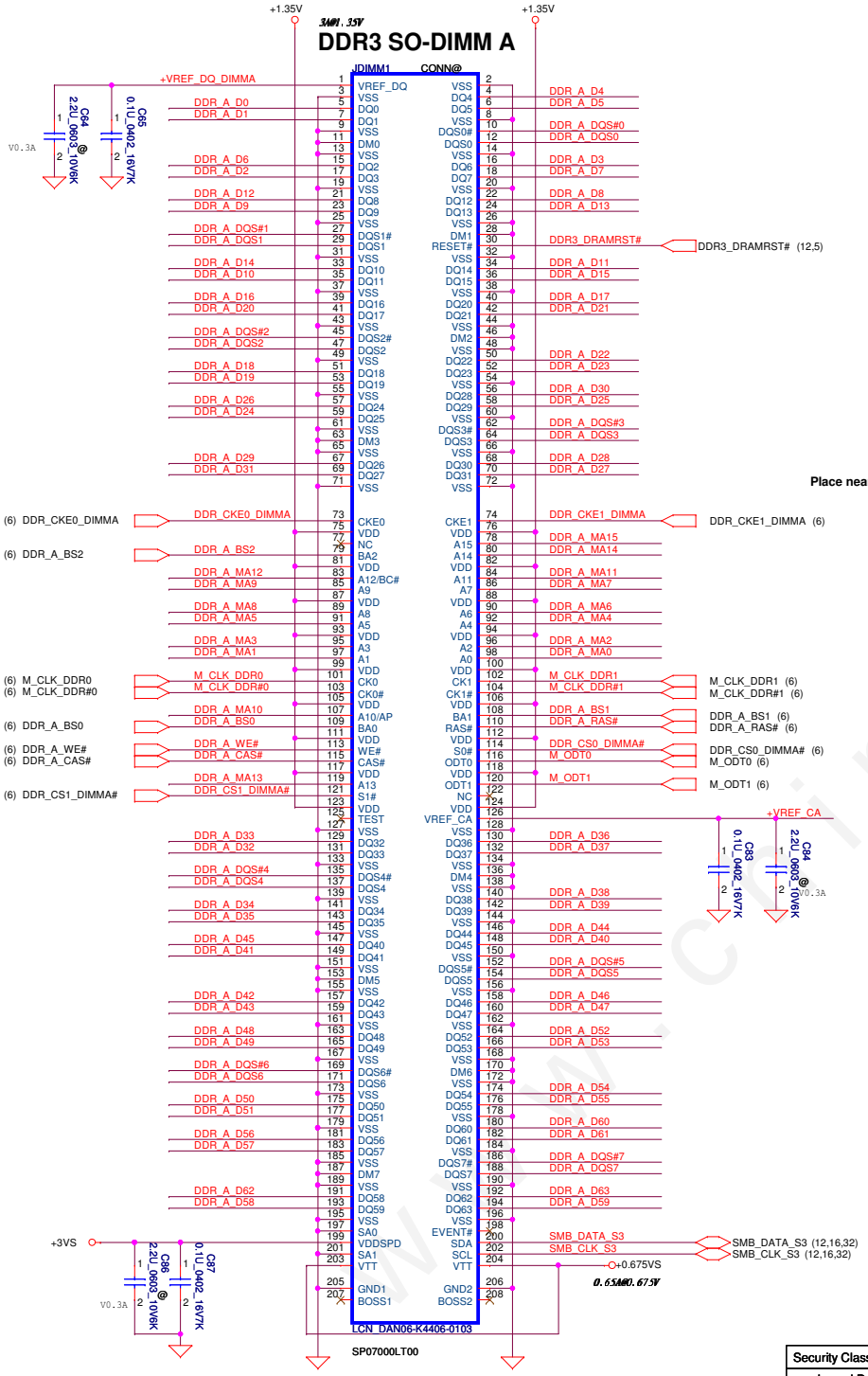
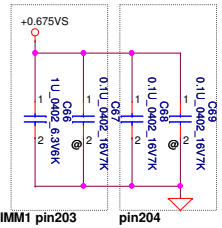
DDR3 SO-DIMM A

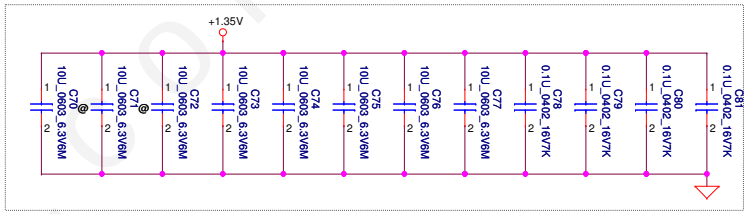


(6) DDR_A_D[0..63]
(6) DDR_A_DQS[0..7]
(6) DDR_A_DQS#[0..7]
(6) DDR_A_MA[0..15]

Layout Note:
Place near JDIMM1

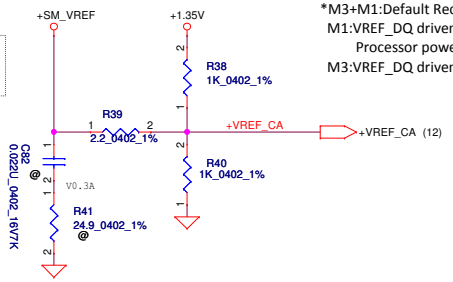


Layout Note:
Place near JDIMM1



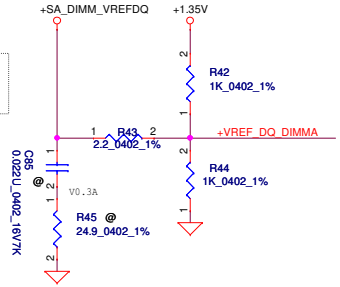
CPU DRIVER VREF PATH IS DEFAULT

Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes



*M3+M1:Default Recommendation
M1:VREF_DQ driven by a voltage Divider Network during Processor power-off state.
M3:VREF_DQ driven by Processor.

Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes



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Title: DDRIII-SODIMM SLOT1

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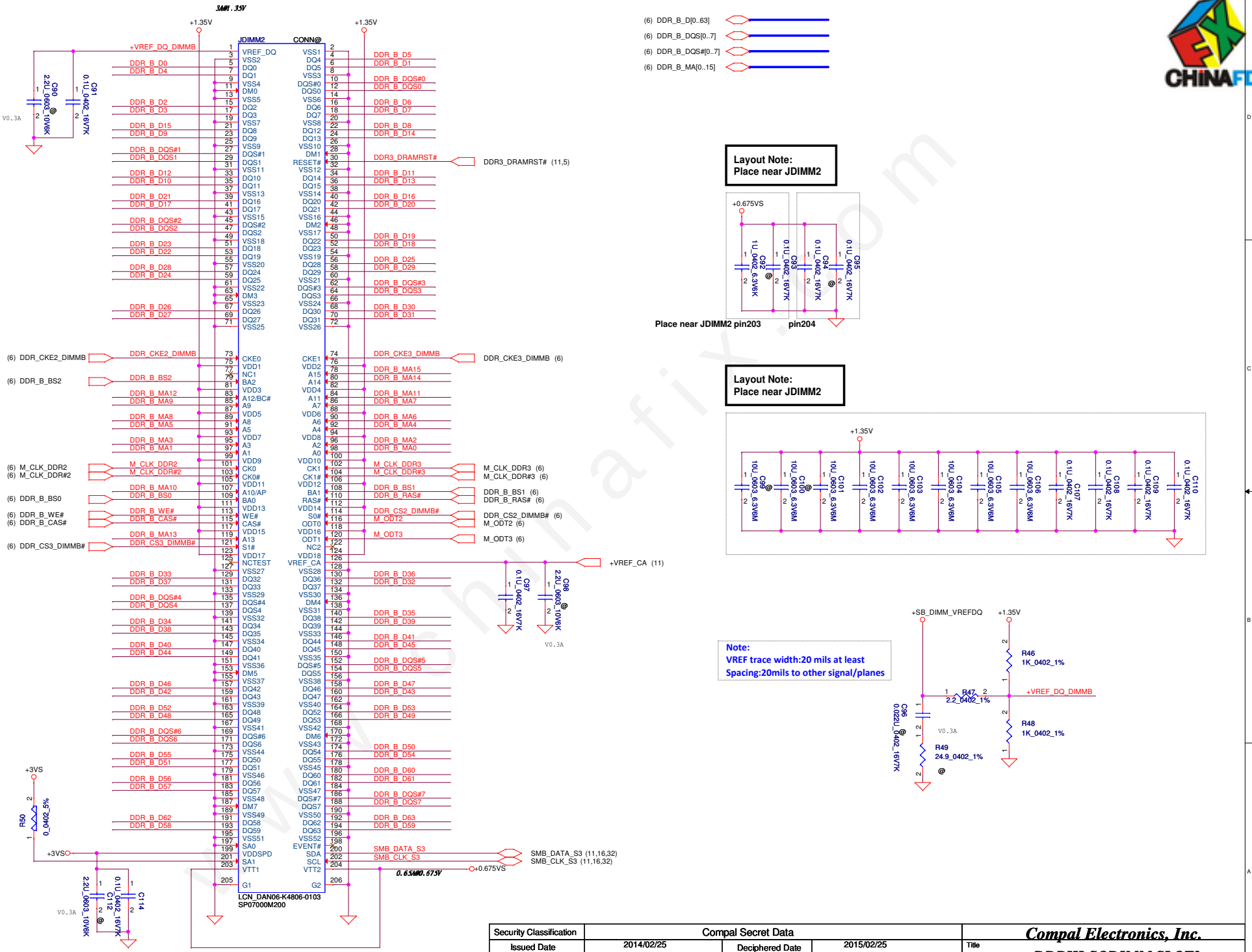

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Compal Electronics, Inc.	
Title	DDRIII-SODIMM SLOT2
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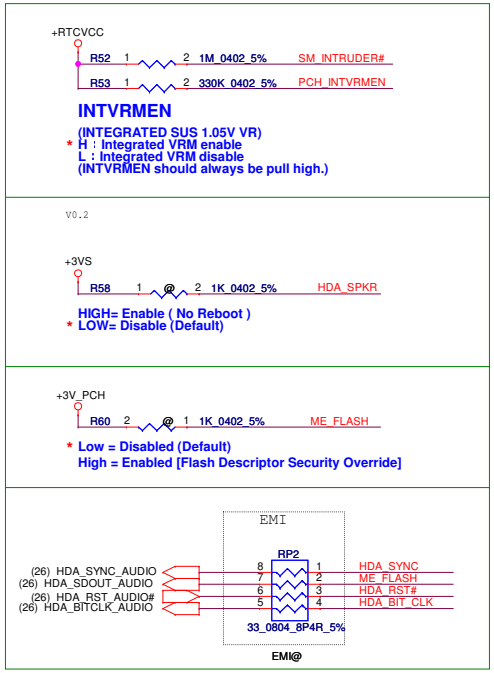
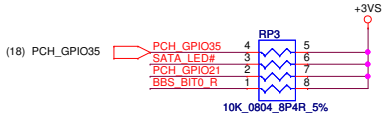
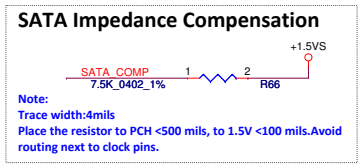
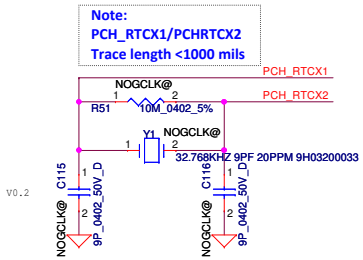
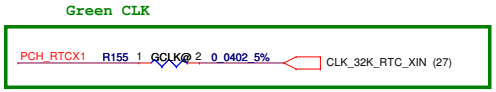


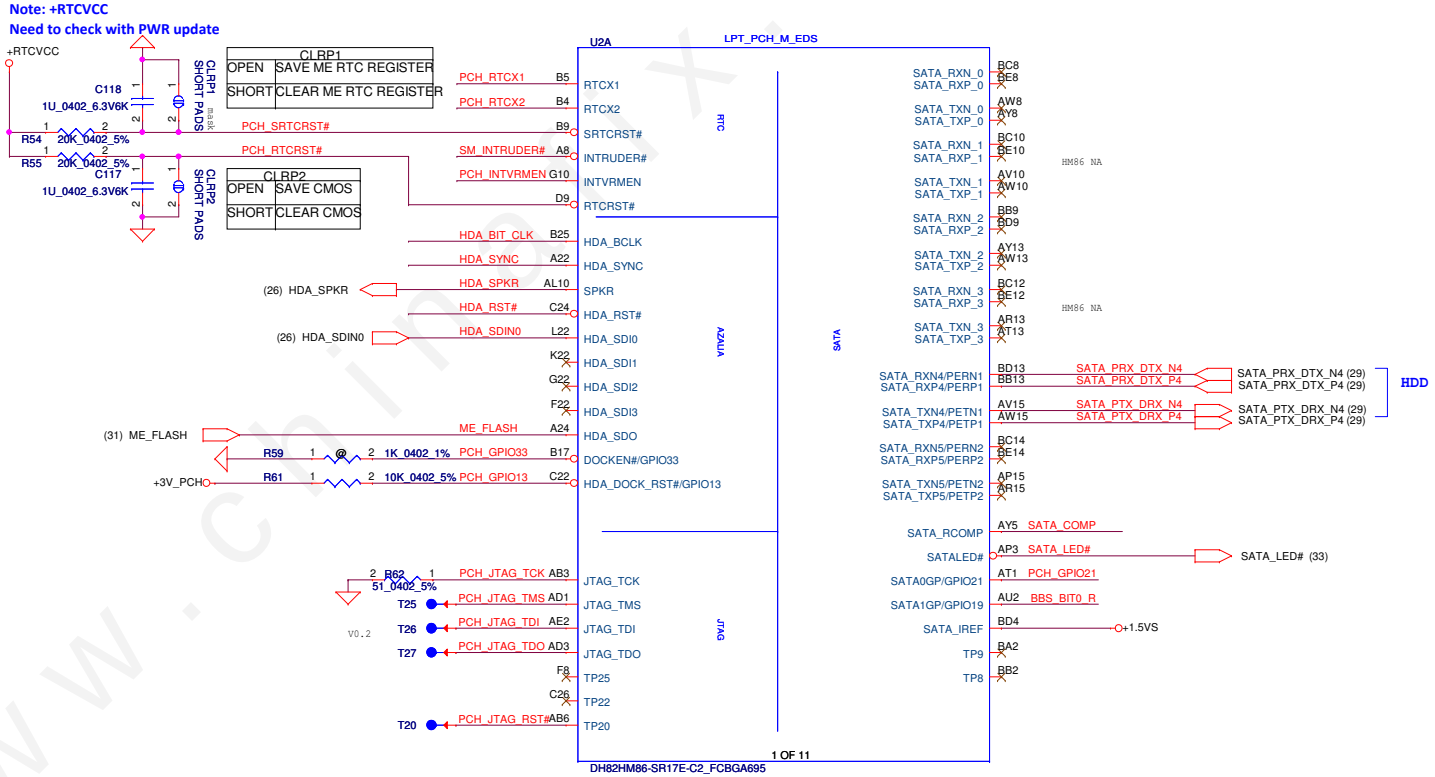
V0.2











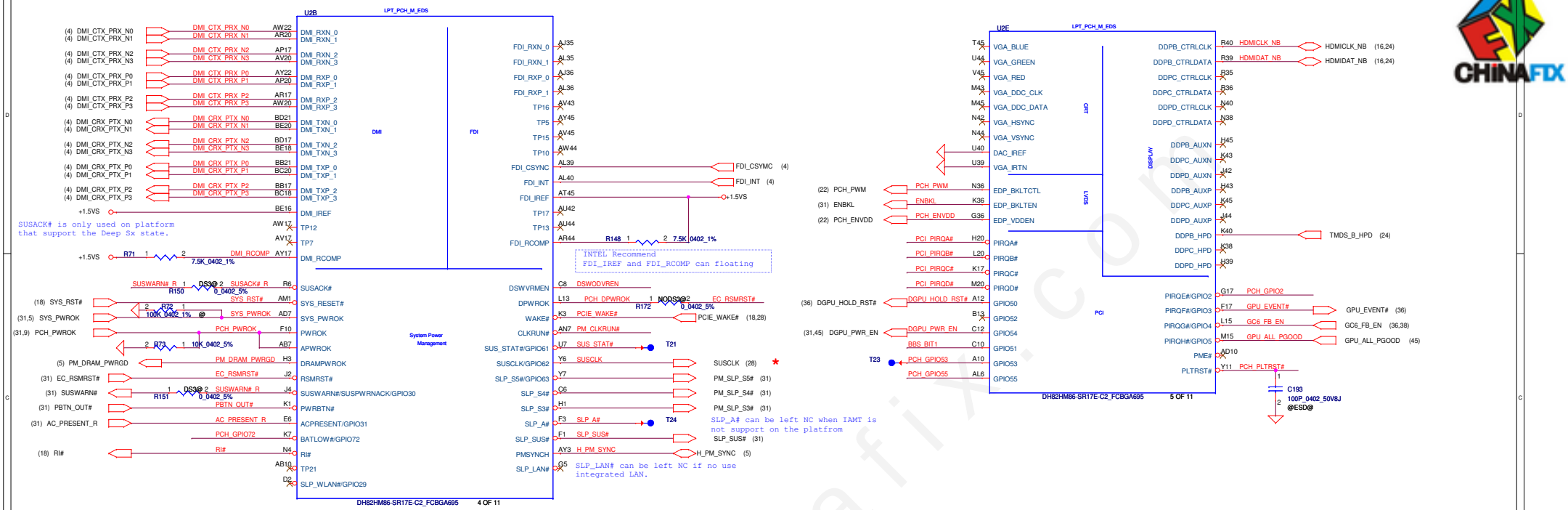
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

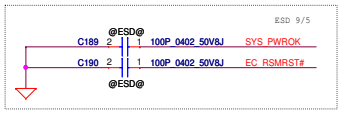
Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 13 of 59



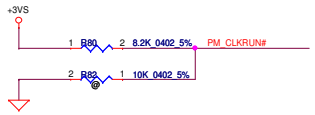


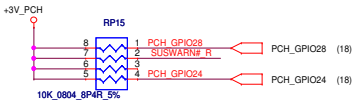
APWROK can be connect to PWROK if iAMT disable

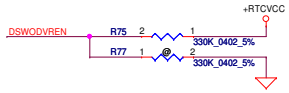
SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.

Follow Intel schematic review-0930

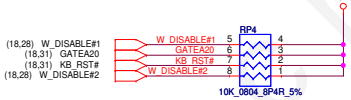
CLKRUN#:
External pull up to core well is required.

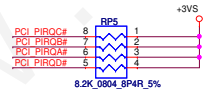




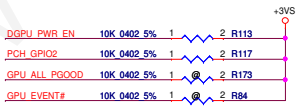


DSWODVREN - On Die DSW VR Enable
H : Enable (DEFAULT)
L : Disable

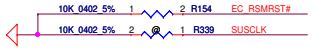


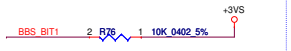


V0.2



Follow Intel schematic review-0930

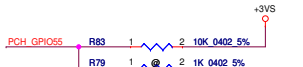




Boot BIOS Strap (GPIO51)

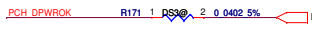
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	* SPI

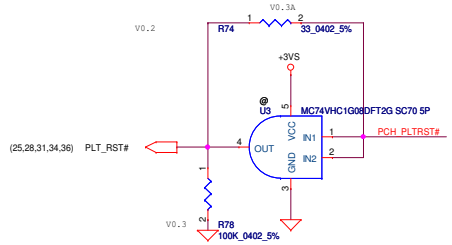
GPIO51 needs pull up 10k to ensure proper behavior.



GPIO55

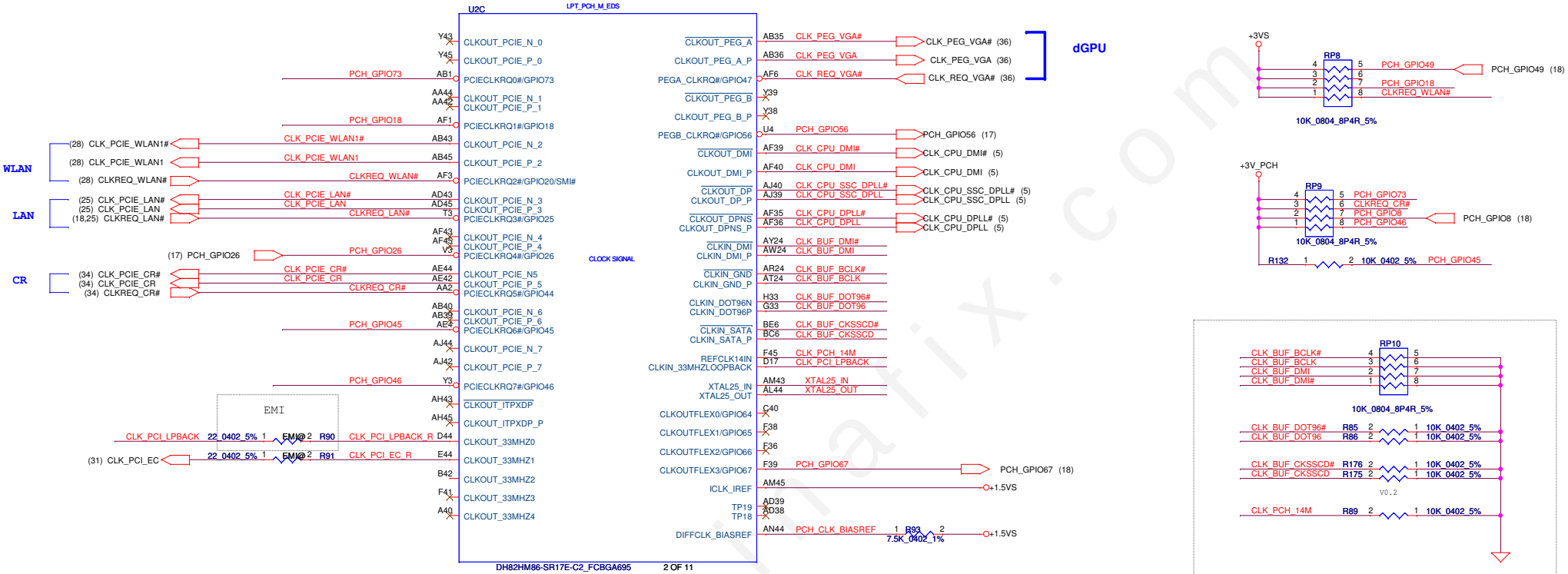
A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default *





Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Title	PCH (2/9) PCIE, SMBUS, CLK		
Size C	Document Number LA-B111P		Rev 1.0
Date: Tuesday, February 25, 2014	Sheet 14 of 59		



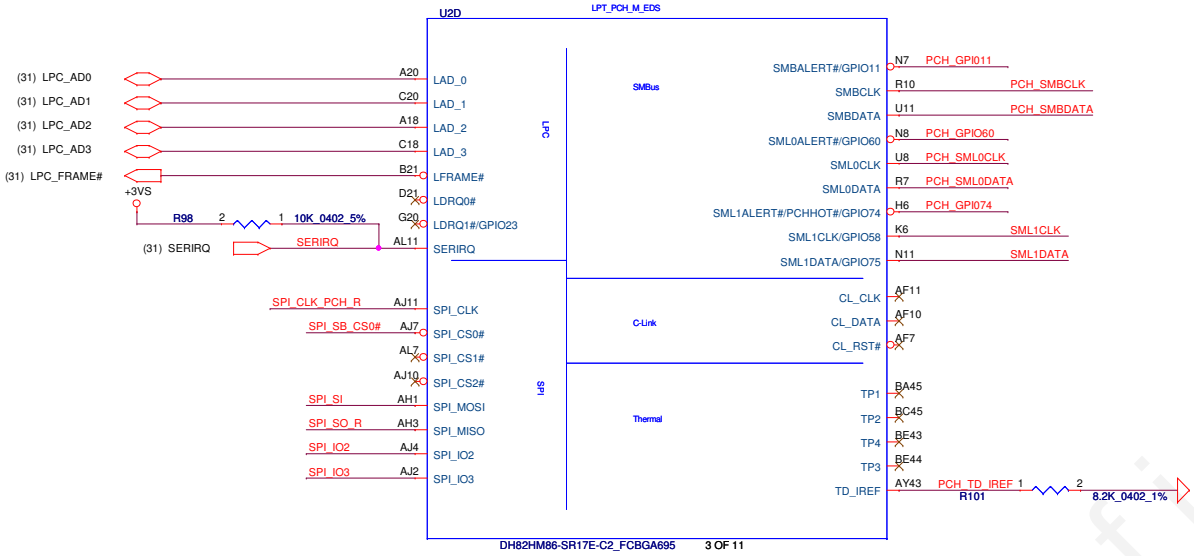
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

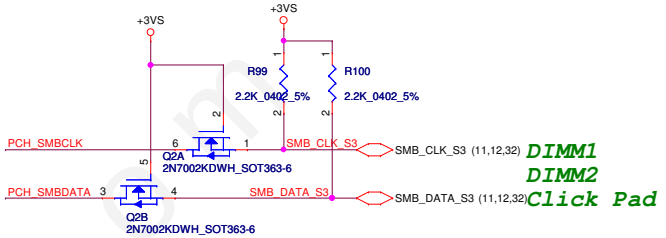
Compal Electronics, Inc.

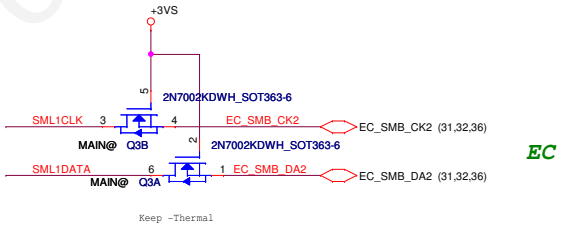
Title: PCH (3/9) DMI,FDI,PM,

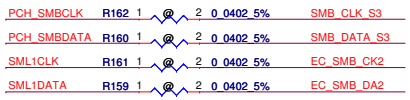
Size: B | Document Number: LA-B111P | Rev: 1.0

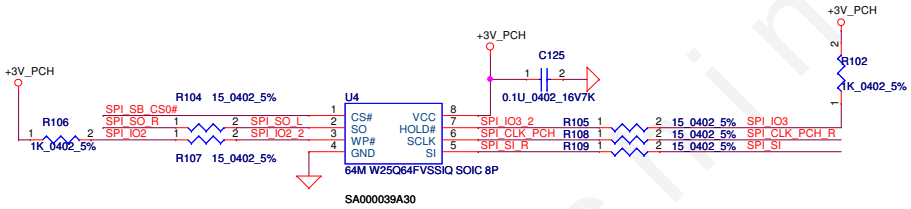
Date: Tuesday, February 25, 2014 | Sheet 15 of 59



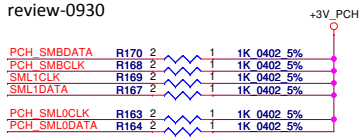


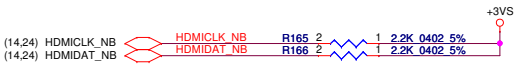


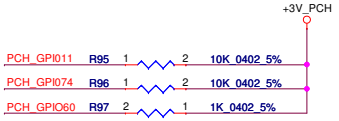


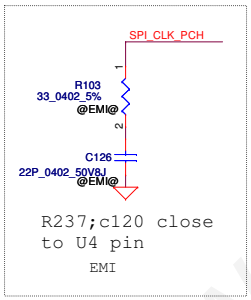


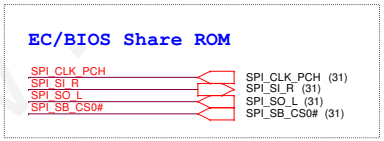
Follow Intel schematic review-0930











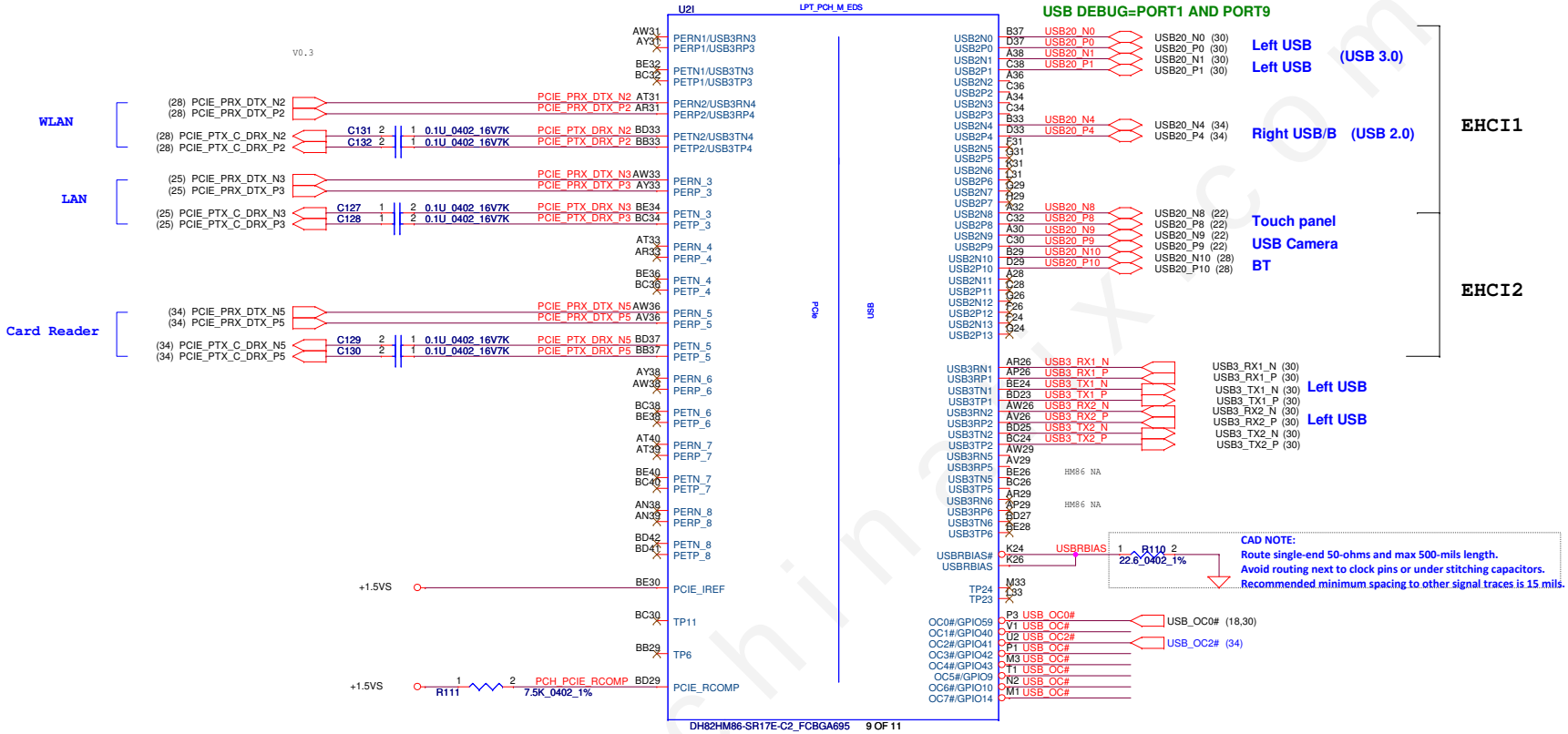
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

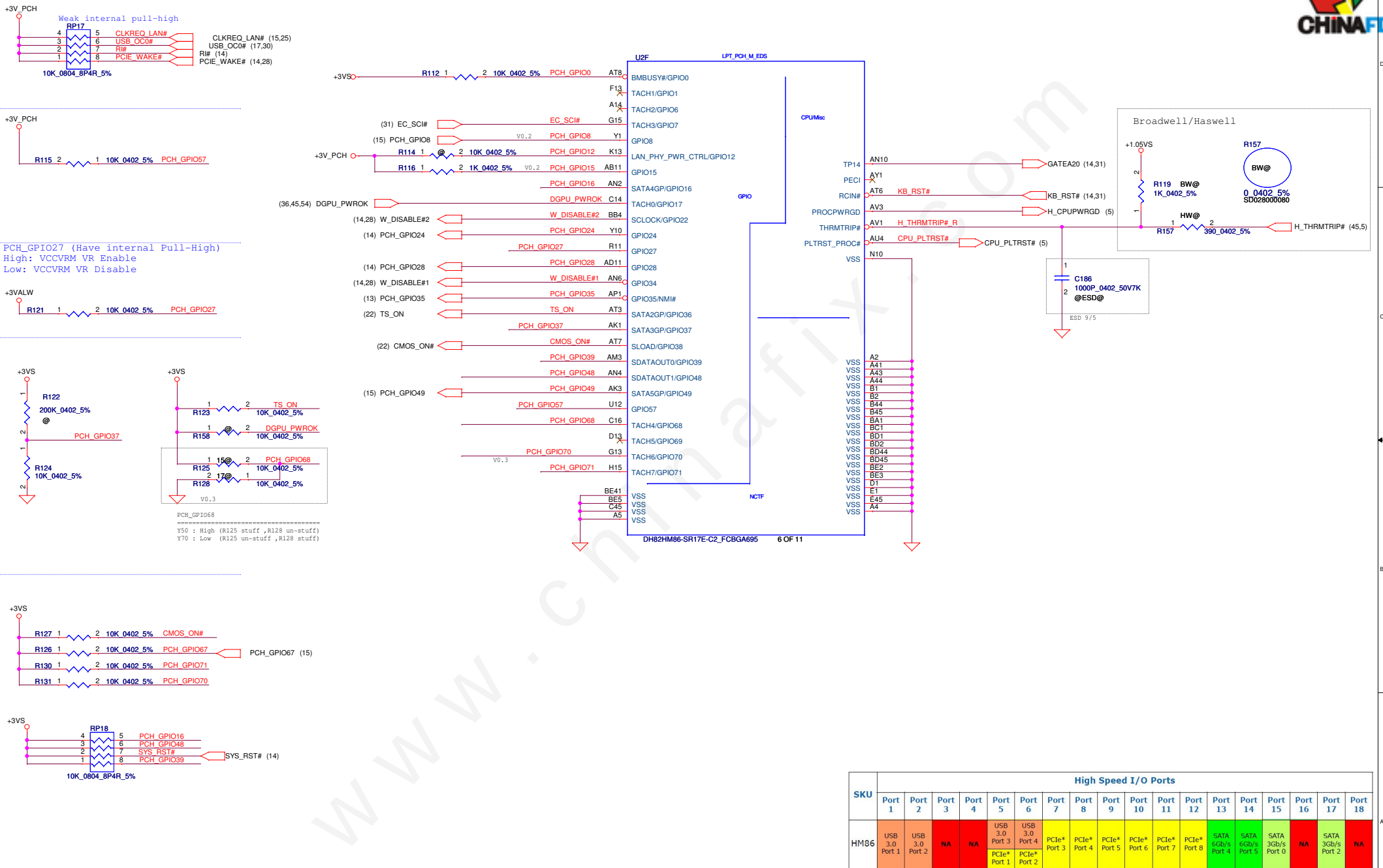
Size: B | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 16 of 59



Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.	
Title	PCH (5/9) PCI, USB
Size: B	Document Number: LA-B111P
Rev	1.0
Date: Tuesday, February 25, 2014	Sheet 17 of 59



SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
HM86	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4	SATA 6Gb/s Port 5	SATA 3Gb/s Port 0	NA	SATA 3Gb/s Port 2	NA

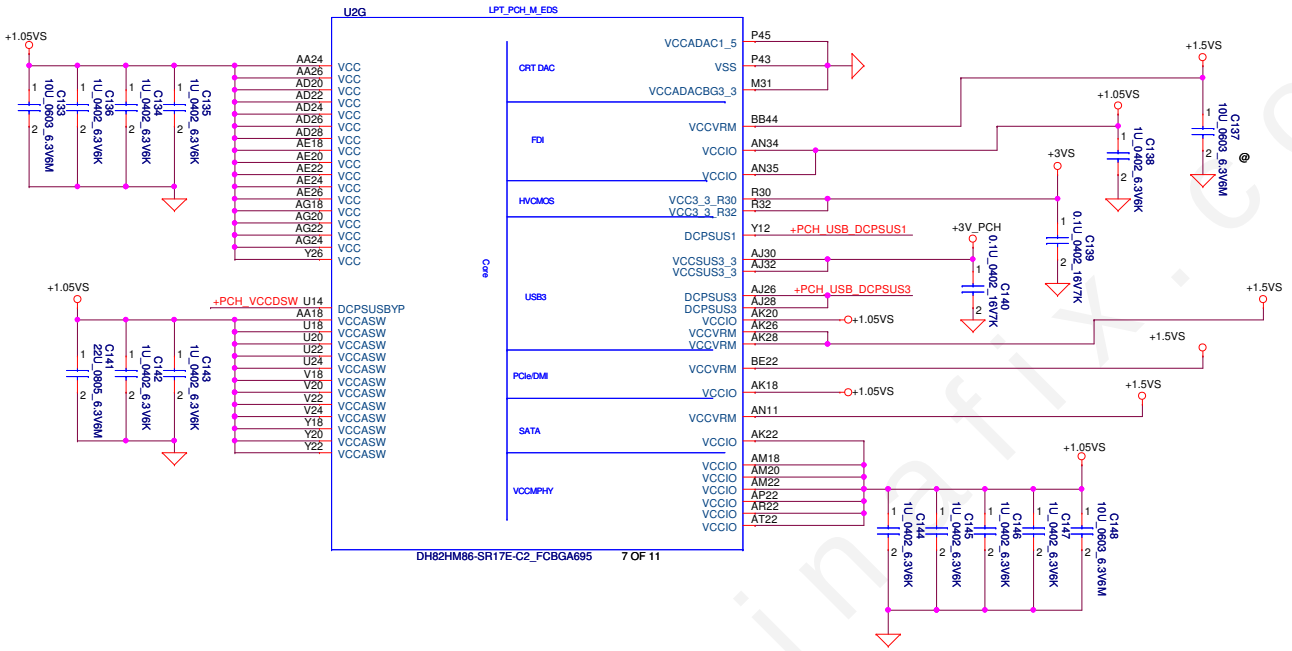
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

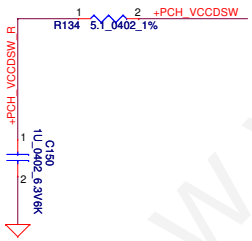
Title: PCH (6/9) GPIO, CPU, MISC

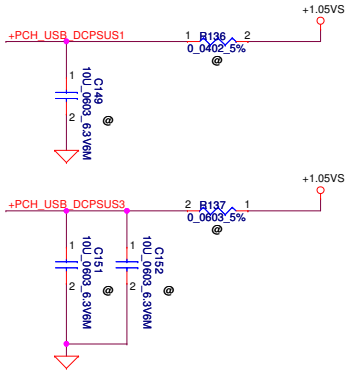
Document Number: LA-B111P

Rev: 1.0

Date: Tuesday, February 25, 2014 Sheet 18 of 59







PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

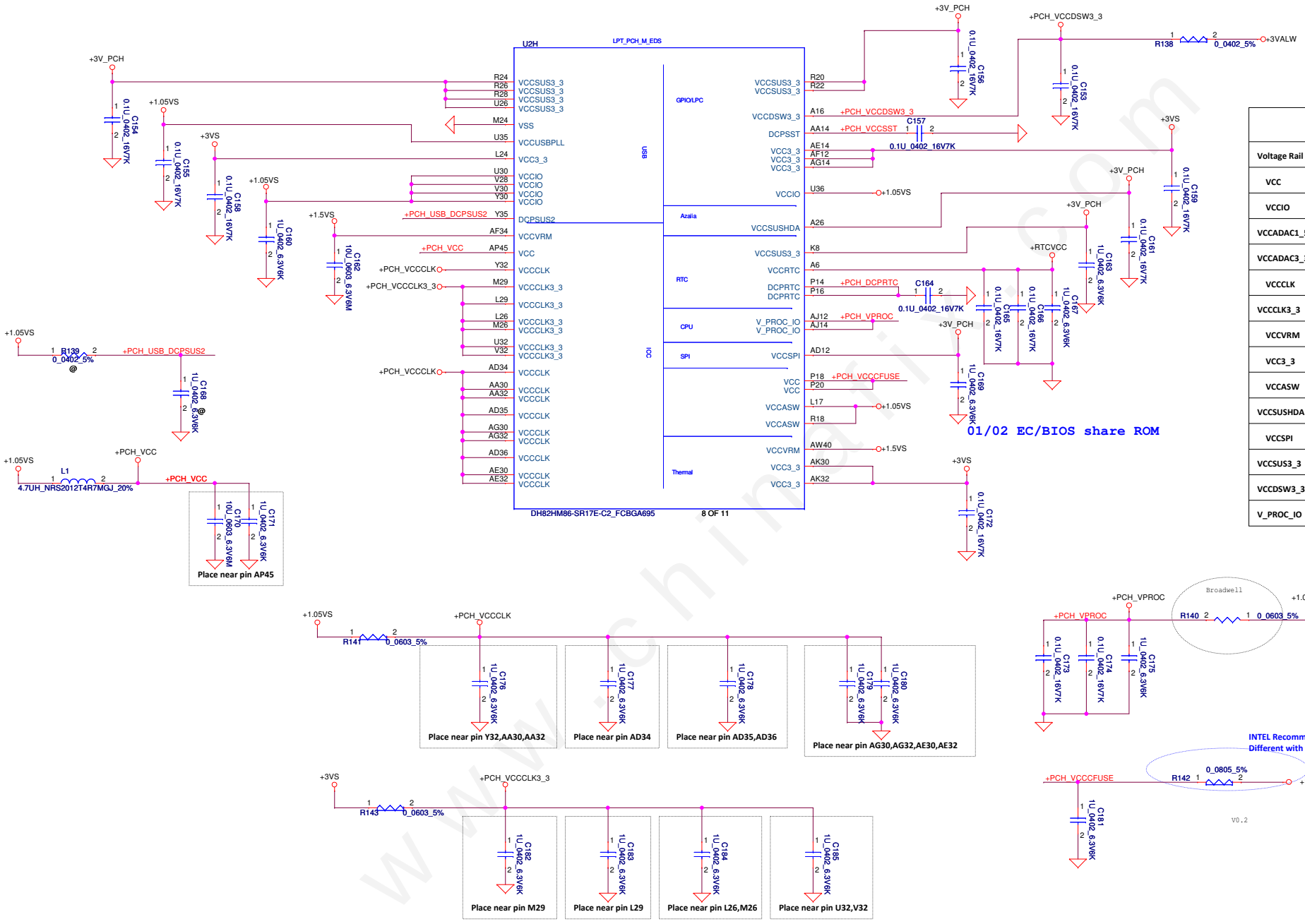
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: B | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 19 of 59

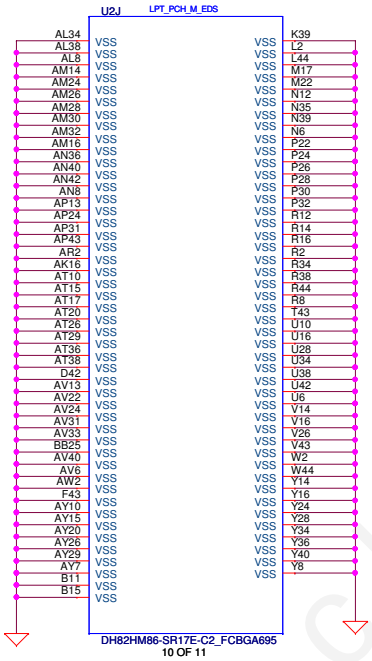


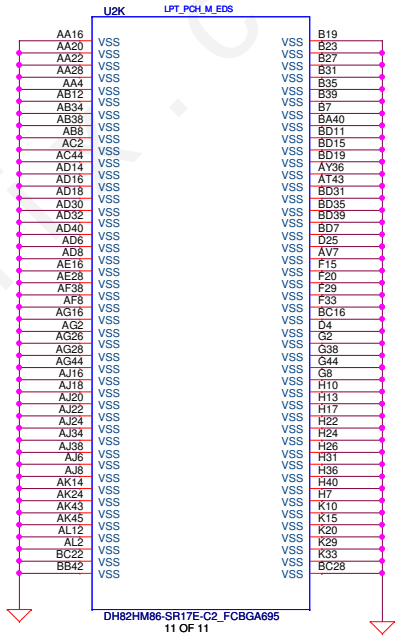
PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Title	PCH (8/9) PWR		
Size	Document Number		Rev
B	LA-B111P		1.0
Date:	Tuesday, February 25, 2014	Sheet	20 of 59





Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

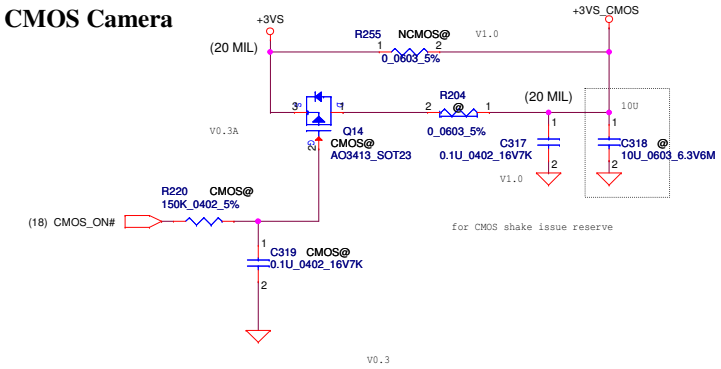
Title: PCH (9/9) VSS

Document Number: LA-B111P

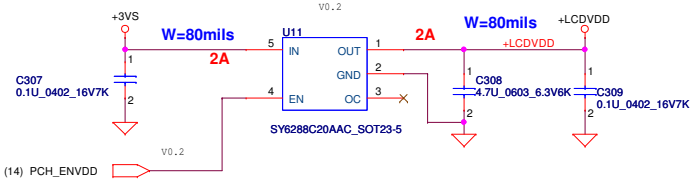
Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 21 of 59

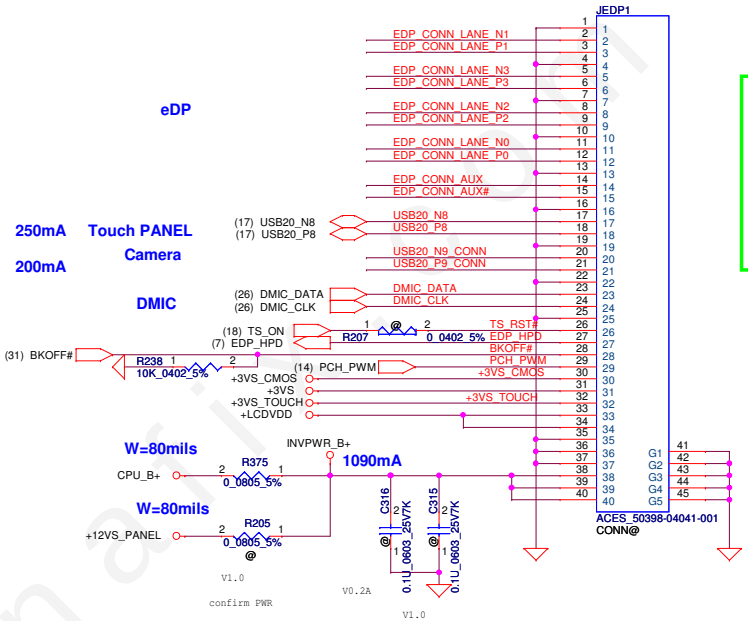
CMOS Camera



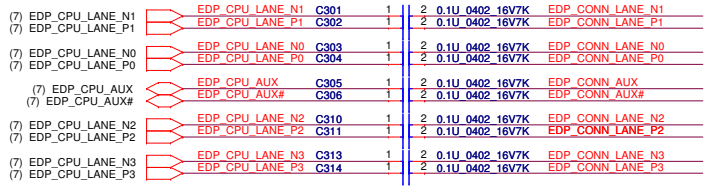
LCD POWER CIRCUIT

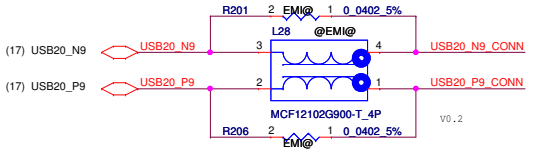


Touch Panel



eDP Panel
CAMERA
DMIC
TOUCH SCREEN





Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

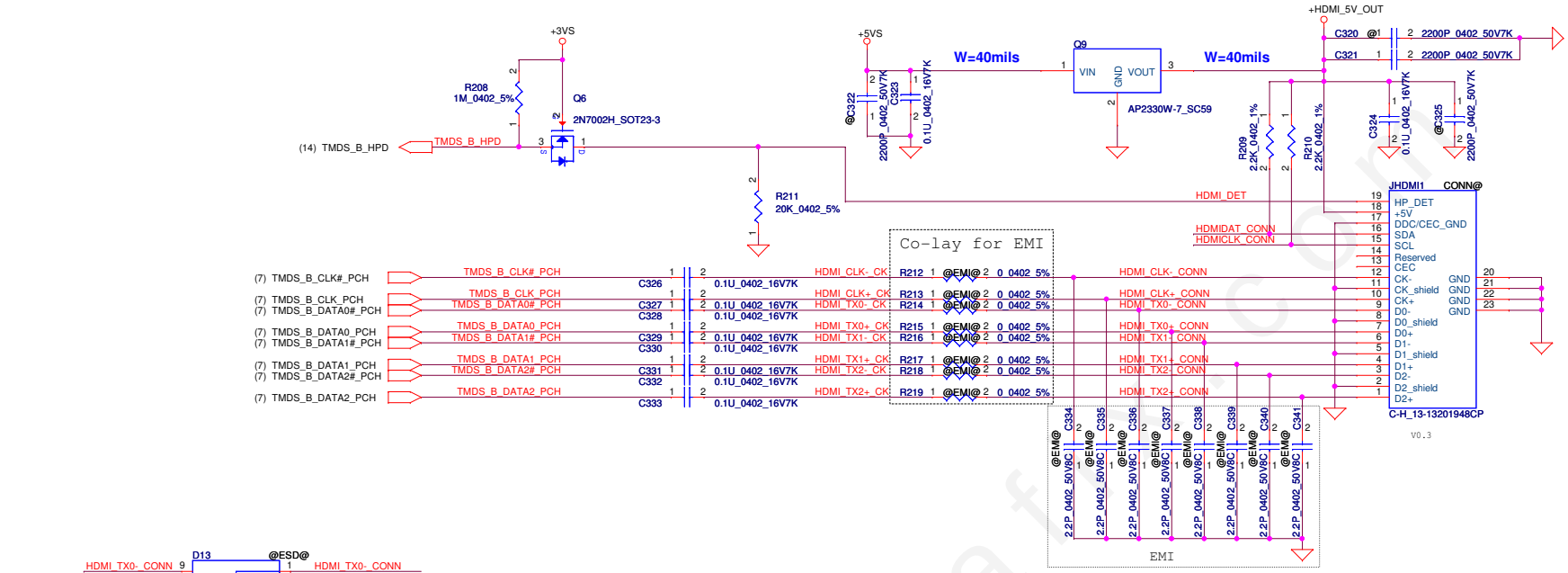
Compal Electronics, Inc.

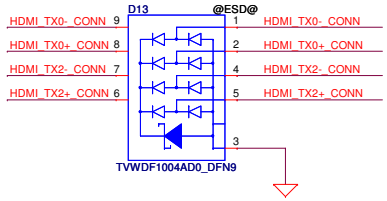
Title: LCD Conn/Camera, Touch

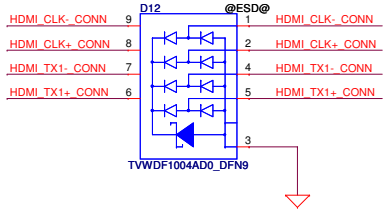
Size: Custom | Document Number: LA-B111P | Rev: 1.0

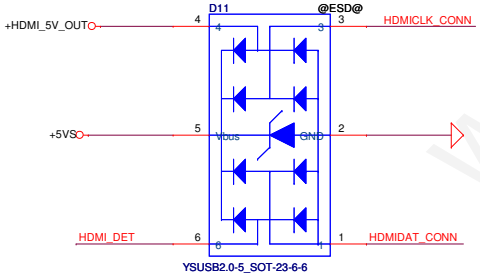
Date: Tuesday, February 25, 2014 | Sheet 22 of 59

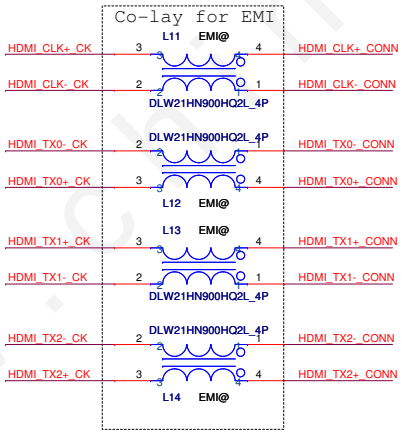
HDMI Connector

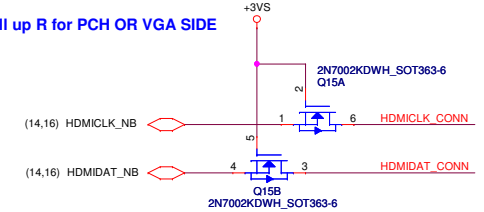


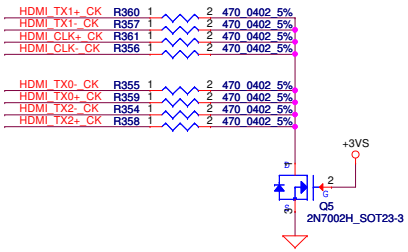












Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.			
Title: HDMI LS & Conn.			
Size: B	Document Number: LA-B111P		Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 24 of 59		

+3_LAN Rising time (10%~90%) >1mS and <100mS

+3VALW W=60mils +3V_LAN

JP6 JP@ JUMP_43X39 370mA

Layout Notice : Place as close chip as possible.

close to U12 : Pin 11, 32

These caps close to U12 : Pin 23

(Should be place within 200 mils)
These components close to U12 : Pin 24

These components close to U12 : Pin 3,8,22,30
1uF reserved on Pin 22

These caps close to U12 : Pin 11,32
DVDD33

Green CLK

XTLI R362 GCLK@ 0_0402_5% CLK_25M_LAN_XIN (27)

NOGCLK@ C356 12P_0402_50V8J R372 100_0402_1% EMI@ XTLI NOGCLK@

Y3 NOGCLK@ GND0 XTAL0 GND1 XTAL1 25MHZ_10PF_7V25000014

NOGCLK@ C359 12P_0402_50V8J XTLO

U12 RTL8111GUL-CG_QFN32_4X4 SA00006ML10

These caps close to U11

(15,18) CLKREQ_LAN#
(17) PCIE_PTX_C_DRX_P3
(17) PCIE_PTX_C_DRX_N3
(15) CLK_PCIE_LAN
(15) CLK_PCIE_LAN#

MDI0+ MDI0- +LAN_VDD10 MDI1+ MDI1- MDI2+ MDI2- +LAN_VDD10 MDI3+ MDI3- +3V_LAN LAN_CLKREQ#

MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 MDIP2 MDIN2 AVDD10 MDIP3 MDIN3 AVDD33 CLKREQB HSIP HSIN REFCLK_P REFCLK_N

HSOP HSON PERSTB ISOLATEB LANWAKEB DVDD10 VDDREG REGOUT LED2 LED1/GPIO LED0 CKXTAL1 CKXTAL2 AVDD10 RSET AVDD33 GND

PCIE_PRX_C_DTX_P3 C357 0.1U_0402_16V7K PCIE_PRX_DTX_P3
PCIE_PRX_C_DTX_N3 C358 0.1U_0402_16V7K PCIE_PRX_DTX_N3

PCIE_PRX_DTX_P3 (17)
PCIE_PRX_DTX_N3 (17)
PLT_RST# (14,28,31,34,36)

ISOLATEB R222 1K_0402_5% +3VS
LAN_WAKE# R R223 0_0402_5% LAN_WAKE# (31)
+LAN_VDD10
+3V_LAN
+LAN_REGOUT
T36
LAN_PWRDN# R R566 0_0402_5% LAN_PWRDN# (31) to EC
T37
XTLO
CKXTAL1
XTLI
CKXTAL2
+LAN_VDD10
LAN_RSET
+3V_LAN
R225 2.49K_0402_1%

ISOLATEB R226 15K_0402_5%

TS1 IH-160-A SP050007E00

+V_DAC MDI0+ MDI0- +V_DAC MDI1+ MDI1- +V_DAC MDI2+ MDI2- +V_DAC MDI3+ MDI3-

TCT1 TD1+ TD1- TCT2 TD2 TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-

MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4-

MDO0+ MDO0- MDO1+ MDO1- MDO2+ MDO2- MDO3+ MDO3-

C300 0.01U_0402_16V7K

R227 75_0805_5% EMI@ C360 10P_0603_50V8-J DL1 BS4200N-C-LV_SMB-F2 EMI@ CHASSIS1_GND

FOR EMI suggest

D10 ESD@ MDI2+ MDI3+ MDI3- MDI2- AZC099-04S.R7G_SOT23-6 Place Close to TS1

D14 ESD@ MDI0- MDI1- MDI0+ MDI1+ AZC099-04S.R7G_SOT23-6 Place Close to TS1

JRJ1 CONN@ SANTA_130460-3 DC234007K00

MDO0+ MDO0- MDO1+ MDO2+ MDO2- MDO1- MDO3+ MDO3-

PR1+ PR1- PR2+ PR3+ PR3- PR2- PR4+ PR4-

GND GND GND GND GND GND

CHASSIS1_GND

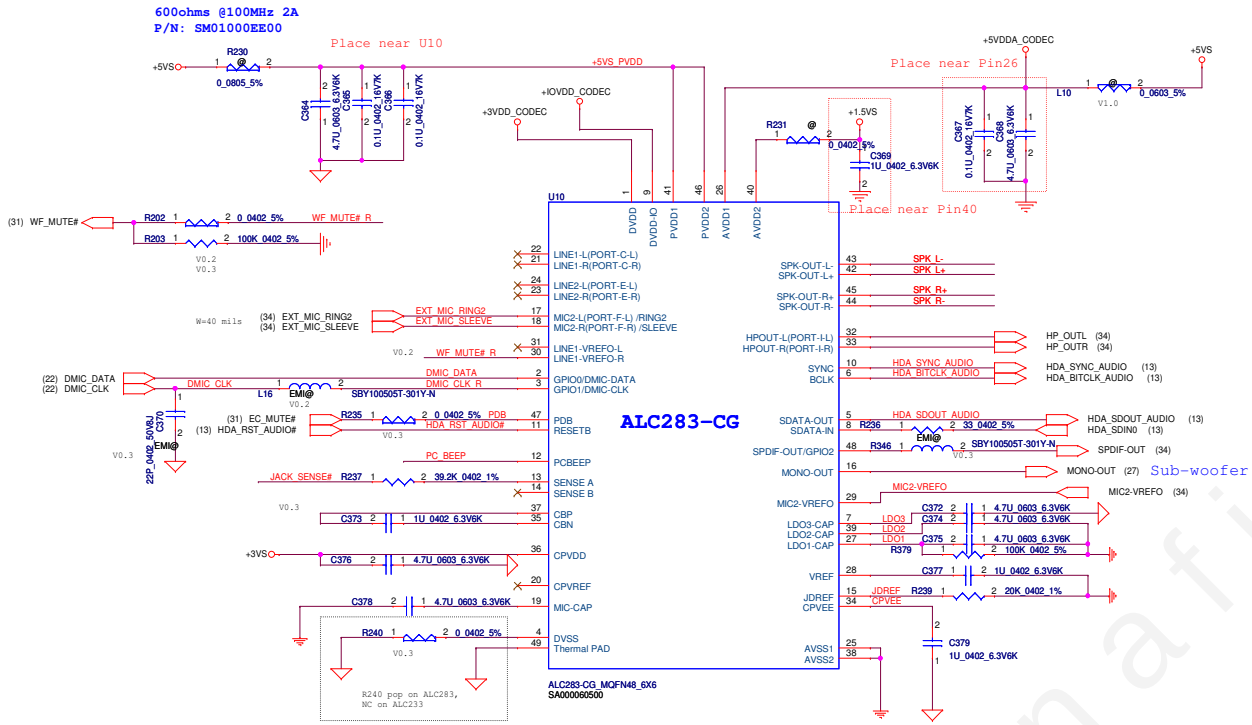
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

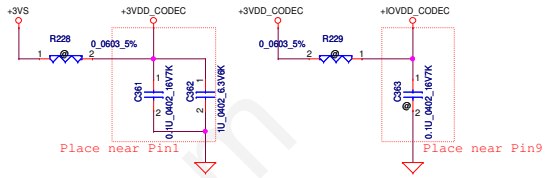
Compal Electronics, Inc.

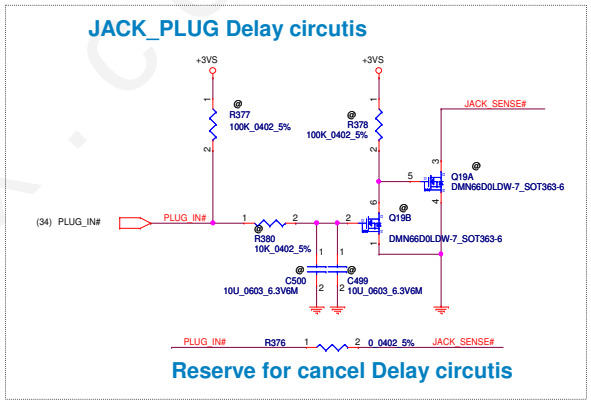
Title: LAN-RTL8111GUL

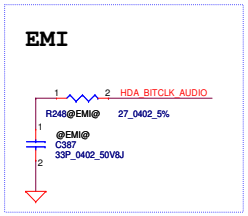
Size: Custom | Document Number: LA-B111P | Rev: 1.0

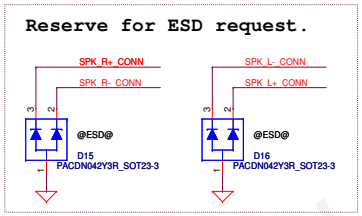
Date: Tuesday, February 25, 2014 | Sheet 25 of 59

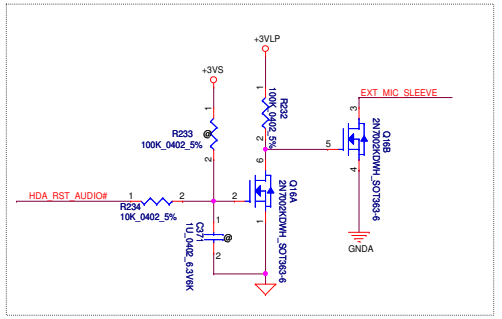


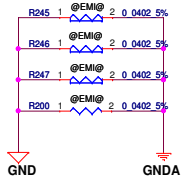


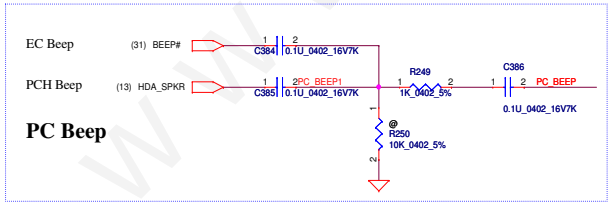


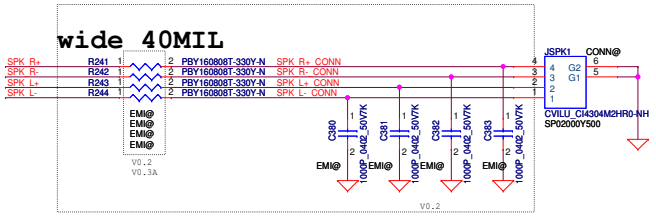












Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.	
Title	HD Audio ALC283
Size: C	Document Number: LA-B111P
Rev	1.0
Date:	Tuesday, February 25, 2014
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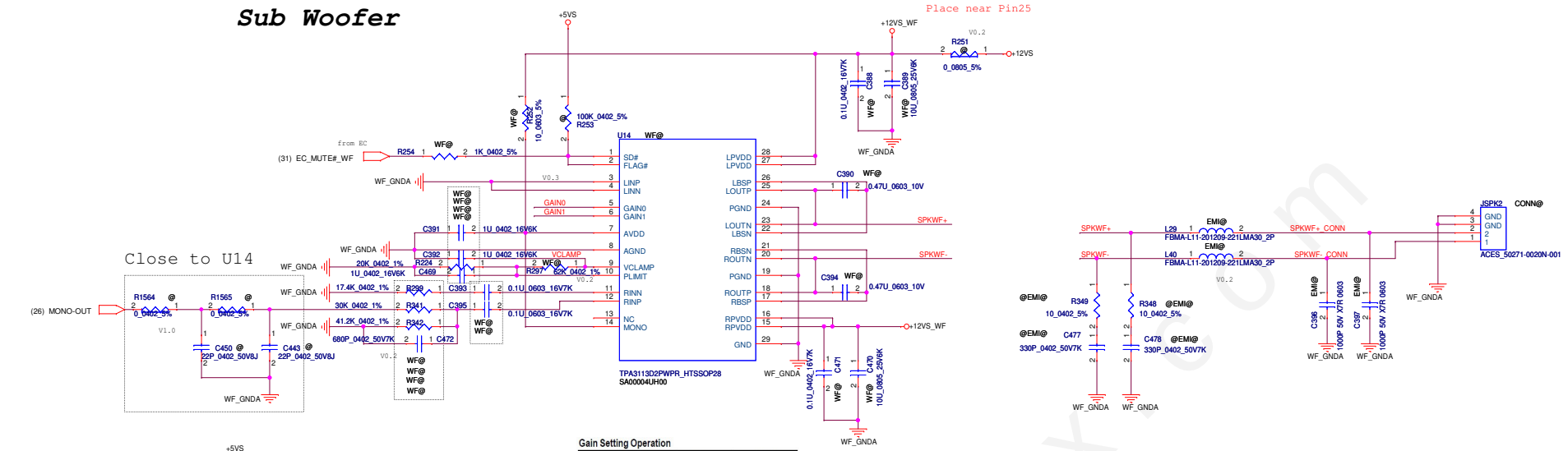
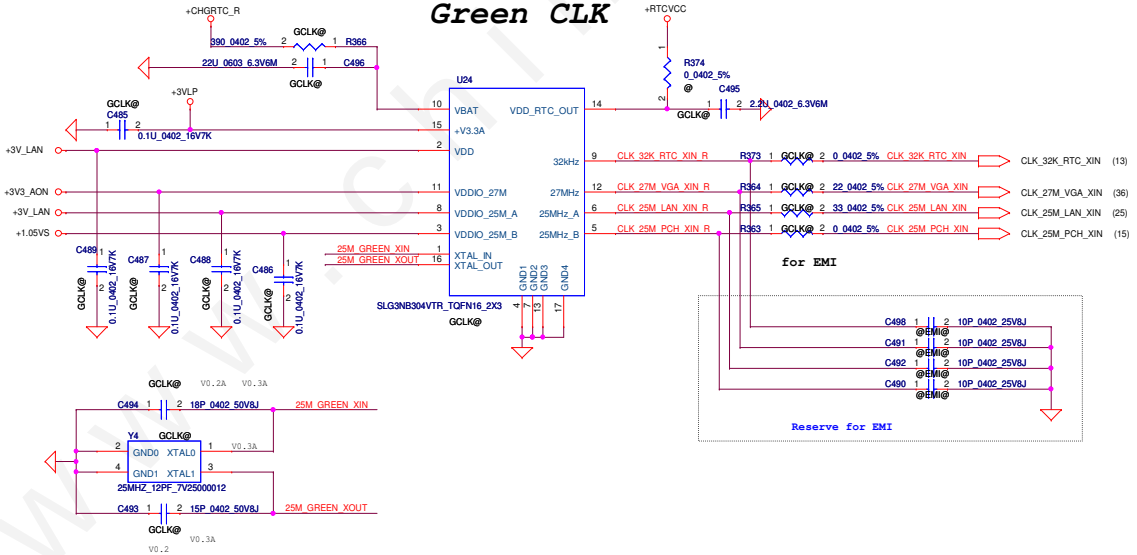
Sub Woofer



Gain Setting Operation

GAIN1	GAIN0	Gain	Ri(Ω)
0	0	20dB	60k
0	1	26dB	30k
1	0	32dB	15k
1	1	36dB	9k

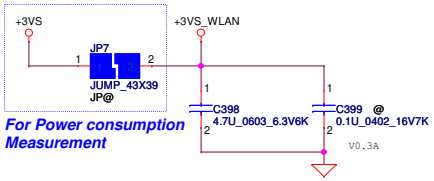
Green CLK



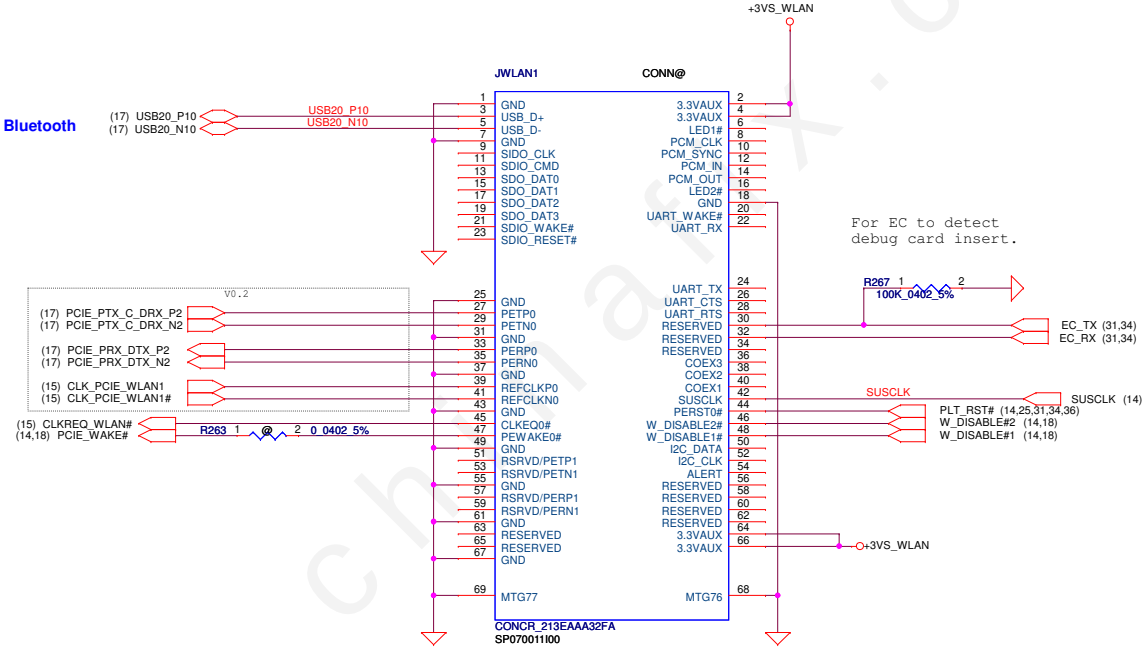
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.			
Title: Sub-Woofer / Green CLK			
Size: C	Document Number: LA-B111P		Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 27 of 59		

WLAN



NGFF for WLAN (TYPE 2230)



Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.		
Title: NGFF (WLAN/BT)		
Size: Custom	Document Number: LA-B111P	Rev: 1.0
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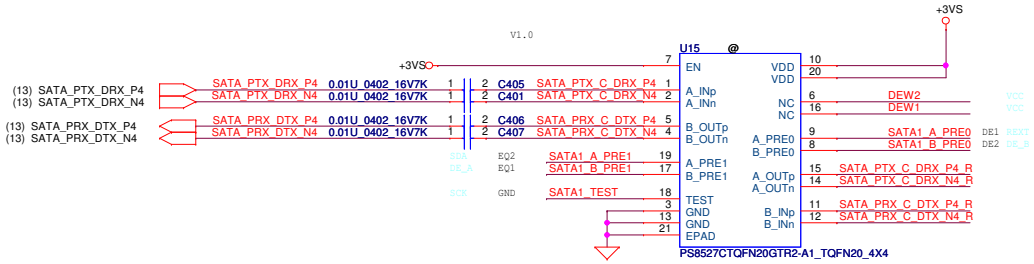
SATA HDD CONN.



U15 Parade@

PS8527CTQFN20GTR2-A1_TQFN20_4X4

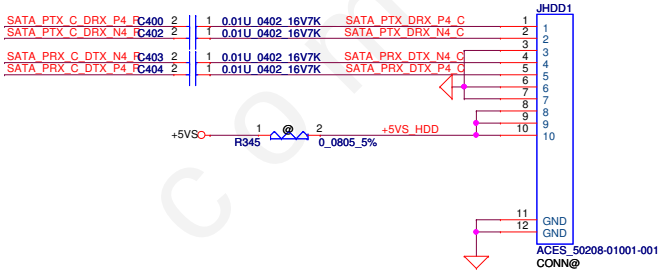
SA00007JU00

V0.2

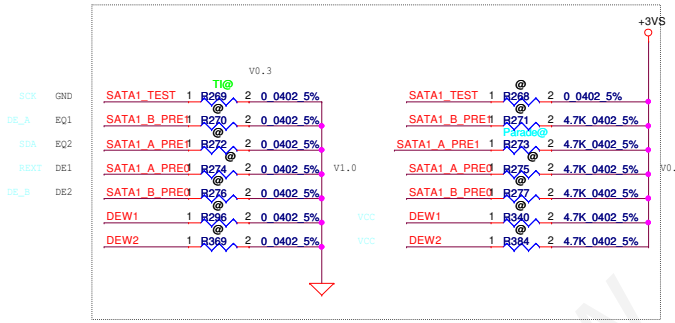
U15 TI@

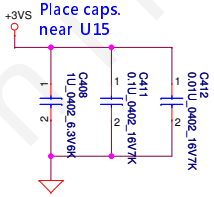
SN75LVCP601RTJR_TQFN20_4X4

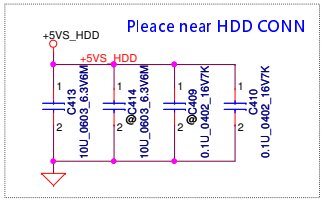
SA00003ZX00



Add EQ pin for PI3EQX6741STZDEX







TI

DE1/DE2	dB
NC	-6
0	0
1	-3

EQ1/EQ2	dB
NC	0
0	7
1	14

V0.3

Asmidia

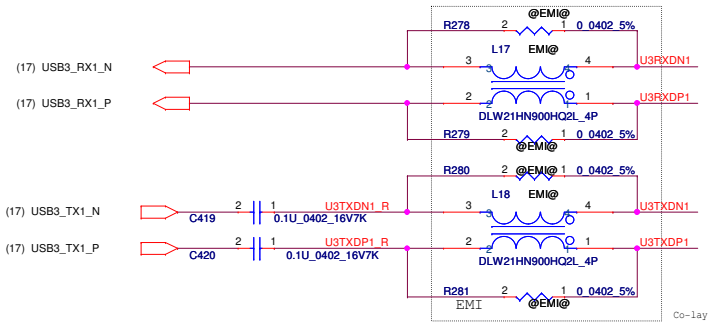
DE_X	dB
0	+1.5
1	+3.0

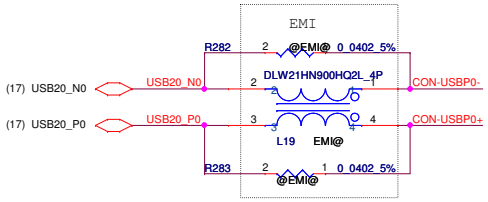
Compal Electronics, Inc.

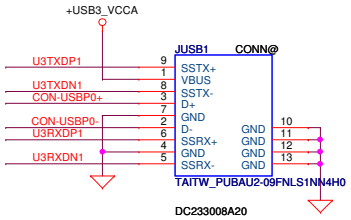
Title: HDD/SSD

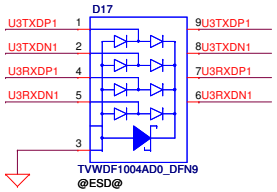
Size: B | Document Number: LA-B111P | Rev: 1.0

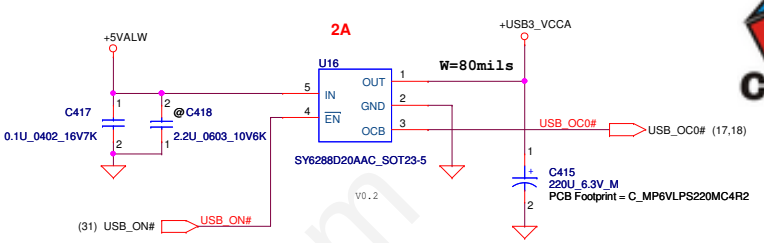
Date: Tuesday, February 25, 2014 | Sheet 29 of 59

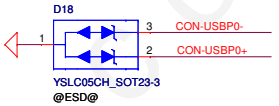


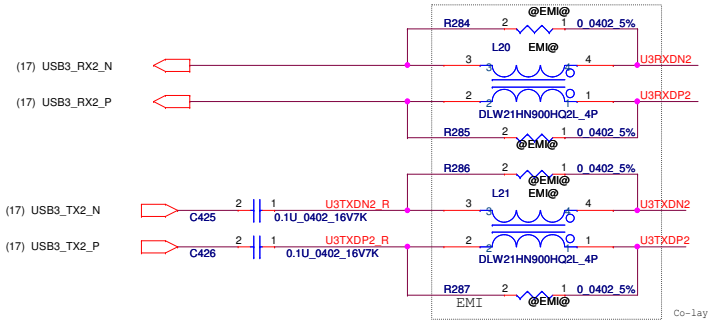


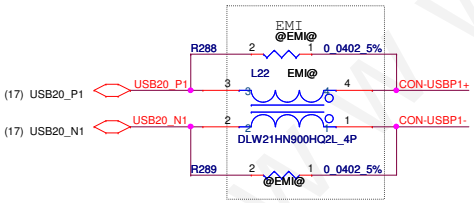


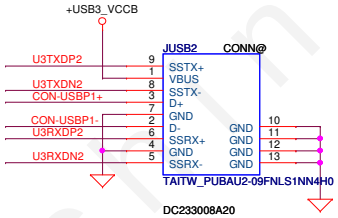


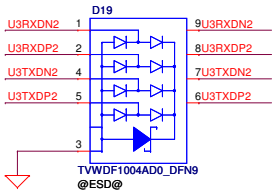


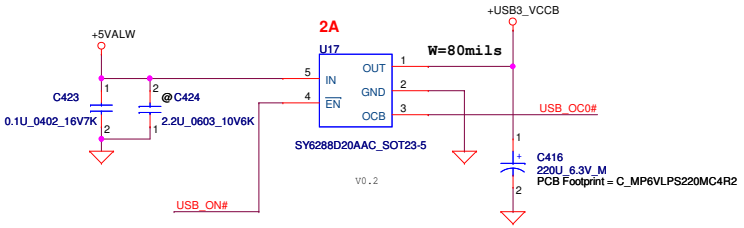


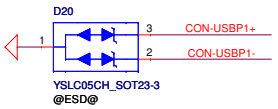






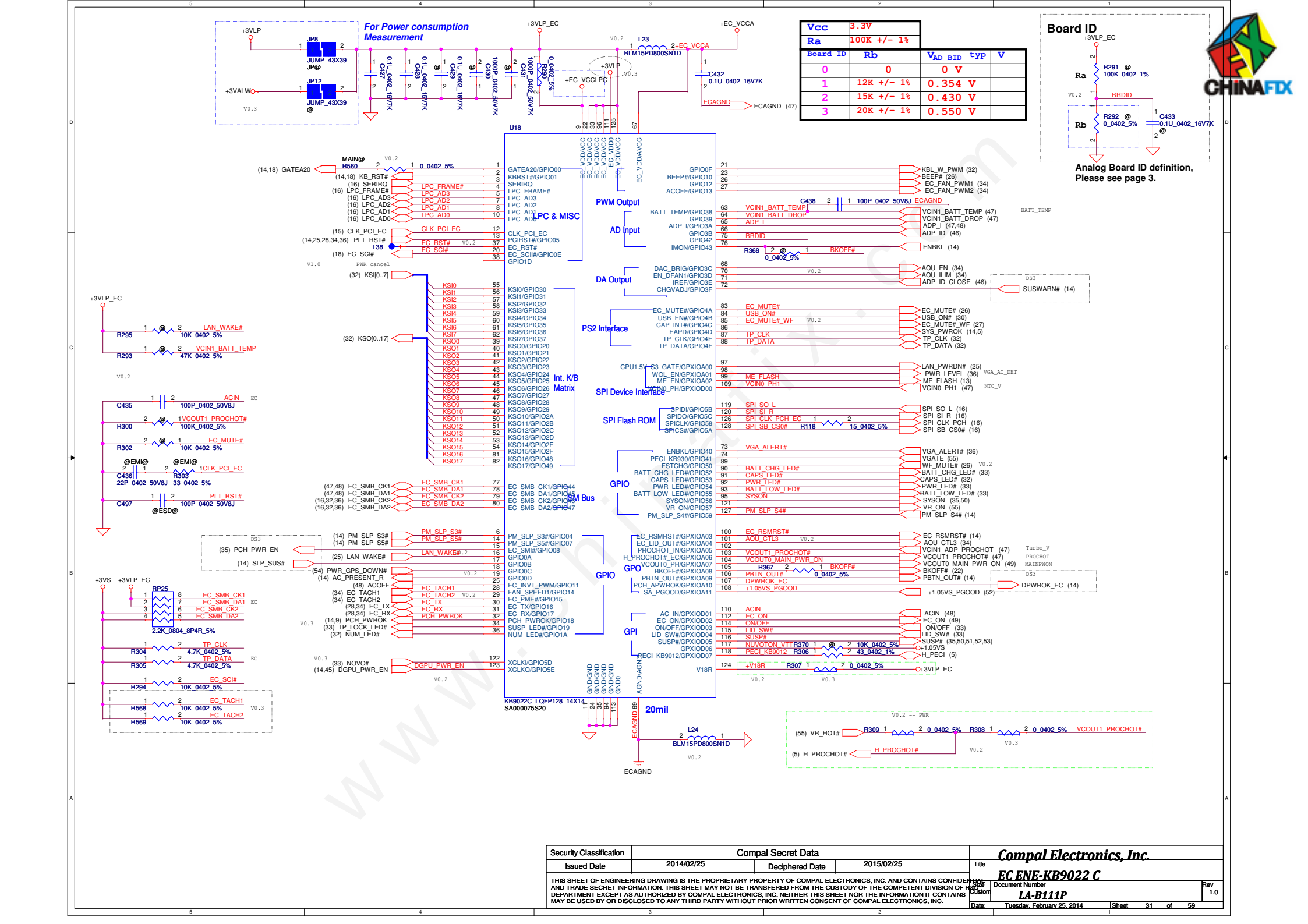






Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.			
Title: USB3.0 Port			
Size: Custom	Document Number: LA-B111P		Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 30 of 59		


For Power consumption Measurement
+3VLP
+3VALW
JP8
JP12
JUMP_43X39
+3VLP_EC
+EC_VCCA
L23
BLM15PD800SN1D
+EC_VCCLPC
ECAGND
ECAGND (47)
Vcc 3.3V
Ra 100K +/- 1%
Board ID | Rb | VAD_BID typ | V
0 | 0 | 0 V
1 | 12K +/- 1% | 0.354 V
2 | 15K +/- 1% | 0.430 V
3 | 20K +/- 1% | 0.550 V
Board ID
R291 @ 100K_0402_1%
R292 @ 0_0402_5%
C433 0.1U_0402_16V7K
BRDID
Analog Board ID definition, Please see page 3.
U18
KB9022C_LQFP128_14X14
SA000075S20
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
20mil
L24
BLM15PD800SN1D
ECAGND
Security Classification
Compal Secret Data
Issued Date
2014/02/25
Deciphered Date
2015/02/25
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EC ENE-KB9022 C
Size: Custom
Document Number: LA-B111P
Rev: 1.0
Date: Tuesday, February 25, 2014
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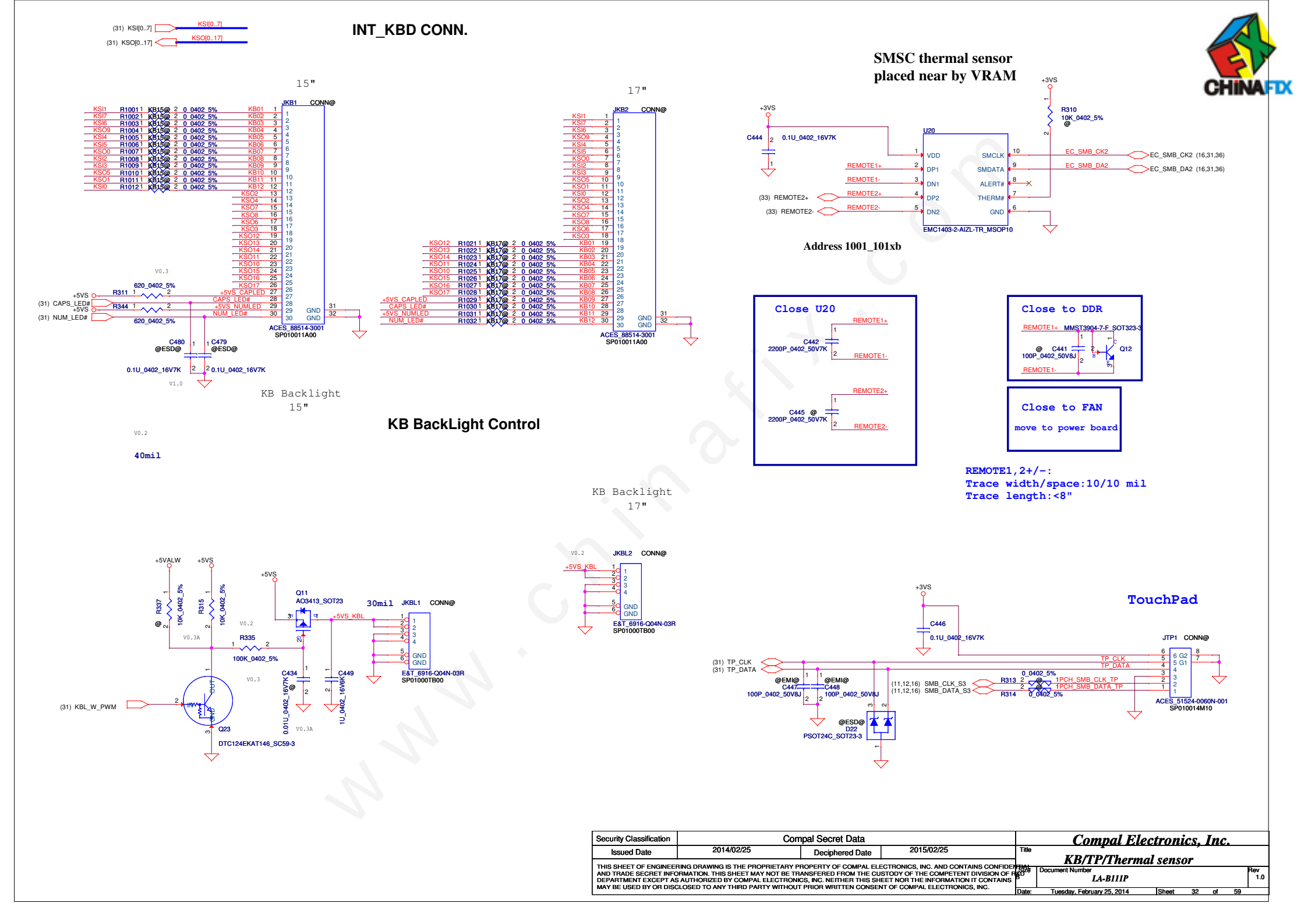
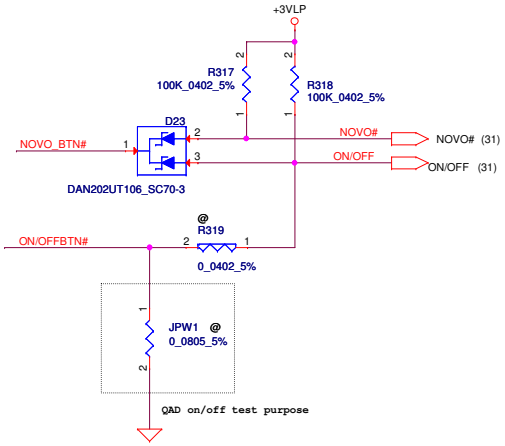


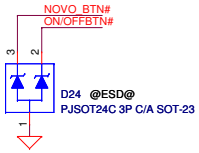
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.			
Title: KB/TP/Thermal sensor			
Size: B	Document Number: LA-B111P		Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 32 of 59		

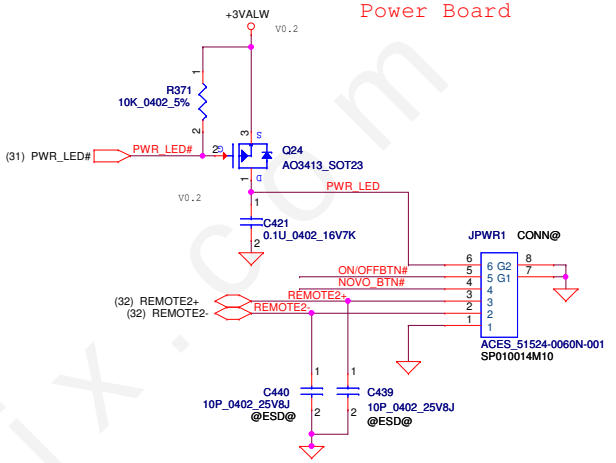
Connector: 0.3A / pin

PWR Board CONN.

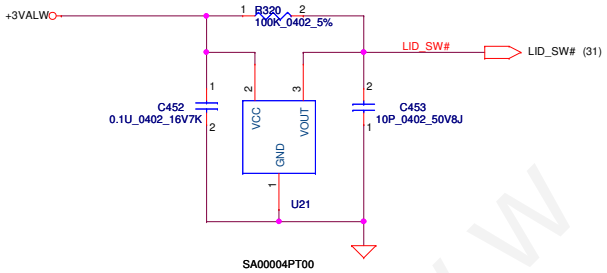




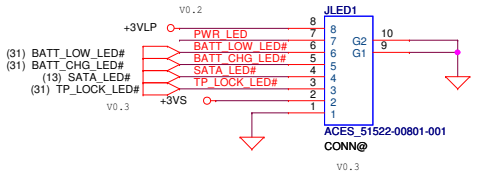
Power Board



Lid switch

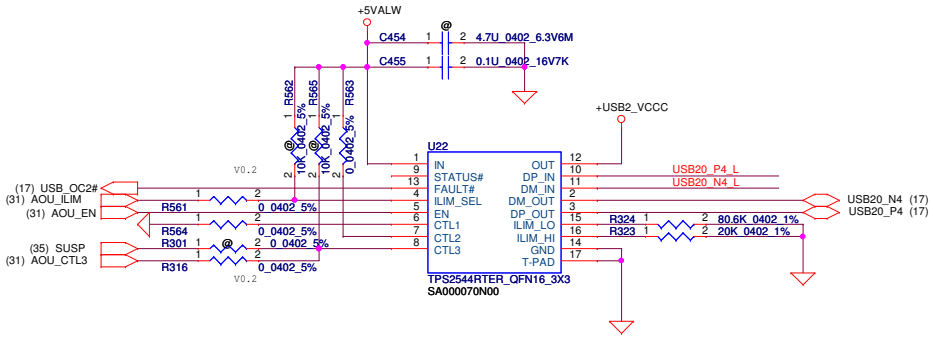


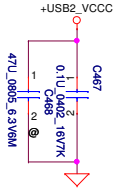
LED-B CONN

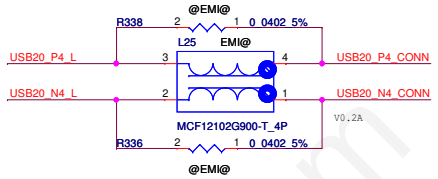


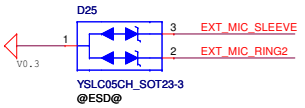
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.	
Title	PWR_BTN/PWR_B/LED_B/LID
Size: B	Document Number: LA-B111P
Rev: 1.0	
Date: Tuesday, February 25, 2014	Sheet 33 of 59





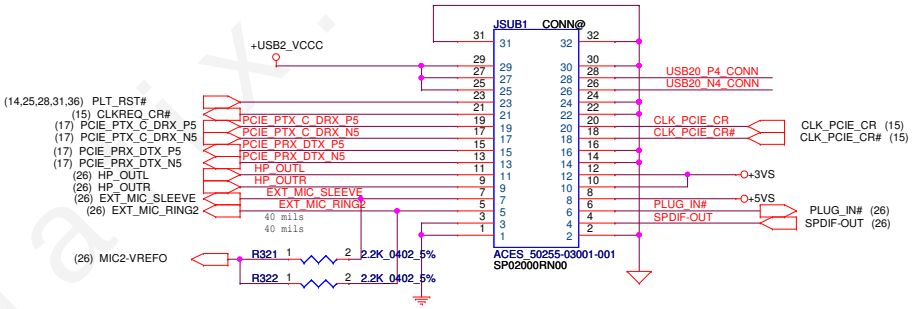


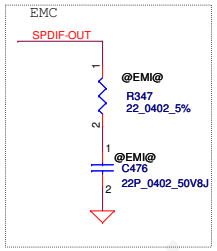


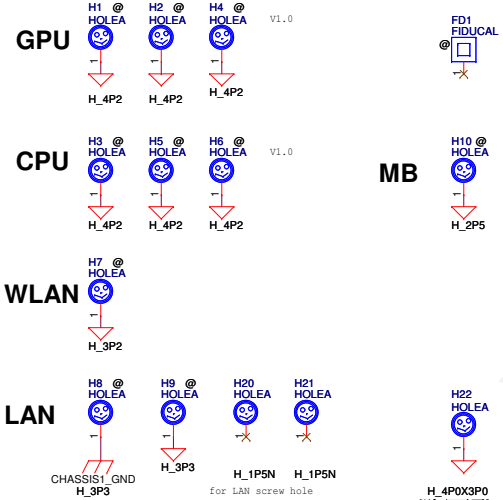
Alway on USB	Mode	CTL1~3,ILIM_SEL
Enable	S0	0 1 0 1
	S3/S4/S5	0 1 1 1
Disable	S0	0 1 0 1
	S3	0 1 0 0
	S4/S5	0 1 0 0

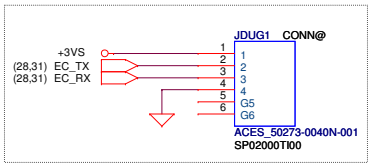
V0.2

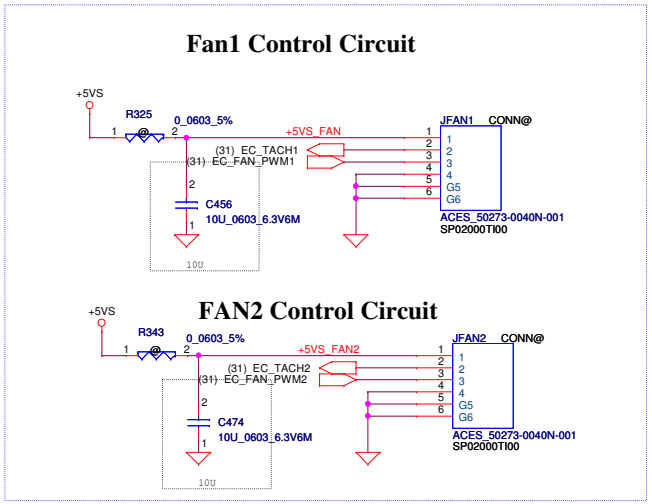
USB Board CONN.











Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.	
Title	USB charge/FAN/Screw holes
Size: B	Document Number: LA-B111P
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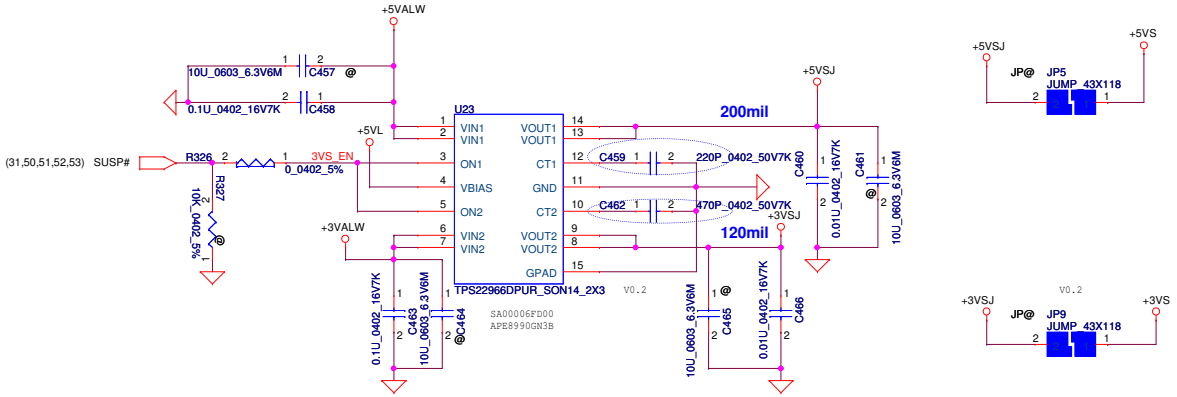
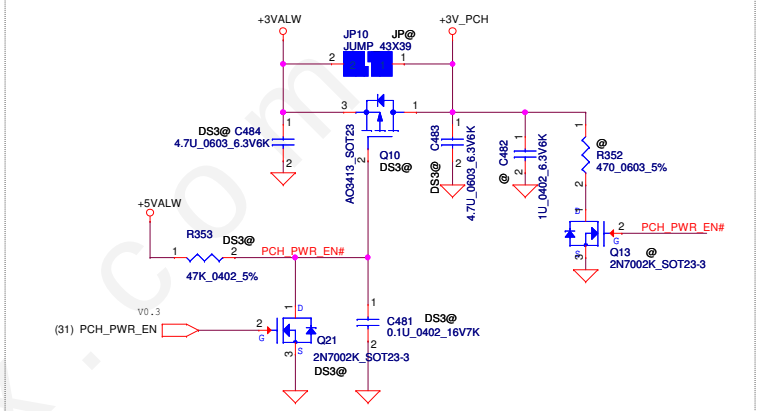
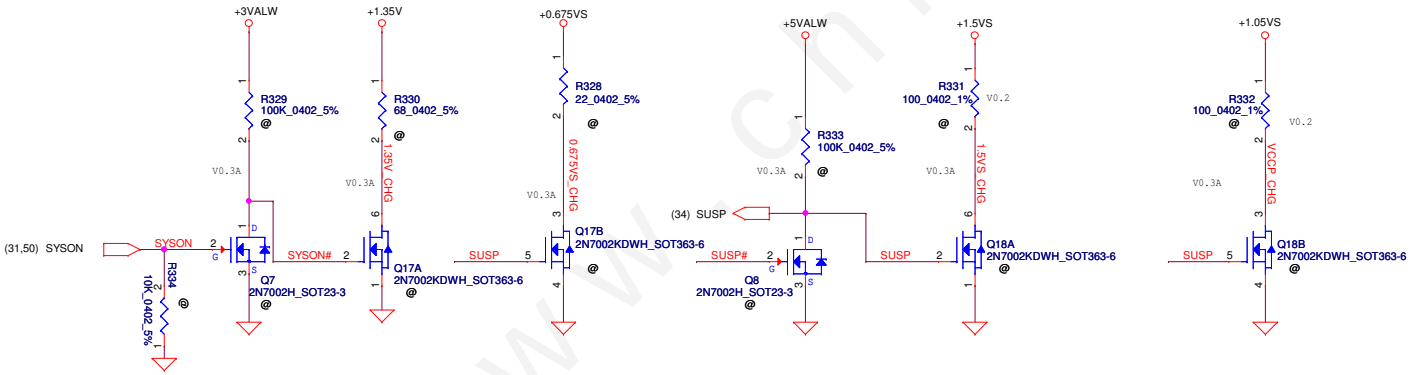
+5VALW to +5VS Transfer



+3VALW to +3VS Transfer



Discharge circuit-1



Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: DC/DC Interface

Document Number: LA-B111P

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(4) PEG_CRX_GTX_P[0..15] — PEG_CRX_GTX_P[0..15]
(4) PEG_CRX_GTX_N[0..15] — PEG_CRX_GTX_N[0..15]
(4) PEG_PTX_C_DRX_P[0..15] — PEG_PTX_C_DRX_P[0..15]
(4) PEG_PTX_C_DRX_N[0..15] — PEG_PTX_C_DRX_N[0..15]

U30A — Part 1 of 7 — PCI EXPRESS — N15P-GX_BGA908

PEG_PTX_C_DRX_P0	AN12	PEX_RX0	
PEG_PTX_C_DRX_N0	AM12	PEX_RX0_N	
PEG_PTX_C_DRX_P1	AN14	PEX_RX1	
PEG_PTX_C_DRX_N1	AM14	PEX_RX1_N	
PEG_PTX_C_DRX_P2	AP14	PEX_RX2	
PEG_PTX_C_DRX_N2	AP15	PEX_RX2_N	
PEG_PTX_C_DRX_P3	AN15	PEX_RX3	
PEG_PTX_C_DRX_N3	AM15	PEX_RX3_N	
PEG_PTX_C_DRX_P4	AN17	PEX_RX4	
PEG_PTX_C_DRX_N4	AM17	PEX_RX4_N	
PEG_PTX_C_DRX_P5	AP17	PEX_RX5	
PEG_PTX_C_DRX_N5	AP18	PEX_RX5_N	
PEG_PTX_C_DRX_P6	AN18	PEX_RX6	
PEG_PTX_C_DRX_N6	AM18	PEX_RX6_N	
PEG_PTX_C_DRX_P7	AN20	PEX_RX7	
PEG_PTX_C_DRX_N7	AM20	PEX_RX7_N	
PEG_PTX_C_DRX_P8	AP20	PEX_RX8	
PEG_PTX_C_DRX_N8	AP21	PEX_RX8_N	
PEG_PTX_C_DRX_P9	AN21	PEX_RX9	
PEG_PTX_C_DRX_N9	AM21	PEX_RX9_N	
PEG_PTX_C_DRX_P10	AN23	PEX_RX10	
PEG_PTX_C_DRX_N10	AM23	PEX_RX10_N	
PEG_PTX_C_DRX_P11	AP23	PEX_RX11	
PEG_PTX_C_DRX_N11	AP24	PEX_RX11_N	
PEG_PTX_C_DRX_P12	AN24	PEX_RX12	
PEG_PTX_C_DRX_N12	AM24	PEX_RX12_N	
PEG_PTX_C_DRX_P13	AN26	PEX_RX13	
PEG_PTX_C_DRX_N13	AM26	PEX_RX13_N	
PEG_PTX_C_DRX_P14	AP26	PEX_RX14	
PEG_PTX_C_DRX_N14	AP27	PEX_RX14_N	
PEG_PTX_C_DRX_P15	AN27	PEX_RX15	
PEG_PTX_C_DRX_N15	AM27	PEX_RX15_N	

GPIO

GPIO0	P6	GC6_FB_EN → GC6_FB_EN (14,38) TO PCH
GPIO1	M3	
GPIO2	L6	
GPIO3	P5	
GPIO4	P7	
GPIO5	L7	3V3_MAIN_EN → 3V3_MAIN_EN (45,54) TO PCH
GPIO6	M7	GPU_EVENT#_R
GPIO7	N8	
GPIO8	L3	SYS_PEX_RST_MON# TO PCH THRMTRIP#
GPIO9	M2	VGA_ALERT# → VGA_ALERT# (31) TO EC
GPIO10	L1	VRAM_VREF_CTL → VRAM_VREF_CTL (41,43)
GPIO11	M5	NVVDD_PWM_VID → NVVDD_PWM_VID (54) TO EC
GPIO12	N3	PWR_LEVEL_R → PWR_LEVEL_R (47) TO EC
GPIO13	M4	NVVDD_PSI → NVVDD_PSI (54) TO EC
GPIO14	N4	
GPIO15	P2	
GPIO16	R8	
GPIO17	M6	
GPIO18	R1	
GPIO19	P3	
GPIO20	P4	
GPIO21	P1	DGPU_RST_HOLD#

DACs

DACA_RED	AK9	
DACA_GREEN	AL10	
DACA_BLUE	AL9	
DACA_HSYNC	AM9	
DACA_VSYNC	AN9	
DACA_VDD	AG10	
DACA_VREF	AP9	
DACA_RSET	AP8	

I2C

I2CA_SCL	R4	VGA_CRT_CLK
I2CA_SDA	R5	VGA_CRT_DATA
I2CB_SCL	R7	HDCP_SCL
I2CB_SDA	R6	HDCP_SDA
I2CC_SCL	R2	VGA_EDID_CLK
I2CC_SDA	R3	VGA_EDID_DATA
I2CS_SCL	T4	SMB_CLK_GPU
I2CS_SDA	T3	SMB_DATA_GPU

CLK

PLLVDD	AD8	+PLLVDD
SP_PLLVDD	AE8	
VID_PLLVDD	AD7	+GPU_PLLVDD
XTAL_IN	H3	XTALIN
XTAL_OUT	H2	XTAL_OUT
XTAL_OUTBUFF	J4	XTAL_OUTBUFF
XTAL_SSIN	H1	XTAL_SSIN

PEG_CRX_GTX_P0	C601	PEG_CRX_C_GTX_P0 AK14
PEG_CRX_GTX_N0	C604	PEG_CRX_C_GTX_N0 AJ14
PEG_CRX_GTX_P1	C606	PEG_CRX_C_GTX_P1 AH14
PEG_CRX_GTX_N1	C609	PEG_CRX_C_GTX_N1 AG14
PEG_CRX_GTX_P2	C610	PEG_CRX_C_GTX_P2 AK15
PEG_CRX_GTX_N2	C611	PEG_CRX_C_GTX_N2 AJ15
PEG_CRX_GTX_P3	C612	PEG_CRX_C_GTX_P3 AL16
PEG_CRX_GTX_N3	C613	PEG_CRX_C_GTX_N3 AK16
PEG_CRX_GTX_P4	C614	PEG_CRX_C_GTX_P4 AK17
PEG_CRX_GTX_N4	C615	PEG_CRX_C_GTX_N4 AJ17
PEG_CRX_GTX_P5	C616	PEG_CRX_C_GTX_P5 AH17
PEG_CRX_GTX_N5	C617	PEG_CRX_C_GTX_N5 AG17
PEG_CRX_GTX_P6	C618	PEG_CRX_C_GTX_P6 AK18
PEG_CRX_GTX_N6	C619	PEG_CRX_C_GTX_N6 AJ18
PEG_CRX_GTX_P7	C620	PEG_CRX_C_GTX_P7 AL19
PEG_CRX_GTX_N7	C621	PEG_CRX_C_GTX_N7 AK19
PEG_CRX_GTX_P8	C622	PEG_CRX_C_GTX_P8 AK20
PEG_CRX_GTX_N8	C623	PEG_CRX_C_GTX_N8 AJ20
PEG_CRX_GTX_P9	C624	PEG_CRX_C_GTX_P9 AH20
PEG_CRX_GTX_N9	C625	PEG_CRX_C_GTX_N9 AG20
PEG_CRX_GTX_P10	C626	PEG_CRX_C_GTX_P10 AK21
PEG_CRX_GTX_N10	C627	PEG_CRX_C_GTX_N10 AJ21
PEG_CRX_GTX_P11	C628	PEG_CRX_C_GTX_P11 AL22
PEG_CRX_GTX_N11	C629	PEG_CRX_C_GTX_N11 AK22
PEG_CRX_GTX_P12	C630	PEG_CRX_C_GTX_P12 AK23
PEG_CRX_GTX_N12	C631	PEG_CRX_C_GTX_N12 AJ23
PEG_CRX_GTX_P13	C632	PEG_CRX_C_GTX_P13 AH23
PEG_CRX_GTX_N13	C633	PEG_CRX_C_GTX_N13 AG23
PEG_CRX_GTX_P14	C634	PEG_CRX_C_GTX_P14 AK24
PEG_CRX_GTX_N14	C635	PEG_CRX_C_GTX_N14 AJ24
PEG_CRX_GTX_P15	C636	PEG_CRX_C_GTX_P15 AL25
PEG_CRX_GTX_N15	C637	PEG_CRX_C_GTX_N15 AK25

SE095224K00 S CER CAP 0.22U 10V K X5R 0402
DIS@ 0.22U_0402_10V6K

AJ11 NC

(15) CLK_PEG_VGA → AL13 PEX_REFCLK
(15) CLK_PEG_VGA# → AK13 PEX_REFCLK_N
VGA_CLKREQ#_R → AK12 PEX_CLKREQ_N

Default unstuffed
R401 @ 200_0402_1%
PEX_TSTCLK_OUT → AJ26 PEX_TSTCLK_OUT
PEX_TSTCLK_OUT# → AK26 PEX_TSTCLK_OUT_N

DGPU_PEX_RST# → AJ12 PEX_RST_N
AP29 PEX_TERMP

R402 2.49K_0402_1% DIS@

+3V_PCH
R501 10K_0402_5%
DGPU_PWROK
Q33 2N7002K_SOT23-3
VGA_CLKREQ#_R → CLK_REQ_VGA# → CLK_REQ_VGA# (15)
R403 @ 0_0402_5%

When REFCLK current is below 20mA, don't need above gate control for CLKREQ_GPU#, and keep REFCLK free running

+PLLVDD
DIS@ C607 0.1U_0402_16V7K
DIS@ C602 22U_0603_6.3V6M
L31 BLM15AX300SN1D DIS@
+1.05VSG
@ C603 10U_0603_6.3V6M
under GPU close to AD8
22U 0603 C941,C945 for layout limitation

+GPU_PLLVDD
L30 BLM15PX181SN1D DIS@
+1.05VSG
DIS@ C640 0.1U_0402_16V7K
DIS@ C642 4.7U_0603_6.3V6M
DIS@ C643 22U_0603_6.3V6M
DIS@ C644 10U_0603_6.3V6M
C640 under GPU close to ball : AE8,AD7

PWR_LEVEL_R — DIS@ D31 RB751V-40_SOD323-2 — PWR_LEVEL (31)
GPU_EVENT#_R — @ D34 RB751V-40_SOD323-2 — GPU_EVENT# (14)
R421 DIS@ 0_0402_5%

+3V_AON
XTAL_OUTBUFF — @ R503 10K_0402_5%
PWR_LEVEL_R — DIS@ R502 100K_0402_5%
XTAL_OUTBUFF — DIS@ R517 10K_0402_5%

(37,45) GPU_OVERT#
RP36 10K_8P4R_5% DIS@: 3V3_MAIN_EN, VGA_ALERT#, GPU_OVERT#, XTAL_SSIN
RP37 2.2K_8P4R_5% DIS@: SMB_CLK_GPU, SMB_DATA_GPU, VGA_EDID_DATA, VGA_EDID_CLK
I2C
RP38 2.2K_8P4R_5% @: VGA_CRT_CLK, VGA_CRT_DATA, HDCP_SDA, HDCP_SCL
RP39 10K_8P4R_5% DIS@: GC6_FB_EN, GPU_EVENT#_R, DGPU_RST_HOLD#
RP35 10K_8P4R_5% DIS@: NVVDD_PSI, VGA_CLKREQ#_R
(37) JTAG_TRST
(37) TESTMODE

(18,45,54) DGPU_PWROK
GC6_FB_EN → SW@ D30 DAN202UT106_SC70-3 → 1.35V_PWR_EN → 1.35V_PWR_EN (45)
DIS@ R488 100K_0402_5%

Green CLK
XTALIN — GCLK@ R516 0_0402_5% — CLK_27M_VGA_XIN (27)

XTALIN — C638 NOGCLK@ 15P_0402_50V8J
Y5 27MHZ 10PF 7V27000050 NOGCLK@ GND GND
C639 NOGCLK@ 15P_0402_50V8J
R423 NOGCLK@ 1K_0402_1% — XTAL_OUT

Internal Thermal Sensor
+3V3_AON
SMB_CLK_GPU → DIS@ Q32B 2N7002KDWH_SOT363-6 → EC_SMB_CK2 (16,31,32)
SMB_DATA_GPU → DIS@ Q32A 2N7002KDWH_SOT363-6 → EC_SMB_DA2 (16,31,32)

+3V3_AON
DIS@ C646 0.1U_0402_25V6K
U40 MC74VHC1G08DFT2G SC70 5P DIS@
(14) DGPU_HOLD_RST#
(14,25,28,31,34) PLT_RST#
SYS_PEX_RST_MON#1
DGPU_RST_HOLD# 2
DGPU_PEX_RST#
DGPU_PEX_RST# (45)

+3V3_AON
SW@ C645 0.1U_0402_25V6K
U39 MC74VHC1G08DFT2G SC70 5P SW@

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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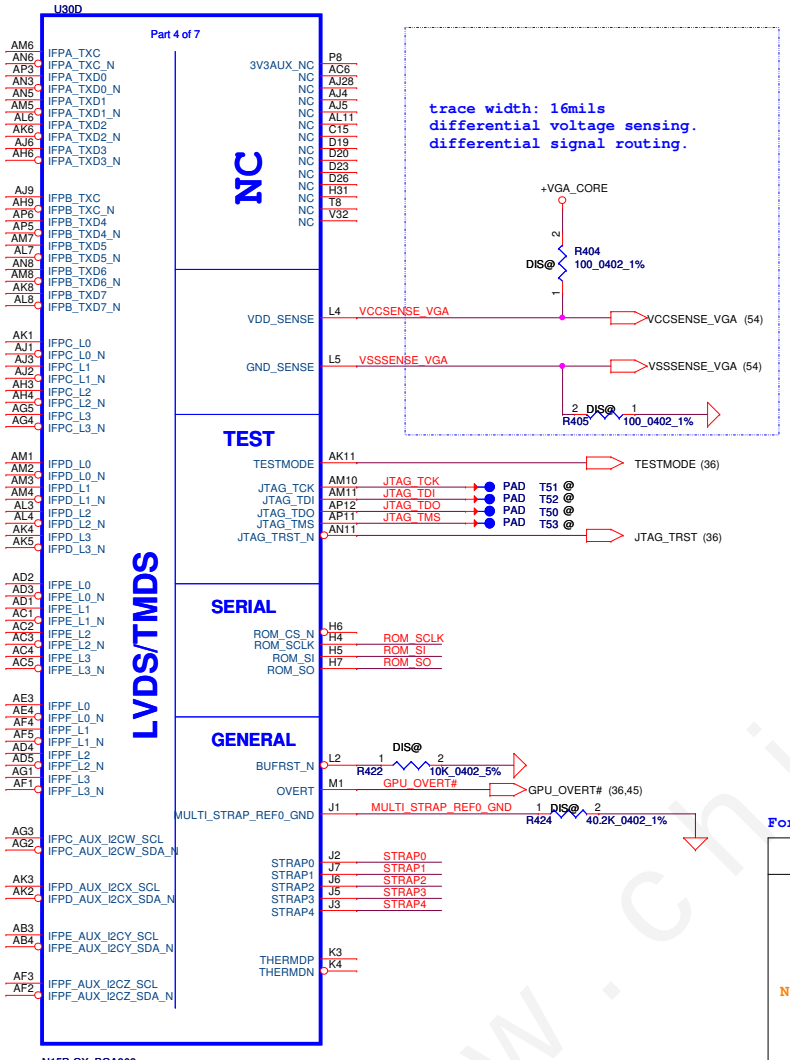
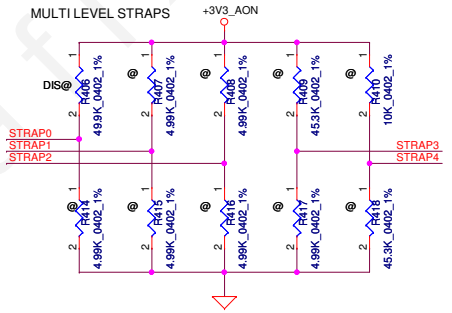
Compal Electronics, Inc.
Title: N15P-GX (1/5) PEG & DAC
Size: Custom | Document Number: LA-B111P | Rev: 1.0
Date: Tuesday, February 25, 2014 | Sheet 36 of 59

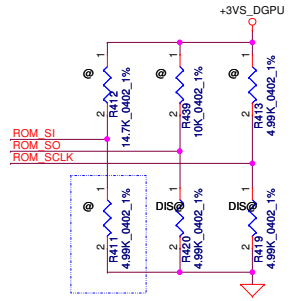


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SO	+3VS_DGPU	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	+3VS_DGPU	**DEVID_SEL**	**PCIE_CFG**	**SMB_ALT_ADDR**	VGA_DEVICE
STRAP0	Keep pull-up to 3V3_AON and pull-down to GND foot print and stuff 50K ohm pull-up				
STRAP1					
STRAP2	RESERVED				
STRAP3					
STRAP4					

SKU	Device ID	bit5 to bit0
N15P-GX	0x1392	

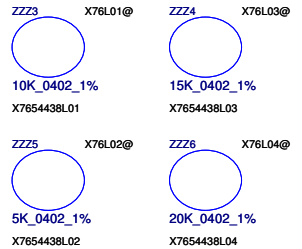
Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111





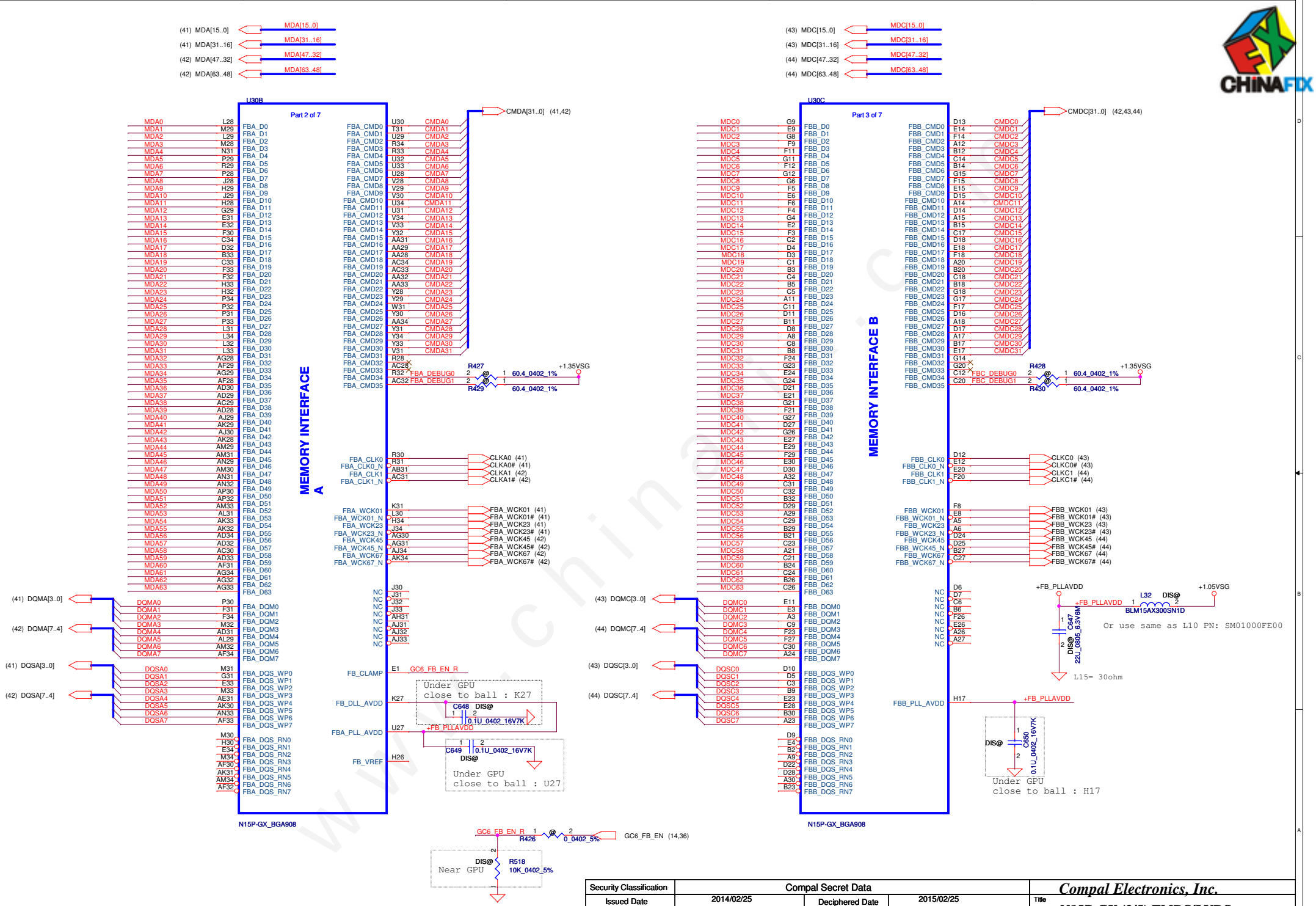
For X76 (N15P-GX)

GPU	FB Memory DDR5					ROM_SI
N15P-GX	128Mx16	X76L02@	Samsung	2G	K4G20325FD-FC03	PD 5K
		X76L01@	Hynix	2G	H5GC2H24BFR-T2C	PD 10K
	256Mx16	X76L03@	Hynix	4G	H5GC4H24MFR-T2C	PD 15K
		X76L04@	Samsung	4G	K4G41325FC-HC03	PD 20K



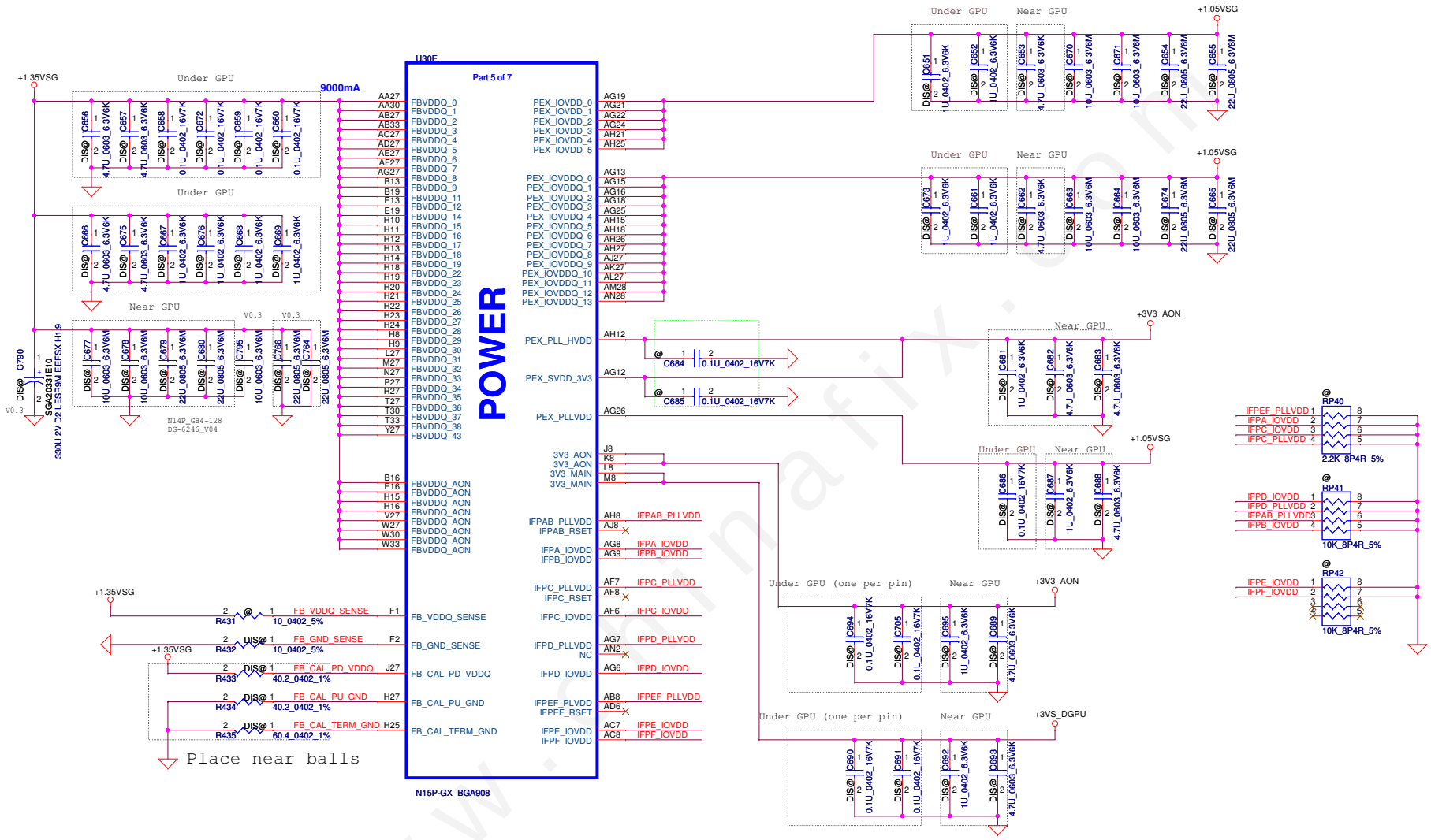
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.			
Title	N15P-GX (2/5) TMDS/LVDS		
Size: Custom	Document Number: LA-B111P		Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 37 of 59		



Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.			
Title: N15P-GX (3/5) TMDS/LVDS			
Size: B (3275 Custom)	Document Number: LA-B111P		Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 38 of 59		



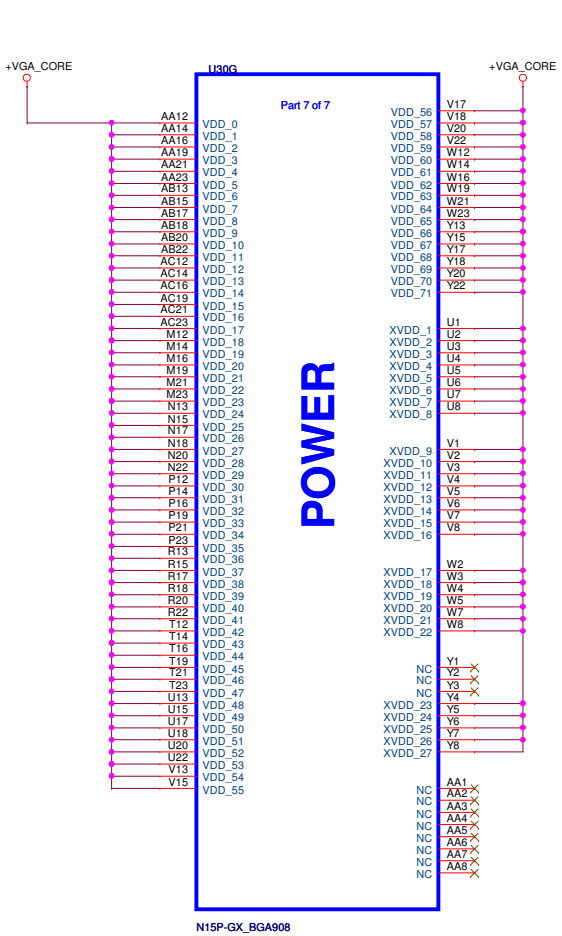
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

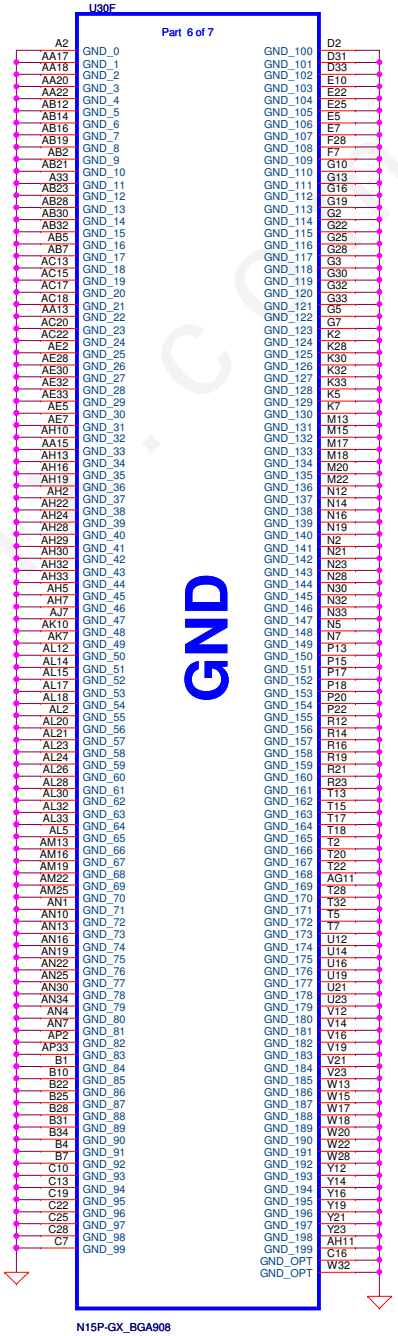
Compal Electronics, Inc.

Title: N15P-GX (4/5) POWER

Size: Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 39 of 59





Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: N15P-GX (5/5) POWER/ GND

Size: Custom | Document Number: LA-B111P | Rev: 1.0

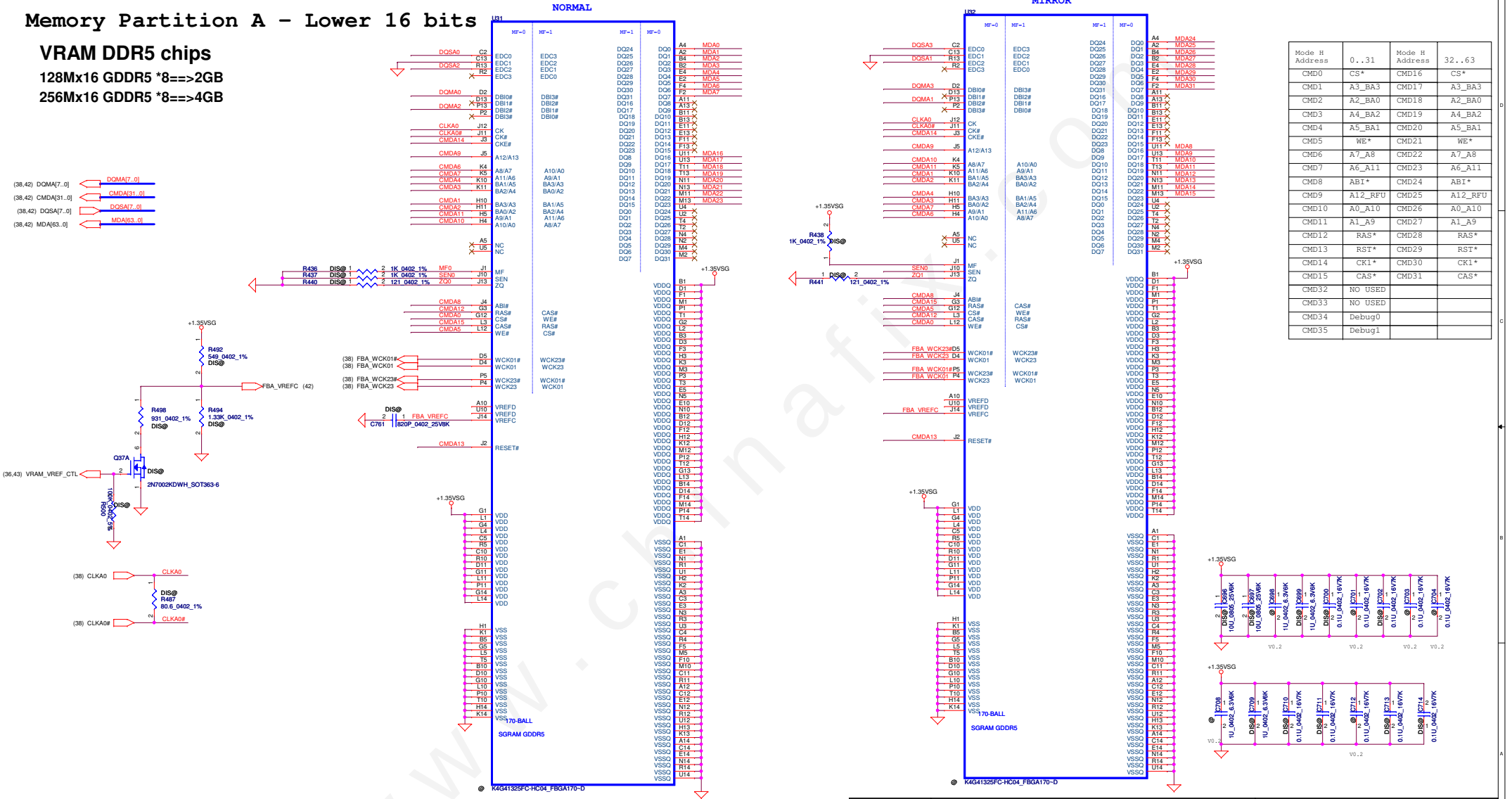
Date: Tuesday, February 25, 2014 | Sheet 40 of 59

Memory Partition A – Lower 16 bits

VRAM DDR5 chips

128Mx16 GDDR5 *8==>2GB

256Mx16 GDDR5 *8==>4GB



Mode H Address	0..31	Mode H Address	32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CK1*	CMD30	CK1*
CMD15	CAS*	CMD31	CAS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

Compal Electronics, Inc.

Title: N15P-GX GDDR5 1/4

Size: Custom | Document Number: LA-B111P | Rev: 1.0

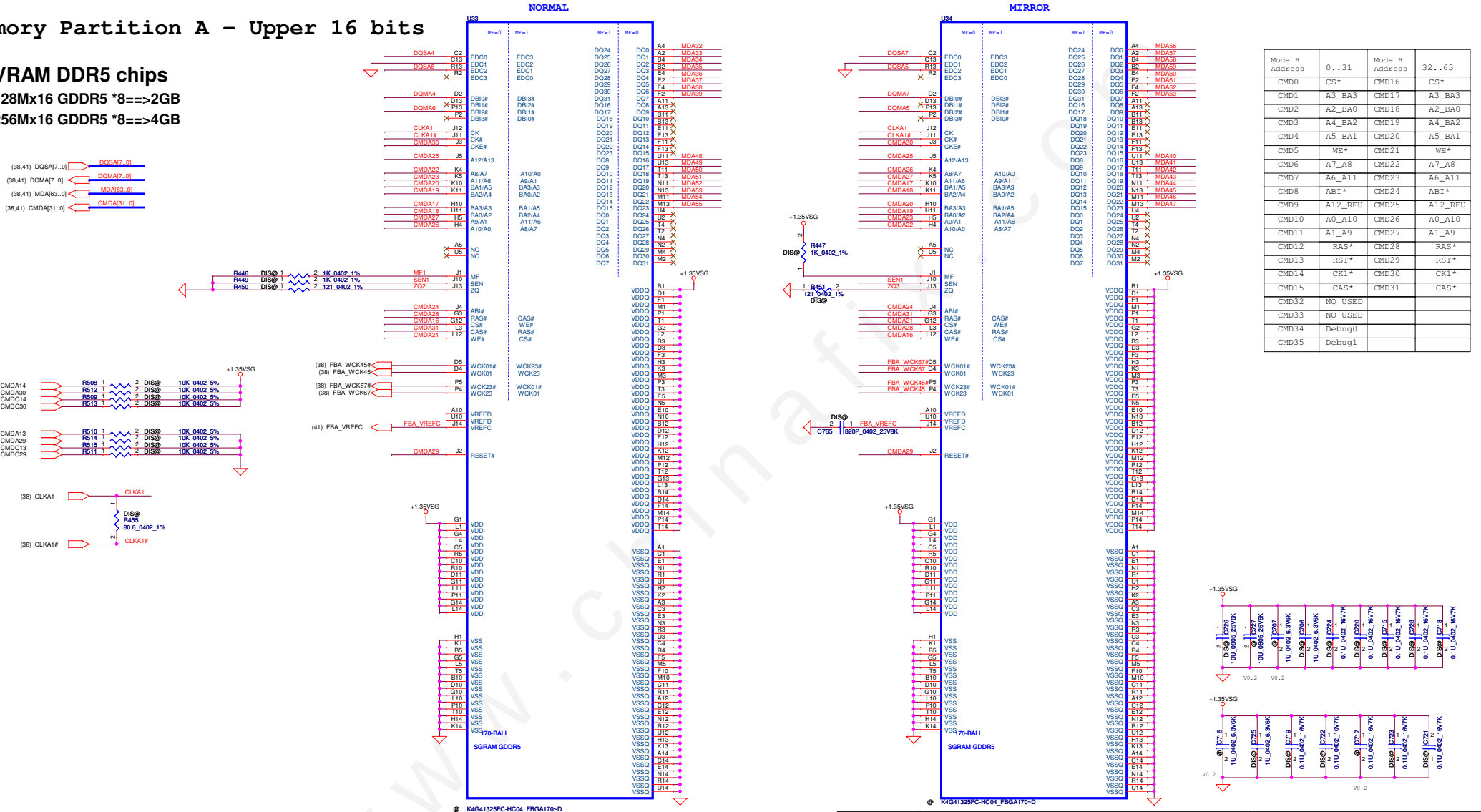
Date: Tuesday, February 25, 2014 | Sheet 41 of 59

Memory Partition A - Upper 16 bits

VRAM DDR5 chips

128Mx16 GDDR5 *8==>2GB

256Mx16 GDDR5 *8==>4GB



Mode H Address	0..31	Mode H Address	32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CK1*	CMD30	CK1*
CMD15	CAS*	CMD31	CAS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

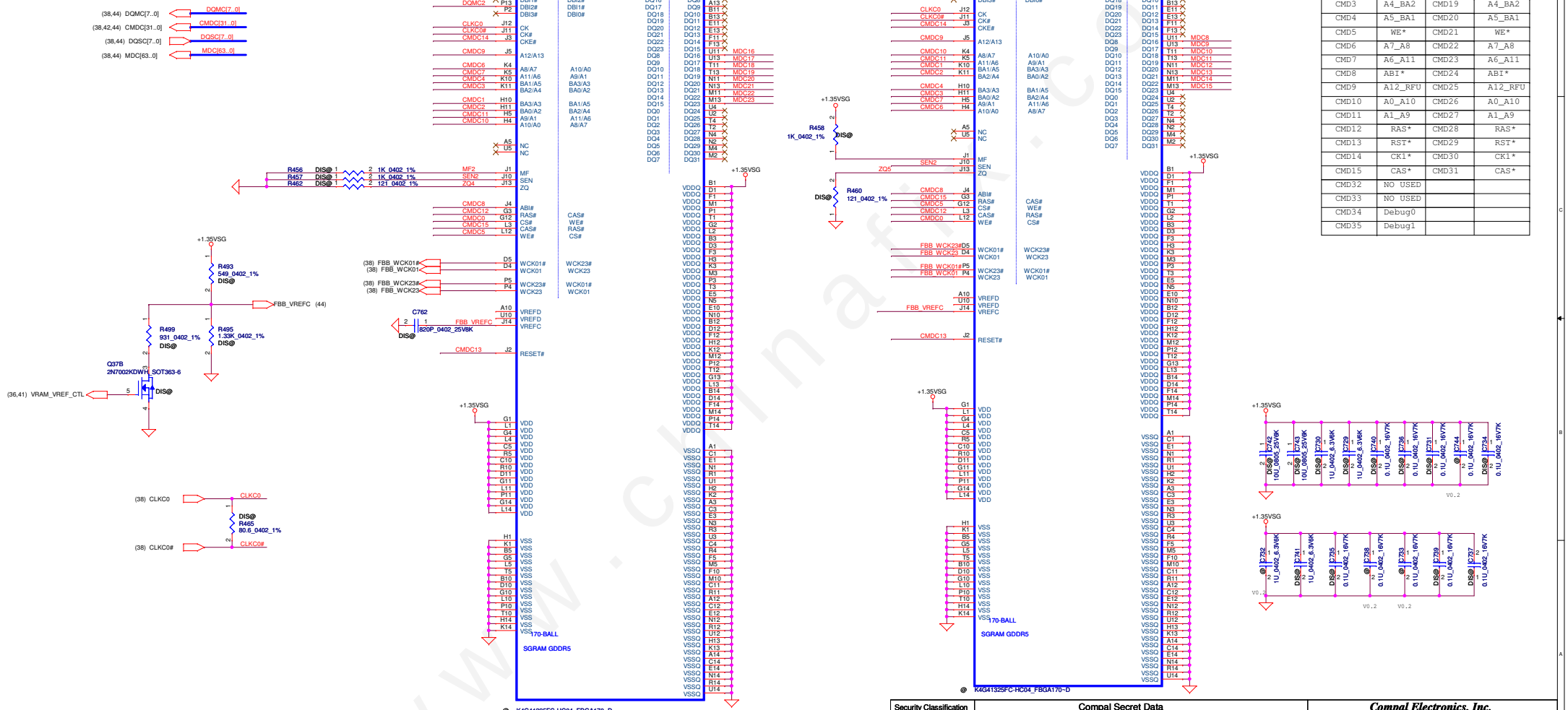
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/02/25	Deciphered Date	2015/02/25
Title	N15P-GX GDDR5 2/4		
Size	Custom	Document Number	LA-B111P
Rev	1.0		
Date:	Tuesday, February 25, 2014	Sheet	42 of 59

Memory Partition B - Lower 16 bits

VRAM DDR5 chips

128Mx16 GDDR5 *8==>2GB

256Mx16 GDDR5 *8==>4GB



Mode H Address	0..31	Mode H Address	32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CK1*	CMD30	CK1*
CMD15	CAS*	CMD31	CAS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/02/25	Deciphered Date	2015/02/25

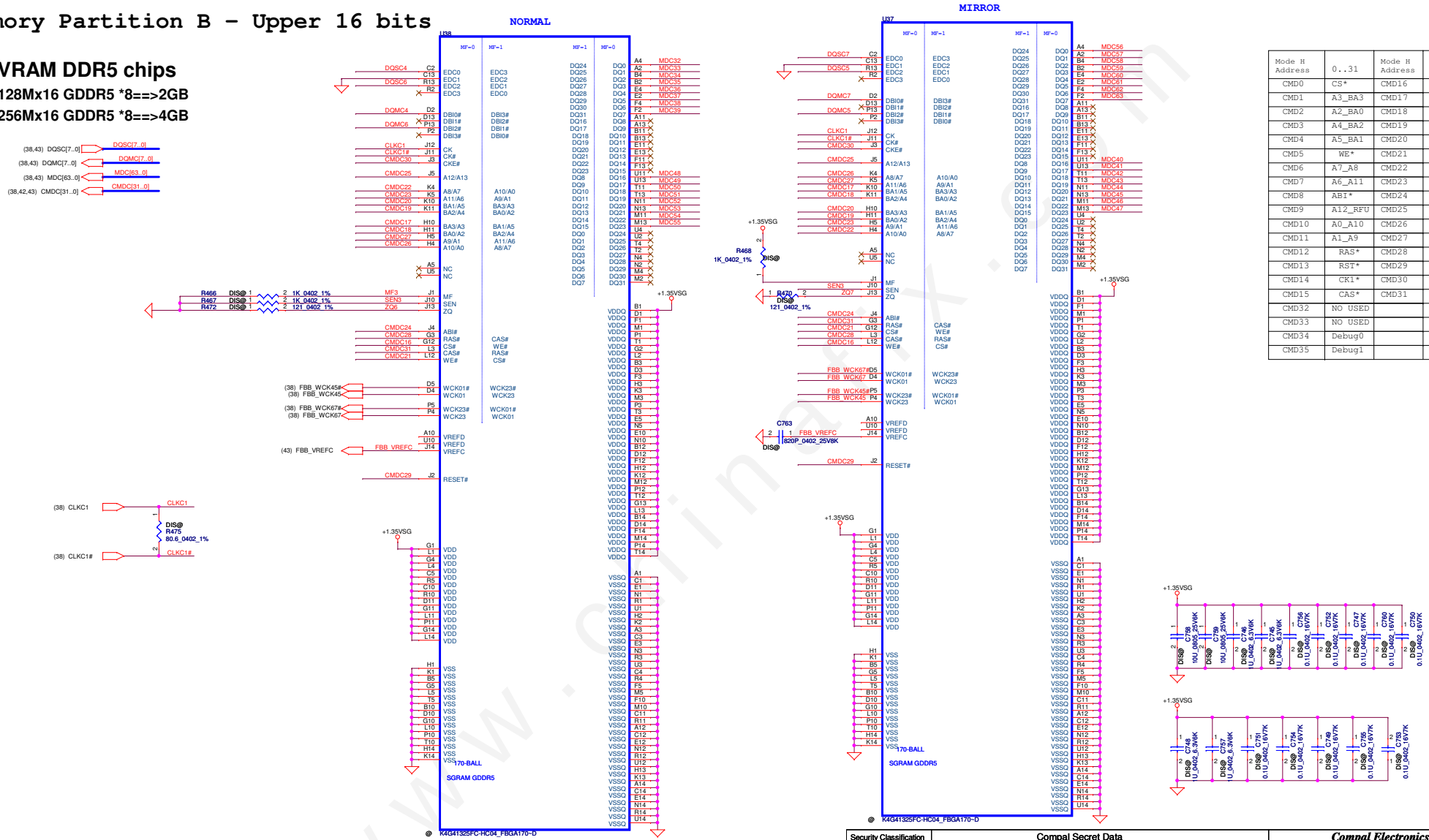
Title	N15P-GX GDDR5 3/4		
Size	Custom	Document Number	LA-B111P
Rev	1.0		
Date:	Tuesday, February 25, 2014	Sheet	43 of 59

Memory Partition B - Upper 16 bits

VRAM DDR5 chips

128Mx16 GDDR5 *8==>2GB

256Mx16 GDDR5 *8==>4GB



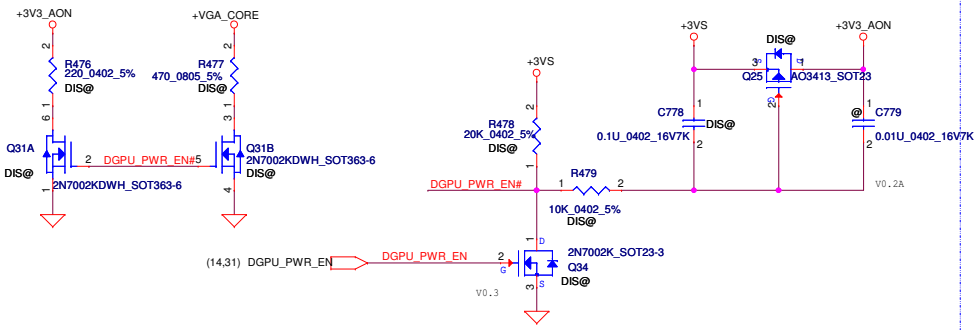
Mode H Address	0..31	Mode H Address	32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CK1*	CMD30	CK1*
CMD15	CAS*	CMD31	CAS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Title	N15P-GX GDDR5 4/4		
Size	Document Number		Rev
Custom	LA-B111P		1.0
Date: Tuesday, February 25, 2014	Sheet 44 of 59		

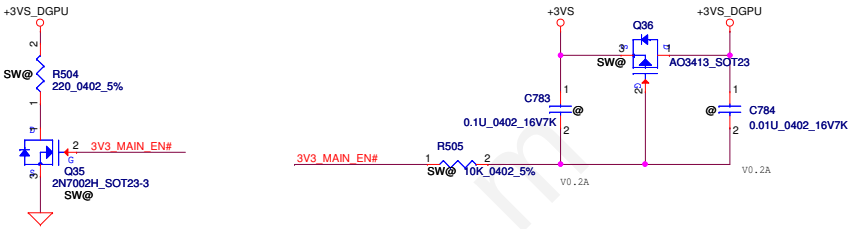
+3VS to +3V3_AON

Vgs=-4.5V,Id=3A,Rds<97mohm

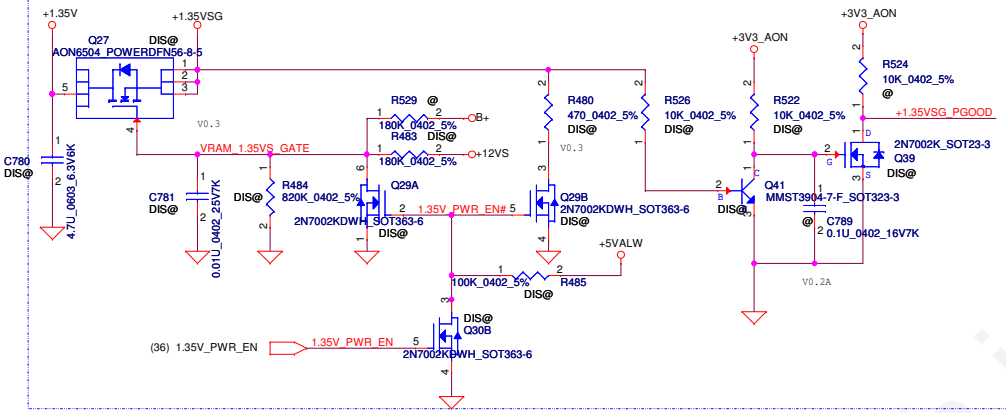


+3VS to +3VS_DGPU

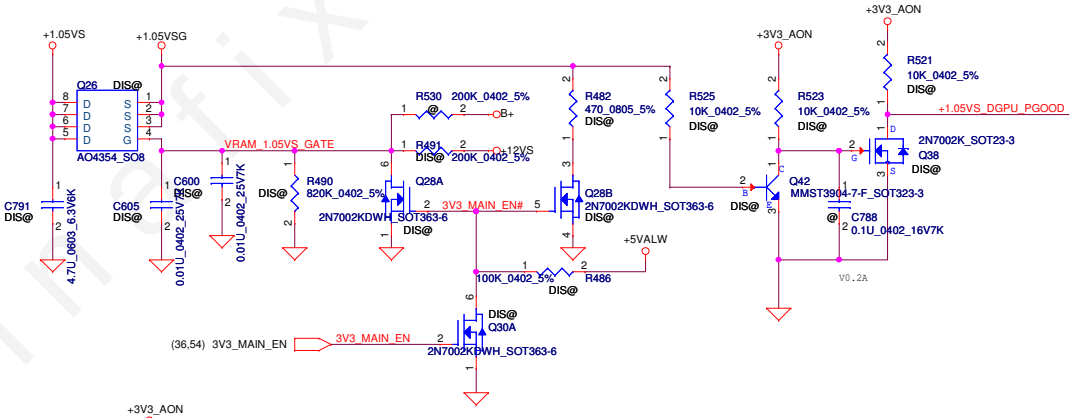
Vgs=-4.5V,Id=3A,Rds<97mohm

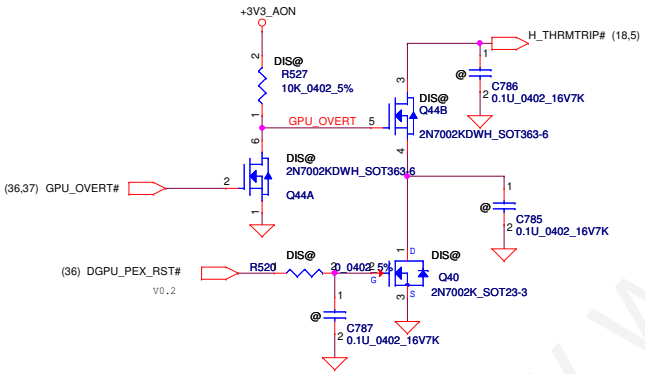


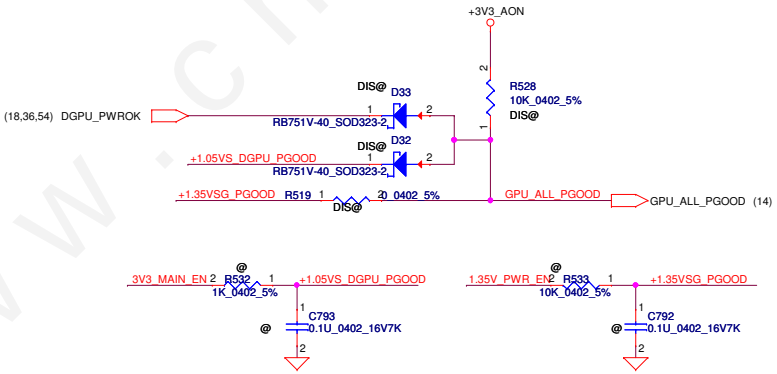
+1.35V to +1.35VSG



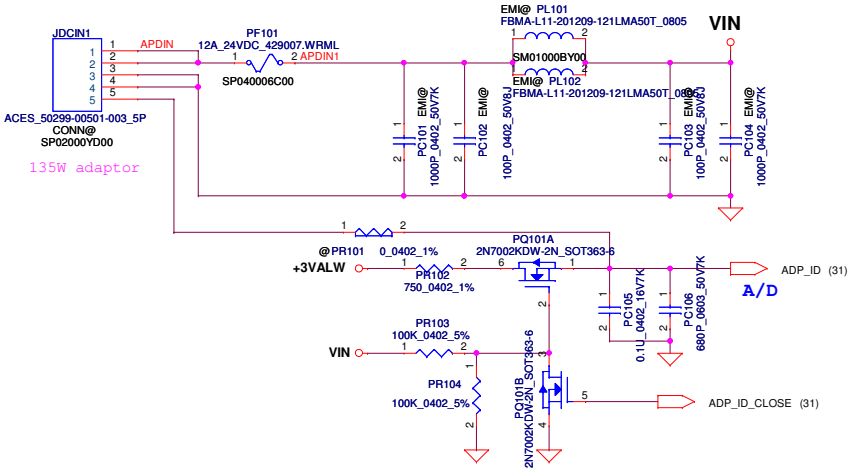
+1.05VS to +1.05VSG

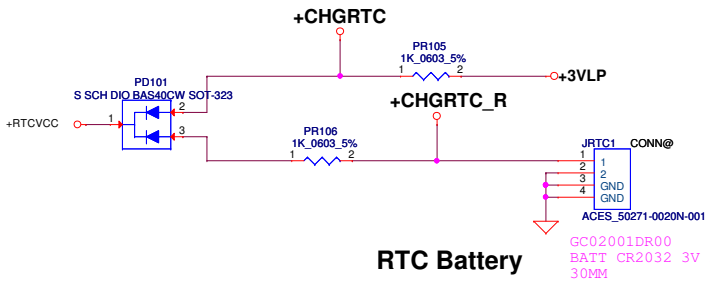






Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/02/25	Deciphered Date 2015/02/25	Title: N15P-GX DC-DC
Size: Custom	Document Number: LA-B111P		Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 45 of 59		





RTC Battery

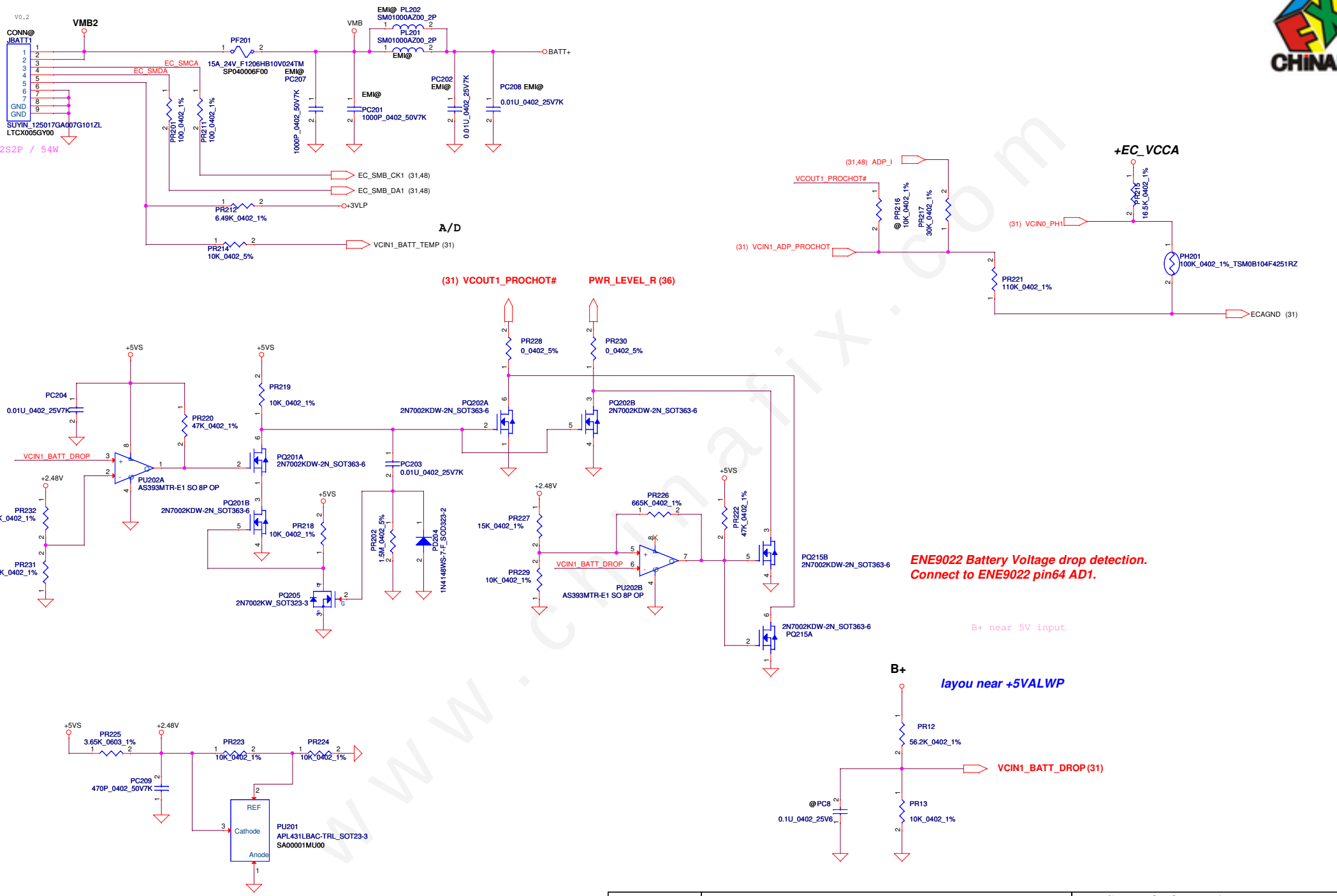
GC02001DR00
BATT CR2032 3V 210MAH MB 5 W/C
30MM

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: **PWR DCIN / RTC Battery**

Size: Custom	Document Number: BE_BDW	Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 46 of 59	



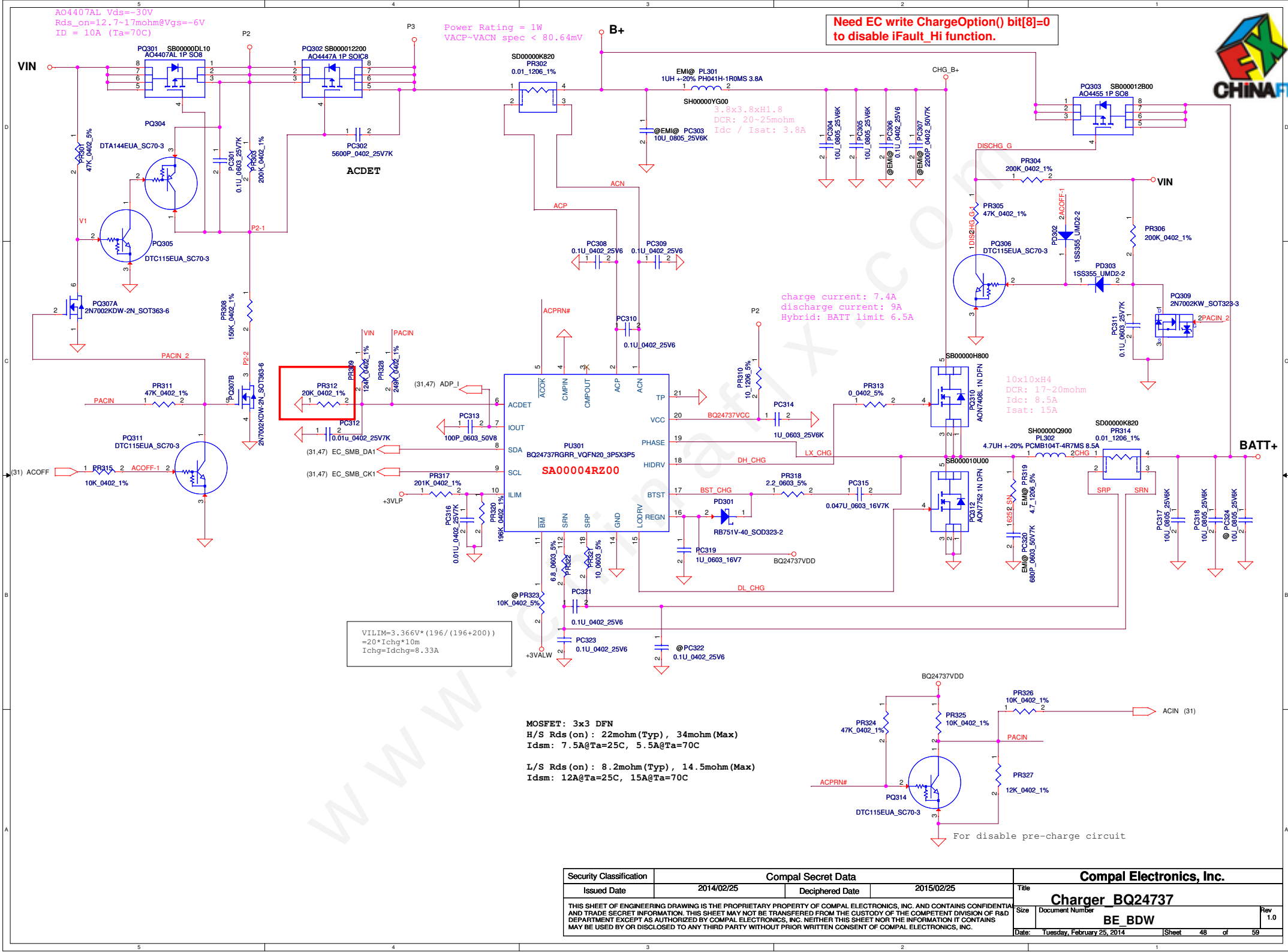
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 47 of 59



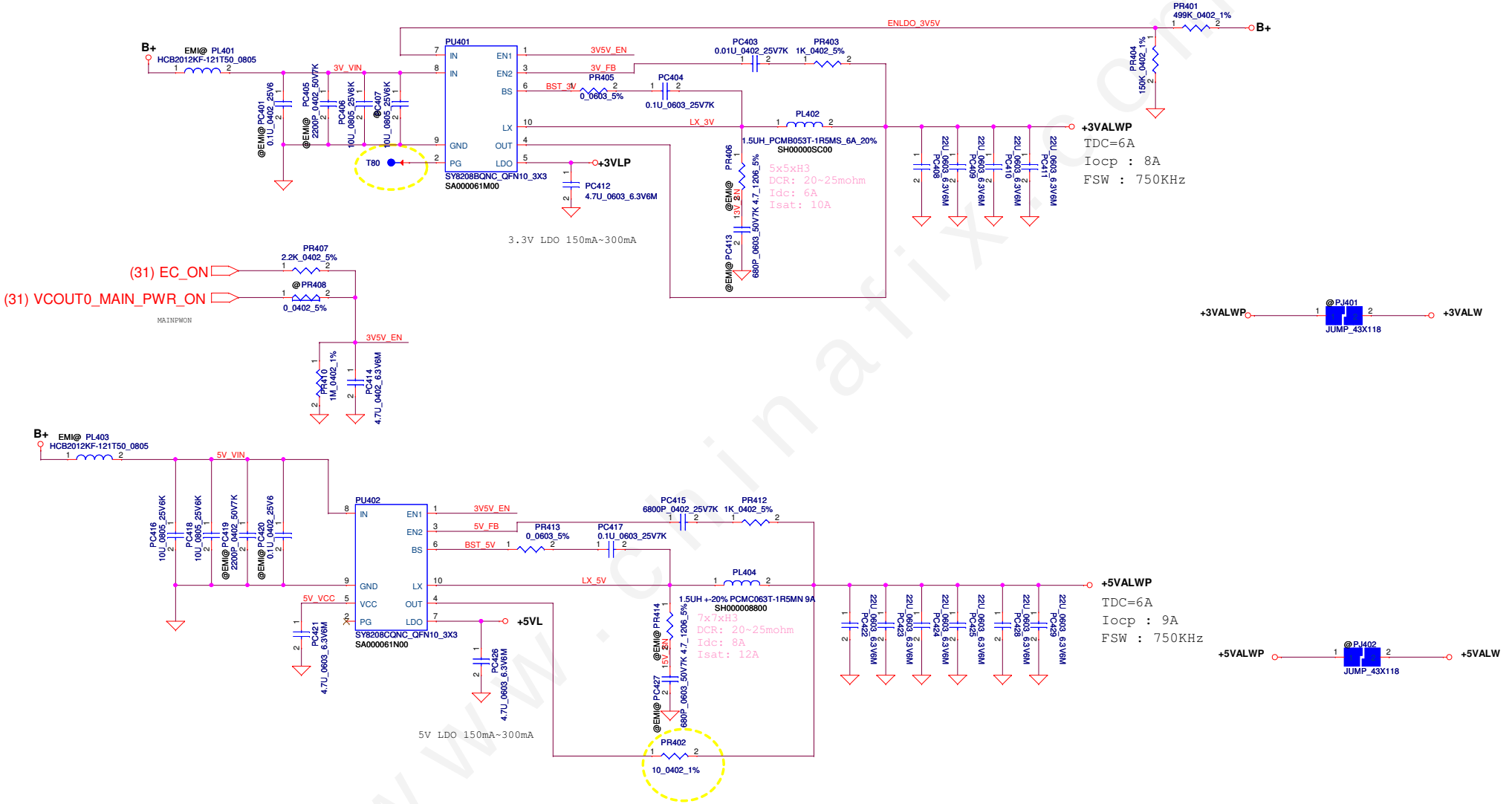
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: **Charger_BQ24737**

Size: | Document Number: **BE_BDW** | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 48 of 59



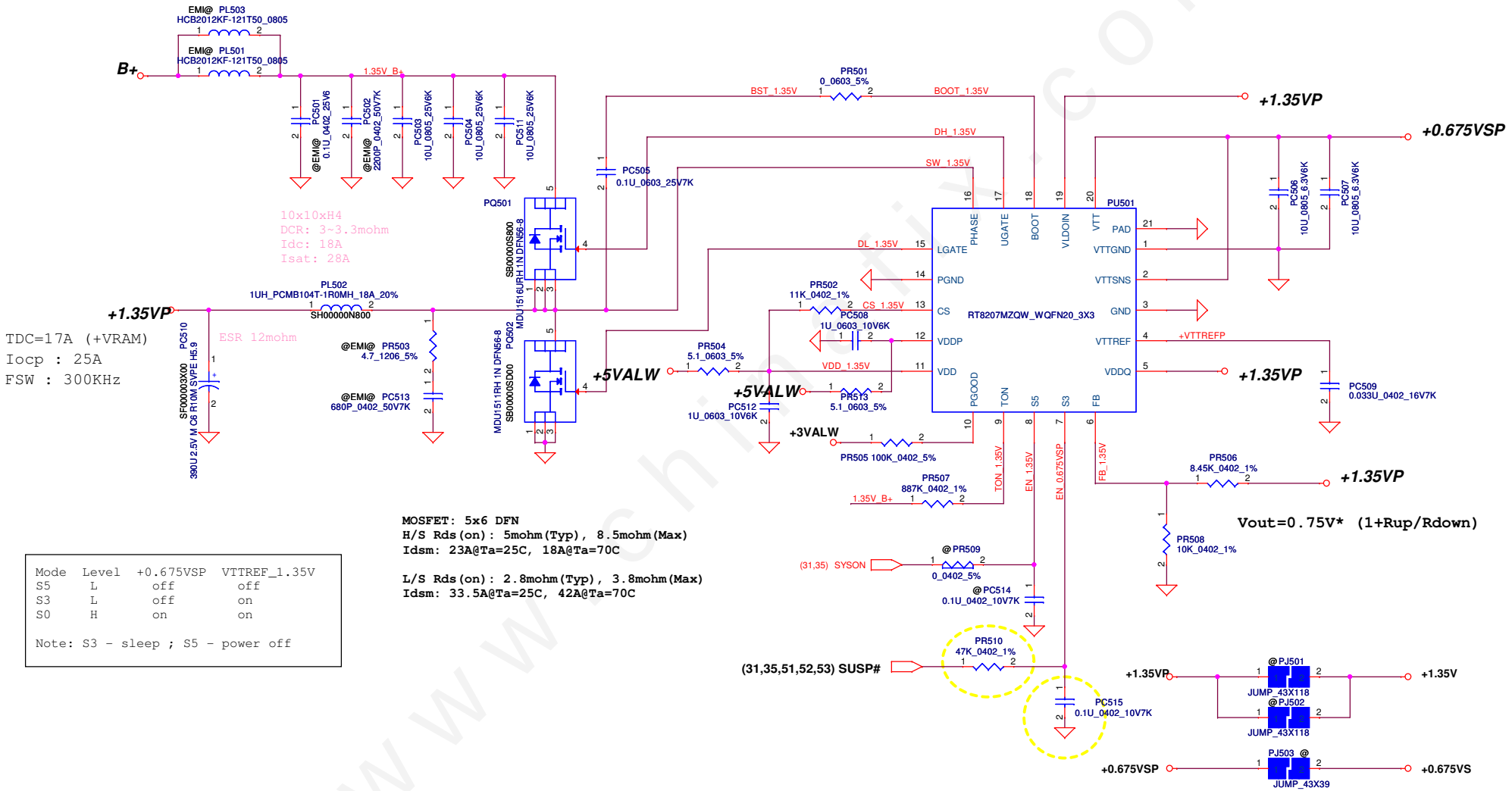
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 49 of 59



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

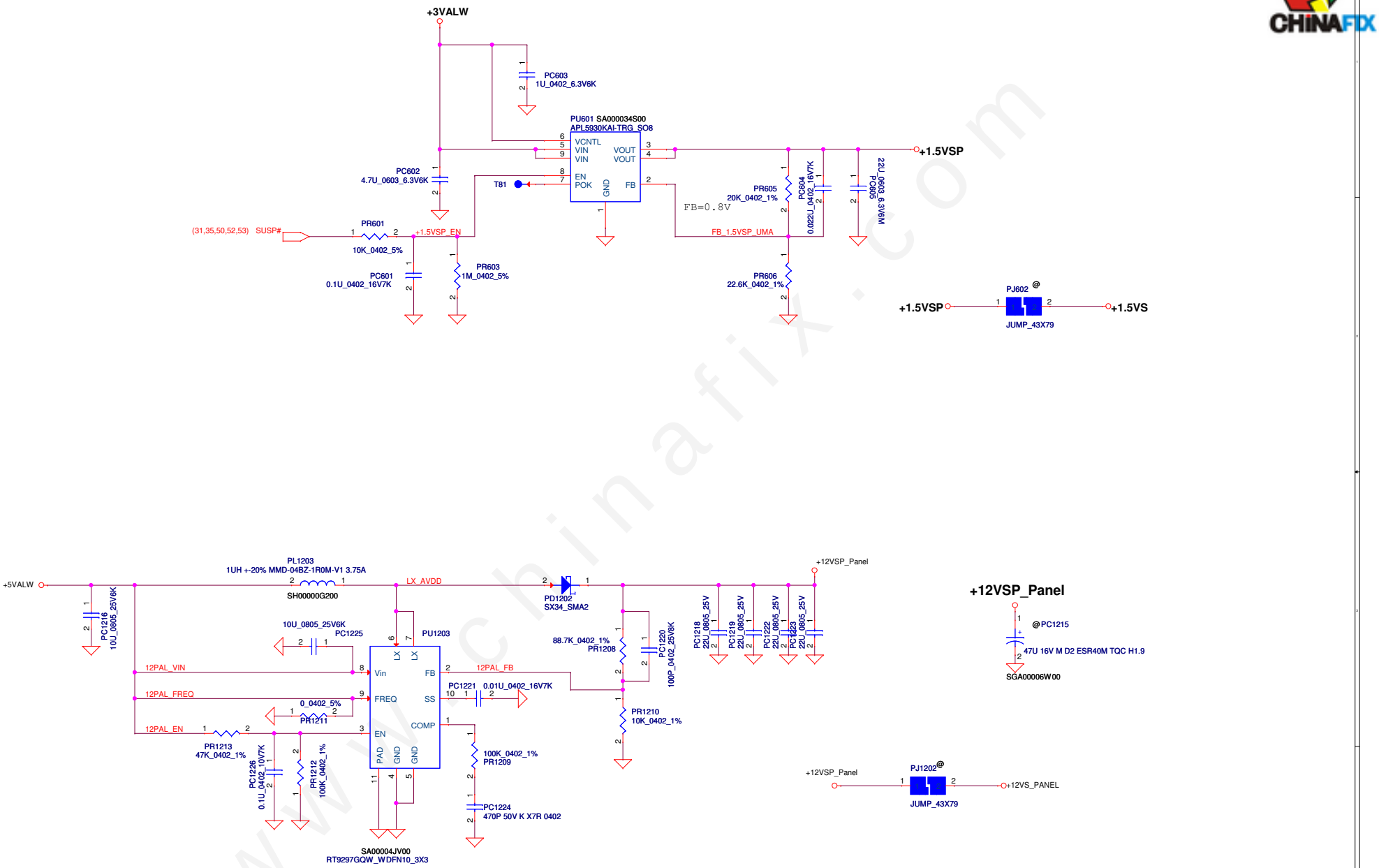
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: RT8207M

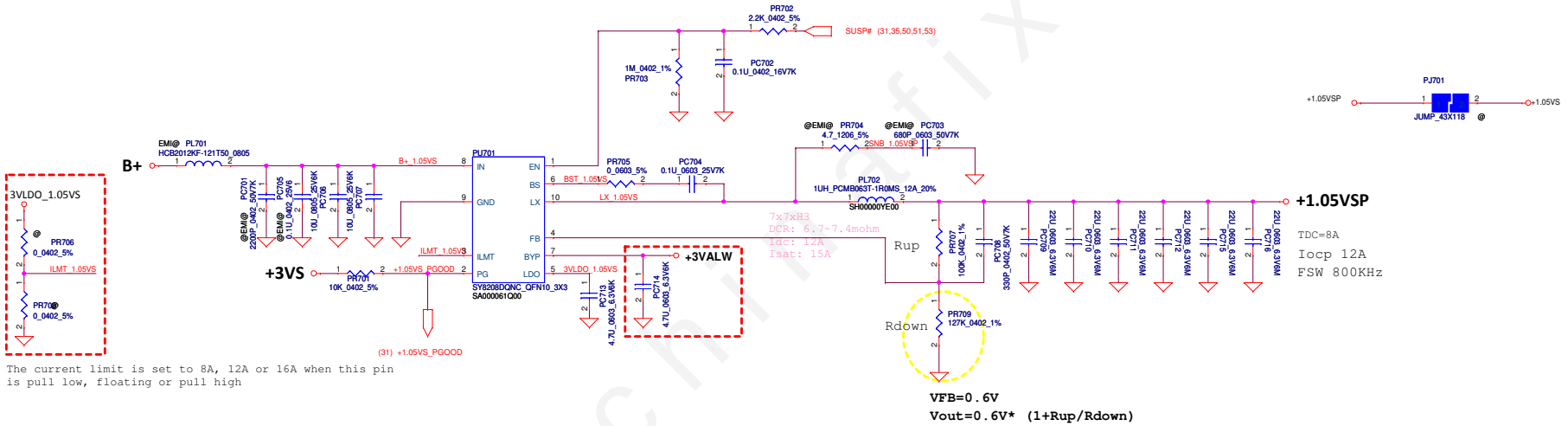
Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 50 of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Title	+1.5VS		
Size: Custom	Document Number: BE_BDW		Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 51 of 59		



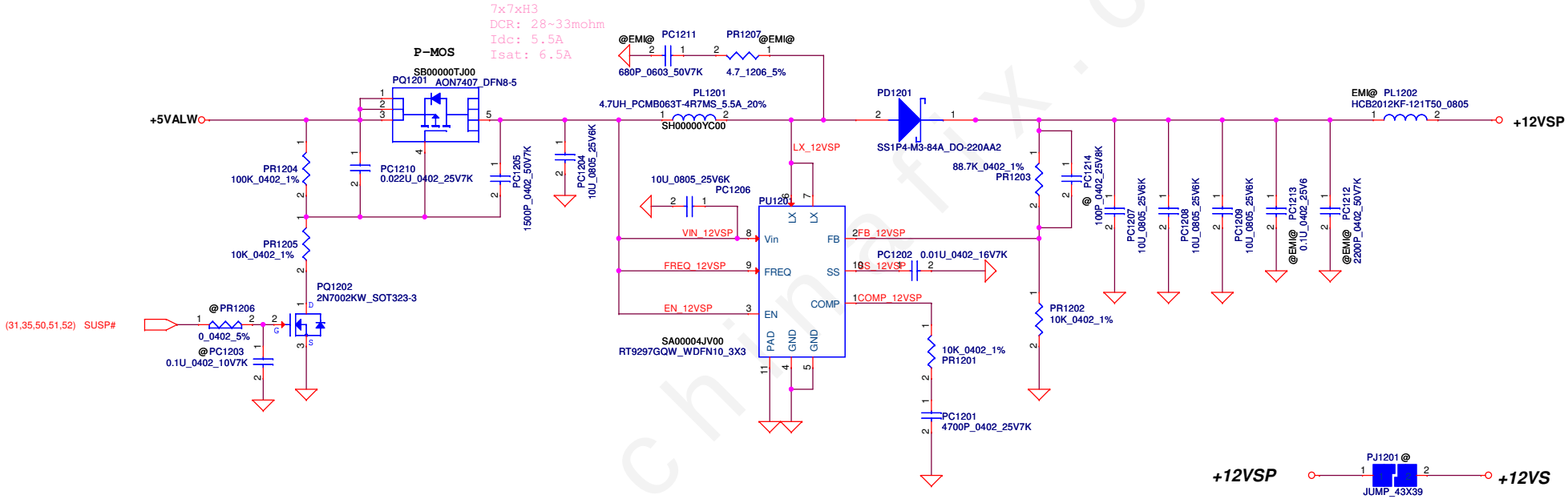
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: +1.05VS

Size	Document Number	Rev
C	BE_BDW	1.0

Date: Tuesday, February 25, 2014 Sheet 52 of 59



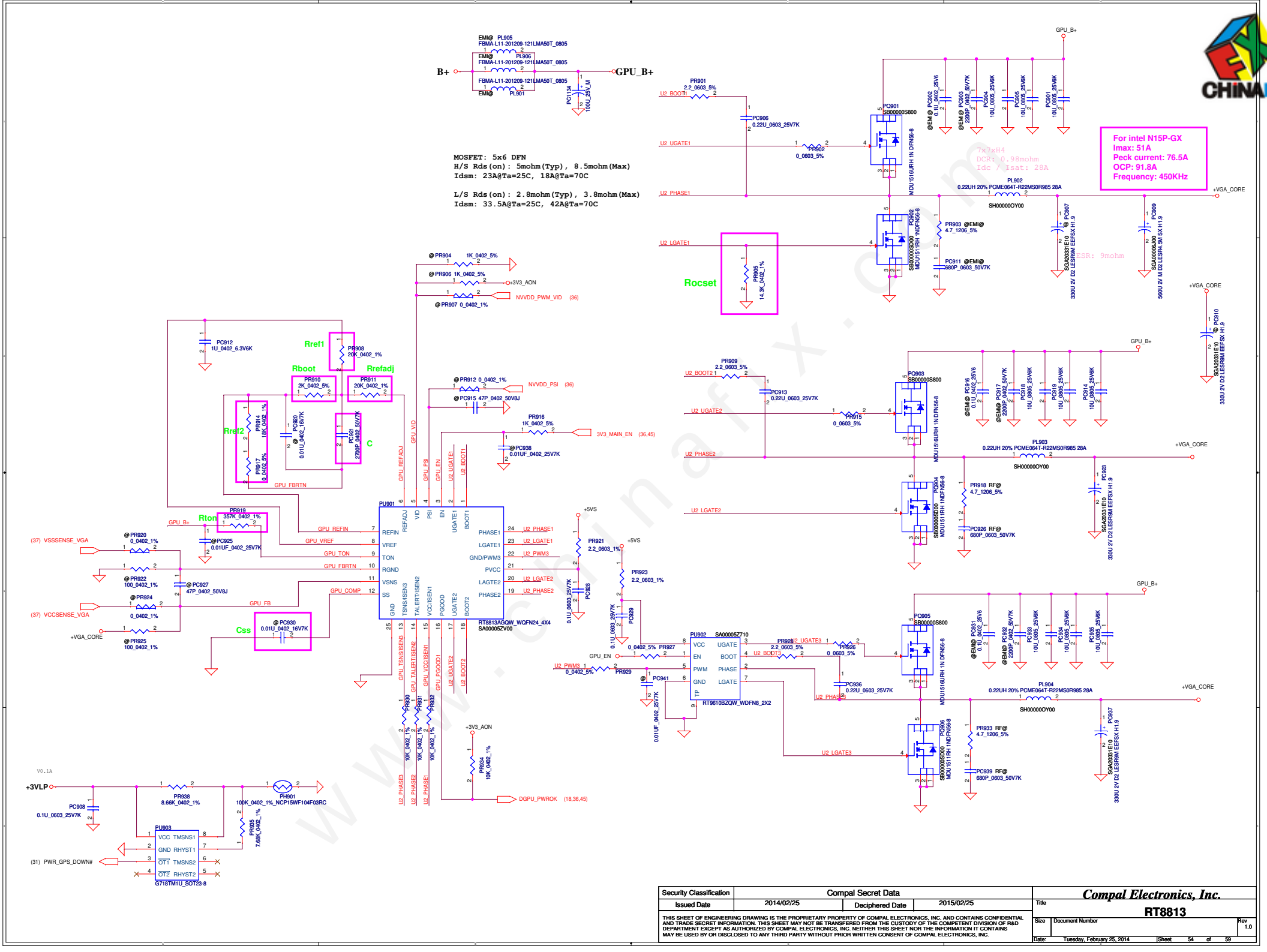
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	

Compal Electronics, Inc.

Title: **+12V-Boost**

Size	Document Number	Rev
A3	VPUAE	1.0

Date: Tuesday, February 25, 2014 Sheet 53 of 59



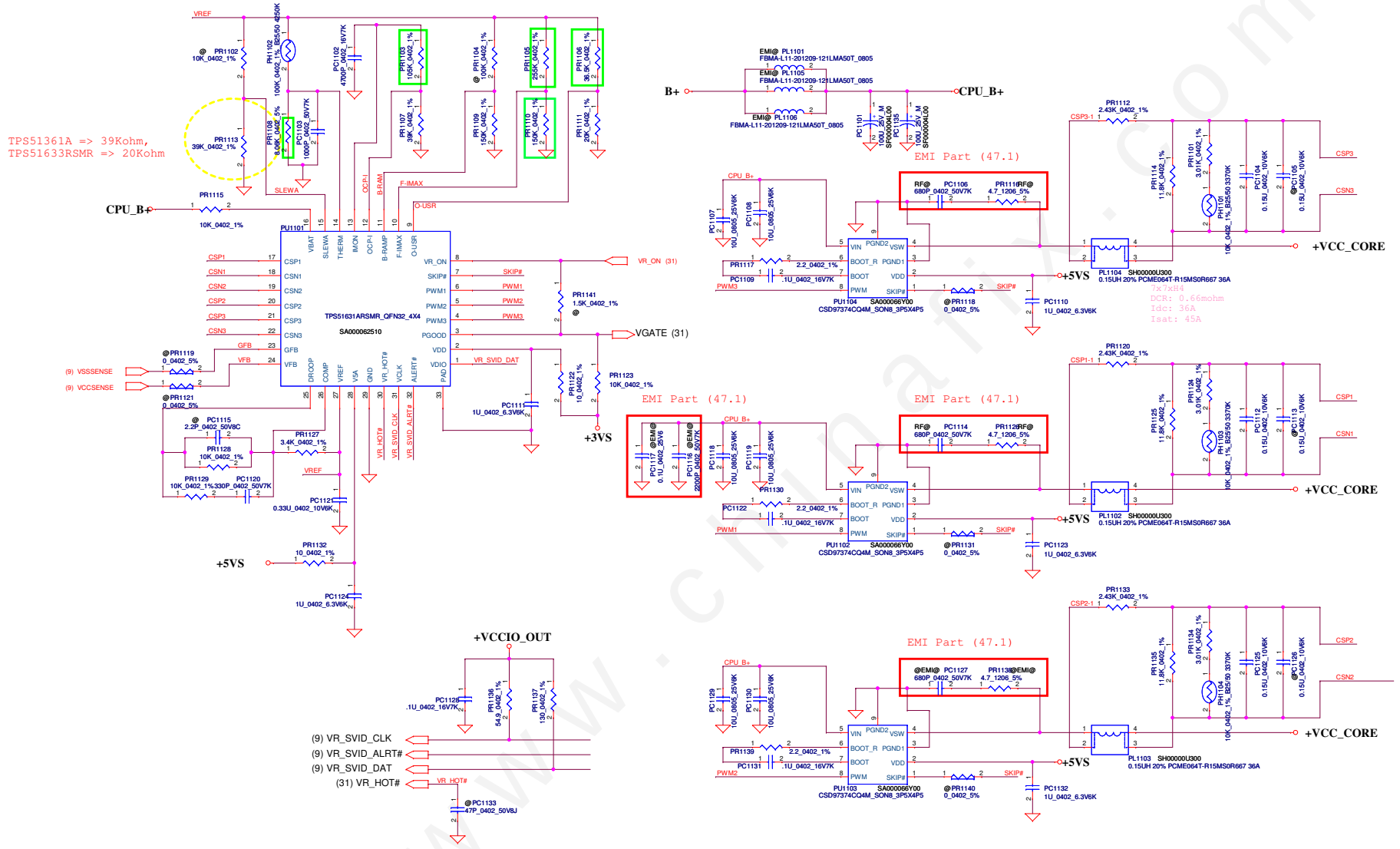
Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: **RT8813**

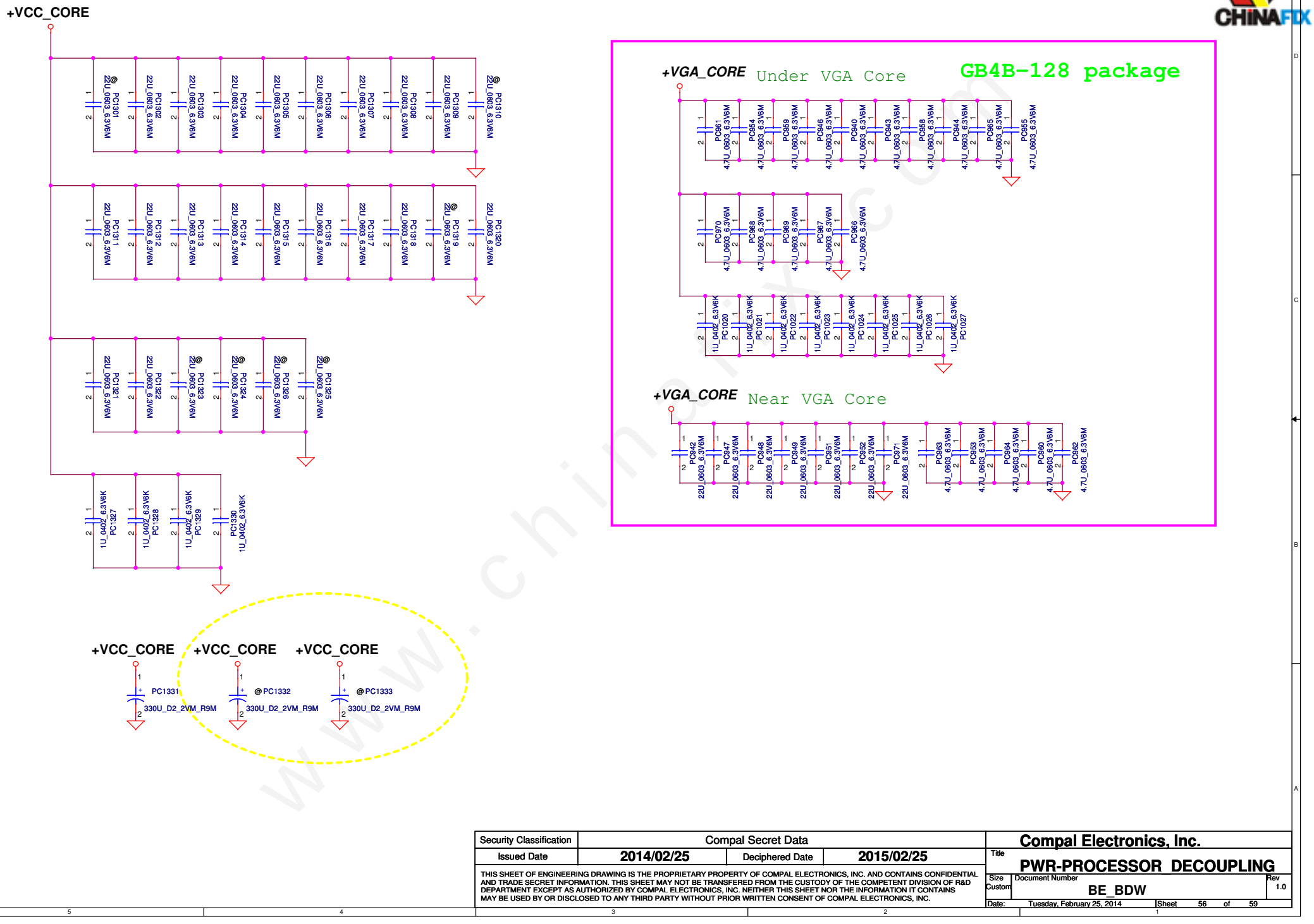
Size	Document Number	Rev
		1.0

Date: Tuesday, February 25, 2014 | Sheet 54 of 59



For intel SB 47W
TDC: 33A
Support Turbo: 95A
OCP setting: 114A
Frequency: 1MHz
DC_LL: -1.5mV/A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/02/25	Deciphered Date	2015/02/25
Title	CPU_CORE-47W		
Size	Custom	Document Number	Rev 1.0
Date:		Sheet 55 of 59	



Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: **PWR-PROCESSOR DECOUPLING**

Size	Document Number	Rev
Custom	BE_BDW	1.0

Date: Tuesday, February 25, 2014 Sheet 56 of 59

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	for panel Vdrop	51	add boost solution	11/15	SIV
2	for EMI request	48	PR319, PC320 change to mount	11/15	SIV
3	for RF request	54	PR918, PC926, PR933, PC939 change to mount	11/18	SIV
4	for RF request	55	PC1114, PR1126, PC1106, PR1116 change to mount	11/18	SIV
6	battery can't be remove	47	del PR222, PR227, PC204, PR220, PU202, PC206, PR226, PD201, PC205, PR218, PR219, PQ201, PQ205, PR228	12/30	SIT
7	for acoustic noise	55, 56	add PC1135, 1332	12/30	SIT
8	SIV rework	48	PR309 is changed from 392K_0402_1% to 124K_0402_1% (SD034124380) PR312 is changed from 59K_0402_1% to 20K_0402_1% (SD034200280) Add a resistor 249K_0402_1% (SD034249380) between pin 6 of PU301 and PACIN. PC312 is changed from 2200pF_0402_25V_X7R to 0.01uF_0402_25V_X7R (SE075103K80) PQ302 change to AO4447A	12/30	SIT
9	SIV rework	47	PR217 change to 30K PR221 change to 110k	12/30	SIT
10	for HW request	50	PR506 change to SD000000680 8.45K 1%	12/30	SIT
11	accuracy modify	52	PR707 change to 100K +-1% PR709 change to 127K +-1%	1/20	SVT
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

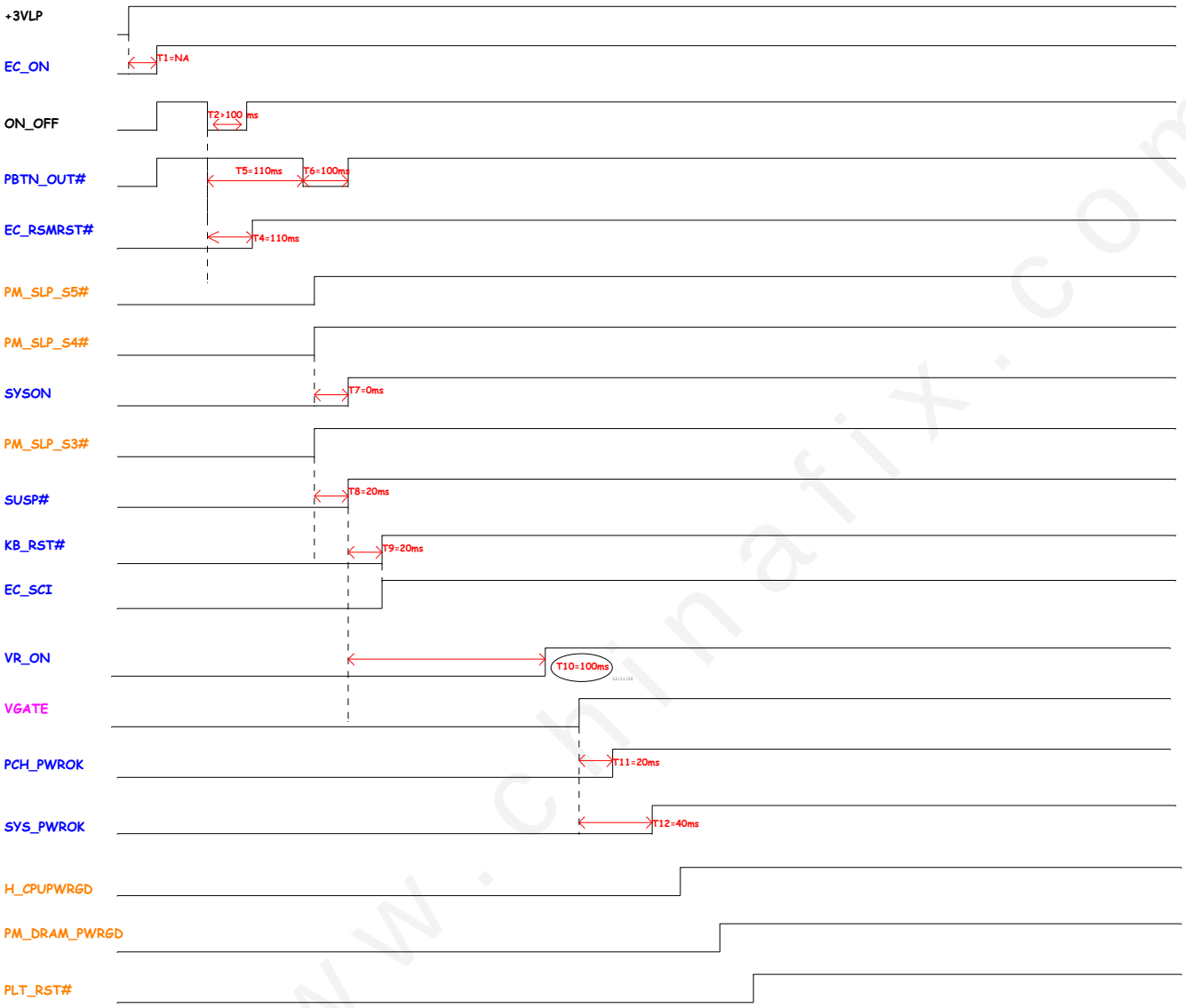
Compal Electronics, Inc.		
Title: PIR (PWR)		
Size: Custom	Document Number: BE_BDW	Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 57 of 59	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase	Verify

1		Add 3D Camera function	0.2	23
				
				22
					Add U25,C502~C511.
					Add R386~R400,R550~R559.
					Del Q14,R205,C319
					Add U13
						10/30	SIV	SIV Phase

2		Remove LPF for woofer amplifier	0.2	27	Change R224->20K,R297->62K Change R1564,R1565->0 ohm,R341->15K, Change R342->20.5K,R81->200K. un-stuff C450,C443	10/30	SIV	Verified by SDV rework.
3		AC/DC detect issue	0.2	14 31	Del D1 Add AC_PRESENT_R to U18 pin 19	11/03	SIV	Verified by SDV rework.
4		Change USB power switch (follow B/E series)	0.2	30	Change U16,U17->SY6288D20AAC	11/04	SIV	Verified by SDV rework.
5		Add resistor for 15"/17" K/B co-lay	0.2	31	Add R1001~R1012,R1021~R1032	11/04	SIV	SIV Phase
6		Cancel 3D Camera function	0.3	23 22	Del U25,C502~C508 Del R387~R400,R550~R557. Del R255,R256,R261,R262,L41,L42,D21. Del R204,R386,R558,R559	12/17	SIT	SIT Phase
7		TP lock LED function	0.3	31	TP_LOCK_LED# from U18_pin34 to LED	12/24	SIT	Verified by SIV rework.
8		KB Backight behavior	0.3	32	Add R337,R335,C434,Q23	12/24	SIT	Verified by SIV rework.
9		Improve VRAM +1.35V	0.3	39	C790 stuff 330uf	12/25	SIT	Verified by SIV rework.
10		Hole size change for Thermal bracket.	1.0	34	H1,H2,H3,H4,H5,H6 : change to 4.2 mm.	2/5	SVT	Verified by SIT rework.
11		ESD reserve	1.0	32	Reserve C479,C480.	2/5	SVT	SVT Phase
12								
13								
14								
15								
16								
17								
18								
19								
20								

Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.		
Title: Power Sequence		
Size: Custom	Document Number: LA-B111P	Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 38 of 60	