ZZZ1
DA2@
MAIN BOARD
DA600007E10
PCB

Compal Confidential

KAYF0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-09

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

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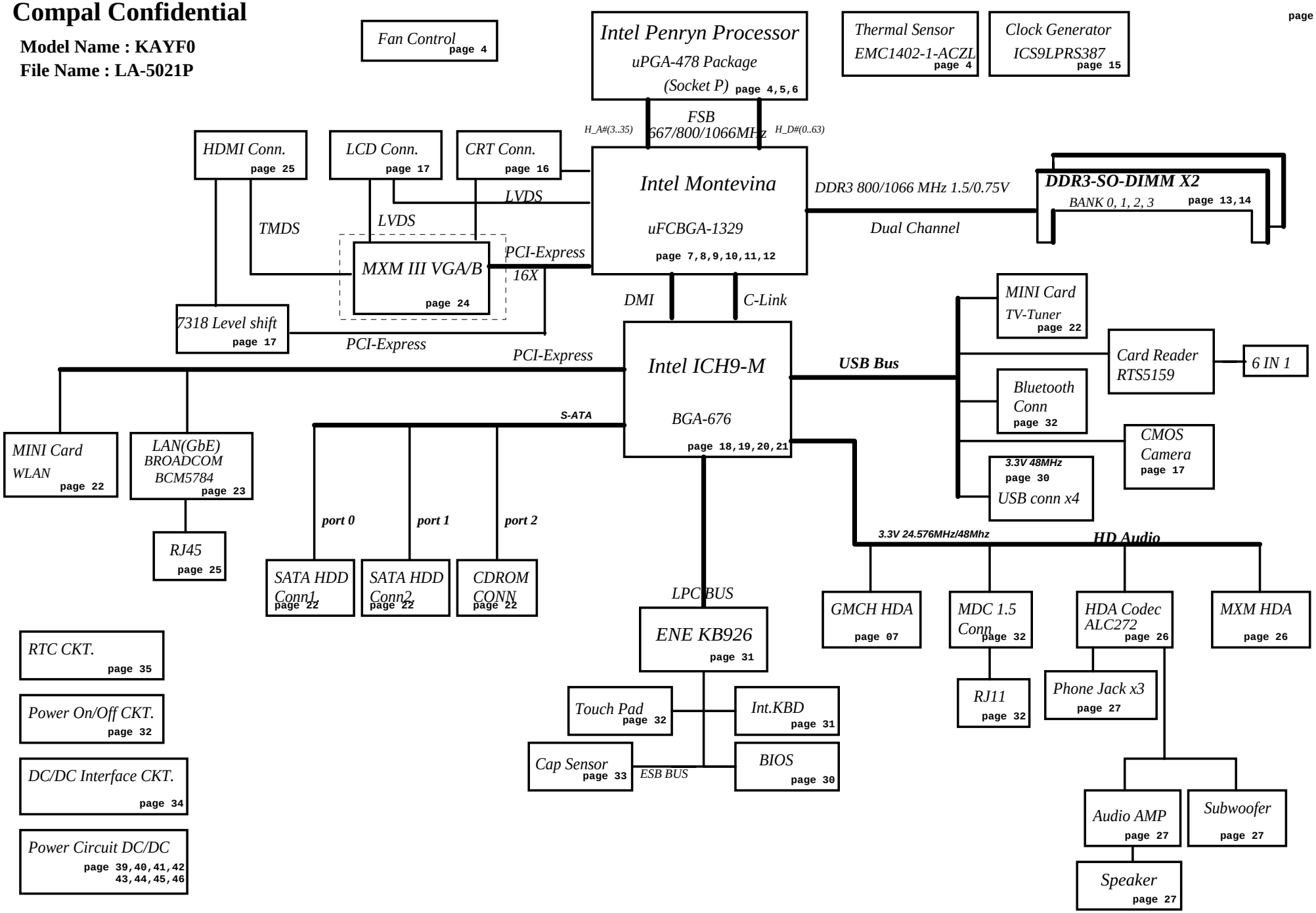
Model Name : KAYF0
File Name : LA-5021P



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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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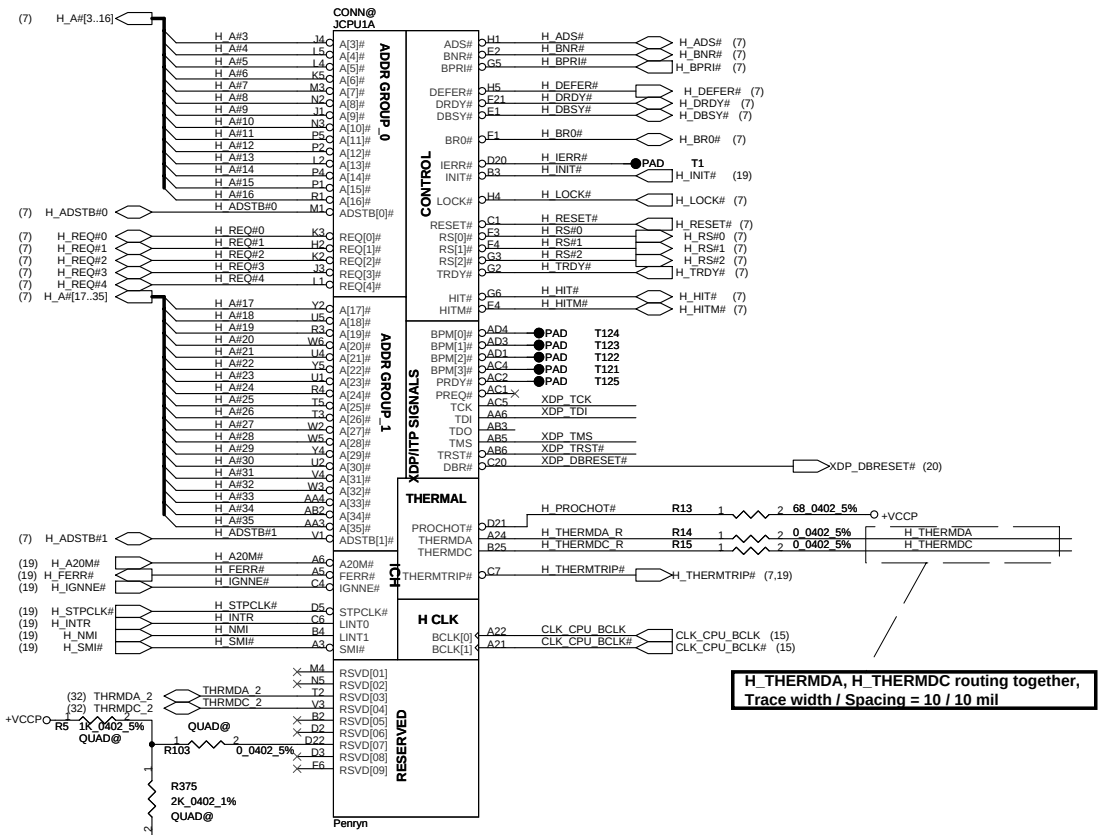
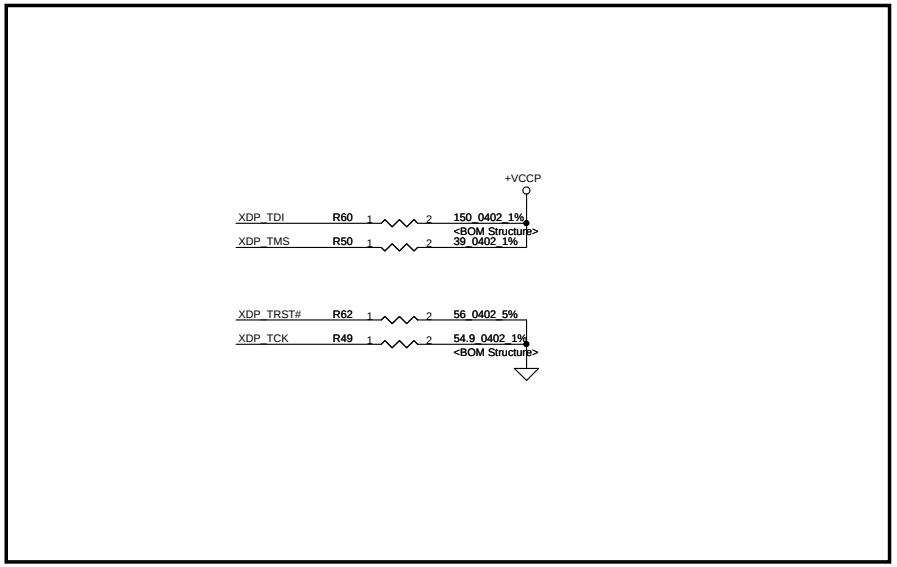
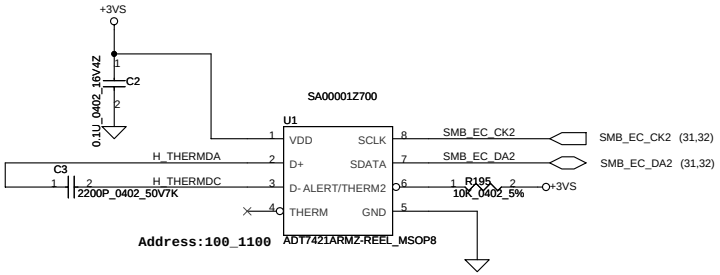
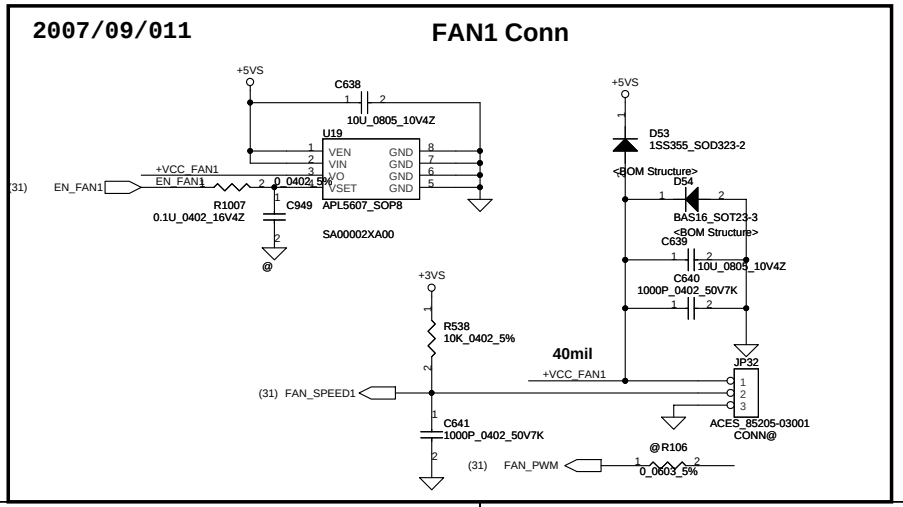


H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil







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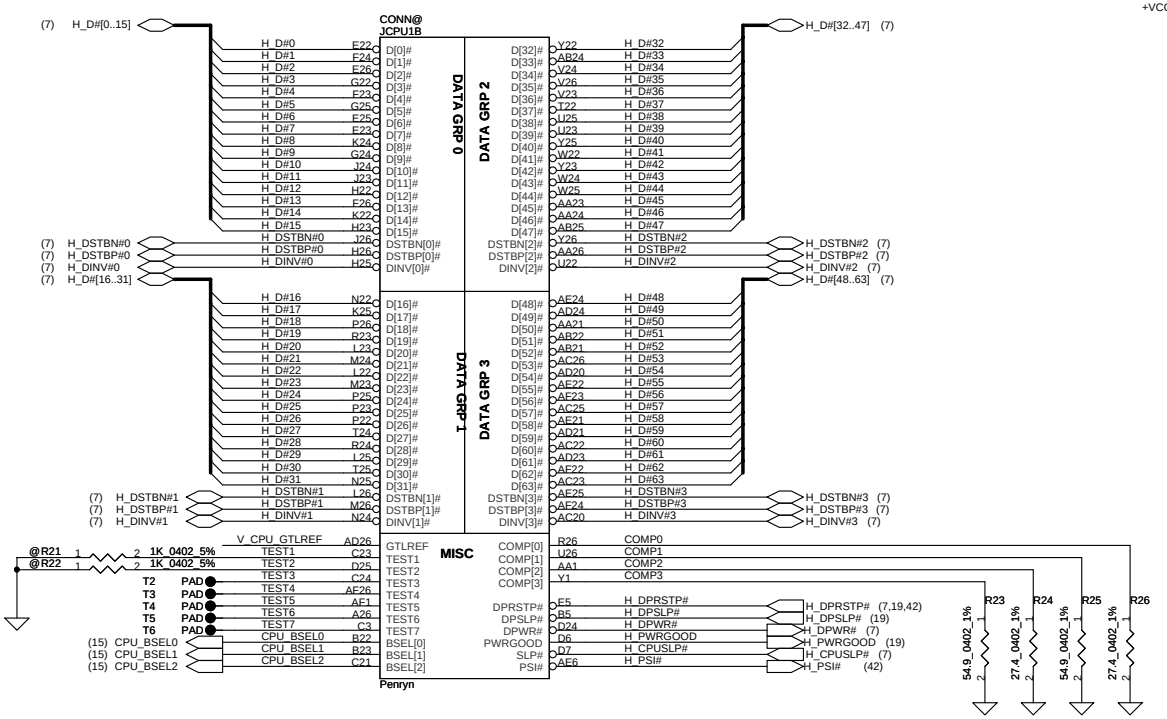
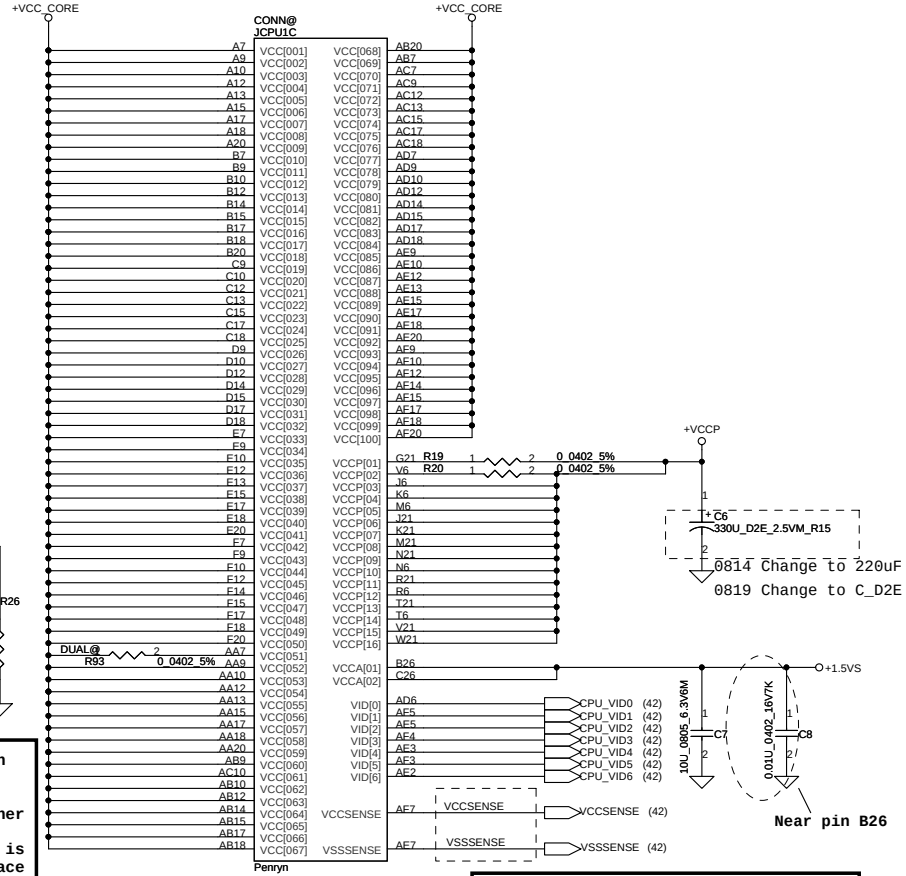


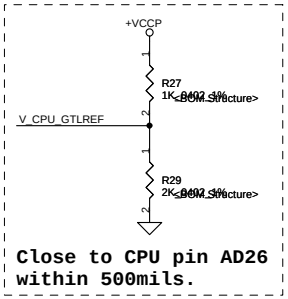


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

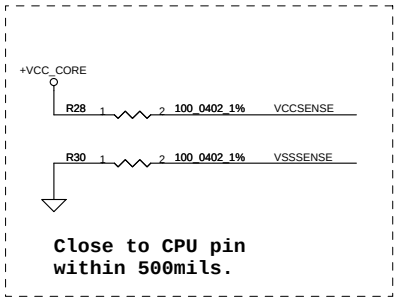
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AD26 within 500mils.



Close to CPU pin within 500mils.

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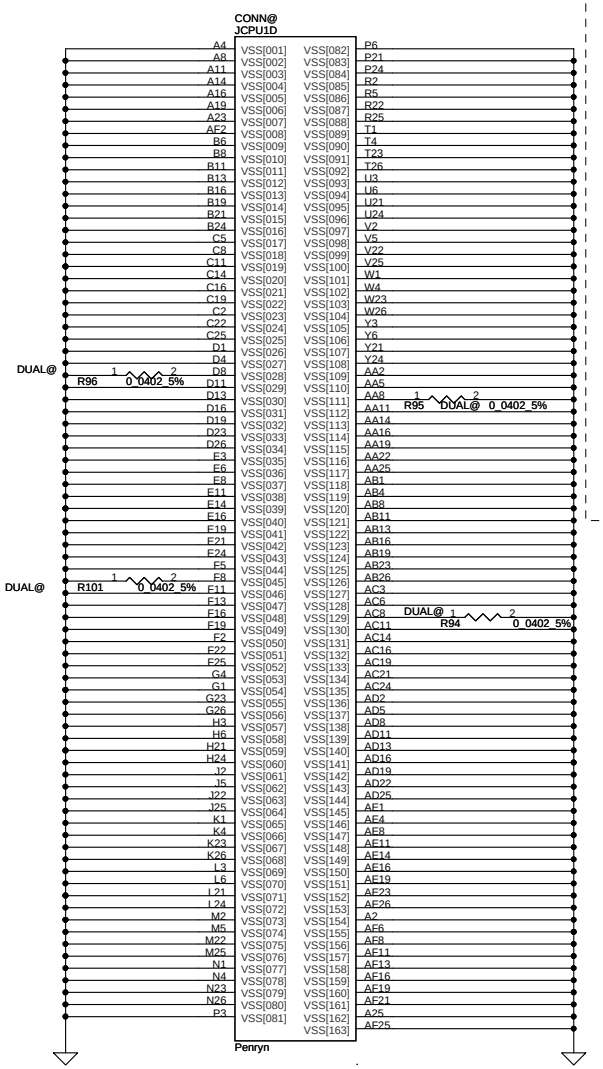
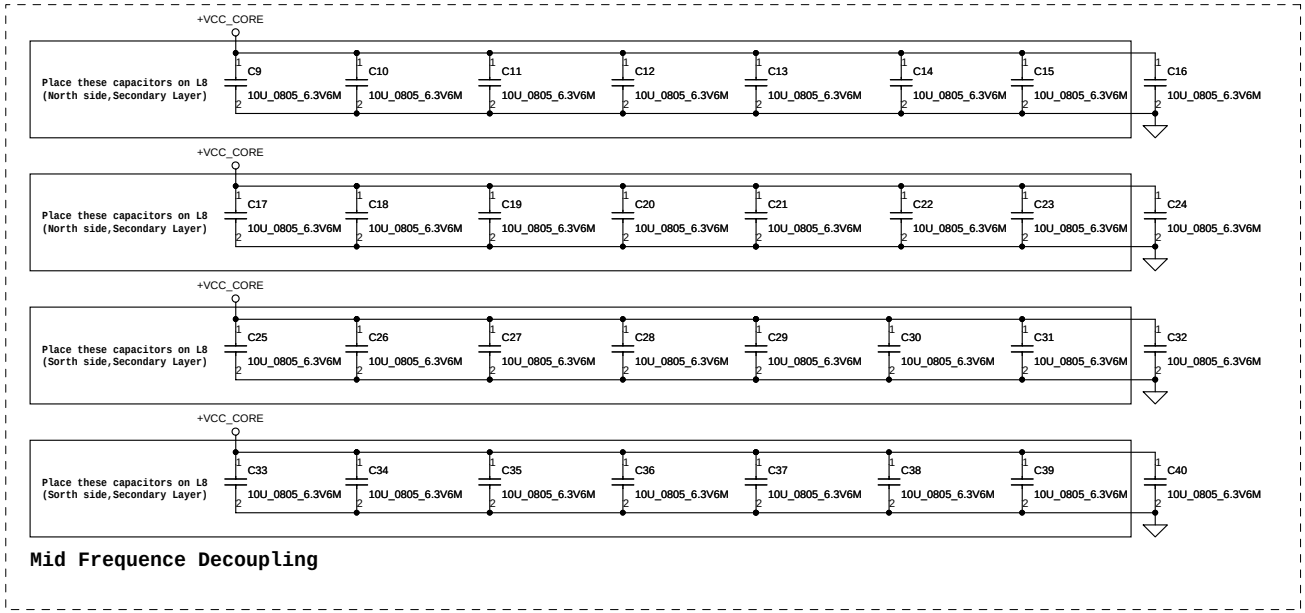
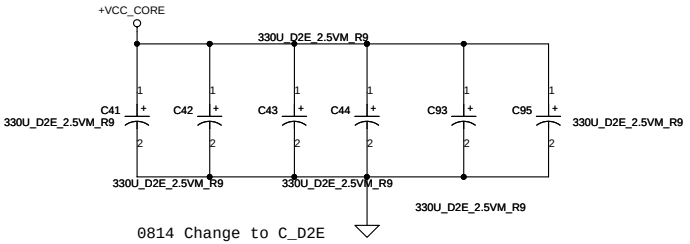


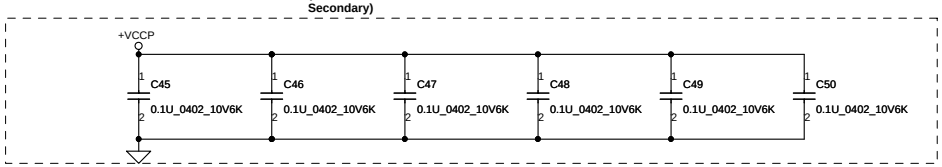


Mid Frequence Decoupling



0814 Change to C_D2E

Place these inside socket cavity on L8 (North side Secondary)



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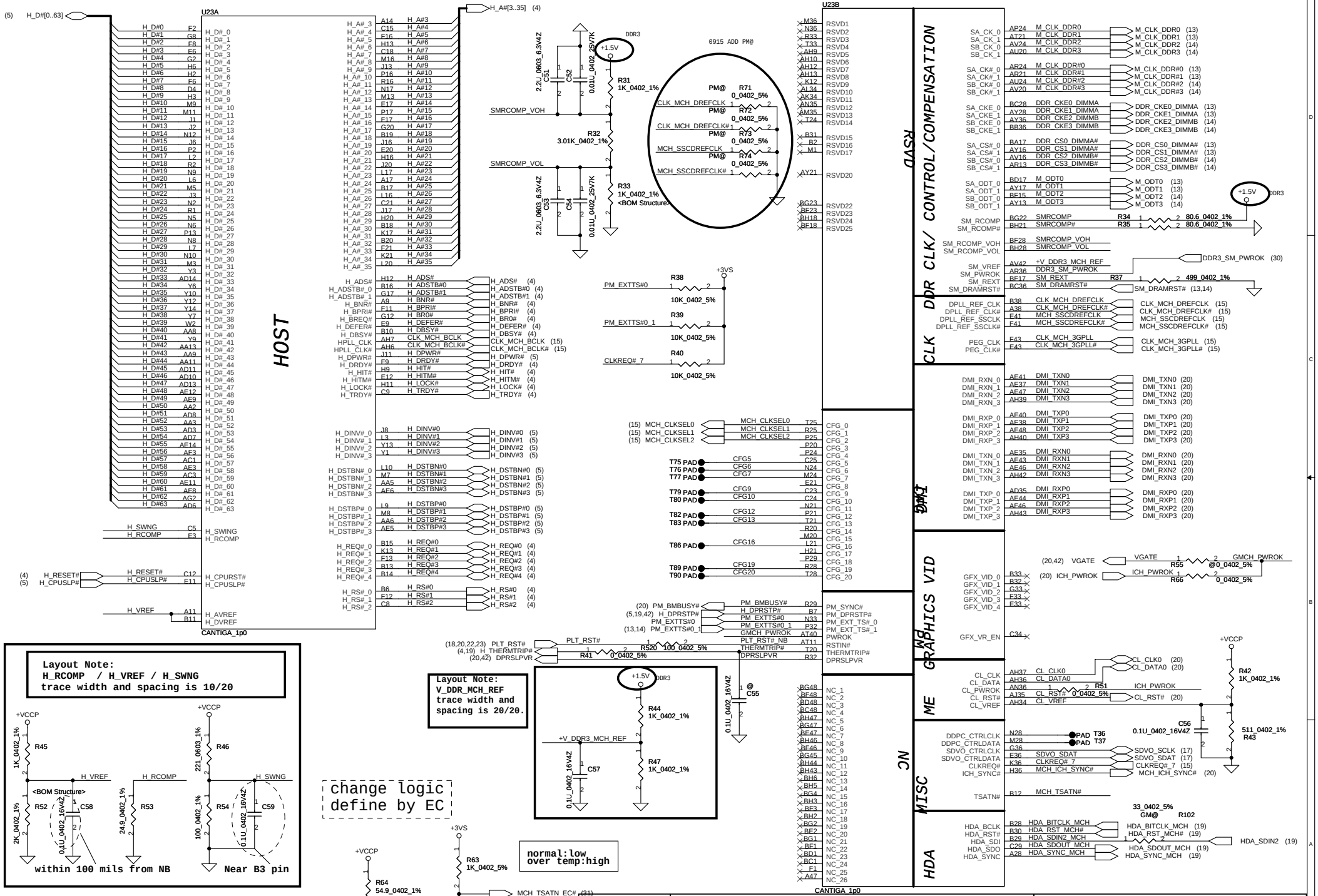

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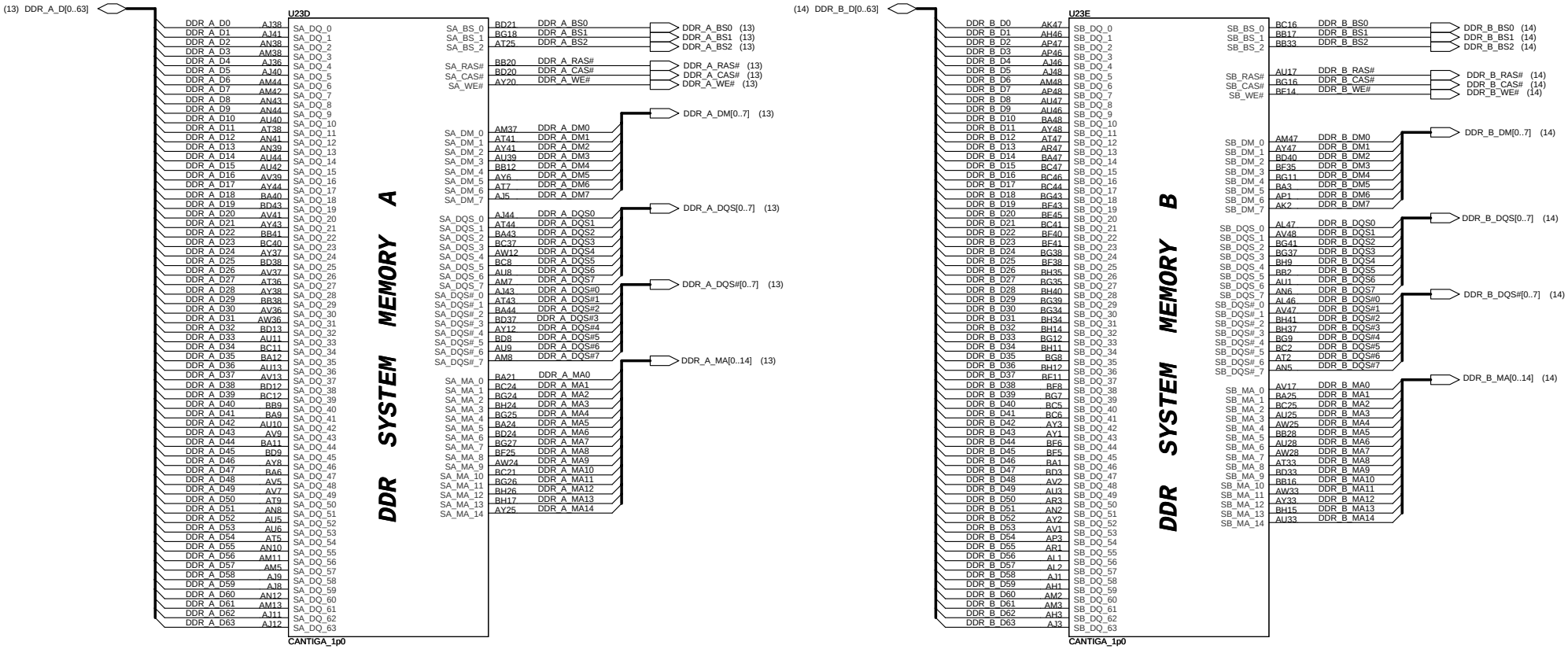

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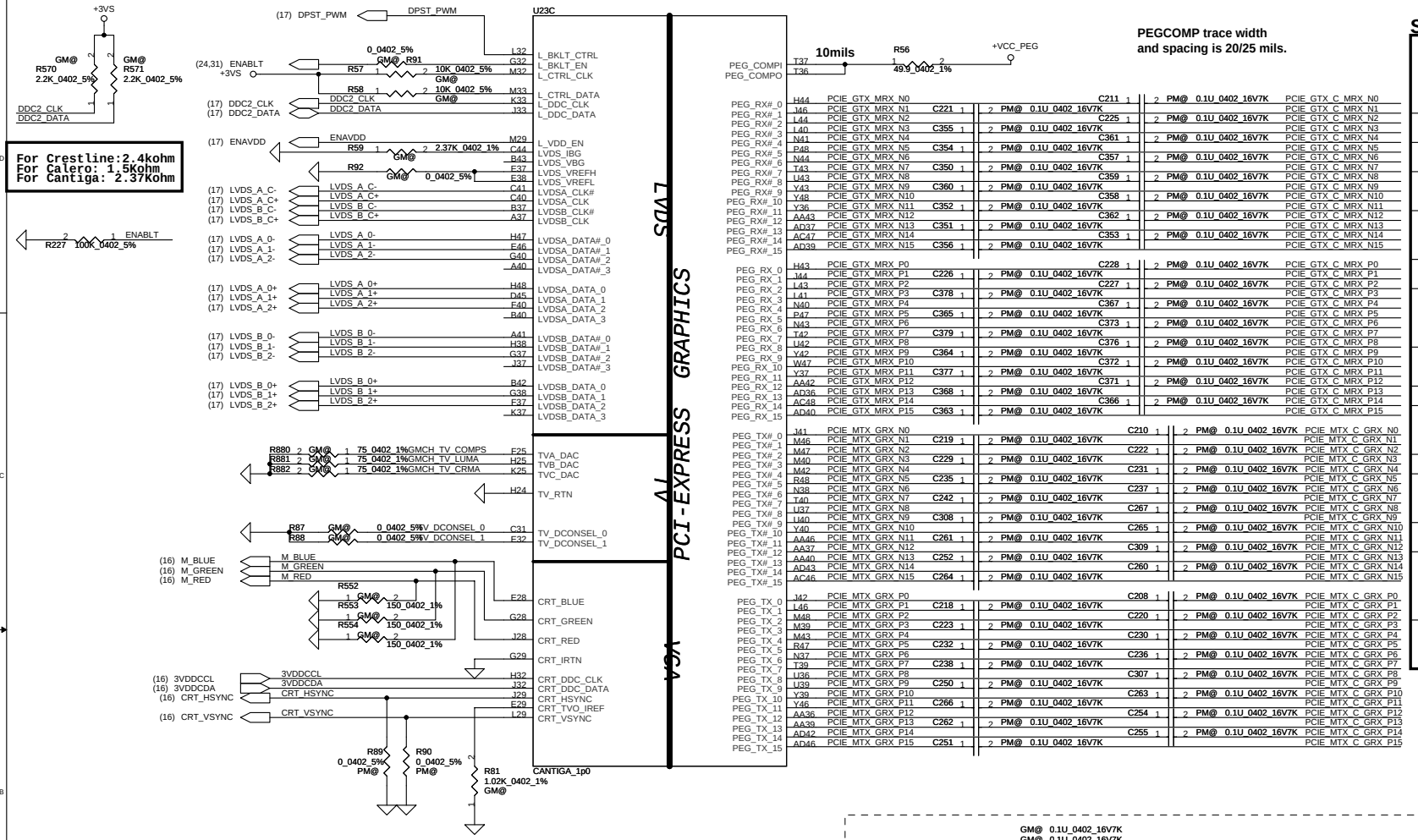

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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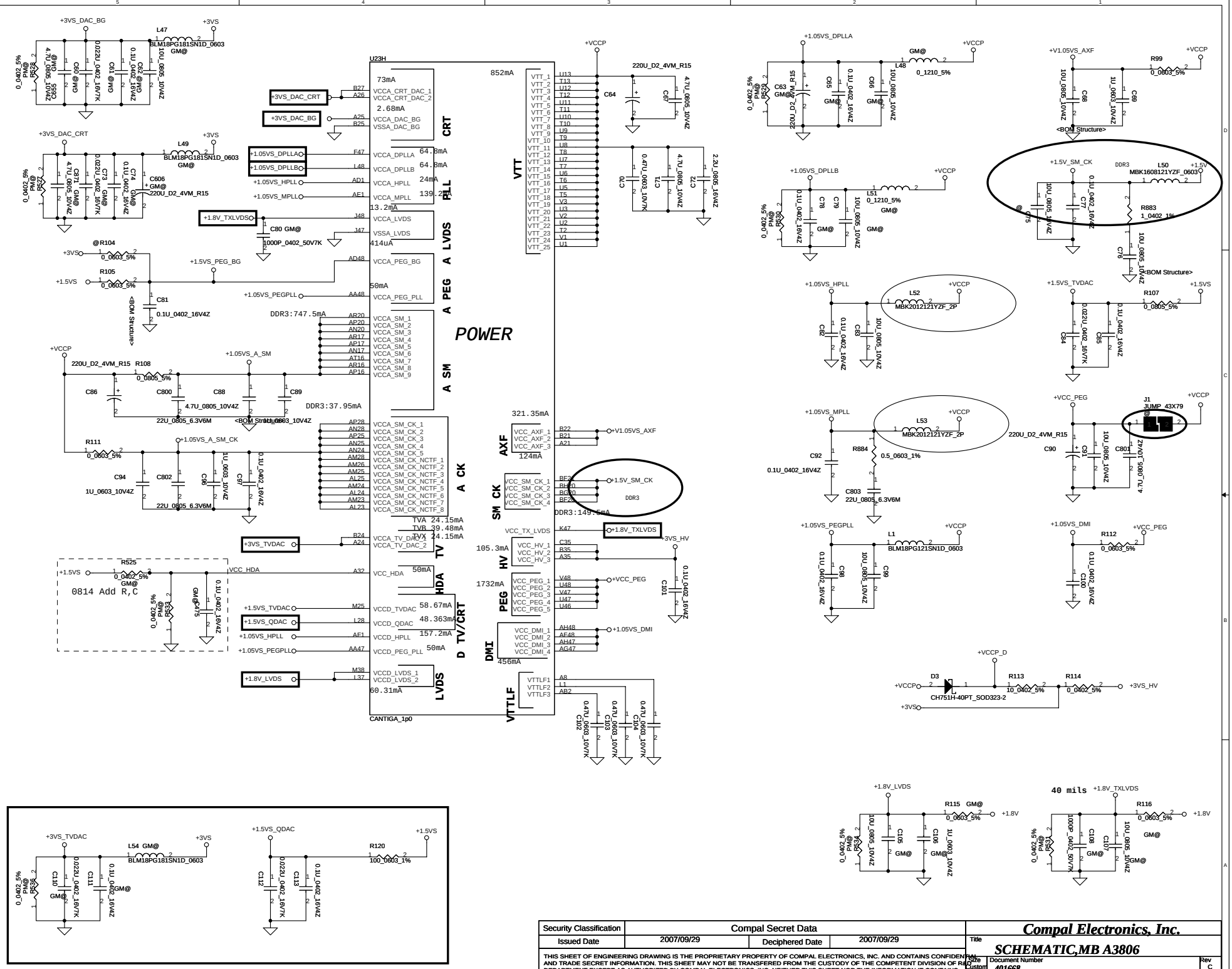

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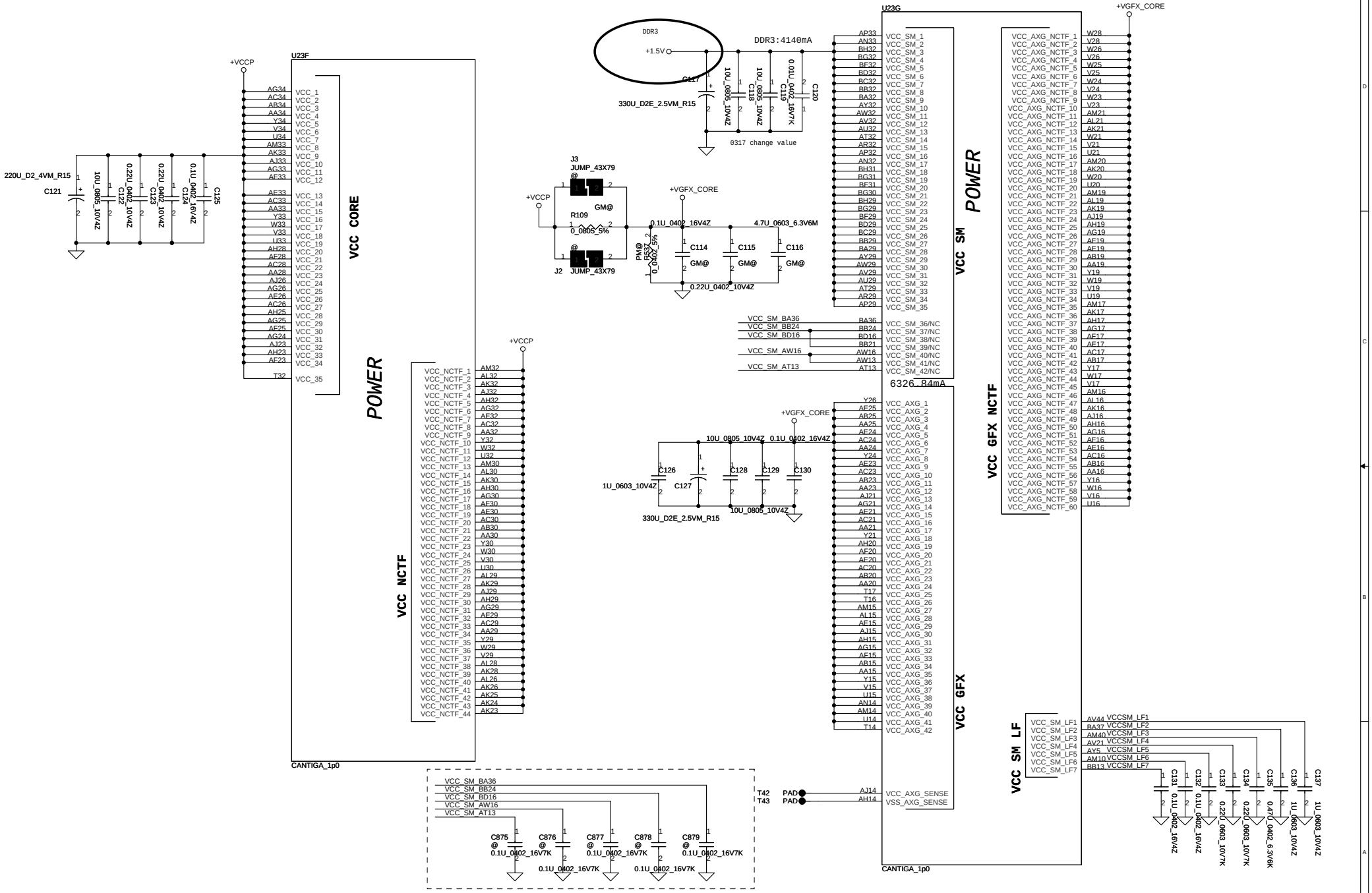

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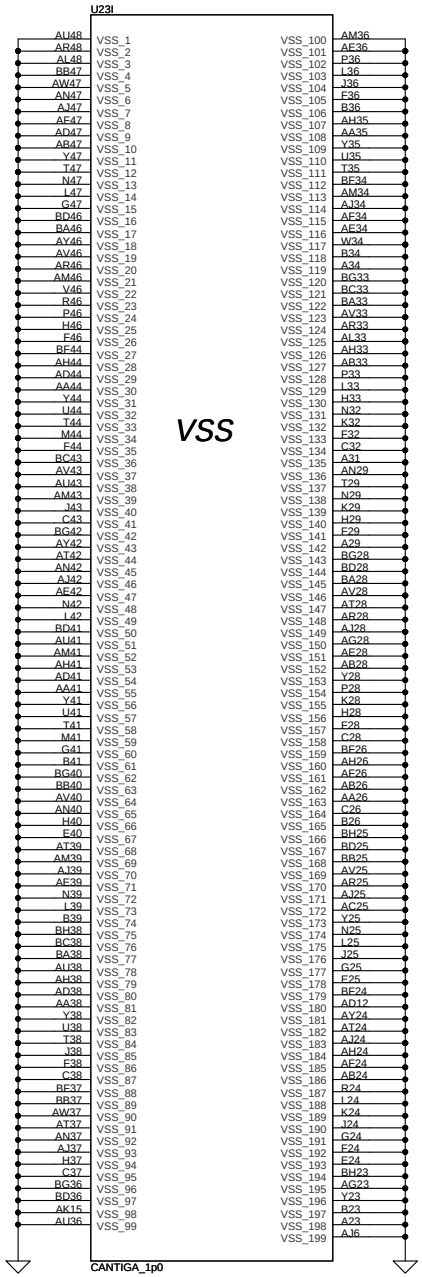

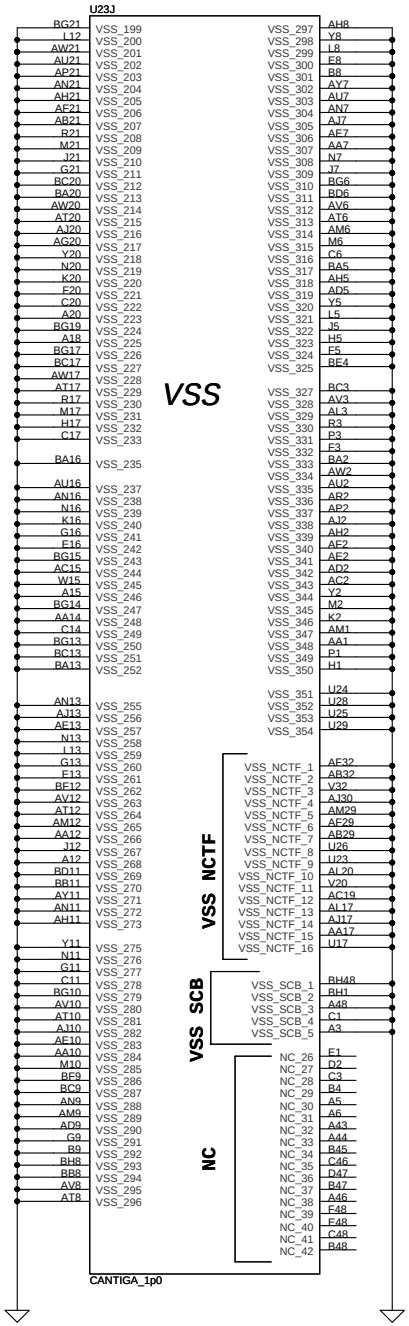

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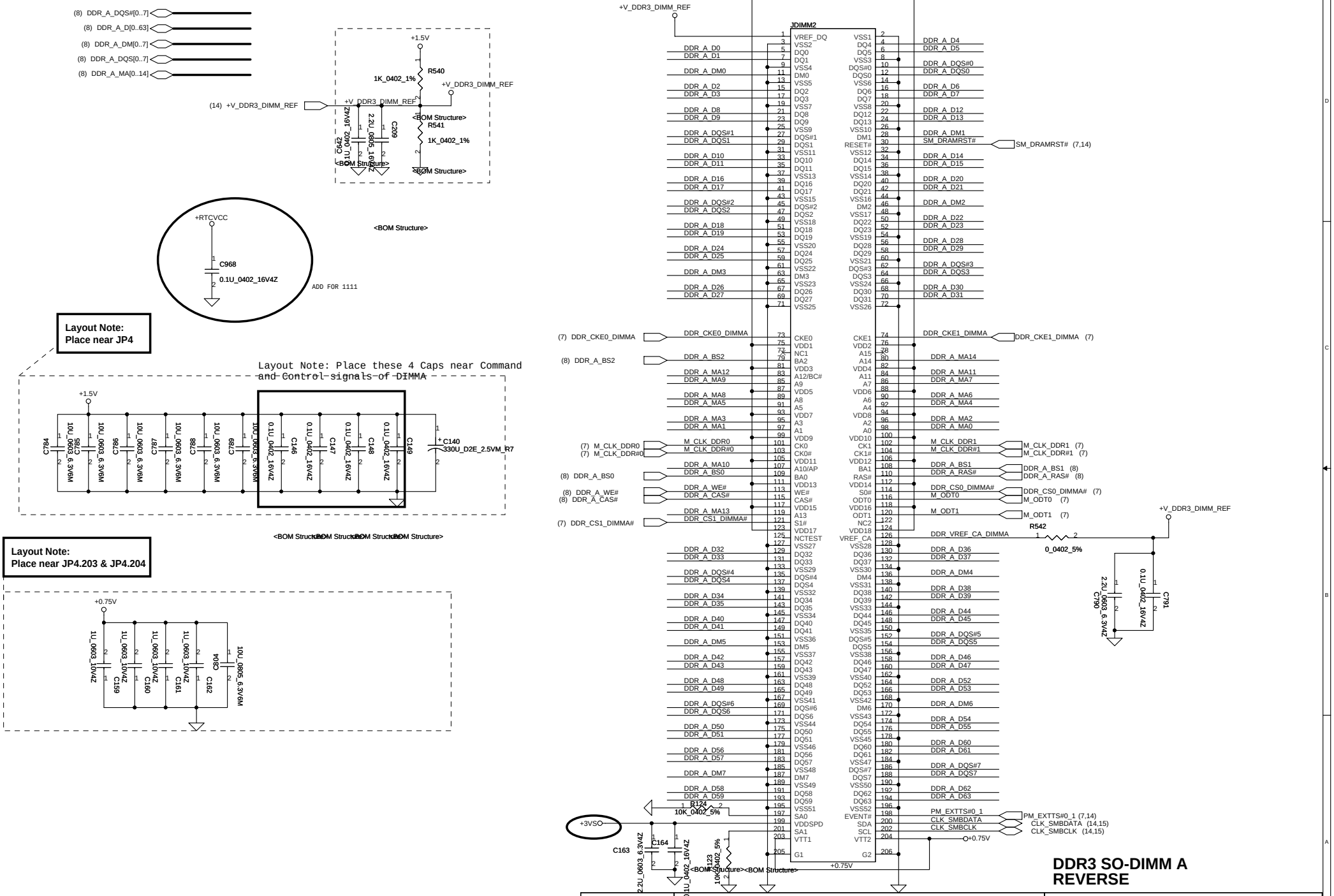

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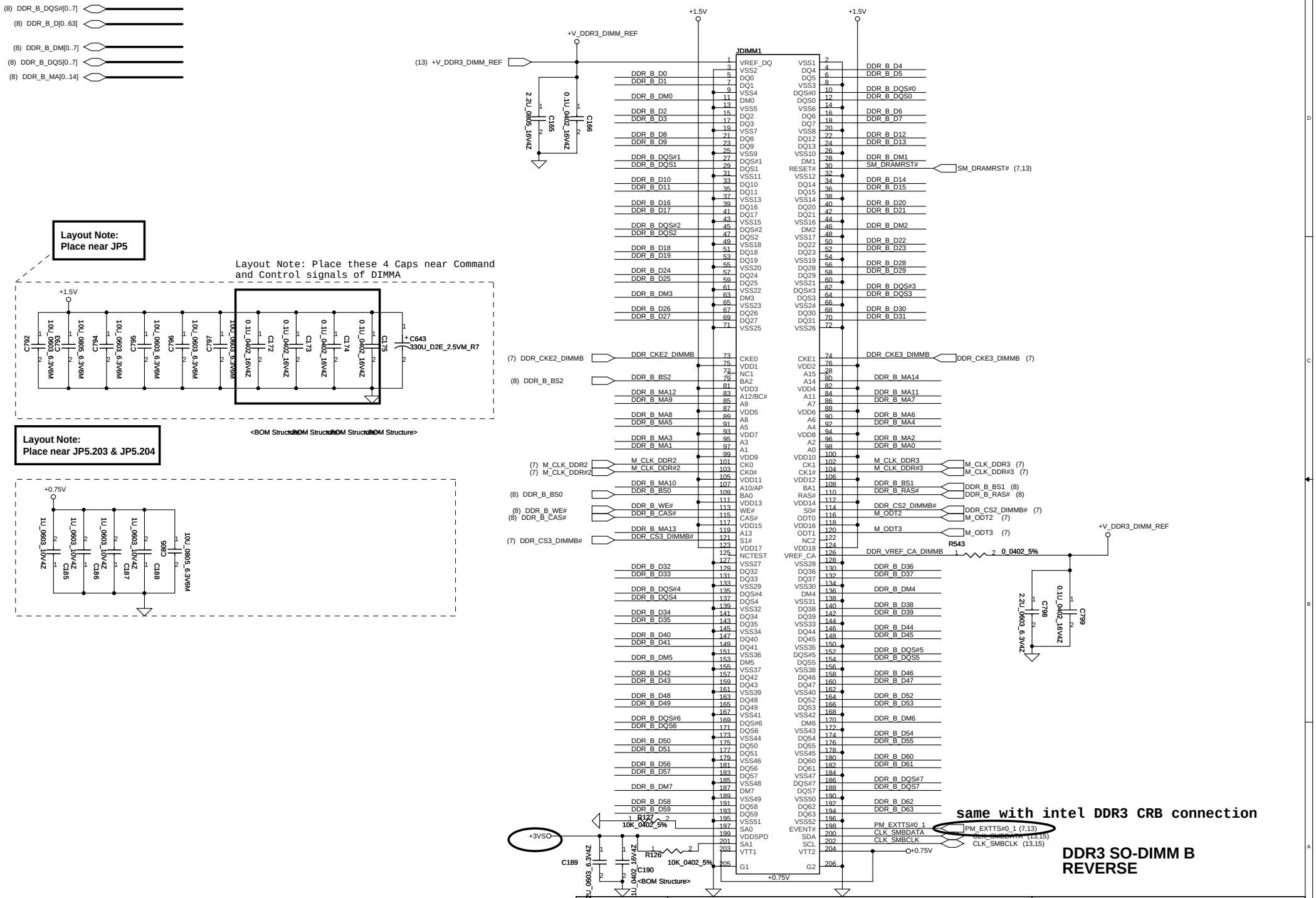

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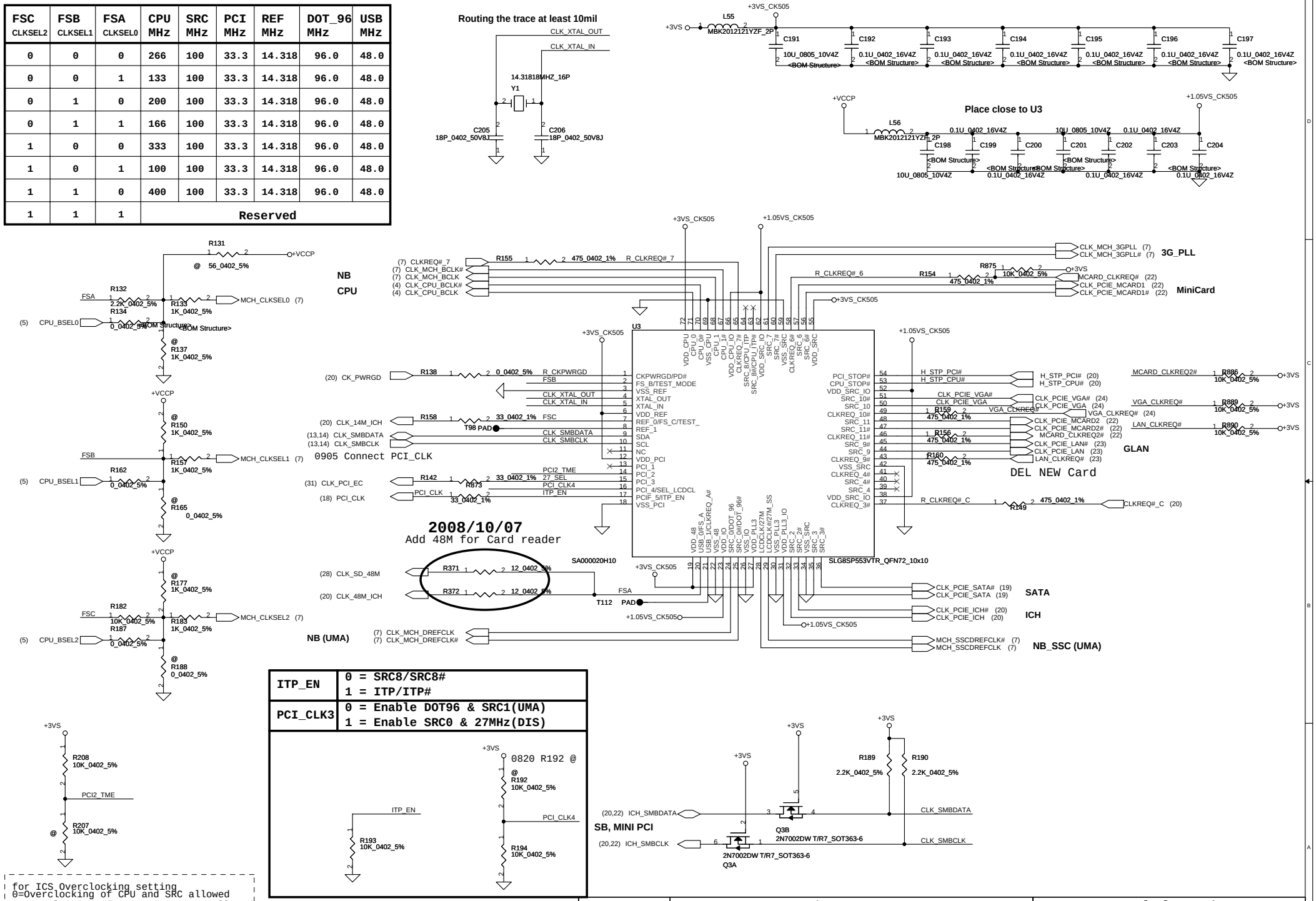
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

for ICS Overclocking setting
0=Overclocking of CPU and SRC allowed
1=Overclocking of CPU and SRC NOT allowed

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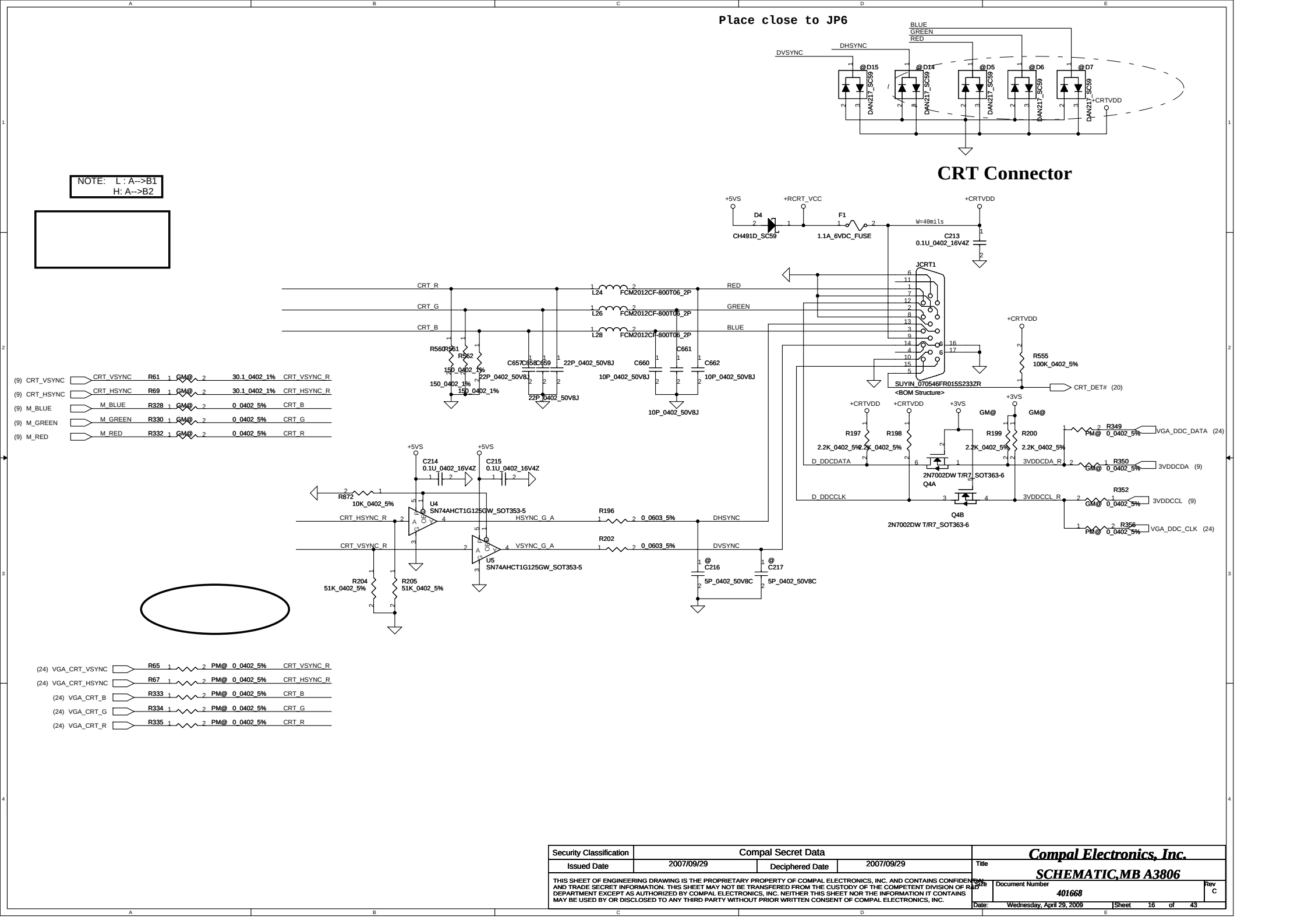

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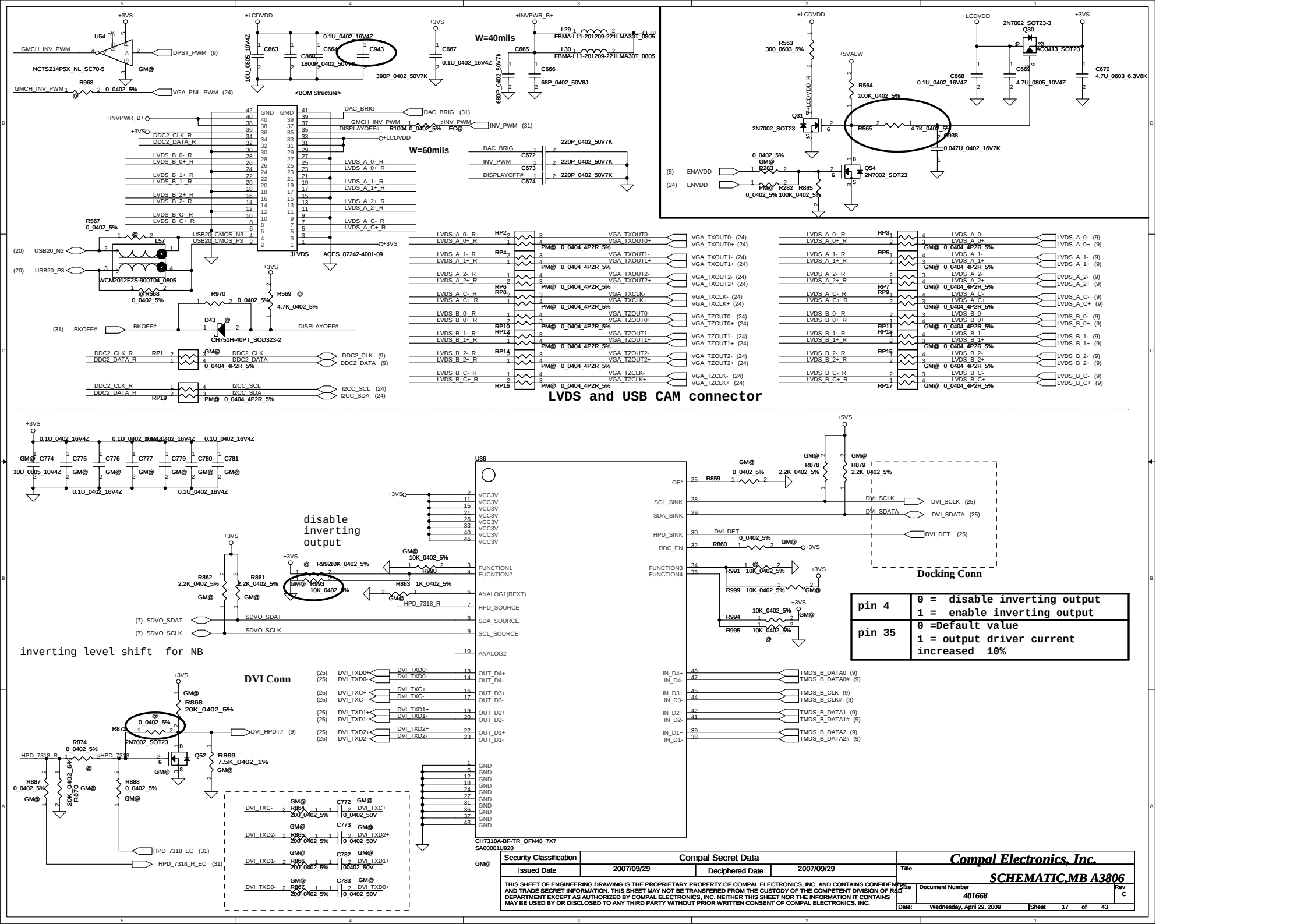
LVDS and USB CAM connector
DVI Conn
Docking Conn
U36
CH7318A-BF-TR_QFN48_7X7
SA00001U920
W=40mils
W=60mils
<BOM Structure>
JLVDS
ACES_87242-4001-09
inverting level shift for NB
disable inverting output
pin 4
0 = disable inverting output
1 = enable inverting output
pin 35
0 =Default value
1 = output driver current increased 10%
Security Classification
Compal Secret Data
Issued Date
2007/09/29
Deciphered Date
2007/09/29
Compal Electronics, Inc.
Title
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Date: Wednesday, April 29, 2009
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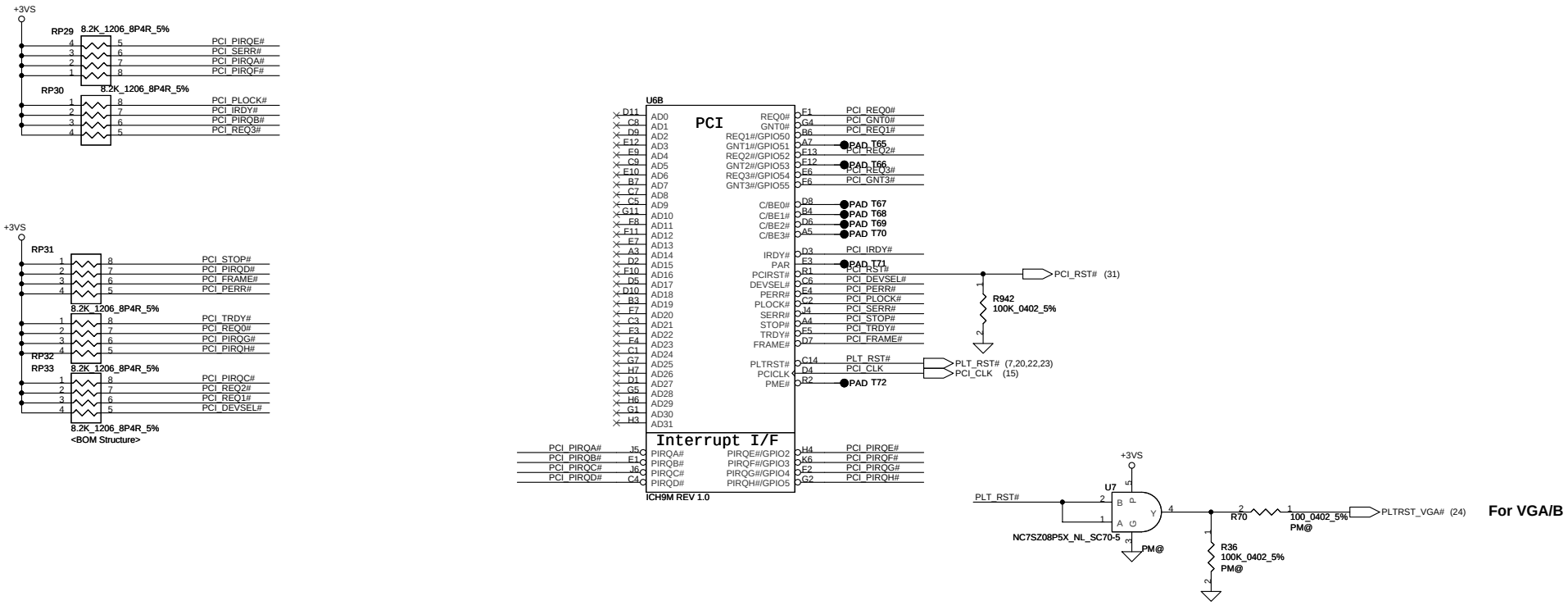
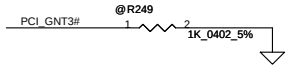
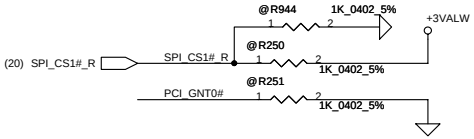


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



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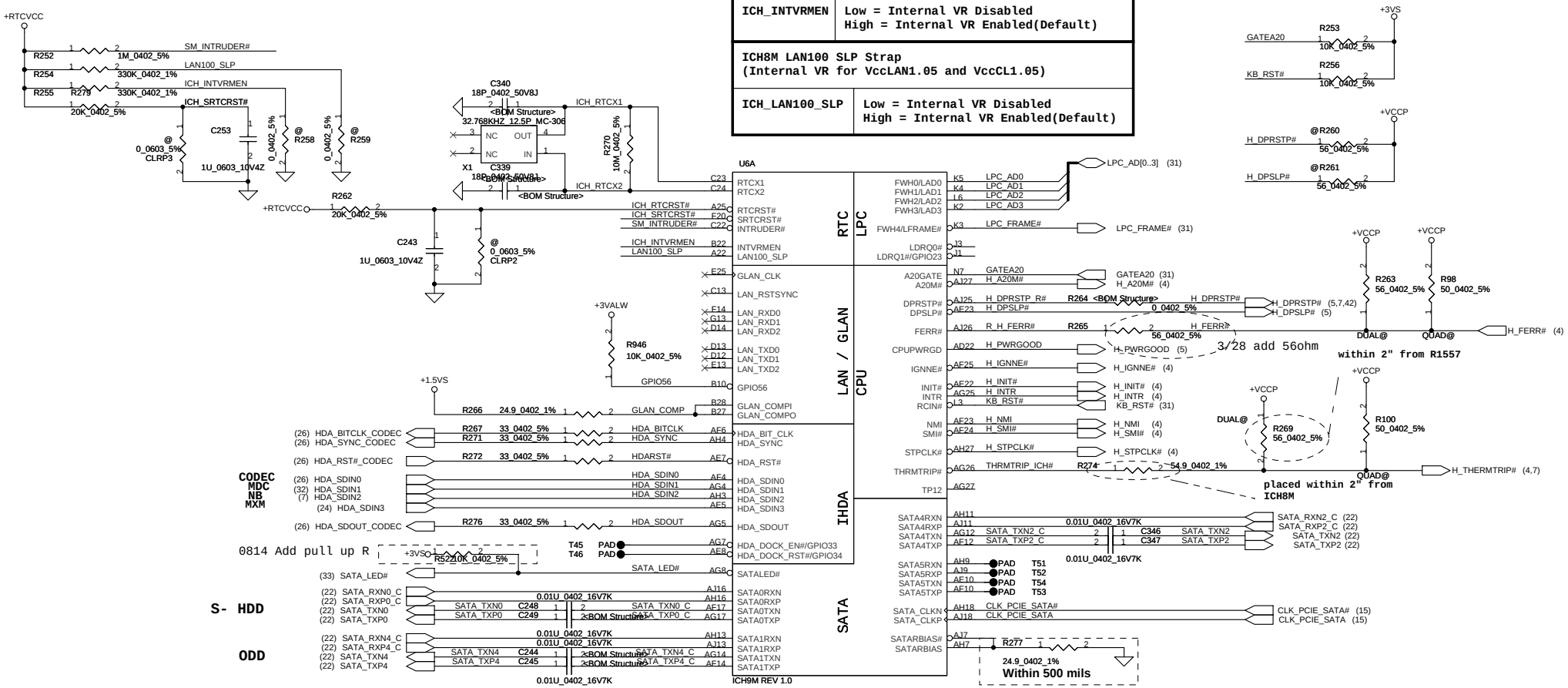
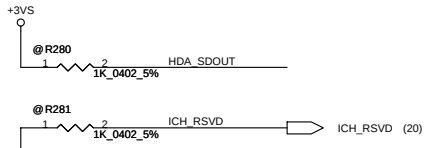
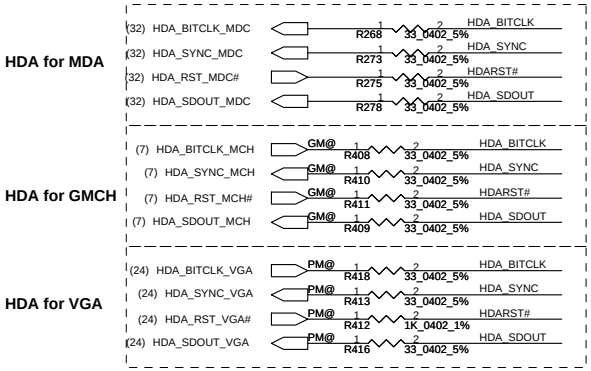
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



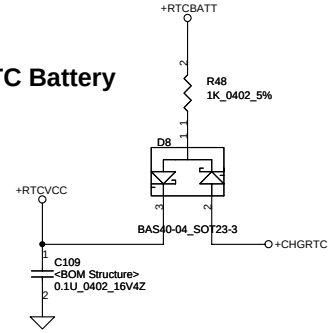


XOR CHAIN ENTRANCE STRAP:RSVD

ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	



RTC Battery



Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

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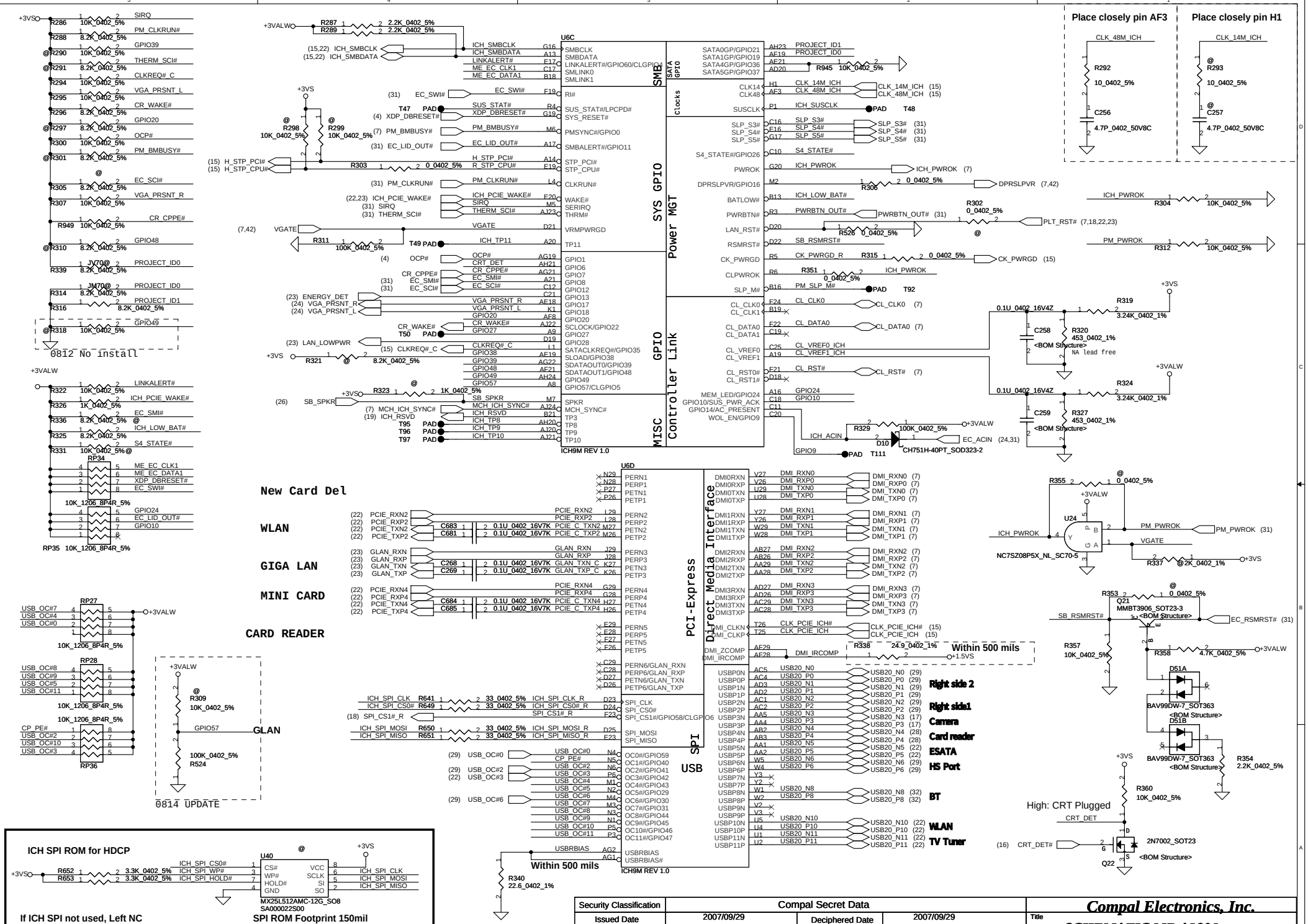
Place closely pin AF3
Place closely pin H1
U6C
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M REV 1.0
0812 No install
New Card Del
WLAN
GIGA LAN
MINI CARD
CARD READER
U6D
PCI-Express
Direct Media Interface
SPI
USB
Right side 2
Right side1
Camera
Card reader
ESATA
HS Port
BT
WLAN
TV Tuner
0814 UPDATE
GLAN
ICH SPI ROM for HDCP
If ICH SPI not used, Left NC
SPI ROM Footprint 150mil
Within 500 mils
High: CRT Plugged
Compal Electronics, Inc.
SCHEMATIC,MB A3806
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Deciphered Date
2007/09/29
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Date: Wednesday, April 29, 2009
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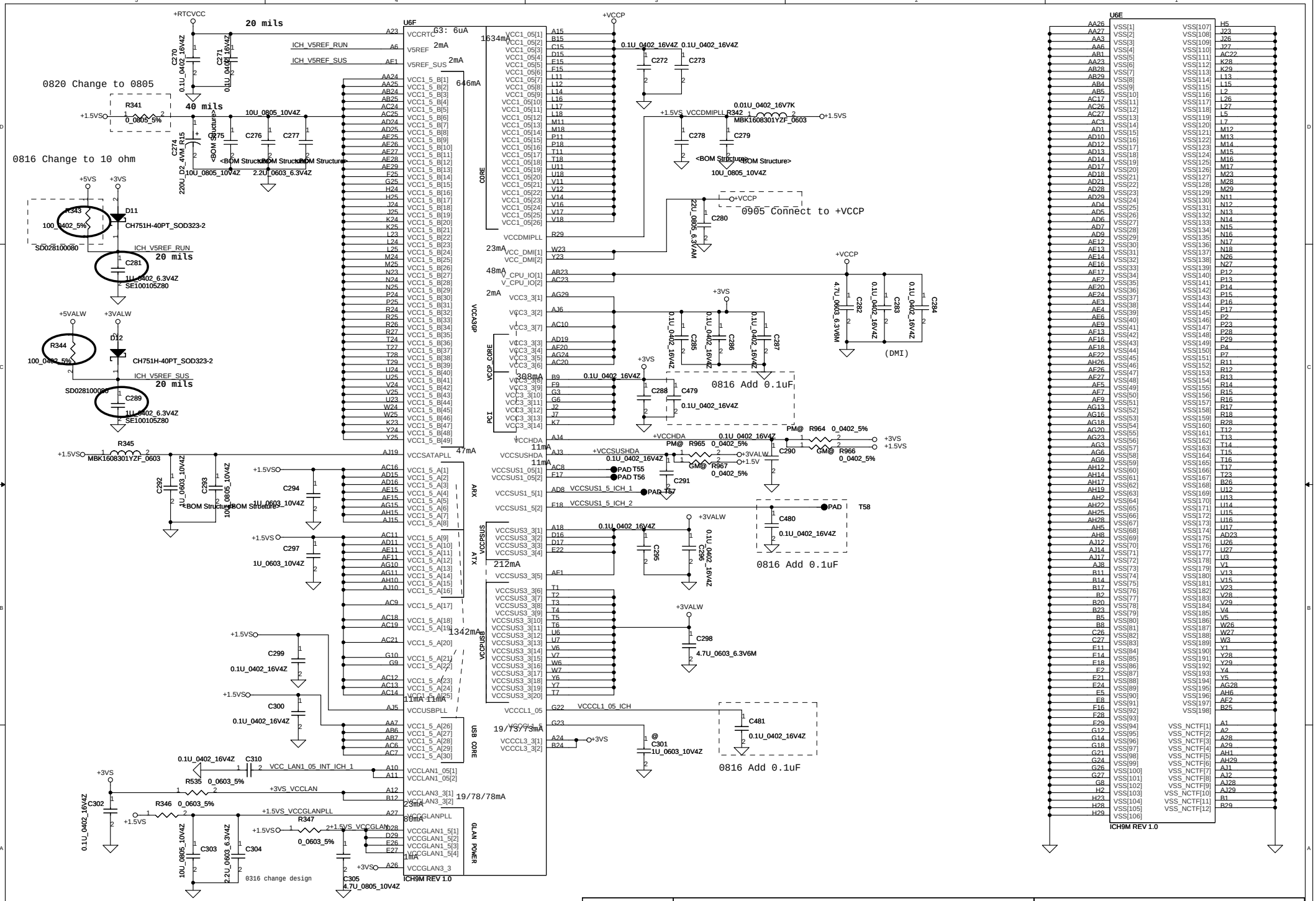

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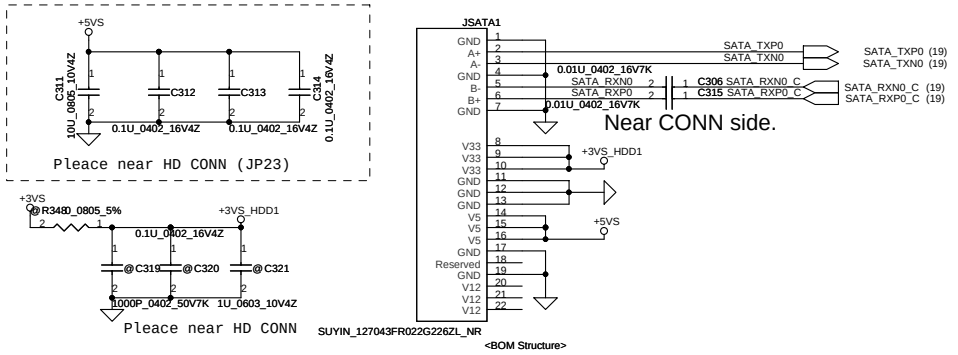
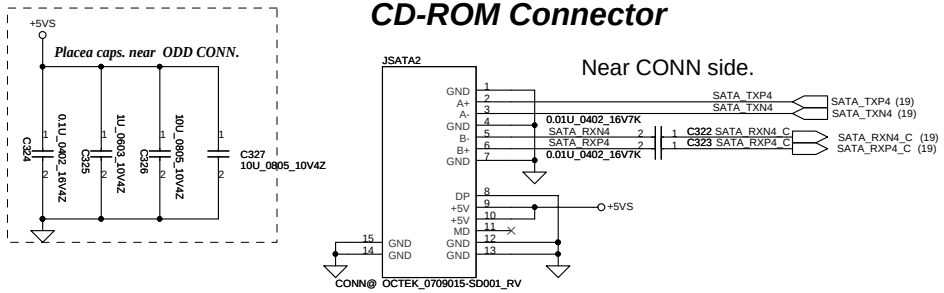
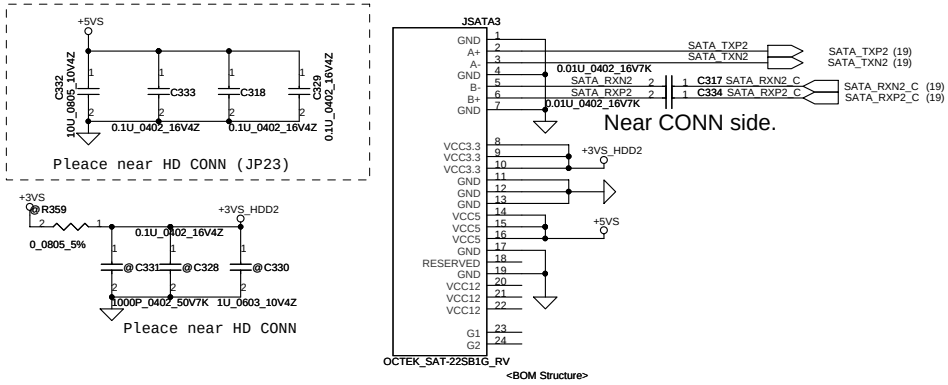
HDD Connector



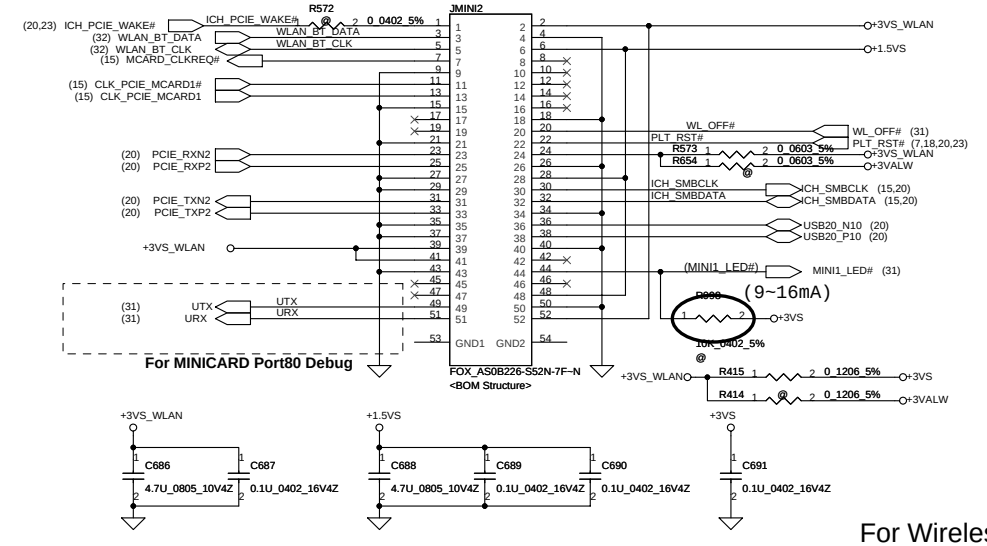
CD-ROM Connector



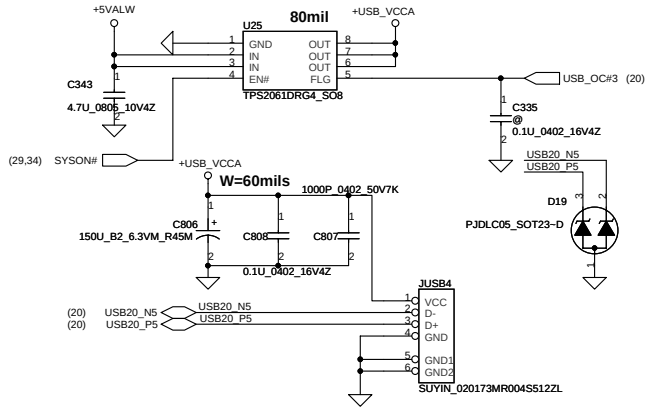
HDD Connector



For Wireless LAN

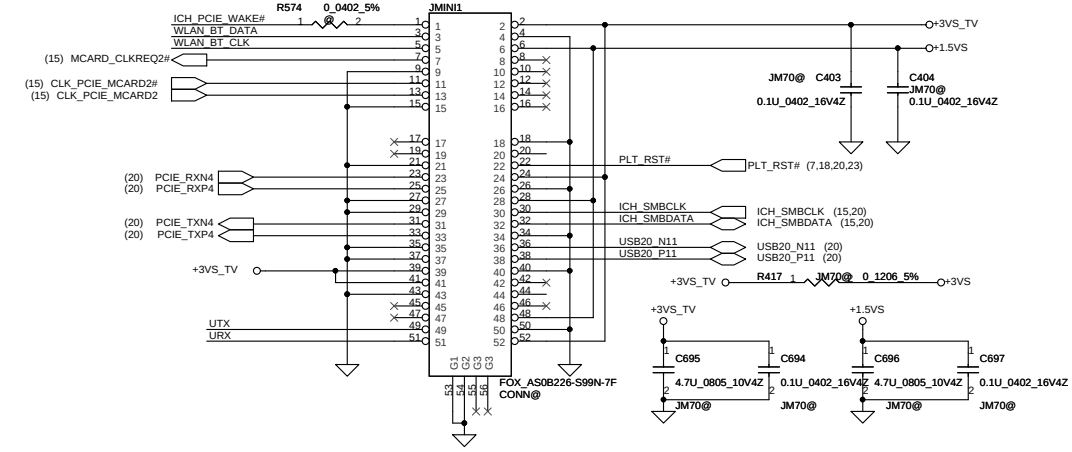


eSATA w/ USB port



PVT- Update ESATA connector footprint for latche hole size.

For TV Tuner



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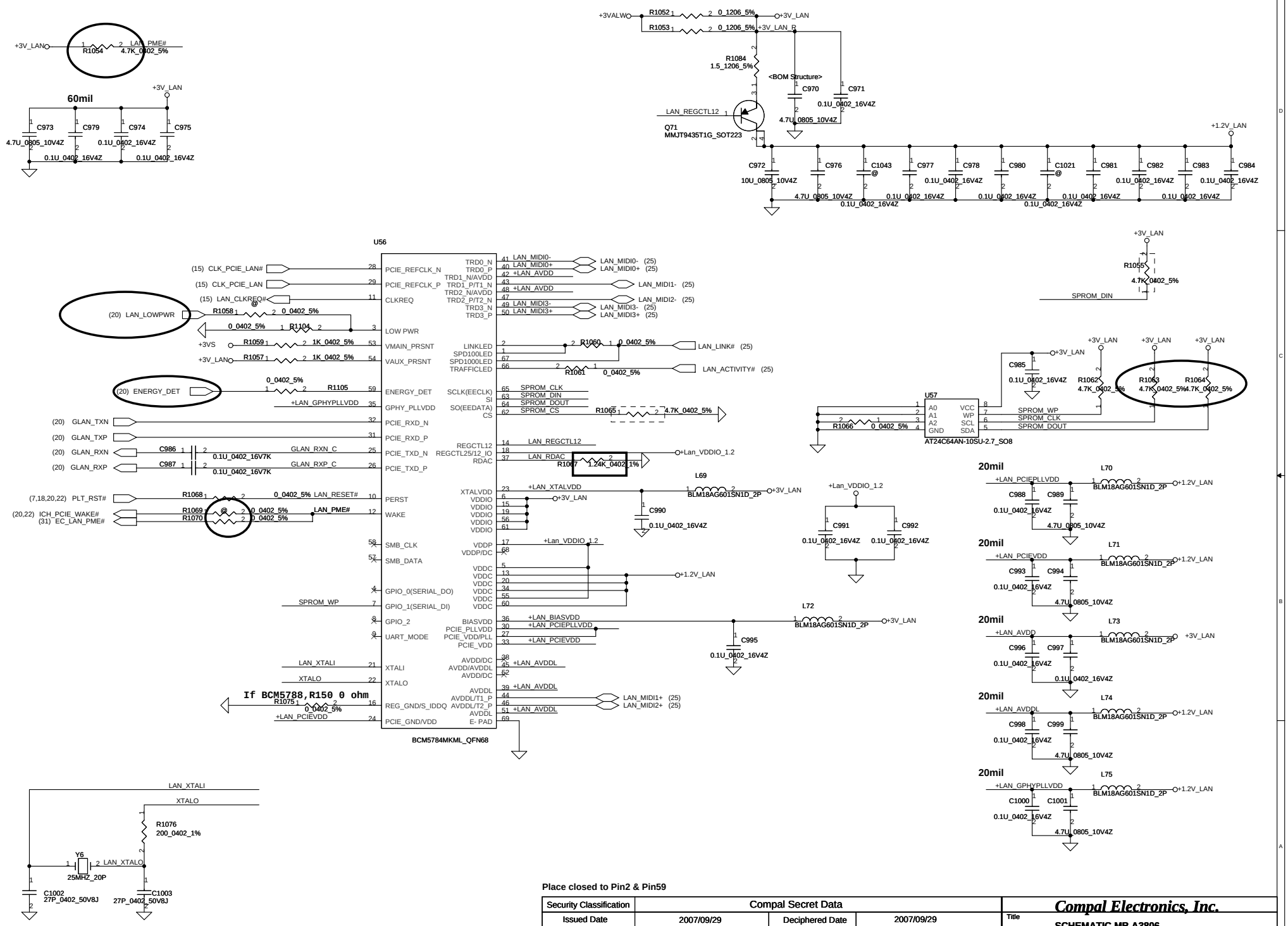

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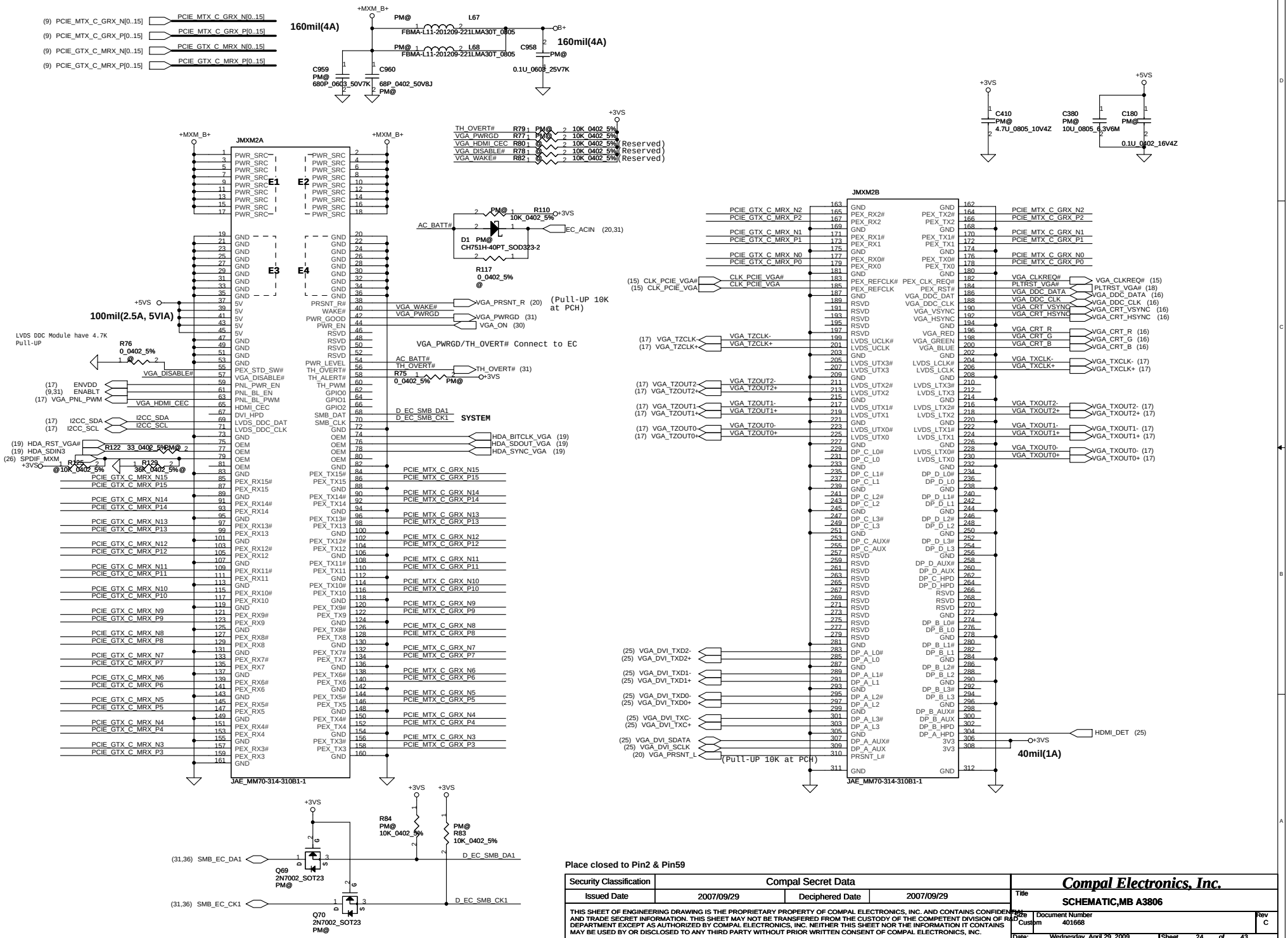

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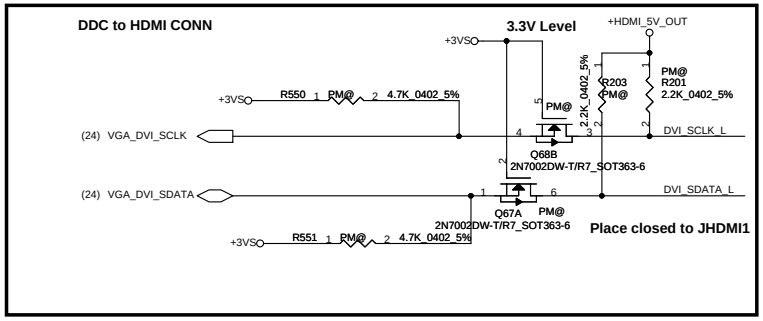
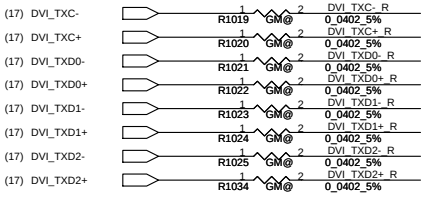
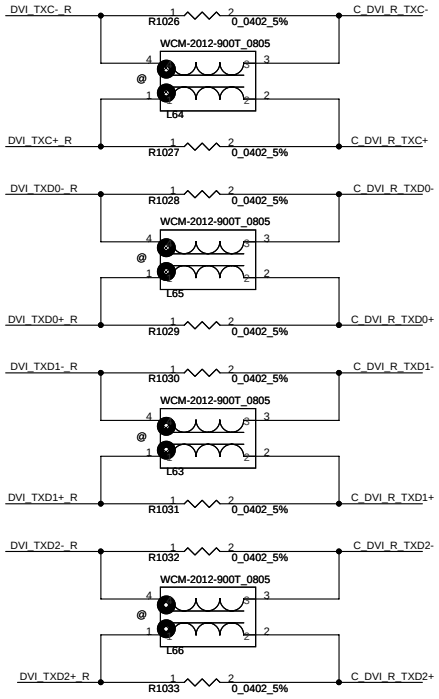
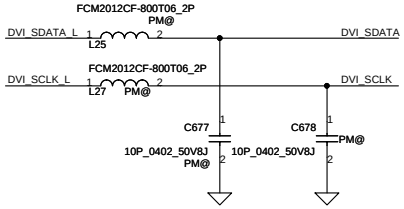
Need Check

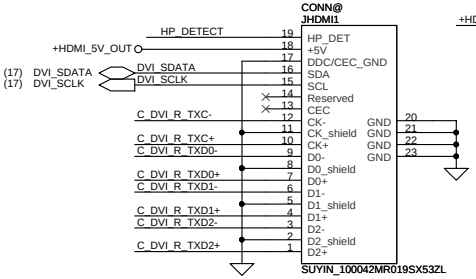


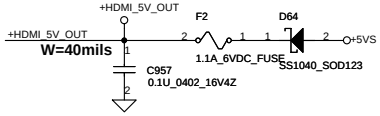


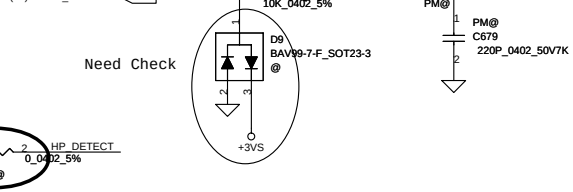


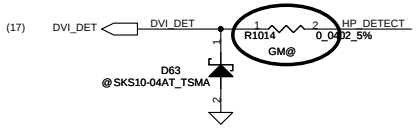


HDMI Connector









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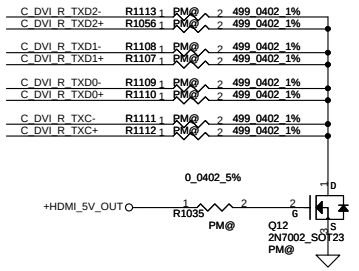

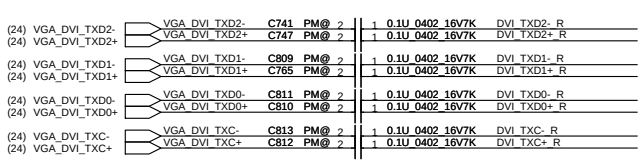

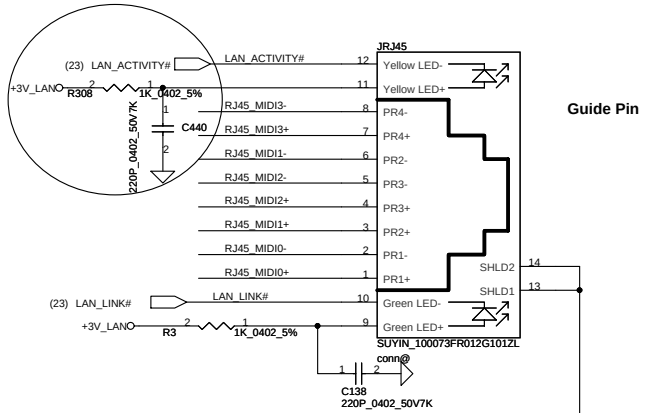

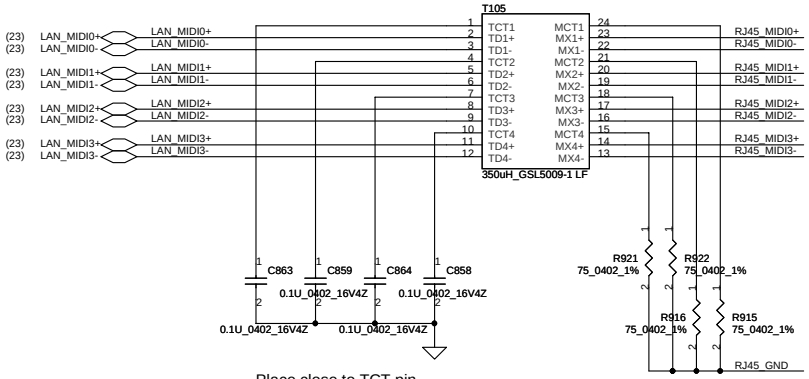

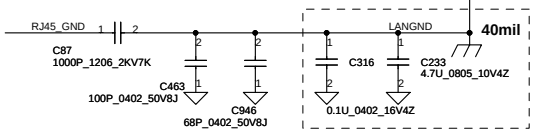

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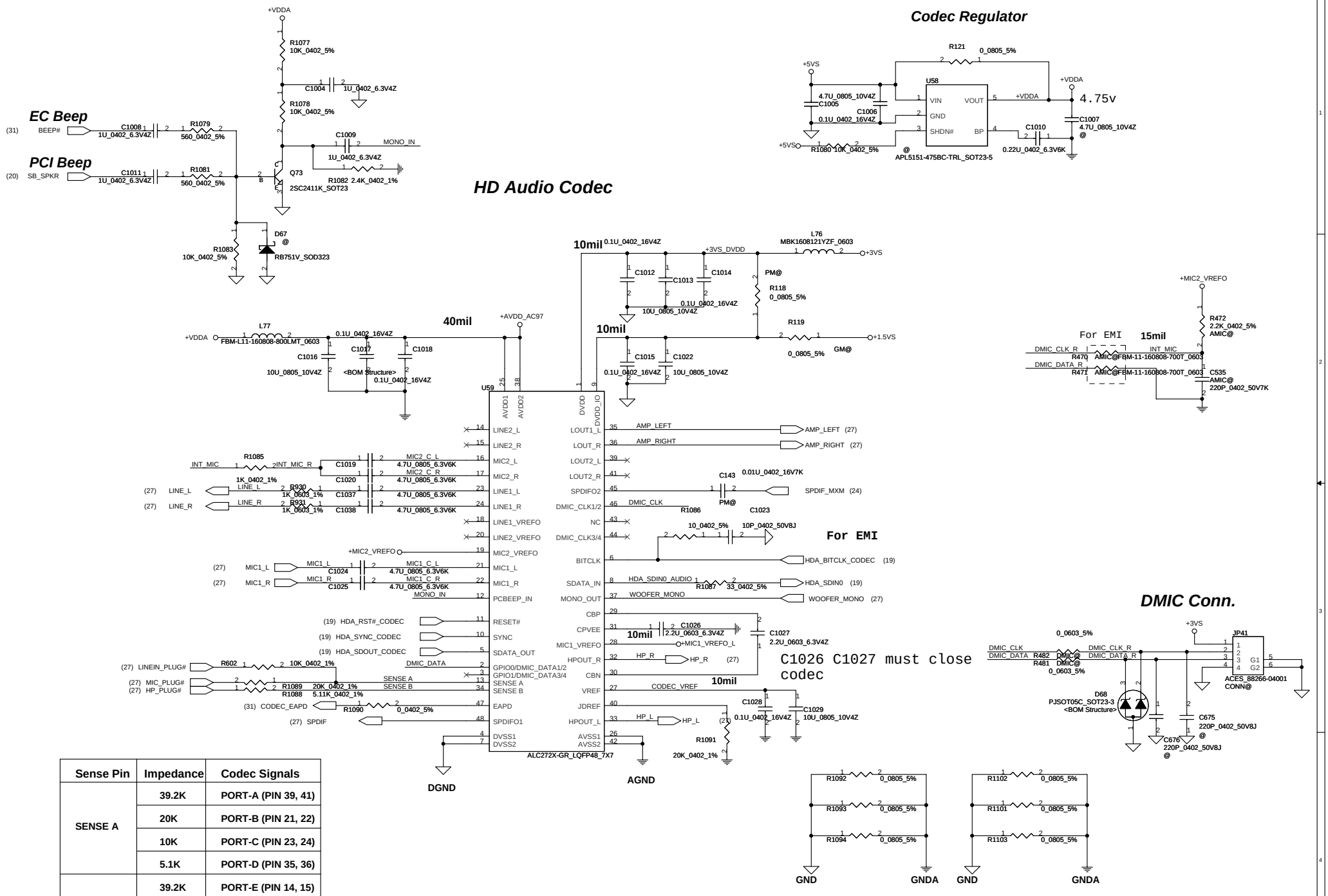

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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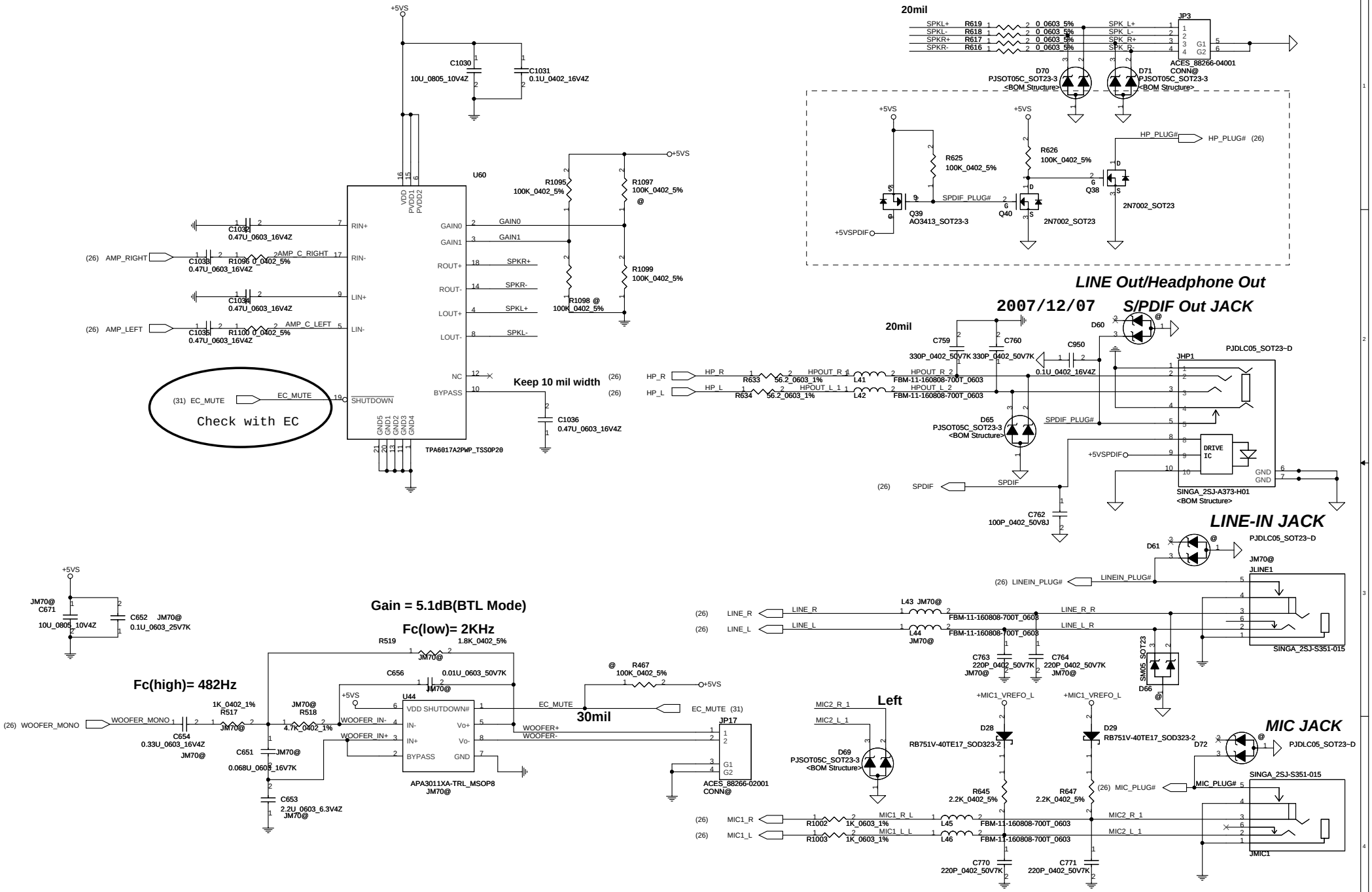
Int. Speaker Conn.



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Title: **SCHEMATIC,MB A3806**

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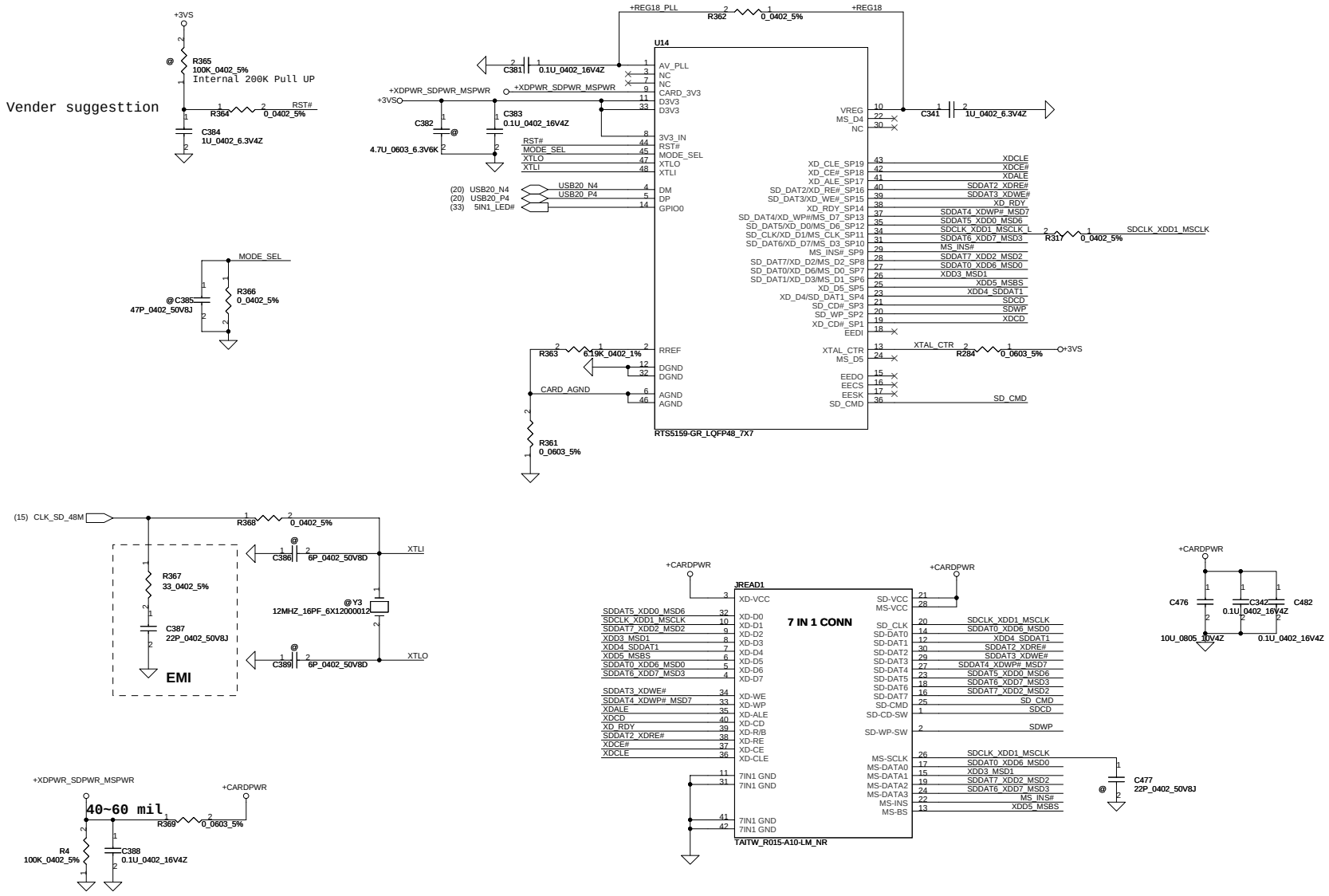

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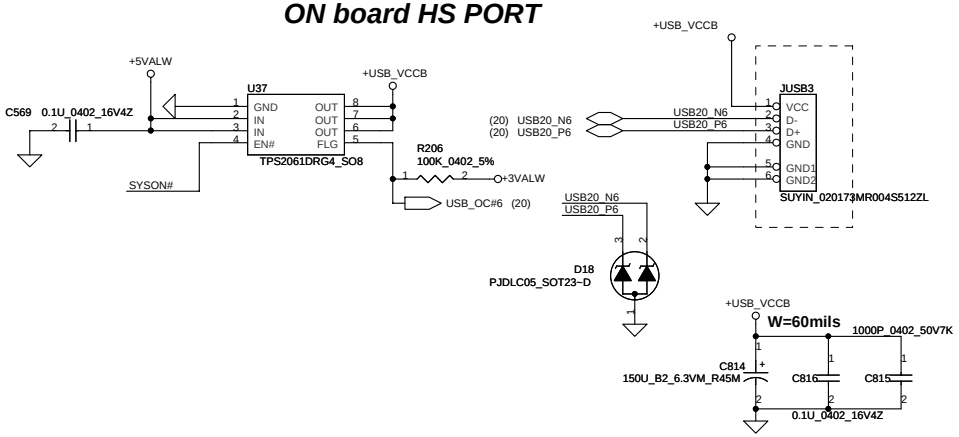
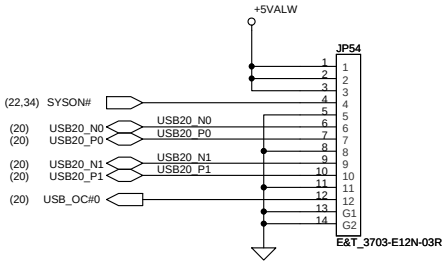
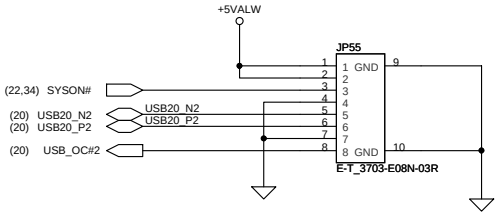
ON board HS PORT





2 PORT



1 PORT

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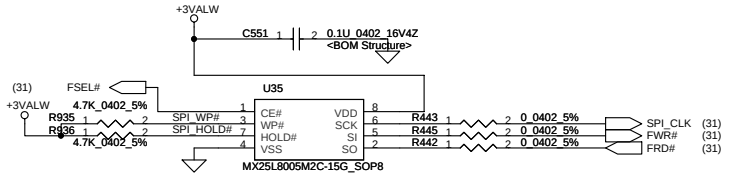
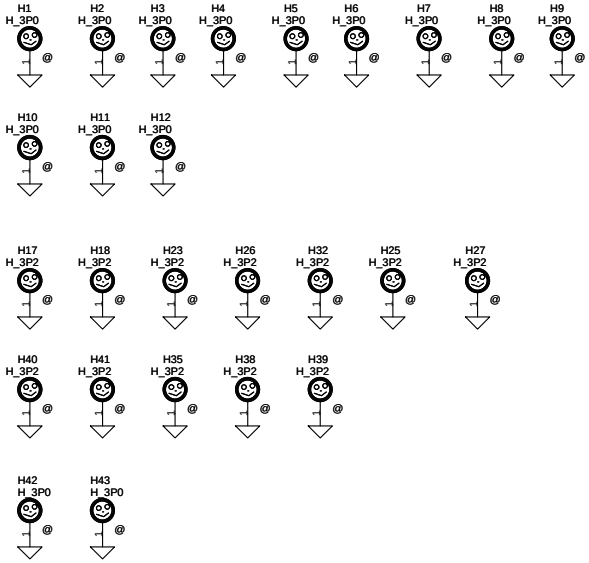
BIOS



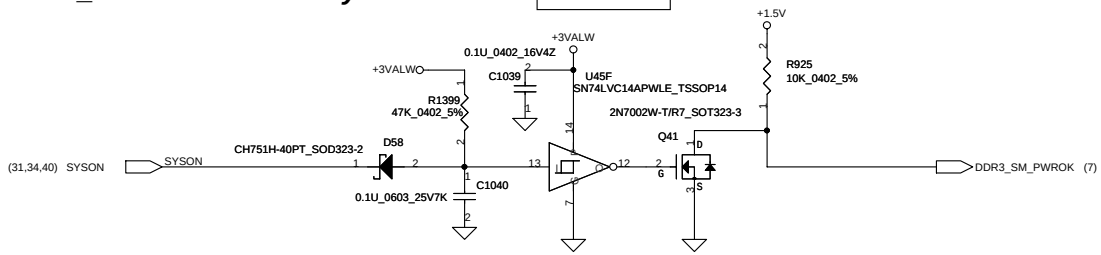
ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

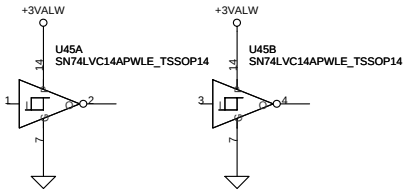


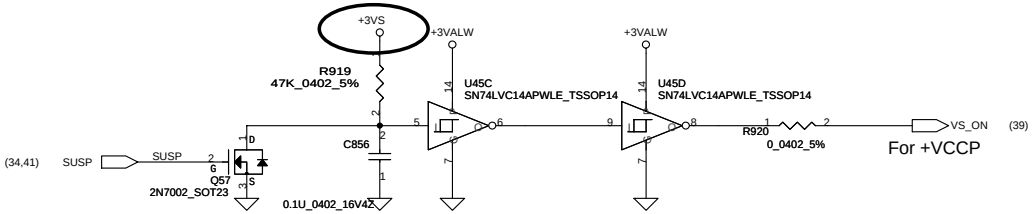
VS_ON will be drived by EC

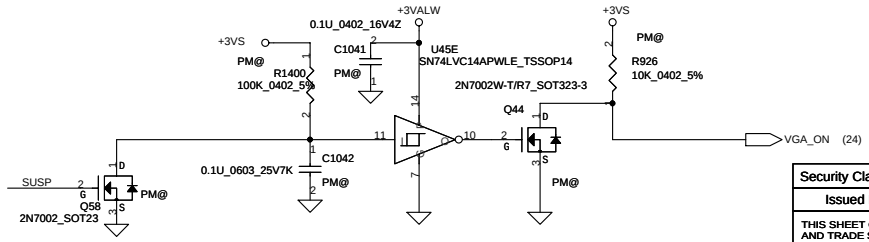
reserve

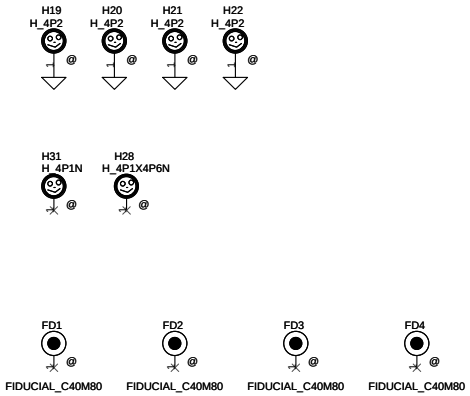
Power ON Circuit











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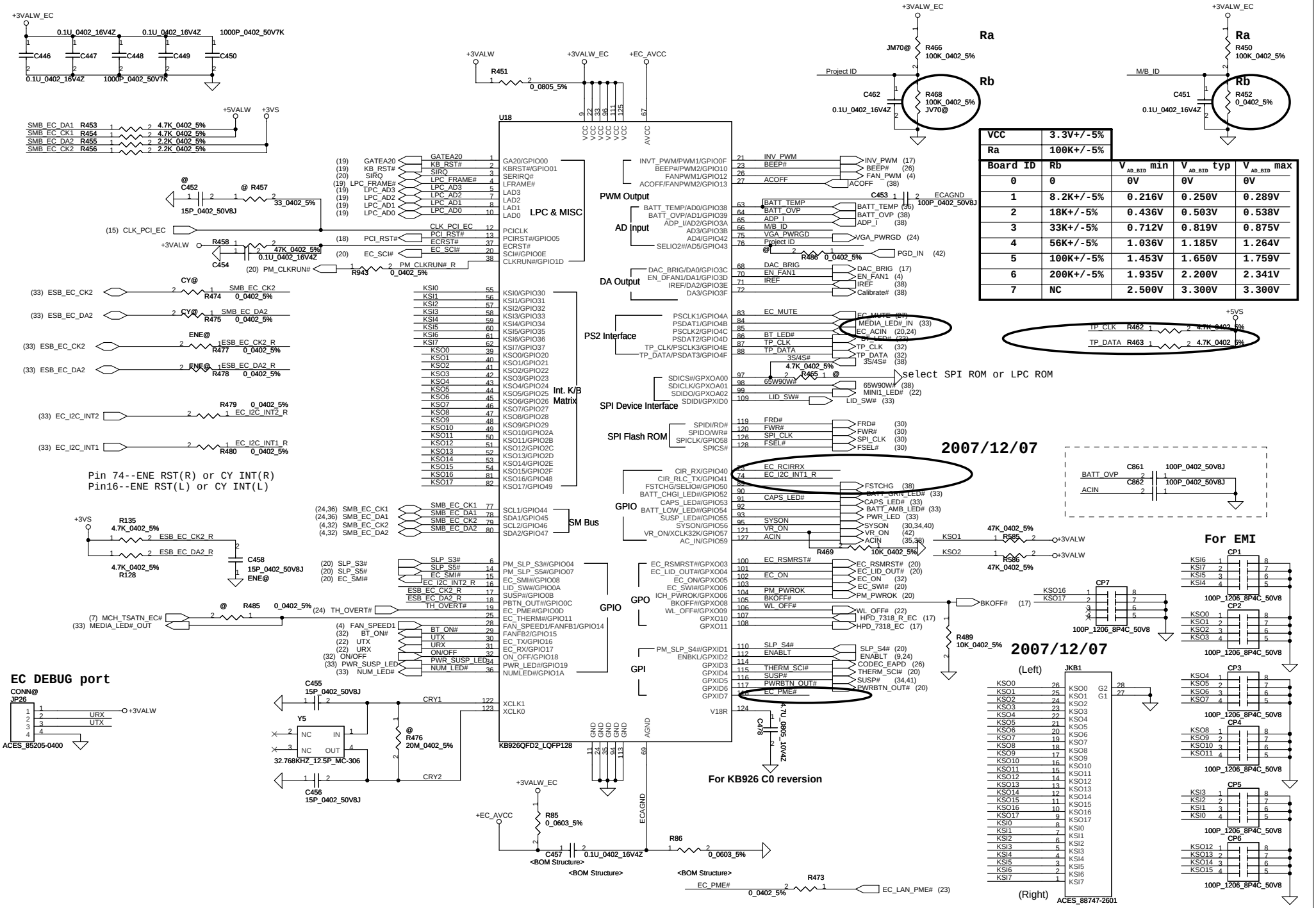

VCC	3.3V+/-5%
Ra	100K+/-5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	18K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V

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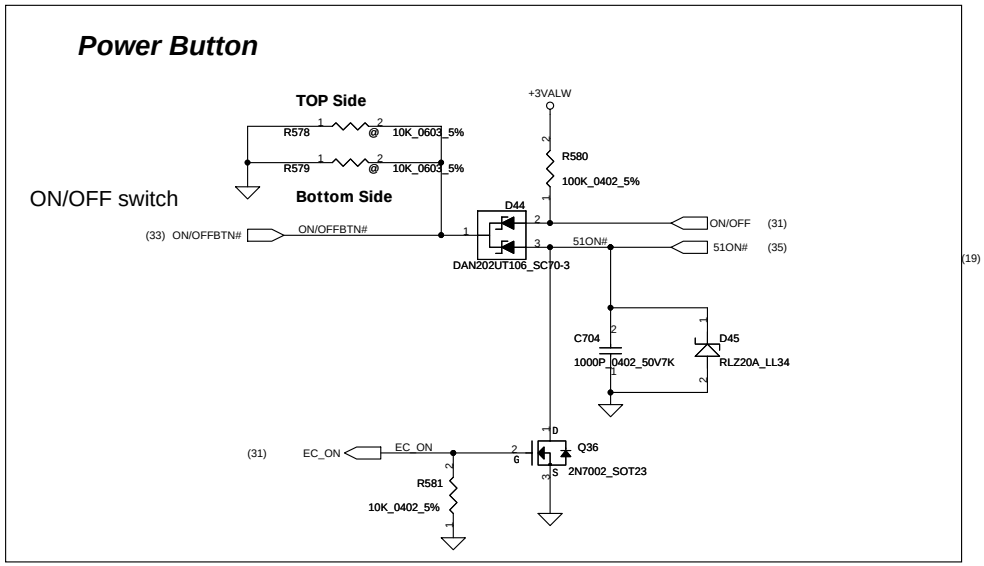

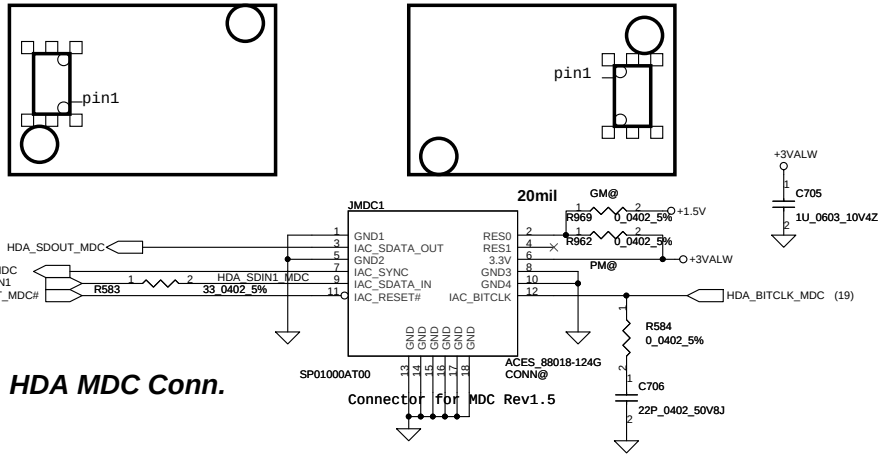

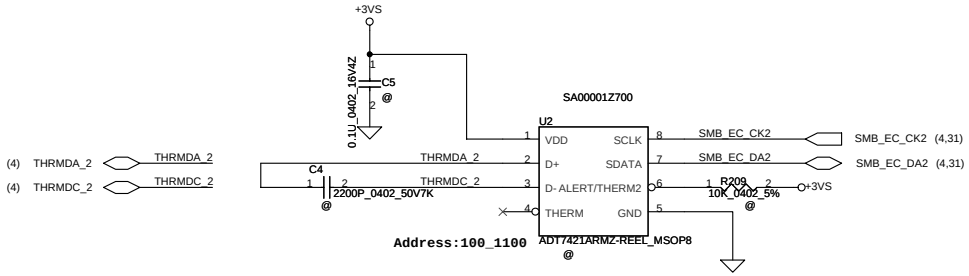

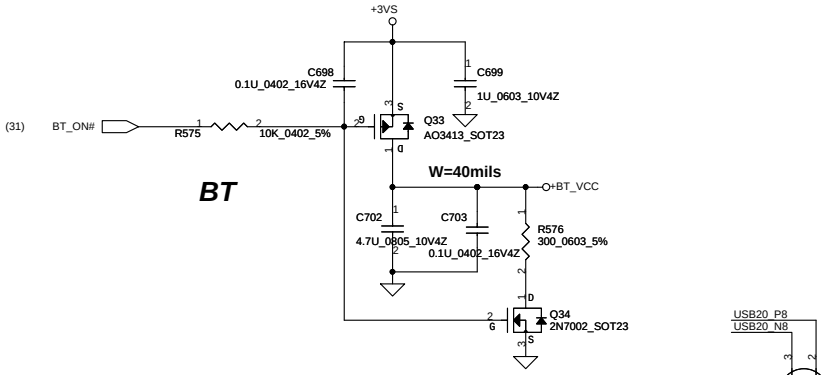

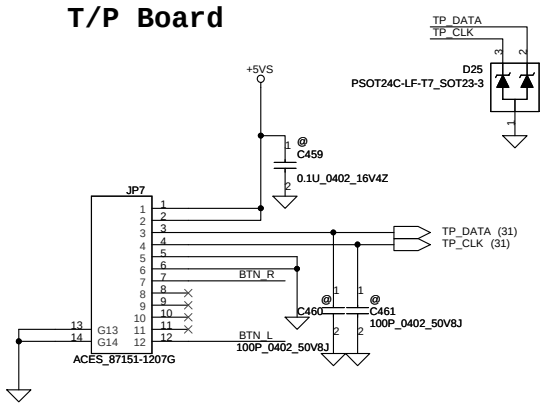

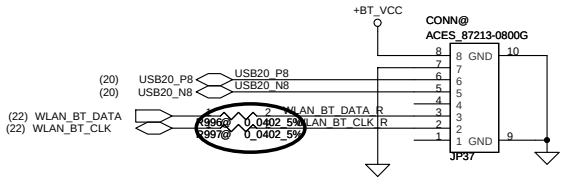

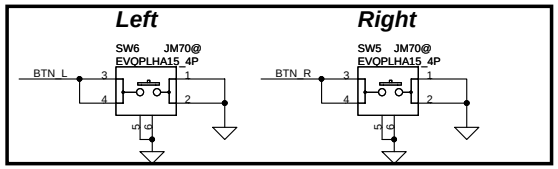

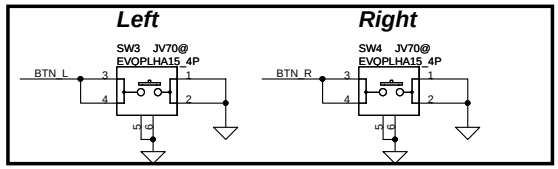

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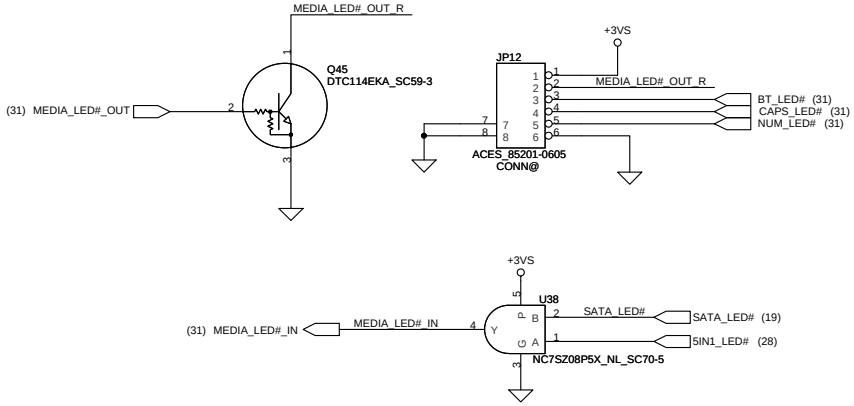
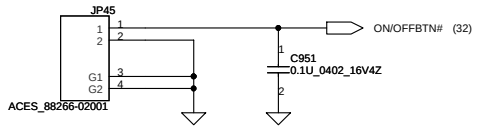
LED/B

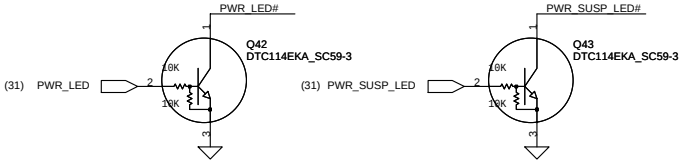
Need Check



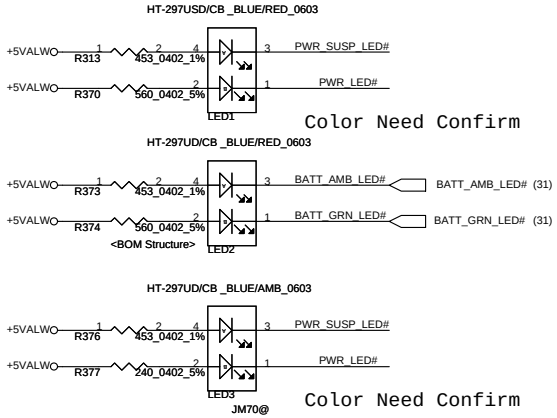
JM70	JV70
1.HDD	1.HDD
2.B/T	2.BT_LED
3.CAP LED	4.NUM LED
4.NUM_LED	3.CAP LED

POWER BOARD





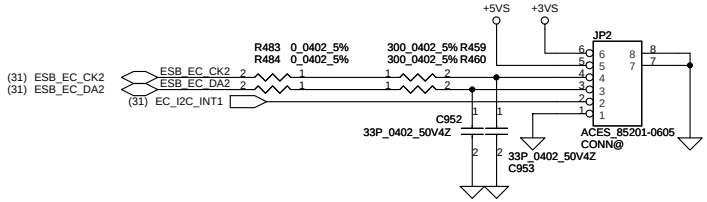
Compal Footprint



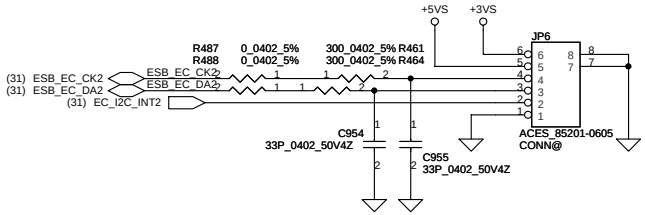
Color Need Confirm

Color Need Confirm

CAP Sansor right

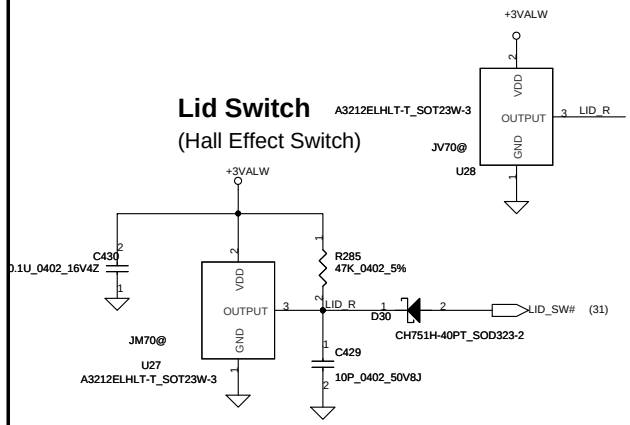


CAP Sansor lift



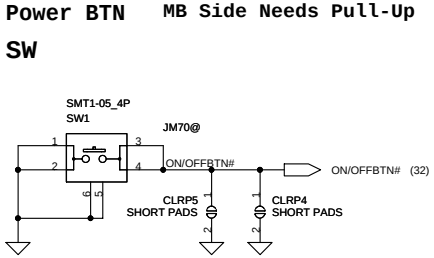
Lid Switch

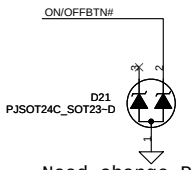
(Hall Effect Switch)



Power BTN SW

MB Side Needs Pull-Up





Need change P/N

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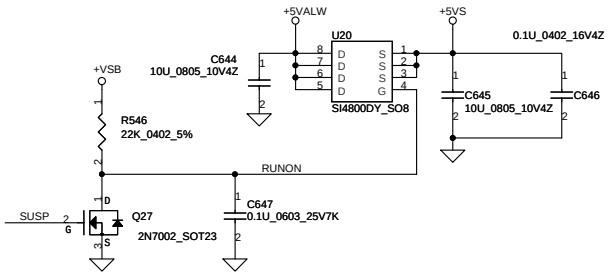
+5VALW to +5VS Transfer



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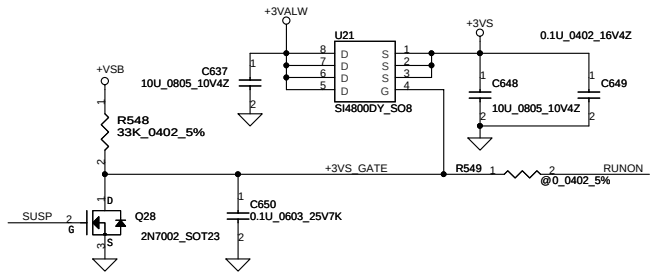
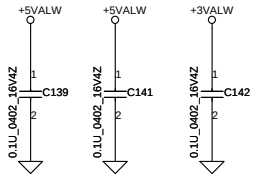
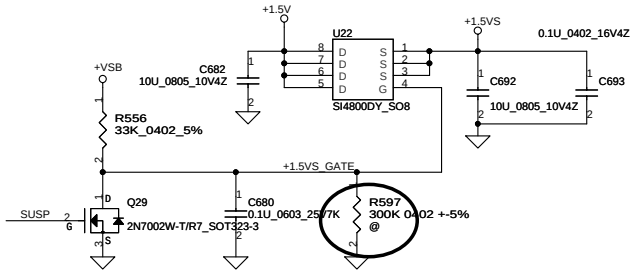


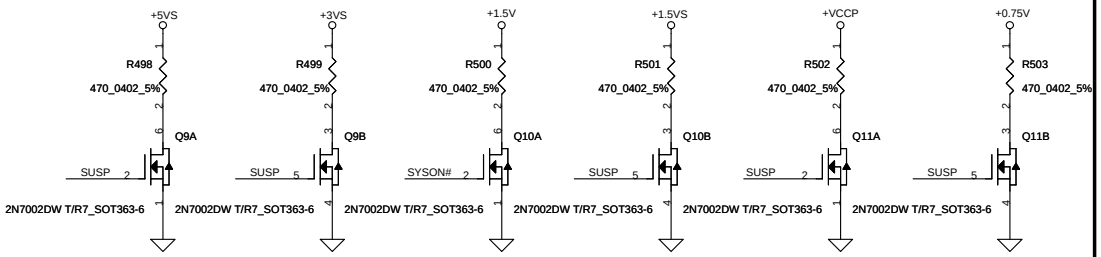


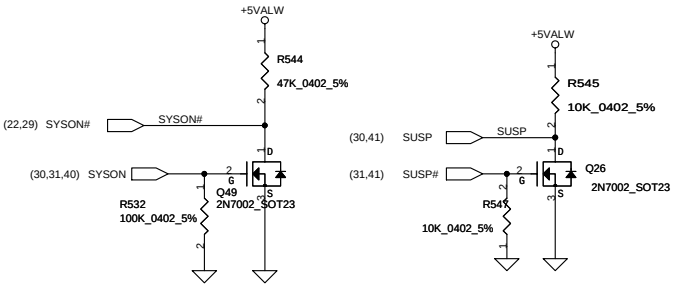
+1.5V to +1.5VS Transfer



1029 DEL

Discharge circuit





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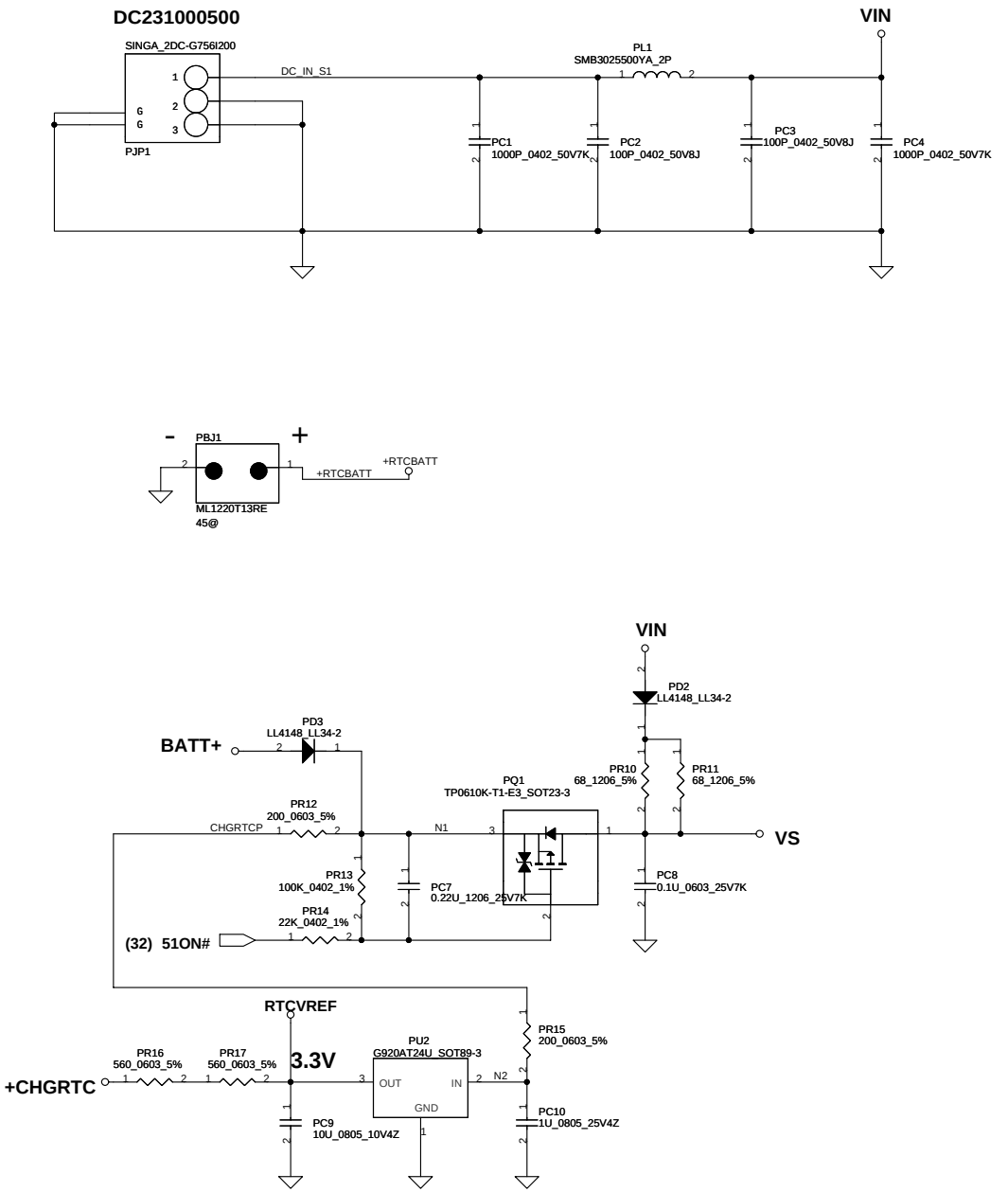

Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

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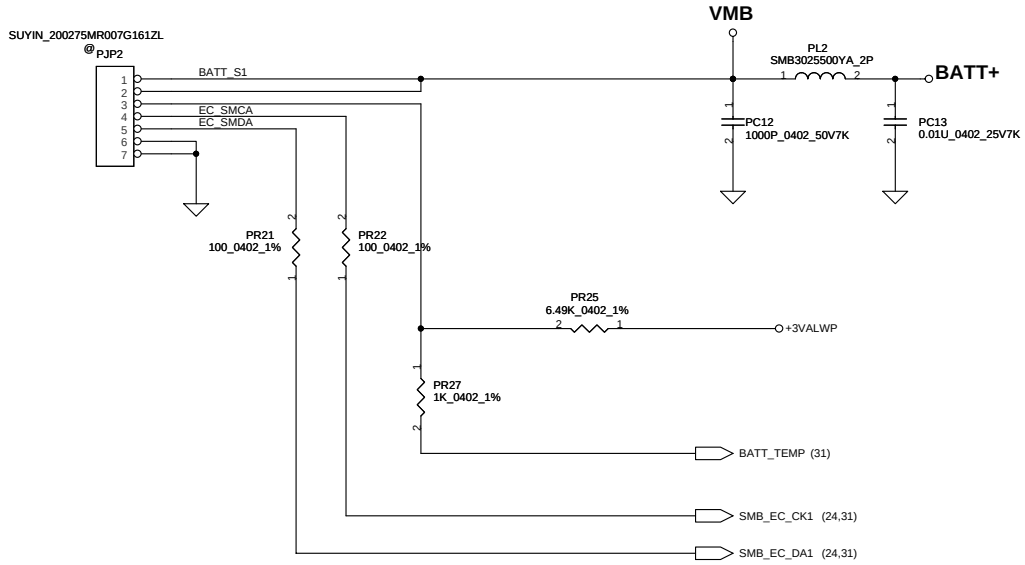
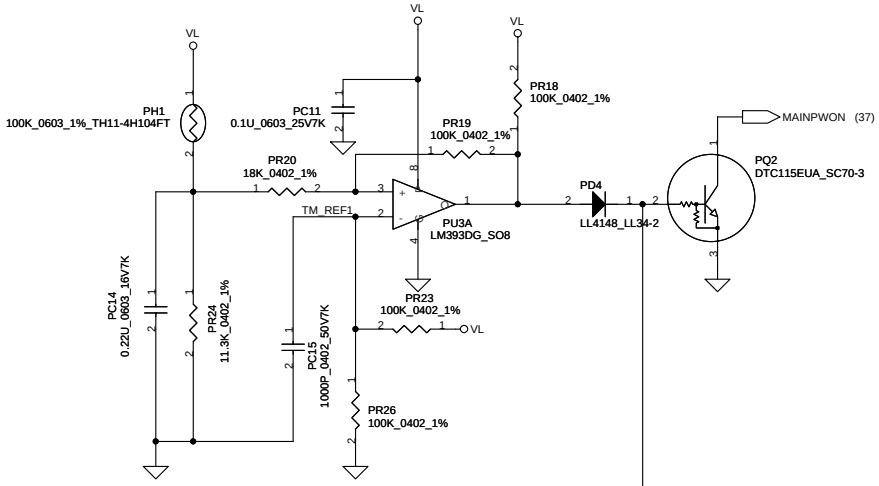
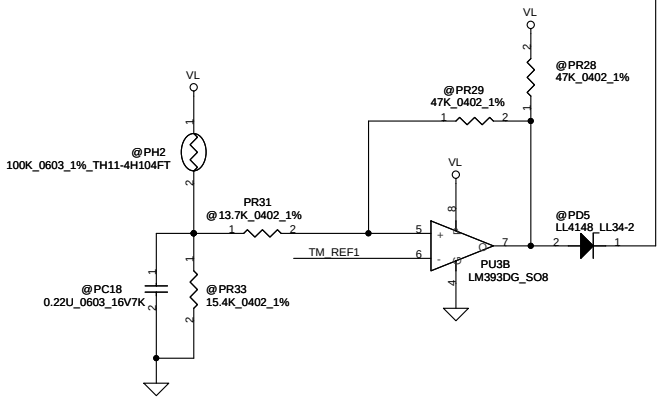
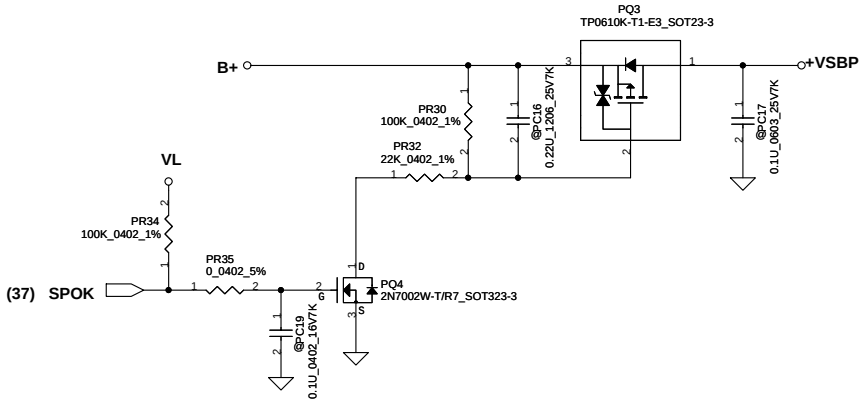
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 70 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C





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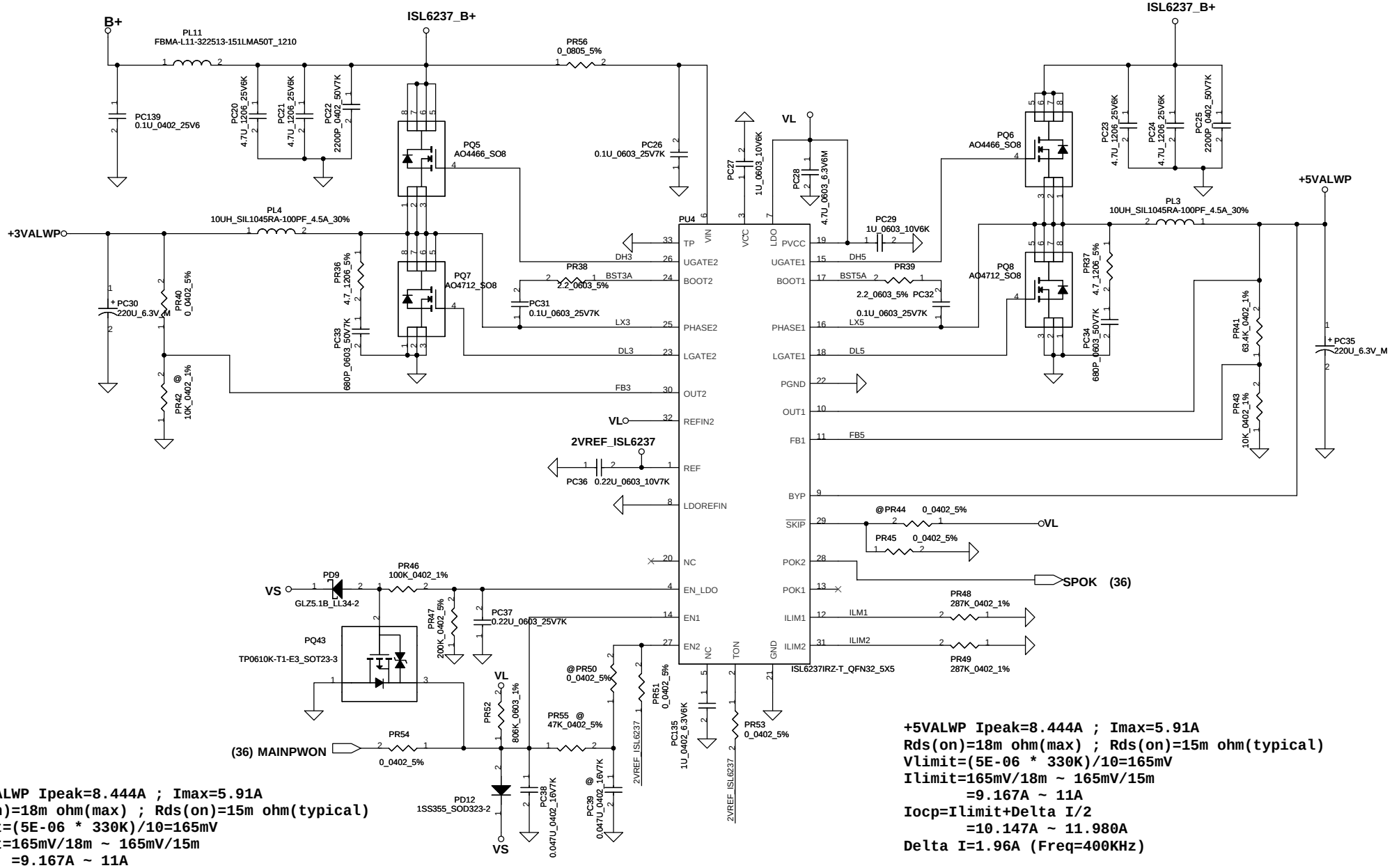

+5VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

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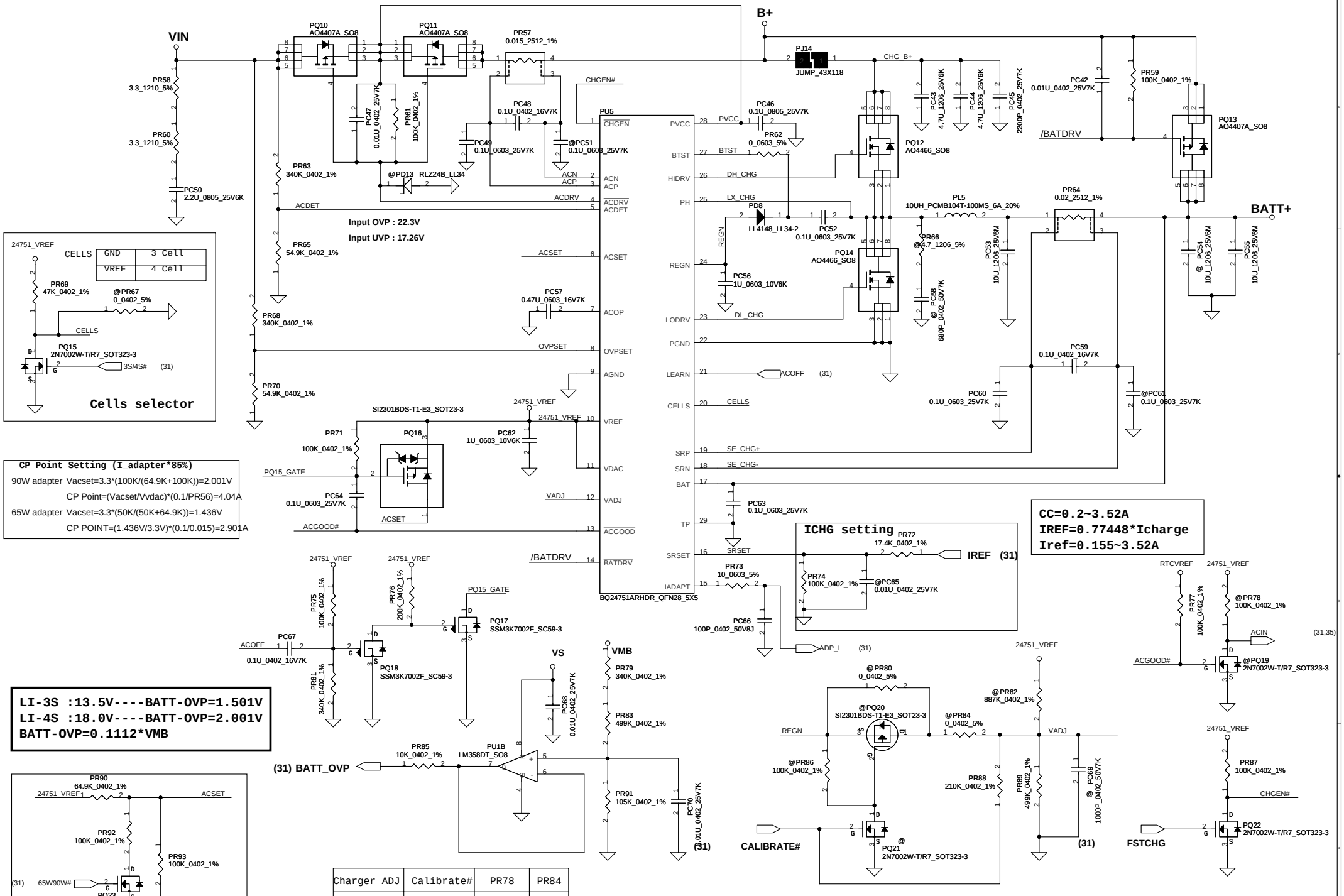

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

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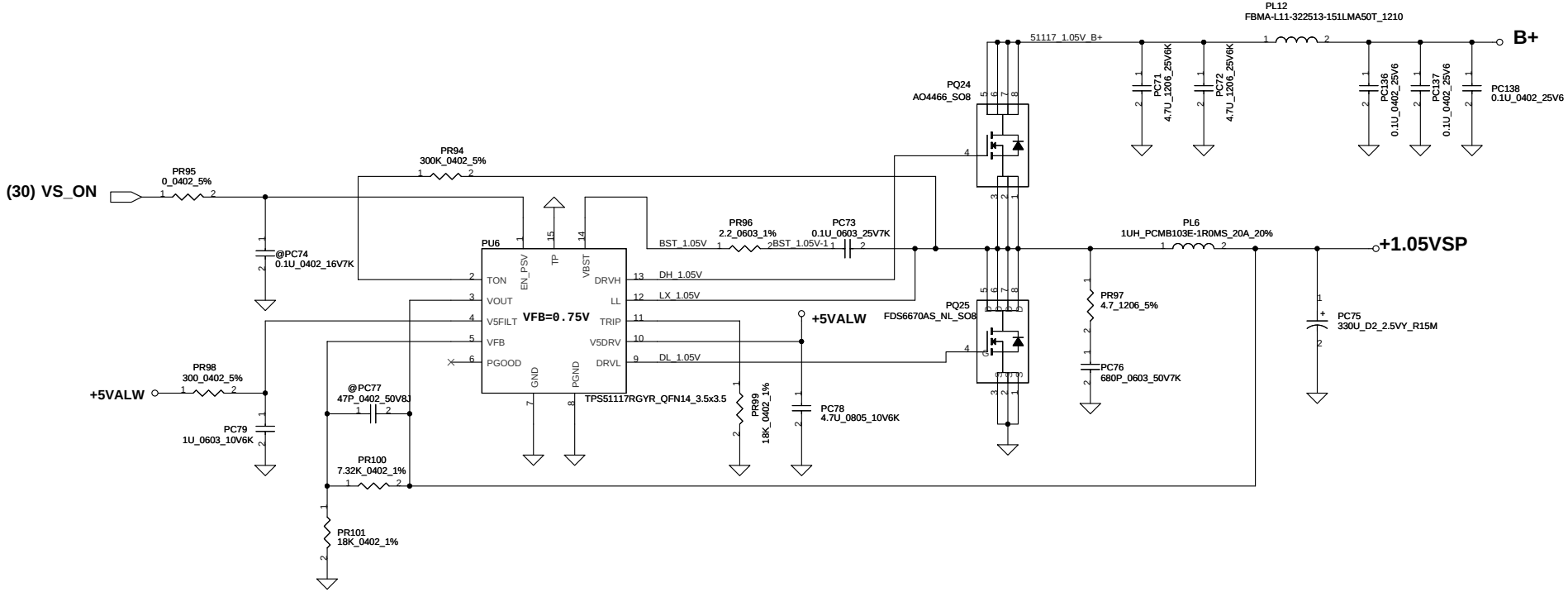

VFB=0.75V
Vo=VFB*(1+PR100/PR101)=1.055V
Fsw=262KHz

Cout ESR=15m ohm
Rdsonmax=11.5m ohm, Rdsontyp=9m ohm
Ipeak=7.15A, Imax=3.5A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=2.103A
=>1/2DeltaI=1.052A
Vtrip=Rtrip*10uA=9.09K*10uA=0.0909V
Iocpmin=Vtrip/Rdsonmax*1.3+1.052A=7.132A
Iocpmax=Vtrip/Rdsontyp*1.1+1.052A=10.233A
Iocp=7.132A~10.233A

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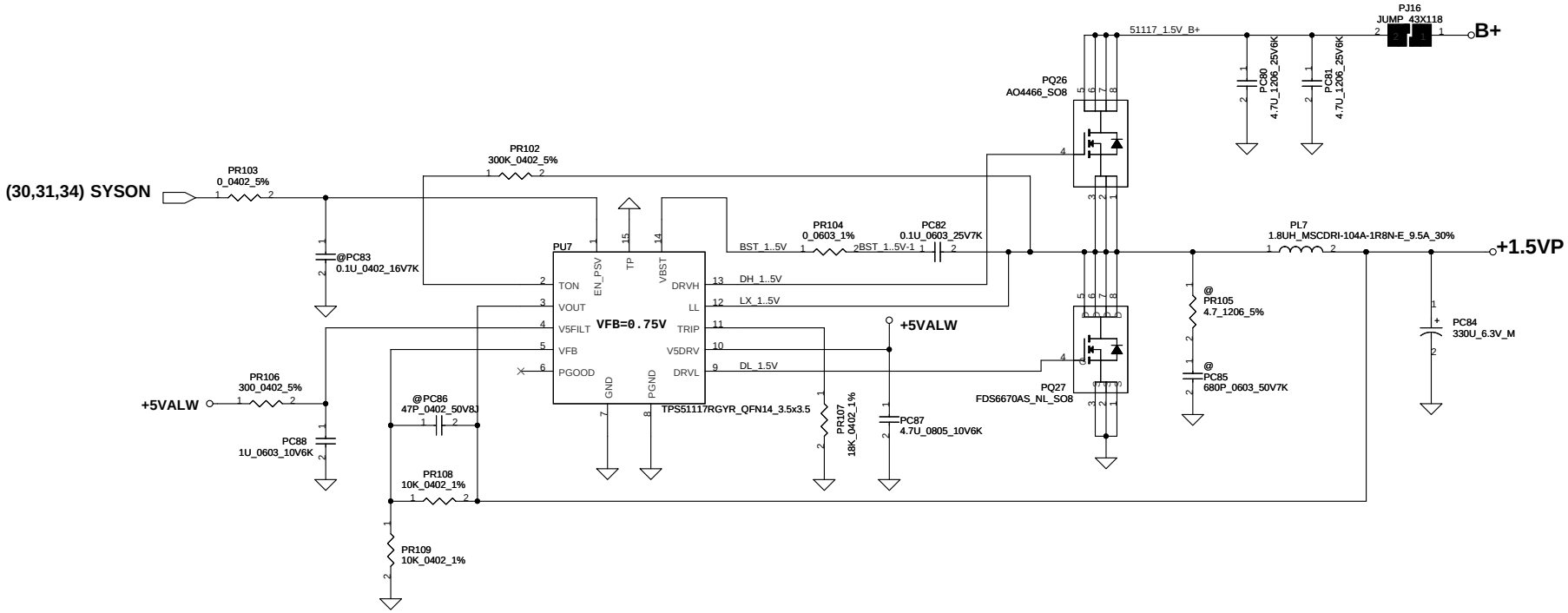

VFB=0.75V
Vo=VFB*(1+PR108/PR109)=1.5V
Fsw=262KHz

Cout ESR=15m ohm
Rdsonmax=11.5m ohm, Rdsontyp=9m ohm
Ipeak=13.67A, Imax=8A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=2.930A
=>1/2DeltaI=1.465A
Vtrip=Rtrip*10uA=18K*10uA=0.180V
Iocpmin=Vtrip/Rdsonmax*1.4+1.465A=12.645A
Iocpmax=Vtrip/Rdsontyp*1.2+1.465A=18.131A
Iocp=12.645A~18.131A

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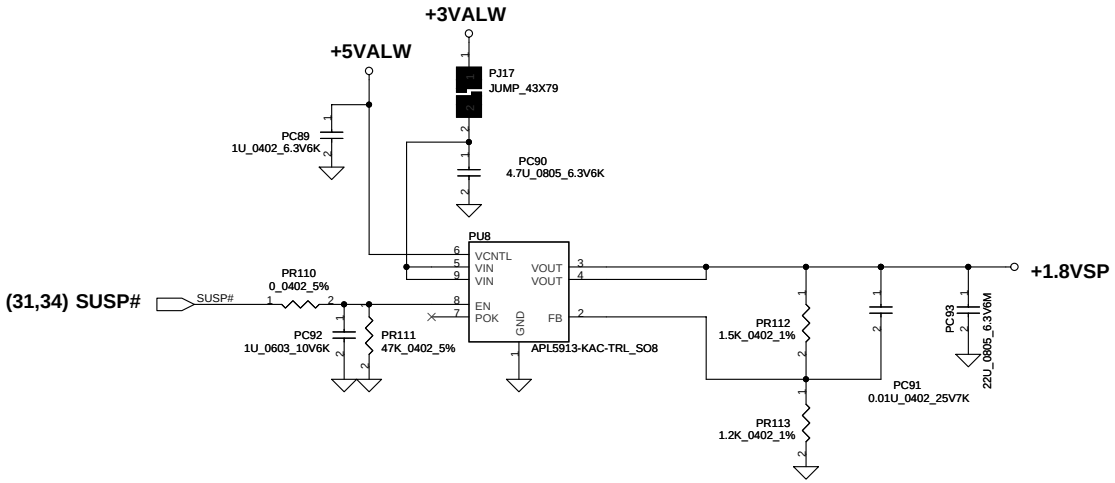

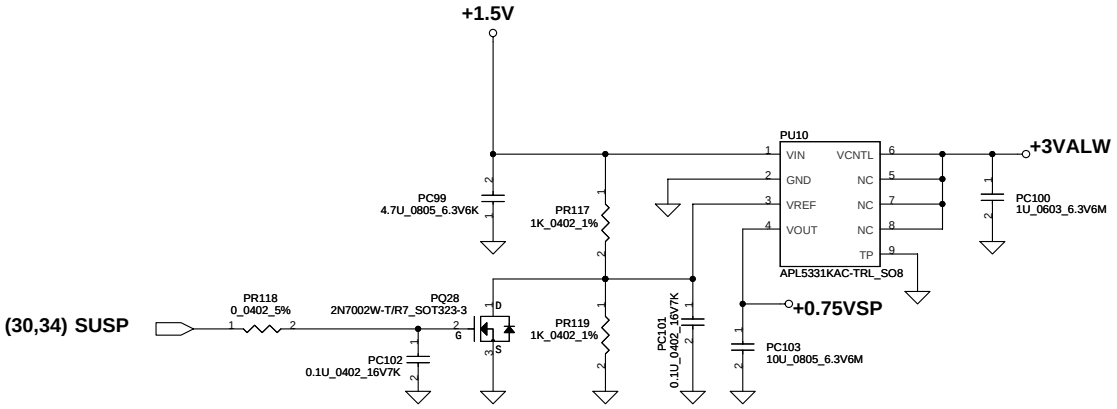

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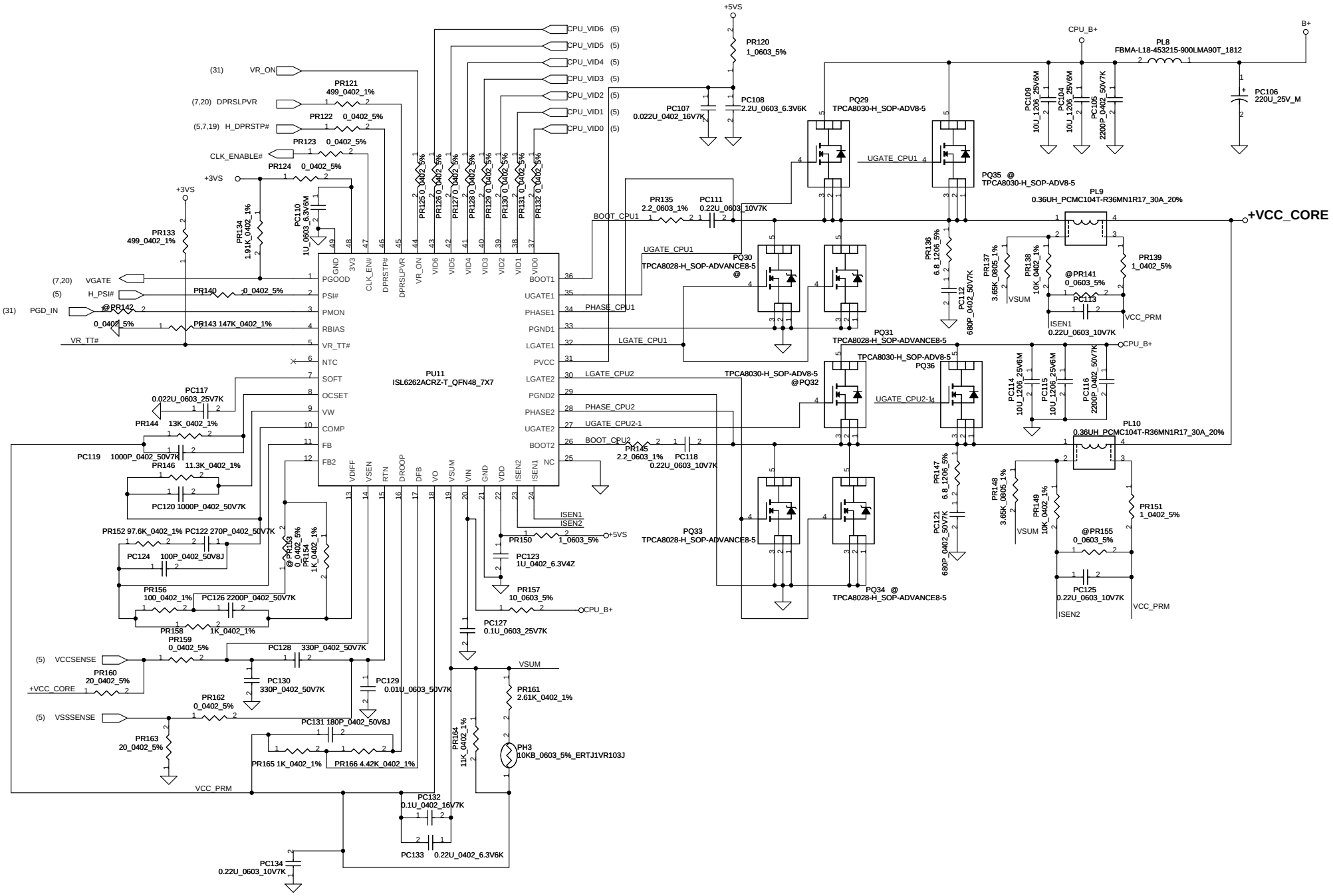

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Solve power noise for HDD signal	Solve power noise for HDD signal	0.1	P37	Change PJ13 to BEAD PL11	12/19	DVT
2	Solve power noise for HDD signal	Solve power noise for HDD signal	0.1	P39	Change PJ15 to BEAD PL12	12/19	DVT
3	+1.05V Efficiency	+1.05V Efficiency	0.1	P39	Change PL6 from 1.2U to 1.0U	12/19	DVT
4	For EMI solution	For EMI solution	0.1	P39	Add PC136,PC137,PC138 ,Change PR96 to 2.2 ohm	12/19	DVT
5	For EMI solution	For EMI solution	0.1	P37	Add PC139	12/19	DVT
6	For EMI solution	For EMI solution	0.1	P42	Change PR135, PR145 to 2.2 ohm	12/19	DVT
7	For EMI solution	For EMI solution	0.2	P39	Pop PR97 and PC76	02/02	PVT
8	Modify CPU MOSFET solution	Modify CPU MOSFET solution	0.2	P42	change PQ29,PQ36 to SB00000HL00	02/02	PVT
9	Modify CPU MOSFET solution	Modify CPU MOSFET solution	0.2	P42	change PQ31,PQ33 to SB00000GL00	02/02	PVT
10	Modify CPU MOSFET solution	Modify CPU MOSFET solution	0.2	P42	Unpop PQ32,PQ35,PQ30,PQ34	02/02	PVT
11	Modify CPU PWM frequency	Modify CPU PWM frequency	0.2	P42	change PR146 to SD034113280	02/02	PVT
12							
13							
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23							

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