Compal Confidential

NAYF0 M/B Schematics Document

Intel Arrandale/Clarksfield Processor with DDRIII + Ibex Peak-M

2009-08-27

REV:0.1

PCB

ZZZ

DAZ@
DA80000GT00

NAYF0 LA-5881P REV0 M/B

LA-5881P MB Rev0: DA80000GT00

VRAM PARK

ZZZ

VRAM PARK@
X76193BOL01

512M HIX

VRAM MAD

ZZZ

VRAM MAD@
X76193BOL03

1G HIX

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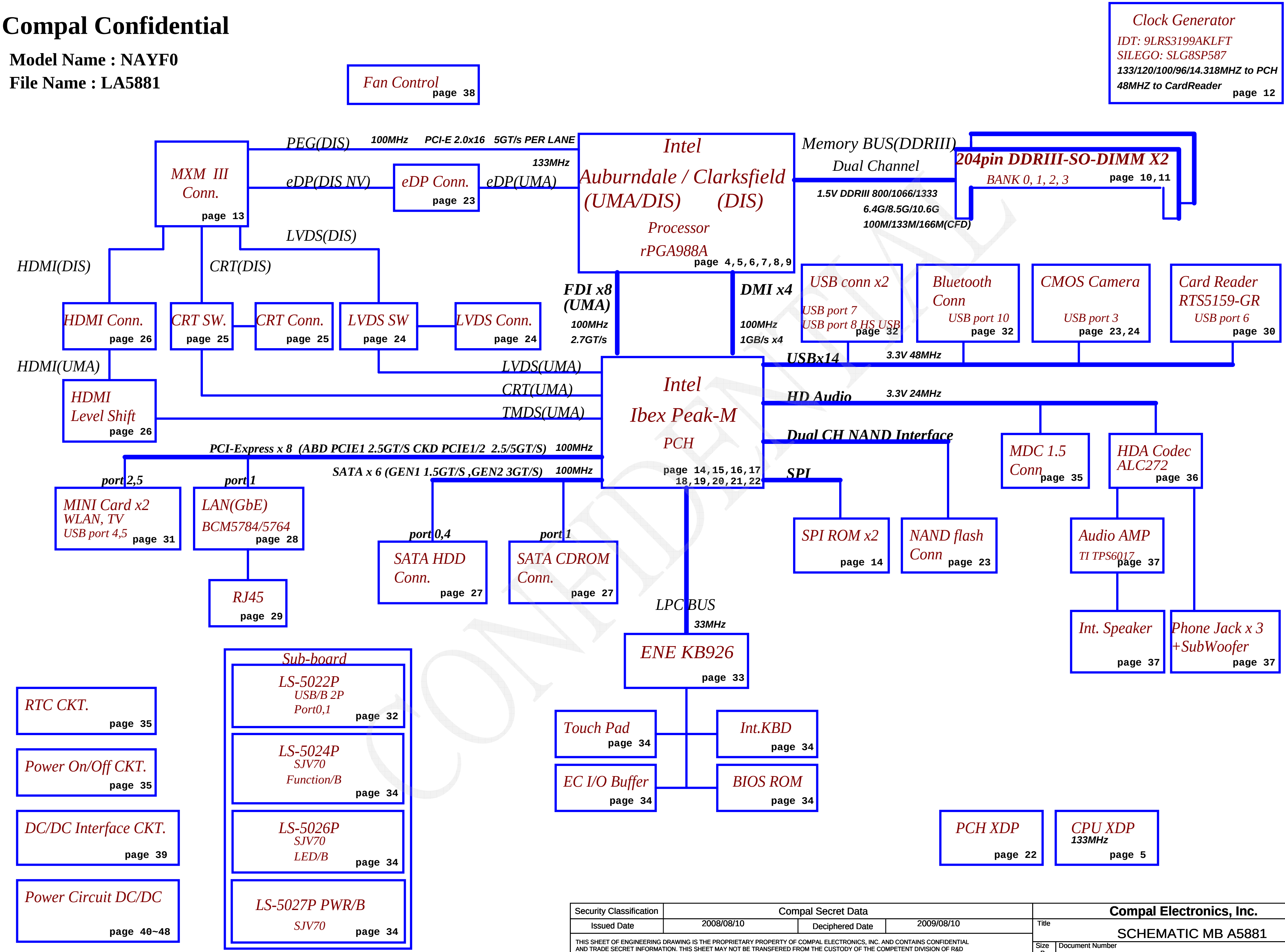
Model Name : NAYF0
File Name : LA5881



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
ALC 271	271@
ALC 272	272@
ASM1442	ASM@
CH7318	CH@
S3	S3@
NONS3	NONS3@
XDP	XDP@
Switchable	SG@
VGA	VGA@
UMA	UMA@
UMAO	UMAO@
DISO	DISO@
MADISON	MAD@
PARK	PARK@
VRAM MADISON	VRAM MAD@
VRAM PARK	VRAM PARK@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 USB	Ext1 USB
		1	Ext2 USB	Ext2 USB
	UHCI1	2	Ext3 USB (JV only)	
		3	Camera	Camera
	UHCI2	4	1st Min-Card	1st Min-Card
		5	2st Min-Card	2st Min-Card
	UHCI3	6	Card Reader	Card Reader
		7	Ext3 USB (JM only)	
EHCI2	UHCI4	8	Ext4 HS USB	Ext3 HS USB
		9		
	UHCI5	10	Blue Tooth	Blue Tooth
		11		
	UHCI6	12		
		13		

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727 ISL90728	0101 1100b 0111 1100b

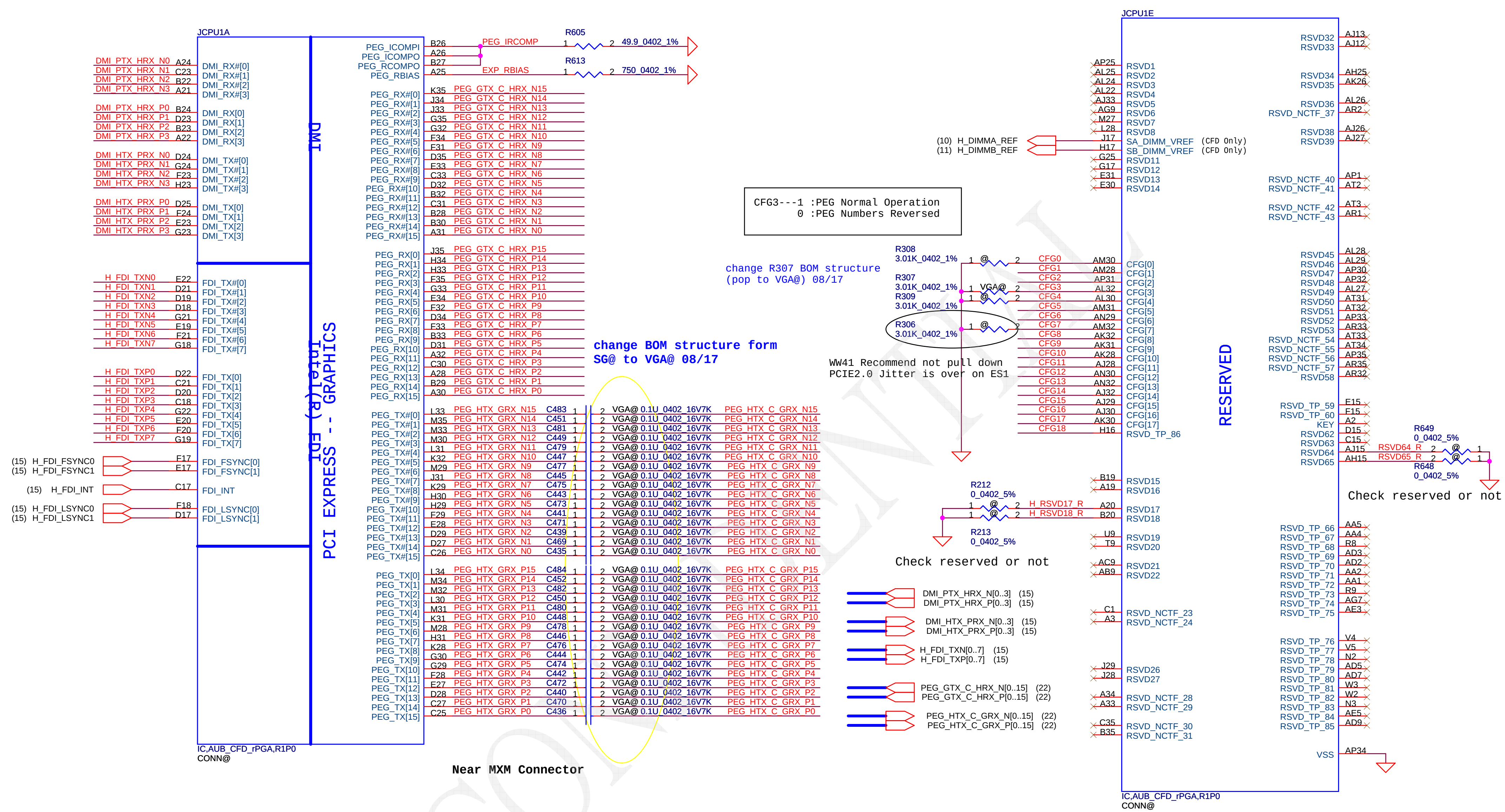
BOM Config

UMA only SKU:UMAO@/UMA@

Switchable PARK SKU: SG@/VGA@/PARK@/VRAM PARK@

Switchable MADISON SKU: SG@/VGA@/MAD@/VRAM MAD@

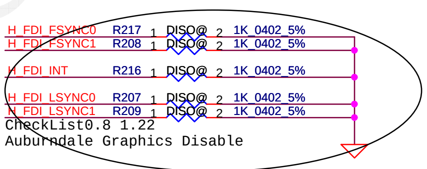
The same: 272@/ASM@/NONS3@/DAZ@



eDP Signals MAPPING

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

Near MXM Connector



CheckList0.8 1.22
Auburndale Graphics Disable

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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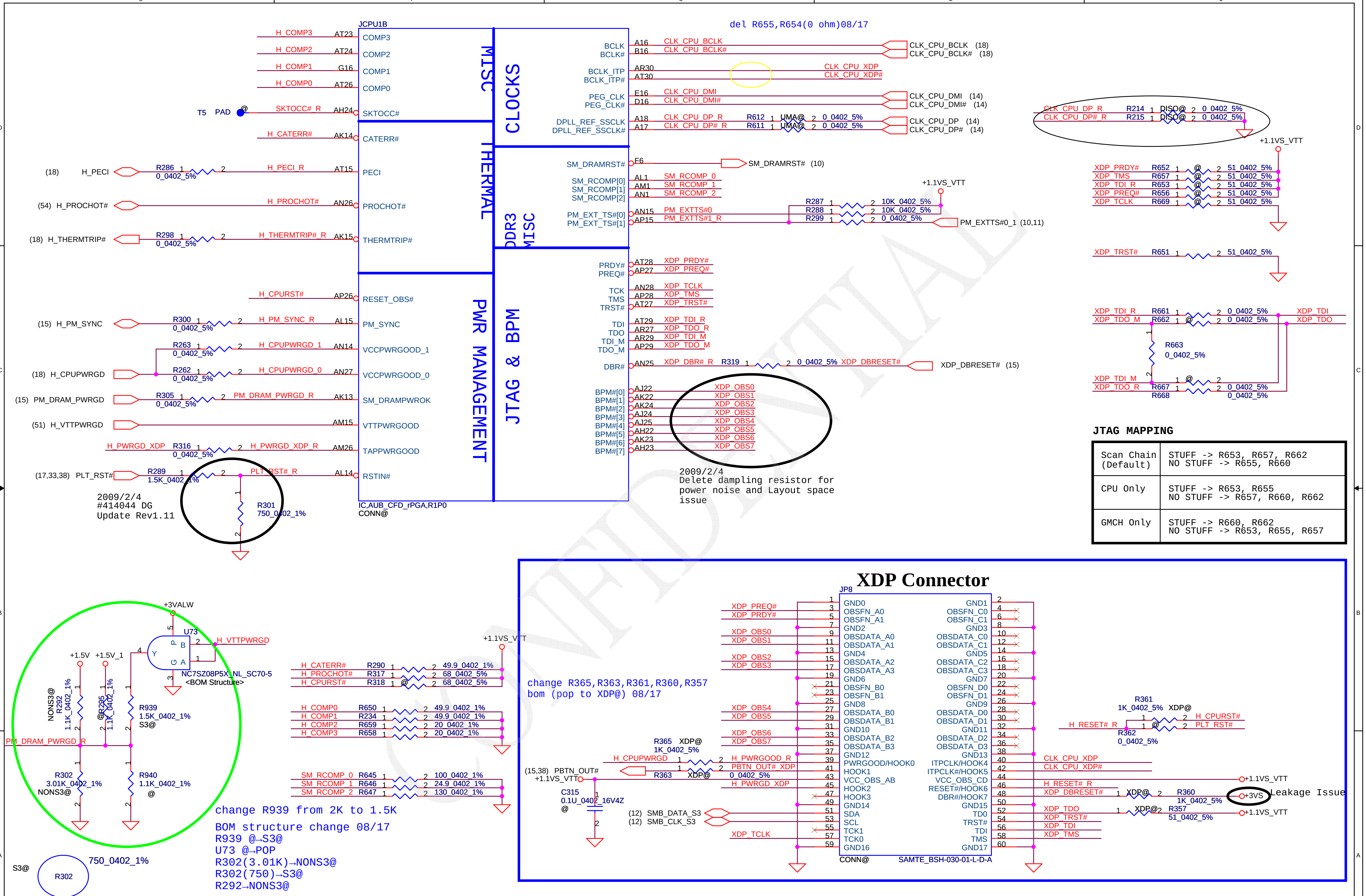

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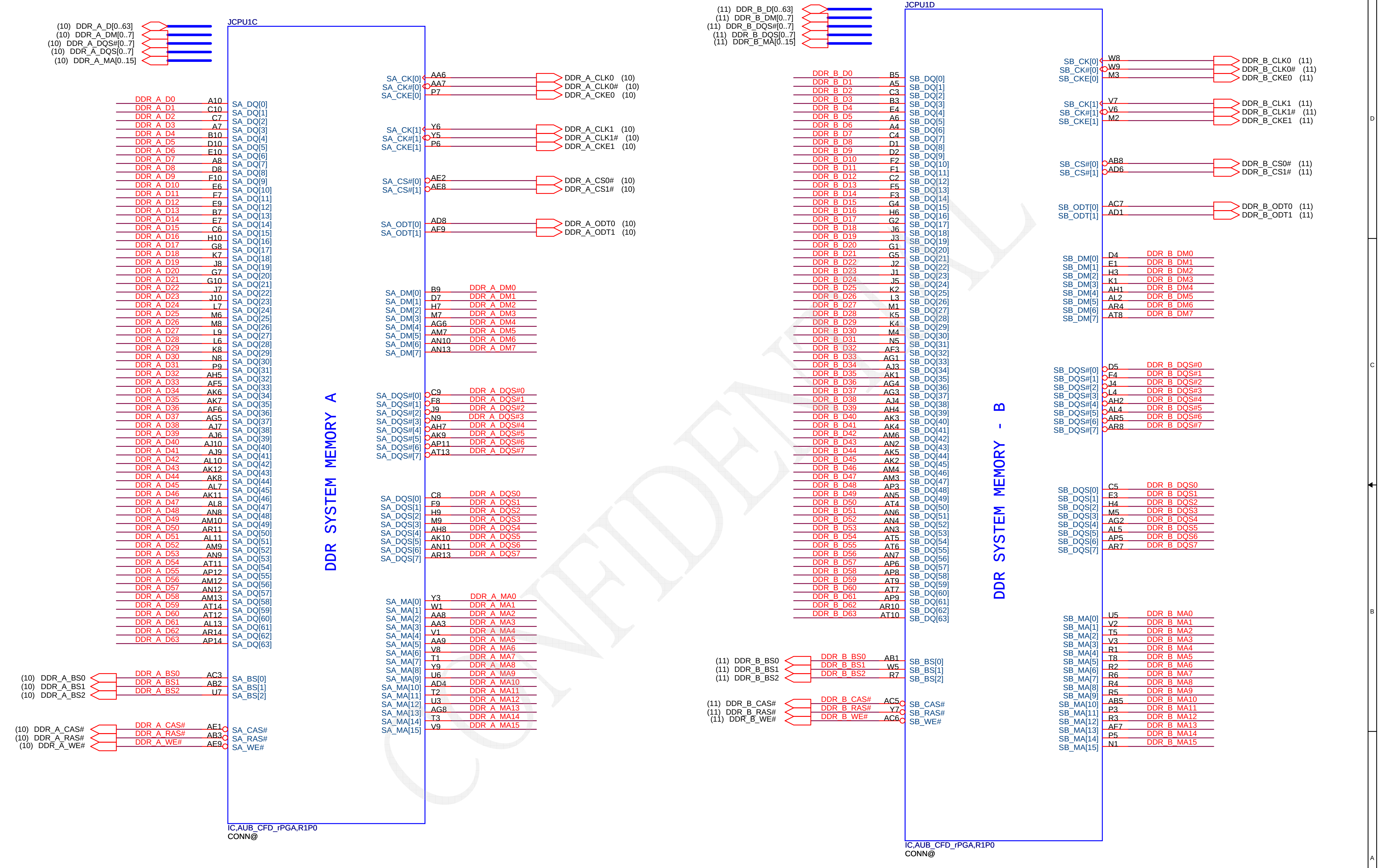

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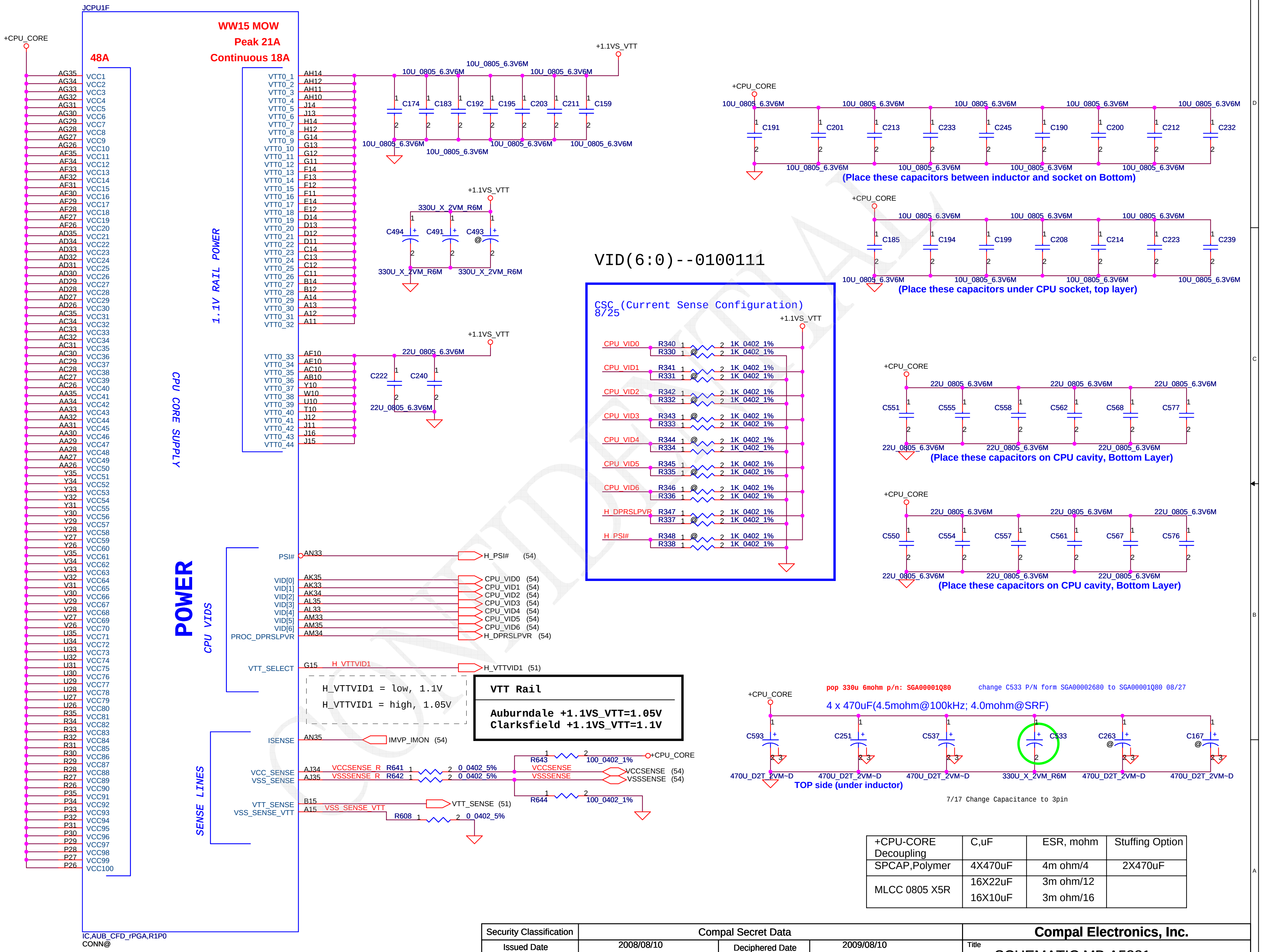

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

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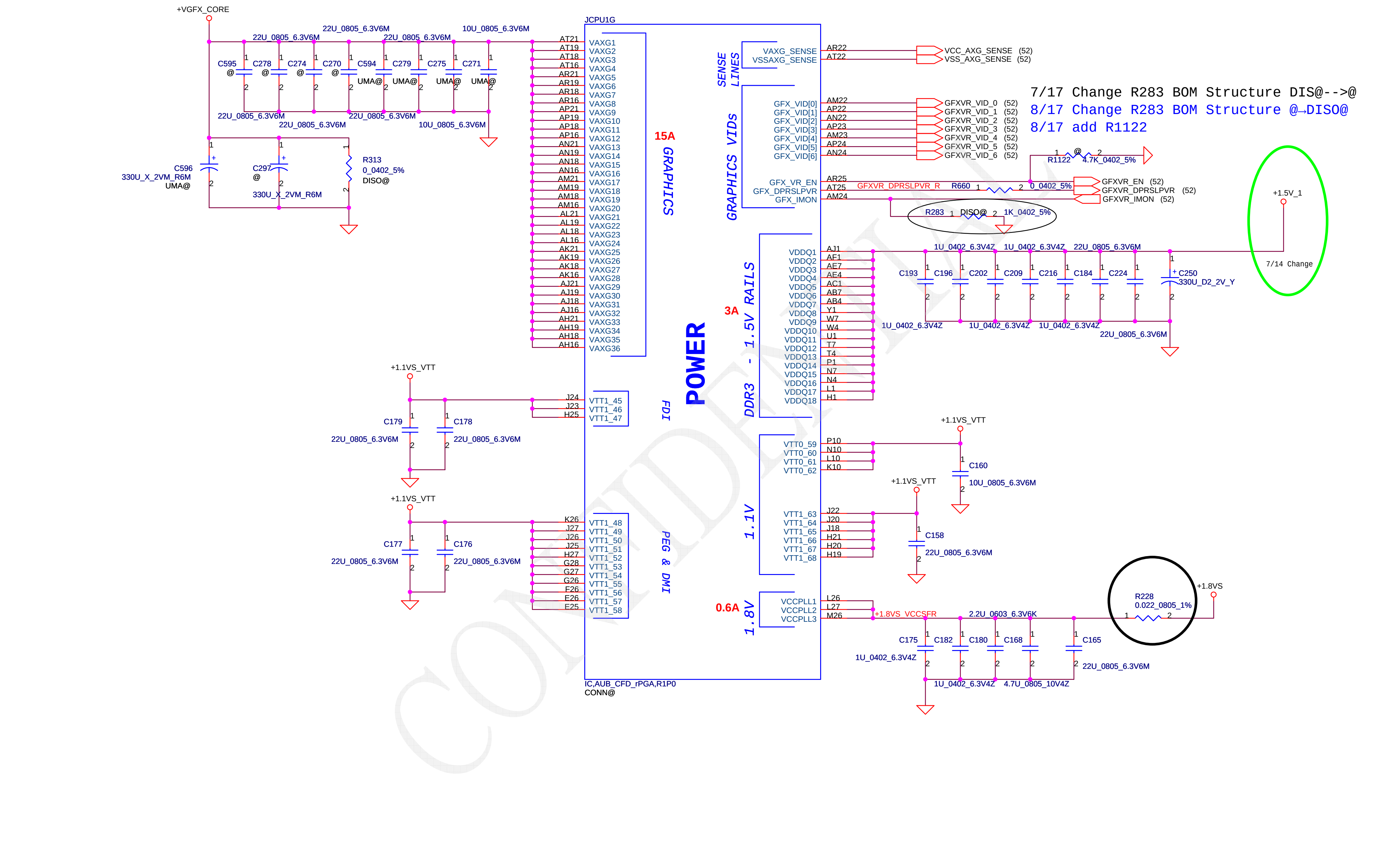

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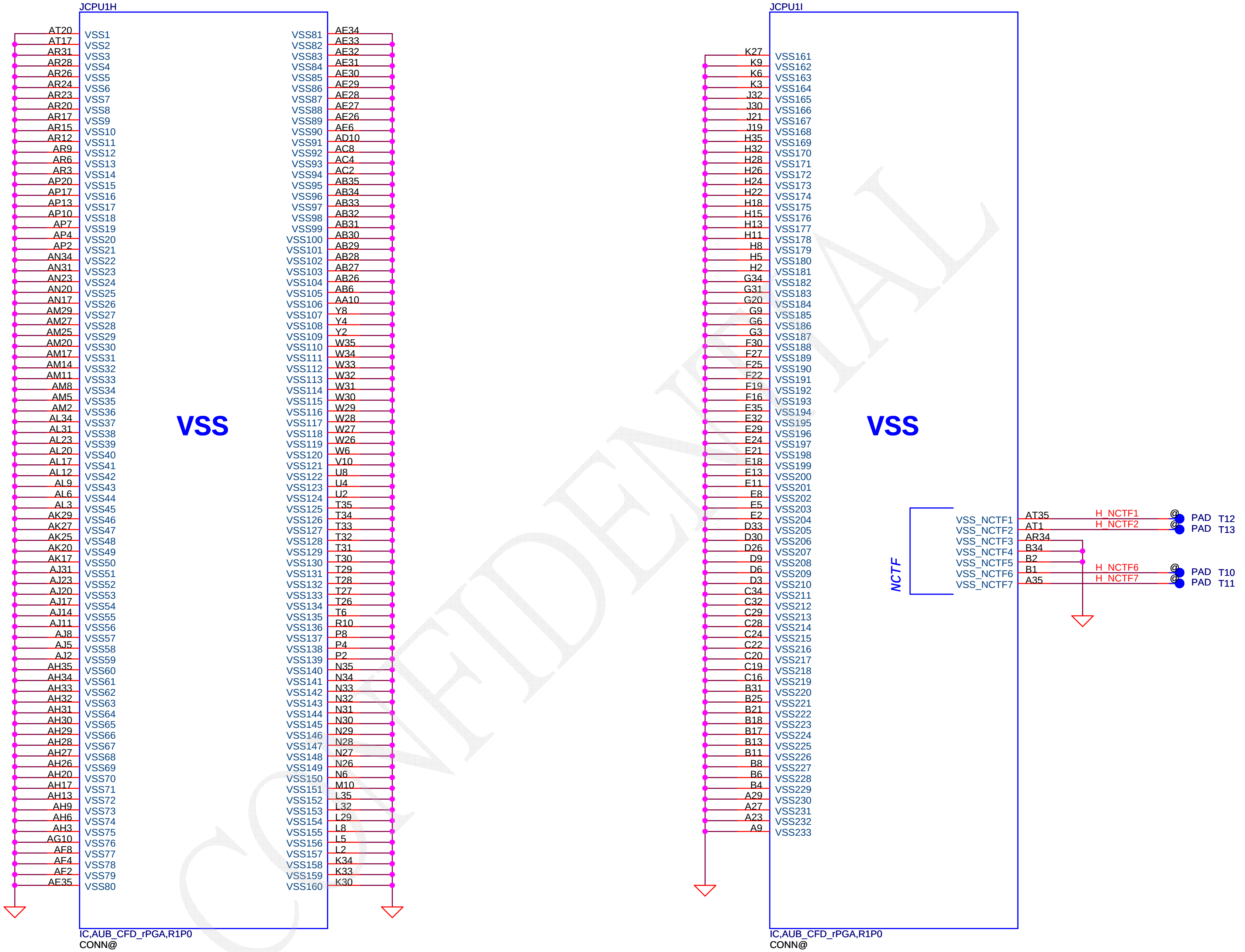

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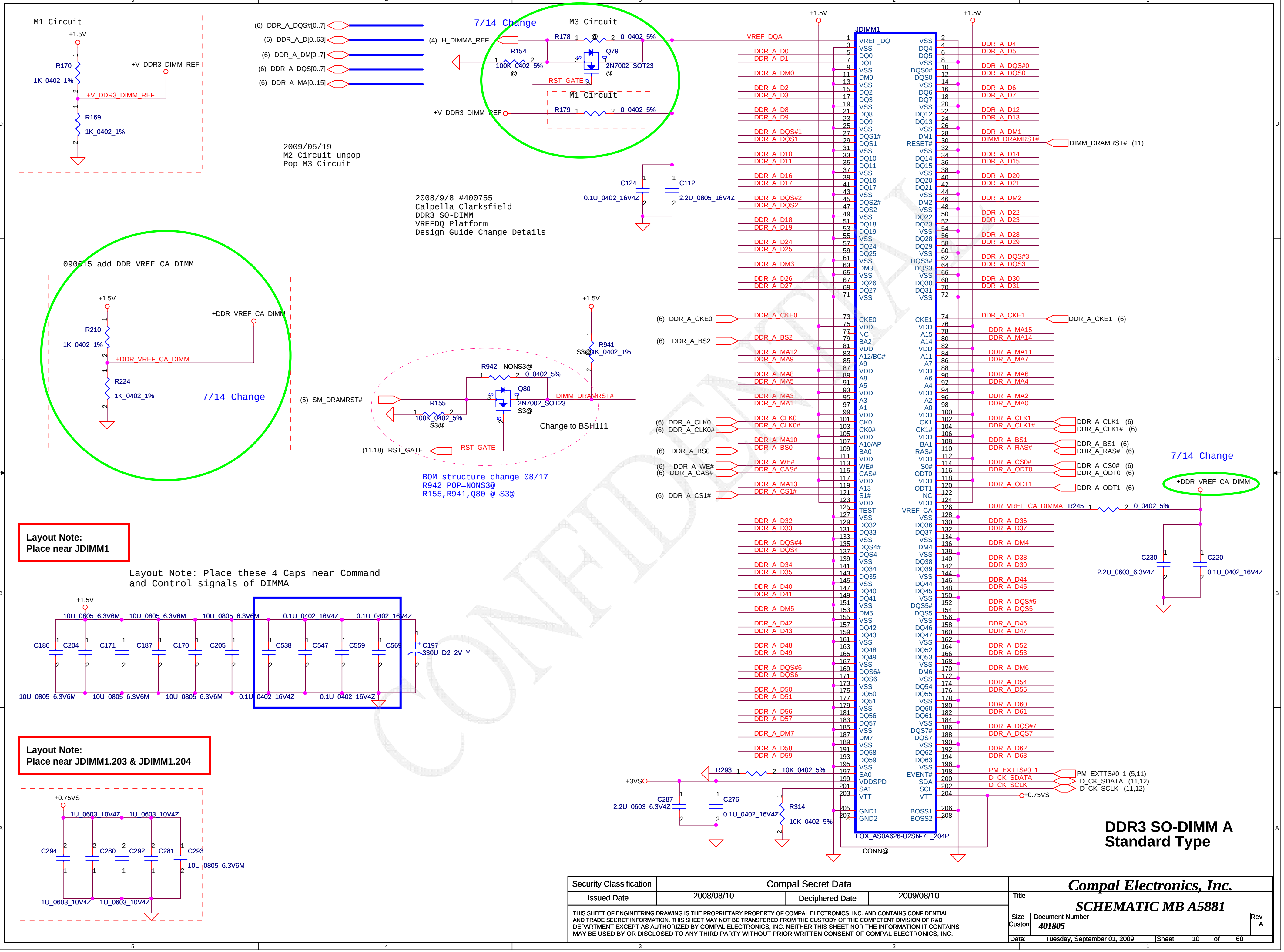
M1 Circuit
M3 Circuit
7/14 Change
2009/05/19
M2 Circuit unpop
Pop M3 Circuit
2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details
090615 add DDR_VREF_CA_DIMM
Change to BSH111
BOM structure change 08/17
R942 POP→NONS3@
R155,R941,Q80 @→S3@
Layout Note:
Place near JDIMM1
Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA
Layout Note:
Place near JDIMM1.203 & JDIMM1.204
JDIMM1
FOX_AS0A626-U2SN-7F_204P
CONN@
DDR3 SO-DIMM A
Standard Type
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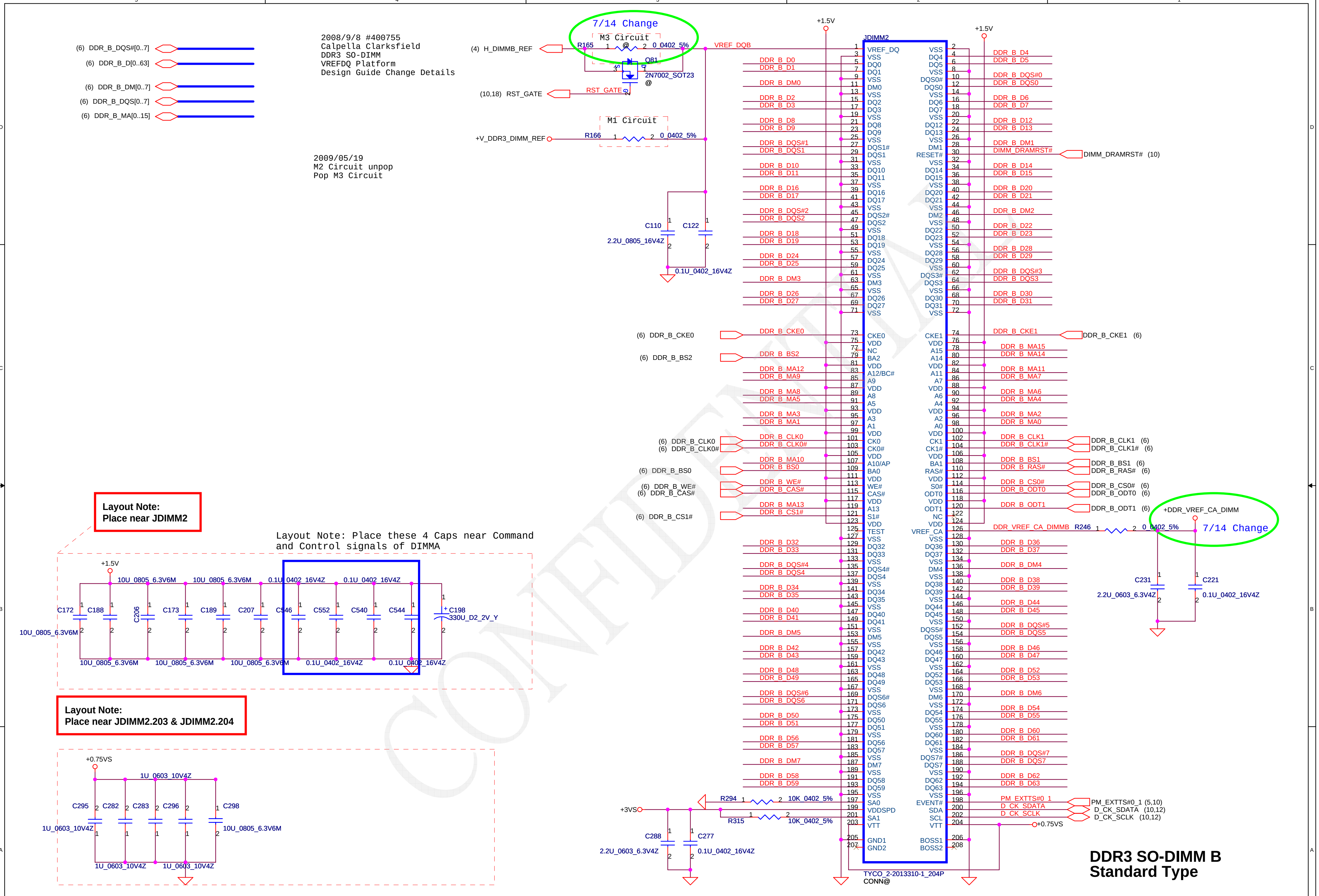

DDR3 SO-DIMM B Standard Type

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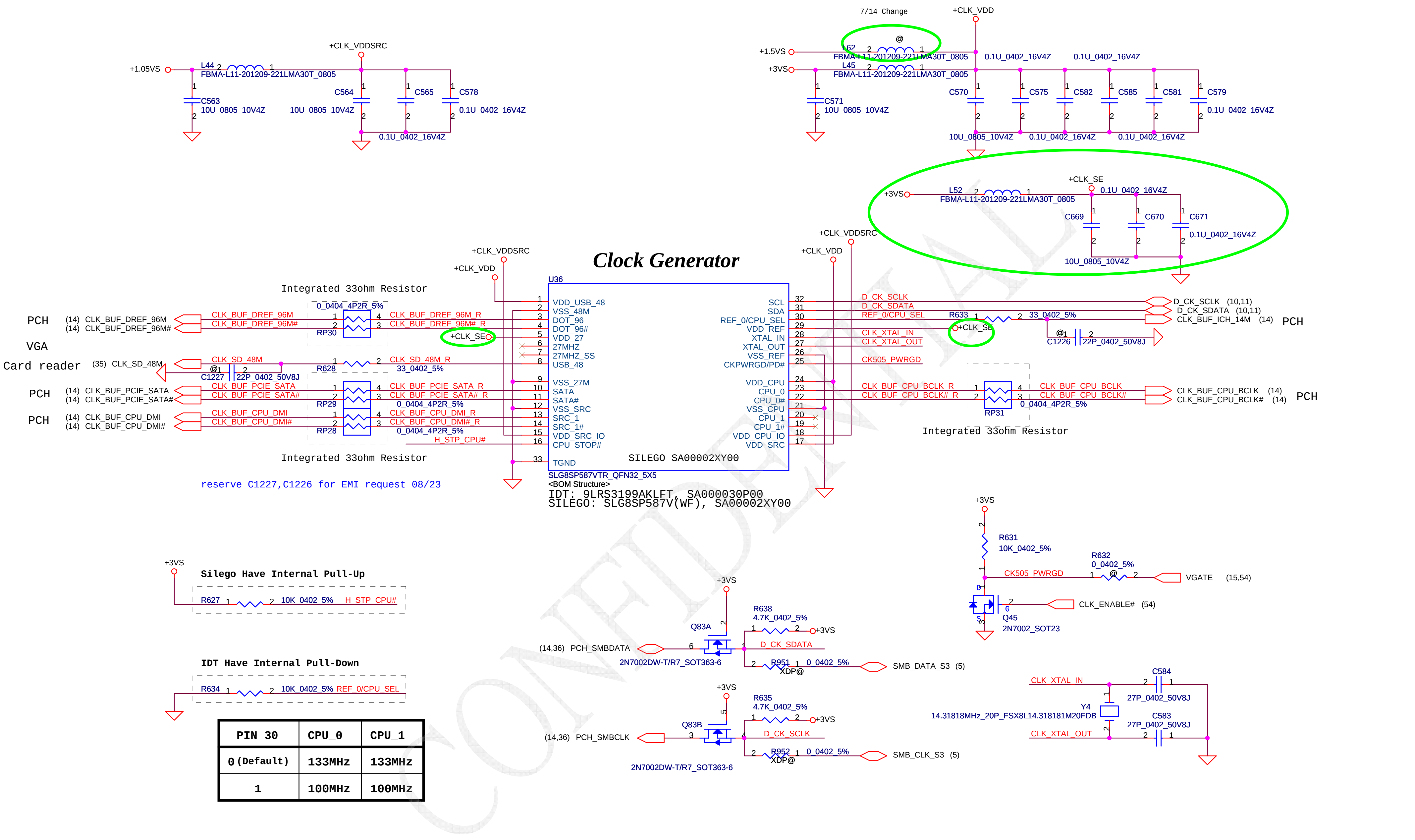

PIN 30	CPU_0	CPU_1
0(Default)	133MHz	133MHz
1	100MHz	100MHz

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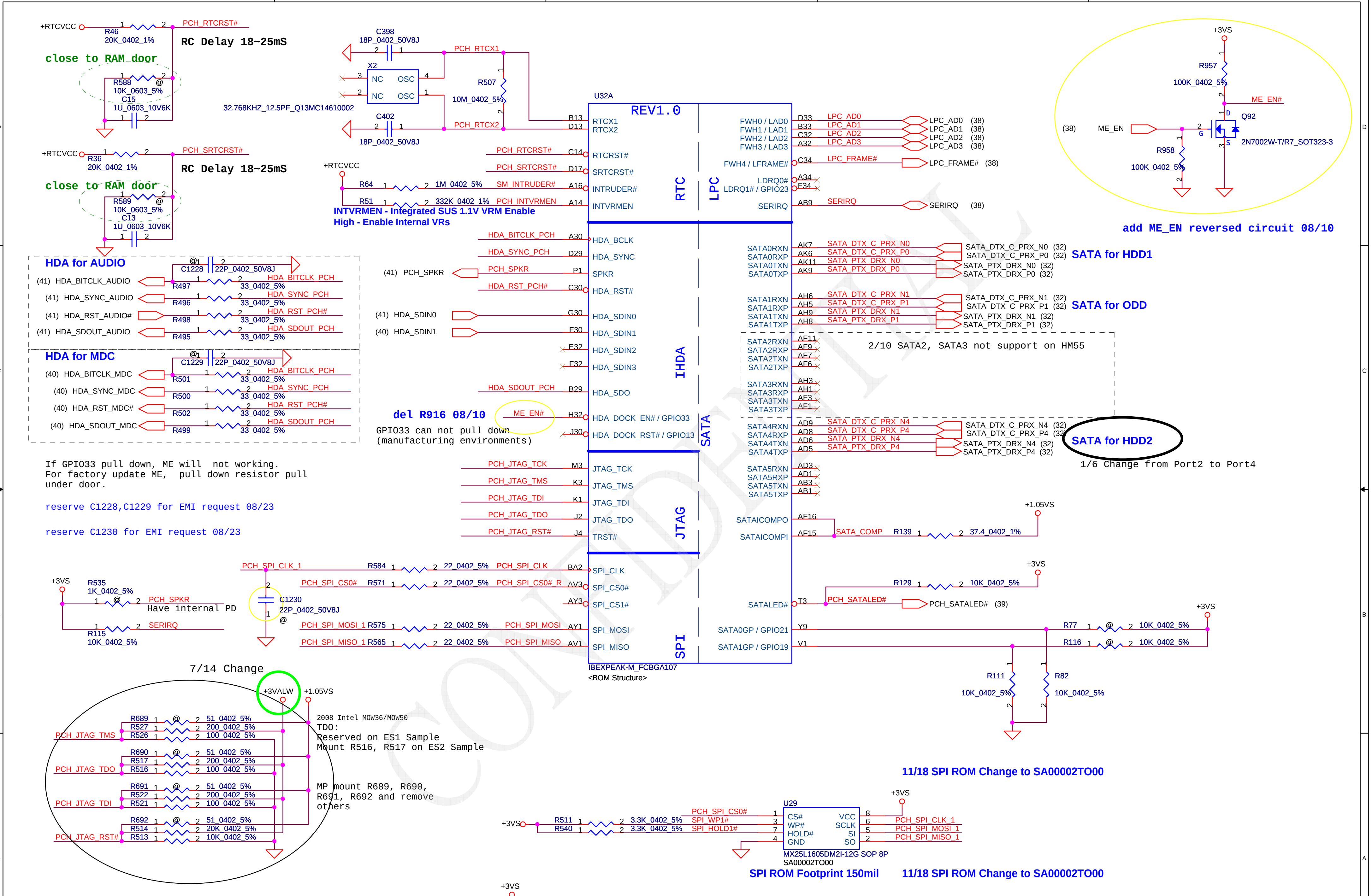

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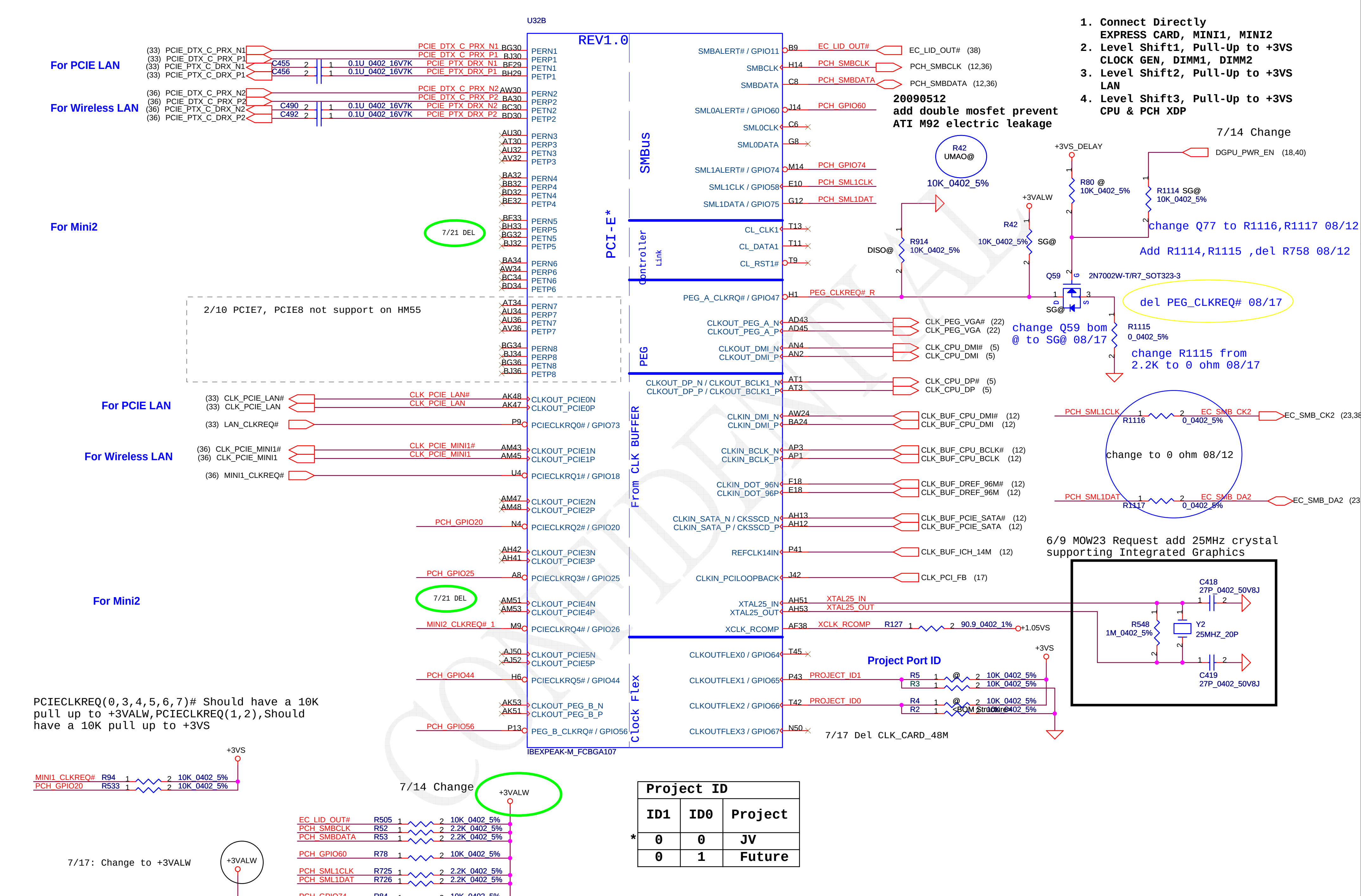

1. Connect Directly
   EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS
   CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS
   LAN
4. Level Shift3, Pull-Up to +3VS
   CPU & PCH XDP

20090512
add double mosfet prevent
ATI M92 electric leakage

Project ID		
ID1	ID0	Project
* 0	0	JV
0	1	Future

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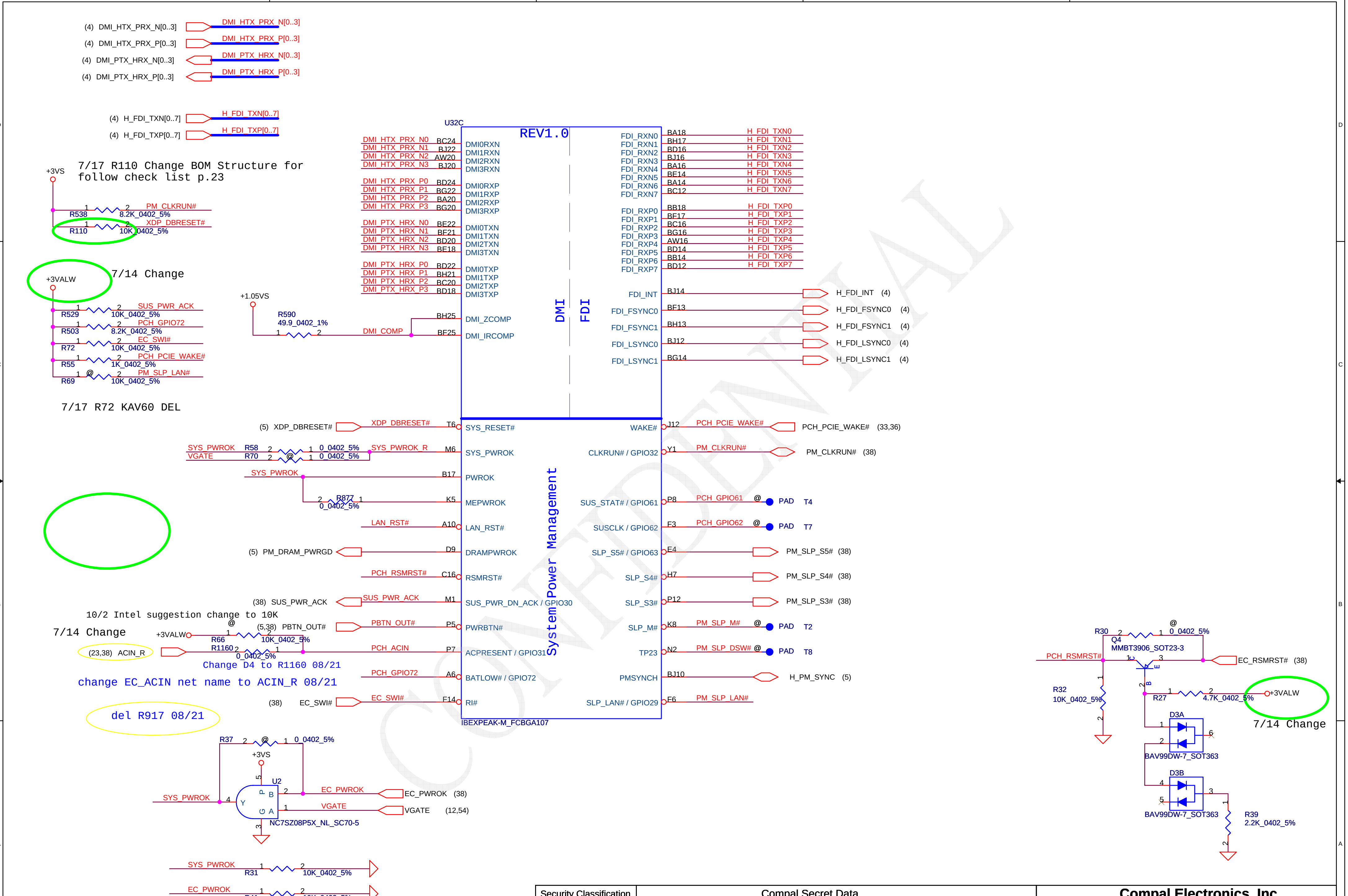

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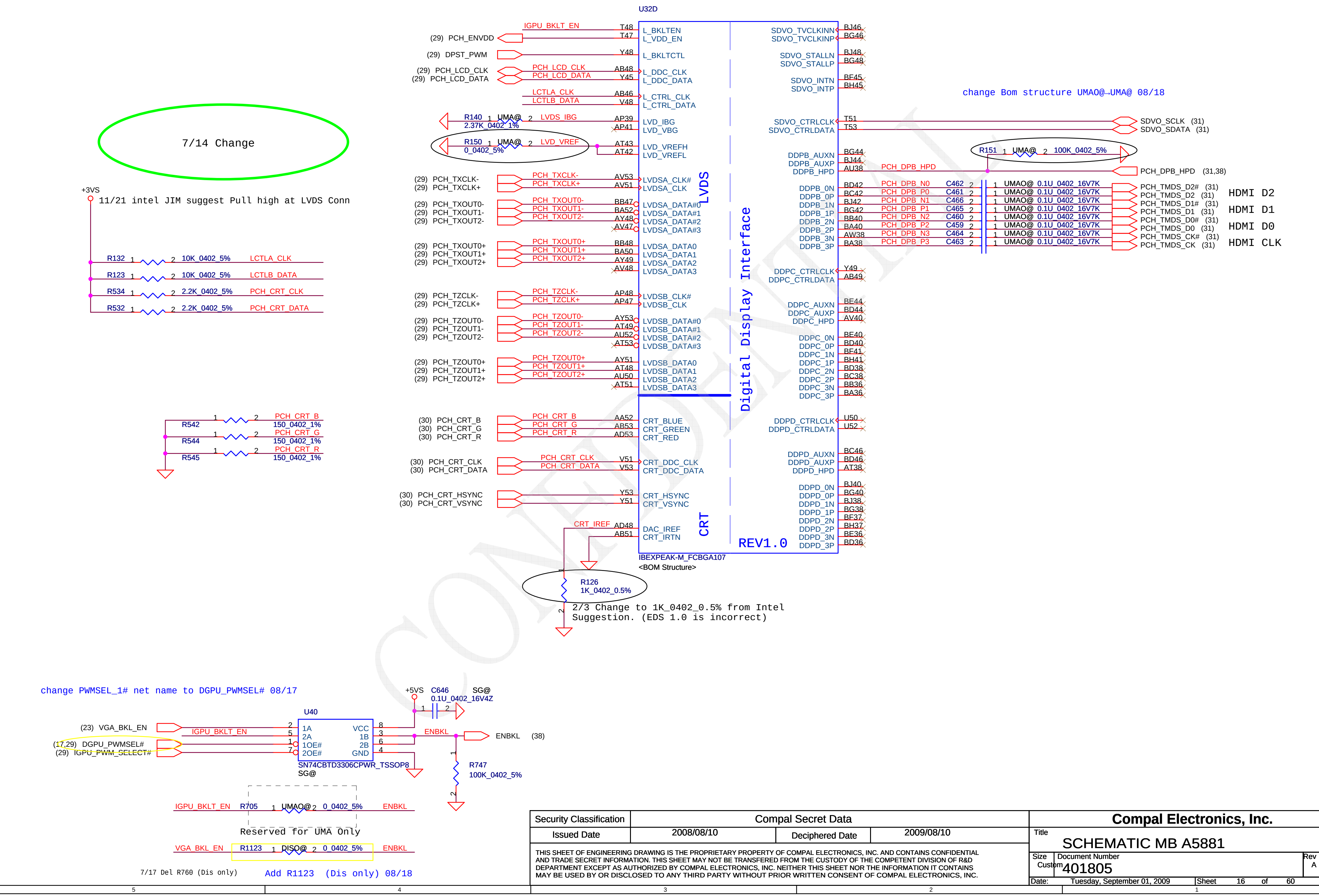

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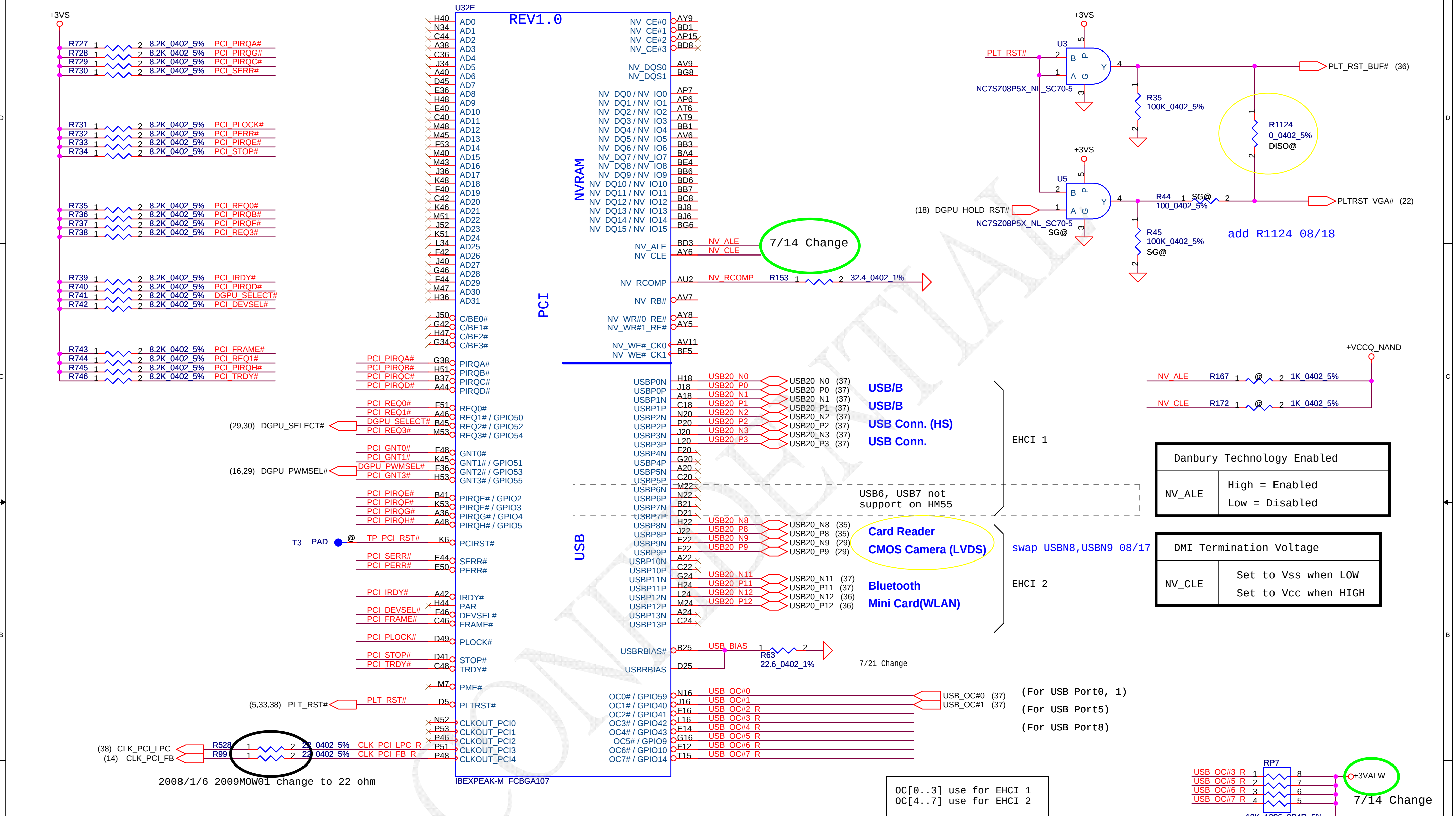

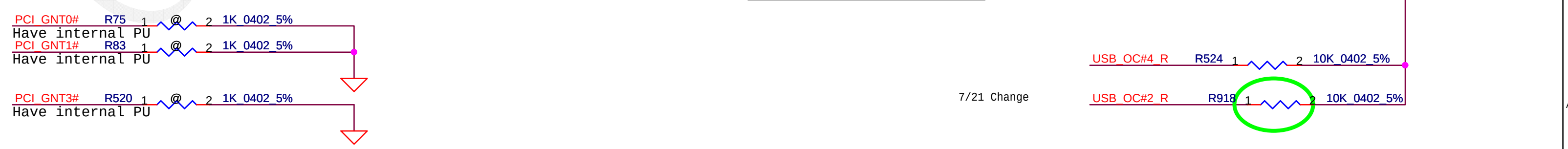

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI *

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

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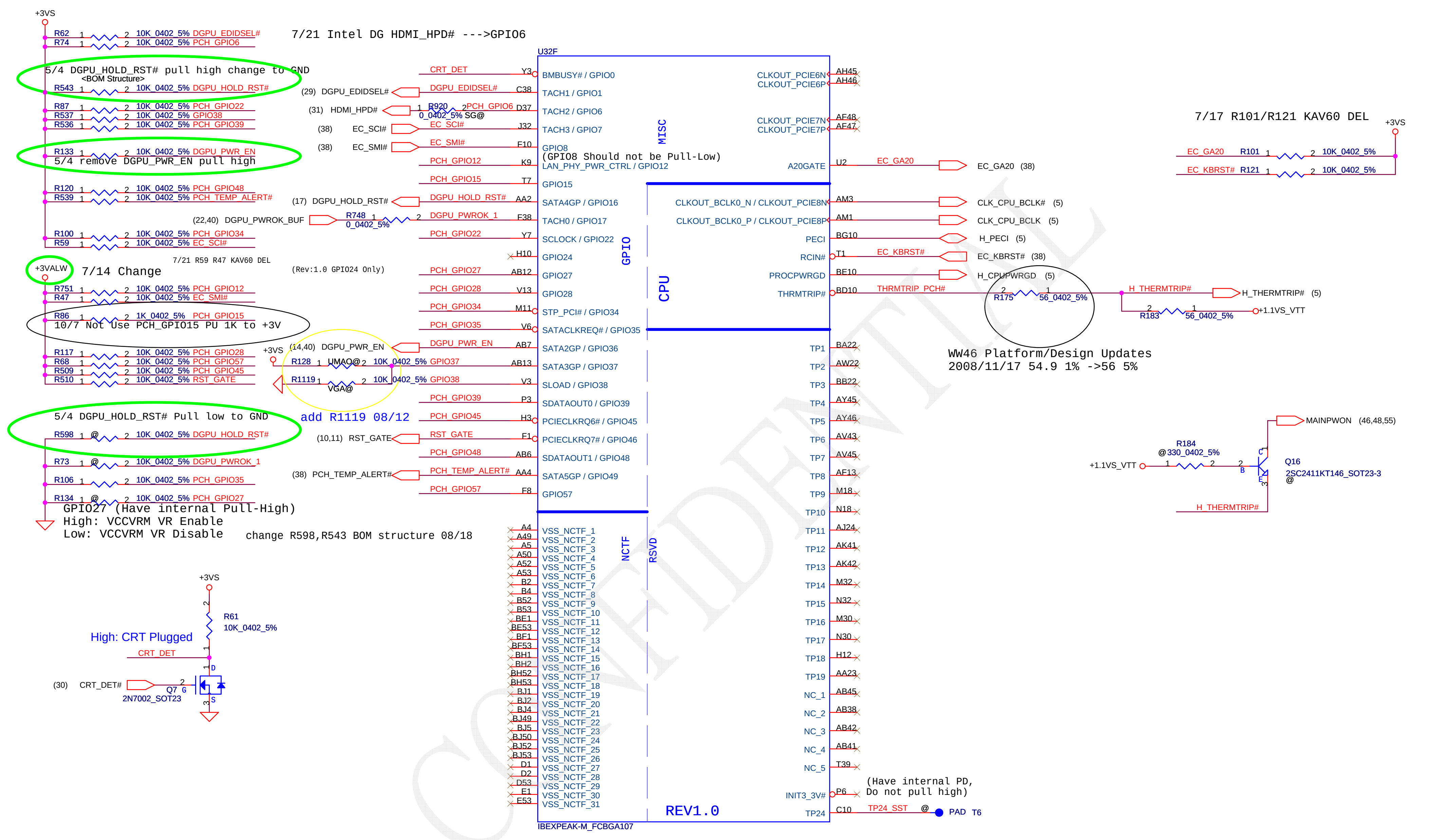

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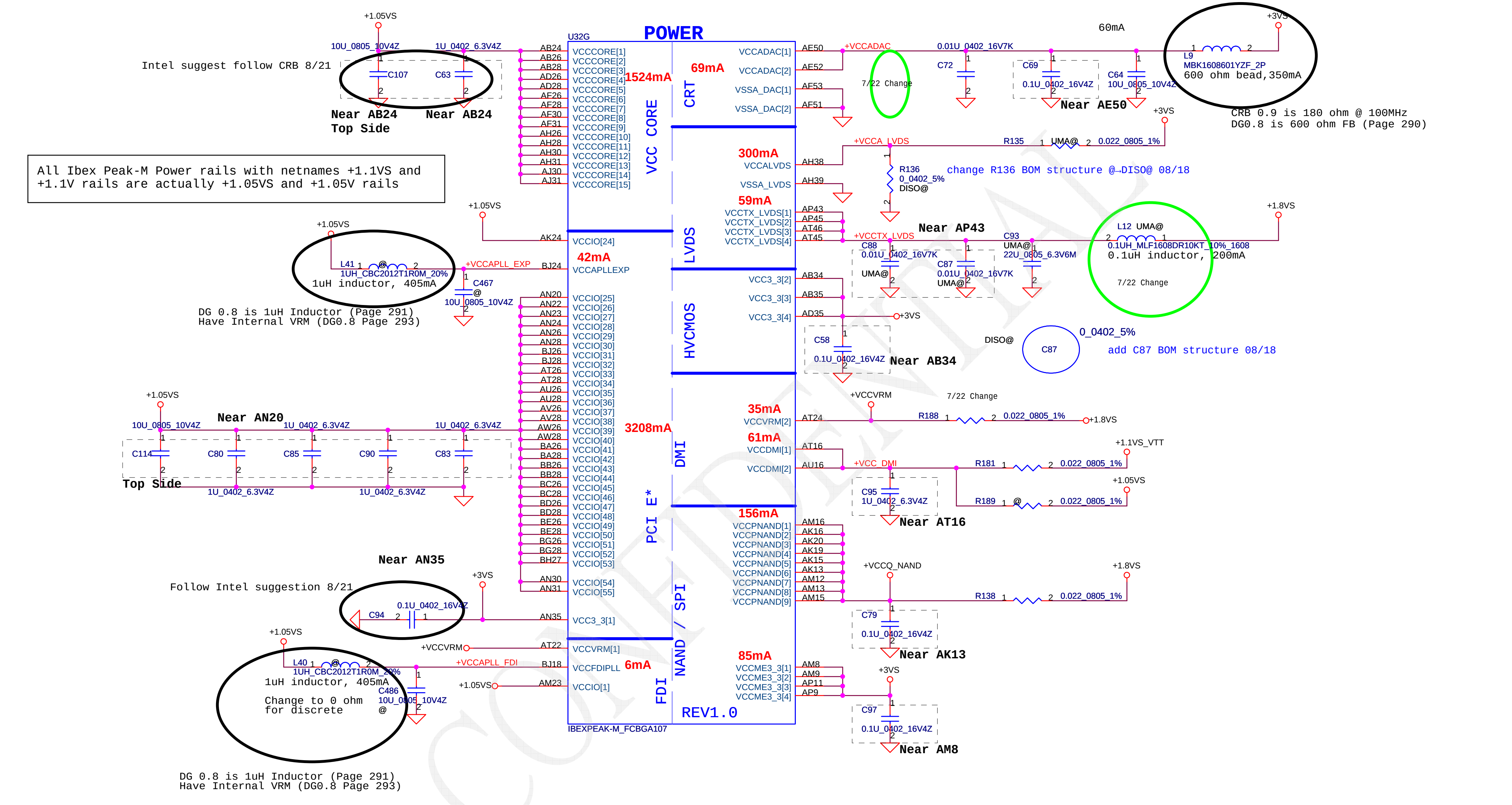

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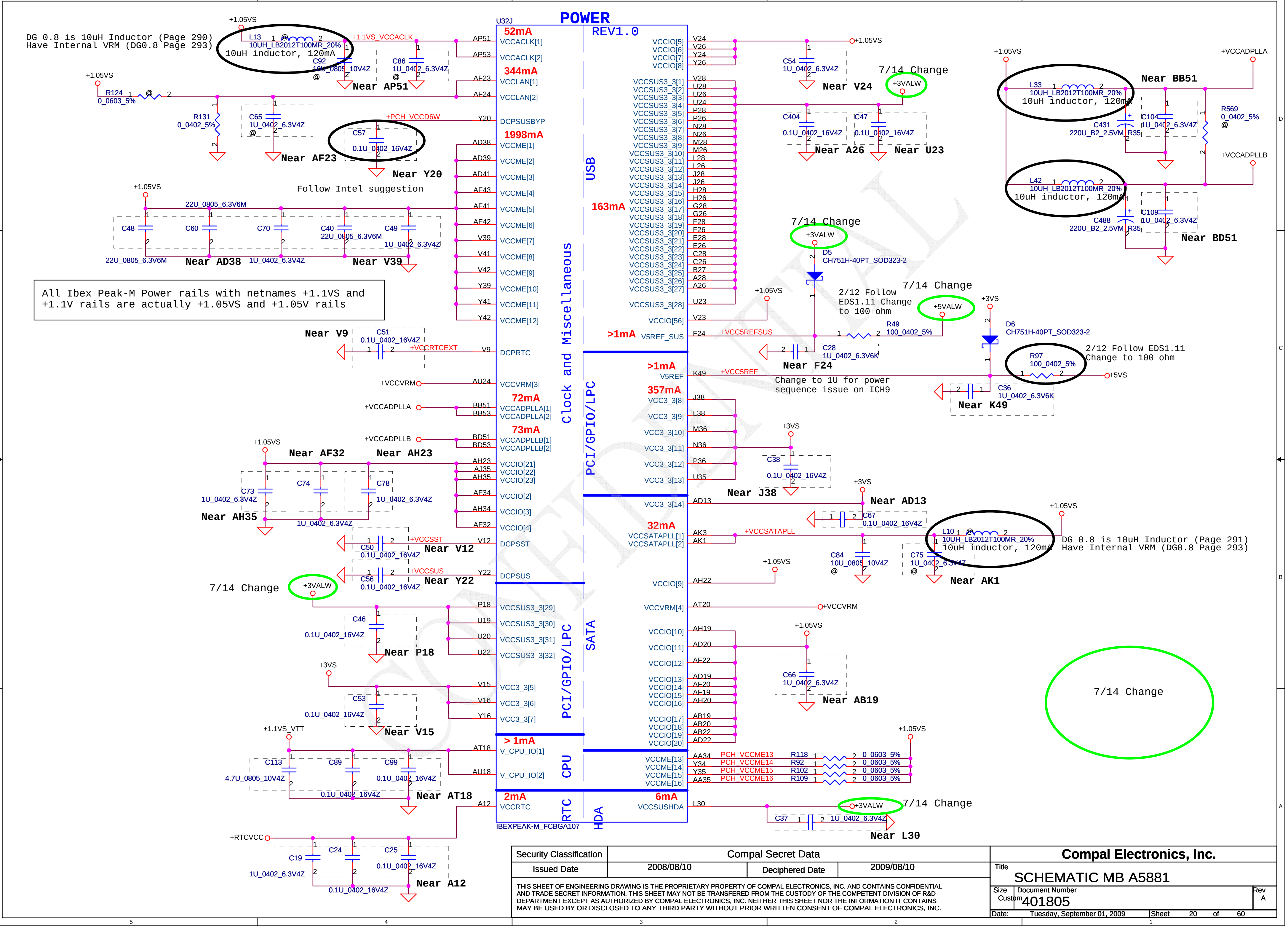

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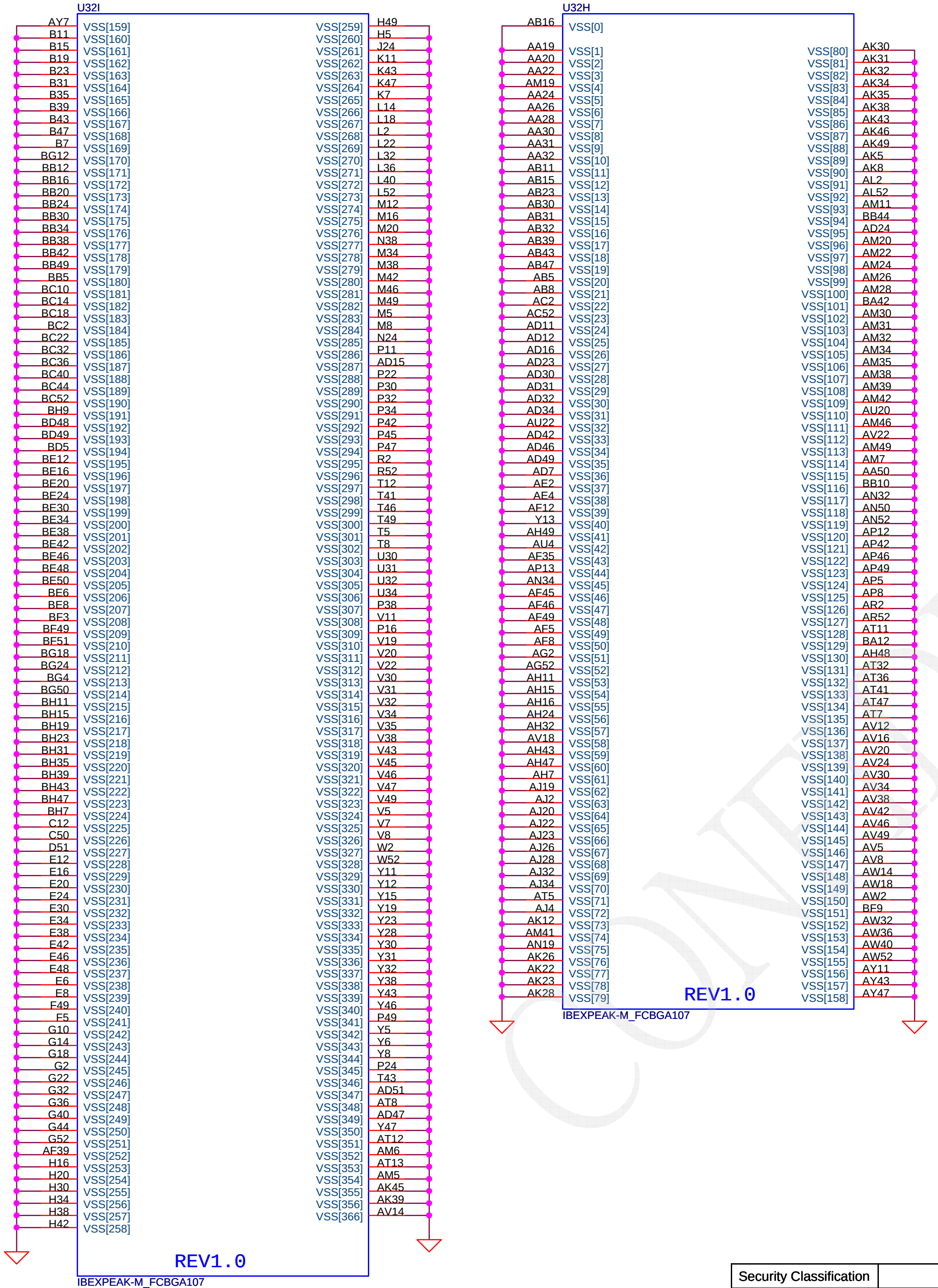

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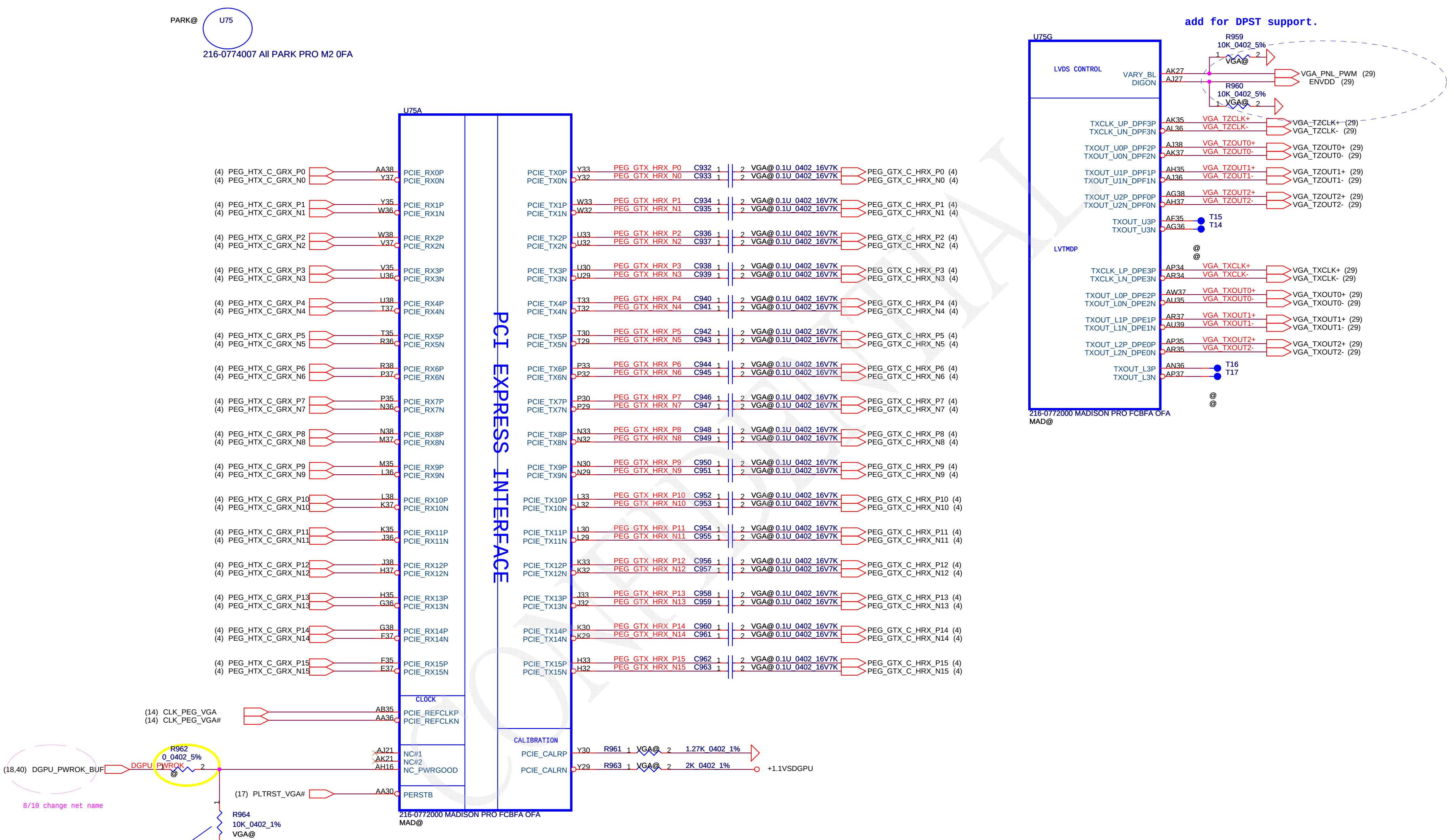

Mannhatton Only
NC in M96

M96 P/N : SA00002UQ50 (S IC 216-0729042-00 A13 M96 FCBGA962 0FA)
M92 P/N : SA00002YX10 (S IC 216-0728014 A12 M92-M2 XT FCBGA 0FA)

MADISON P/N:SA00003M300 (S IC 216-0772000 MADISON PRO FCBGA 0FA)
PARK P/N:SA00003MC00 (S IC 216-0774007 All PARK PRO M2 0FA)

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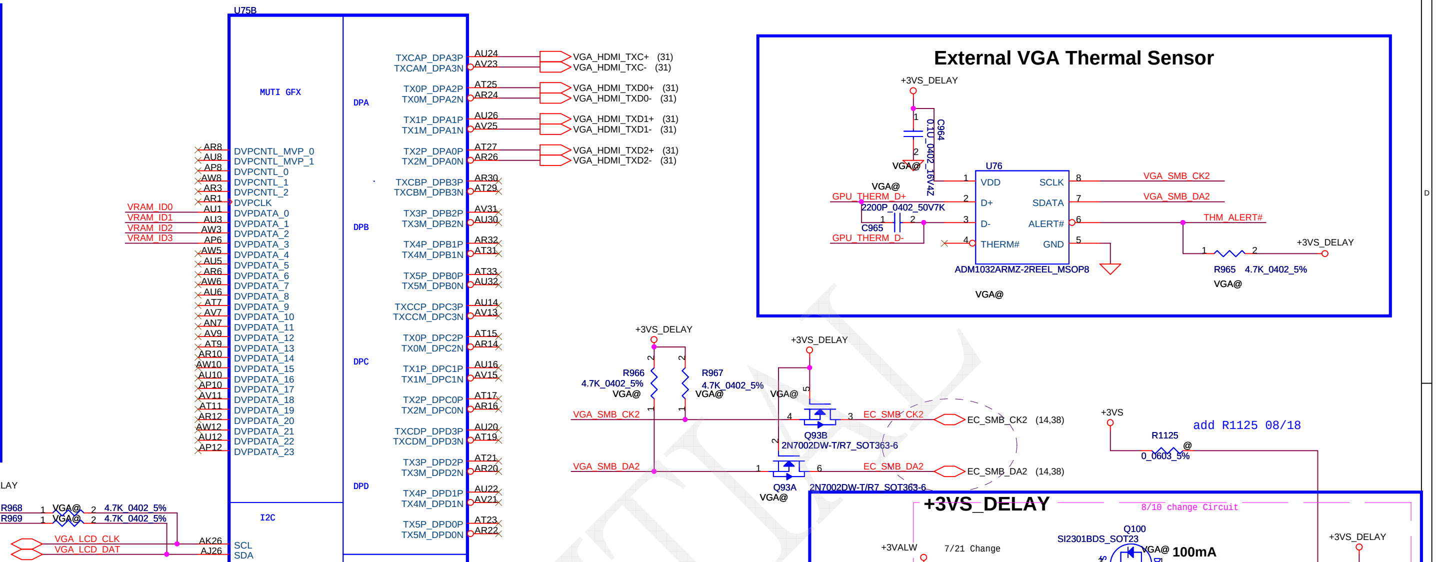
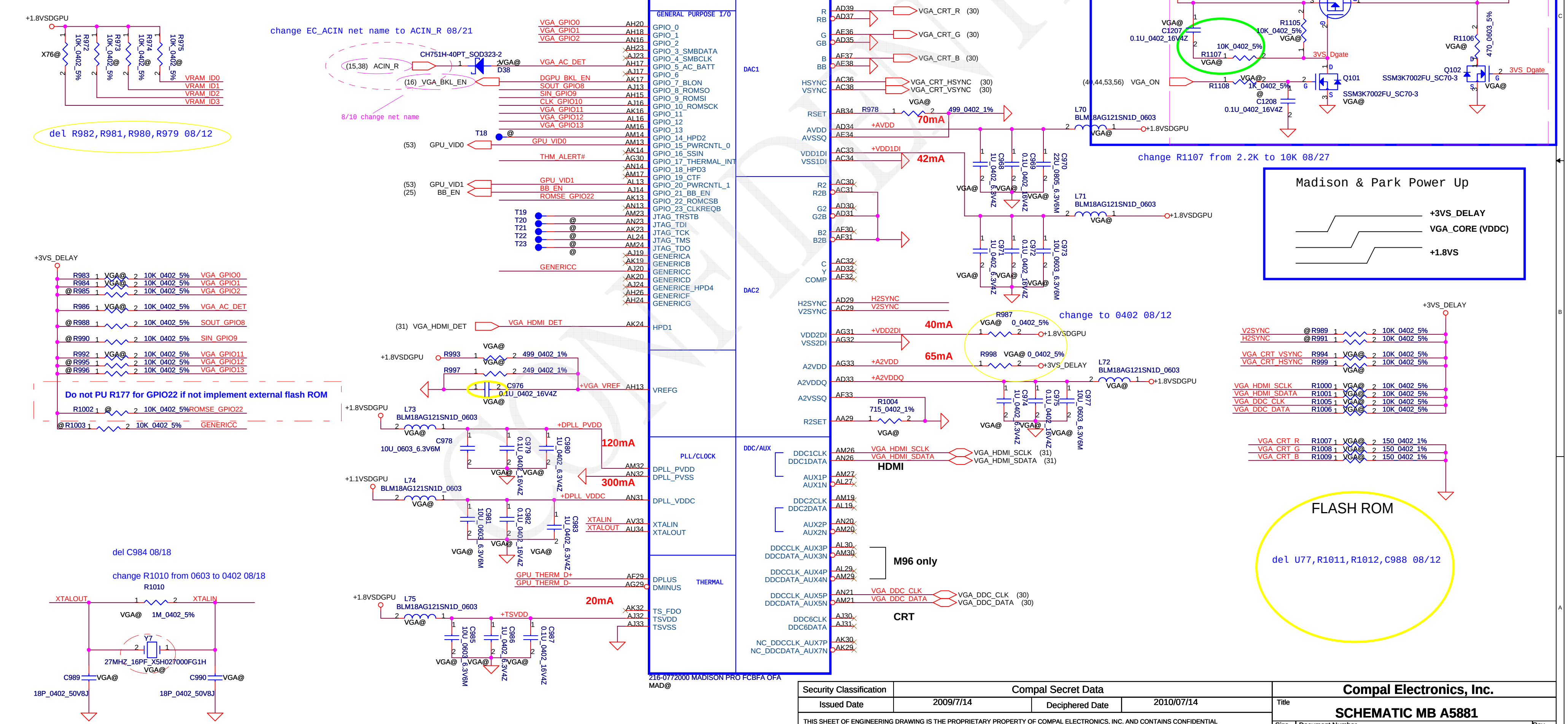
Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defalult setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF _CLK_PM_EN	GPIO22	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
CCBYPASS	GENERICC		0
SMS_EN_HARD	H2SYNC		0
VIP_DEVICE _STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

Location / VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	O	O	O	O
HYNIX	1	O	O	O





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Issued Date	2009/7/14	Deciphered Date	2010/07/14

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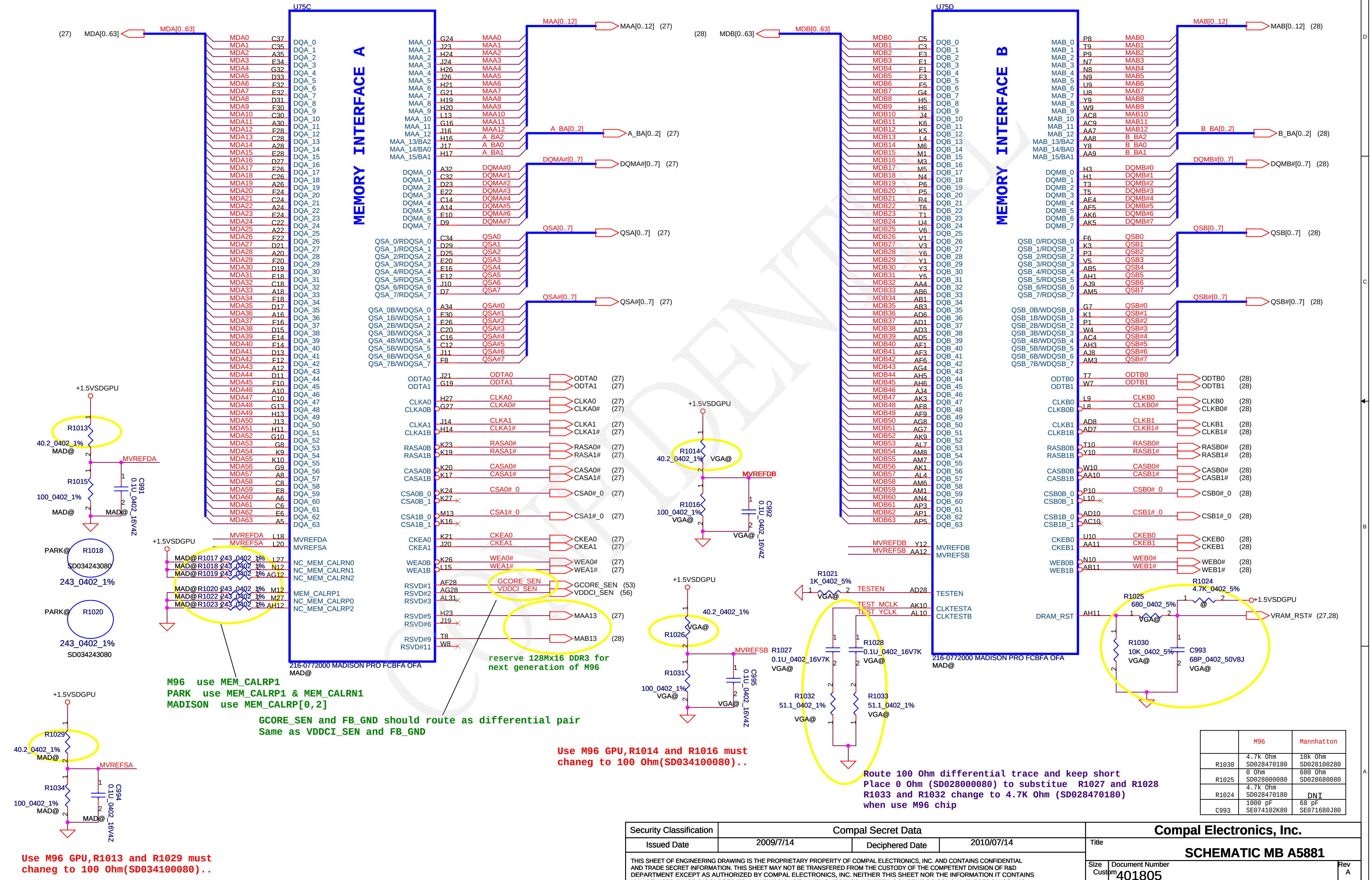
Title: **SCHEMATIC MB A5881**

Size: C | Document Number: 401805 | Rev: A



	M96	Mannhatton
R1030	4.7k Ohm SD028470180	10k Ohm SD028100280
R1025	0 Ohm SD028000080	680 Ohm SD028680080
R1024	4.7k Ohm SD028470180	DNI
C993	1000 pF SE074102K80	68 pF SE071680J80

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Issued Date	2009/7/14	Deciphered Date	2010/07/14

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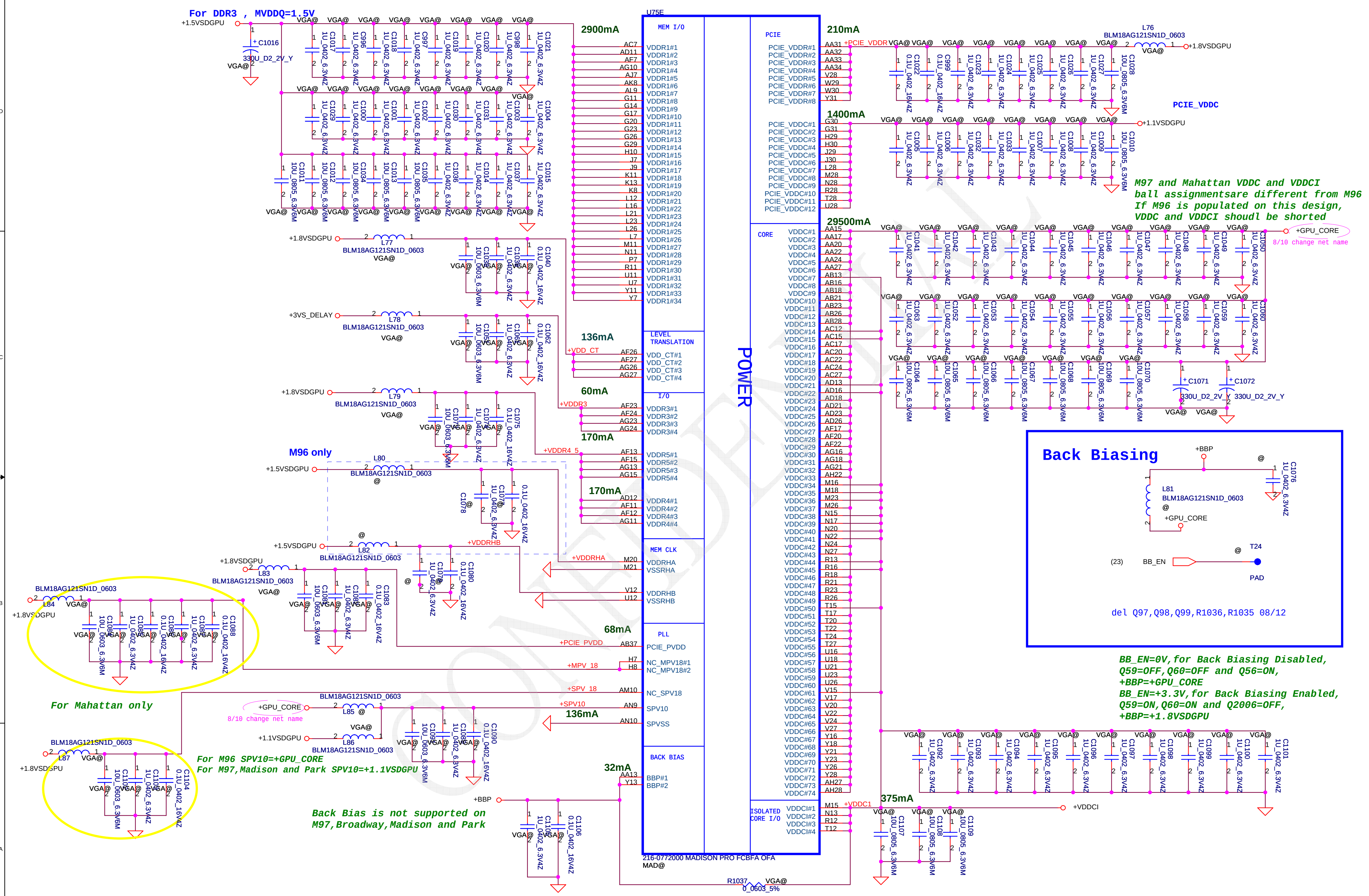
Size: Custom | Document Number: 401805 | Rev: A



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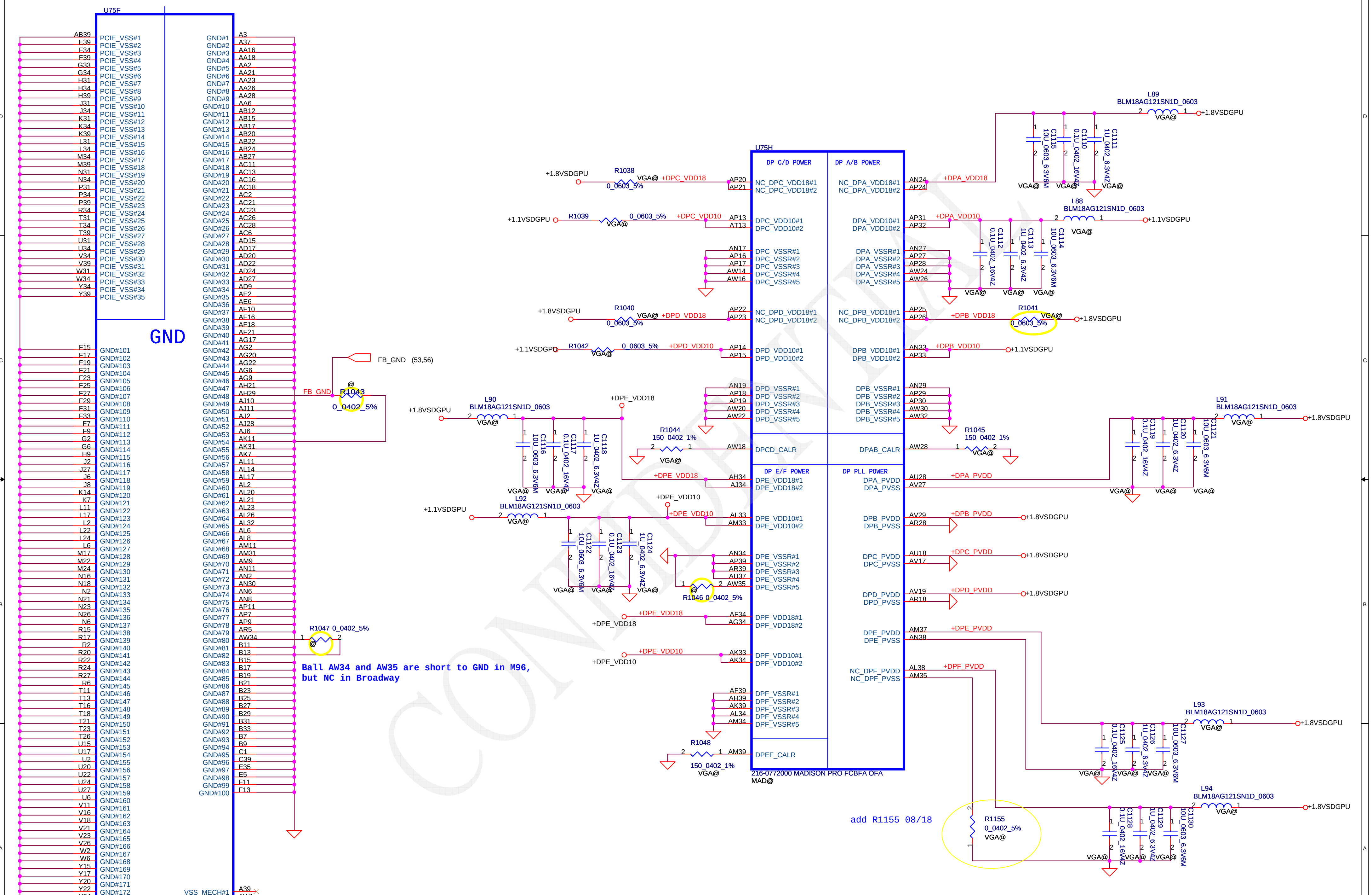

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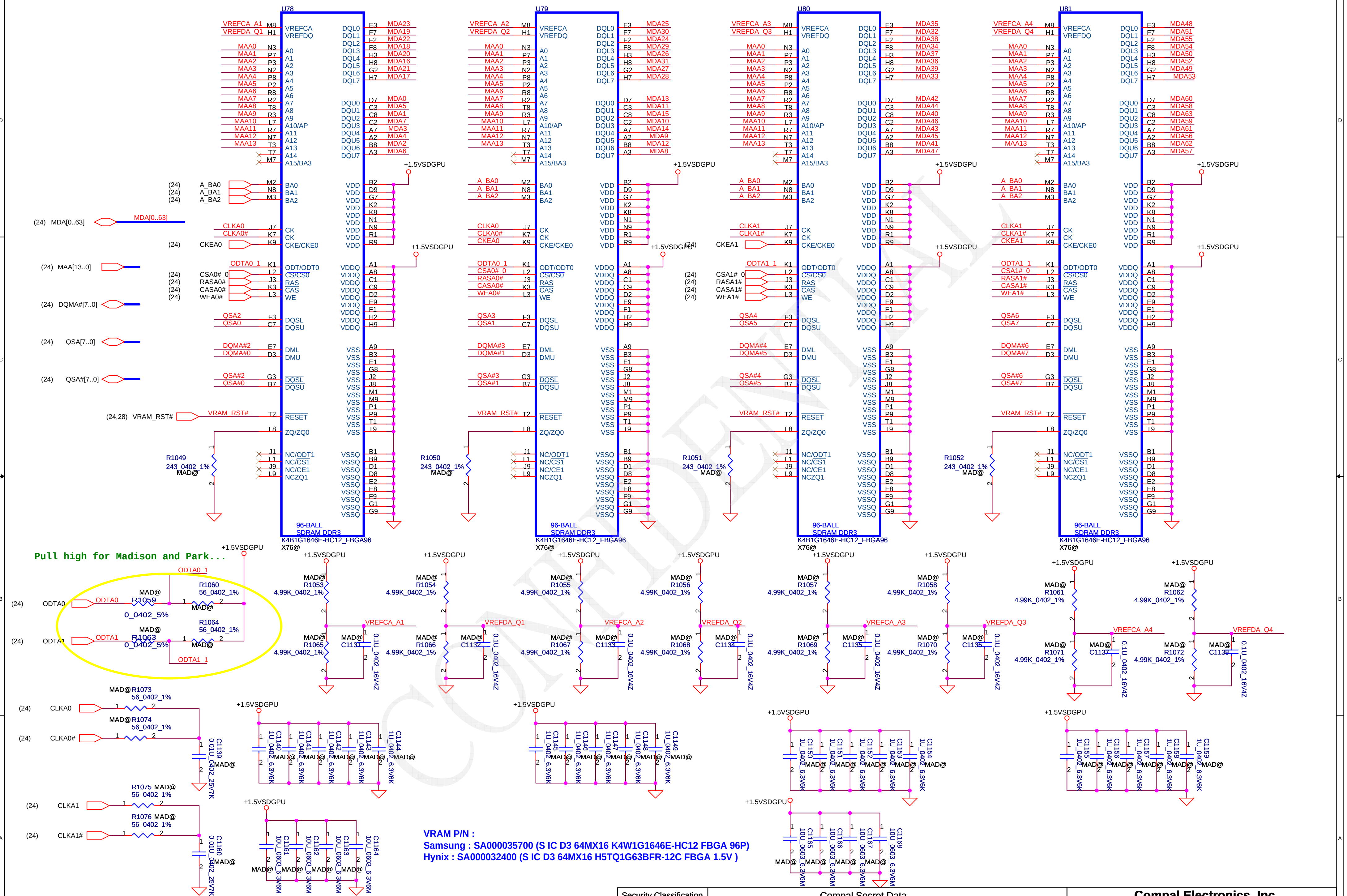
				Date: Tuesday, September 01, 2009; Sheet 26 of 60



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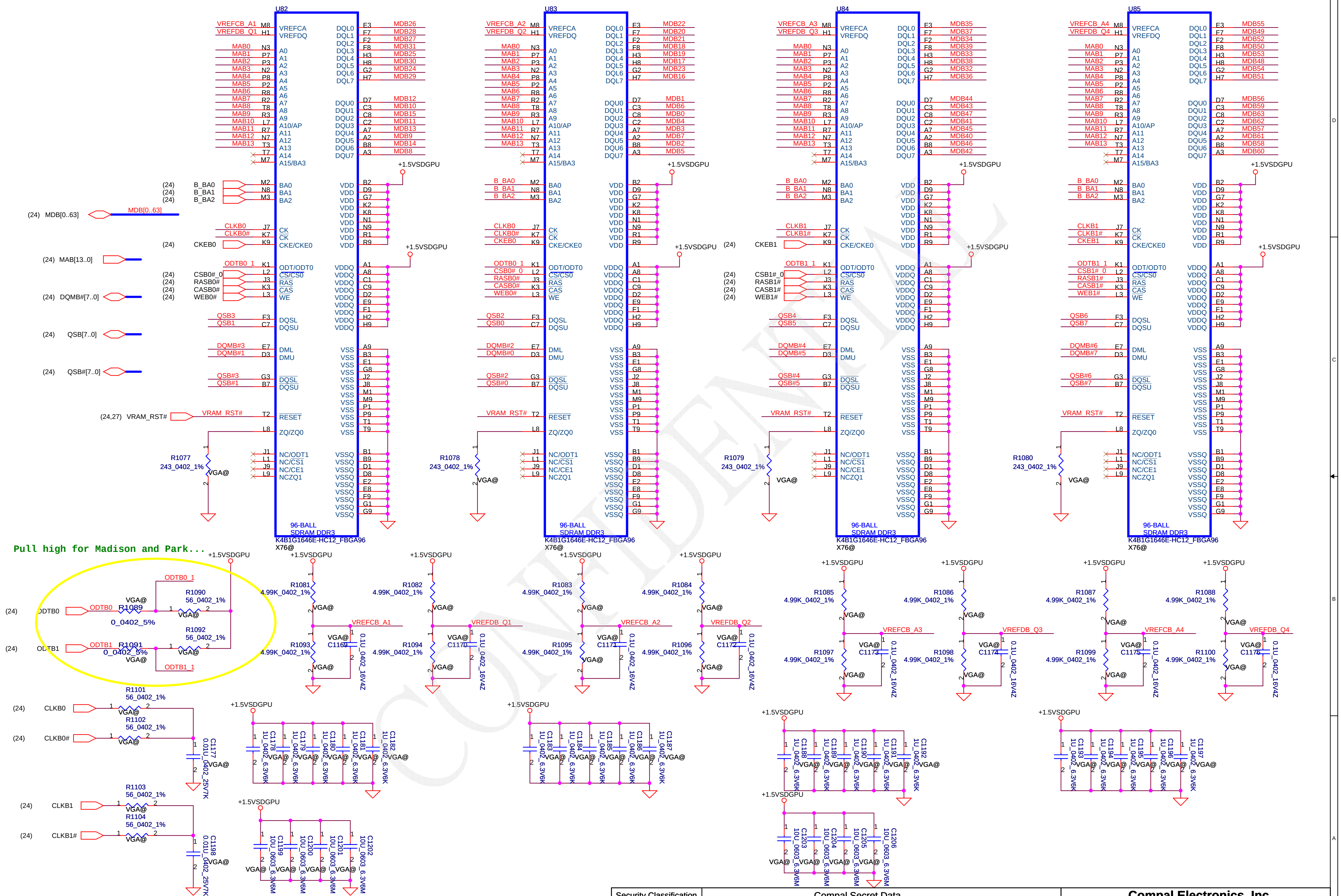

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Title

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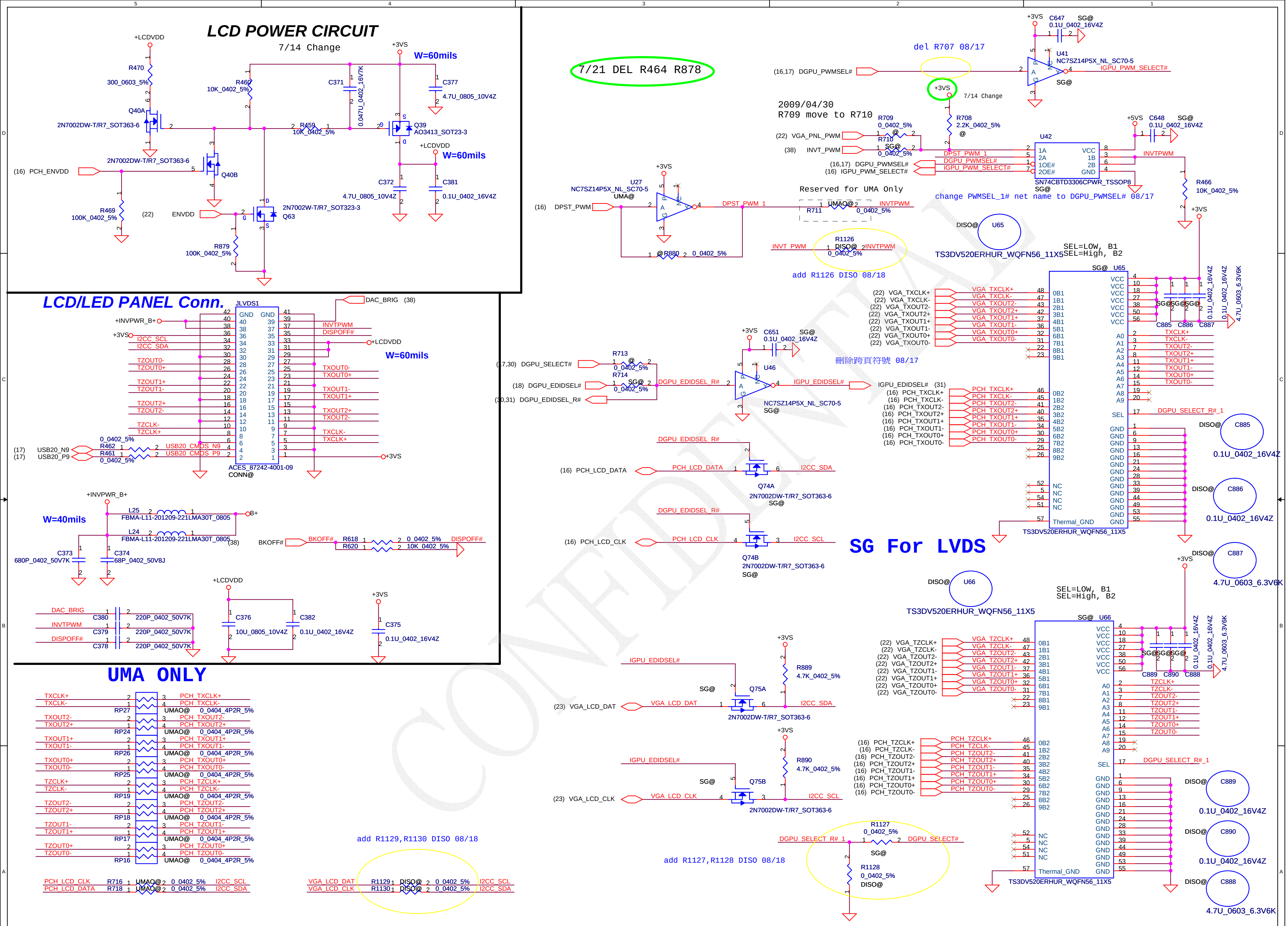

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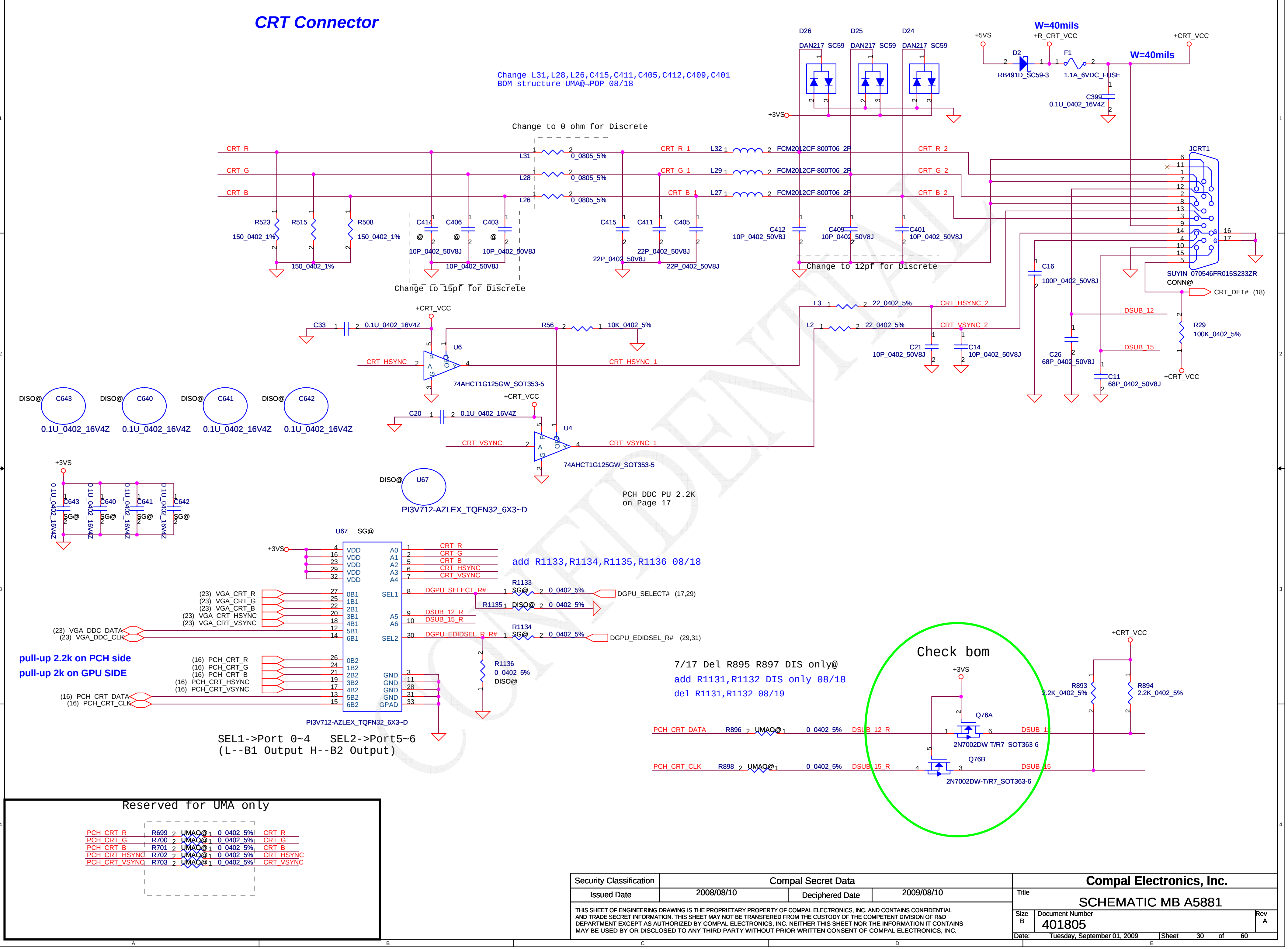
CRT Connector



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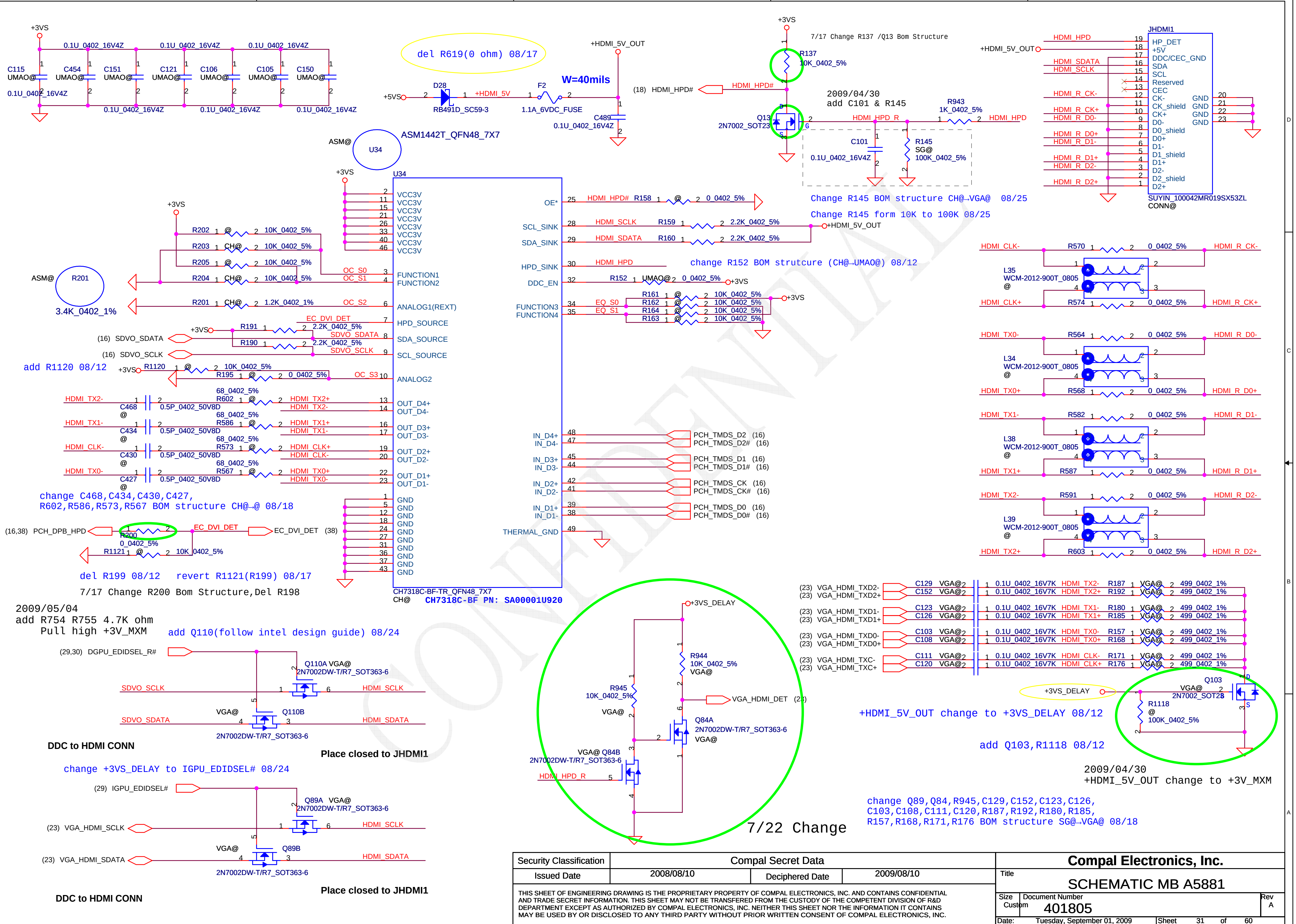

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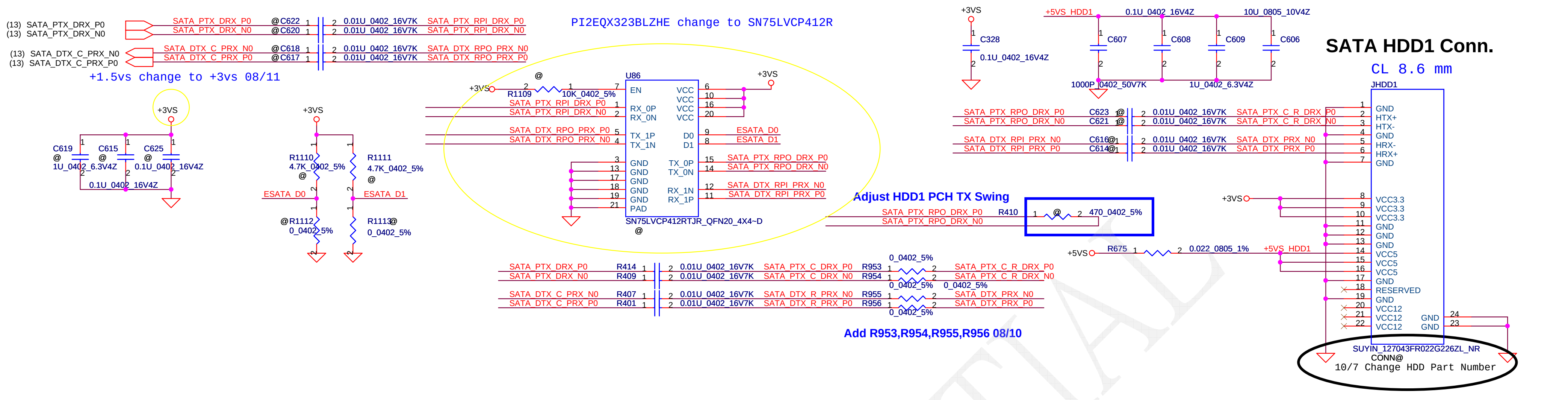
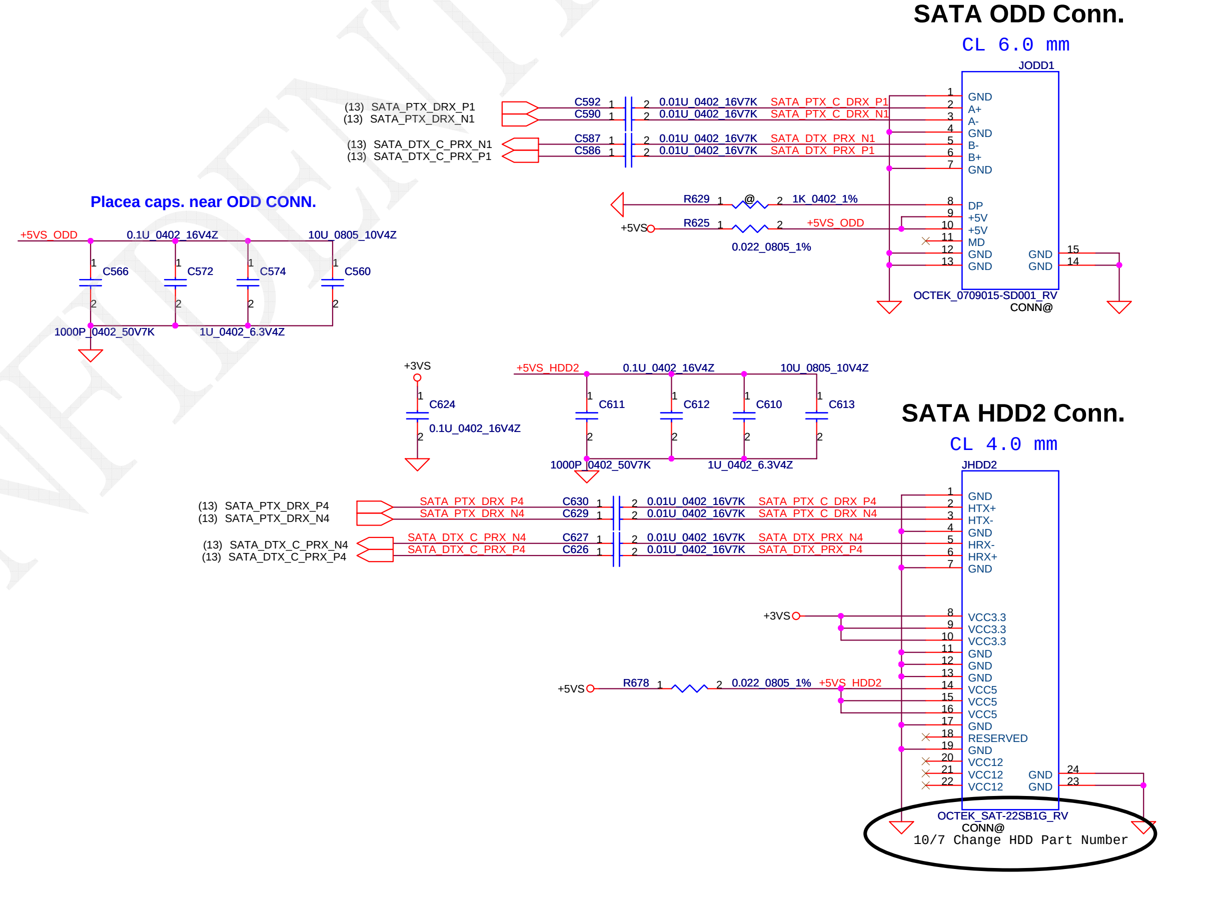


x_EQ	Compliance Channel @ 1.5 GHz
0	1.5dB ± 1.0dB
1	5.5dB ± 1.0dB

x_EM	Compliance Channel @ 1.5 GHz
0	0dB
1	-3.5dB



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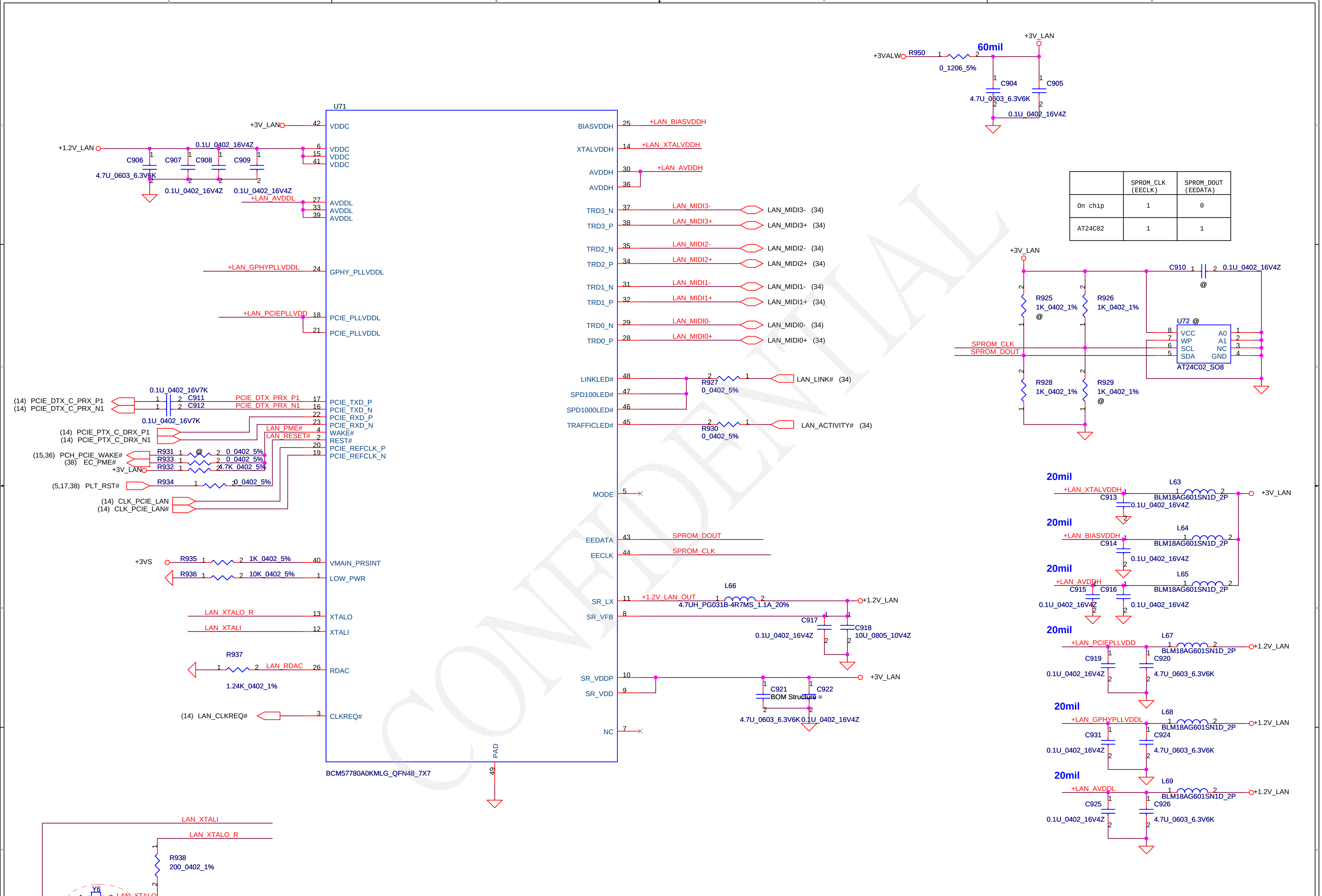

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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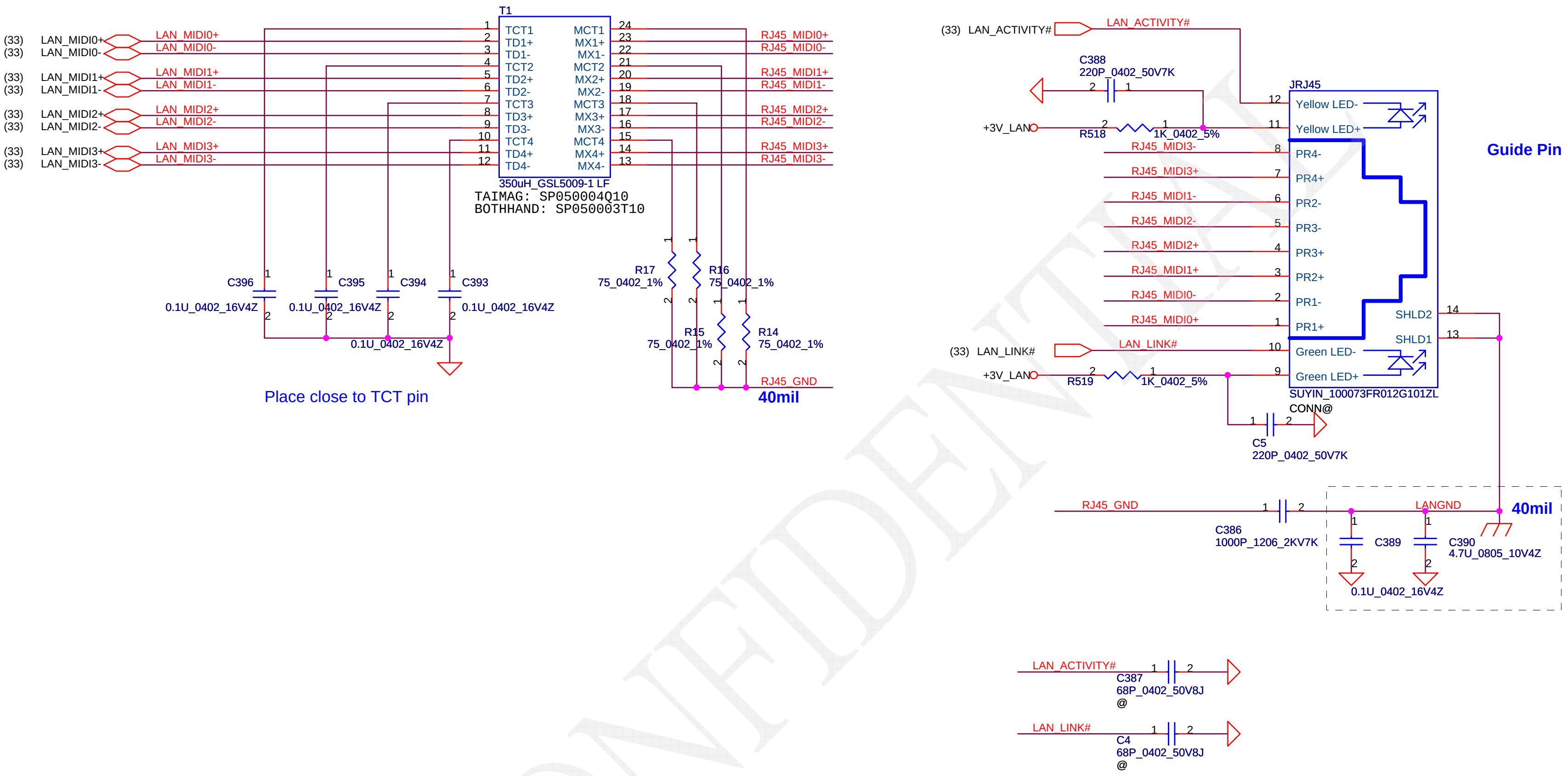

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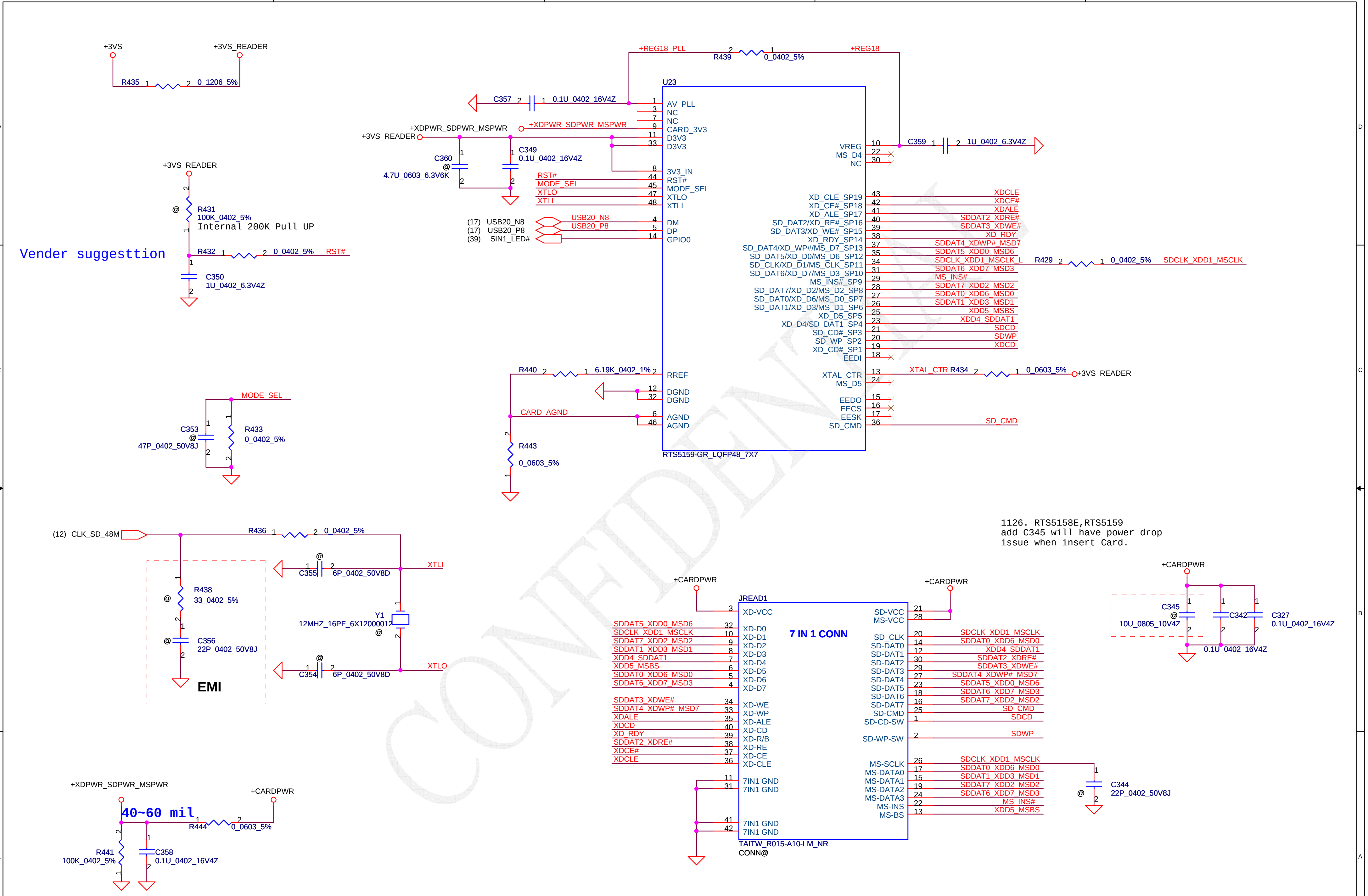

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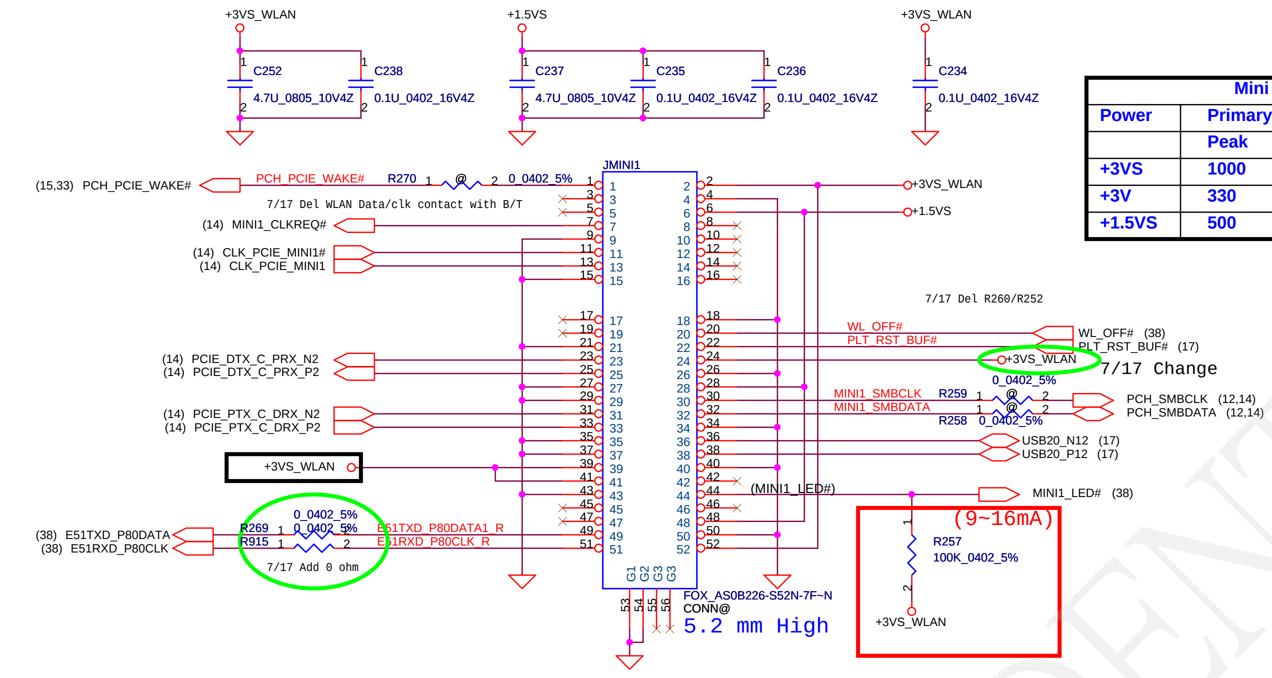
For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
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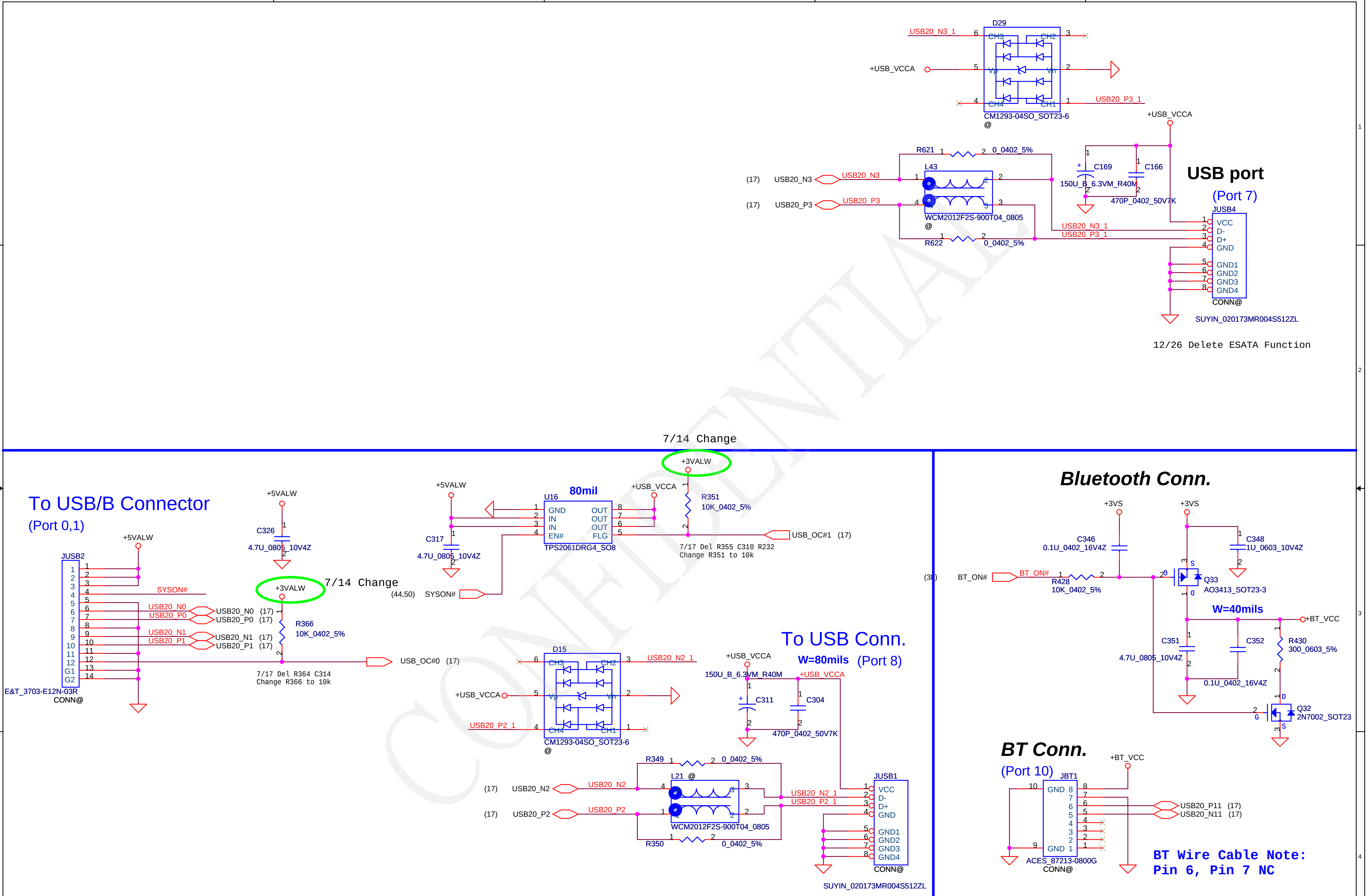

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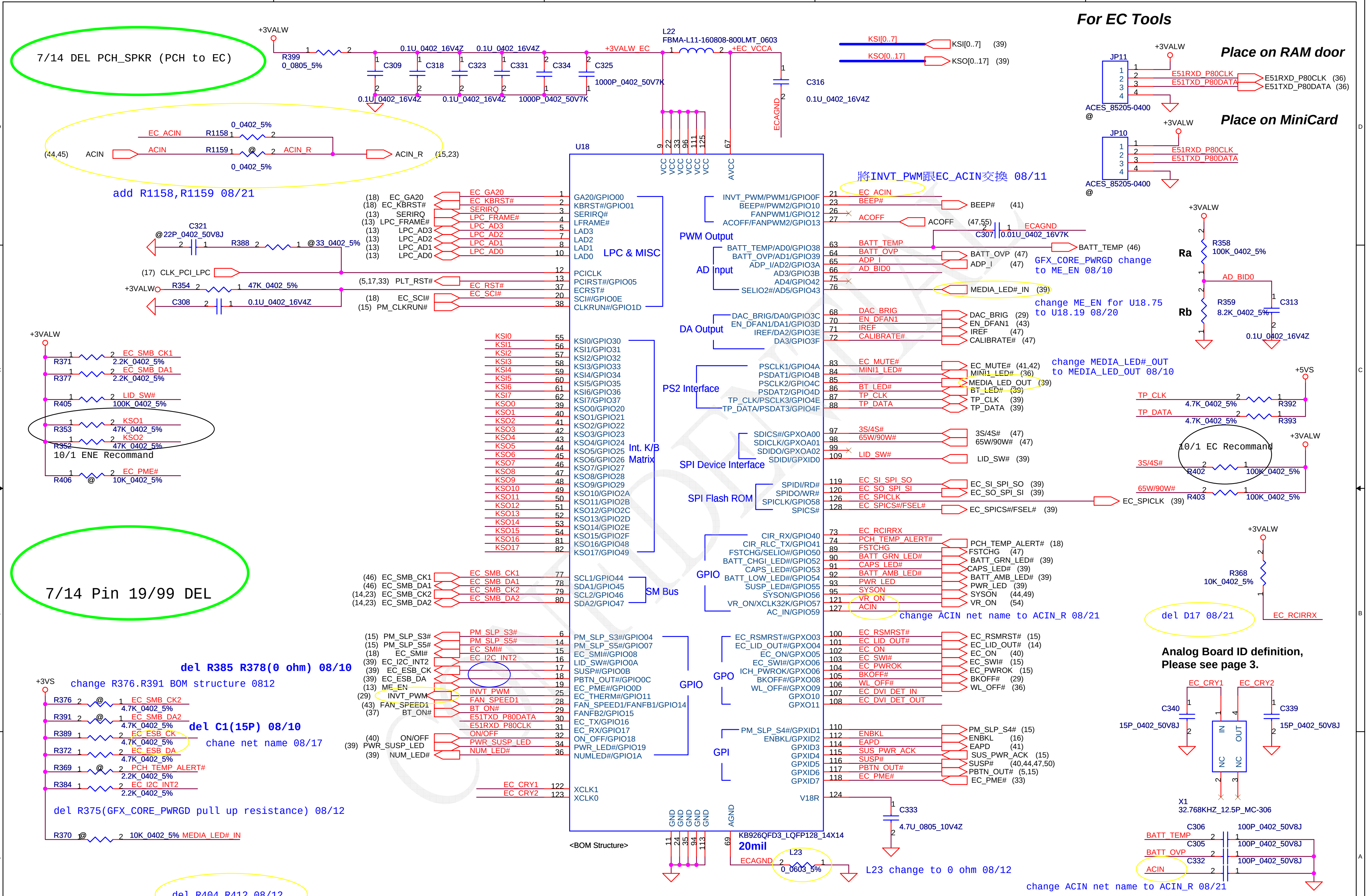

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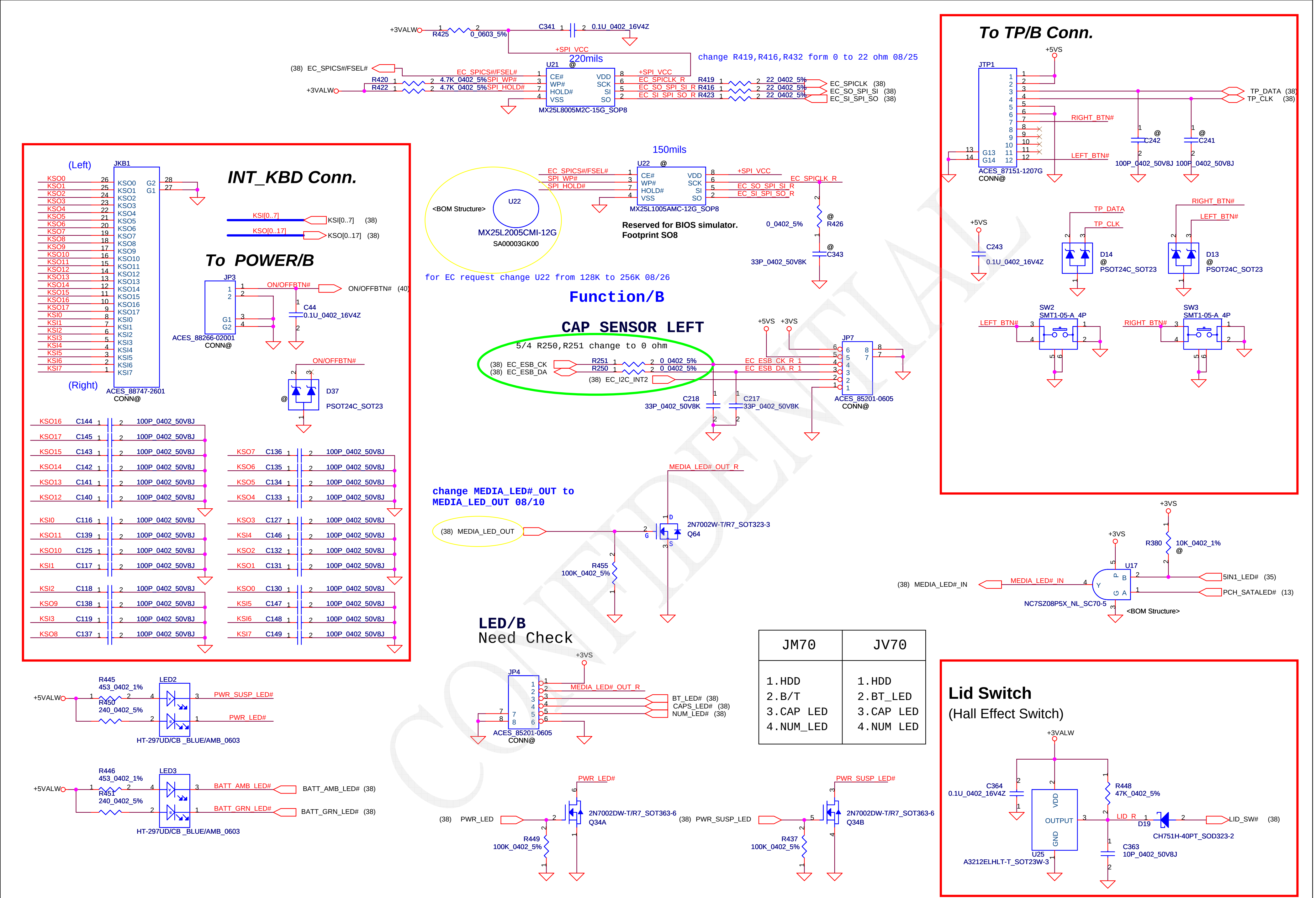

JM70	JV70
1.HDD 2.B/T 3.CAP LED 4.NUM_LED	1.HDD 2.BT_LED 3.CAP LED 4.NUM LED

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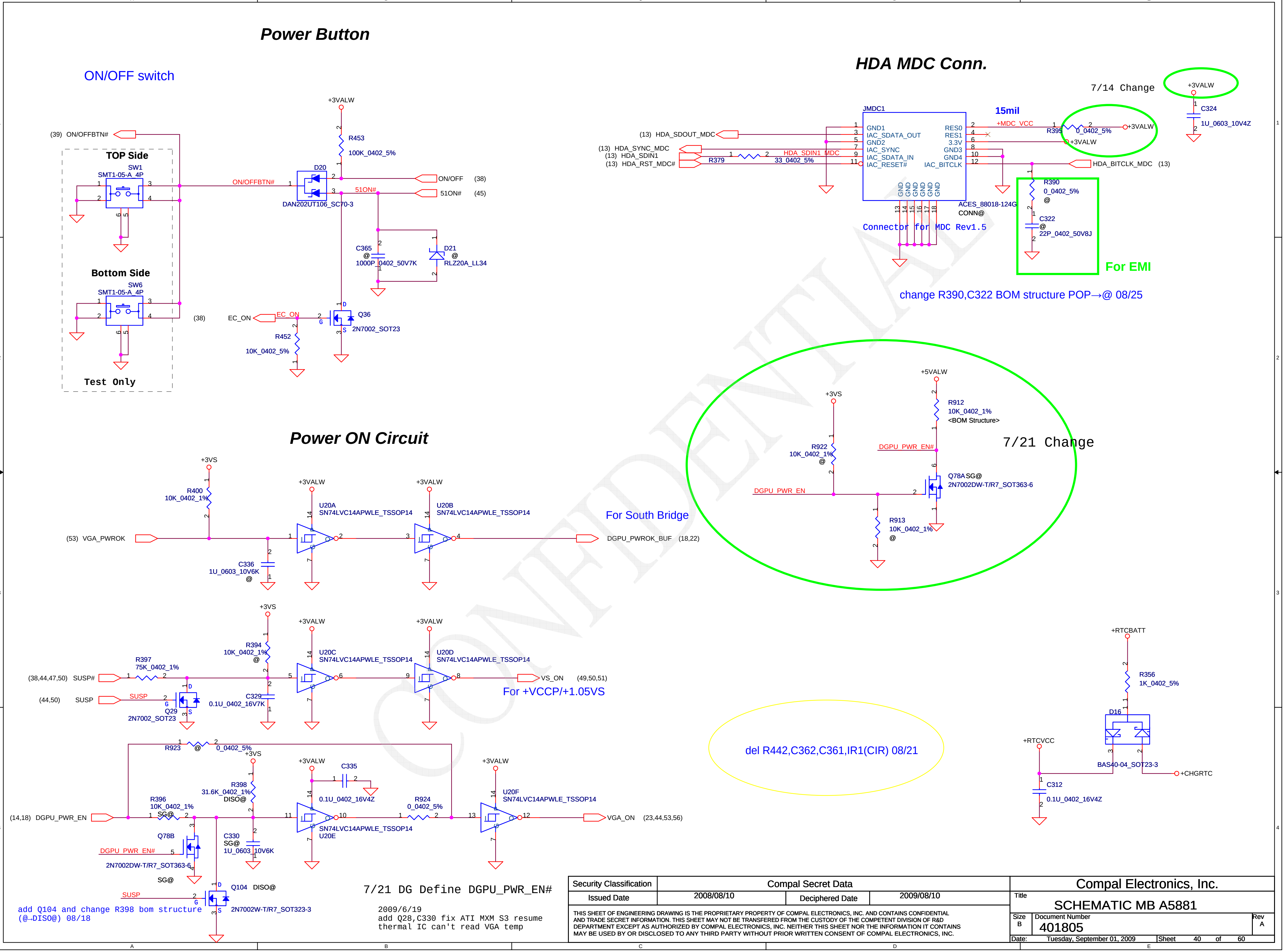

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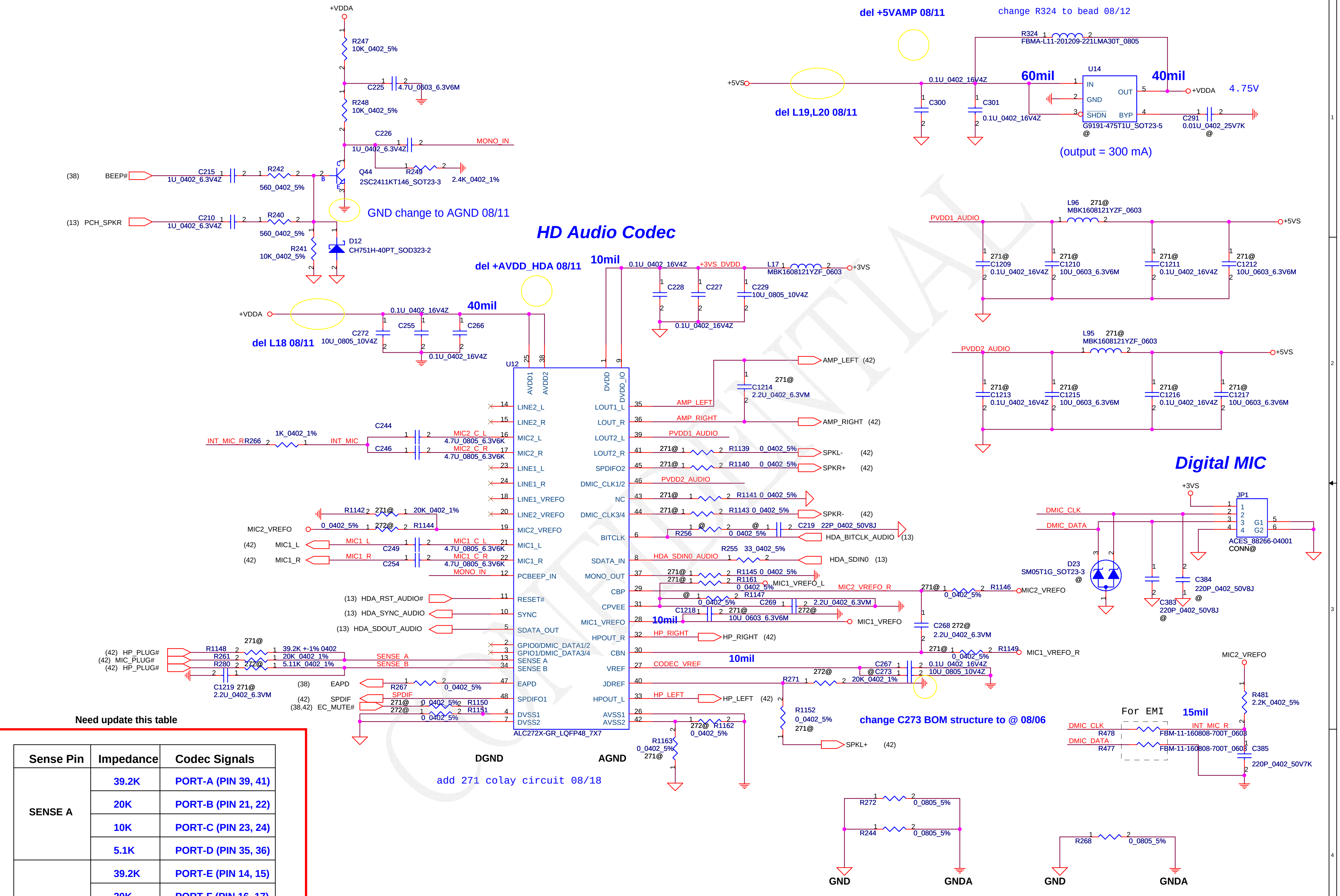
				Date: Tuesday, September 01, 2009; Sheet 40 of 60



Need update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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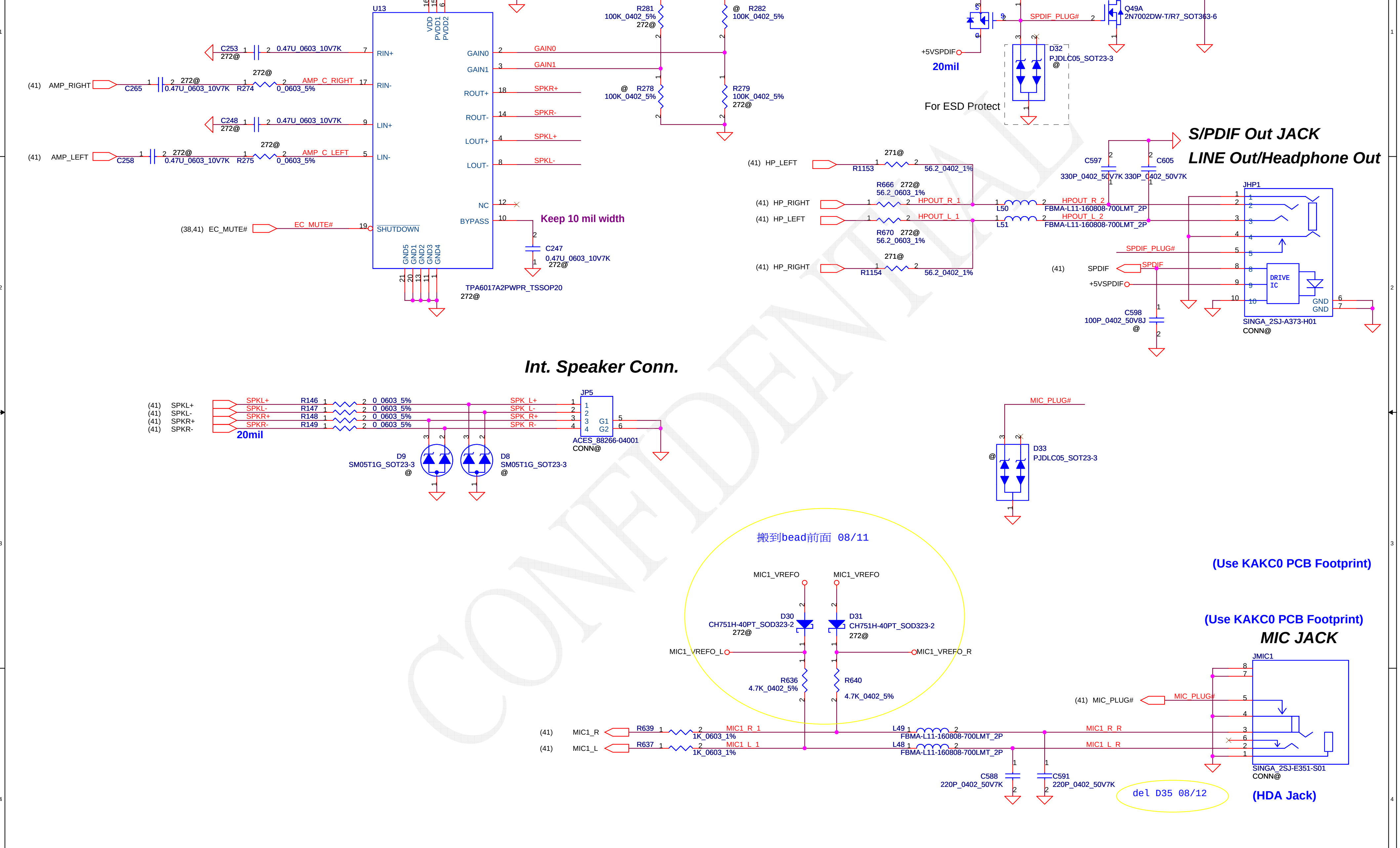
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



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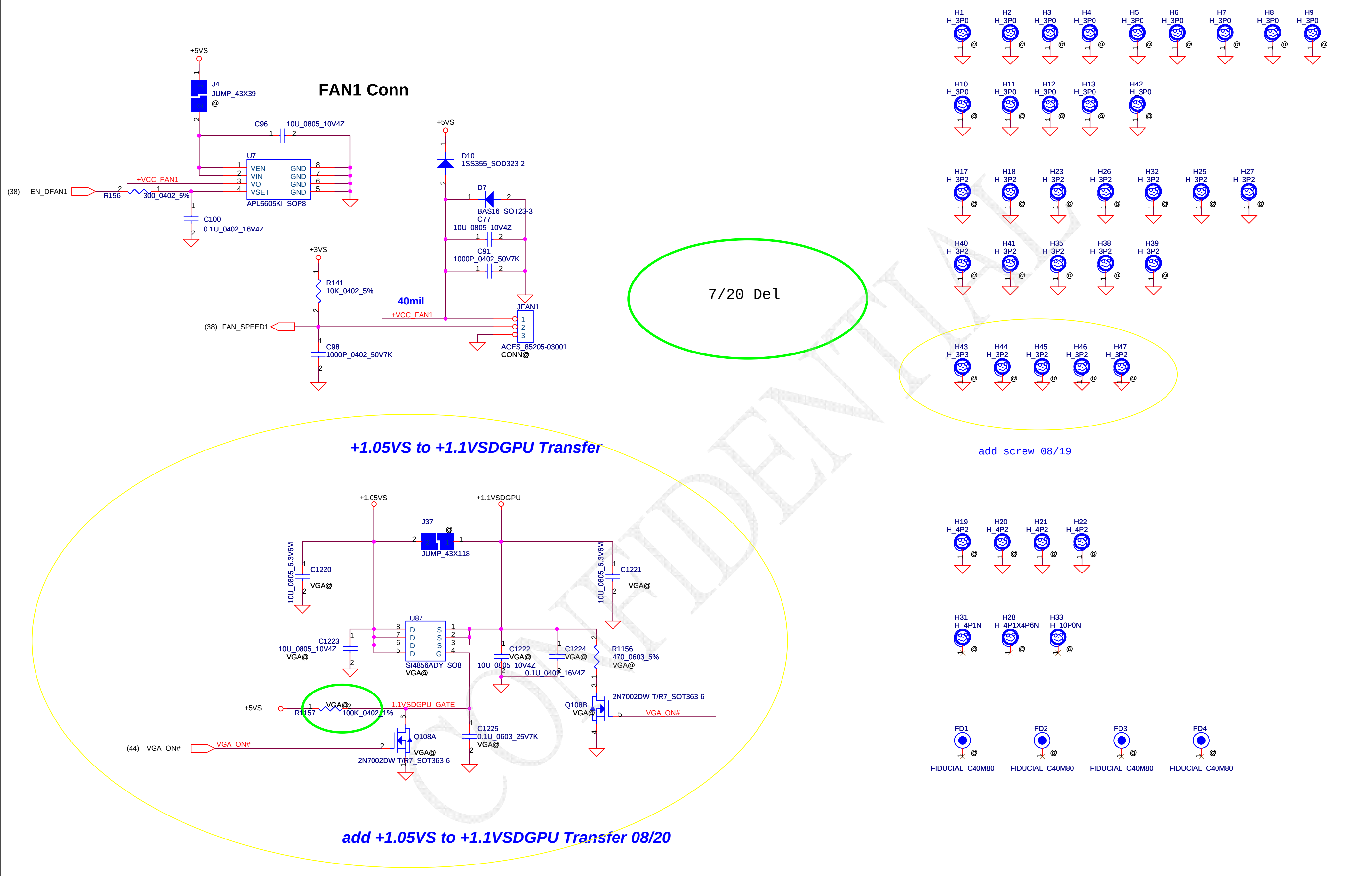

change BOM structure @→VGA@ 08/25

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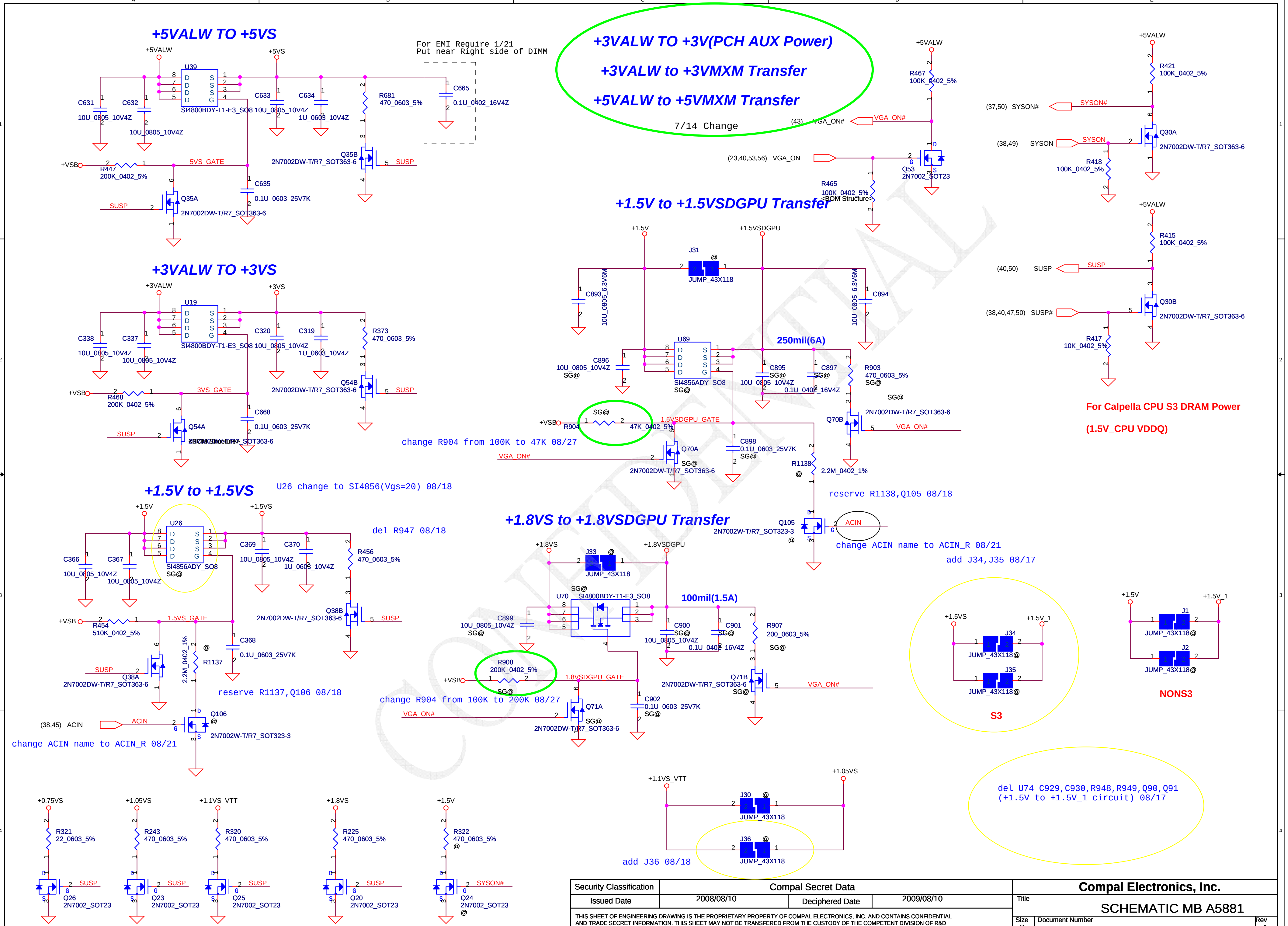
				Date: Tuesday, September 01, 2009; Sheet 43 of 60



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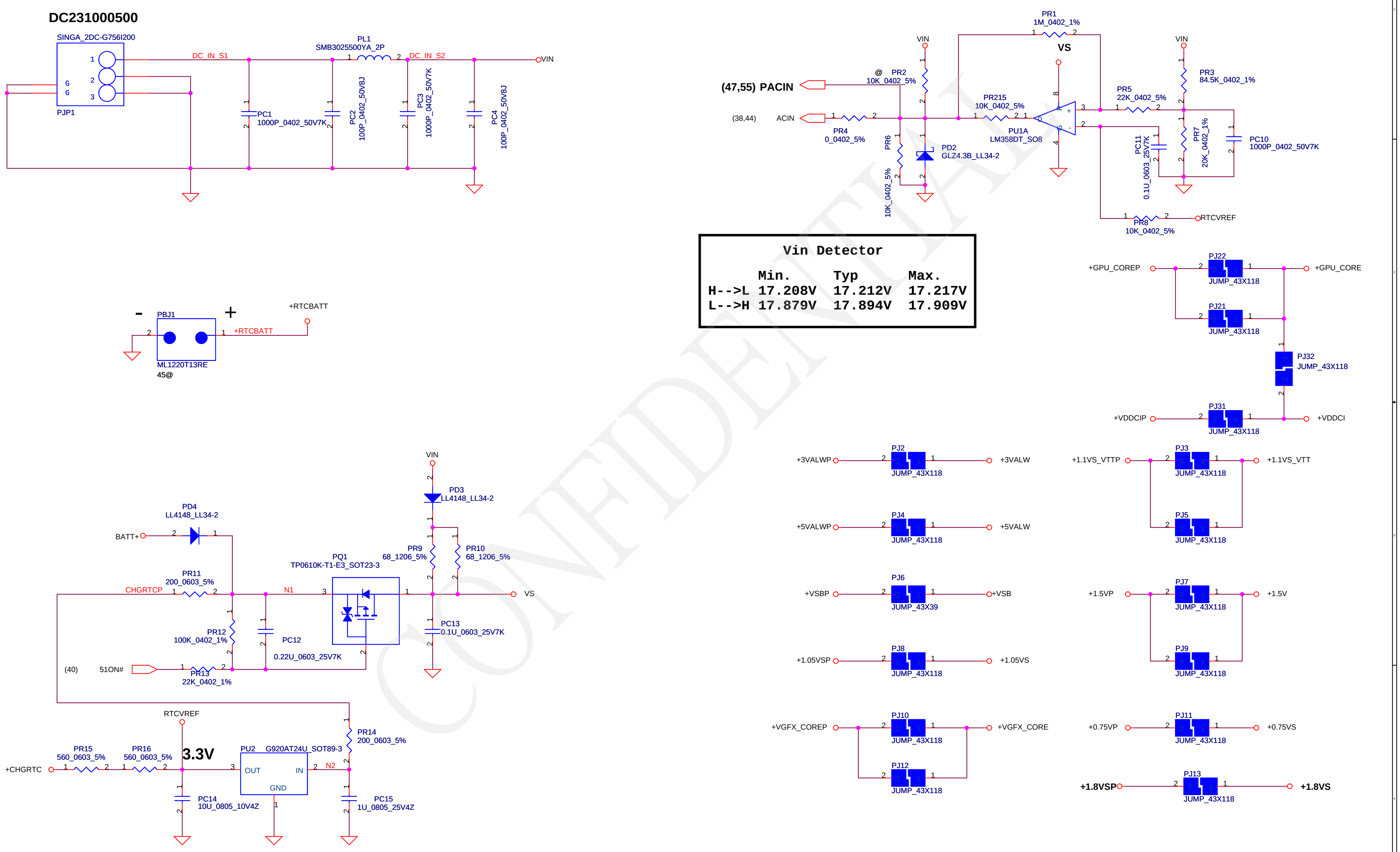
			Date: Tuesday, September 01, 2009; Sheet 44 of 60



Vin Detector

	Min.	Typ	Max.
H-->L	17.208V	17.212V	17.217V
L-->H	17.879V	17.894V	17.909V

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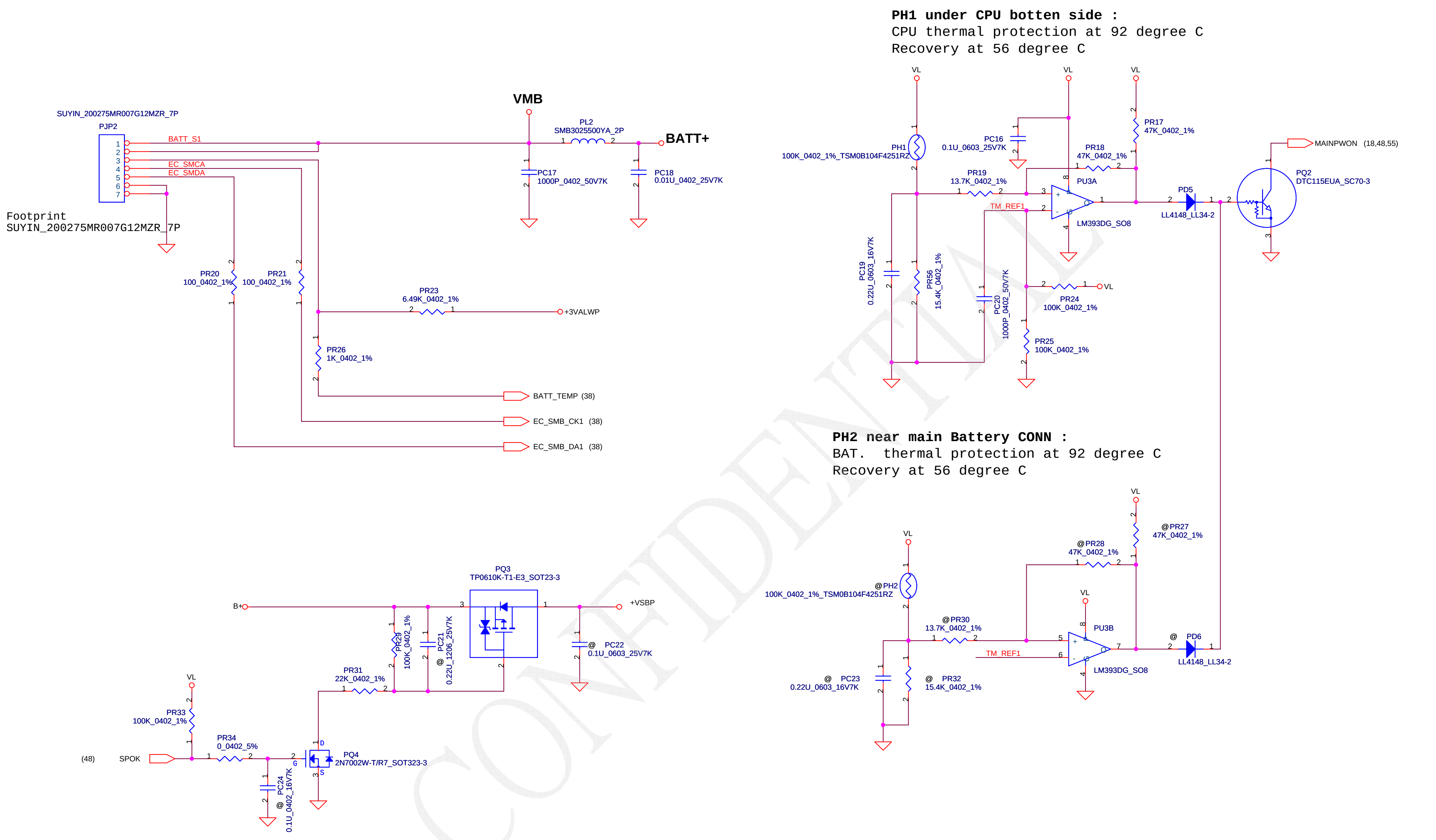

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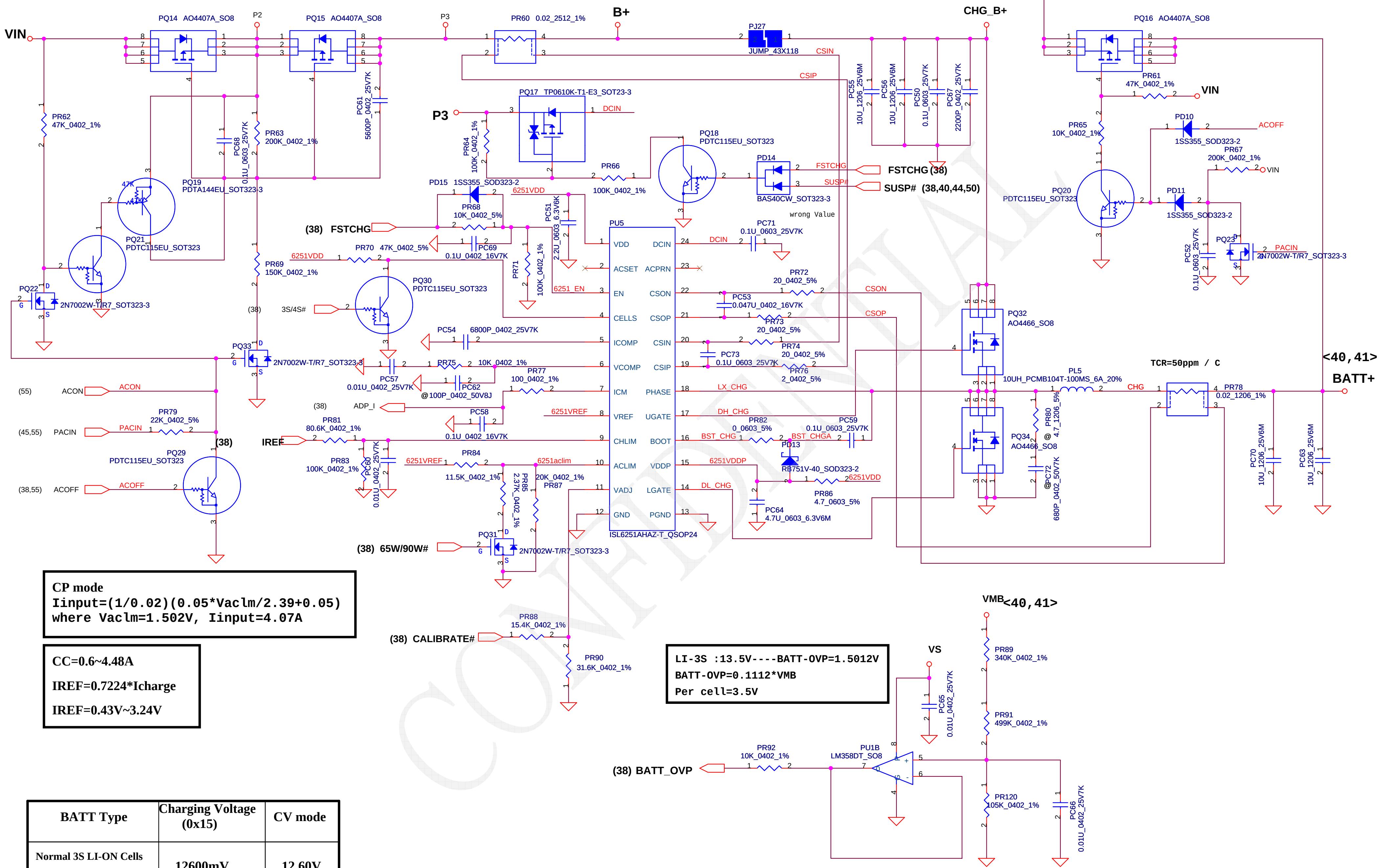
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

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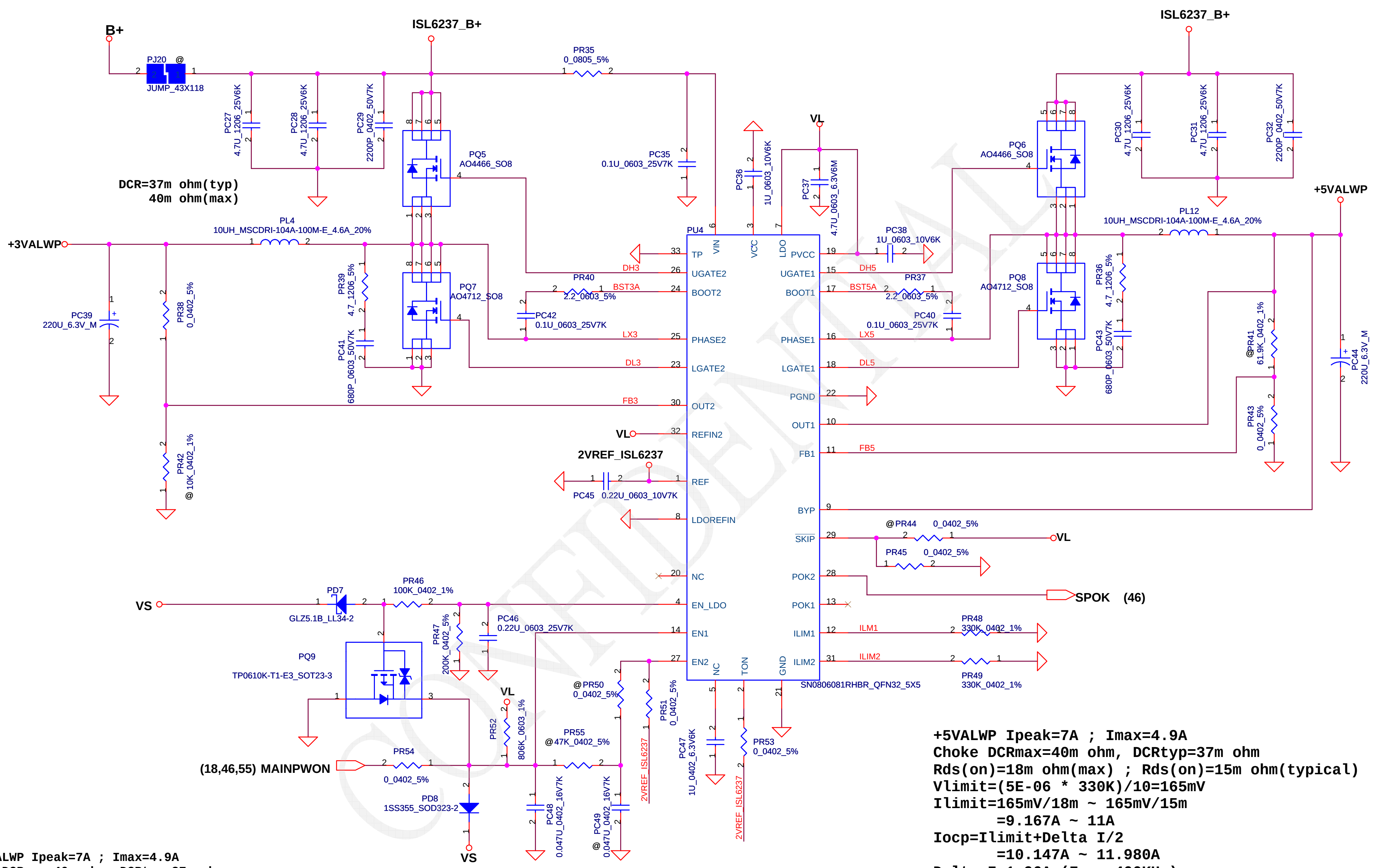

+5VALWP Ipeak=7A ; Imax=4.9A
Choke DCRmax=40m ohm, DCRtyp=37m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

+3.3VALWP Ipeak=7A ; Imax=4.9A
Choke DCRmax=40m ohm, DCRtyp=37m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

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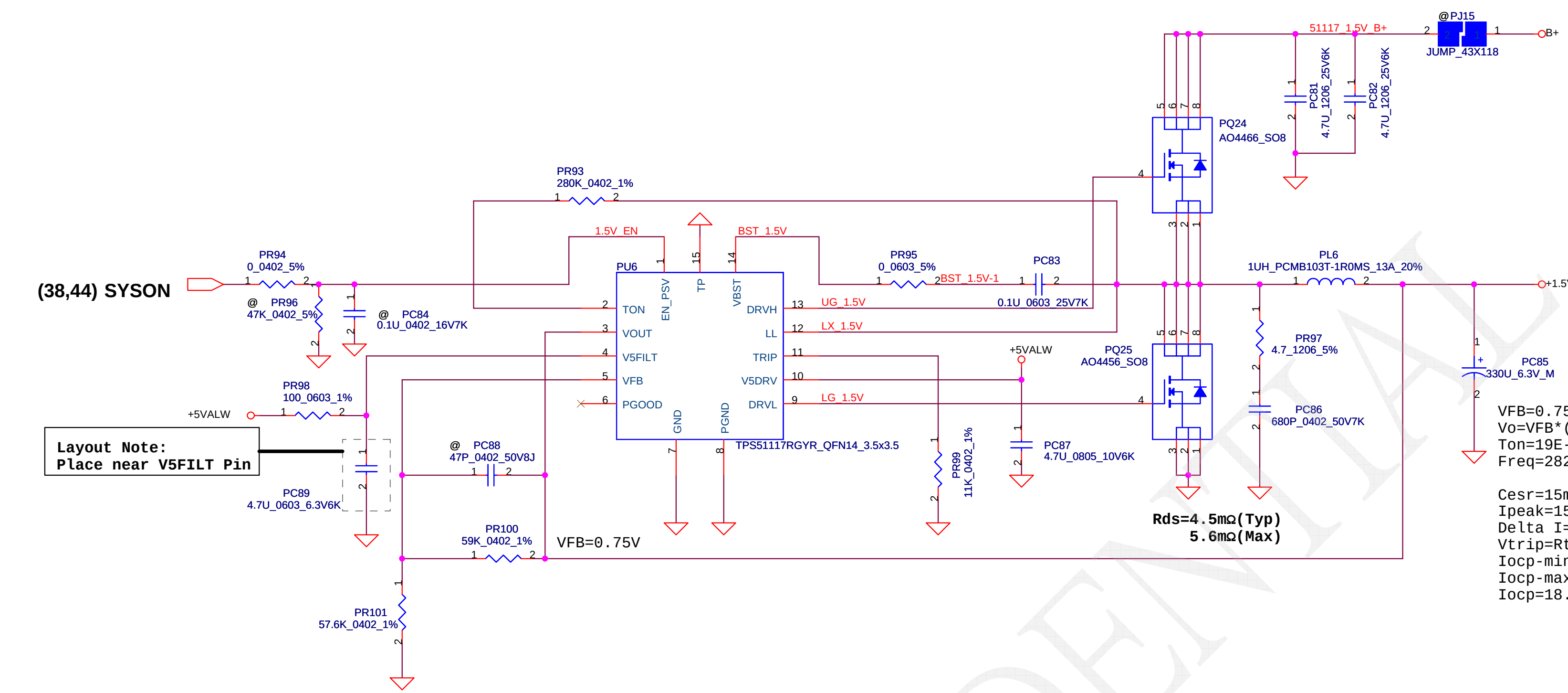
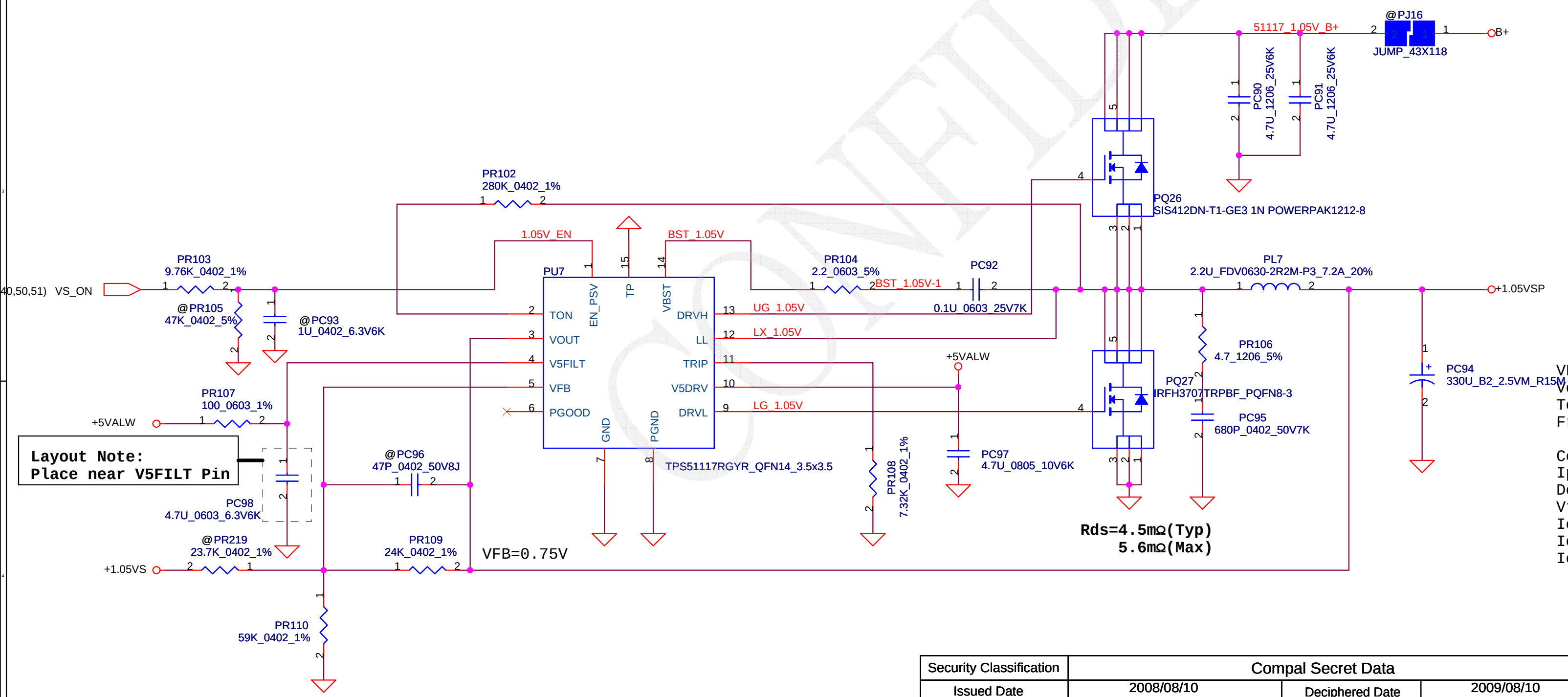
				Date: Tuesday, September 01, 2009; Sheet 48 of 60



VFB=0.75V
Vo=VFB*(1+PR298/PR299)=1.52V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=3.8E-7
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=15.58A Imax=10.906A
Delta I=((19-1.5)*(1.5/19))/(L*Freq)=4.61A
Vtrip=Rtrip*10uA=0.11V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 18.674A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=22.675A
Iocp=18.674~22.675A



VFB=0.75V
Vo=VFB*(1+PR308/PR309)=1.05V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=2.74E-07
Freq=282KHz , 300KHz(typ)

Cesr=15m ohm
Ipeak=10.9A Imax=7.63A
Delta I=((19-1.05)*(1.05/19))/(L*Freq)=1.837A
Vtrip=Rtrip*10uA=0.0732V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 11.81A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=14.47A
Iocp=11.81~14.47A

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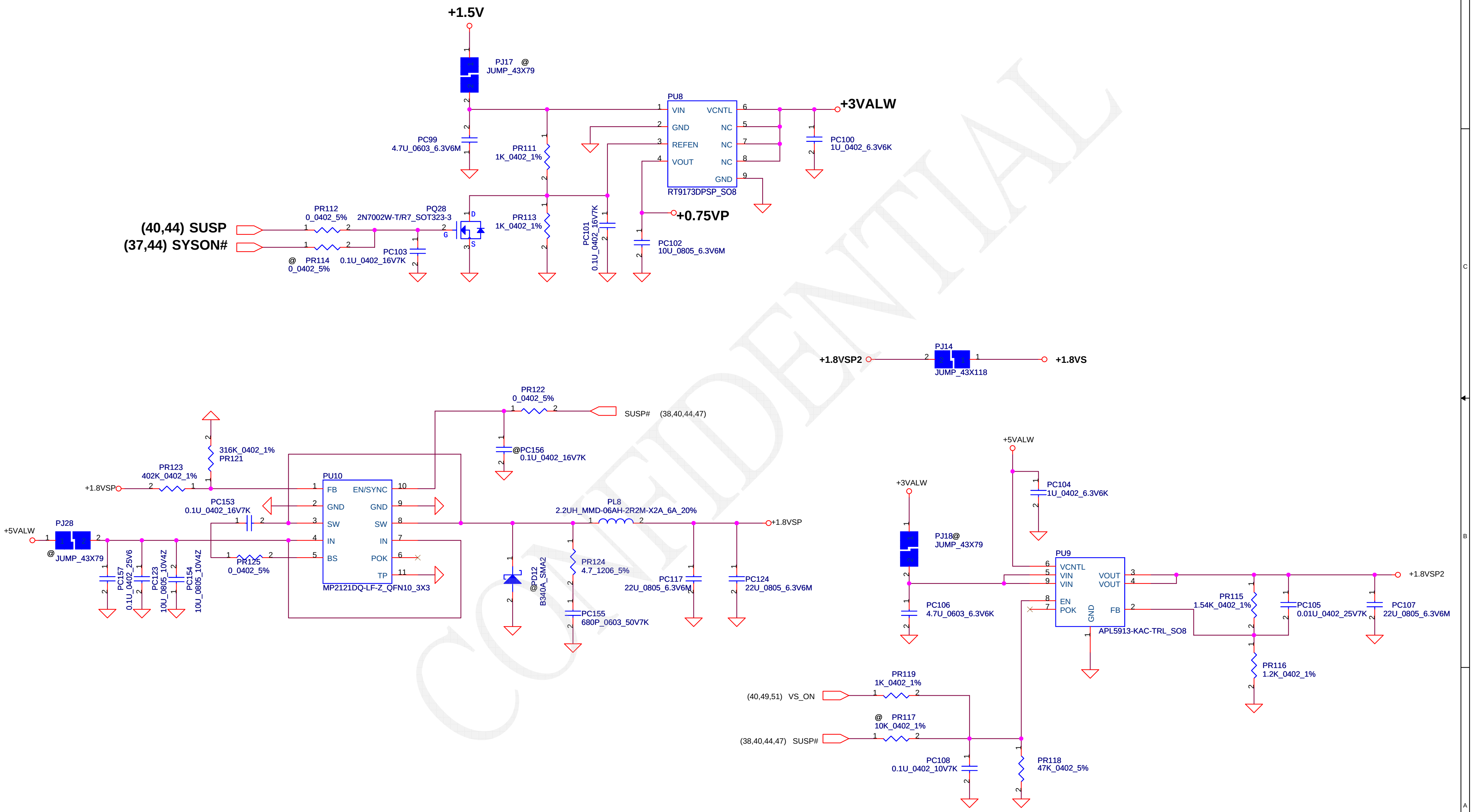

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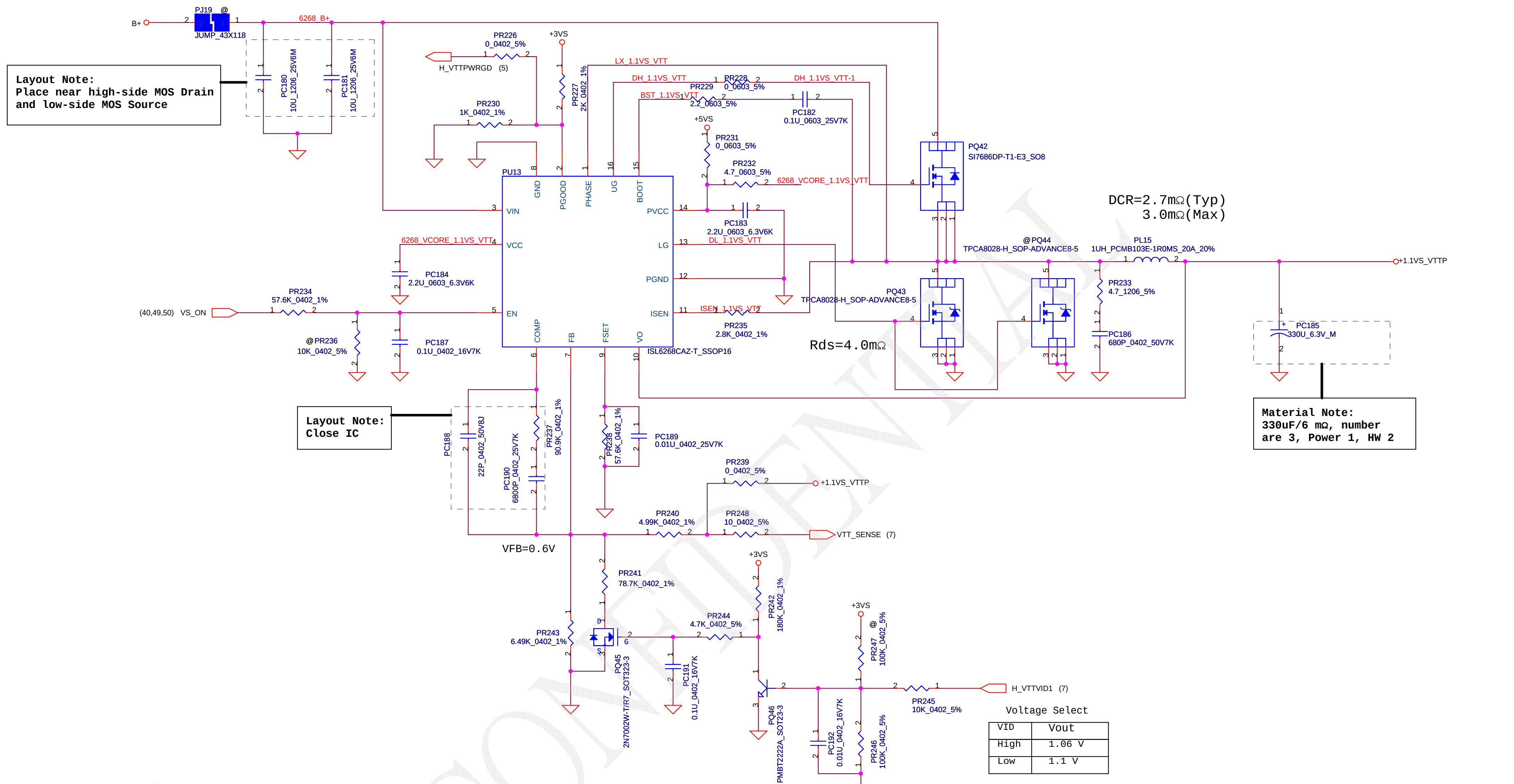

+1.1VS_VTT
Ipeak=25.41A
Imax=17.79A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=Ipeak + Delta I / 2 = 27.586A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=2.787K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=38.372A
Iocp=27.586~38.272A

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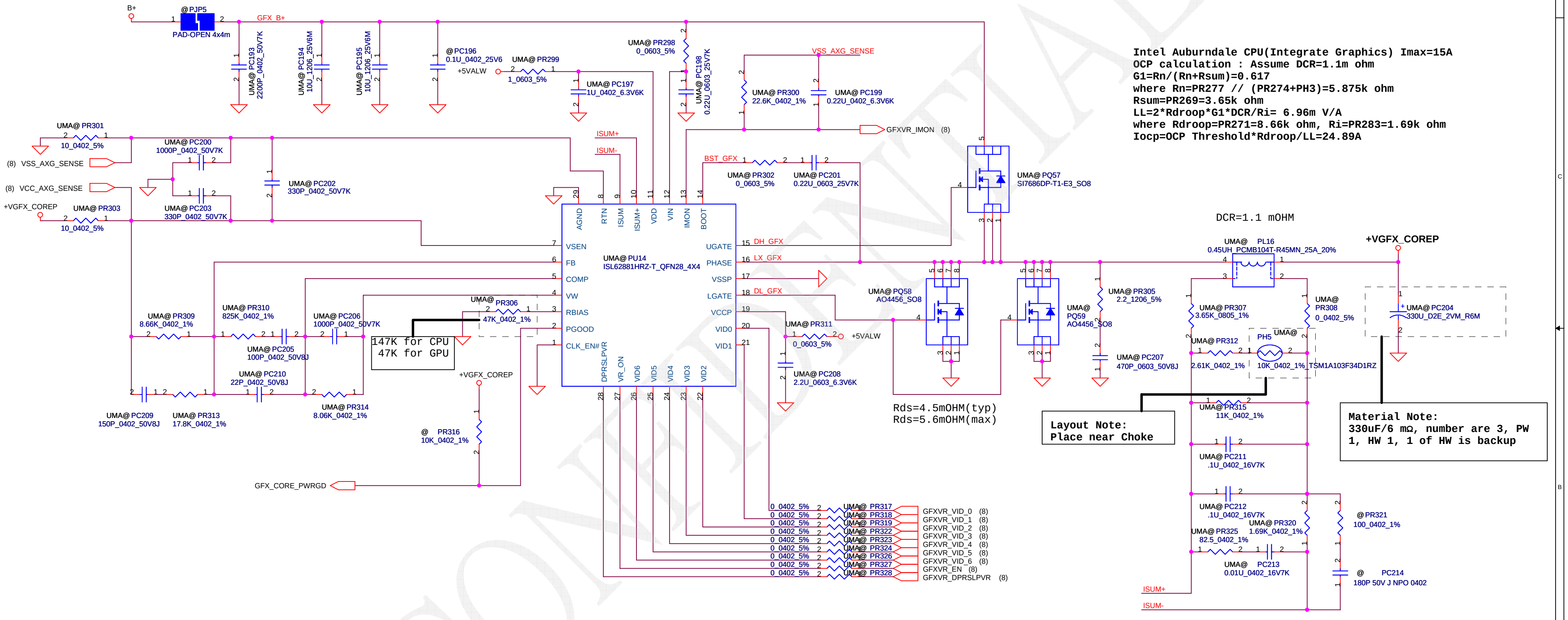

Intel Auburndale CPU(Integrate Graphics) Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A

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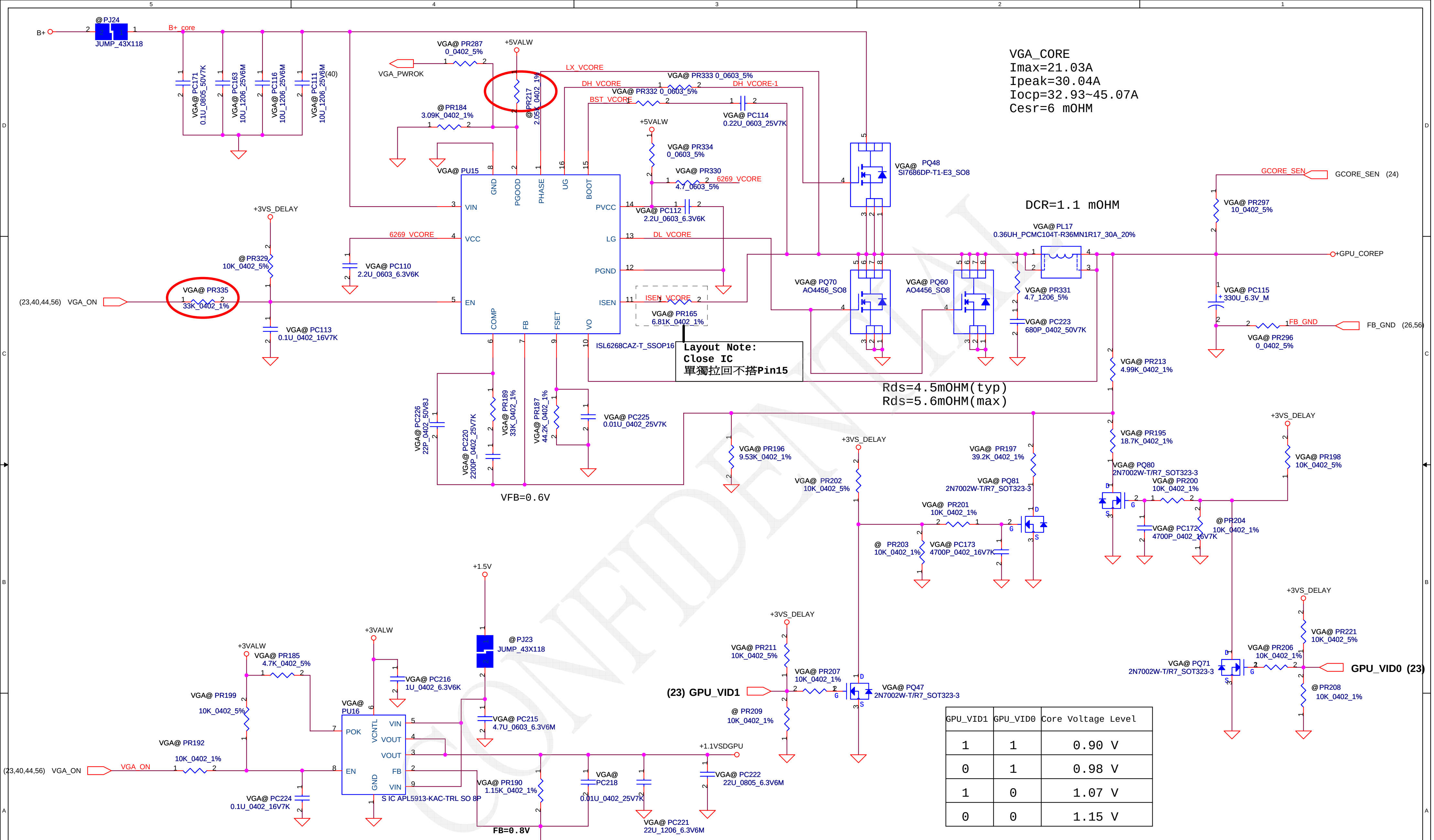

GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.90 V
0	1	0.98 V
1	0	1.07 V
0	0	1.15 V

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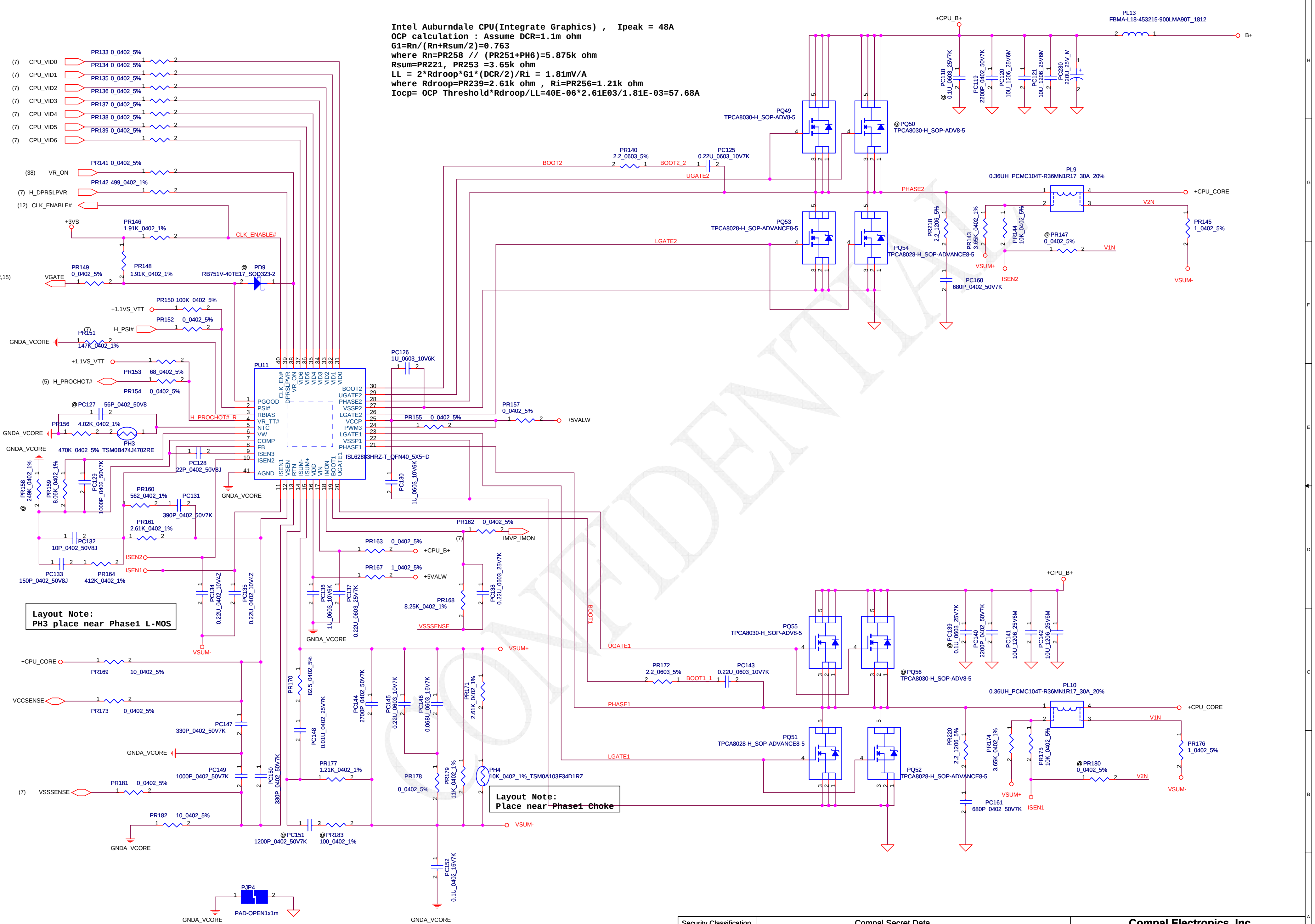
Rds=4.5mΩ(Typ)
5.6mΩ(Max)

Intel Auburndale CPU(Integrate Graphics) , Ipeak = 48A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum/2)=0.763
where Rn=PR258 // (PR251+PH6)=5.875k ohm
Rsum=PR221, PR253 =3.65k ohm
LL = 2*Rdroop*G1*(DCR/2)/Ri = 1.81mV/A
where Rdroop=PR239=2.61k ohm , Ri=PR256=1.21k ohm
Iocp= OCP Threshold*Rdroop/LL=40E-06*2.61E03/1.81E-03=57.68A



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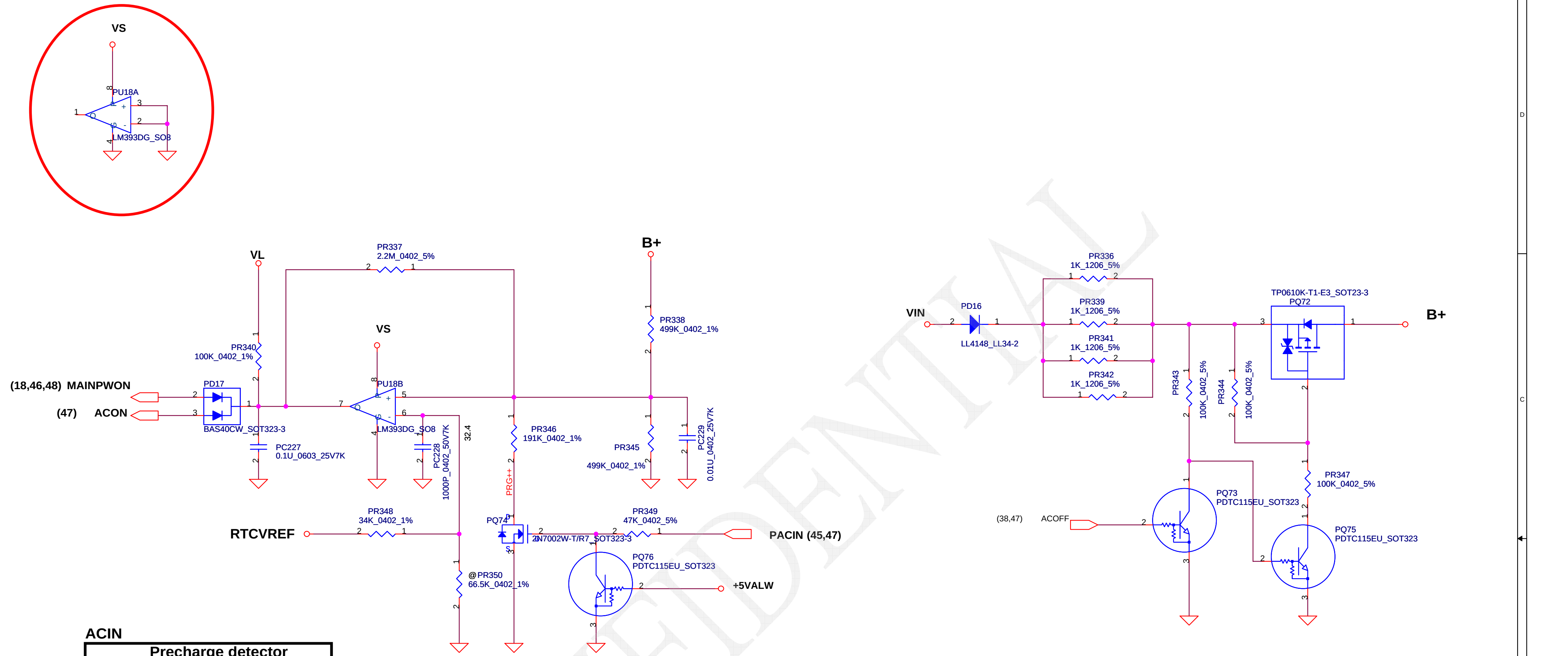

ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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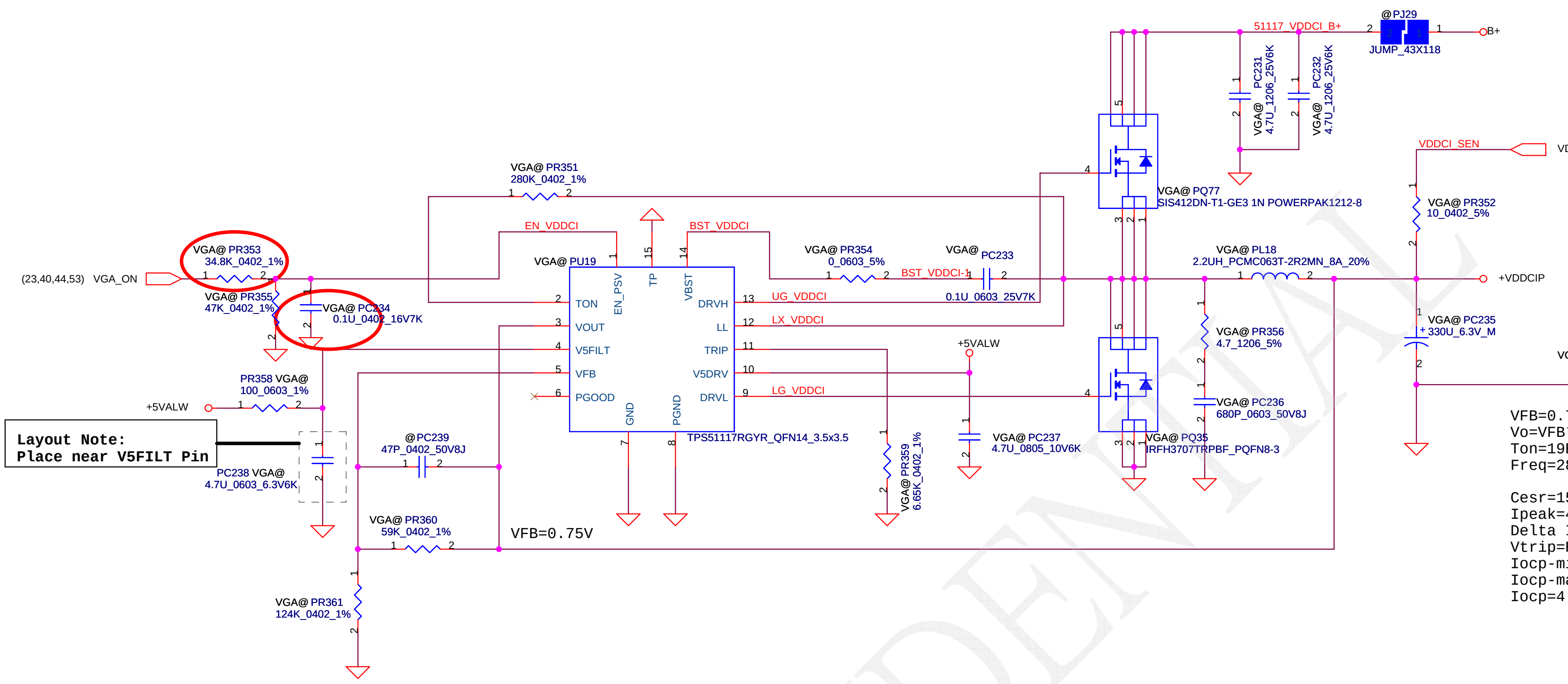

VFB=0.75V
Vo=VFB*(1+PR156/PR150)=1.1V
Ton=19E-12*Ron*(((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7
Freq=282KHz

Cesr=15m ohm
Ipeak=4.00A Imax=2.80A
Delta I=((19.5-1.1)*(1.1/19.5))/(L*Freq)=1.67A
Vtrip=Rtrip*10uA=0.0665V
Iocp-min=4.06A
Iocp-max=5.83A
Iocp=4.06~5.83A

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A --> B Change List

Reference to KBLA0 LA4811 Change List Excel File

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add all sunbber R	EMI solution	0.1	52		09/08/27	DVT
2	add all sunbber C	EMI solution	0.1	52		09/08/27	DVT
3	remove VGA enable R	HW request	0.1	53	delete PR217 2.05K_0402_1%	09/08/27	DVT
4	VDDCI EN sequency regulate	HW request	0.1	53	PR335:32k P/N:SD034330280	09/08/27	DVT
5	VGA EN sequency regulate	HW request	0.1	53	PR353 : 35k P/N:SD00000UD80 PC234 :@==> add	09/08/27	DVT
6							
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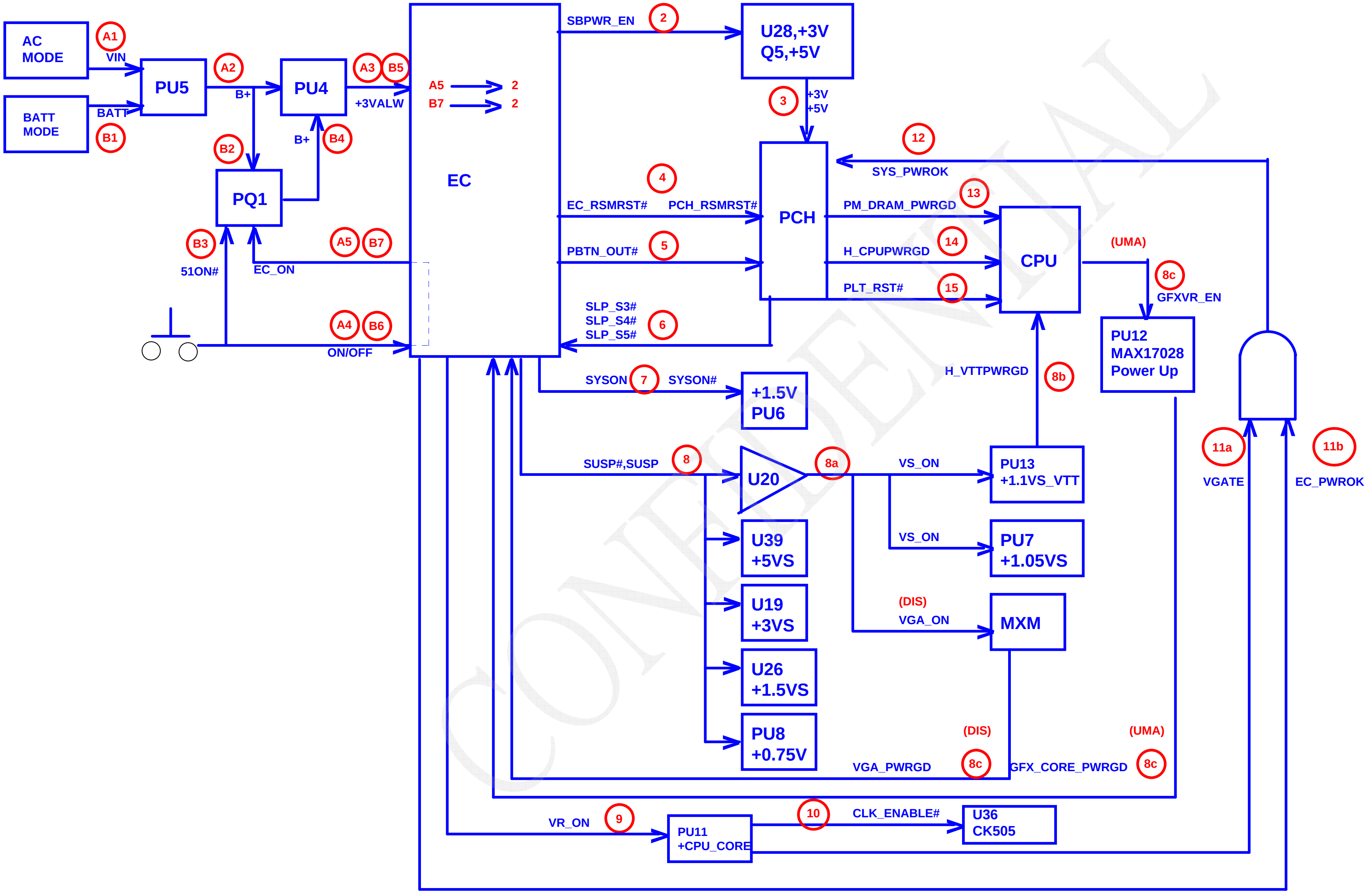
MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



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