Compal Confidential

NAYF0 M/B Schematics Document

Intel Arrandale/Clarksfield Processor with DDRIII + Ibex Peak-M

2009-08-27

REV:0.1

PCB

ZZZ

DAZ@
DA80000GT00

NAYF0 LA-5881P REV0 M/B

LA-5881P MB Rev0: DA80000GT00

VRAM PARK

ZZZ

VRAM PARK@
X76193BOL01

512M HIX

VRAM MAD

ZZZ

VRAM MAD@
X76193BOL03

1G HIX

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Title: SCHEMATIC MB A5881

Size	Document Number	Rev
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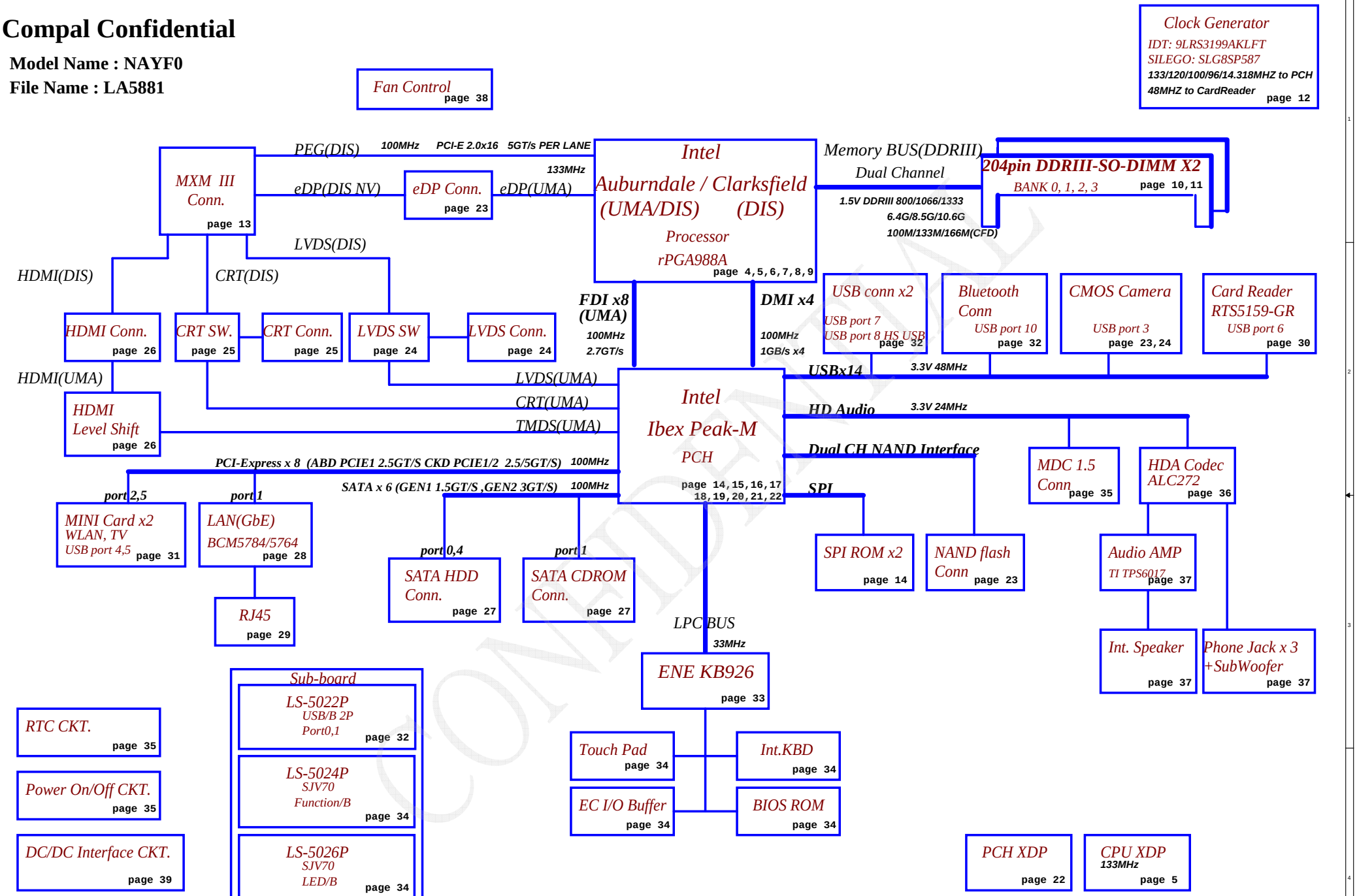
Model Name : NAYF0
File Name : LA5881



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727 ISL90728	0101 1100b 0111 1100b

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
ALC 271	271@
ALC 272	272@
ASM1442	ASM@
CH7318	CH@
S3	S3@
NONS3	NONS3@
XDP	XDP@
Switchable	SG@
VGA	VGA@
UMA	UMA@
UMAO	UMAO@
DISO	DISO@
MADISON	MAD@
PARK	PARK@
VRAM MADISON	VRAM MAD@
VRAM PARK	VRAM PARK@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 USB	Ext1 USB
		1	Ext2 USB	Ext2 USB
	UHCI1	2	Ext3 USB (JV only)	
		3	Camera	Camera
	UHCI2	4	1st Min-Card	1st Min-Card
		5	2st Min-Card	2st Min-Card
	UHCI3	6	Card Reader	Card Reader
		7	Ext3 USB (JM only)	
EHCI2	UHCI4	8	Ext4 HS USB	Ext3 HS USB
		9		
	UHCI5	10	Blue Tooth	Blue Tooth
		11		
	UHCI6	12		
		13		

BOM Config

UMA only SKU:UMAO@/UMA@

Switchable PARK SKU: SG@/VGA@/PARK@/VRAM PARK@

Switchable MADISON SKU: SG@/VGA@/MAD@/VRAM MAD@

The same: 272@/ASM@/NONS3@/DAZ@

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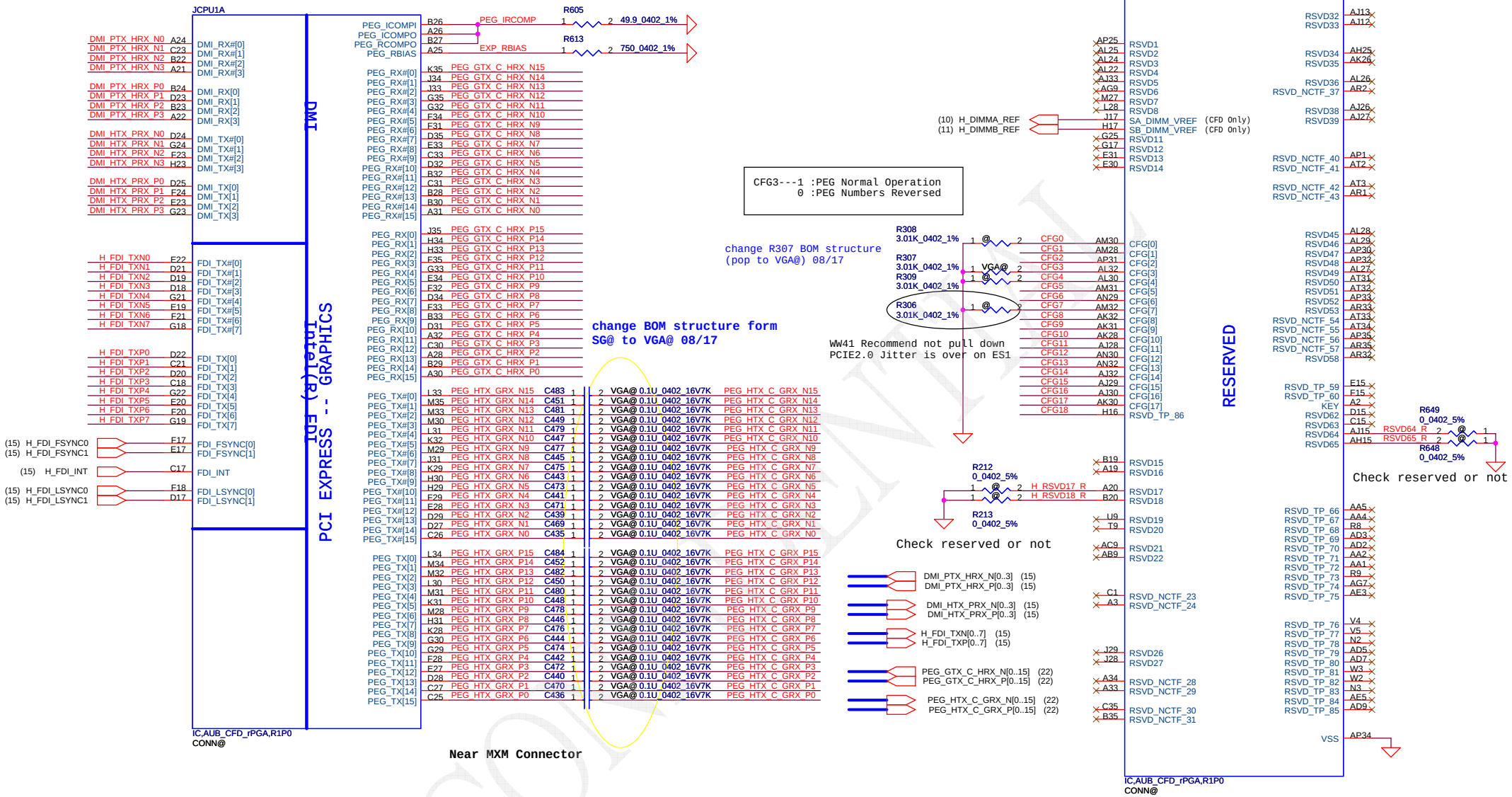

eDP Signals MAPPING

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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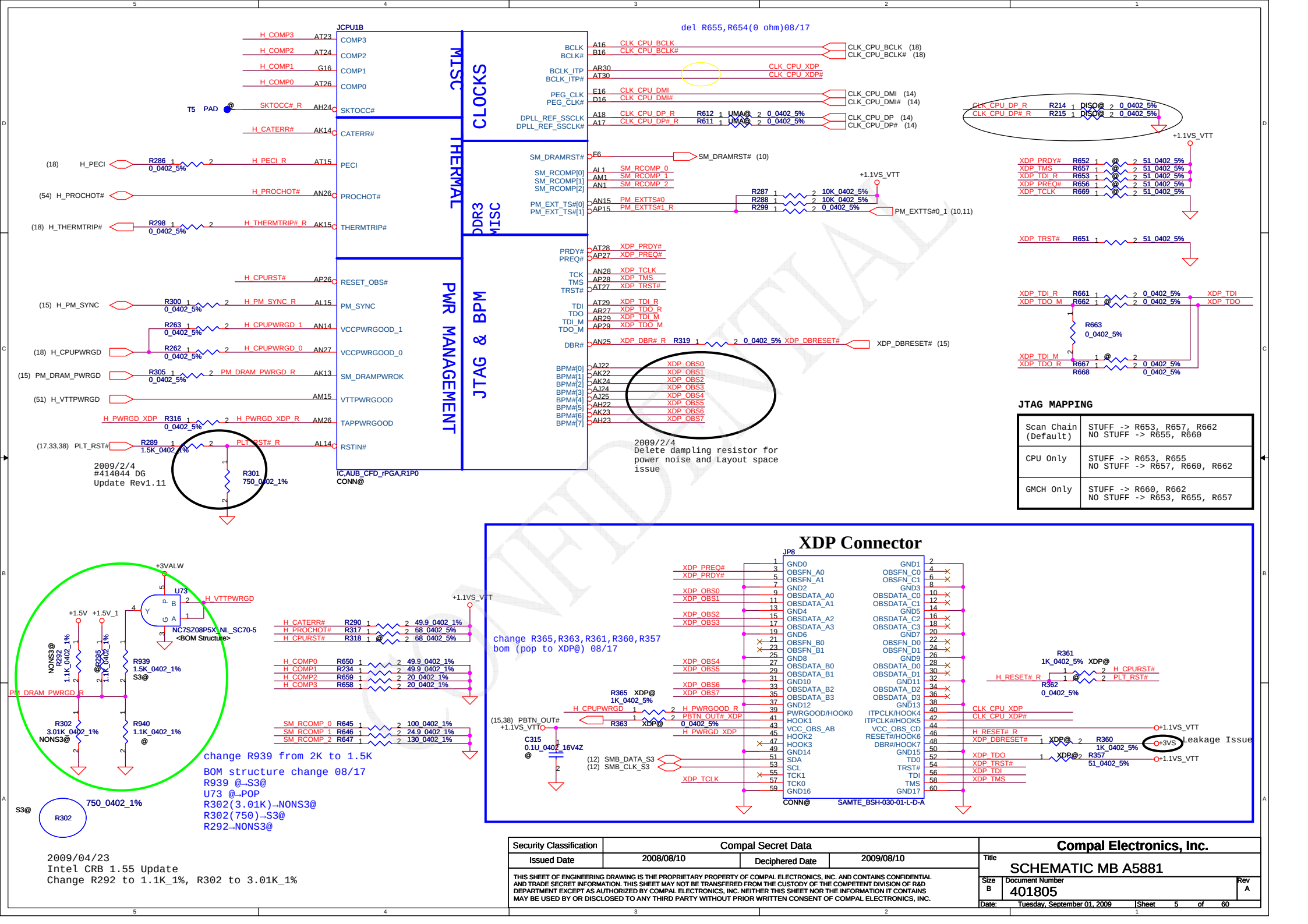

2009/04/23
Intel CRB 1.55 Update
Change R292 to 1.1K_1%, R302 to 3.01K_1%

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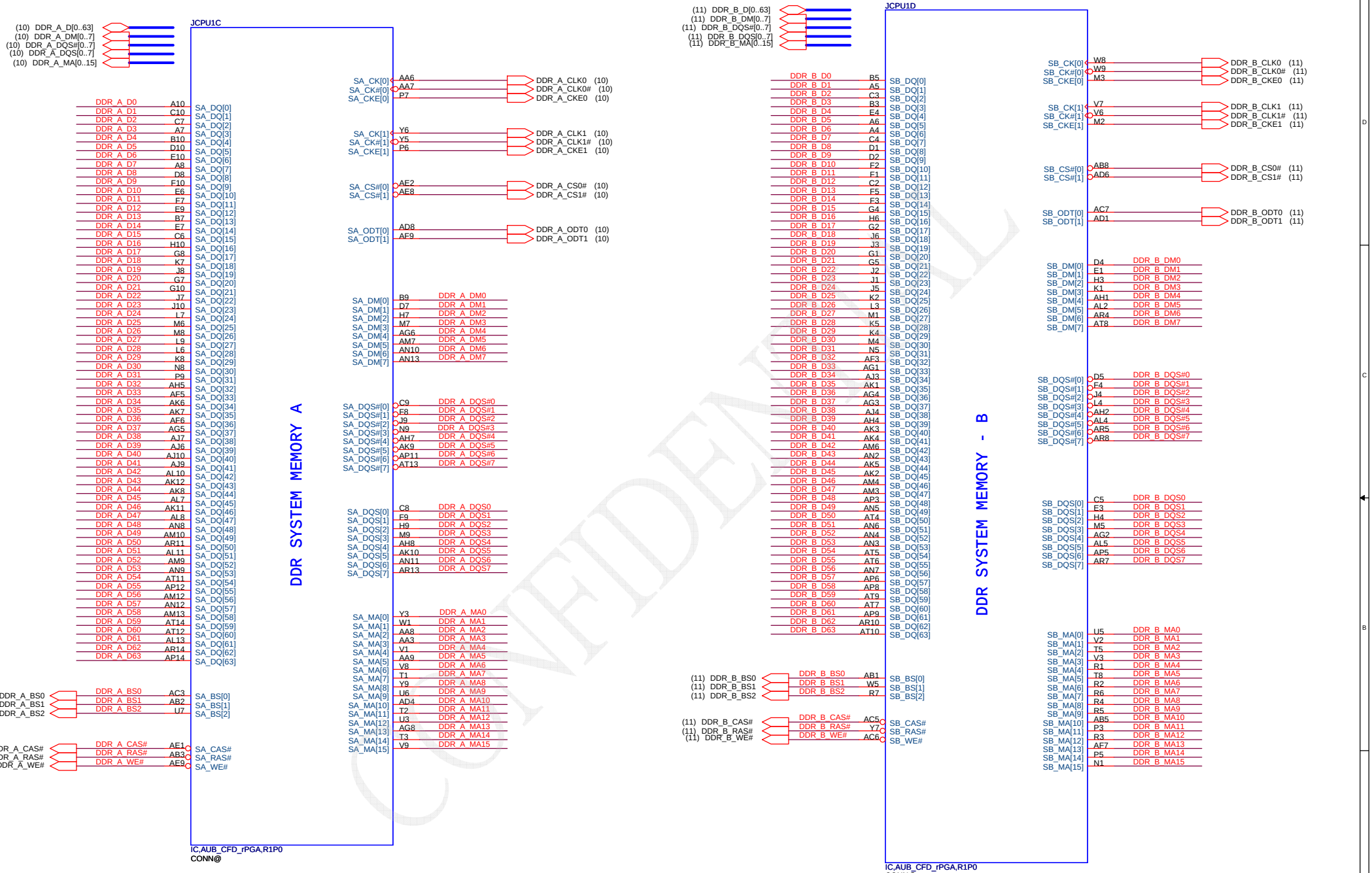

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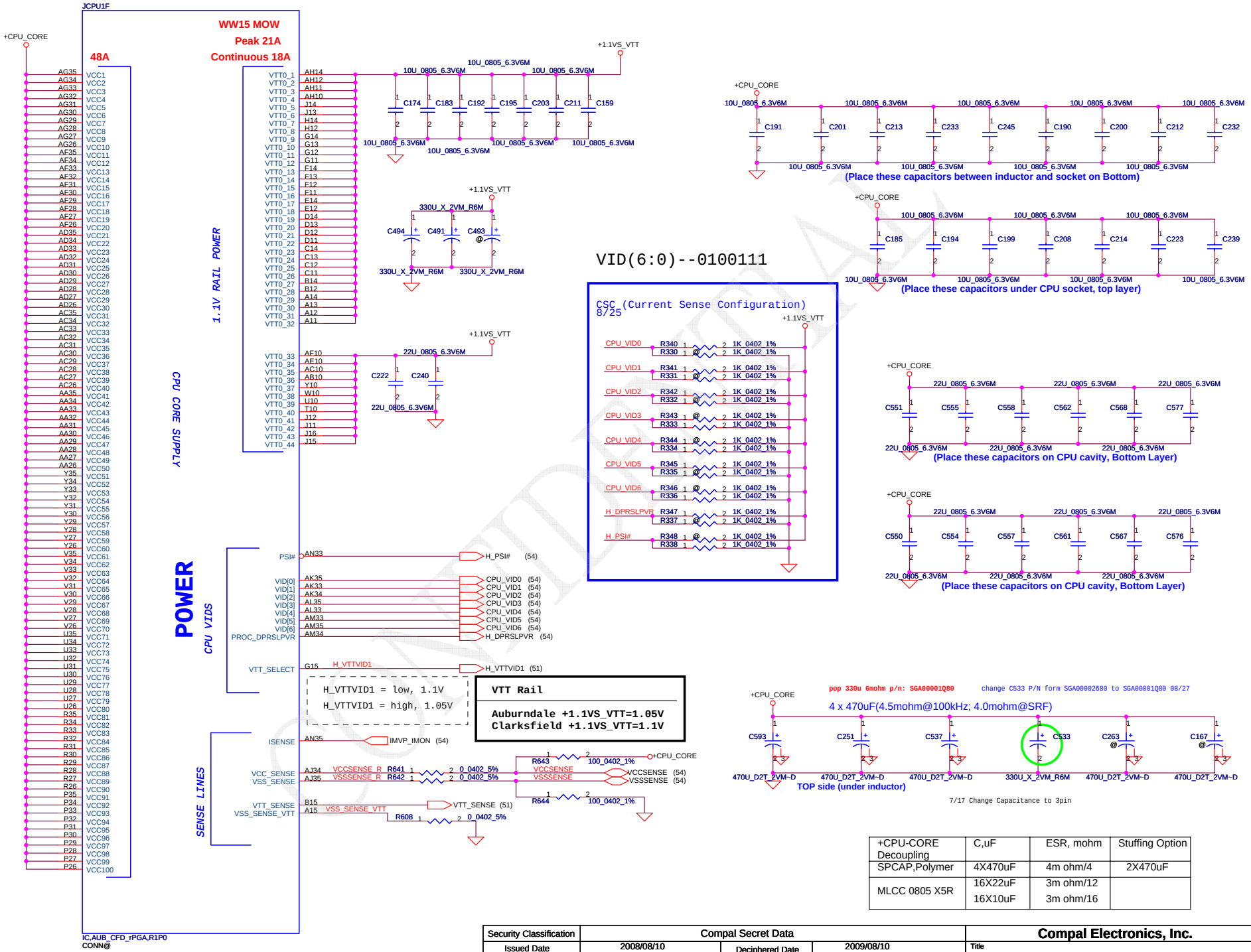

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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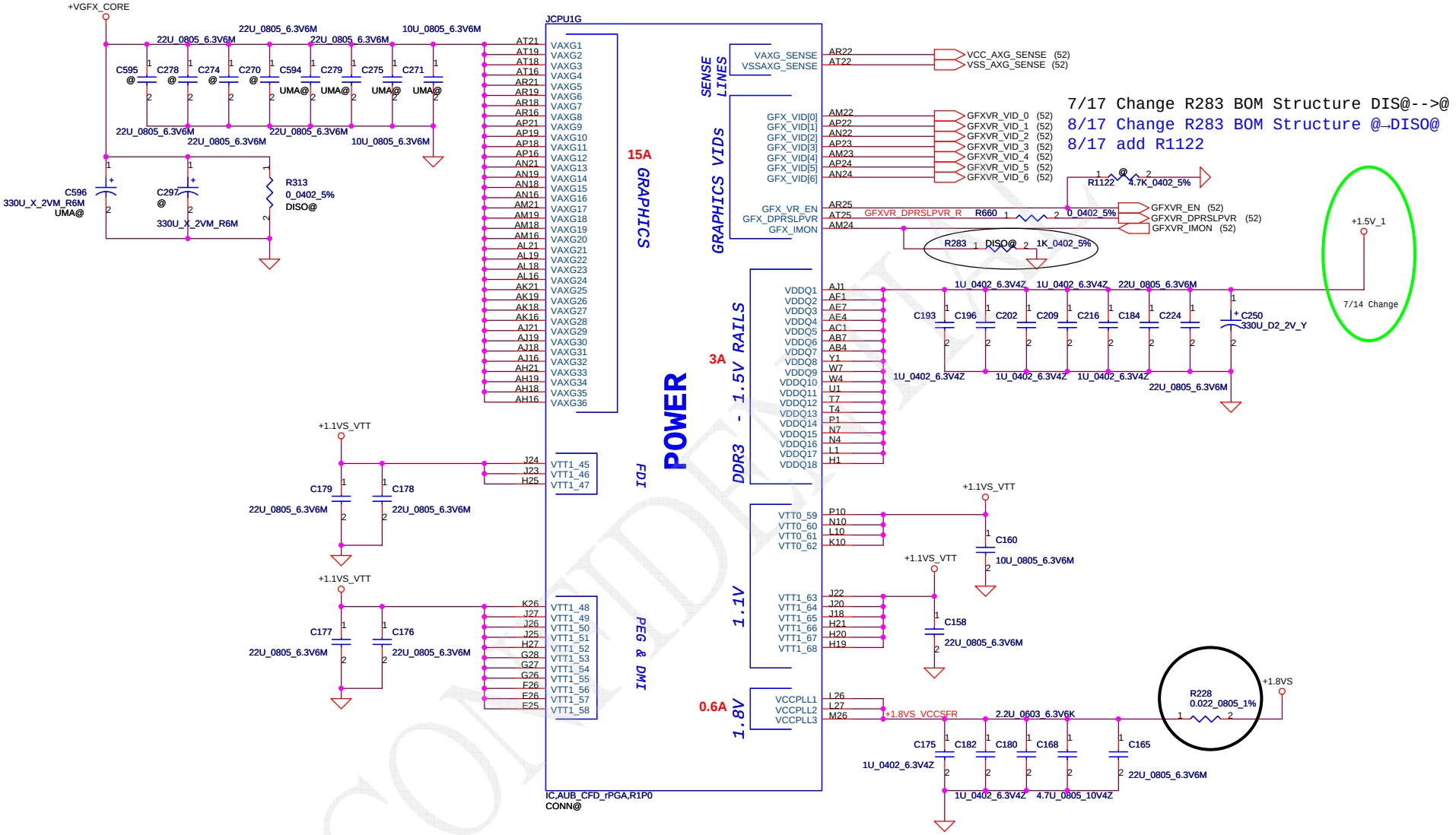

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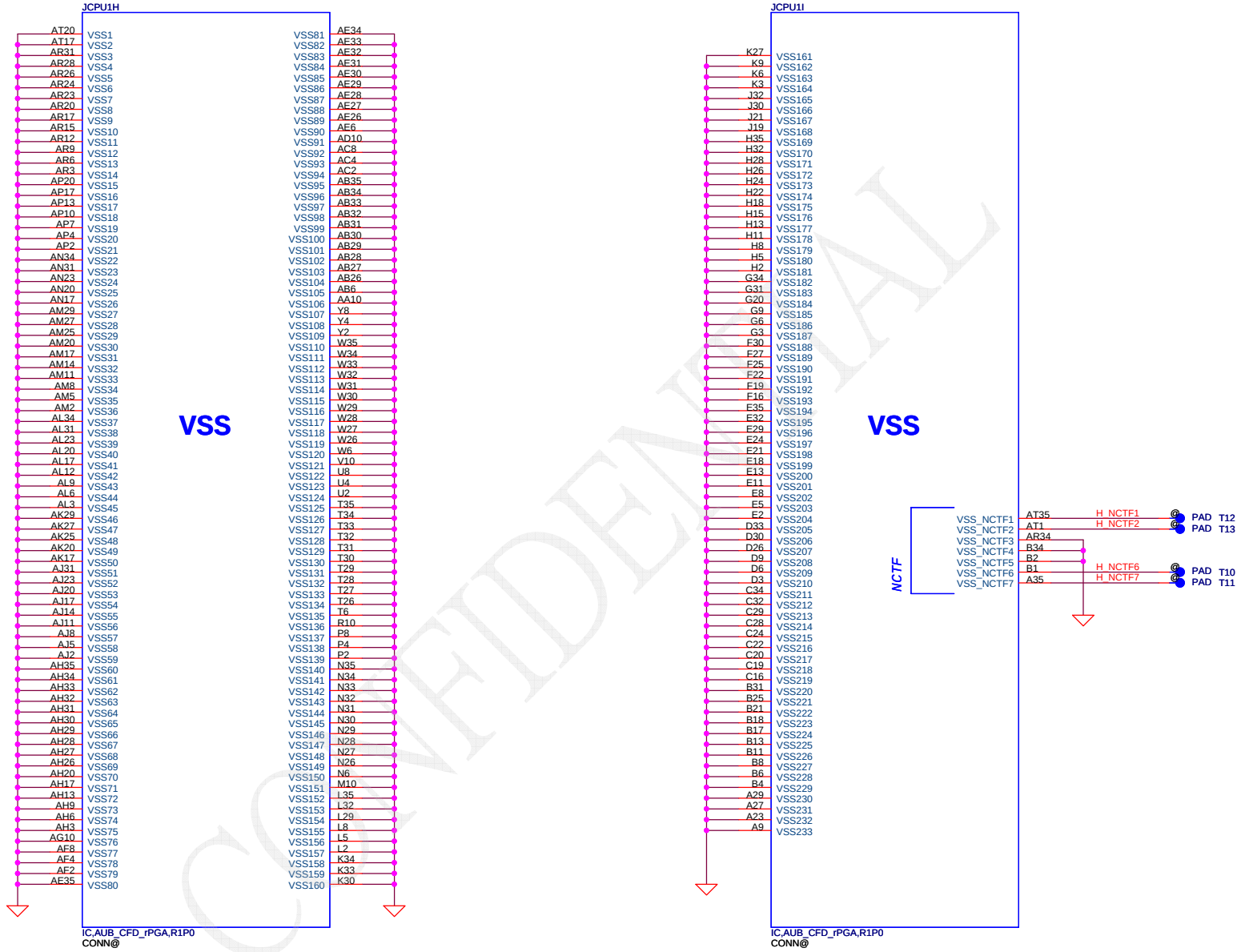

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M1 Circuit

+1.5V
R170 1K_0402_1%
+V_DDR3_DIMM_REF
R169 1K_0402_1%

(6) DDR_A_DQS#[0..7]
(6) DDR_A_D[0..63]
(6) DDR_A_DM[0..7]
(6) DDR_A_DQS[0..7]
(6) DDR_A_MA[0..15]
(4) H_DIMMA_REF

7/14 Change

M3 Circuit
R178 @ 0_0402_5%
R154 100K_0402_5% @
Q79 2N7002_SOT23 @
RST_GATE
M1 Circuit
R179 0_0402_5%

2009/05/19
M2 Circuit unpop
Pop M3 Circuit

2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

090615 add DDR_VREF_CA_DIMM

+1.5V
R210 1K_0402_1%
+DDR_VREF_CA_DIMM
R224 1K_0402_1%
7/14 Change

(5) SM_DRAMRST#
R942 NONS3@ 0_0402_5%
R155 100K_0402_5% S3@
Q80 2N7002_SOT23 S3@
R941 S3@1K_0402_1%
DIMM_DRAMRST#
Change to BSH111
(11,18) RST_GATE

BOM structure change 08/17
R942 POP→NONS3@
R155,R941,Q80 @→S3@

C124 0.1U_0402_16V4Z
C112 2.2U_0805_16V4Z

JDIMM1

		VREF_DQA	1	2	
		VSS	3	4	DDR_A_D4
DDR_A_D0		DQ0	5	6	DDR_A_D5
DDR_A_D1		DQ1	7	8	
		VSS	9	10	DDR_A_DQS#0
DDR_A_DM0		DM0	11	12	DDR_A_DQS0
		VSS	13	14	
DDR_A_D2		DQ2	15	16	DDR_A_D6
DDR_A_D3		DQ3	17	18	DDR_A_D7
		VSS	19	20	
DDR_A_D8		DQ8	21	22	DDR_A_D12
DDR_A_D9		DQ9	23	24	DDR_A_D13
		VSS	25	26	
DDR_A_DQS#1		DQS1#	27	28	DDR_A_DM1
DDR_A_DQS1		DQS1	29	30	DIMM_DRAMRST# → DIMM_DRAMRST# (11)
		VSS	31	32	
DDR_A_D10		DQ10	33	34	DDR_A_D14
DDR_A_D11		DQ11	35	36	DDR_A_D15
		VSS	37	38	
DDR_A_D16		DQ16	39	40	DDR_A_D20
DDR_A_D17		DQ17	41	42	DDR_A_D21
		VSS	43	44	
DDR_A_DQS#2		DQS2#	45	46	DDR_A_DM2
DDR_A_DQS2		DQS2	47	48	
		VSS	49	50	DDR_A_D22
DDR_A_D18		DQ18	51	52	DDR_A_D23
DDR_A_D19		DQ19	53	54	
		VSS	55	56	DDR_A_D28
DDR_A_D24		DQ24	57	58	DDR_A_D29
DDR_A_D25		DQ25	59	60	
		VSS	61	62	DDR_A_DQS#3
DDR_A_DM3		DM3	63	64	DDR_A_DQS3
		VSS	65	66	
DDR_A_D26		DQ26	67	68	DDR_A_D30
DDR_A_D27		DQ27	69	70	DDR_A_D31
		VSS	71	72	
(6) DDR_A_CKE0	DDR_A_CKE0	CKE0	73	74	DDR_A_CKE1 → DDR_A_CKE1 (6)
		VDD	75	76	
(6) DDR_A_BS2	DDR_A_BS2	NC	77	78	DDR_A_MA15
		BA2	79	80	DDR_A_MA14
DDR_A_MA12		VDD	81	82	
DDR_A_MA9		A12/BC#	83	84	DDR_A_MA11
		A9	85	86	DDR_A_MA7
DDR_A_MA8		VDD	87	88	
DDR_A_MA5		A8	89	90	DDR_A_MA6
		A5	91	92	DDR_A_MA4
DDR_A_MA3		VDD	93	94	
DDR_A_MA1		A3	95	96	DDR_A_MA2
		A1	97	98	DDR_A_MA0
		VDD	99	100	
(6) DDR_A_CLK0	DDR_A_CLK0	CK0	101	102	DDR_A_CLK1 → DDR_A_CLK1 (6)
(6) DDR_A_CLK0#	DDR_A_CLK0#	CK0#	103	104	DDR_A_CLK1# → DDR_A_CLK1# (6)
		VDD	105	106	
DDR_A_MA10		A10/AP	107	108	DDR_A_BS1 → DDR_A_BS1 (6)
(6) DDR_A_BS0	DDR_A_BS0	BA0	109	110	DDR_A_RAS# → DDR_A_RAS# (6)
		VDD	111	112	
DDR_A_WE#		WE#	113	114	DDR_A_CS0# → DDR_A_CS0# (6)
(6) DDR_A_CAS#	DDR_A_CAS#	CAS#	115	116	DDR_A_ODT0 → DDR_A_ODT0 (6)
		VDD	117	118	
DDR_A_MA13		A13	119	120	DDR_A_ODT1 → DDR_A_ODT1 (6)
(6) DDR_A_CS1#	DDR_A_CS1#	S1#	121	122	NC
		VDD	123	124	
		TEST	125	126	DDR_VREF_CA_DIMMA R245 0_0402_5%
		VSS	127	128	VREF_CA
DDR_A_D32		DQ32	129	130	DDR_A_D36
DDR_A_D33		DQ33	131	132	DDR_A_D37
		VSS	133	134	
DDR_A_DQS#4		DQS4#	135	136	DDR_A_DM4
DDR_A_DQS4		DQS4	137	138	
		VSS	139	140	DDR_A_D38
DDR_A_D34		DQ34	141	142	DDR_A_D39
DDR_A_D35		DQ35	143	144	
		VSS	145	146	DDR_A_D44
DDR_A_D40		DQ40	147	148	DDR_A_D45
DDR_A_D41		DQ41	149	150	
		VSS	151	152	DDR_A_DQS#5
DDR_A_DM5		DM5	153	154	DDR_A_DQS5
		VSS	155	156	
DDR_A_D42		DQ42	157	158	DDR_A_D46
DDR_A_D43		DQ43	159	160	DDR_A_D47
		VSS	161	162	
DDR_A_D48		DQ48	163	164	DDR_A_D52
DDR_A_D49		DQ49	165	166	DDR_A_D53
		VSS	167	168	
DDR_A_DQS#6		DQS6#	169	170	DDR_A_DM6
DDR_A_DQS6		DQS6	171	172	
		VSS	173	174	DDR_A_D54
DDR_A_D50		DQ50	175	176	DDR_A_D55
DDR_A_D51		DQ51	177	178	
		VSS	179	180	DDR_A_D60
DDR_A_D56		DQ56	181	182	DDR_A_D61
DDR_A_D57		DQ57	183	184	
		VSS	185	186	DDR_A_DQS#7
DDR_A_DM7		DM7	187	188	DDR_A_DQS7
		VSS	189	190	
DDR_A_D58		DQ58	191	192	DDR_A_D62
DDR_A_D59		DQ59	193	194	DDR_A_D63
		VSS	195	196	
		SA0	197	198	PM_EXTTS#0_1 → PM_EXTTS#0_1 (5,11)
		VDDSPD	199	200	D_CK_SDATA → D_CK_SDATA (11,12)
		SA1	201	202	D_CK_SCLK → D_CK_SCLK (11,12)
		VTT	203	204	+0.75VS
		GND1	205	206	
		GND2	207	208	

FOX_AS0A626-U2SN-7F_204P
CONN@

+3VS
R293 10K_0402_5%
C287 2.2U_0603_6.3V4Z
C276 0.1U_0402_16V4Z
R314 10K_0402_5%

7/14 Change
+DDR_VREF_CA_DIMM
C230 2.2U_0603_6.3V4Z
C220 0.1U_0402_16V4Z

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
10U_0805_6.3V6M C186
10U_0805_6.3V6M C204
10U_0805_6.3V6M C171
10U_0805_6.3V6M C187
10U_0805_6.3V6M C170
10U_0805_6.3V6M C205
0.1U_0402_16V4Z C538
0.1U_0402_16V4Z C547
0.1U_0402_16V4Z C559
0.1U_0402_16V4Z C569
330U_D2_2V_Y C197

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS
1U_0603_10V4Z C294
1U_0603_10V4Z C280
1U_0603_10V4Z C292
1U_0603_10V4Z C281
10U_0805_6.3V6M C293
1U_0603_10V4Z
1U_0603_10V4Z

DDR3 SO-DIMM A
Standard Type

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(6) DDR_B_DQS#[0..7]
(6) DDR_B_D[0..63]
(6) DDR_B_DM[0..7]
(6) DDR_B_DQS[0..7]
(6) DDR_B_MA[0..15]

2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

2009/05/19
M2 Circuit unpop
Pop M3 Circuit

7/14 Change
M3 Circuit
(4) H_DIMMB_REF
R165 1 @ 2 0_0402_5%
VREF_DQB
Q81
2N7002_SOT23
@
(10,18) RST_GATE
RST_GATE
M1 Circuit
+V_DDR3_DIMM_REF
R166 1 2 0_0402_5%

C110 1 2 2.2U_0805_16V4Z
C122 1 2 0.1U_0402_16V4Z

+1.5V

JDIMM2

1	VREF_DQ	VSS	2		
3	VSS	DQ4	4	DDR_B_D0	DDR_B_D4
5	DQ0	DQ5	6	DDR_B_D1	DDR_B_D5
7	DQ1	VSS	8		
9	VSS	DQS0#	10	DDR_B_DM0	DDR_B_DQS#0
11	DM0	DQS0	12		DDR_B_DQS0
13	VSS	VSS	14		
15	DQ2	DQ6	16	DDR_B_D2	DDR_B_D6
17	DQ3	DQ7	18	DDR_B_D3	DDR_B_D7
19	VSS	VSS	20		
21	DQ8	DQ12	22	DDR_B_D8	DDR_B_D12
23	DQ9	DQ13	24	DDR_B_D9	DDR_B_D13
25	VSS	VSS	26		
27	DQS1#	DM1	28	DDR_B_DQS#1	DDR_B_DM1
29	DQS1	RESET#	30	DDR_B_DQS1	DIMM_DRAMRST#
31	VSS	VSS	32		
33	DQ10	DQ14	34	DDR_B_D10	DDR_B_D14
35	DQ11	DQ15	36	DDR_B_D11	DDR_B_D15
37	VSS	VSS	38		
39	DQ16	DQ20	40	DDR_B_D16	DDR_B_D20
41	DQ17	DQ21	42	DDR_B_D17	DDR_B_D21
43	VSS	VSS	44		
45	DQS2#	DM2	46	DDR_B_DQS#2	DDR_B_DM2
47	DQS2	VSS	48	DDR_B_DQS2	
49	VSS	DQ22	50		DDR_B_D22
51	DQ18	DQ23	52	DDR_B_D18	DDR_B_D23
53	DQ19	VSS	54	DDR_B_D19	
55	VSS	DQ28	56		DDR_B_D28
57	DQ24	DQ29	58	DDR_B_D24	DDR_B_D29
59	DQ25	VSS	60	DDR_B_D25	
61	VSS	DQS3#	62		DDR_B_DQS#3
63	DM3	DQS3	64	DDR_B_DM3	DDR_B_DQS3
65	VSS	VSS	66		
67	DQ26	DQ30	68	DDR_B_D26	DDR_B_D30
69	DQ27	DQ31	70	DDR_B_D27	DDR_B_D31
71	VSS	VSS	72		
73	CKE0	CKE1	74	(6) DDR_B_CKE0 DDR_B_CKE0	DDR_B_CKE1 DDR_B_CKE1 (6)
75	VDD	VDD	76		
77	NC	A15	78		DDR_B_MA15
79	BA2	A14	80	(6) DDR_B_BS2 DDR_B_BS2	DDR_B_MA14
81	VDD	VDD	82		
83	A12/BC#	A11	84	DDR_B_MA12	DDR_B_MA11
85	A9	A7	86	DDR_B_MA9	DDR_B_MA7
87	VDD	VDD	88		
89	A8	A6	90	DDR_B_MA8	DDR_B_MA6
91	A5	A4	92	DDR_B_MA5	DDR_B_MA4
93	VDD	VDD	94		
95	A3	A2	96	DDR_B_MA3	DDR_B_MA2
97	A1	A0	98	DDR_B_MA1	DDR_B_MA0
99	VDD	VDD	100		
101	CK0	CK1	102	(6) DDR_B_CLK0 DDR_B_CLK0	DDR_B_CLK1 DDR_B_CLK1 (6)
103	CK0#	CK1#	104	(6) DDR_B_CLK0# DDR_B_CLK0#	DDR_B_CLK1# (6)
105	VDD	VDD	106		
107	A10/AP	BA1	108	DDR_B_MA10	DDR_B_BS1 (6)
109	BA0	RAS#	110	DDR_B_BS0 (6) DDR_B_BS0	DDR_B_RAS# (6)
111	VDD	VDD	112		
113	WE#	S0#	114	(6) DDR_B_WE# DDR_B_WE#	DDR_B_CS0# (6)
115	CAS#	ODT0	116	(6) DDR_B_CAS# DDR_B_CAS#	DDR_B_ODT0 (6)
117	VDD	VDD	118		
119	A13	ODT1	120	DDR_B_MA13	DDR_B_ODT1 DDR_B_ODT1 (6)
121	S1#	NC	122	(6) DDR_B_CS1# DDR_B_CS1#	
123	VDD	VDD	124		
125	TEST	VREF_CA	126		DDR_VREF_CA_DIMM
127	VSS	VSS	128		
129	DQ32	DQ36	130	DDR_B_D32	DDR_B_D36
131	DQ33	DQ37	132	DDR_B_D33	DDR_B_D37
133	VSS	VSS	134		
135	DQS4#	DM4	136	DDR_B_DQS#4	DDR_B_DM4
137	DQS4	VSS	138	DDR_B_DQS4	
139	VSS	DQ38	140		DDR_B_D38
141	DQ34	DQ39	142	DDR_B_D34	DDR_B_D39
143	DQ35	VSS	144	DDR_B_D35	
145	VSS	DQ44	146		DDR_B_D44
147	DQ40	DQ45	148	DDR_B_D40	DDR_B_D45
149	DQ41	VSS	150	DDR_B_D41	
151	VSS	DQS5#	152		DDR_B_DQS#5
153	DM5	DQS5	154	DDR_B_DM5	DDR_B_DQS5
155	VSS	VSS	156		
157	DQ42	DQ46	158	DDR_B_D42	DDR_B_D46
159	DQ43	DQ47	160	DDR_B_D43	DDR_B_D47
161	VSS	VSS	162		
163	DQ48	DQ52	164	DDR_B_D48	DDR_B_D52
165	DQ49	DQ53	166	DDR_B_D49	DDR_B_D53
167	VSS	VSS	168		
169	DQS6#	DM6	170	DDR_B_DQS#6	DDR_B_DM6
171	DQS6	VSS	172	DDR_B_DQS6	
173	VSS	DQ54	174		DDR_B_D54
175	DQ50	DQ55	176	DDR_B_D50	DDR_B_D55
177	DQ51	VSS	178	DDR_B_D51	
179	VSS	DQ60	180		DDR_B_D60
181	DQ56	DQ61	182	DDR_B_D56	DDR_B_D61
183	DQ57	VSS	184	DDR_B_D57	
185	VSS	DQS7#	186		DDR_B_DQS#7
187	DM7	DQS7	188	DDR_B_DM7	DDR_B_DQS7
189	VSS	VSS	190		
191	DQ58	DQ62	192	DDR_B_D58	DDR_B_D62
193	DQ59	DQ63	194	DDR_B_D59	DDR_B_D63
195	VSS	VSS	196		
197	SA0	EVENT#	198		PM_EXTTS#0_1 (5,10)
199	VDDSPD	SDA	200		D_CK_SDATA (10,12)
201	SA1	SCL	202		D_CK_SCLK (10,12)
203	VTT	VTT	204		+0.75VS
205	GND1	BOSS1	206		
207	GND2	BOSS2	208		

TYCO_2-2013310-1_204P
CONN@

+1.5V
R294 1 2 10K_0402_5%
+3VS
R315 1 2 10K_0402_5%
C288 1 2 2.2U_0603_6.3V4Z
C277 1 2 0.1U_0402_16V4Z

+DDR_VREF_CA_DIMM
DDR_VREF_CA_DIMM R246 1 2 0_0402_5%
7/14 Change
C231 1 2 2.2U_0603_6.3V4Z
C221 1 2 0.1U_0402_16V4Z

Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
10U_0805_6.3V6M
10U_0805_6.3V6M
0.1U_0402_16V4Z
0.1U_0402_16V4Z
C172 C188 C206 C173 C189 C207 C546 C552 C540 C544 C198
330U_D2_2V_Y
10U_0805_6.3V6M
10U_0805_6.3V6M
10U_0805_6.3V6M
10U_0805_6.3V6M
0.1U_0402_16V4Z
0.1U_0402_16V4Z

Layout Note:
Place near JDIMM2.203 & JDIMM2.204

+0.75VS
1U_0603_10V4Z
C295 C282 C283 C296 C298
1U_0603_10V4Z
10U_0805_6.3V6M
1U_0603_10V4Z
1U_0603_10V4Z

DDR3 SO-DIMM B
Standard Type

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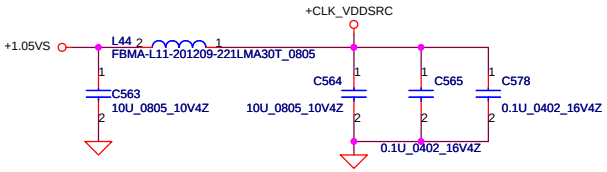
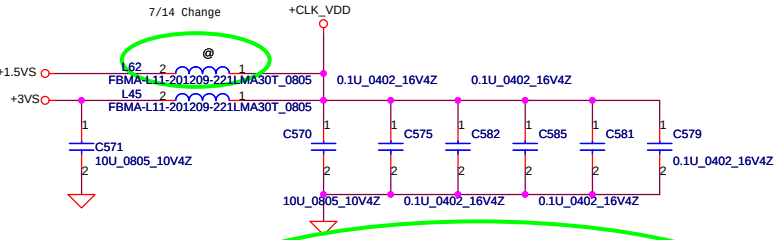
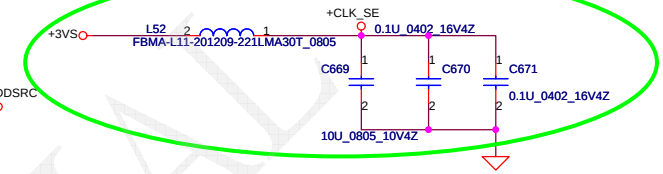
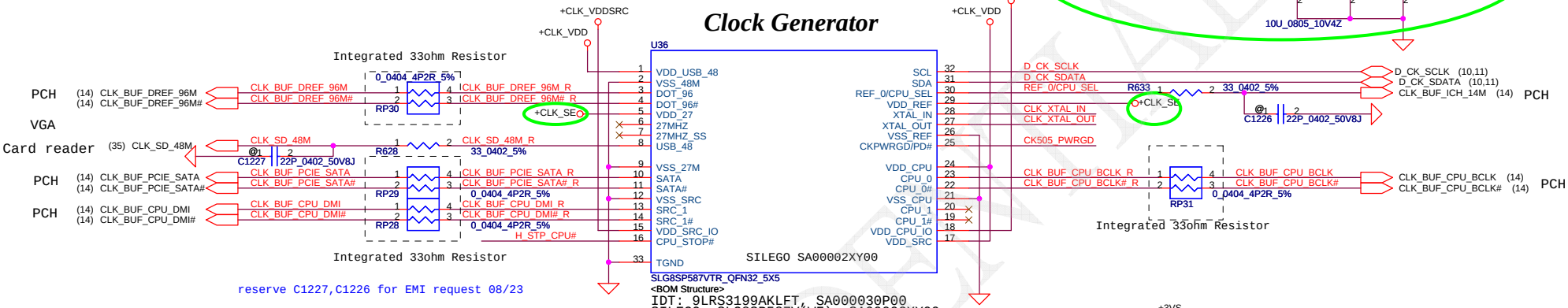
Clock Generator



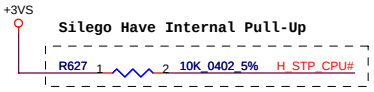


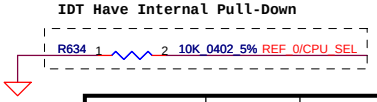




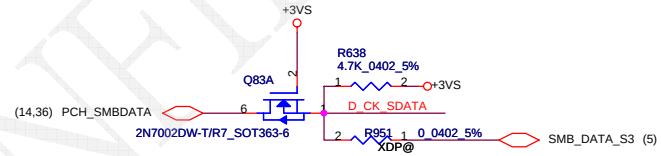
reserve C1227,C1226 for EMI request 08/23

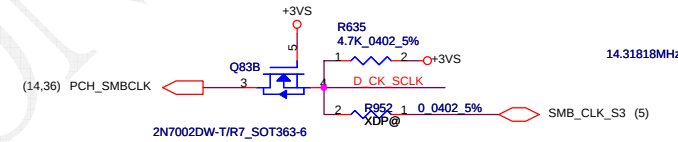
IDT: 9LRS3199AKLFT, SA000030P00
SILEGO: SLG8SP587V(WF), SA00002XY00

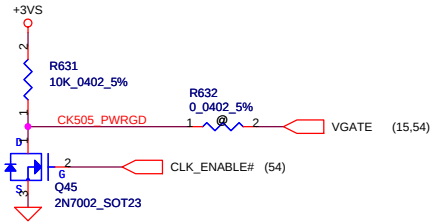


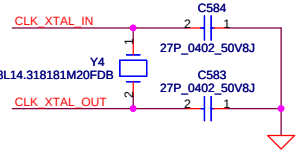


PIN 30	CPU_0	CPU_1
0(Default)	133MHz	133MHz
1	100MHz	100MHz









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RC Delay 18~25mS

close to RAM door

RC Delay 18~25mS

close to RAM door

32.768KHZ_12.5PF_Q13MC14610002

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

HDA for AUDIO

HDA for MDC

del R916 08/10

GPIO33 can not pull down
(manufacturing environments)

If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull
under door.

reserve C1228,C1229 for EMI request 08/23

reserve C1230 for EMI request 08/23

Have internal PD

7/14 Change

2008 Intel MOW36/MOW50
TDO:
Reserved on ES1 Sample
Mount R516, R517 on ES2 Sample

MP mount R689, R690,
R691, R692 and remove
others

enable iTPM: SPI_MOSI High

CRB 1.0 Change to 4.7K

add ME_EN reversed circuit 08/10

SATA for HDD1

SATA for ODD

2/10 SATA2, SATA3 not support on HM55

SATA for HDD2

1/6 Change from Port2 to Port4

11/18 SPI ROM Change to SA00002TO00

SPI ROM Footprint 150mil

11/18 SPI ROM Change to SA00002TO00

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U32B

REV1.0

IBEXPEAK-M_FCBGA107

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

20090512 add double mosfet prevent ATI M92 electric leakage

7/14 Change

change Q77 to R1116,R1117 08/12

Add R1114,R1115 ,del R758 08/12

del PEG_CLKREQ# 08/17

change Q59 bom @ to SG@ 08/17

change R1115 from 2.2K to 0 ohm 08/17

change to 0 ohm 08/12

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

2/10 PCIE7, PCIE8 not support on HM55

PCIECLKREQ(0,3,4,5,6,7)# Should have a 10K pull up to +3VALW,PCIECLKREQ(1,2),Should have a 10K pull up to +3VS

7/17: Change to +3VALW

7/14 Change

7/17 Del CLK_CARD_48M

Project ID		
ID1	ID0	Project
* 0	0	JV
0	1	Future

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(4) DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
(4) DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
(4) DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
(4) DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

(4) H_FDI_TXN[0..7] H_FDI_TXN[0..7]
(4) H_FDI_TXP[0..7] H_FDI_TXP[0..7]

7/17 R110 Change BOM Structure for follow check list p.23

+3VS
R538 8.2K_0402_5% PM_CLKRUN#
R110 10K_0402_5% XDP_DBRESET#

+3VALW
7/14 Change
R529 10K_0402_5% SUS_PWR_ACK
R503 8.2K_0402_5% PCH_GPIO72
R72 10K_0402_5% EC_SWI#
R55 1K_0402_5% PCH_PCIE_WAKE#
R69 @ 10K_0402_5% PM_SLP_LAN#

7/17 R72 KAV60 DEL

+1.05VS
R590 49.9_0402_1% DMI_COMP

U32C
REV1.0
DMI
FDI
System Power Management
IBEXPEAK-M_FCBGA107

DMI_HTX_PRX_N0	BC24	DMI0RXN	
DMI_HTX_PRX_N1	BJ22	DMI1RXN	
DMI_HTX_PRX_N2	AW20	DMI2RXN	
DMI_HTX_PRX_N3	BJ20	DMI3RXN	
DMI_HTX_PRX_P0	BD24	DMI0RXP	
DMI_HTX_PRX_P1	BG22	DMI1RXP	
DMI_HTX_PRX_P2	BA20	DMI2RXP	
DMI_HTX_PRX_P3	BG20	DMI3RXP	
DMI_PTX_HRX_N0	BE22	DMI0TXN	
DMI_PTX_HRX_N1	BF21	DMI1TXN	
DMI_PTX_HRX_N2	BD20	DMI2TXN	
DMI_PTX_HRX_N3	BE18	DMI3TXN	
DMI_PTX_HRX_P0	BD22	DMI0TXP	
DMI_PTX_HRX_P1	BH21	DMI1TXP	
DMI_PTX_HRX_P2	BC20	DMI2TXP	
DMI_PTX_HRX_P3	BD18	DMI3TXP	
	BH25	DMI_ZCOMP	
	BF25	DMI_IRCOMP	

FDI_RXN0	BA18	H_FDI_TXN0	
FDI_RXN1	BH17	H_FDI_TXN1	
FDI_RXN2	BD16	H_FDI_TXN2	
FDI_RXN3	BJ16	H_FDI_TXN3	
FDI_RXN4	BA16	H_FDI_TXN4	
FDI_RXN5	BE14	H_FDI_TXN5	
FDI_RXN6	BA14	H_FDI_TXN6	
FDI_RXN7	BC12	H_FDI_TXN7	
FDI_RXP0	BB18	H_FDI_TXP0	
FDI_RXP1	BF17	H_FDI_TXP1	
FDI_RXP2	BC16	H_FDI_TXP2	
FDI_RXP3	BG16	H_FDI_TXP3	
FDI_RXP4	AW16	H_FDI_TXP4	
FDI_RXP5	BD14	H_FDI_TXP5	
FDI_RXP6	BB14	H_FDI_TXP6	
FDI_RXP7	BD12	H_FDI_TXP7	
FDI_INT	BJ14	H_FDI_INT	(4)
FDI_FSYNC0	BF13	H_FDI_FSYNC0	(4)
FDI_FSYNC1	BH13	H_FDI_FSYNC1	(4)
FDI_LSYNC0	BJ12	H_FDI_LSYNC0	(4)
FDI_LSYNC1	BG14	H_FDI_LSYNC1	(4)

(5) XDP_DBRESET#	XDP_DBRESET#	T6	SYS_RESET#
SYS_PWROK R58 / VGATE R70	SYS_PWROK_R	M6	SYS_PWROK
SYS_PWROK		B17	PWROK
R877 0_0402_5%		K5	MEPWROK
LAN_RST#		A10	LAN_RST#
(5) PM_DRAM_PWRGD		D9	DRAMPWROK
PCH_RSMRST#		C16	RSMRST#
(38) SUS_PWR_ACK	SUS_PWR_ACK	M1	SUS_PWR_DN_ACK / GPIO30
(5,38) PBTN_OUT#	PBTN_OUT#	P5	PWRBTN#
(23,38) ACIN_R	PCH_ACIN	P7	ACPRESENT / GPIO31
	PCH_GPIO72	A6	BATLOW# / GPIO72
(38) EC_SWI#	EC_SWI#	F14	RI#

WAKE#	J12	PCH_PCIE_WAKE#	PCH_PCIE_WAKE# (33,36)
CLKRUN# / GPIO32	Y1	PM_CLKRUN#	PM_CLKRUN# (38)
SUS_STAT# / GPIO61	P8	PCH_GPIO61 @	PAD T4
SUSCLK / GPIO62	F3	PCH_GPIO62 @	PAD T7
SLP_S5# / GPIO63	F4		PM_SLP_S5# (38)
SLP_S4#	H7		PM_SLP_S4# (38)
SLP_S3#	P12		PM_SLP_S3# (38)
SLP_M#	K8	PM_SLP_M# @	PAD T2
TP23	N2	PM_SLP_DSW# @	PAD T8
PMSYNCH	BJ10		H_PM_SYNC (5)
SLP_LAN# / GPIO29	F6	PM_SLP_LAN#	

10/2 Intel suggestion change to 10K
7/14 Change
+3VALW R66 10K_0402_5% R1160 0_0402_5%
Change D4 to R1160 08/21
change EC_ACIN net name to ACIN_R 08/21
del R917 08/21

R37 @ 0_0402_5%
+3VS
U2 NC7SZ08P5X_NL_SC70-5
SYS_PWROK EC_PWROK (38)
VGATE (12,54)

SYS_PWROK R31 10K_0402_5%
EC_PWROK R41 10K_0402_5%
LAN_RST# R506 10K_0402_5%
No used Integrated LAN, connecting LAN_RST# to GND

R30 @ 0_0402_5%
Q4 MMBT3906_SOT23-3
PCH_RSMRST# EC_RSMRST# (38)
R32 10K_0402_5%
R27 4.7K_0402_5% +3VALW
7/14 Change
D3A BAV99DW-7_SOT363
D3B BAV99DW-7_SOT363
R39 2.2K_0402_5%

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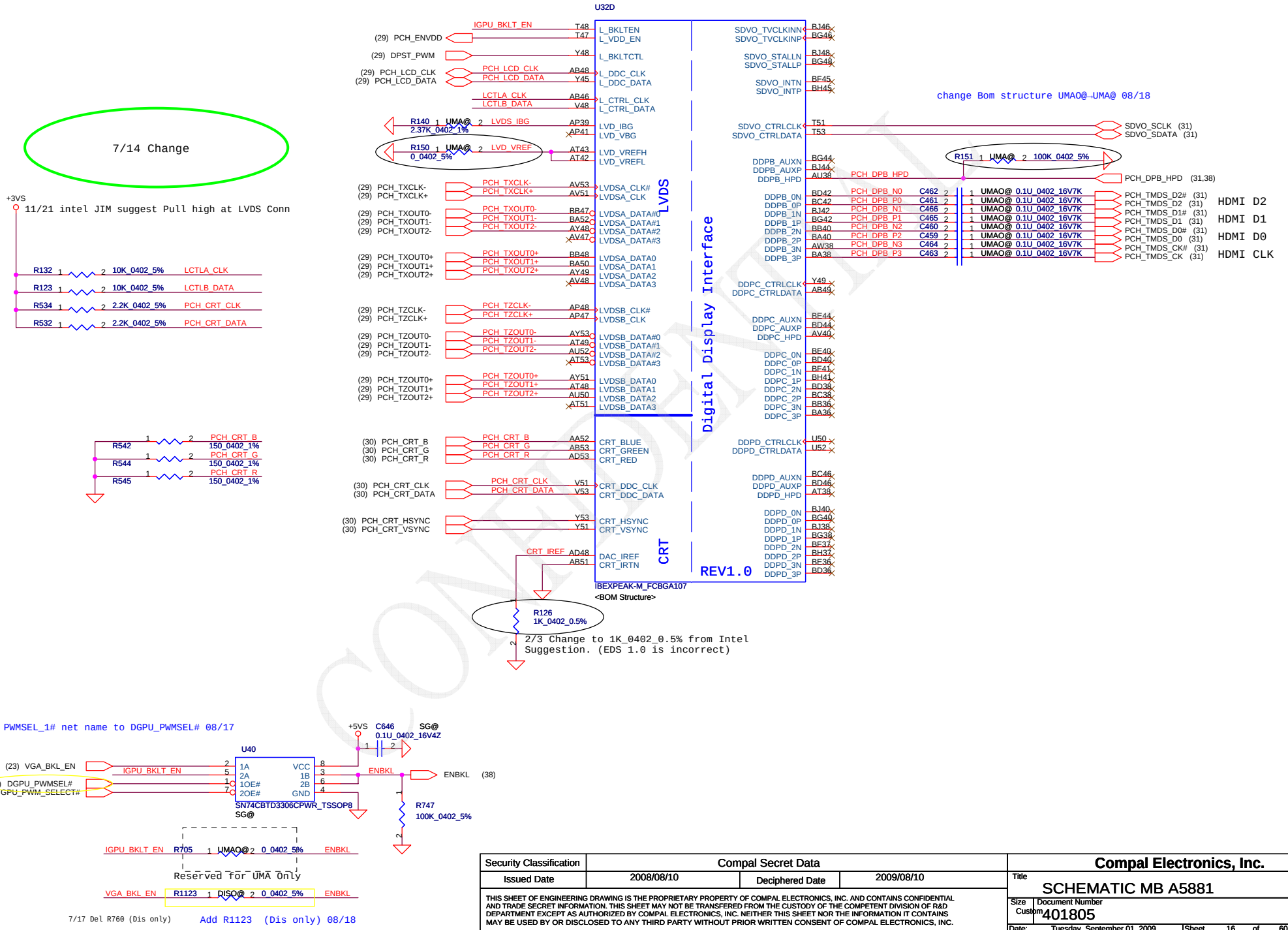

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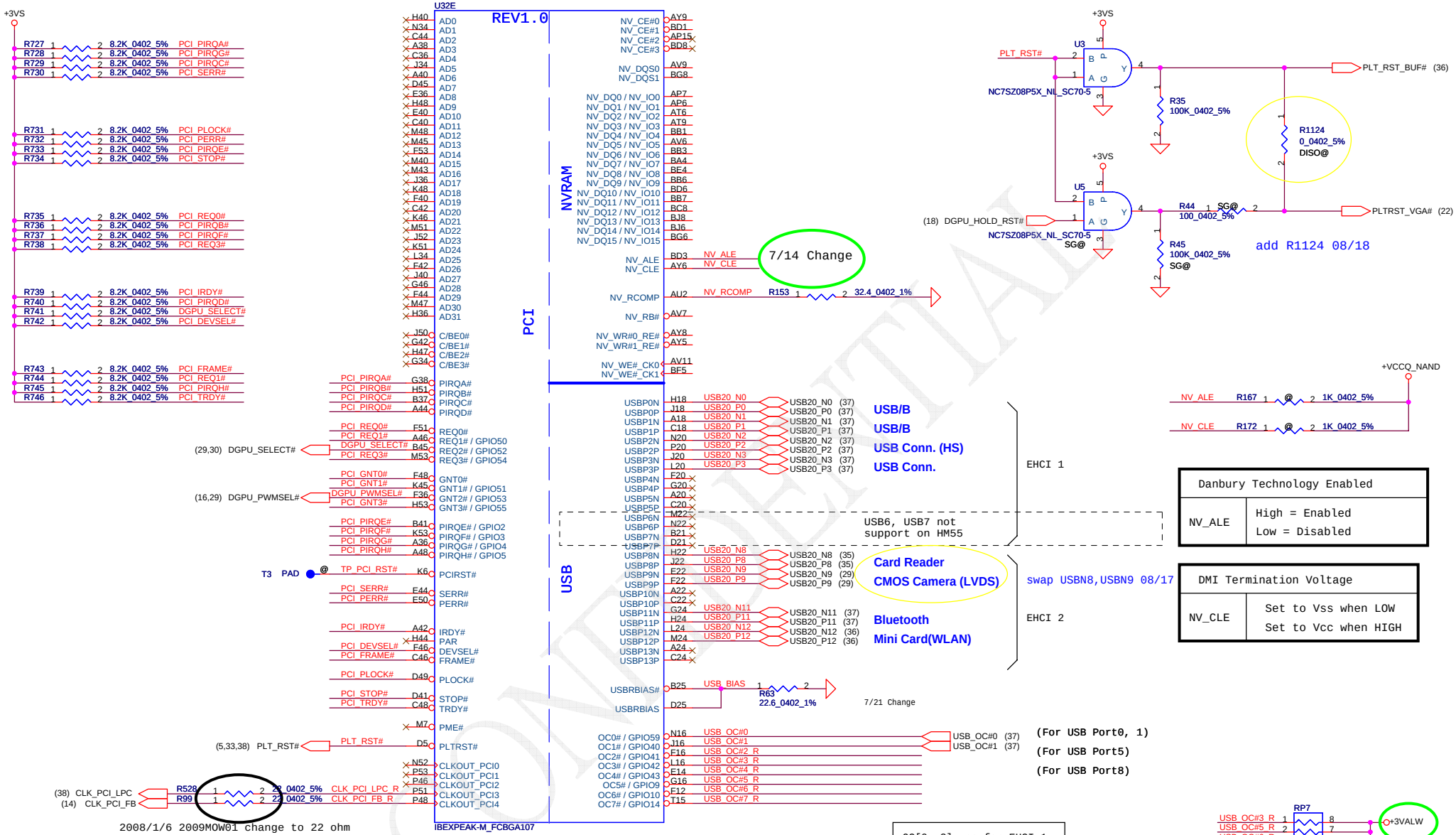

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI *

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

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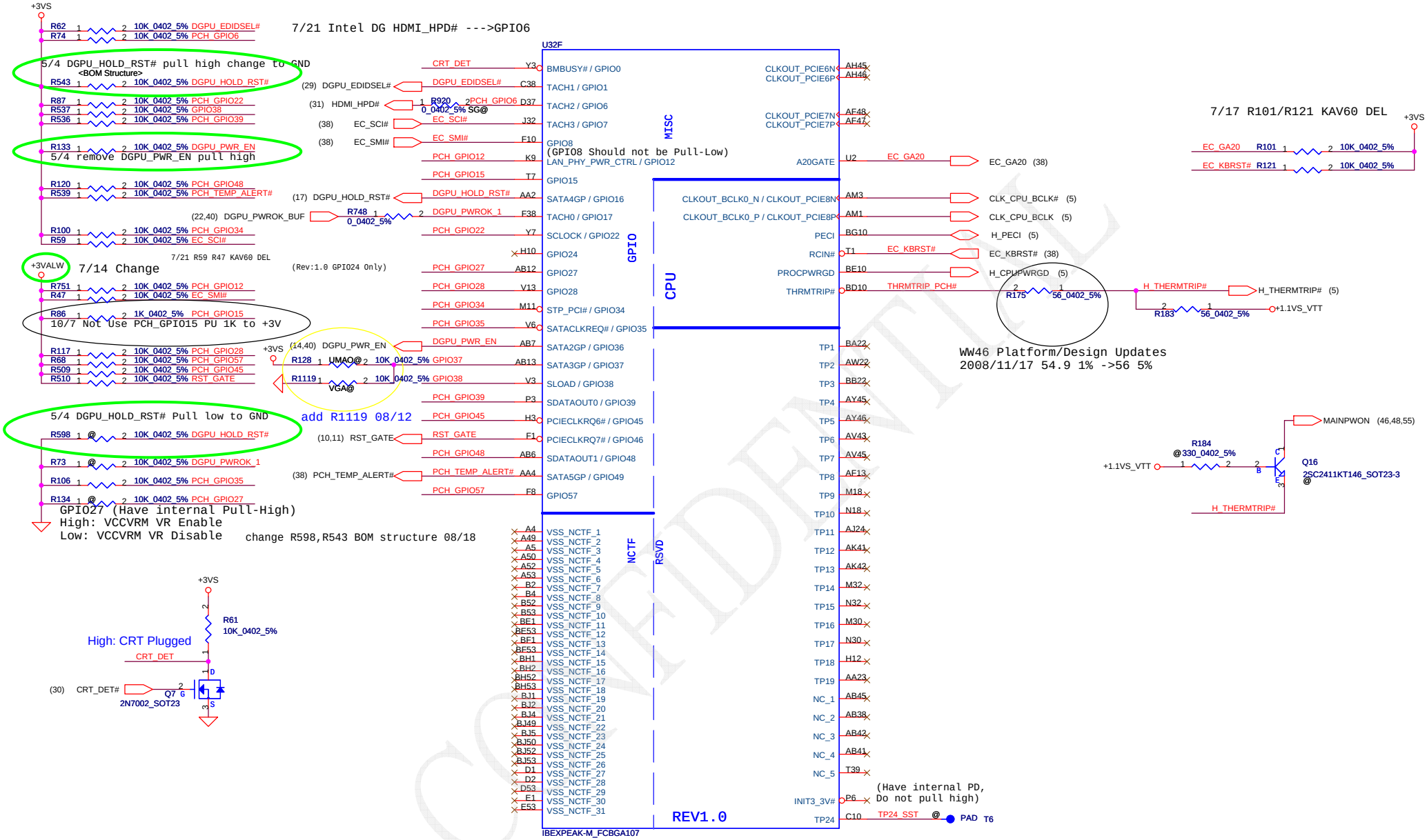

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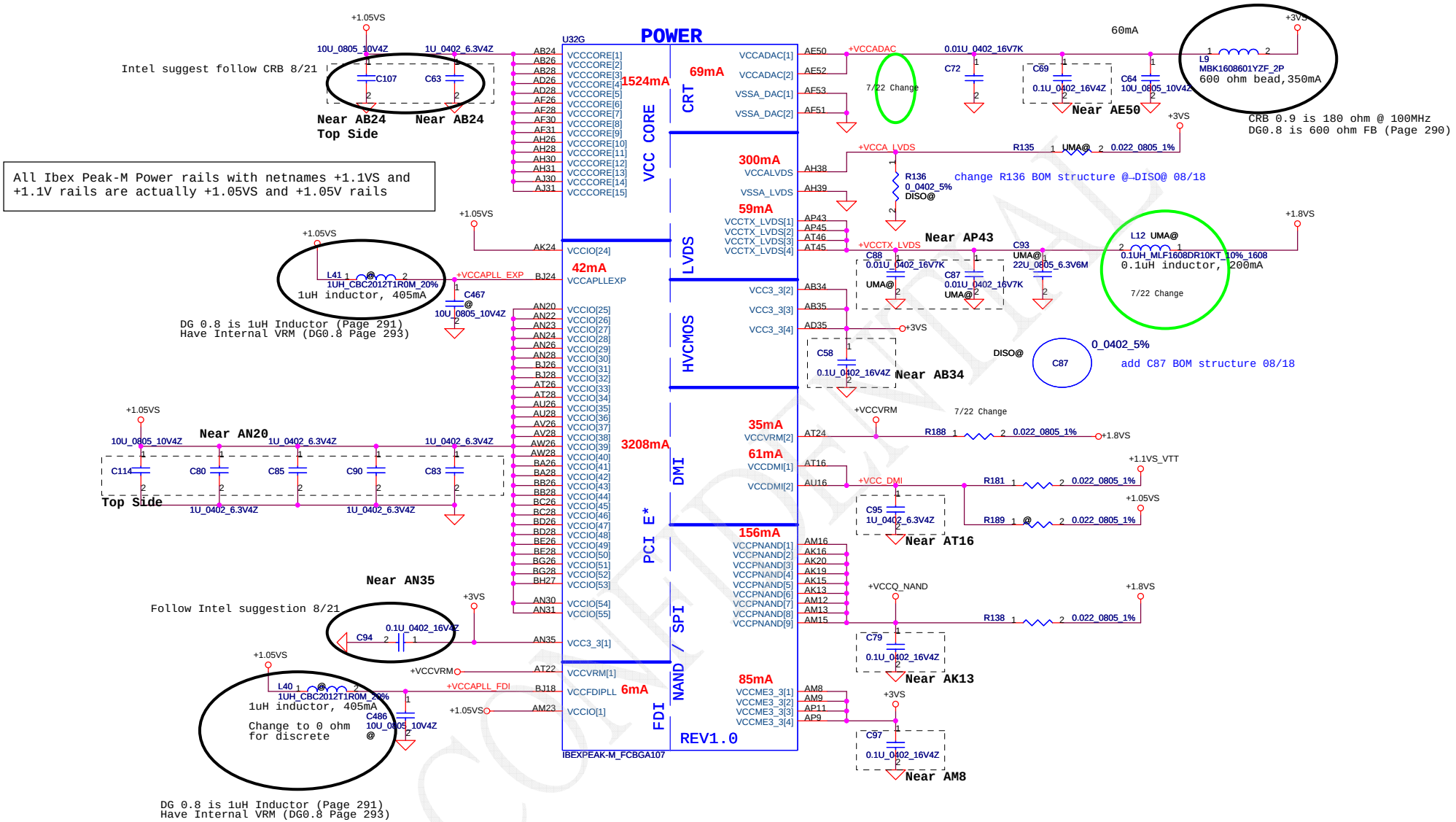

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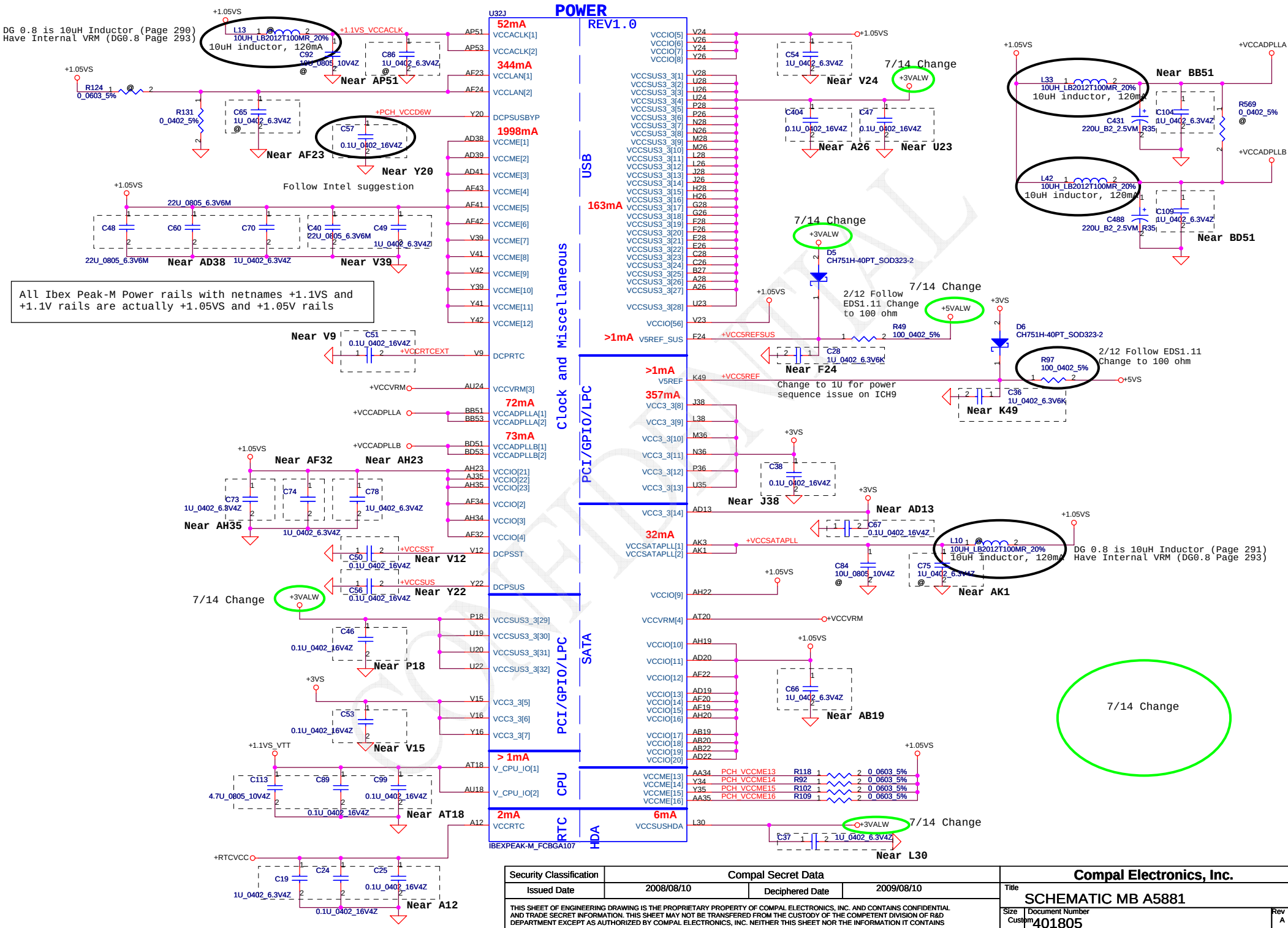

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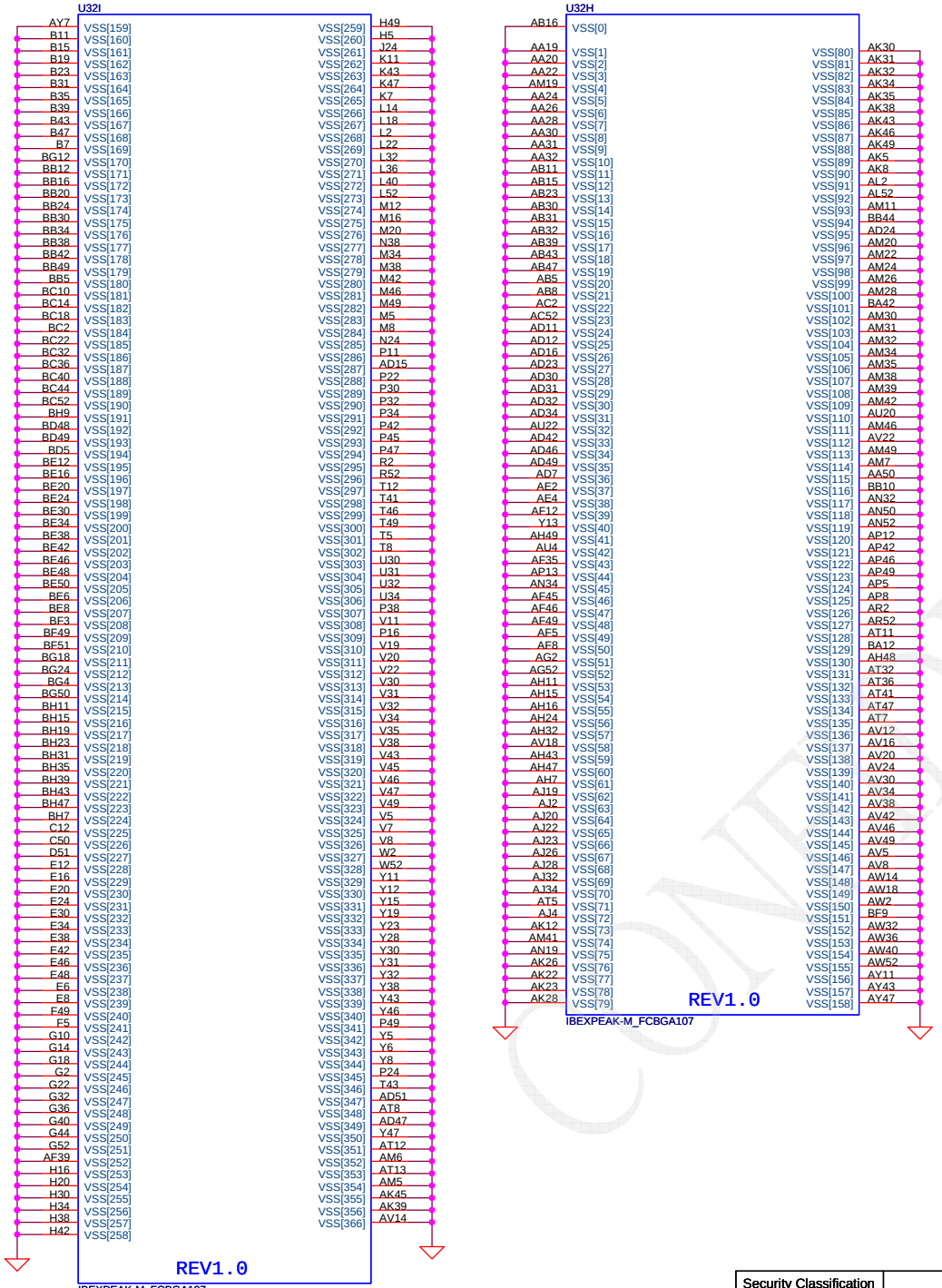

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PARK@ U75

216-0774007 All PARK PRO M2 0FA

U75A

PCI EXPRESS INTERFACE

(4) PEG_HTX_C_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_GTX_HRX_P0	C932	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P0 (4)
(4) PEG_HTX_C_GRX_N0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_GTX_HRX_N0	C933	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N0 (4)
(4) PEG_HTX_C_GRX_P1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_GTX_HRX_P1	C934	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P1 (4)
(4) PEG_HTX_C_GRX_N1	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_GTX_HRX_N1	C935	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N1 (4)
(4) PEG_HTX_C_GRX_P2	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_GTX_HRX_P2	C936	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P2 (4)
(4) PEG_HTX_C_GRX_N2	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_GTX_HRX_N2	C937	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N2 (4)
(4) PEG_HTX_C_GRX_P3	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_GTX_HRX_P3	C938	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P3 (4)
(4) PEG_HTX_C_GRX_N3	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_GTX_HRX_N3	C939	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N3 (4)
(4) PEG_HTX_C_GRX_P4	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_GTX_HRX_P4	C940	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P4 (4)
(4) PEG_HTX_C_GRX_N4	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_GTX_HRX_N4	C941	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N4 (4)
(4) PEG_HTX_C_GRX_P5	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_GTX_HRX_P5	C942	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P5 (4)
(4) PEG_HTX_C_GRX_N5	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_GTX_HRX_N5	C943	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N5 (4)
(4) PEG_HTX_C_GRX_P6	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_GTX_HRX_P6	C944	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P6 (4)
(4) PEG_HTX_C_GRX_N6	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_GTX_HRX_N6	C945	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N6 (4)
(4) PEG_HTX_C_GRX_P7	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_GTX_HRX_P7	C946	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P7 (4)
(4) PEG_HTX_C_GRX_N7	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_GTX_HRX_N7	C947	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N7 (4)
(4) PEG_HTX_C_GRX_P8	N38	PCIE_RX8P	PCIE_TX8P	N33	PEG_GTX_HRX_P8	C948	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P8 (4)
(4) PEG_HTX_C_GRX_N8	M37	PCIE_RX8N	PCIE_TX8N	N32	PEG_GTX_HRX_N8	C949	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N8 (4)
(4) PEG_HTX_C_GRX_P9	M35	PCIE_RX9P	PCIE_TX9P	N30	PEG_GTX_HRX_P9	C950	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P9 (4)
(4) PEG_HTX_C_GRX_N9	L36	PCIE_RX9N	PCIE_TX9N	N29	PEG_GTX_HRX_N9	C951	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N9 (4)
(4) PEG_HTX_C_GRX_P10	L38	PCIE_RX10P	PCIE_TX10P	L33	PEG_GTX_HRX_P10	C952	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P10 (4)
(4) PEG_HTX_C_GRX_N10	K37	PCIE_RX10N	PCIE_TX10N	L32	PEG_GTX_HRX_N10	C953	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N10 (4)
(4) PEG_HTX_C_GRX_P11	K35	PCIE_RX11P	PCIE_TX11P	L30	PEG_GTX_HRX_P11	C954	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P11 (4)
(4) PEG_HTX_C_GRX_N11	J36	PCIE_RX11N	PCIE_TX11N	L29	PEG_GTX_HRX_N11	C955	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N11 (4)
(4) PEG_HTX_C_GRX_P12	J38	PCIE_RX12P	PCIE_TX12P	K33	PEG_GTX_HRX_P12	C956	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P12 (4)
(4) PEG_HTX_C_GRX_N12	H37	PCIE_RX12N	PCIE_TX12N	K32	PEG_GTX_HRX_N12	C957	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N12 (4)
(4) PEG_HTX_C_GRX_P13	H35	PCIE_RX13P	PCIE_TX13P	J33	PEG_GTX_HRX_P13	C958	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P13 (4)
(4) PEG_HTX_C_GRX_N13	G36	PCIE_RX13N	PCIE_TX13N	J32	PEG_GTX_HRX_N13	C959	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N13 (4)
(4) PEG_HTX_C_GRX_P14	G38	PCIE_RX14P	PCIE_TX14P	K30	PEG_GTX_HRX_P14	C960	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P14 (4)
(4) PEG_HTX_C_GRX_N14	F37	PCIE_RX14N	PCIE_TX14N	K29	PEG_GTX_HRX_N14	C961	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N14 (4)
(4) PEG_HTX_C_GRX_P15	F35	PCIE_RX15P	PCIE_TX15P	H33	PEG_GTX_HRX_P15	C962	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P15 (4)
(4) PEG_HTX_C_GRX_N15	E37	PCIE_RX15N	PCIE_TX15N	H32	PEG_GTX_HRX_N15	C963	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N15 (4)

CLOCK

(14) CLK_PEG_VGA — AB35 PCIE_REFCLKP
(14) CLK_PEG_VGA# — AA36 PCIE_REFCLKN

AJ21 NC#1
AK21 NC#2
AH16 NC_PWRGOOD

(18,40) DGPU_PWROK_BUF — R962 0_0402_5% @ — DGPU_PWROK

(17) PLTRST_VGA# — AA30 PERSTB

8/10 change net name

R964 10K_0402_1% VGA@

Mannhatton Only
NC in M96

CALIBRATION

PCIE_CALRP — Y30 — R961 1 VGA@ 2 1.27K_0402_1%
PCIE_CALRN — Y29 — R963 1 VGA@ 2 2K_0402_1%

+1.1VSDGPU

216-0772000 MADISON PRO FCBFA OFA
MAD@

M96 P/N : SA00002UQ50 (S IC 216-0729042-00 A13 M96 FCBGA962 0FA)
M92 P/N : SA00002YX10 (S IC 216-0728014 A12 M92-M2 XT FCBGA 0FA)

MADISON P/N:SA00003M300 (S IC 216-0772000 MADISON PRO FCBGA 0FA)
PARK P/N:SA00003MC00 (S IC 216-0774007 All PARK PRO M2 0FA)

add for DPST support.

U75G

LVDS CONTROL

VARY_BL — AK27 — R959 10K_0402_5% VGA@ — VGA_PNL_PWM (29)
DIGON — AJ27 — R960 10K_0402_5% VGA@ — ENVDD (29)

TXCLK_UP_DPF3P	AK35	VGA_TZCLK+	VGA_TZCLK+ (29)
TXCLK_UN_DPF3N	AL36	VGA_TZCLK-	VGA_TZCLK- (29)
TXOUT_U0P_DPF2P	AJ38	VGA_TZOUT0+	VGA_TZOUT0+ (29)
TXOUT_U0N_DPF2N	AK37	VGA_TZOUT0-	VGA_TZOUT0- (29)
TXOUT_U1P_DPF1P	AH35	VGA_TZOUT1+	VGA_TZOUT1+ (29)
TXOUT_U1N_DPF1N	AJ36	VGA_TZOUT1-	VGA_TZOUT1- (29)
TXOUT_U2P_DPF0P	AG38	VGA_TZOUT2+	VGA_TZOUT2+ (29)
TXOUT_U2N_DPF0N	AH37	VGA_TZOUT2-	VGA_TZOUT2- (29)
TXOUT_U3P	AF35	T15	
TXOUT_U3N	AG36	T14	

LVTMDP

@
@

TXCLK_LP_DPE3P	AP34	VGA_TXCLK+	VGA_TXCLK+ (29)
TXCLK_LN_DPE3N	AR34	VGA_TXCLK-	VGA_TXCLK- (29)
TXOUT_L0P_DPE2P	AW37	VGA_TXOUT0+	VGA_TXOUT0+ (29)
TXOUT_L0N_DPE2N	AU35	VGA_TXOUT0-	VGA_TXOUT0- (29)
TXOUT_L1P_DPE1P	AR37	VGA_TXOUT1+	VGA_TXOUT1+ (29)
TXOUT_L1N_DPE1N	AU39	VGA_TXOUT1-	VGA_TXOUT1- (29)
TXOUT_L2P_DPE0P	AP35	VGA_TXOUT2+	VGA_TXOUT2+ (29)
TXOUT_L2N_DPE0N	AR35	VGA_TXOUT2-	VGA_TXOUT2- (29)
TXOUT_L3P	AN36	T16	
TXOUT_L3N	AP37	T17	

@
@

216-0772000 MADISON PRO FCBFA OFA
MAD@

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Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF _CLK_PM_EN	GPIO22	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
CCBYPASS	GENERICC		0
SMS_EN_HARD	H2SYNC		0
VIP_DEVICE _STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

Location / VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	O	O	O	O
HYNIX	1	O	O	O

External VGA Thermal Sensor

U76 ADM1032ARMZ-2REEL_MSOP8 VGA@

+3VS_DELAY

8/10 change Circuit

Q100 SI2301BDS_SOT23 VGA@ 100mA

Q101 SSM3K7002FU_SC70-3

Q102 SSM3K7002FU_SC70-3

change R1107 from 2.2K to 10K 08/27

Madison & Park Power Up

+3VS_DELAY

VGA_CORE (VDDC)

+1.8VS

FLASH ROM

del U77,R1011,R1012,C988 08/12

HDMI

CRT

M96 only

change EC_ACIN net name to ACIN_R 08/21

8/10 change net name

del R982,R981,R980,R979 08/12

Do not PU R177 for GPIO22 if not implement external flash ROM

del C984 08/18

change R1010 from 0603 to 0402 08/18

add R1125 08/18

change to 0402 08/12

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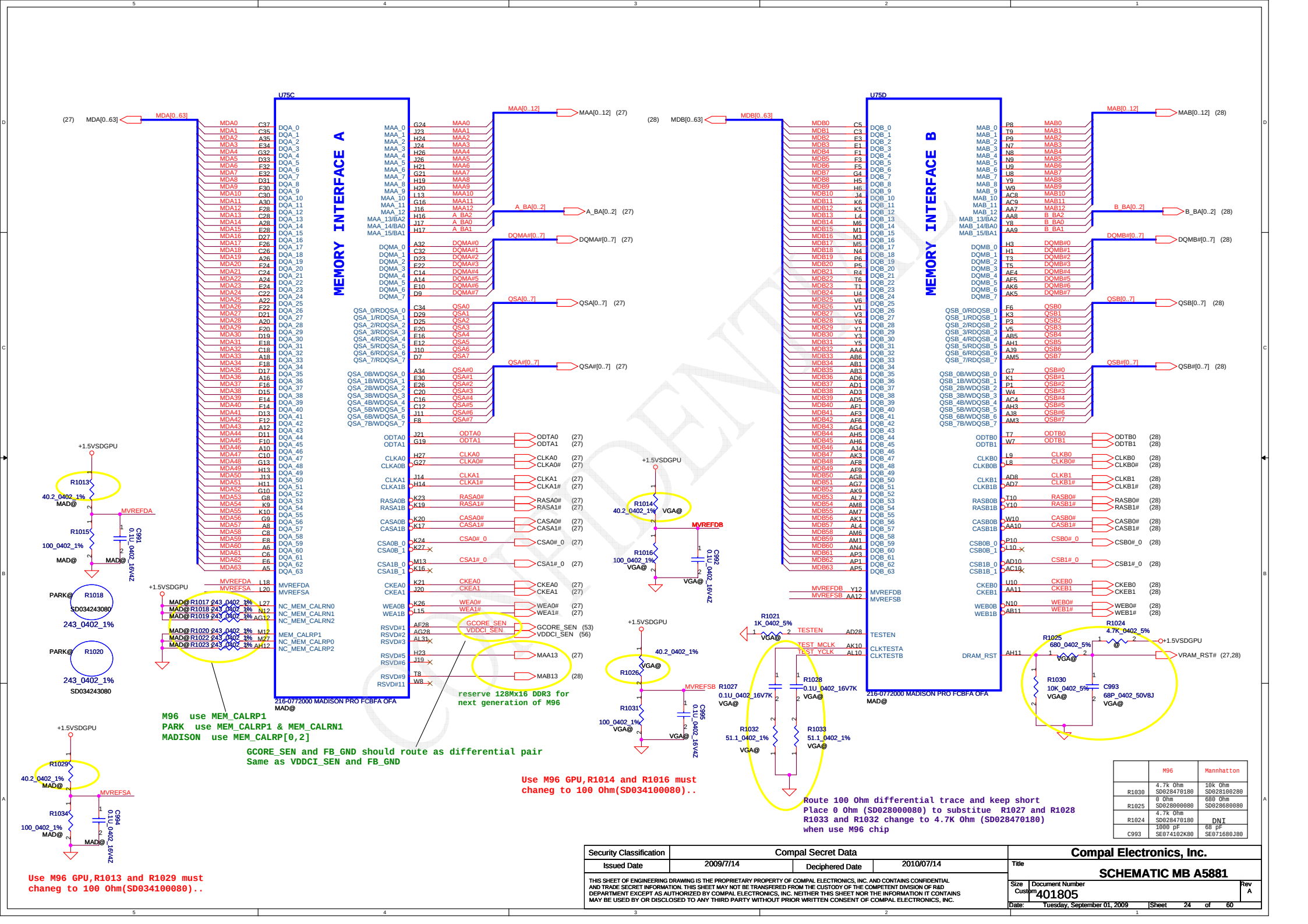

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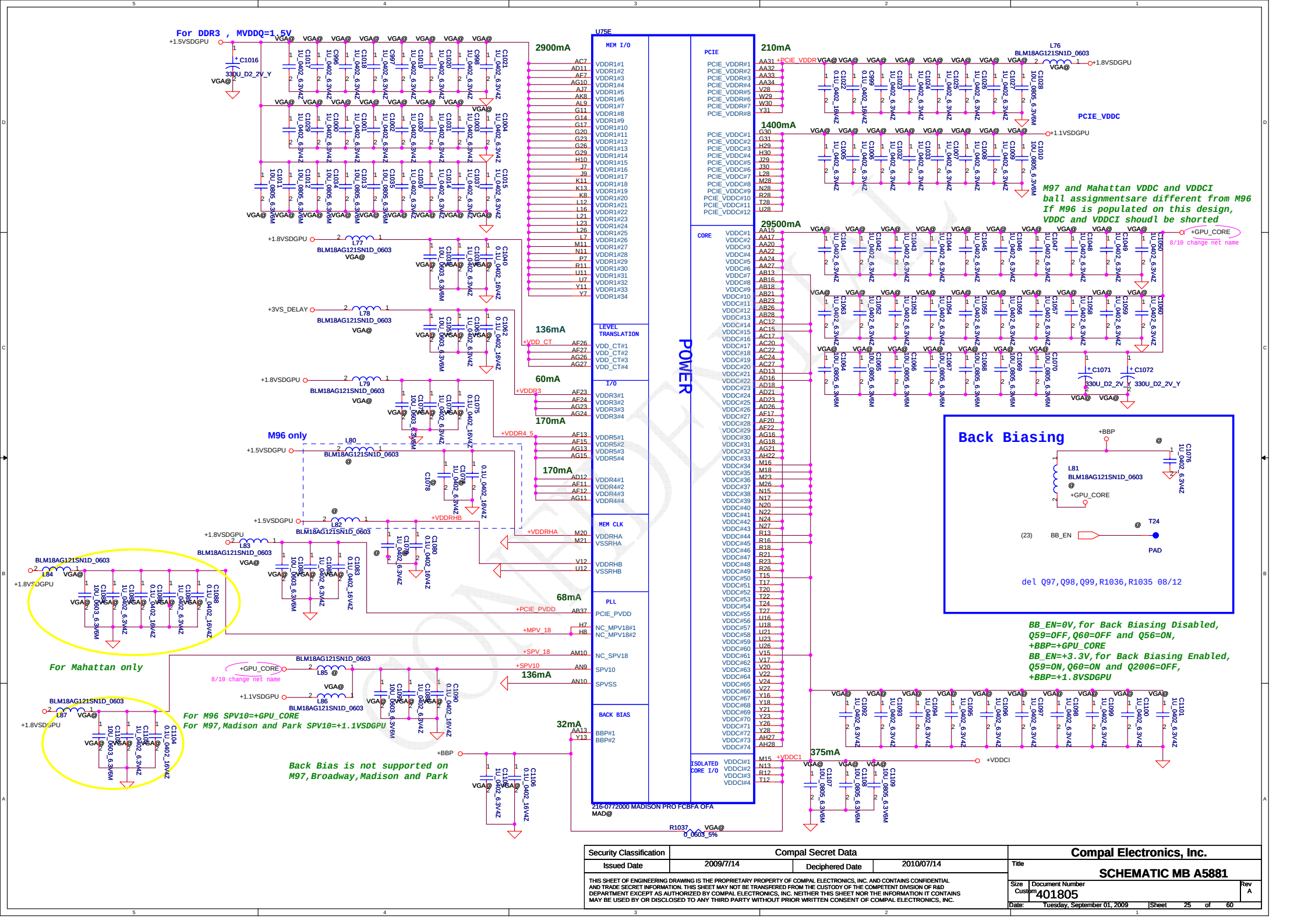

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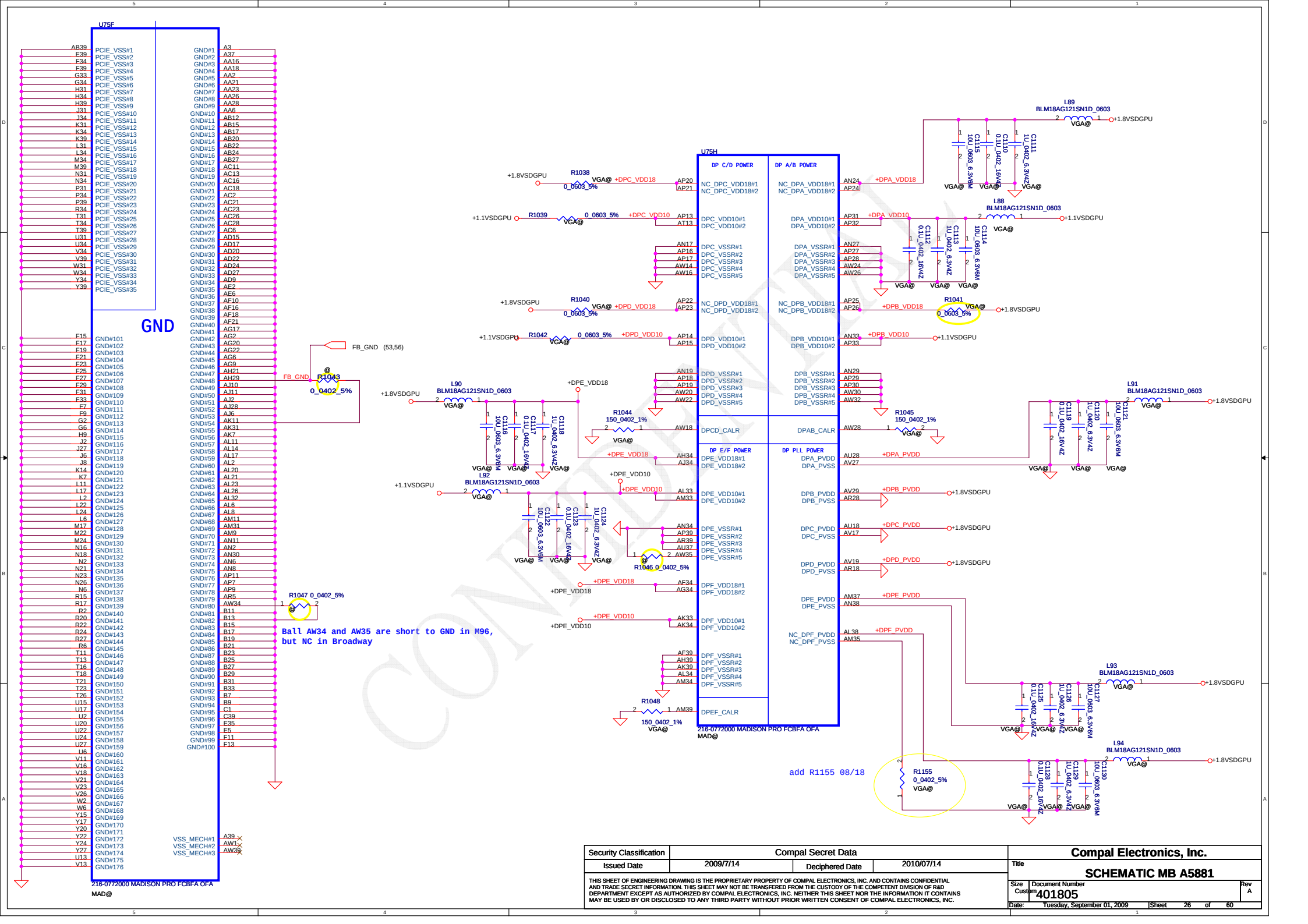
U75F
GND
216-0772000 MADISON PRO FCBFA OFA
MAD@
U75H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
216-0772000 MADISON PRO FCBFA OFA
MAD@
FB_GND (53,56)
R1043 @ 0_0402_5%
R1047 0_0402_5%
Ball AW34 and AW35 are short to GND in M96, but NC in Broadway
R1046 @ 0_0402_5%
add R1155 08/18
R1155 0_0402_5% VGA@
L89 BLM18AG121SN1D_0603
L88 BLM18AG121SN1D_0603
L90 BLM18AG121SN1D_0603
L91 BLM18AG121SN1D_0603
L92 BLM18AG121SN1D_0603
L93 BLM18AG121SN1D_0603
L94 BLM18AG121SN1D_0603
+1.8VSDGPU
+1.1VSDGPU
+1.1VSDGPU
+1.8VSDGPU
+DPA_VDD18
+DPA_VDD10
+DPB_VDD18
+DPB_VDD10
+DPA_PVDD
+DPB_PVDD
+DPC_PVDD
+DPD_PVDD
+DPE_PVDD
+DPF_PVDD
+DPC_VDD18
+DPC_VDD10
+DPD_VDD18
+DPD_VDD10
+DPE_VDD18
+DPE_VDD10
R1038 0_0603_5%
R1039 0_0603_5%
R1040 0_0603_5%
R1041 0_0603_5%
R1042 0_0603_5%
R1044 150_0402_1%
R1045 150_0402_1%
R1048 150_0402_1%
VGA@
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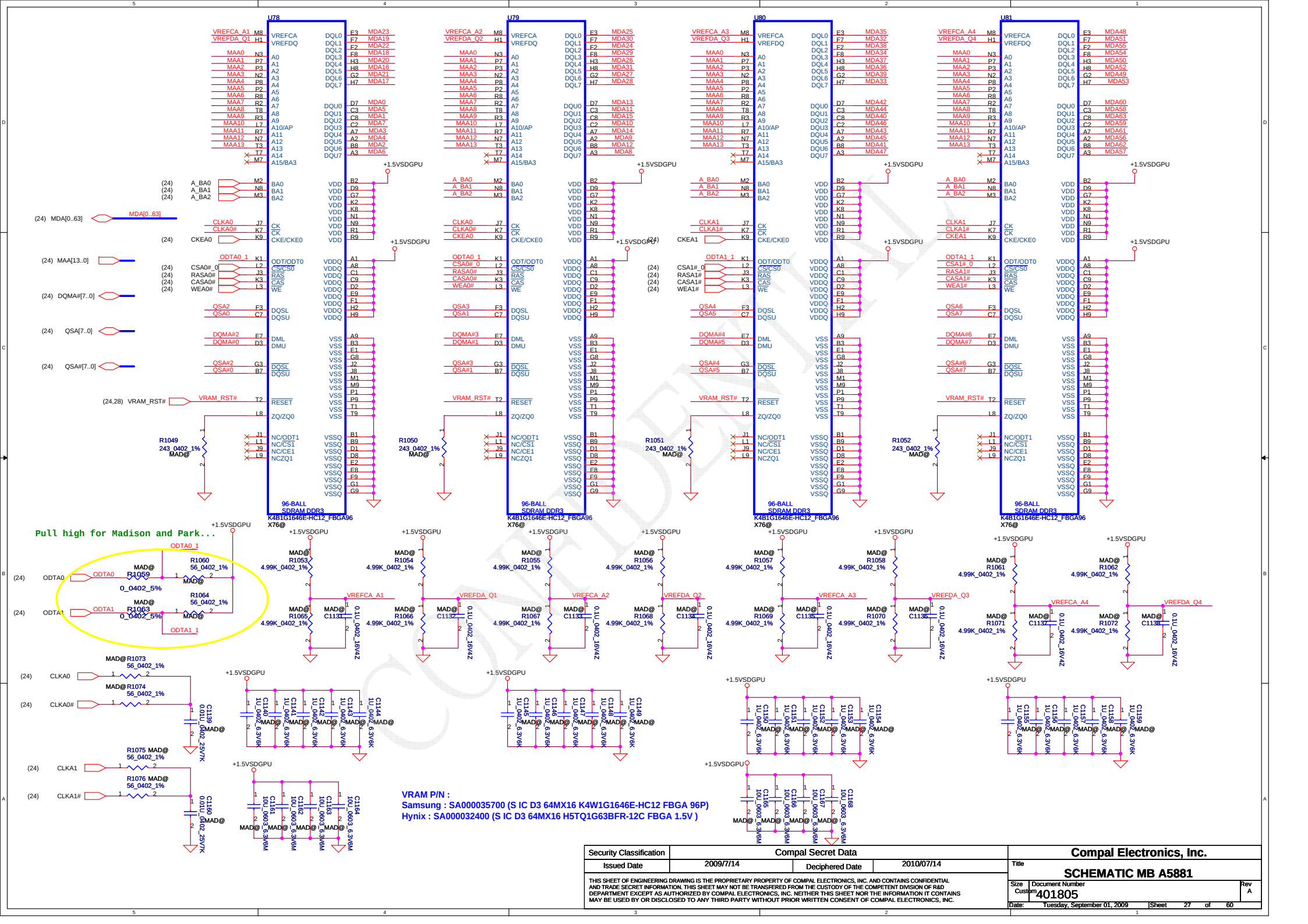
U78
U79
U80
U81
96-BALL SDRAM DDR3
K4B1G1646E-HC12_FBGA96
X76@
+1.5VSDGPU
Pull high for Madison and Park...
VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
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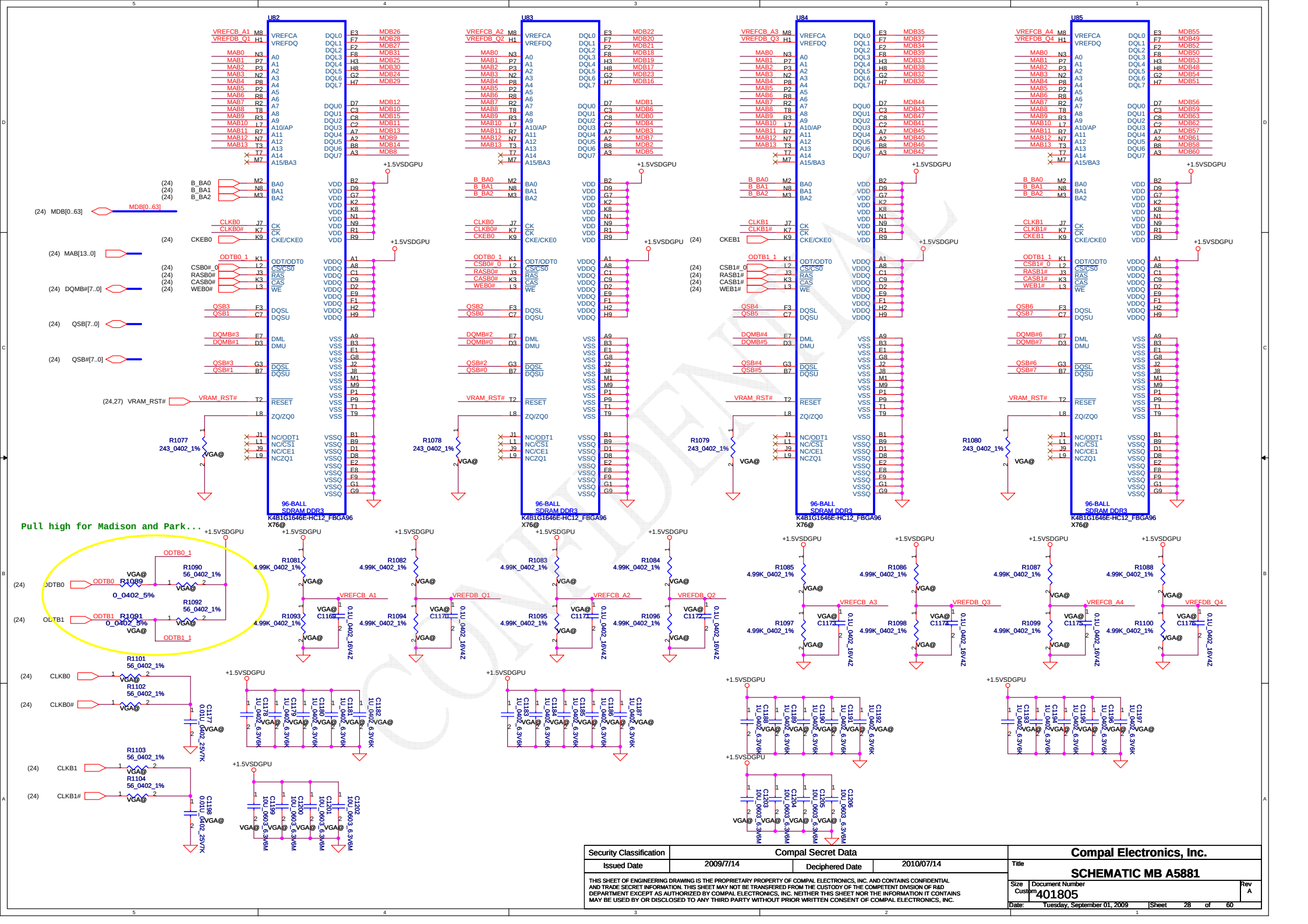

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LCD POWER CIRCUIT

7/14 Change

W=60mils

W=60mils

LCD/LED PANEL Conn.

W=40mils

UMA ONLY

7/21 DEL R464 R878

del R707 08/17

2009/04/30
R709 move to R710

Reserved for UMA Only

change PWMSEL_1# net name to DGPU_PWMSEL# 08/17

add R1126 DISO 08/18

SEL=LOW, B1
SEL=High, B2

TS3DV520ERHUR_WQFN56_11X5

删除跨頁符號 08/17

SG For LVDS

SEL=LOW, B1
SEL=High, B2

TS3DV520ERHUR_WQFN56_11X5

add R1129,R1130 DISO 08/18

add R1127,R1128 DISO 08/18

5/4 PCH_LCD_CLK& PCH_LCD_DATA
Pull high 2.2K change to 4.7K

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CRT Connector

Change L31,L28,L26,C415,C411,C405,C412,C409,C401
BOM structure UMA@→POP 08/18

Change to 0 ohm for Discrete

Change to 15pf for Discrete

Change to 12pf for Discrete

W=40mils

W=40mils

D26 DAN217_SC59 D25 DAN217_SC59 D24 DAN217_SC59

+5VS +R_CRT_VCC +CRT_VCC

D2 RB491D_SC59-3 F1 1.1A_6VDC_FUSE C399 0.1U_0402_16V4Z

+3VS

CRT_R CRT_G CRT_B

L31 L28 L26 0_0805_5%

CRT_R_1 CRT_G_1 CRT_B_1

L32 L29 L27 FCM2012CF-800T06_2P

CRT_R_2 CRT_G_2 CRT_B_2

R523 150_0402_1% R515 150_0402_1% R508 150_0402_1%

C414 C406 C403 10P_0402_50V8J

C415 C411 C405 22P_0402_50V8J

C412 10P_0402_50V8J C409 10P_0402_50V8J C401 10P_0402_50V8J

JCRT1 SUYIN_070546FR015S233ZR CONN@

CRT_DET# (18)

C16 100P_0402_50V8J C26 68P_0402_50V8J C11 68P_0402_50V8J

DSUB_12 DSUB_15

R29 100K_0402_5%

+CRT_VCC

C33 0.1U_0402_16V4Z R56 10K_0402_5%

U6 74AHCT1G125GW_SOT353-5

CRT_HSYNC CRT_HSYNC_1

L3 22_0402_5% L2 22_0402_5%

CRT_HSYNC_2 CRT_VSYNC_2

C21 10P_0402_50V8J C14 10P_0402_50V8J

C20 0.1U_0402_16V4Z

U4 74AHCT1G125GW_SOT353-5

CRT_VSYNC CRT_VSYNC_1

DISO@ C643 C640 C641 C642 0.1U_0402_16V4Z

DISO@ U67 PI3V712-AZLEX_TQFN32_6X3~D

PCH DDC PU 2.2K
on Page 17

+3VS

C643 C640 C641 C642 0.1U_0402_16V4Z SG@

U67 SG@

+3VS

VDD VDD VDD VDD VDD

A0 A1 A2 A3 A4

CRT_R CRT_G CRT_B CRT_HSYNC CRT_VSYNC

add R1133,R1134,R1135,R1136 08/18

(23) VGA_CRT_R (23) VGA_CRT_G (23) VGA_CRT_B (23) VGA_CRT_HSYNC (23) VGA_CRT_VSYNC

0B1 1B1 2B1 3B1 4B1

A5 A6

DSUB_12_R DSUB_15_R

SEL1

DGPU_SELECT_R#

R1133 SG@ 0_0402_5%

R1135 DISO@ 0_0402_5%

DGPU_SELECT# (17,29)

(23) VGA_DDC_DATA (23) VGA_DDC_CLK

5B1 6B1

SEL2

DGPU_EDIDSEL_R_R#

R1134 SG@ 0_0402_5%

DGPU_EDIDSEL_R# (29,31)

pull-up 2.2k on PCH side

pull-up 2k on GPU SIDE

(16) PCH_CRT_R (16) PCH_CRT_G (16) PCH_CRT_B (16) PCH_CRT_HSYNC (16) PCH_CRT_VSYNC

0B2 1B2 2B2 3B2 4B2

GND GND GND GND GPAD

R1136 0_0402_5% DISO@

(16) PCH_CRT_DATA (16) PCH_CRT_CLK

5B2 6B2

PI3V712-AZLEX_TQFN32_6X3~D

SEL1->Port 0~4 SEL2->Port5~6
(L--B1 Output H--B2 Output)

7/17 Del R895 R897 DIS only@
add R1131,R1132 DIS only 08/18
del R1131,R1132 08/19

Check bom

+3VS

PCH_CRT_DATA R896 UMAQ@ 0_0402_5% DSUB_12_R

PCH_CRT_CLK R898 UMAQ@ 0_0402_5% DSUB_15_R

Q76A 2N7002DW-T/R7_SOT363-6

Q76B 2N7002DW-T/R7_SOT363-6

+CRT_VCC

R893 2.2K_0402_5% R894 2.2K_0402_5%

Reserved for UMA only

PCH_CRT_R R699 UMAQ@ 0_0402_5% CRT_R
PCH_CRT_G R700 UMAQ@ 0_0402_5% CRT_G
PCH_CRT_B R701 UMAQ@ 0_0402_5% CRT_B
PCH_CRT_HSYNC R702 UMAQ@ 0_0402_5% CRT_HSYNC
PCH_CRT_VSYNC R703 UMAQ@ 0_0402_5% CRT_VSYNC

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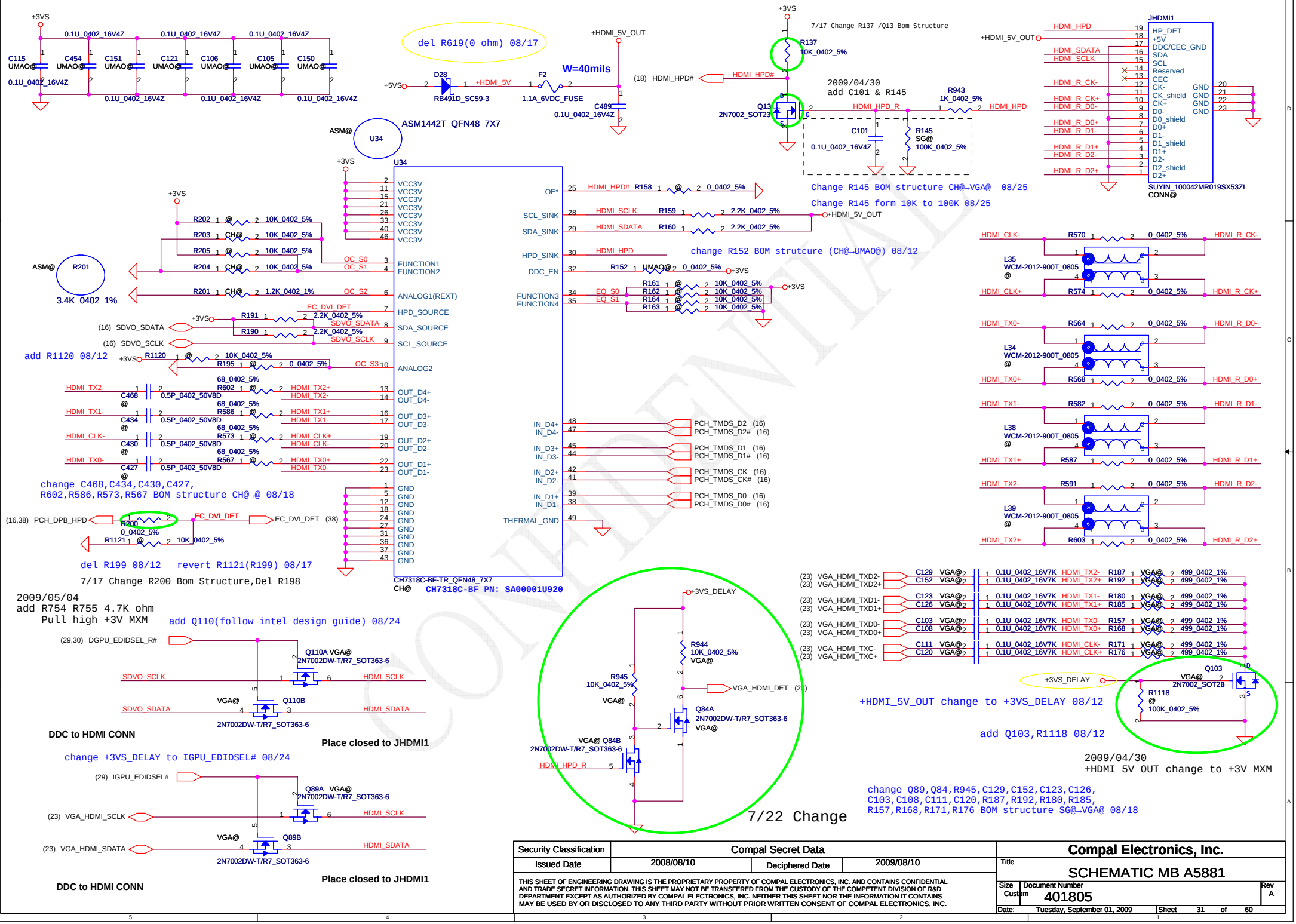
B	401805	A

Date: Tuesday, September 01, 2009 Sheet 30 of 60



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Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: SCHEMATIC MB A5881

Size	Document Number	Rev
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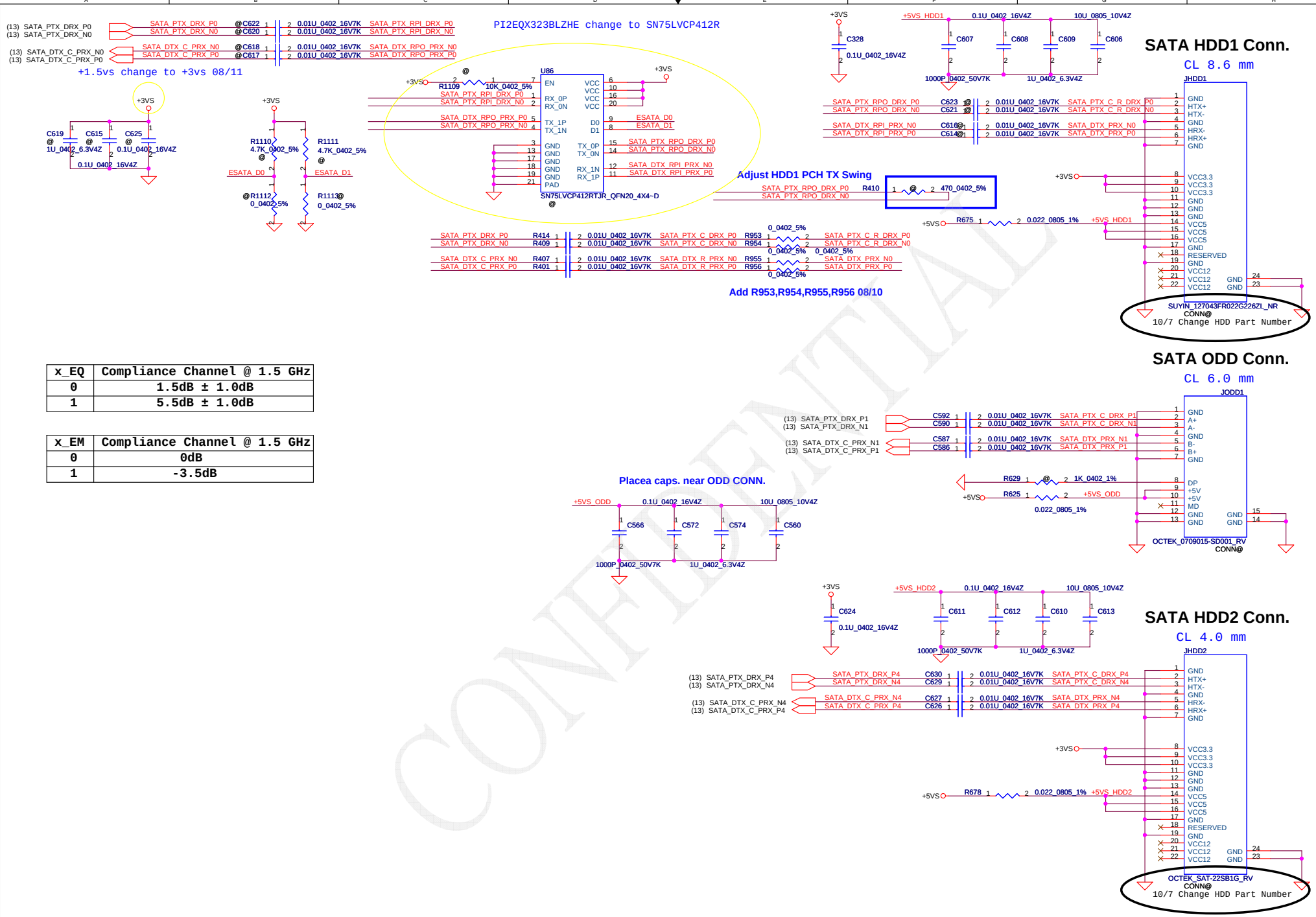

x_EQ	Compliance Channel @ 1.5 GHz
0	1.5dB ± 1.0dB
1	5.5dB ± 1.0dB

x_EM	Compliance Channel @ 1.5 GHz
0	0dB
1	-3.5dB

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

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Size	Document Number	Rev
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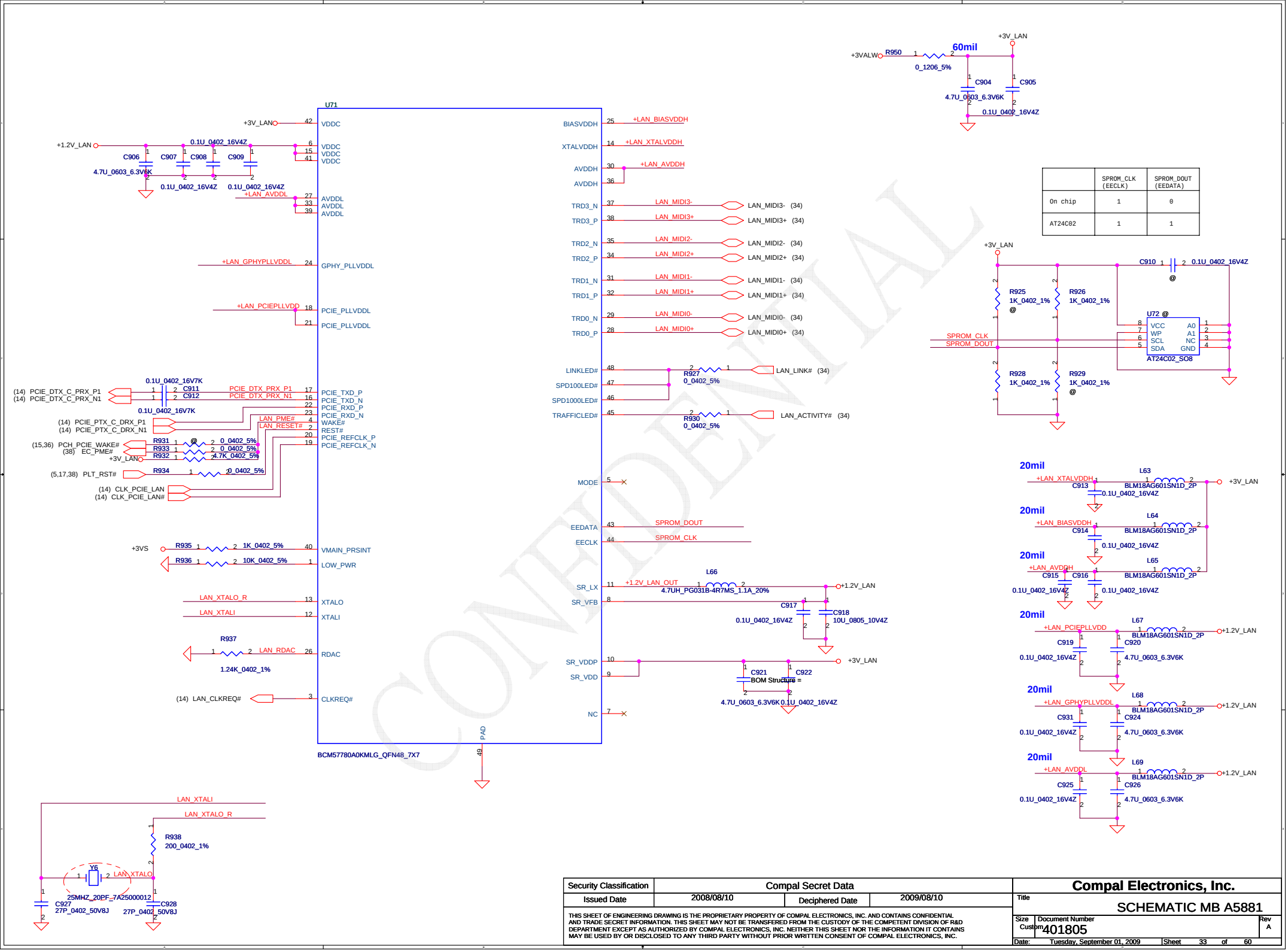

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

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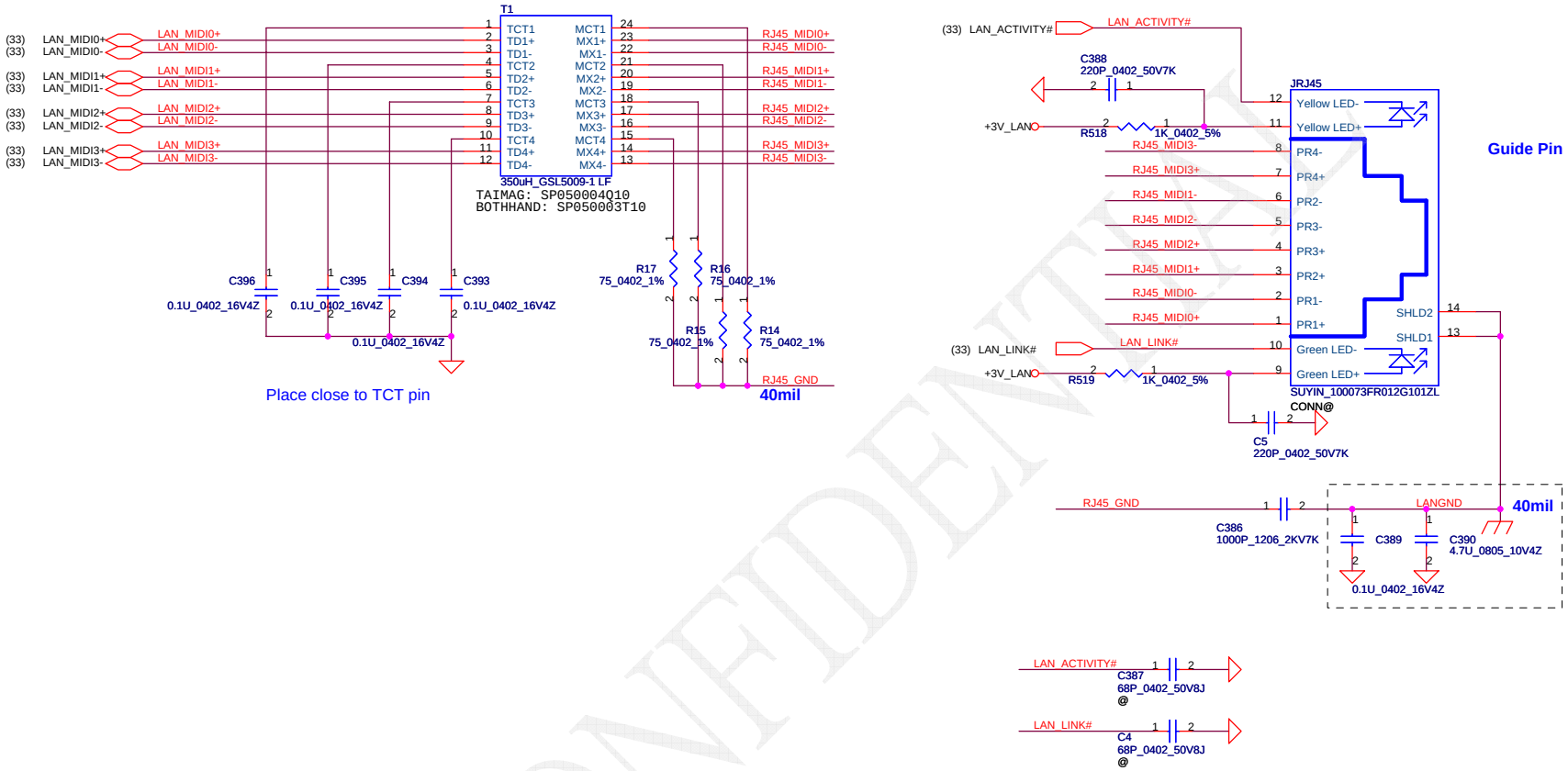

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

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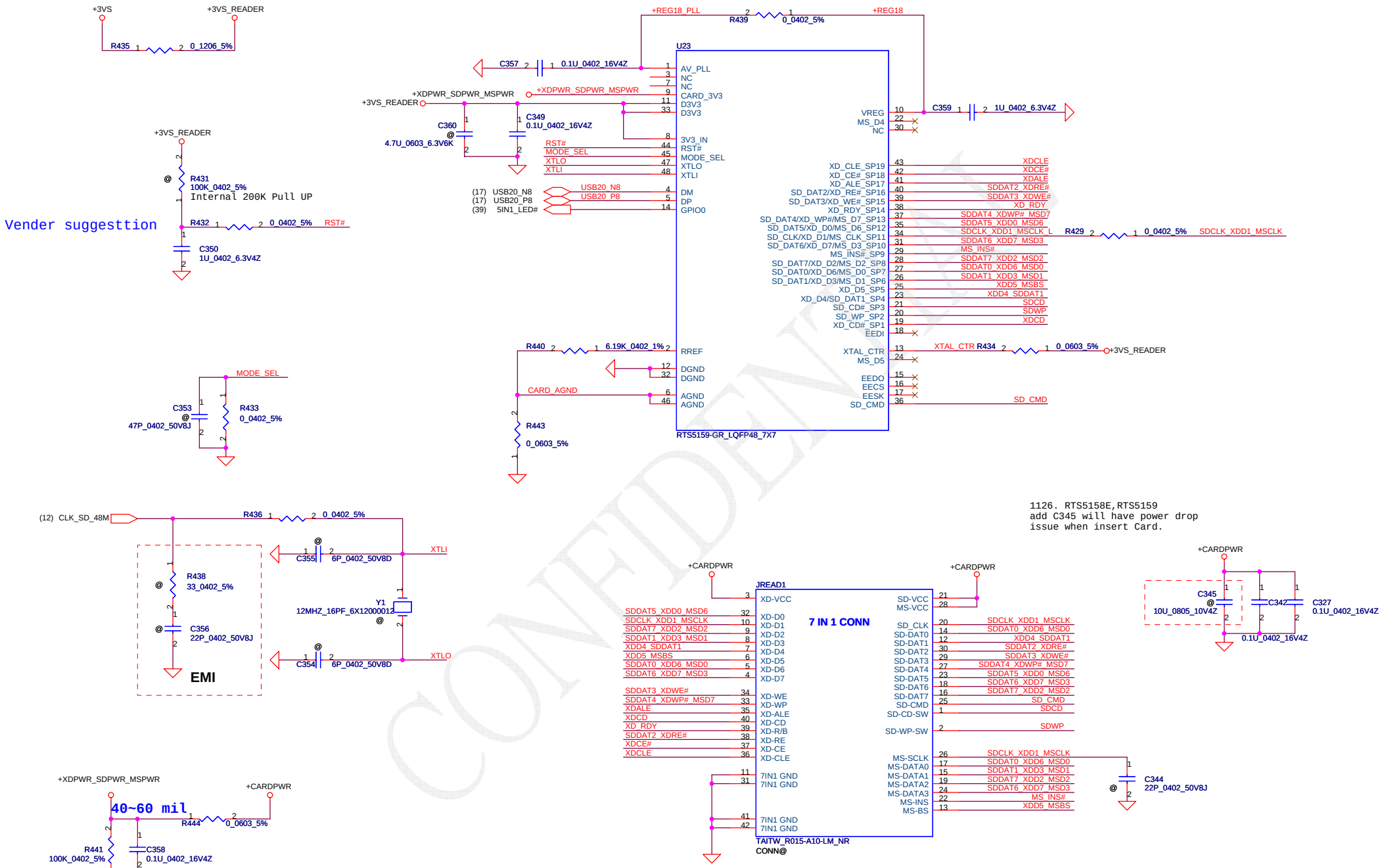

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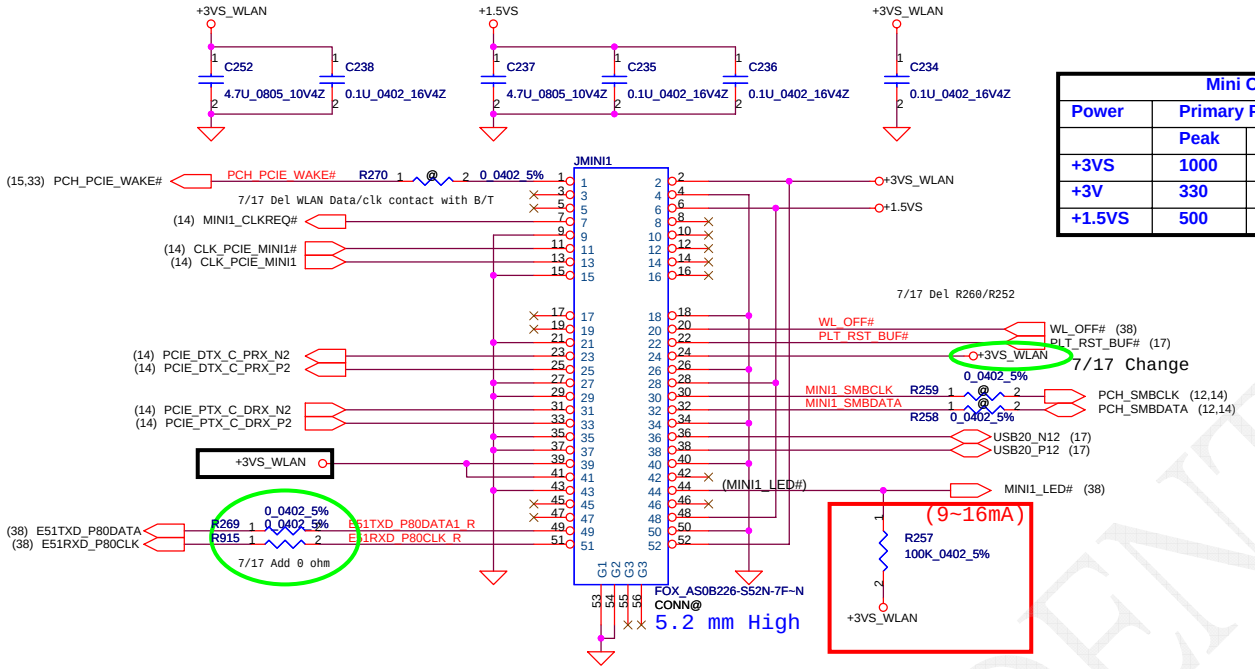
+3VS_WLAN R273 1 2 0_1206_5% +3VS

For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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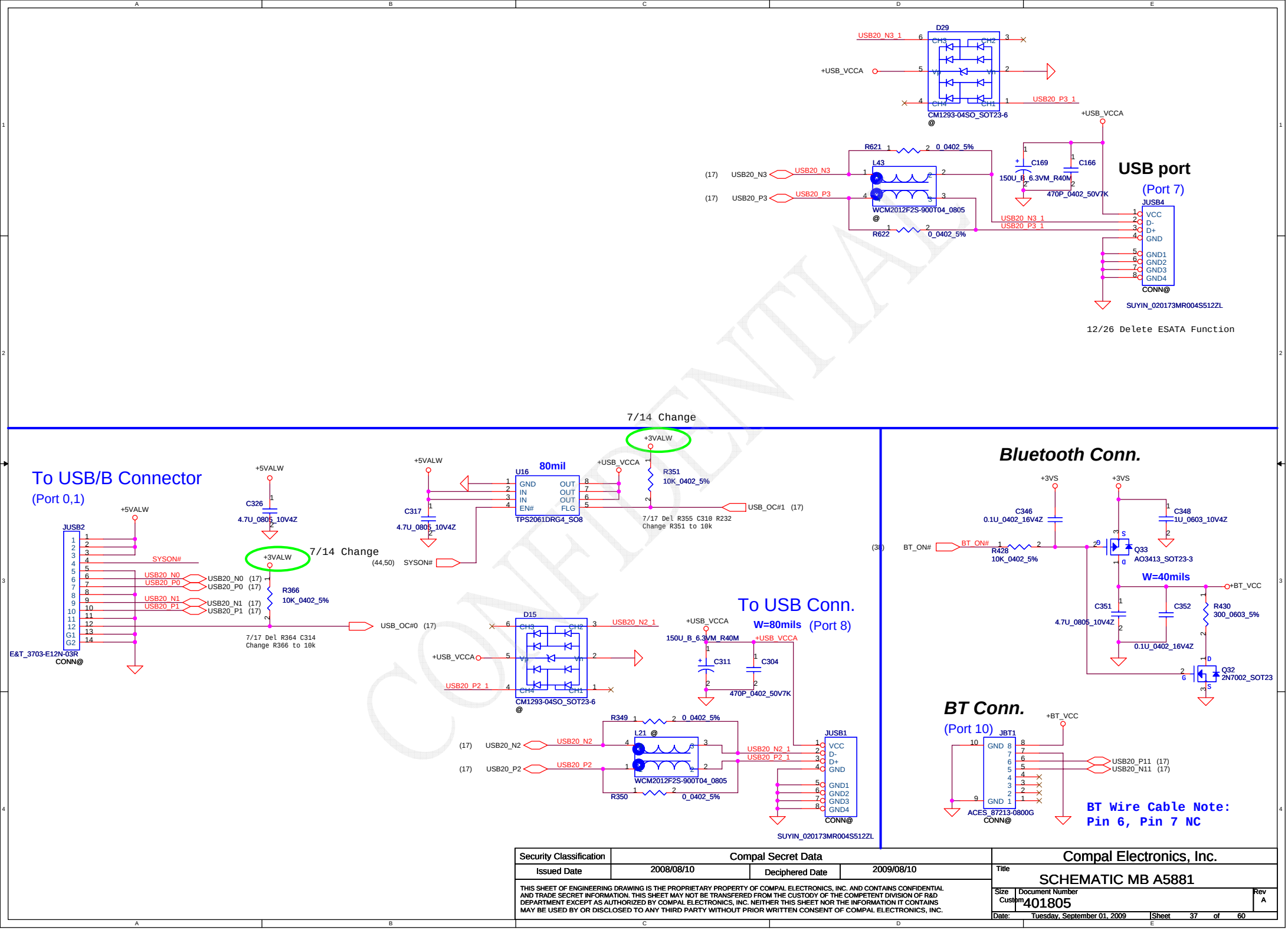

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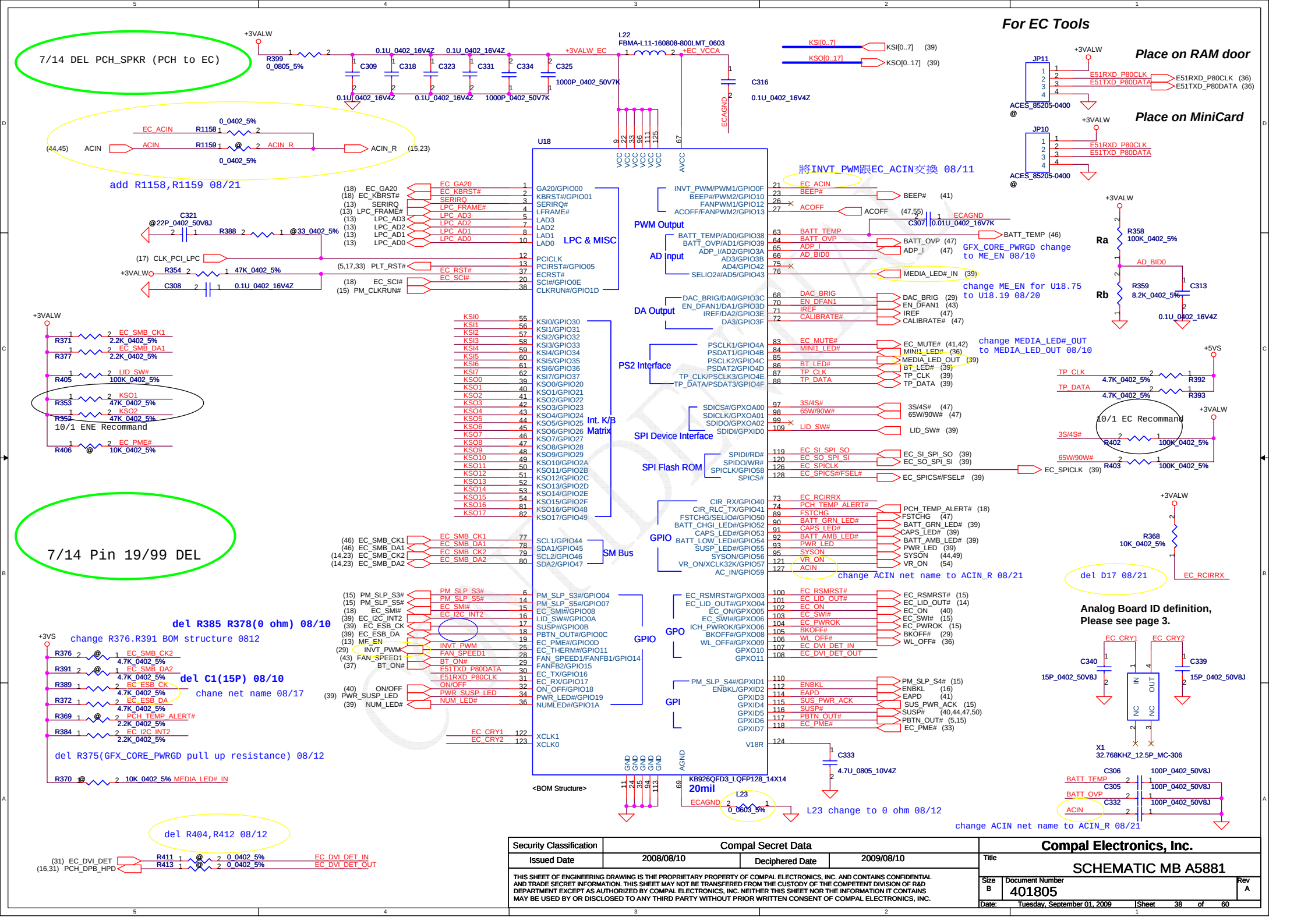

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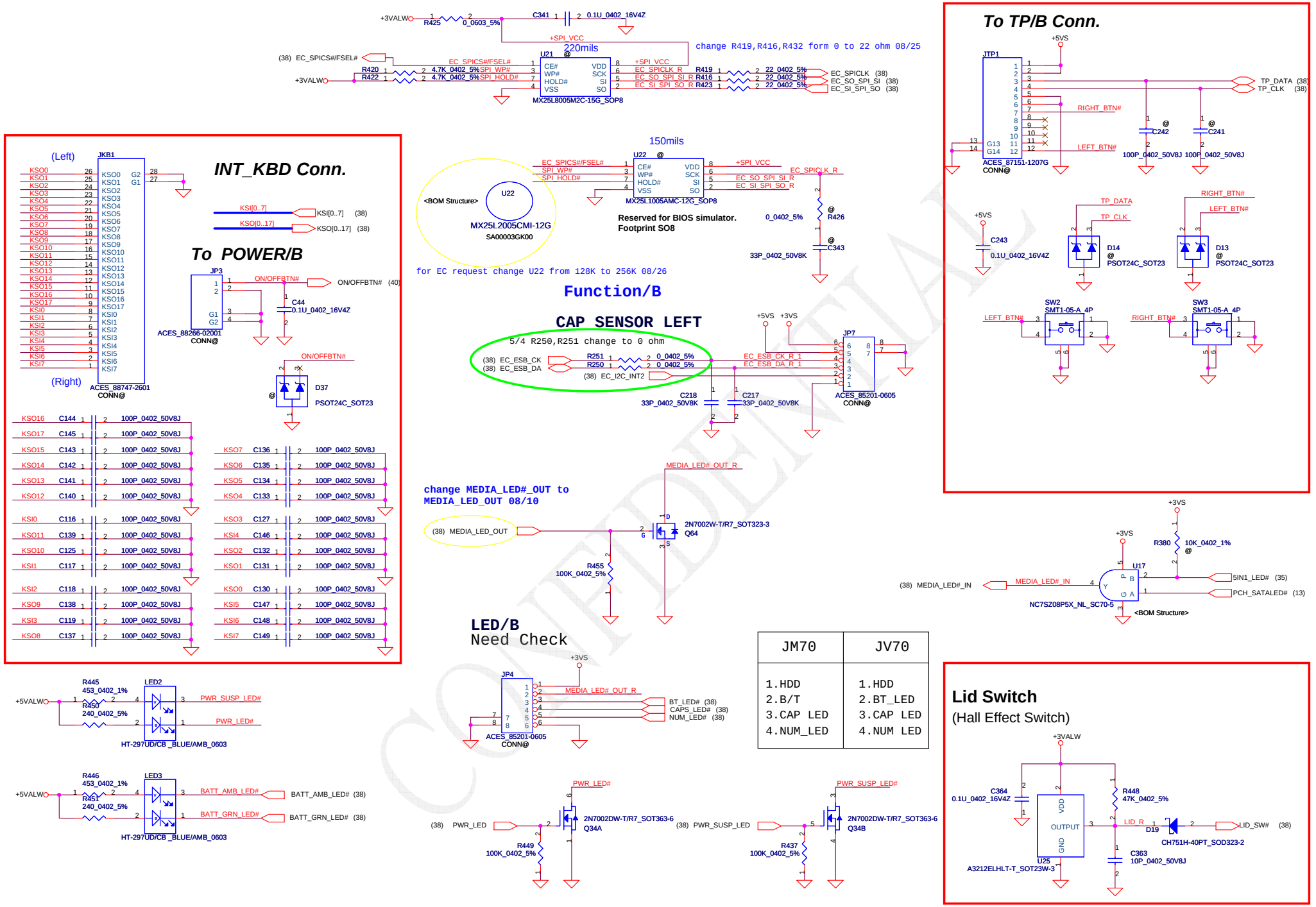

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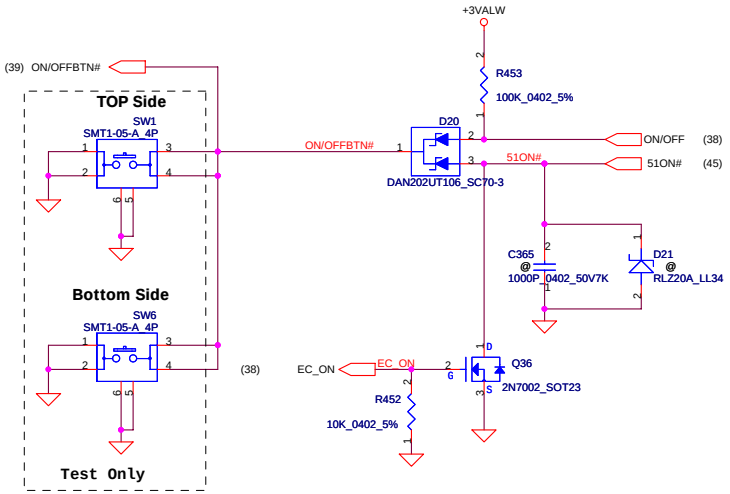
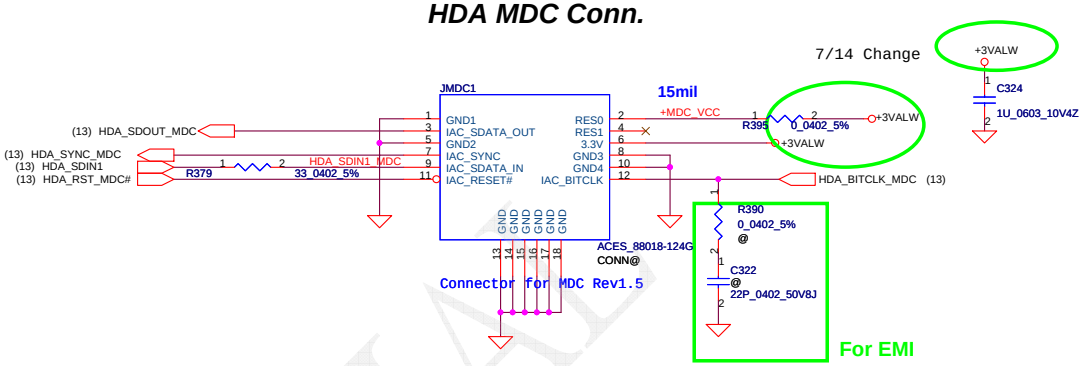
Power Button

ON/OFF switch



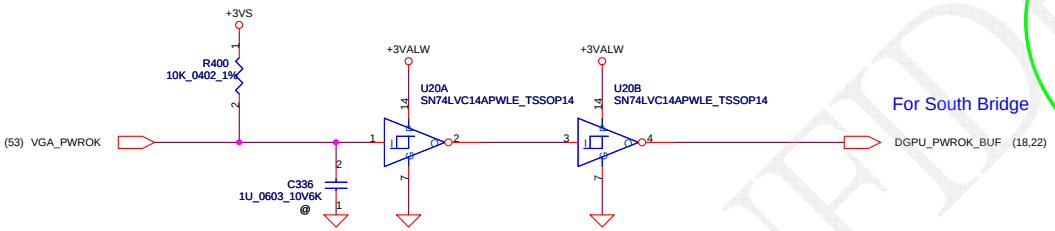
HDA MDC Conn.

7/14 Change

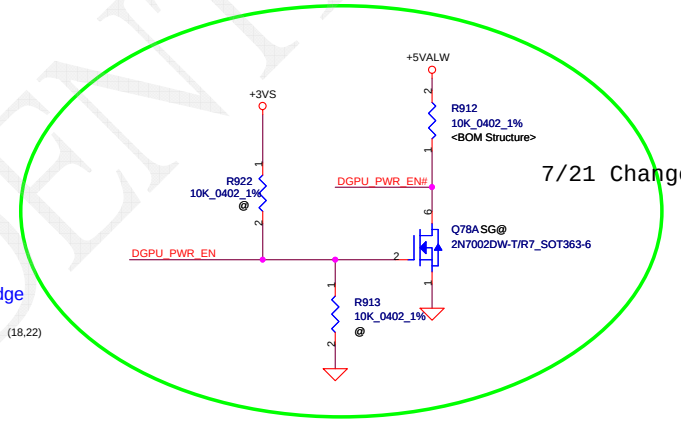


change R390,C322 BOM structure POP→@ 08/25

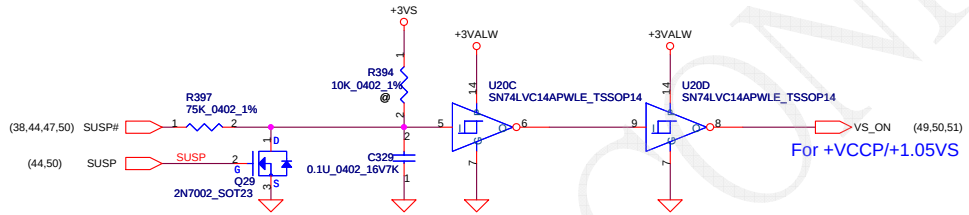
Power ON Circuit



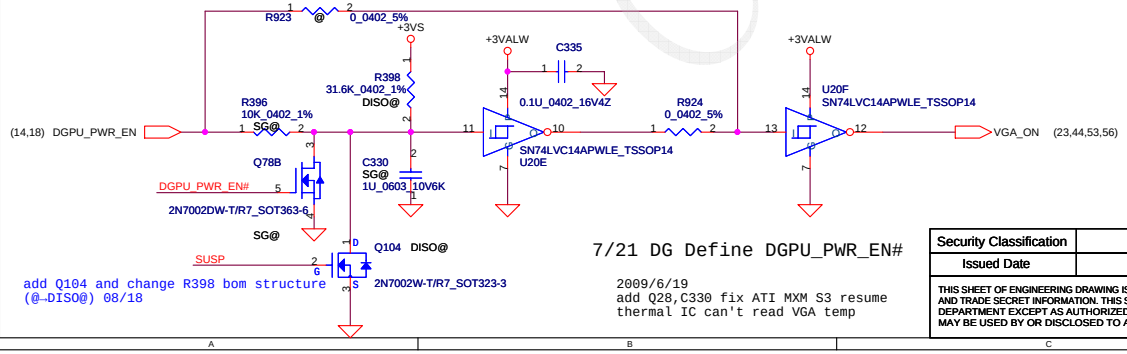
For South Bridge



7/21 Change



For +VCCP/+1.05VS

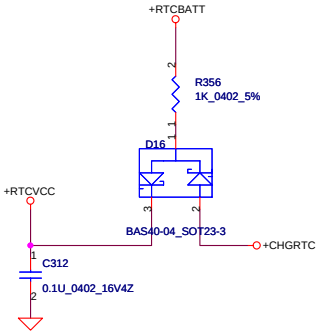


add Q104 and change R398 bom structure (@→DISO@) 08/18

7/21 DG Define DGPU_PWR_EN#

2009/6/19
add Q28,C330 fix ATI MXM S3 resume thermal IC can't read VGA temp

del R442,C362,C361,IR1(CIR) 08/21



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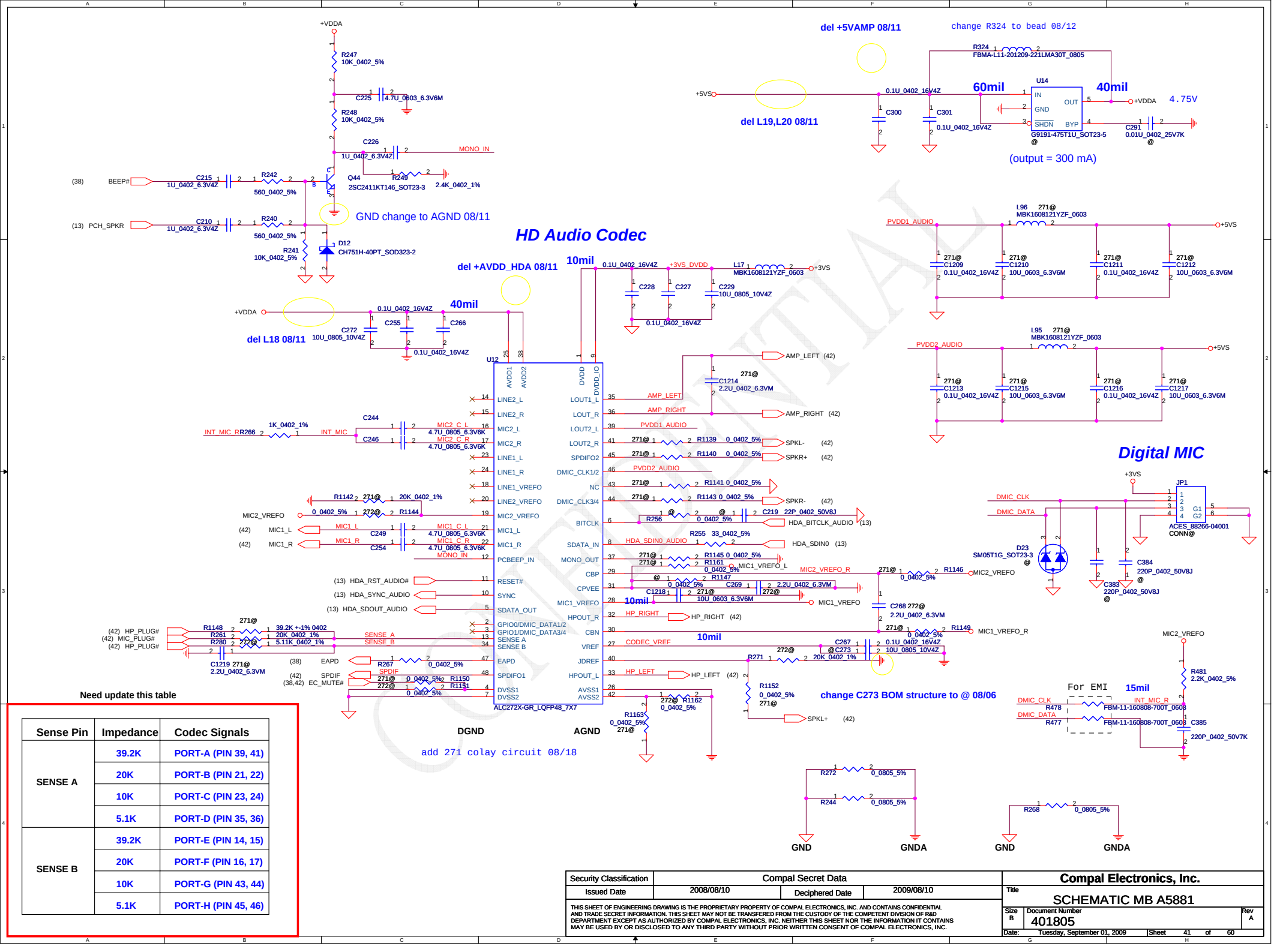

Need update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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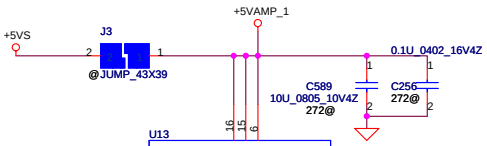
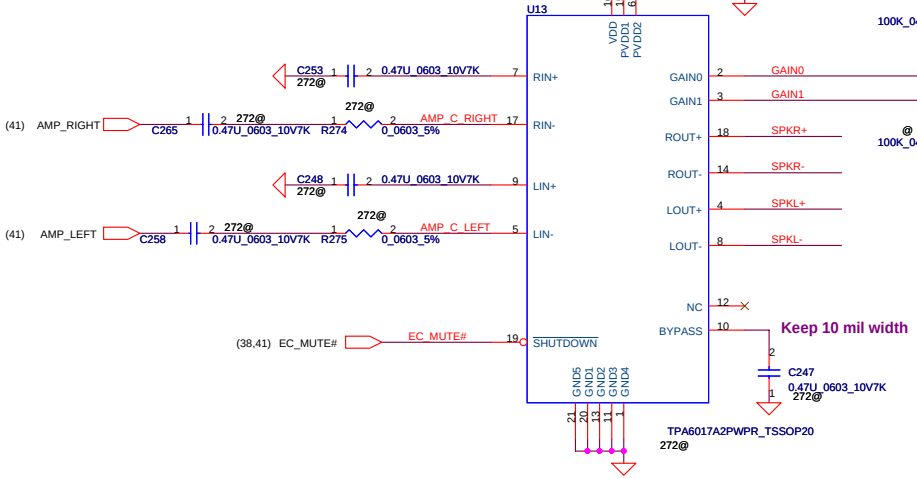
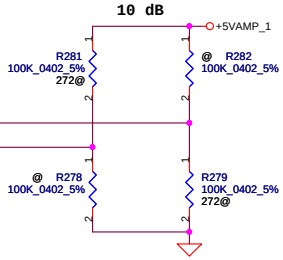
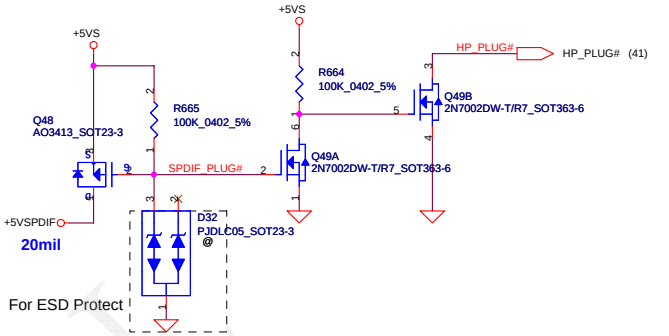
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

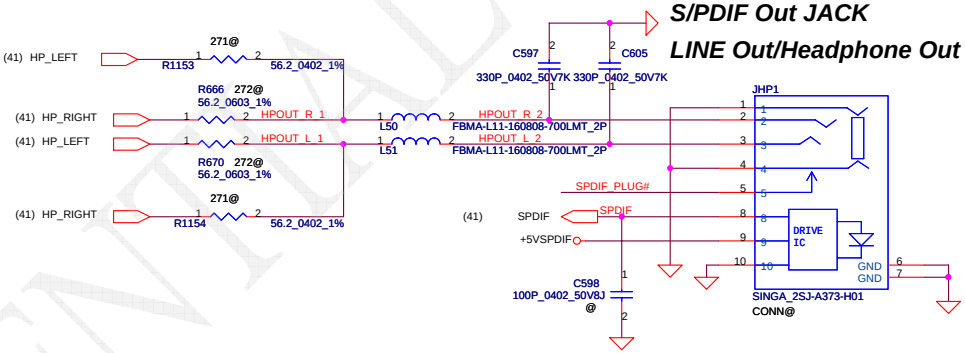






Keep 10 mil width

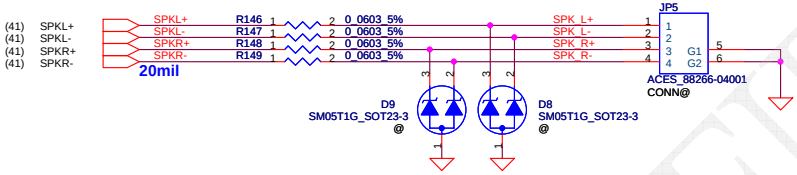


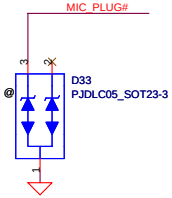


S/PDIF Out JACK

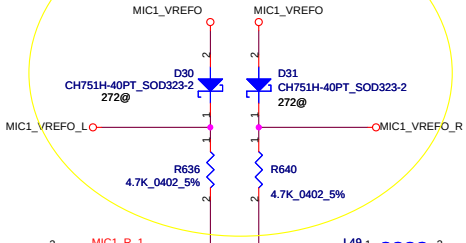
LINE Out/Headphone Out

Int. Speaker Conn.





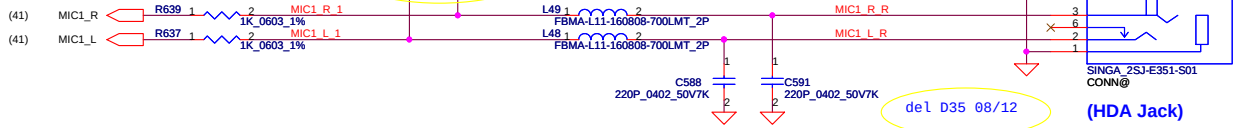
搬到bead前面 08/11



(Use KAKC0 PCB Footprint)

(Use KAKC0 PCB Footprint)

MIC JACK



del D35 08/12

(HDA Jack)

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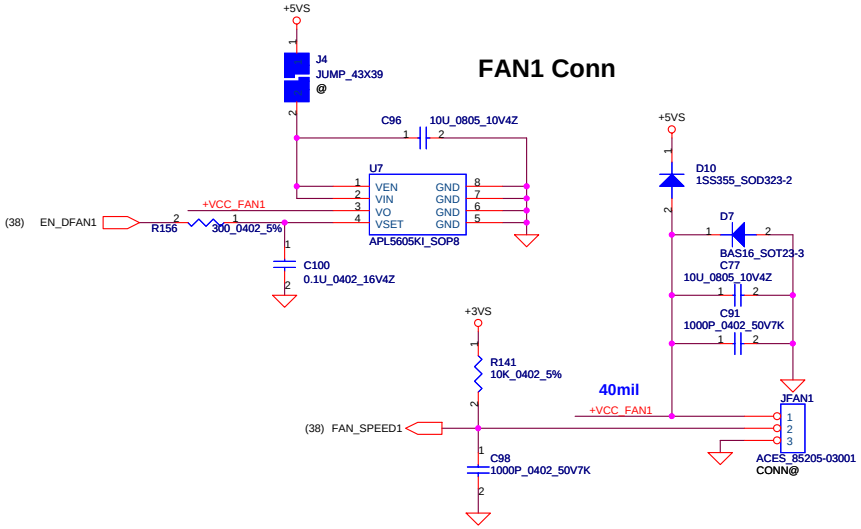
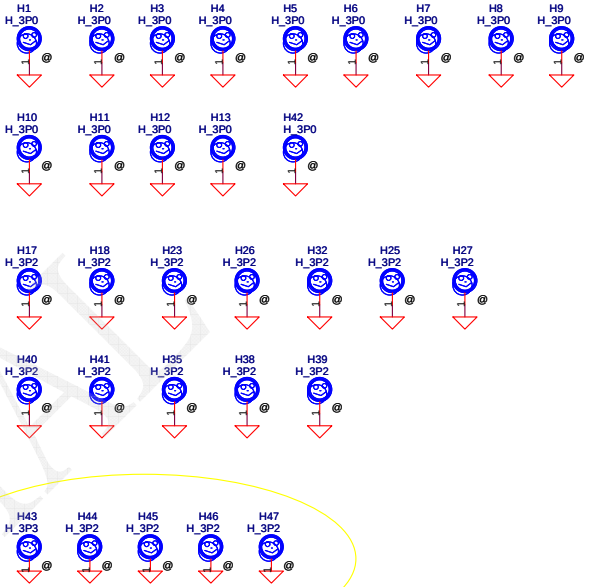
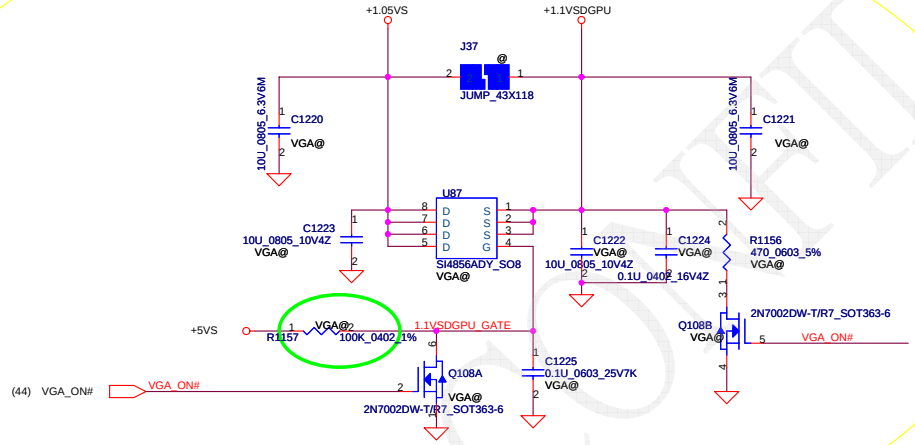


7/20 Del

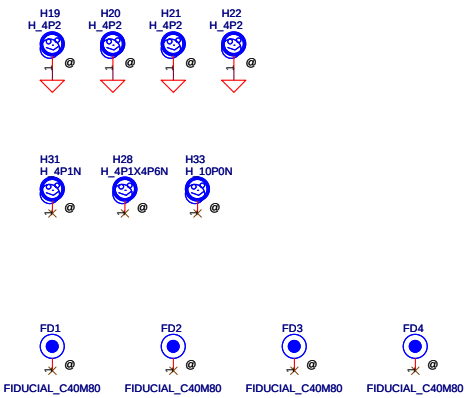


add screw 08/19

+1.05VS to +1.1VSDGPU Transfer



add +1.05VS to +1.1VSDGPU Transfer 08/20



change BOM structure @→VGA@ 08/25

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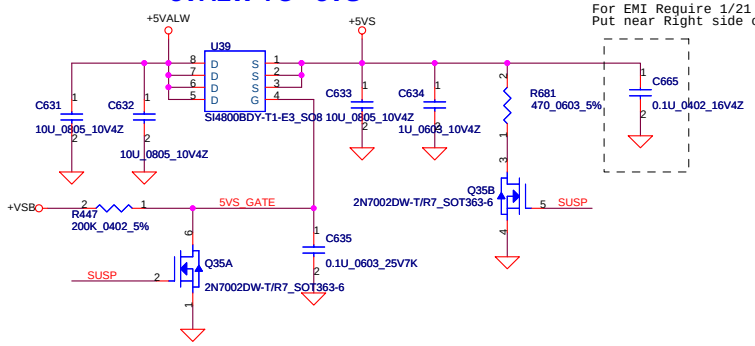
+5VALW TO +5VS

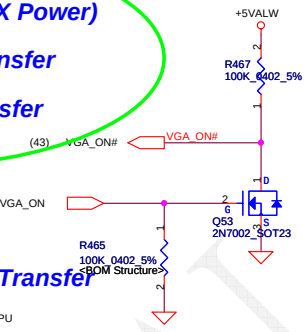


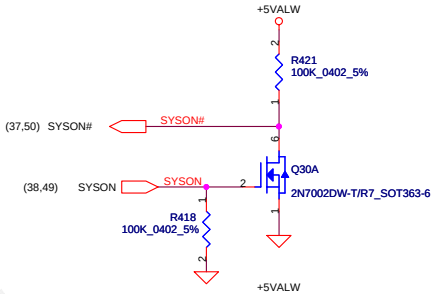
For EMI Require 1/21
Put near Right side of DIMM

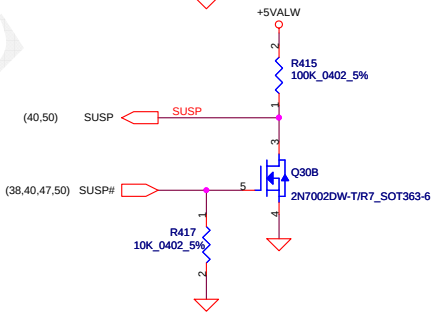
+3VALW TO +3VMXM Transfer

+5VALW to +5VMXM Transfer

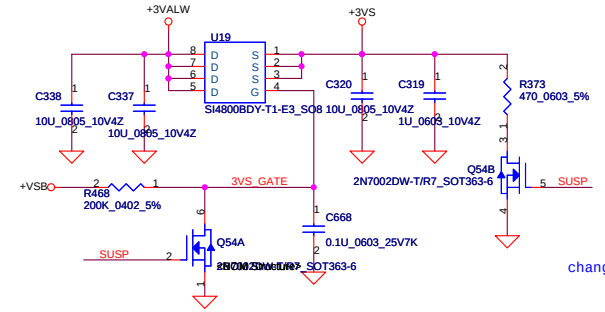
7/14 Change



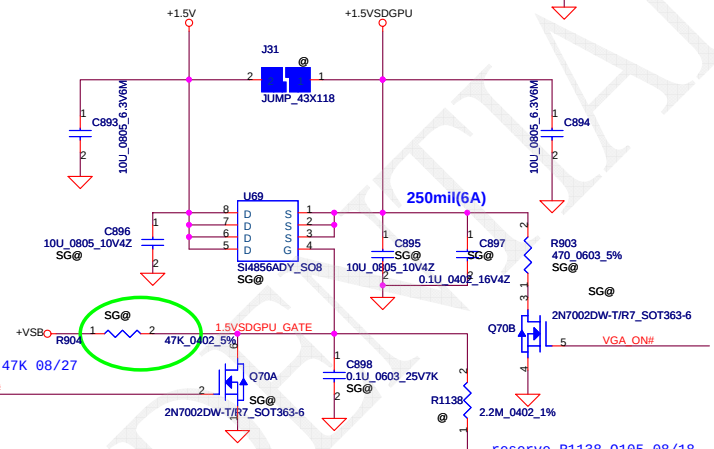




+3VALW TO +3VS

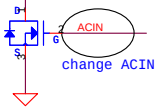


+1.5V to +1.5VSDGPU Transfer



change R904 from 100K to 47K 08/27

reserve R1138,Q105 08/18



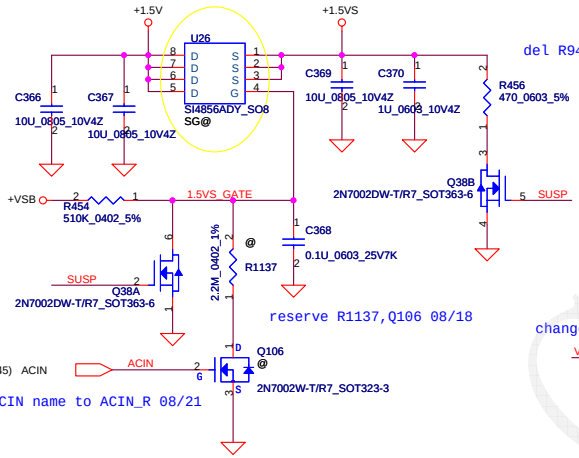
change ACIN name to ACIN_R 08/21

For Calpella CPU S3 DRAM Power

(1.5V_CPU VDDQ)

+1.5V to +1.5VS

U26 change to SI4856(Vgs=20) 08/18

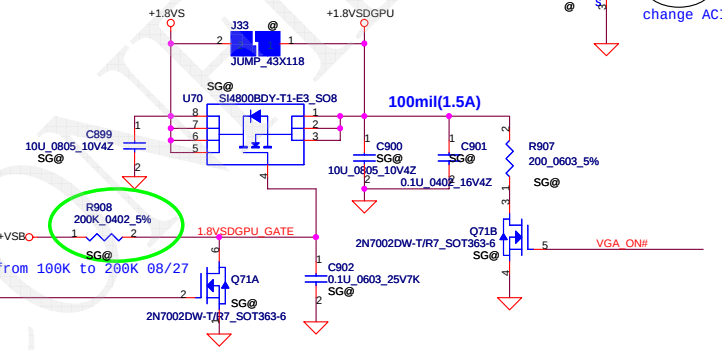


del R947 08/18

reserve R1137,Q106 08/18

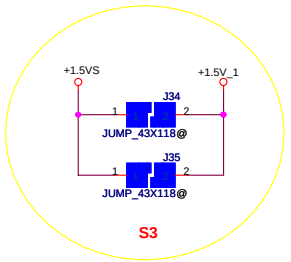
change ACIN name to ACIN_R 08/21

+1.8VS to +1.8VSDGPU Transfer

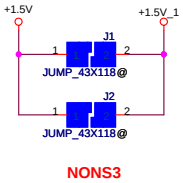


change R904 from 100K to 200K 08/27

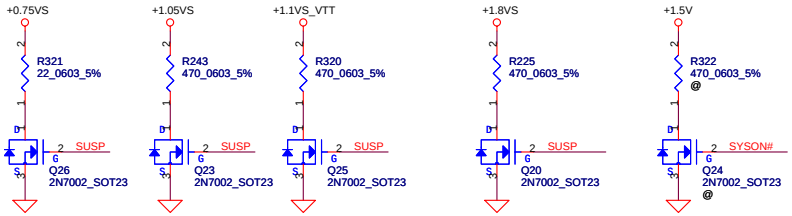
add J34,J35 08/17

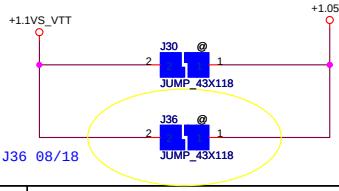


S3



NONS3





add J36 08/18

del U74 C929,C930,R948,R949,Q90,Q91
(+1.5V to +1.5V_1 circuit) 08/17

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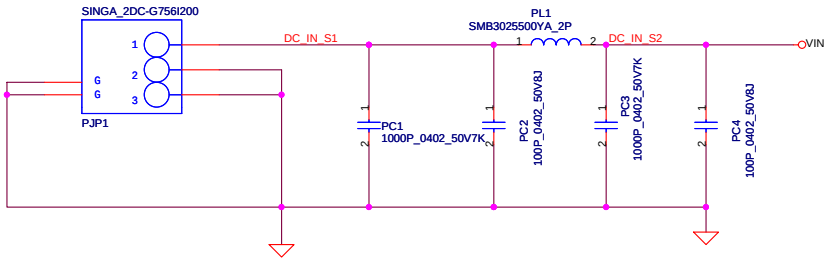
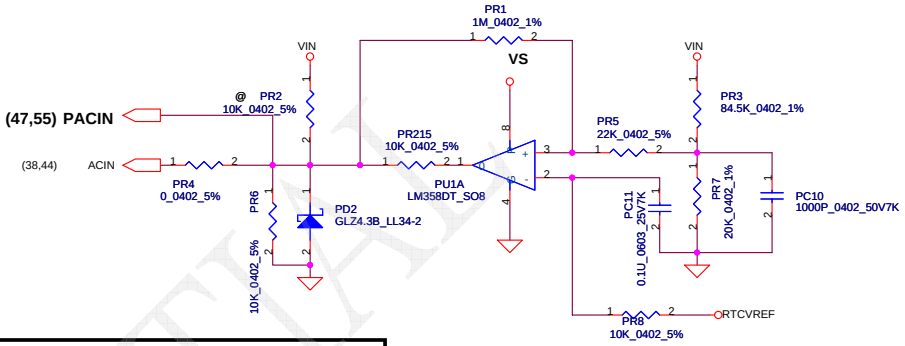
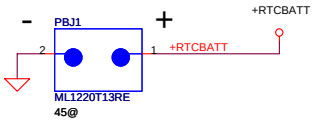
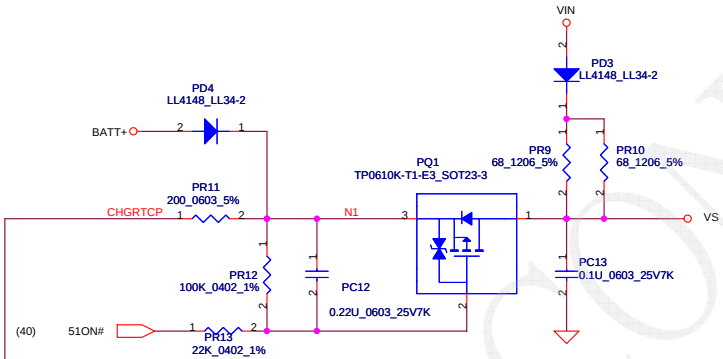
DC231000500

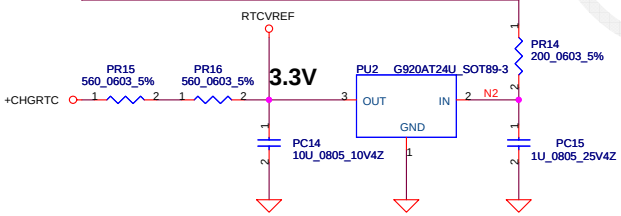


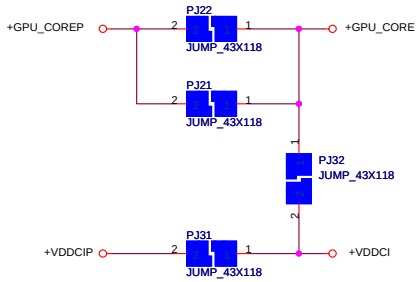


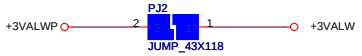
Vin Detector			
	Min.	Typ	Max.
H-->L	17.208V	17.212V	17.217V
L-->H	17.879V	17.894V	17.909V

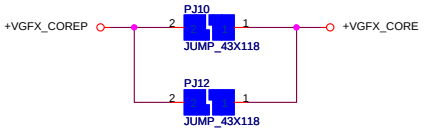


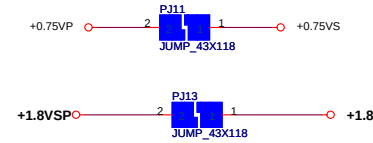












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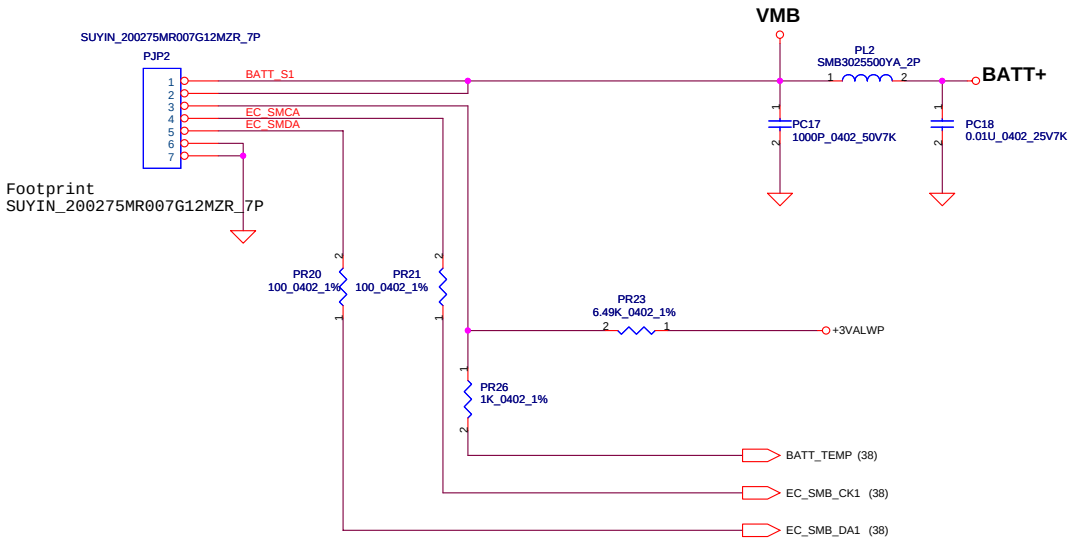
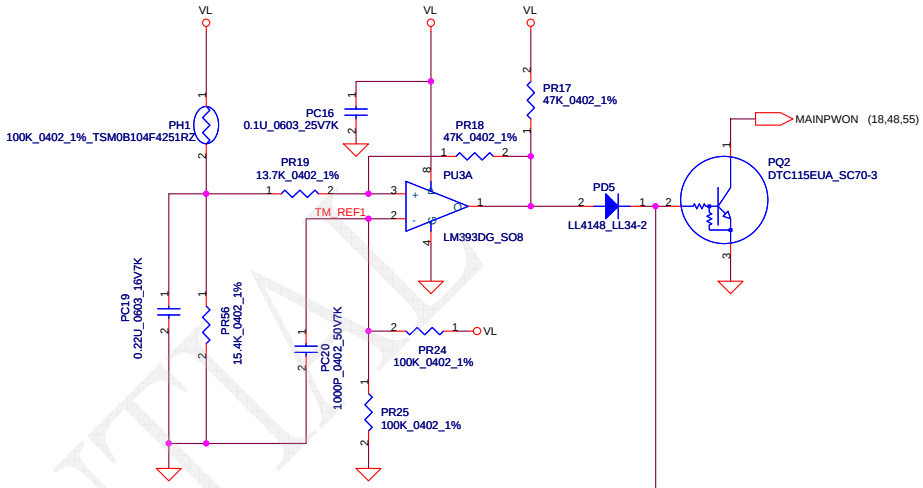
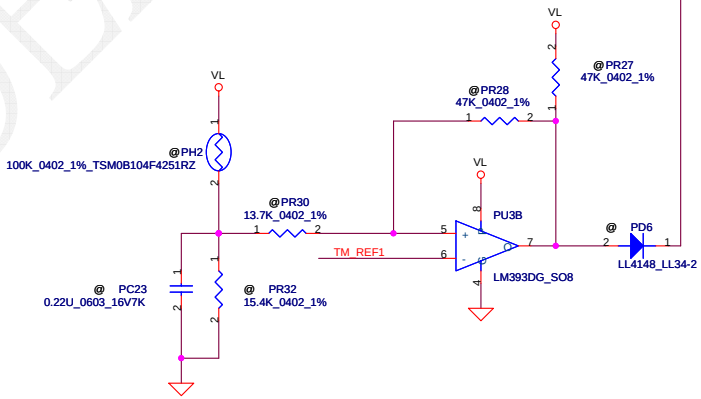
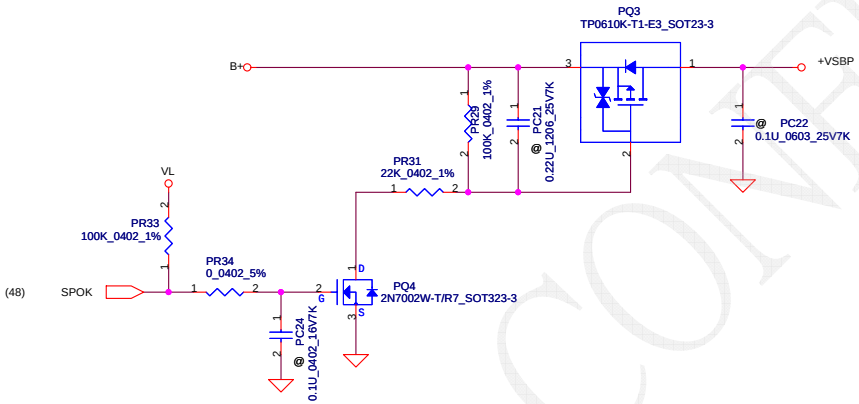
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C





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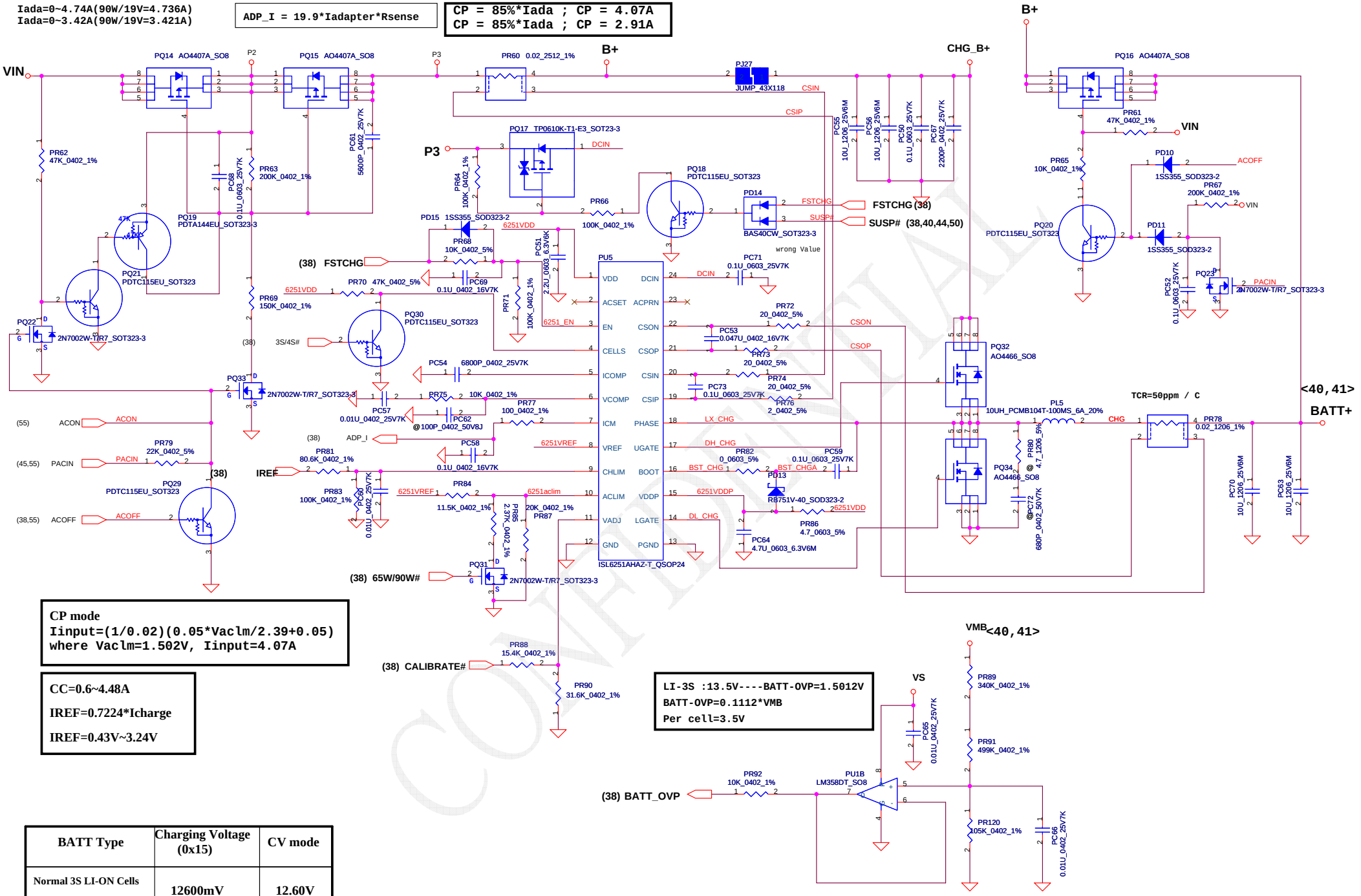
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

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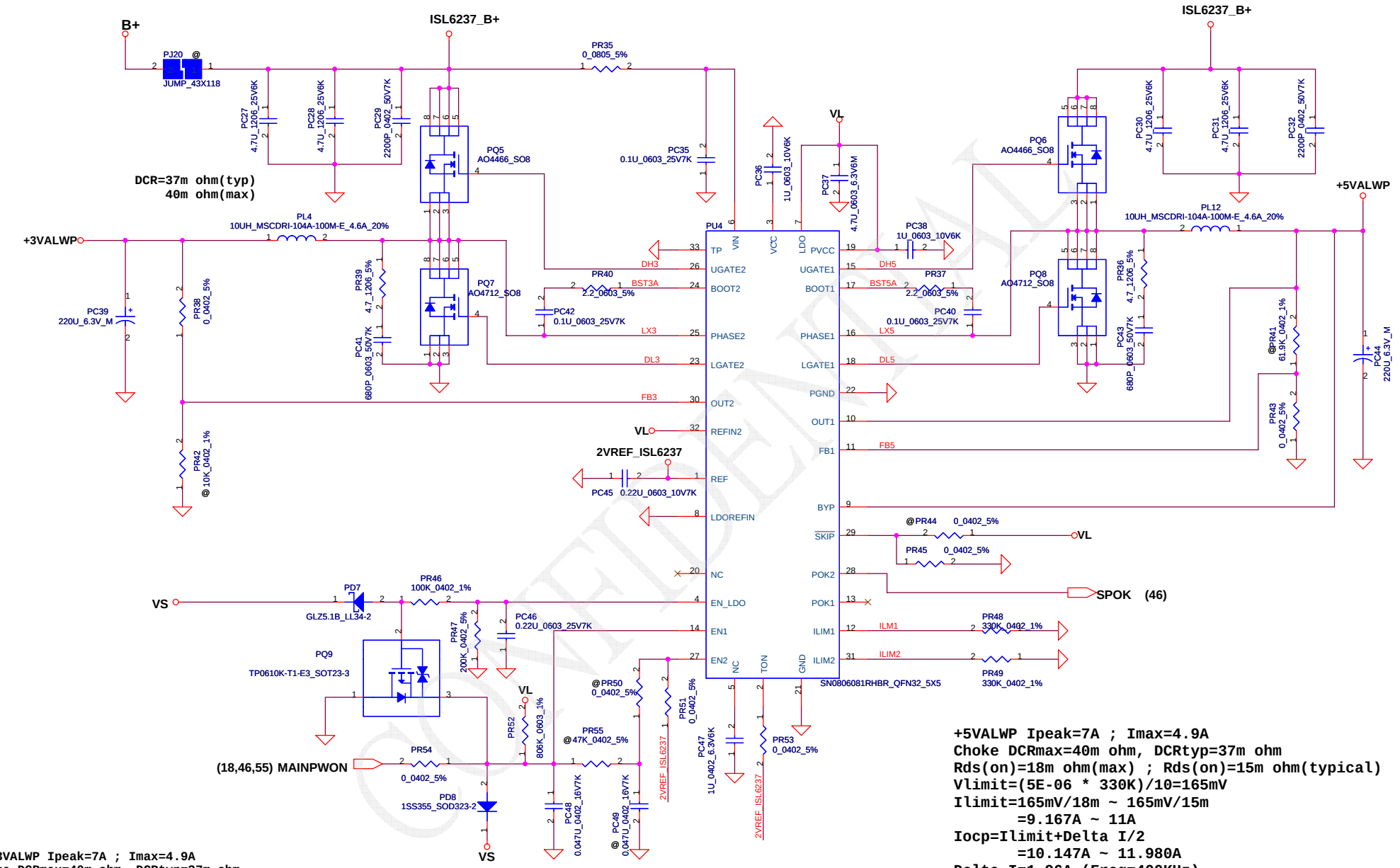

+3.3VALWP Ipeak=7A ; Imax=4.9A
Choke DCRmax=40m ohm, DCRtyp=37m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=7A ; Imax=4.9A
Choke DCRmax=40m ohm, DCRtyp=37m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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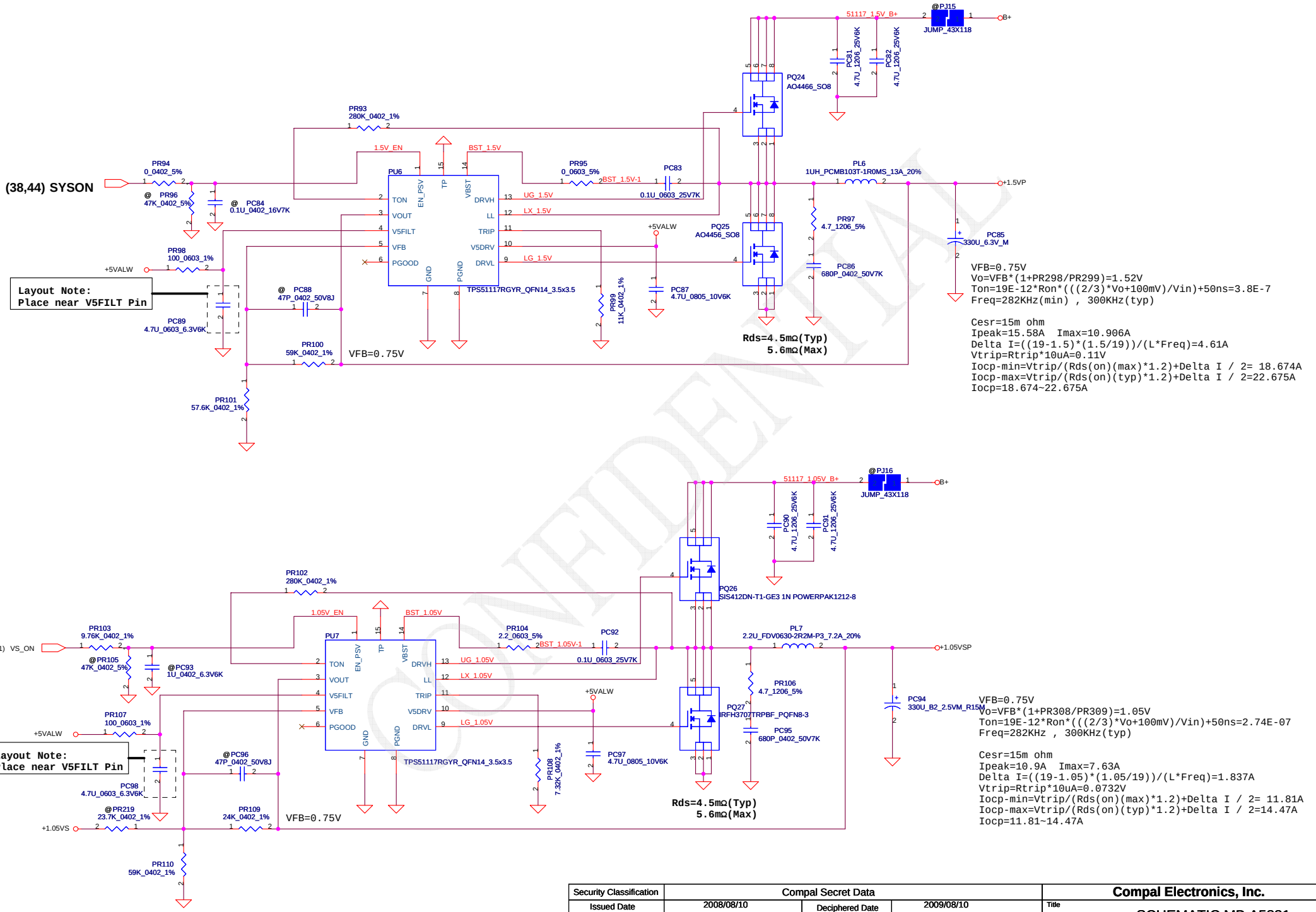

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.			
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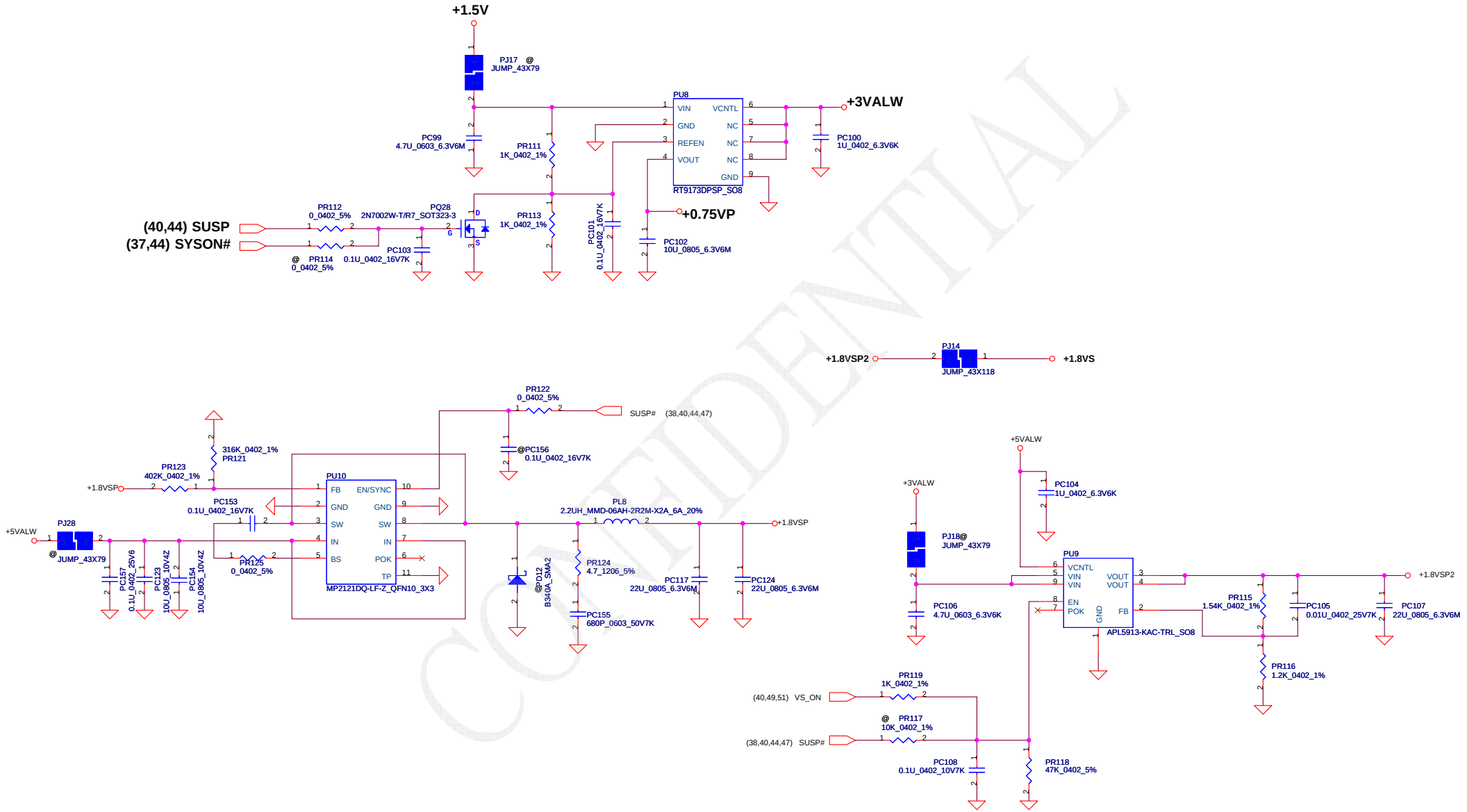

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

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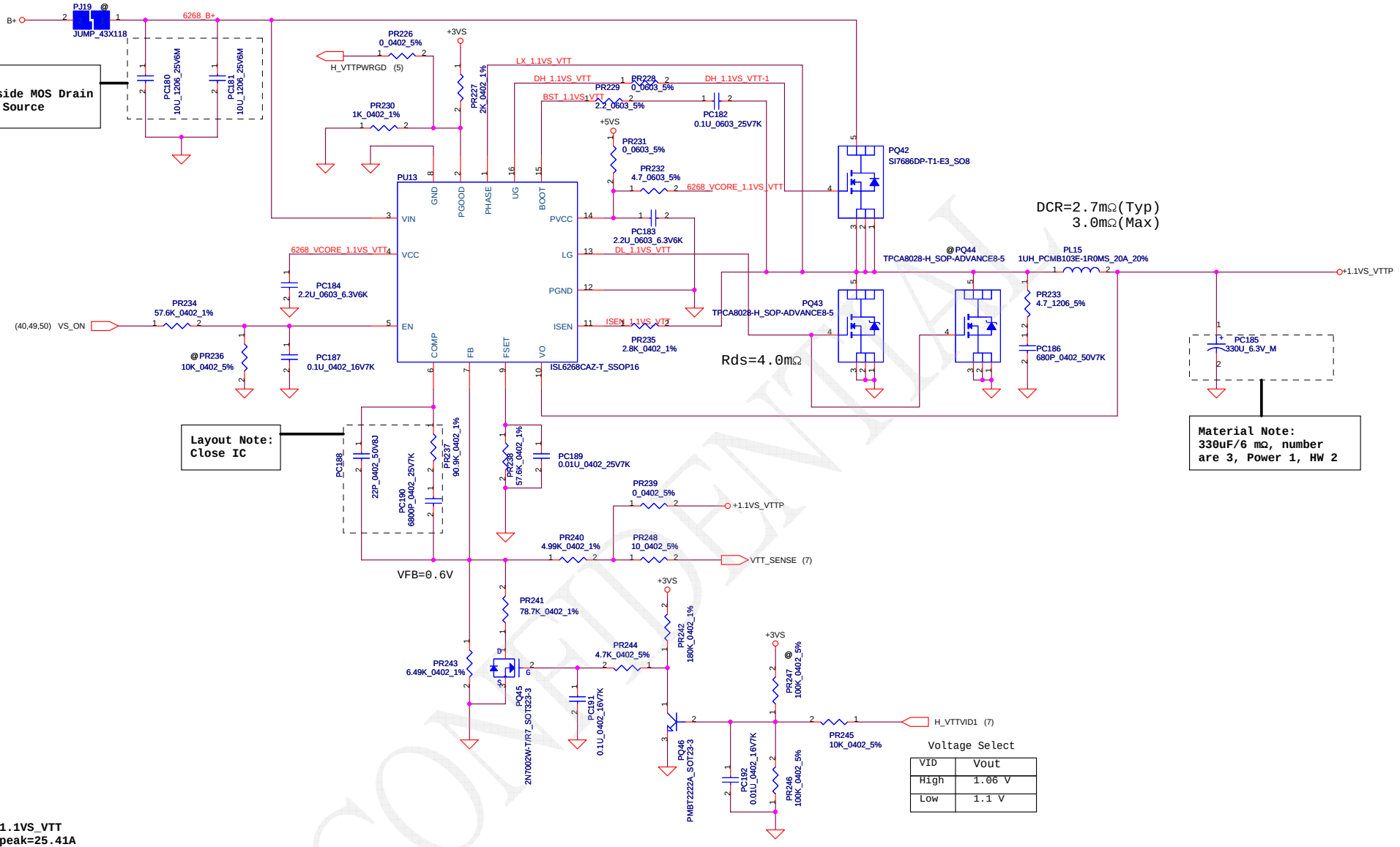

Security Classification	Compal Secret Data		
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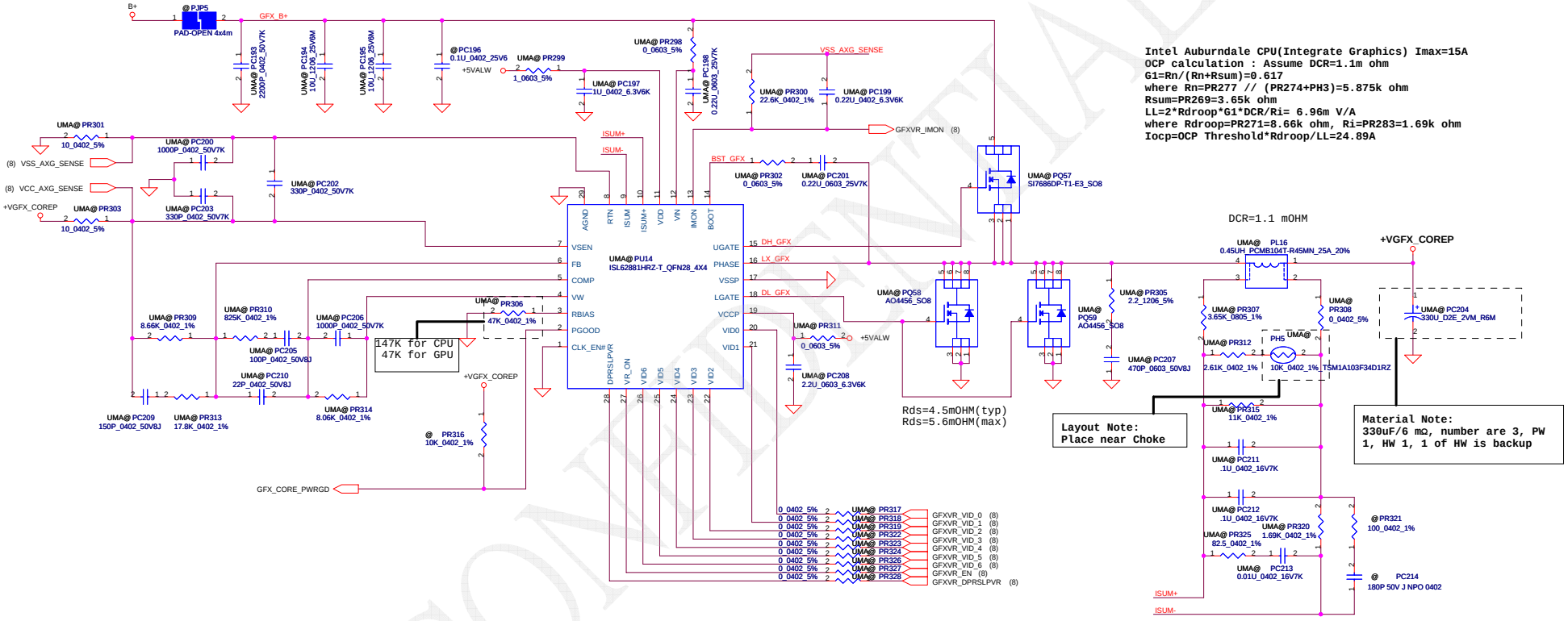

Security Classification	Compal Secret Data		
Issued Date	2009/5/14	Deciphered Date	2010/05/14

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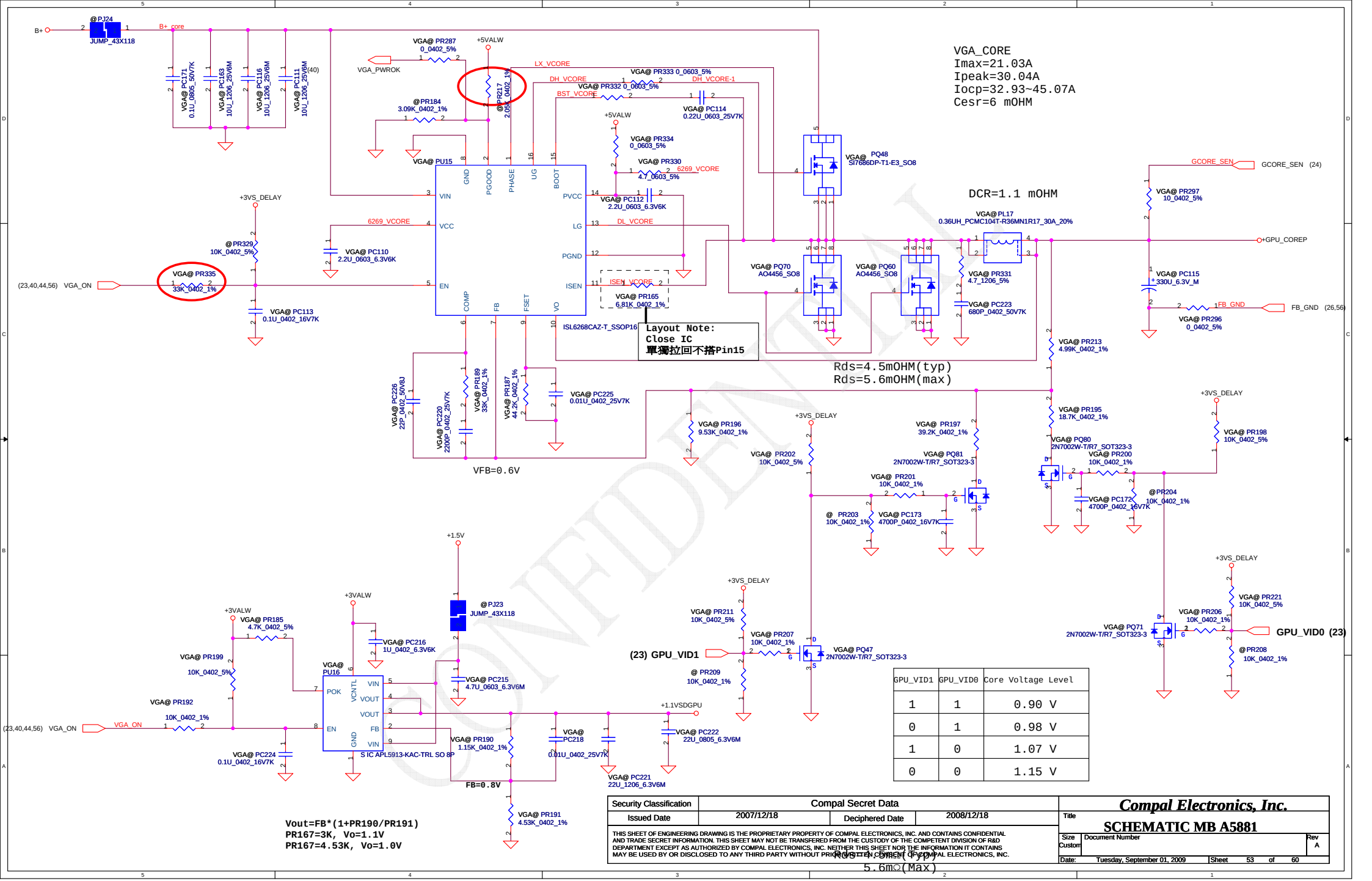

GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.90 V
0	1	0.98 V
1	0	1.07 V
0	0	1.15 V

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Issued Date	2007/12/18	Deciphered Date	2008/12/18

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Intel Auburndale CPU(Integrate Graphics) , Ipeak = 48A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum/2)=0.763
where Rn=PR258 // (PR251+PH6)=5.875k ohm
Rsum=PR221, PR253 =3.65k ohm
LL = 2*Rdroop*G1*(DCR/2)/Ri = 1.81mV/A
where Rdroop=PR239=2.61k ohm , Ri=PR256=1.21k ohm
Iocp= OCP Threshold*Rdroop/LL=40E-06*2.61E03/1.81E-03=57.68A

Layout Note:
PH3 place near Phase1 L-MOS

Layout Note:
Place near Phase1 Choke

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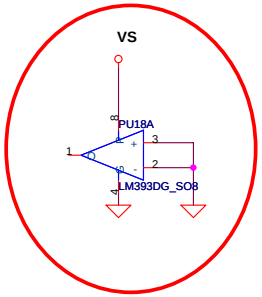

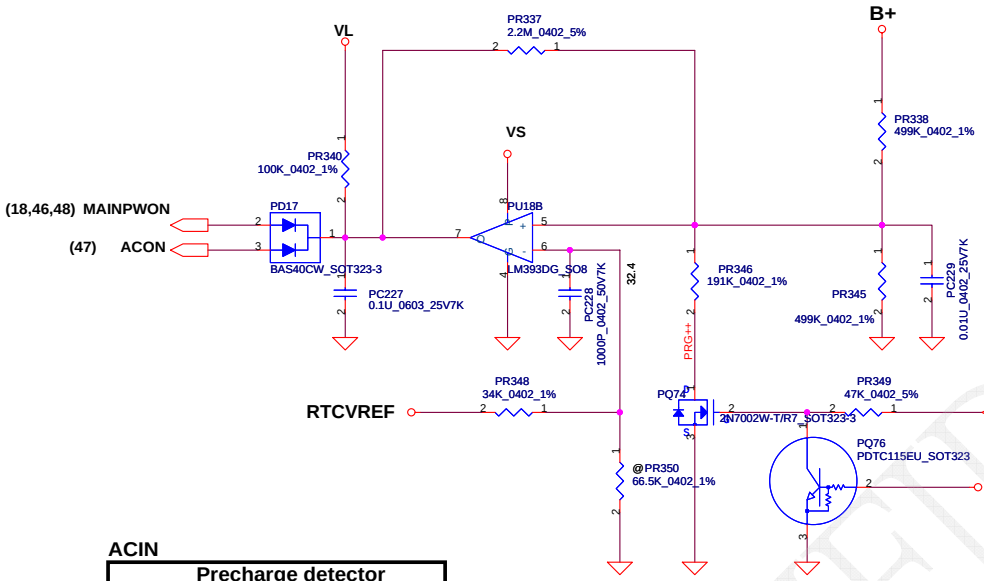

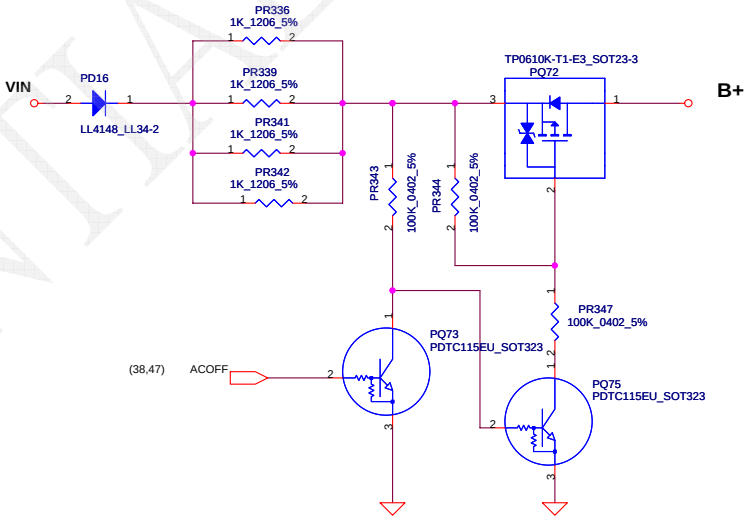

ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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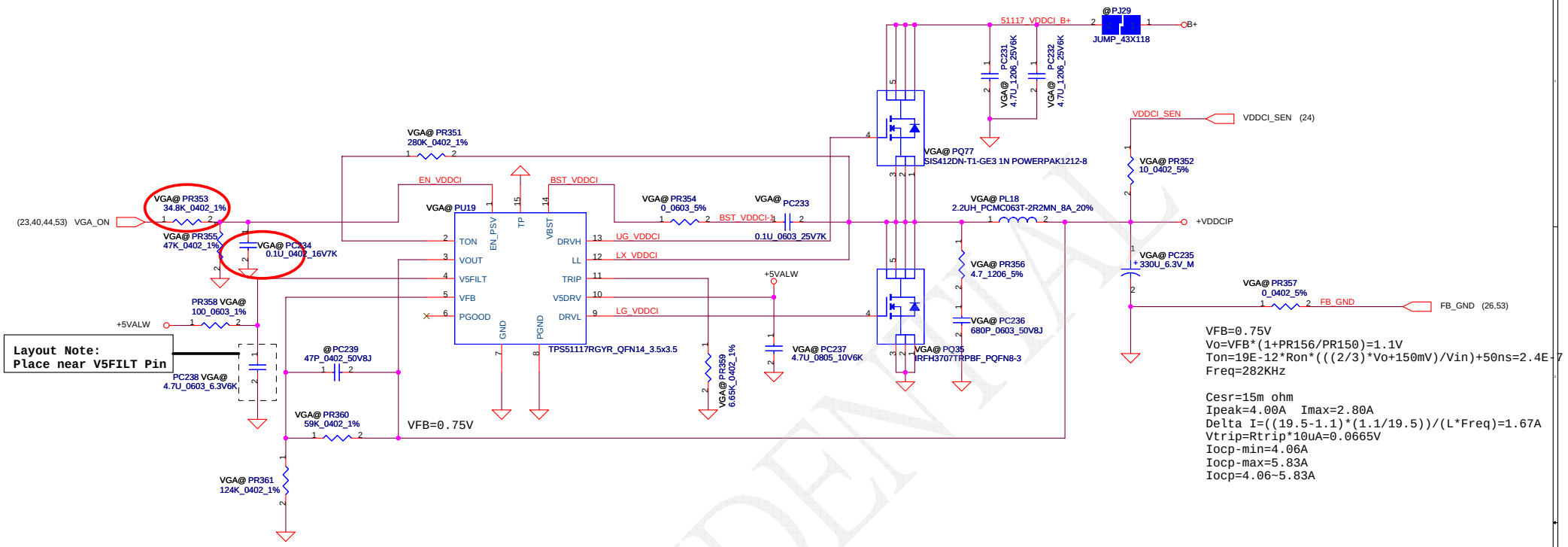

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A --> B Change List

Reference to KBLA0 LA4811 Change List Excel File

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add all sunbber R	EMI solution	0.1	52		09/08/27	DVT
2	add all sunbber C	EMI solution	0.1	52		09/08/27	DVT
3	remove VGA enable R	HW request	0.1	53	delete PR217 2.05K_0402_1%	09/08/27	DVT
4	VDDCI EN sequency regulate	HW request	0.1	53	PR335:32k P/N:SD034330280	09/08/27	DVT
5	VGA EN sequency regulate	HW request	0.1	53	PR353 : 35k P/N:SD00000UD80 PC234 :@==> add	09/08/27	DVT
6							
7							
8							
9							
10							
11							
12							
13							
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16							
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21							
22							
23							

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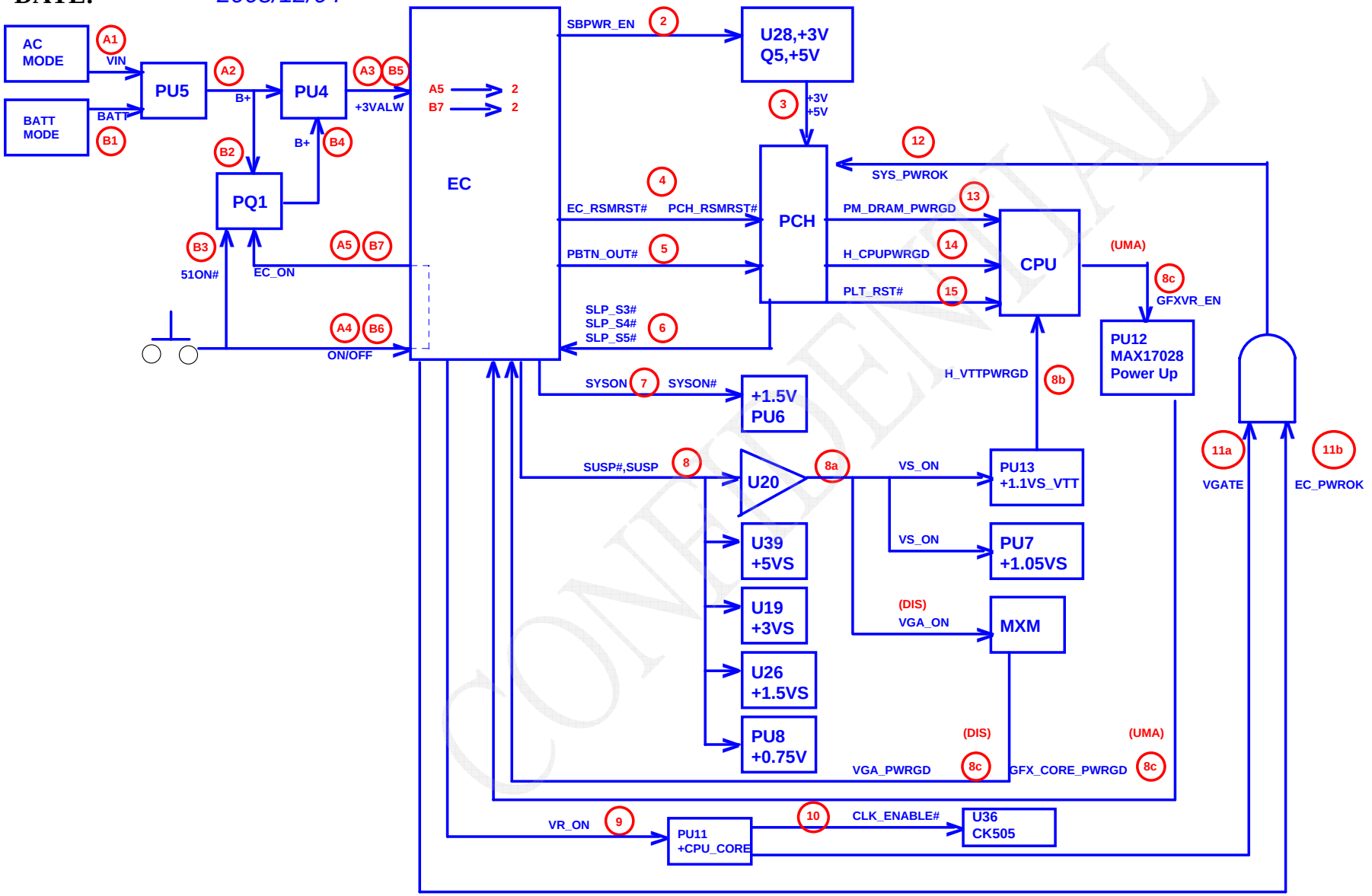
COMPAL CONFIDENTIAL

MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



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