

# Compal Confidential

Model Name : P7YE0/P7YH0/P7YS0

File Name : LA-6911P

BOM P/N:43

# Compal Confidential

## P7YE0/P7YH0/P7YS0 M/B Schematics Document

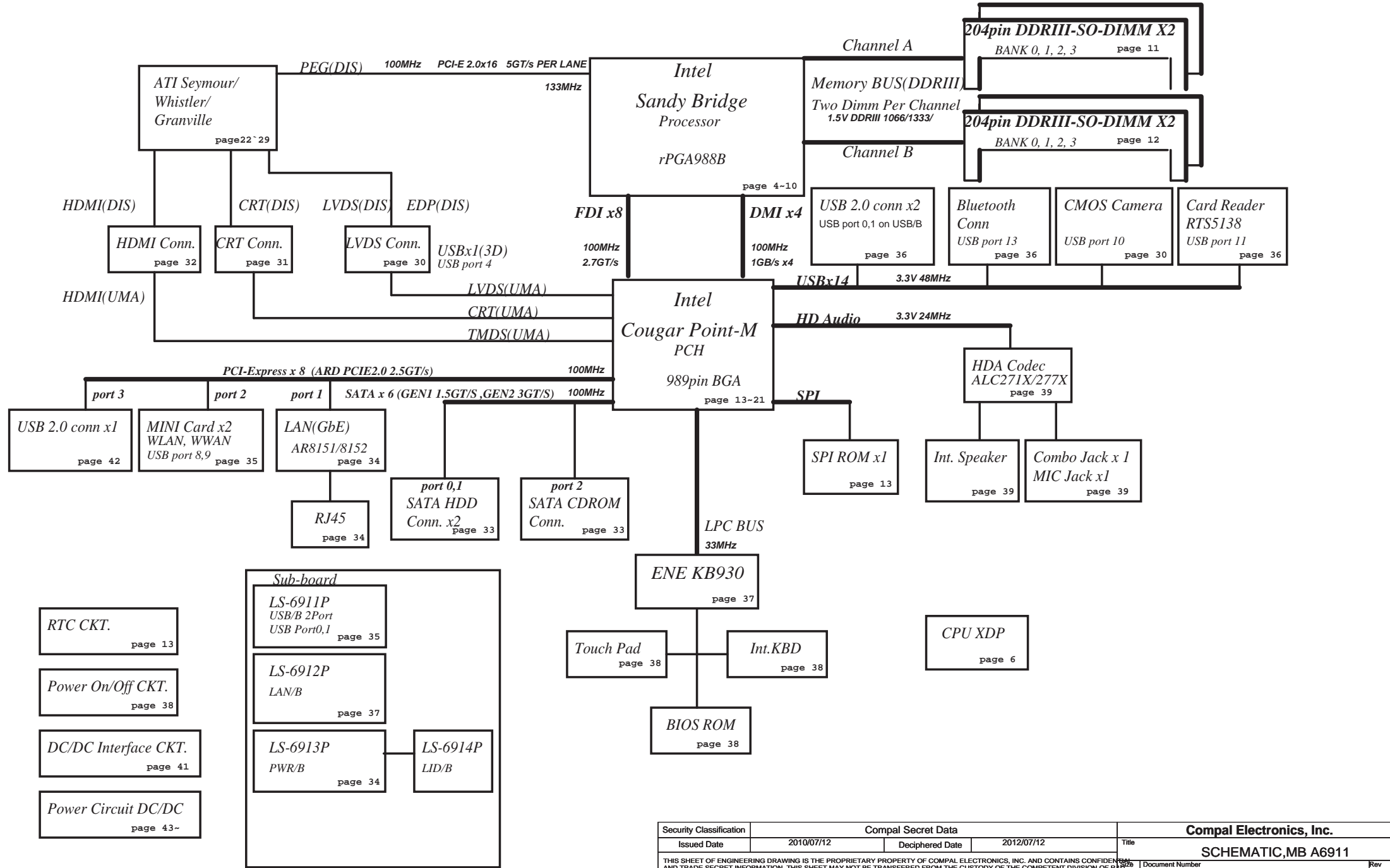
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH  
ATI Seymour/Whistler/Granville

2010-11-01

REV:0.3

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Fan Control  
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# Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

## EC SM Bus2 address

Device	Address
--------	---------

## PCH SM Bus address

Device	Address	VRAM P/N
ChannelA DIMM0 A0	1010 000X	JDIMM1
DIMM1 A2	1010 001X	JDIMM3
ChannelB DIMM0 A4	1010 010X	JDIMM2
DIMM1 A6	1010 011X	JDIMM4

**SAM** 64\*16 900M SA00004GS10(S IC D3 64M16 K4W1G1646G-BC11 FBGA ABOI)  
**SAM** 64\*16 800M SA000035720(S IC D3 64M16 K4W1G1646G-HC12 FBGA ABOI)  
**SAM** 128\*16 800M SA00003MG60(S IC D3 128M16 K4W2G1646C-HC12 FBGA ABOI)  
**HYN** 64\*16 900M SA000041S40(S IC D3 64M16 H5TQ1G63DFR-11C FBGA ABOI)  
**HYN** 64\*16 800M SA000032420(S IC D3 64M16 H5TQ1G63BFR-12C FBGA ABOI)  
**HYN** 128\*16 800M SA00003VS10(S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABOI)  
**HYN** 64\*16 800M SA0000324G0(S IC D3 64M16 H5TQ1G63DFR-12C FBGA ABOI)

BT Config	GPU config	BACO config
BT SKU: BT@	Whistler: WHIS@	BACO: BACO@
4DIMM config	Seymour: SEYM@	nonBACO: NOBACO@
4 DIMM: 4DIMM@	Granville: GRAN@	Muxless config
LVDS/eDP config	Granville config	Muxless: MUXL@
UMA LVDS: ULVDS@	Granville: GRAN@ (VDDCI)	nonMuxless: NOMUXL@ (DISO,UMAO)
DIS LVDS: DLVDS@	nonGranville: NOGRAN@ (VGA_CORE)	
DIS eDP: DEDP@	GPU Frame config	
	128bit: 128@ (WHIS,GRAN)	
		<b>VRAM BOM Config</b>
		X76264BOL01: 64Mx16x4 Seymour 512M HYN NEW
		X76264BOL02: 64Mx16x4 Seymour 512M HYN OLD
		X76264BOL03: 64Mx16x8 Whistler/Granville 1G HYN NEW
		X76264BOL04: 64Mx16x8 Whistler/Granville 1G HYN OLD
		X76264BOL05: 128Mx16x8 Whistler/Granville 2G HYN
		X76264BOL06: 128Mx16x8 Whistler/Granville 2G SAM
		X76264BOL07: 128Mx16x4 Seymour 1G SAM
		X76264BOL08: 128Mx16x4 Seymour 1G HYN

BOM Config		
* UMA Only LVDS Panel:	BT@/UMAO@/UMA@/ULVDS@/NOMUXL@	+DIMM,USB option
* DIS Only LVDS Panel:	BT@/DIS@/VGA@/DISO@/DLVDS@/NOMUXL@	+DIMM,USB option
* DIS Only EDP Panel:	BT@/DIS@/VGA@/DISO@/DEDP@/NOMUXL@	+DIMM,USB option
* Muxless BACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/BACO@/MUXL@	+X76+GPU(S,W) +DIMM,USB option
* Muxless nonBACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/NOBACO@/MUXL@	+X76+GPU(G) +DIMM,USB option

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

## BTO Option Table

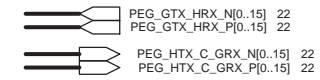
BTO Item	BOM Structure
UMA Only	UMAO@
Muxless/UMA	UMA@
DIS Only	DISO@
Muxless/DIS	DIS@
Muxless/DIS	VGA@
BACO mode	BACO@
nonBACO mode	NOBACO@
VRAM	X76@
128bit VRAM	128@
Granville GPU	GRAN@
Whistler GPU	WHIS@
Seymour GPU	SEYM@
non Granville GPU	NOGRAN@
Blue Tooth	BT@
Connector	CONN@
Unpop	@
DIS eDP	DEDP@
UMA LVDS	ULVDS@
DIS LVDS	DLVDS@
Muxless	MUXL@
non Muxless	NOMUXL@
USB2.0 Conn	USB2@
USB3.0 Conn	USB3@
4 Dimm	4DIMM@

## USB Port Table

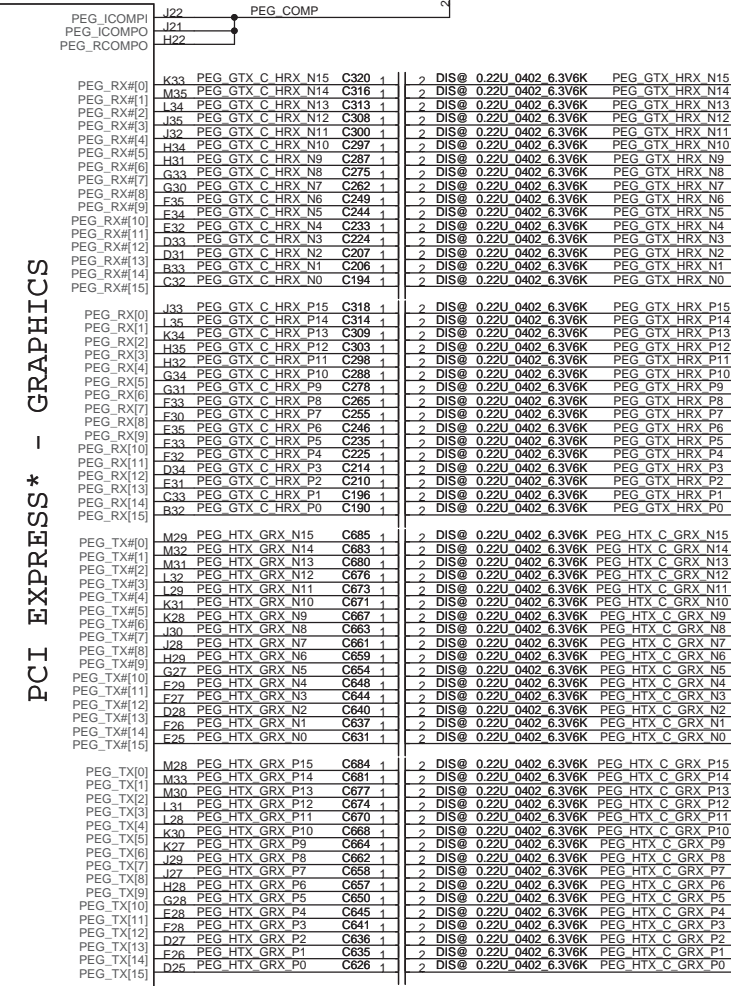
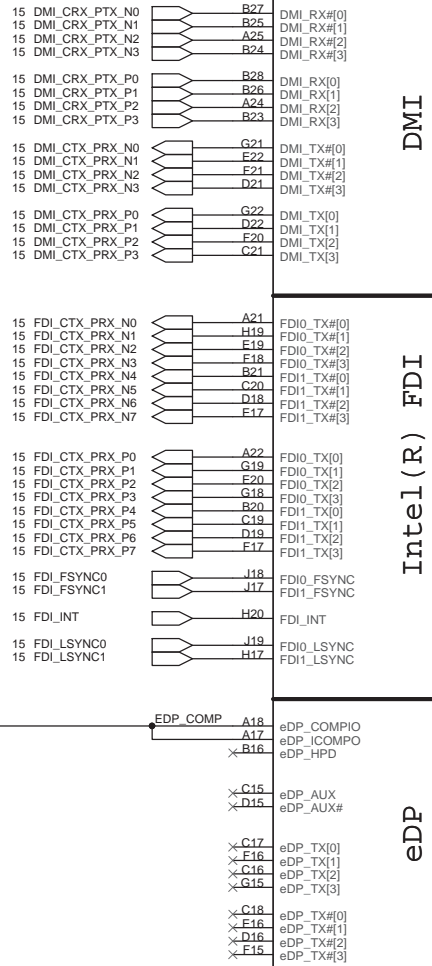
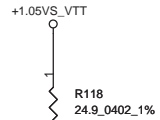
USB 2.0	USB 1.1	Port	3 External USB Port
	UHCI0	0	USB/B(Right side 2.0 option)
		1	USB/B(Right side 2.0 option)
		2	USB port(left side 2.0)
		3	USB/B(Right side 3.0 option)
		4	
		5	
		6	
	UHCI3	7	
		8	Mini Card(WLAN)
		9	Mini Card
		10	Camera
	UHCI4	11	Card Reader
		12	
		13	Blue Tooth

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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



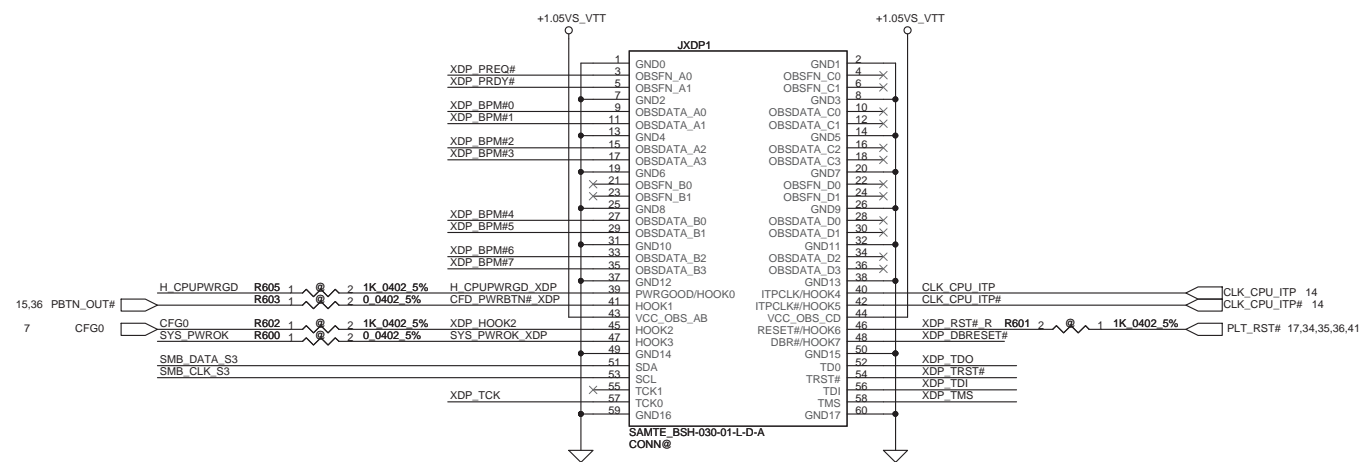
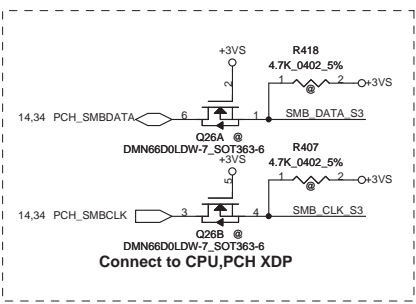
eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms should not be left floating ,even if disable eDP function...



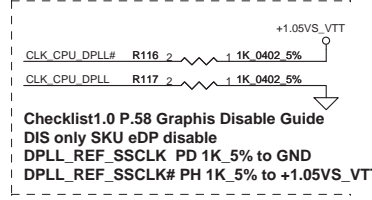
Sandy Bridge\_rPGA\_Rev0p61  
 CONN@

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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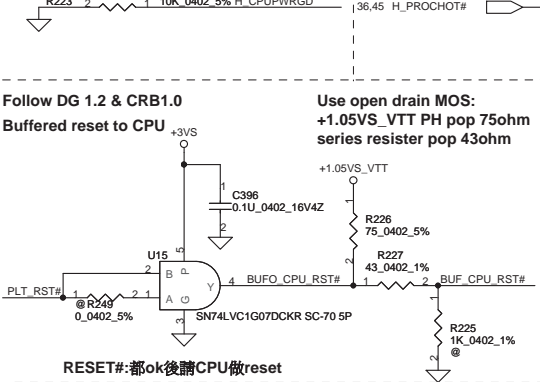
Debug port DG 0.65-  
 Note: 1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed



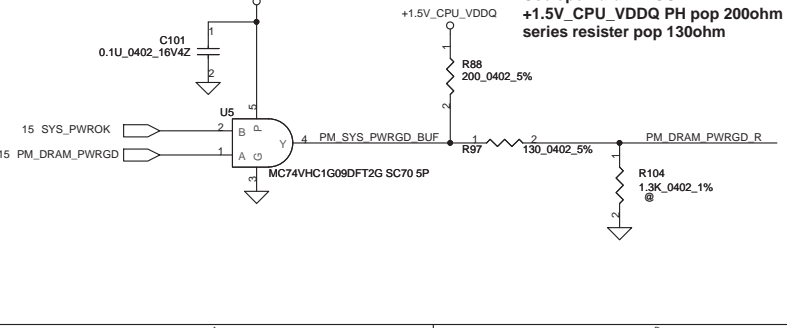
Checklist 1.0 P.58 Graphis Disable Guide  
 DIS only SKU eDP disable  
 DPLL\_REF\_SSCLK PD 1K 5% to GND  
 DPLL\_REF\_SSCLK# PH 1K 5% to +1.05VS\_VTT

PCH->CPU  
 UNCOREPWRGOOD:非CORE外的電OK  
 SM\_DRAMPWROK:DRAM power ok  
 RESET#:都ok後請CPU做reset

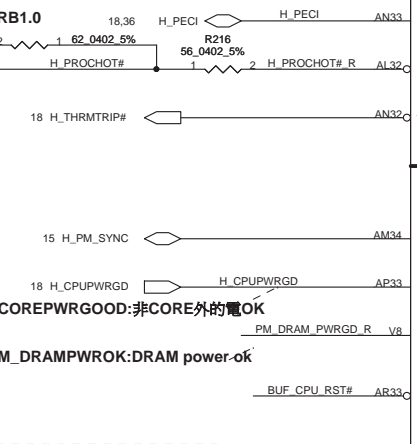
Follow DG 1.2 & CRB1.0



Follow DG 1.2 & CRB1.0



Processor Pullups follow CRB1.0

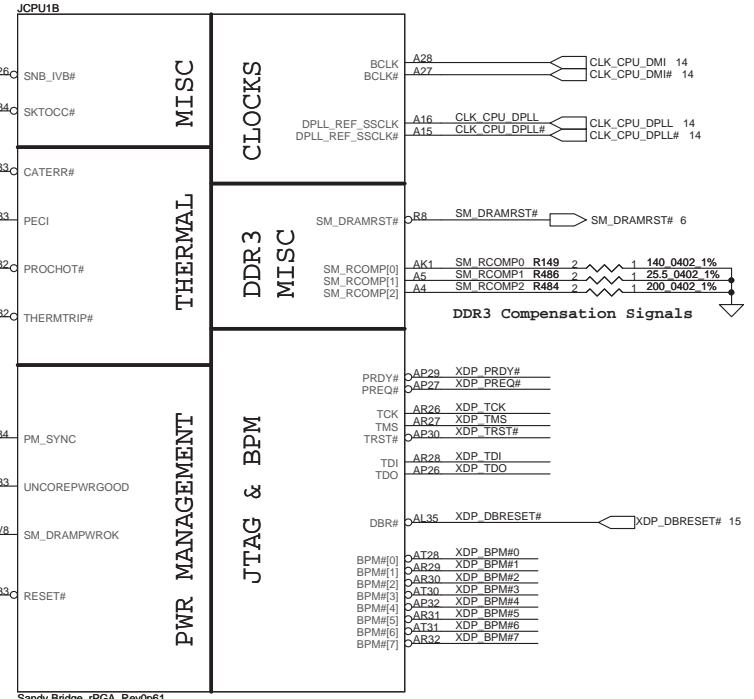


UNCOREPWRGOOD:非CORE外的電OK  
 SM\_DRAMPWROK:DRAM power ok

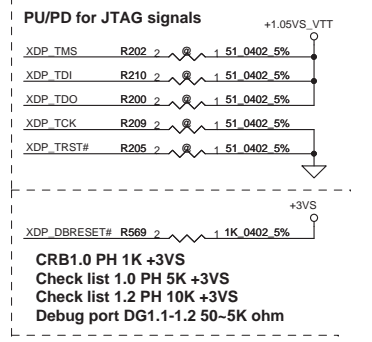
PROC\_SELECT#  
 Future platforms, PH VCPLL and connect to PCH DF\_TVSS

偵測CPU有無安裝

XBOX三紅功能

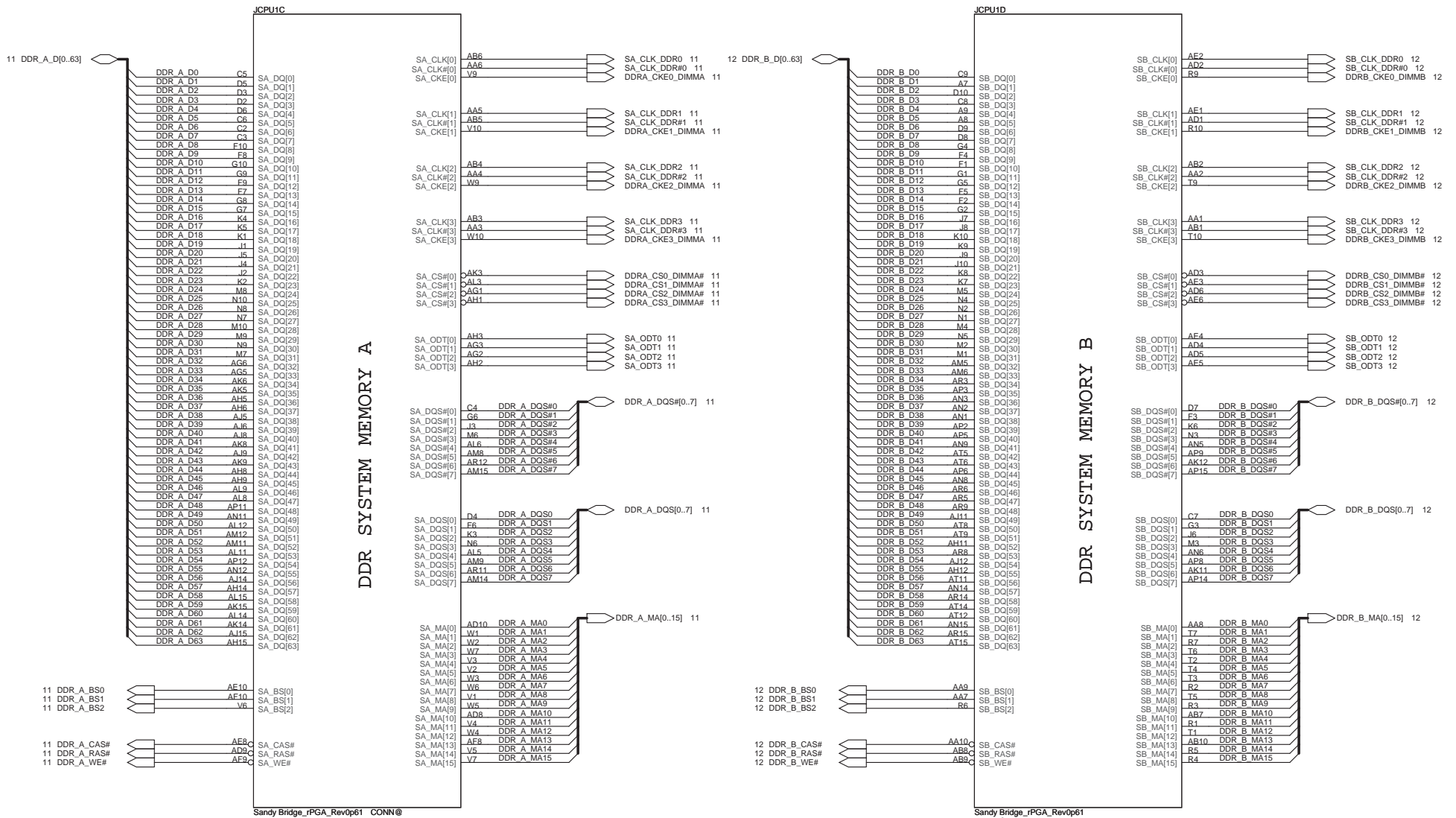


Sandy Bridge iPGA\_Rev0p61  
 CONN@



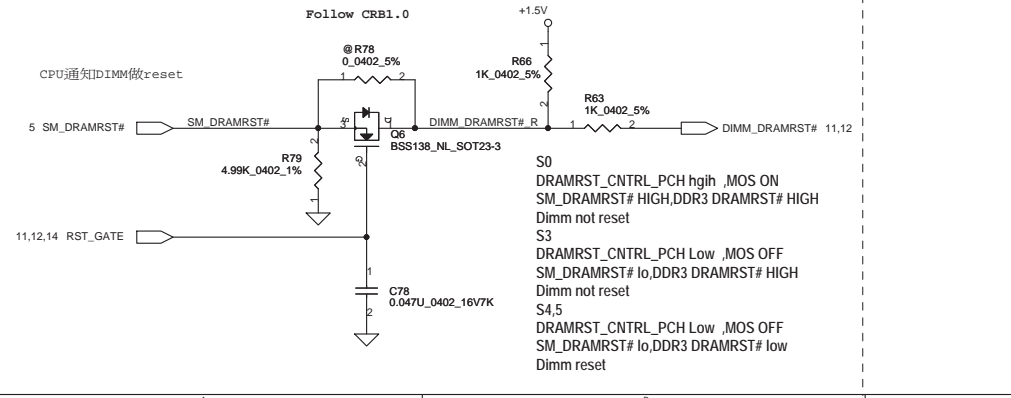
CRB1.0 PH 1K +3VS  
 Check list 1.0 PH 5K +3VS  
 Check list 1.2 PH 10K +3VS  
 Debug port DG1.1-1.2 50-5K ohm

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Sandy Bridge\_rPGA\_Rev0p61 CONN@

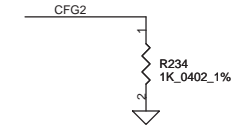
Sandy Bridge\_rPGA\_Rev0p61 CONN@



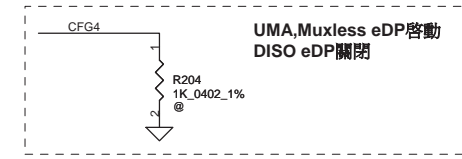
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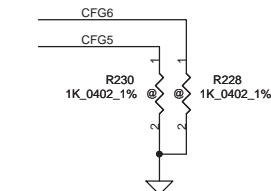
# CFG Straps for Processor



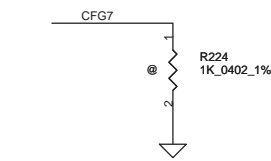
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>* 0: Lane Reversed</p>



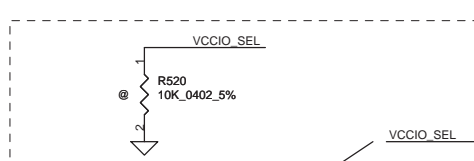
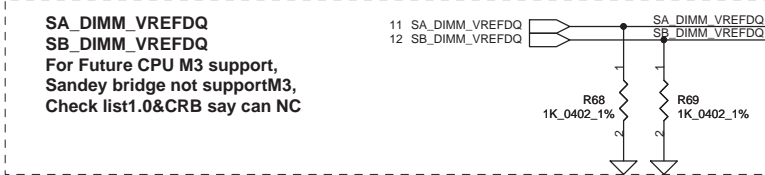
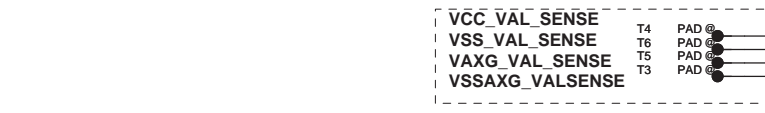
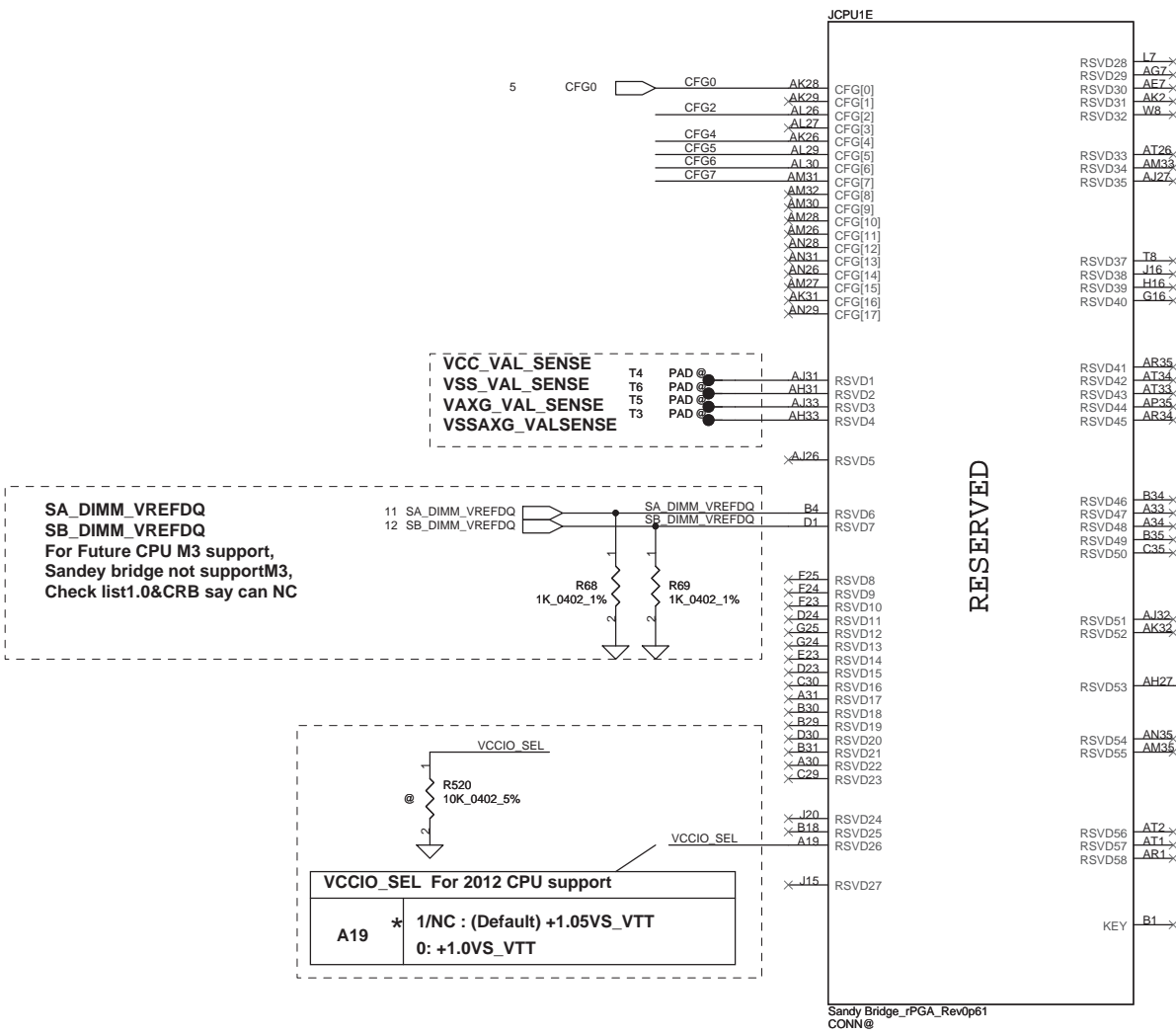
eDP enable	
CFG4	<p>* 1: Disable</p> <p>0: Enable</p>



PCIe Port Bifurcation Straps	
CFG[6:5]	<p>*11: (Default) 1x16 PCI Express</p> <p>10: 2x8 PCI Express</p> <p>01: Reserved</p> <p>00: 1x8,2x4 PCI Express</p>



PEG DEFER TRAINING		CRB1.0 P.12
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>	

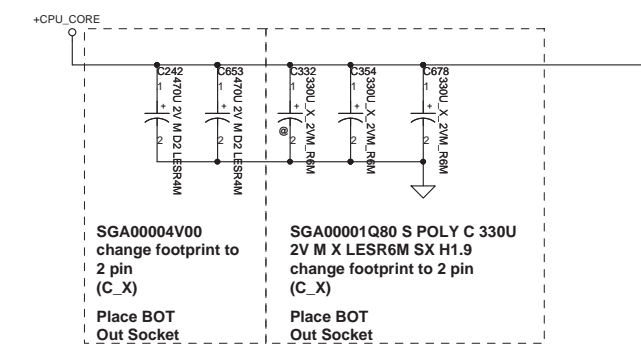
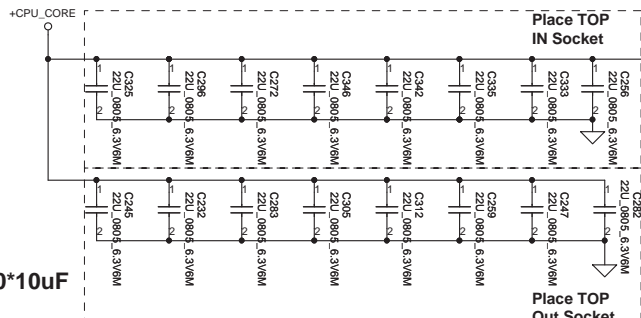
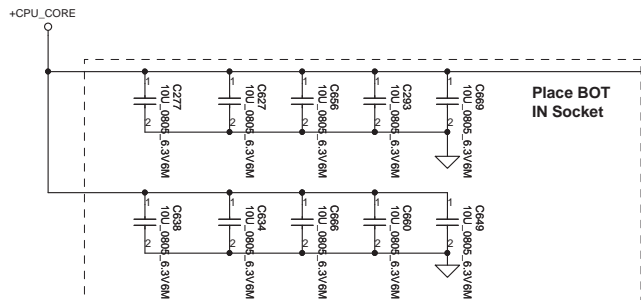


VCCIO_SEL For 2012 CPU support	
A19	<p>* 1/NC : (Default) +1.05VS_VTT</p> <p>0: +1.0VS_VTT</p>

SV type CPU

JCPU1F

POWER



INTEL Recommend  
4\*470uF,16\*22uF and 10\*10uF  
from PDDG 1.0

SGA00004V00  
change footprint to  
2 pin  
(C\_X)  
Place BOT  
Out Socket

SGA00001Q80 S POLY C 330U  
2V M X LESR6M SX H1.9  
change footprint to 2 pin  
(C\_X)  
Place BOT  
Out Socket

QC 94A  
DC 53A

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- VCC51
- Y34
- Y33
- Y32
- Y31
- Y30
- Y29
- Y28
- Y27
- Y26
- Y25
- V34
- V33
- V32
- V31
- V30
- VCC67
- V29
- V28
- V27
- V26
- VCC70
- U35
- U34
- U33
- U32
- VCC74
- U31
- U30
- U29
- U28
- U27
- U26
- R35
- R34
- R33
- R32
- R31
- R30
- R29
- R28
- R27
- R26
- P35
- P34
- P33
- P32
- P31
- P30
- P29
- P28
- P27
- P26

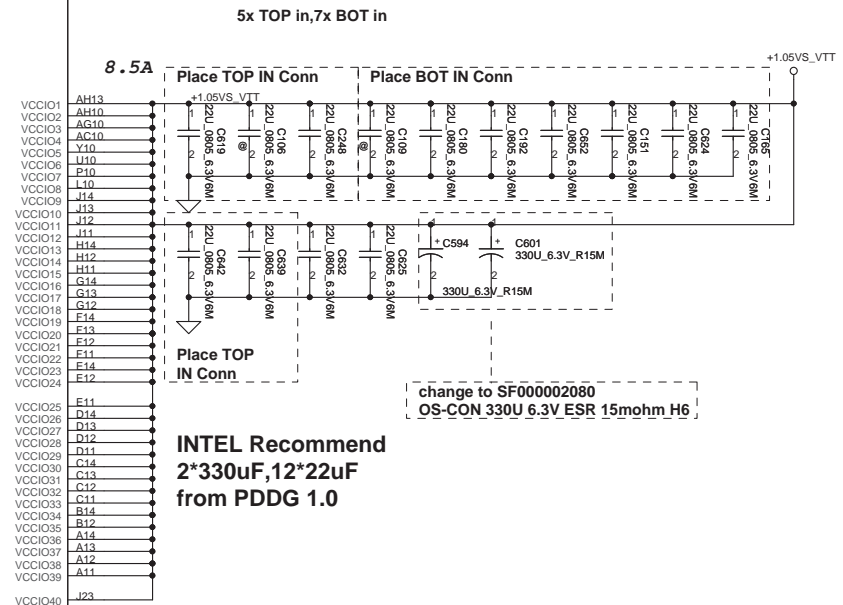
CONN@

Sandy Bridge\_rPGA\_Rev0p61

CORE SUPPLY

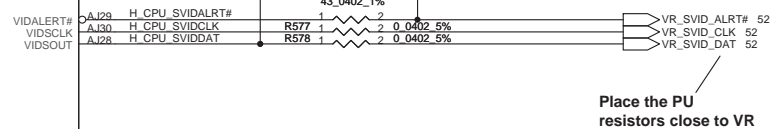
SVID

SENSE LINES

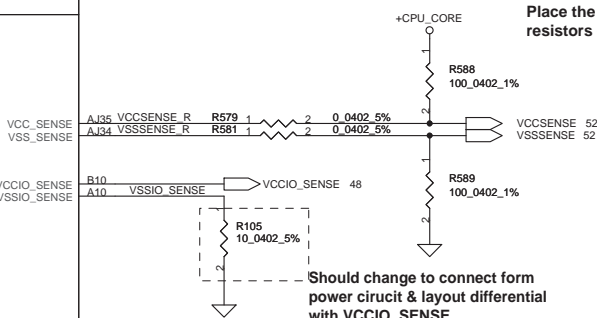


INTEL Recommend  
2\*330uF,12\*22uF  
from PDDG 1.0

change to SF000002080  
OS-CON 330U 6.3V ESR 15mohm H6



Place the PU resistors close to VR



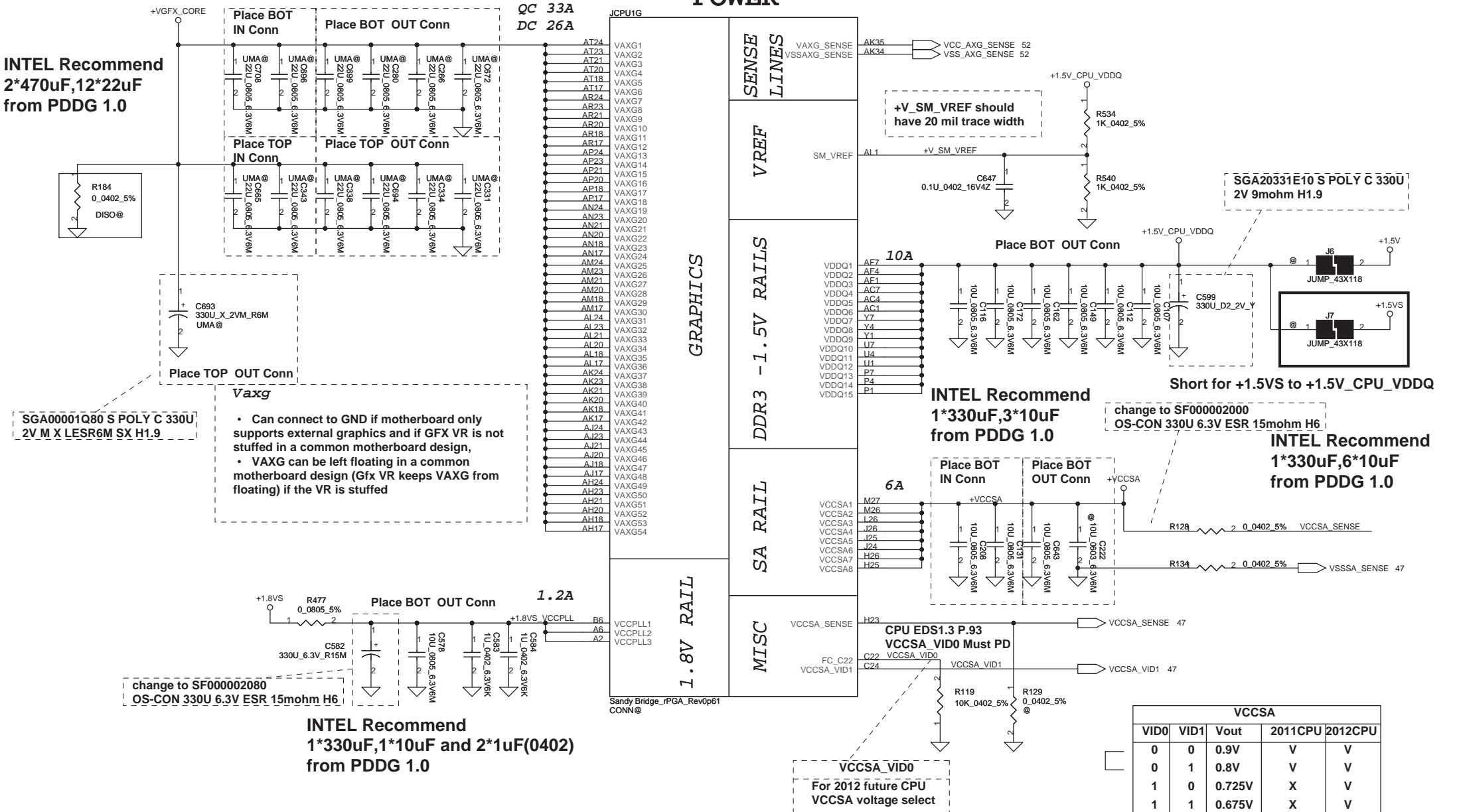
Should change to connect form  
power circuit & layout differential  
with VCCIO\_SENSE.

Place the PU resistors close to CPU

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Sandy Bridge_rPGA_Rev0p61				4019A9	
Date: Tuesday, November 09, 2010				Sheet 8 of 60	



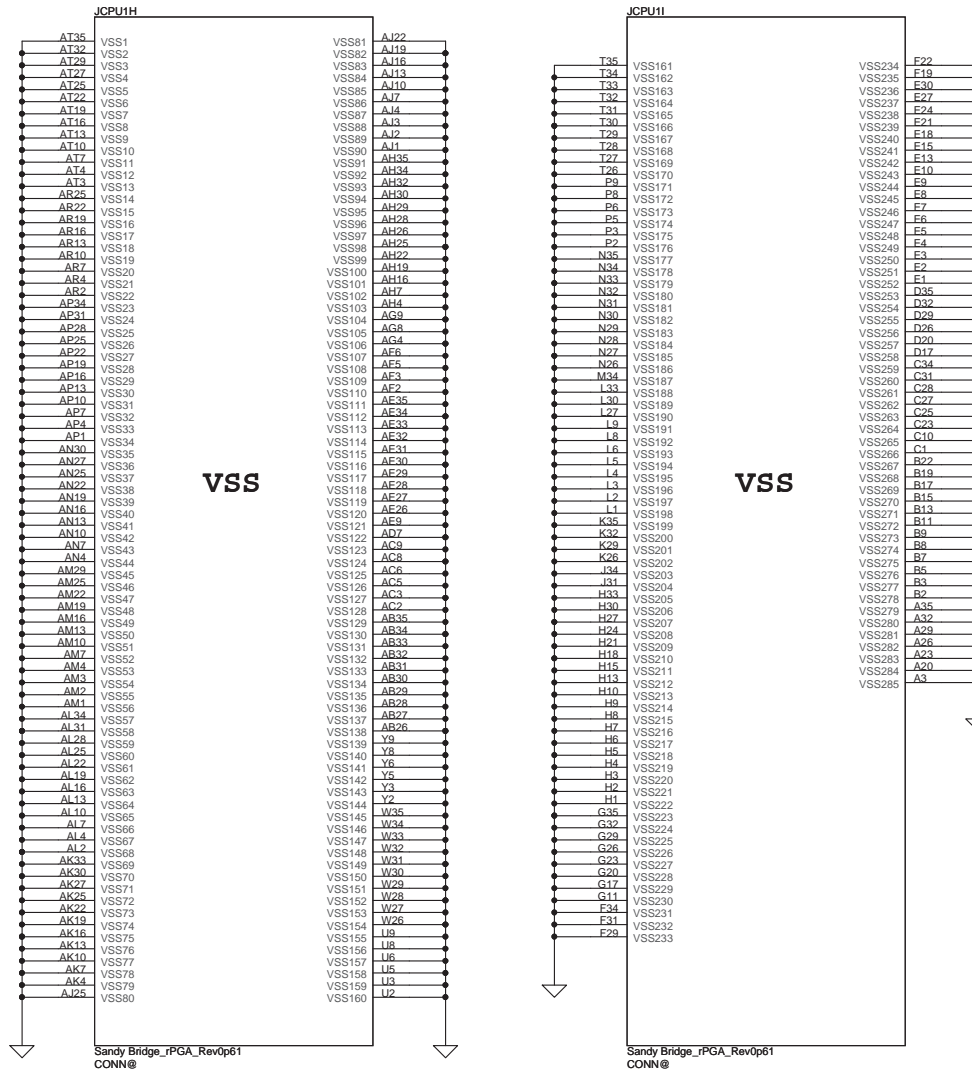
# POWER



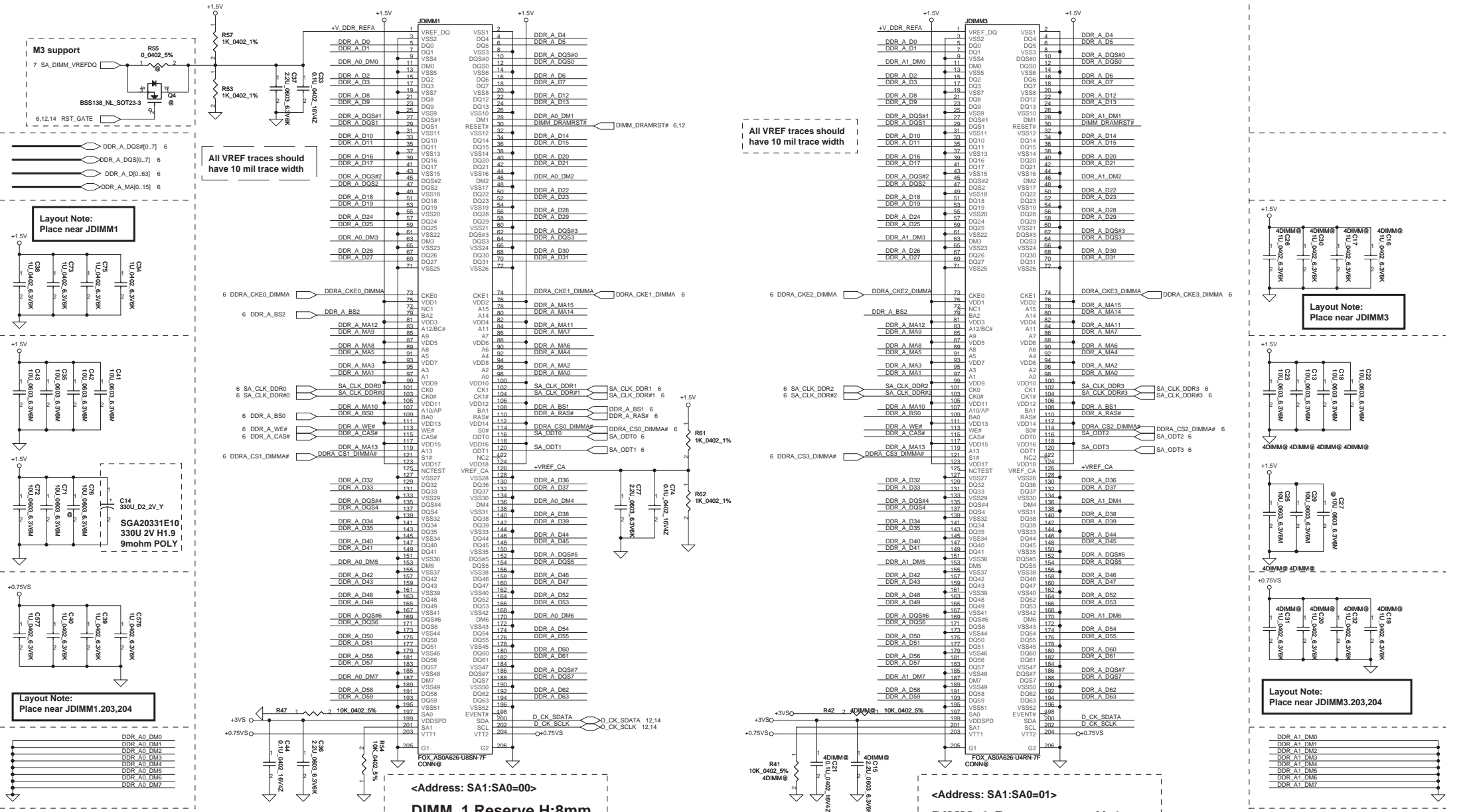
**Vaxg**

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

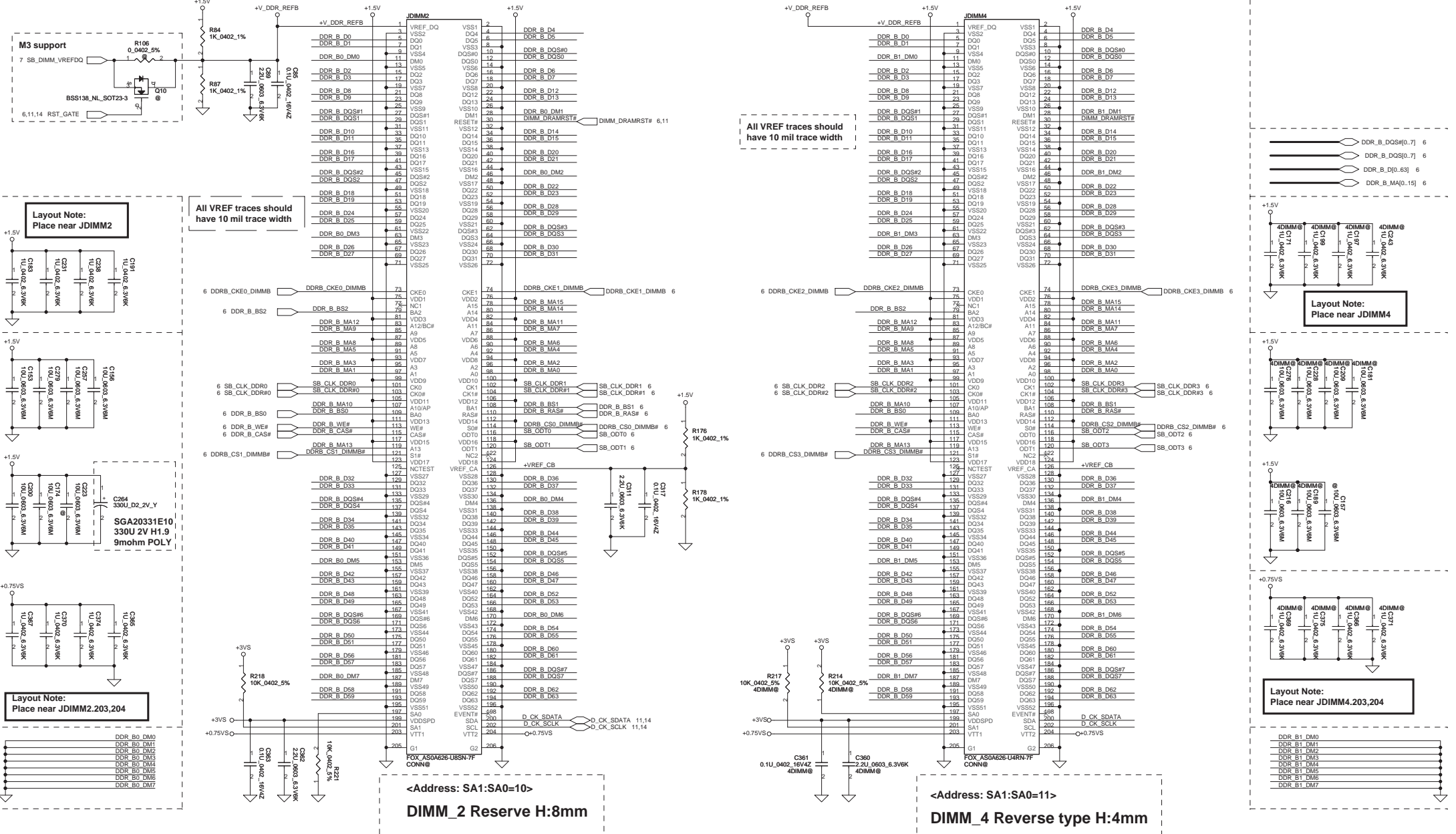
**VCCSA\_VID0**  
For 2012 future CPU  
VCCSA voltage select



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Date:	Tuesday, November 09, 2010	Sheet	10	of	60

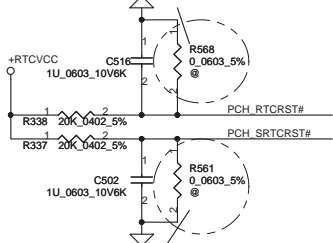


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Document Number	4019A9	Rev	B	Date	Tuesday, November 09, 2010
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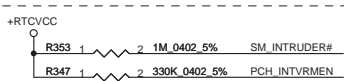


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Document Number	4019A9	Rev	B	Date	Tuesday, November 09, 2010
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**RTCST close RAM door J1**

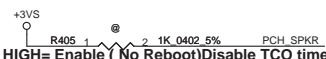


**SRTCST close RAM door J2**



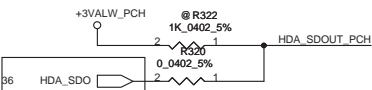
**INTVRMEN**

\* H : Integrated VRM enable  
 L : Integrated VRM disable  
 (INTVRMEN should always be pull high.)

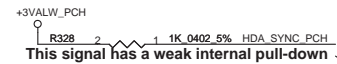


**HIGH= Enable (No Reboot) Disable TCO timer system reboot feature**

\* **LOW= Disable (Default internal PD)**

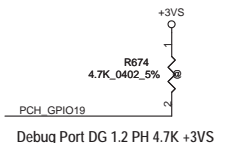
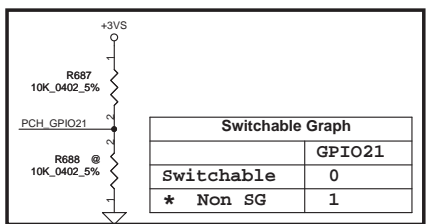
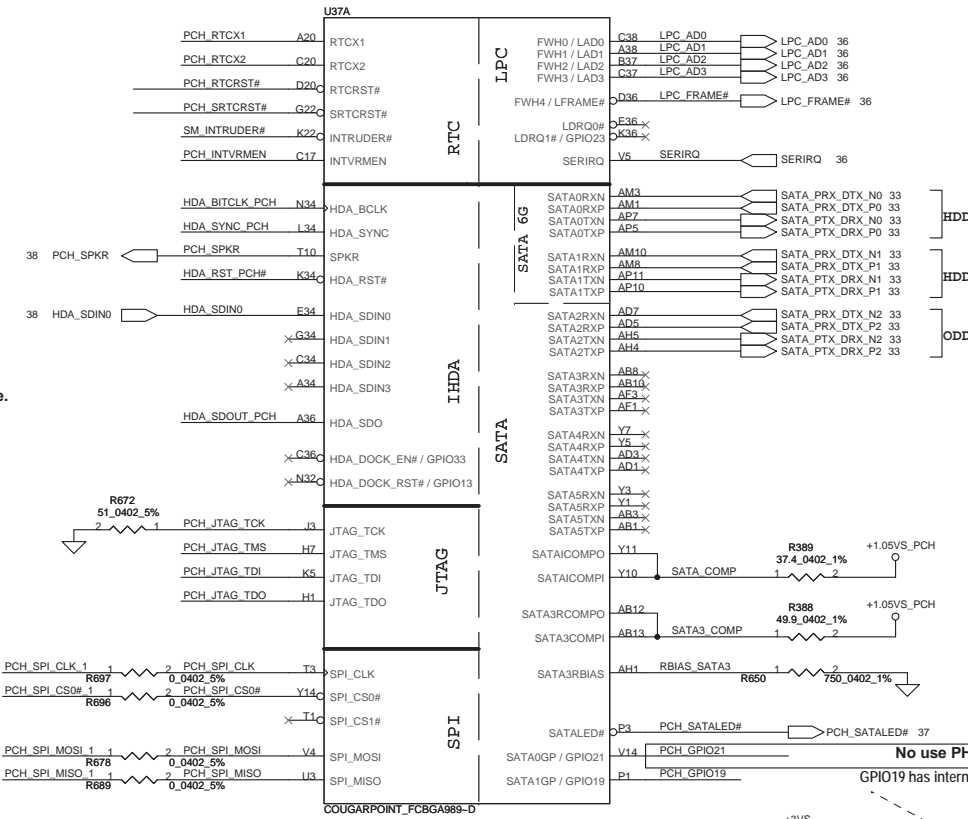
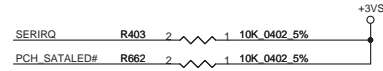
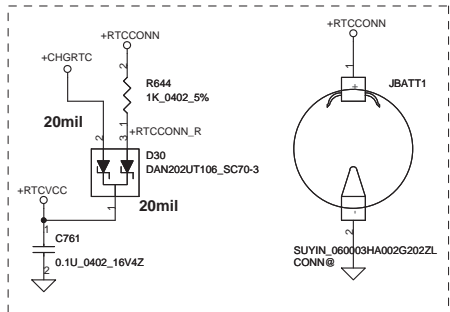
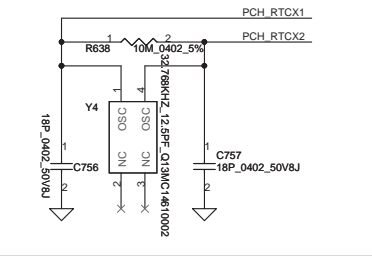
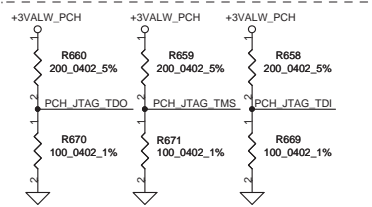
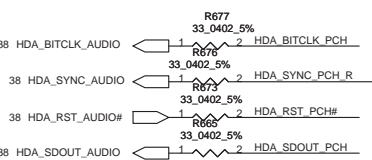


**HDA\_SDO** 為何接至BIC  
 ME debug mode this signal has a weak internal PD  
 Low = Disabled (Default)  
 High = Enabled (Flash Descriptor Security Override)



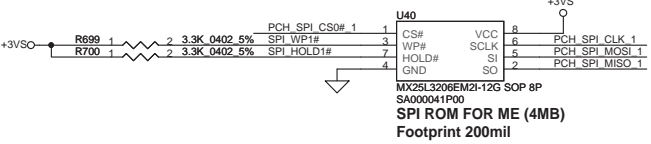
**On Die PLL VR Select is supplied by +1.5V when sampled high  
 1.8V when sampled low  
 Needs to be pulled High for Huron River platform**

Prevent back drive issue.

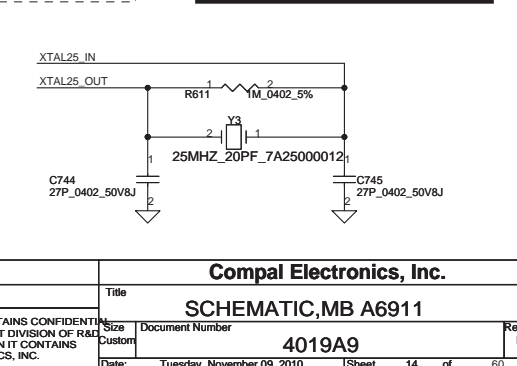
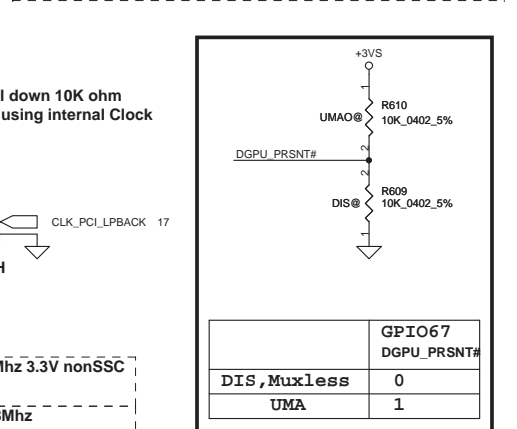
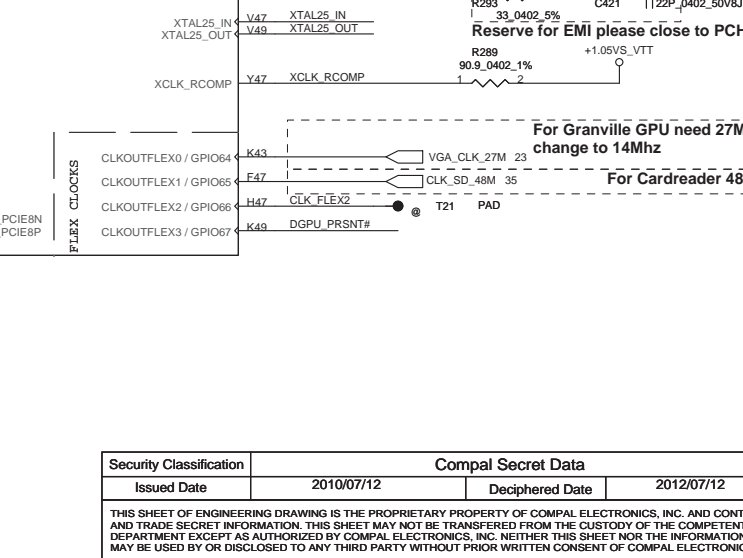
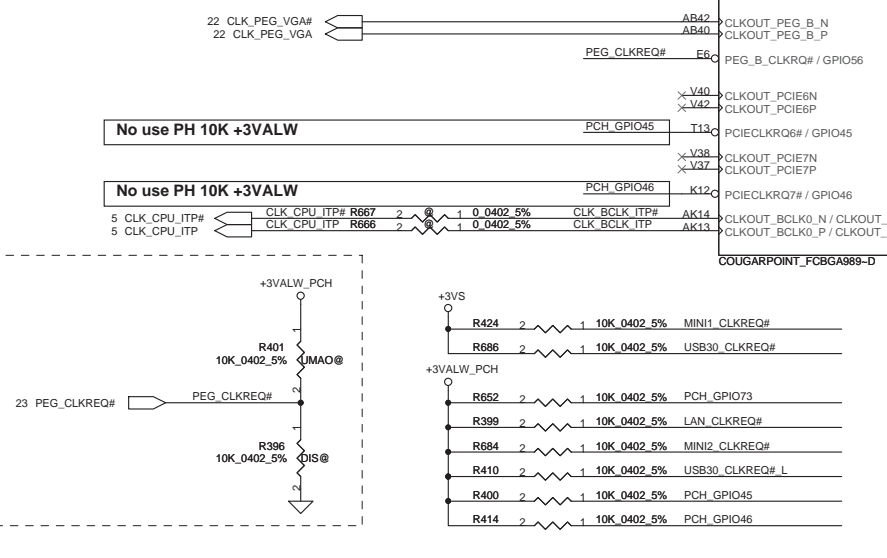
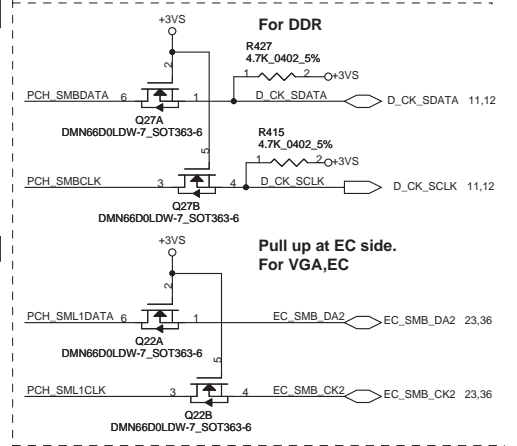
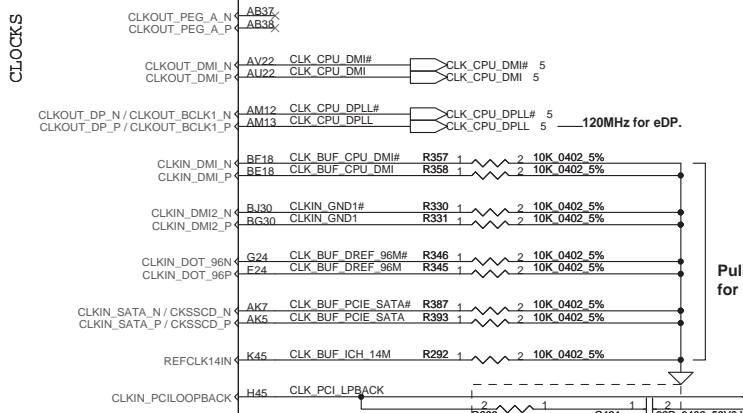
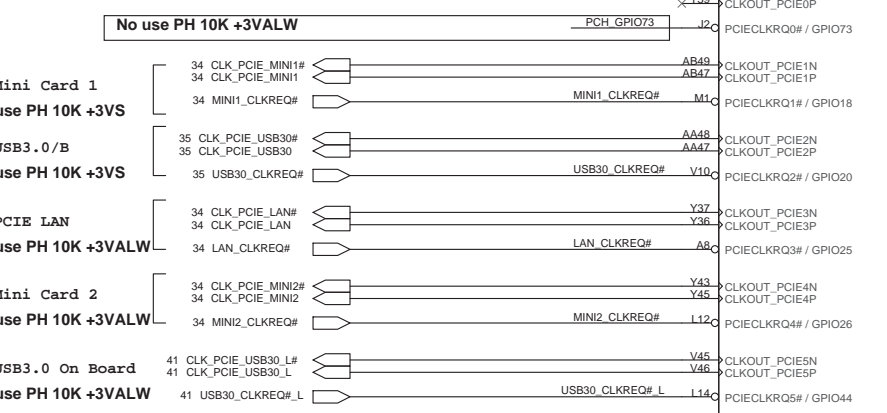
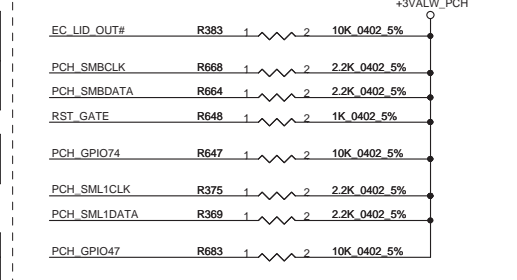
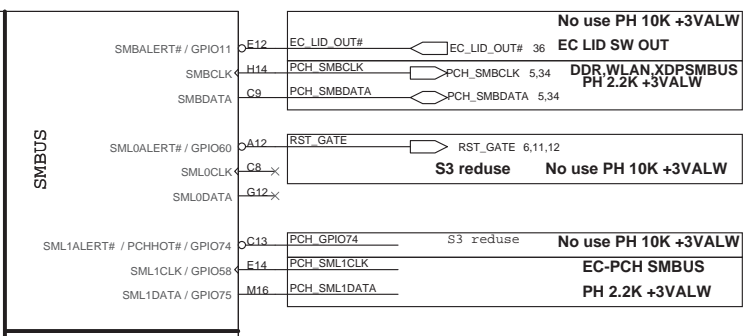
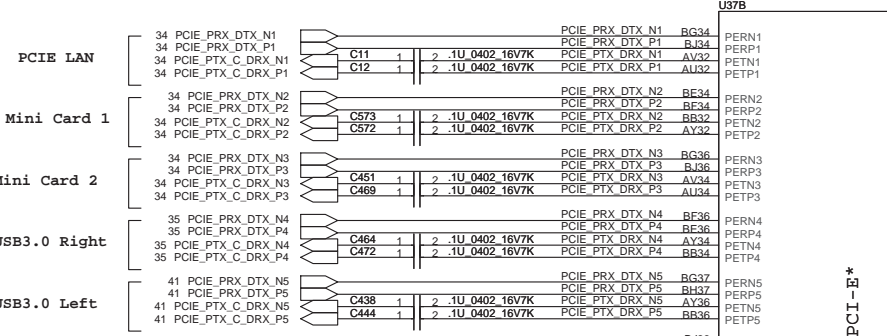


Debug Port DG 1.2 PH 4.7K +3VS

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
* SPI	1	1

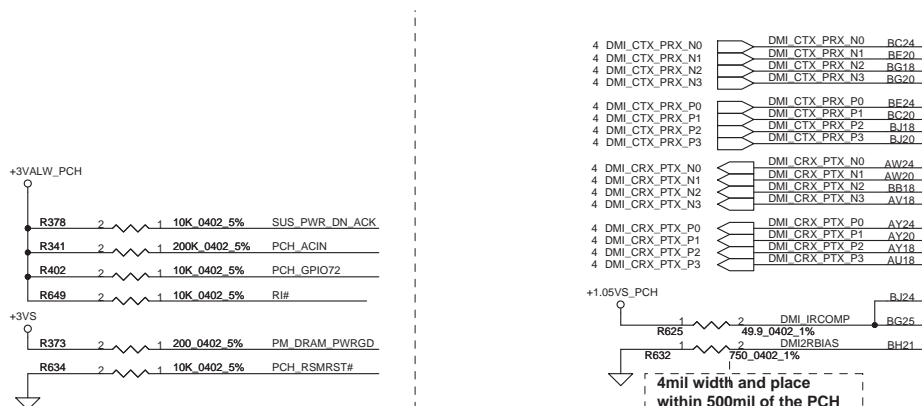






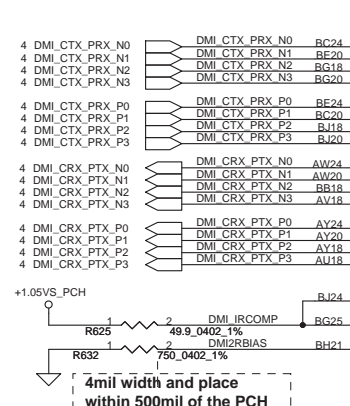
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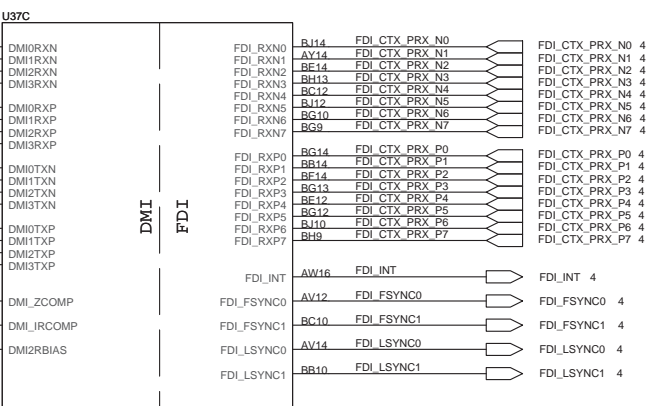


not support Deep S4,S5 mux with SUS\_PWR\_DN\_ACK

not support AMT APWROK can mux with PWROK (check list1.0 P.40)



4mil width and place within 500mil of the PCH

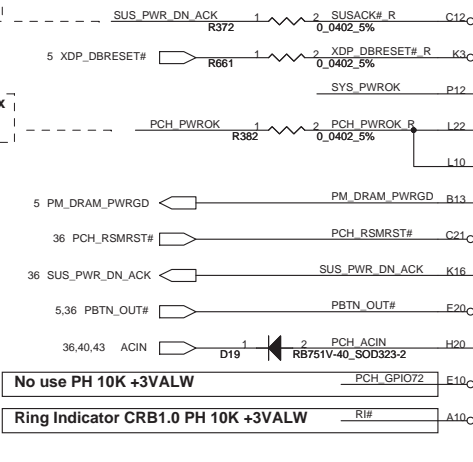
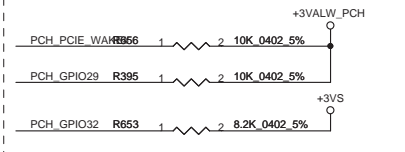
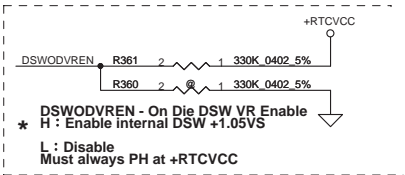


not support Deep S4,S5 DPWROK mux with PWROK check list1.0 P.42

No use PH 10K +3VS

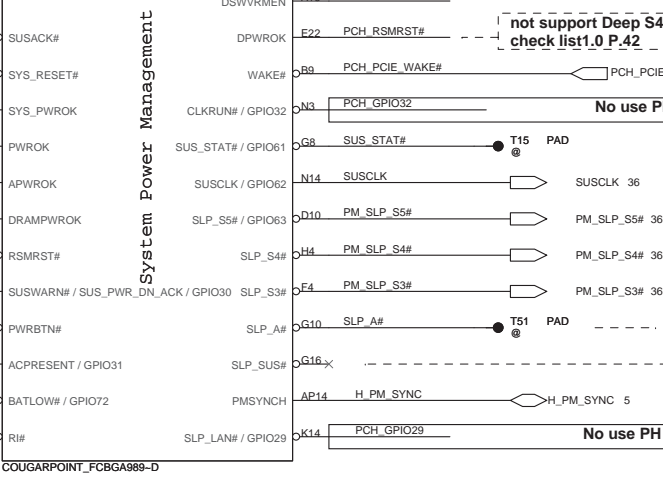
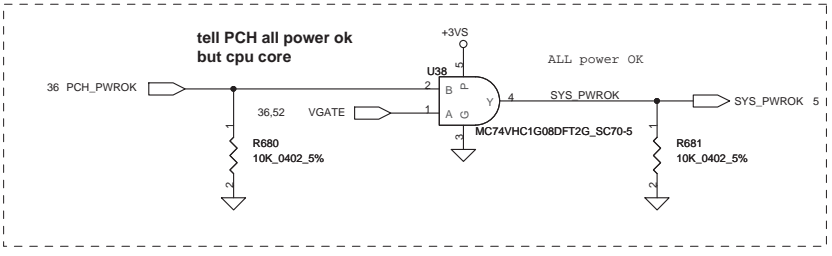
Can be left NC when IAMT is not support on the platform

not support Deep S4,S5 can NC PCH EDS1.2 P.74



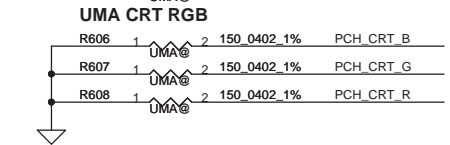
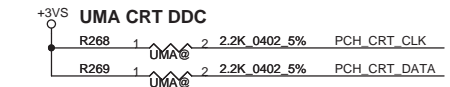
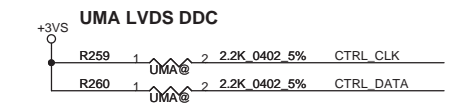
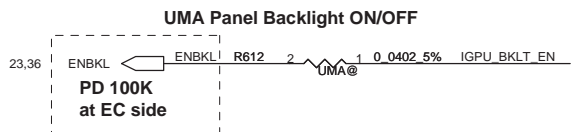
No use PH 10K +3VALW

Ring Indicator CRB1.0 PH 10K +3VALW



No use PH 10K +3VALW

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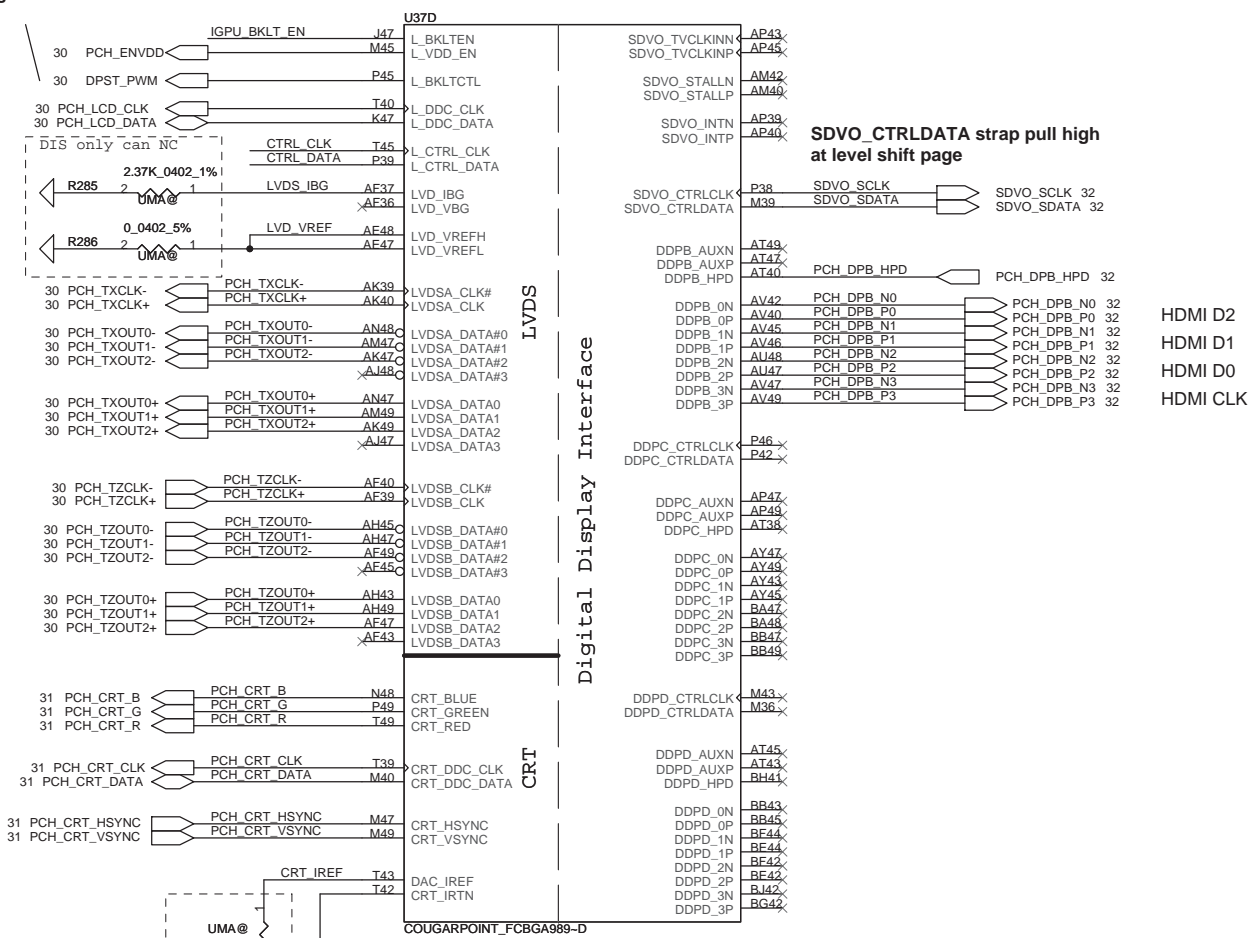


Check list1.0 P.55 disable Graphics  
ALL Can NC  
but DAC\_IREF still need PD

**LVDS disable:**  
DATA/Clock/Control an NC  
VCC\_TX\_LVDS,VCCA\_LVDS PD to GND

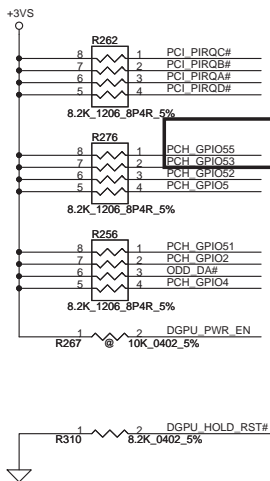
**CRT disable:**  
DATA/Clock/Control an NC  
VCCADAC connect to +3VS

Pull high at LVDS conn side.



DIS only sku can use 1K\_0402\_5% to GND

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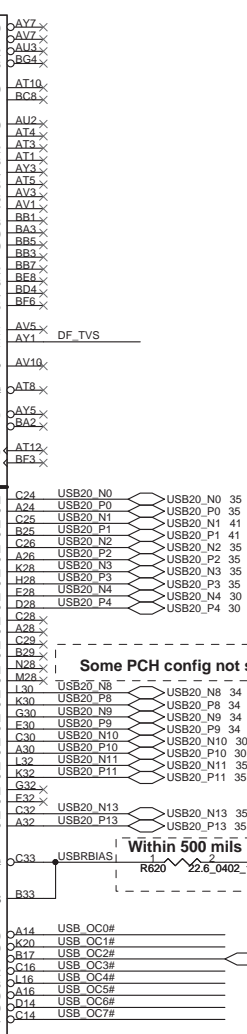
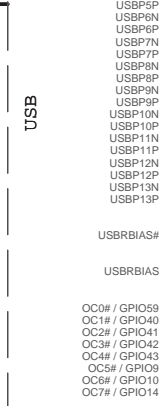
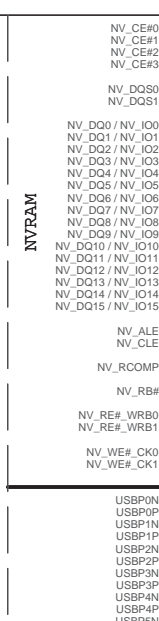
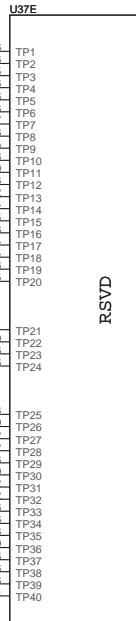
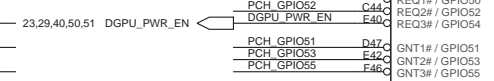
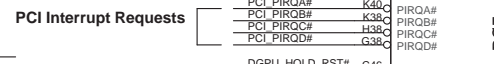
可以不用PH,如做GPIO使用PH+3VS

Boot BIOS Strap			
GNT1#/ GPIO51	GPIO19 GPIO51 Boot BIOS		Destination
	Bit11	Bit10	
Internal	0	1	Reserved
PH	1	0	PCI *
	0	0	SPI
	1	1	LPC

Only GPIO function

只剩GPIO的功能没有strap function  
不做GPIO要PH +3VS,如做GPIO PH +3VS

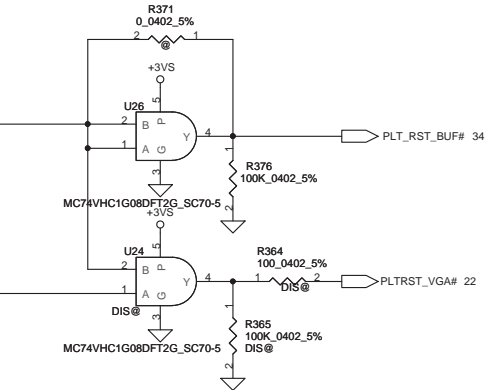
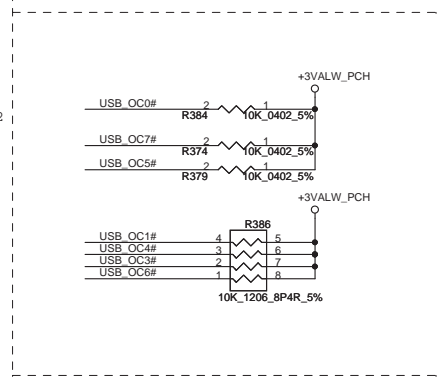
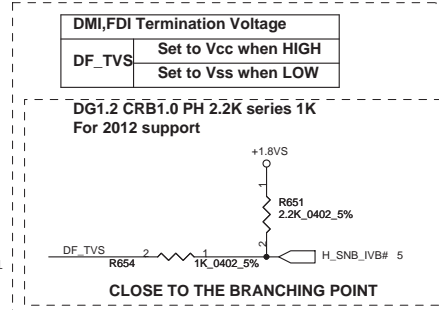
只剩GPIO的功能没有strap function  
無須PH(Internal PH),如做GPIO PH +3VS



Some PCH config not support USB port 6 & 7.

USB2/B (Right side)  
USB2/B (Right side)  
USB Port (Left side)  
USB3/B (right side)  
3D Panel

Mini Card (WLAN)  
Mini Card (WWAN)  
CMOS Camera (LVDS)  
Card Reader  
Mini Card (SIM card)  
Bluetooth



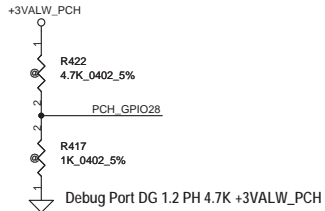
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HDA\_SYNC PH(PLL =+1.5VS)

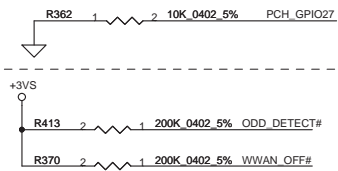
**GPIO28**

**On-Die PLL Voltage Regulator**

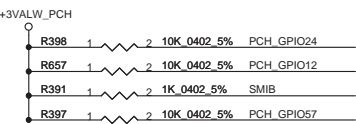
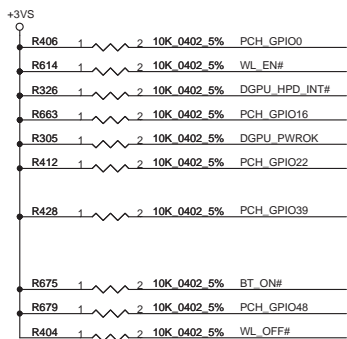
This signal has a weak internal pull up  
 \* H : On-Die PLL voltage regulator enable  
 L : On-Die PLL Voltage Regulator disable



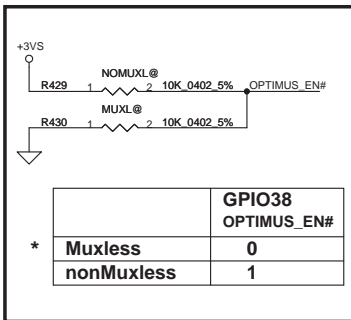
**Deep S4,S5 wake event signal**  
 RTC alarm,Power BTN,GPIO27  
 PCH\_GPIO27 (Have internal Pull-High)  
 Deep S4,S5 wake event signal  
 No use PD to GND Check list1.0 P.70



**SATA2GP/GPIO36 & SATA3GP/GPIO37**  
 Sampled at Rising edge of PWROK.  
 Weak internal pull-down.  
 (weak internal pull-down is disabled after PLTRST# de-asserts)  
 NOTE: This signal should NOT be pulled high when strap is sampled

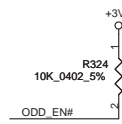


No use PH 10K +3VS	PCH_GPIO0	TZ
No use PH 10K +3VS	35 WL_EN#	A42
No use PH 10K +3VS	32 DGPU_HPD_INT#	H36
	36 EC_SCI#	E38
	36 EC_SMI#	C10
No use PH +3VALW	PCH_GPIO12	C4
USB3.0 System management Interrupt signal "SMIB#"	35,41 SMIB	G2
No use PH +3VS	PCH_GPIO16	U2
	29,49 VGA_PWROK	R304
No use PH 10K +3VS	PCH_GPIO22	T5
CRB1.0 PH 10K +3VALW	PCH_GPIO24	E8
No use PD 10K to GND	PCH_GPIO27	E16
No use PH 10K +3VALW	PCH_GPIO28	P8
No use PH 10K +3VS BT ON/OFF	34,35 BT_ON#	K4
No use can NC	PAD T16 @	K4
Can't PH	33 ODD_DETECT#	V8
Can't PH	34 WWAN_OFF#	M5
No use PH 10K +3VS Optimus(L)/ non optimus(H)	OPTIMUS_EN#	N2
No use PH 10K +3VS	PCH_GPIO39	M3
No use PH 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PH 10K +3VSWL_OFF#	WL_OFF#	V3
No use PH +3VALW or PD to GND	PCH_GPIO57	D6

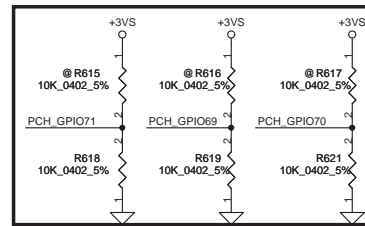


	GPIO38 OPTIMUS_EN#
* Muxless	0
nonMuxless	1

**GPIO24 Unmultiplexed**  
 NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.  
 CRB1.0 PH10K to +3VALW



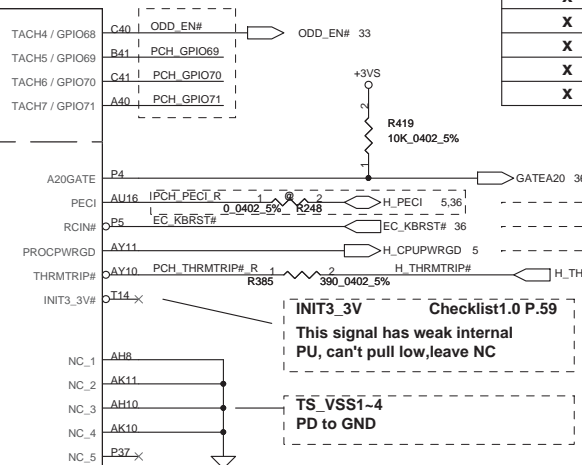
Fan Tachometer Inputs  
 TACH1-7 only on server can insted to GPIO



Project ID	GPIO69	GPIO70	GPIO71
* P7YE0	0	0	0
X	0	0	1
X	0	1	0
X	0	1	1
X	1	0	0
X	0	0	1
X	0	1	0
X	0	1	1
X	1	0	0
X	1	0	1
X	1	1	0
X	1	1	1

U37F	GPIO	GPIO
BMBUSY# / GPIO0	TACH4 / GPIO68	C40
TACH1 / GPIO1	TACH5 / GPIO69	B41
TACH2 / GPIO6	TACH6 / GPIO70	C41
TACH3 / GPIO7	TACH7 / GPIO71	A40
GPIO8		
LAN_PHY_PWR_CTRL / GPIO12		
GPIO15		
SATA4GP / GPIO16		
TACH0 / GPIO17		
SCLOCK / GPIO22		
GPIO24 / MEM_LED		
GPIO27		
GPIO28		
STP_PC# / GPIO34		
GPIO35		
SATA2GP / GPIO36		
SATA3GP / GPIO37		
SLOAD / GPIO38		
SDATAOUT0 / GPIO39		
SDATAOUT1 / GPIO48		
SATA5GP / GPIO49		
GPIO57		

GPIO  
 CPU/MISC  
 NCTF

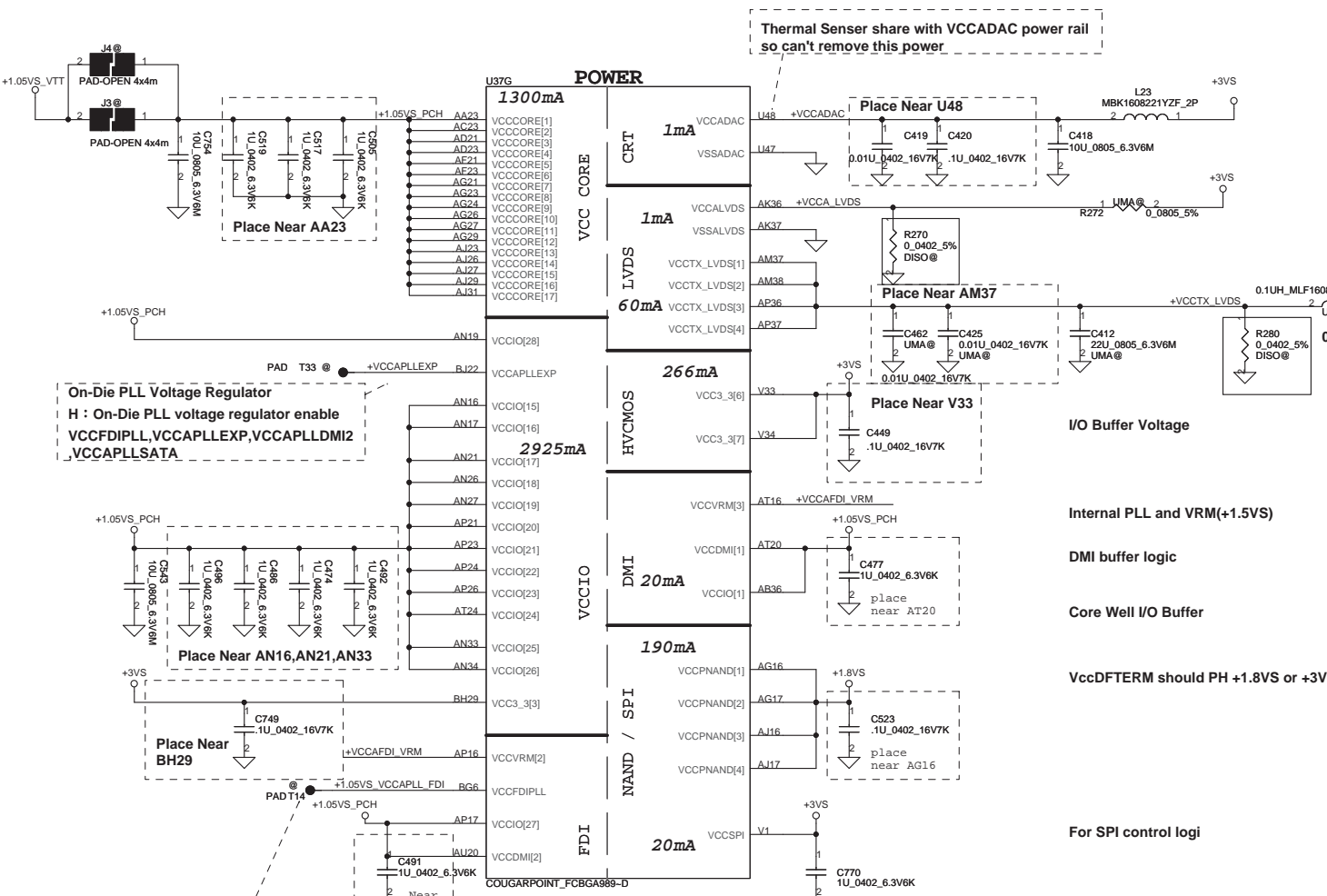


INIT3\_3V Checklist1.0 P.59  
 This signal has weak internal PU, can't pull low,leave NC  
 TS\_VSS1-4 PD to GND

PECI CPU-EC  
 CTRL+ALT+DEL non CPU power ok  
 130c shut sown

PAD T47 @	A4	VSS_NCTF_1
PAD T30 @	A44	VSS_NCTF_2
PAD T28 @	A45	VSS_NCTF_3
PAD T27 @	A46	VSS_NCTF_4
PAD T49 @	A5	VSS_NCTF_5
PAD T46 @	A6	VSS_NCTF_6
PAD T50 @	B3	VSS_NCTF_7
PAD T26 @	B47	VSS_NCTF_8
PAD T43 @	BD1	VSS_NCTF_9
PAD T17 @	BD49	VSS_NCTF_10
PAD T44 @	BE1	VSS_NCTF_11
PAD T23 @	BE49	VSS_NCTF_12
PAD T45 @	BE1	VSS_NCTF_13
PAD T18 @	BF49	VSS_NCTF_14

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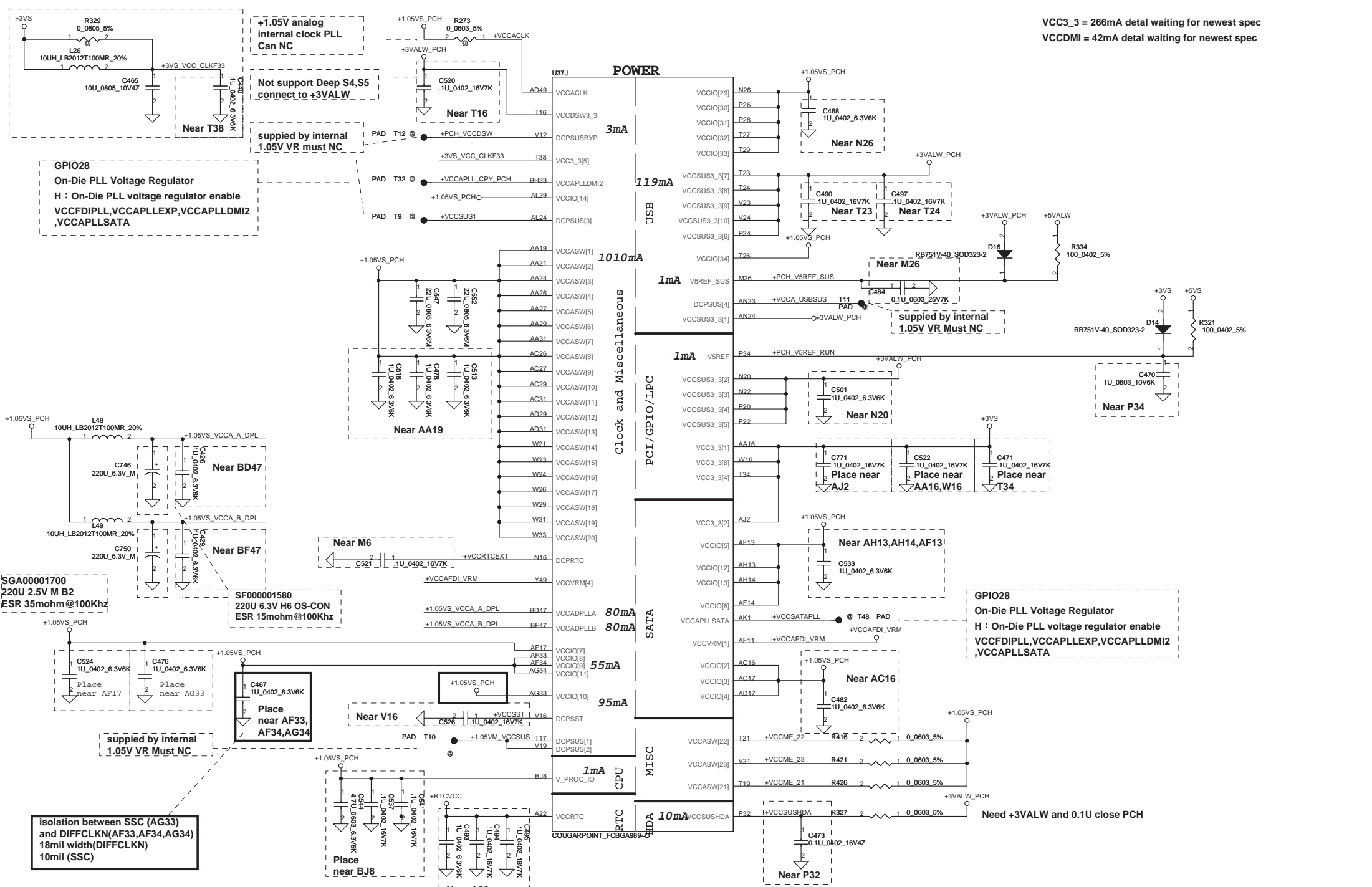


**On-Die PLL Voltage Regulator**  
 H : On-Die PLL voltage regulator enable  
 VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

**On-Die PLL Voltage Regulator**  
 H : On-Die PLL voltage regulator enable  
 VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

VCCVRM ==> 1.5V FOR MOBILE  
 VCCVRM ==> 1.8V FOR DESKTOP  
 VCCVRM = 160mA detat waiting for newest spec  
 HDA\_SYNC PH(PLL ==+1.5VS)

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TV5
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)



VCC3\_3 = 266mA detal waiting for newest spec  
VCCDMI = 42mA detal waiting for newest spec

**POWER**

**USB**

**Clock and Miscellaneous**

**PCI/GPIO/LPC**

**SATA**

**MISC**

**CPU**

**RTC**

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		2012/07/12

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U37H		H5	
VSS[0]		VSS[0]	
VSS[1]	AK38	VSS[1]	
VSS[2]	AK4	VSS[2]	
VSS[3]	AK42	VSS[3]	
VSS[4]	AK46	VSS[4]	
VSS[5]	AK8	VSS[5]	
VSS[6]	AL16	VSS[6]	
VSS[7]	AL17	VSS[7]	
VSS[8]	AL19	VSS[8]	
VSS[9]	AL2	VSS[9]	
VSS[10]	AL21	VSS[10]	
VSS[11]	AL23	VSS[11]	
VSS[12]	AL26	VSS[12]	
VSS[13]	AL27	VSS[13]	
VSS[14]	AL31	VSS[14]	
VSS[15]	AL33	VSS[15]	
VSS[16]	AL34	VSS[16]	
VSS[17]	AL46	VSS[17]	
VSS[18]	AM11	VSS[18]	
VSS[19]	AM14	VSS[19]	
VSS[20]	AM36	VSS[20]	
VSS[21]	AM39	VSS[21]	
VSS[22]	AM43	VSS[22]	
VSS[23]	AM45	VSS[23]	
VSS[24]	AM7	VSS[24]	
VSS[25]	AM7	VSS[25]	
VSS[26]	AN2	VSS[26]	
VSS[27]	AN29	VSS[27]	
VSS[28]	AN3	VSS[28]	
VSS[29]	AN31	VSS[29]	
VSS[30]	AP12	VSS[30]	
VSS[31]	AP19	VSS[31]	
VSS[32]	AP28	VSS[32]	
VSS[33]	AP30	VSS[33]	
VSS[34]	AP32	VSS[34]	
VSS[35]	AP38	VSS[35]	
VSS[36]	AP4	VSS[36]	
VSS[37]	AP42	VSS[37]	
VSS[38]	AP46	VSS[38]	
VSS[39]	AP8	VSS[39]	
VSS[40]	AR2	VSS[40]	
VSS[41]	AR48	VSS[41]	
VSS[42]	AT11	VSS[42]	
VSS[43]	AT13	VSS[43]	
VSS[44]	AT18	VSS[44]	
VSS[45]	AT22	VSS[45]	
VSS[46]	AT26	VSS[46]	
VSS[47]	AT28	VSS[47]	
VSS[48]	AT30	VSS[48]	
VSS[49]	AT32	VSS[49]	
VSS[50]	AT34	VSS[50]	
VSS[51]	AT39	VSS[51]	
VSS[52]	AT42	VSS[52]	
VSS[53]	AT46	VSS[53]	
VSS[54]	AT7	VSS[54]	
VSS[55]	AU24	VSS[55]	
VSS[56]	AU30	VSS[56]	
VSS[57]	AV16	VSS[57]	
VSS[58]	AV20	VSS[58]	
VSS[59]	AV24	VSS[59]	
VSS[60]	AV30	VSS[60]	
VSS[61]	AV38	VSS[61]	
VSS[62]	AV4	VSS[62]	
VSS[63]	AV43	VSS[63]	
VSS[64]	AV8	VSS[64]	
VSS[65]	AW14	VSS[65]	
VSS[66]	AW18	VSS[66]	
VSS[67]	AW2	VSS[67]	
VSS[68]	AW22	VSS[68]	
VSS[69]	AW26	VSS[69]	
VSS[70]	AW28	VSS[70]	
VSS[71]	AW32	VSS[71]	
VSS[72]	AW34	VSS[72]	
VSS[73]	AW36	VSS[73]	
VSS[74]	AW40	VSS[74]	
VSS[75]	AW48	VSS[75]	
VSS[76]	AY11	VSS[76]	
VSS[77]	AY12	VSS[77]	
VSS[78]	AY22	VSS[78]	
VSS[79]	AY28	VSS[79]	

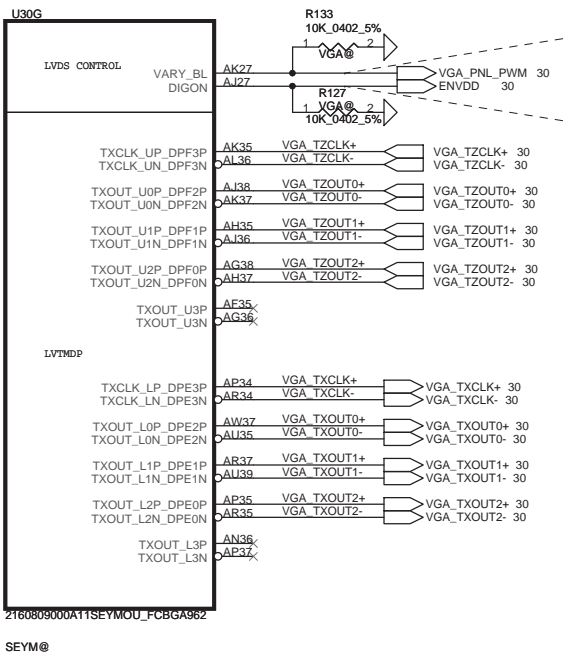
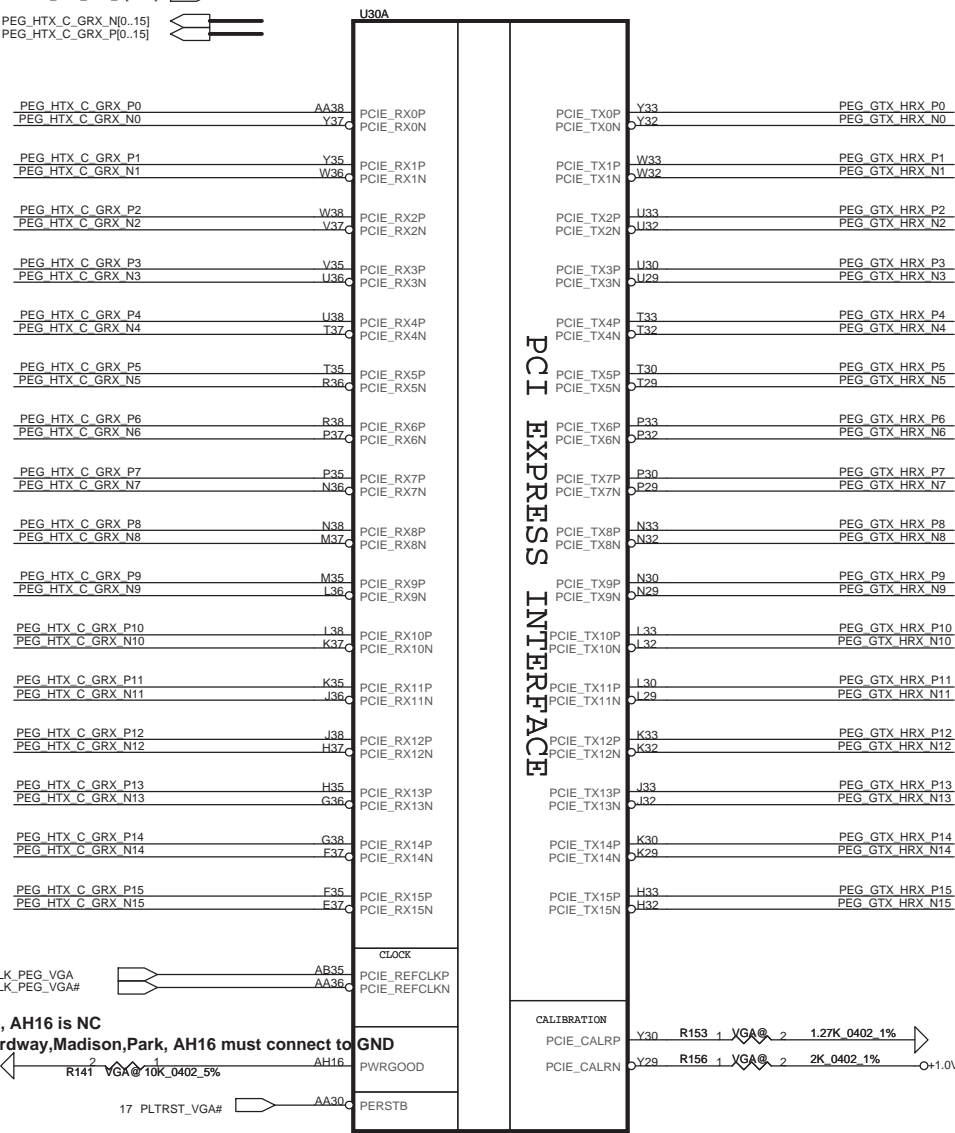
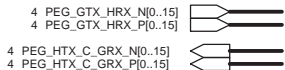
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U37I		H46	
VSS[159]		VSS[259]	
VSS[160]		VSS[260]	K18
VSS[161]		VSS[261]	K26
VSS[162]		VSS[262]	K36
VSS[163]		VSS[263]	K46
VSS[164]		VSS[264]	K7
VSS[165]		VSS[265]	L18
VSS[166]		VSS[266]	L2
VSS[167]		VSS[267]	L20
VSS[168]		VSS[268]	L26
VSS[169]		VSS[269]	L28
VSS[170]		VSS[270]	L36
VSS[171]		VSS[271]	L48
VSS[172]		VSS[272]	M12
VSS[173]		VSS[273]	P16
VSS[174]		VSS[274]	M18
VSS[175]		VSS[275]	M22
VSS[176]		VSS[276]	M24
VSS[177]		VSS[277]	M30
VSS[178]		VSS[278]	M32
VSS[179]		VSS[279]	M34
VSS[180]		VSS[280]	M38
VSS[181]		VSS[281]	M4
VSS[182]		VSS[282]	M42
VSS[183]		VSS[283]	M46
VSS[184]		VSS[284]	M8
VSS[185]		VSS[285]	N18
VSS[186]		VSS[286]	P30
VSS[187]		VSS[287]	N47
VSS[188]		VSS[288]	P11
VSS[189]		VSS[289]	P18
VSS[190]		VSS[290]	T33
VSS[191]		VSS[291]	P40
VSS[192]		VSS[292]	P43
VSS[193]		VSS[293]	P47
VSS[194]		VSS[294]	P7
VSS[195]		VSS[295]	R2
VSS[196]		VSS[296]	R48
VSS[197]		VSS[297]	T12
VSS[198]		VSS[298]	T31
VSS[199]		VSS[299]	T37
VSS[200]		VSS[300]	T4
VSS[201]		VSS[301]	W34
VSS[202]		VSS[302]	T46
VSS[203]		VSS[303]	T47
VSS[204]		VSS[304]	T8
VSS[205]		VSS[305]	V11
VSS[206]		VSS[306]	V17
VSS[207]		VSS[307]	V26
VSS[208]		VSS[308]	V27
VSS[209]		VSS[309]	V29
VSS[210]		VSS[310]	V31
VSS[211]		VSS[311]	V36
VSS[212]		VSS[312]	V38
VSS[213]		VSS[313]	V43
VSS[214]		VSS[314]	V7
VSS[215]		VSS[315]	W17
VSS[216]		VSS[316]	W19
VSS[217]		VSS[317]	W27
VSS[218]		VSS[318]	W48
VSS[219]		VSS[319]	Y12
VSS[220]		VSS[320]	Y28
VSS[221]		VSS[321]	Y4
VSS[222]		VSS[322]	Y42
VSS[223]		VSS[323]	Y46
VSS[224]		VSS[324]	Y8
VSS[225]		VSS[325]	BG29
VSS[226]		VSS[326]	N24
VSS[227]		VSS[327]	A13
VSS[228]		VSS[328]	AD47
VSS[229]		VSS[329]	B43
VSS[230]		VSS[330]	BE10
VSS[231]		VSS[331]	BG41
VSS[232]		VSS[332]	G14
VSS[233]		VSS[333]	H16
VSS[234]		VSS[334]	T36
VSS[235]		VSS[335]	BG22
VSS[236]		VSS[336]	C22
VSS[237]		VSS[337]	AP13
VSS[238]		VSS[338]	M14
VSS[239]		VSS[339]	AP3
VSS[240]		VSS[340]	AP1
VSS[241]		VSS[341]	BE16
VSS[242]		VSS[342]	BC16
VSS[243]		VSS[343]	BG28
VSS[244]		VSS[344]	RJ28
VSS[245]		VSS[345]	
VSS[246]		VSS[346]	
VSS[247]		VSS[347]	
VSS[248]		VSS[348]	
VSS[249]		VSS[349]	
VSS[250]		VSS[350]	
VSS[251]		VSS[351]	
VSS[252]		VSS[352]	
VSS[253]			
VSS[254]			
VSS[255]			
VSS[256]			
VSS[257]			
VSS[258]			

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# GFX PCIE LANE REVERSAL



LCD PWM (pulse width modulated) output to adjust LCD brightness Active High ,external PD need

Controls panel digital power on/off. Active High ,external PD need

Display Port F config

Display Port E config

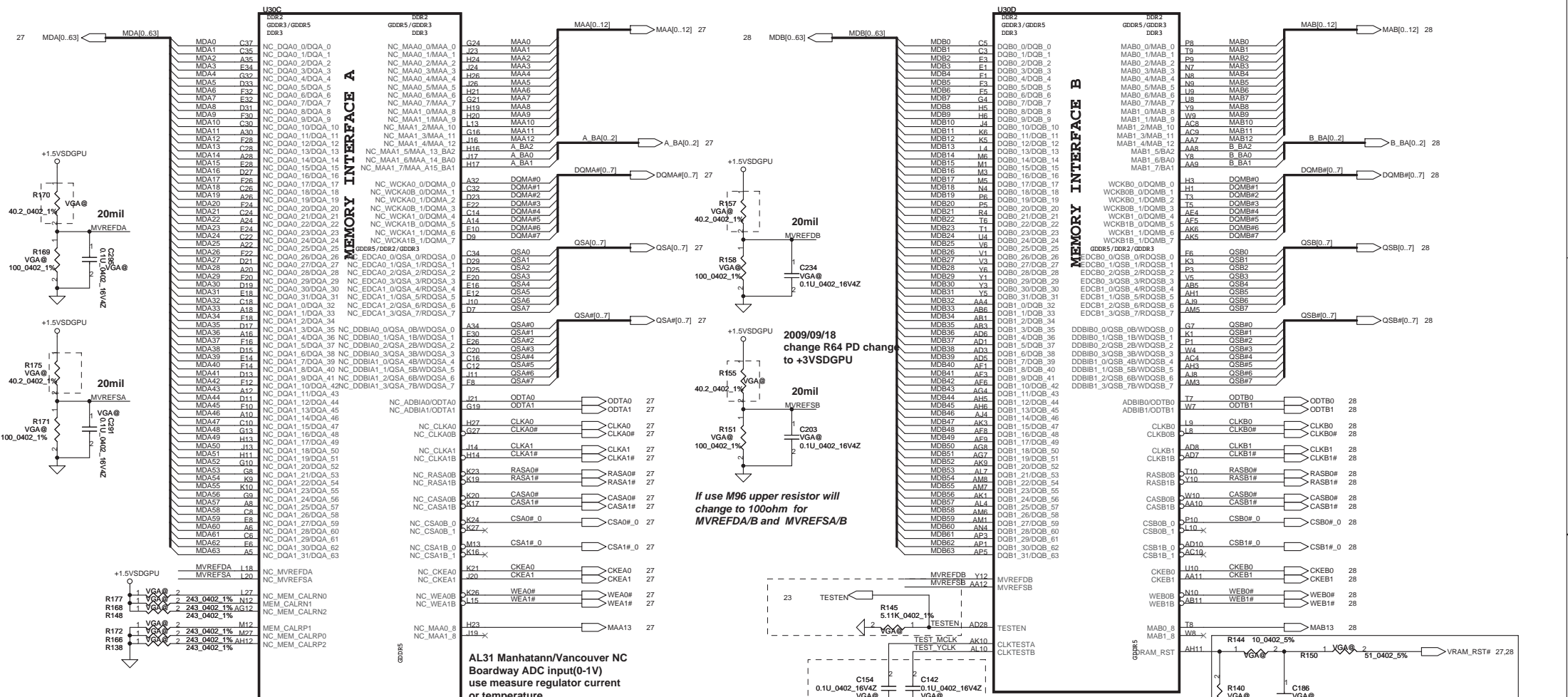
eDP  
DP3  
DP2  
DP1  
DP0

For M96, AH16 is NC  
For Boardway, Madison, Park, AH16 must connect to GND

SEYM@  
Park XT P/N : SA00003M570 ( S IC 216-0774009 A11 PARK XT S3 631P C38)  
Madison Pro P/N : SA00003M360 ( S IC 216-0772000 MADISON PRO FCBGA 0FA)  
Seymour XT P/N: SA000047H00 ( S IC 216-0809000 A11 SEYMOUR XT M2 0FH)

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				Rev	B





**MEMORY INTERFACE A**

**MEMORY INTERFACE B**

AL31 Manhattan/Vancouver NC Boardway ADC input(0-1V) use measure regulator current or temperature

AG28: VDDC\_SEN feedback path to regulator no use can CN AF28:VDDC\_SEN feedback path to regulator no use can CN

In M97, Medison and Park, AF28 is FB\_VDDC, AG28 is FB\_VDDCI, AH29 is FB\_GND, GCORE\_SEN and FB\_GND should route as differential pair Same as VDDC\_SEN and FB\_GND

If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B

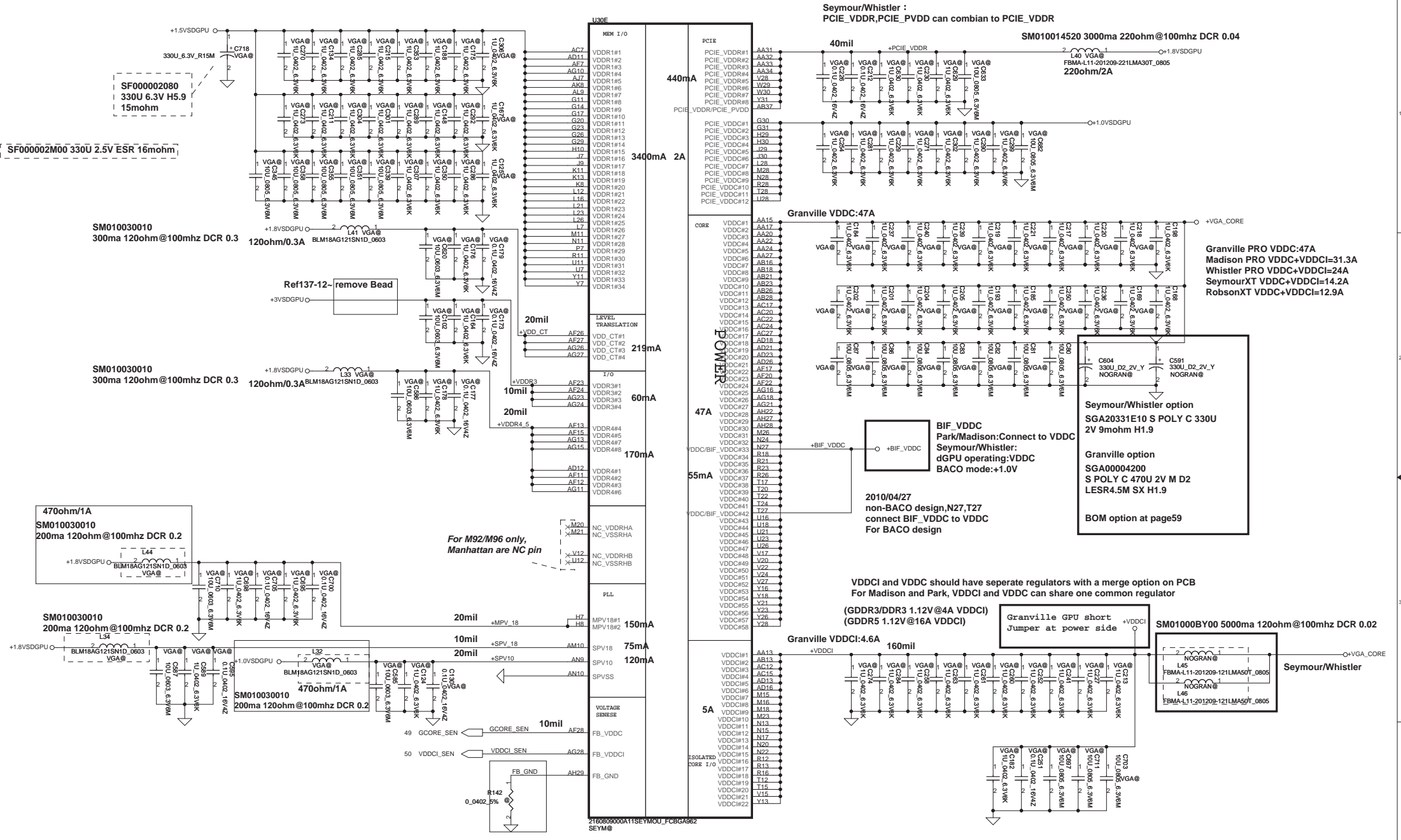
M96 use 4.7K to PD directly.

**Seymour is single channel for memory (channel B only)**

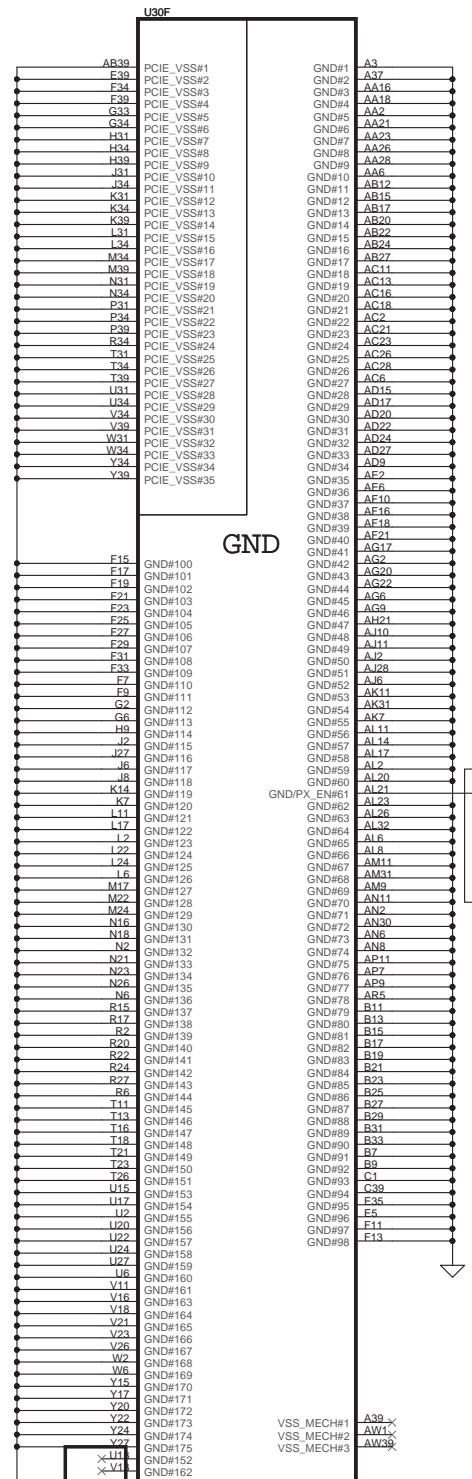
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within5mm) except Rser2

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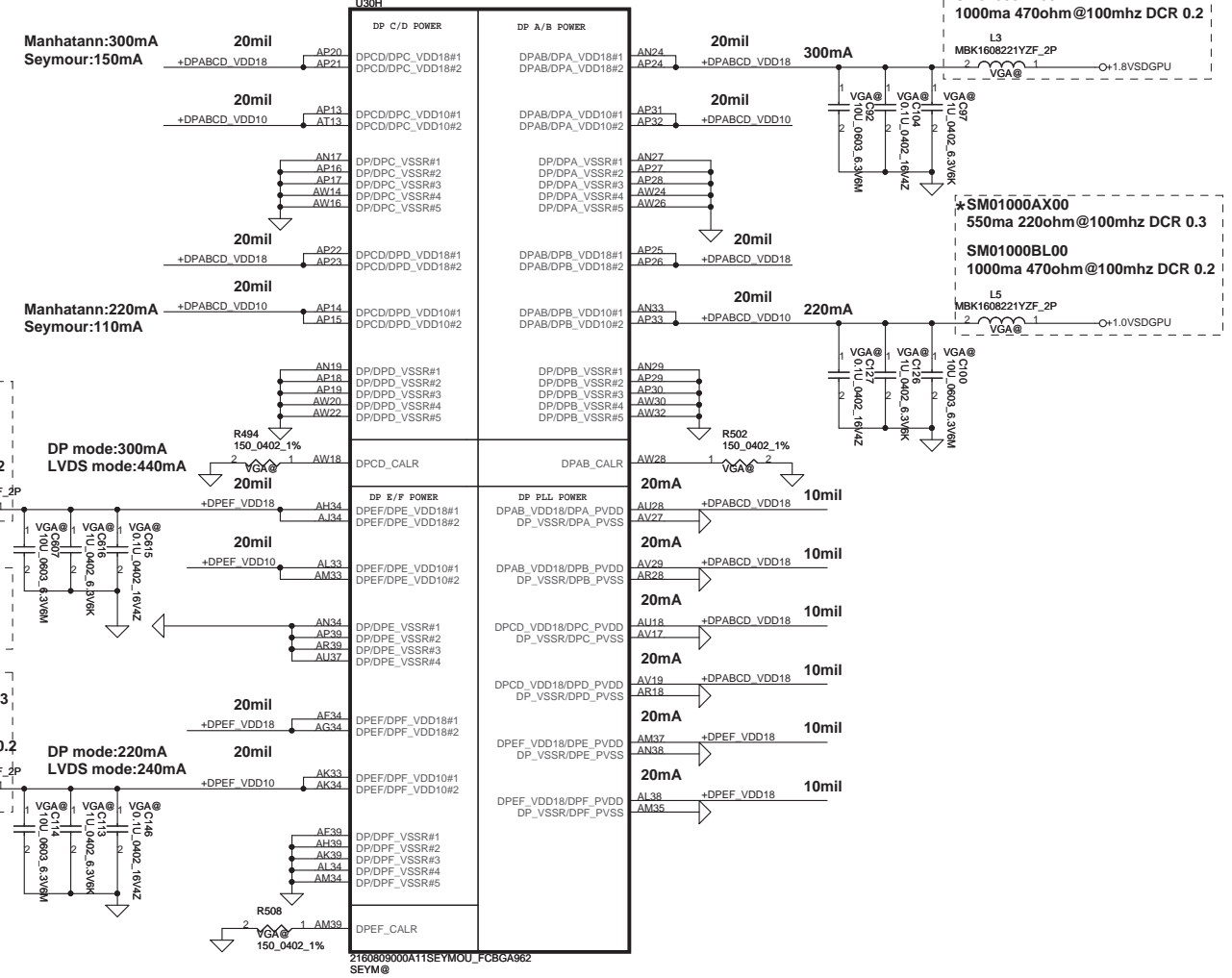


2160809000A11SEYMOU\_FCBGA962  
SEYM@  
REF137-13 update

DPA\_VDD18, DPA\_PVDD, DPB\_VDD18, DPB\_PVDD  
can combian to DPAB\_VDD18  
DPC\_VDD18, DPC\_PVDD, DPD\_VDD18, DPD\_PVDD  
can combian to DPCD\_VDD18  
(DPD\_VDD18, DPD\_PVDD not applicable on Robson/Park)  
DPE\_VDD18, DPE\_PVDD, DPF\_VDD18, DPF\_PVDD  
can combian to DPEF\_VDD18

Seymour/Whistler :  
DPA\_VDD10, DPB\_VDD10  
can combian to DPAB\_VDD10  
DPC\_VDD10, DPD\_VDD10  
can combian to DPCD\_VDD10  
DPE\_VDD10, DPF\_VDD10  
can combian to DPEF\_VDD10

DPx-VSSR, DPx\_PVSS can combian to DP\_VSSR  
(Manhattan should have individual GND)  
where x is A,B,C,D,E,F



\*SM01000AX00  
550ma 220ohm@100mhz DCR 0.3  
SM01000BL00  
1000ma 470ohm@100mhz DCR 0.2

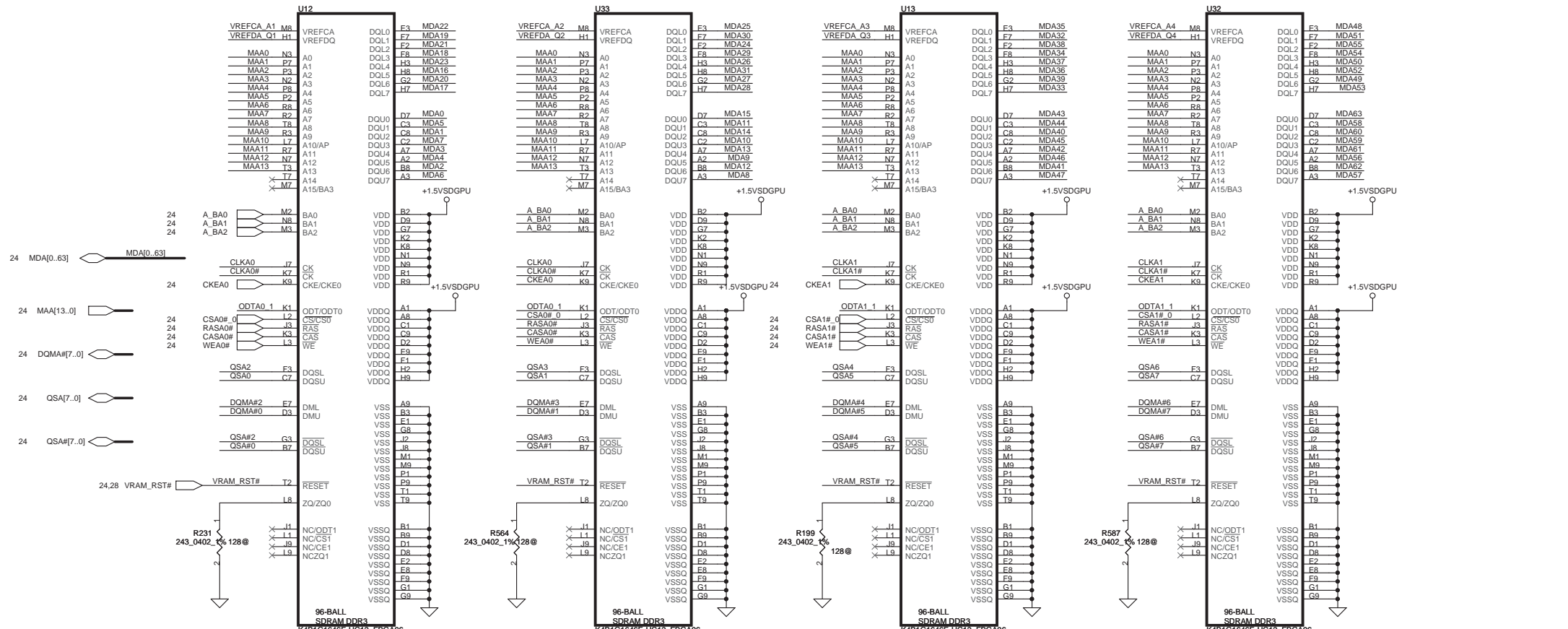
\*SM01000AX00  
550ma 220ohm@100mhz DCR 0.3  
SM01000BL00  
1000ma 470ohm@100mhz DCR 0.2

PX\_EN: SBIOS will control VGA power on/off.  
High :BACO mode enable  
LOWLBACO disable

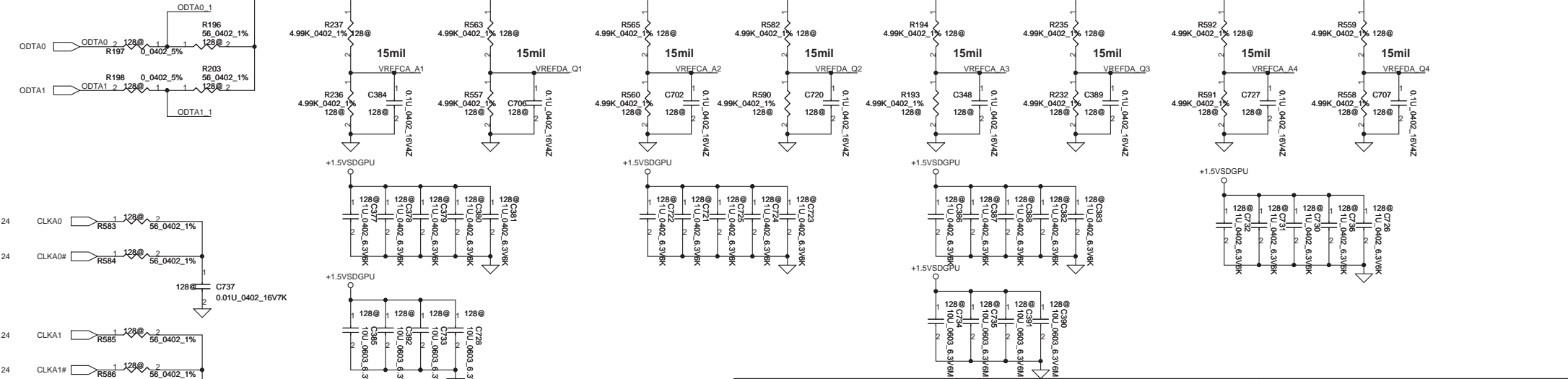
Park/Madison :AL21:left NC  
  
Seymour/Whistler:  
AL21:PX\_EN  
use to control discreate GPU regulators  
for power express BACO mode  
Support BACO:  
output High3.3V:turn off regulators (BACO mode on)  
output Low0V:turn on regulators (BACO mode off)  
need PD resistor  
No support BACO:  
left NC

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				Schematic, MB A6911	
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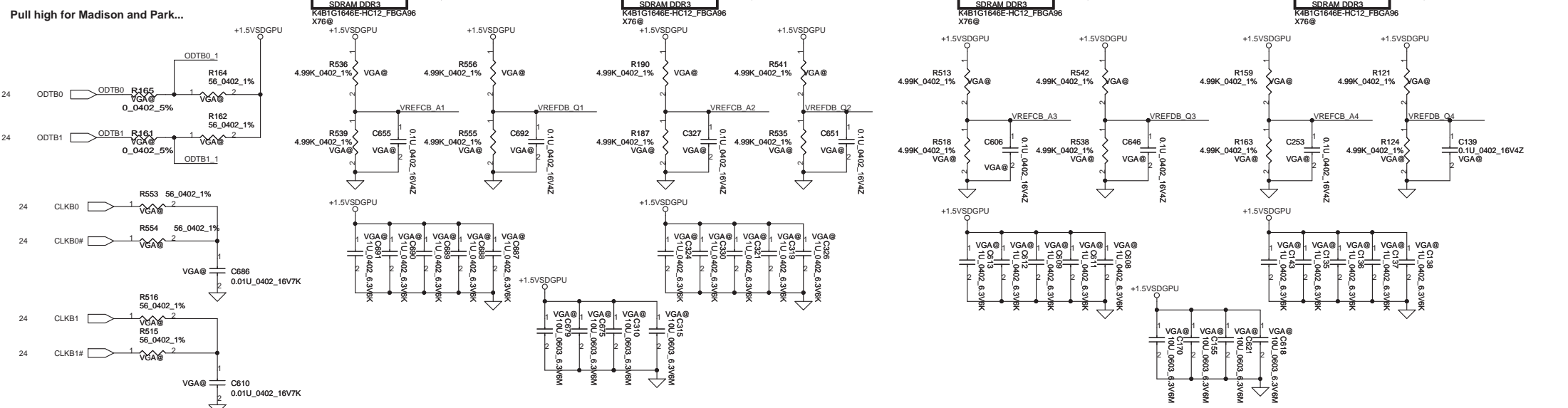
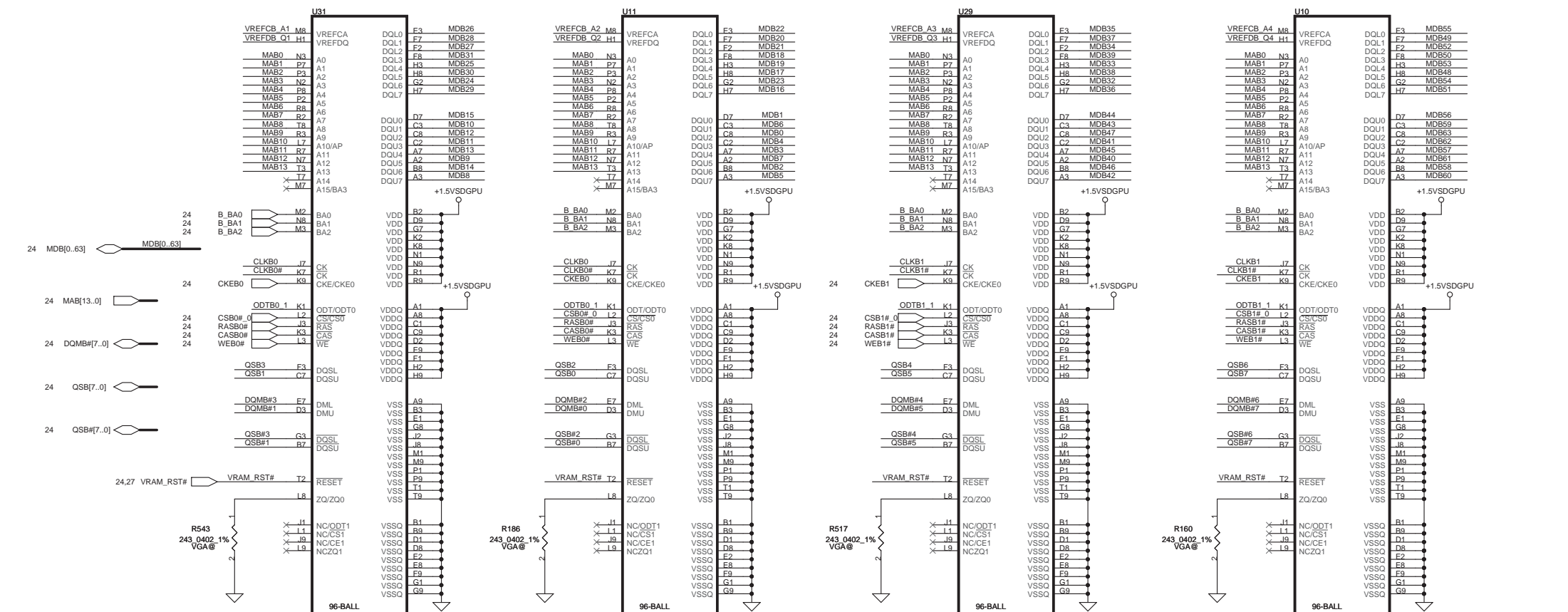


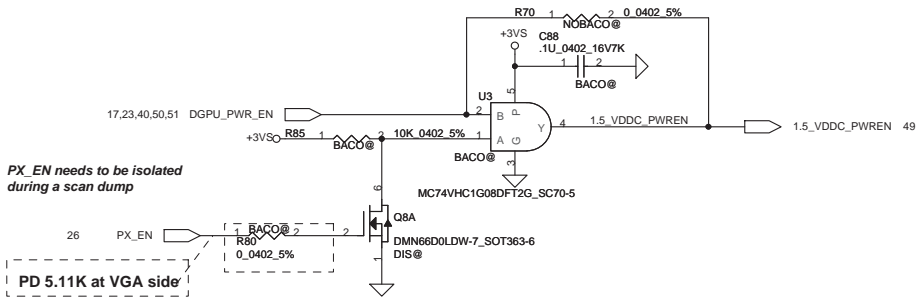


Pull high for Madison and Park...



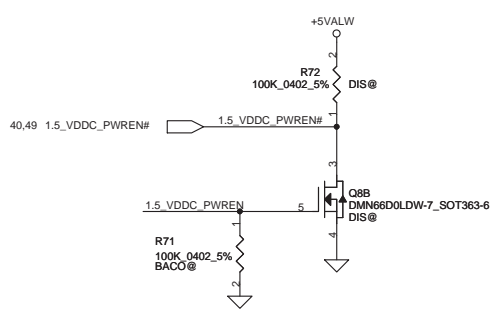
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/12	Title	
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				Date:	Tuesday, November 09, 2010
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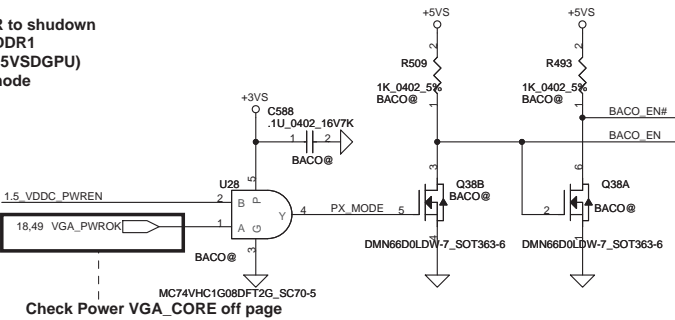
PX\_EN = 1, For BACO Mode  
 PX\_EN = 0, For Normal Mode

PX\_EN:  
 Connect to PWR to shutdown  
 VDDC/VDDCI/VDDR1  
 (VGA\_CORE,+1.5VSDGPU)  
 High in BACO mode



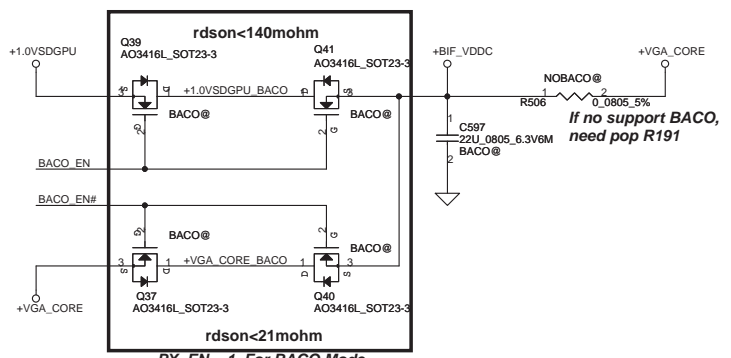
BACO\_EN/BACO\_EN#:  
 0: BACO Mode->BACO\_EN High->  
 BIF\_VDDC=>+1.0VSDGPU(N-MOS),VGA\_CORE(P-MOS)  
 1: Normal mode->BACO\_EN# High->  
 BIF\_VDDC=>+VGA\_CORE(N-MOS),VGA\_CORE(N-MOS)

VGA Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
BACO_EN#	1	0
BACO_EN	0	1
+3VSDGPU	ON	ON
+1.8VSDGPU	ON	ON
+1.0VSDGPU	ON	ON
+VGA_CORE	ON	OFF
+1.5VSDGPU	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSDGPU



BACO\_EN# = 1 (BACO mode)  
 BACO\_EN# = 0 (Normal mode)  
 BACO\_EN = 0 (BACO mode)  
 BACO\_EN = 1 (Normal mode)

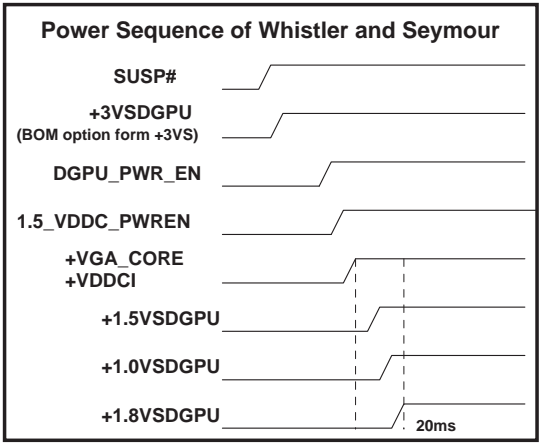
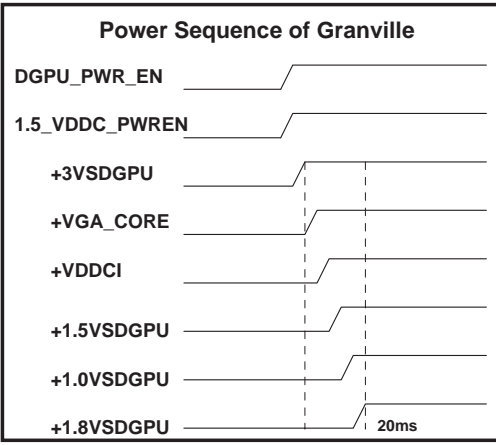
VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
+3VSDGPU	DGPU_PWR_EN	SUSP#
+1.8VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+1.0VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+VDDCI	DGPU_PWR_EN	Combine with +VGA_CORE
+VGA_CORE	DGPU_PWR_EN	1.5_VDDC_PWREN
+1.5VSDGPU	DGPU_PWR_EN	1.5_VDDC_PWREN



rdson < 140 mohm  
 Q39 AO3416L\_SOT23-3  
 rdson < 21 mohm  
 Q41 AO3416L\_SOT23-3  
 Q37 AO3416L\_SOT23-3  
 Q40 AO3416L\_SOT23-3  
 PX\_EN = 1, For BACO Mode  
 BACO\_EN# = 0  
 BACO\_EN# = 1(5V) => BIF\_VDDC = +1.0VSDGPU  
 PX\_EN = 0, For Normal Mode  
 BACO\_EN# = 1(5V) => BIF\_VDDC = VGA\_CORE  
 BACO\_EN# = 0

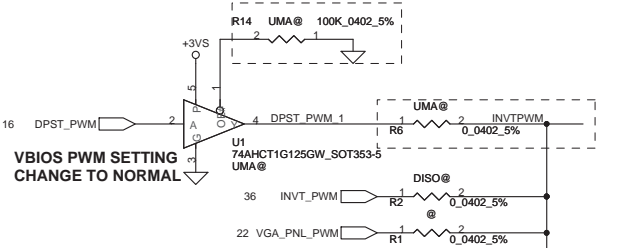
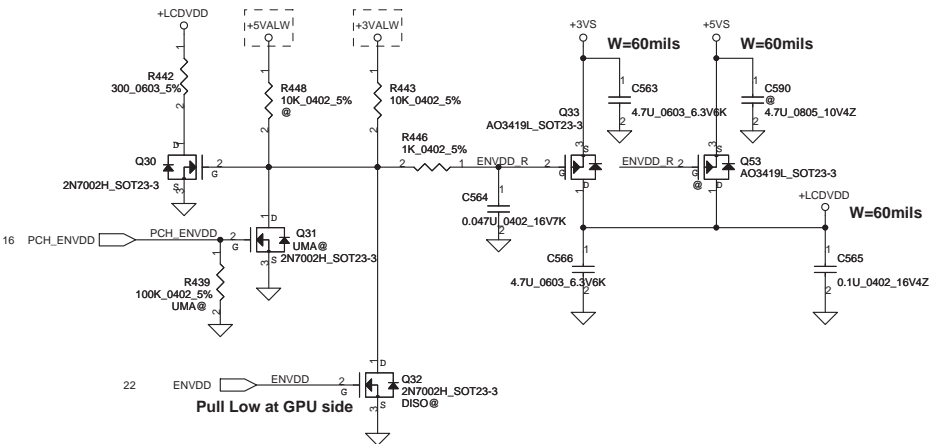
For the MOSFETS on the path of delivering  
 PCIE\_VDDC(+1.0VSDGPU) to  
 BIF\_VDDC Rds(on) of 140 mOhms or less is required.

For the MOSFETS on the path of delivering VGA\_CORE to  
 BIF\_VDDC, Rds(on) of 21 mOhms or less is required.



100505 change to +3VALW  
101029 add +5VALW

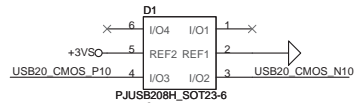
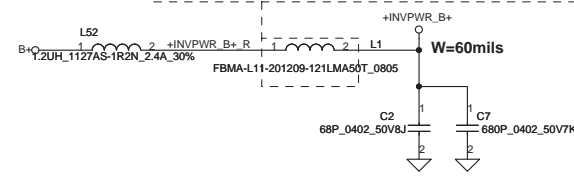
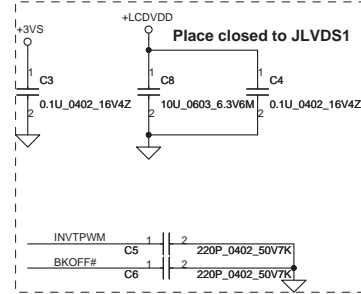
### LCD POWER CIRCUIT



UMA/DIS LVDS/eDP Mapping table				
UMA	eDP	LVDS	DIS	Panel Conn.
PCH_TXOUT0+		VGA_TXOUT0+		TXOUT0+
PCH_TXOUT0-		VGA_TXOUT0-		TXOUT0-
PCH_TXOUT1+	EDP_TXP1	VGA_TXOUT1+		TXOUT1+
PCH_TXOUT1-	EDP_TXN1	VGA_TXOUT1-		TXOUT1-
PCH_TXOUT2+	EDP_TXP0	VGA_TXOUT2+		TXOUT2+
PCH_TXOUT2-	EDP_TXN0	VGA_TXOUT2-		TXOUT2-
PCH_TXCLK+		VGA_TXCLK+		TXCLK+
PCH_TXCLK-		VGA_TXCLK-		TXCLK-
PCH_TZOUT0+		VGA_TZOUT0+		TZOUT0+
PCH_TZOUT0-		VGA_TZOUT0-		TZOUT0-
PCH_TZOUT1+		VGA_TZOUT1+		TZOUT1+
PCH_TZOUT1-		VGA_TZOUT1-		TZOUT1-
PCH_TZOUT2+		VGA_TZOUT2+		TZOUT2+
PCH_TZOUT2-		VGA_TZOUT2-		TZOUT2-
PCH_TZCLK+		VGA_TZCLK+		TZCLK+
PCH_TZCLK-		VGA_TZCLK-		TZCLK-
PCH_LCD_CLK+	EDP_AUXP	VGA_LCD_CLK	AUXP	I2CC_SCL
PCH_LCD_DATA+	EDP_AUXN	VGA_LCD_DATA	AUXN	I2CC_SDA

SM010014520 3000ma 220ohm@100mhz DCR 0.04

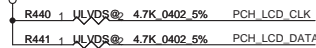
SM01000BY00 5000ma 120ohm@100mhz DCR 0.02



### UMA ONLY/Muxless

16 PCH_TXOUT0+	PCH_TXOUT0+	R452	1	ULVDS@	0.0402_5%	TXOUT0+
16 PCH_TXOUT0-	PCH_TXOUT0-	R450	1	ULVDS@	0.0402_5%	TXOUT0-
16 PCH_TXOUT1+	PCH_TXOUT1+	R455	1	ULVDS@	0.0402_5%	TXOUT1+
16 PCH_TXOUT1-	PCH_TXOUT1-	R453	1	ULVDS@	0.0402_5%	TXOUT1-
16 PCH_TXOUT2+	PCH_TXOUT2+	R456	1	ULVDS@	0.0402_5%	TXOUT2+
16 PCH_TXOUT2-	PCH_TXOUT2-	R454	1	ULVDS@	0.0402_5%	TXOUT2-
16 PCH_TXCLK+	PCH_TXCLK+	R458	1	ULVDS@	0.0402_5%	TXCLK+
16 PCH_TXCLK-	PCH_TXCLK-	R457	1	ULVDS@	0.0402_5%	TXCLK-
16 PCH_TZOUT0+	PCH_TZOUT0+	R460	1	ULVDS@	0.0402_5%	TZOUT0+
16 PCH_TZOUT0-	PCH_TZOUT0-	R459	1	ULVDS@	0.0402_5%	TZOUT0-
16 PCH_TZOUT1+	PCH_TZOUT1+	R462	1	ULVDS@	0.0402_5%	TZOUT1+
16 PCH_TZOUT1-	PCH_TZOUT1-	R461	1	ULVDS@	0.0402_5%	TZOUT1-
16 PCH_TZOUT2+	PCH_TZOUT2+	R465	1	ULVDS@	0.0402_5%	TZOUT2+
16 PCH_TZOUT2-	PCH_TZOUT2-	R463	1	ULVDS@	0.0402_5%	TZOUT2-
16 PCH_TZCLK+	PCH_TZCLK+	R467	1	ULVDS@	0.0402_5%	TZCLK+
16 PCH_TZCLK-	PCH_TZCLK-	R466	1	ULVDS@	0.0402_5%	TZCLK-
16 PCH_LCD_CLK	PCH_LCD_CLK	R444	1	ULVDS@	0.0402_5%	I2CC_SCL
16 PCH_LCD_DATA	PCH_LCD_DATA	R445	1	ULVDS@	0.0402_5%	I2CC_SDA

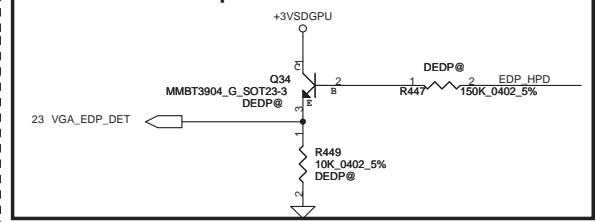
5/4 PCH\_LCD\_CLK & PCH\_LCD\_DATA  
Pull high 2.2K change to 4.7K



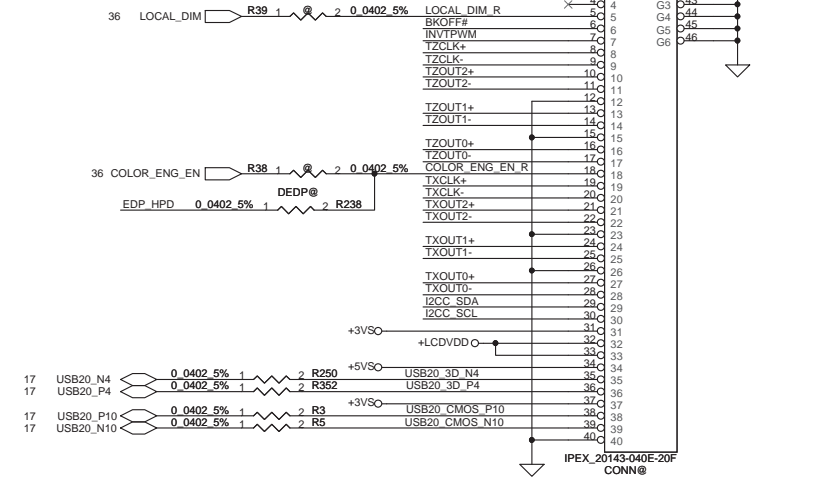
### Discrete ONLY

22 VGA_TXOUT0+	VGA_TXOUT0+	R13	1	ULVDS@	0.0402_5%	TXOUT0+
22 VGA_TXOUT0-	VGA_TXOUT0-	R12	1	ULVDS@	0.0402_5%	TXOUT0-
22 VGA_TXOUT1+	VGA_TXOUT1+	R23	1	ULVDS@	0.0402_5%	TXOUT1+
22 VGA_TXOUT1-	VGA_TXOUT1-	R17	1	ULVDS@	0.0402_5%	TXOUT1-
22 VGA_TXOUT2+	VGA_TXOUT2+	R24	1	ULVDS@	0.0402_5%	TXOUT2+
22 VGA_TXOUT2-	VGA_TXOUT2-	R22	1	ULVDS@	0.0402_5%	TXOUT2-
22 VGA_TXCLK+	VGA_TXCLK+	R26	1	ULVDS@	0.0402_5%	TXCLK+
22 VGA_TXCLK-	VGA_TXCLK-	R25	1	ULVDS@	0.0402_5%	TXCLK-
22 VGA_TZOUT0+	VGA_TZOUT0+	R28	1	ULVDS@	0.0402_5%	TZOUT0+
22 VGA_TZOUT0-	VGA_TZOUT0-	R27	1	ULVDS@	0.0402_5%	TZOUT0-
22 VGA_TZOUT1+	VGA_TZOUT1+	R30	1	ULVDS@	0.0402_5%	TZOUT1+
22 VGA_TZOUT1-	VGA_TZOUT1-	R29	1	ULVDS@	0.0402_5%	TZOUT1-
22 VGA_TZOUT2+	VGA_TZOUT2+	R32	1	ULVDS@	0.0402_5%	TZOUT2+
22 VGA_TZOUT2-	VGA_TZOUT2-	R31	1	ULVDS@	0.0402_5%	TZOUT2-
22 VGA_TZCLK+	VGA_TZCLK+	R34	1	ULVDS@	0.0402_5%	TZCLK+
22 VGA_TZCLK-	VGA_TZCLK-	R33	1	ULVDS@	0.0402_5%	TZCLK-
23 VGA_LCD_CLK	VGA_LCD_CLK	R9	1	ULVDS@	0.0402_5%	I2CC_SCL
23 VGA_LCD_DATA	VGA_LCD_DATA	R7	1	ULVDS@	0.0402_5%	I2CC_SDA

### BOM option for Discrete eDP

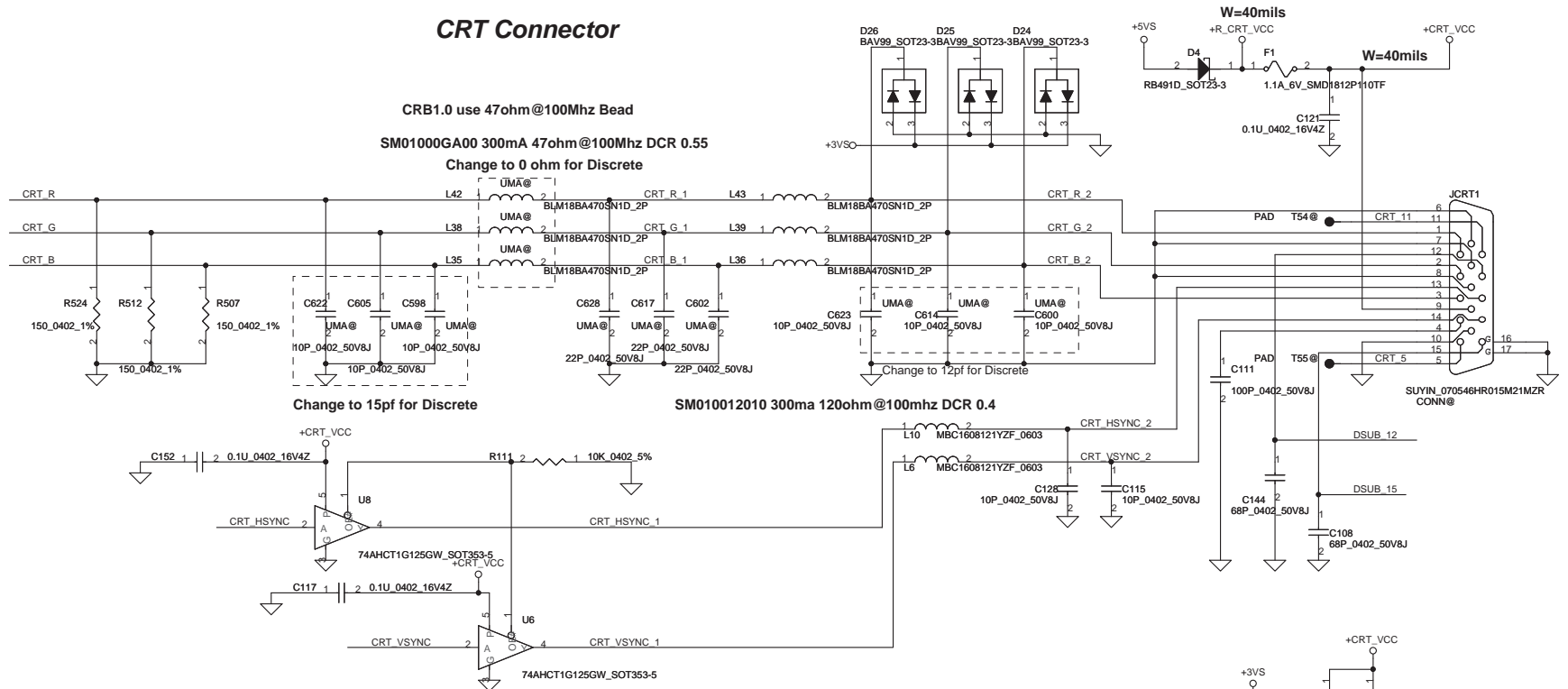


### LED PANEL Conn.



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# CRT Connector



CRB1.0 use 47ohm@100Mhz Bead

SM01000GA00 300mA 47ohm@100Mhz DCR 0.55

Change to 0 ohm for Discrete

Change to 15pf for Discrete

SM010012010 300ma 120ohm@100mhz DCR 0.4

Change to 12pf for Discrete

UMA only/Muxless

16	PCH_CRT_R	PCH CRT R	R529	UMA	1	0.0402 5%	CRT R
16	PCH_CRT_G	PCH CRT G	R519	UMA	1	0.0402 5%	CRT G
16	PCH_CRT_B	PCH CRT B	R511	UMA	1	0.0402 5%	CRT B
16	PCH_CRT_HSYNC	PCH CRT HSYNC	R137	UMA	1	33.0402 5%	CRT HSYNC
16	PCH_CRT_VSYNC	PCH CRT VSYNC	R110	UMA	1	33.0402 5%	CRT VSYNC
16	PCH_CRT_CLK	PCH CRT CLK	R102	UMA	1	0.0402 5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH CRT DATA	R89	UMA	1	0.0402 5%	CRT_DDC_DATA

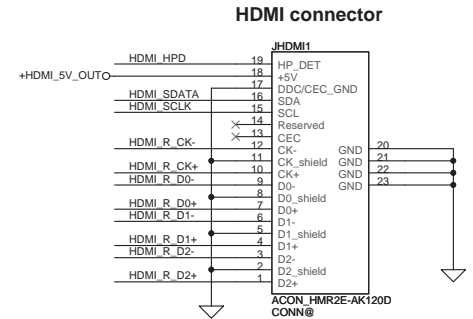
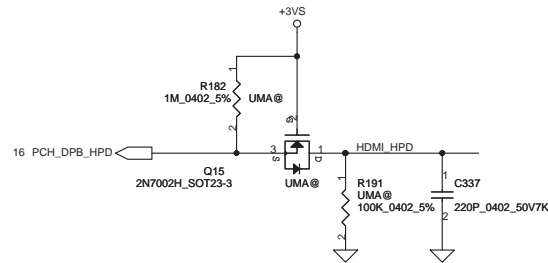
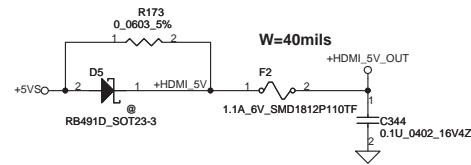
PCH DDC PU 2.2K on Page 17

Discrete only

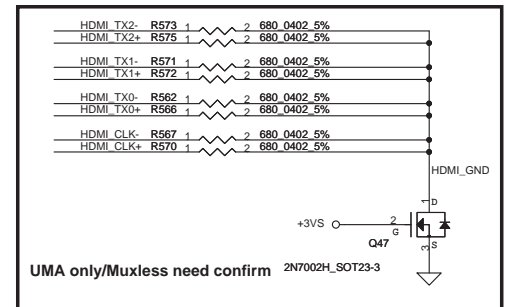
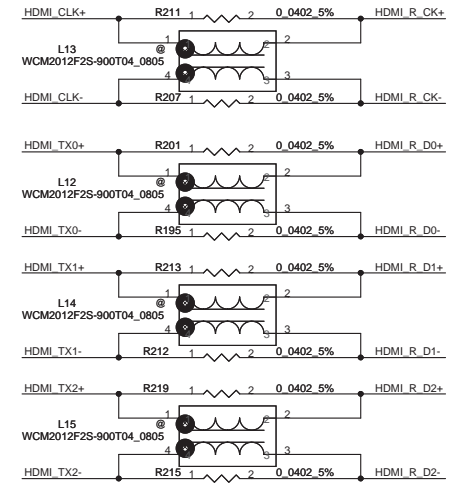
23	VGA_CRT_R	VGA CRT R	R527	RISOR	1	0.0402 5%	CRT R
23	VGA_CRT_G	VGA CRT G	R514	RISOR	1	0.0402 5%	CRT G
23	VGA_CRT_B	VGA CRT B	R510	RISOR	1	0.0402 5%	CRT B
23	VGA_CRT_HSYNC	VGA CRT HSYNC	R131	RISOR	1	0.0402 5%	CRT HSYNC
23	VGA_CRT_VSYNC	VGA CRT VSYNC	R107	RISOR	1	0.0402 5%	CRT VSYNC
23	VGA_DDC_CLK	VGA DDC CLK	R98	RISOR	1	0.0402 5%	CRT_DDC_CLK
23	VGA_DDC_DATA	VGA DDC DATA	R86	RISOR	1	0.0402 5%	CRT_DDC_DATA

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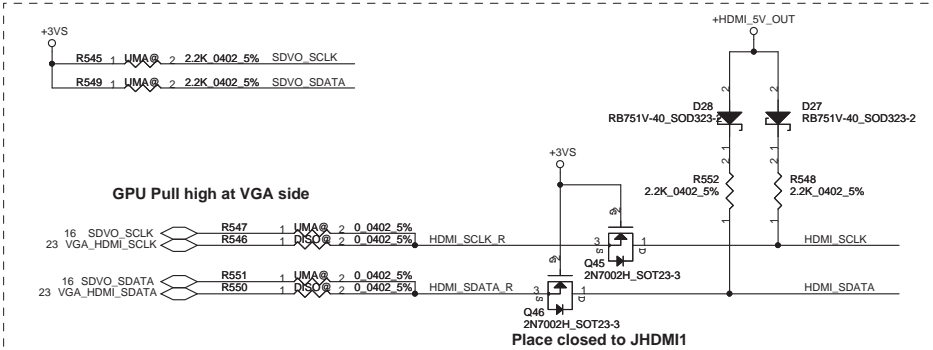
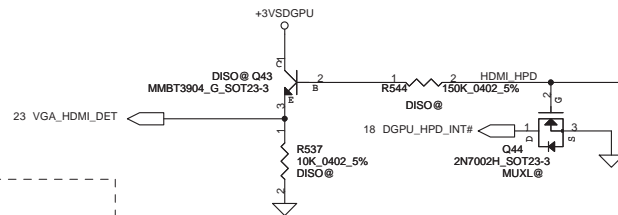


SM070001310 400ma 90ohm@100mhz DCR 0.3



UMA/Muxless			
16 PCH_DPB_N0	C364	UMA@ 2	1 .1U 0402 16V7K HDMI TX2-
16 PCH_DPB_P0	C368	UMA@ 2	1 .1U 0402 16V7K HDMI TX2+
16 PCH_DPB_N1	C357	UMA@ 2	1 .1U 0402 16V7K HDMI TX1-
16 PCH_DPB_P1	C359	UMA@ 2	1 .1U 0402 16V7K HDMI TX1+
16 PCH_DPB_N2	C347	UMA@ 2	1 .1U 0402 16V7K HDMI TX0-
16 PCH_DPB_P2	C349	UMA@ 2	1 .1U 0402 16V7K HDMI TX0+
16 PCH_DPB_N3	C352	UMA@ 2	1 .1U 0402 16V7K HDMI CLK-
16 PCH_DPB_P3	C356	UMA@ 2	1 .1U 0402 16V7K HDMI CLK+

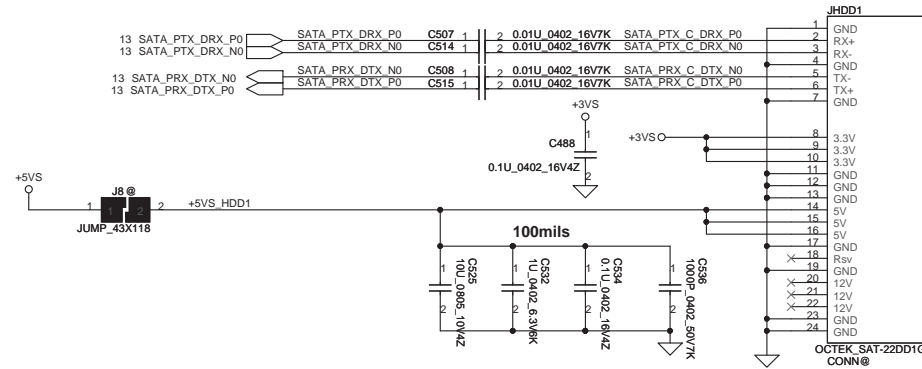
DIS Only			
23 VGA_HDMI_TXD2-	C716	DISO@ 2	1 .1U 0402 16V7K HDMI TX2-
23 VGA_HDMI_TXD2+	C717	DISO@ 2	1 .1U 0402 16V7K HDMI TX2+
23 VGA_HDMI_TXD1-	C714	DISO@ 2	1 .1U 0402 16V7K HDMI TX1-
23 VGA_HDMI_TXD1+	C715	DISO@ 2	1 .1U 0402 16V7K HDMI TX1+
23 VGA_HDMI_TXD0-	C704	DISO@ 2	1 .1U 0402 16V7K HDMI TX0-
23 VGA_HDMI_TXD0+	C709	DISO@ 2	1 .1U 0402 16V7K HDMI TX0+
23 VGA_HDMI_TXC-	C712	DISO@ 2	1 .1U 0402 16V7K HDMI CLK-
23 VGA_HDMI_TXC+	C713	DISO@ 2	1 .1U 0402 16V7K HDMI CLK+



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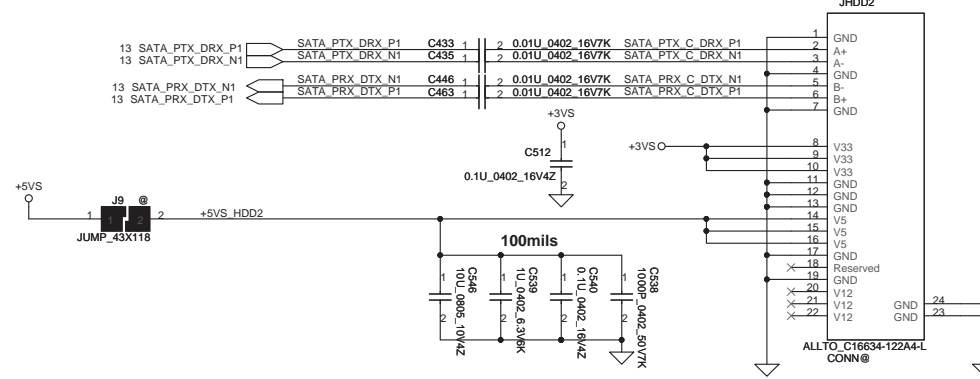
### SATA HDD1 Conn.

CL 2.9 mm

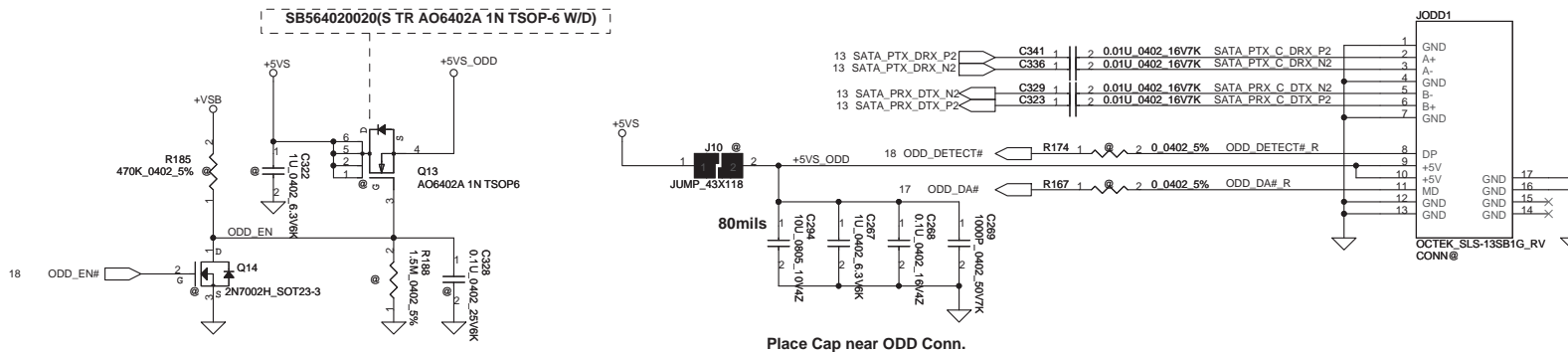


### SATA HDD2 Conn.

CL 4.4 mm

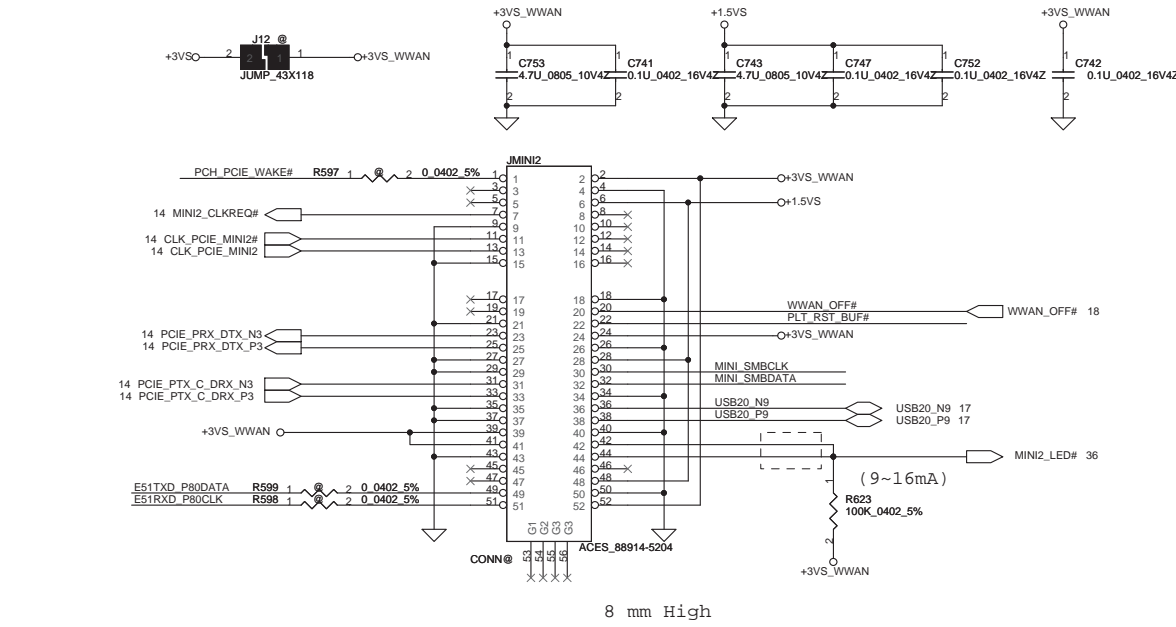
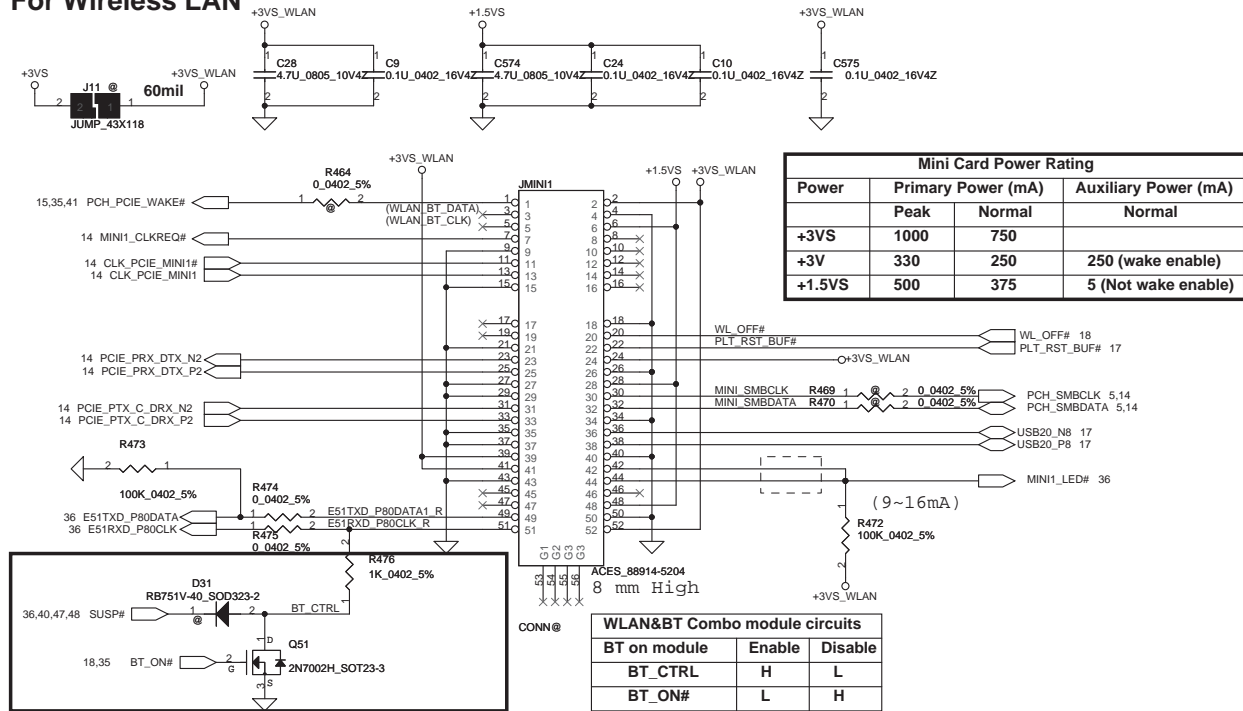


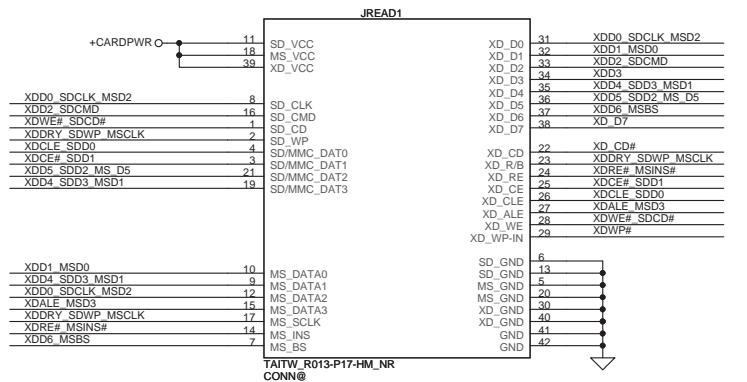
### SATA ODD Conn.



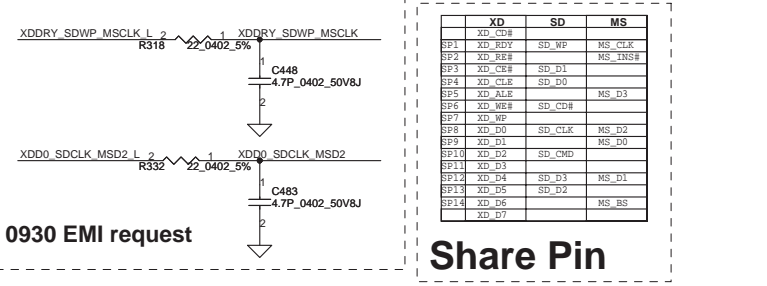
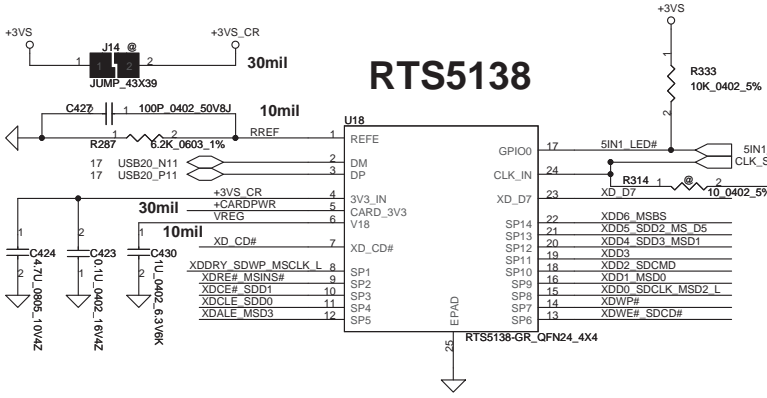
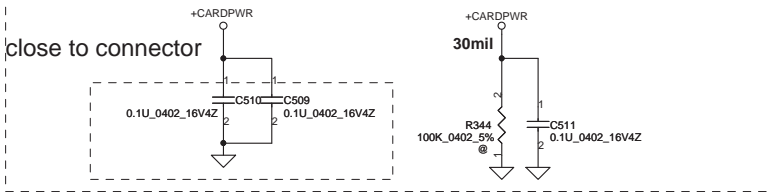
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/12	Title
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				4019A9
				Date: Tuesday, November 09, 2010
				Sheet 33 of 60

# For Wireless LAN





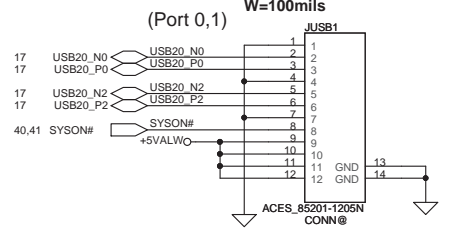
close to connector



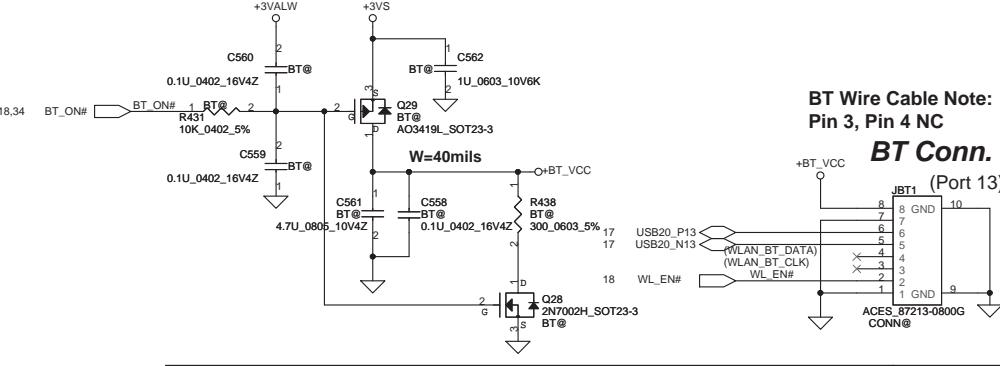
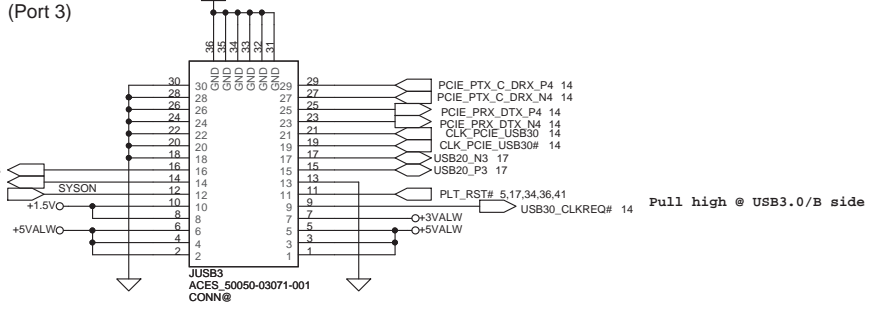
0930 EMI request

Share Pin

### LS-6911P USB/B Conn. (USB2.0 SKU)

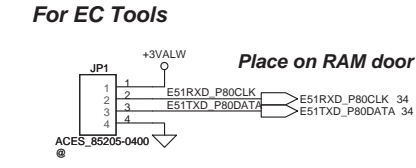
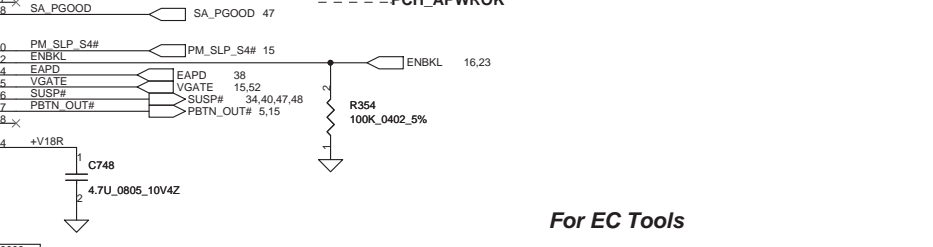
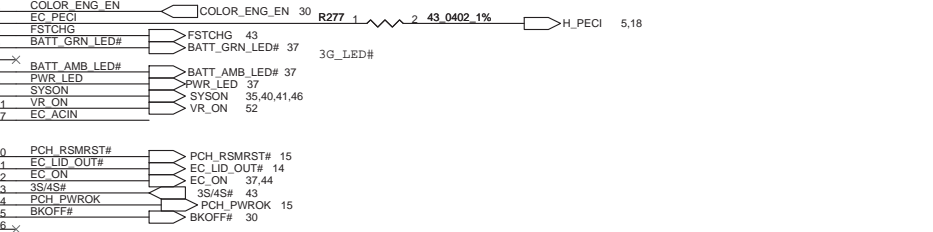
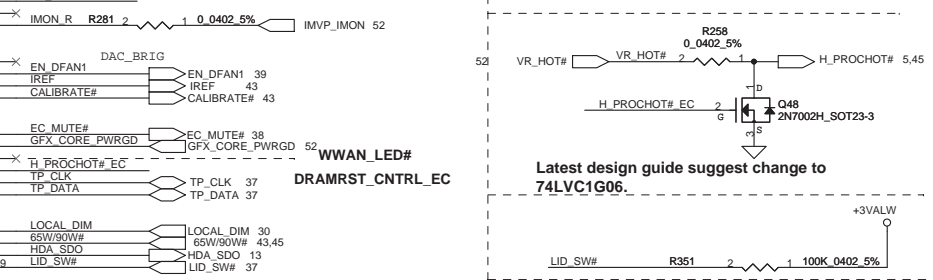
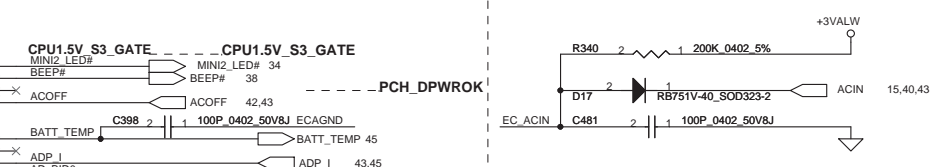
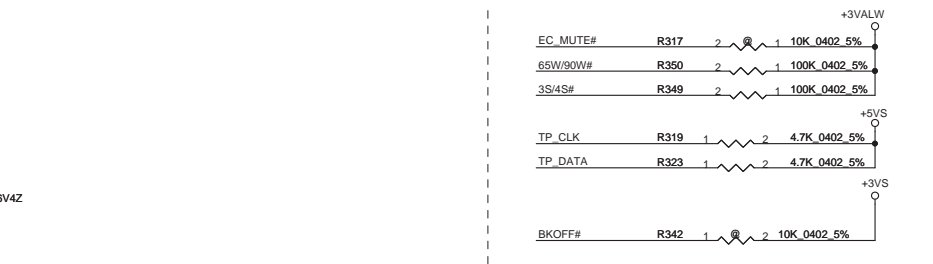
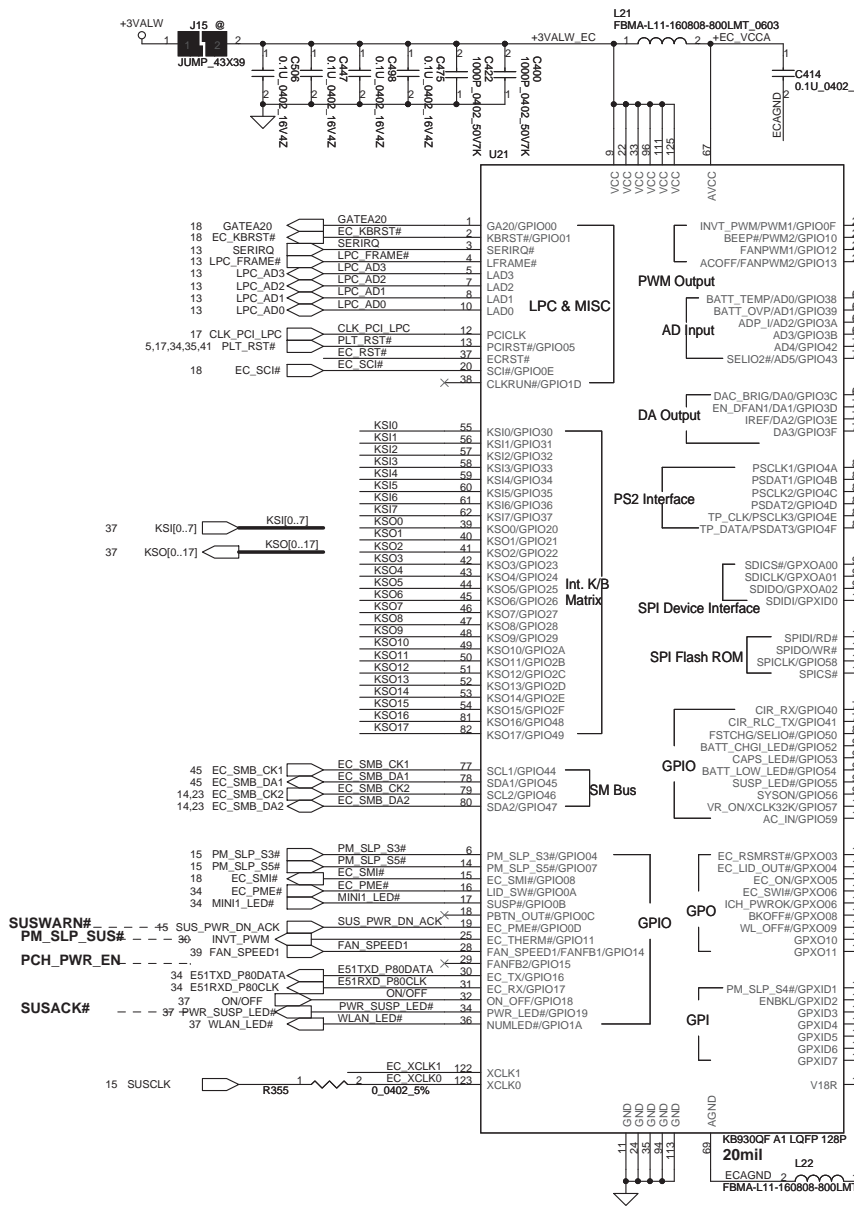
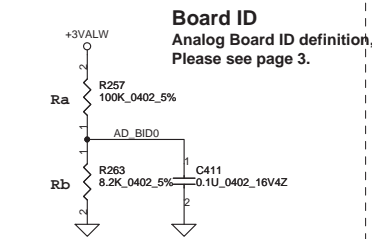
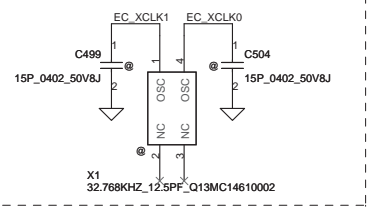
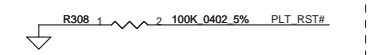
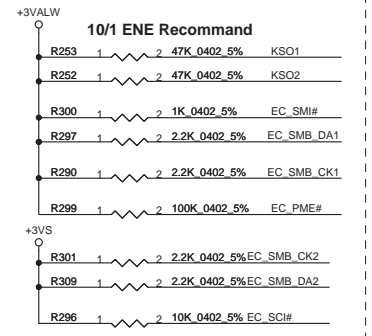
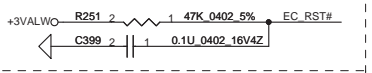
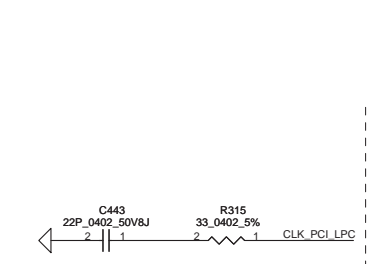


### USB/B USB3.0 Conn.(USB3.0 SKU)



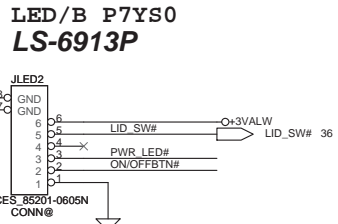
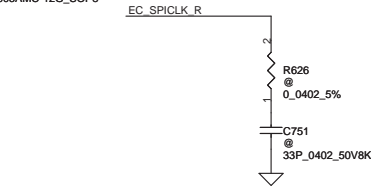
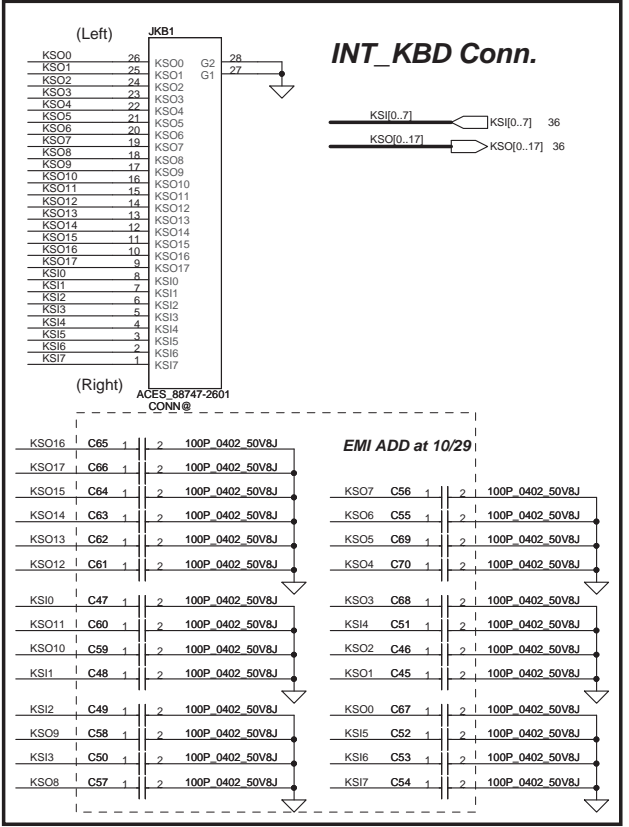
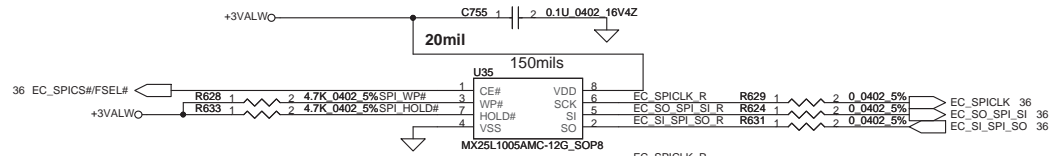
BT Wire Cable Note: Pin 3, Pin 4 NC

BT Conn. (Port 13)

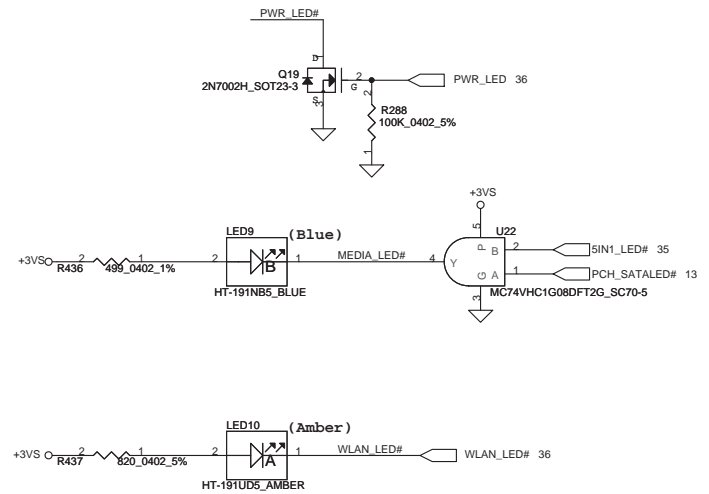
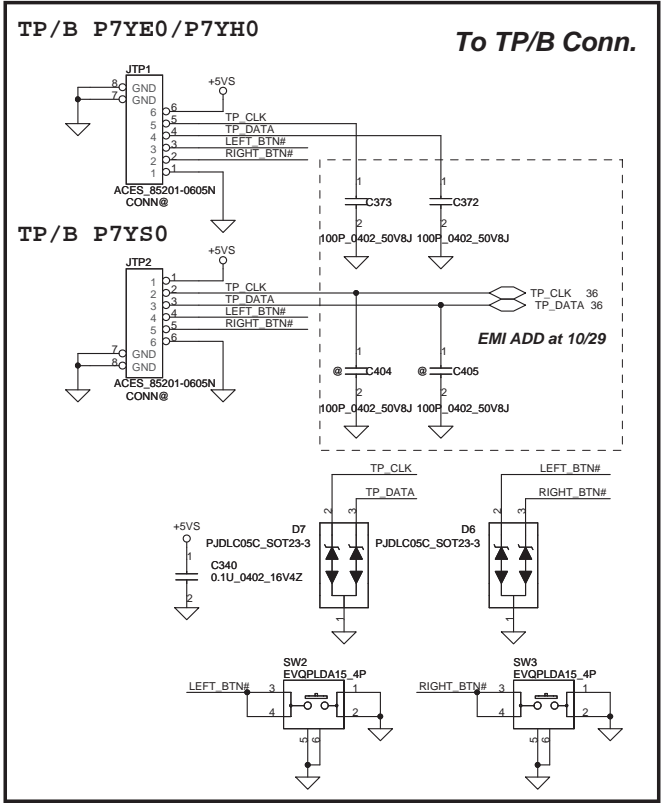
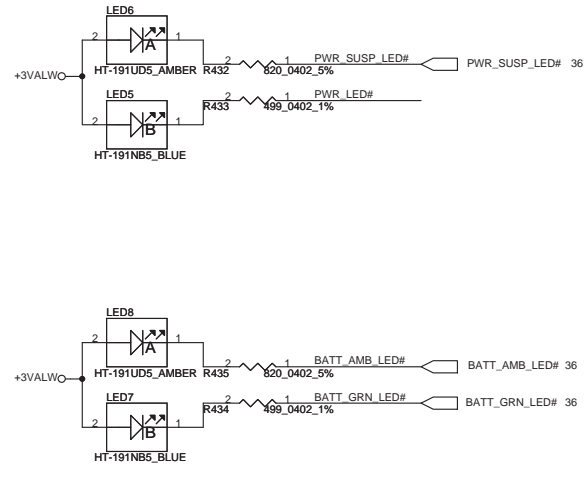
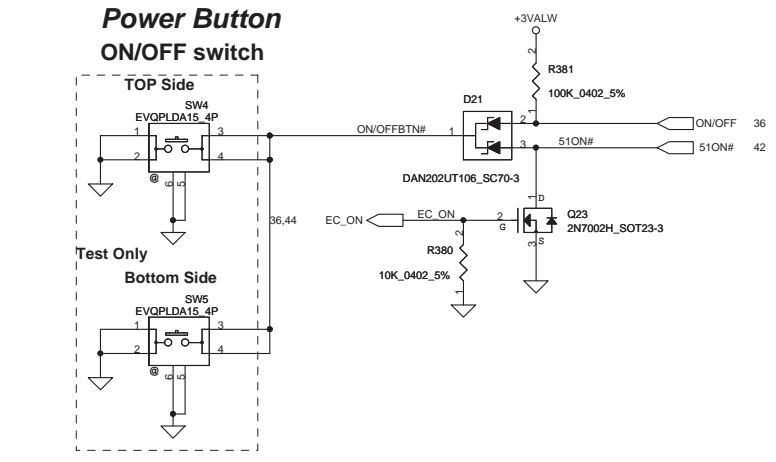


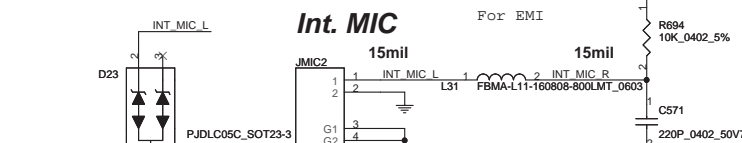
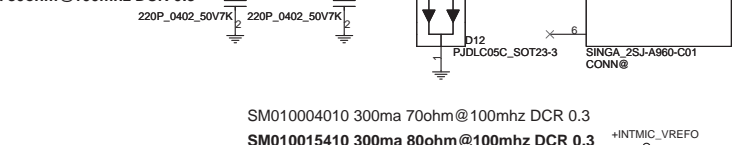
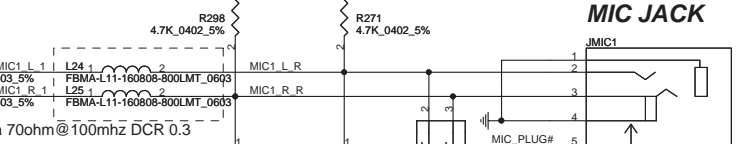
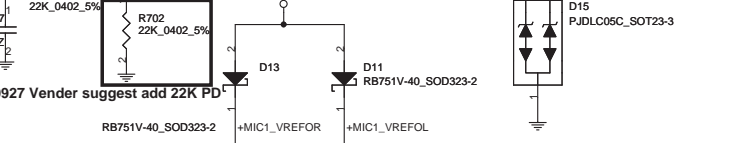
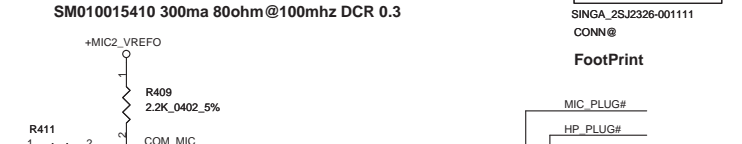
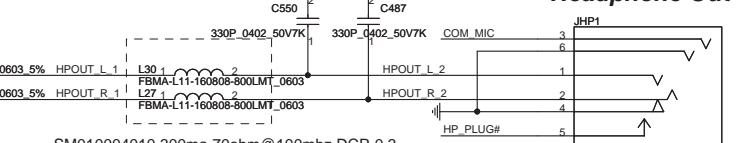
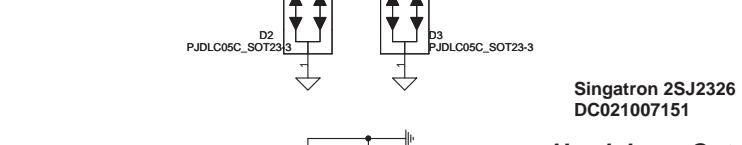
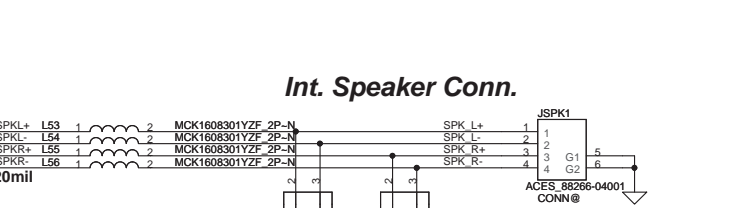
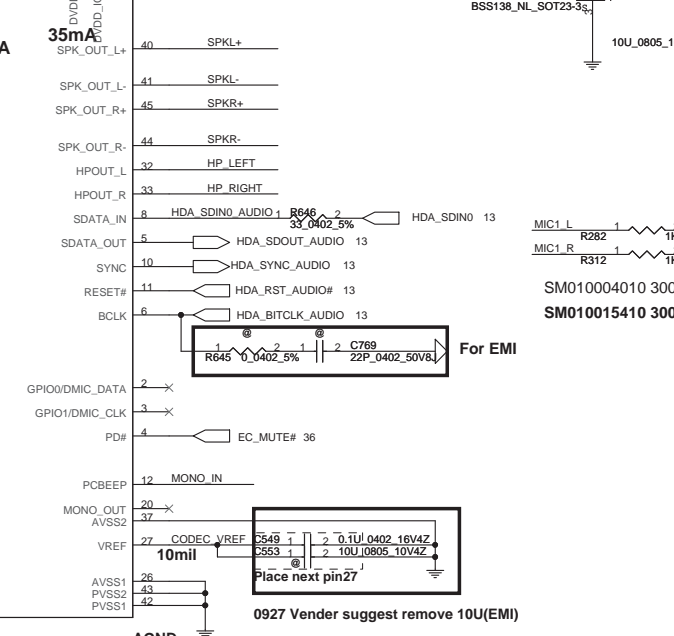
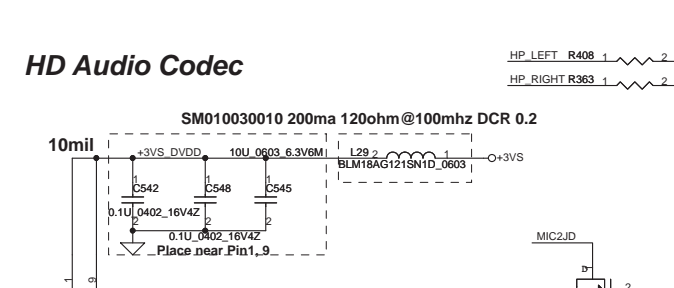
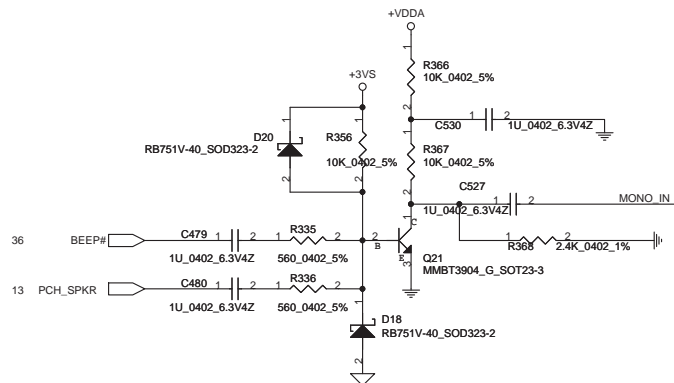
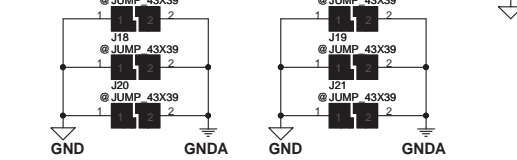
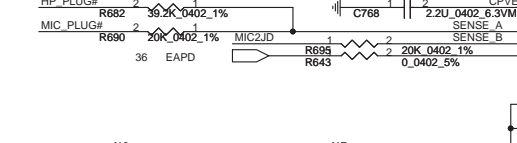
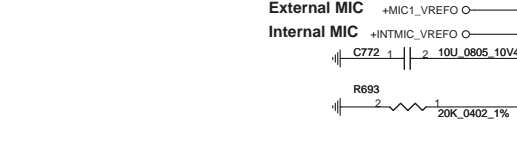
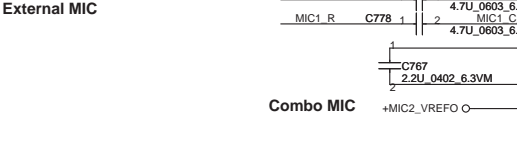
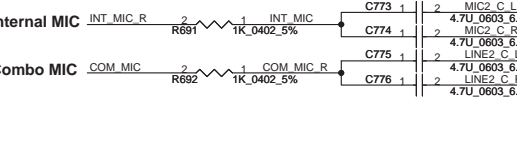
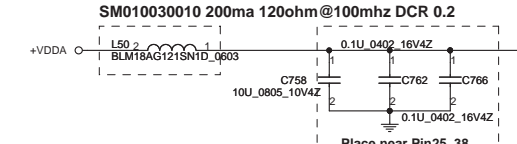
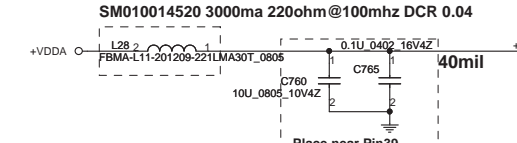
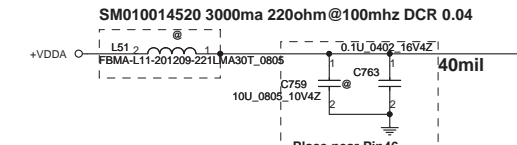
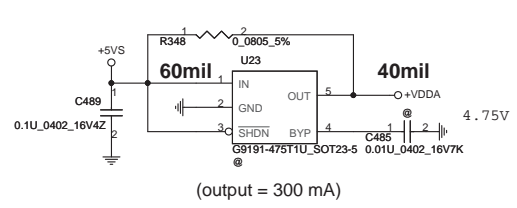
Security Classification	Compal Secret Data		Title
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Date			Tuesday, November 09, 2010
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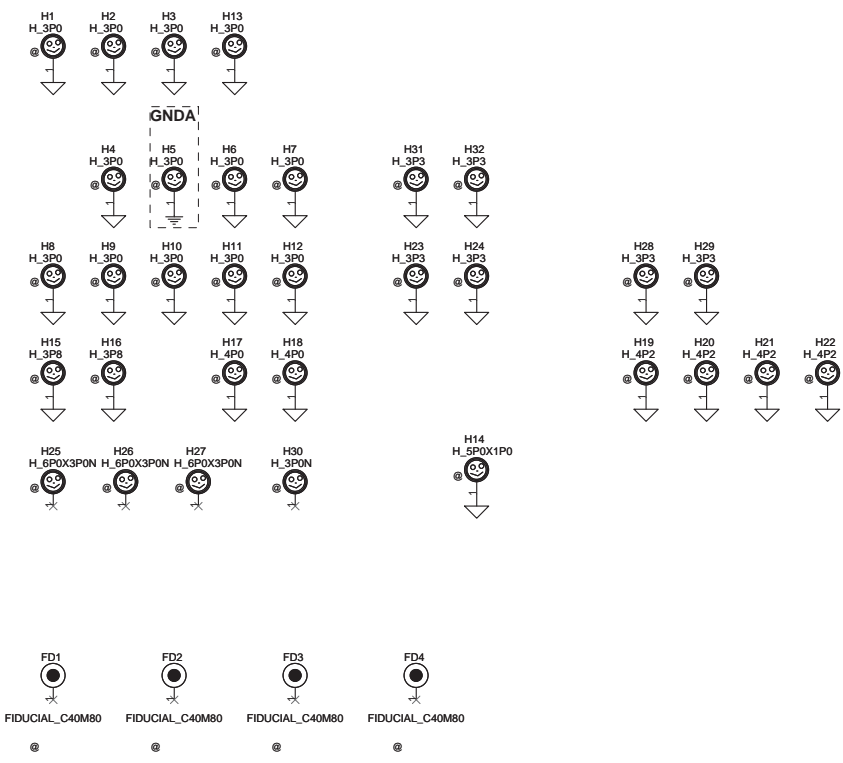
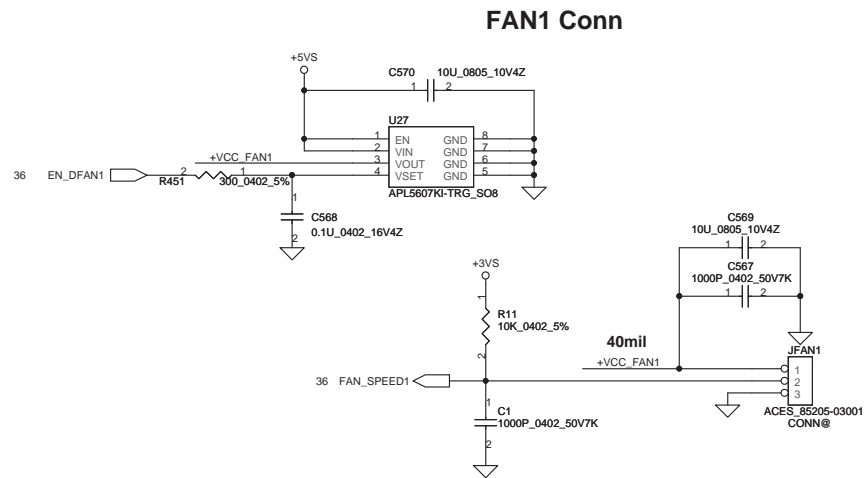


LED Status	Power/SUS		Battery		3G/WLAN	BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN	
NEW70/80/90	Blue	Amber	Blue		Blue	Amber	



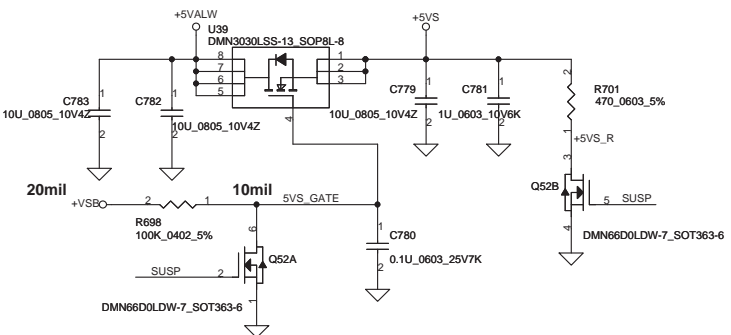


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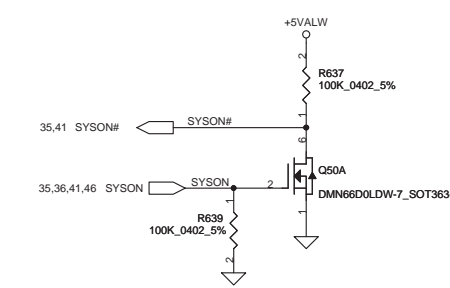
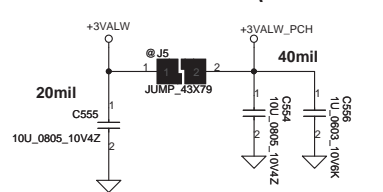


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				Date:	Tuesday, November 09, 2010
				Sheet	39 of 60
				Rev	B

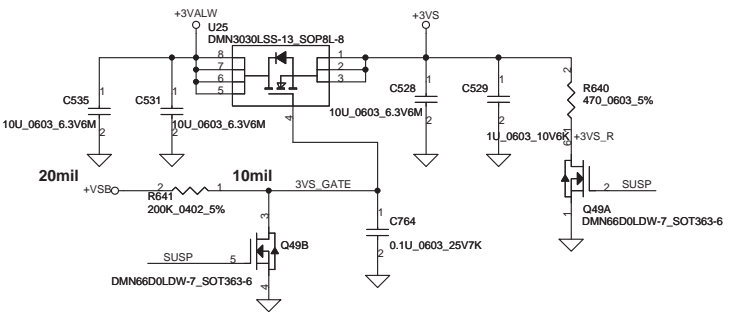
**+5VALW TO +5VS**



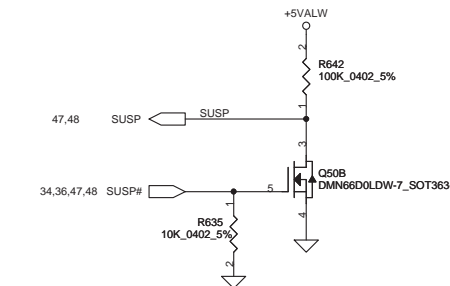
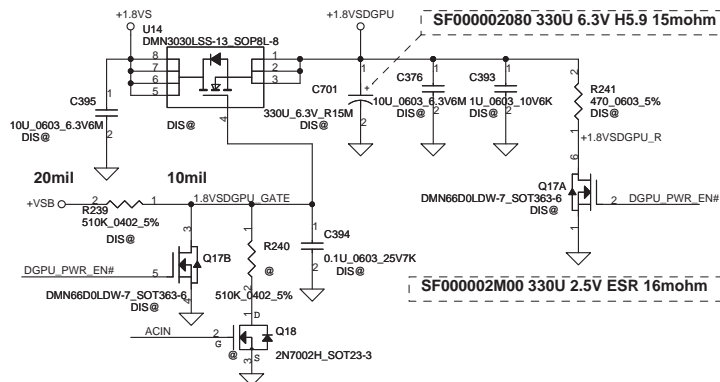
**+3VALW TO +3VALW(PCH AUX Power)**



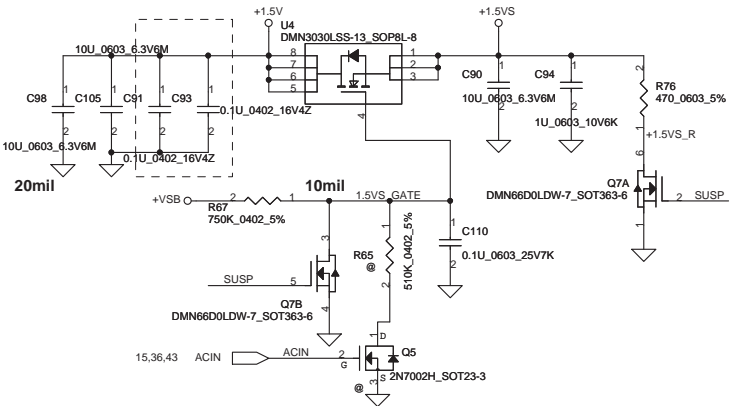
**+3VALW TO +3VS**



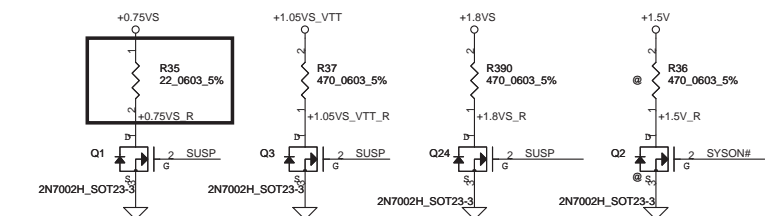
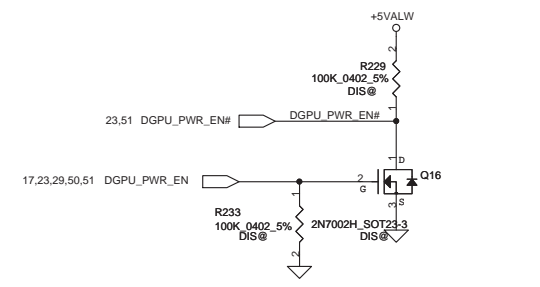
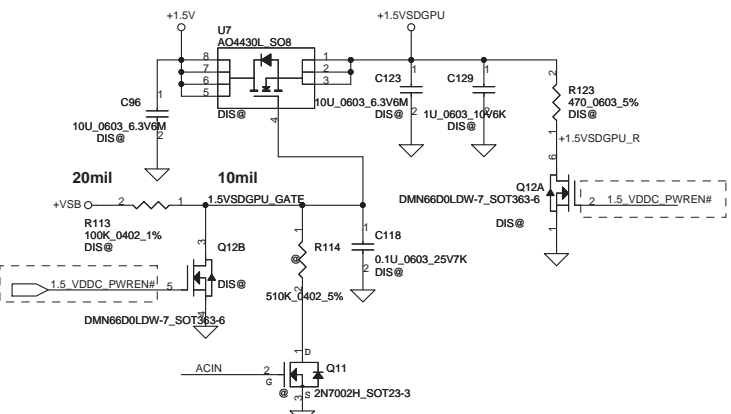
**+1.8VS to +1.8VSDGPU for GPU**



**+1.5V to +1.5VS**

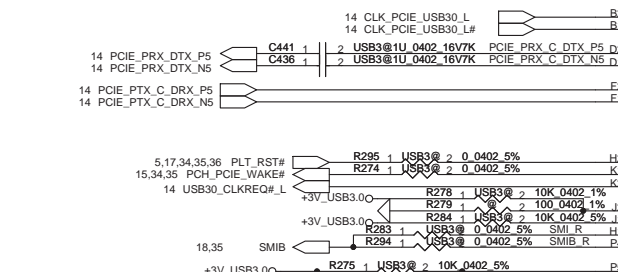
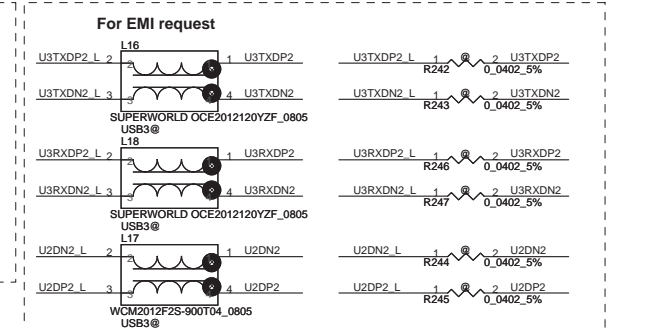
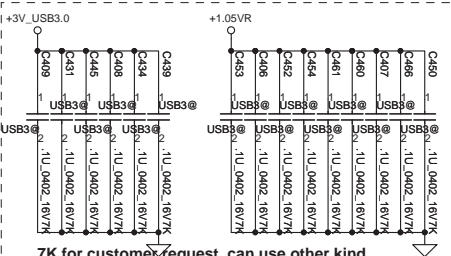
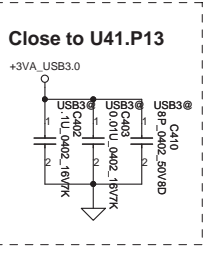
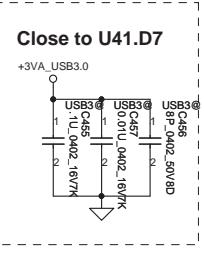
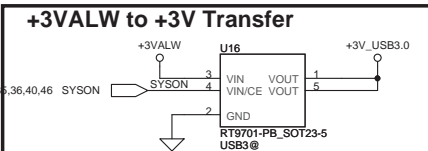
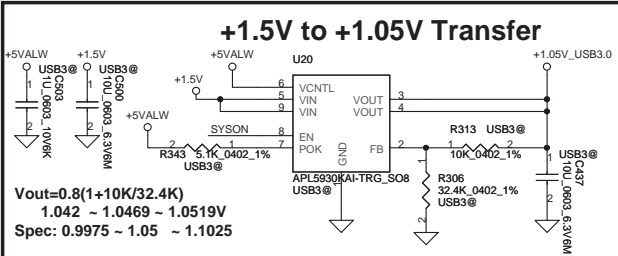


**+1.5V to +1.5VSDGPU for GPU**



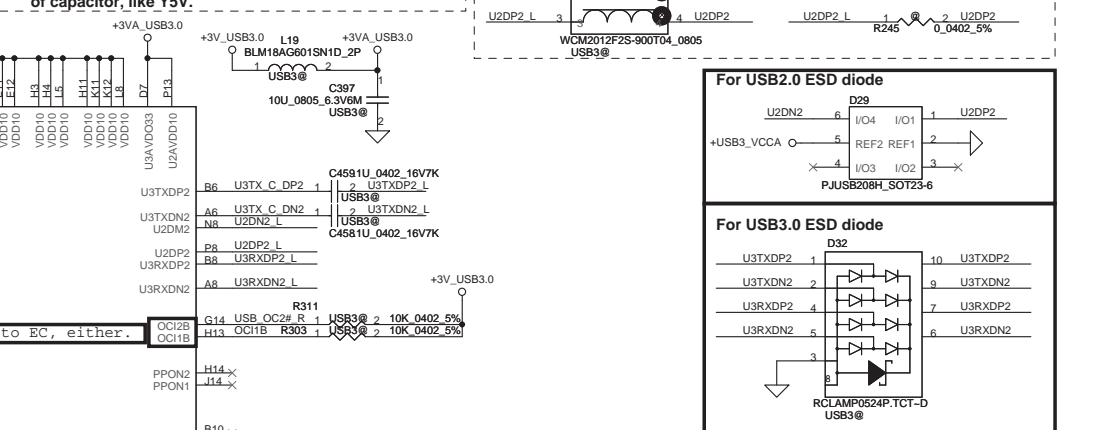
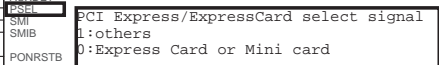
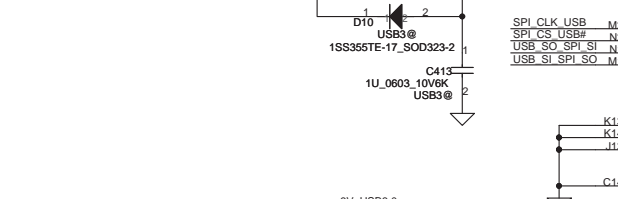
2009/08/14  
CP\_S3PowerReduction  
WhitePaper\_Rev0.9  
0.75VS speed up discharge

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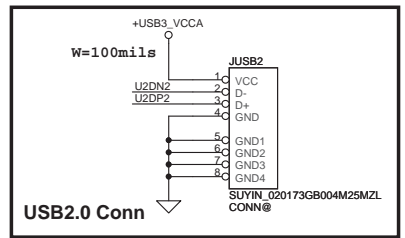
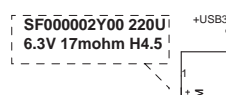
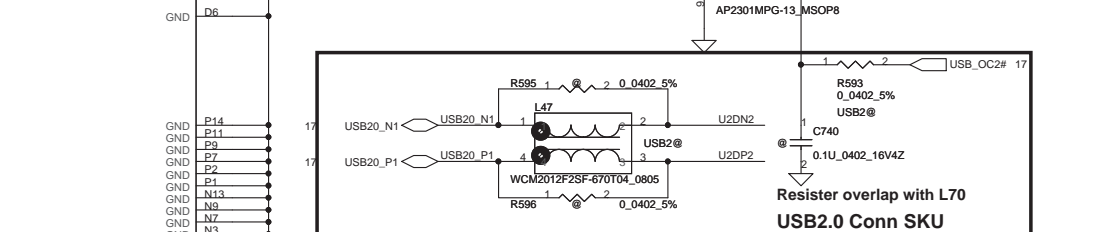
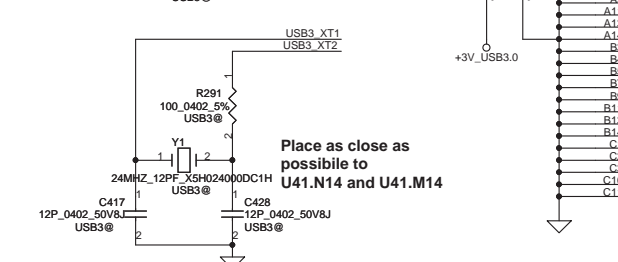
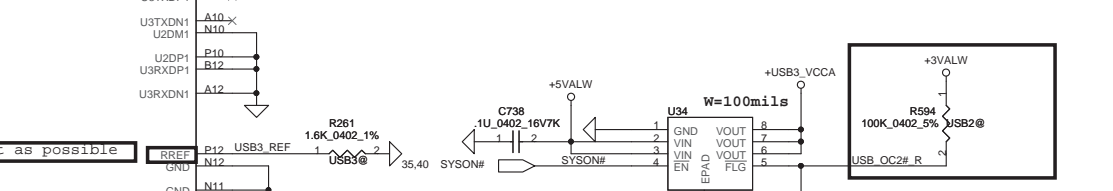
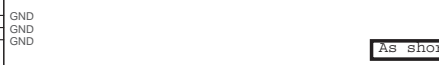
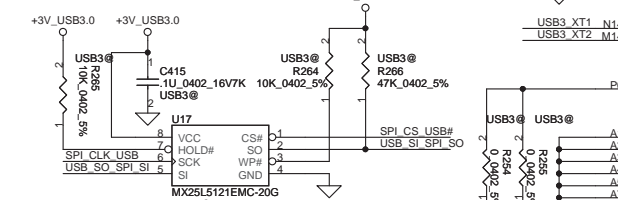


**SPEC Max: +3V---200mA; +1.05V---800mA**  
**Idle mode: 0.489W;**  
**+3V---43mA; +1.05V---328mA**  
**D3 mode: 0.066W;**  
**+3V---5.4mA; +1.05V---45mA**

Can be attach to EC, either.



As short as possible



Pin compare table for support USB remote wakeup or not

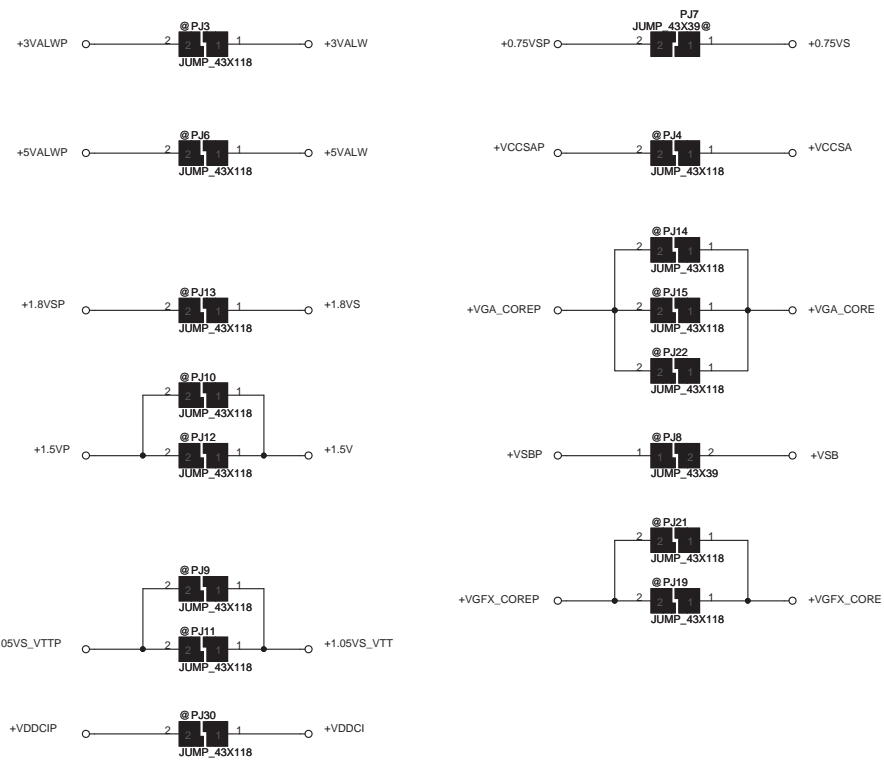
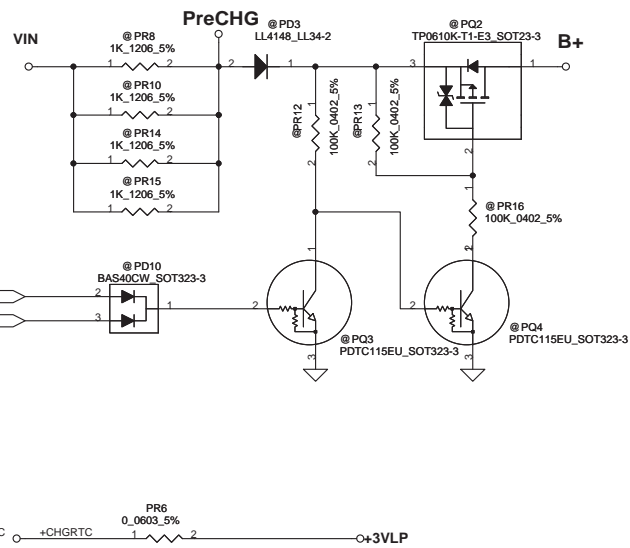
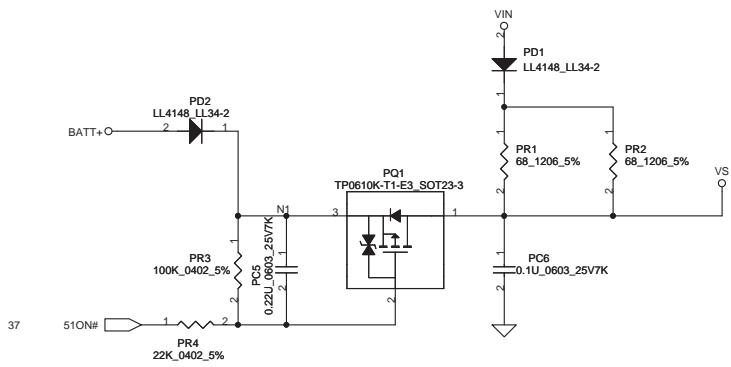
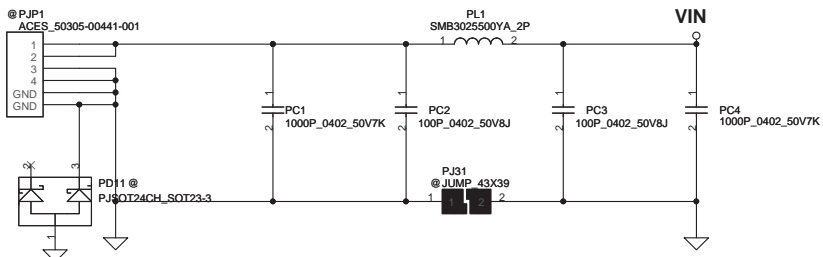
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y5,R816,C879,C880
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

UPD720200AF1-DAP-A,FBGA176

P/N: SA00048H10 (S IC UPD720200AF1-DAP-SSA-A FBGA USB3.0)

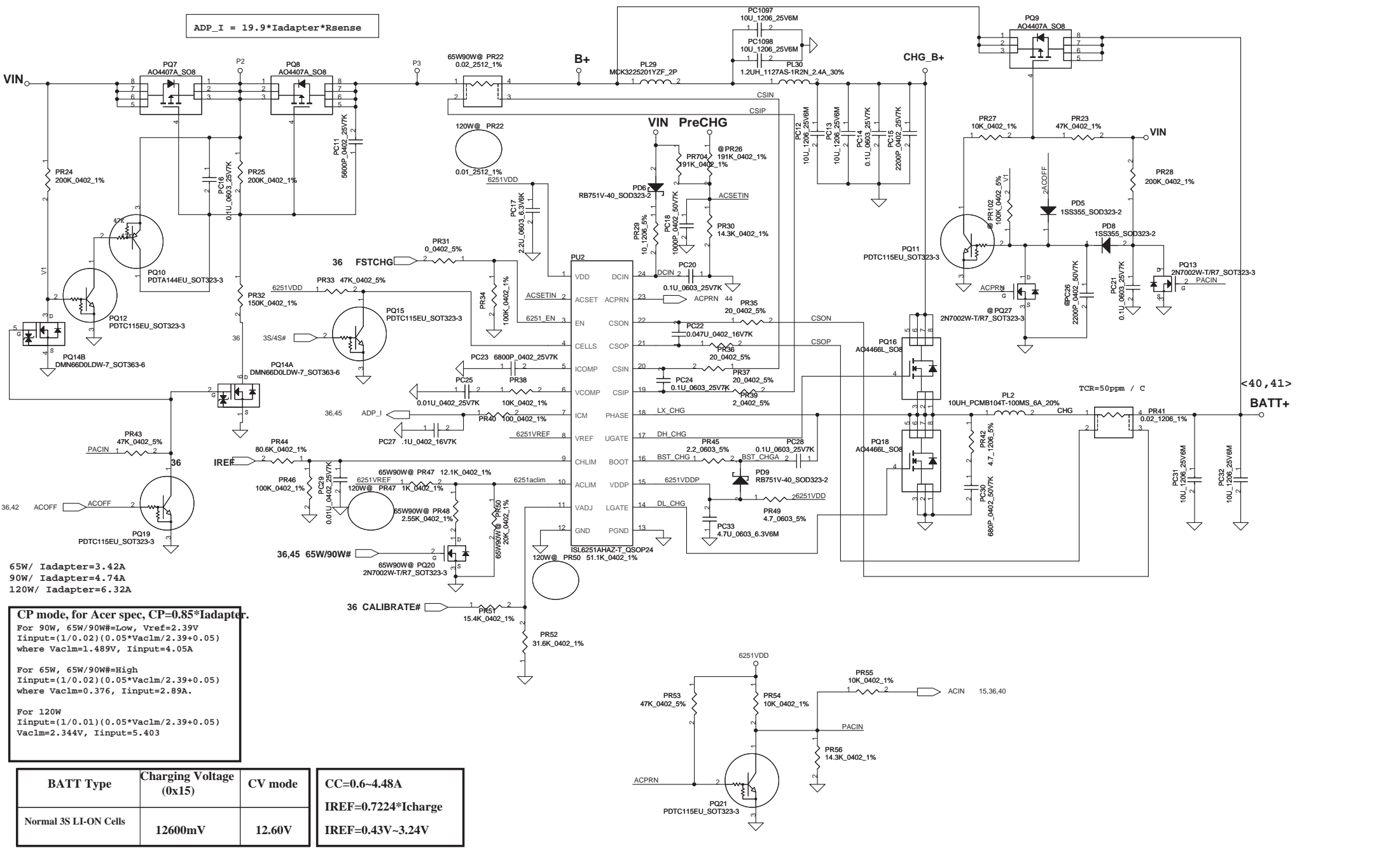
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$$ADP\_I = 19.9 * I_{adapter} * R_{sense}$$

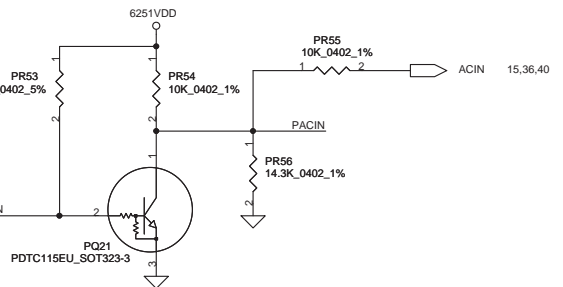


65W/ Iadapter=3.42A  
 90W/ Iadapter=4.74A  
 120W/ Iadapter=6.32A

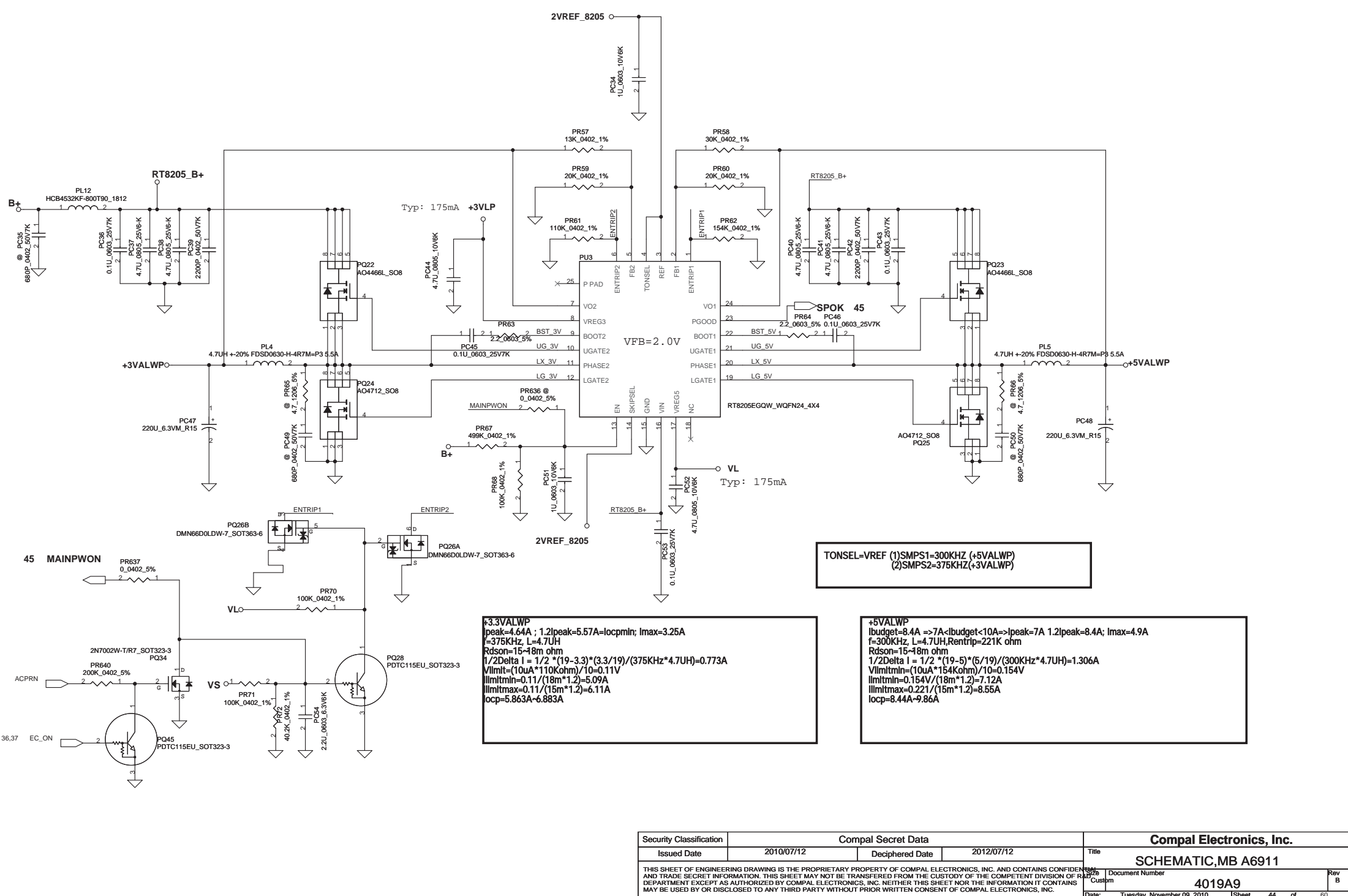
**CP mode, for Acer spec, CP=0.85\*Iadapter.**  
 For 90W, 65W/90W#=#Low, Vref=2.39V  
 $I_{input} = (1/0.02) (0.05 * V_{aclm} / 2.39 + 0.05)$   
 where  $V_{aclm} = 1.489V$ ,  $I_{input} = 4.05A$   
 For 65W, 65W/90W#=#High  
 $I_{input} = (1/0.02) (0.05 * V_{aclm} / 2.39 + 0.05)$   
 where  $V_{aclm} = 0.376V$ ,  $I_{input} = 2.89A$   
 For 120W  
 $I_{input} = (1/0.01) (0.05 * V_{aclm} / 2.39 + 0.05)$   
 $V_{aclm} = 2.344V$ ,  $I_{input} = 5.403$

<b>BATT Type</b>	<b>Charging Voltage (0x15)</b>	<b>CV mode</b>	<b>CC=0.6~4.48A</b>
Normal 3S LI-ON Cells	12600mV	12.60V	<b>IREF=0.7224*Icharge</b>
			<b>IREF=0.43V~3.24V</b>

Kv  
 $R_{internal} = ic = 514K$  Rec=3K R1=PR379=15.4K  
 $R2 = PR381 = 31.6K$   
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$   
 $r = 514K // 514K // 31.6K = 28.14K$   
 $V_{cell} = 0.175 * V_{adj} + 3.99V$   
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$   
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$   
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$   
 $1.899 = (4.2 - (V_{cell} * A * 0.175)) * Kv = (4.2 - (4.2 * A * 0.175)) * Kv$   
 $A = V_{ref} * (R / (R + 514K)) = 0.052$   
 $Kv = 9.451$



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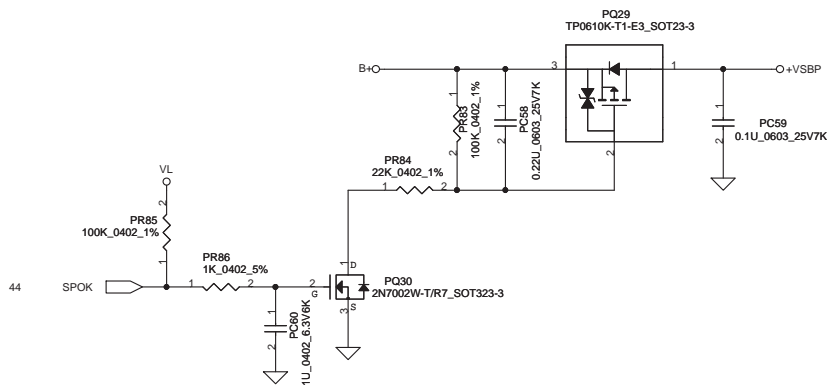
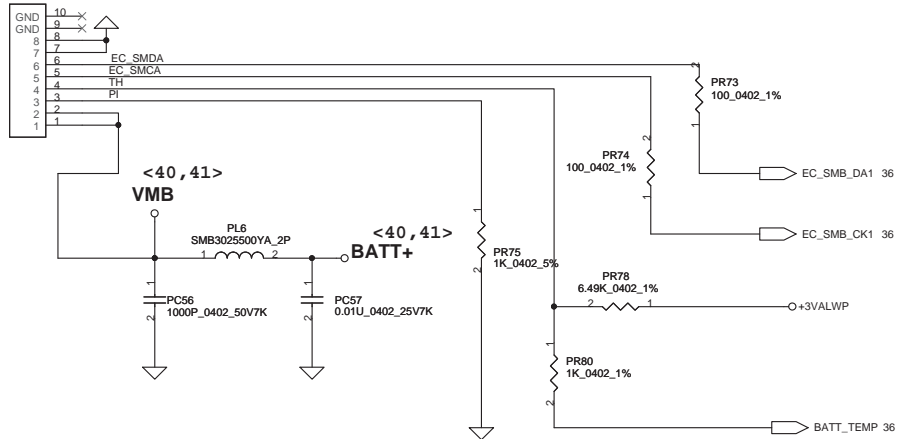
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)  
 (2)SMPS2=375KHZ(+3VALWP)

**+3.3VALWP**  
 $I_{peak}=4.64A$  ;  $1.2I_{peak}=5.57A=I_{ocpmin}$  ;  $I_{max}=3.25A$   
 $f=375KHz$  ,  $L=4.7UH$   
 $R_{ds(on)}=15-18m\ ohm$   
 $1/2\Delta I = 1/2 * (19-3.3) * (3.3/19) / (375KHz * 4.7UH) = 0.773A$   
 $V_{limin} = (10uA * 110Kohm) / 10 = 0.11V$   
 $I_{limin} = 0.11V / (18m * 1.2) = 5.09A$   
 $I_{limimax} = 0.11V / (15m * 1.2) = 6.11A$   
 $I_{ocp} = 5.863A \sim 6.883A$

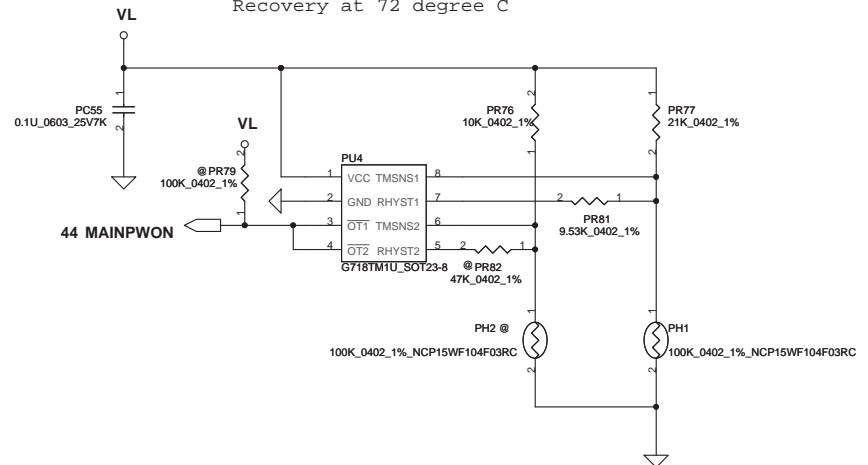
**+5VALWP**  
 $I_{budget}=8.4A \Rightarrow 7A < I_{budget} < 10A \Rightarrow I_{peak}=7A$   $1.2I_{peak}=8.4A$  ;  $I_{max}=4.9A$   
 $f=300KHz$  ,  $L=4.7UH$ ,  $R_{entrip}=221K\ ohm$   
 $R_{ds(on)}=15-18m\ ohm$   
 $1/2\Delta I = 1/2 * (19-5) * (5/19) / (300KHz * 4.7UH) = 1.306A$   
 $V_{limin} = (10uA * 154Kohm) / 10 = 0.154V$   
 $I_{limin} = 0.154V / (18m * 1.2) = 7.12A$   
 $I_{limimax} = 0.154V / (15m * 1.2) = 8.55A$   
 $I_{ocp} = 8.44A \sim 9.86A$

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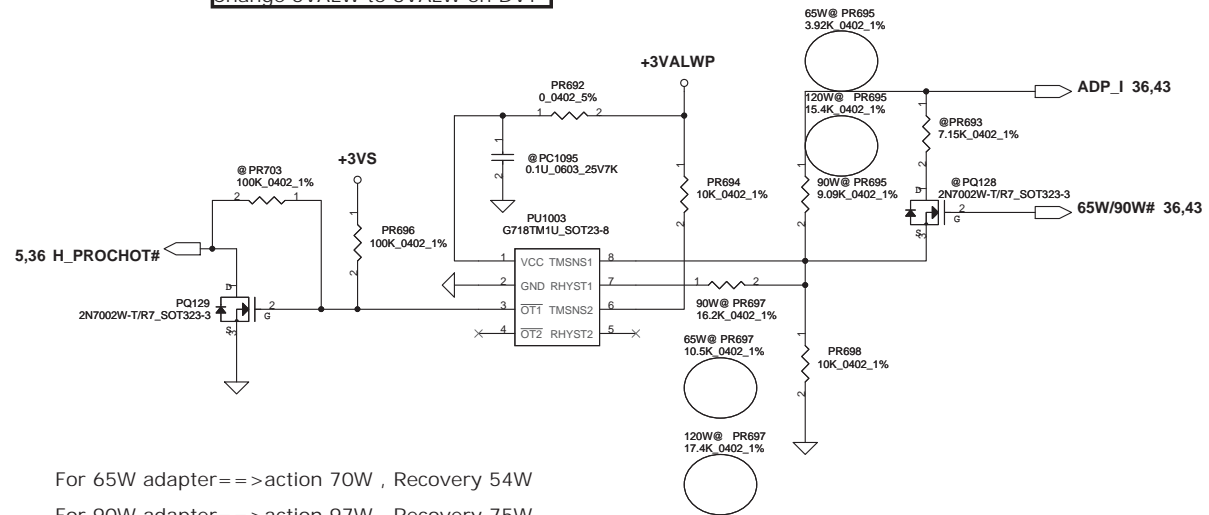
@PJP2  
SUYIN\_200275GR008G13GZR



PH1 under CPU botten side :  
CPU thermal protection at 92 degree C  
Recovery at 72 degree C

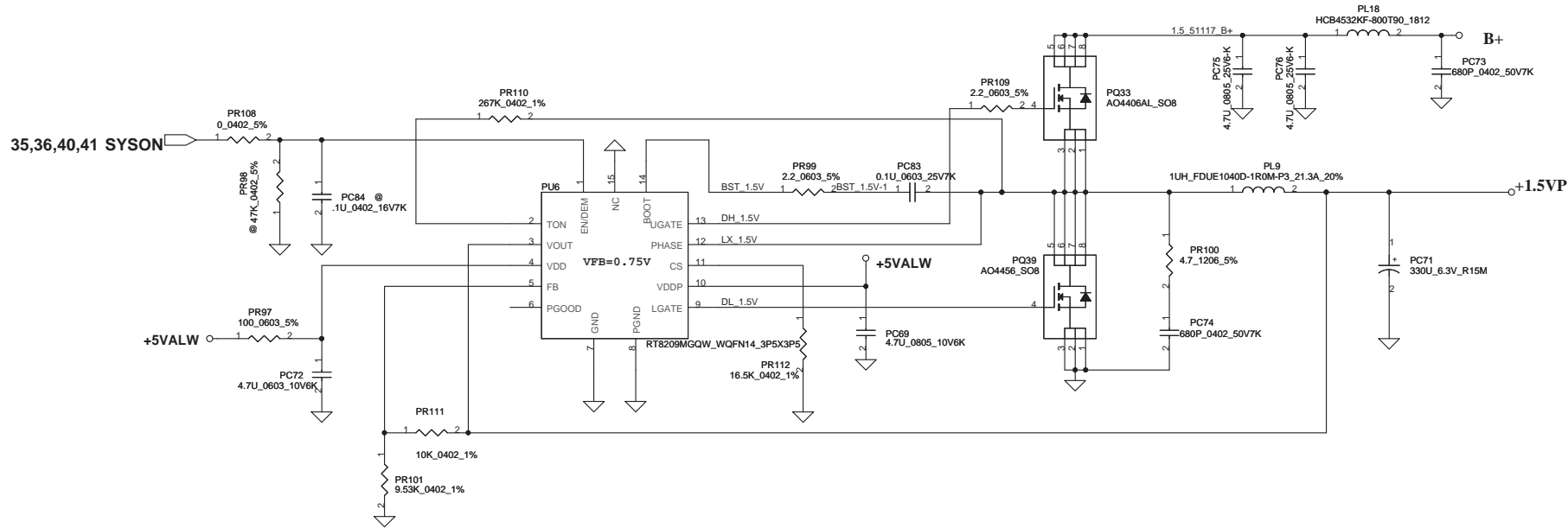


Change 5VALW to 3VALW on DVT



For 65W adapter==>action 70W , Recovery 54W  
For 90W adapter==>action 97W , Recovery 75W  
For 120W adapter==>action 135W , Recovery 100W

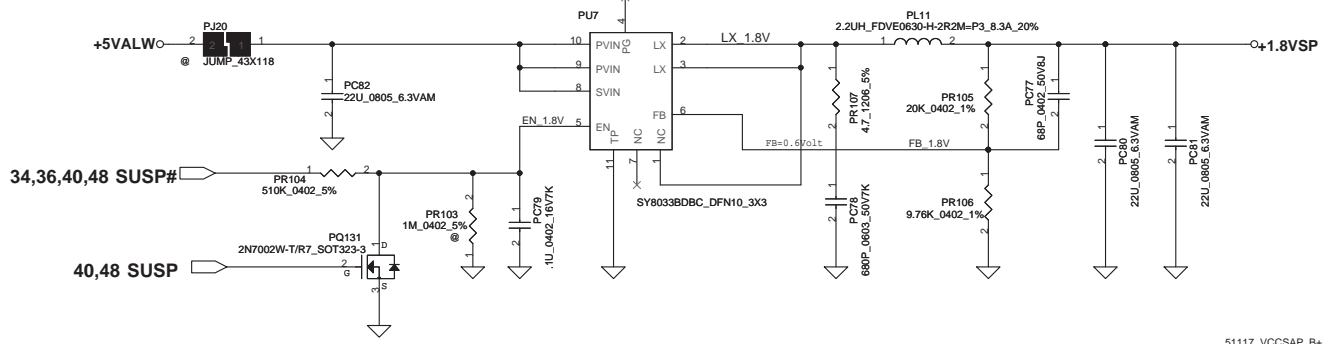
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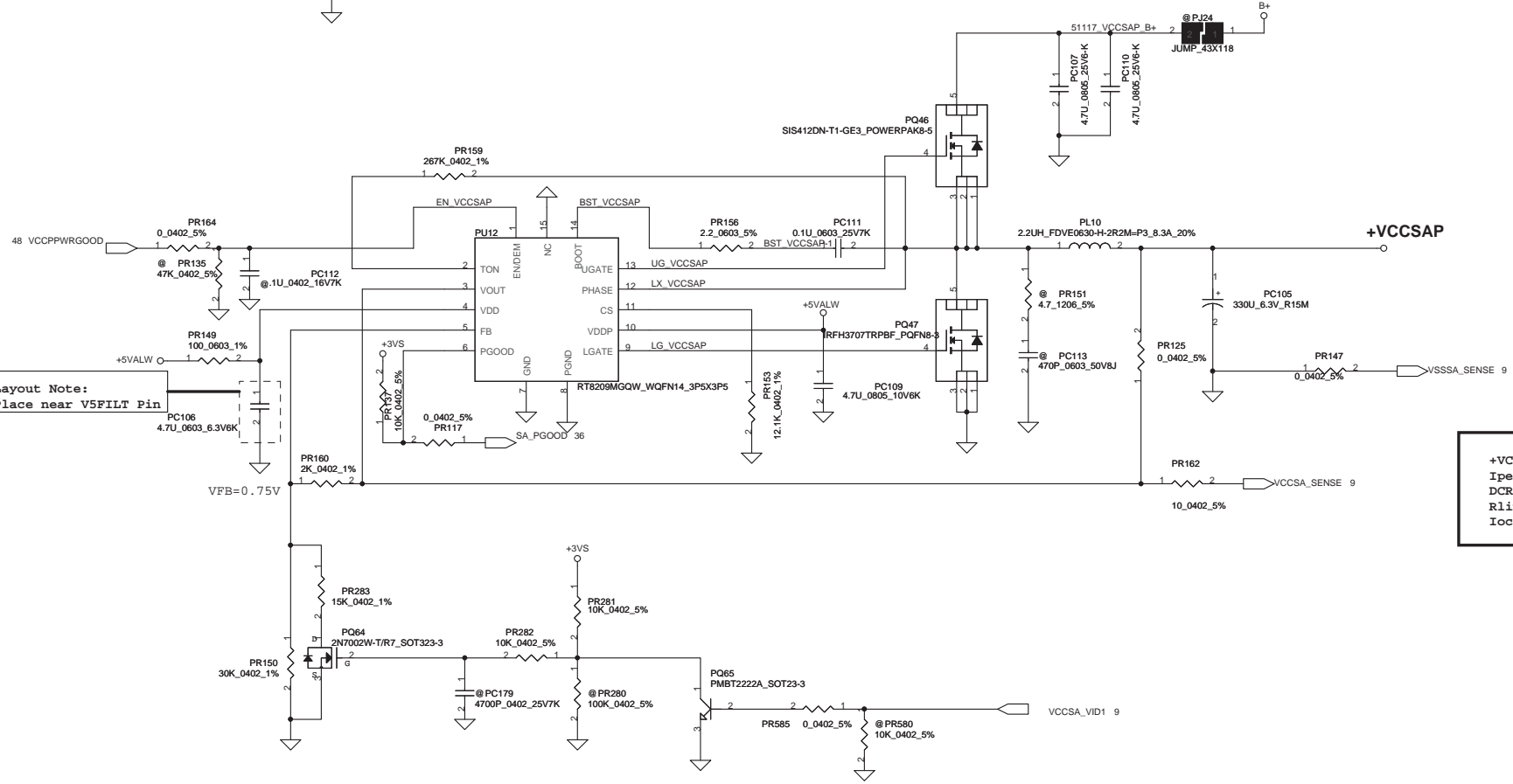
+1.5VP  
 $I_{peak} = 21.56A$ ;  $1.2I_{peak} = 25.87A$  ;  $I_{max} = 15.09A$   
 $R_{ton} = 267K$ ,  $F_{sw} = 298KHz$ ,  $R_{dson} = 4.5-5.6m\Omega$   
 $R_{trip} = 16.5K$   
 $I_{ocp} = 25.97A-42.41A$

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1.8VSP  
 Ipeak=3.35A ; 1.2Ipeak=4.02 ; Imax=2.345A  
 Vout=0.6\*(1+(20K/10K))=1.8V  
 -DVT-



+VCCSAP  
 Ipeak=6A , Imax=4.2A, 1.2Ipeak=7.2A  
 DCR= 9 m(typ)-10 m(max)  
 Rlimit=12.1K,Rdson=14.5-17.9mohm  
 Iocp=7.24A-12.59A

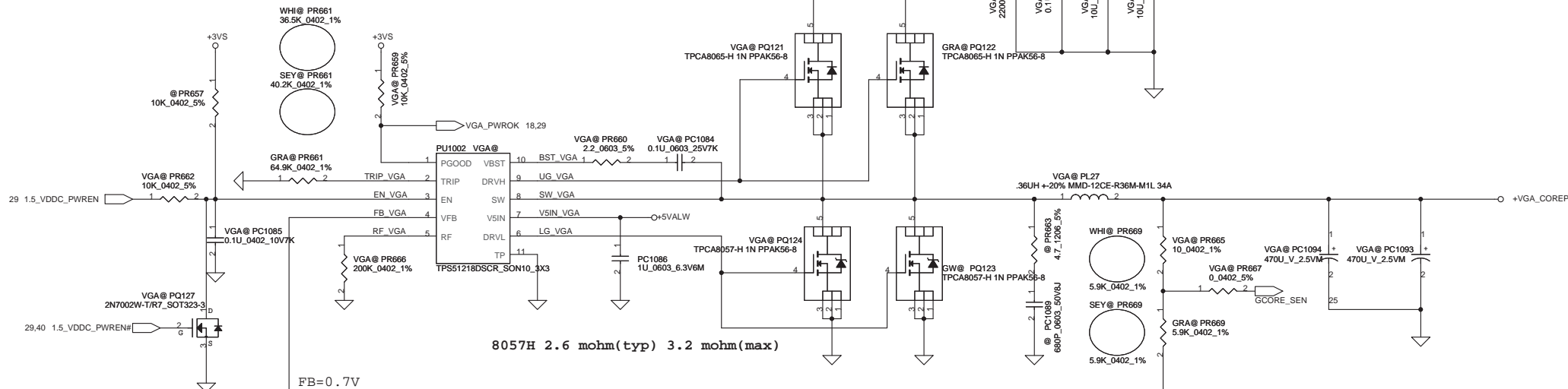
Layout Note:  
 Place near V5FILT Pin

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	
0	1	0.8 V	Yes/Yes	
1	1	0.75V	No/Yes	
1	1	0.65V	No/Yes	

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Note: Use VCCSA\_SEL to switch High & Low Level for VID[1]



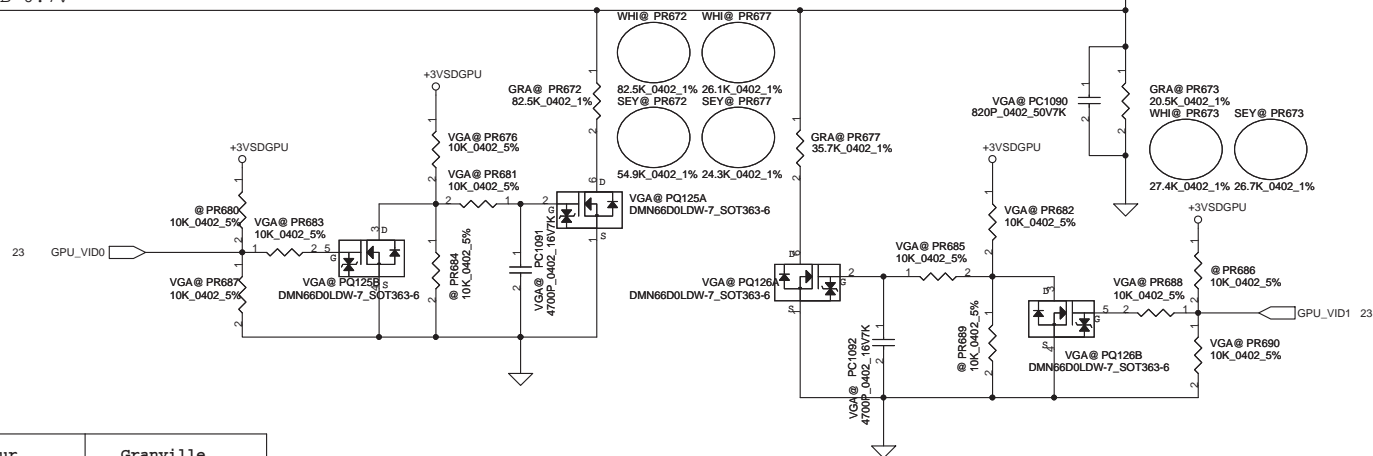


8057H 2.6 mohm(typ) 3.2 mohm(max)

FB=0.7V

**Ipeak**  
**Granville(35W) 47A**  
**Whistler(25W) 27A(VDDC+VDDCI)**  
**Seymour(15W) 14.2A(VDDC+VDDCI)**

Switch freq. (RF pin setting)  
 47K ==>450KHz  
 100K ==>390KHz  
 200K ==>350KHz (Currently setting)  
 470K ==>300KHz



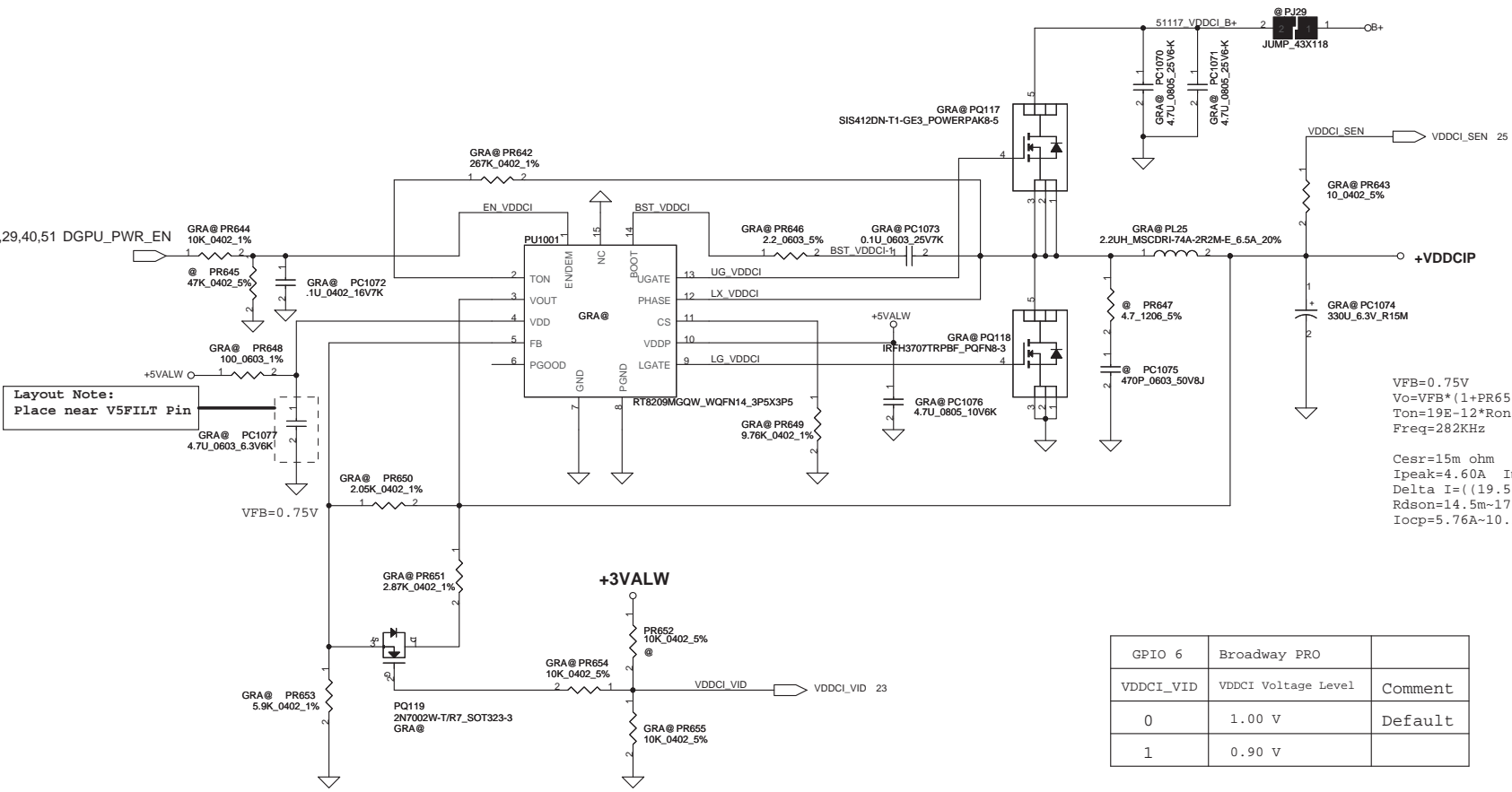
For Whistler  
 $1/2\Delta I = 4.05A$   
 $V_{trip} = 36.5K * 10\mu A = 0.365V$   
 $I_{ocpmin} = 0.365V / (8 * 1.6m) + 1/2\Delta I = 28.51A + 4.05A = 32.56A$

For Granville  
 $1/2\Delta I = 4.05A$   
 $V_{trip} = R_{trip} * I_{trip} = 64.9K * 10\mu A = 0.649V$   
 $I_{ocpmin} = (V_{trip} / (8 * R_{son})) + 1/2\Delta I = (0.649V / (8 * 1.6m)) + 4.05A = 50.7A + 4.05A = 54.75A$

For Seymour  
 $1/2\Delta I = 4.31A$   
 $V_{trip} = 40.2K * 10\mu A = 0.402V$   
 $I_{ocp} = 0.402V / (8 * 3.2m) + 1/2\Delta I = 15.70A + 4.31A = 20.01A$

GPIO 15	GPIO 20	Whistler	Seymour	Granville
GPU_VID0	GPU_VID1	Core Voltage Level	Core Voltage Level	Core Voltage Level
1	1	0.85V	0.85V(0.855V)	0.90V
0	1	0.9V	0.9V(0.930V)	0.95V
1	0	1.00V	1.00V(1.025V)	1.00V
0	0		1.1V(1.100V)	1.05V

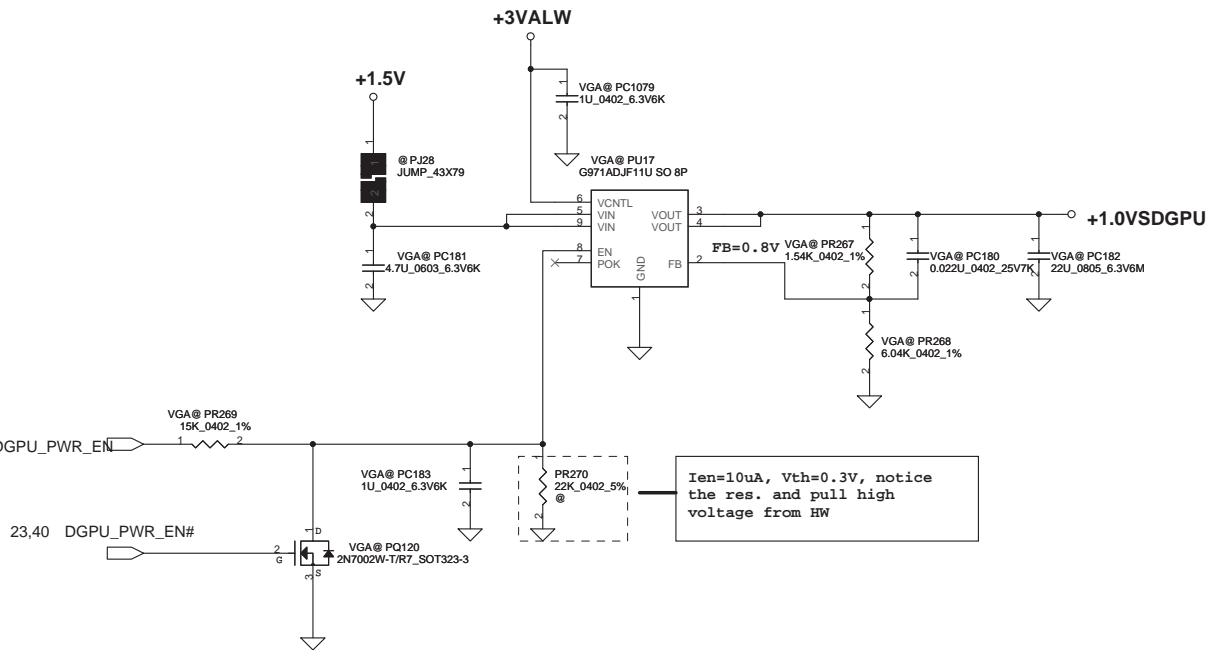
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Layout Note:  
Place near V5FILT Pin

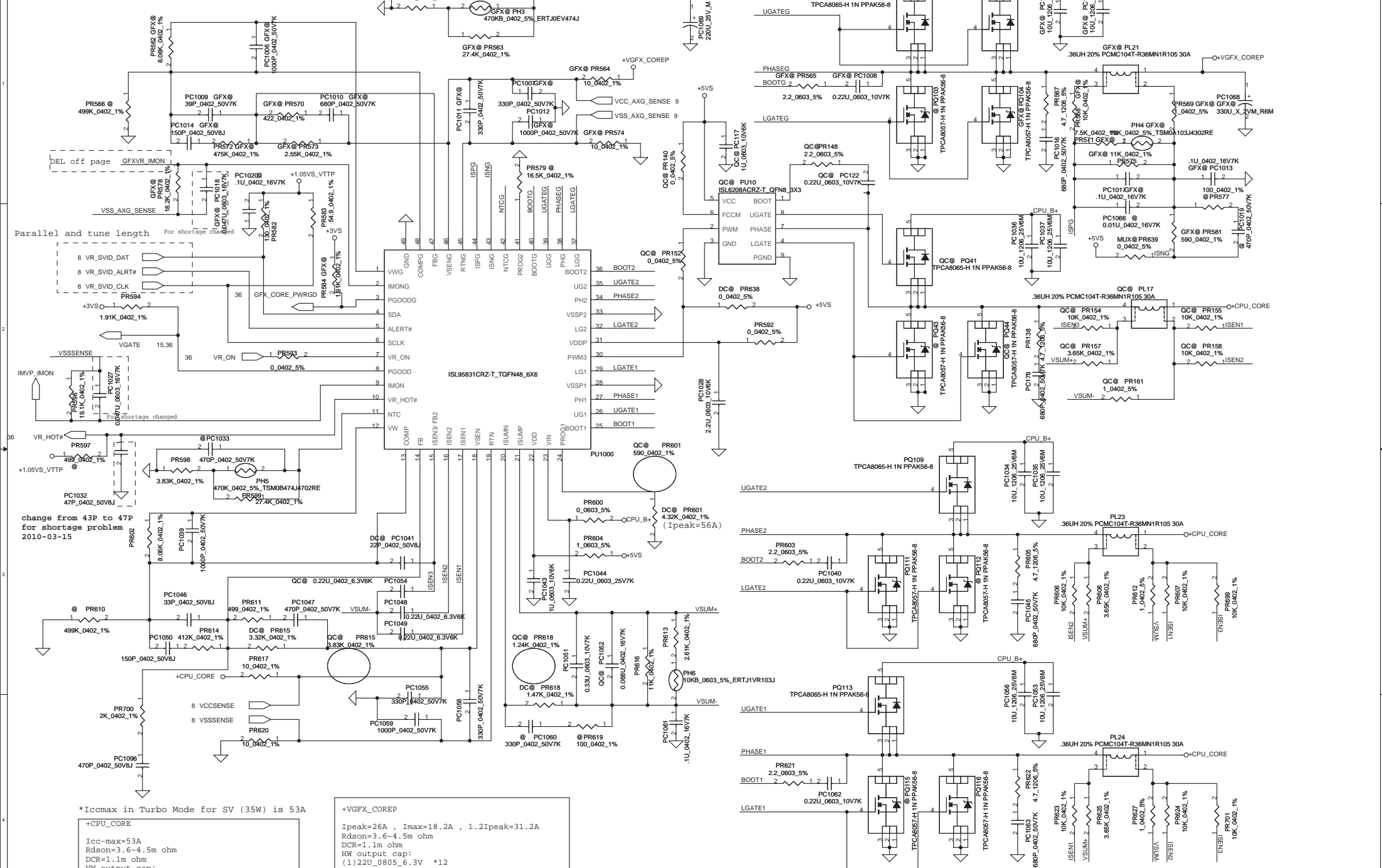
$VFB=0.75V$   
 $V_o=VFB*(1+PR650/PR653)=1.01V$   
 $Ton=19E-12*Ron*((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7$   
 $Freq=282KHz$   
 $Cesr=15m\ ohm$   
 $Ipeak=4.60A\ I_{max}=2.70A\ 1.2I_{peak}=5.52A$   
 $\Delta I=(19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A$   
 $Rdson=14.5m-17.9m\ ohm$   
 $Iocp=5.76A-10.19A$

GPIO 6	Broadway PRO	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	



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Alert# PU resistor need close CPU, so the PU resistor in HW schematic. but DAT and CLK need close PWM-IC, so the PU resistor in POWER schematic.



Parallel and tune length For shorrtage changed

change from 43P to 47P for shorrtage problem 2010-03-15

\*Iccmax in Turbo Mode for SV (35W) is 53A  
 +CPU\_CORE  
 Icc-max=53A  
 Rdsn=3.6~4.5m ohm  
 DCR=1.1m ohm  
 HW output cap:  
 (1)10U\_0805\_4V \*10  
 (2)22U\_0805\_6.3V \*15  
 (3)470U\_D2\_2V \*4(ESR=4.5m ohm)

+V GFX\_COREP  
 Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A  
 Rdsn=3.6~4.5m ohm  
 DCR=1.1m ohm  
 HW output cap:  
 (1)22U\_0805\_6.3V \*12  
 (2)470U\_D2\_2V \*2(ESR=4.5m ohm)

Rdroop is PR615  
 Ri is PR618

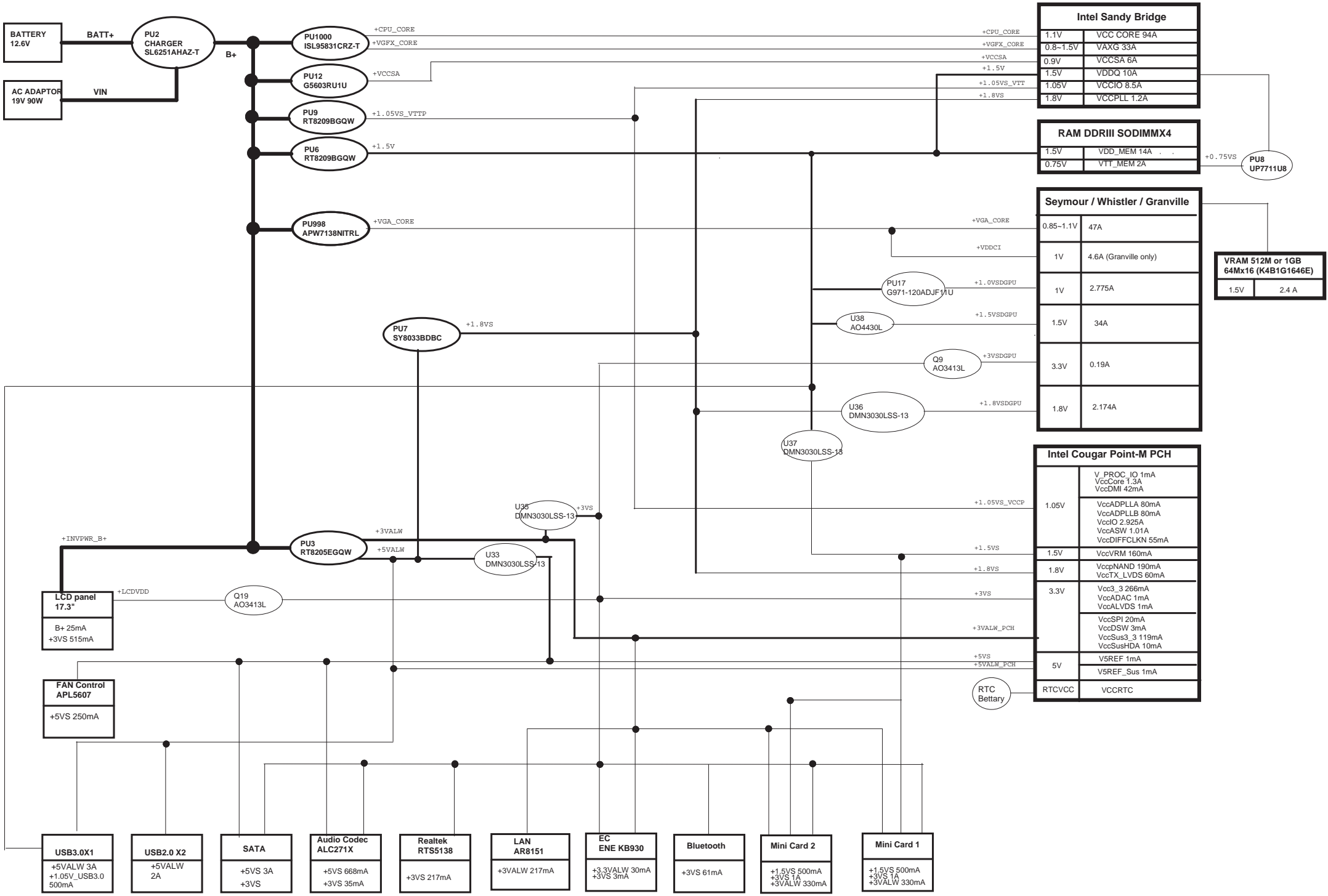
\*OCP setting value=40A

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW increase 1.8V voltage.	HW need to increase 1.8V voltage.	0.1	47	Change PR106 from SD034100280 to SD034976180.	2010/09/23	DVT
2	VGA Granville OVP issue.	Because VGA has happened OVP issue in Granville SKU, that is caused by output capacitor too small. change PC1094 to SGA00004200 to solve it. PC1088 must remove.	0.1	49	Add PC1094 to SGA00004200 and delete PC1088 SF000002000.	2010/09/23	DVT
3	1.8V Power sequence adjust.	HW adjust 1.8V power sequence.	0.1	47	change PR104 from SD028100380 to SD028150380.	2010/09/23	DVT
4	0.75V Power sequence adjust.	HW adjust 0.75V power sequence.	0.1	48	Change PR127 from SD028150380 to SD034267380.	2010/09/23	DVT
5	adjust +1.05VS_VTT power sequence	HW adjust +1.05VS_VTT power sequence	0.1	48	Change PC99 from SE107475K80 to SE076104K80.	2010/09/23	DVT
6	adjust +VDDCI power sequence	HW adjust +VDDCI power sequence	0.1	50	Change PR644 from SD034301380 to SD034100280.	2010/09/23	DVT
7	HW request to delete PR103.	HW request to delete PR103.	0.2	47	Delete PR103 SD028100480.	2010/09/28	DVT
8	PR104 BOM error.	PR104 BOM error for power sequence.	0.2	47	Change PR104 from SD034150380 to SD034510380.	2010/09/28	DVT
9	PR669 BOM error for Seymour only.	PR669 BOM error for Seymour only.	0.2	49	Change PR669 from SD034681180 to SD034590180.	2010/09/28	DVT
10	To same as P5WE0 VCCSAP choke.	To same as P5WE0 VCCSAP choke.	0.2	47	Change PL10 from SH000009Q00 to SH00000M700.	2010/09/28	DVT
11	HW request to add PQ130 and PQ131 to speed up to 放电.	HW request to add PQ130 and PQ131 to speed up to 放电.	0.3	47 48	Add PQ130 and PQ131 SB000006800.	2010/10/05	DVT
12	Remove chargeable RTC battery.	We reserve chargeable RTC battery to prevent over heat issue, Thermal team result is pass, so remove chargeable RTC battery.	0.3	42	Delete PR691 SD013000080 Change PR6 from SD013560080 to SD013000080.	2010/10/05	DVT
13	Change PL4 and PL5 to TOKO new part.	Change PL4 and PL5 to TOKO new part.	0.3	44	Change PL4 and PL5 from SH000006J80 to SH00000MB00	2010/10/05	DVT
14	for ISN issue.	for ISN issue.	0.3	43	Add PL30 SH000009Q00 Delete PL28 SM010018210	2010/10/05	DVT
15	to same as P5WE0 choke.	to same as P5WE0 choke.	0.3	47	Change PL10 and PL11 from SH000009Q00 to SH00000F800	2010/10/05	DVT
16	for QC+25WGPU and QC+35W GPU change CP point.	Because Acer define QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Delete PQ20 SB000006800. Delete PR48 SD034255180 Change PR22 from SD000001F00 to SD021100B80.	2010/10/05	DVT
17	for QC+25WGPU and QC+35W GPU change CP point.	Because Acer define QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Change PR47 from SD034121280 to SD034100180 Change PR50 from SD034200280 to SD034511280	2010/10/05	DVT
18	Modify adapter throttling at turbo mode setting point.	Modify adapter throttling at turbo mode setting point.	0.3	45	Add PR695 SD034154280 Add PR697 SD034174280	2010/10/05	DVT
19	CPU Transient responds issue.	Change CPU transient responds RC time constant.	0.4	52	Add PC1052 SE000003J80. Add PC1096 SE071471J80. Add PR700 SD034200180.	2010/10/07	DVT
20	for ISN issue.	for ISN issue.	0.4	43	Change PL30 from SH000009Q00 to SH00000M700.	2010/10/07	DVT
21	Make BOM same as P5WE0.	Make BOM same as P5WE0.	0.4	52	Change PL21,PL23,PL24 from SH000005680 to SH00000HK00.	2010/10/07	DVT
22	BOM loss.	Because BOM Config loss 65@ and 90W@, so miss PR695 and PR697.	0.5	45	Add PR695 SD034909180 9.09K_0402_1% ADD PR697 SD034162280 16.2K_0402_1%	2010/10/26	PVT
23	Modify CPU OCP.	Because original design is for 3 phase DC, now change to 2 phase DC, so modify OCP.	0.5	52	Change PR618 from SD034698080 to SD000009480	2010/10/26	PVT
24	Modify DC LL.	Because DC OCP was modified, must also update LL of DC.	0.5	52	Change PR615 from SD034215180 to SD034332180	2010/10/26	PVT

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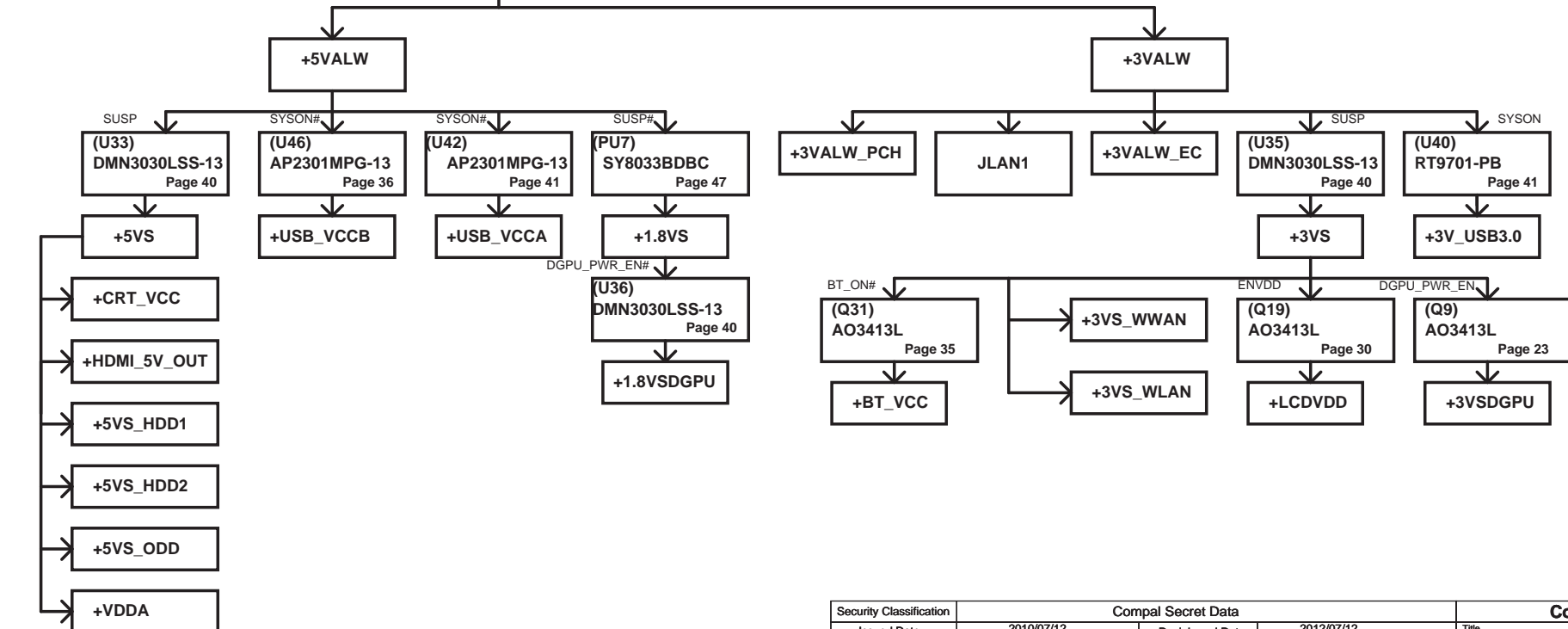
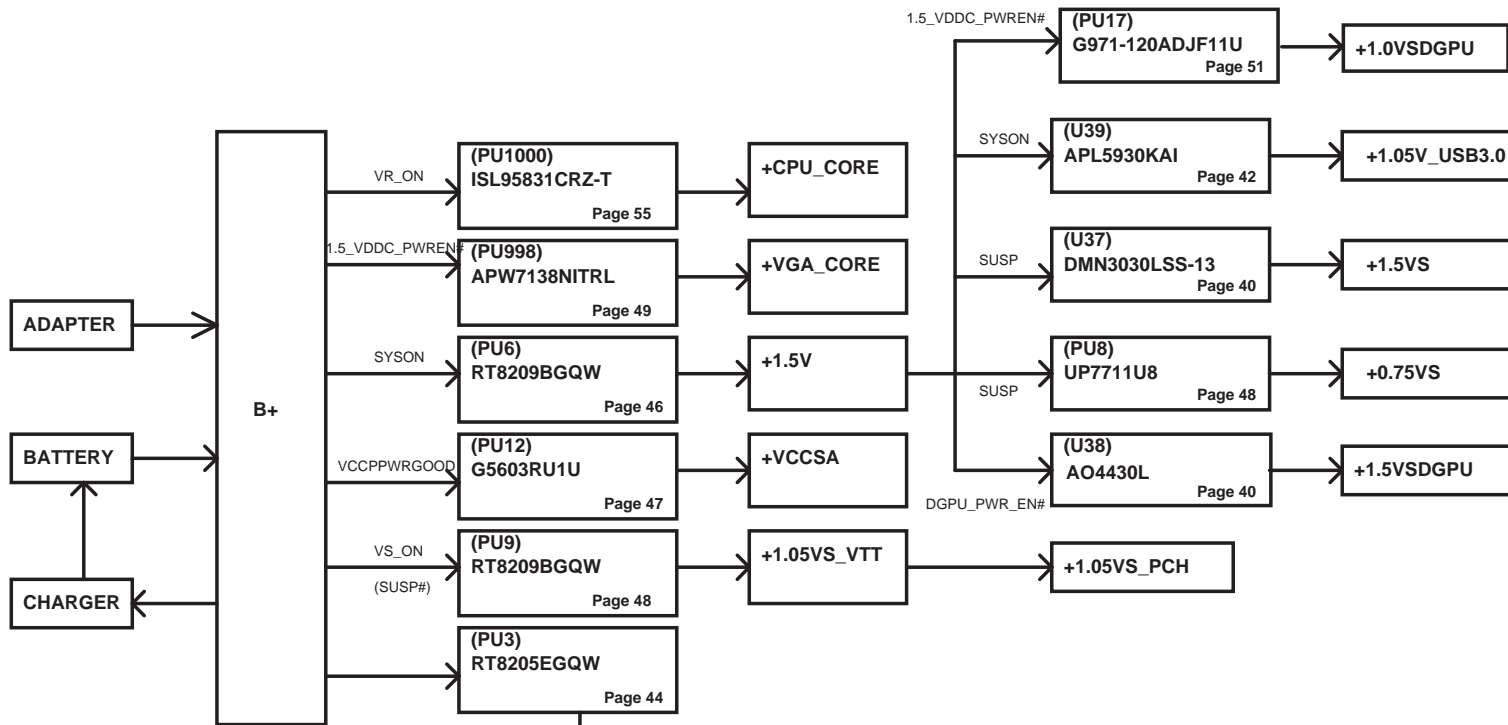
Intel Sandy Bridge	
1.1V	VCC CORE 94A
0.8-1.5V	VAXG 33A
0.9V	VCCSA 6A
1.5V	VDDQ 10A
1.05V	VCCIO 8.5A
1.8V	VCCPLL 1.2A

RAM DDRIII SODIMMX4	
1.5V	VDD_MEM 14A
0.75V	VTT_MEM 2A

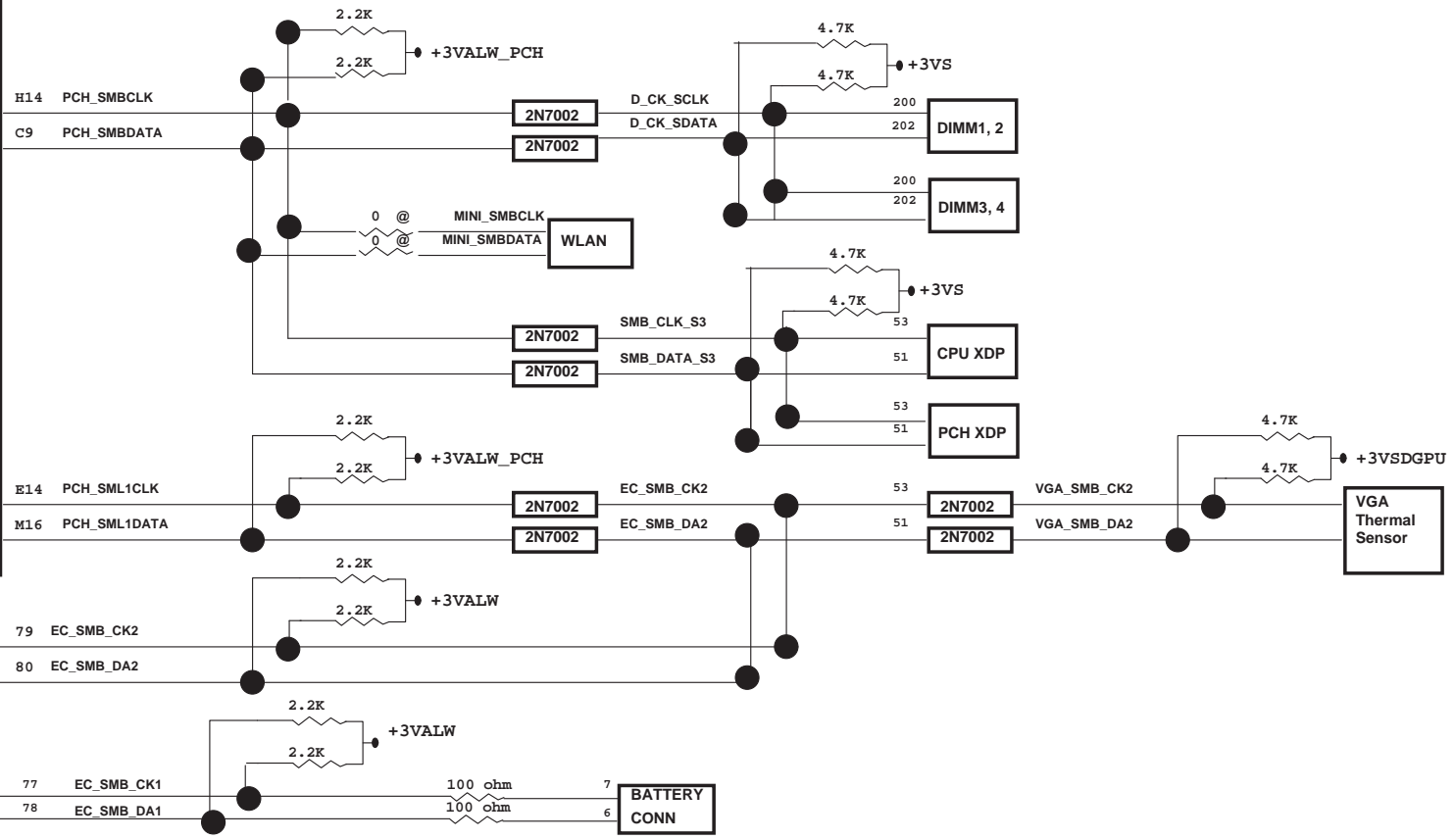
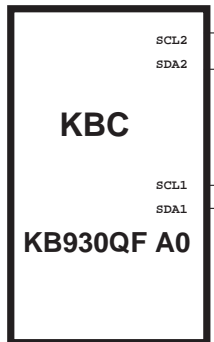
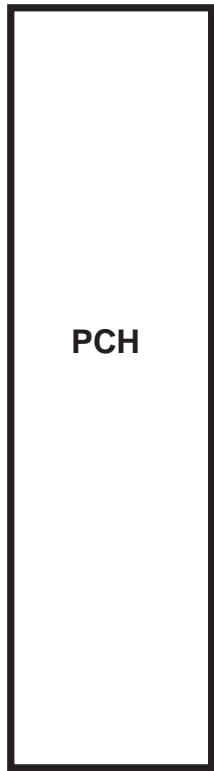
Seymour / Whistler / Granville	
0.85-1.1V	47A
1V	4.6A (Granville only)
1V	2.775A
1.5V	34A
3.3V	0.19A
1.8V	2.174A

Intel Cougar Point-M PCH	
1.05V	V_PROC_IO 1mA VccCore 1.3A VccDMI 42mA VccADPLL 80mA VccADPLL 80mA VccIO 2.925A VccASW 1.01A VccDIFFCLKN 55mA
1.5V	VccVRM 160mA
1.8V	VccpNAND 190mA VccTX_LVDS 60mA
3.3V	Vcc3_3 266mA VccDAC 1mA VccALVDS 1mA VccSPI 20mA VccDSW 3mA VccSus3_3 119mA VccSusHDA 10mA
5V	V5REF 1mA V5REF_Sus 1mA
RTC	RTCVCC VCCRTC

VRAM 512M or 1GB 64Mx16 (K4B1G1646E)	
1.5V	2.4 A

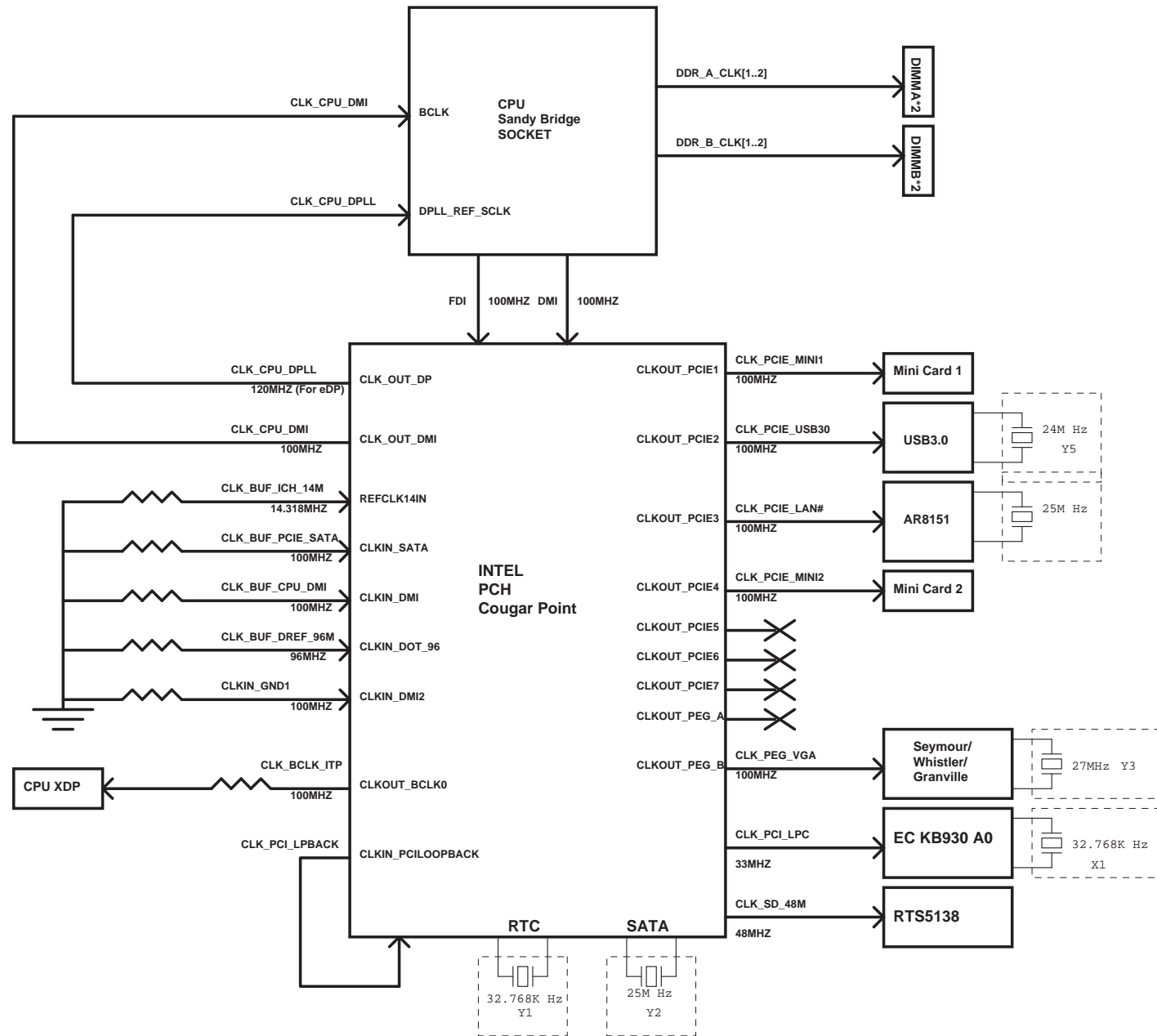


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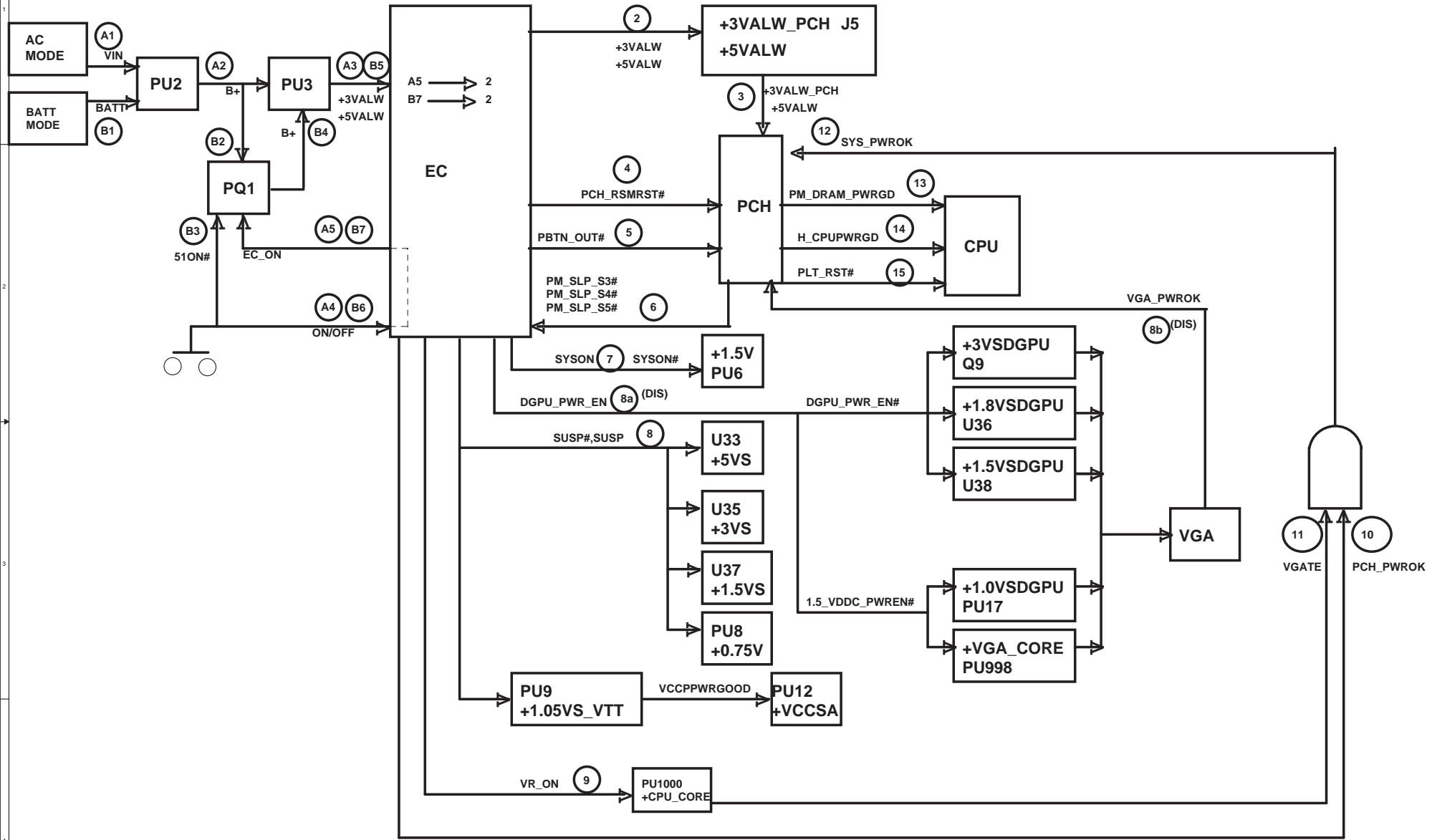


**PCH SM Bus address**

Device	Address
ChannelA DIMM0	A0 1010 000X
DIMM1	A2 1010 001X
ChannelB DIMM0	A4 1010 010X
DIMM1	A6 1010 011X




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**PCB**


ZZZ  
 LA-6911P MB Rev0: DA8000LC00  
 LA-6911P MB Rev1: DA8000LC10  
 LA-6911P MB with Small Board Rev1: DAZ  
 LA-6911P REV0 MB

**VGA**


U30  
 GRAN@ Granville PRO M2 A12:  
 SA00004C820(S IC 216-0769024 A12 GRANVILLE PRO ABO!)

U30  
 WHIS@ WHISTLER PRO M2 A11:  
 SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)


**X76**

ZZZ X76264BOL01  
 X761@ X76264BOL01 VRAM 512M SAM P7YE0  
 Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)


X76264BOL01 64Mx16x4 Seymour

ZZZ X76264BOL02  
 X762@ X76264BOL02 VRAM 512M HYN P7YE0  
 Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)


X76264BOL02 64Mx16x4 Seymour

ZZZ X76264BOL03  
 X763@ X76264BOL03 VRAM 1G SAM P7YE0  
 Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)


X76264BOL03 64Mx16x8 Whistler/Granville

ZZZ X76264BOL04  
 X764@ X76264BOL04 VRAM 1G HYN P7YE0  
 Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)


X76264BOL04 64Mx16x8 Whistler/Granville

ZZZ X76264BOL05  
 X765@ X76264BOL05 VRAM 2G HYN P7YE0  
 Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)


X76264BOL05 128Mx16x8 Whistler/Granville

ZZZ X76264BOL06  
 X766@ X76264BOL06 VRAM 2G SAM P7YE0  
 Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

X76264BOL06 128Mx16x8 Whistler/Granville

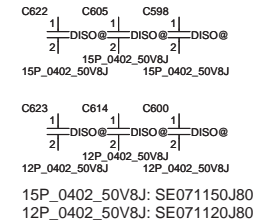
ZZZ X76264BOL07  
 X767@ X76264BOL07 VRAM 1G SAM P7YE0  
 Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

X76264BOL07 128Mx16x4 Seymour

ZZZ X76264BOL08  
 X768@ X76264BOL08 VRAM 1G HYN P7YE0  
 Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)

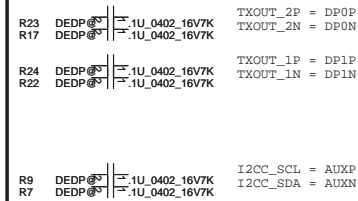
X76264BOL08 128Mx16x4 Seymour

**CRT Option Components**

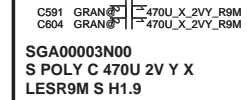


DIS only PCH DAC\_IREF  
 can use 1K\_0402\_5% PD to GND

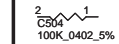
**DIS EDP Option Components**



**Granville VGA\_CORE CAP Option**



**EC susclk/crystal Option Components**



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0923:  
 REWORK:  
 ADD Q8 DMN66D0LDW-7(SB00000DH00) & change BOM structure to DIS@(DIS@ Granville can't power on issue)  
 R72 100K\_0402\_5%(SD028100380)change BOM structure to DIS@(DIS@ Granville can't power on issue)  
 R674 4.7K PH change BOM structure to @(+3VS GPIO19 leakage)  
 D31 change BOM structure to @(EC debug CLK leakage)  
 R531,R530 change BOM structure to DISO@(HSYN:VSYNC 11: Audio for both DisplayPort and HDMI)  
 ADD C591 C604 BOM option  
 (Seymour/Whistler option NOGRAN@ SGA20331E10 S POLY C 330U 2V 9mohm H1.9)  
 (Granville option GRAN@ SGA00004200 S POLY C 470U 2V M D2 LESR4.5M SX H1.9)  
 C746,C750 change from SF000001500 to SF000001580

Power sequence:  
 1. BOT (adjust +5VS power sequence)  
   R698 change from 200K to 100K\_0402\_5% (SD028100380)  
 2. BOT (adjust +1.8VS power sequence)  
   PR104 change from 100K to 510K\_0402\_5%(SD028510380)  
   remove PR103 1M\_0402\_5%  
 3. TOP (adjust +1.5VS power sequence)  
   R67 change from 510K\_0402\_5% to 750K\_0402\_5%(SD028750380)  
 4. TOP (adjust +0.75VS power sequence)  
   PR127 change from 150K\_0402\_5% to 267K\_0402\_5%(SD034267380)  
 5. TOP (adjust +1.05VS\_VTT power sequence)  
   PC99 change from 4.7U to .1U\_0402\_16V7K (SE076104K80)  
 6. TOP (adjust +1.5VSDGPU power sequence)  
   R113 510K change to 100K\_0402\_1% (SD034100380)  
 7. BOT (adjust +VDDCI power sequence)  
 PR644 301K change to 10K\_0402\_1% (SD034100280)

Power:  
 PR101 change from 10K to 9.53K (adjust +1.5V power)  
 PR106 change from 10K to 9.76K (adjust +1.8VS power)  
 Layout:  
 D21 change to SC600000B00 (for sourcer 2nd source)  
 DEL C590,C603 (DEL colay Cap)  
 L24,25,27,30,31 change from SM010004010 to SM010015410  
 BATT Blue light place at front side  
 H1 change H3P0 to H4P6  
 DEL LED1,LED2,LED3,LED4

0924:  
 Q37,Q39,Q40,Q41, change from SB00000FG00 to SB00000FG10  
 U7 change from SB000007000 to SB000007010  
 USB3.0 schmetic change to unpop  
 XDP change to unpop  
 U19 A10,N10,P10,B12 connect to GND

0925:  
 R249 change from U15.2 to U15.1(footprint issue)  
 R105 change form 10K to 10\_0402\_5%(SD028100A80)  
 R422 change BOM structure to @(crystal issue debug port1.2)  
 R422 change +3VS to +3VALW\_PCH (GPIO28)  
 R674 change BOM structure to @(leakage issue debug port1.2)  
 R674 change +3VALW\_PCH to +3VS (GPIO19)  
 ADD LED11 pop WLAN\_LED#(SC500007700),LED12 @ MEDIA\_LED#(SC591NB5A30)  
 LED10 WLAN\_LED#(SC500007700) change BOM structure to @  
 DEL D9,D10 USB3.0 old ESD diode  
 ADD D32 new USB3.0 ESD diode (SC300001D00)  
 DEL R238,R250,C401 USB3.0 conn PD resistor & CAP  
 EMI request:  
 R595,R596 change to @ L47 change to POP(USB2.0 common mode choke)

0927:  
 Audio vender suggest:  
 C913 change BOM structure to @  
 ADD C702 22K\_0402\_5%(SD028220280)  
 change USB conn to USB2.0(SUYIN\_020133GB004M25MZL\_4P-T)  
 modify Debug port note(GPIO19 PH +3VS GPIO28 PH +3VALW\_PCH)  
 R667,R666 change BOM structure to @(XDP CLK source)  
 change SW4,SW5 BOM structure to @ (debug PWRBTN)  
 change R432,R435,R437 from 1K\_0402\_5% to 300\_0402\_5%(orange LED resistor)  
 change USB3.0 schmetic BOM structure back to USB3@  
 C746,C750 change from SF000001500 to SF000001580  
 D4,D5 change from SC5H491D010(S SCH DIO CH491DPT SOT-23) to SC500002000(S SCH DIO RB491D SOT-23 PANJIT)  
 Q29,Q33,Q36 change from SB934130020(S TR A034113L 1P SOT23-3) to SB000006R10(S TR A034119L 1P SOT23-3)

0928:  
 DEL R468  
 JMINI1.24 change power source from +3VS to +3VS\_WLAN  
 DEL R613  
 JMINI2.24change power source from +3VS to +3VS\_WWAN  
 DEL R352  
 change power source from +XDPWR\_SDPWR\_MSPWR to +CARDPWR  
 Q21 change from SB324110080(2SC2411K) to SB039040020(MMBT3904)  
 Change JUSB2 footprint to "SUYIN\_020173GB004M25MZL\_4P"  
 ADD R613 1M PD to GND(HDA\_SYNC\_PCH\_R)  
 ADD SLP\_A# at U37.G10 test point(for DFT request)  
 ADD JTAG\_TDI at U30.AN23 test point(for DFT request)  
 ADD JTAG\_TDO at U30.AM24 test point(for DFT request)  
 JREAD1 change conn from TAITW\_R013-P12-HM\_44P\_NR to TAITW\_R013-P17-HM\_40P\_NR

0929:  
 DEL Rechargeable RTC schematic D21,R425,C551

0930:  
 R534,R540 change from 100\_0402\_1% to 1K\_0402\_5%(SD028100180)(DGL1.5 change save cost)  
 C744,C745 change from 18P\_0402\_50V8J to 27P\_0402\_50V8J(SE071270J80)(25Mhz Crystal modify)  
 R357,R358,R330,R331,R345,R346,R387,R393,R292 change BOM structure to @ (10K\_0402\_5%)PD to GND(DGL1.5 unuse CLK NC)  
 R666,R667 change BOM structure to @(XDP unuse)  
 R573,R575,R571,R572,R562,R564,R567,R570 DEL option 499\_0402\_1% leave 680\_0402\_5%  
 R318,R332 change from 0ohm to 22\_0402\_5%(SD028220A80)  
 C448,C483 change to 4.7P\_0402\_50V8J(SE07147AC80)  
 L47 change to 67ohm common mode choke CHENG HANN WCM2012F2SF-670T04(SM070000S80)  
 -----

1025:  
 R370,R413 change from SD028100380(100K\_0402\_5%) to SD028200380(200K\_0402\_5%)  
 PCH\_GPIO1 change net to WL\_EN#  
 LVDS  
 Add +5VS (Pin34) & USB20\_N4/P4 (Pin35, 36)  
 change EDP\_HPD to Pin18  
 PCH side add USB20\_N4/P4 (Pin35, 36)

For eDP interface AUX channel, please request Layout routing as differential signal to follow eDP Layout Guide.  
 (VGA\_LCD\_CLK & VGA\_LCD\_DATA / I2CC\_SCL & I2CC\_SDA)

DEL DDR DM  
 R50,R58,R59,R48,R56,R51,R60,R49 DIMMA  
 R39,R52,R44,R43,R46,R38,R45,R40 DIMMA  
 R77,R73,R109,R112,R180,R181,R192,R206 DIMMB  
 R64,R83,R108,R115,R179,R183,R189,R208 DIMMB

1026:  
 C604,C591 change from SGA00004200(470 4.5mohm)to SGA00003N00(470 9mohm)  
 Pop R257(SD028100380 100K\_0402\_5%),R622(SD028820180 8.2K\_0402\_5%) Board ID  
 R443 change from 100K\_0402\_5% to 10K\_0402\_5% (SD028100280)

remove R471,R622(JMINI1,JMINI2 Pin42 0ohm series resistor)  
 J1,J2 change location to J6,J7  
 remove R222 0ohm\_0402 (H\_CUPWRGRD\_R)  
 remove R423,0ohm\_0402 (MINI1\_CLKREQ#\_R)  
 remove R392 0ohm\_0402 (LAN\_CLKREQ#\_R)  
 remove R685 0ohm\_0402 (MINI2\_CLKREQ#\_R)  
 remove R655 0ohm\_0402 (WAKE#)  
 remove R636 0ohm\_0402 (PCH\_RSMRST#)  
 remove R377 0ohm\_0402 (SDS\_PWR\_DM\_ACK)  
 remove R339 0ohm\_0402 (PBTN\_OUT#)  
 remove R359 0ohm\_0402 (DGPU\_HOLD\_RST#)  
 remove R16 0ohm\_0402 (BKOPF#)  
 remove R448 0ohm\_0402 (VGA\_EDP\_DET)  
 remove R533 0ohm\_0402 (VGA\_HDMI\_DET)  
 remove R627 0ohm\_0603 (+SP1\_VCC)

ADD R39 0ohm\_0402 LOCAL\_DIM  
 ADD R38 0ohm\_0402 COLOR\_ENG\_EN

C242,C653,C332,C354,C678 change footprint to C\_X(2pin)

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