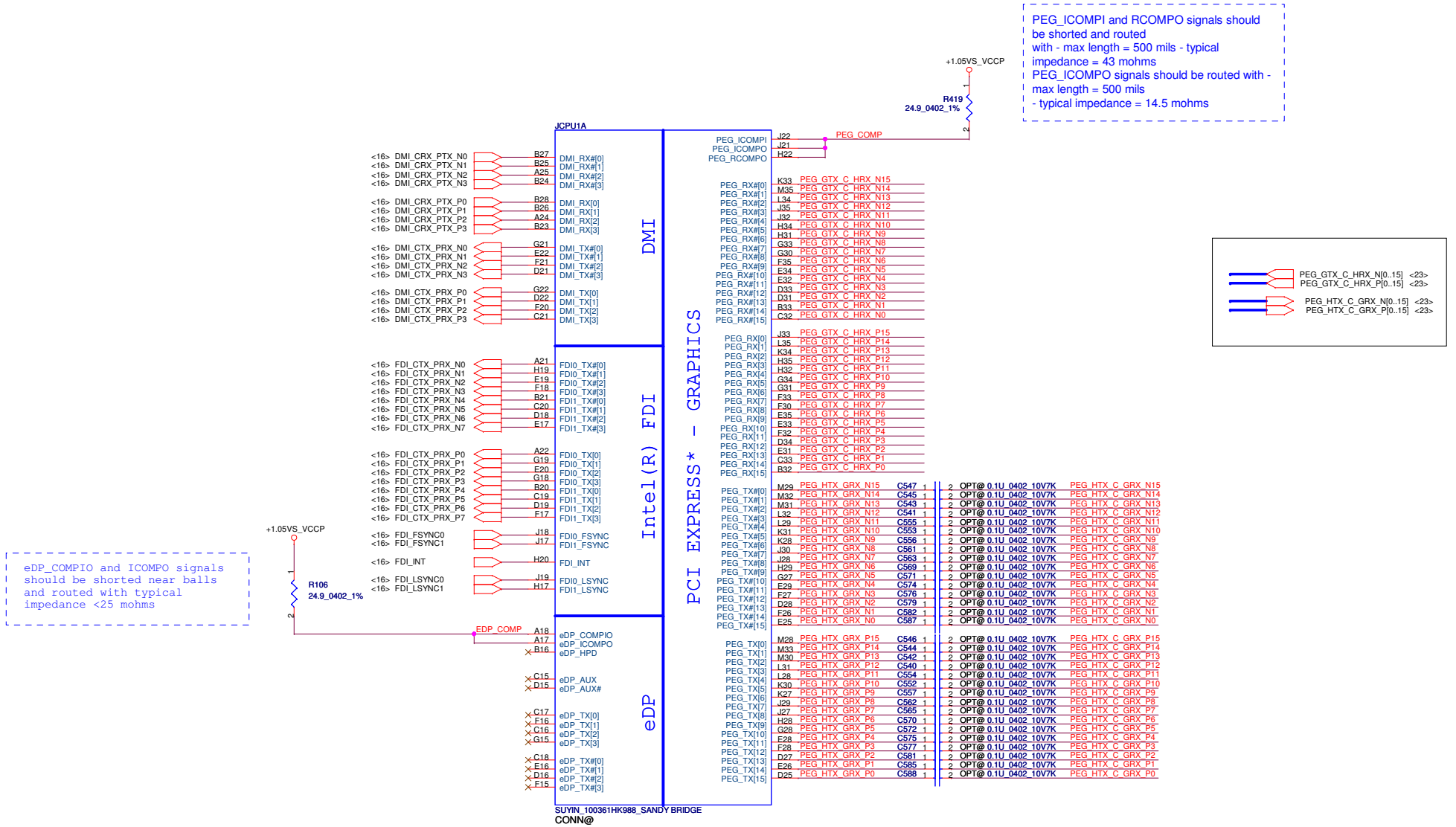


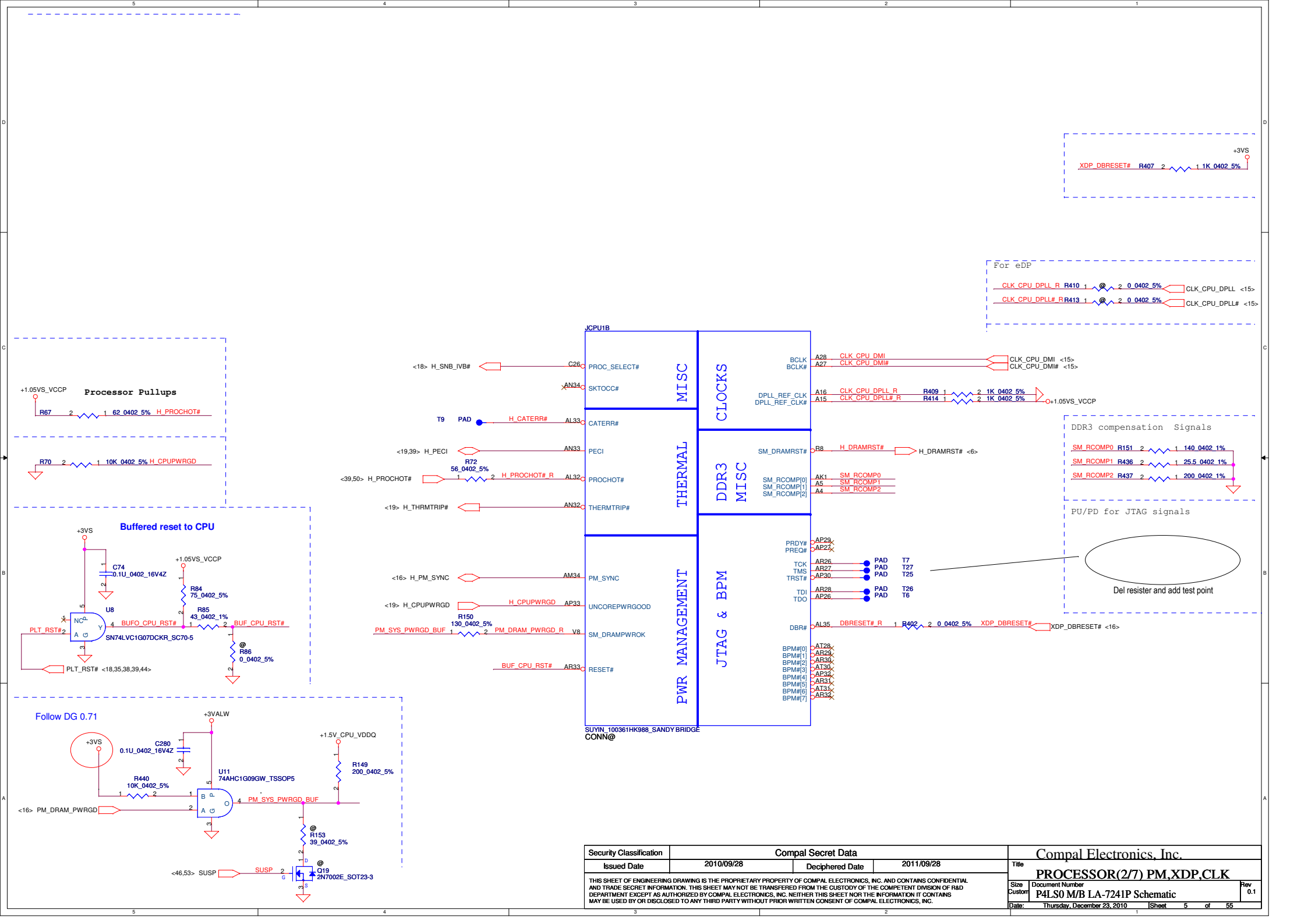
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 4 of 55



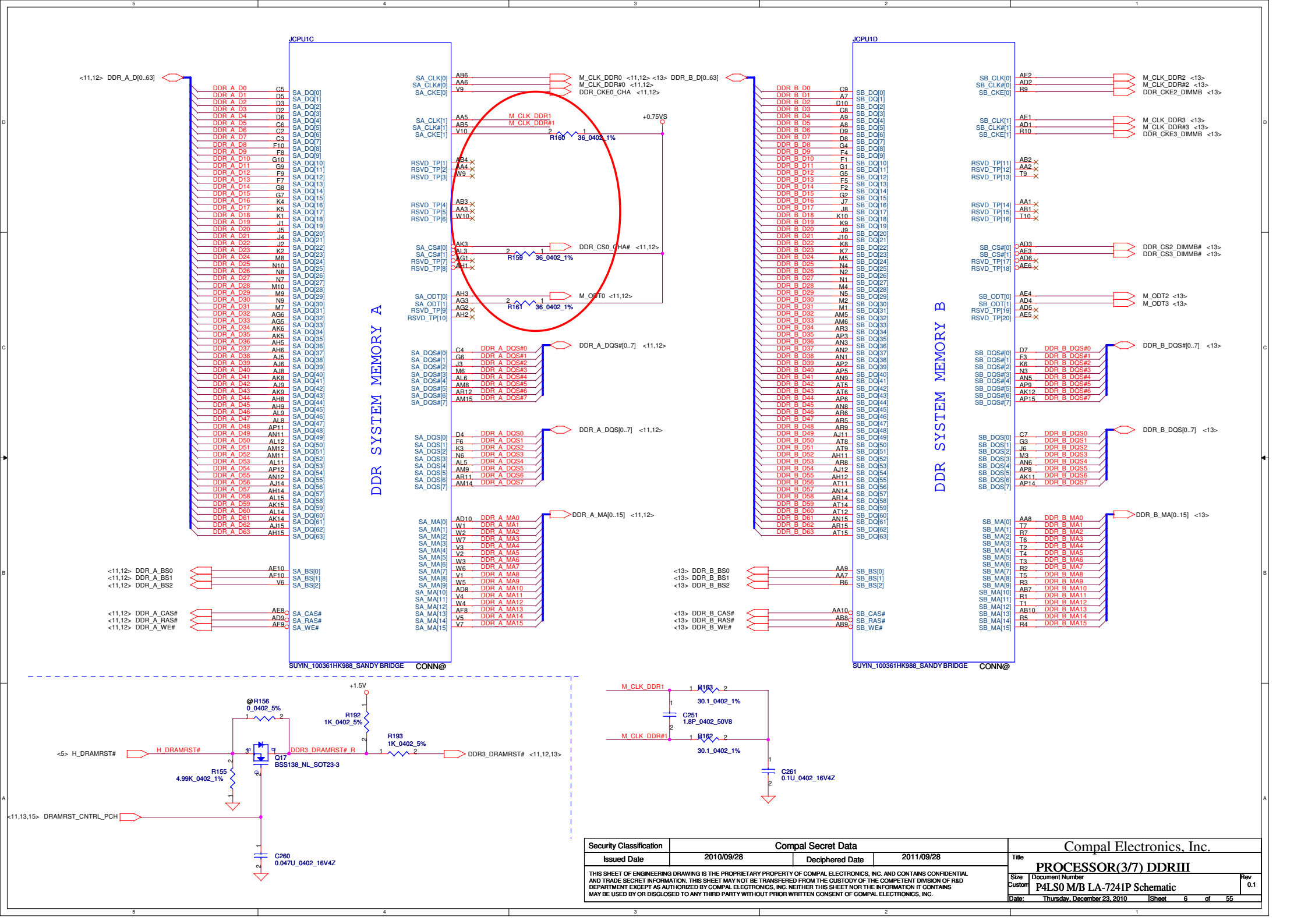
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 5 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

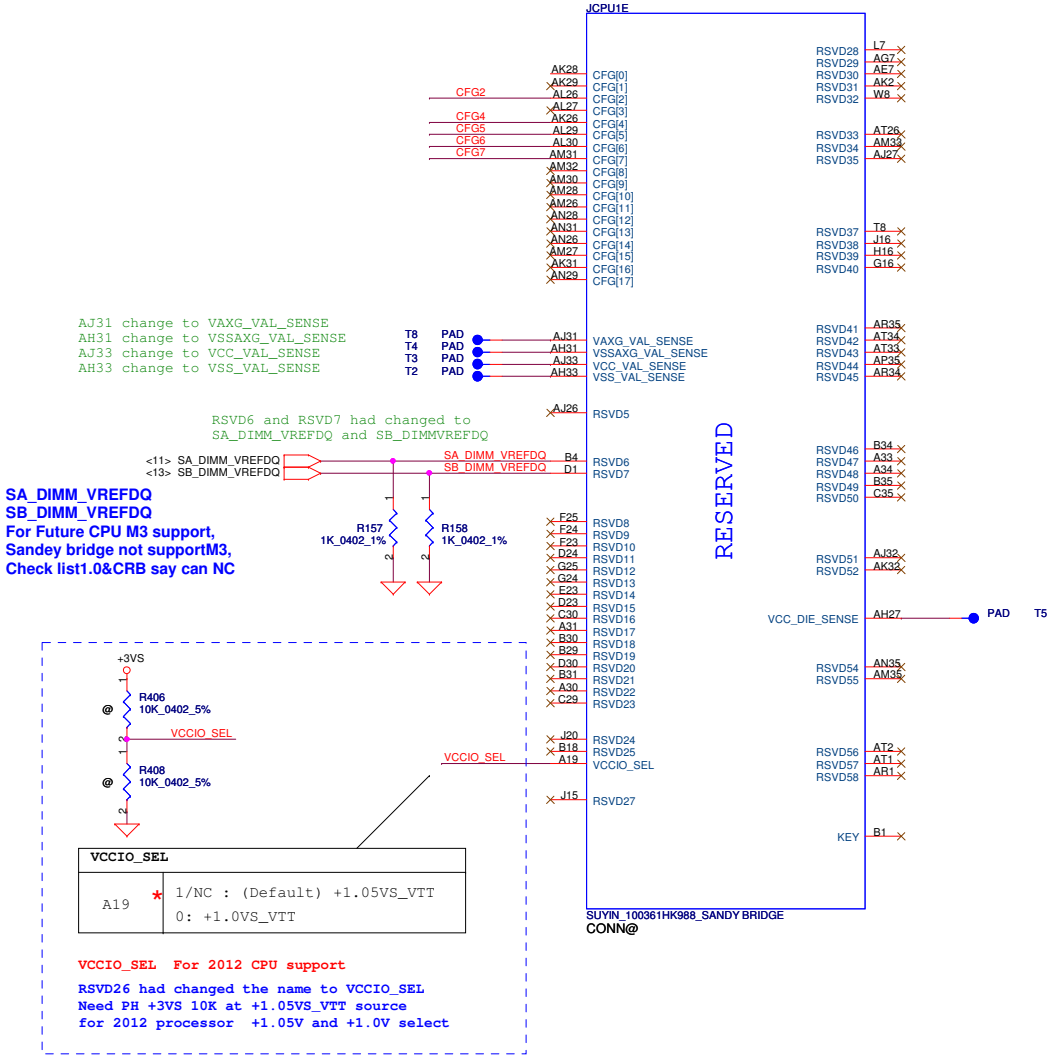
Compal Electronics, Inc.

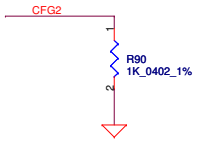
Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

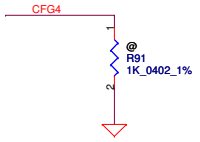
Date: Thursday, December 23, 2010 Sheet 6 of 55

CFG Straps for Processor

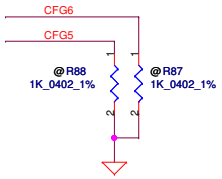




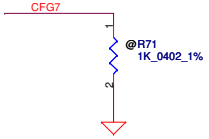
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 7 of 55

POWER

SV type CPU

QC 94A
DC 53A

JCPU1F

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

8.5A

+CPU_CORE

+1.05VS_VCCP

Cap quantity follow 43890_HR_CHKLST_Rev07

Place the PU resistors close to VR

Place the PU resistors close to CPU

SUYIN_100361HK988_SANDY BRIDGE_CONN@

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

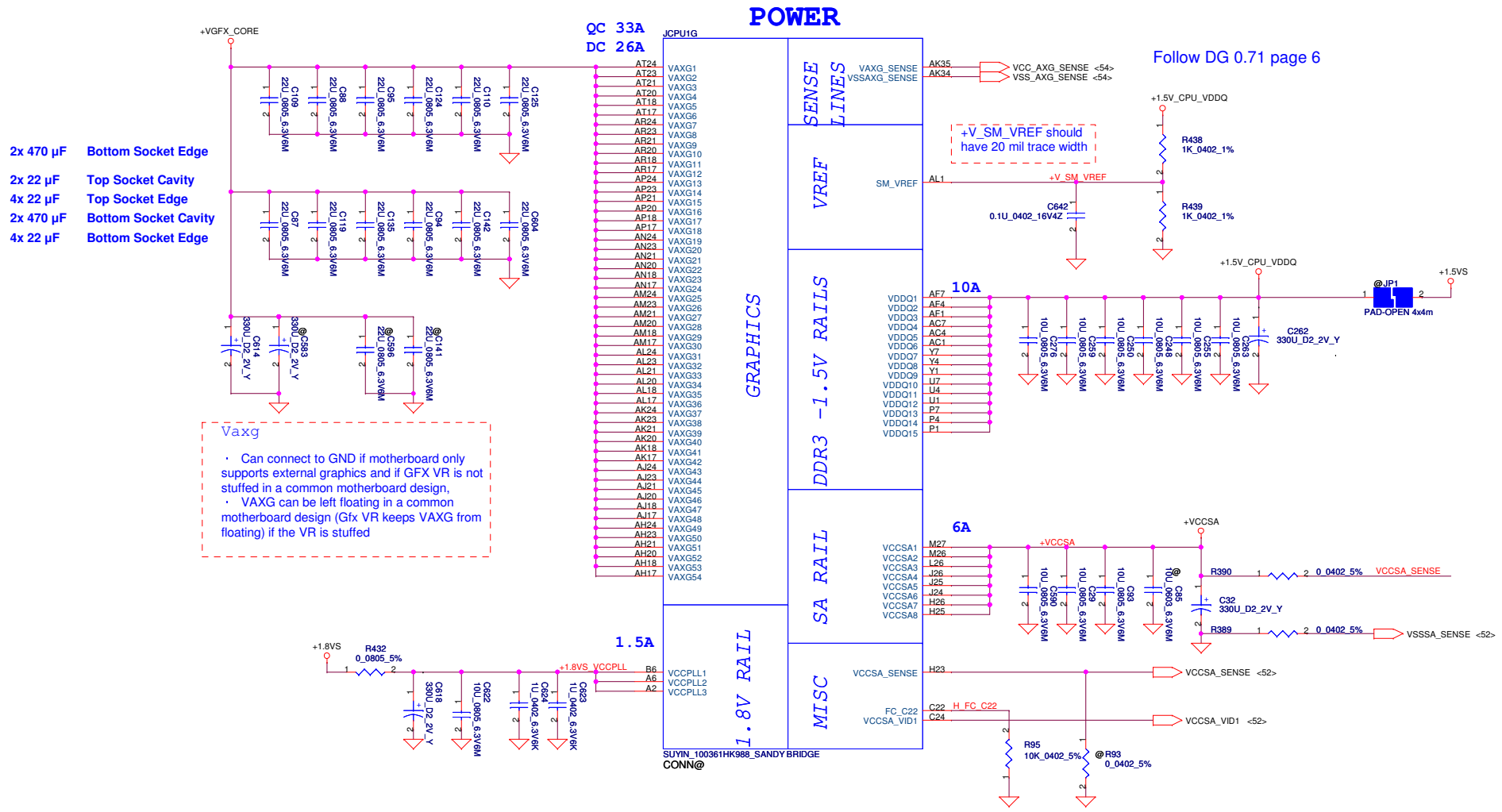
Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

Date: Thursday, December 23, 2010 | Sheet 8 of 55

POWER



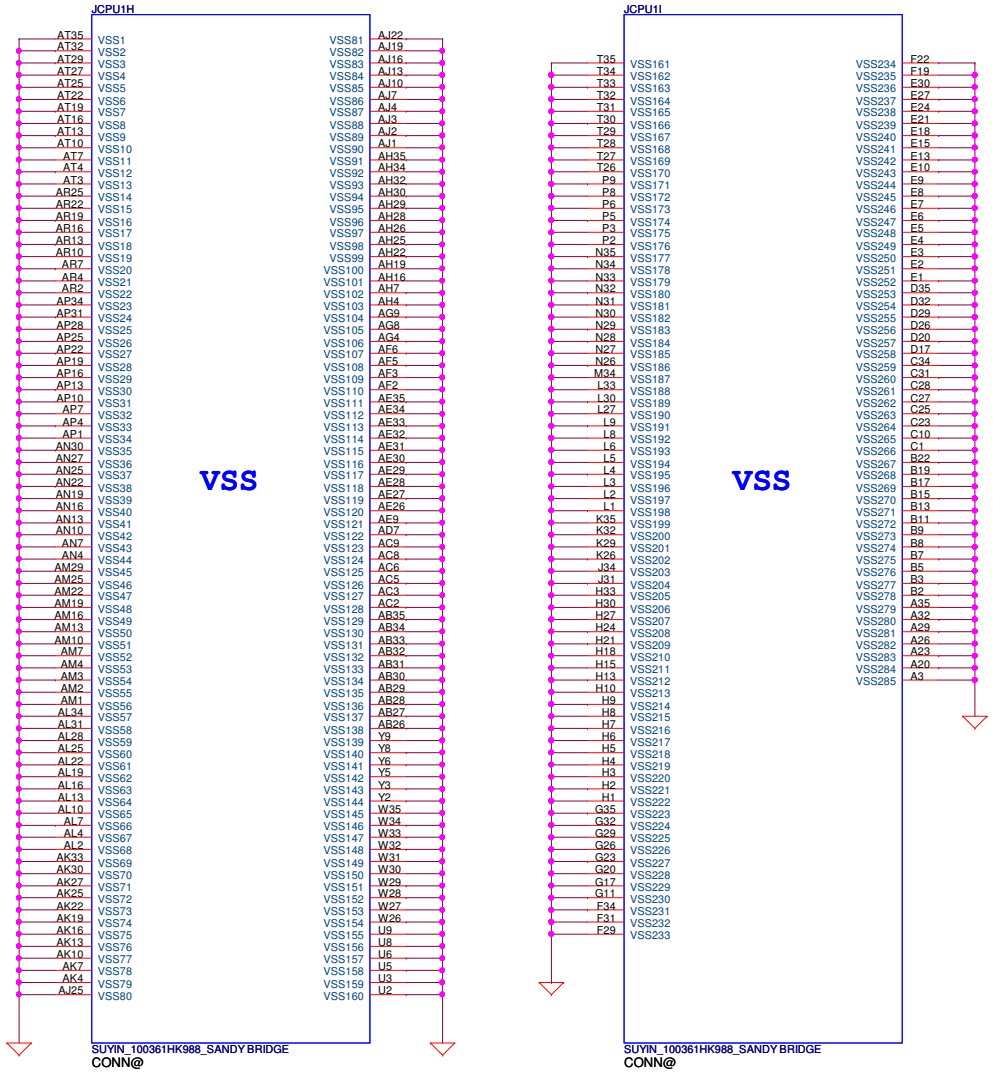
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 9 of 55



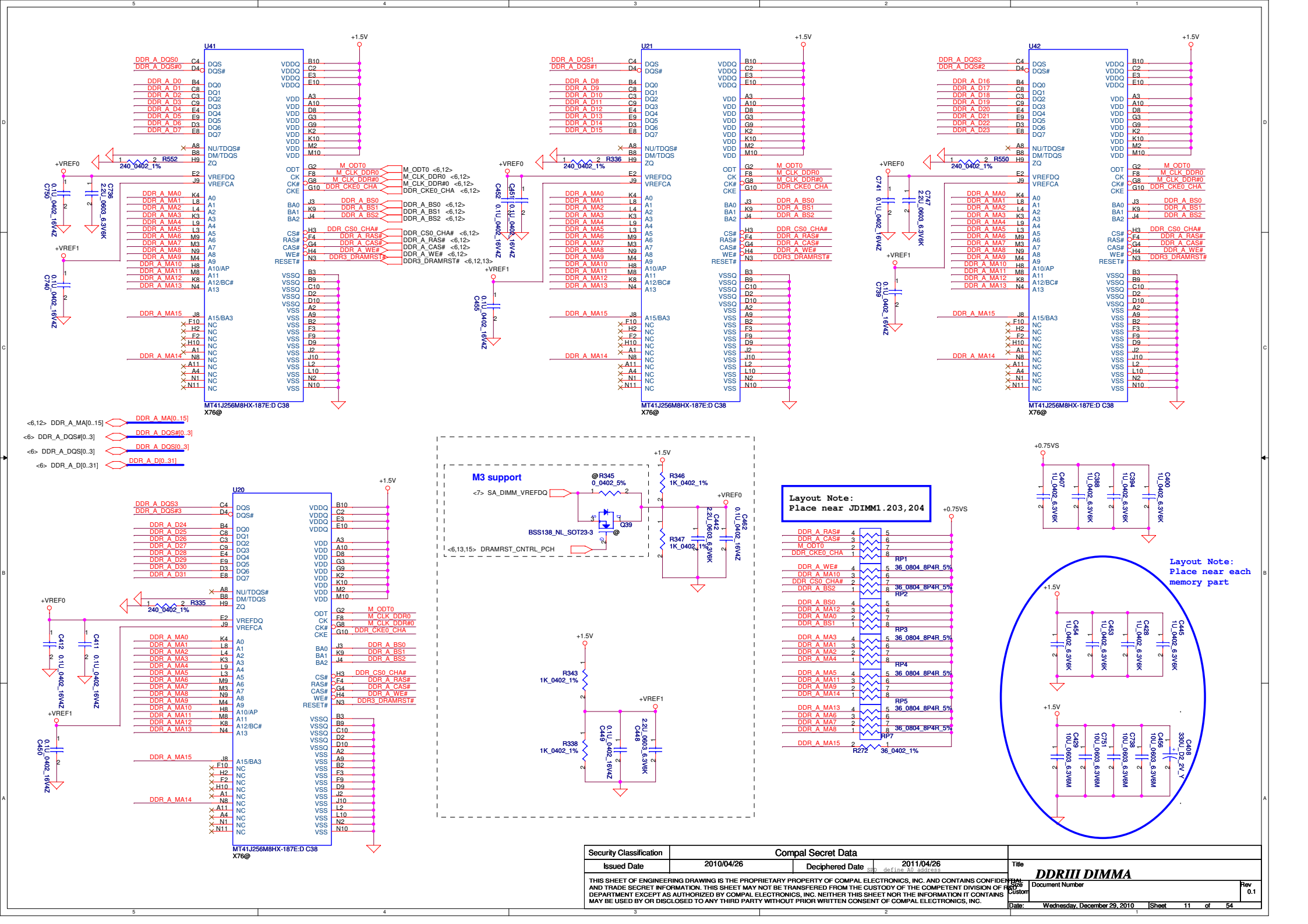
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Friday, November 19, 2010 Sheet 10 of 55

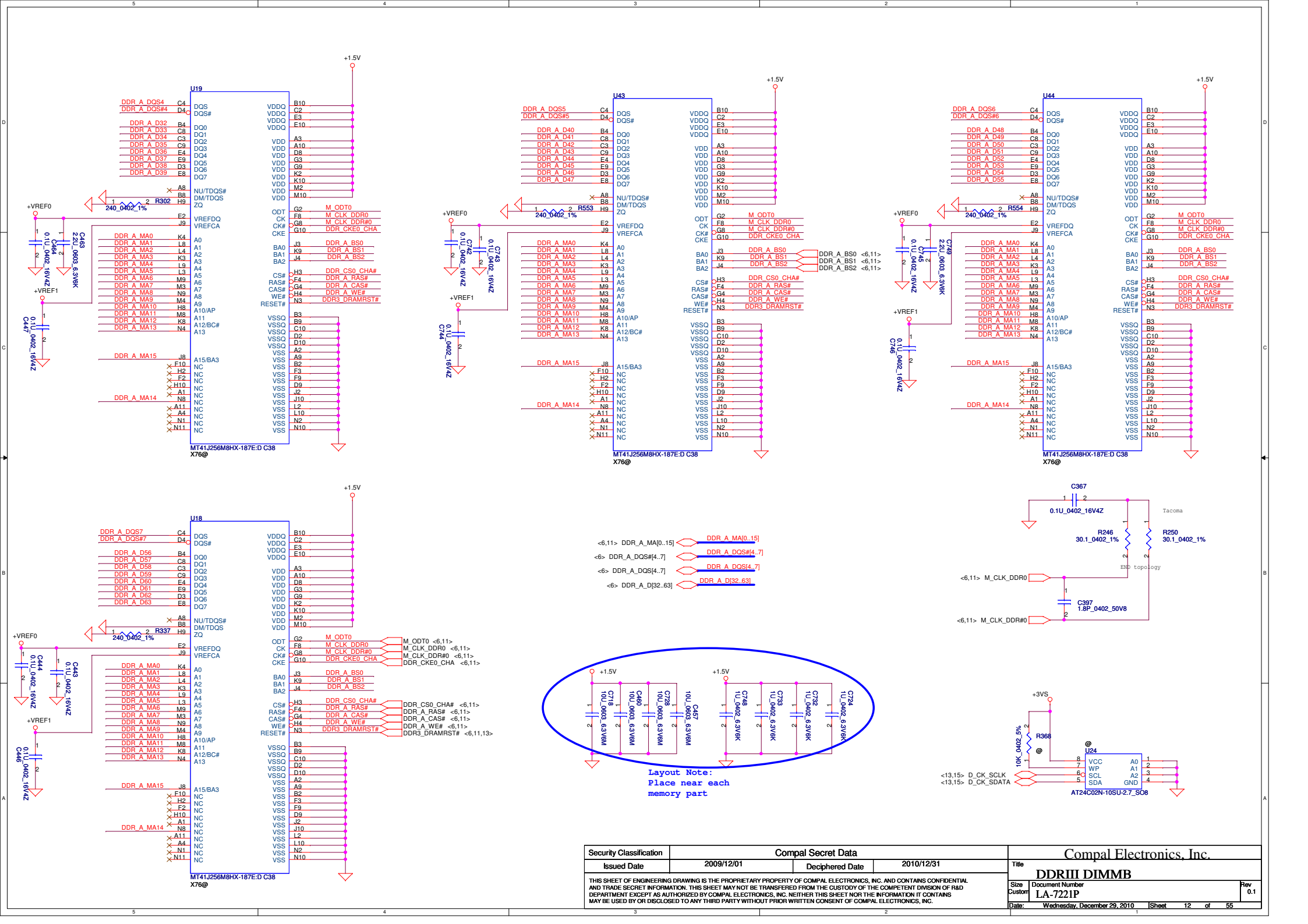


Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2011/04/26

Title: **DDRIII DIMMA**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, December 29, 2010 | Sheet 11 of 54



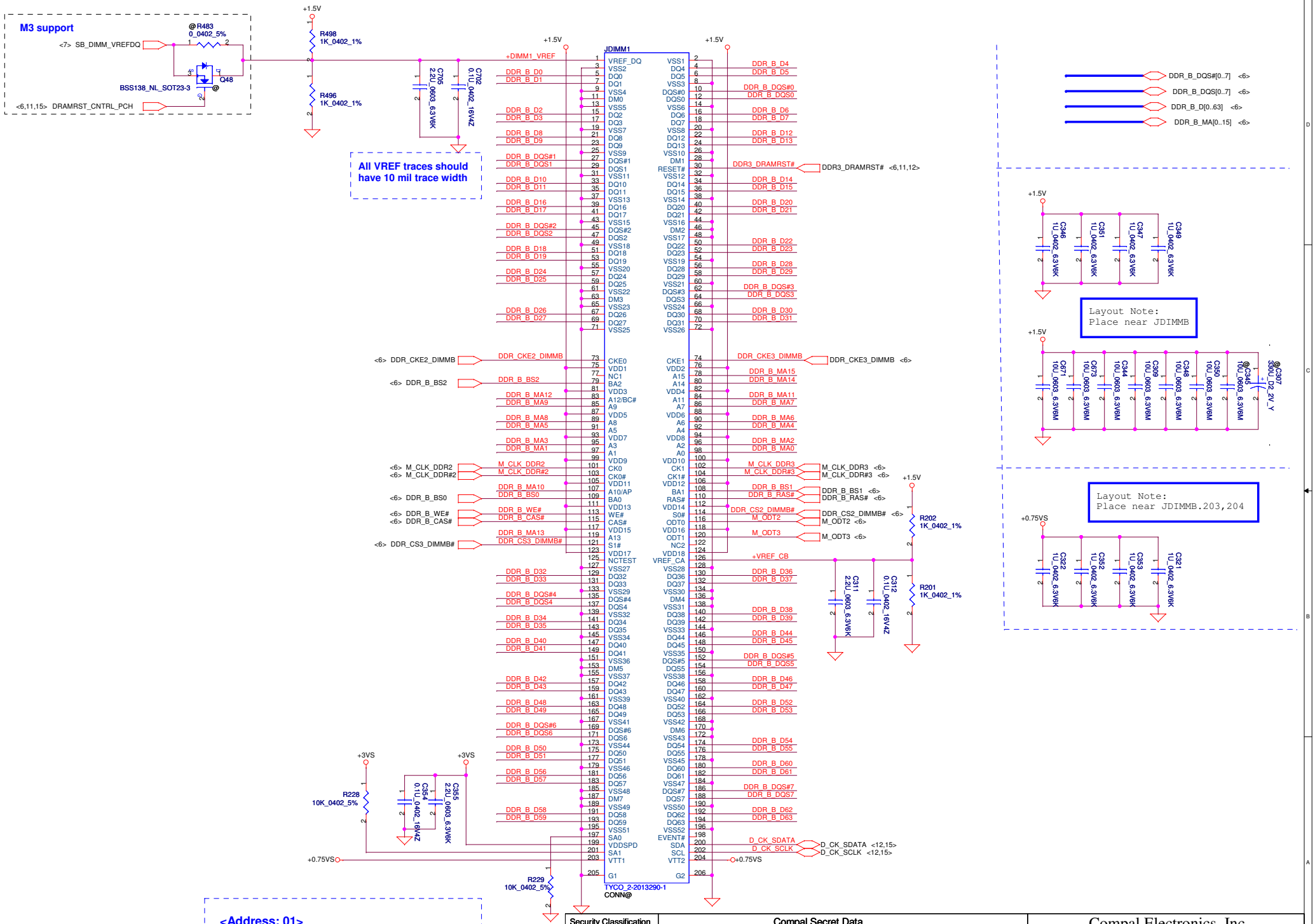
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: DDRIII DIMMB

Size	Document Number	Rev
Custom	LA-7221P	0.1

Date: Wednesday, December 29, 2010 Sheet 12 of 55



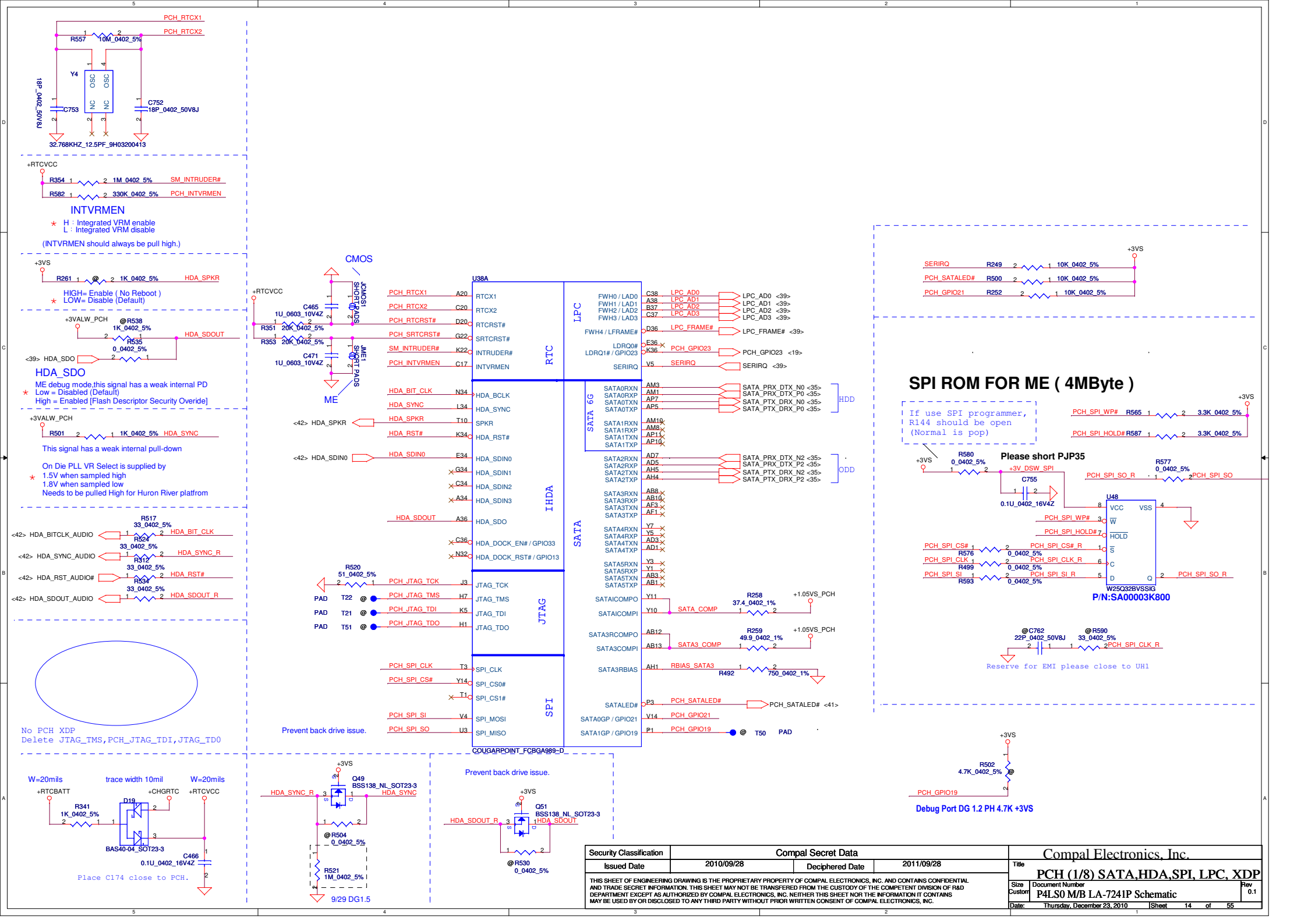
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: DDRIII DIMMB

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 13 of 55



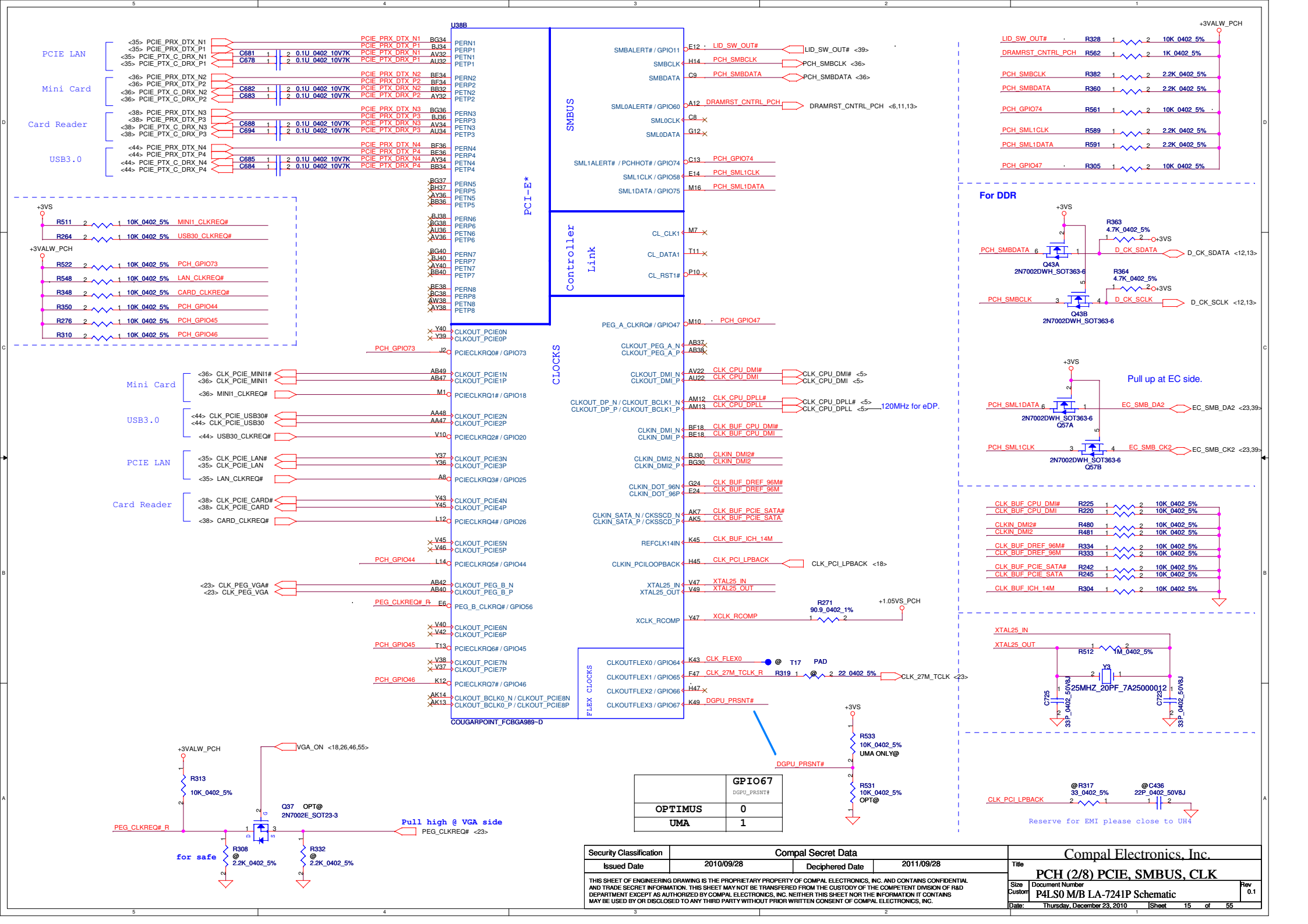
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 14 of 55



Security Classification	Compal Secret Data
Issued Date	2010/09/28
Deciphered Date	2011/09/28

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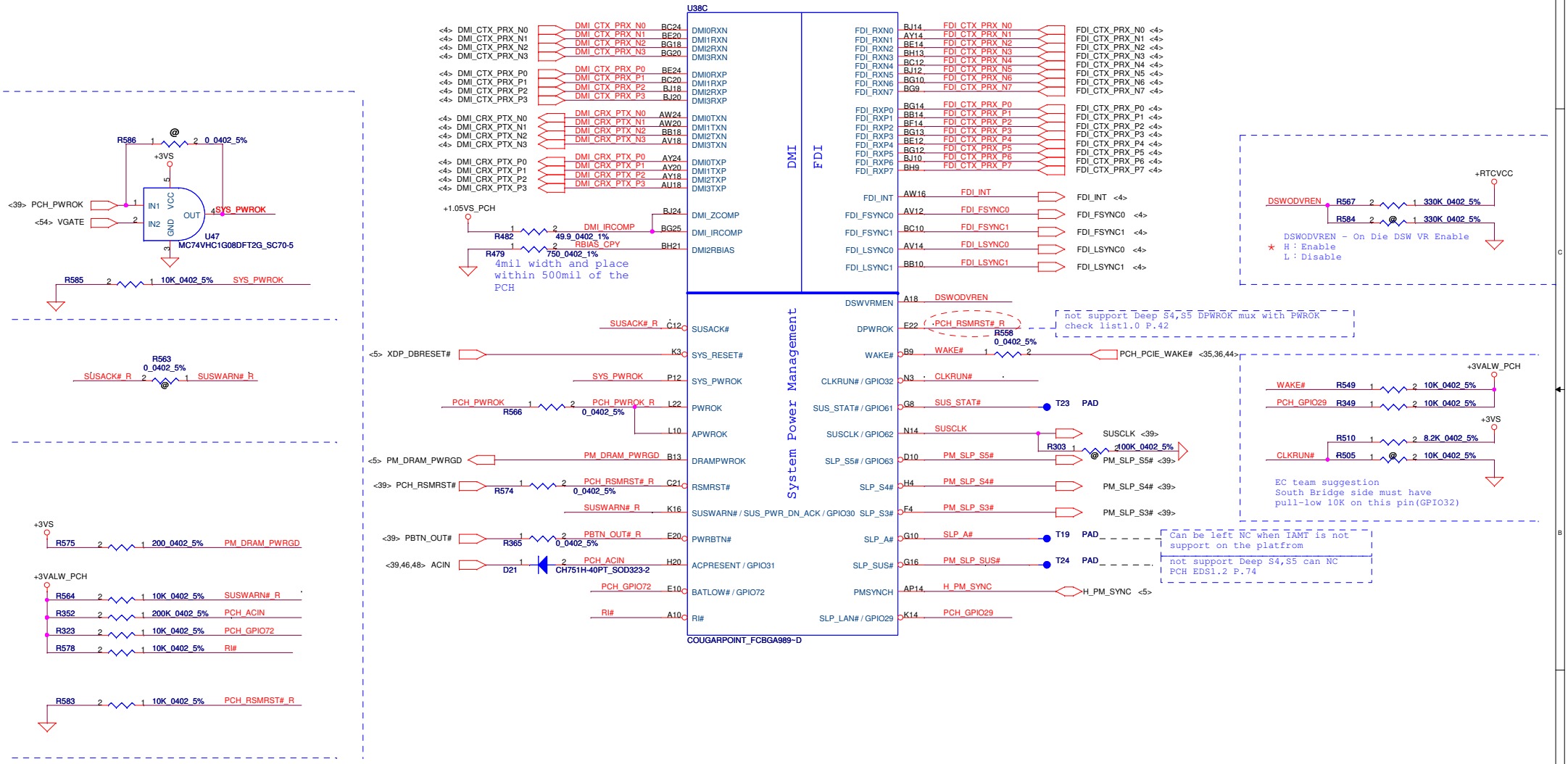
Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 15 of 55



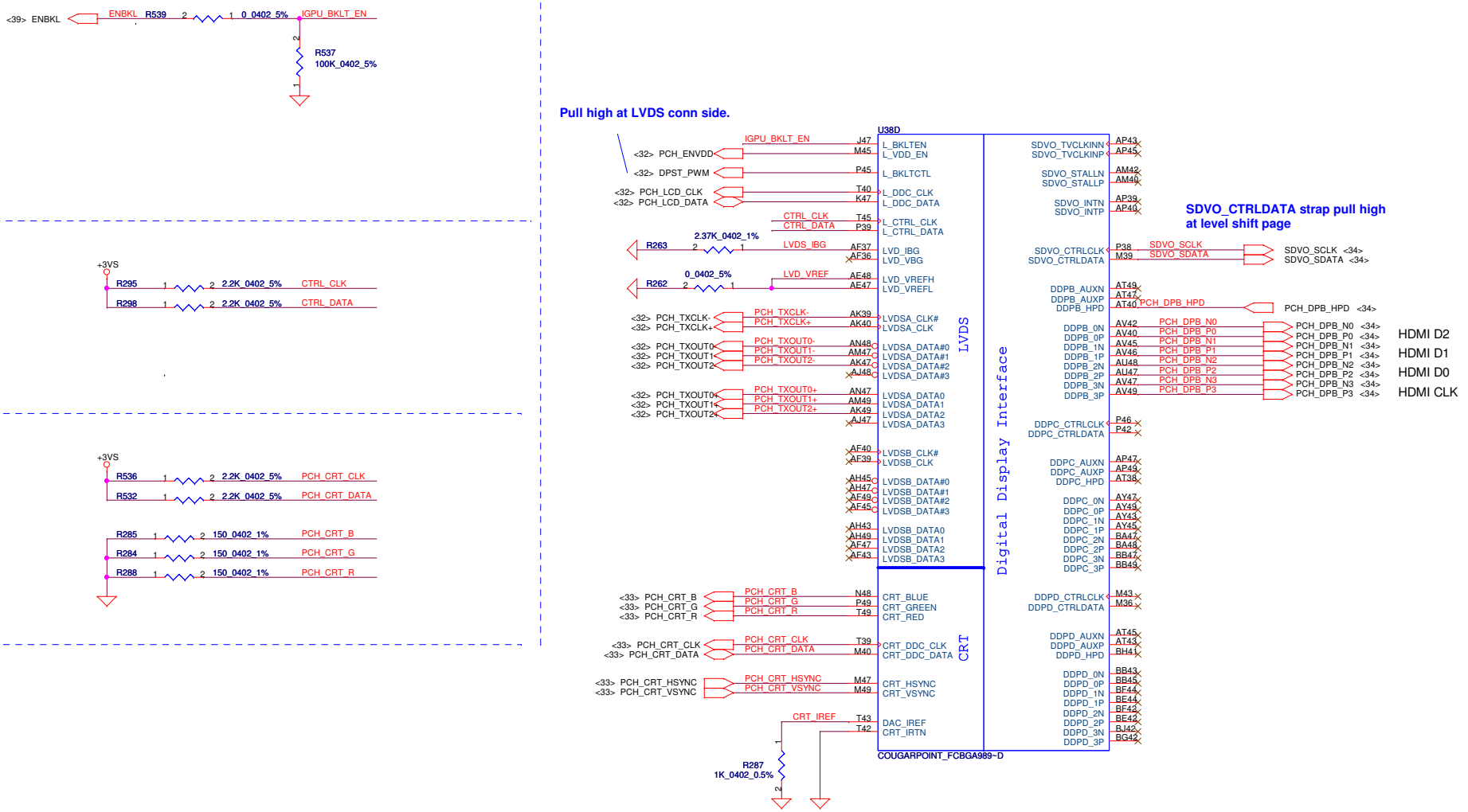
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 16 of 55



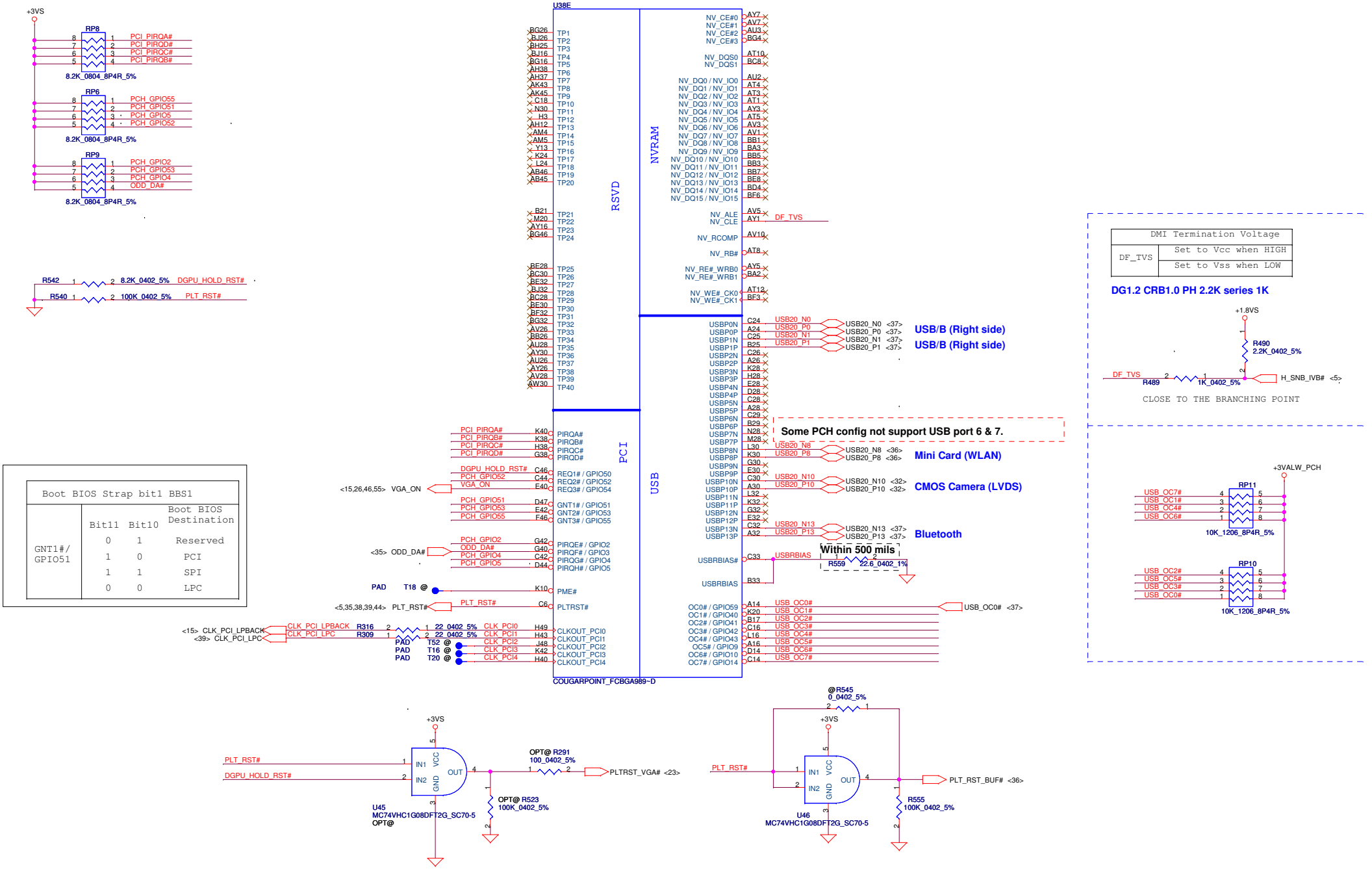
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 17 of 55



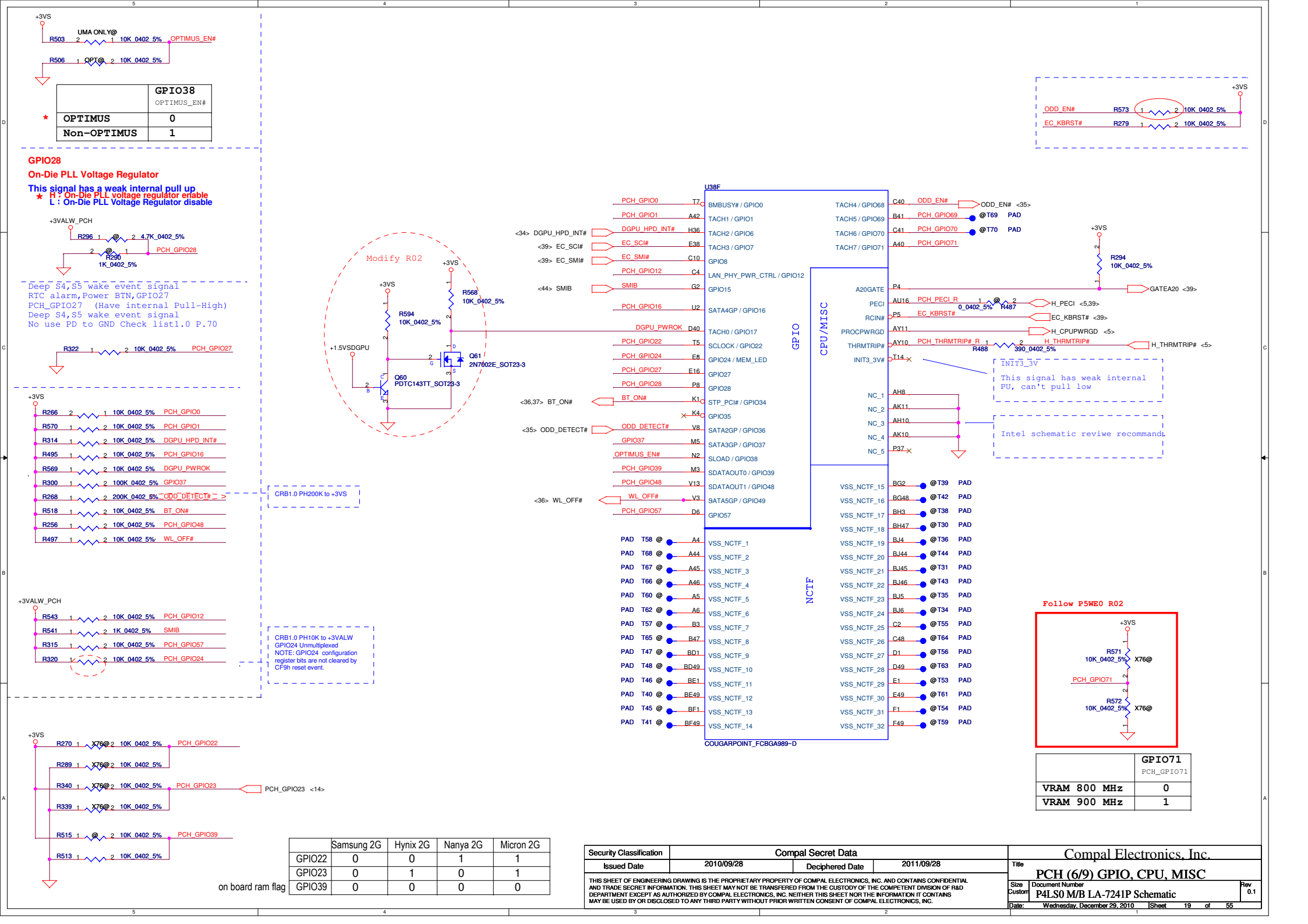
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

Date: Thursday, December 23, 2010 | Sheet 18 of 55


+3VS
UMA ONLY@
R503 2 1 10K_0402_5% OPTIMUS_EN#
R506 1 OPT@ 2 10K_0402_5%
GPIO38
OPTIMUS_EN#
* OPTIMUS 0
Non-OPTIMUS 1
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable
+3VALW_PCH
R296 1 @ 2 4.7K_0402_5%
2 @ 1 R290 1K_0402_5%
PCH_GPIO28
Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70
R322 1 2 10K_0402_5% PCH_GPIO27
+3VS
R266 10K_0402_5% PCH_GPIO0
R570 10K_0402_5% PCH_GPIO1
R314 10K_0402_5% DGPU_HPD_INT#
R495 10K_0402_5% PCH_GPIO16
R569 10K_0402_5% DGPU_PWROK
R300 100K_0402_5% GPIO37
R268 200K_0402_5% ODD_DETECT#
R518 10K_0402_5% BT_ON#
R256 10K_0402_5% PCH_GPIO48
R497 10K_0402_5% WL_OFF#
CRB1.0 PH200K to +3VS
+3VALW_PCH
R543 10K_0402_5% PCH_GPIO12
R541 1K_0402_5% SMIB
R315 10K_0402_5% PCH_GPIO57
R320 10K_0402_5% PCH_GPIO24
CRB1.0 PH10K to +3VALW
GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
+3VS
R270 X76@ 10K_0402_5% PCH_GPIO22
R289 X76@ 10K_0402_5%
R340 X76@ 10K_0402_5% PCH_GPIO23
R339 X76@ 10K_0402_5%
R515 @ 10K_0402_5% PCH_GPIO39
R513 10K_0402_5%
PCH_GPIO23 <14>
Modify R02
+3VS
R568 10K_0402_5%
R594 10K_0402_5%
+1.5VSDGPU
Q61 2N7002E_SOT23-3
Q60 PDTC143TT_SOT23-3
U38F
PCH_GPIO0 T7 BMBUSY# / GPIO0
PCH_GPIO1 A42 TACH1 / GPIO1
<34> DGPU_HPD_INT# DGPU_HPD_INT# H36 TACH2 / GPIO6
<39> EC_SCI# EC_SCI# E38 TACH3 / GPIO7
<39> EC_SMI# EC_SMI# C10 GPIO8
PCH_GPIO12 C4 LAN_PHY_PWR_CTRL / GPIO12
<44> SMIB SMIB G2 GPIO15
PCH_GPIO16 U2 SATA4GP / GPIO16
DGPU_PWROK D40 TACH0 / GPIO17
PCH_GPIO22 T5 SCLOCK / GPIO22
PCH_GPIO24 E8 GPIO24 / MEM_LED
PCH_GPIO27 E16 GPIO27
PCH_GPIO28 P8 GPIO28
<36,37> BT_ON# BT_ON# K1 STP_PCI# / GPIO34
K4 GPIO35
<35> ODD_DETECT# ODD_DETECT# V8 SATA2GP / GPIO36
GPIO37 M5 SATA3GP / GPIO37
OPTIMUS_EN# N2 SLOAD / GPIO38
PCH_GPIO39 M3 SDATAOUT0 / GPIO39
PCH_GPIO48 V13 SDATAOUT1 / GPIO48
<36> WL_OFF# WL_OFF# V3 SATA5GP / GPIO49
PCH_GPIO57 D6 GPIO57
PAD T58 @ A4 VSS_NCTF_1
PAD T68 @ A44 VSS_NCTF_2
PAD T67 @ A45 VSS_NCTF_3
PAD T66 @ A46 VSS_NCTF_4
PAD T60 @ A5 VSS_NCTF_5
PAD T62 @ A6 VSS_NCTF_6
PAD T57 @ B3 VSS_NCTF_7
PAD T65 @ B47 VSS_NCTF_8
PAD T47 @ BD1 VSS_NCTF_9
PAD T48 @ BD49 VSS_NCTF_10
PAD T46 @ BE1 VSS_NCTF_11
PAD T40 @ BE49 VSS_NCTF_12
PAD T45 @ BF1 VSS_NCTF_13
PAD T41 @ BF49 VSS_NCTF_14
COUGARPOINT_FCBGA989~D
GPIO
CPU/MISC
NCTF
TACH4 / GPIO68 C40 ODD_EN# ODD_EN# <35>
TACH5 / GPIO69 B41 PCH_GPIO69 @T69 PAD
TACH6 / GPIO70 C41 PCH_GPIO70 @T70 PAD
TACH7 / GPIO71 A40 PCH_GPIO71
A20GATE P4 GATEA20 <39>
PECI AU16 PCH_PECI_R 0_0402_5% R487 H_PECI <5,39>
RCIN# P5 EC_KBRST# EC_KBRST# <39>
PROCPWRGD AY11 H_CPUPWRGD <5>
THRMTRIP# AY10 PCH_THRMTRIP#_R R488 390_0402_5% H_THRMTRIP# H_THRMTRIP# <5>
INIT3_3V# T14
INIT3_3V
This signal has weak internal PU, can't pull low
NC_1 AH8
NC_2 AK11
NC_3 AH10
NC_4 AK10
NC_5 P37
Intel schematic reviwe recommand.
VSS_NCTF_15 BG2 @T39 PAD
VSS_NCTF_16 BG48 @T42 PAD
VSS_NCTF_17 BH3 @T38 PAD
VSS_NCTF_18 BH47 @T30 PAD
VSS_NCTF_19 BJ4 @T36 PAD
VSS_NCTF_20 BJ44 @T44 PAD
VSS_NCTF_21 BJ45 @T31 PAD
VSS_NCTF_22 BJ46 @T43 PAD
VSS_NCTF_23 BJ5 @T35 PAD
VSS_NCTF_24 BJ6 @T34 PAD
VSS_NCTF_25 C2 @T55 PAD
VSS_NCTF_26 C48 @T64 PAD
VSS_NCTF_27 D1 @T56 PAD
VSS_NCTF_28 D49 @T63 PAD
VSS_NCTF_29 E1 @T53 PAD
VSS_NCTF_30 E49 @T61 PAD
VSS_NCTF_31 F1 @T54 PAD
VSS_NCTF_32 F49 @T59 PAD
+3VS
R294 10K_0402_5%
ODD_EN# R573 10K_0402_5%
EC_KBRST# R279 10K_0402_5%
Follow P5WE0 R02
+3VS
R571 10K_0402_5% X76@
PCH_GPIO71
R572 10K_0402_5% X76@
GPIO71
PCH_GPIO71
VRAM 800 MHz 0
VRAM 900 MHz 1
on board ram flag
Samsung 2G Hynix 2G Nanya 2G Micron 2G
GPIO22 0 0 1 1
GPIO23 0 1 0 1
GPIO39 0 0 0 0
Security Classification Compal Secret Data
Issued Date 2010/09/28 Deciphered Date 2011/09/28
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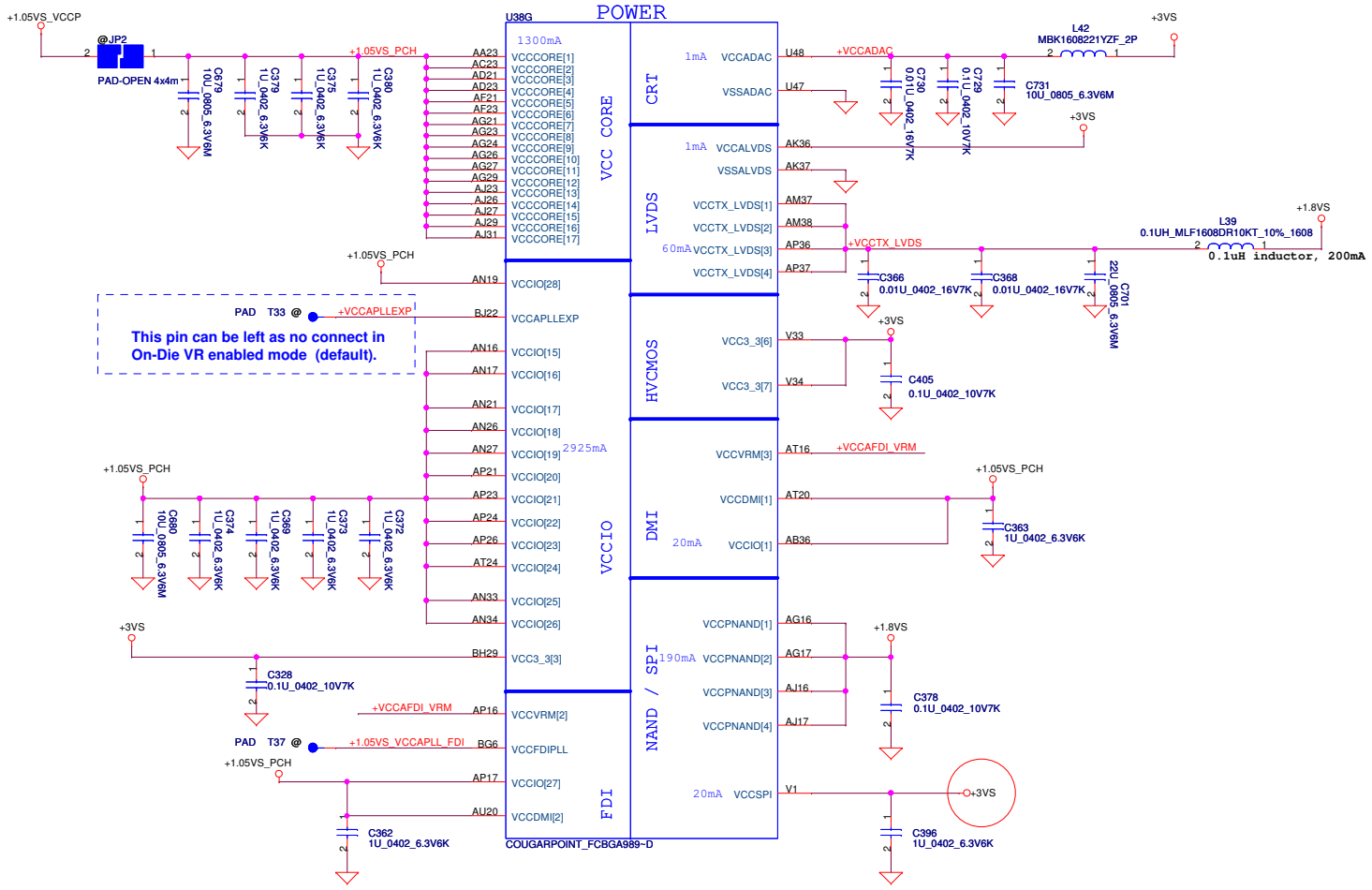
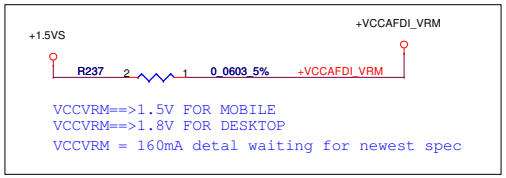
Compal Electronics, Inc.
Title PCH (6/9) GPIO, CPU, MISC
Size Custom Document Number P4LS0 M/B LA-7241P Schematic Rev 0.1
Date: Wednesday, December 29, 2010 Sheet 19 of 55





PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

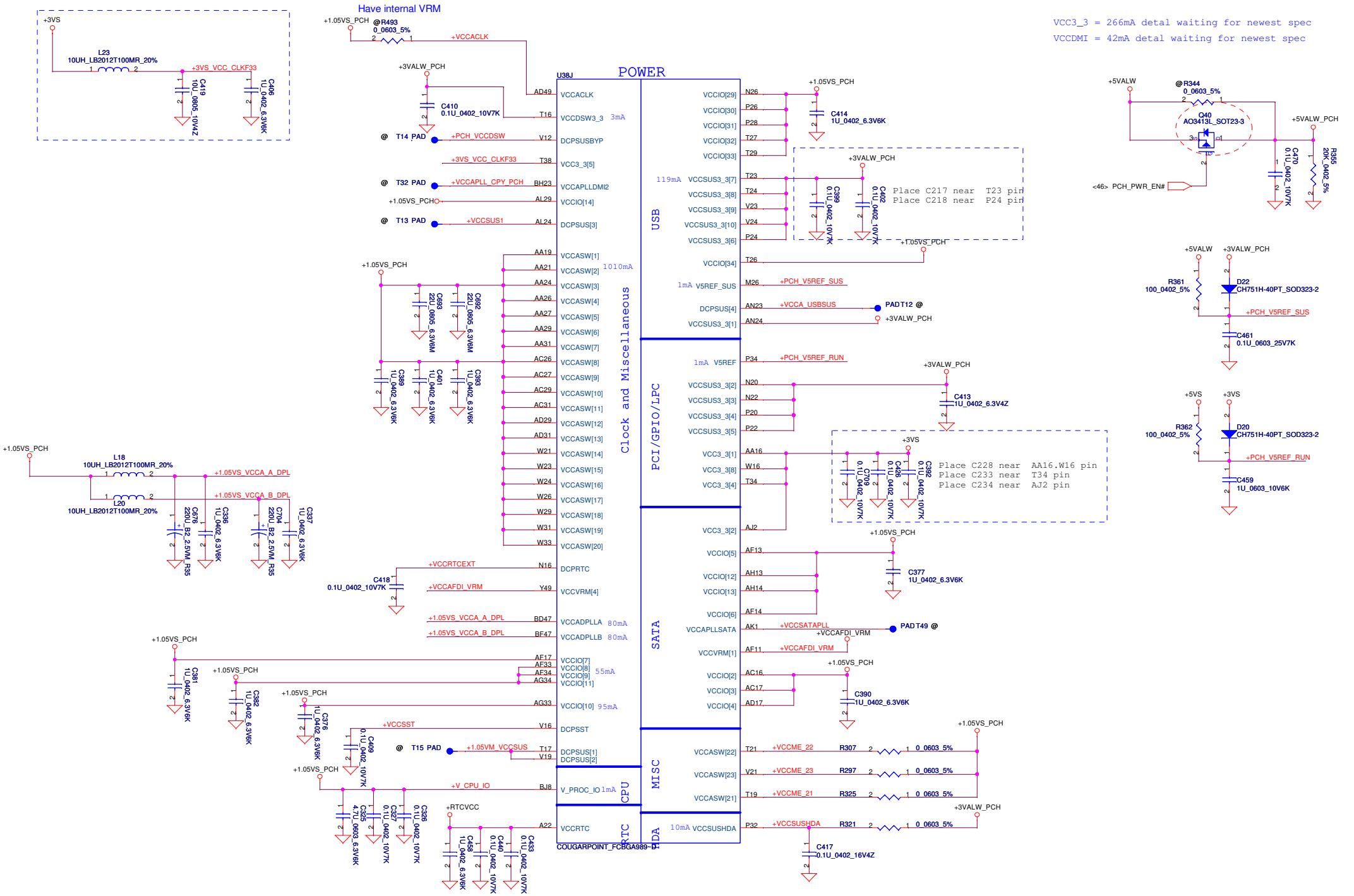
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

Date: Friday, November 19, 2010 | Sheet 20 of 55



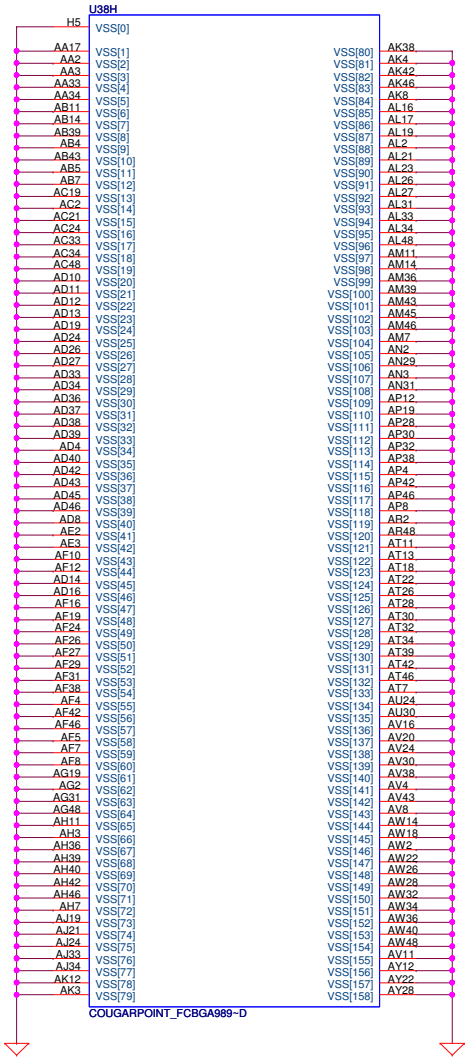
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

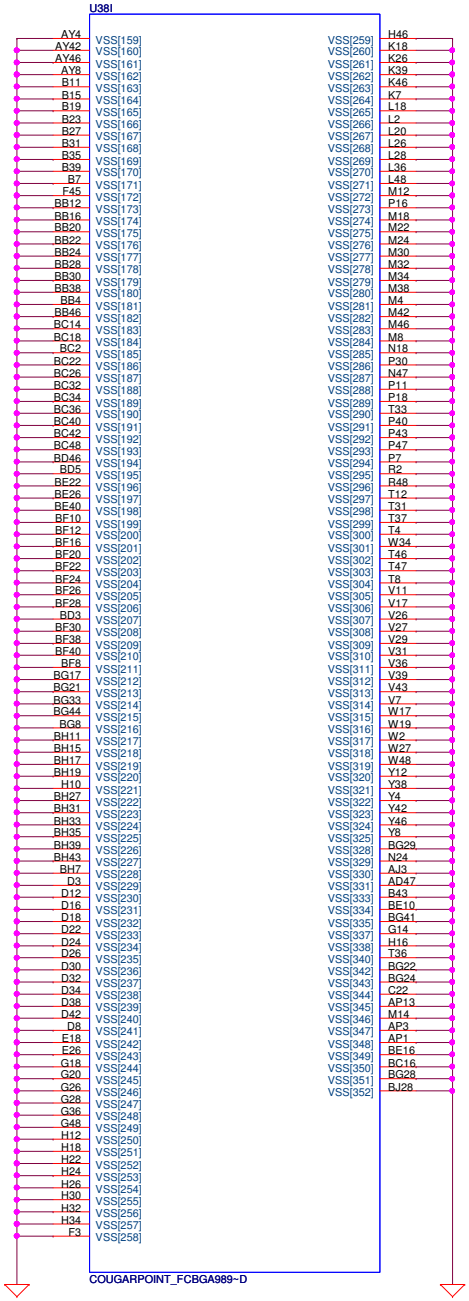
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Thursday, December 23, 2010 Sheet 21 of 55





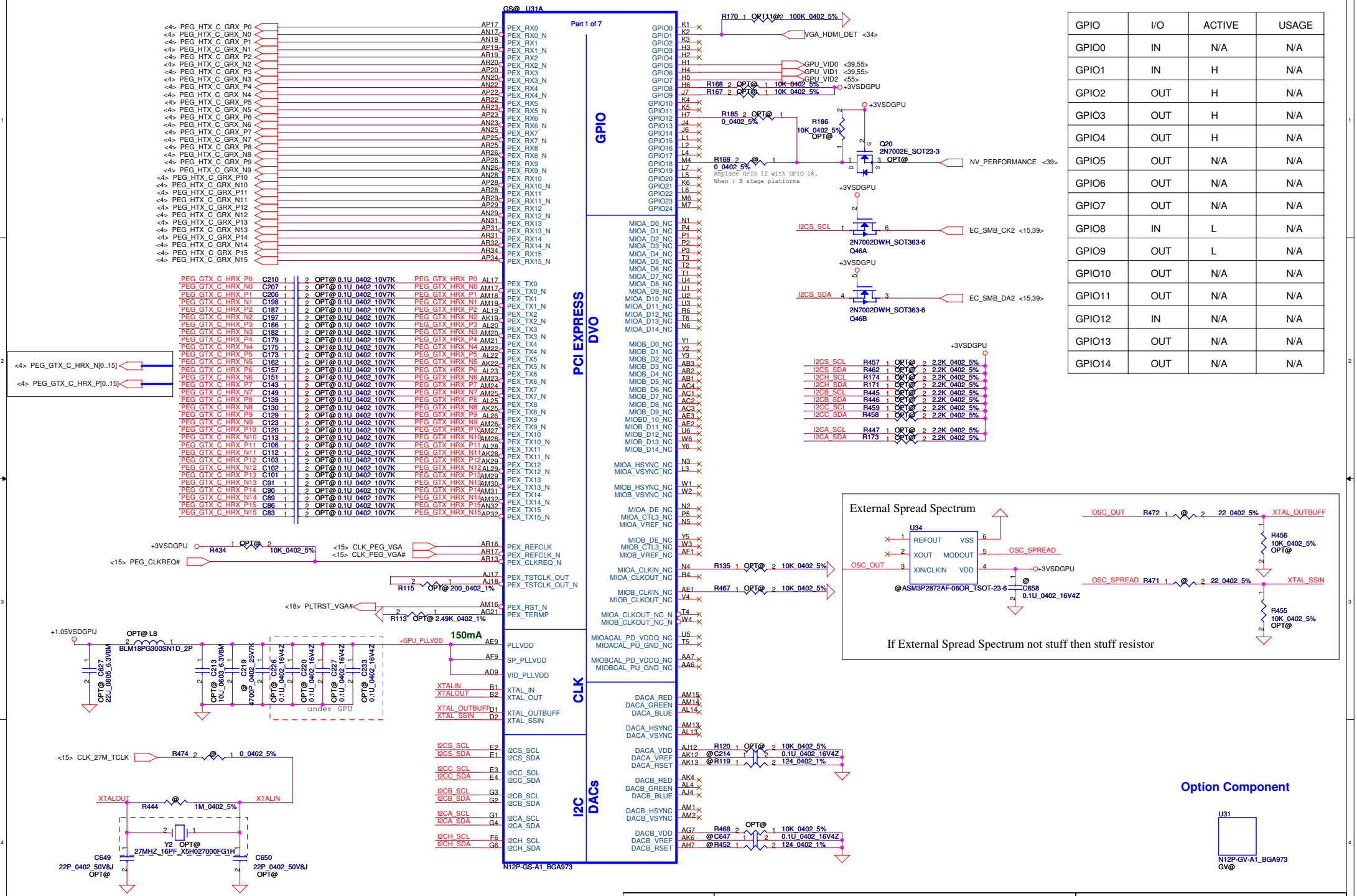
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size	Document Number	Rev
Custom	P4LS0 M/B LA-7241P Schematic	0.1

Date: Friday, November 19, 2010 Sheet 22 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: N11P PEG 1/9

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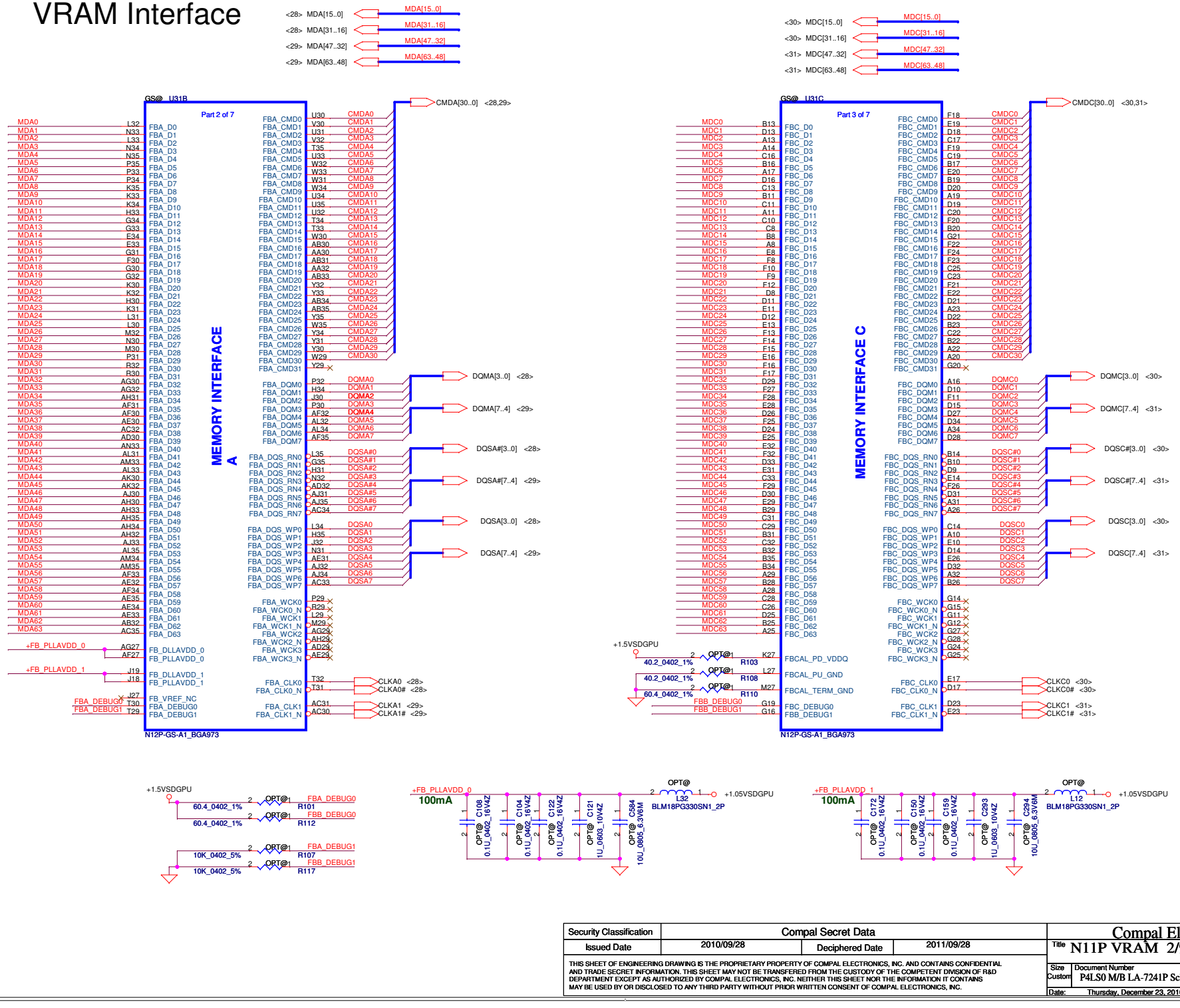
VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: N11P VRAM 2/9

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Custom	P4LS0 M/B LA-7241P Schematic	0.1

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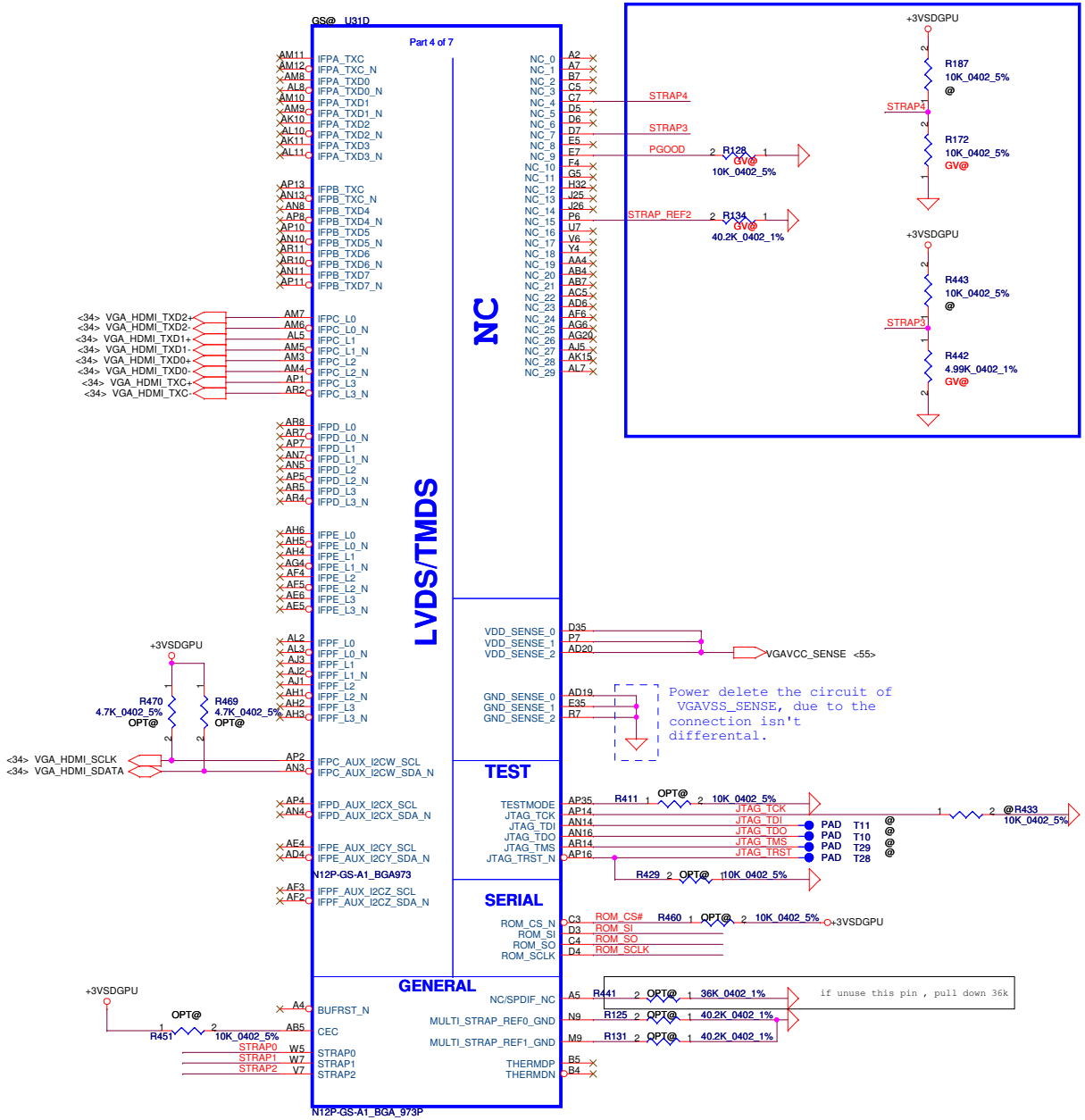
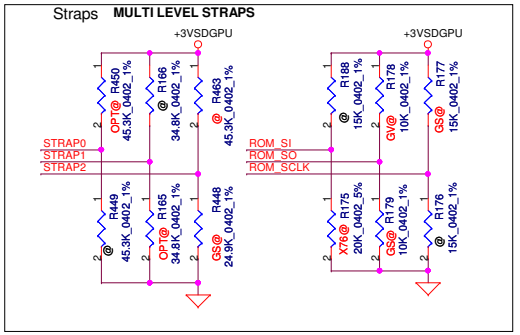
For GB2-128 & GB2b-128 colayout....



Option Component

ROM_SCLK	--->	R177 2 GV@ 1	4.99K_0402_1%	
STRAP2	--->	R448 2 GV@ 1	4.99K_0402_1%	



N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
128MX16 Samsung SA000047Q20	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

N12P-GV	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L 5K	L 5K	L 10K	L 20K	H 10K	H 5K
64MX16 Hynix SA000032400	H 45K	L 35K	L 5K	L 5K	L 10K	L 15K	H 10K	H 5K
128MX16 Samsung SA000047Q20	H 45K	L 35K	L 5K	L 5K	L 10K	L 45K	H 10K	H 5K

GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GV	0x0DF7	Pull up 5K	Pull down 5K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S40	512MB	0010	PD 15K (SD034150280)
	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128M16 H5TQ2G63BFR-11C SA00003YO20	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64M16 K4W1G1646G-BC11 SA00004GS10	512MB	0011	PD 20K (SD034200280)
	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q20	2GB	0111	PD 45.3K(SD034453280)

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Compal Electronics, Inc.

Title: N11P LVDS 3/9

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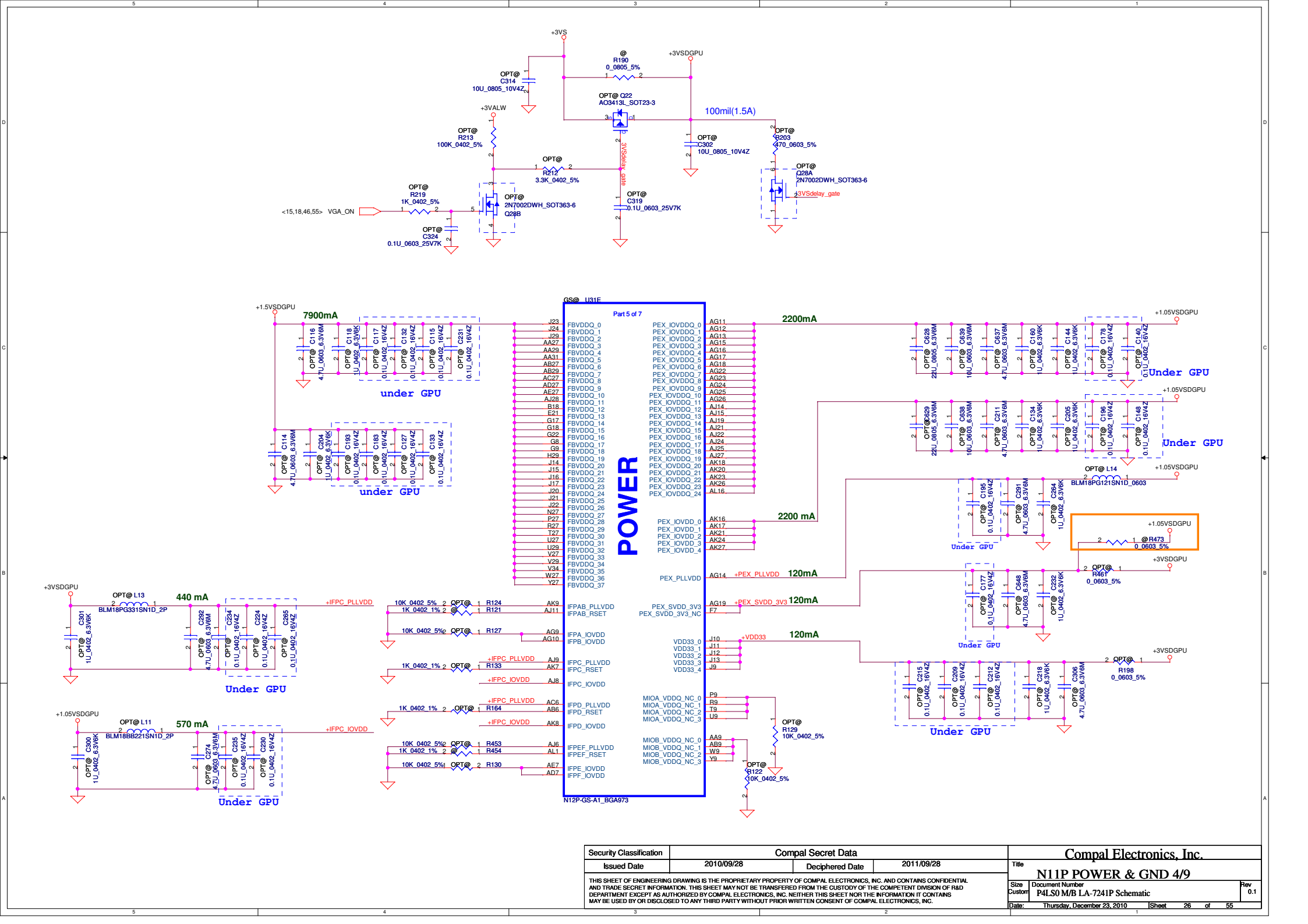

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: N11P POWER & GND 4/9

Size	Document Number	Rev
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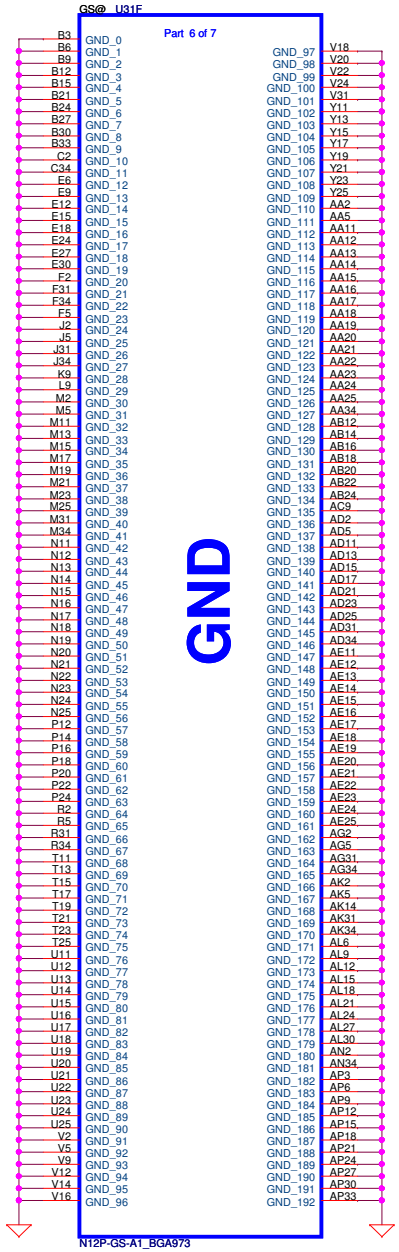

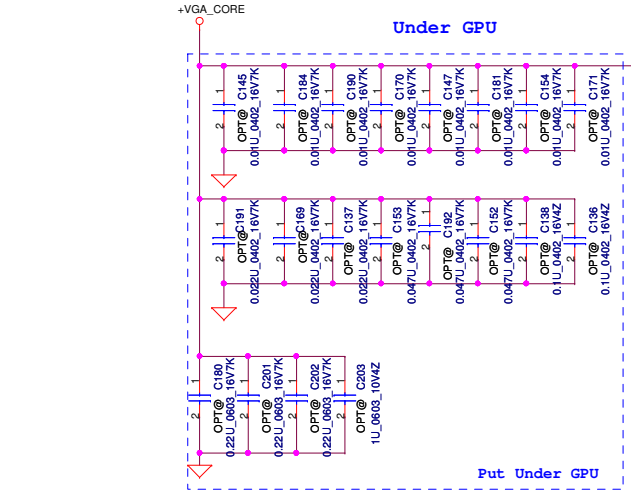

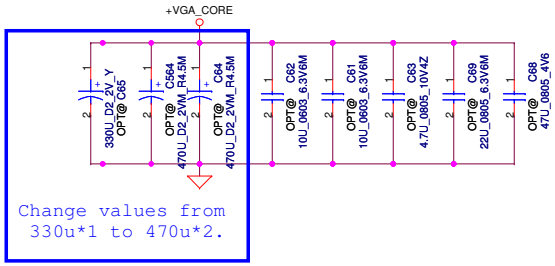

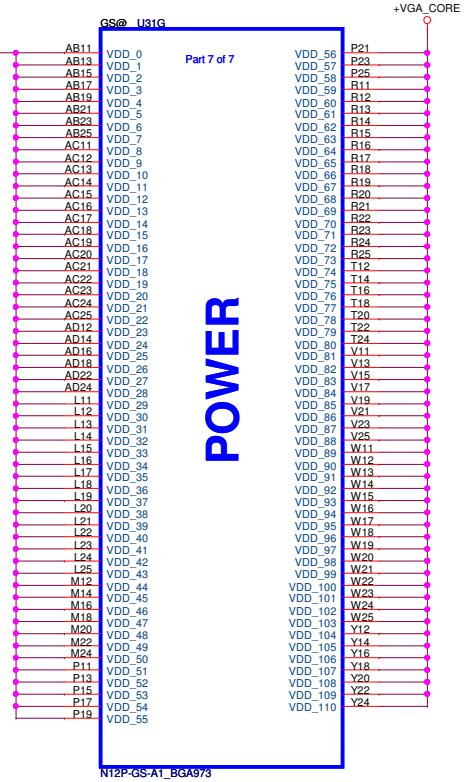

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: N11P POWER & GND 5/9

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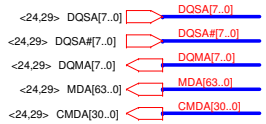
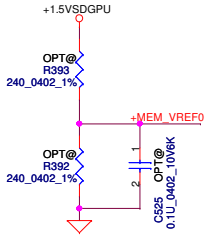
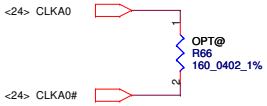
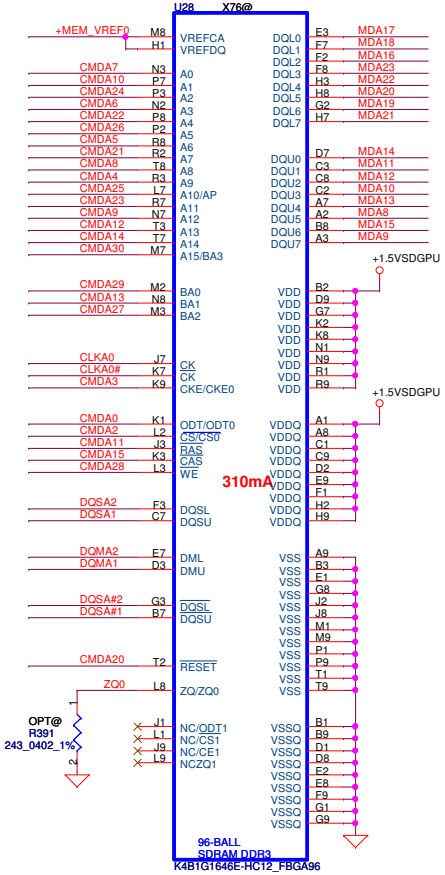
VRAM DDR3 chips (1GB)

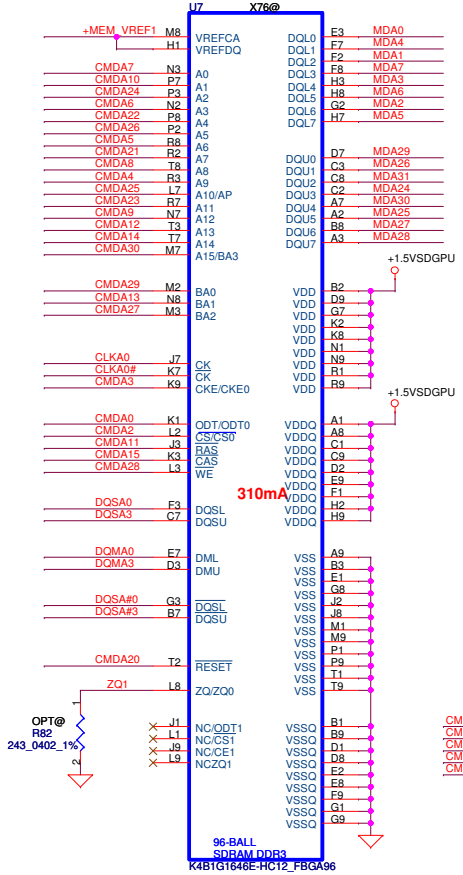
64Mx16 DDR3 *8==>1GB

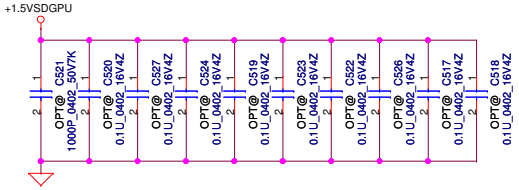


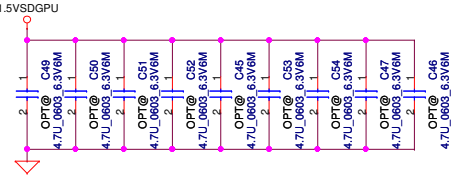




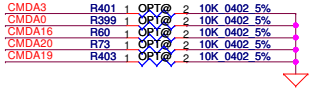








Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

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Issued Date	2010/09/28	Deciphered Date	2011/09/28

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Title: N11P DDR3 6/9

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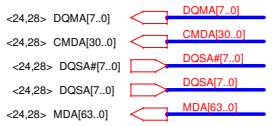
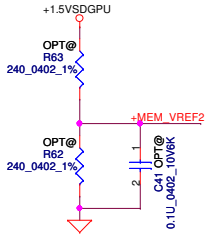
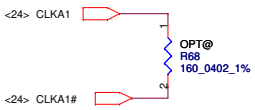
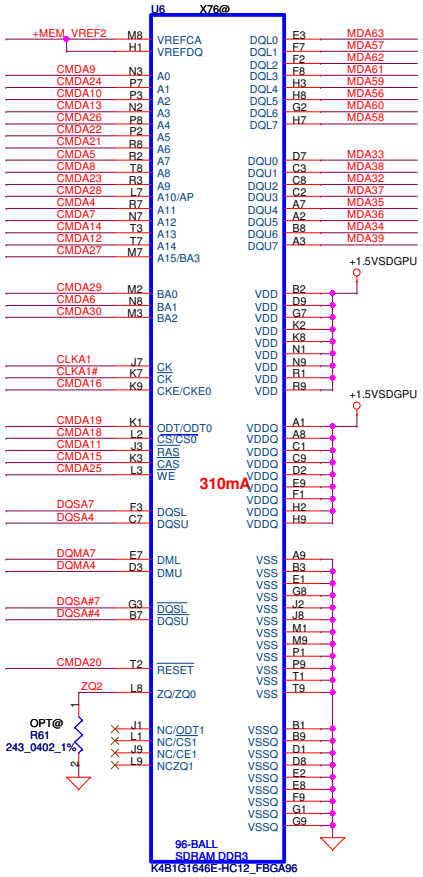
VRAM DDR3 chips (1GB)

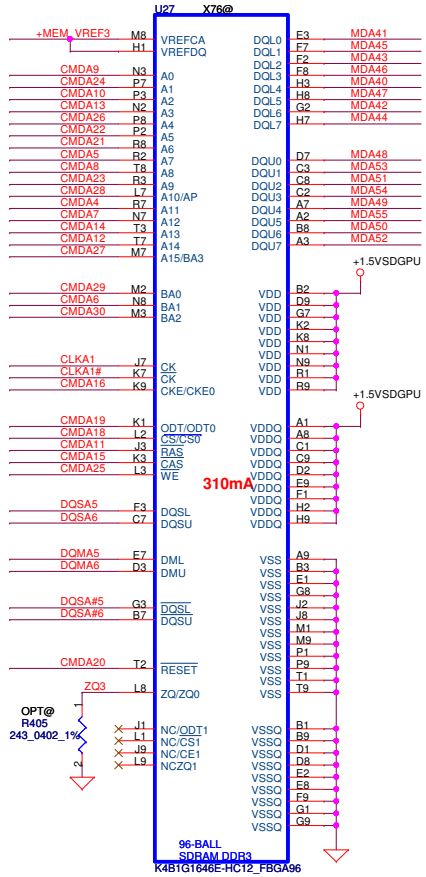
64Mx16 DDR3 *8==>1GB

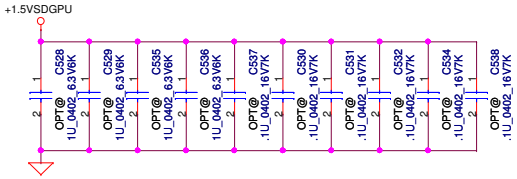


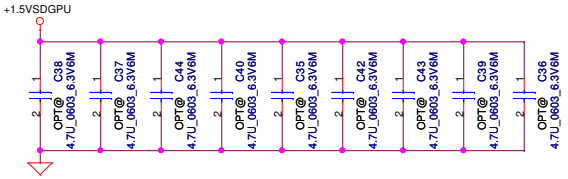












Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

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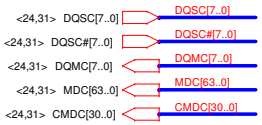
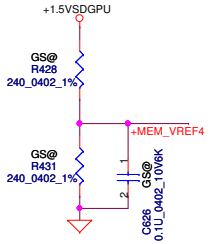
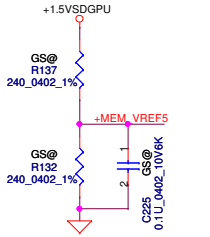
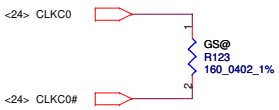
VRAM DDR3 chips (1GB)

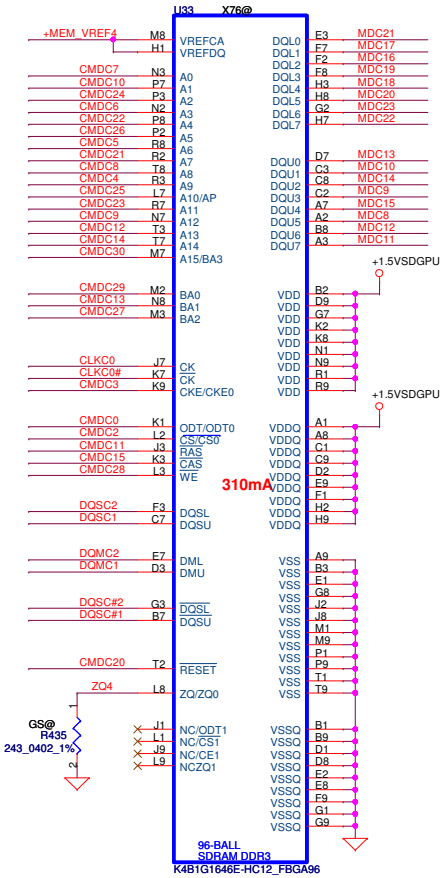
64Mx16 DDR3 *8==>1GB

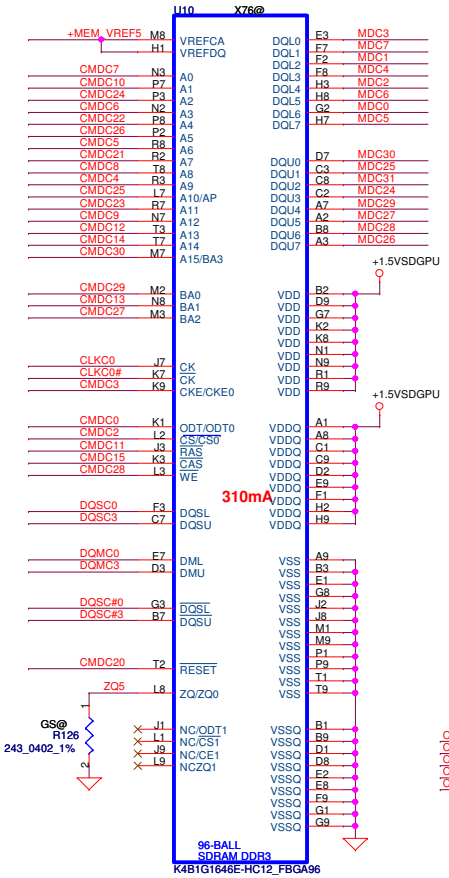


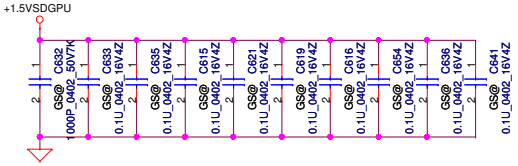


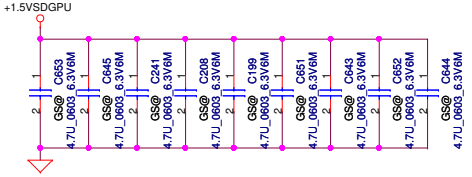




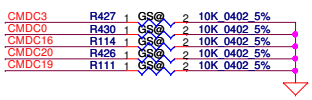








Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

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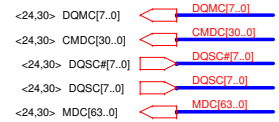
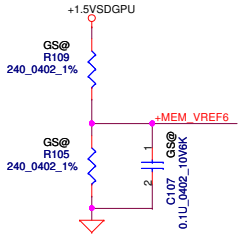
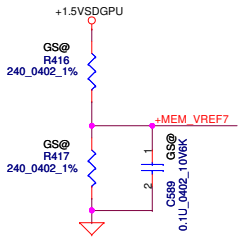
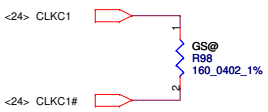
VRAM DDR3 chips (1GB)

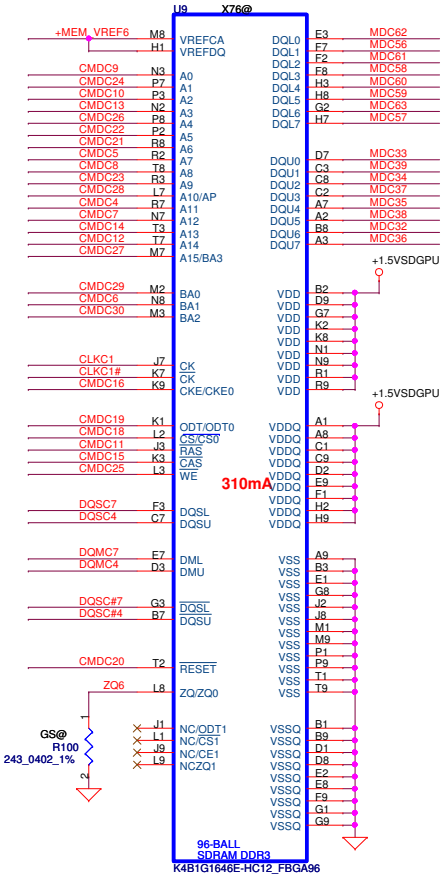
64Mx16 DDR3 *8==>1GB

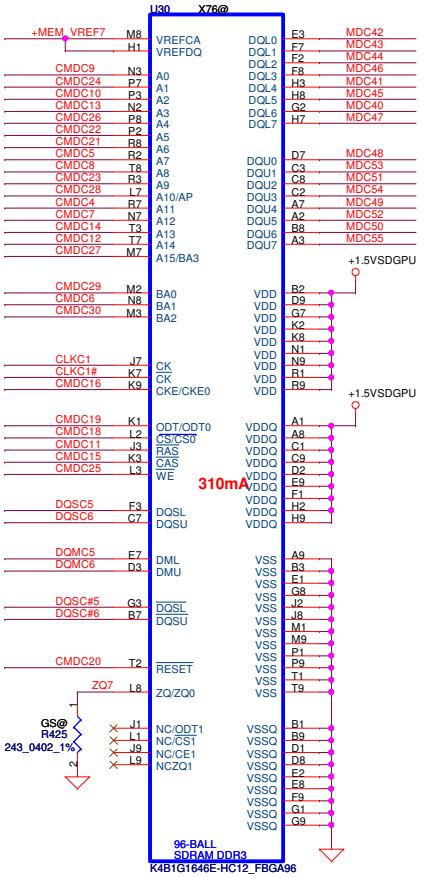


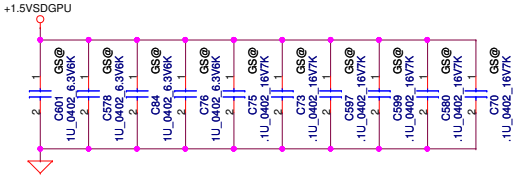


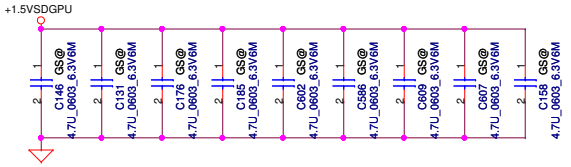












Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

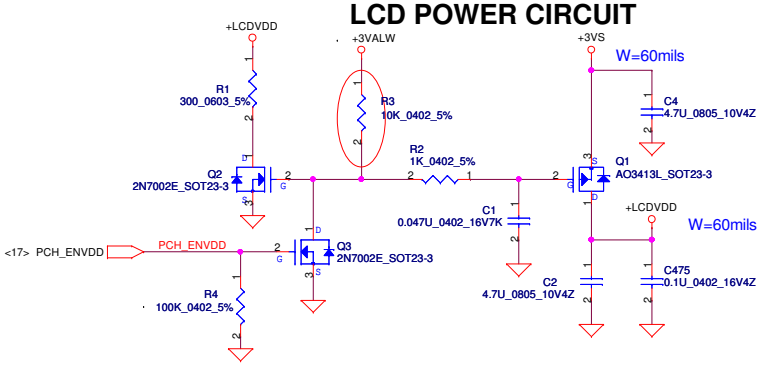
Compal Electronics, Inc.

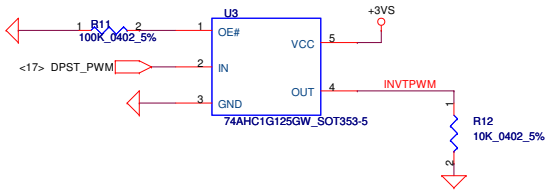
Title: N11P DDR3 9/9

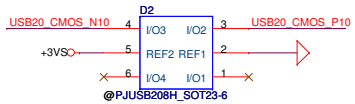
Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

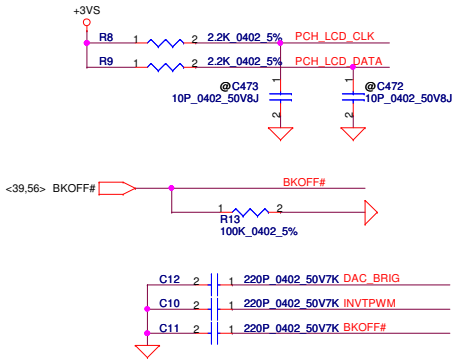
Date: Thursday, December 23, 2010 | Sheet 31 of 55

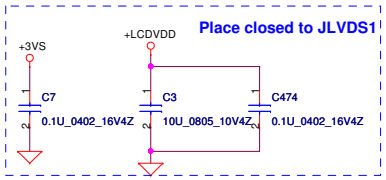
LCD POWER CIRCUIT



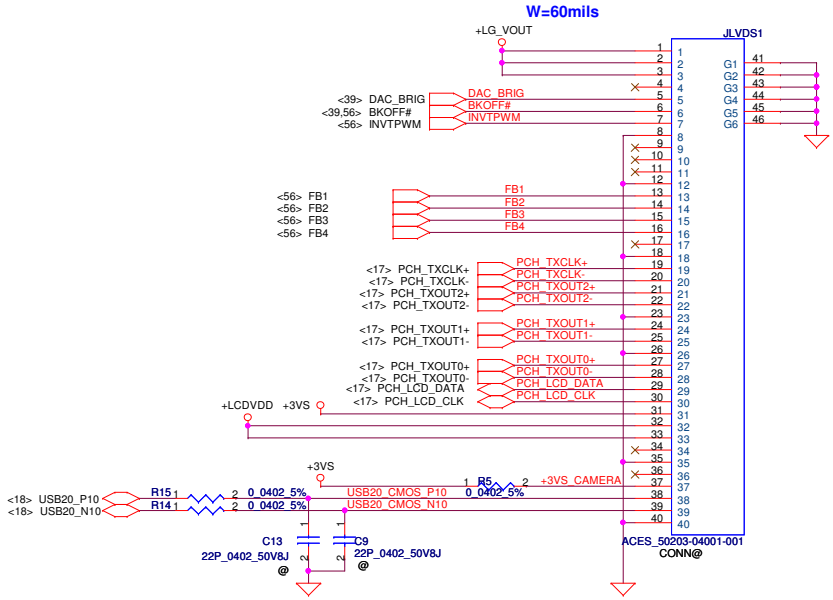








LCD/LED PANEL Conn.



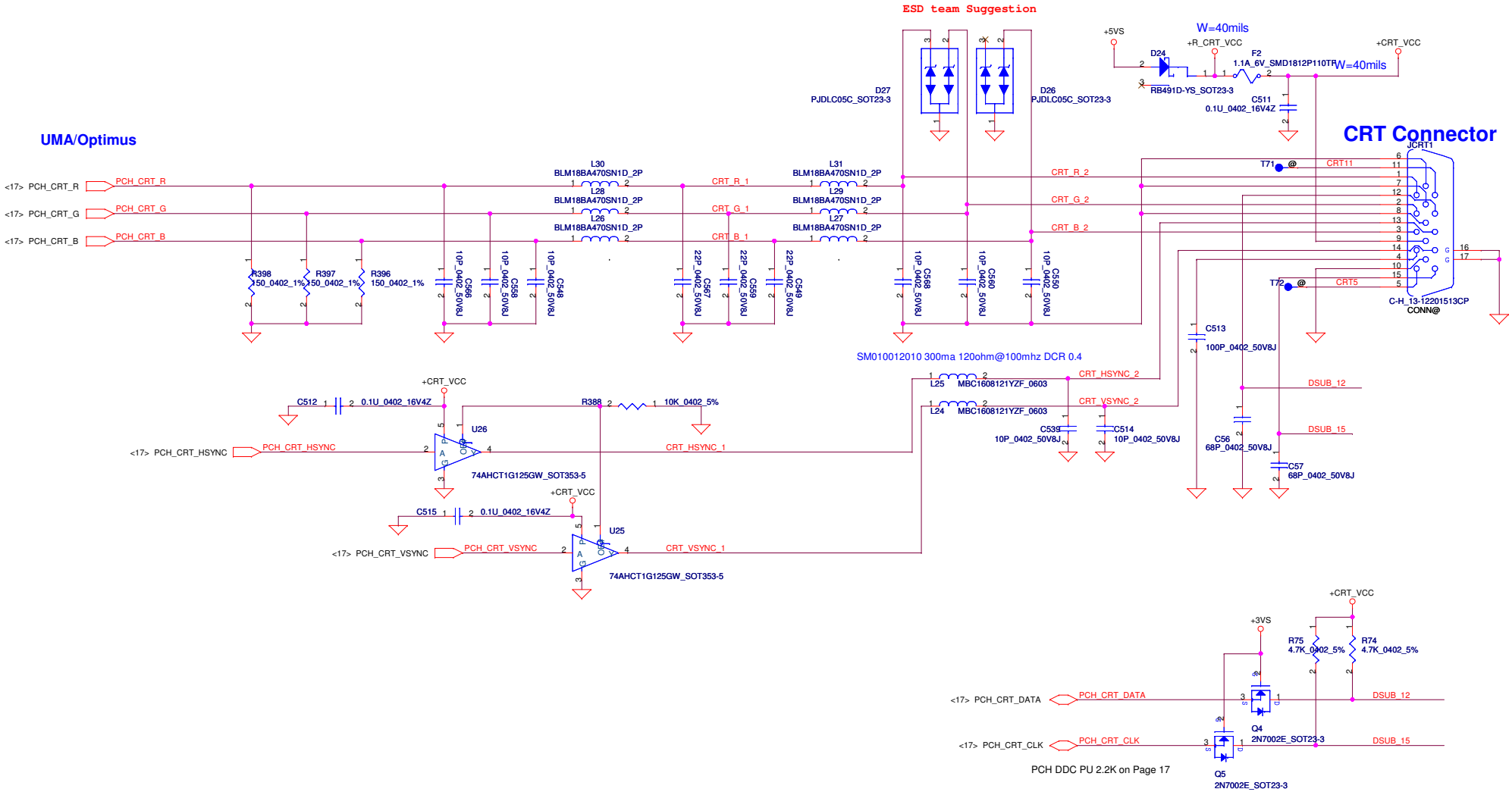
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

Date: Thursday, December 23, 2010 | Sheet 32 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.		
Title: CRT Connector		
Size: Custom	Document Number: P4LS0 M/B LA-7241P Schematic	Rev: 0.1
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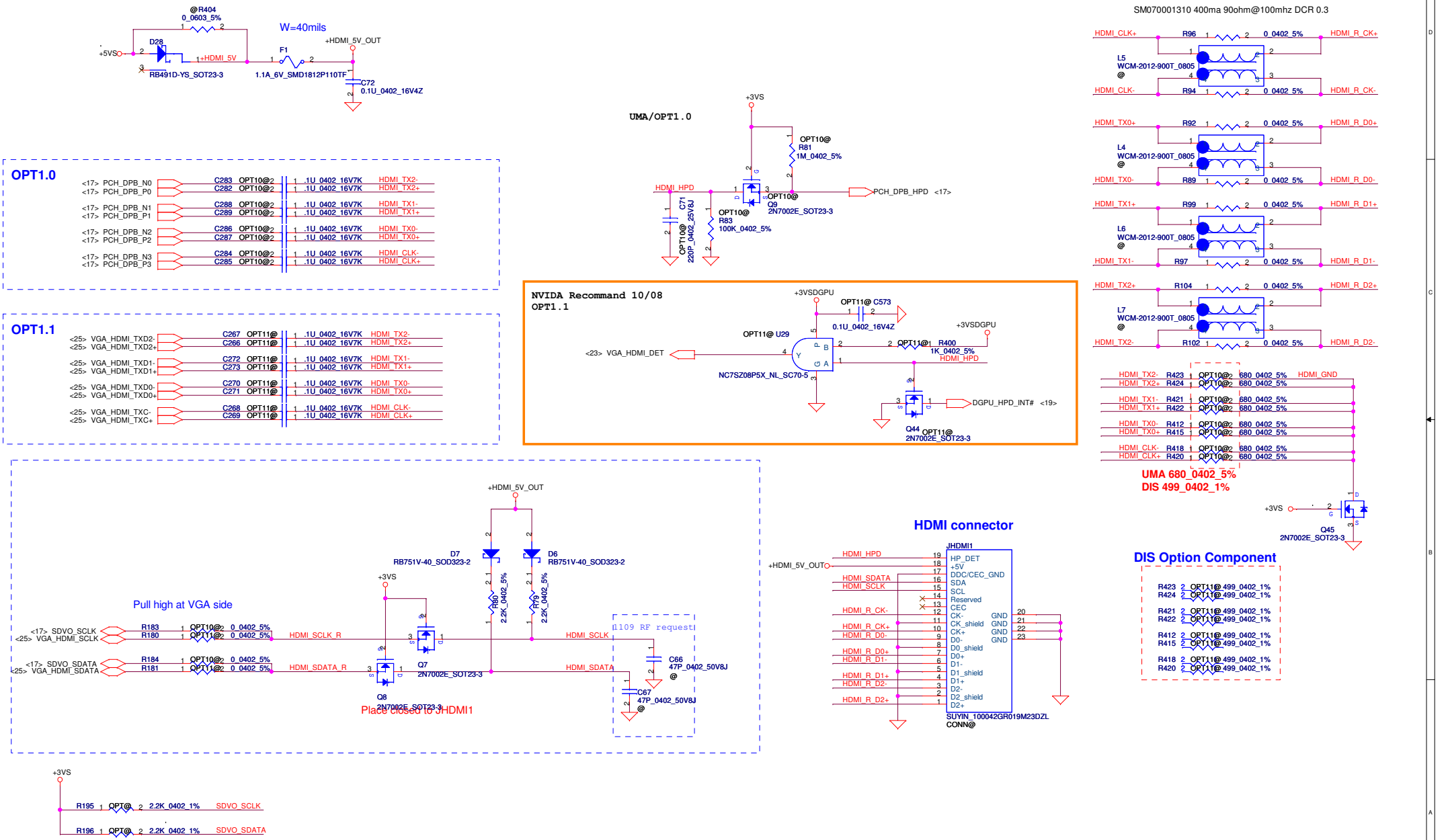


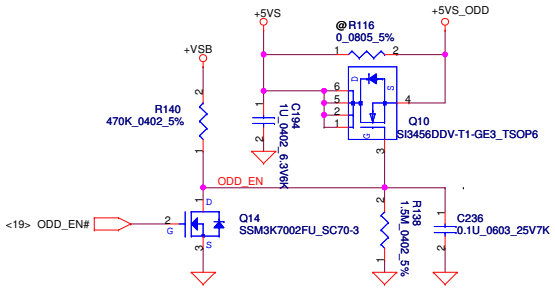
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: HDMI Conn

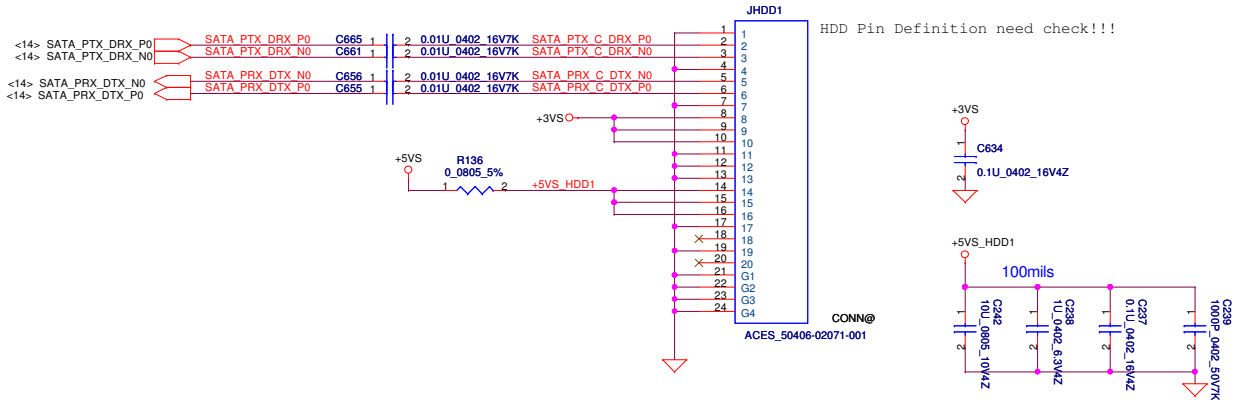
Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

Date: Thursday, December 23, 2010 | Sheet 34 of 55

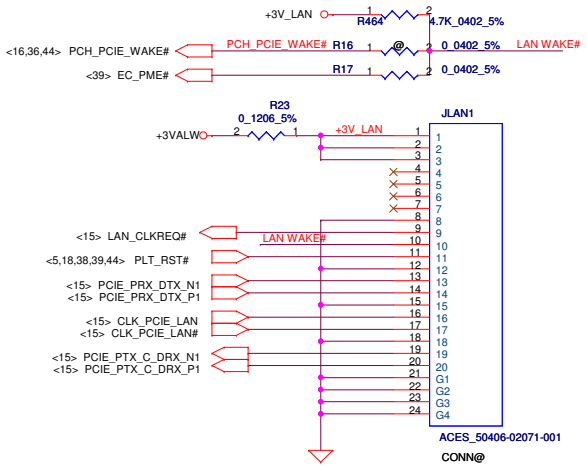


SATA HDD1 Conn.

CL 4.0 mm

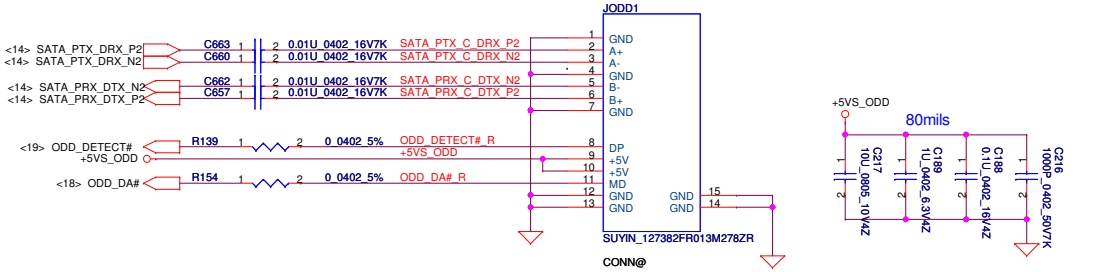


LAN CONN.



M/B side

SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: HDD, ODD & LAN Connector

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

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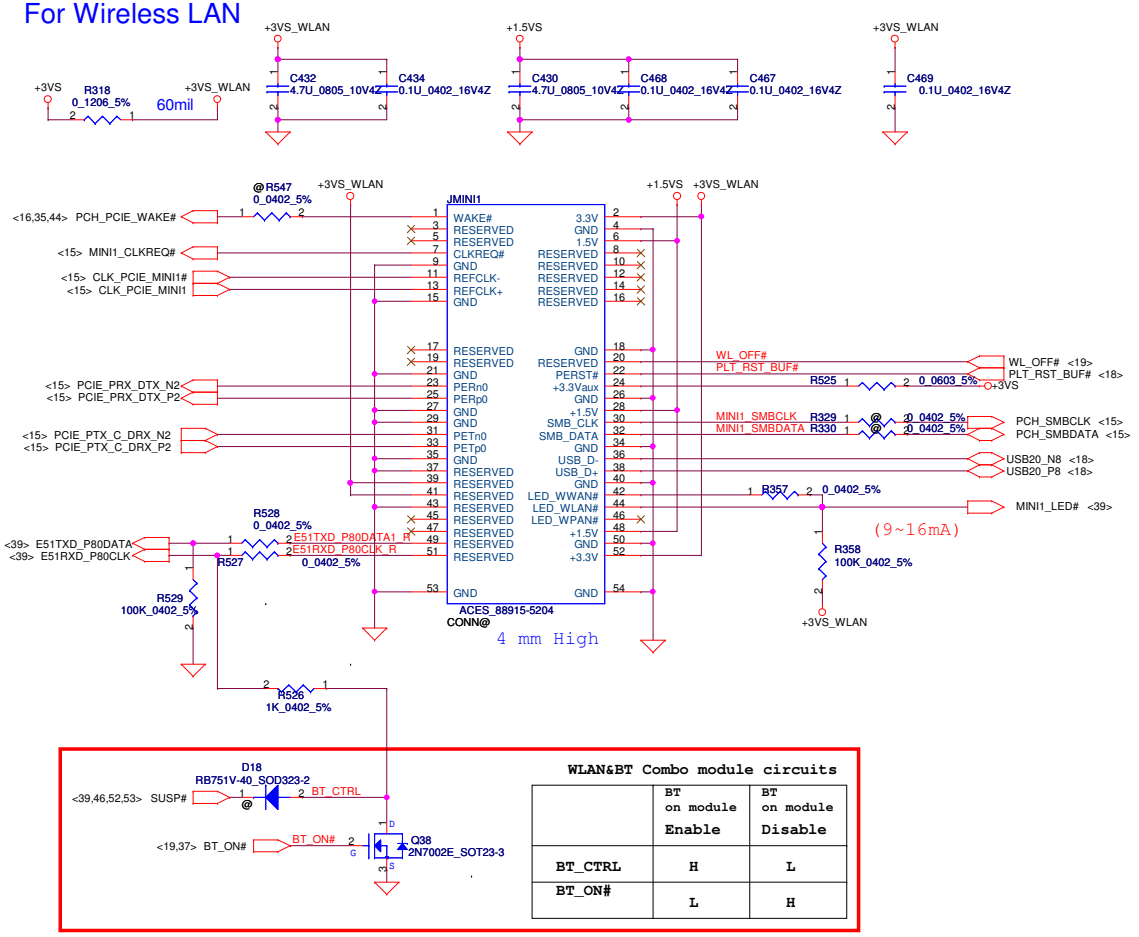
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For Wireless LAN



WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)/USB/BT

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

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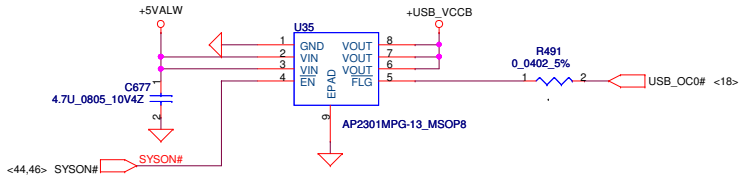
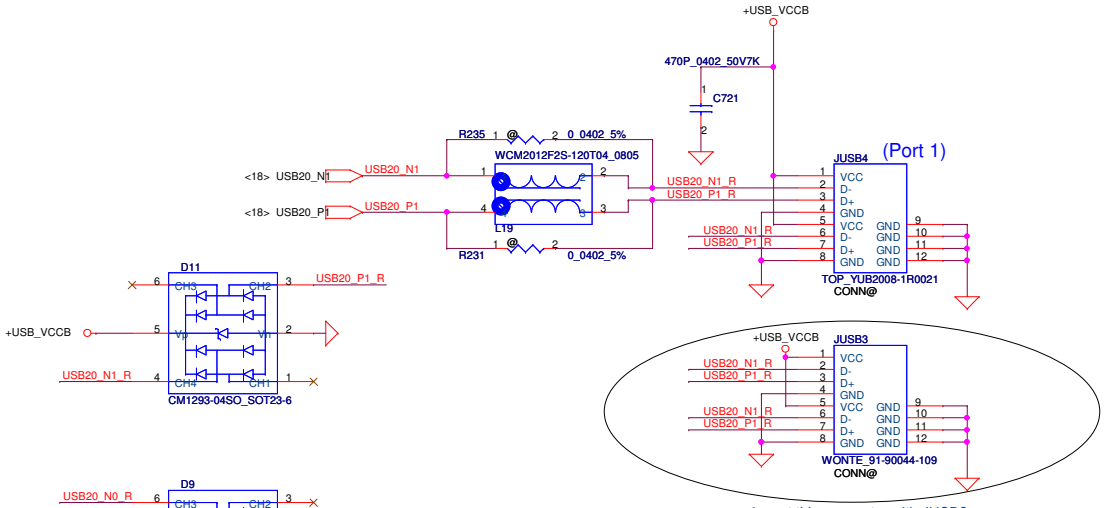
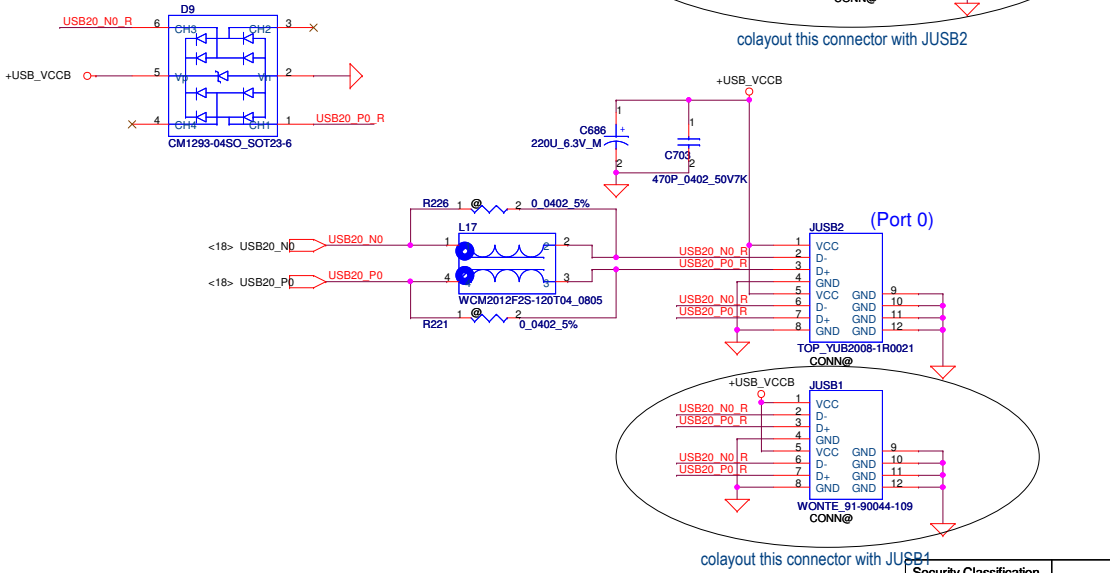
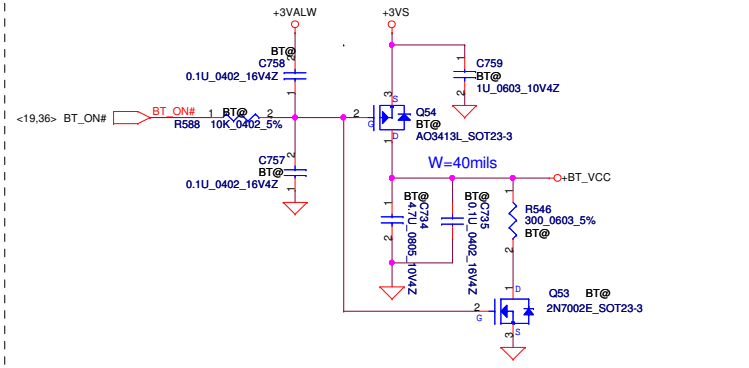


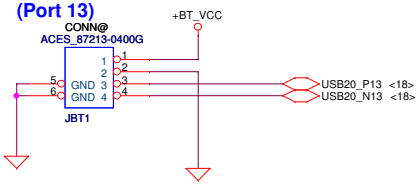






BT Conn.

(Port 13)



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)/USB/BT

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

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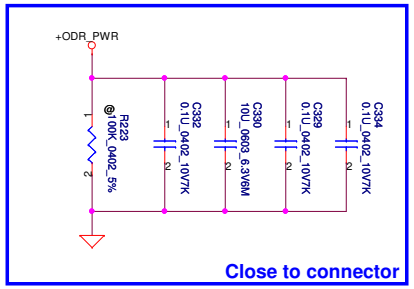
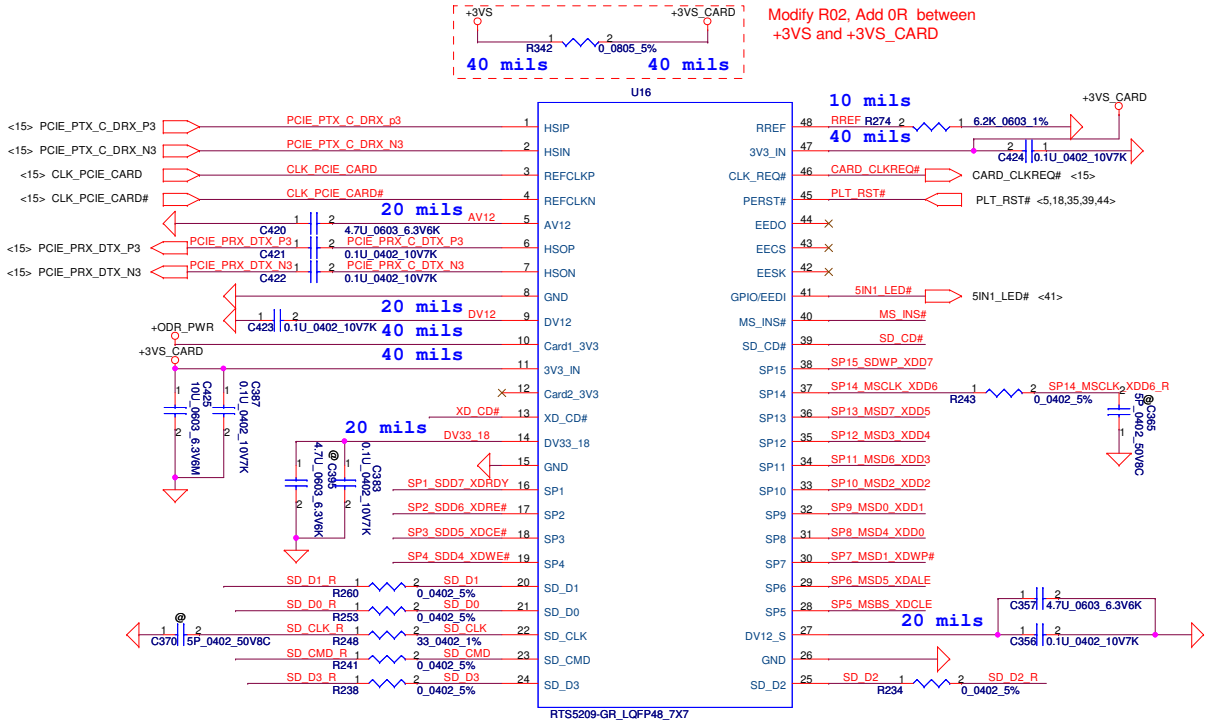
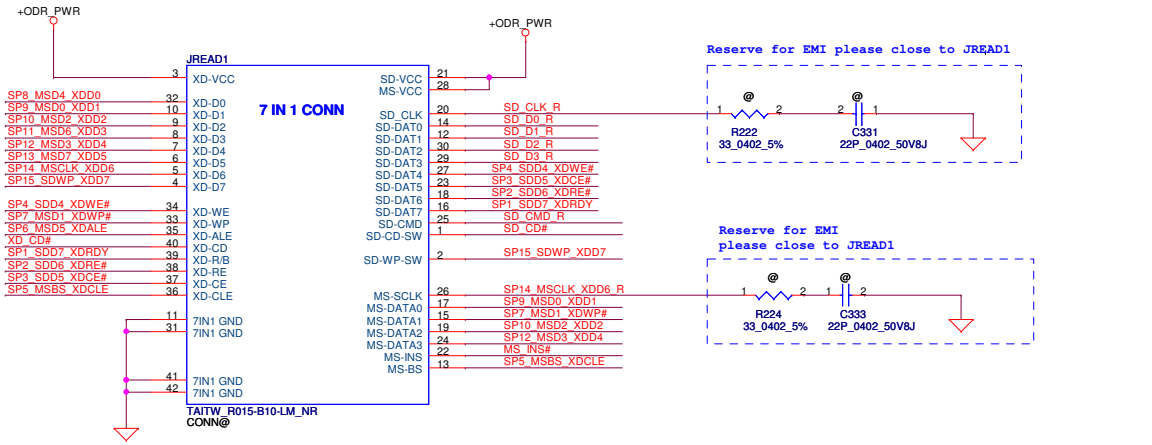
Card Reader







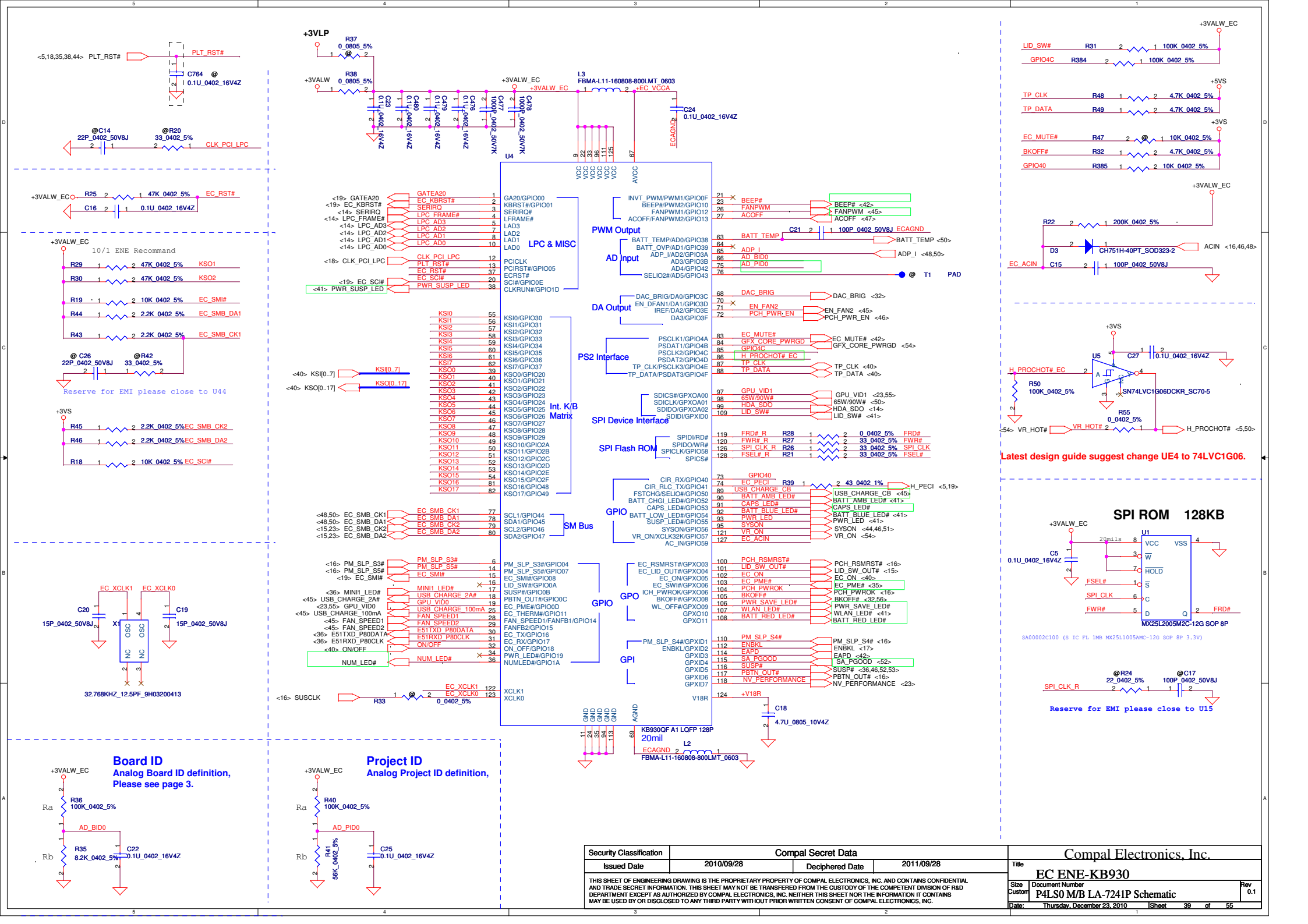
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: Card Reader RTS5209

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

Date: Thursday, December 23, 2010 | Sheet 38 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: EC ENE-KB930

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

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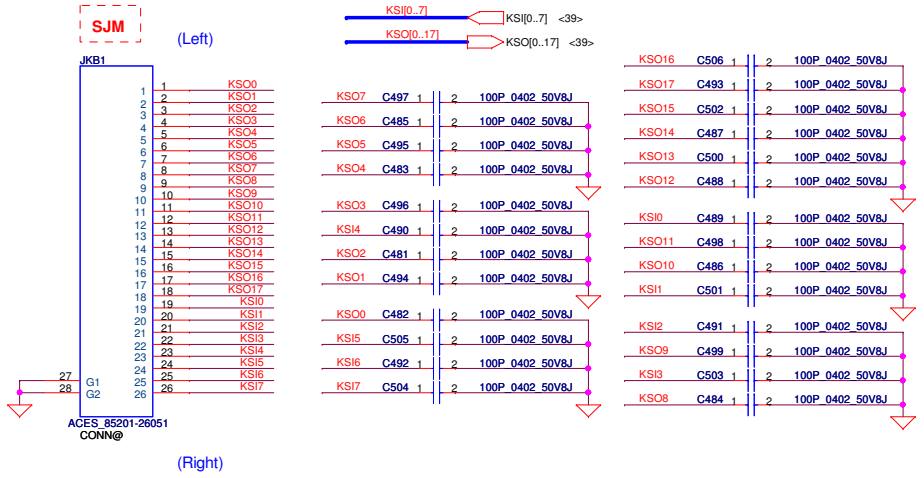
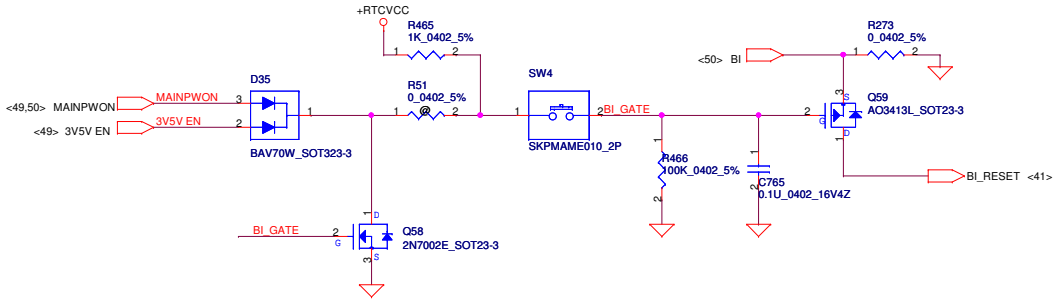
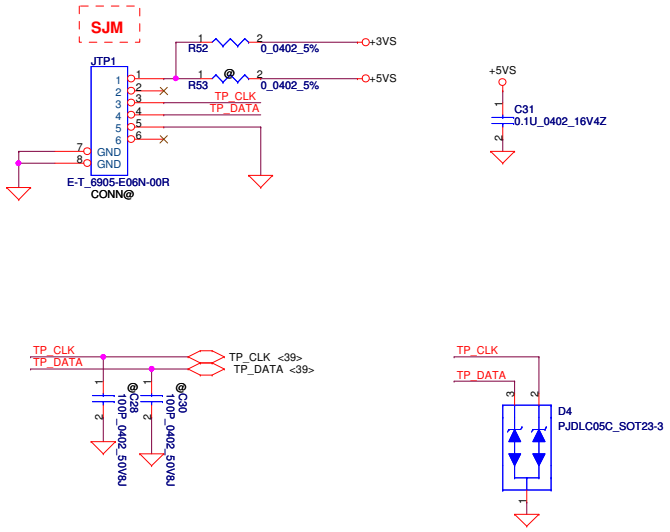
INT_KBD Conn.



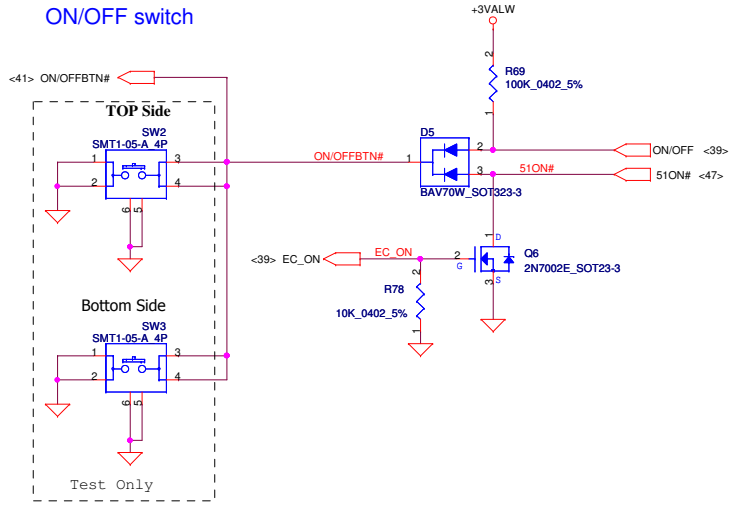
Reset Button



To TP/B Conn.



Power Button



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: I/O Port & K/B Connector/PWR OK

Size	Document Number	Rev
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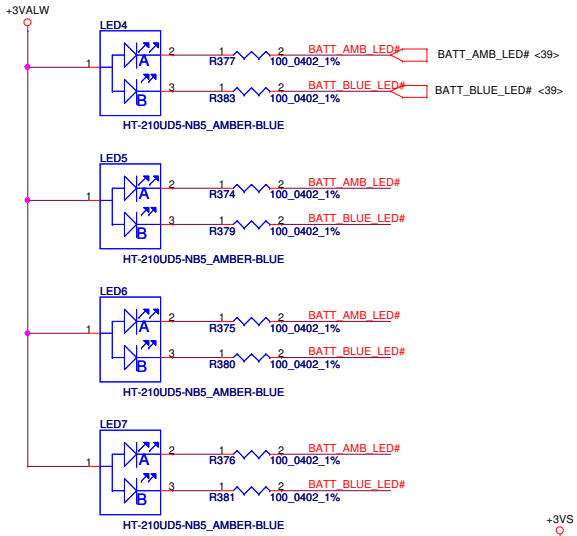
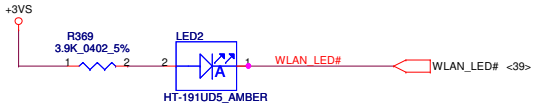
Battery LED

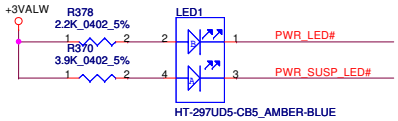
Side View LED with Blue/Amber/Red Color



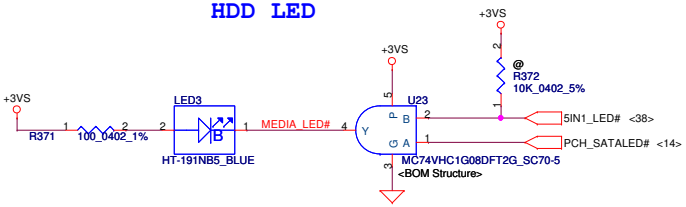
Wireless LED(SJM)

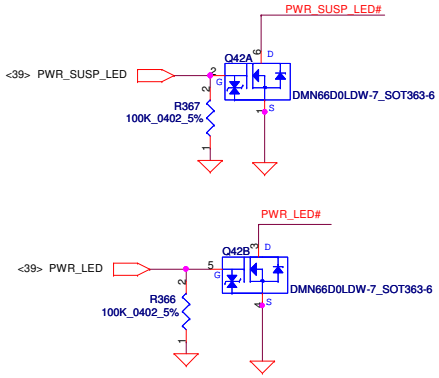


Power LED(SJM)

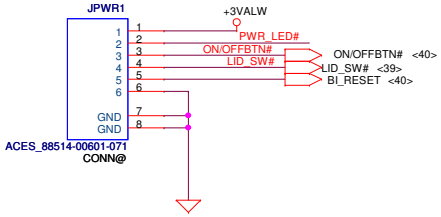


HDD LED





PWR/B



LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
	Blue	Amber	Blue	Amber	Blue	Amber		

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: LED

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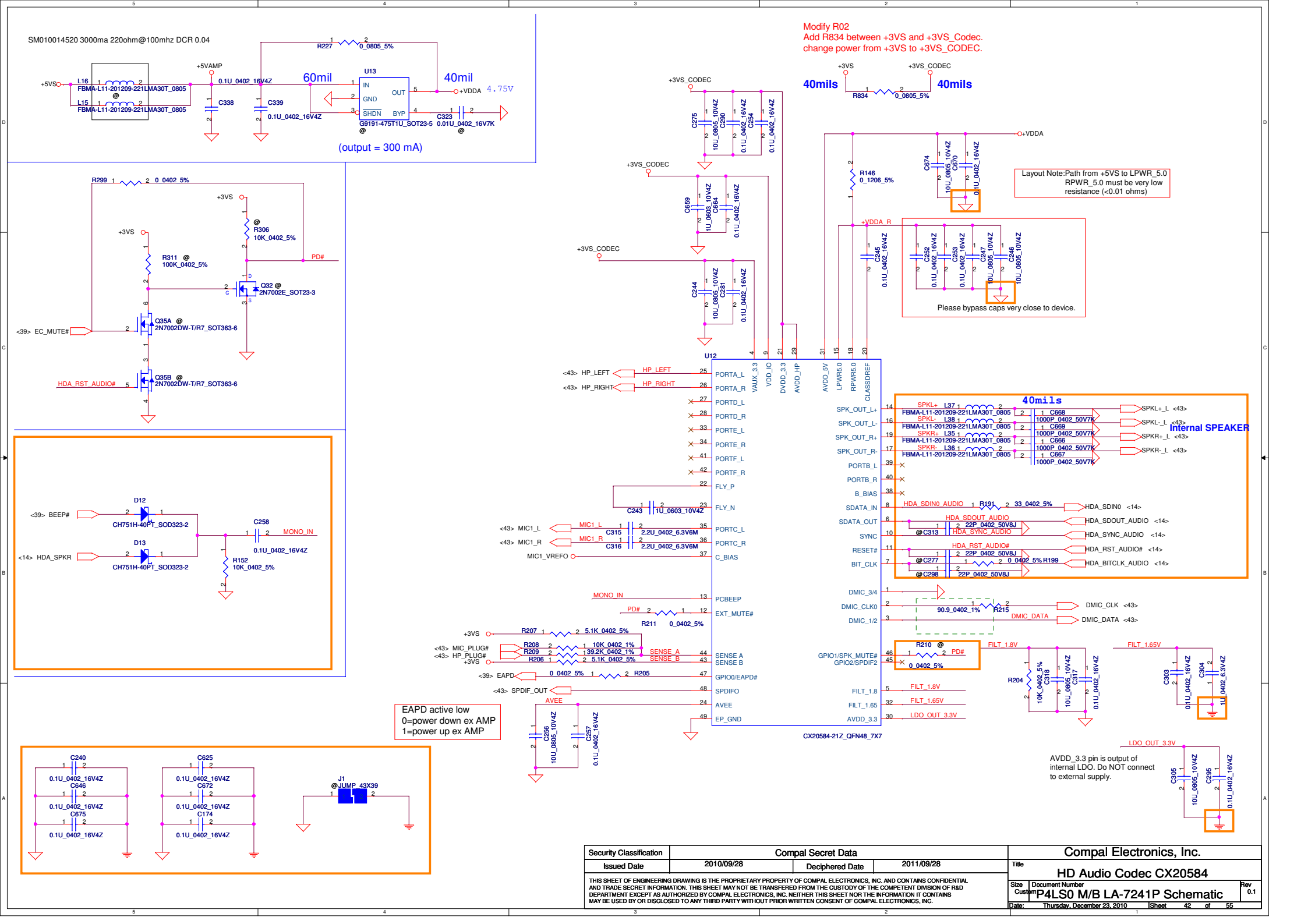
Date: Thursday, December 23, 2010 | Sheet 41 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: HD Audio Codec CX20584

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

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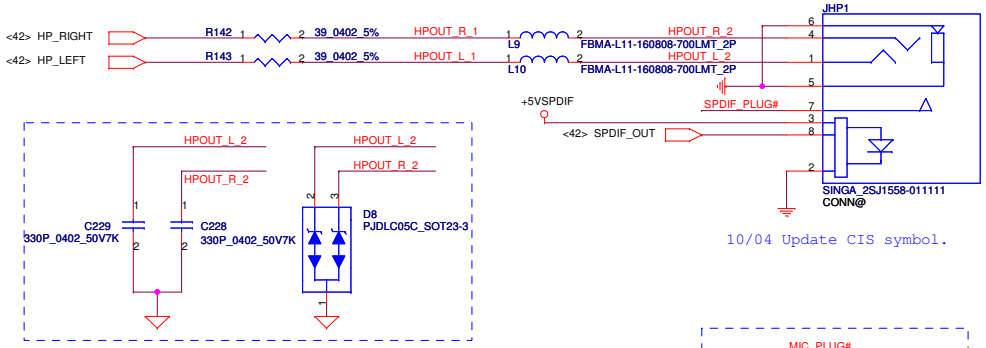
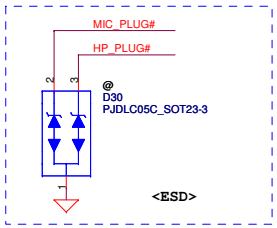
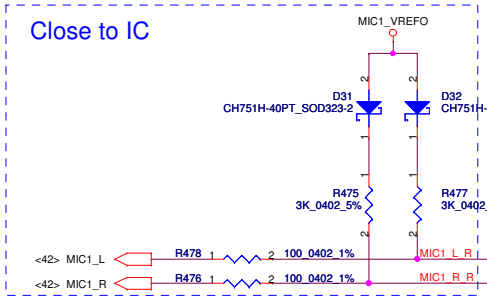
Headphone Out/SPDIF

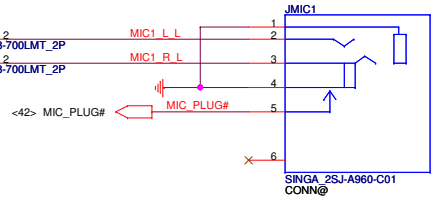


10/04 Update CIS symbol.

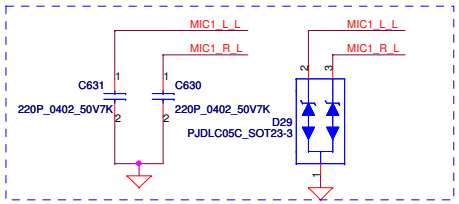




MIC JACK

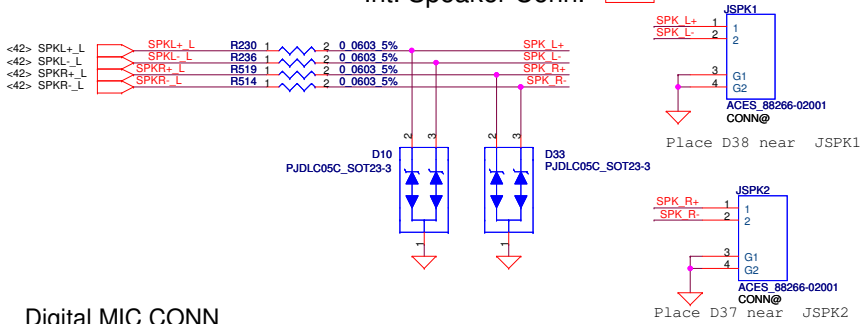


10/04 Check footprint ok
Footprint:SINGA_2SJ-0960-D06_6P

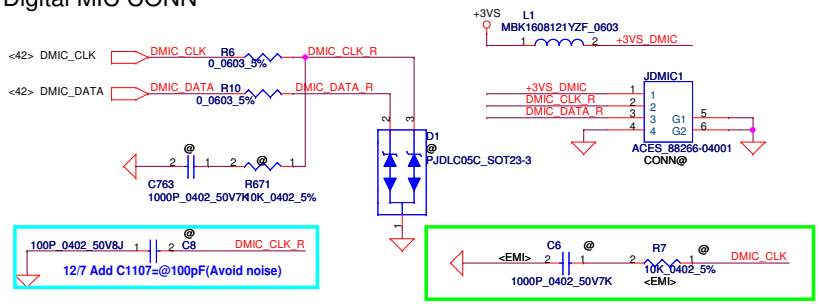


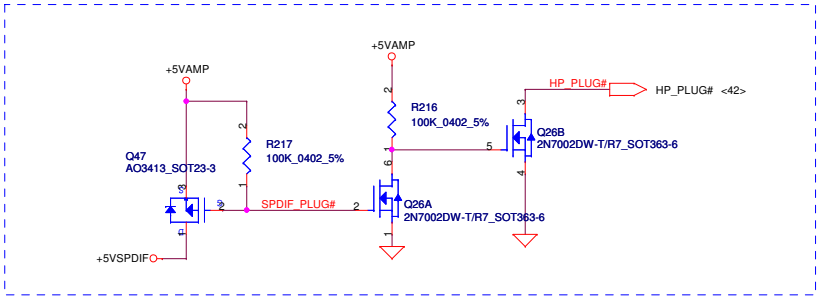
Int. Speaker Conn.

SJM



Digital MIC CONN





Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: Amplifier & Audio Jack

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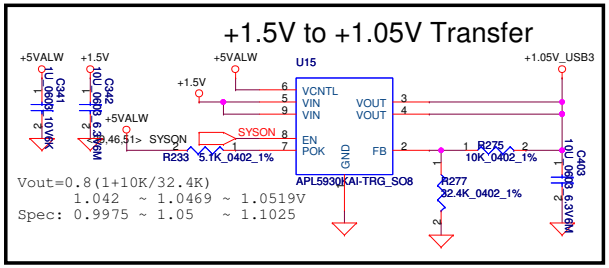
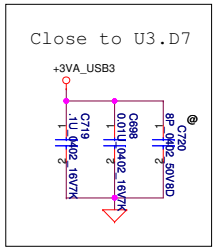
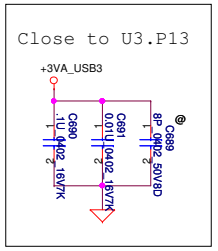
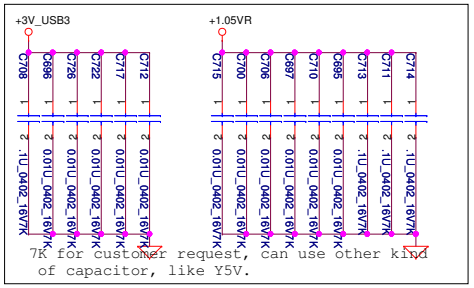
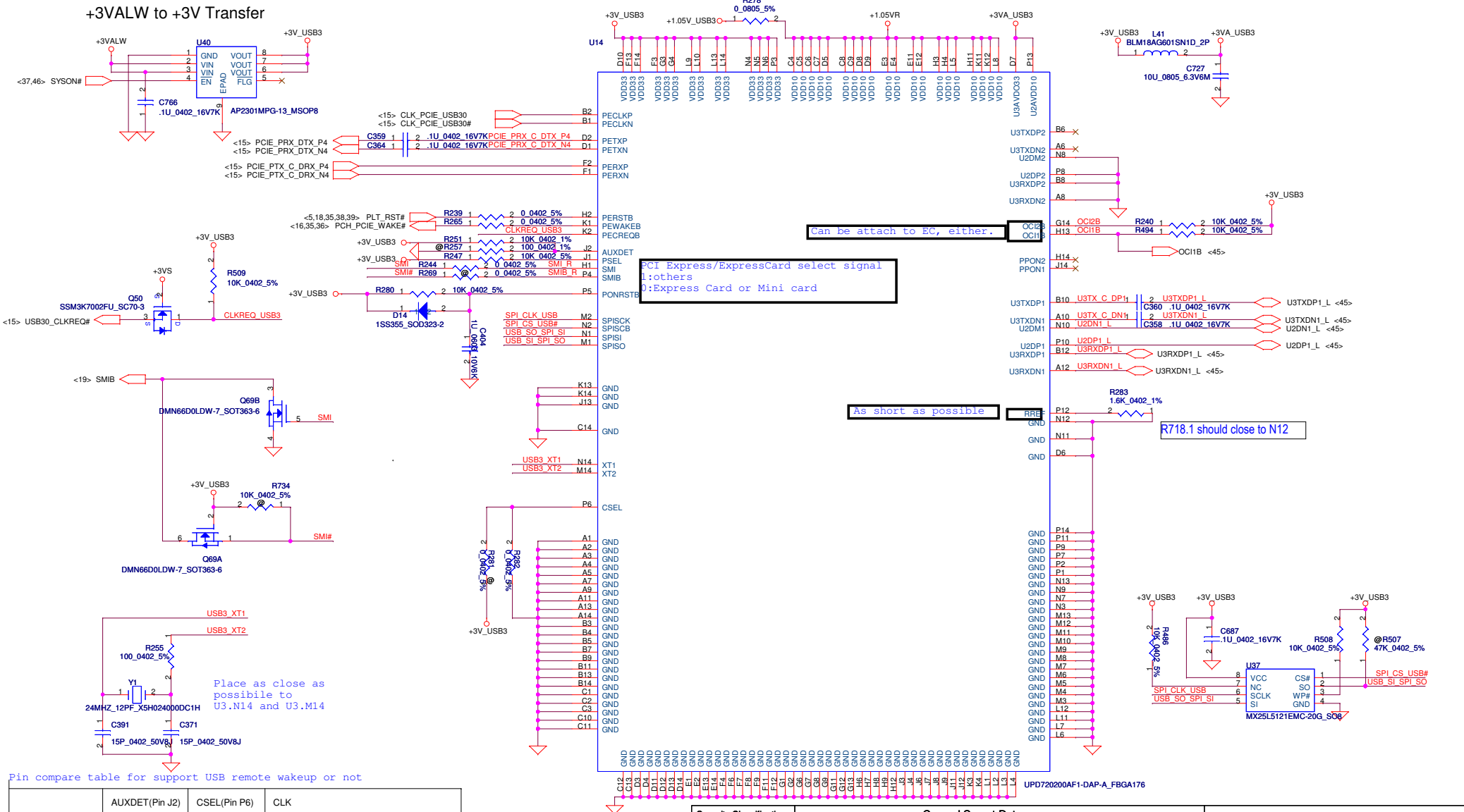










Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

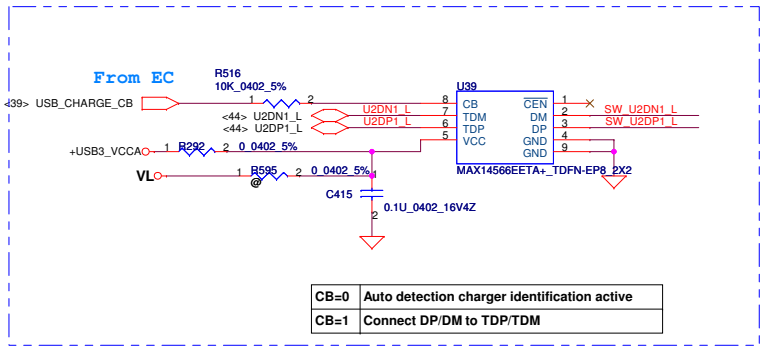
P/N: SA000048H10
(S IC UPD720200AF1-DAP-A FBGA176 USB3.0)

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

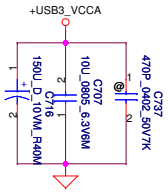
Title: USB3.0 PD720200

Size: Custom	Document Number: P4LS0 M/B LA-7241P Schematic	Rev: 0.1
Date: Thursday, December 23, 2010	Sheet 44 of 55	

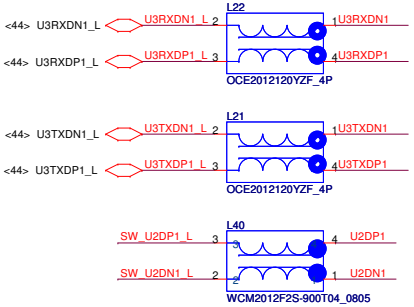
USB Host Charger



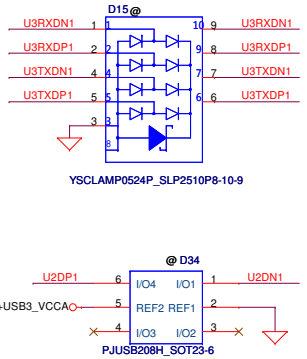
CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM



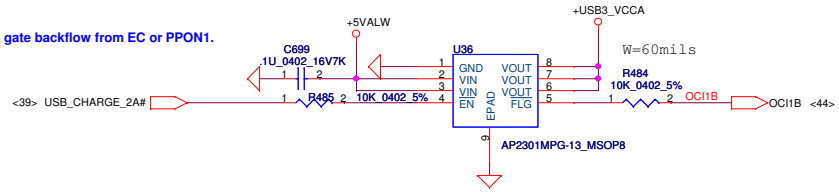
For EMI request

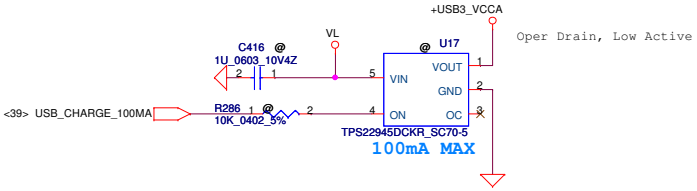


For ESD request

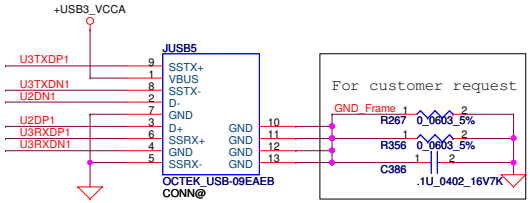


Stuff diodes to gate backflow from EC or PPON1.

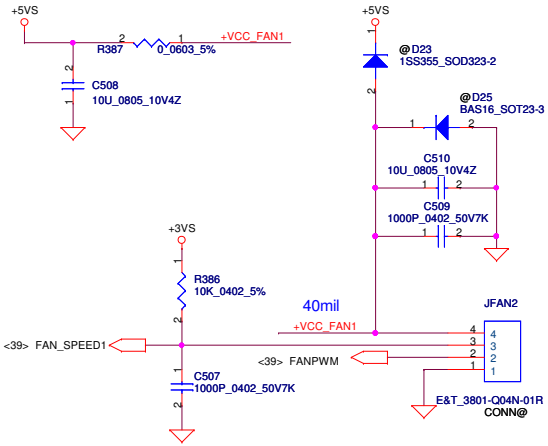




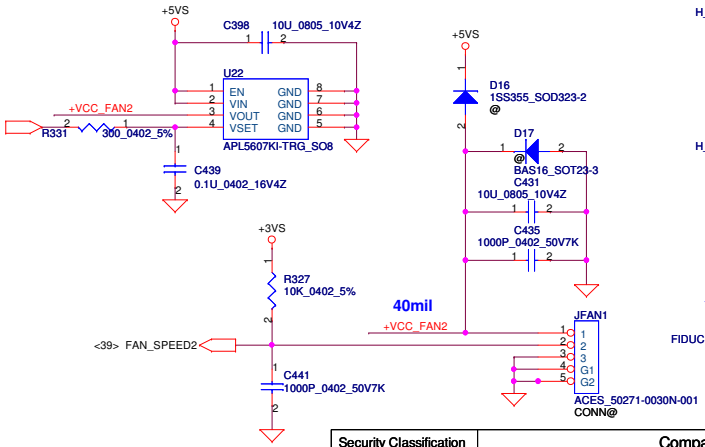
USB3.0 Connector

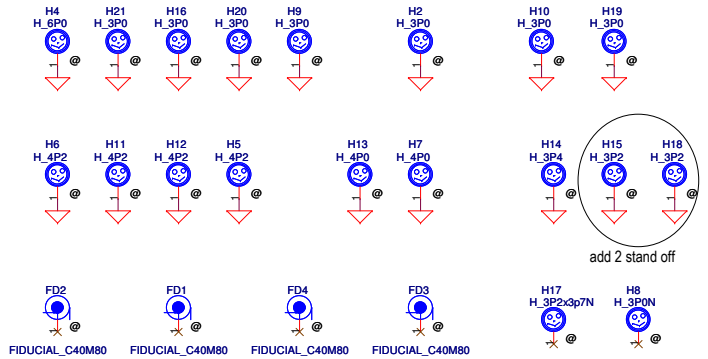


FAN1 Conn



FAN2 Conn





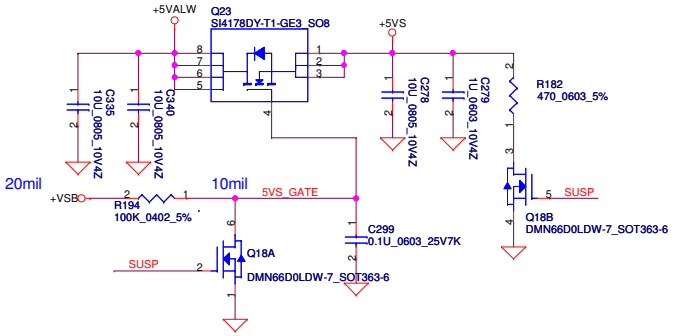
Compal Electronics, Inc.

Title: FAN & Screw Hole

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

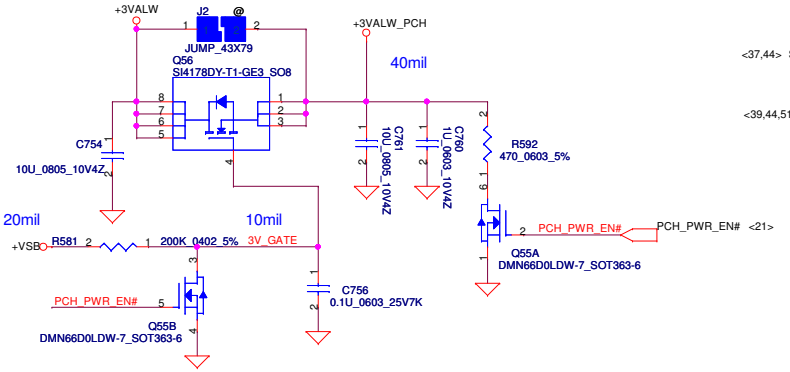
Date: Thursday, December 23, 2010 | Sheet 45 of 55

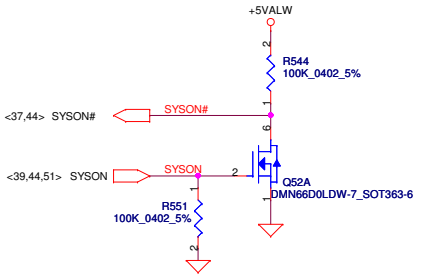
+5VALW TO +5VS

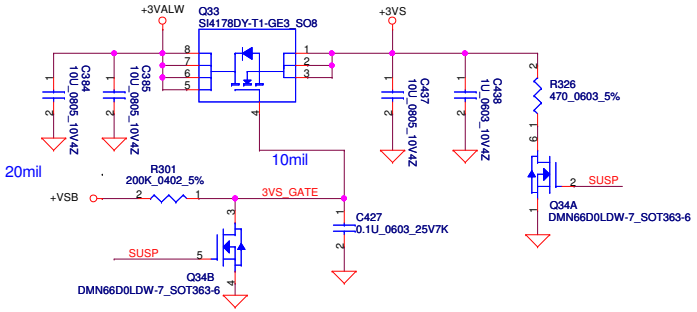


+3VALW TO +3VALW(PCH AUX Power)

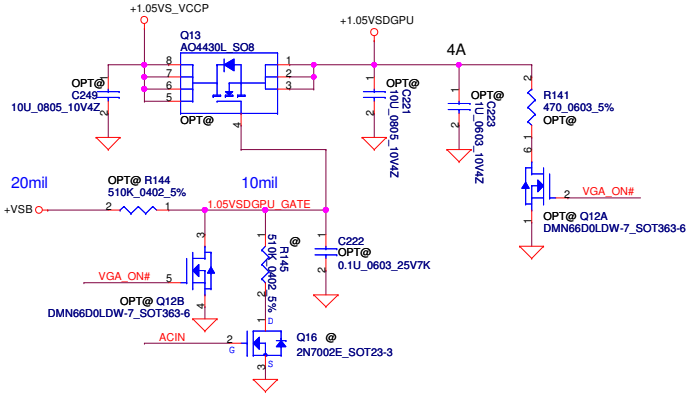
Short J5 for PCH VCCSUS3.3

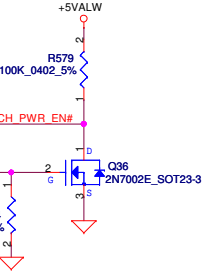






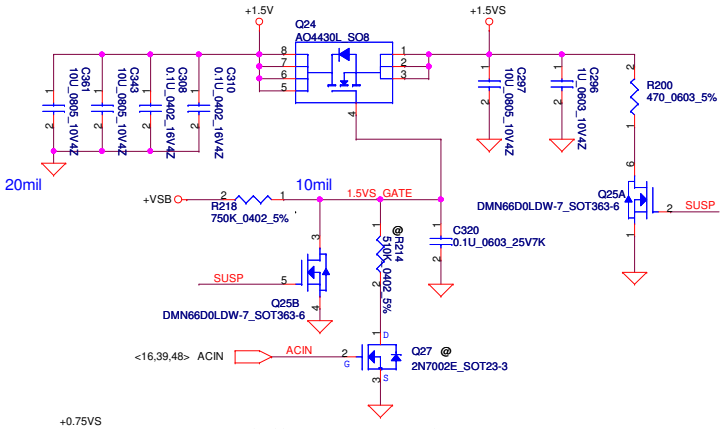
+1.05VS_VCCP to +1.05VSDGPU for GPU



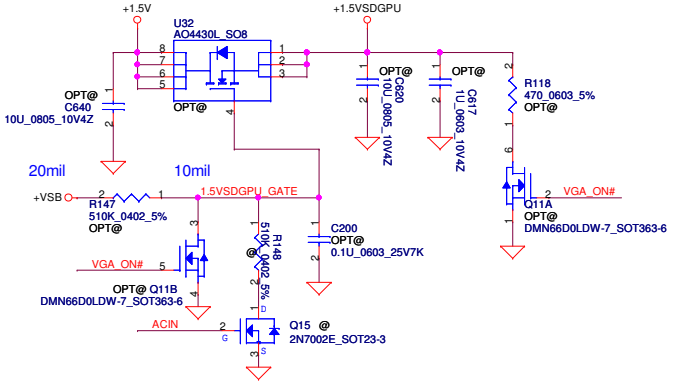


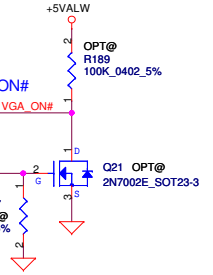
1211 EMI ADD 0.1U close PJ5

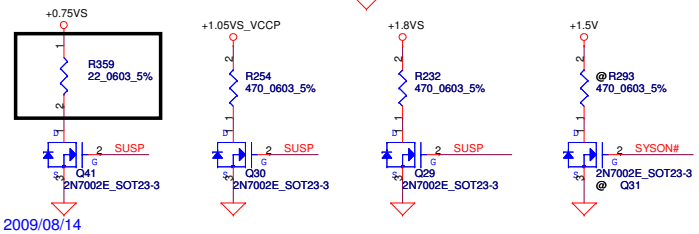
+1.5V to +1.5VS



+1.5V to +1.5VSDGPU for GPU







2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

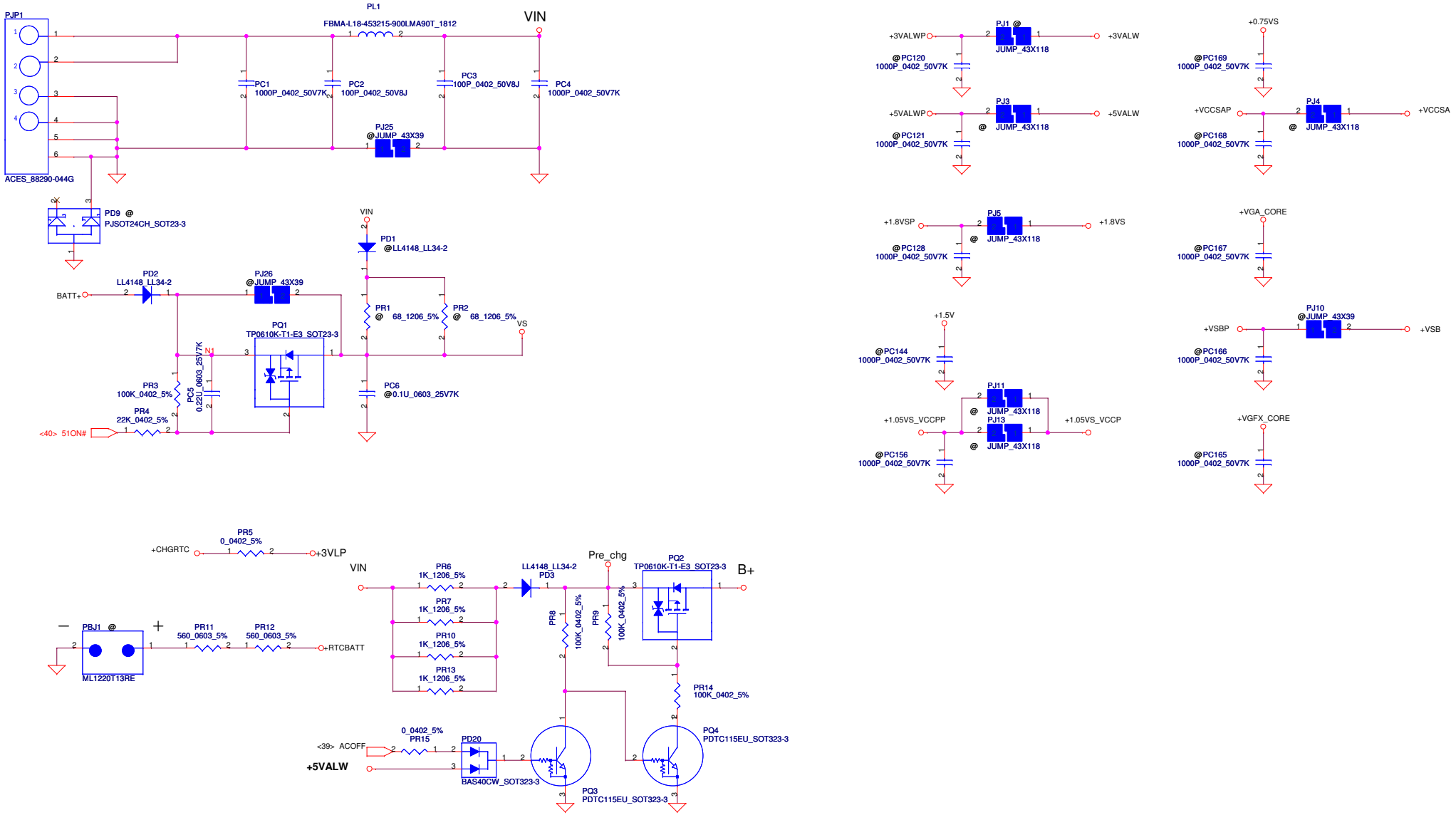
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: P4LS0 M/B LA-7241P Schematic | Rev: 0.1

Date: Thursday, December 23, 2010 | Sheet 46 of 55



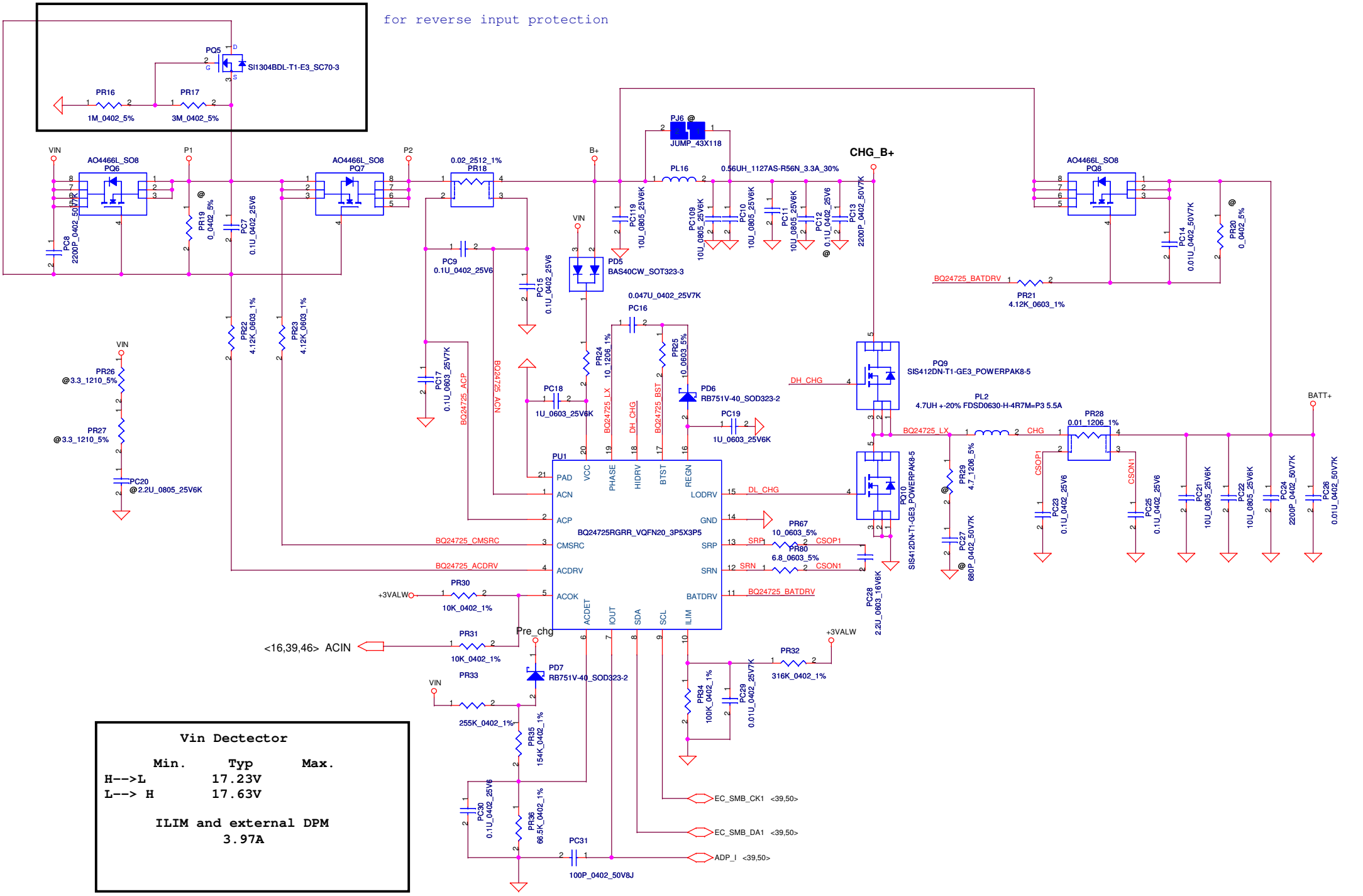
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: LA-7221P | Rev: 0.1

Date: Thursday, December 23, 2010 | Sheet 47 of 55



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

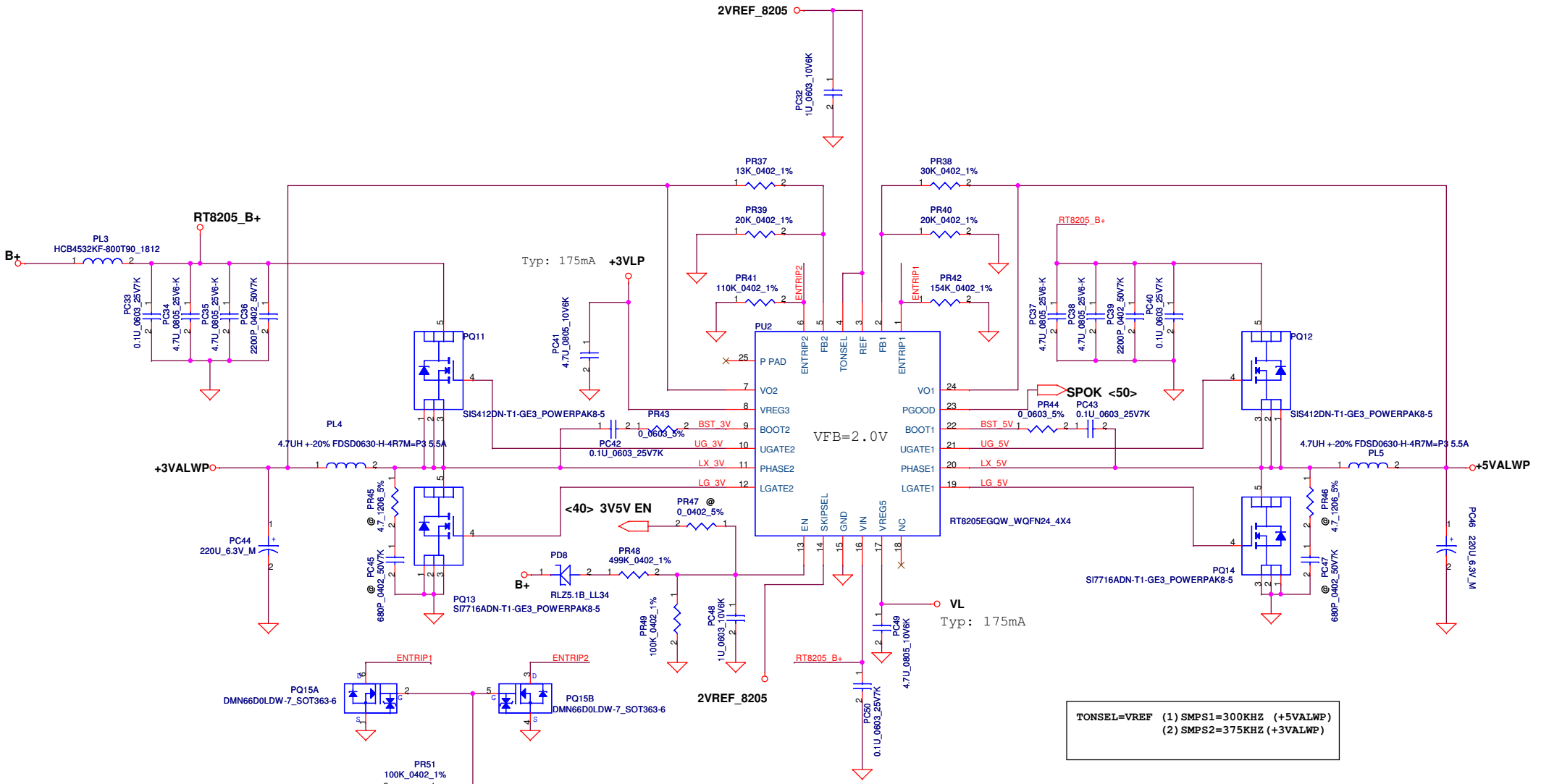
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: LA-7221P | Rev: 0.1

Date: Thursday, December 23, 2010 | Sheet 48 of 55



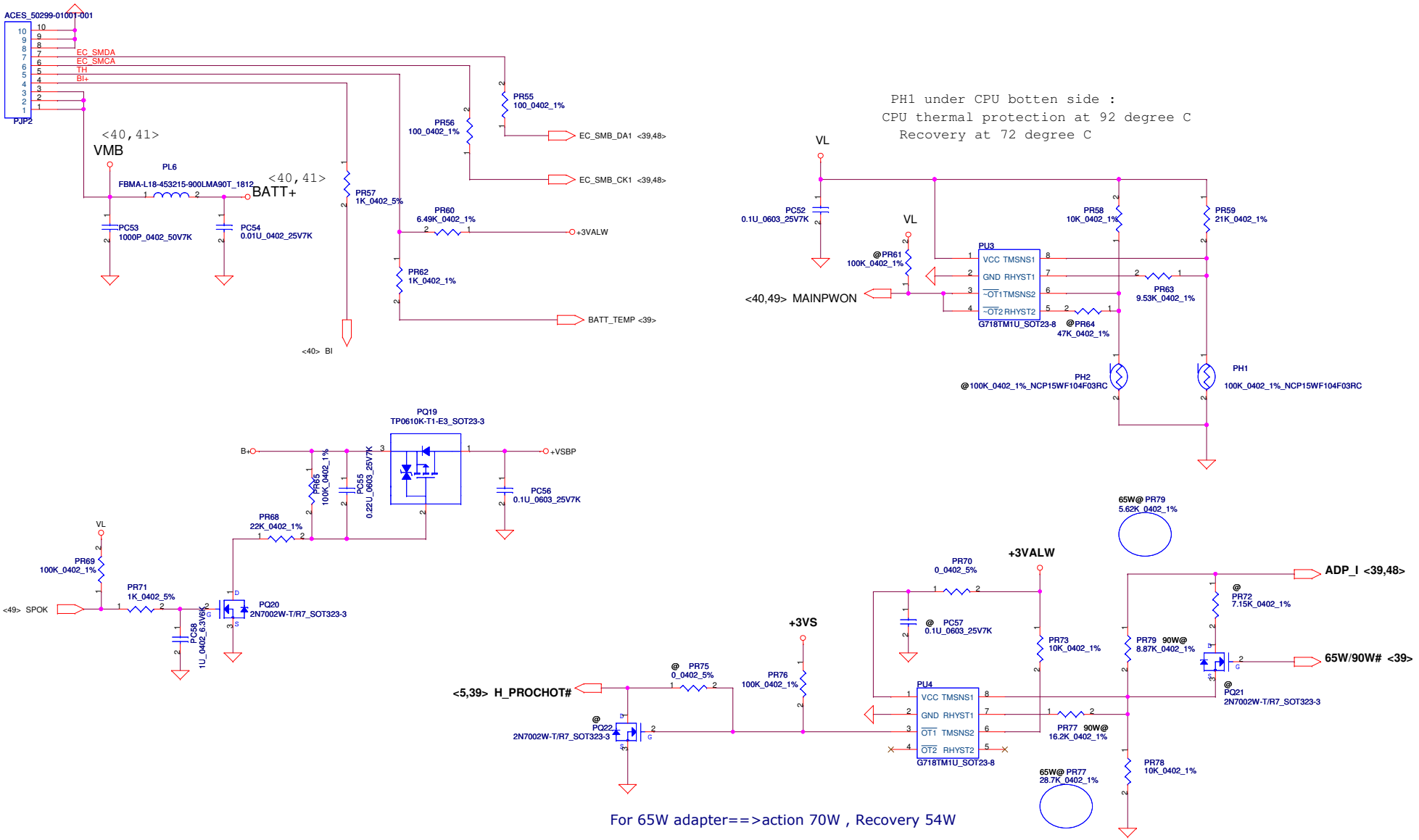
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	LA-7221P	0.1

Date: Thursday, December 23, 2010 Sheet 49 of 55



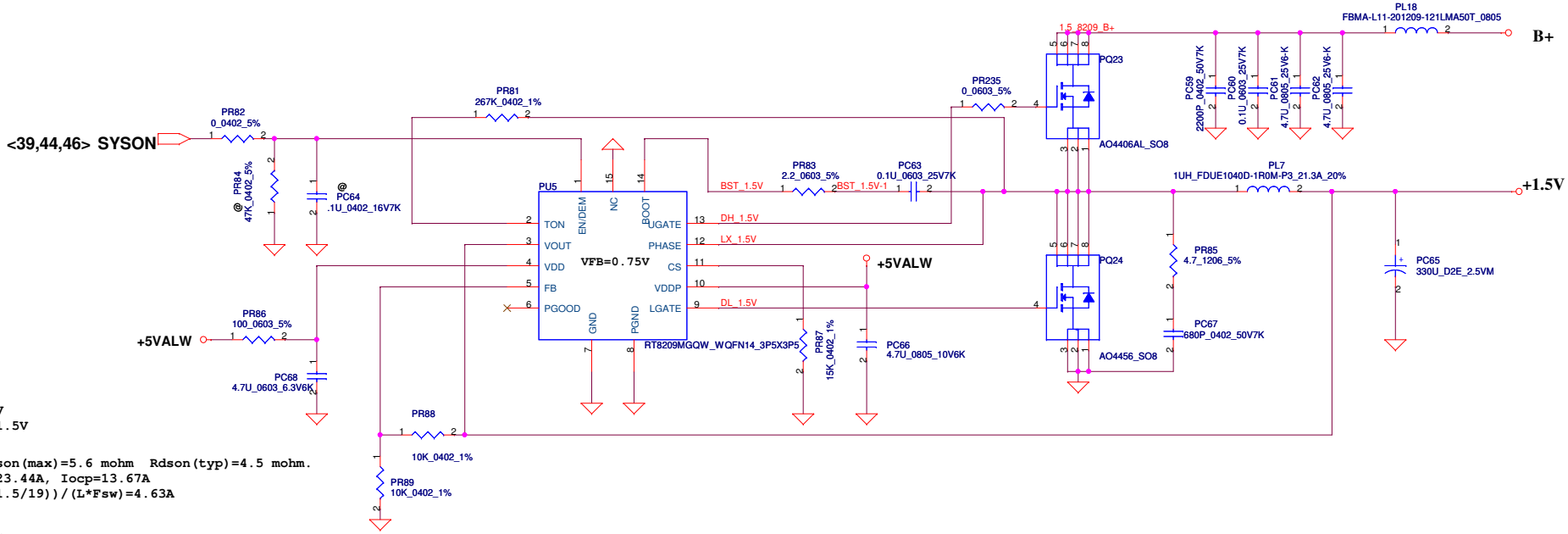
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: LA-7221P | Rev: 0.1

Date: Thursday, December 23, 2010 | Sheet 50 of 55



<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=19.53A, Imax=23.44A, Iocp=13.67A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+2.315A=35.65A
Iocpmin=((15K*9uA)/(0.0056*1.3))+2.315A=23.06A
Iocp=23.06A~35.65A

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

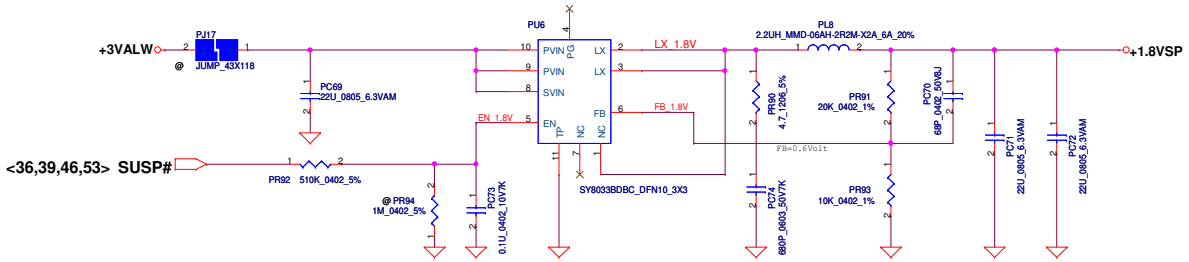
Compal Electronics, Inc.

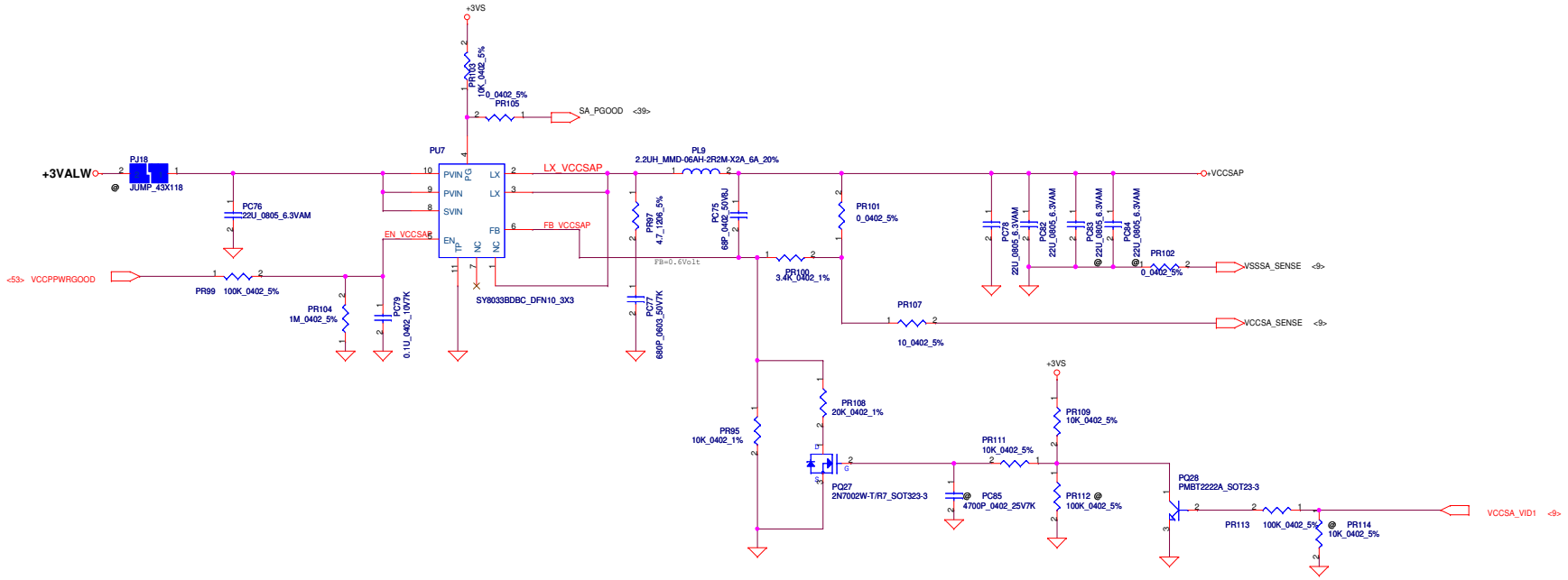
Title: PWR-+1.5VP

Size	Document Number	Rev
Custom	LA-7221P	0.1

Date: Thursday, December 23, 2010 | Sheet 51 of 55

1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ;Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V





VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

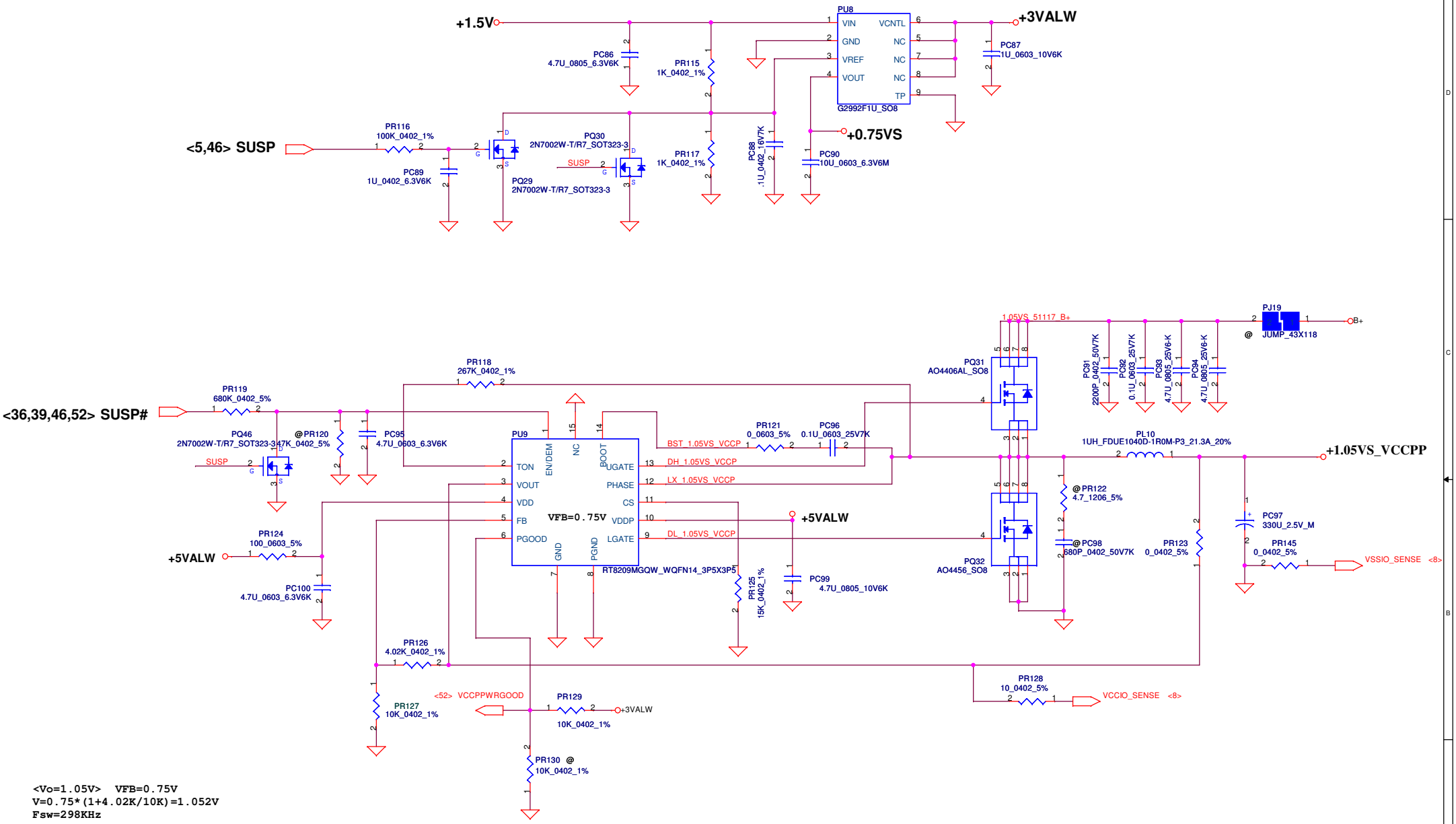
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size	Document Number	Rev
C	LA-7221P	0.1

Date: Thursday, December 23, 2010 | Sheet 52 of 55



<Vo=1.05V> VFB=0.75V
V=0.75*(1+4.02K/10K)=1.052V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=12.866A, Imax=9A, Iocp=15.439A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.33A
=>1/2Delta I=1.665A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+1.665A=37.62A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=23.02A
Iocp=23.02A~37.62A

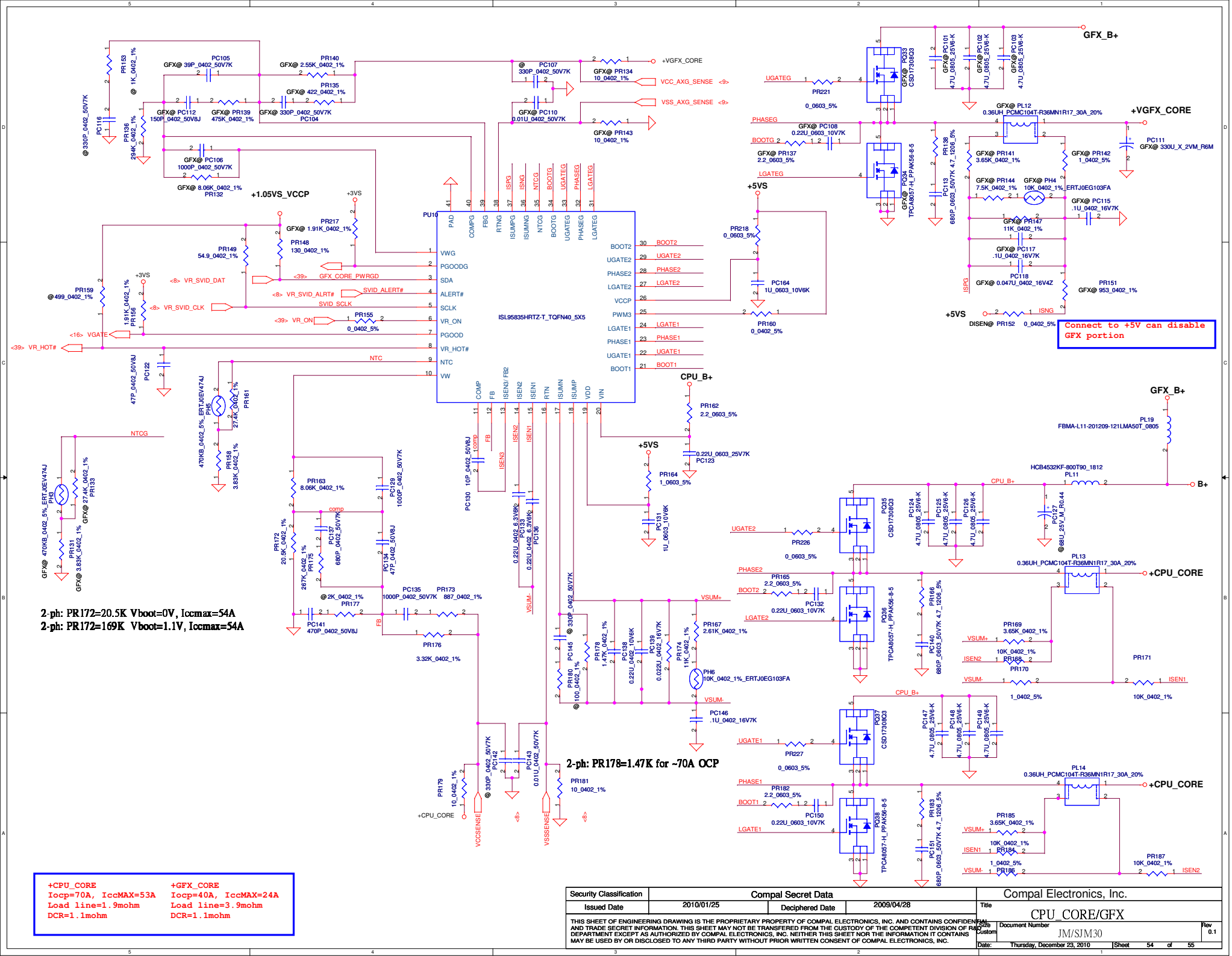
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

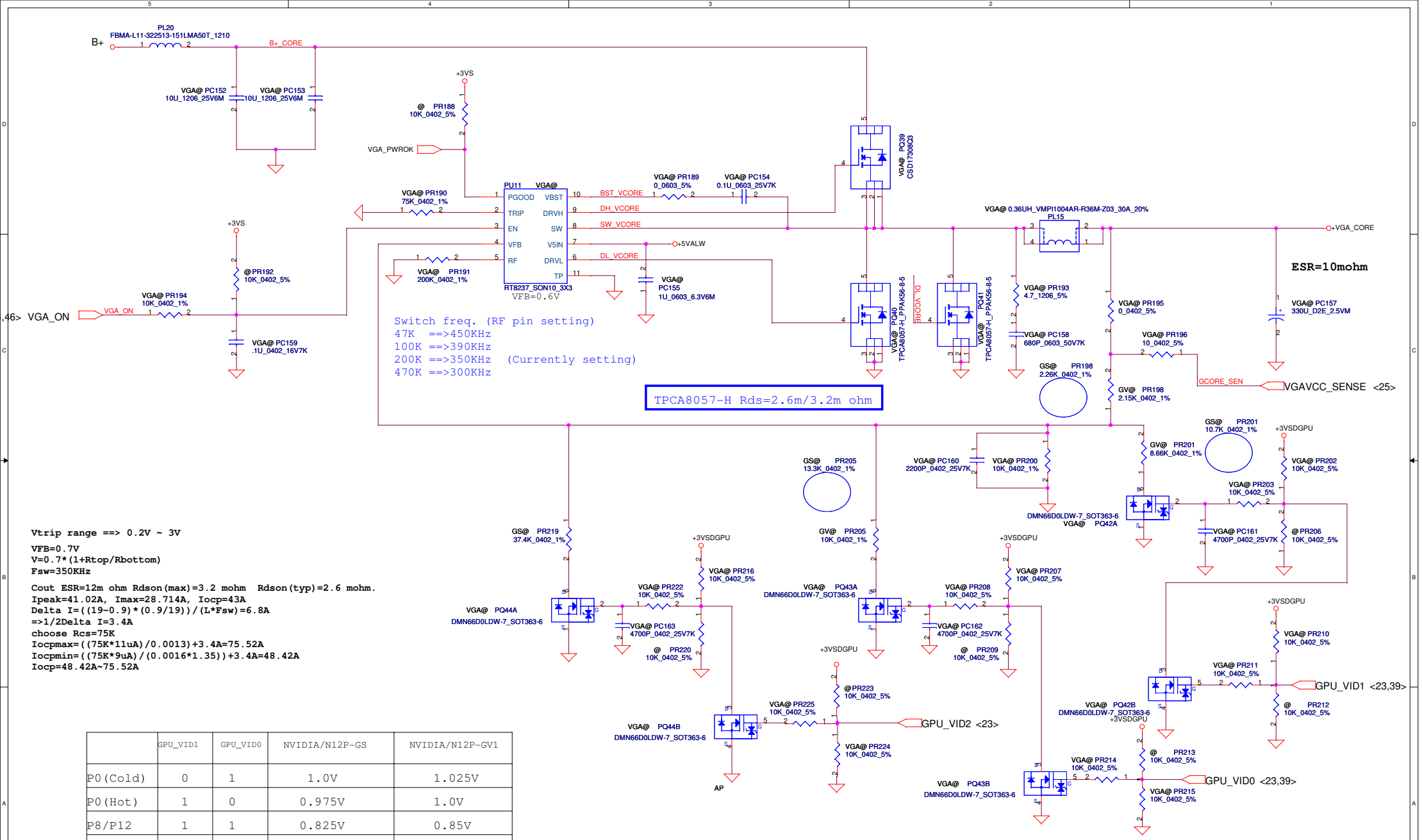
Title: PWR +1.05VS_VCCPP/+0.75VSP

Size	Document Number	Rev
Custom	LA-7221P	0.1

Date: Thursday, December 23, 2010 | Sheet 53 of 55



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/01/25	Deciphered Date	2009/04/28
Title	CPU_CORE/GFX		
Size: Custom	Document Number: JM/SJM30		Rev: 0.1
Date: Thursday, December 23, 2010	Sheet 54 of 55		



Vtrip range ==> 0.2V ~ 3V

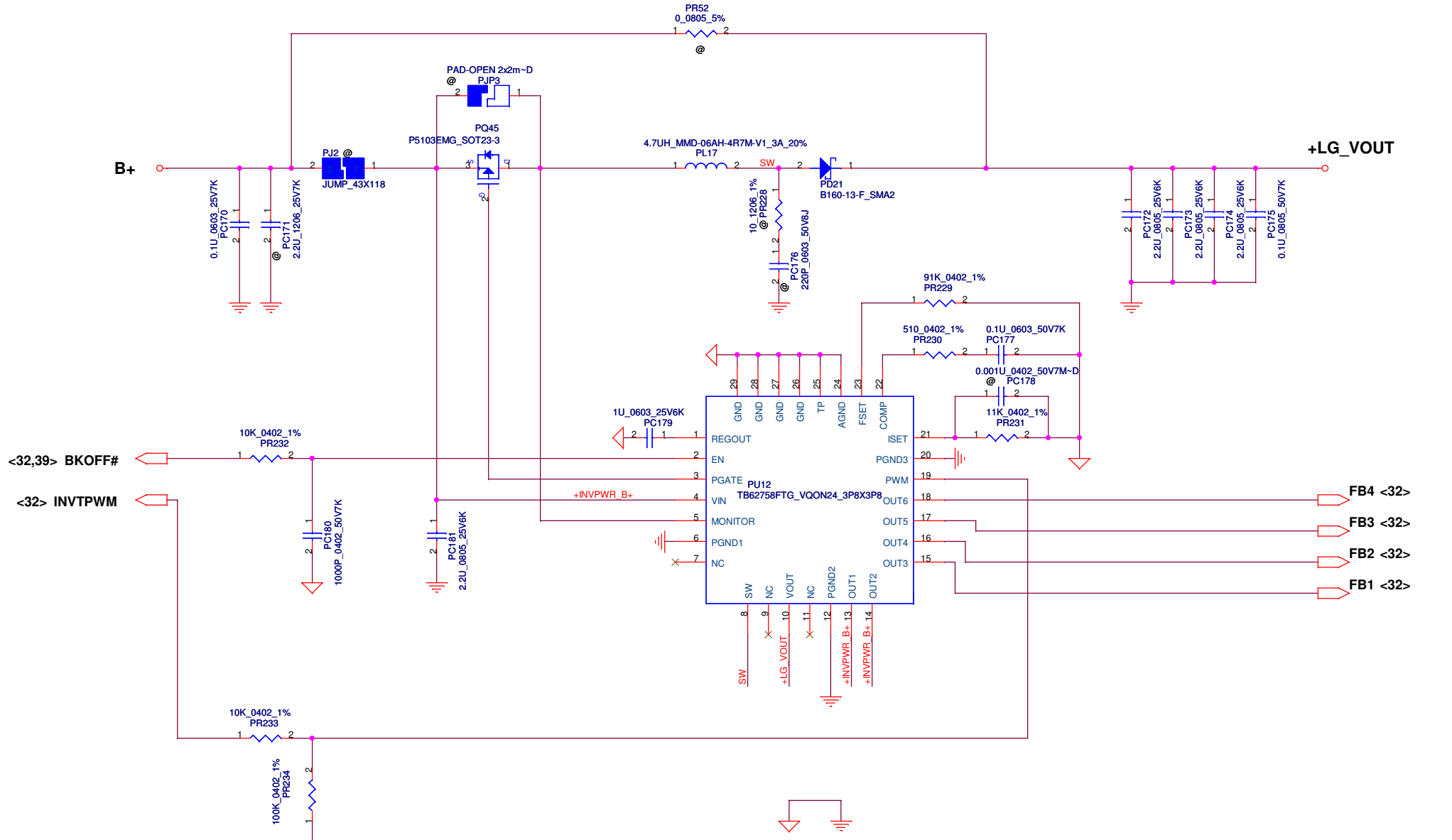
VFB=0.7V
V=0.7*(1+Rtop/Rbottom)
Fsw=350KHz

Cout ESR=12m ohm Rdson(max)=3.2 mohm Rdson(typ)=2.6 mohm.
Ipeak=41.02A, Imax=28.714A, Iocp=43A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A
=>1/2Delta I=3.4A
choose Rcs=75K
Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A
Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A
Iocp=48.42A~75.52A

	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P0(Cold)	0	1	1.0V	1.025V
P0(Hot)	1	0	0.975V	1.0V
P8/P12	1	1	0.825V	0.85V
ES	----	----	----	0.925V

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.			
Title	+VGA_COREP		
Size: Custom	Document Number: JM/SJM30		Rev: 0.1
Date: Thursday, December 23, 2010	Sheet 55 of 55		



Title	LED converter	
Size B	Document Number Toshiba(TB62758FTG)_LS5796_ES1	Rev X01
Date: Thursday, December 23, 2010	Sheet 56 of 56	