PF1/2/PF1Q BLOCK DIAGRAM

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

Daughter Board

- MMB Board
- USB Board
- Touch Pad board
- Switch board

DDRII-SODIMM1 PG 8,9
DDRII-SODIMM2 PG 8,9
DDR II 667 MHZ

AMD S1g2
Griffin Processor
(638 S1g2 socket)
PG 4,5,6,7

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

CLOCK GENERATOR
ICS9LPRS476AKLFT
SLG8SP628VTR
PG 3

HOST 200MHz
PCIE 100MHz
USB 48MHz
REF 14MHz

HT_LINK

LVDS
LVDS PG 19
LVDS(2ch)

DVI PG 18
CRT PG 18
MXM Module PG 20
PCI-E X16
HDMI PG 18

RX781/RS780MC
21mm X 21mm, 528pin BGA
PG 10,11,12,13

PCI-E, 1X (port2) → RTL8102EL(10/100) PG 23 → RJ45 PG 23
PCI-E, 1X (port0) / USB2.0 (P3) → Mini Card (WLAN) PG 24
PCI-E, 1X (port1) / USB2.0 (P8) → Mini Card (TV) PG 24
PCI-E, 1X (port3) / USB2.0 (P10) → NEW CARD PG 24
PCI-E, 1X (port4) → JMB380 PG 25 → Card Reader 4 IN 1 PG 25
IEEE1394 CN PG 25

A_LINK (X4)

SBSRC_CLK

SB700
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)

SATA - HDD1 PG 26 — SATA0
SATA - HDD2 PG 26 — SATA1
SATA - ODD PG 26 — SATA2
E - SATA PG 27 — SATA3

USB2.0 (P7) → USB2.0 I/O Ports X1 (MB) PG 27
USB2.0 (P0) → USB2.0 I/O Ports X1 (DB) PG 27
USB2.0 (P1) → USB2.0 I/O Ports X1 (DB) PG 27
USB2.0 (P6) → USB2.0 I/O Ports X1 (DB) PG 27

USB2.0 (P2) → CCD PG 27
USB2.0 (P9) → Bluetooth PG 27

Azalia

Azalia Audio Codec
ALC272/ALC268
PG 21

PORT-A
PORT-B

Speaker Amplifier G1441 PG 21

H.P/ JACK PG 22
MIC JACK PG 22
INT. MIC PG 22
INT. S.P. PG 21
WOOFER PG 22

Flash PG 26
PG 14,15,16,17,18

LPC

EC
IT8512
PG 28

SPI

FAN PG 6
Keyboard PG 29
Flash ROM PG 28
Touch Pad PG 27
CIR PG 28

CPU_CORE1
CPU_CORE2
CPU VDDNB_CORE
→ **CPU CORE**

NB_CORE
→ **NB CORE** (1.0~1.1V)

RVCC1.2
VCC1.2
→ **RVCC1.2**

1.8VSUS
VCC1.8
SMDDR_VTERM
VCC1.5
1.1V_NB
→ **1.8VSUS SMDDR VTERM**

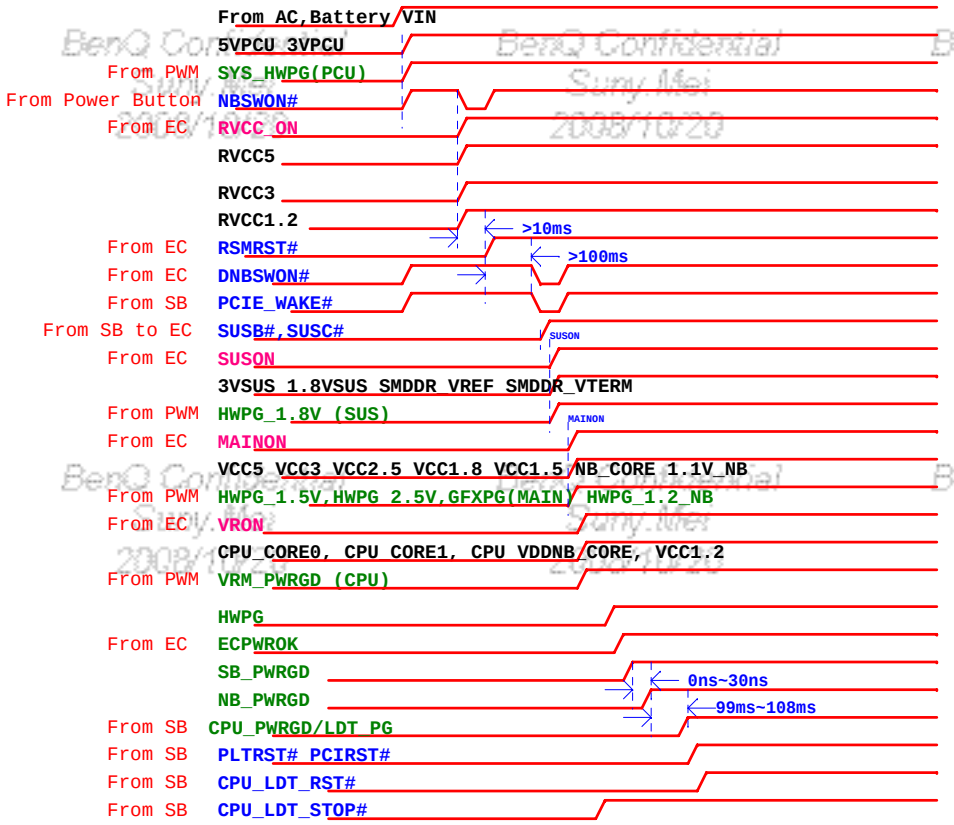
3VPCU
RVCC3
3VSUS
VCC3
5VPCU
5VSUS
VCC5
VCC2.5
→ **3V/5V**

PROJECT : PF1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	2A

Date: Wednesday, June 11, 2008 Sheet 1 of 40

PF1 Power On Sequence



BOM naming rule

Items	Function	BTO	Name	Description
1	UMA	v	IV@	Internal VGA stuff
2	Discrete VGA	v	EV@	External VGA stuff
3	Subwoofer	v	WF@	Only for PF2P
4	IEEE 1394	v	EV@	External VGA model stuff
5	DVI-I	v	EV@	External VGA model stuff
6	D-SUB(CRT)	v	IV@	Internal VGA model stuff
7	HDMI	v	EV@	External VGA model stuff
8	CIR	v	CIR@	For PF1P and PF2P(M86)
9	TV		TV@	For PF1P and PF2P(M86)
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				
24				
25				

*Note: EC will sampling SUSB# & SUSC# every 5ms.

AMD SB700 SMBUS Table

	CLK GEN	RAM	Mini Card (TV)	Mini-card(WL)	New Card	HDMI
SB700 SDATA0/SCLK0(VCC3)	V	V	V	V	V	
SB700 SDATA1/SCLK1(3V_S5)						V
SB700 SDATA2/SCLK2(3V_S5)						
Power	VCC3	VCC3	VCC3	VCC3(Atheros)	VCC3	RVCC3
Reserve MOS ckt	V	V	V	V	V	V

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM	VGA thermal Sensor	Touch Sensor	HDMI CEC
EC775 SDATA1/SCLK1(3VPCU)	V					
EC775 SDATA2/SCLK2(3VPCU)		V	V			
EC775 SDATA3/SCLK3(3VPCU)				V	V	V
EC775 SDATA4/SCLK4(3VPCU)						
Power	3VPCU	VCC3	3VPCU	VCC3	3VPCU	5VPCU
Reserve MOS ckt	X	V	X	V	X	V

PROJECT : PF1
Quanta Computer Inc.
Size: Document Number: SYSTEM INFORMATION Rev: 2A
Date: Wednesday, June 11, 2008 Sheet 2 of 40

CLK_GEN_SLG8SP628

ICS9LPRS480 P/N : ALPRS480000

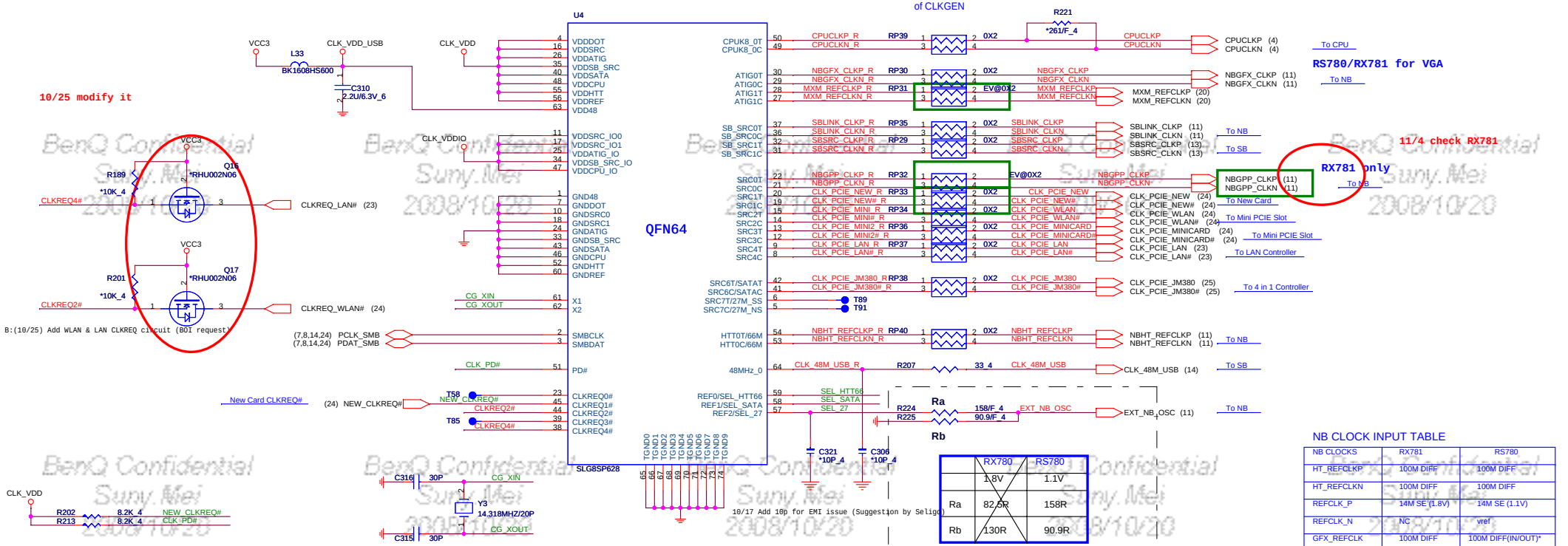
SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN

10/25 modify it

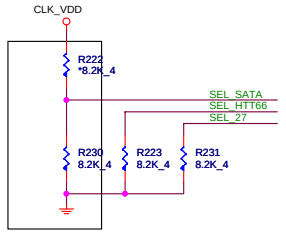


	RX780 1.8V	RX780 1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

NB CLOCK INPUT TABLE

NB CLOCKS	RX781	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF



SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

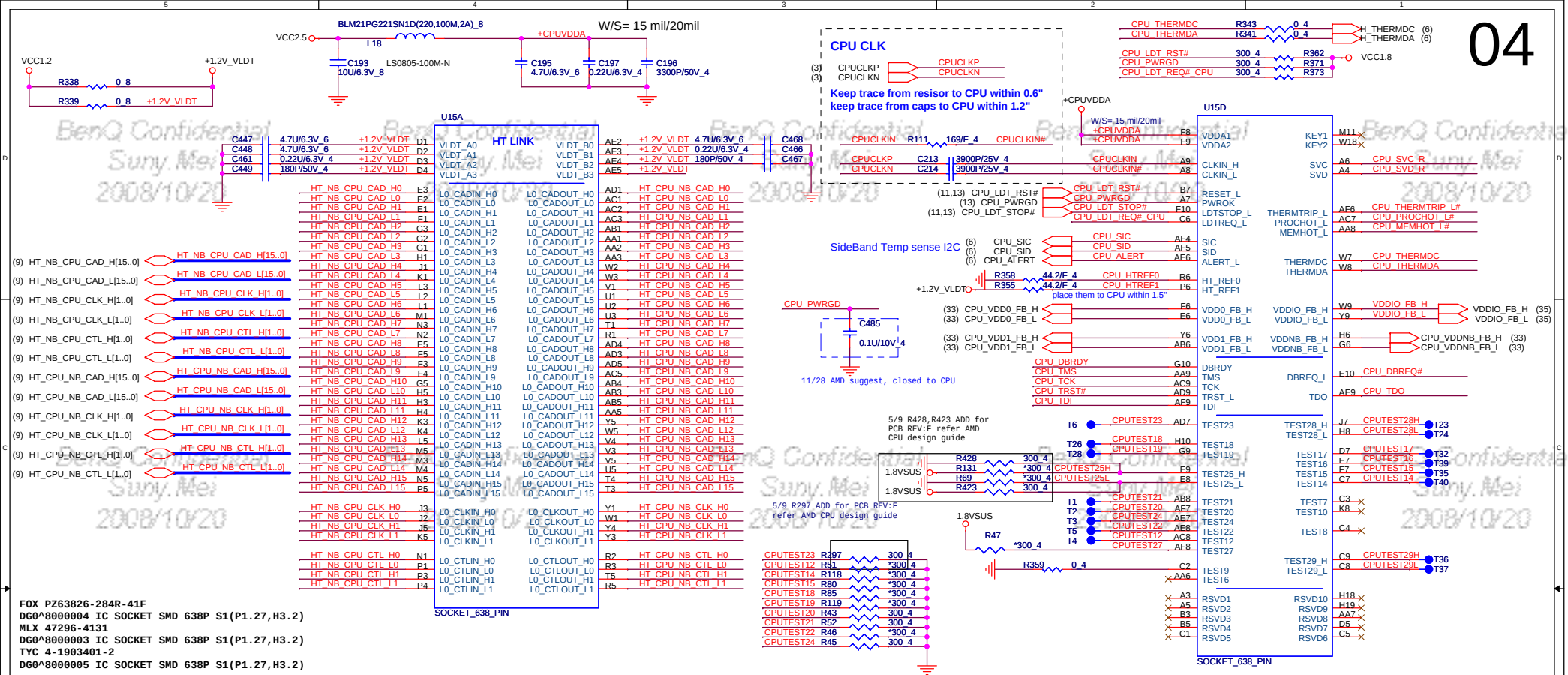
* default

CLOCKS name	RX781	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP30 STUFF	RP30 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP31 STUFF	RP31 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP32 STUFF	RP32 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP35 STUFF	RP35 STUFF	to NB for AC-LINK reference clock

PROJECT : PF1

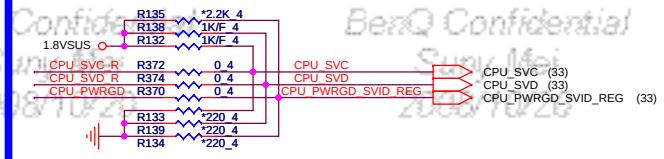
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR_SLG8SP628	1A
Date: Wednesday, June 11, 2008	Sheet 3 of 40	



FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

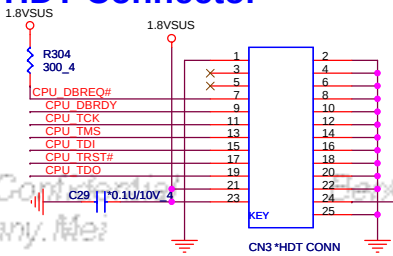
Serial VID

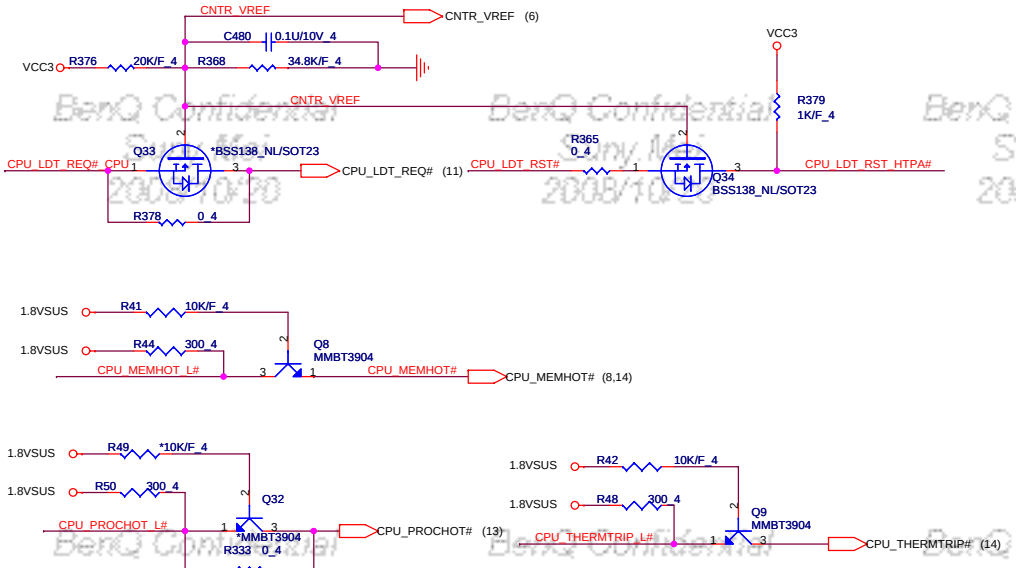


VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

HDT Connector





PROJECT : PF1
Quanta Computer Inc.

Size	Document Number	Rev
	S1G2 HT,CTL I/F 1/3	1A
Date: Wednesday, June 11, 2008	Sheet 4 of 40	

Processor Memory Interface

05

PLACE THEM CLOSE TO CPU WITHIN 1"

U15B — MEM:CMD/CTRL/CLK

SOCKET_638_PIN

U15C — MEM:DATA

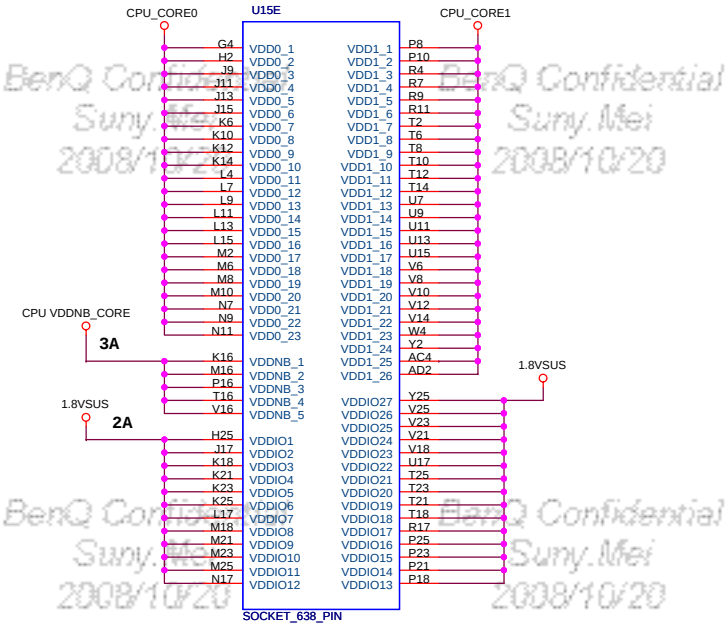
SOCKET_638_PIN

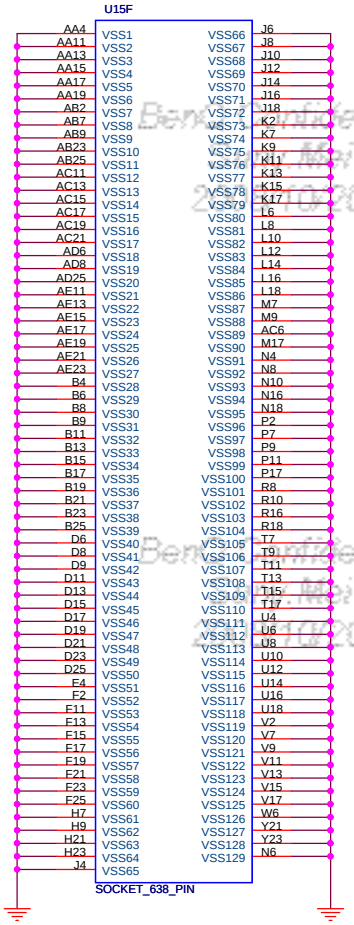
Place close to socket

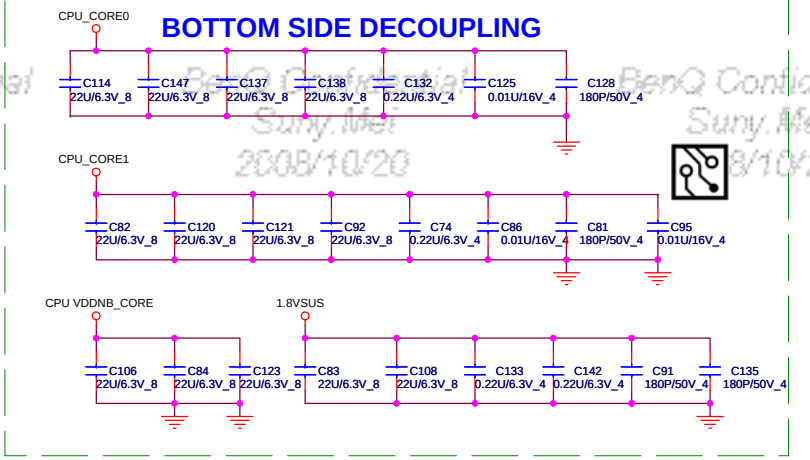
Close to CPU within 1500 mils

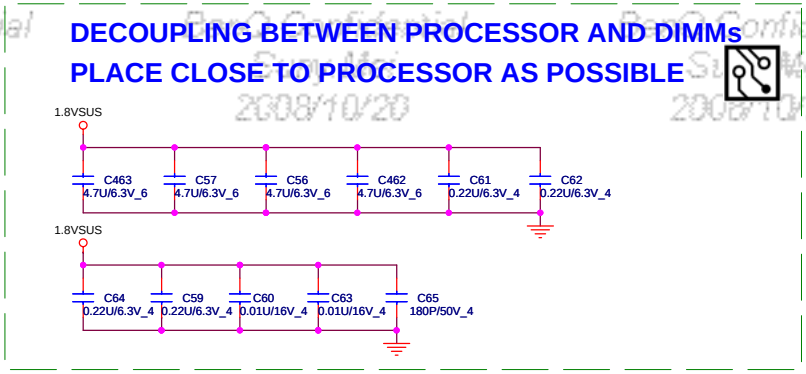
PROJECT : PF1	
Quanta Computer Inc.	
Size	Document Number: S1G2 DDRII MEMORY I/F 2/3 — Rev: 1A
Date: Wednesday, June 11, 2008	Sheet 5 of 40

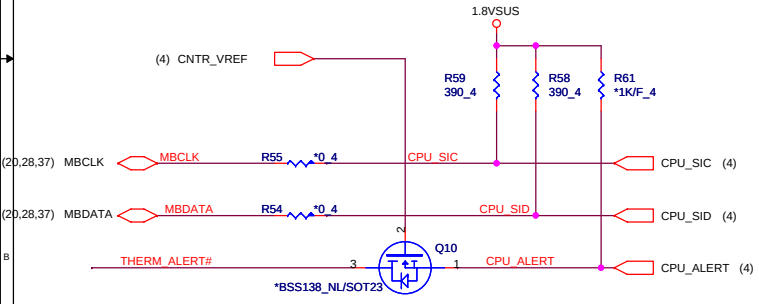
PROCESSOR POWER AND GROUND

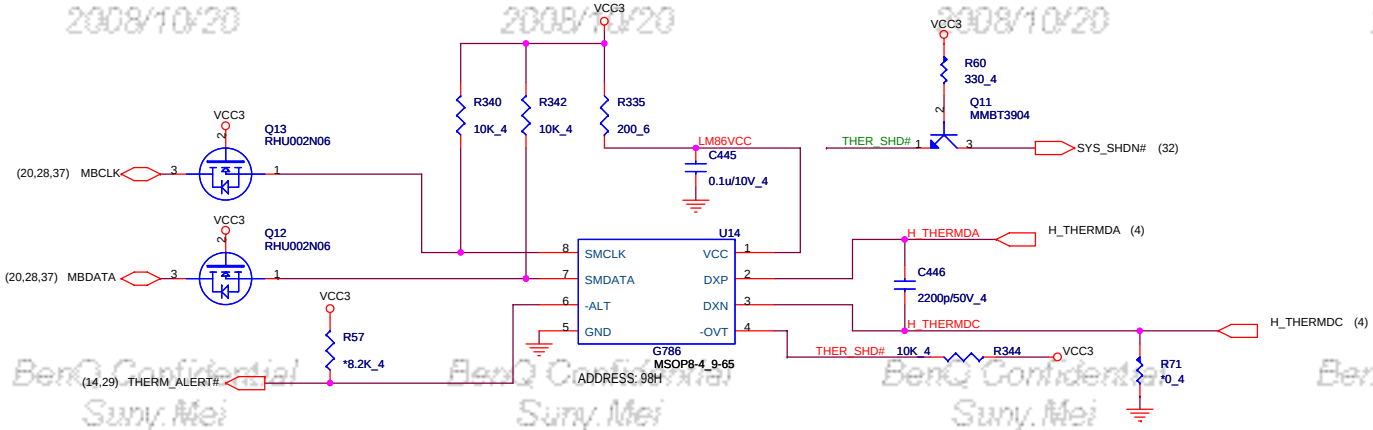


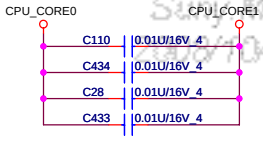








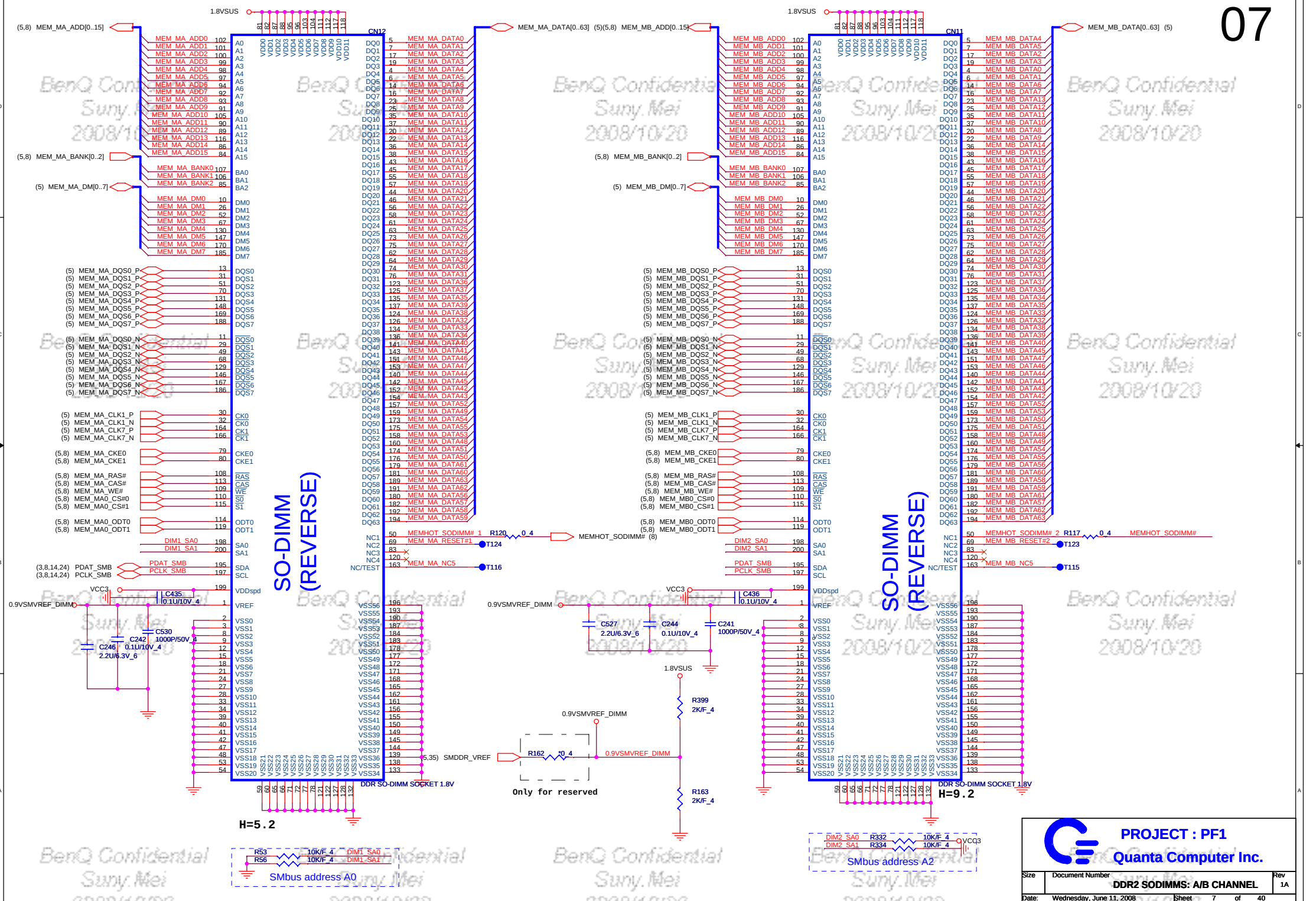




PROJECT : PF1

Quanta Computer Inc.

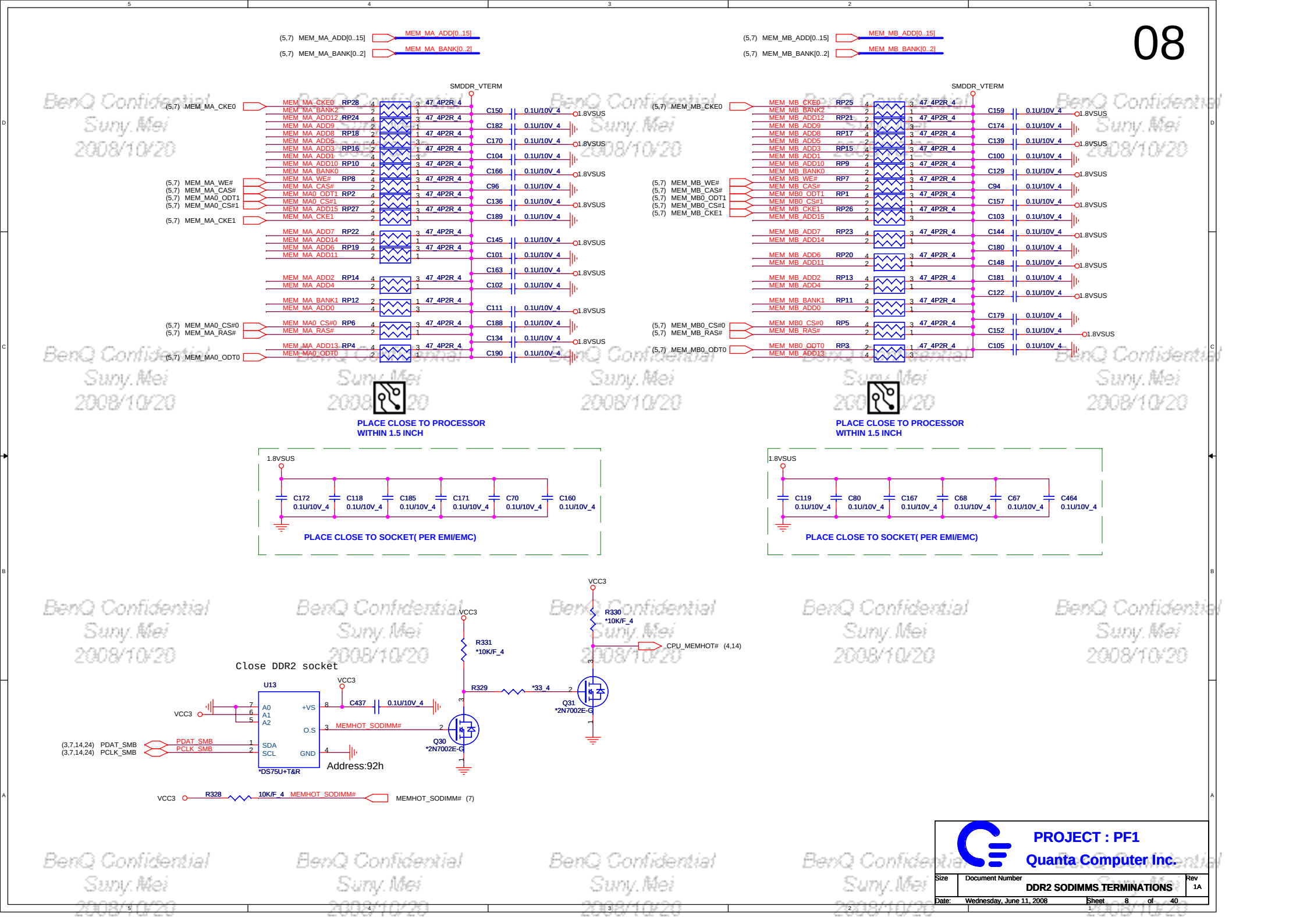
Size	Document Number	Rev
	S1G2 PWR & GND 3/3	1A
Date: Wednesday, June 11, 2008	Sheet 6 of 40	



PROJECT : PF1

Quanta Computer Inc.

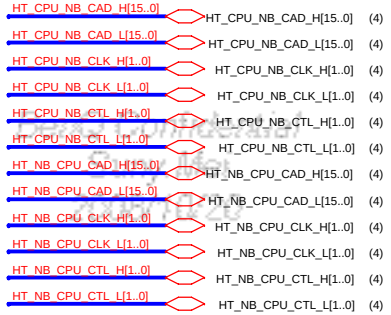
Size	Document Number	Rev
	DDR2 SODIMMS: A/B CHANNEL	1A
Date: Wednesday, June 11, 2008	Sheet 7 of 40	



PROJECT : PF1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SODIMMS TERMINATIONS	1A
Date: Wednesday, June 11, 2008	Sheet 8 of 40	

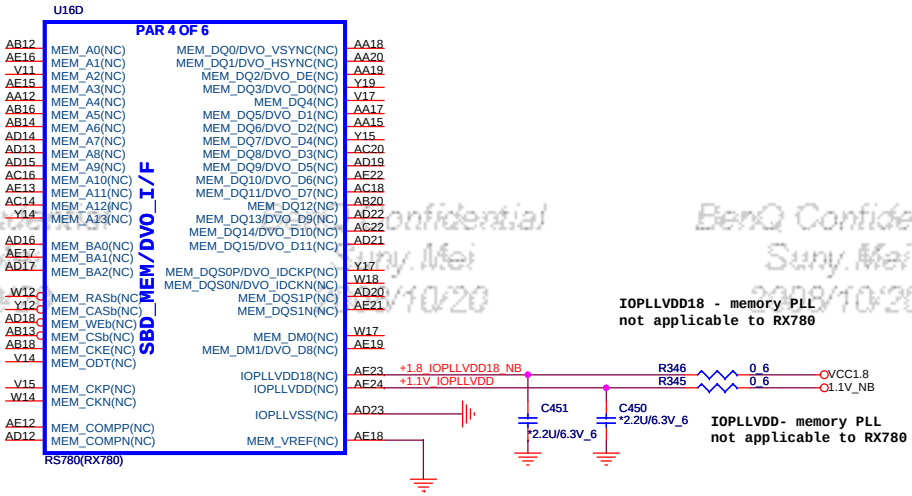


signals	RS780	RX781
HT_TXCALP	R351 300 ohm 1%	R351 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R352 300 ohm 1%	R352 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

This block is for UMA RS780 only , RX781 can remove all component

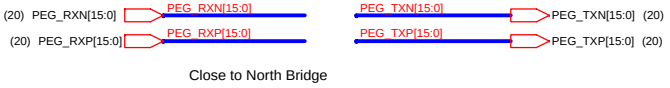


IOPLLVDD18 - memory PLL not applicable to RX780

IOPLLVDD- memory PLL not applicable to RX780

PROJECT : PF1
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-HT LINK I/F 1/5	1A
Date: Wednesday, June 11, 2008	Sheet 9 of 40	

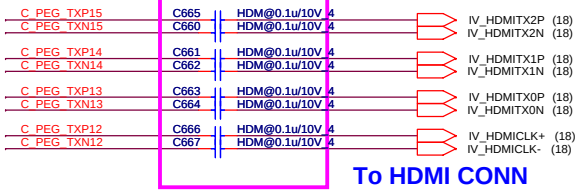


Close to North Bridge

Close to North Bridge

BTO

Close to North Bridge



To HDMI CONN

TO WLAN
TO MINI CARD
TO PCIE-LAN
TO EPRESS CARD
TO CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT : PF1

Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-PCIE I/F 2/5	1A
Date: Wednesday, June 11, 2008	Sheet 10 of 40	

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

RX780
(4,13) CPU_LDT_RST# — R75 *0_4 — NB_RST# IN
RS780
(13) NB_PLTRST# — R79 0_4
North Bridge RESET

RX780
VCC3 — R104 4.7K_4 — INT_CRT_DDCDAT
R105 4.7K_4 — INT_CRT_DDCCLK
11/30 add 2K pull up to DDCDAT /DDCCLK to VCC3 for RX780

11/4 no stuff for RS780M/MC/RX781

+NB_CORE_ON — R103 *10K/F_4 — VCC3
R93 *10K/F_4

U16C
PART 3 OF 6
RS780(RX780)

CRT/TVOUT
AVDD1(NC) F12
AVDD2(NC) F12
AVDDI(NC) F14
AVSSDI(NC) G15
AVDDQ(NC) H15
AVSSQ(NC) H14
C_Pr(DFT_GPIO5) E17
Y(DFT_GPIO2) F17
COMP_Pb(DFT_GPIO4) F15
RED(DFT_GPIO0) G18
REDb(NC) G17
GREEN(DFT_GPIO1) E18
GREENb(NC) F18
BLUE(DFT_GPIO3) E19
BLUEb(NC) F19
DAC_HSYNC(PWM_GPIO4) A11
DAC_VSYNC(PWM_GPIO6) B11
DAC_SDA(PCE_TCALRN) E8
DAC_SCL(PCE_RCALRN) F8
DAC_RSET(PWM_GPIO1) G14

PLL PWR
PLLVDD(NC) A12
PLLVDD18(NC) D14
PLLVSS(NC) B12
VDDA18HTPLL H17
VDDA18PCIEPLL1 D7
VDDA18PCIEPLL2 E7

PM
SYSRESETb D8
POWERGOOD A10
LDTSTOPb C10
ALLOW_LDTSTOP C12

CLOCKs
HT_REFCLKP C25
HT_REFCLKN C24
REFCLK_P/OSCIN(OSCIN) E11
REFCLK_N(PWM_GPIO3) E11
GFX_REFCLKP T2
GFX_REFCLKN T1
GPP_REFCLKP U1
GPP_REFCLKN U2
GPPSB_REFCLKP(SB_REFCLKP) V4
GPPSB_REFCLKN(SB_REFCLKN) V3

MIS.
I2C_DATA A9
I2C_CLK B9
DDC_DATA/AUXON(NC) B8
DDC_CLK/AUX0P(NC) A8
AUX1P(NC) B7
AUX1N(NC) A7
STRP_DATA B10
RSVD G11
AUX_CAL(NC) C8

LVTM
TXOUT_L0P(NC) A22
TXOUT_L0N(NC) B22
TXOUT_L1P(NC) A21
TXOUT_L1N(NC) B21
TXOUT_L2P(NC) B20
TXOUT_L2N(DBG_GPIO0) A20
TXOUT_L3P(NC) A19
TXOUT_L3N(DBG_GPIO2) B19
TXOUT_U0P(NC) B18
TXOUT_U0N(NC) A18
TXOUT_U1P(PCIE_RESET_GPIO3) A17
TXOUT_U1N(PCIE_RESET_GPIO2) B17
TXOUT_U2P(NC) D20
TXOUT_U2N(NC) D21
TXOUT_U3P(PCIE_RESET_GPIO5) D18
TXOUT_U3N(NC) D19
TXCLK_LP(DBG_GPIO1) B16
TXCLK_LN(DBG_GPIO3) A16
TXCLK_UP(PCIE_RESET_GPIO4) D16
TXCLK_UN(PCIE_RESET_GPIO1) D17
VDDLTP18(NC) A13
VSSLTP18(NC) B13
VDDLT18_1(NC) A15
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22
LVDS_DIGON(PCE_TCALRP) E9
LVDS_BLON(PCE_RCALRP) E7
LVDS_ENA_BL(PWM_GPIO2) G12
TMDS_HPD(NC) D9
HPD(NC) D10
TVCLKIN(PWM_GPIO5) D12
THERMALDIODE_P AE8
THERMALDIODE_N AD8
TESTMODE D13

+3V_AVDD_NB — +1.8V_AVDDDI_NB — +1.8V_AVDDQ_NB
INT_TV_C/R — T34 T21 T29
(18) INT_CRT_RED — R89 IV@150/F_4 — INT_CRT_RED
(18) INT_CRT_GRN — R91 IV@150/F_4 — INT_CRT_GRN
(18) INT_CRT_BLU — R90 IV@150/F_4 — INT_CRT_BLU
(18) INT_HSYNC — INT_HSYNC
(18) INT_VSYNC — INT_VSYNC
(18) INT_CRT_DDCDAT — DDCDATA_INT
(18) INT_CRT_DDCCLK — DDCCLK_INT
R68 IV@715/F_6 — DAC_RSET_NB
+1.1V_PLLVDD — +1.8V_PLLVDD18 — +1.8V_VDDA18HTPLL — +1.8V_VDDA18PCIEPLL
(17) NB_PWRGD_IN — NB_RST# IN — NB_PWRGD_IN — NB_LDT_STOP# — NB_ALLOW_LDTSTOP
(3) NBHT_REFCLKP — NBHT_REFCLKP
(3) NBHT_REFCLKN — NBHT_REFCLKN
(3) EXT_NB_OSC — R95 0_4 NB_REFCLK_P — R94 0_4 NB_REFCLK_N
1.1V_NB — R100 4.7K_4 RS780 R101 4.7K_4
(3) NBGFX_CLKP — NBGFX_CLKP
(3) NBGFX_CLKN — NBGFX_CLKN
(3) NBGPP_CLKP — NBGPP_CLKP
(3) NBGPP_CLKN — NBGPP_CLKN
(3) SBLINK_CLKP — SBLINK_CLKP
(3) SBLINK_CLKN — SBLINK_CLKN
(19) INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA
(19) INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK
(18) IV_HDMI_DDCDATA — IV_HDMI_DDCDATA
(18) IV_HDMI_DDCCLK — IV_HDMI_DDCCLK
T30 T31 — RS740_DFT_GPIO1
(34) +NB_CORE_ON — R97 0_4 STRP_DATA
T33 — RS780_AUX_CAL — C8

INT_TXLOUT0+ (19) — INT_TXLOUT0- (19) — INT_TXLOUT1+ (19) — INT_TXLOUT1- (19) — INT_TXLOUT2+ (19) — INT_TXLOUT2- (19)
T120 T121
INT_TXUOUT0+ (19) — INT_TXUOUT0- (19) — INT_TXUOUT1+ (19) — INT_TXUOUT1- (19) — INT_TXUOUT2+ (19) — INT_TXUOUT2- (19)
T119 T122
INT_TXCLKOUT+ (19) — INT_TXCLKOUT- (19) — INT_TXUCLKOUT+ (19) — INT_TXUCLKOUT- (19)
+1.8V_VDDLTP18_NB
+1.8V_VDDLT_18_NB
+3V_VDLT33_NB
VSSLT1(VSS) — VSSLT2(VSS) — VSSLT3(VSS) — VSSLT4(VSS) — VSSLT5(VSS) — VSSLT6(VSS) — VSSLT7(VSS)

RS780 only 1/01 exchange LVDS_PWM /LVDS_BLON
INT_LVDS_DIGON (19)
INT_LVDS_BLON (19)
R78 EV@1.27K/F_4
R77 EV@1.27K/F_4
For RX780 only

TMDS_HPD0 — T27 T22
SUS_STAT#_NB — R113 0_4 — SUS_STAT# (14)
R_NB_THRMDA — T118
R_NB_THRMDC — T117
TEST_EN — R96 1.82K/F_4

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT
RX780: RS780_AUX_CAL — R83 3K_4

Enables Debug Bus acess through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)
RS780: INT_VSYNC — R116 3K_4 — VCC3

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)
RS780: INT_HSYNC — R114 3K_4 — VCC3; R106 *3K_4

For extrnal EEPROM Debug only
RS780/RX780: STRP_DATA — R92 *10K/F_4 — +VDDG_NB; R84 2.2K/F_4

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780
RX780: INT_TV_C/R — R88 *3K_4
Reserved only

RX780 -->NC / RS780 --- ADD

VCC3 — L21 BLM18PG221SN1D(220,1.4A)_6 — +3V_AVDD_NB
AVDD-DAC Analog not applicable to RX780
C199 2.2U/6.3V_6

1.1V_NB — BLM18PG221SN1D(220,1.4A)_6 — +1.1V_PLLVDD
L13
C162 2.2U/6.3V_6
PLLVDD - Graphics PLL not applicable to RX780

VCC1.8 — L22 BLM18PG221SN1D(220,1.4A)_6 — +1.8V_PLLVDD18
C200 10U/6.3V_8
C151 2.2U/6.3V_6
PLLVDD18 - Graphics PLL not applicable to RX780

VCC1.8 — R82 0_6 — +1.8V_AVDDDI_NB
C143 2.2U/6.3V_6
AVDDI-DAC Digital not applicable to RX780

BLM18PG221SN1D(220,1.4A)_6 — +1.8V_AVDDQ_NB
L11
C165 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

VCC1.8 — IV@BLM18PG221SN1D(220,1.4A)_6 — +1.8V_VDDLTP18_NB
L14
C153 IV@2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

BLM21PG221SN1D(220,100M,2A)_8 — +1.8V_VDDLT_18_NB
L16
C175 IV@4.7U/6.3V_6
C164 IV@0.1U/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

VCC1.8 — VDDA18PCIEPLL -PCIE PLL
L10 — 20mils width — +1.8V_VDDA18PCIEPLL — BLM18PG221SN1D(220,1.4A)_6
C154 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
L19 — 20mils width — +1.8V_VDDA18HTPLL — BLM18PG221SN1D(220,1.4A)_6
C127 2.2U/6.3V_6

VCC1.8 — R122 300_4 — Q14 *BSS138_NL/SOT23 — R126 *4.7K_4 — +VDDG_NB
(4,13) CPU_LDT_STOP# — NB_LDT_STOP#
R125 0_4
RX780

VCC1.8 — Q15 *BSS138_NL/SOT23 — R108 *4.7K_4 — +VDDG_NB
RS780
(4) CPU_LDT_REQ# — R129 0_4 — NB_ALLOW_LDTSTOP
(13) ALLOW_LDTSTOP — R121 0_4
RX780

RX780: R124 EV@0_6 — VCC1.8 — +VDDG_NB
RS780: R123 IV@0_6 — VCC3

VCC3 — L15 — +3V_VDLT33_NB
*BLM21PG221SN1D(220,100M,2A)_8 — C177 *2.2U/6.3V_6
VDDLT33 - LVDS or DVI/HDMI ANALOG RS740 only

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Quanta Computer Inc.
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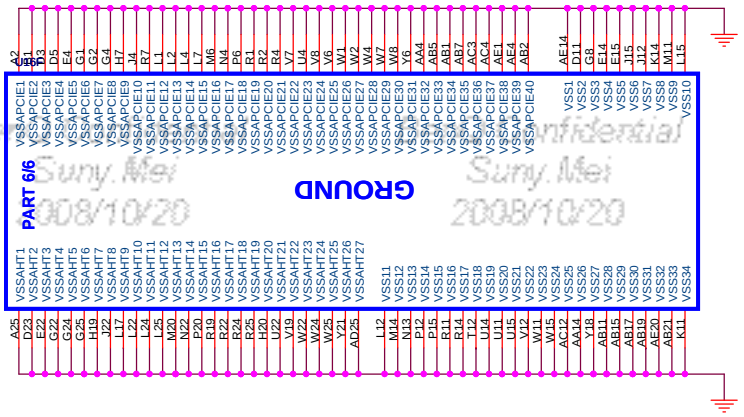
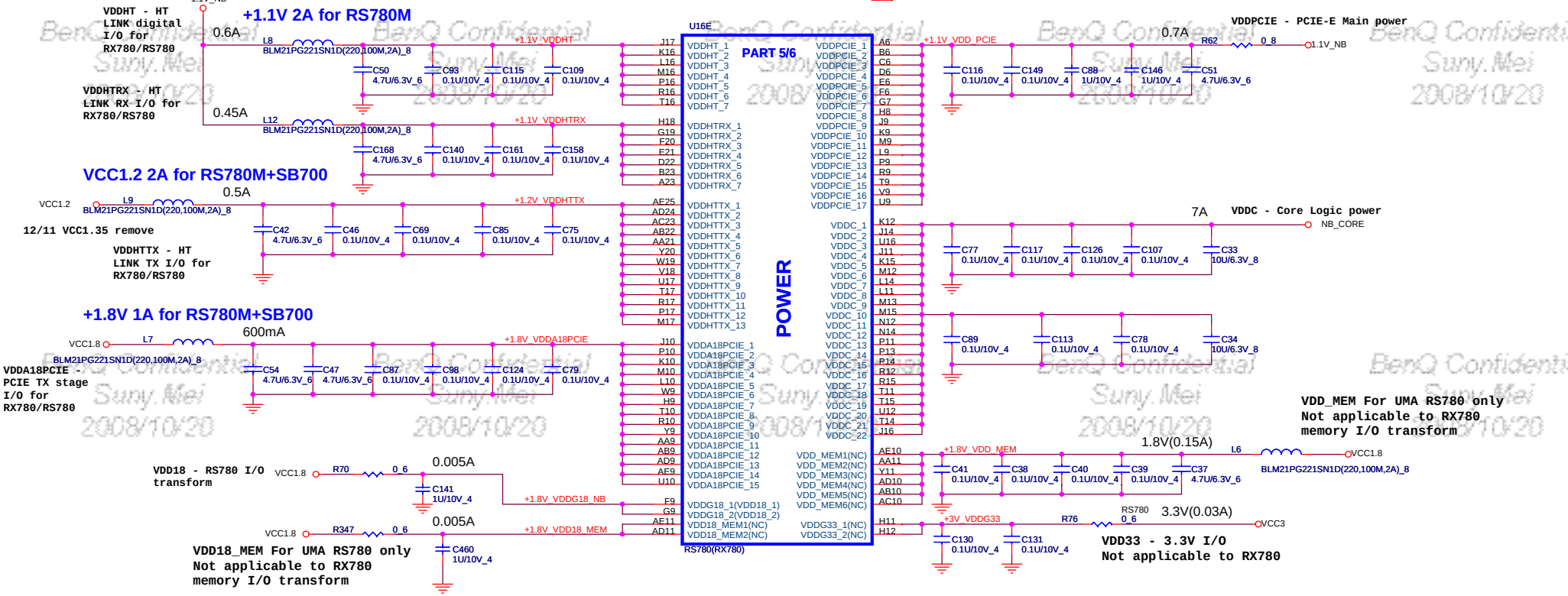
RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



(3,4,13,15,16,30,34,37) VCC1.2
(3,4,6,7,8,11,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,32,33,36) VCC3
(4,9,11,13,16,17,25,26,35,36) VCC1.8

(9,10,11,36) 1.1V_NB
(30,34) NB_CORE



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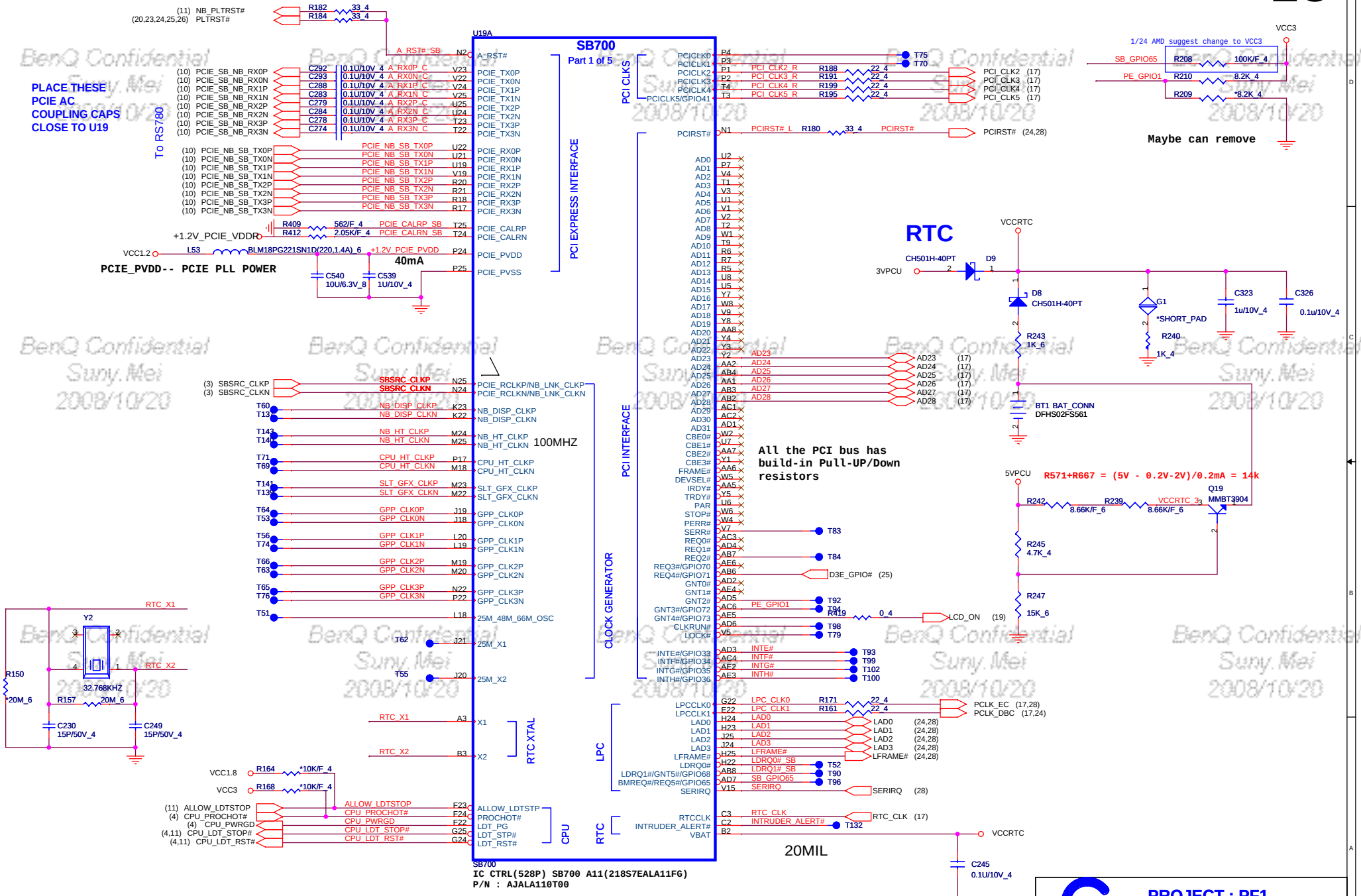

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Size	Document Number	Rev
	SB700-PCIE/PCI/CPU/LPC 1/4	1A
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NC only ,Can't be install

RVCC3
R169 *2.2K_4 SB_TEST0
R170 *2.2K_4 SB_TEST1
R172 *2.2K_4 SB_TEST2

RVCC3
R398 *10K/F_4 SWI#

VCC3 SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R219 2.2K_4 PCLK_SMB
R218 2.2K_4 PDAT_SMB
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

RVCC3 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R401 10K/F_4 SB_SMBCLK1
R400 10K/F_4 SB_SMBDATA1
Wlan Card

RVCC3 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R156 10K/F_4 SB_SCLK2
R152 10K/F_4 SB_SDATA2
epress card

VCC3
R176 4.7K_4 SUS_STAT#

U19D

SB700 Part 4 of 5

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

T135 RI#
T134 SLP_S2
T54 SUSB#
(28) SUSB#
(28) SUSC#
(28) DNBSWON#
(17) SB_PWRGD_IN
(11) SUS_STAT#
SB_TEST2
SB_TEST1
SB_TEST0
(28) GATEA20
(28) RCIN#
(28) SCI#
(28) KBSMI#
T158
SYS_RST#
(23,24) PCIE_WAKE#
(28) SWI#
(4) CPU_THERMTRIP#
(17) WD_PWRGD
(28) RSMRST#
R165 0_4 SWI#_C
R154 0_4 RSMRST#_C

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

T146 SATA_IS1
T147
(28) BIOS_WP#
ADD for BIOS Write Protect
T86
T81
R217 0_4 ACZ_SPKR
(21) PCBEEP
(3,7,8,24) PCLK_SMB
(3,7,8,24) PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
T82
(26) PDMA66
T88 SES_INT
(25) D3E_SCI# GEVENT7#

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#

USB OC

D6 CH501H-40PT
(4,8) CPU_MEMHOT#
(6,29) THERM_ALERT#
(24) NEW_DET#
CPU_MEMHOT#_IN
R384 0_4 SMBALERT#_1
R392 0_4
R414 *0_4 SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

HD AUDIO

ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0_R
ACZ_SDIN1_R
T59
T142
ACZ_SYNC
ACZ_RST#
(17) ACZ_RST#

HD audio interface is 3.3V voltage

IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7

INTEGRATED uC

VCC3
R166 22K_4
(26) HDD_AUX_RST#
HDD_AUX_RST#

SB700

USBCLK/14M_25M_48M_OSC
USB_RCOMP

USB MISC

C8 CLK_48M_USB
CLK_48M_USB (3)
G8 USB_RCOMP_SB
R167 11.8K/F_6

USB 1.1

USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
E6 USB_FSD13P
E7 USB_FSD13N
F7 USB_FSD12P
E8 USB_FSD12N
T45
T41
T44
T43

USB 2.0

USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

H11 T61
J10 T57
E11 NEW_USBP10+ (24) To New Card
F11 NEW_USBP10- (24)
A11 BT_USBP9+ (27) To Bluetooth
B11 BT_USBP9- (27)
C10 USBP8+ (24) To min-card 1(TV)
D10 USBP8- (24)
G11 USBP7+ (27) To M/B USB
H12 USBP7- (27)
E12 USBP6+ (27) To USB board
E14 USBP6- (27)
C12
D12
B12 WL_USBP4+ (24) To WLAN
A12 WL_USBP4- (24)
G12
G14
H14 CCD_USBP2+ (19) To Camera
H15 CCD_USBP2- (19)
A13 USBP1+ (27) To USB Board
B13 USBP1- (27)
B14 USBP0+ (27) To USB Board
A14 USBP0- (27)

IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPIO17
SB_SCLK2
SB_SDATA2
SB_SCLK3
SB_SDATA3
SB_GPIO16
SB_GPIO17
T47
T49
SB_GPIO16 (17)
SB_GPIO17 (17)
SPI/LPC define

IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41

INTEGRATED uC

CLK_48M_USB
R155 *10_6
C222 *10P/50V_4
for EMI

To Azalia

ACZ_SDOUT R183 33_4 ACZ_SDOUT_AUDIO (21)
C541 *10P/50V_4
ACZ_SYNC R187 33_4 ACZ_SYNC_AUDIO (21)
C281 *10P/50V_4
ACZ_BCLK R402 33_4 BIT_CLK_AUDIO (21)
C538 *10P/50V_4
ACZ_RST# R181 33_4 ACZ_RST#_AUDIO (21)
ACZ_SDIN0_R R175 0_4 ACZ_SDIN0 (21)

PROJECT : PF1
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Size	Document Number	Rev
	SB700-ACPI/GPIO/USB 2/4	1A
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SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

SATA1

SATA2

E-SATA

SATA ODD

U19B

SB700

Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

SATA PWR

HW MONITOR

SB700

0514 REVF: Reserve for Hitachi ODD

SATA PORT 4,5 are only support IDE mode

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:

R190 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

10/18 AMD suggest to connect to GND

AVDD--H/W monitor Analog power

5mA

77mA

1mA

11/23 Board ID define MXM

MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
15" UMA	x	x	0	0	0
15" M82	x	x	0	0	1
15" M86	x	x	0	1	1
17" UMA	x	x	1	0	0
17" M82	x	x	1	0	1
17" M86	x	x	1	1	1

PROJECT : PF1

Quanta Computer Inc.

Size	Document Number	Rev
	SB700-SATA/IDE/HWM/SPI 3/4	1A
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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

+3.3V_SB_R — 0.8A

R200 0_8 — VCC3

C311 22U/6.3V_8; C302 10U/6.3V_8; C282 1U/10V_4; C287 1U/10V_4; C276 1U/10V_4; C280 0.1U/10V_4; C255 0.1U/10V_4; C291 0.1U/10V_4

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power

+VDD33_18 — 0.45A

VCC1.8 — R205 0_8

C305 4.7U/6.3V_6; C298 1U/10V_4; C303 0.1U/10V_4; C304 0.1U/10V_4; C294 0.1U/10V_4

PCIE_VDDR--PCIE I/O power

+1.2V_PCIE_VDDR — 844mA

VCC1.2 — L54 BLM18PG221SN1D(220,1.4A)_6

C544 10U/6.3V_8; C269 1U/10V_4; C547 0.1U/10V_4; C270 0.1U/10V_4; C542 0.1U/10V_4; C265 0.1U/10V_4

AVDD_SATA--SATA phy power

+1.2V_AVDD_SATA — 0.2A

VCC1.2 — L55 BLM18PG221SN1D(220,1.4A)_6

C561 22U/6.3V_8; C555 0.1U/10V_4; C297 0.1U/10V_4; C295 1U/10V_4; C552 1U/10V_4

AVDDTX--USB Phy
Analog I/O power

For support USB wakeup-->RVCC3

+3V_AVDD_USB — 0.2A

RVCC3 — L52 BLM18PG221SN1D(220,1.4A)_6

C513 10U/6.3V_8; C514 10U/6.3V_8; C529 0.1U/10V_4; C524 0.1U/10V_4

C238 1U/10V_4; C247 1U/10V_4; C528 1U/10V_4; C235 0.1U/10V_4; C243 0.1U/10V_4; C525 0.1U/10V_4; C253 0.1U/10V_4

USB_PHY_1.2V--USB Phy
digital power

RVCC1.2 — R381 0_6 — +1.2V_USB_PHY_R

C522 0.1U/10V_4; C521 0.1U/10V_4; C512 10U/6.3V_8

AVDDCK_1.2--USB Phy
digital power

VCC1.2 / RVCC1.2 — +1.2V_AVDDCK

L27 *BLM18PG221SN1D(220,1.4A)_6
L24 BLM18PG221SN1D(220,1.4A)_6

C232 2.2U/6.3V_6

AVDDDC--USB Analog PLL power

RVCC3 — L25 BLM18PG221SN1D(220,1.4A)_6 — +3V_AVDDC

C231 0.1U/10V_4; C226 10U/6.3V_8

AVDDCK_3.3--Analog
system PLL power

VCC3 — L28 BLM18PG221SN1D(220,1.4A)_6 — +3V_AVDDCK

C229 2.2U/6.3V_6

SB700 — Part 3 of 5 — POWER

U19C

VDDQ_1 … VDDQ_12 — PCI/GPIO I/O

VDD_1 … VDD_9 — CORE S0

VDD33_18_1 … VDD33_18_4 — IDE/FLSH I/O

CKVDD_1.2V_1 … CKVDD_1.2V_4 — CLKGEN I/O

PCIE_VDDR_1 … PCIE_VDDR_7 — A-LINK I/O

S5_3.3V_1 … S5_3.3V_7 — 3.3V_S5 I/O

AVDD_SATA_1 … AVDD_SATA_7 — SATA I/O

S5_1.2V_1 … S5_1.2V_2 — CORE S5

USB_PHY_1.2V_1 … USB_PHY_1.2V_2

AVDDTX_0 … AVDDRX_5 — USB I/O

V5_VREF — AVDDCK_3.3V — AVDDCK_1.2V — AVDDC — PLL

SB700

VDD-- S/B CORE power

+1.2V_VCC_SB_R — 604mA

C275 0.1U/10V_4; C261 0.1U/10V_4; C257 1U/10V_4; C268 1U/10V_4; C551 10U/6.3V_8

R415 0_8 — VCC1.2

CKVDD_1.2V-- Internal
clock Generator I/O
power

+1.2V_CKVDD — 286mA

C256 1U/10V_4; C263 0.1U/50V_6; C264 0.1U/50V_6; C262 10U/6.3V_8

L31 BLM18PG221SN1D(220,1.4A)_6 — VCC1.2

S5_3.3--3.3v standby power

+3VALW_R — 0.01A

C236 0.1U/10V_4; C254 2.2U/6.3V_6; C526 2.2U/6.3V_6

R386 0_6 — RVCC3

Change to 0603

S5_1.2V--1.2V standby power

+1.2VALW_R — 0.22A

C251 2.2U/6.3V_6; C252 2.2U/6.3V_6

R174 0_6 — RVCC1.2

0.2A — +1.2V_USB_PHY_R

V5_VREF--PCI 5V TOLERANCE

+5V_VREF — 4mA

R422 1K/F_4 — VCC5

+3V_AVDDCK — 7mA

+1.2V_AVDDCK — 44mA

C556 1U/10V_4

+3V_AVDDC — 16mA

D29 CH501H-40PT — VCC3

D30 CH501H-40PT — VCC1.8

SB700 — Part 5 of 5 — GROUND

U19E

AVSS_SATA_1 … AVSS_SATA_20

AVSS_USB_1 … AVSS_USB_24

PCIE_CK_VSS_1 … PCIE_CK_VSS_8

AVSSC / AVSSCK

VSS_1 … VSS_50

PCIE_CK_VSS_9 … PCIE_CK_VSS_21

(32,37)	RVCC1.2
(14,15,17,23,24,25,32)	RVCC3
(3,4,12,13,15,30,34,37)	VCC1.2
(4,9,11,12,13,17,25,26,35,36)	VCC1.8
(3,4,6,7,8,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,27,28,29,30,32,33,36)	VCC3
(18,19,20,21,22,25,26,27,28,29,32,33,36)	VCC5

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Quanta Computer Inc.

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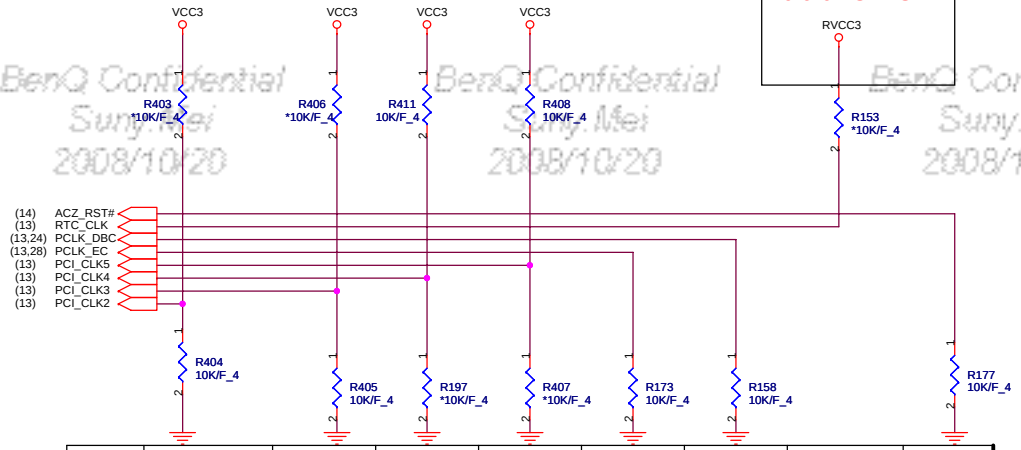
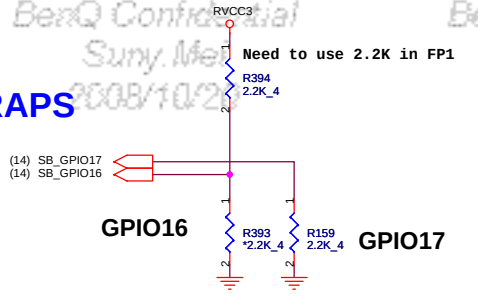
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



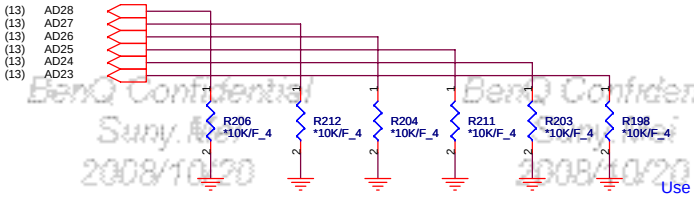
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

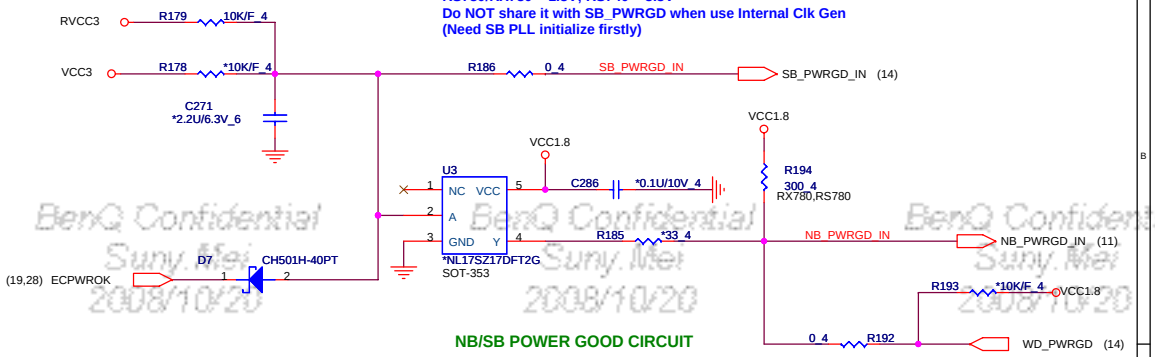
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



NB/SB POWER GOOD CIRCUIT

	U11	R230	R229	R245	R234
RX780 RS780M	V	V	V	X	X

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

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HDMI

close to NB & VGA connector

(10) IV_HDMITX2P / (10) IV_HDMITX2N
(20) EXT_HDMITX2P / (20) EXT_HDMITX2N
RN28 / RN24 — IV@0X2 / EV@0X2 — HDMITX2P / HDMITX2N

(10) IV_HDMITX1P / (10) IV_HDMITX1N
(20) EXT_HDMITX1P / (20) EXT_HDMITX1N
RN21 / RN20 — IV@0X2 / EV@0X2 — HDMITX1P / HDMITX1N

(10) IV_HDMITX0P / (10) IV_HDMITX0N
(20) EXT_HDMITX0P / (20) EXT_HDMITX0N
RN27 / RN25 — IV@0X2 / EV@0X2 — HDMITX0P / HDMITX0N

(10) IV_HDMICLK+ / (10) IV_HDMICLK-
(20) EXT_HDMICLK+ / (20) EXT_HDMICLK-
RN19 / RN22 — IV@0X2 / EV@0X2 — HDMICLK+ / HDMICLK-

(11) IV_HDMI_DDCCLK / (11) IV_HDMI_DDCDATA
(20) EXT_HDMI_DDCCLK / (20) EXT_HDMI_DDCDAT
RN26 / RN23 — IV@0X2 / EV@0X2 — HDMI_DDCCLK / HDMI_DDCDATA

3/17 Modify AMD commend

VCC5 — R349 100K_4 — Q40 RHU002N06

R238 499/F_4 HDMICLK-
R252 499/F_4 HDMICLK+
R234 499/F_4 HDMITX0N
R246 499/F_4 HDMITX0P
R348 499/F_4 HDMITX1N
R244 499/F_4 HDMITX1P
R255 499/F_4 HDMITX2N
R241 499/F_4 HDMITX2P

UMA RS780M stuff 750ohm
DIS M82-S/M86 stuff 499ohm
Close to connector

Near connector

HDMICLK+ / HDMICLK-
C209 *EV@22P50V_4
C204 *EV@22P50V_4

Add resistor 0320

HDMITX2P — R29 EV@100_4 — HDMITX2N
HDMITX1P — R31 EV@100_4 — HDMITX1N
HDMITX0P — R33 EV@100_4 — HDMITX0N
HDMICLK+ — R37 EV@100_4 — HDMICLK-

CN15
D2+ / D2 Shield / D2- / D1+ / D1 Shield / D1- SHELL1 / D0+ SHELL2 / D0 Shield / D0- SHELL3 / CK+ SHELL4 / CK Shield / CK- / CE Remote / NC / DDC CLK / DDC DATA / GND / +5V / HP DET
EV@HDMI-C12816-119A5-L

HDMI_SCL_C / HDMI_SDA_C
F2 EV@POLY_SWITCH
VCC5 — HDMI_HPD — R417 20K_4 — HDMIC_5V
(20) HDMI_HPD
R418 100K_4

VCC3 — R72 2.2K — Q44 2N7002E-T1-E3 — R353 *0 — R38 10K — VCC5
HDMI_DDCDATA — HDMI_SDA_C — C201 *EV@10P
VCC3 — R86 2.2K — Q45 2N7002E-T1-E3 — R356 *0 — R81 10K — VCC5
HDMI_DDCCLK — HDMI_SCL_C — C184 *EV@10P

DVI

For EMI
Modify 11/28

DVI-I

CN9

(20) EXT_DVITX2N / (20) EXT_DVITX2P — R1 *EV@33_4
CRT_DDCCLK / CRT_DDCDATA / VSYNC1
(20) EXT_DVITX1N / (20) EXT_DVITX1P — R2 *EV@33_4
CRT_VCC
DVI_HPD — R9 EV@20K
(20) EXT_DVITX0N / (20) EXT_DVITX0P — R3 *EV@33_4
(20) EXT_DVICLK+ / (20) EXT_DVICLK- — R6 *EV@33_4

C1 CRT_R1
C2 CRT_G1
C3 CRT_B1
C4 HSYNC1
C5

EV@DVI-I_CNN
DVI-070939FR029S237PR-C-30P-H
P/N:DFDS29FR019

(20) DVI_HPD — DVI_HPD — R10 EV@100K

Activate: H

3/17 Modify AMD commend

VCC5 — R361 100K_4 — Q41 RHU002N06

R416 499/F_4 EXT_DVITX2N
R369 499/F_4 EXT_DVITX2P
R363 499/F_4 EXT_DVITX1N
R364 499/F_4 EXT_DVITX1P
R375 499/F_4 EXT_DVITX0N
R380 499/F_4 EXT_DVITX0P
R377 499/F_4 EXT_DVICLK+
R368 499/F_4 EXT_DVICLK-

UMA RS780M stuff 750ohm
DIS M82-S/M86 stuff 499ohm
Close to connector

CRT PORT

VCC3 — R23 2.2K — Q6 2N7002E-T1-E3 — VCC5 — R25 10K
DDCDAT — DDCDAT_L — L5 BLM11A121S — CRT_DDCDATA

VCC3 — R22 2.2K — Q5 2N7002E-T1-E3 — VCC5 — R24 10K
DDCCLK — DDCCLK_L — L4 BLM11A121S — CRT_DDCCLK

close to NB & VGA connector

(20) EXT_VGA_RED — R148 EV@0_4 — CRT_R
(20) EXT_VGA_GRN — R147 EV@0_4 — CRT_G
(20) EXT_VGA_BLU — R149 EV@0_4 — CRT_B
(20) EXT_HSYNC — R143 EV@0_4 — HSYNC
(20) EXT_VSYNC — R144 EV@0_4 — VSYNC
(20) EXT_CRT_DDCCLK — R145 EV@0_4 — DDCCLK
(20) EXT_CRT_DDCDAT — R146 EV@0_4 — DDCDAT

(11) INT_CRT_RED — R141 IV@0_4
(11) INT_CRT_GRN — R140 IV@0_4
(11) INT_CRT_BLU — R142 IV@0_4
(11) INT_HSYNC — R112 IV@0_4
(11) INT_VSYNC — R115 IV@0_4
(11) INT_CRT_DDCCLK — R136 IV@0_4
(11) INT_CRT_DDCDAT — R137 IV@0_4

C419 0.1U/10V_4
VSYNC — U11 *AHCT1G125DCH — VSYNCL — R322 0
HSYNC — U12 *AHCT1G125DCH — HSYNCL — R323 0

6/14

L45 BLM11A121S — VSYNC1
L46 BLM11A121S — HSYNC1
C420 *10P — C422 *10P — C418 10P — C421 10P

VCC3 — D25 DA204U — D28 DA204U
Change to DA204U 4/30

PTC:DK100TPU028

VCC3 — D3 DA204U — D4 DA204U — D2 DA204U
CRT_VCC — L44 FBM2125HM330 — D1 CH501H-40PT — DK200TFU101 F1 — POLY_SWITCH RD1206 — VCC5
*0.1U/10V_4 C413

Placed as close as possible to CN7

CRT_R — L2 MLB-160808-0070B-N3 — CRT_R1
CRT_G — L3 MLB-160808-0070B-N3 — CRT_G1
CRT_B — L1 MLB-160808-0070B-N3 — CRT_B1

R17 150/F — R21 150/F — R14 150/F
C14 5.6P — C16 5.6P — C9 5.6P
C8 5.6P — C15 5.6P — C13 5.6P

CN8
CRT_DDCDATA
HSYNC1
VSYNC1
CRT_DDCCLK
D36 1SS355 — CRT_SENSE# (28)

P/N:DFDS15FR084
IV@DSUB-070549FR015SX03CX-15P-V

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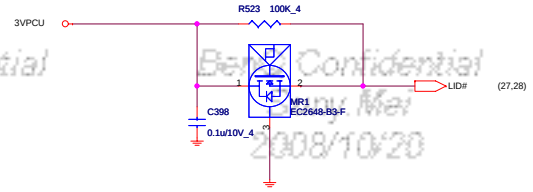
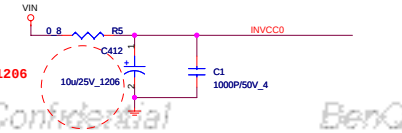
LCD TYPE CONNECTOR

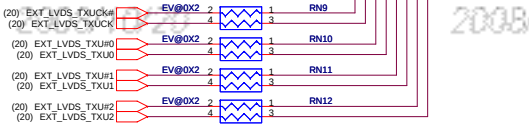
HALL SENSOR

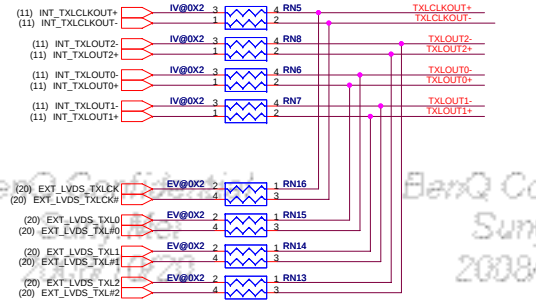


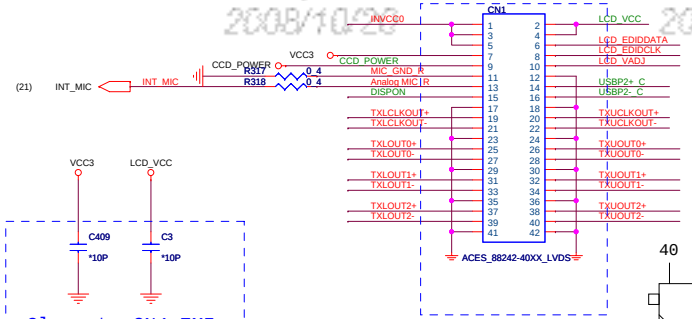
8/13 Change Size To 1206



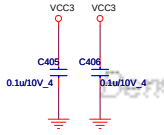
10/22 update p/n From DFHS40FS825 to DFWF40MS000



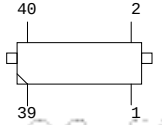


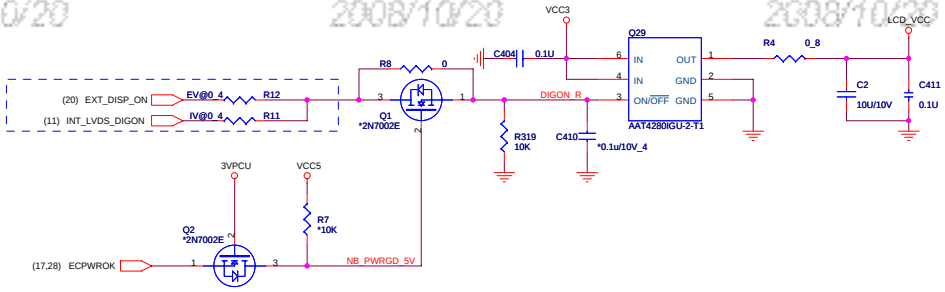


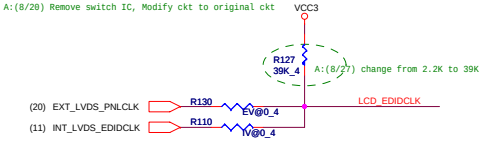
11/01 add stitch cap for LVDS

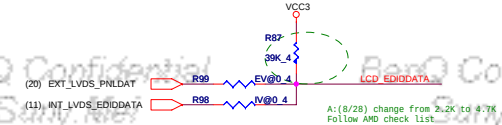


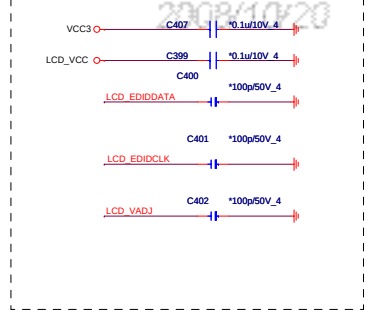
LCD PANEL MODULE

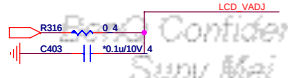




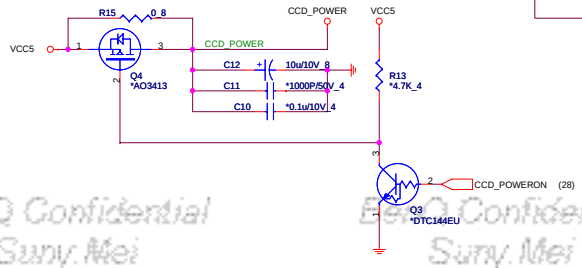


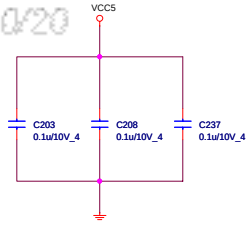


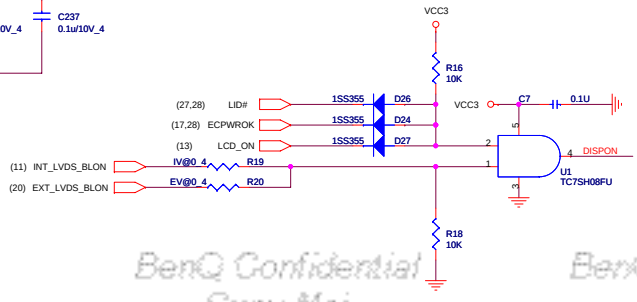




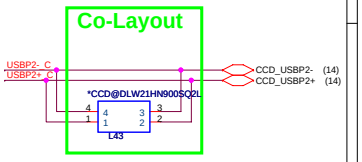
CAMERA MODULE







Co-Layout



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Quanta Computer Inc.

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	LCD CONN & CAMERA	2A
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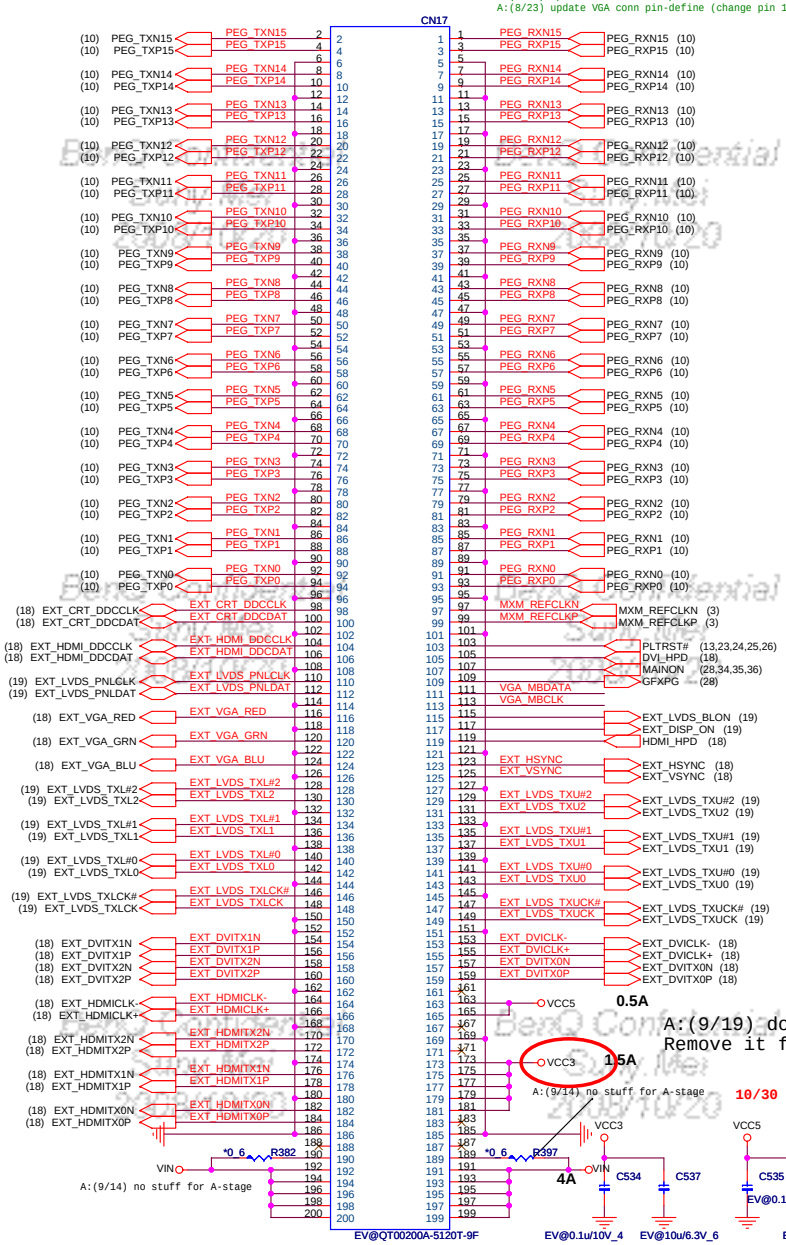
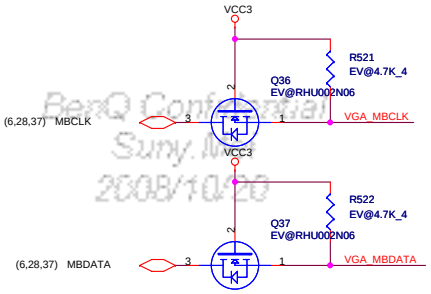
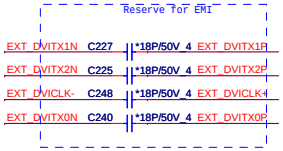
A:(8/18) update VGA conn footprint base on Allan information
A:(8/23) update VGA conn pin-define (change pin 1 location)







0.5A

A:(9/19) don't have enough space to put the test point, Remove it for A-test

15A

A:(9/14) no stuff for A-stage

10/30 modify to +3V

4A

PROJECT : PF1
Quanta Computer Inc.

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	MXM CONNECTOR / TV	2A
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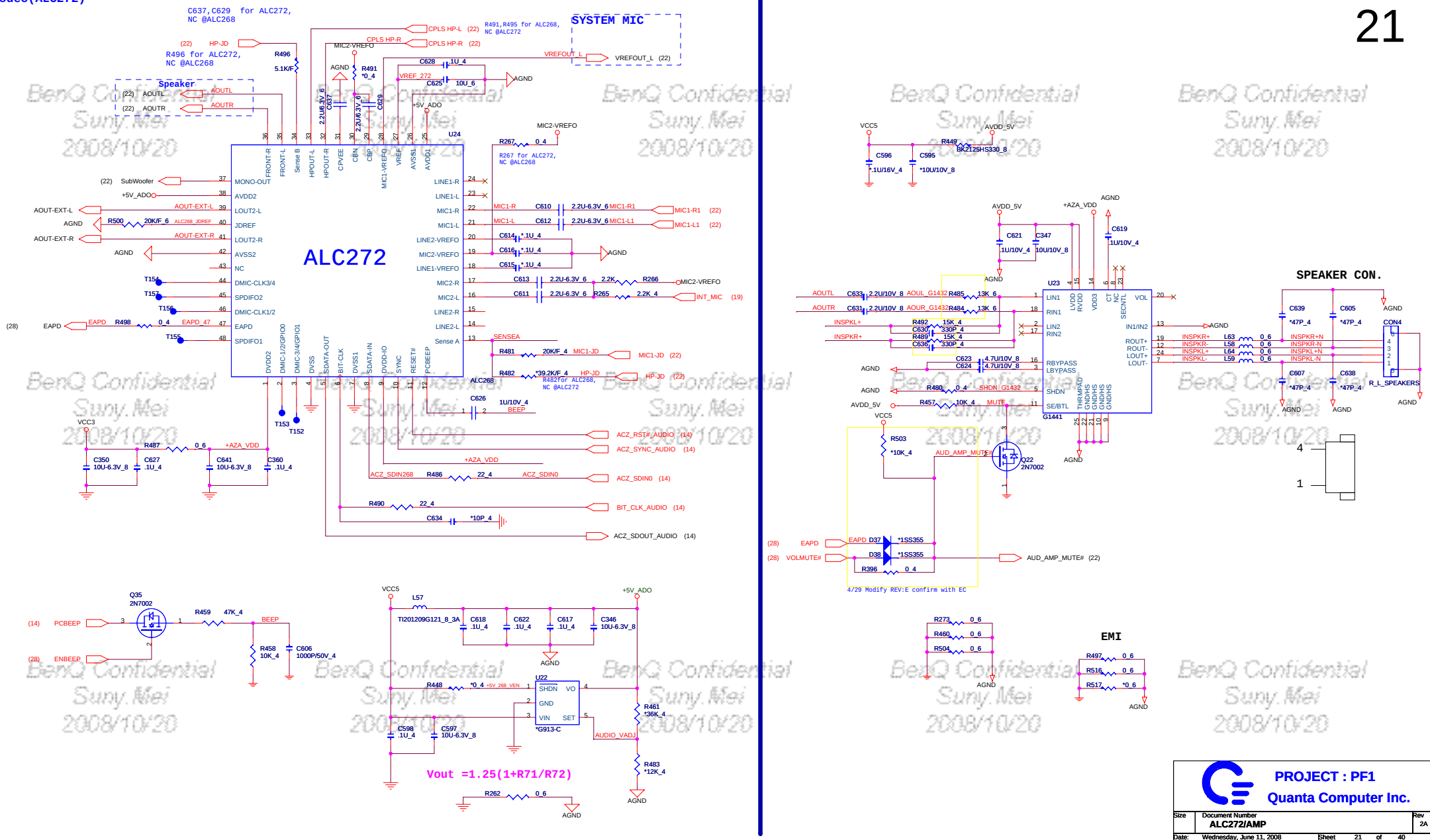
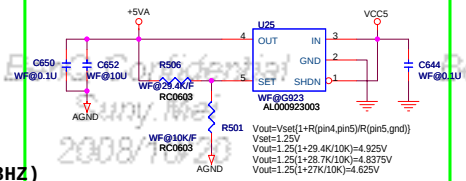
Codec(ALC272)

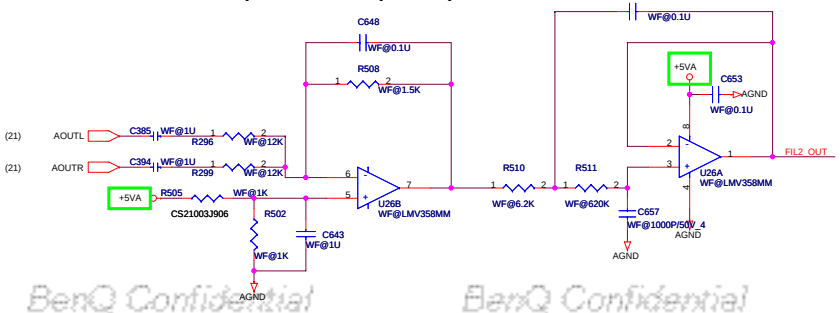


Subwoofer

LM358 Power



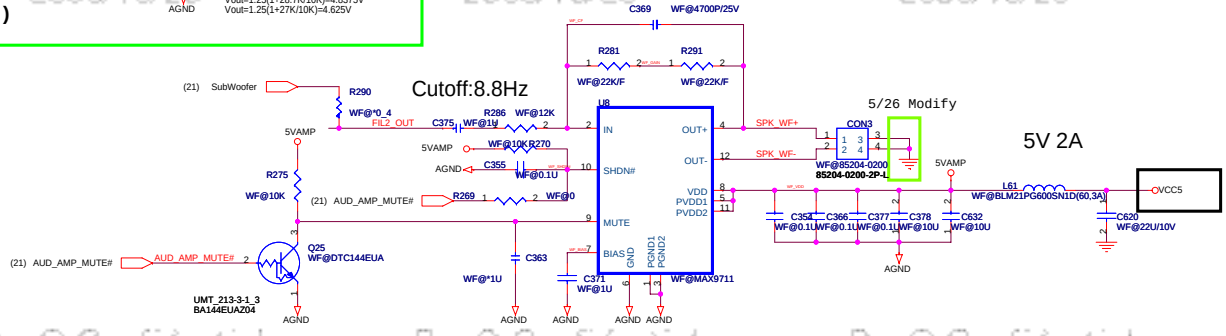
Mixer & 1nd order low pass filter(338HZ)



2nd order low pass filter(338HZ)

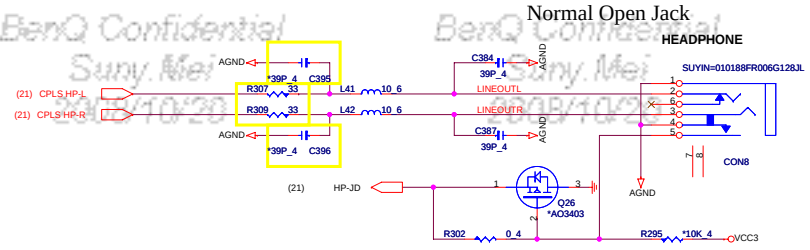
Cutoff:770Hz

Cutoff:8.8Hz

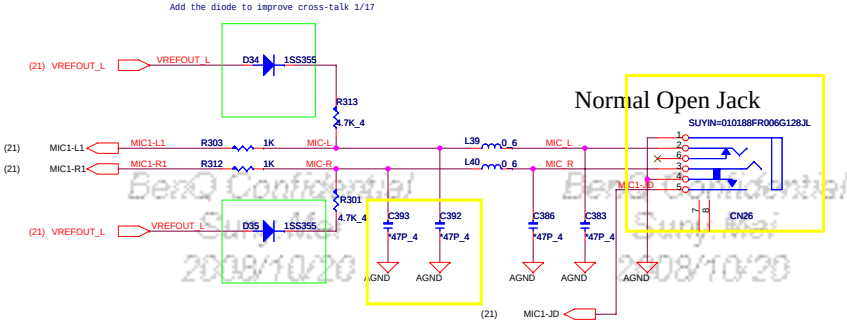


HP

Normal Open Jack



SYSTEM MIC



PROJECT : PF1
Quanta Computer Inc.

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	Audio JACK /Woofer	2A
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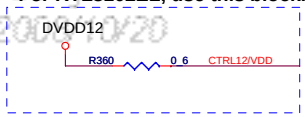
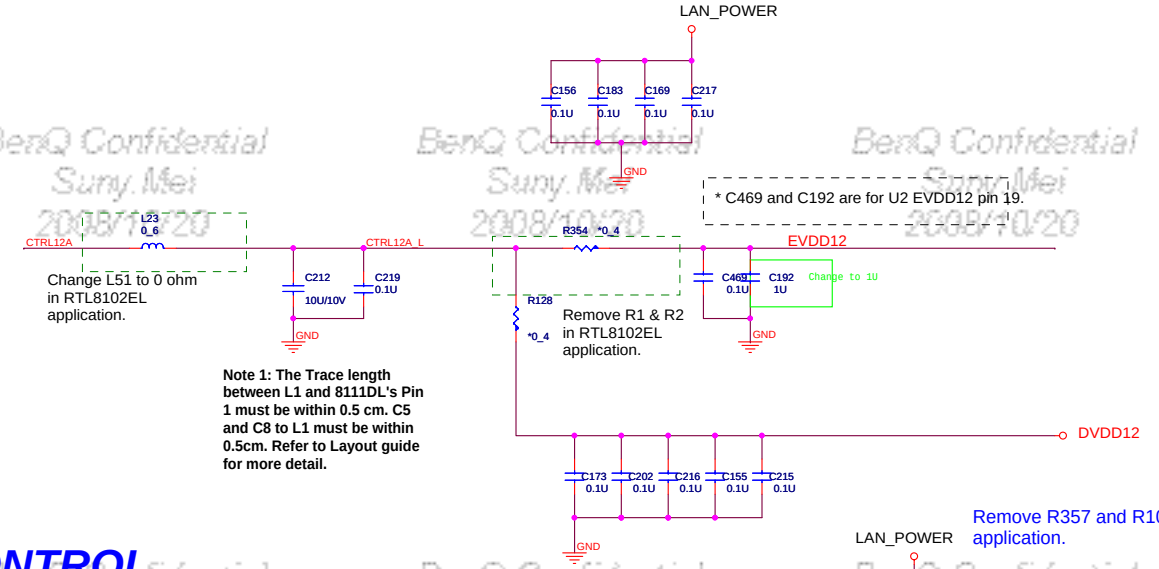
LAN_REALTEK_RTL8102E

For RTL8102EL, use this block.

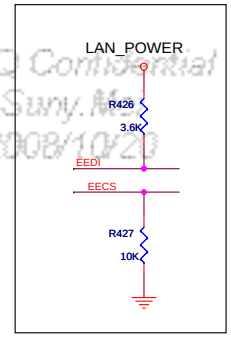




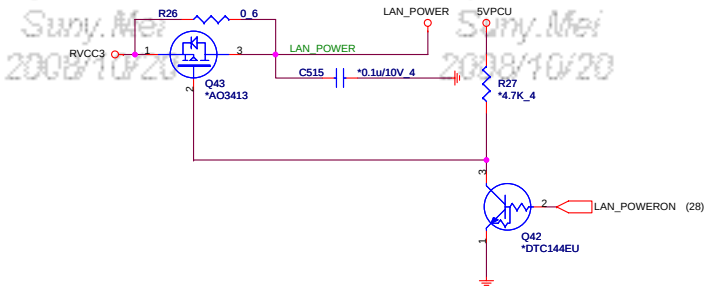
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

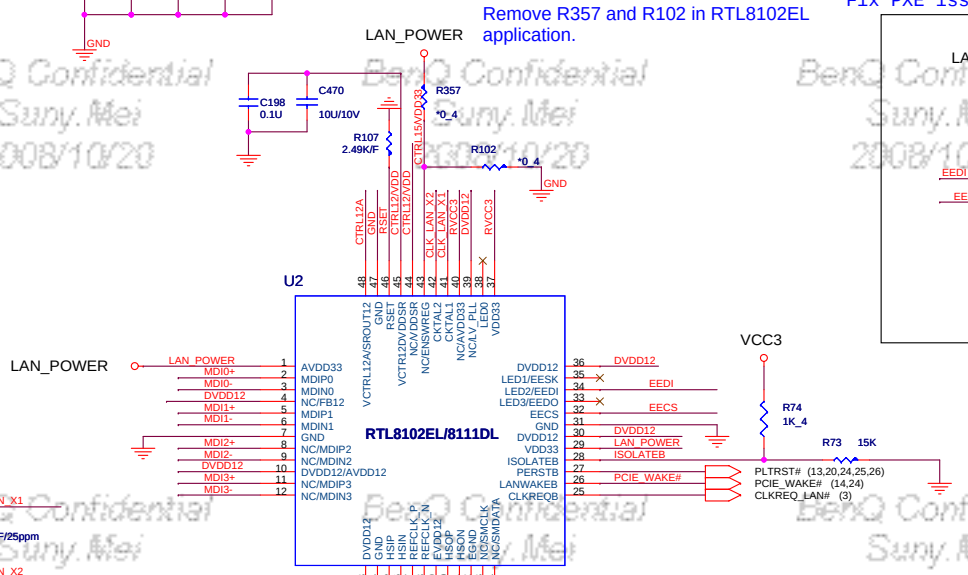
Remove R357 and R102 in RTL8102EL application.

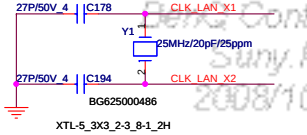
Fix PXE issue (ADD for B+)

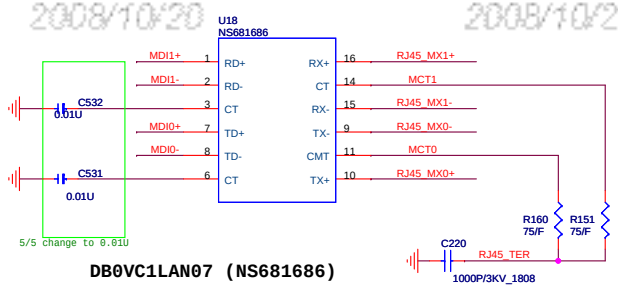


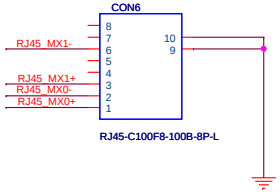
LAN POWER CONTROL

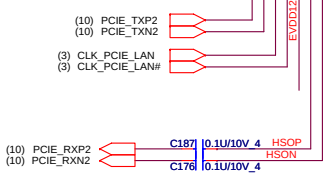


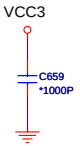






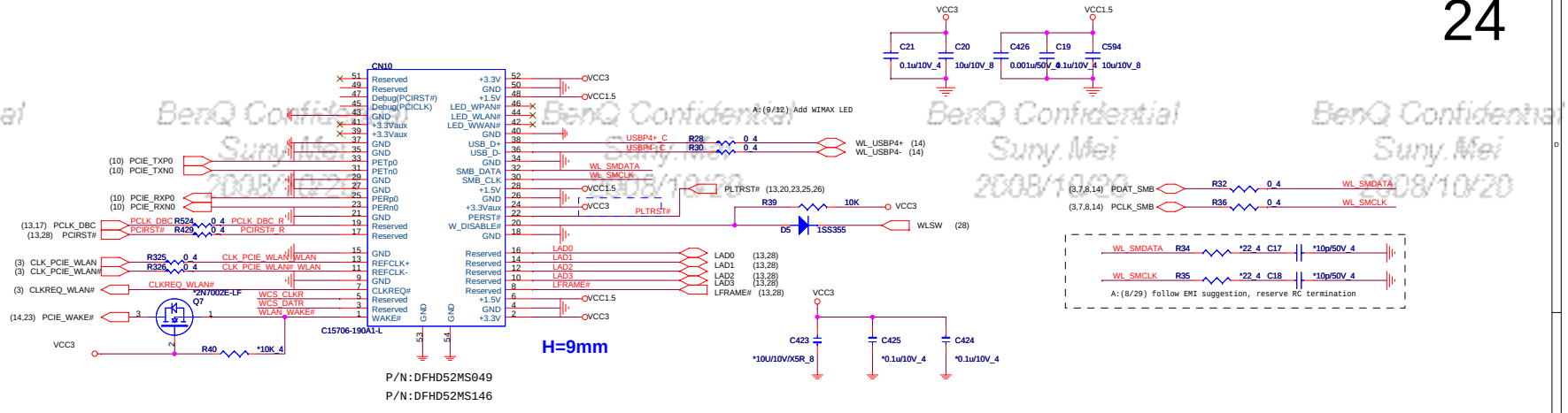




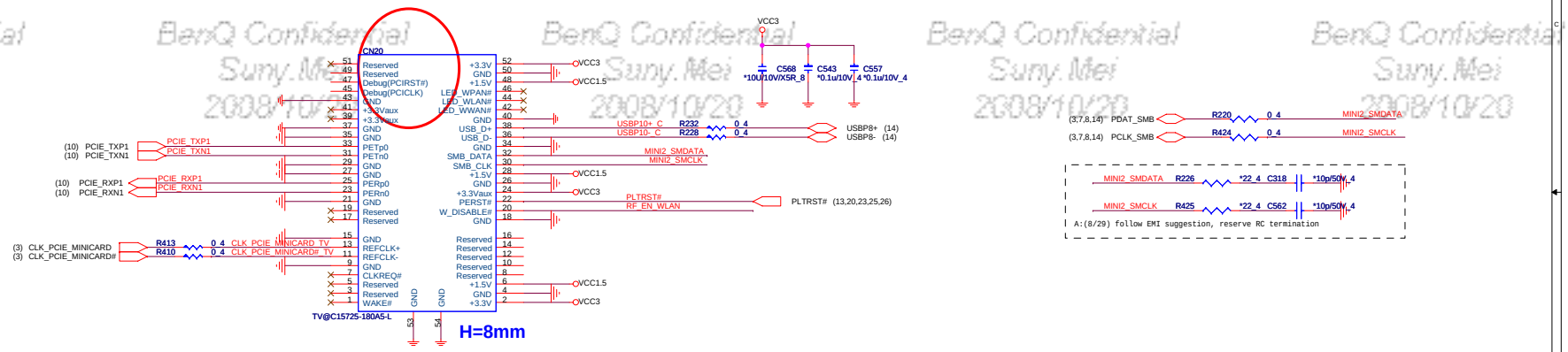


PROJECT : PF1		
Quanta Computer Inc.		
Size	Document Number: LAN_REALTEK_RTL8102EL	Rev: 2A
Date: Wednesday, June 11, 2008	Sheet 23 of 40	

MINI-Card I (WLAN)



MINI-Card II (TV)



A:(9/7) per TI FAE suggestion:
(1)Please keep all Input and Output capacitor value > 4.8uF (0.1uF +4.7uF)
(2)Please put these caps closed to IC
(3)R4101(pin 19,OC#) value should change to 2k ohm.

NEW CARD'S POWER SWITCH

CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)

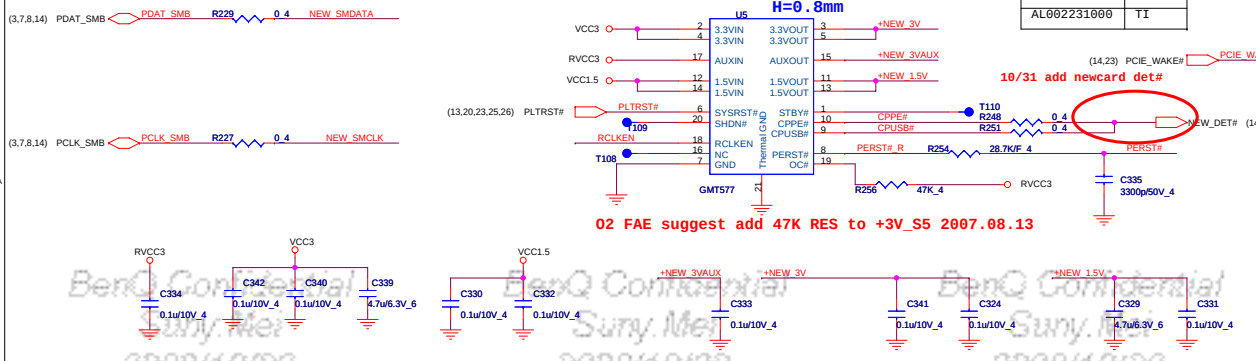
New Card's Power Switch

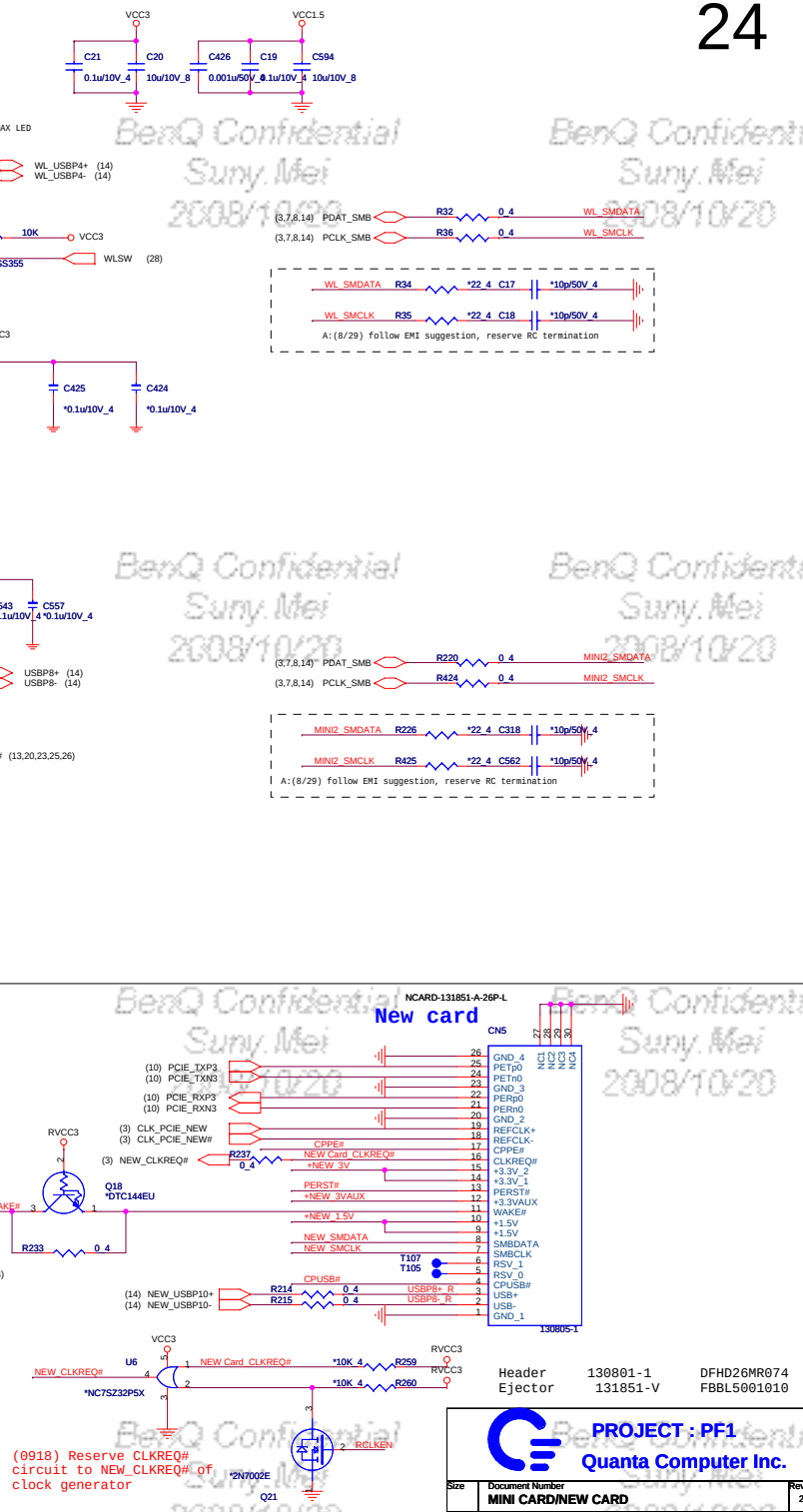
QCI PN	Vendor
AL000577001	GMT
AL027C10003	OMC
AL005538001	Ricoh
AL002231000	TI

H=0.8mm

10/31 add newcard det#

O2 FAE suggest add 47K RES to +3V_S5 2007.08.13





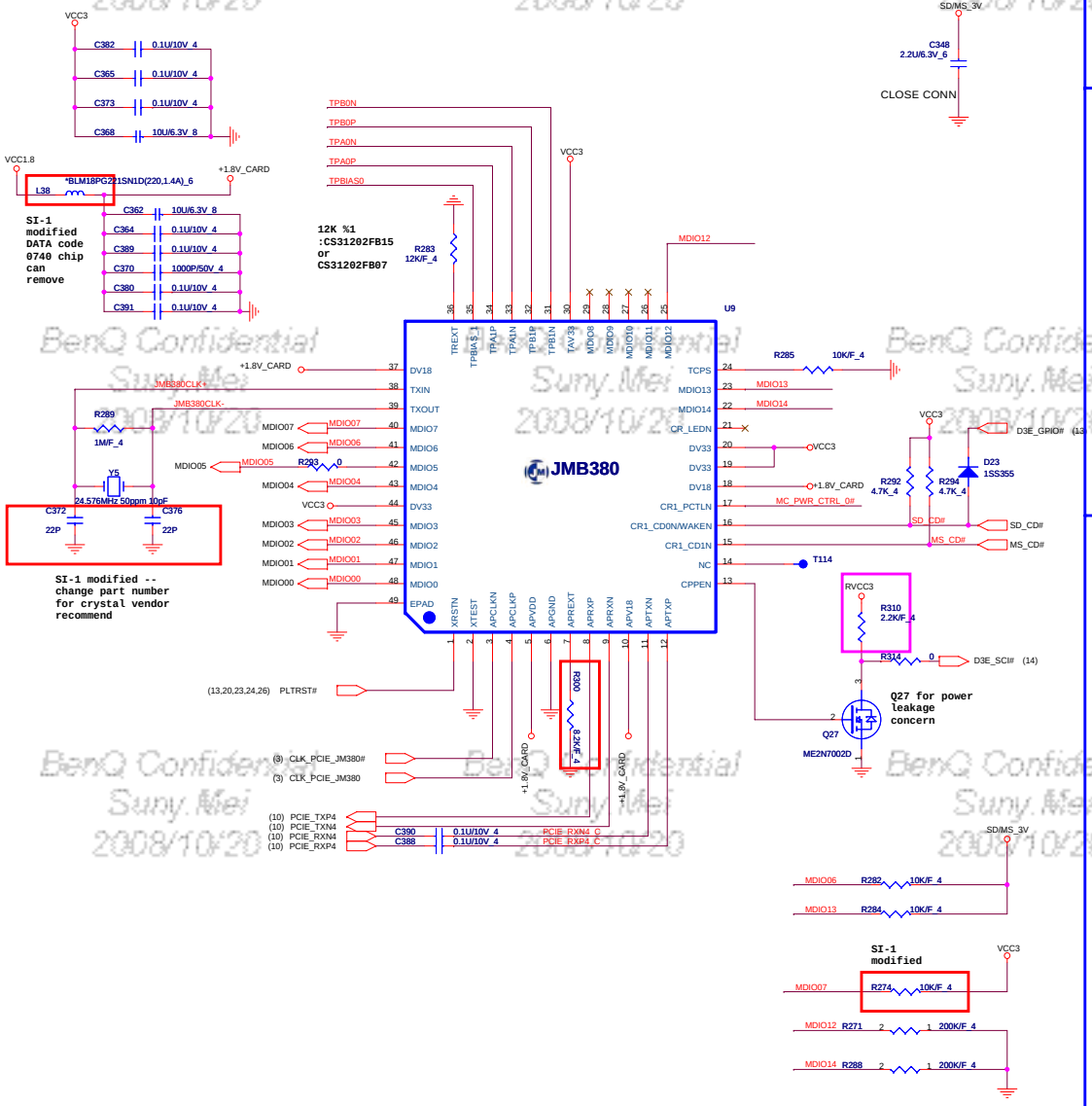
(0918) Reserve CLKREQ# circuit to NEW_CLKREQ# of clock generator

Header	130801-1	DFHD26MR074
Ejector	131851-V	FBBL5001010

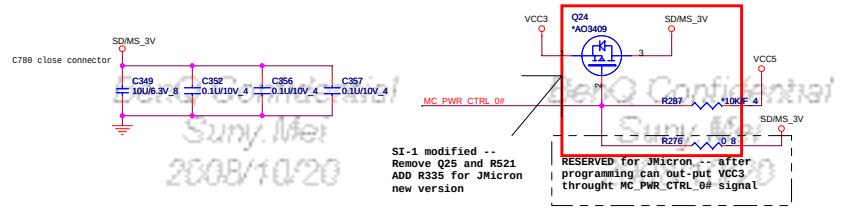
PROJECT : PF1
Quanta Computer Inc.

Size	Document Number	Rev
	MINI CARD/NEW CARD	2A
Date: Wednesday, June 11, 2008	Sheet 24 of 40	

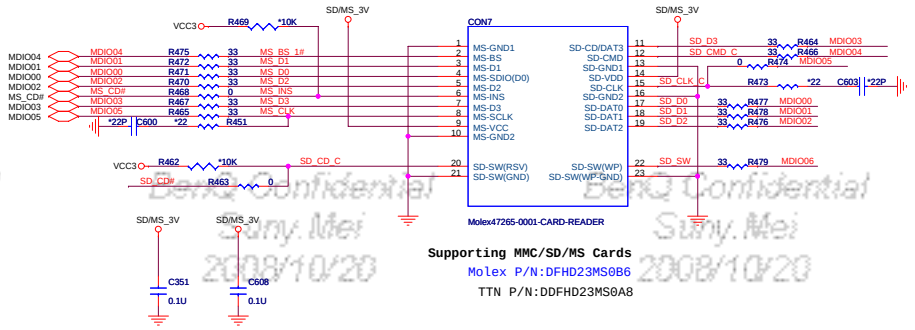
CARD READER



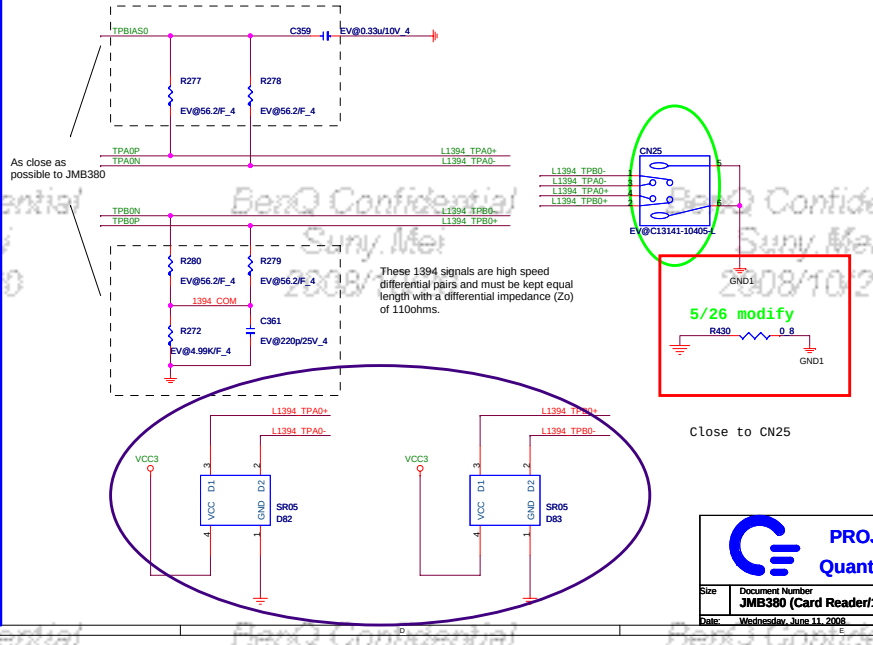
CARDREADER POWER



4 IN 1 CONN



1394

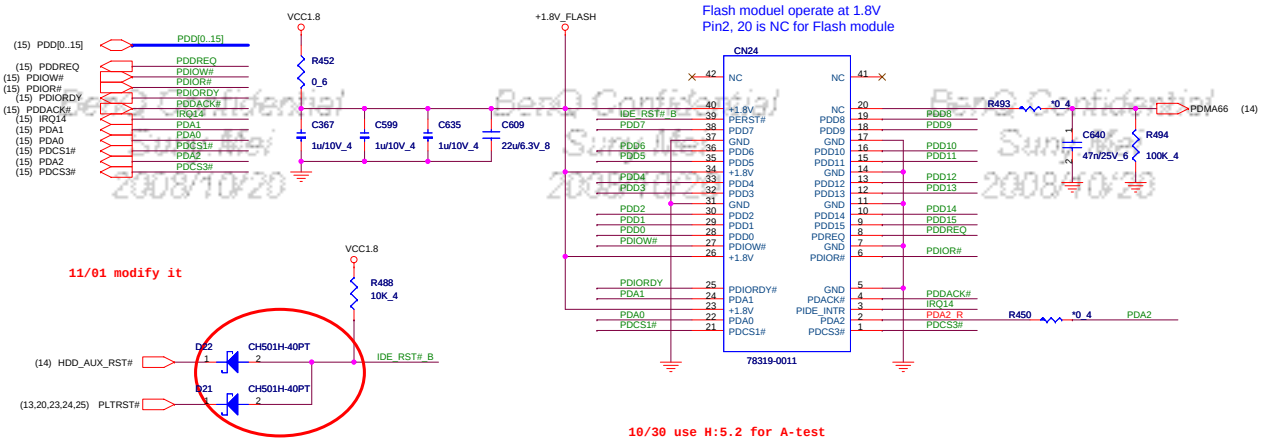


PROJECT : PF1
Quanta Computer Inc.

Size	Document Number	Rev
	JMB380 (Card Reader/1394)	2A

Date: Wednesday, June 11, 2008 Sheet 25 of 40

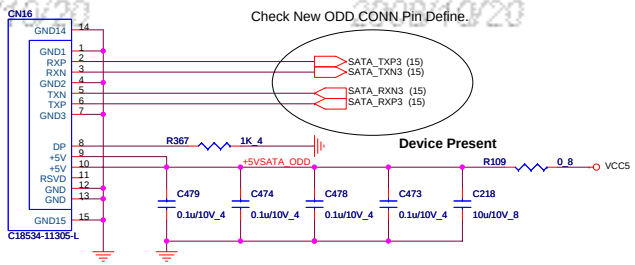
FLASH



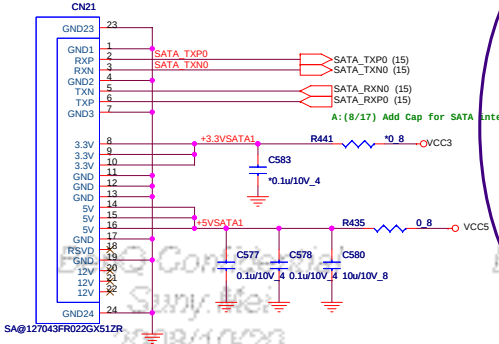
10/30 use H:5.2 for A-test

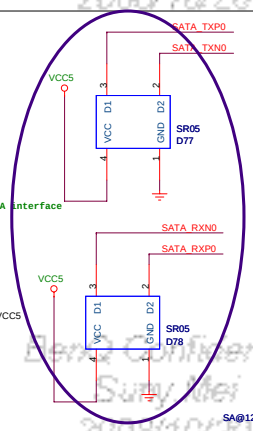
SATA ODD

9/28 change to SATA_ODD conn to BD3G use

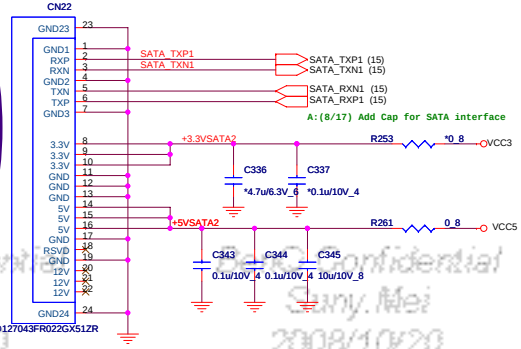


SATA HDD





2'nd SATA HDD

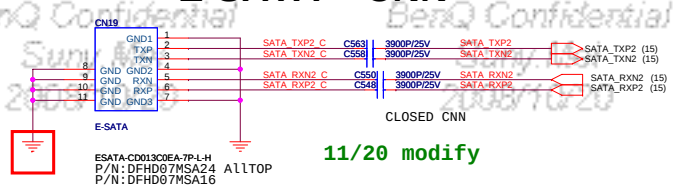


PROJECT : PF1

Quanta Computer Inc.

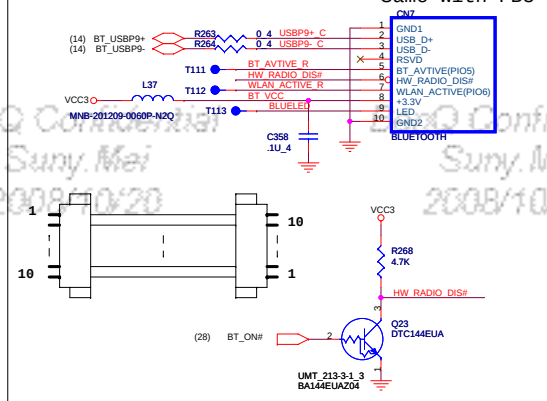
Size	Document Number	Rev
	SATA / HyberFLASH	2A
Date: Wednesday, June 11, 2008	Sheet 26 of 40	

E-SATA CNN

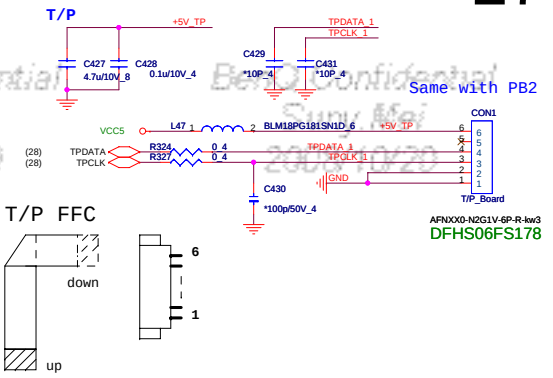


BLUETOOTH MODULE CONNECTOR

Same with PB3



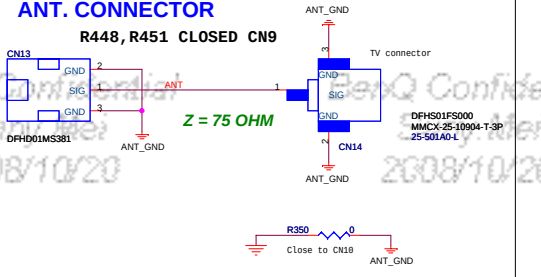
To TP board



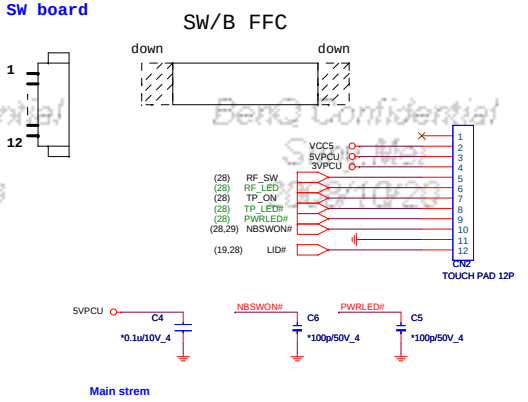
ON MB USB

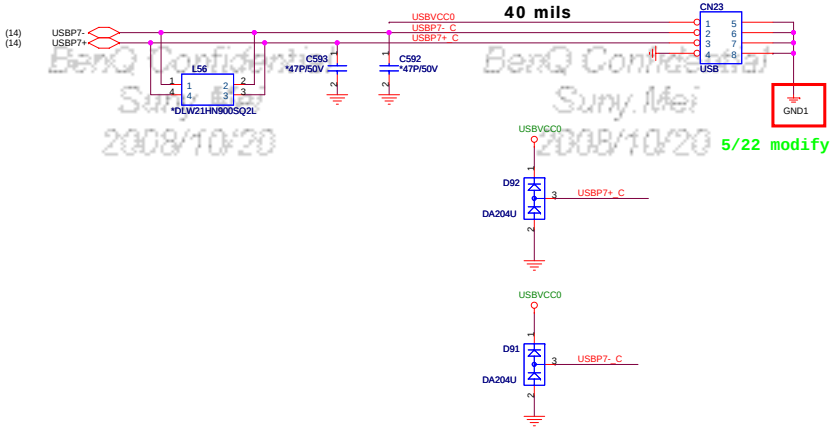
ANT. CONNECTOR

R448,R451 CLOSED CN9

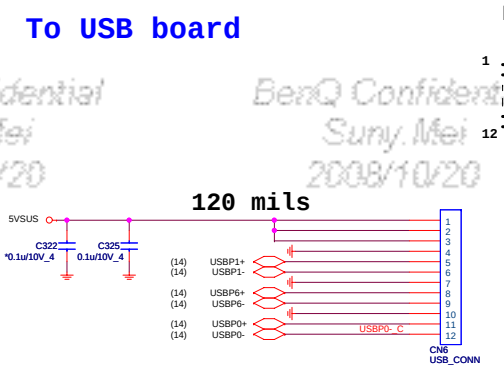


To SW board



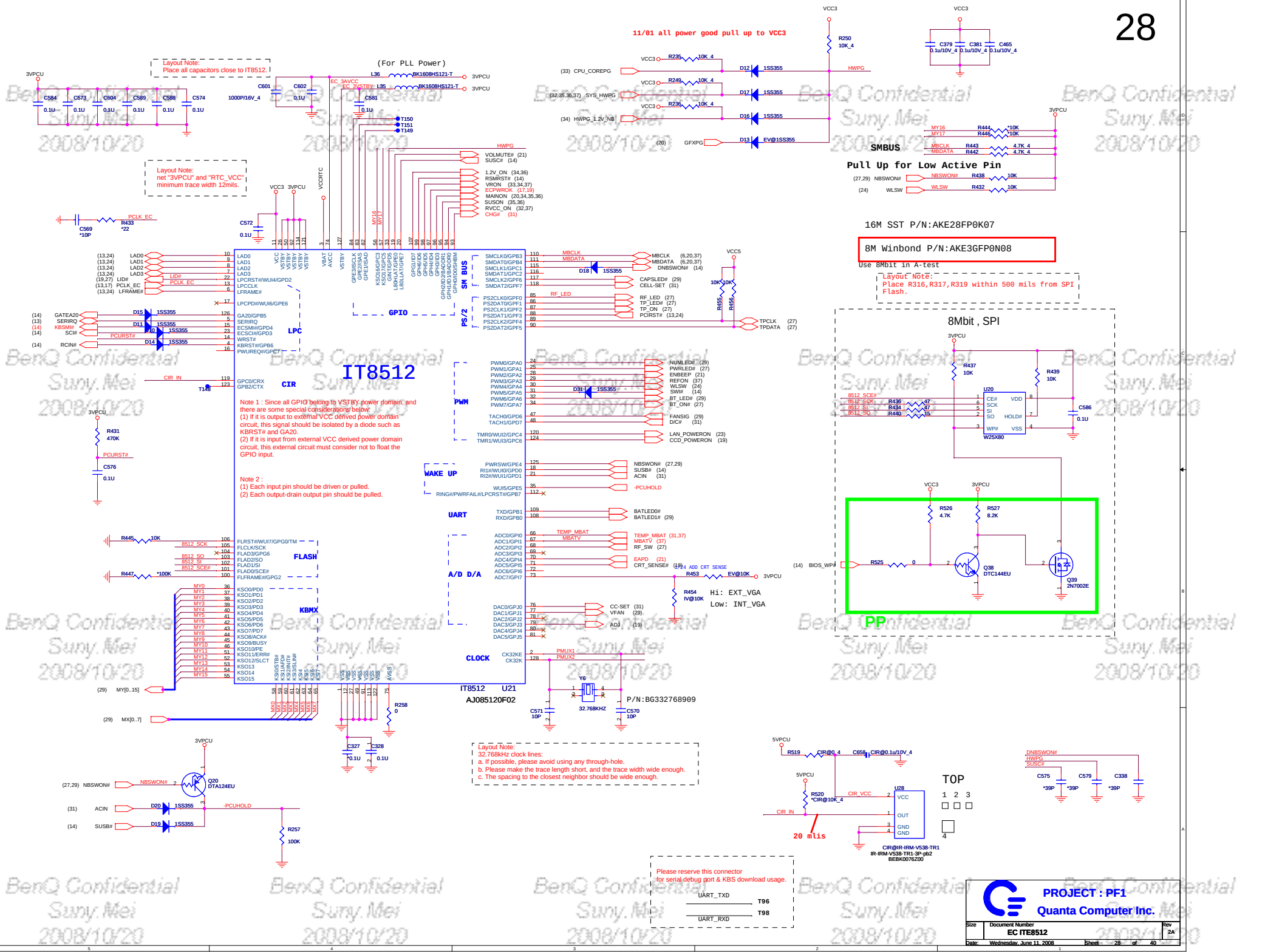


To USB board



PROJECT : PF1
Quanta Computer Inc.

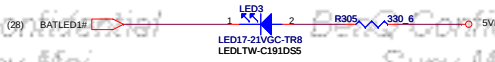
Size	Document Number	Rev
	ESATA/SW/ TP/ USB /BT/TV	2A
Date: Wednesday, June 11, 2008	Sheet 27 of 40	



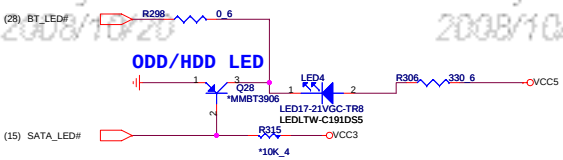
LED

BAT CAPS NUM Bluetooth

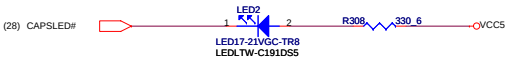
BATTERY CHARGE LED



ODD/HDD LED

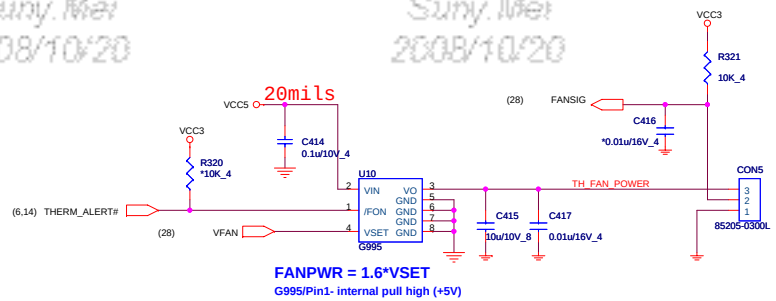


CAPS LED



Number Lock LED

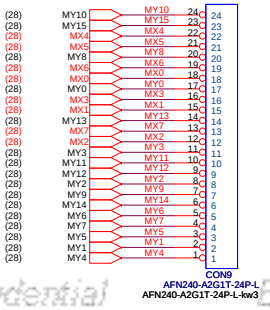
CPU FAN



FANPWR = 1.6*VSET

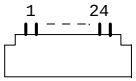
G995/Pin1- internal pull high (+5V)

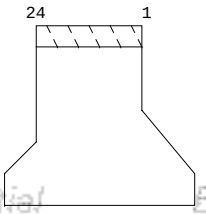
Keyboard CONN

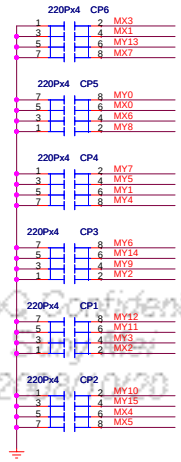


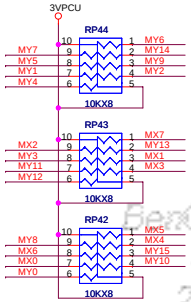
P/N:DFFC24FR181

Bot contact







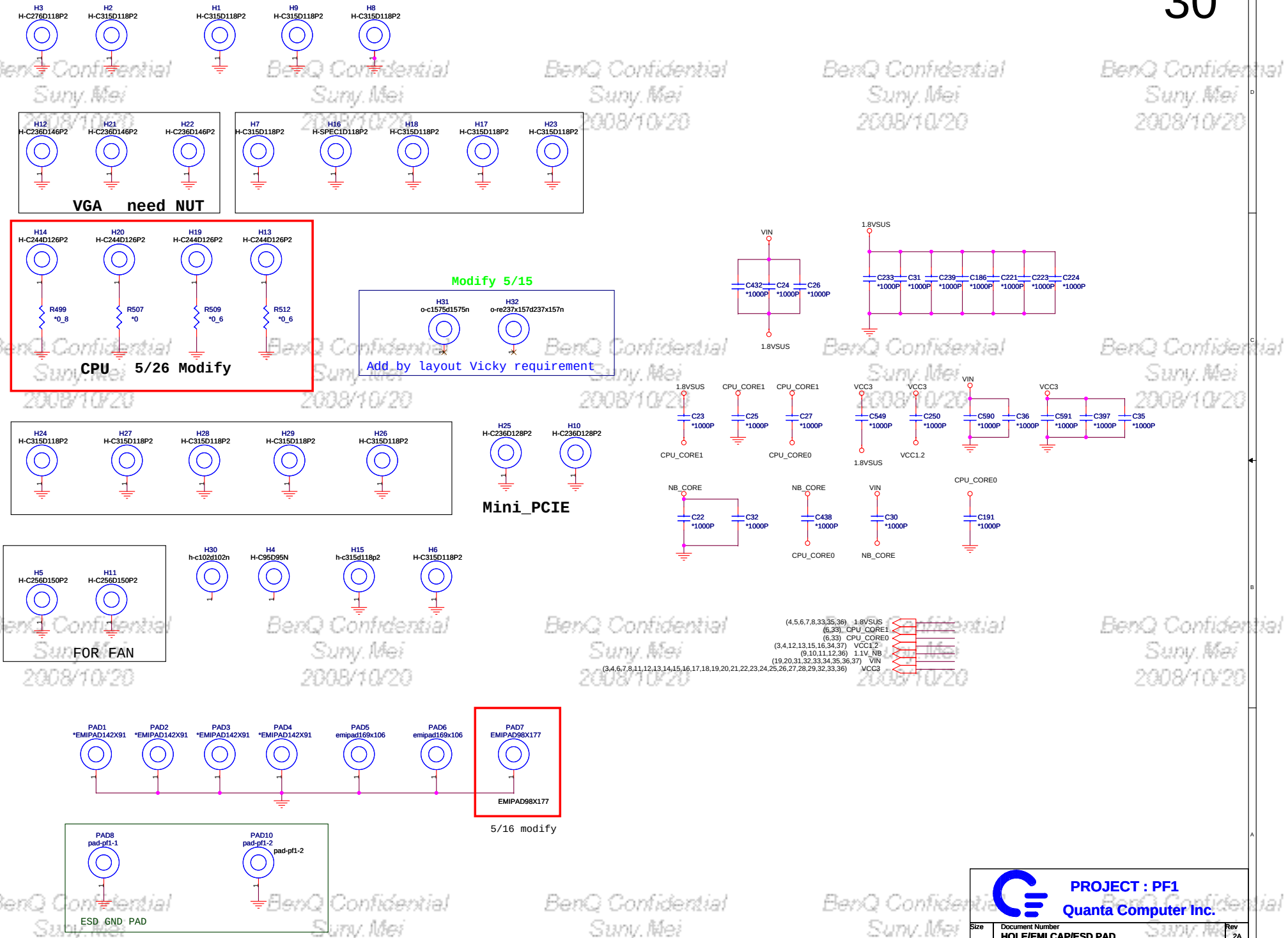


PROJECT : PF1

Quanta Computer Inc.

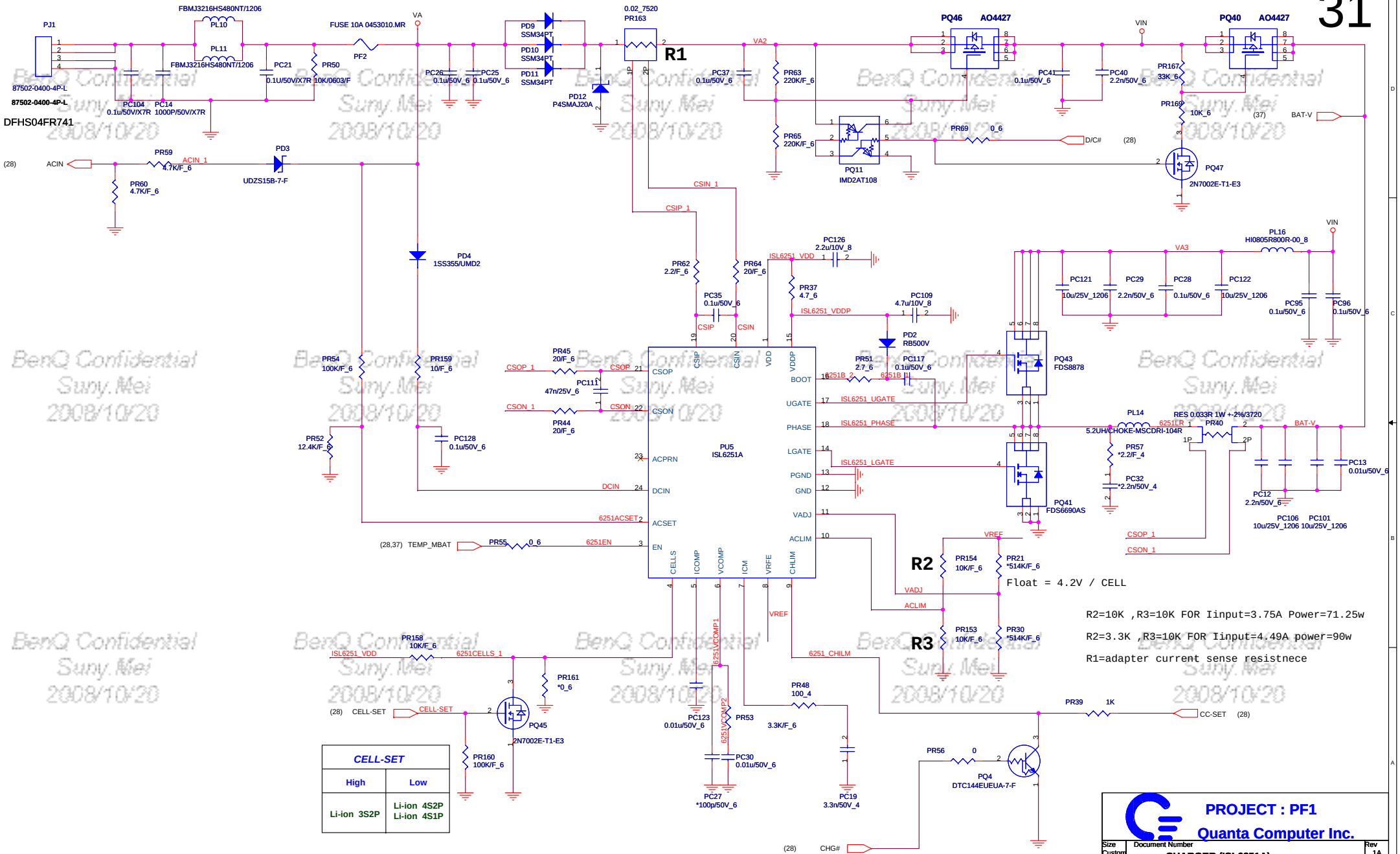
Size	Document Number	Rev
	SW/LED/Keyboard	2A

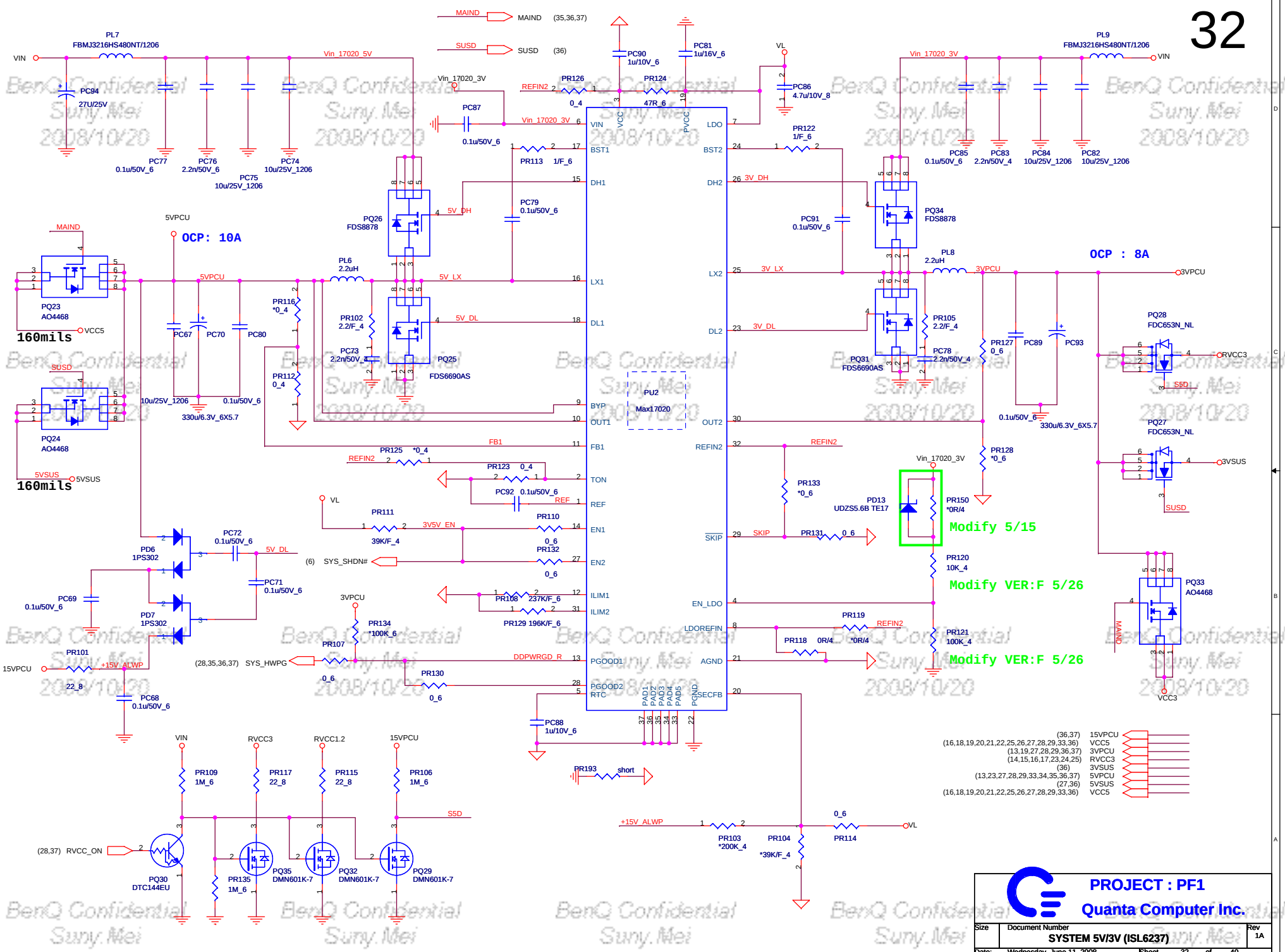
Date: Wednesday, June 11, 2008 Sheet 29 of 40

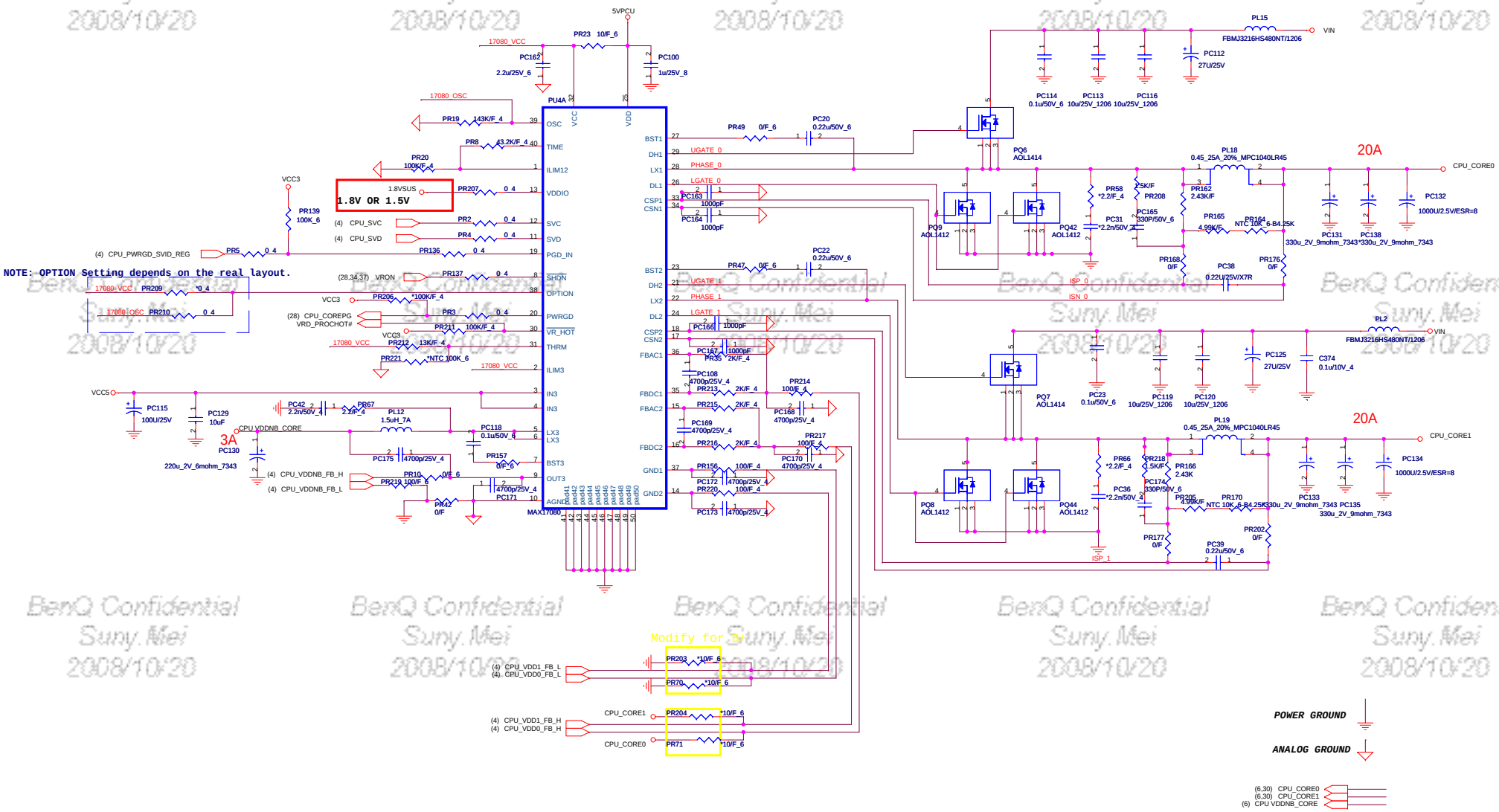


PROJECT : PF1
Quanta Computer Inc.

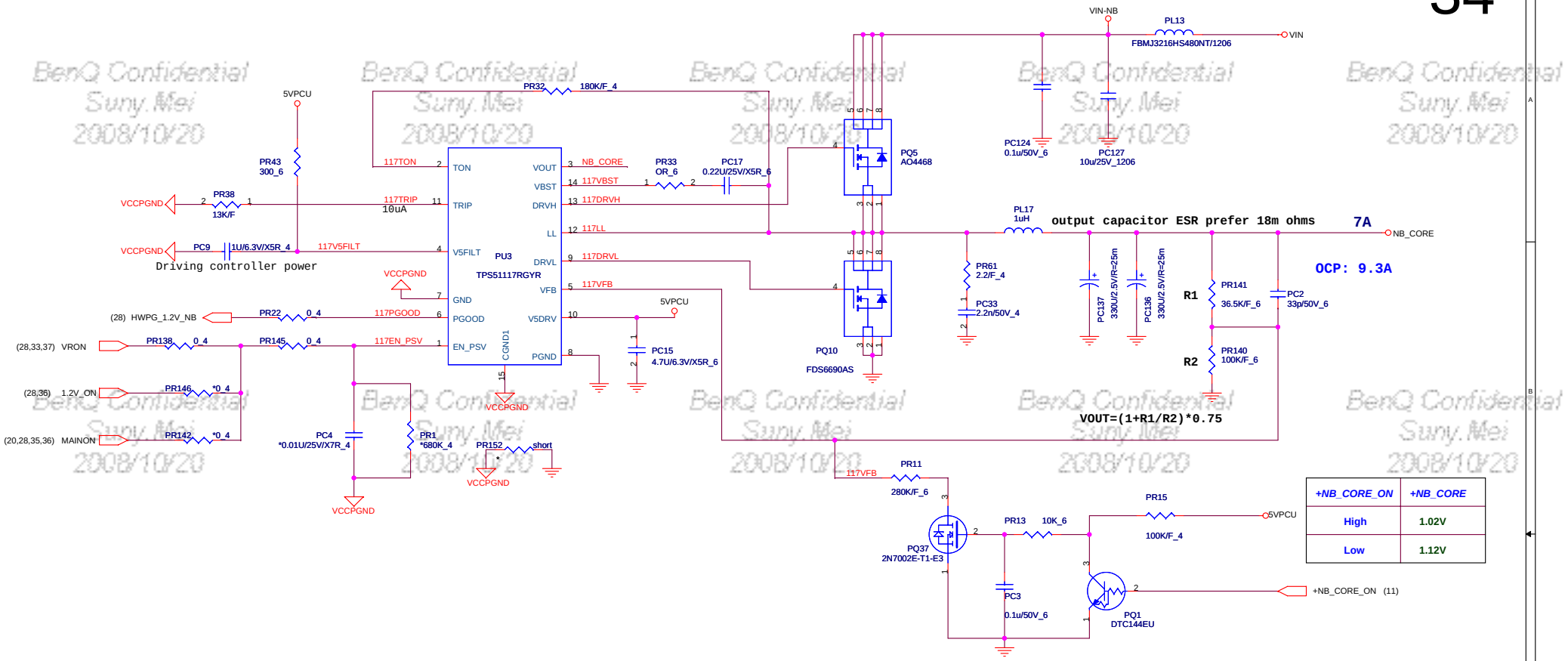
Size	Document Number	Rev
	HOLE/EMI CAP/ESD PAD	2A
Date: Wednesday, June 11, 2008	Sheet 30 of 40	



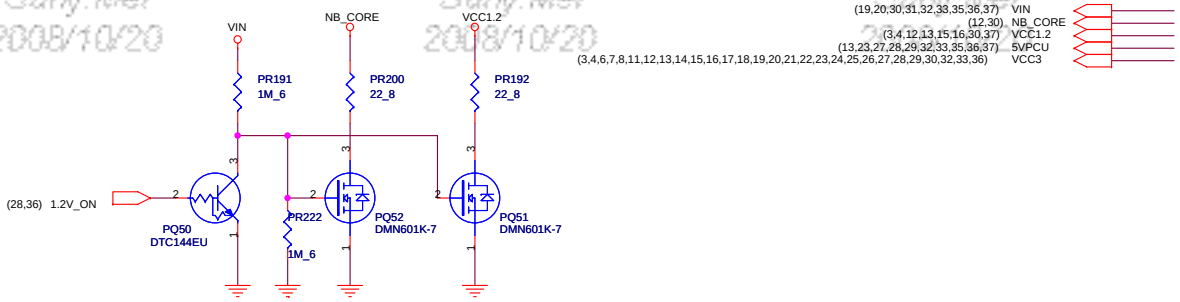




PROJECT : PF1		
Quanta Computer Inc.		
Size: C	Document Number: OZ826 CPU	Rev: 1A
Date: Wednesday, June 11, 2008	Sheet 33 of 40	

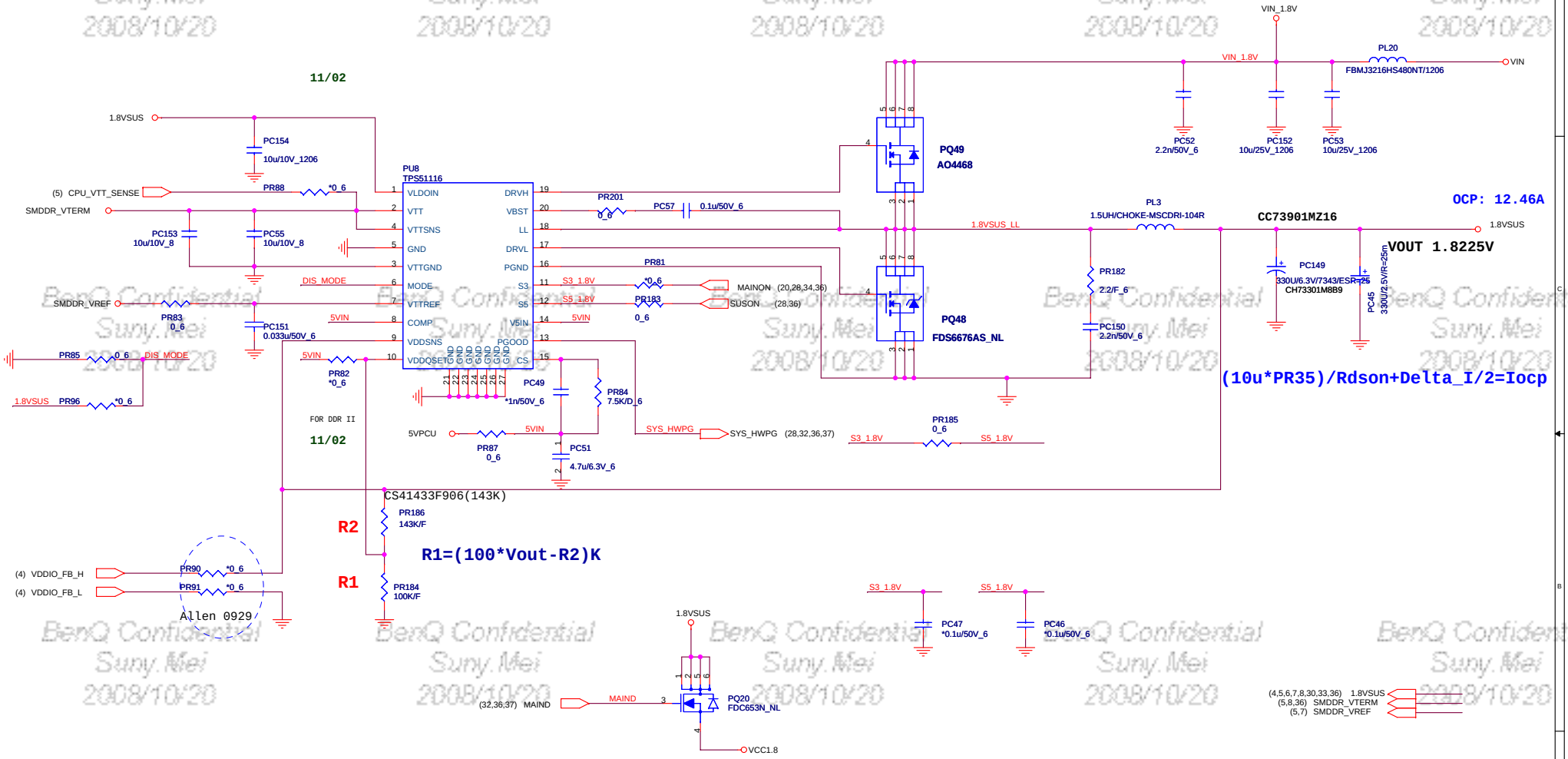


+NB_CORE_ON	+NB_CORE
High	1.02V
Low	1.12V

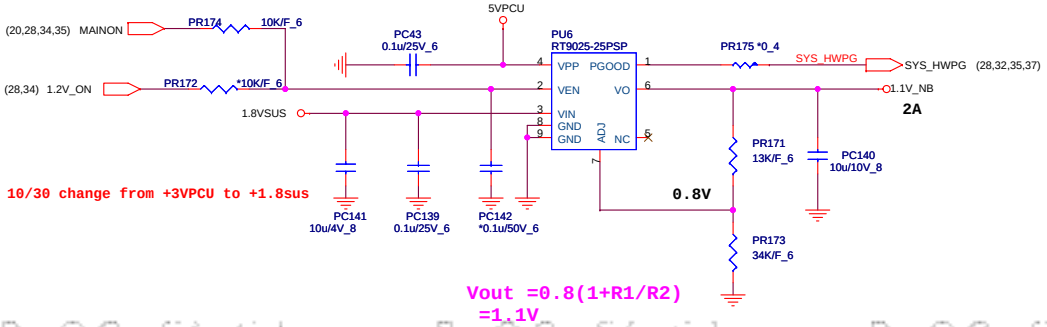


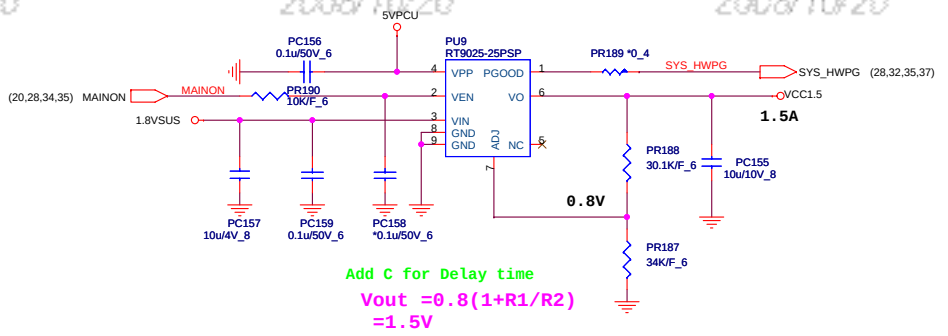
PROJECT : PF1
Quanta Computer Inc.

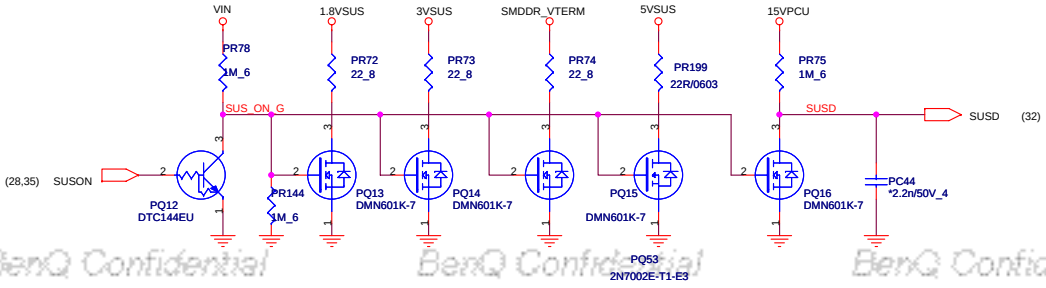
Size	Document Number	Rev
	NB_VCC (RT8202)	1A
Date: Wednesday, June 11, 2008	Sheet 34 of 40	

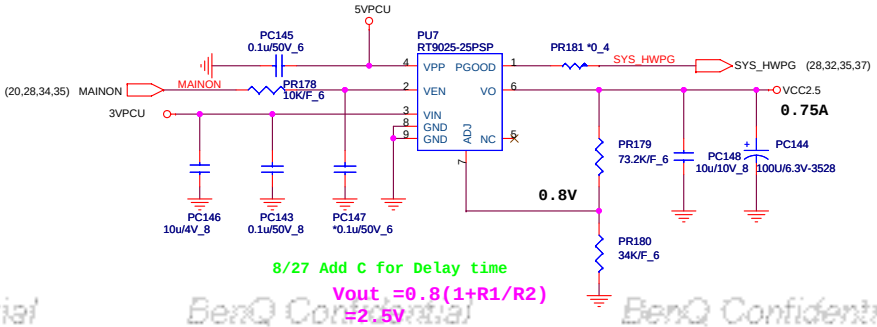


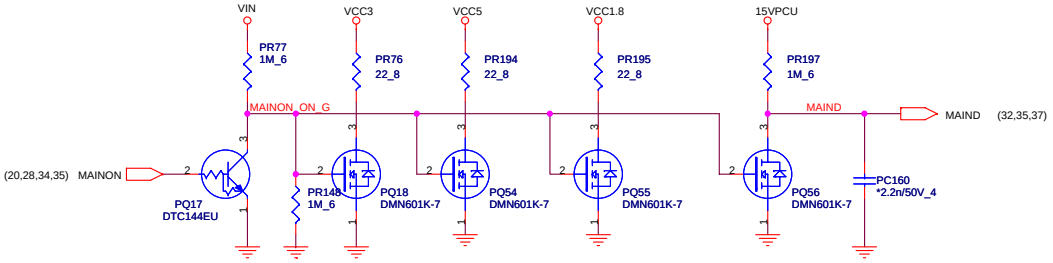
PROJECT : PF1			
Quanta Computer Inc.			
Size	Document Number		Rev
	DDR 1.8V(TPS51116)		1A
Date:	Wednesday, June 11, 2008	Sheet 35 of 40	

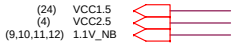






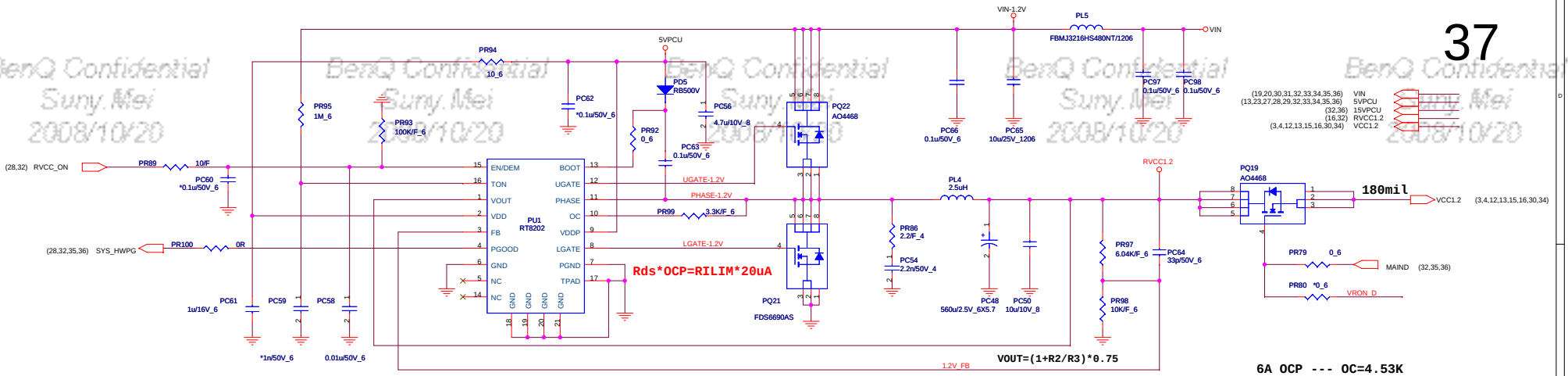






PROJECT : PF1
Quanta Computer Inc.

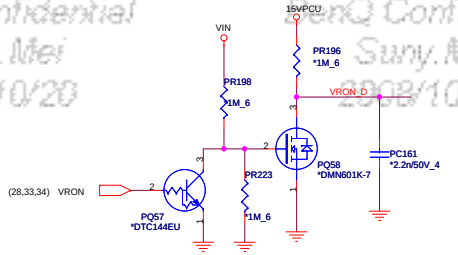
Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A
Date: Wednesday, June 11, 2008	Sheet 36 of 40	

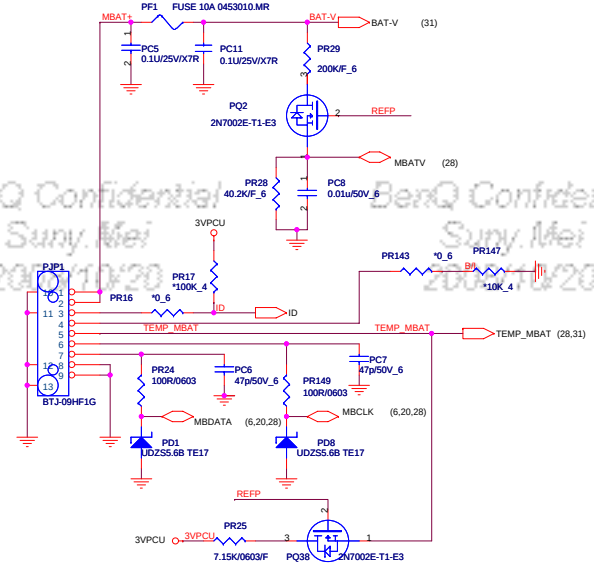


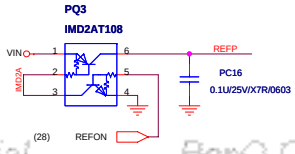
TON=3.85p*RTON*Vout/(Vin-0.5)

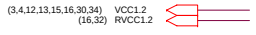
Frequency=Vout/(Vin*TON)

6A OCP --- OC=4.53K
FDS6690AS Rds=15mOhm









MBATV voltage :	
Li-ion 4S*P	16.8V*40.2/(200+40.2)= 2.812V 12.0V*40.2/(200+40.2)= 2.008V
Ni-MH 8S1P	8.0V*40.2/(200+40.2)= 1.34V

TEMP_MBAT voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

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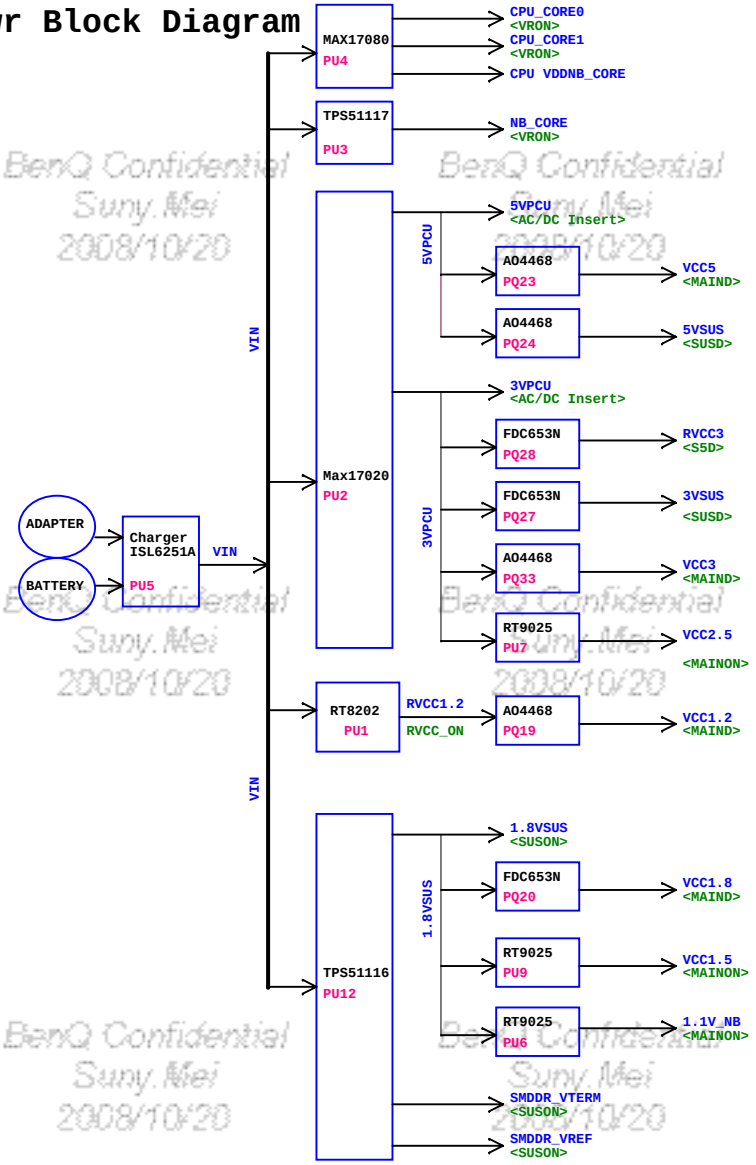
Powr Block Diagram



Below table need be modify (waiting other schematic ready)

POWER	Distribution
VCC_CORE	CPU
5VPCU	Battery LED , Power LED , CIR , RTC
3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
NB_CORE	RS780MC/RX781/RS780MN
VCC5	CAMERA , Card Reader LED , ODD/HDD LED , T/P , T/sensor , CRT , HDMI , SB700 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
VCC3	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , DVI , REQUIRED STRAPS , DEBUG STRAPS , SB700 , RS780MC , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , Headphone , EC , LAN , Audio Codec
RVCC3	WLAN , NEW CARD , SB700 , MXM , LAN
3VSUS	SB700
VCC2.5	CPU
RVCC1.2	SB700
1.8VSUS	SB700 , DDR , CPU , HDT
VCC1.8	SB700 , LCD , LVDS , RS780MC
VCC1.2	SB700 , RS780MC , CPU , WLAN , TV , NEW CARD
SMDDR_VTERM	DDR , CPU
SMDDR_VREF	DDR
5VSUS	USB

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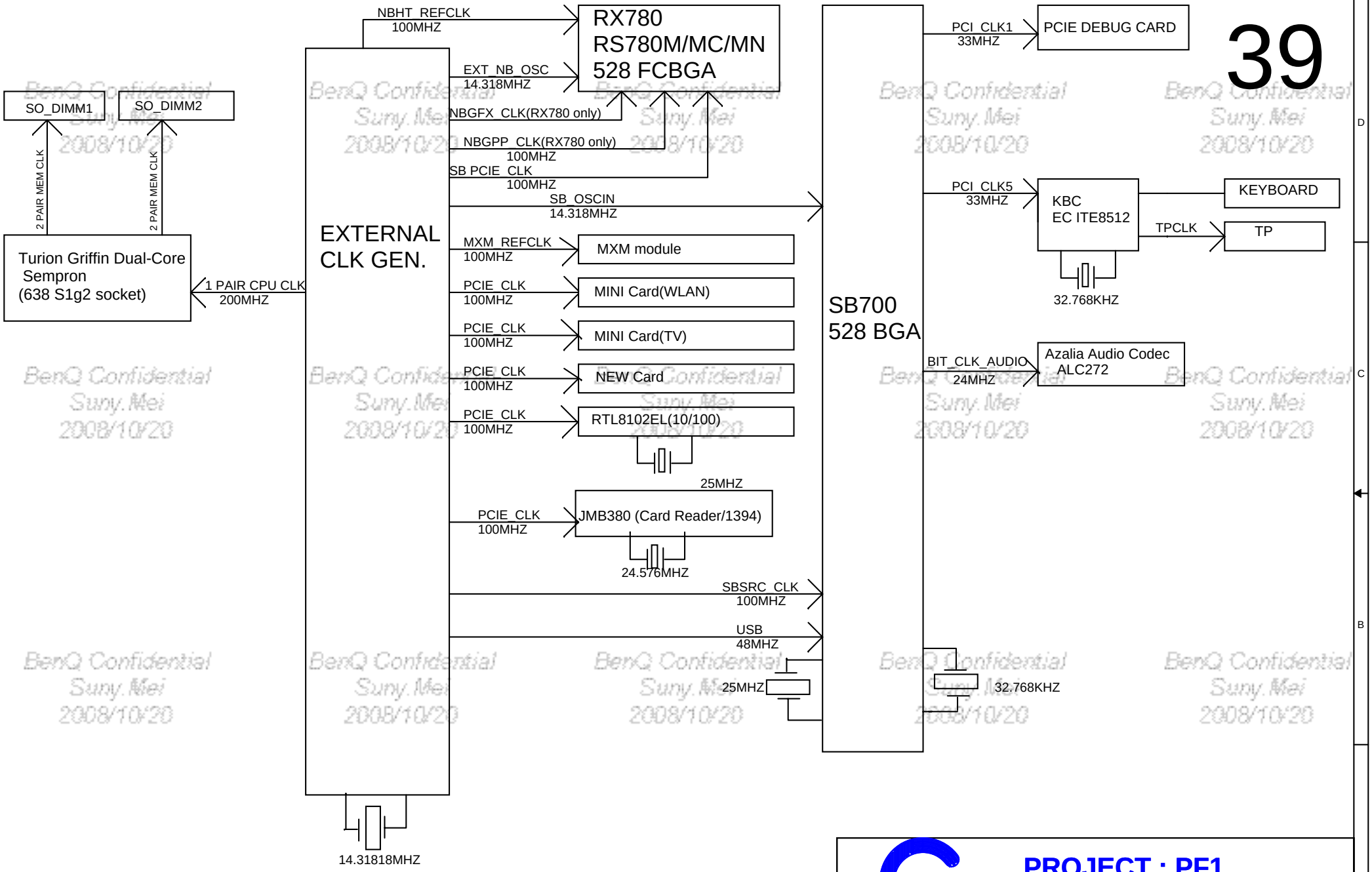

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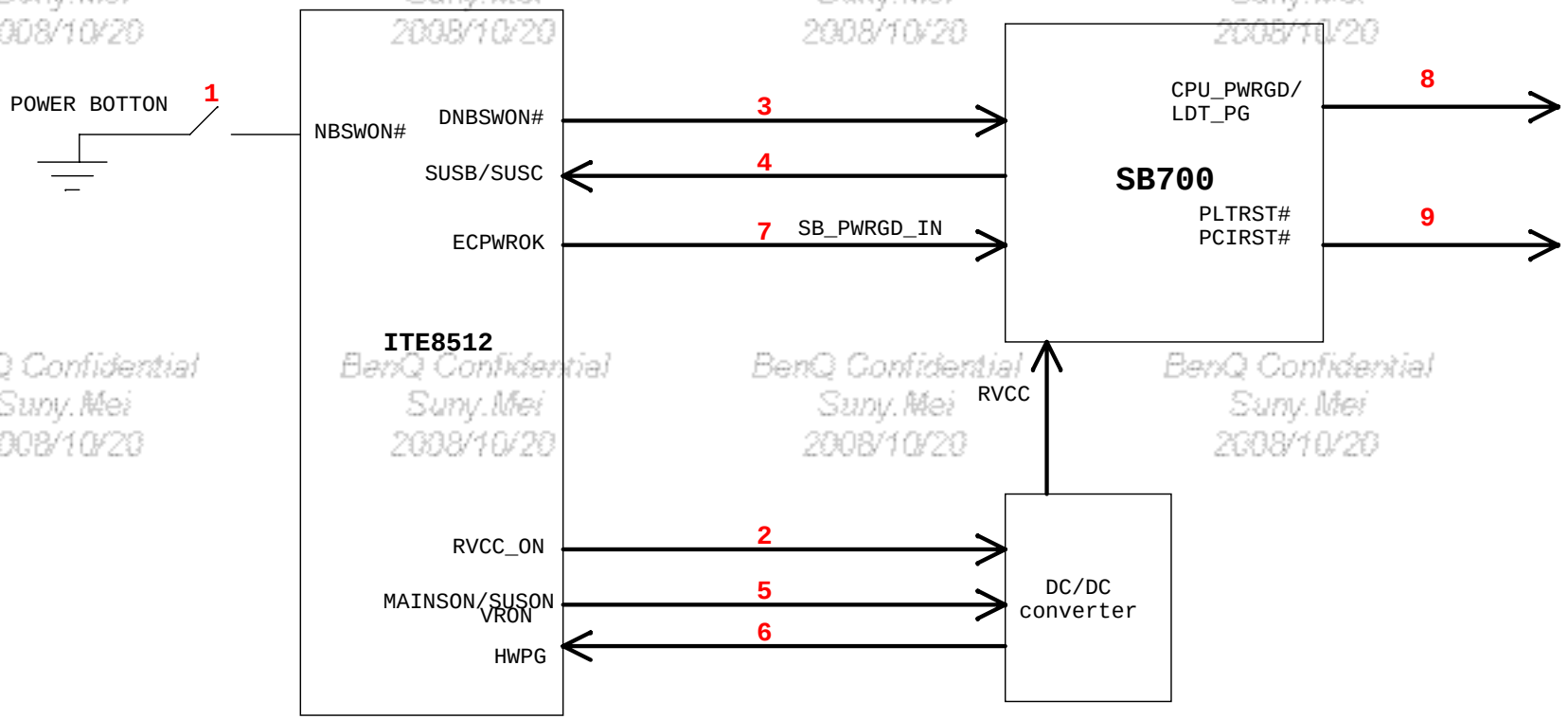
Reset&Power Good Diagram



RVCC_ON → (RSMRST#) SUSB SUSC → SUSON MAINON SUSD MAIND → HWPG VCORE_PG → EC Pin97 ECPWROK → CPU_PWRGD/ LDT_PG → PLTRST# PCIRST#

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