

Compal Confidential

Model Name : EA/EG50_CX (Z5WE1)

File Name : LA-9535P

Compal Confidential

EA/EG50_CX (Z5WE1) M/B Schematics Document

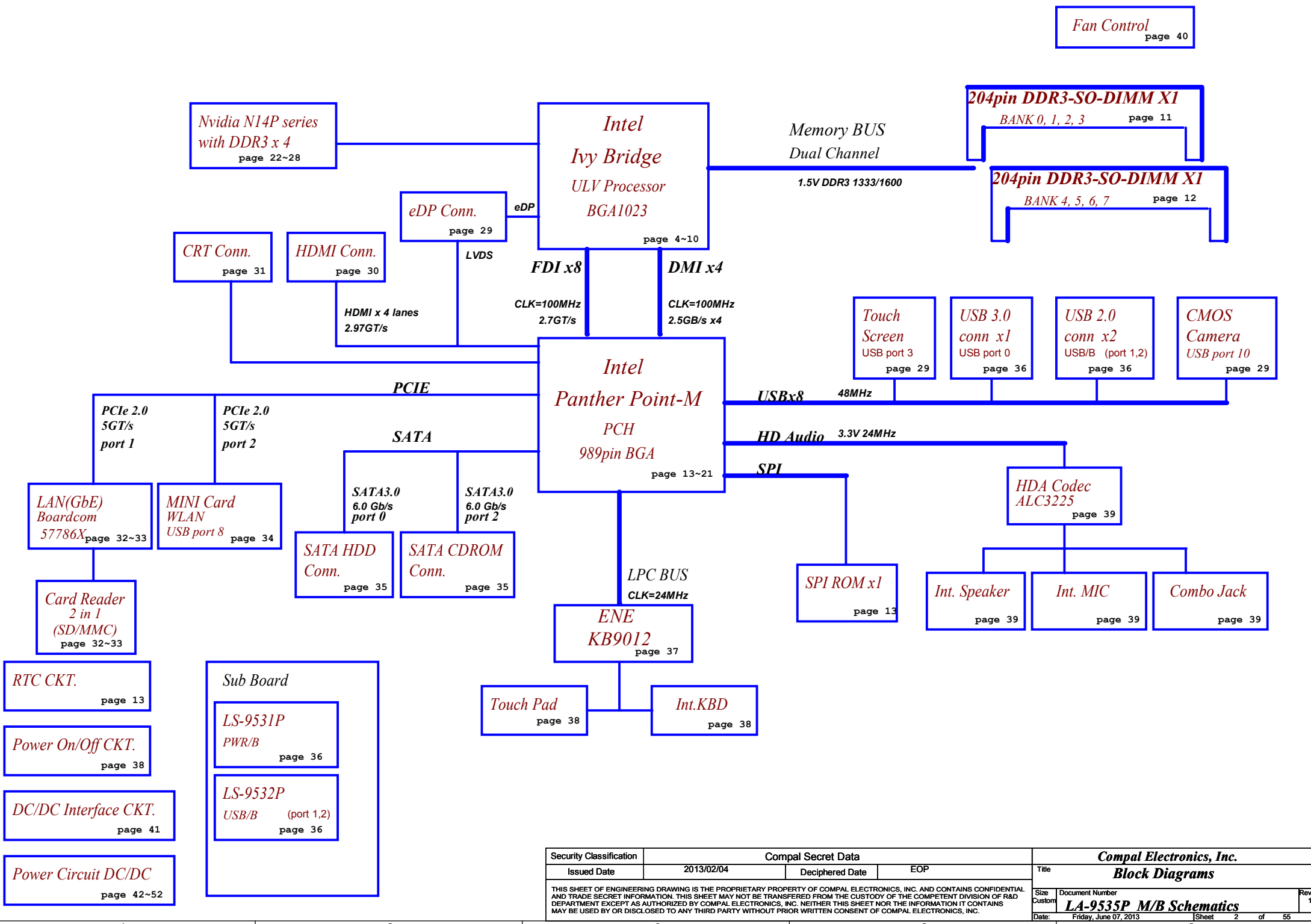
Intel Ivy Bridge ULV Processor + Panther Point PCH

Nvidia N14M-GE & N14P-GV2

2013-06-07

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/02/04	Deciphered Date	EOP	Cover Page		
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					LA-9535P M/B Schematics	1.0
				Date: Friday, June 07, 2013	Sheet 1	of 55



Fan Control
page 40

Nvidia N14P series
with DDR3 x 4
page 22~28

Intel
Ivy Bridge
ULV Processor
BGA1023
page 4~10

Memory BUS
Dual Channel

204pin DDR3-SO-DIMM X1
BANK 0, 1, 2, 3
page 11

204pin DDR3-SO-DIMM X1
BANK 4, 5, 6, 7
page 12

1.5V DDR3 1333/1600

CRT Conn.
page 31

HDMI Conn.
page 30

eDP Conn.
page 29

HDMI x 4 lanes
2.97GT/s

LVDS

FDI x8

CLK=100MHz
2.7GT/s

DMI x4

CLK=100MHz
2.5GB/s x4

Intel
Panther Point-M
PCH
989pin BGA
page 13~21

PCIe

PCIe 2.0
5GT/s
port 1

PCIe 2.0
5GT/s
port 2

SATA

SATA3.0
6.0 Gb/s
port 0

SATA3.0
6.0 Gb/s
port 2

SATA HDD
Conn.
page 35

SATA CDROM
Conn.
page 35

LAN(GbE)
Boardcom
57786X
page 32~33

MINI Card
WLAN
USB port 8
page 34

Card Reader
2 in 1
(SD/MMC)
page 32~33

RTC CKT.
page 13

Power On/Off CKT.
page 38

DC/DC Interface CKT.
page 41

Power Circuit DC/DC
page 42~52

Sub Board

LS-9531P
PWR/B
page 36

LS-9532P
USB/B (port 1,2)
page 36

Touch
Screen
USB port 3
page 29

USB 3.0
conn x1
USB port 0
page 36

USB 2.0
conn x2
USB/B (port 1,2)
page 36

CMOS
Camera
USB port 10
page 29

USBx8

48MHz

HD Audio

3.3V 24MHz

SPI

SPI ROM x1
page 13

HDA Codec
ALC3225
page 39

Int. Speaker
page 39

Int. MIC
page 39

Combo Jack
page 39

LPC BUS
CLK=24MHz

ENE
KB9012
page 37

Touch Pad
page 38

Int.KBD
page 38

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				Date: Friday, June 07, 2013	Sheet 2 of 55	

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.75VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	+0.95VSDGPUP to +0.95VSDGPU switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.35VP to +1.35V power rail for DDRIML	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VSDGPUP to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	+3VS to 1.8V switched power rail to CPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU switched power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X	VGA Internal Thermal Sensor	1001 111x (0x9E)

EC SM Bus2 address

PCH SM Bus address

Device	Address
ChannelA DIMM0	1001 000x JDIMM1
ChannelB DIMM1	1001 010x JDIMM2

BOM Config

UMAO: EDP@/IOAC@/BL@/EMC@/UMAO@/
DIS GV2: EDP@/IOAC@/BL@/EMC@/VGA@/
DIS GE: EDP@/IOAC@/BL@/EMC@/VGA@/

CPU config
CPU config + X76
CPU config + X76

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID_min	VAD_BID_typ	VAD_BID_max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

USB Port Table

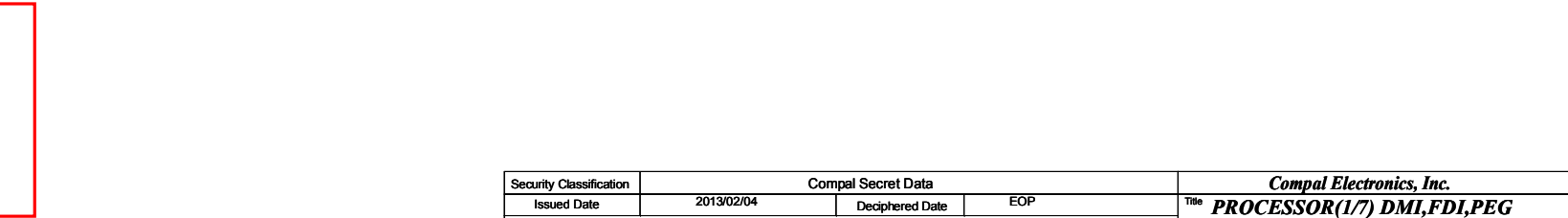
USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	Touch Screen
	4	
	5	
	6	
	7	

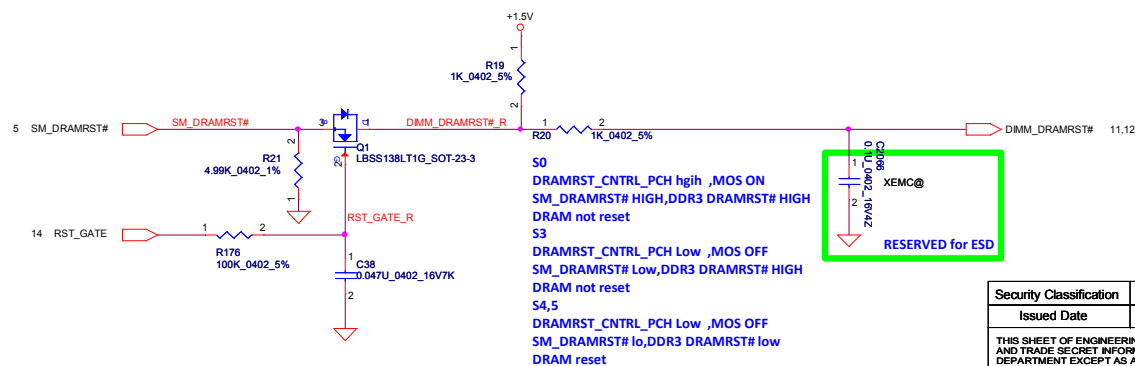
USB 2.0	Port	
EHCI2	8	Mini Card (WLAN+BT)
	9	
	10	Camera
	11	
	12	
	13	

USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
	3	

BTO Option Table

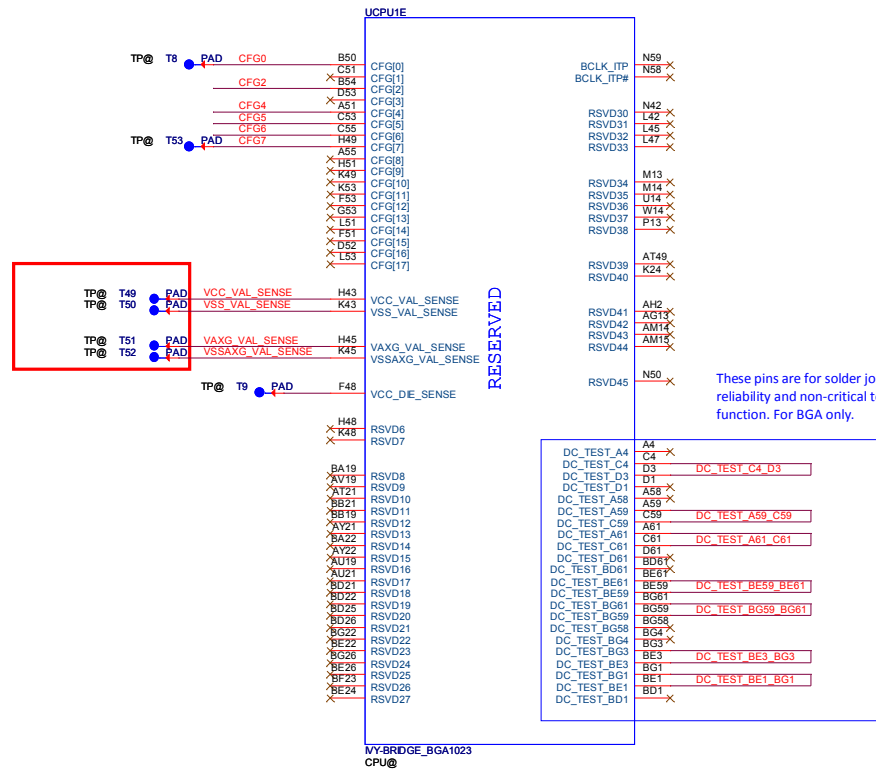
BTO Item	BOM Structure
Unpop	@
Connector	CONN@
PCH RTC CMOS	SP@
TEST PAD	TP@
Unpop SPI2	SPI2@
Unpop CPU	CPU@
Unpop GPU	GPU@
Unpop VRAM	VRAM@
Back light	BL@
IOAC	IOAC@
Celeron 847	847@
Celeron 1007	1007@
I3-3227M	I33227@
I5-3337M	I53337@
I7-3537M	I73537@
UMA ONLY GPIO	UMAO@
EDP	EDP@
LVDS	LVDS@
EMC POP	EMC@
EMC NON POP	XEMC@
N14M-GE option	N14MGE@
N14P-GT option	N14PGT@
N14P-GV2 option	N14PGV2@
N14P-GT/GV2 Strap	GV2GT@
VGA SKU	VGA@
VRAM x 8pcs	128@
PEG 16X	16X@
PEG 8X	8X@
GC6	GC6@
NON GC6	NGC6@



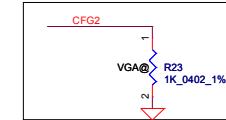


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Size	Document Number	Rev
Custom	LA-9535P M/B Schematics	1.0
Date	Friday, June 07, 2013	
	Sheet 6 of 55	



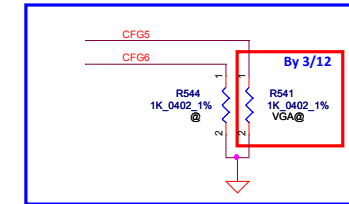
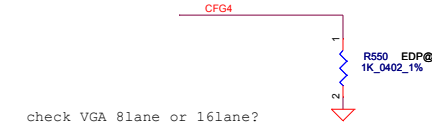
CFG Straps for Processor



current placement need to support
PEG bus lan reversal

PCIe Static x16 Lane Numbering Reversal

CFG2	1: (Default)Normal Operation Lane # definition matches socket pin map definition
* 0:	Lane Reversed



eDP Enable Strap

CFG4	1: (Default)Disable
* 0:	Enable

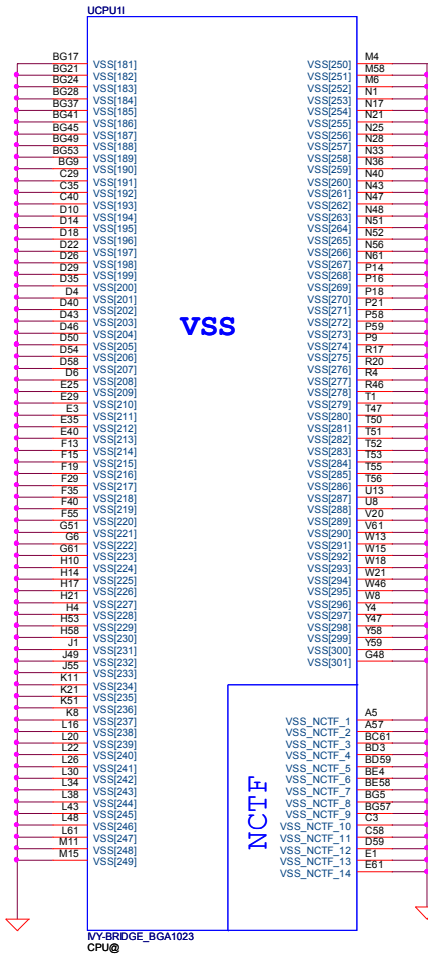
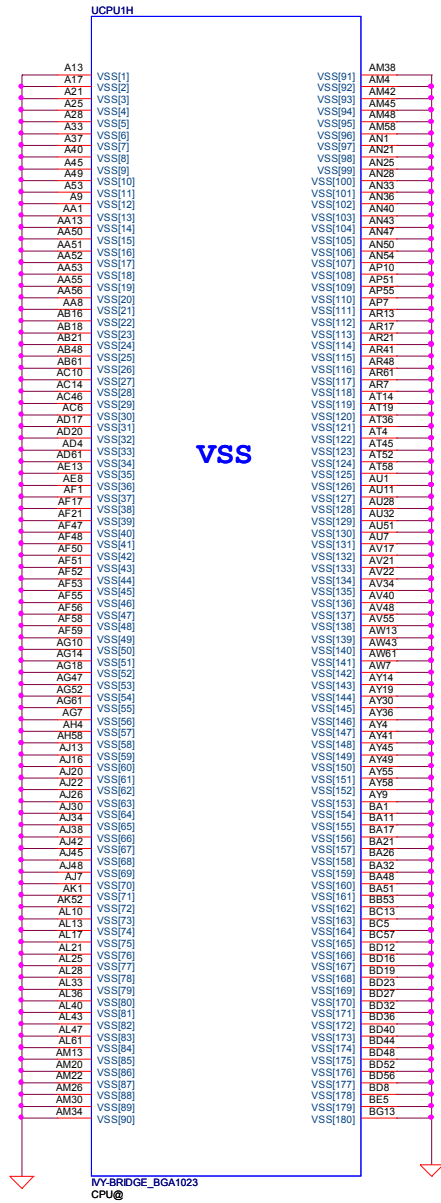
PCIe Port Bifurcation Straps

CFG[6:5]	11: (Default) 1x16 PCI Express
* 10:	2x8 PCI Express
01:	Reserved
00:	1x8,2x4 PCI Express

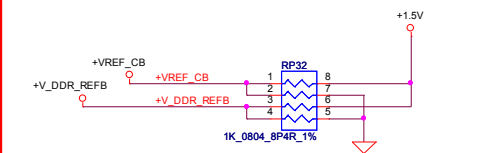
PEG DEFER TRAINING Tacoma_Fall2 1.0 P.12

CFG7	* 1: (Default) PEG Trains immediately and follows xxRESETB de-assertion
0:	PEG Wait for BIOS for training

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Date:	Friday, June 07, 2013	Sheet	7	of	55	

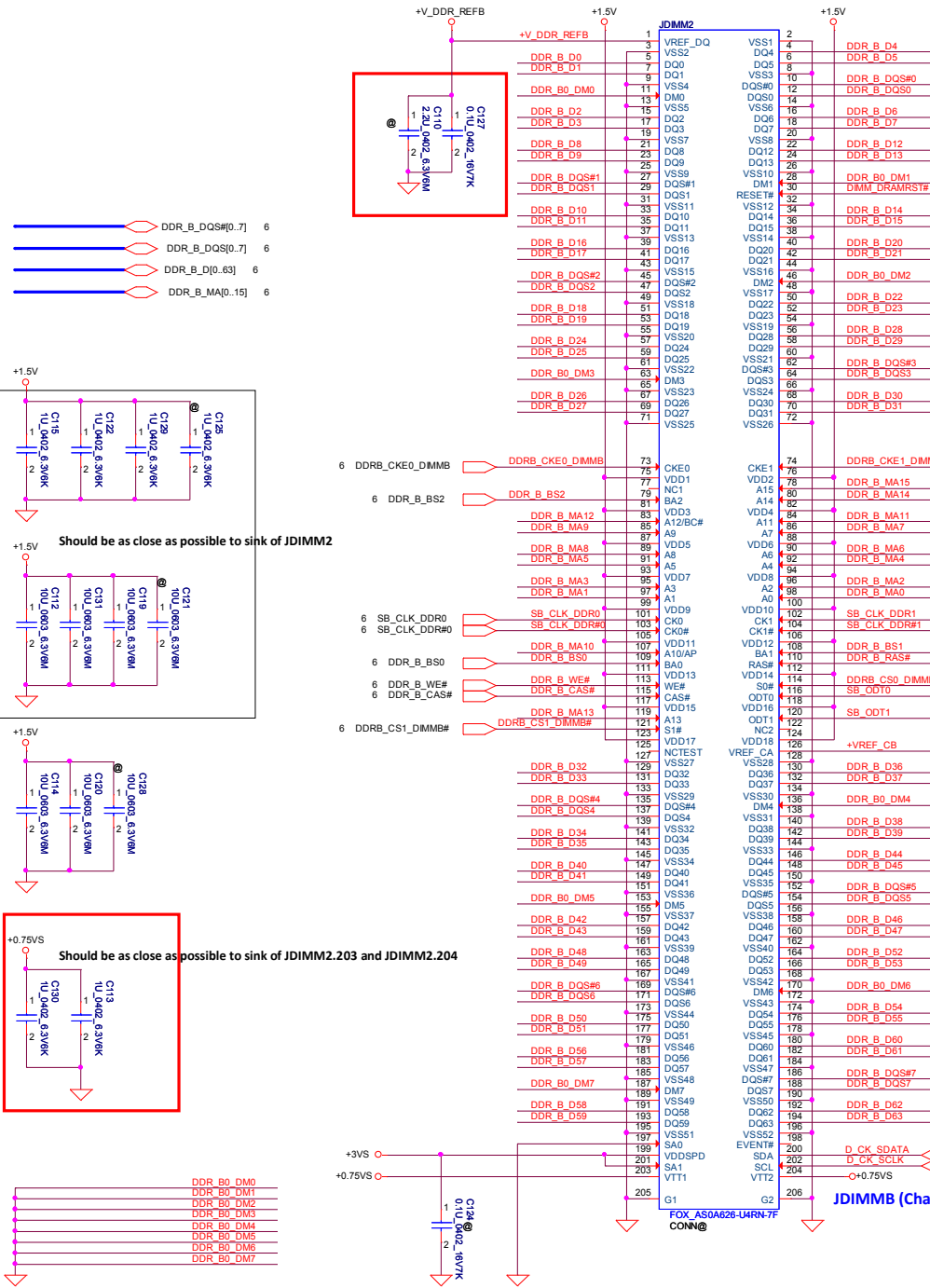


RP 1% P/N SD300002V00



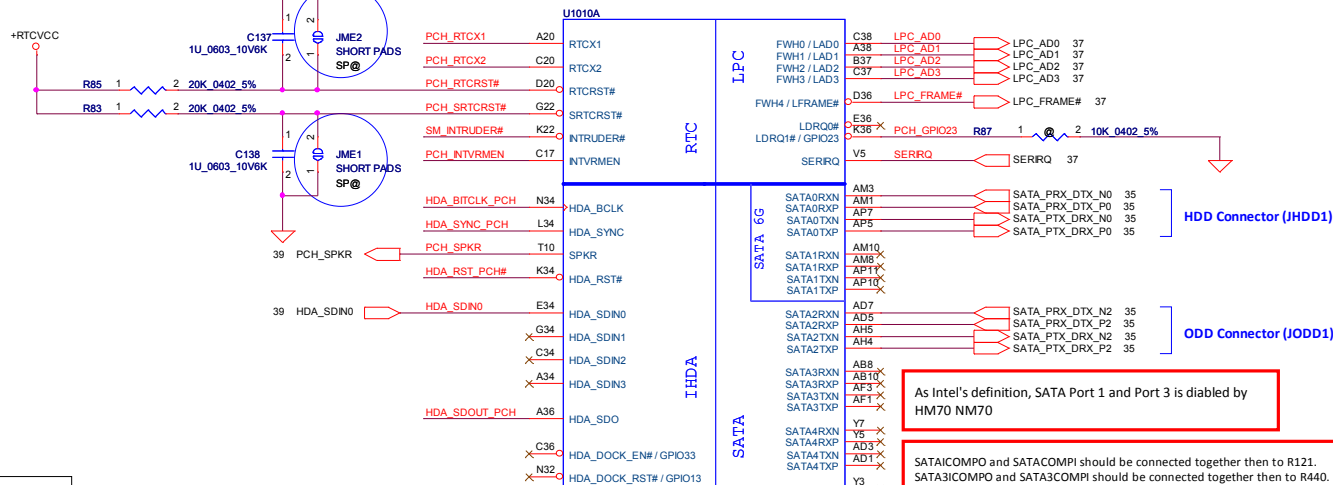
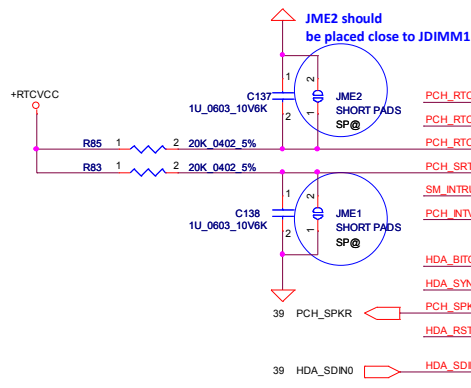
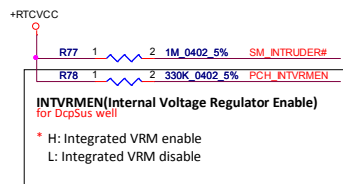
All VREF_DQ and VREFCA should be routed with width at least 20-mil and with spacing at least 20-mil.

1. +V_DDR_REFB
2. +VREF_CB



JDIMMB (Channel B) H4 RVS TYPE Slot

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					Size	Document Number	Rev
					Custodian	LA-9535P M/B Schematics	1.0
Date:		Friday, June 07, 2013		Sheet	12	of 55	

[illegible]

37 HDA_SDOUT_PCH

Reserve for EMI

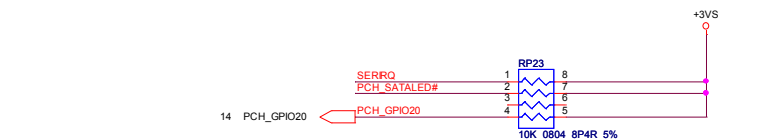
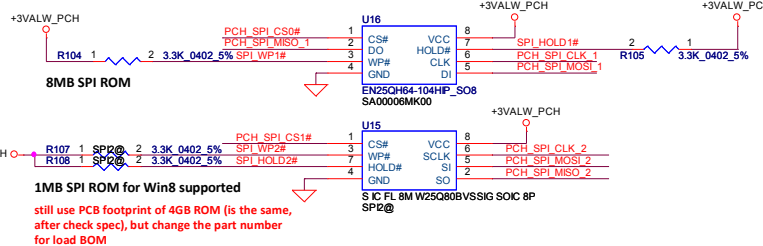
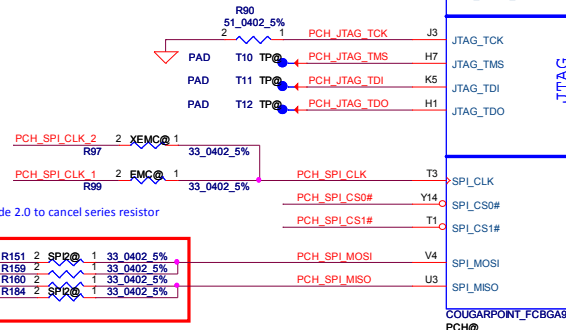
C141
10P_0402_50V8J

1 2

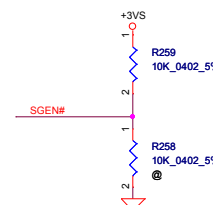
2 1

XEMC@ R109 XEMC@

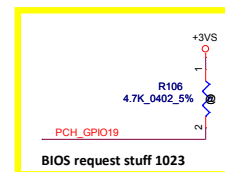
PCH_SPI_CLK 33_0402_5%



SATA1COMPO and SATA1COMPI should be connected together then to R121.
SATA31COMPO and SATA31COMPI should be connected together then to R440.
Trace Impedance= 50-ohm
Keep-out to other Signals, especially to CLK= 15-mil

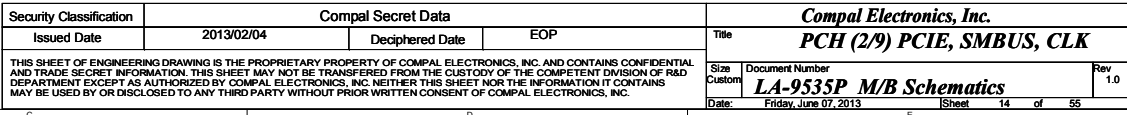


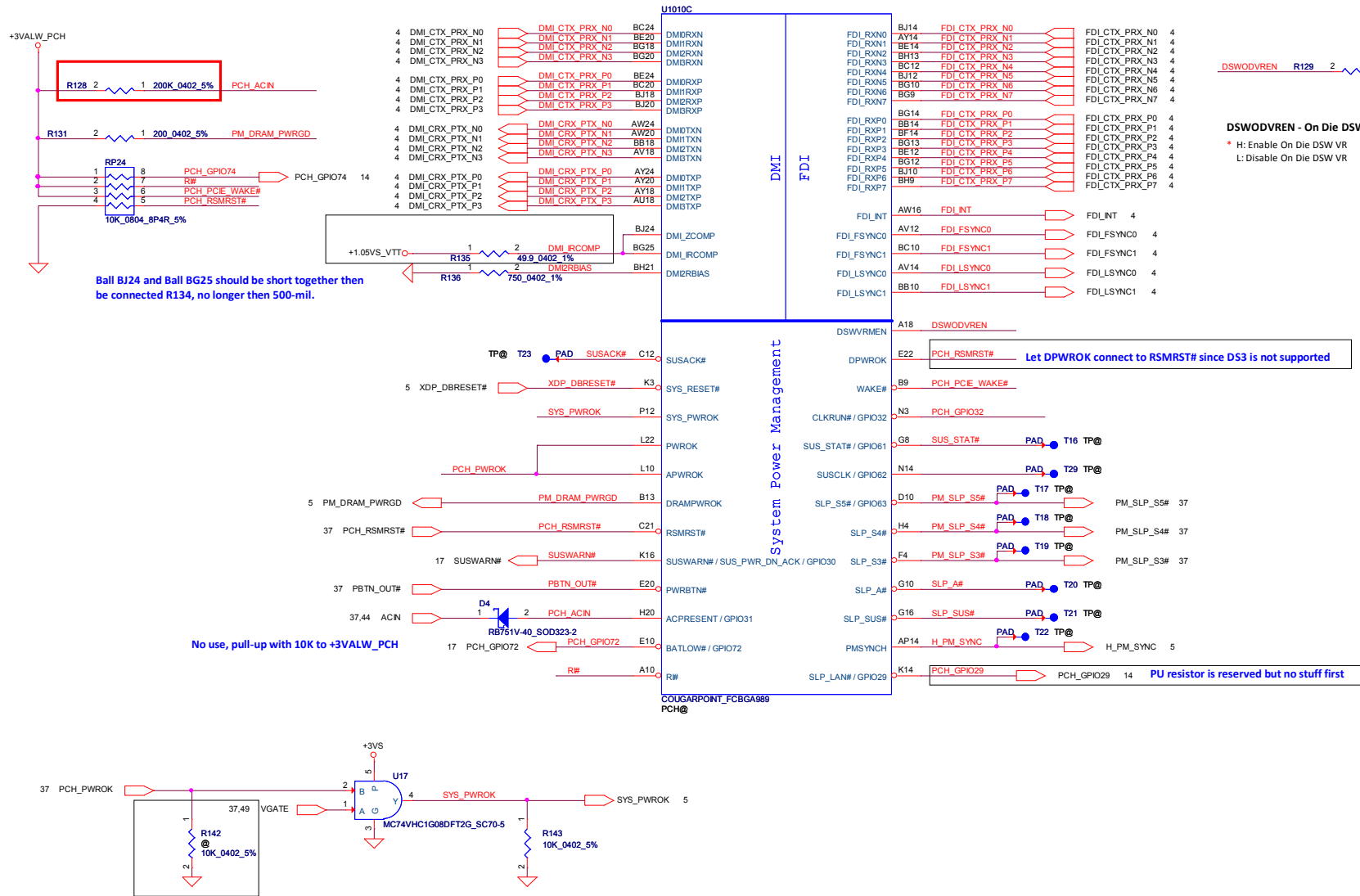
	GPIO21 SGEN#
Switchable GPU	0
*Non-Switchable	1

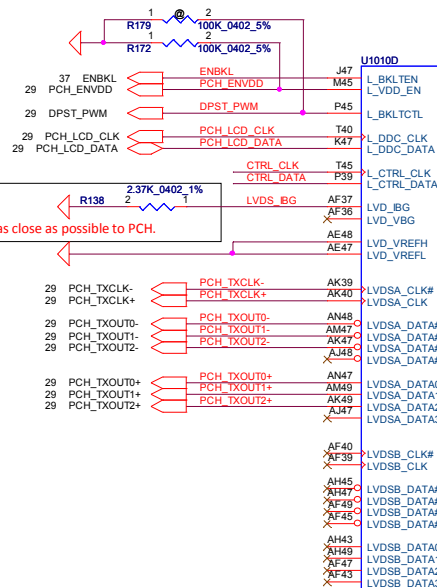
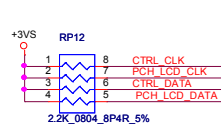


Boot BIOS Destination Selection		
Routing	GTN1#/GPIO51 (BBS1)	SATA1GP/GPIO19 (BBS0)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1

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				Date:	Friday, June 07, 2013
				Sheet	13 of 55

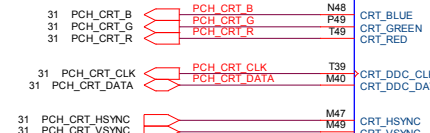
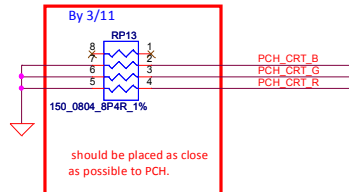




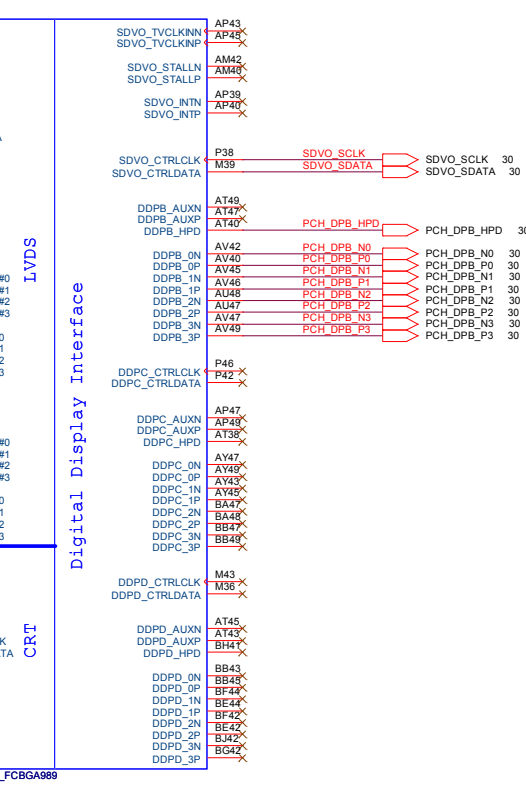


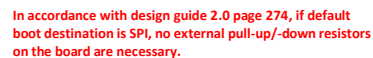
should be placed as close as possible to PCH.

If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects. The supply pins VCC1X_LVDS and VCCA_LVD can be connected to ground.

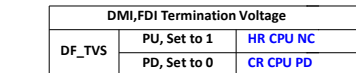
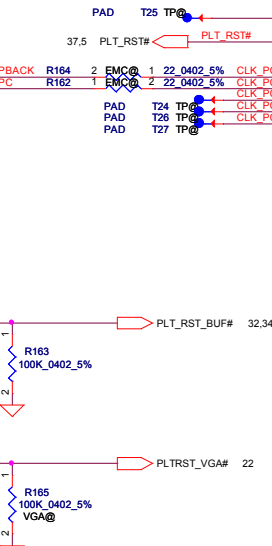


should be placed as close as possible to PCH T43, and keep the trace is at least 30-mil away from other signals (especially clocks).





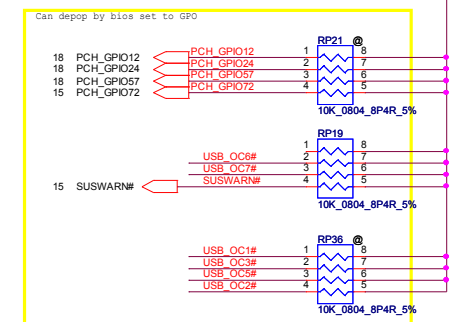
Boot BIOS Destination Selection		
Routing	GTN1#/GPIO51 (BBS1)	SATA1GP/GPIO19 (BBS0)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1



EDS

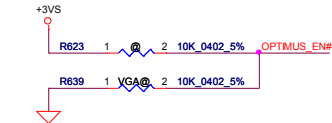
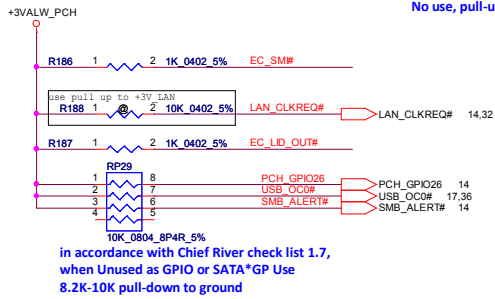
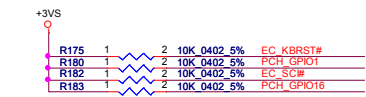
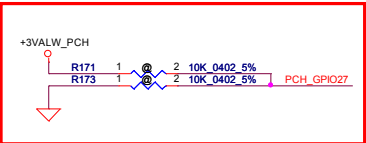
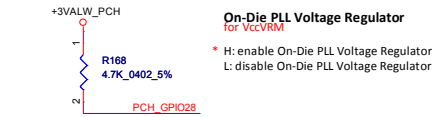
Processor Select: This pin is an output that indicates if the processor used is Sandy Bridge or Ivy Bridge. For Sandy Bridge the output will be high, and for Ivy Bridge the output will be low

Sandy Bridge + Ivy Bridge Compatible:
 Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1k $\pm$ 5% series resistor. PROC_SELECT# also needs a 2.2K $\pm$ 5% pull up resistor to PCH VccDFTerm rail.

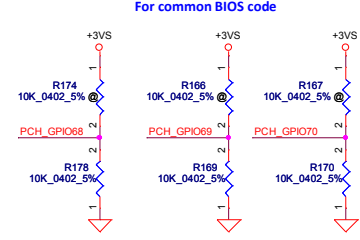
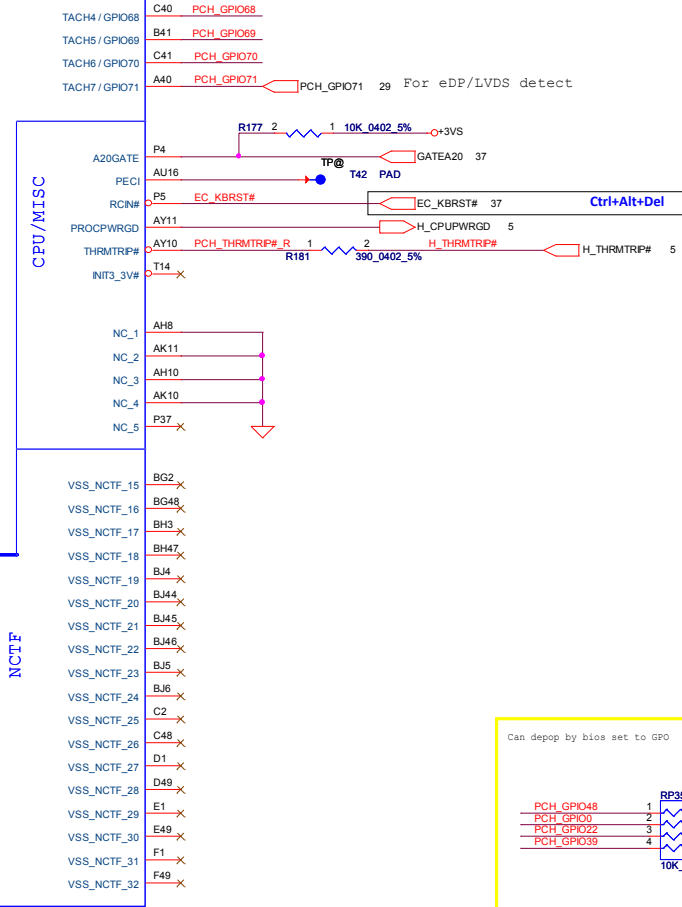
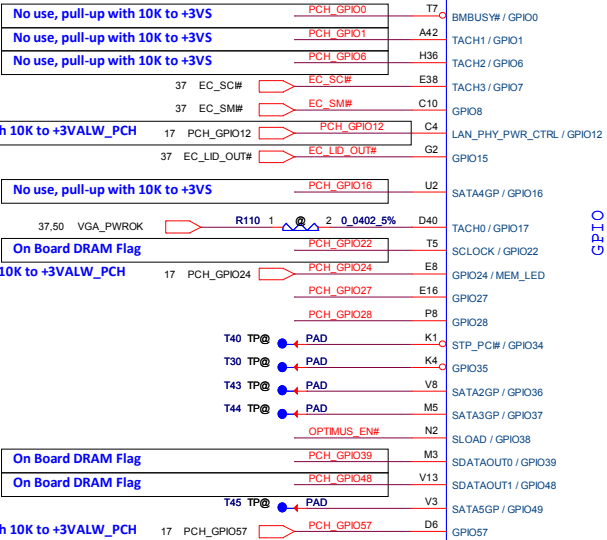


	HM77	HM70	NM70	Note
USB2.0	14	8	8	HM70/NM70 USB port 4, 5, 6,7,12 and 13 are disabled on 8 port SKUs.
USB3.0	4	2	0	USB 3.0 port 3 and 4 are disabled on HM70 USB 3.0 are all disabled on NM70
PCIe	8	4	4	HM70/NM70 PCIe port 5–8 are disabled on this SKU.
SATA	6	4	4	HM70/NM70 SATA port 1 and 3 are disabled on 4 port SKUs. HM70/NM70 SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s & 1.5 Gb/s HM77 SATA 6 Gb/s support on port 0 & port 1. SATA port 0 and 1 also support 3 Gb/s & 1.5 Gb/s.

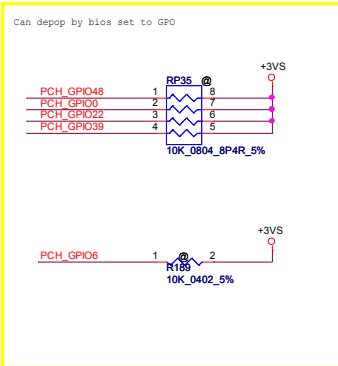
Security Classification	Compal Secret Data			Compal Electronics, Inc. PCH (5/9) PCI, USB, NVRAM		
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				Date:	Friday, June 07, 2013	Sheet 17 of 55

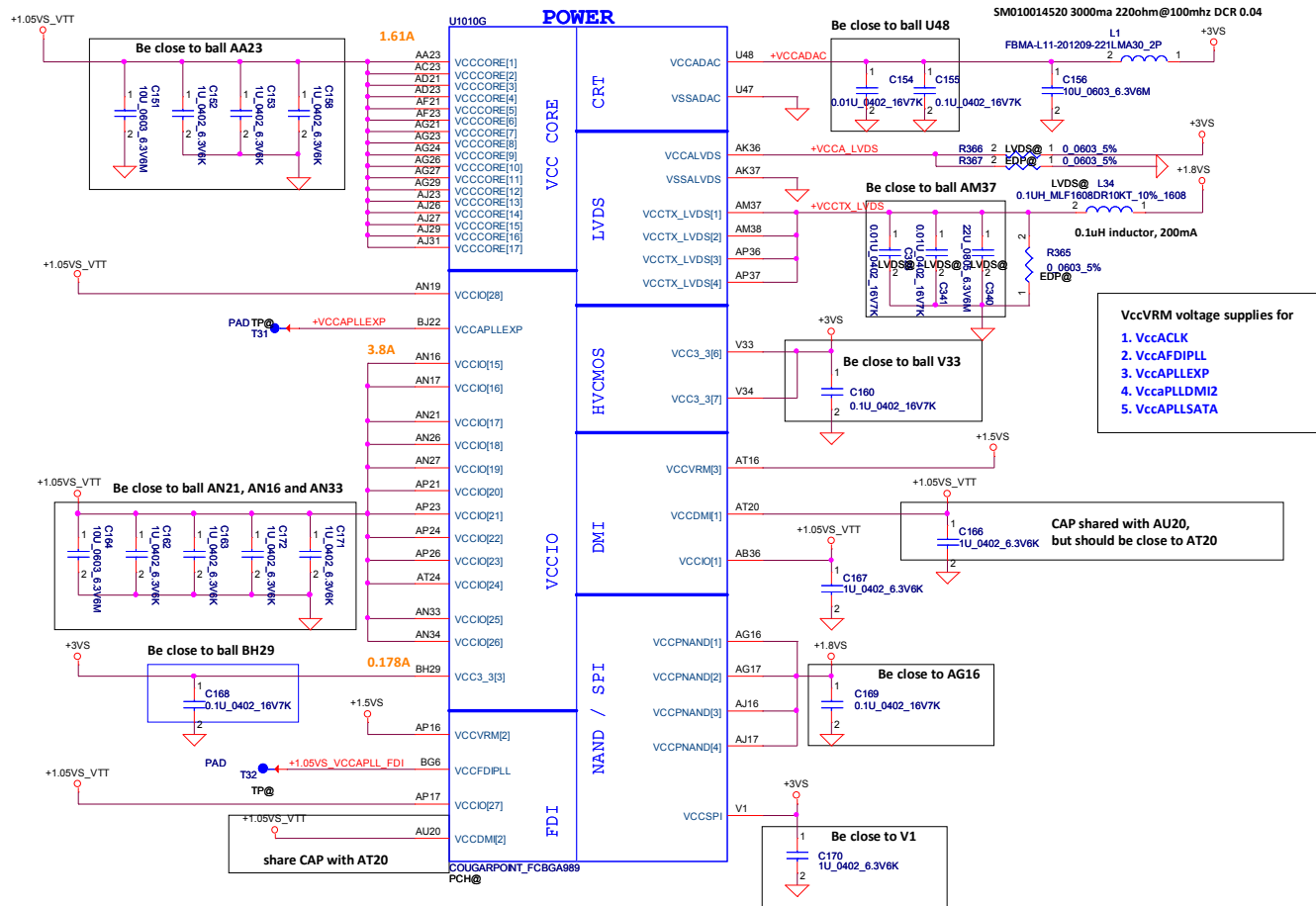


	GPIO38
	OPTIMUS_EN#
* OPTIMUS	0
DIS Only	1



Project ID	GPIO68	GPIO69	GPIO70
Q5WE0	1	0	0
Q7YE0	1	0	1
Q5Wxx-QC	1	1	0
V5VT1	1	1	1
*Z5WE1_CR	0	0	0





Refer to Intel® 7 Series / C216 Chipset Family Platform Controller Hub (PCH) External Design Specification (EDS) Revision 2.1

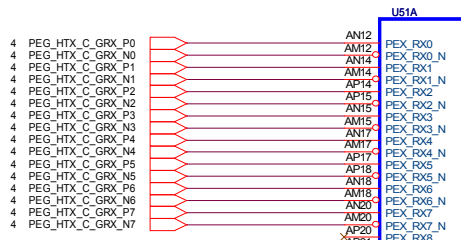
PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/O
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltage
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLL	1.05	0.075	Display PLL A power
VccADPLL	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW3_3	3.3	0.001	3.3v supply for Deep Sx well
VccDFTERN (VccPNAND)	1.8	0.002	1.8V power supply for DF_TV5
VccRTC	3.3	6 uA	RTC Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.5	0.147	1.5 V Internal PLL and VRMs
VccCLKDMI	1.05	0.075	DMI differential Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.05	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.04	I/O power supply for LVDS (Mobile Only)

U1010H		
H5	VSS[0]	
AA17	VSS[1]	AK38
AA2	VSS[2]	
AA3	VSS[3]	
AA33	VSS[4]	
AA34	VSS[5]	
AB11	VSS[6]	
AB14	VSS[7]	
AB39	VSS[8]	
AB4	VSS[9]	
AB43	VSS[10]	
AB5	VSS[11]	
AB7	VSS[12]	
AC19	VSS[13]	
AC2	VSS[14]	
AC21	VSS[15]	
AC24	VSS[16]	
AC33	VSS[17]	
AC34	VSS[18]	
AC48	VSS[19]	
AD10	VSS[20]	
AD11	VSS[21]	
AD12	VSS[22]	
AD13	VSS[23]	
AD19	VSS[24]	
AD24	VSS[25]	
AD26	VSS[26]	
AD27	VSS[27]	
AD33	VSS[28]	
AD34	VSS[29]	
AD36	VSS[30]	
AD37	VSS[31]	
AD38	VSS[32]	
AD39	VSS[33]	
AD4	VSS[34]	
AD40	VSS[35]	
AD42	VSS[36]	
AD43	VSS[37]	
AD45	VSS[38]	
AD46	VSS[39]	
AD8	VSS[40]	
AE2	VSS[41]	
AE3	VSS[42]	
AF10	VSS[43]	
AF12	VSS[44]	
AD14	VSS[45]	
AD16	VSS[46]	
AF16	VSS[47]	
AF19	VSS[48]	
AF24	VSS[49]	
AF26	VSS[50]	
AF27	VSS[51]	
AF29	VSS[52]	
AF31	VSS[53]	
AF38	VSS[54]	
AF4	VSS[55]	
AF42	VSS[56]	
AF46	VSS[57]	
AF5	VSS[58]	
AF7	VSS[59]	
AF8	VSS[60]	
AG19	VSS[61]	
AG32	VSS[62]	
AG31	VSS[63]	
AG48	VSS[64]	
AH11	VSS[65]	
AH3	VSS[66]	
AH36	VSS[67]	
AH39	VSS[68]	
AH40	VSS[69]	
AH42	VSS[70]	
AH46	VSS[71]	
AH7	VSS[72]	
AJ19	VSS[73]	
AJ21	VSS[74]	
AJ24	VSS[75]	
AJ33	VSS[76]	
AJ34	VSS[77]	
AK12	VSS[78]	
AK3	VSS[79]	

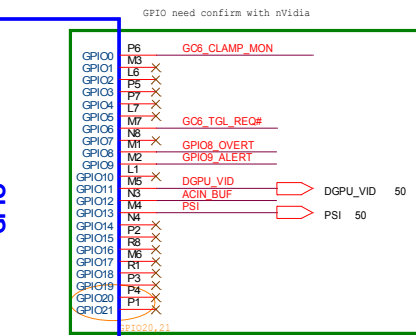
COUGARPOINT_FCBGA989
PCH@

U1010I		
AY4	VSS[159]	H46
AY42	VSS[160]	K18
AY46	VSS[161]	K26
AY8	VSS[162]	K39
B11	VSS[163]	K46
B15	VSS[164]	K7
B19	VSS[165]	L18
B23	VSS[166]	L2
B27	VSS[167]	L20
B31	VSS[168]	L26
B35	VSS[169]	L28
B39	VSS[170]	L36
B45	VSS[171]	L48
F46	VSS[172]	M12
BB12	VSS[173]	P16
BB16	VSS[174]	M18
BB20	VSS[175]	M22
AL2	VSS[176]	M24
BB22	VSS[177]	M30
BB24	VSS[178]	M32
BB26	VSS[179]	M34
BB30	VSS[180]	M38
BB38	VSS[181]	M4
BB4	VSS[182]	M42
BC14	VSS[183]	M46
BC18	VSS[184]	M8
BC2	VSS[185]	N18
BC22	VSS[186]	P30
BC26	VSS[187]	N47
BC32	VSS[188]	P11
BC34	VSS[189]	P18
BC36	VSS[190]	P33
BC40	VSS[191]	P40
BC42	VSS[192]	P43
BC48	VSS[193]	P47
AN3	VSS[194]	P7
AN31	VSS[195]	R2
BE22	VSS[196]	R48
BE26	VSS[197]	T12
BE40	VSS[198]	T31
BF10	VSS[199]	VSS[298]
BF12	VSS[200]	VSS[299]
BF16	VSS[201]	VSS[300]
BF20	VSS[202]	VSS[301]
BF22	VSS[203]	VSS[302]
BF24	VSS[204]	VSS[303]
BF26	VSS[205]	VSS[304]
BF28	VSS[206]	VSS[305]
BF30	VSS[207]	VSS[306]
BF38	VSS[208]	VSS[307]
BF40	VSS[209]	VSS[308]
BF8	VSS[210]	VSS[309]
BG17	VSS[211]	VSS[310]
BG21	VSS[212]	VSS[311]
BG33	VSS[213]	VSS[312]
BG44	VSS[214]	VSS[313]
BH11	VSS[215]	VSS[314]
BH12	VSS[216]	VSS[315]
BH15	VSS[217]	VSS[316]
BH17	VSS[218]	VSS[317]
BH19	VSS[219]	VSS[318]
BH22	VSS[220]	VSS[319]
BH27	VSS[221]	VSS[320]
BH31	VSS[222]	VSS[321]
BH33	VSS[223]	VSS[322]
BH35	VSS[224]	VSS[323]
BH39	VSS[225]	VSS[324]
BH43	VSS[226]	VSS[325]
BH7	VSS[227]	VSS[326]
D3	VSS[228]	VSS[327]
D12	VSS[229]	VSS[328]
D16	VSS[230]	VSS[329]
D18	VSS[231]	VSS[330]
D22	VSS[232]	VSS[331]
D24	VSS[233]	VSS[332]
D26	VSS[234]	VSS[333]
D30	VSS[235]	VSS[334]
D32	VSS[236]	VSS[335]
D34	VSS[237]	VSS[336]
D38	VSS[238]	VSS[337]
D42	VSS[239]	VSS[338]
D8	VSS[240]	VSS[339]
E18	VSS[241]	VSS[340]
E26	VSS[242]	VSS[341]
G18	VSS[243]	VSS[342]
G20	VSS[244]	VSS[343]
G26	VSS[245]	VSS[344]
G28	VSS[246]	VSS[345]
G36	VSS[247]	VSS[346]
G48	VSS[248]	VSS[347]
H12	VSS[249]	VSS[348]
H18	VSS[250]	VSS[349]
H22	VSS[251]	VSS[350]
H24	VSS[252]	VSS[351]
H26	VSS[253]	VSS[352]
H30	VSS[254]	
H32	VSS[255]	
H34	VSS[256]	
F3	VSS[257]	
	VSS[258]	

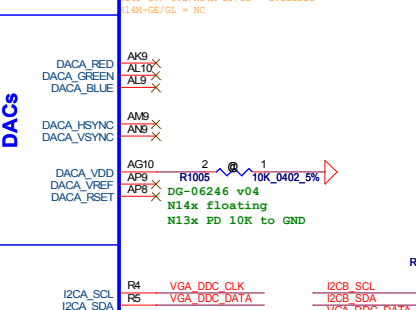
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PCH@



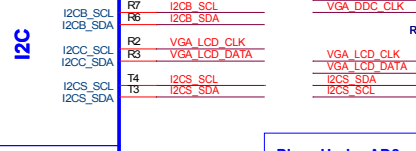
GPIO



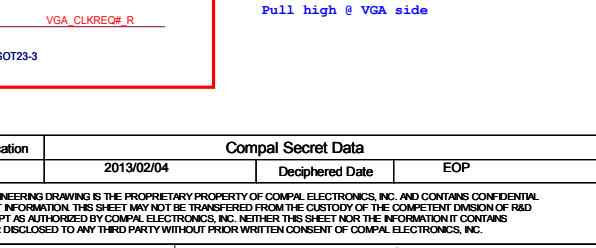
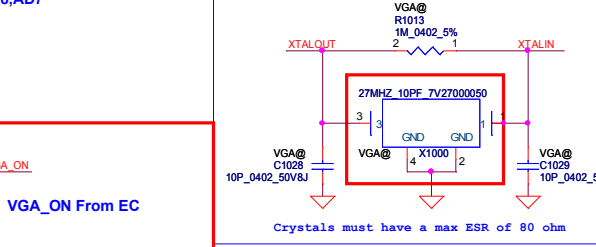
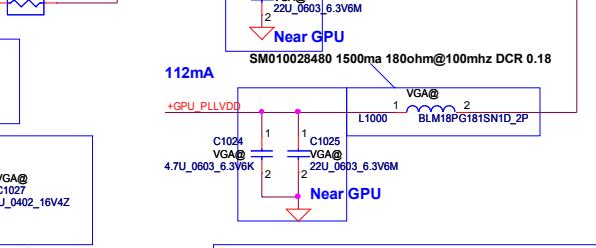
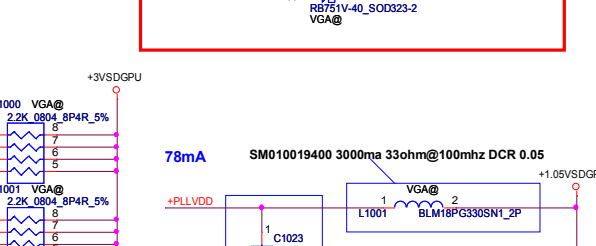
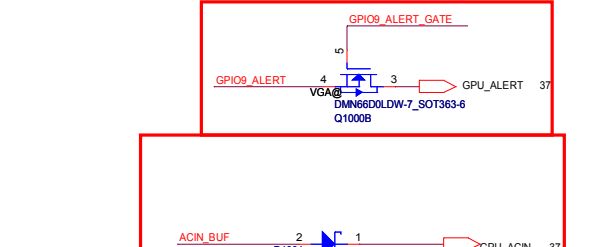
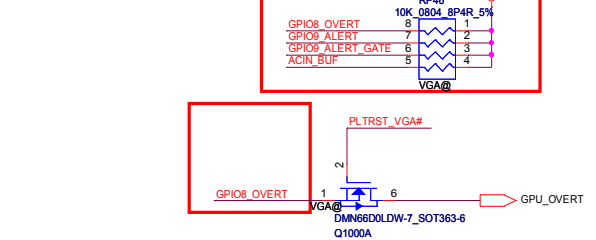
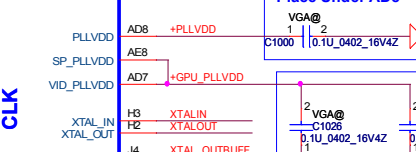
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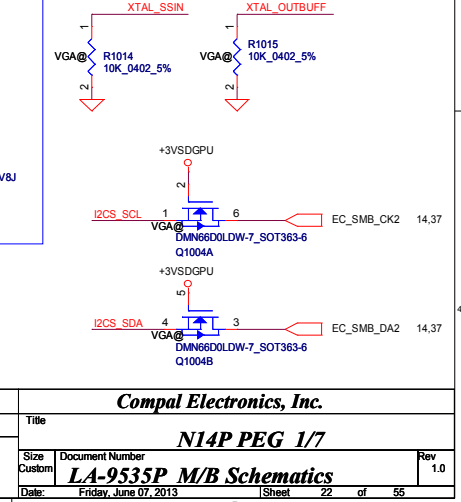
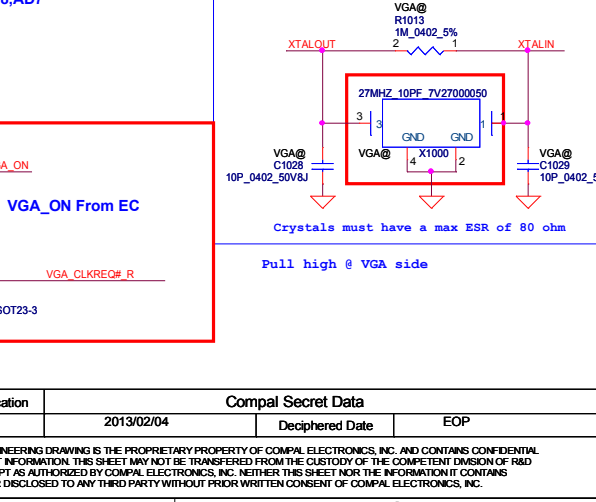
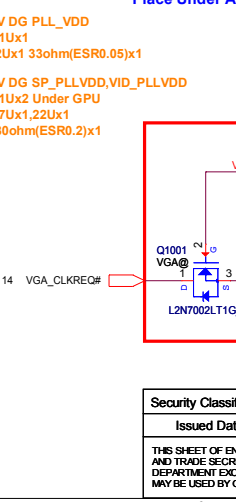
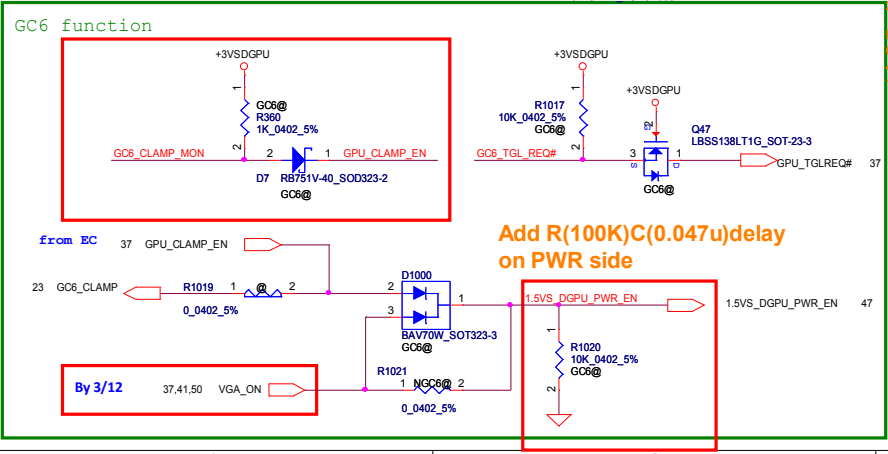
I2C



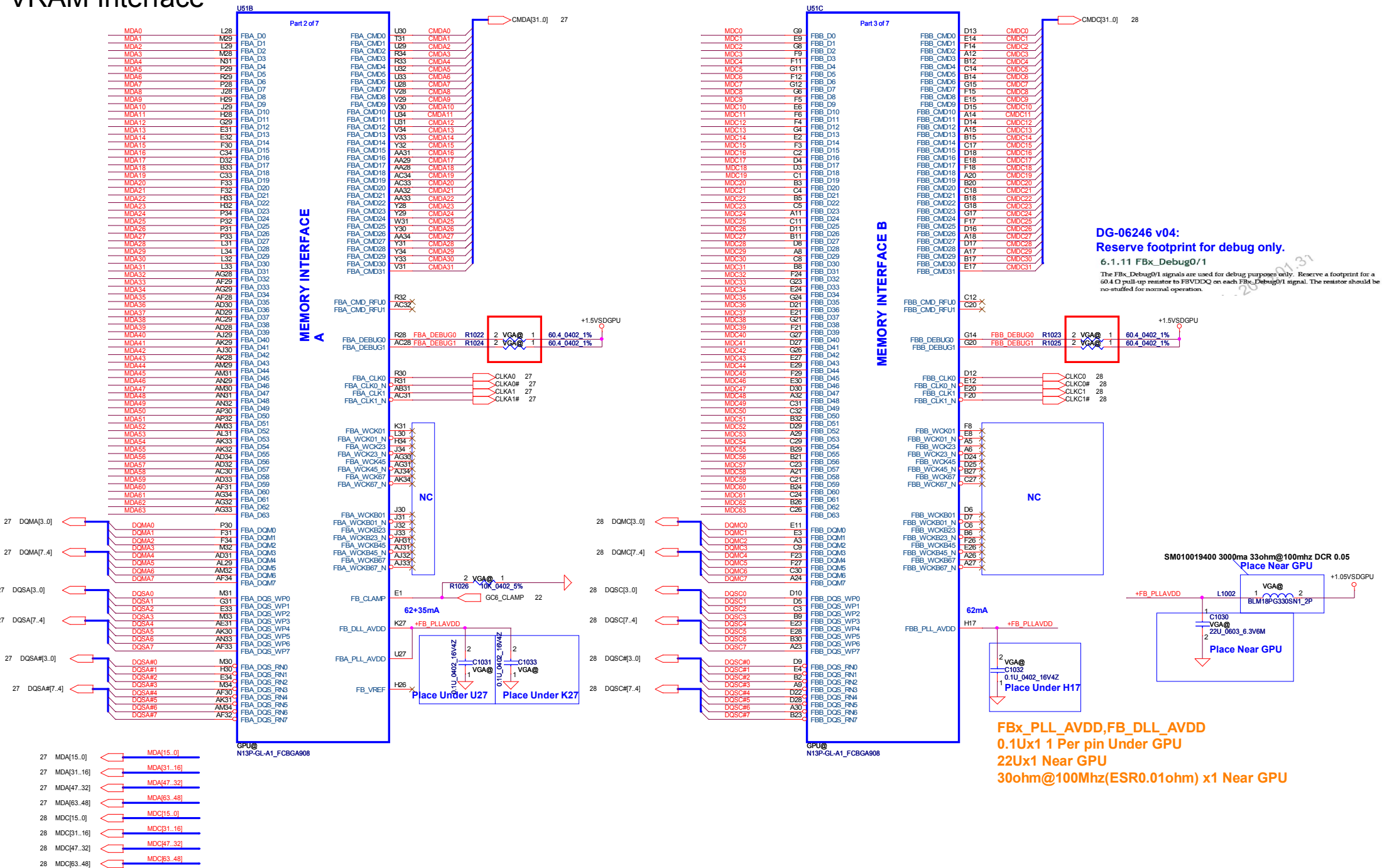
CLK



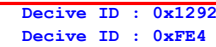
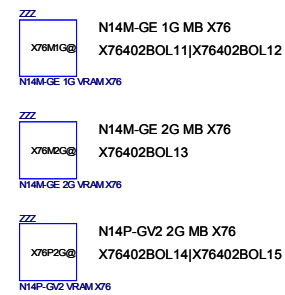
GPIO	I/O	USAGE
GPIO0	I	FB_CLAMP_MON
GPIO1	O	MEM_VD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	Reserved
GPIO6	O	FB_CLAMP_TGL_REQ
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	O	FRM_CLK
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21		Reserved
GPIO22		
GPIO23		
GPIO24		



VRAM Interface



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						Custom	LA-9535P M/B Schematics					
						Date	Friday, June 07, 2013		Sheet	23		of

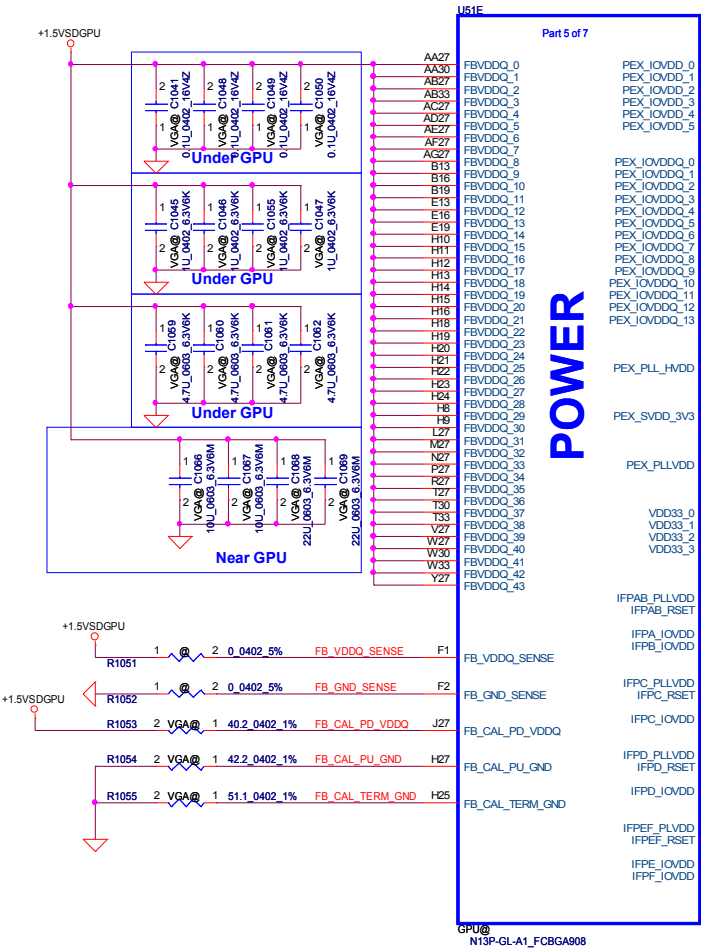
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				Size	Document Number
				Customer	LA-9535P M/B Schematics
Date	Friday, June 07, 2013	Sheet	24	of	56

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADOR	10k Ω	Pull-down to GND
ROM_SI	SUB_VEHODR	10k Ω	Pull-up to 3V3 if VHDOS ROM exists Pull-down to GND if no VHDOS-ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	So0 Hoto balow
STRAP1	RAM_CFG[1]	10k Ω	So0 Hoto balow
STRAP2	RAM_CFG[2]	10k Ω	So0 Hoto balow
STRAP3	RAM_CFG[3]	10k Ω	So0 Hoto balow
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

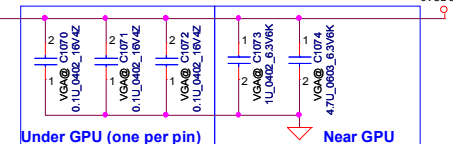
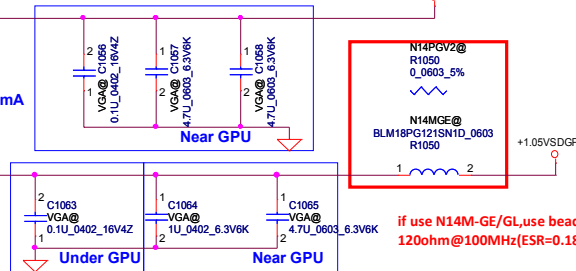
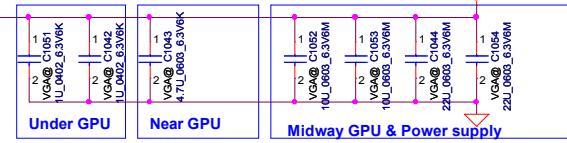
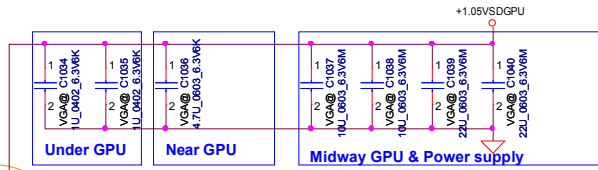
NV 14x DG FBVDDQ(DDR3) GB4-128
0.1Ux4,1Ux4,4.7Ux4 Under GPU
10Ux2,22Ux2 Near GPU

NV DG PEX_IOVVD/Q combined
1Ux4 Under GPU
4.7Ux2 Near GPU
10Ux4,22Ux4 Midway GPU & Power supply



PEX_SVDD/PLL_HVDD
connect to NV3V3
0.1Ux1,4.7Ux2 Near GPU

3300 mA
total 3300mA
Design guide page.76



NV DG PEX_PLLVDD
0.1Ux1 Under GPU
1Ux1,4.7Ux1 Near GPU

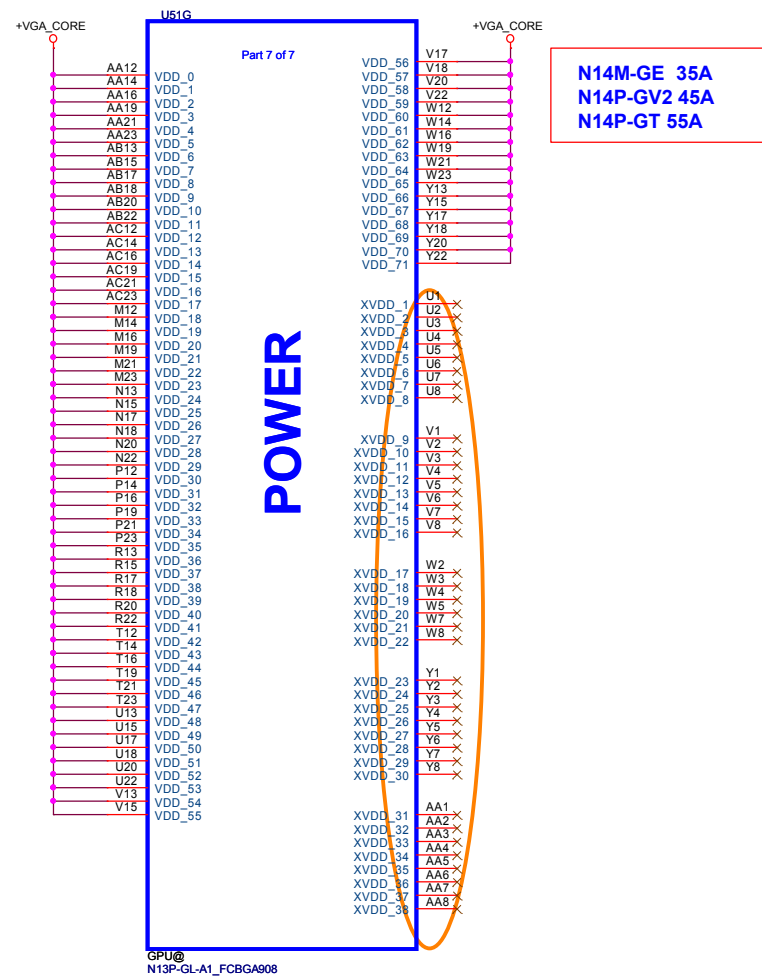
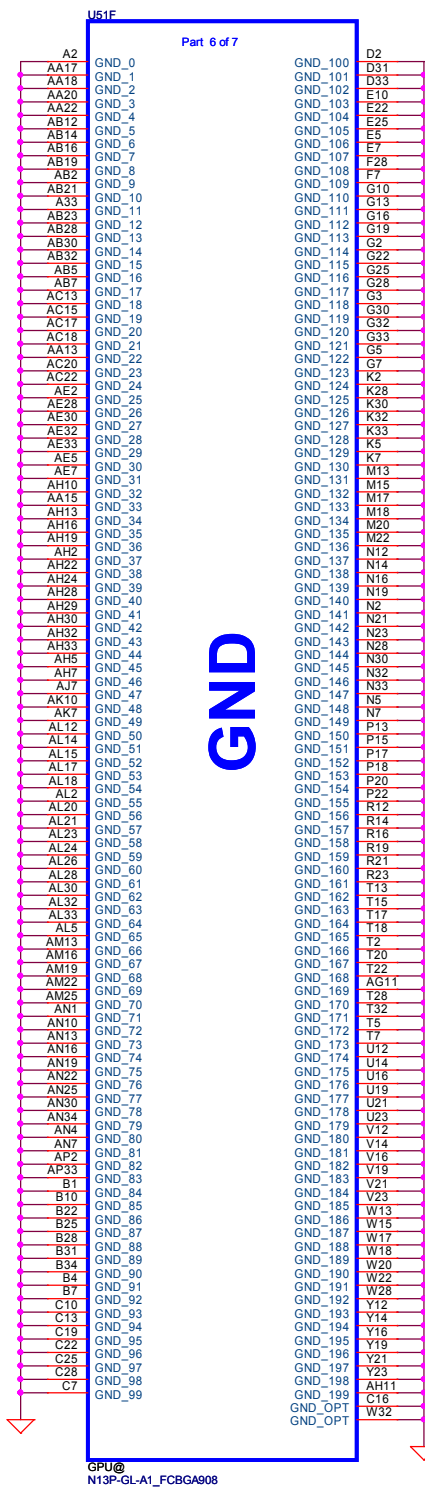
NV DG VDD33/3VSMISC
0.1Ux3 Under GPU 1Per pin
1Ux1,4.7Ux1 Near GPU

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0xB	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0xD	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4		H5TC4G63AFR-11C			

Table 7. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 256Mx16 Configuration

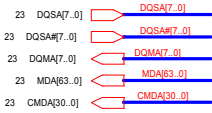
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x2	1.5V/ 1.5V	H5TC4G63AFR-11C	900	N/A	Production ready



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				Custom	LA-9535P M/B Schematics	1.0
				Date:	Friday, June 07, 2013	Sheet 26 of 55

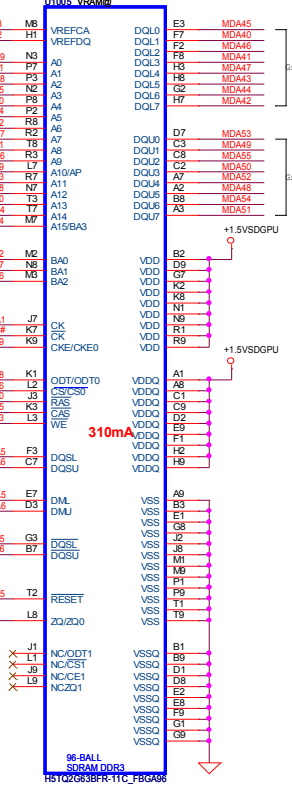
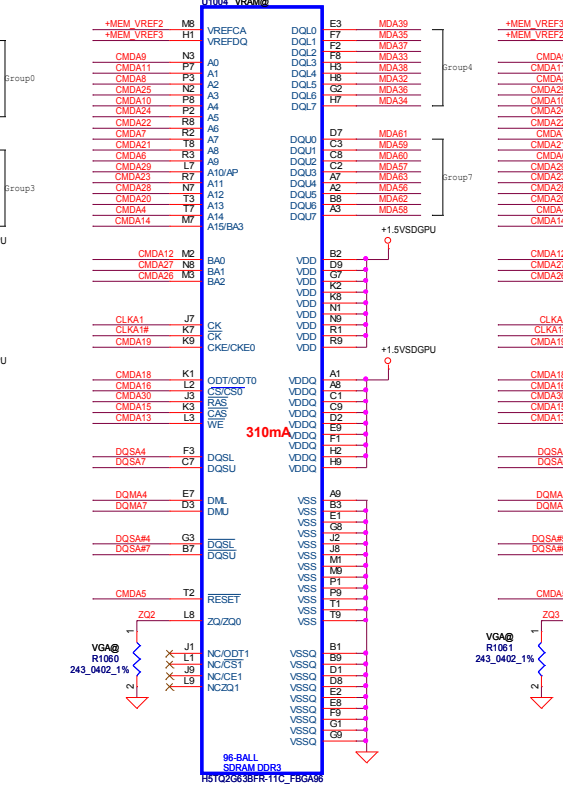
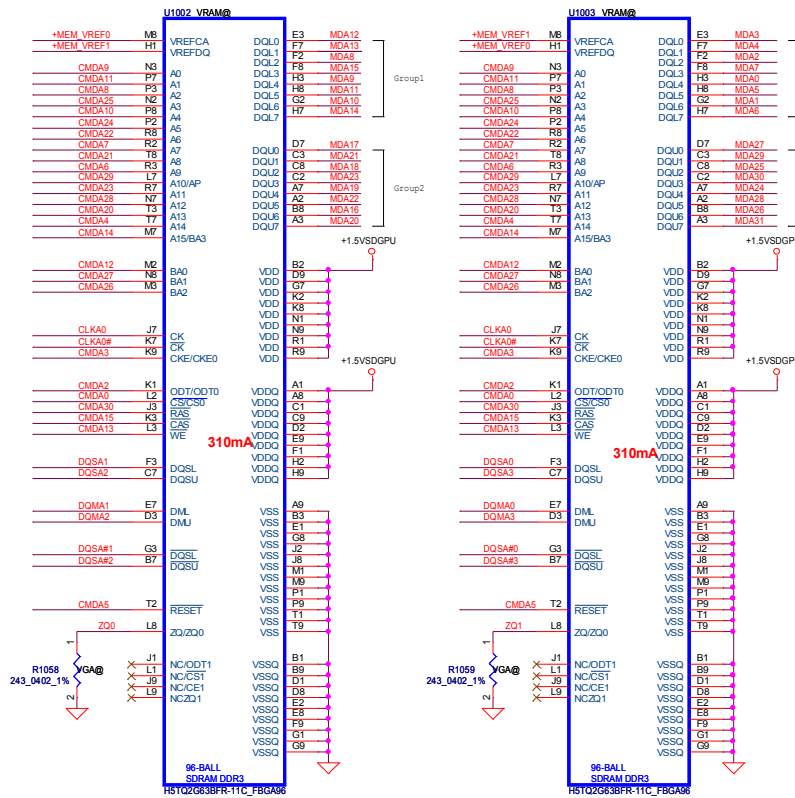
VRAM DDR3 chips

128Mx16 DDR3 *8==>2GB
256Mx16 DDR3 *8==>4GB



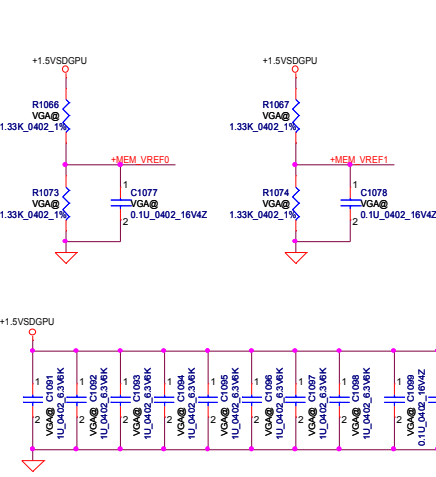
Low 32

High 32

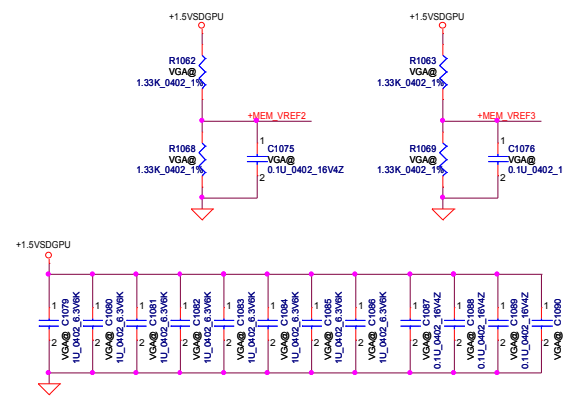


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1	ODT_L	
CMD2	CKE_L	
CMD3	A14	A14
CMD4	RST	RST
CMD5	A9	A9
CMD6	A7	A7
CMD7	A2	A2
CMD8	A0	A0
CMD9	A4	A4
CMD10	A1	A1
CMD11	BA0	BA0
CMD12	WE*	WE*
CMD13	CAS*	CAS*
CMD14	CS0_H#	
CMD15	ODT_H	
CMD16	CHE_H	
CMD17	A13	A13
CMD18	A8	A8
CMD19	A6	A6
CMD20	A11	A11
CMD21	A5	A5
CMD22	A3	A3
CMD23	BA2	BA2
CMD24	BA1	BA1
CMD25	A12	A12
CMD26	A10	A10
CMD27	RAS*	RAS*
CMD28		
CMD29		
CMD30		

LOW HIGH

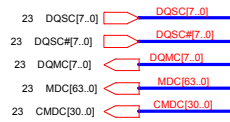


Command Bit	Default Pull-down
ODT#	10k
CKE#	10k
RST	10k
CS*	No Termination



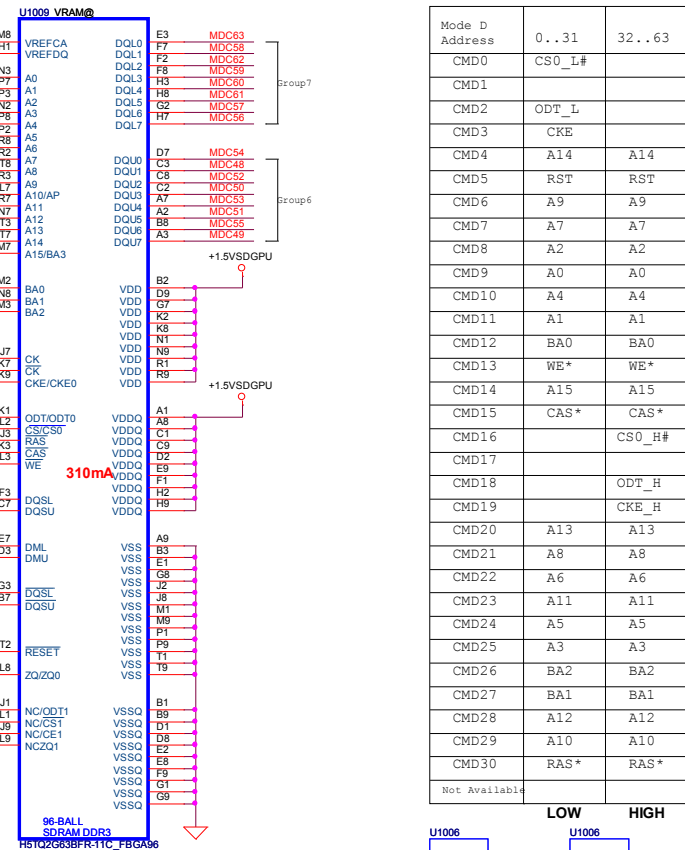
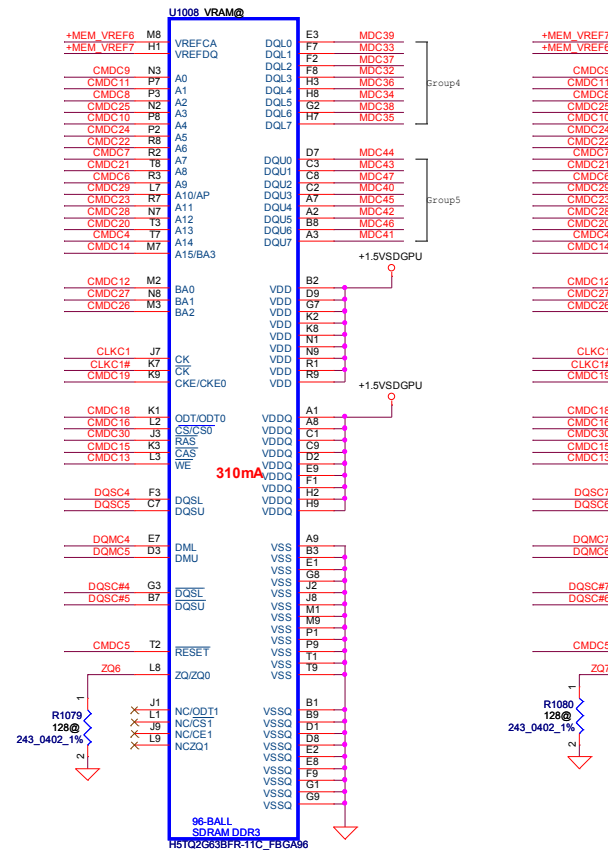
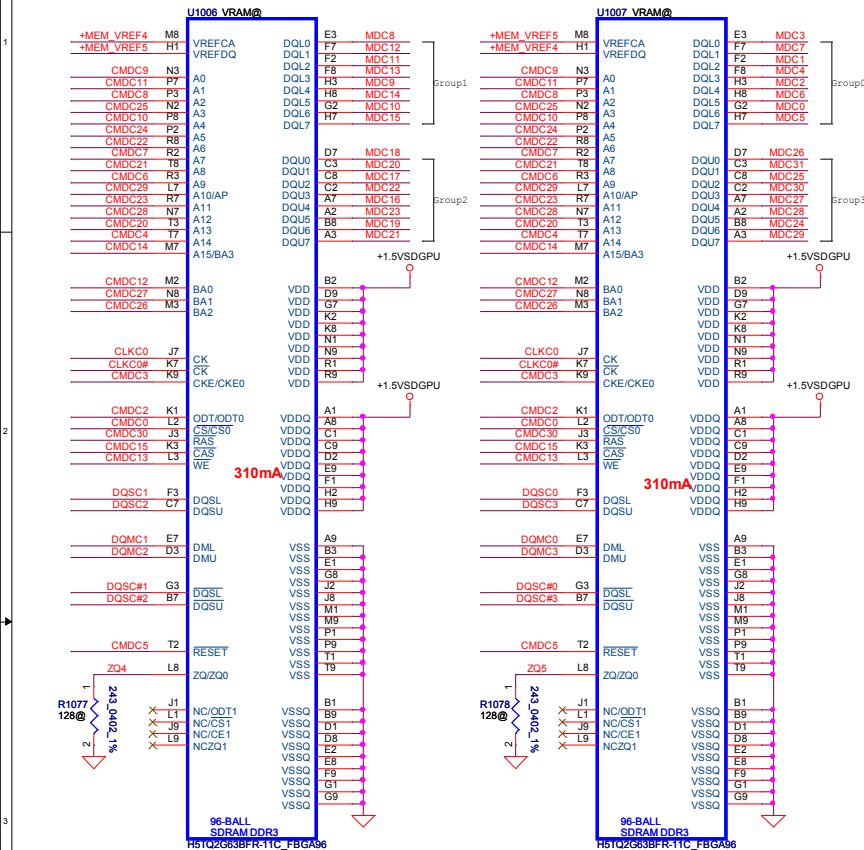
VRAM DDR3 chips

128Mx16 DDR3 *8==>2GB
256Mx16 DDR3 *8==>4GB



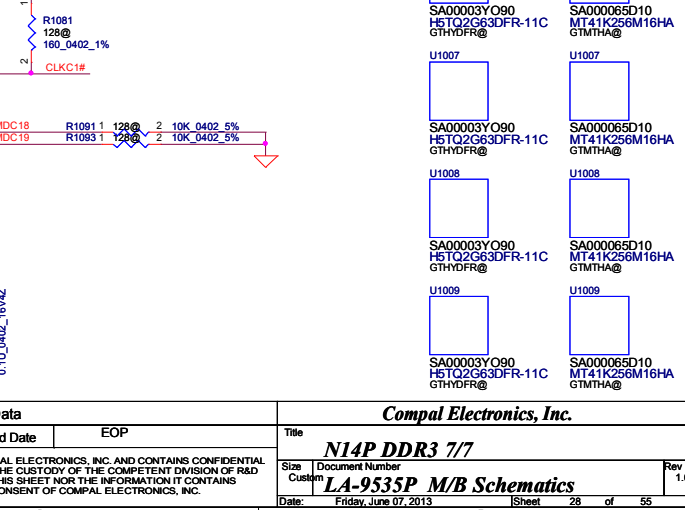
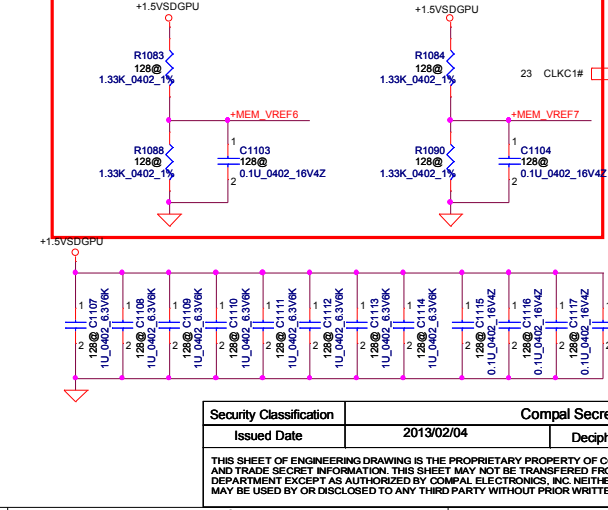
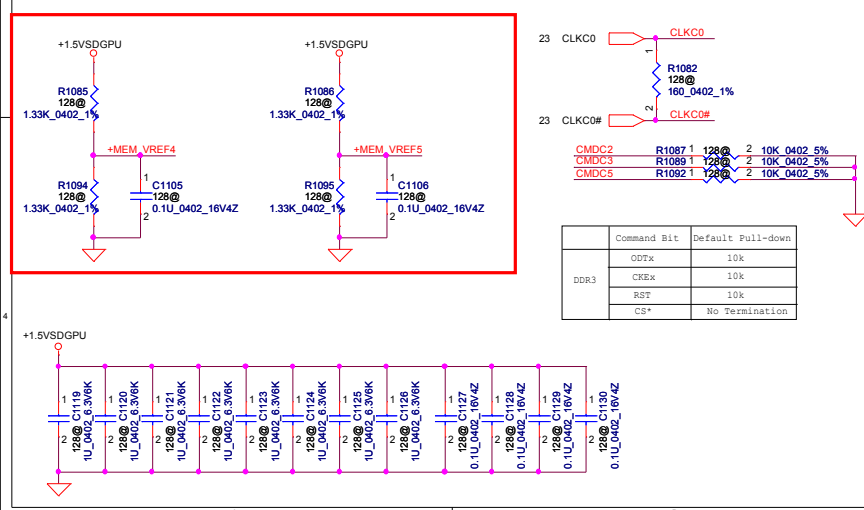
Low 32

High 32

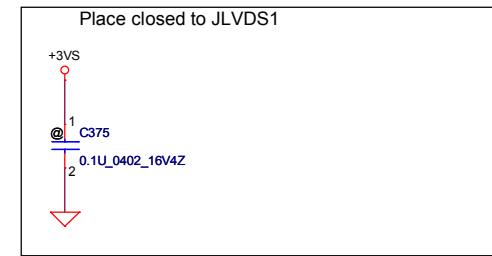
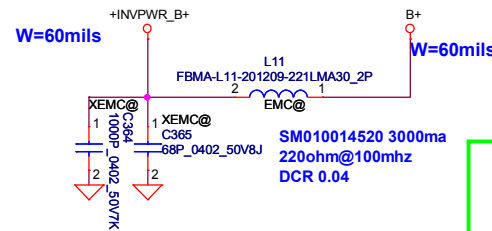
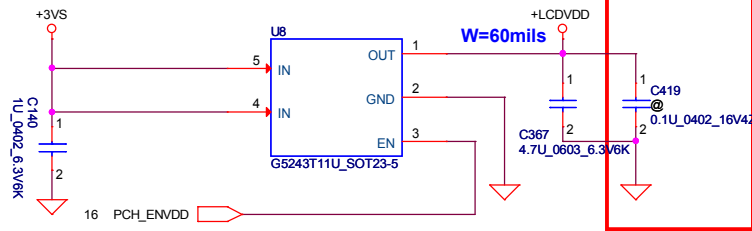


Mode D	Address	0..31	32..63
CMD0	CS0_L#		
CMD1			
CMD2	ODT_L		
CMD3	CKE		
CMD4	A14	A14	
CMD5	RST	RST	
CMD6	A9	A9	
CMD7	A7	A7	
CMD8	A2	A2	
CMD9	A0	A0	
CMD10	A4	A4	
CMD11	A1	A1	
CMD12	BA0	BA0	
CMD13	WE*	WE*	
CMD14	A15	A15	
CMD15	CAS*	CAS*	
CMD16		CS0_H#	
CMD17			
CMD18	ODT_H		
CMD19	CKE_H		
CMD20	A13	A13	
CMD21	A8	A8	
CMD22	A6	A6	
CMD23	A11	A11	
CMD24	A5	A5	
CMD25	A3	A3	
CMD26	BA2	BA2	
CMD27	BA1	BA1	
CMD28	A12	A12	
CMD29	A10	A10	
CMD30	RAS*	RAS*	
Not Available			

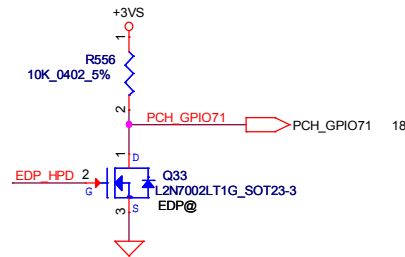
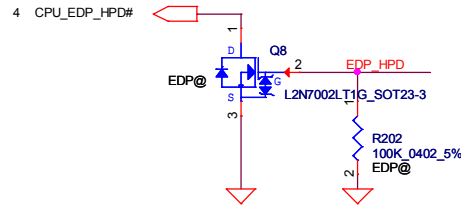
LOW HIGH



LCD POWER CIRCUIT

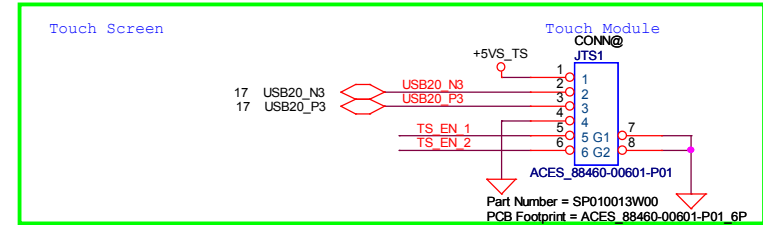
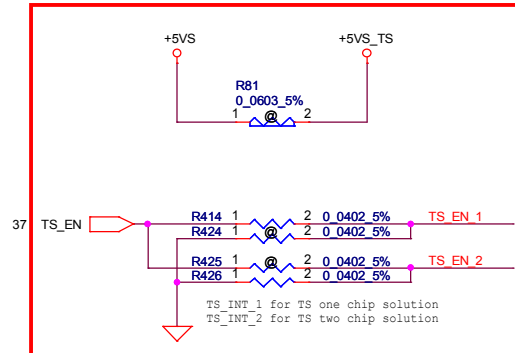
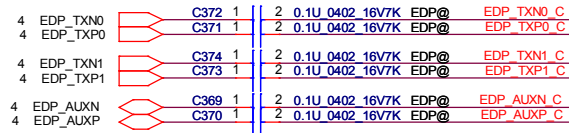


HPD

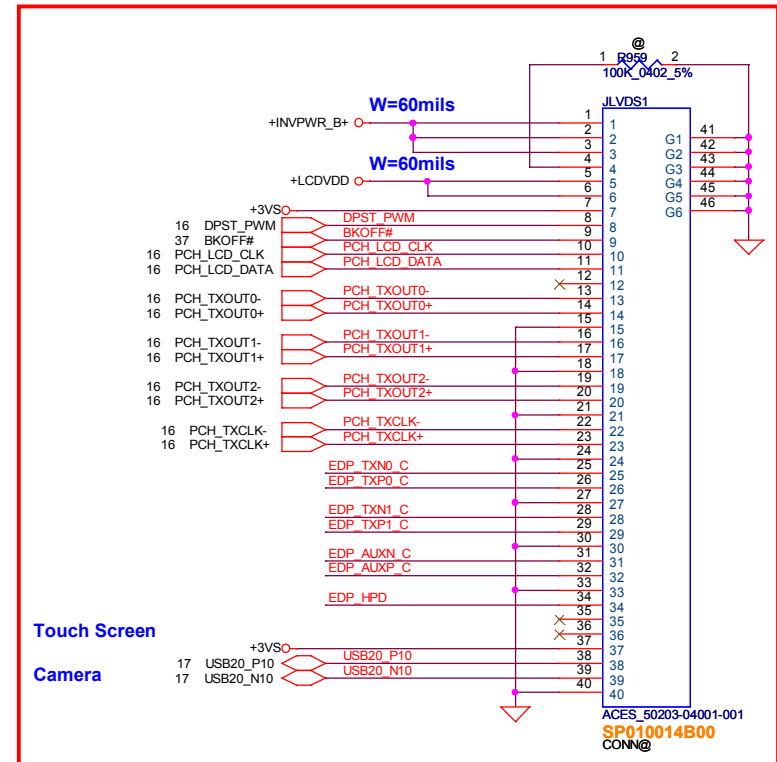


	GPIO71
	PCH_GPIO71
eDP	0
LVDS	1

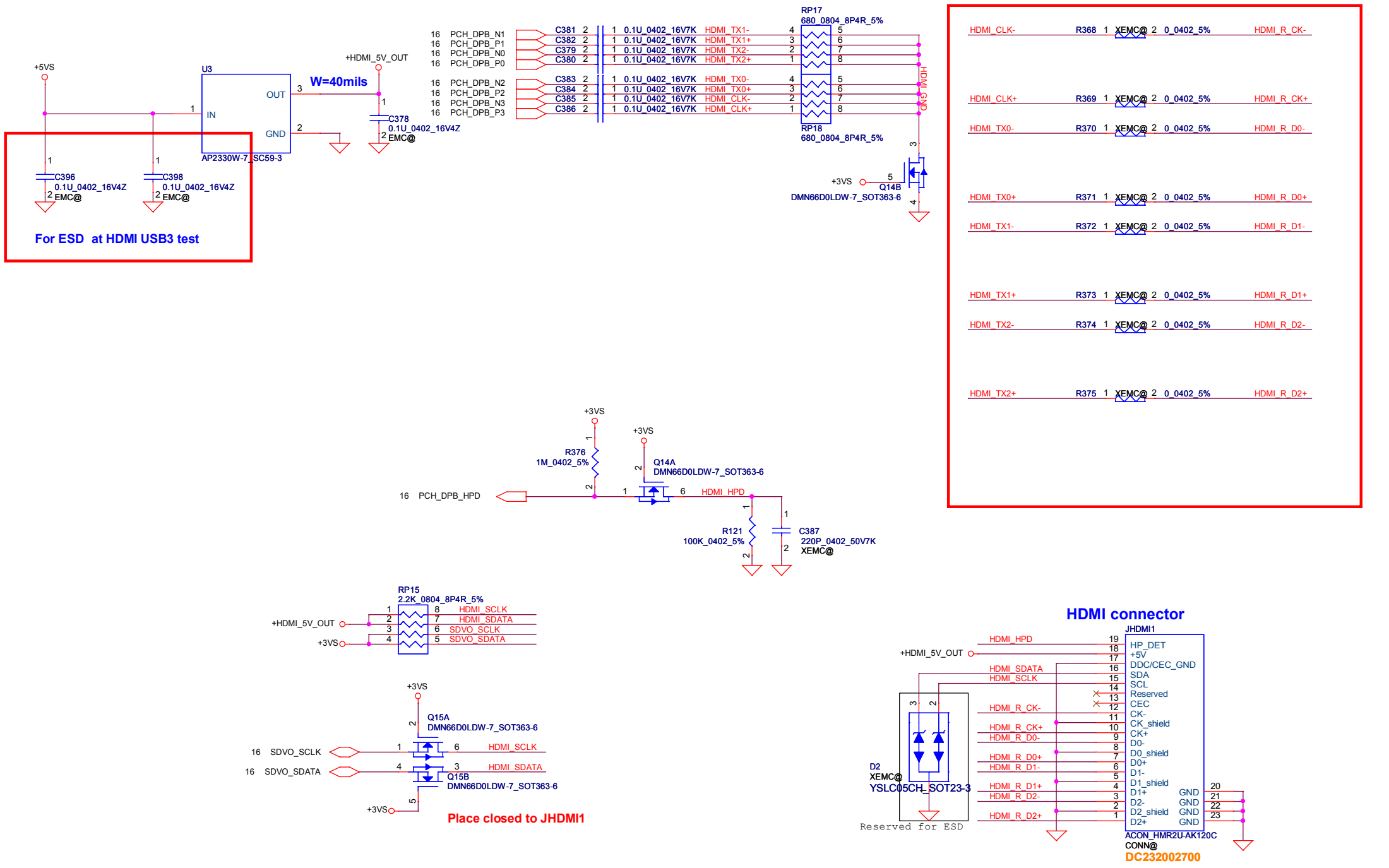
eDP



LCD/LED PANEL Conn.

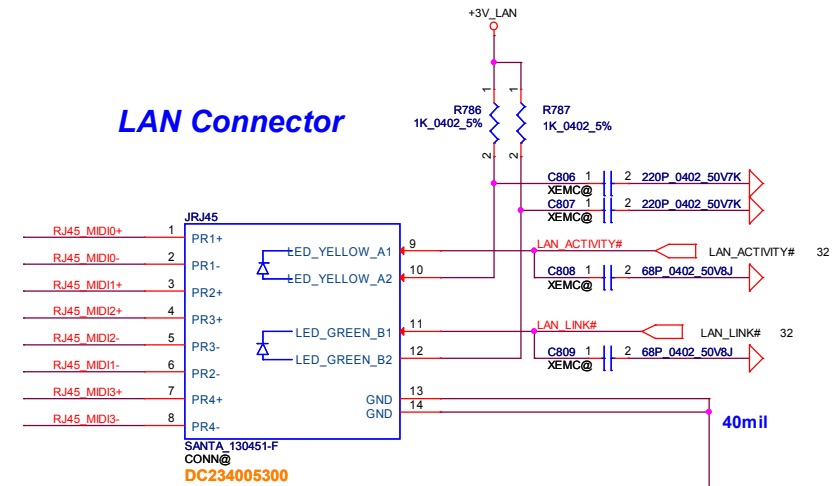
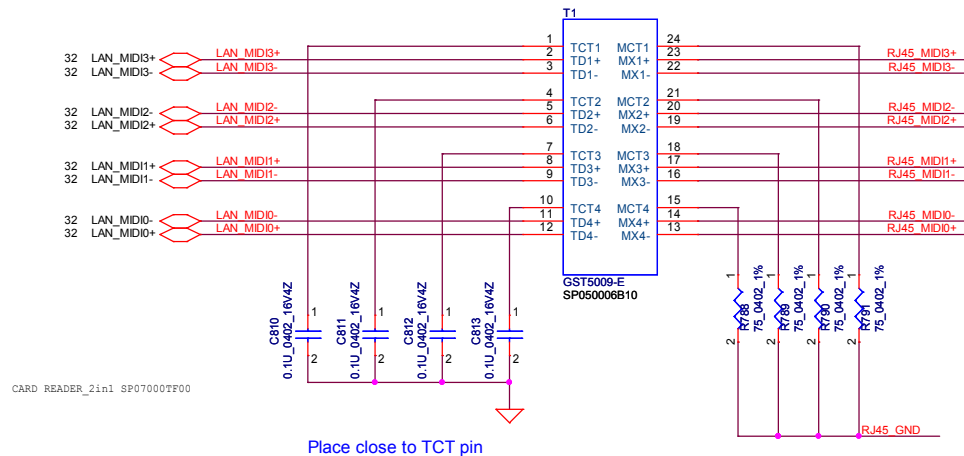


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				Date	Friday, June 07, 2013
				Sheet	29 of 55

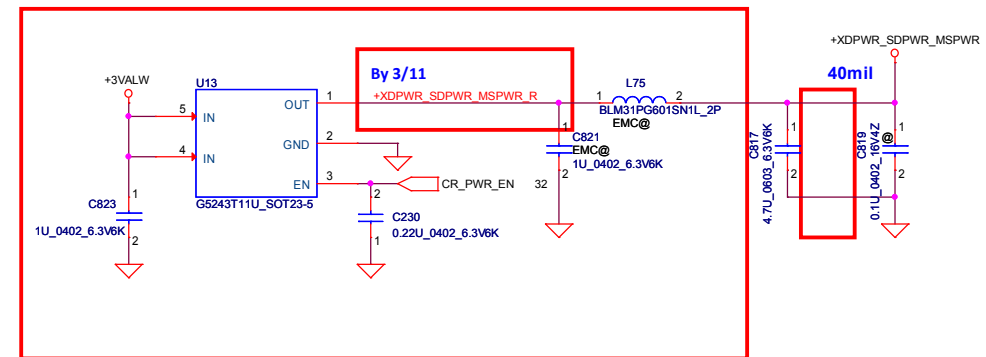
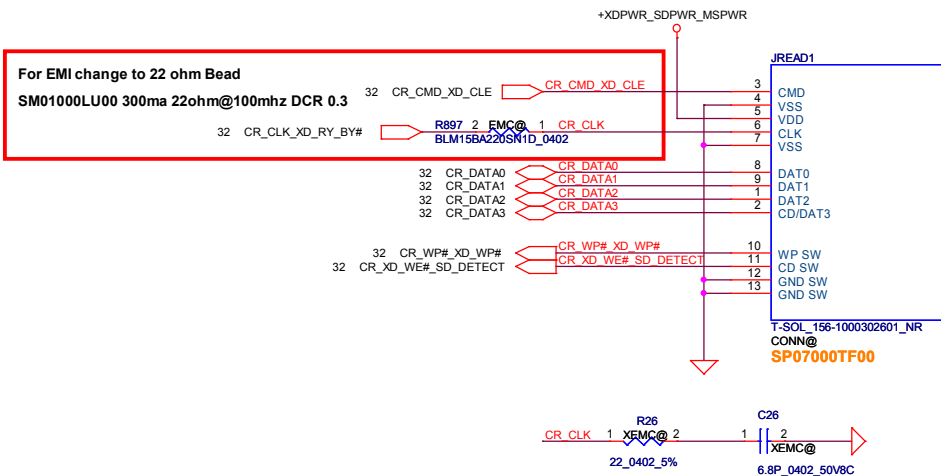


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						HDMI Conn		Rev
						Size Document Number		1.0
						Custom LA-9535P M/B Schematics		
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Card Reader Connector



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				Sheet	33 of 55

60mil

J3

JUMP_43X118

3V3S

3V3S_WLAN

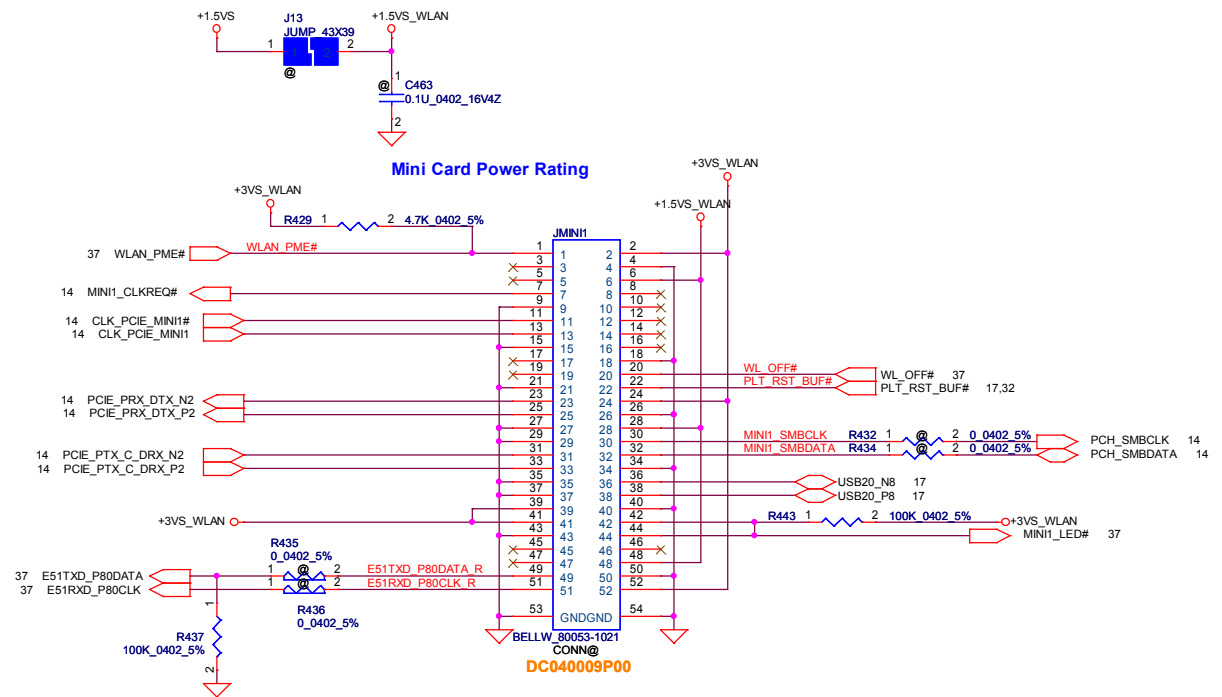
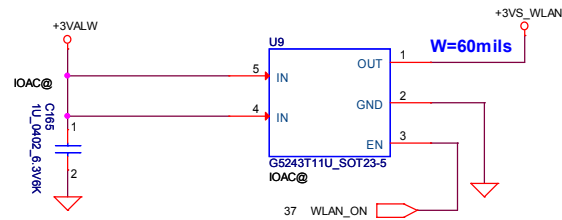
C441 470P_0402_50V7K EMC@

C458 4.7U_0603_6.3V6K

C459 0.1U_0402_16V4Z

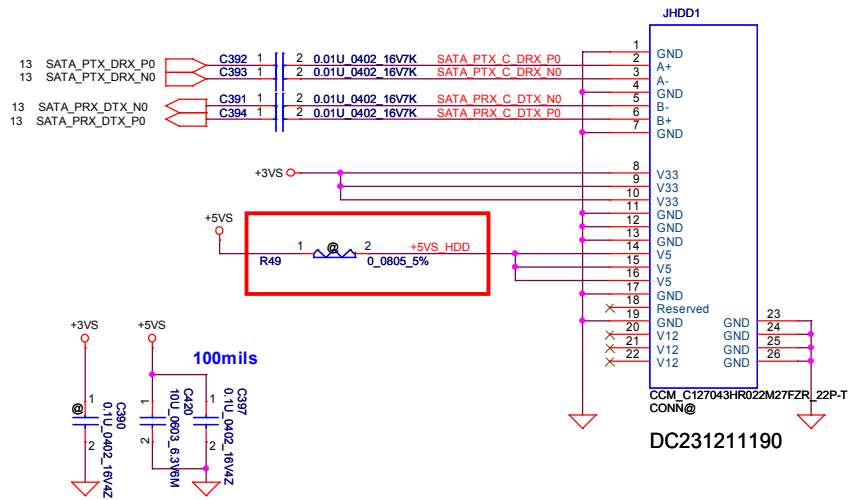
C460 0.1U_0402_16V4Z

Add 3/12

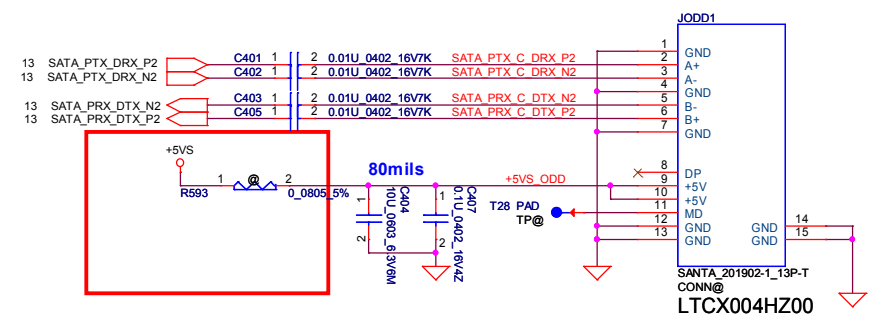


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				Date:	Friday, June 07, 2013	Sheet 34 of 55

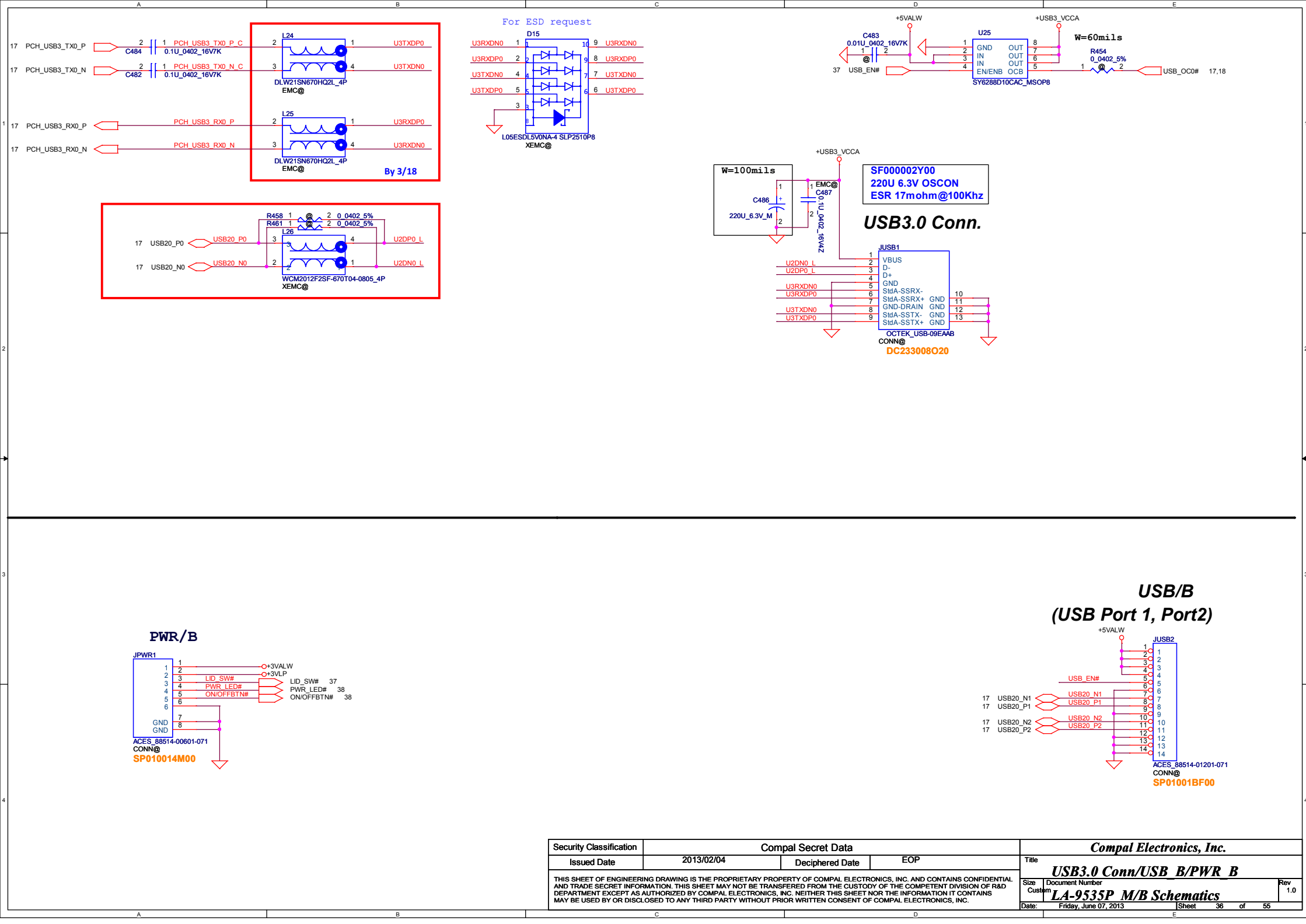
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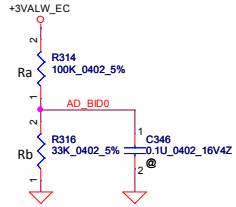
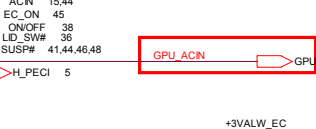
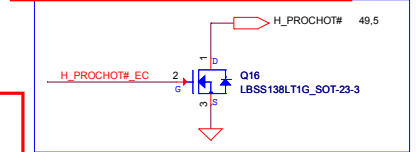
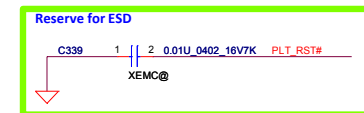


SATA ODD Conn.



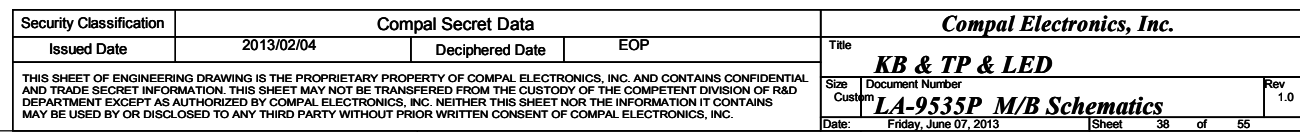
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Date:	Friday, June 07, 2013	Sheet	35	of	55



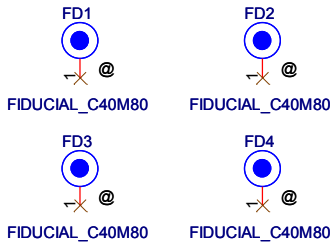
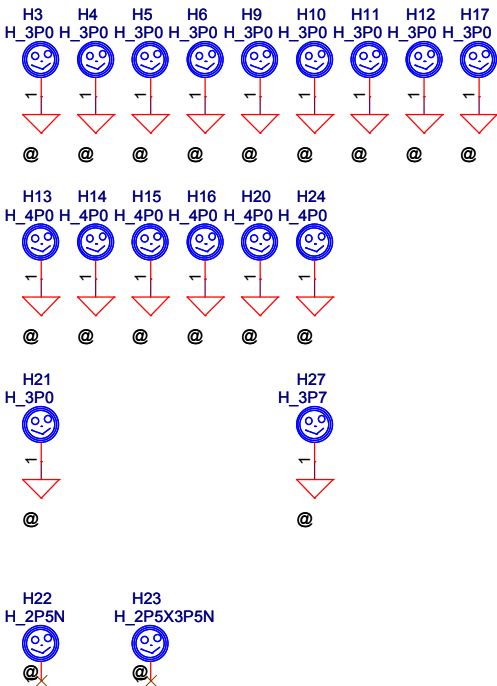
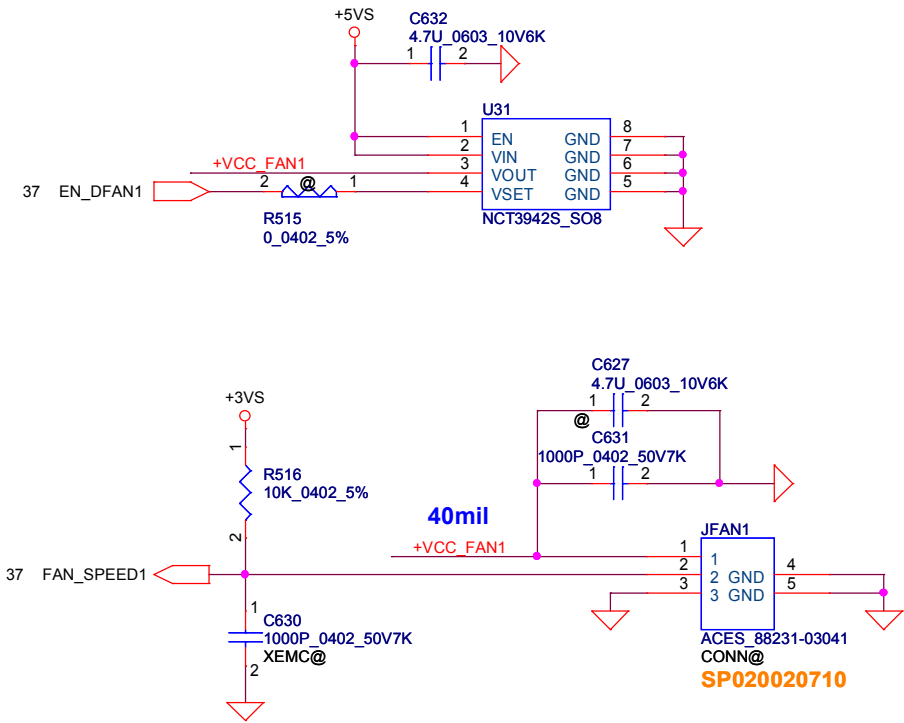


Phase	Revision	BID0	BID1
EVT	0.1	0	X
* PVT	0.2	1	X
PVT2	0.3	2	X
MP	1.0	3	X

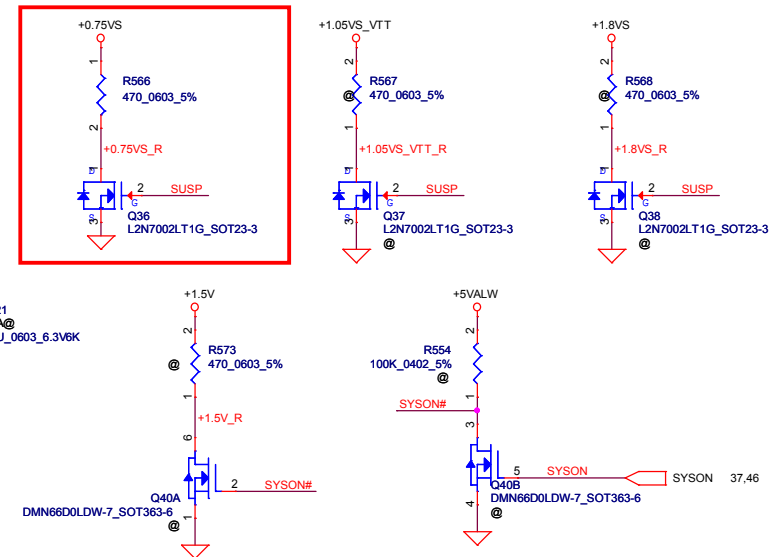
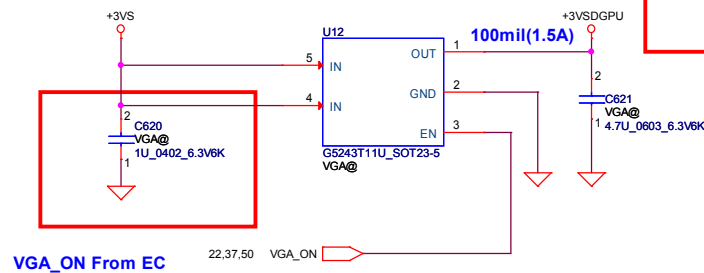
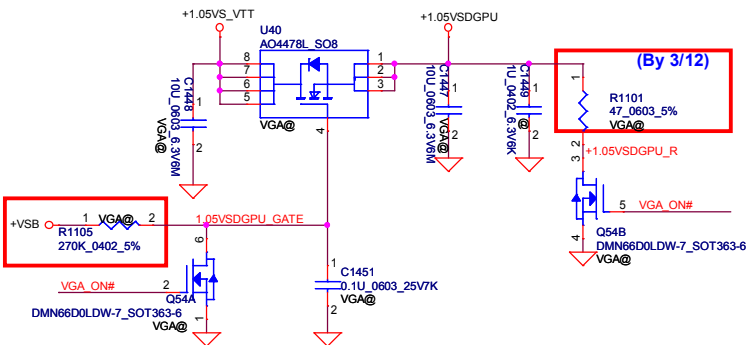
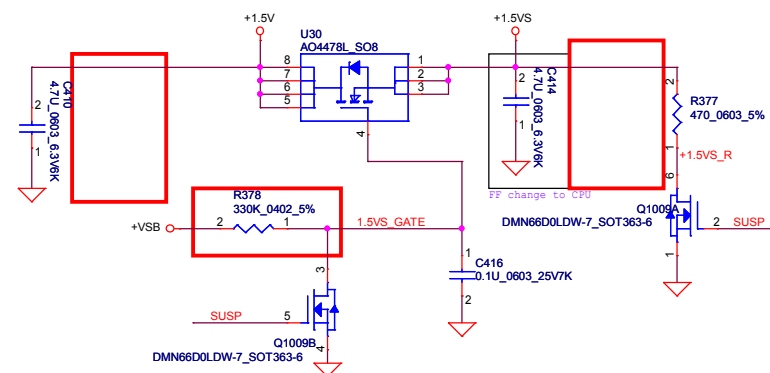
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				Date:	Friday, June 07, 2013	Sheet	37 of 55



FAN1 Conn

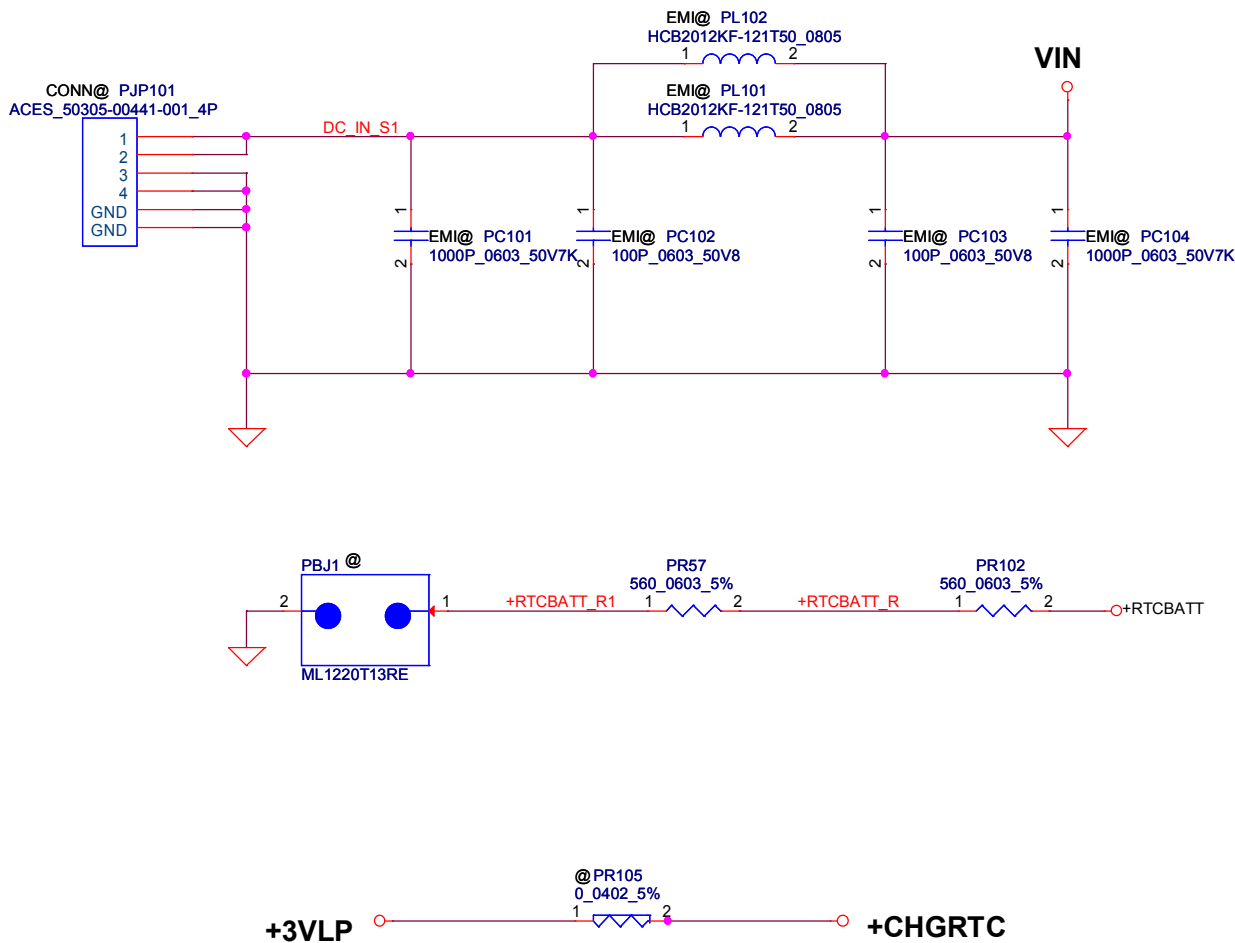


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								Date:	Friday, June 07, 2013	Sheet

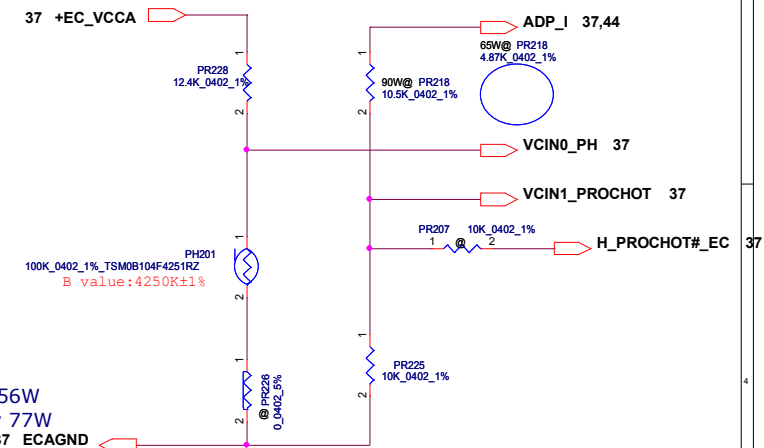
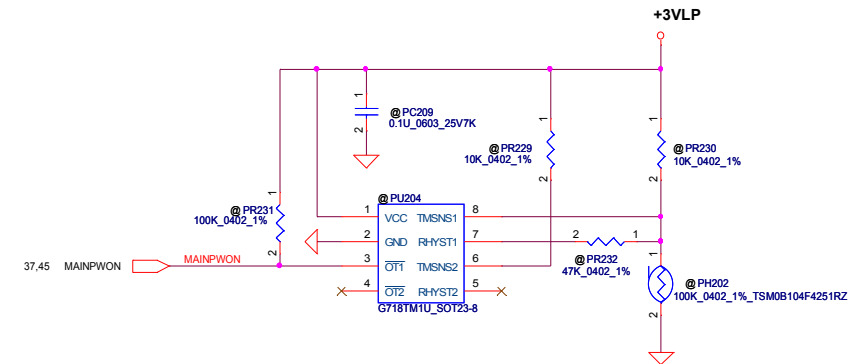


The schematic diagram illustrates the VGA input circuit for the L2N7002LT1G_SOT23-3 component. A 5V power supply (+5VALW) is connected to a 100K_0402_5% resistor (R560), which is connected to the VGA+ input. A 100K_0402_5% resistor (R561) is connected between the VGA- input and ground. The VGA input is connected to the L2N7002LT1G_SOT23-3 component.

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				Date: Friday, June 07, 2013	Rev 1.0
				Sheet 42	of 55



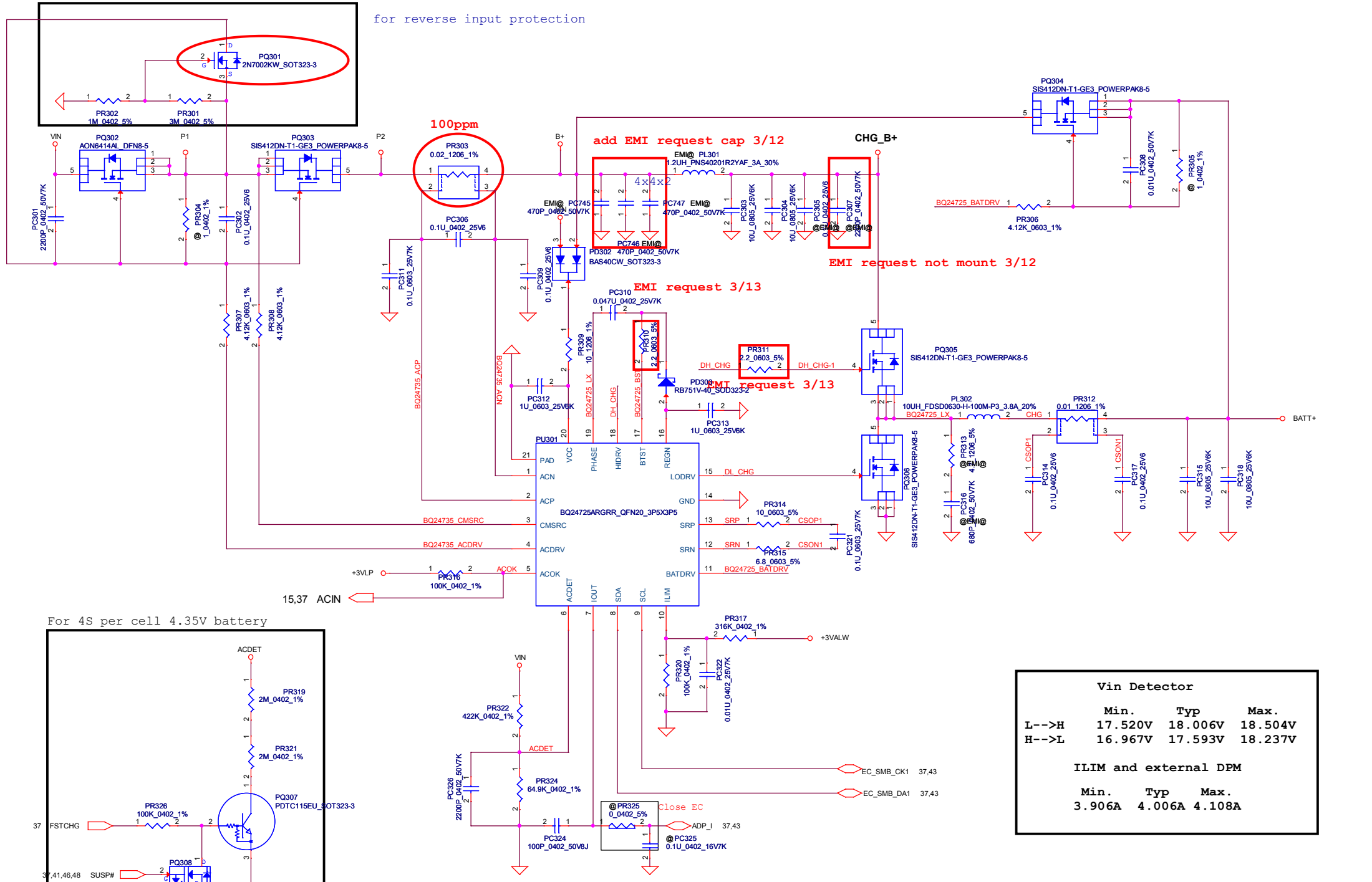
For KB9012 OTP	
92°C	1.2V, Active
56°C	2.255V, Recovery

For KB9012 sense 20mΩ	Active	Recovery
65W	84W, 1.2V	56W, 0.793V
90W	117W, 1.2V	77W, 0.791V
120W		

```
PH201 under CPU botten side :
CPU thermal protection at 92 degree C ( shutdown )
Recovery at 56 degree C
```

For 65W adapter==>action 84W , Recovery 56W
For 90W adapter==>action 117W , Recovery 77W

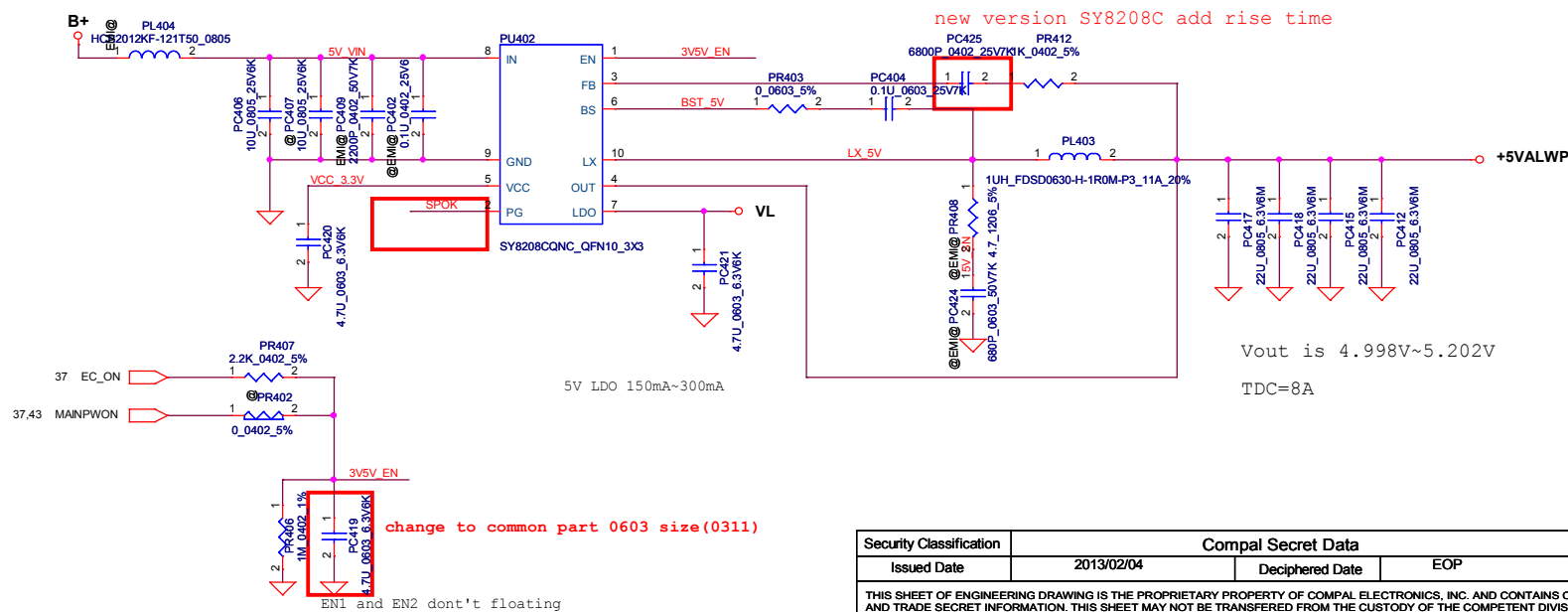
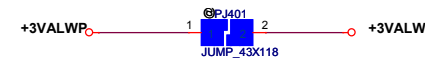
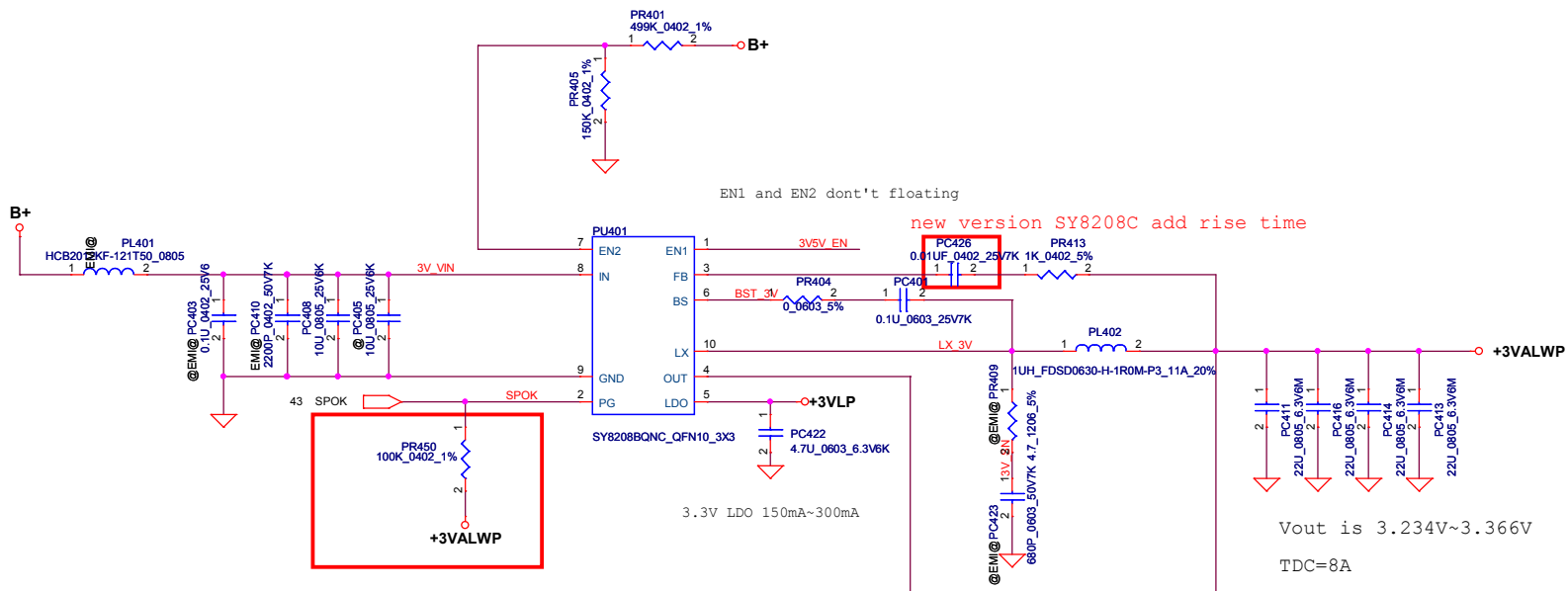
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				Custn	LA-9535P M/B Schematics	1.0
				Date:	Friday, June 07, 2013	Sheet 43 of 55



Vin Detector			
	Min.	Typ	Max.
L-->H	17.520V	18.006V	18.504V
H-->L	16.967V	17.593V	18.237V

ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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				Date	Friday, June 07, 2013
				Sheet	44 of 55



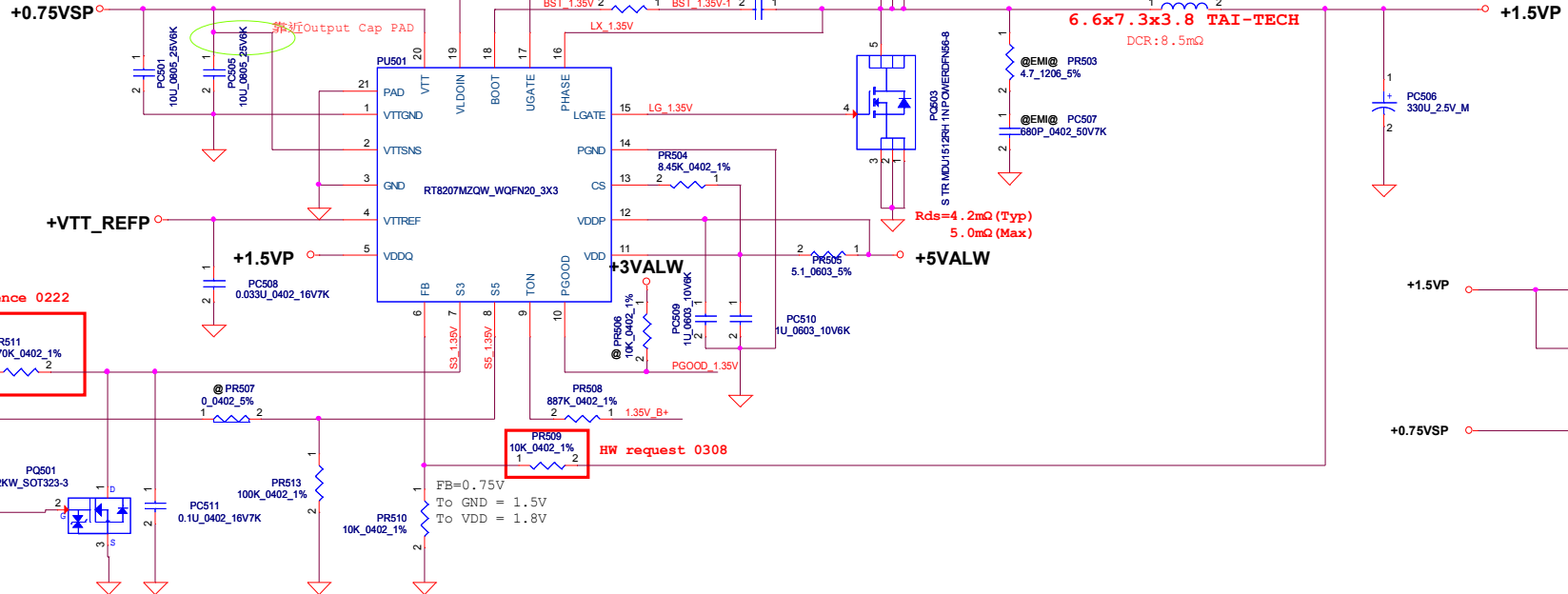
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								Document Number		Rev 1.0	
								LA-9535P M/B Schematics			
								Date: Friday, June 07, 2013		Sheet 45 of 55	

```

+1.35VP
Ipeak = max{ 0.7*Ibudget, 1st +2nd max loading}
Ipeak = max{ 12.34*0.7 , 4.2+8.14 }
Ipeak=12.34A ; 1.2Ipeak=14.808A ;Imax=8.638A
1/2Delta I=0.7353A (F=300K Hz)
PR504=(1.2Ipeak-1/2Delta I) *Rds(on) (max) *1.2/9uA=8.45Kohm
choose PR504=8.45Kohm (for safety >1.2Ipeak)
Rds(on)=5.0m ohm(max) ; Rds(on)=4.2m ohm(typical)
Ilimit_min=(8.366K*9uA) / (5.0m*1.2)=15.058A
Ilimit_max=(8.535K*11uA) / (4.2m*1.2)=22.352A
Iocp=Ilimit+1/2Delta I=15.79A~23.09A
Iocp(min)>1.2Ipeak
  
```

2012/9/6

OVP=110% 115% 120%



37,41,44,48 SUSP#
37,41 SYSON
41 SUSP

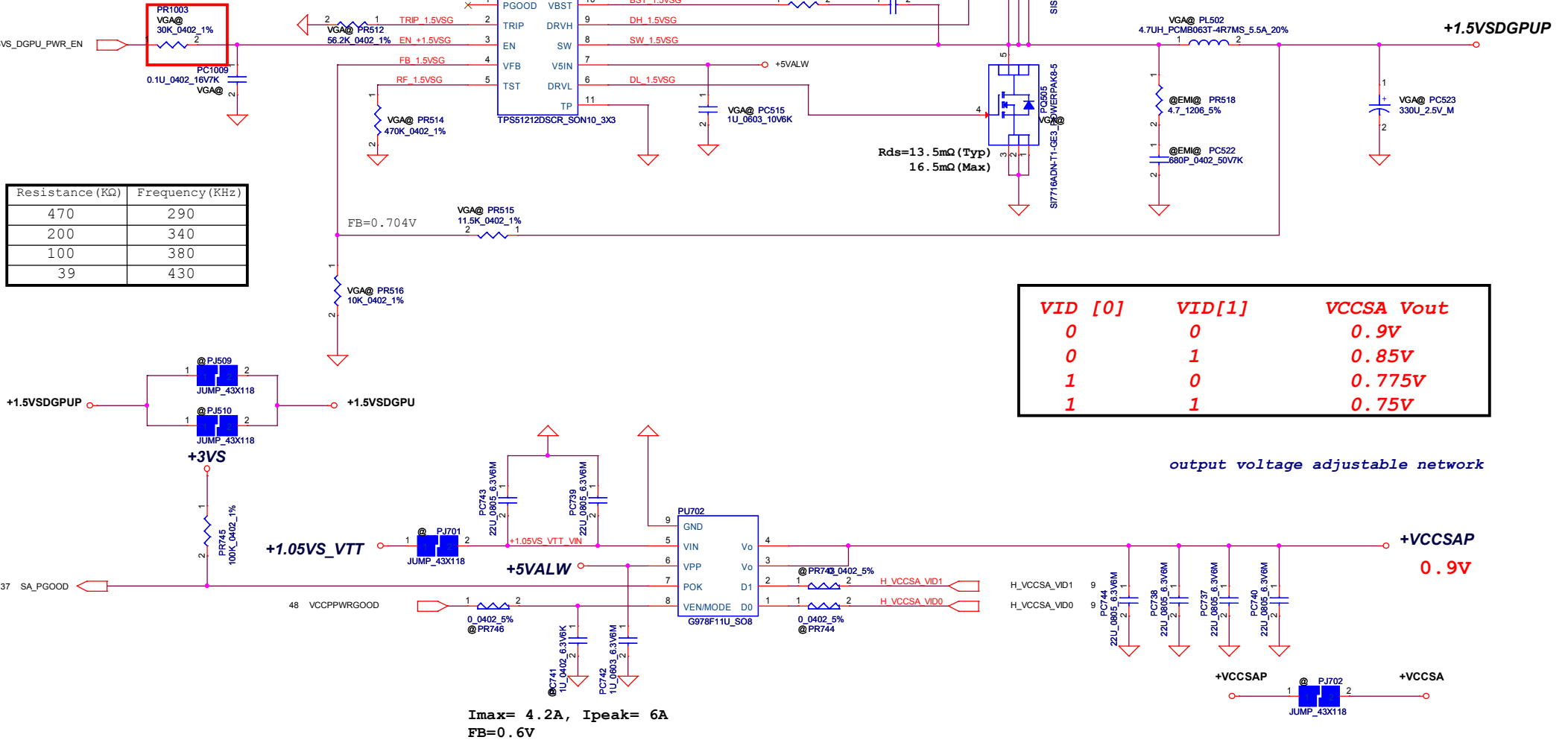
STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

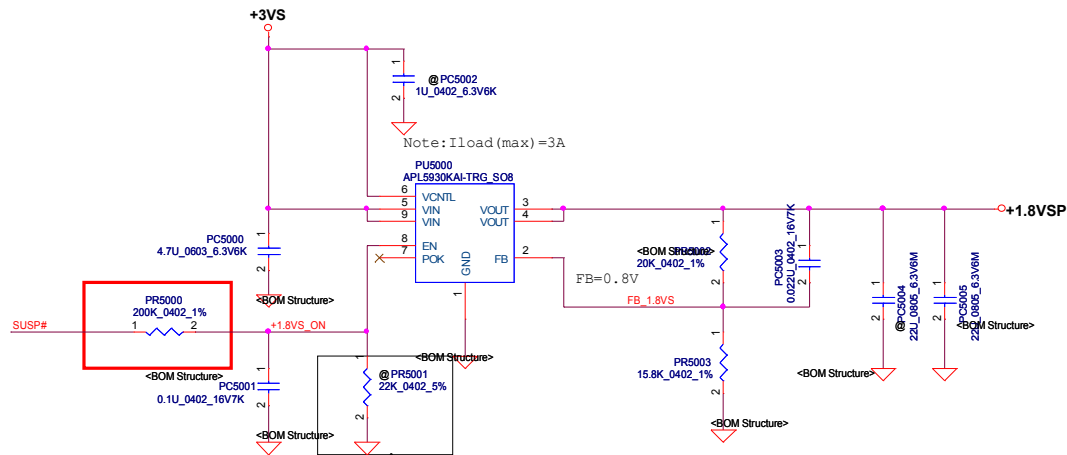
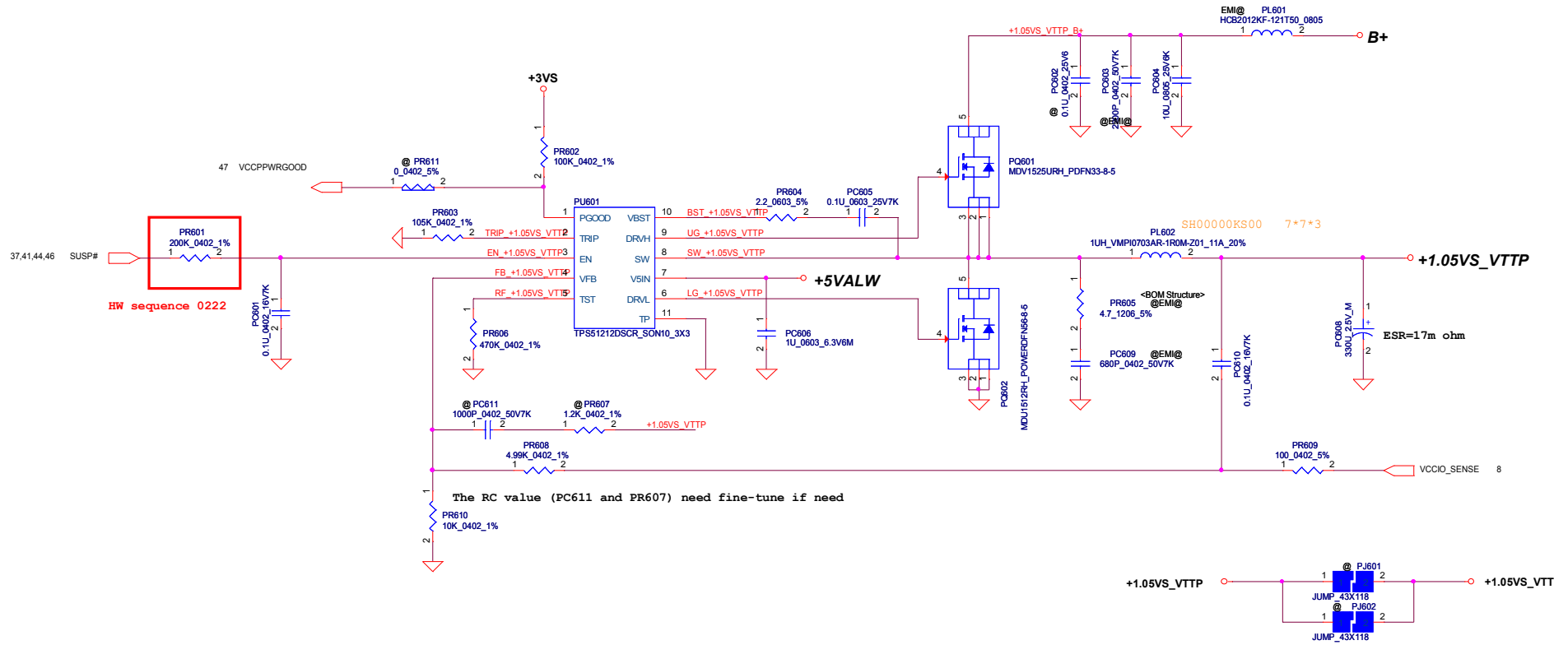
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2013/02/04				Title			
Deciphered Date				EOP				1.5VP/0.75VSP			
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				Date				Friday, June 07, 2013			
				Sheet				46 of 55			
				Rev				1.0			

$V_{FB} = 0.704V$
 $V_o = V_{FB} * (1 + 11.5K/10K) = 1.5V$
 $Freq = 290KHz (typ)$
 $C_{esr} = 15m\ ohm$
 $I_{peak} = 4.7A$ $I_{max} = 3.29A$ $I_{ocp} = 5.64A$
 $I_{ocp} = 5.72A \sim 6.43A$

HW sequence (0311)



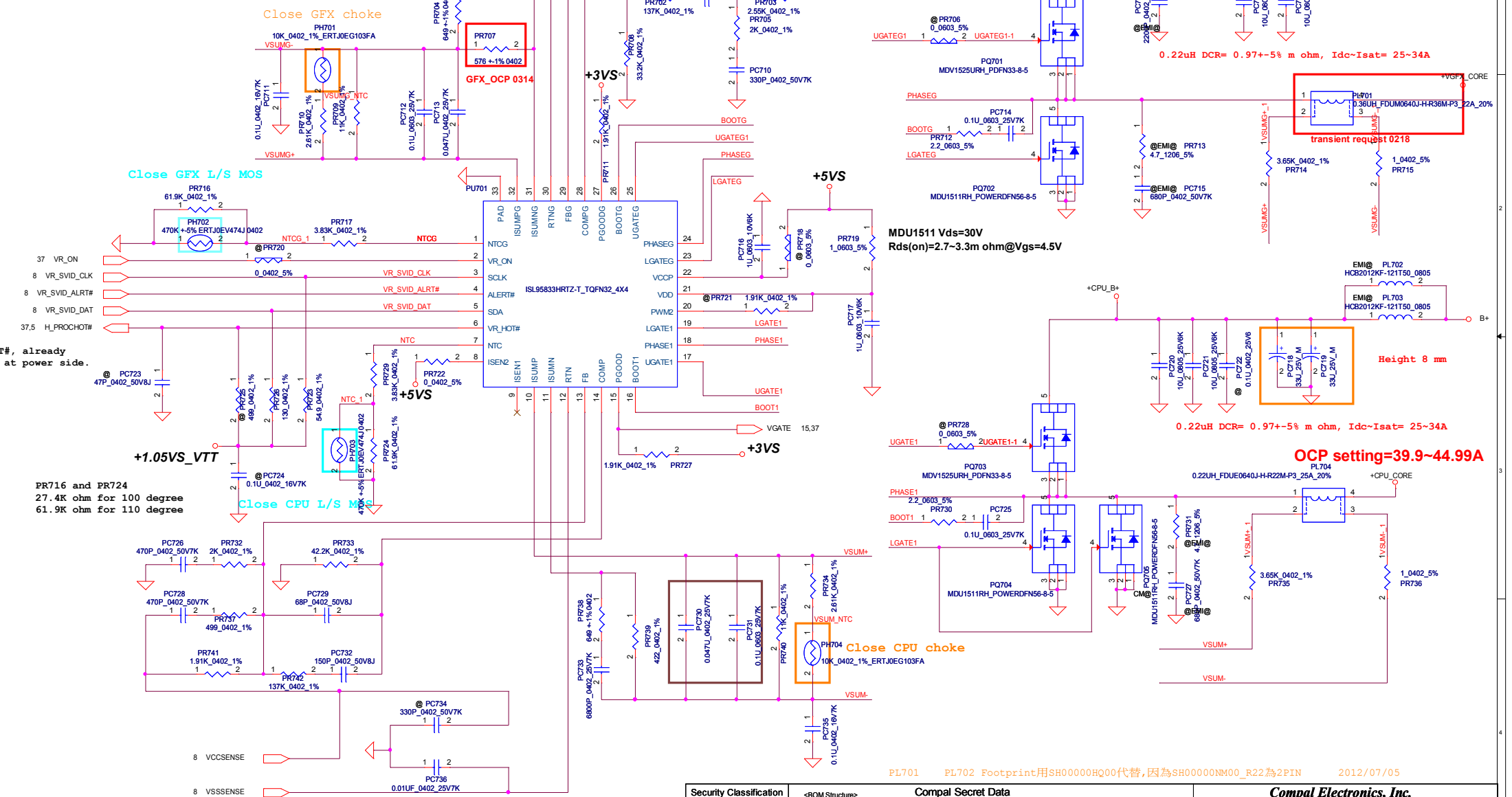
+1.05VSP Ipeak=5.36A ; Imax=3.752A ; 1.2Ipeak=6.432
Delta I=0.xxxxA=>1/2Delta I=0.xxxxA,F= 800K Hz(typ)



Ien=10uA, Vth=0.3V, notice the res. and pull high voltage from HW

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				Custn	LA-9535P M/B Schematics
				Date:	Friday, June 07, 2013
				Sheet	48 of 55

Layout Note
SVID routing
1. Alert# signal must be routed between the Clock and Data lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Data
2. SVID spacing requirement is 18mils(0.475mm).
3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
4. The SVID bus must be ground reference. It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.



Layout Note
Reduce Acoustic Noise
1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
2. Input ceramic caps must place on symmetry same location on top side and bottom side.

VDD source use +5VS and PGOOD source use +3VS
Please confirm power on and down sequence,
make sure VGATE after CPU_CORE on.

OCP setting=39.9~44.99A

0.22uH DCR= 0.97+-5% m ohm, Idc~Isat= 25~34A

MDU1511 Vds=30V
Rds(on)=2.7~3.3m ohm@Vgs=4.5V

0.22uH DCR= 0.97+-5% m ohm, Idc~Isat= 25~34A

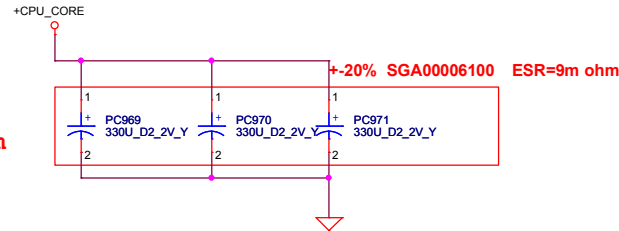
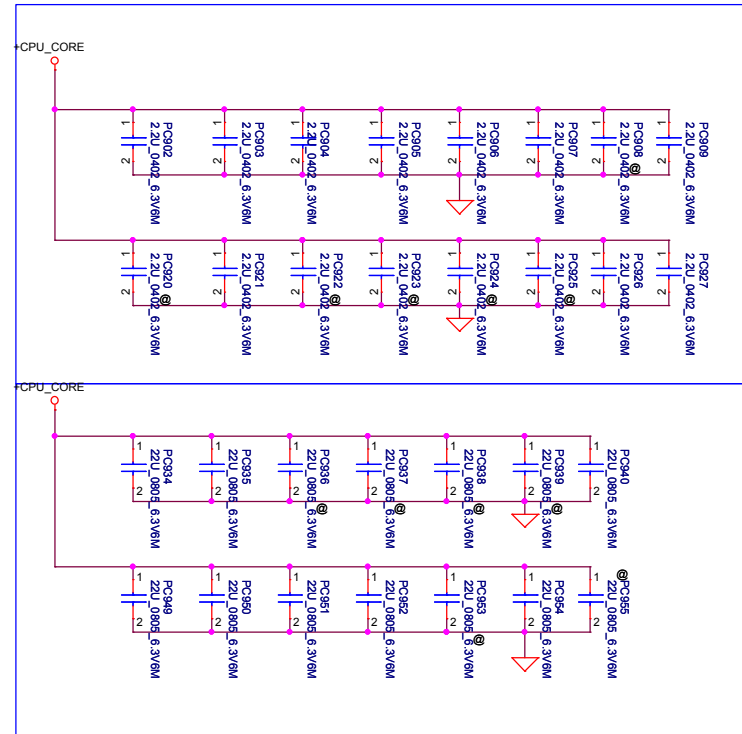
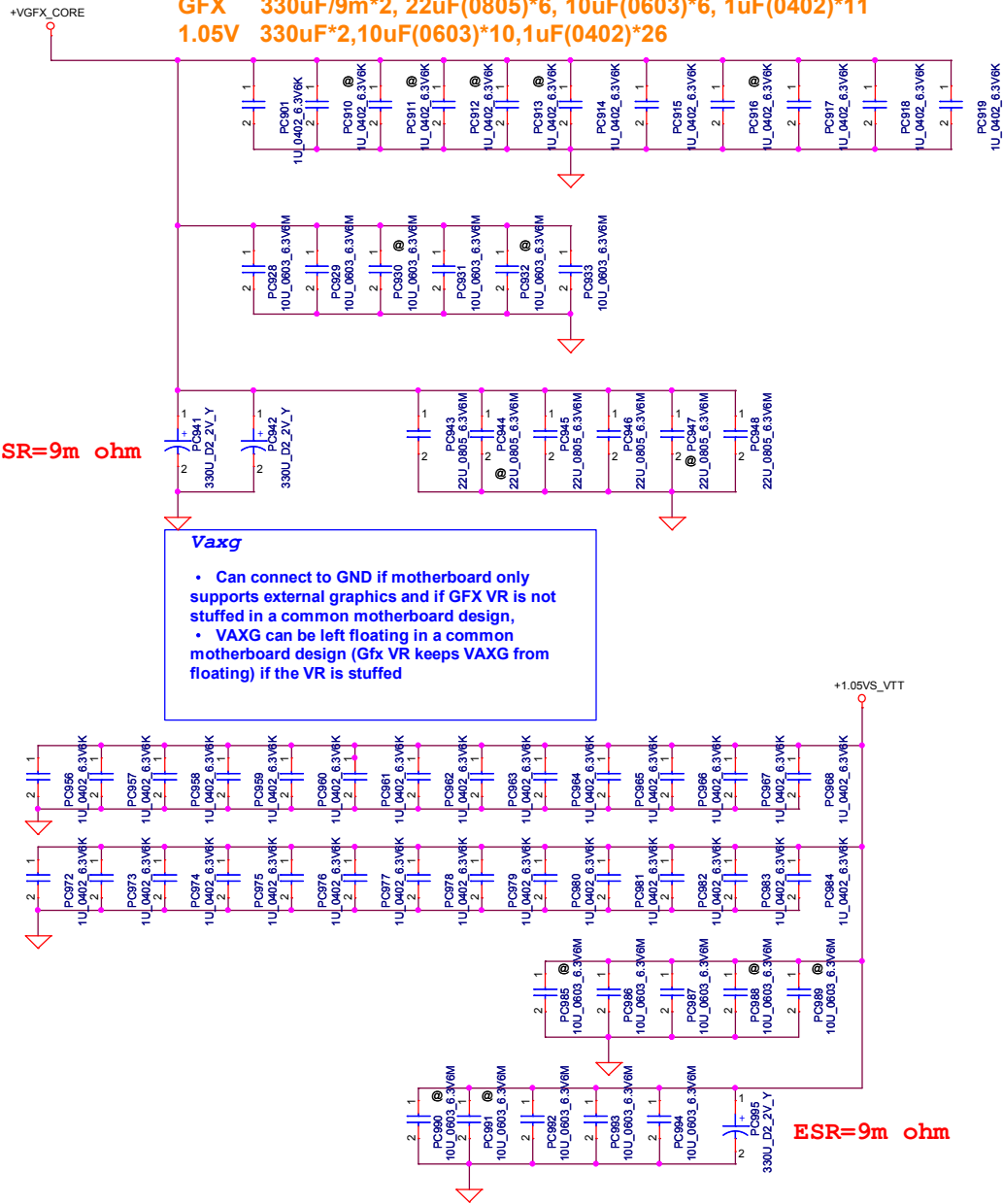
OCP setting=39.9~44.99A

PL701 PL702 Footprint用SH00000HQ00代替,因为SH00000NM00_R22为2PIN

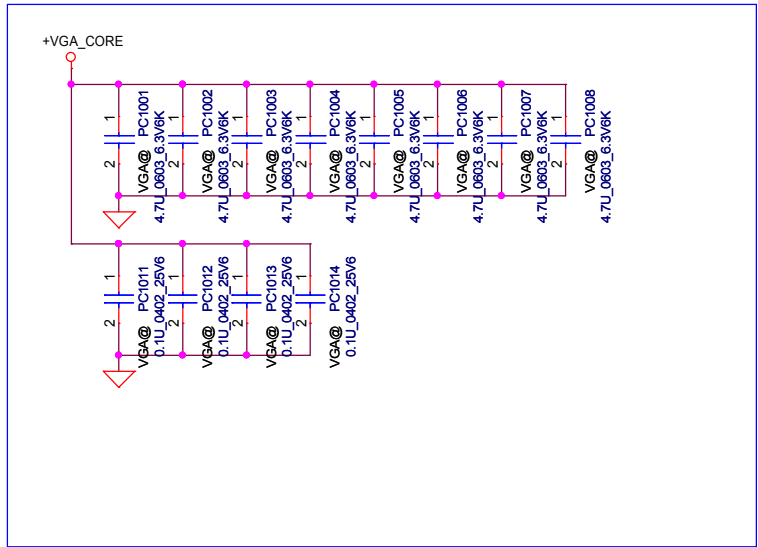
2012/07/05

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								Size	Document Number	Rev
								Cuskm	LA-9535P M/B Schematics	1.0
								Date:	Friday, June 07, 2013	Sheet
C		D		E						

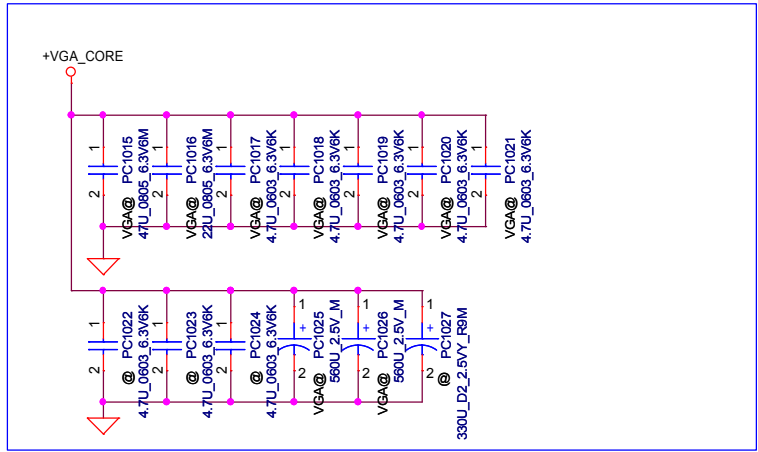
PWR Rule 17W@ULV(CR BGA1023_GT2) CPU2.9m GFx3.9m
CPU 330uF/9m *3, 22uF(0805) *12, 2.2uF(0402)*16
GFx 330uF/9m*2, 22uF(0805)*6, 10uF(0603)*6, 1uF(0402)*11
1.05V 330uF*2,10uF(0603)*10,1uF(0402)*26



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				Date	Friday, June 07, 2013
				Sheet	51 of 55
				Rev	1.0

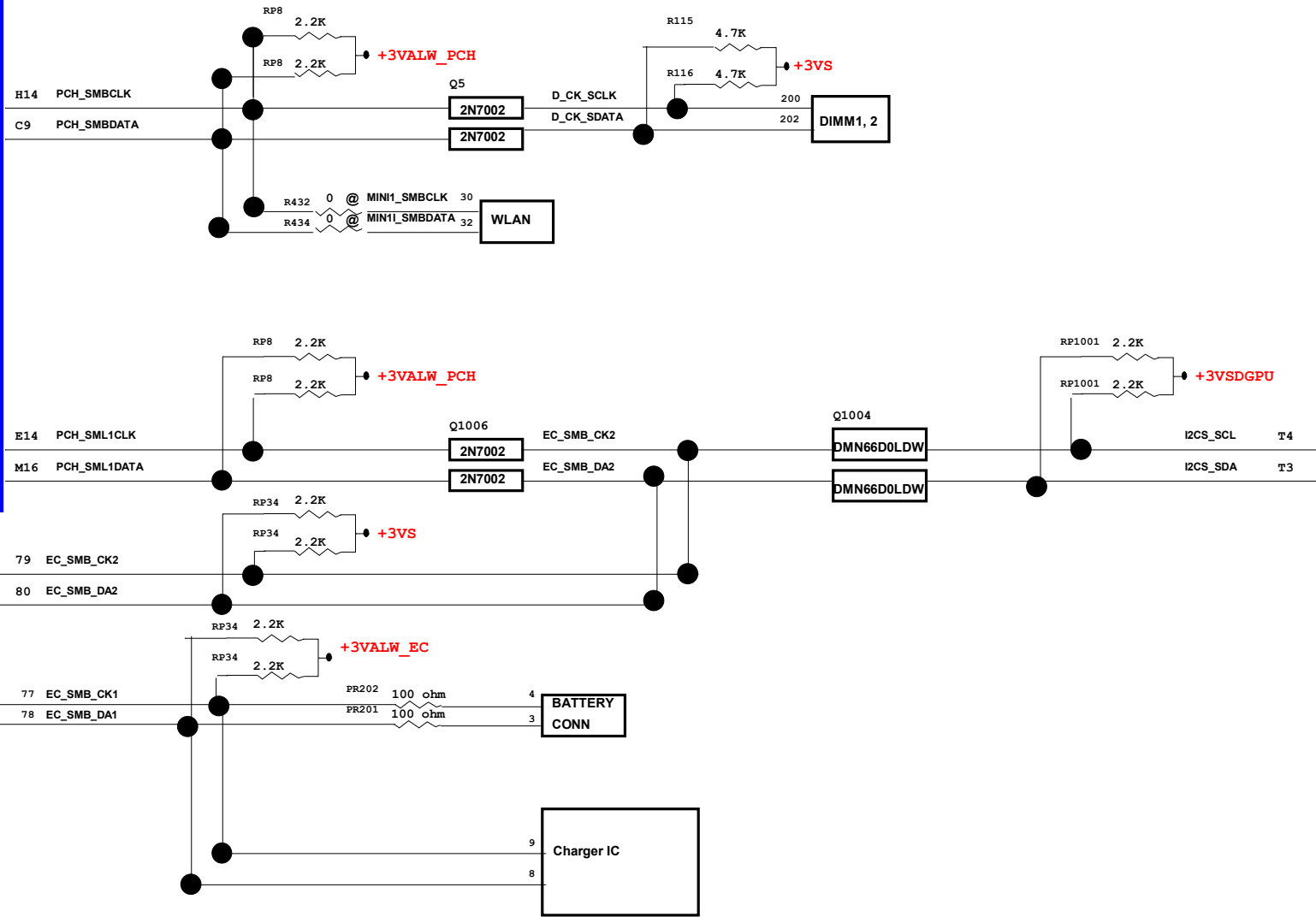
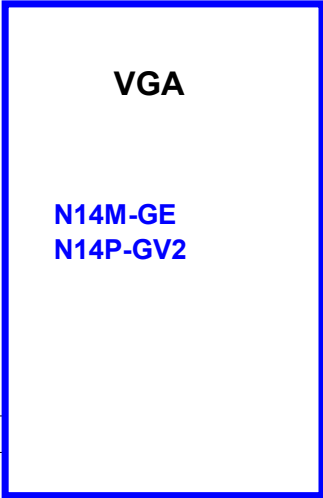
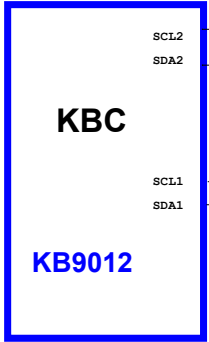
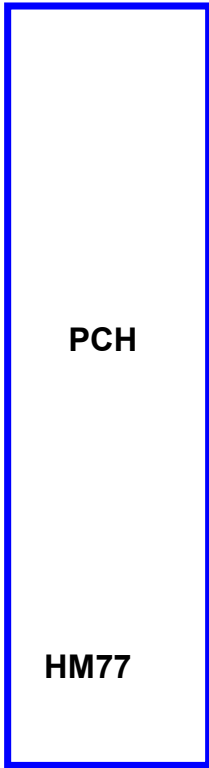


nVidia GB4-128 package
Under GPU
4.7uF 0603 * 10
0.1uF 0402 * 4



nVidia GB4-128 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5 (0603)
330uF POS *1 <6mΩ

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				Date: Friday, June 07, 2013	Rev 1.0
Sheet		52	of	55	



Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	For 4S battery request	44	mount PR319,PR321,PR326,PQ307,PQ308	0310	C
2	change size to common part	45	PC419 change to 0603 common part	0310	C
3	HW sequence request	47	PR1003 to 30k	0311	C
4	EMI request	44	not mount PC307	0312	C
5	EMI request	44	add PC745 PC746 PC747	0313	C
6	EMI request	44	change PR311 PR310 to 2.2Ohm	0313	C
7	GFX_OCP	49	change PR707 to 576hm	0314	C
8					
9					
10					
11					
12					
13				3/5	EVT
14				3/5	EVT
15					
16					
17					
18					
19					
20					

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				Date: Friday, June 07, 2013	Rev 1.0
				Sheet 54 of 55	

03/06
Change R1033 from 4.99K to 10K(ROM_SO VGA_DEVICE)
Change U51 N14P-GV2 from SA00006B500 to SA00006B510
Change Y6 P/N to SJ10000E800(合併用料)

03/11
Add net +XDPWR_SDPWR_MSPWR_R
Add share rom feature
Add R112 R140 R141 R144
Add EC_SPI_MISO_1 , PCH_SPI_MISO_1
Add EC_SPI_CS0# , PCH_SPI_CS0#
Add EC_SPI_CLK_1 , PCH_SPI_CLK_1
Add EC_SPI_MOSI_1 , PCH_SPI_MOSI_1
R541 pop 1K VGA@
R1101 470-->47 SD013470A80
D1000.3 VGA_PWROK changes into VGA_ON

SW3 @ 拿掉不上
Removed U15,R107,R108
Removed R151,R159,R160,R184,R97
Removed R524,R525,R526 換 RP13 5%--->1%

03/12
Add C441 470pF(SE074471K80),EMC@, EMI solution
Change U51 N14P-GV2 SA00006B510-->SA00006B530 R3 P/N
Change U51 N14M-GE SA000068A00-->SA000068A10 R3 P/N

0313a
Combine with PWR_Z5WE1_LA9535PR02_PWR_0313.DSN

0313b
Remove RP14,
PCH_GPIO2 不接
PCH_GPIO3 不接
PCH_GPIO53 不接

RP13 5%--->1%(SD300002Y00)

0313C
2nd rom 加回去
Add U15,R107,R108
Add R97 R151 R159 R160 R184
Del R112 R140 R141 R144

0314
R285 XEMC@-->EMC@
C329 22P-->10P, XEMC@-->EMC@

Add C230 0.1U for card reader enable

Board ID
R316 0ohm 改 8.2K 上件
R314 @-->改上件
C346 @-->改上件

0314C
R774 change from 10 to 56ohm
R1027,R1028,R1029,R1030,R1035,R1036,R1039,R1033,R1042
at N14M-GE SKU 10K_0402_5% change to 10K_0402_1%

0314d
L33 changes into SM010014520

0315a
Add net CRT_4, CRT_11 for 測點
R541 bom structure--->VGA@
C346 board ID cap改@ 不上

0318
L24,L25 change from SM070001600 (12ohm USB3.0 common mode choke)
to SM070001R00 (Murata 67ohm)

0419
Add Touch screen feature and JTS1

0422
Remove PEG 16X

0425
Add HM70 NM70 文字敘述
Add FFR VRAM strap for N14M-GE N14P-GV2

0502
Update CPU,PCH,VRAM P/N

0505
Pop RP16 for LAN loopback

0528
N14M-GE ROM_SO keep 10K pull low.
N14P-GV2 need change be to EVT R1033 as 4.99K_0402_1%

C142-->15pF(SE071150J80) to meet off mode timing

0604
Correct page1 date code
Update page24 3D device/vga device notice

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						Date:		Friday, June 07, 2013		Sheet 55 of 55	