

Compal Confidential

PEW76/86/96 M/B Schematics Document

AMD Danube Only UMA

AMD Champlain Processor with RS880M/SB820M

2010-07-20

LA6552P REV: 1.0

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Model Name : PEW96

File Name : LA-6552P

P/N : DA60000IM10

PCB



LA-6552P MB Rev0: DA60000IM00
LA-6552P MB Rev1: DA60000IM10
LA-6552P MB Rev1: DAZ0FQ00200

Danube

AMD S1G4 Processor

uPGA-638 Package
Champlain page 6,7,8,9

Memory BUS(DDR3)

Dual Channel

1.5V DDRIII 1066~1333MHz

204pin DDRIII-SO-DIMM X2

BANK 0, 1, 2, 3 page 10,11

Hyper Transport Link
16 x 16

ATI RS880M

uFCBGA-528

page 12,13,14

A link Express2
Gen1

ATI SB820M

uFCBGA-605

page 18,19,20,21,22

Thermal Sensor

ADM1032

page 8

page 27

USB
conn
X 3

USB port 0,1,2

page 15

CMOS
Camera

USB port 5

page 27

Bluetooth
Conn

<Option>
USB port 7

page 26

Mini
card
(WL)X1

USB port 8

page 26

Card
Reader

RTS5137
USB port 6

3.3V 48MHz

3.3V 24.576MHz/48MHz

HD Audio

S-ATA

Gen2

SATA HDD
Conn.

page 23

port 0

SATA ODD
FFC Conn.

page 23

port 1

HDA Codec

ALC272X

page 30

Audio AMP

page 31

Phone Jack x2

page 31

LPC BUS

ENE KB926

page 28

Touch Pad

page 29

Int.KBD

page 29

EC I/O Buffer

page 29

BIOS

page 29

LVDS

page 15

CRT

page 17

HDMI Conn.

page 16

MINI Card 1

WLAN

page 26

GPP1

LAN(GbE)

Broadcom

BCM57780

page 24

GPP0

RJ45

page 25

LED

page 29

Fan Control

page 32

RTC CKT.

page 18

LID SW / MEDIA/B

page 28

Power On/Off CKT.

page 32

DC/DC Interface CKT.

page 33

Power Circuit

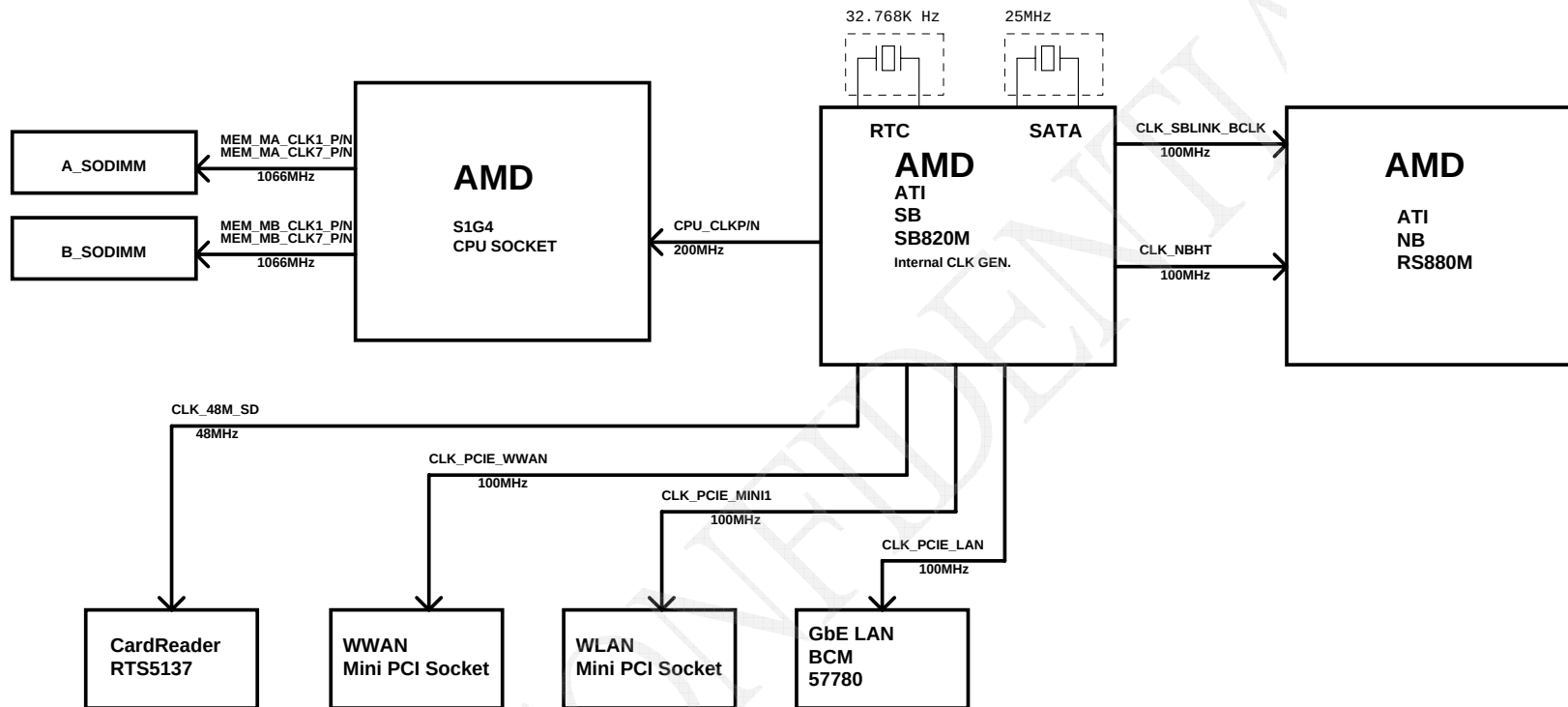
page 34,35,36,37,38
39,40,41,42

Extend Card/B

1. USB X2

2. ODD X1

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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU (1.375-1.5V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+CPU_VDDR	1.05V switched power rail	ON	OFF	OFF
+0.75V	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V power rail for MINI Card	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

EC SM Bus1 address

EC SM Bus2 address

SB820
SM Bus 0 address

SB820
SM Bus 1 address

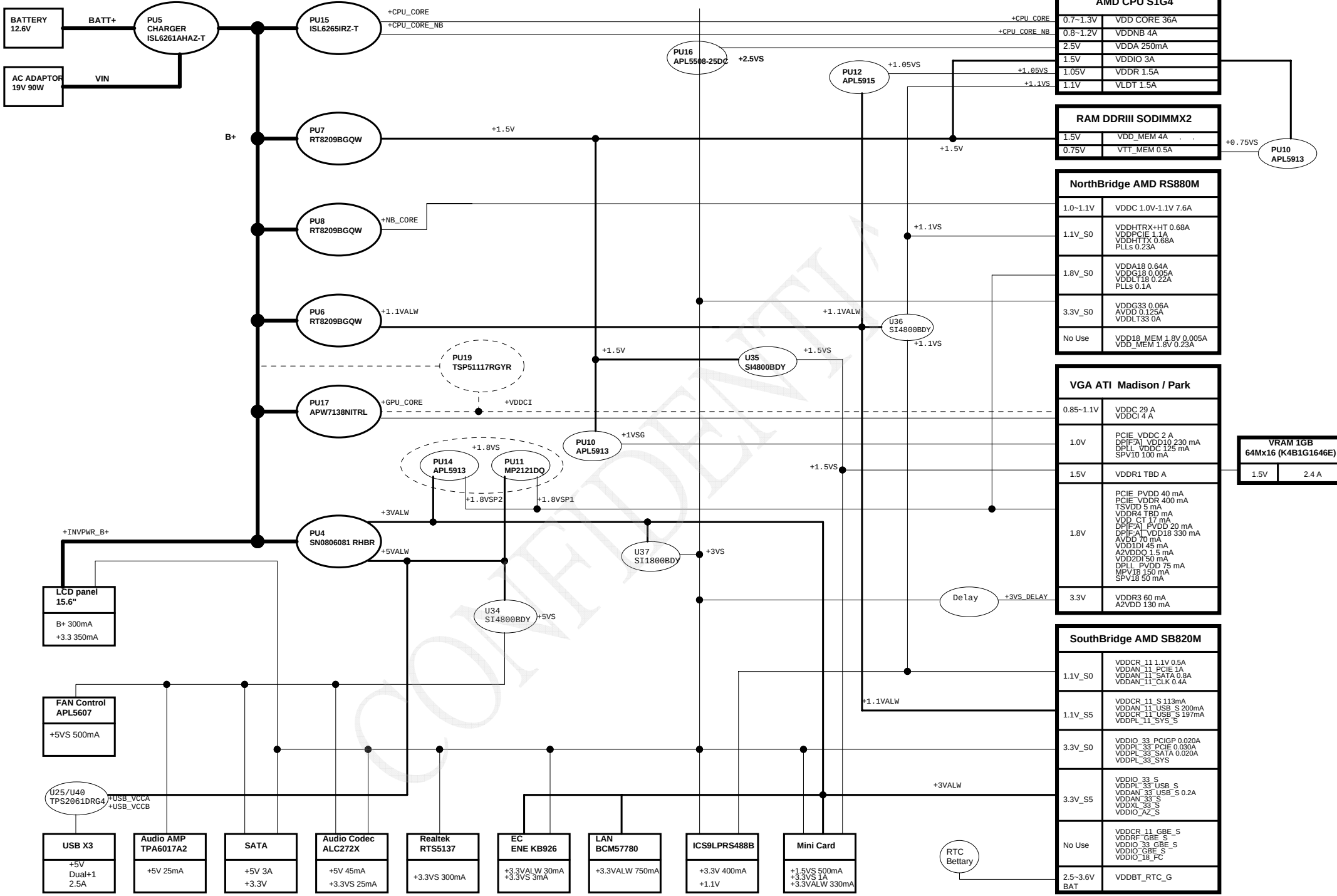
STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	<i>EVT / PVT stage (w/ pach code)</i>
1	
2	
3	
4	
5	
6	
7	

Board ID	PCB Revision
0	
1	PEW76/86/96
2	
3	
4	
5	
6	
7	

[illegible]



AMD CPU S1G4	
0.7~1.3V	VDD CORE 36A
0.8~1.2V	VDDNB 4A
2.5V	VDDA 250mA
1.5V	VDDIO 3A
1.05V	VDDR 1.5A
1.1V	VLDI 1.5A

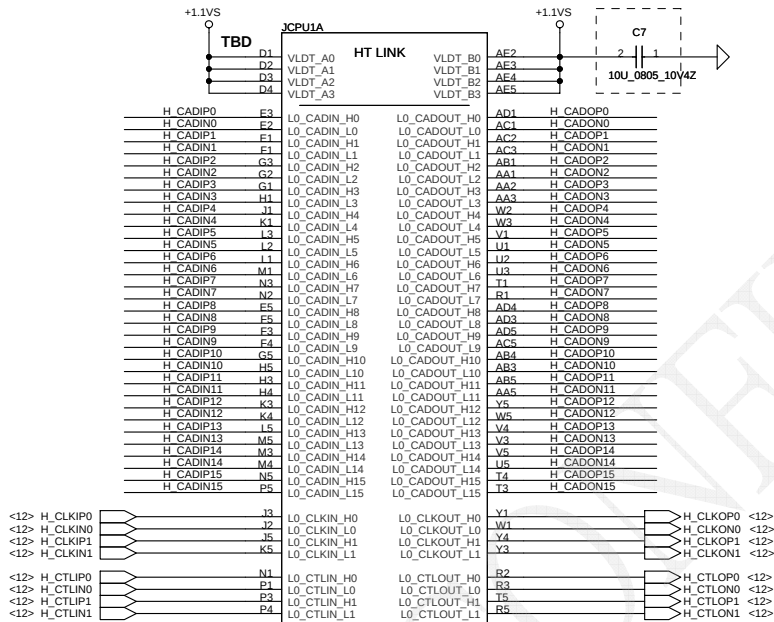
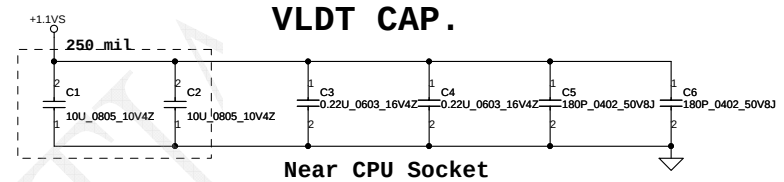
RAM DDRIII SODIMMX2	
1.5V	VDD_MEM 4A
0.75V	VTT_MEM 0.5A

NorthBridge AMD RS880M	
1.0~1.1V	VDDC 1.0V~1.1V 7.6A
1.1V_S0	VDDHTRX+HT 0.68A VDDPOIE 1.1A VDDHTTX 0.68A PLLs 0.23A
1.8V_S0	VDDA18 0.64A VDDG18 0.005A VDDL18 0.22A PLLs 0.1A
3.3V_S0	VDDG33 0.06A AVDD 0.125A VDDL33 0A
No Use	VDD18_MEM 1.8V 0.005A VDD_MEM 1.8V 0.23A

VGA ATI Madison / Park	
0.85~1.1V	VDDC 29 A VDDCI 4 A
1.0V	PCIE_VDDC 2 A DP1E_A1 VDD10 230 mA DPLL_VDDC 125 mA SPV10 100 mA
1.5V	VDDR1 TBD A
1.8V	PCIE_PVDD 40 mA PCIE_VDDR 400 mA TSVDD 5 mA VDDR4 TBD mA VDD_CT 17 mA DP1E_A1 PVDD 20 mA DP1E_A1 VDD18 330 mA AVDD 70 mA VDD1D1 45 mA AZVDDQ 1.5 mA VDD2D1 50 mA DPLL_PVDD 75 mA MPV18 150 mA SPV18 50 mA
3.3V	VDDR3 60 mA AZVDD 130 mA

VRAM 1GB 64Mx16 (K4B1G1646E) * 8	
1.5V	2.4 A

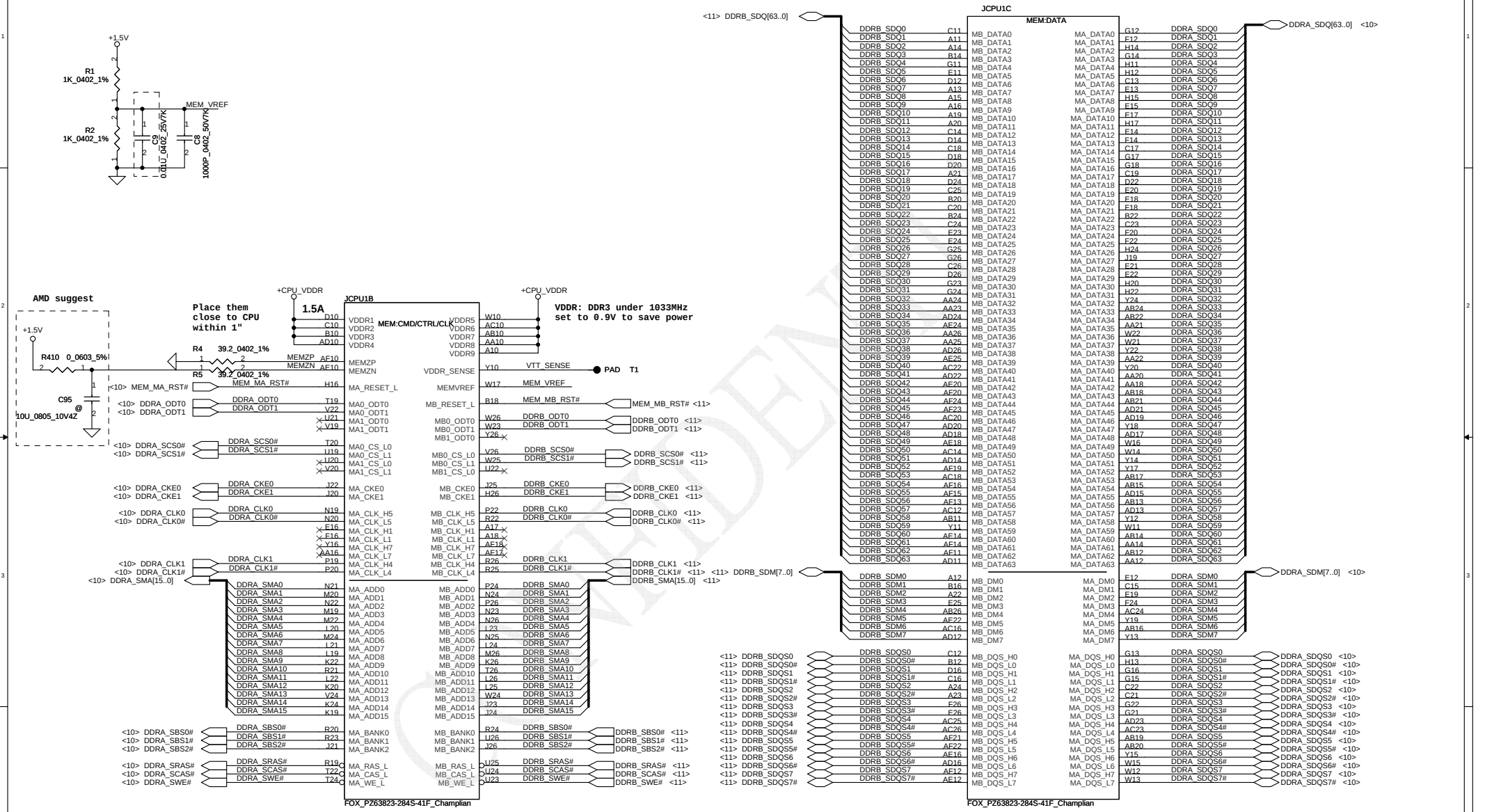
SouthBridge AMD SB820M	
1.1V_S0	VDDCR_11_S 1.1V 0.5A VDDAN_11_PCIE 1A VDDAN_11_SATA 0.8A VDDAN_11_CLK 0.4A
1.1V_S5	VDDCR_11_S 113mA VDDAN_11_USB_S 200mA VDDCR_11_USB_S 197mA VDDPL_11_SYS_S
3.3V_S0	VDDIO_33_PCIGP 0.020A VDDPL_33_PCIE 0.030A VDDPL_33_SATA 0.020A VDDPL_33_SYS
3.3V_S5	VDDIO_33_S VDDPL_33_USB_S VDDAN_33_USB_S 0.2A VDDAN_33_S VDDXL_33_S VDDIO_AZ_S
No Use	VDDCR_11_GBE_S VDDRF_GBE_S VDDIO_33_GBE_S VDDIO_GBE_S VDDIO_18_FC
2.5~3.6V BAT	VDDBT_RTC_G



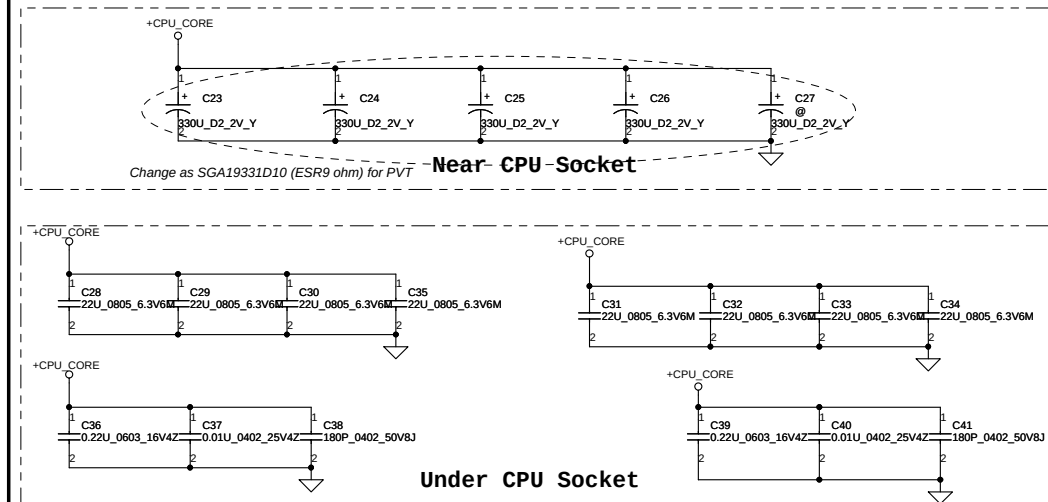
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				AMD CPU S1G4 HT I/F			
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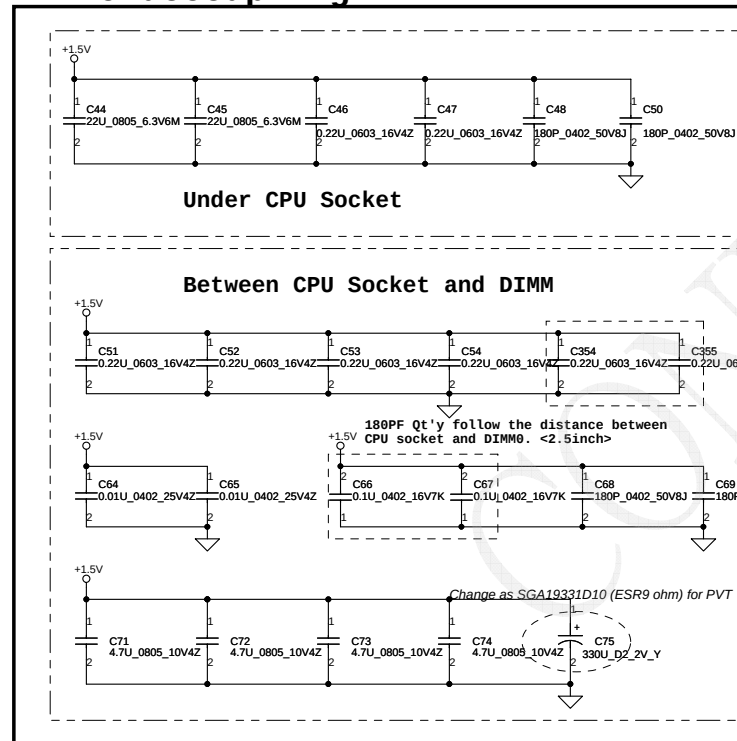
Processor DDR3 Memory Interface



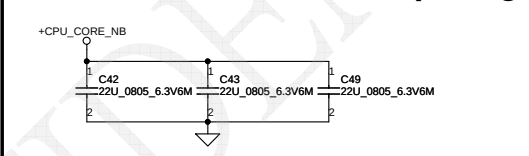
VDD(+CPU_CORE) decoupling.



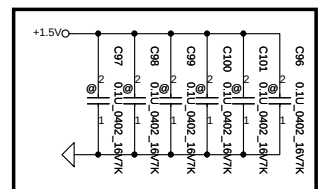
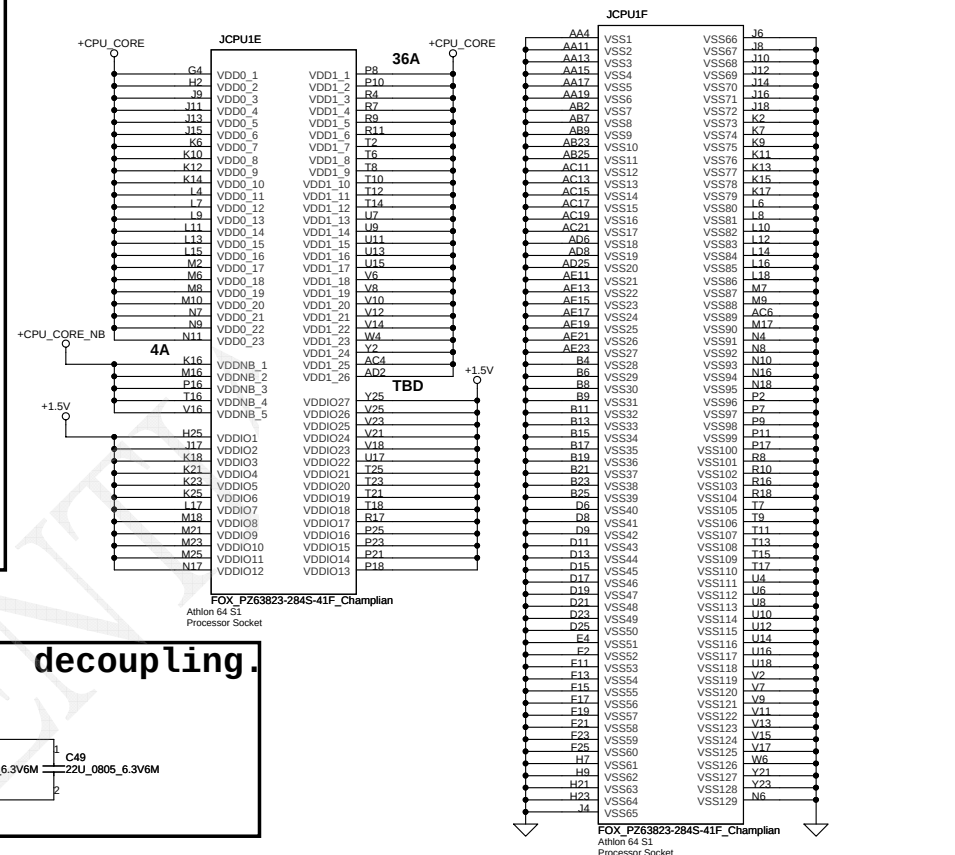
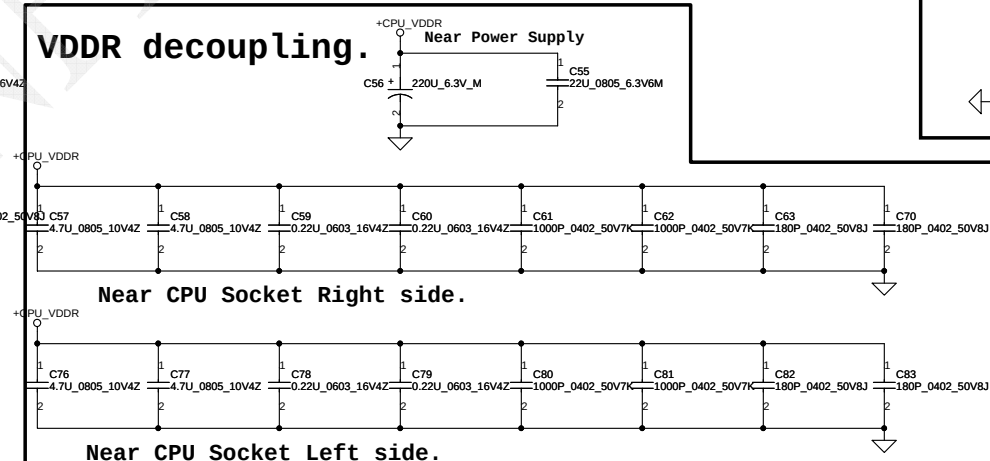
VDDIO decoupling.

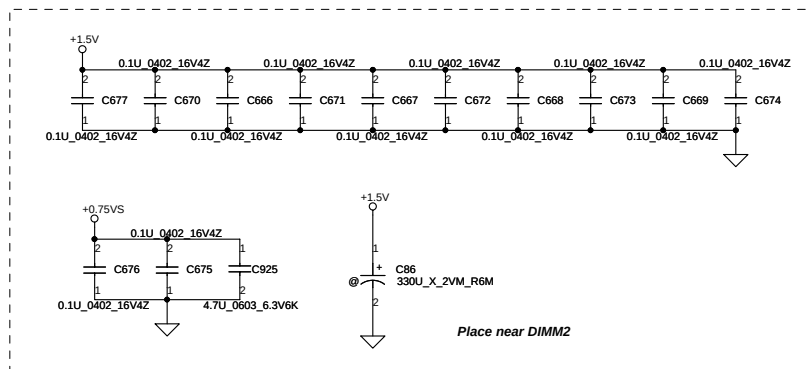


+CPU_CORE_NB decoupling.

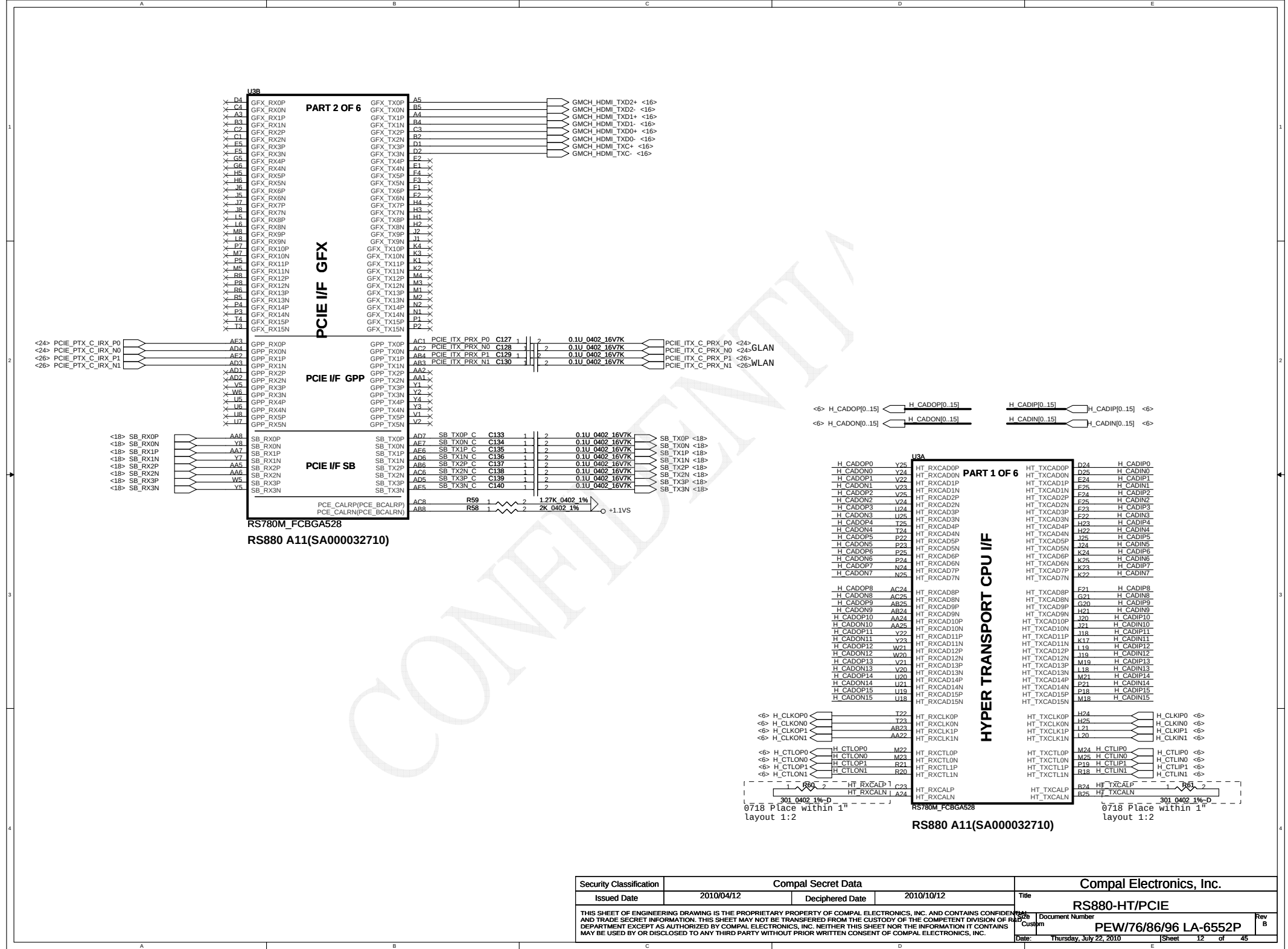


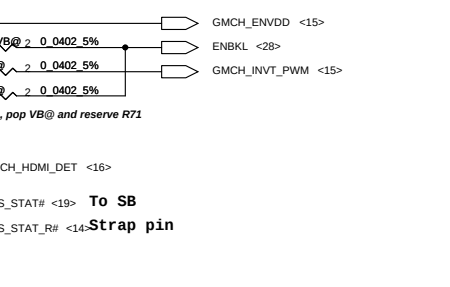
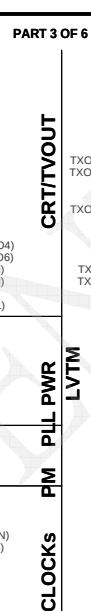
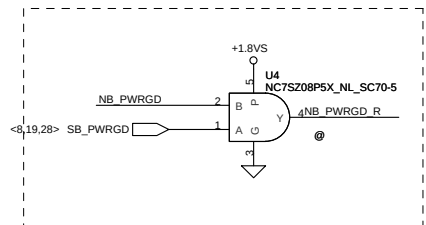
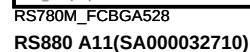
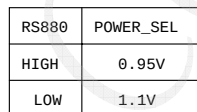
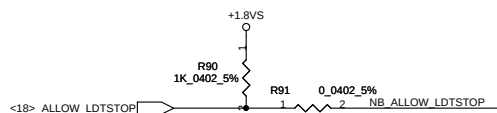
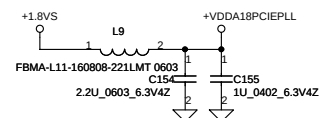
VDDR decoupling.





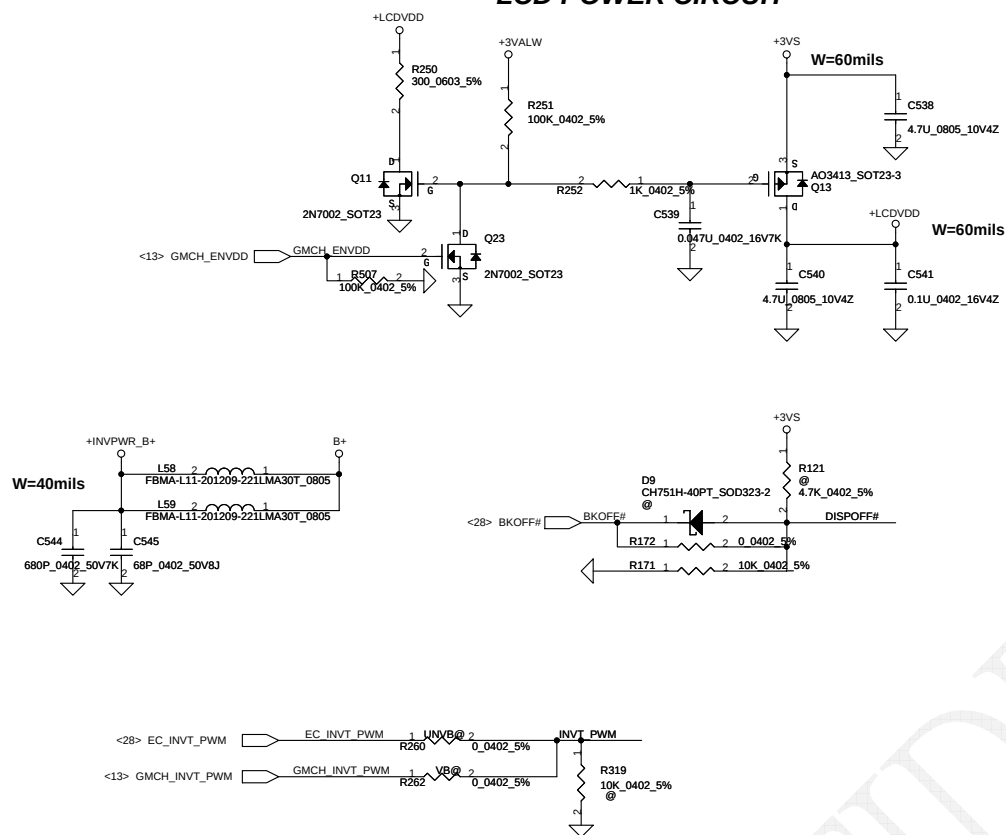
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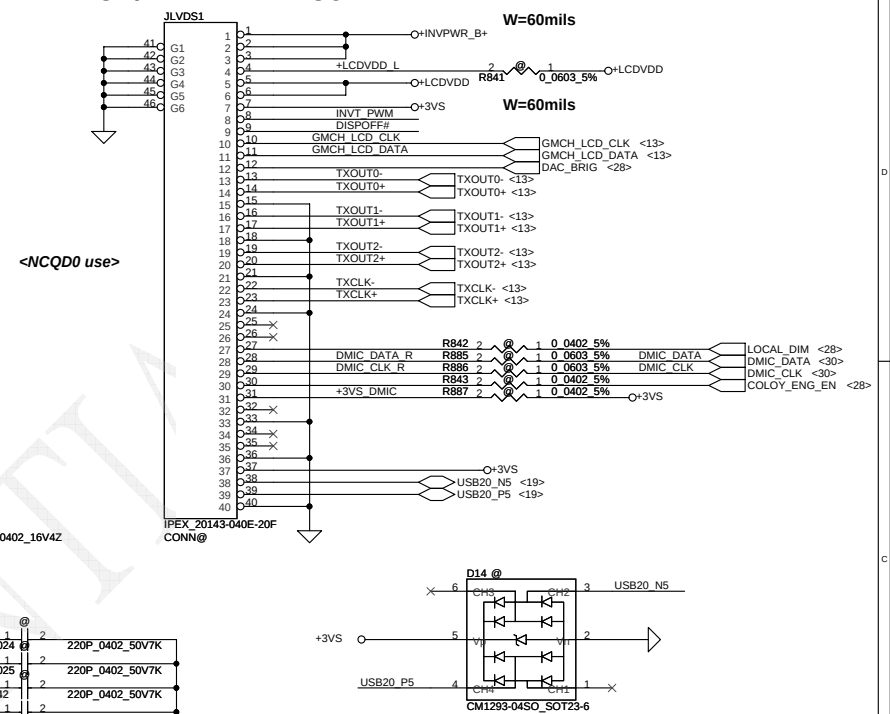


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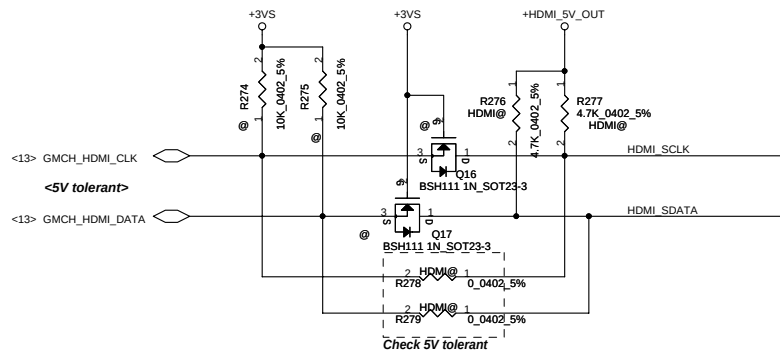
LCD POWER CIRCUIT



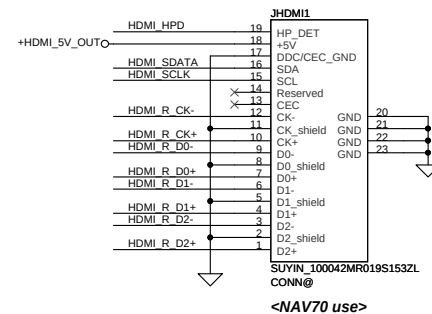
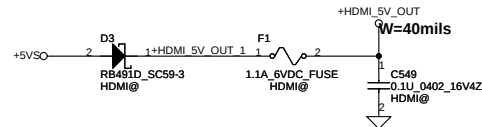
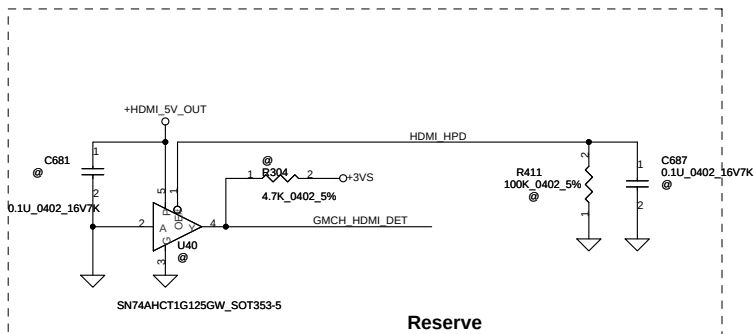
LCD/LED PANEL Conn.



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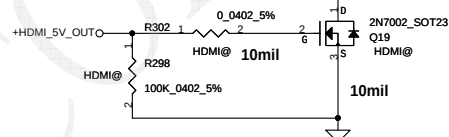


Place closed to JHDMI1

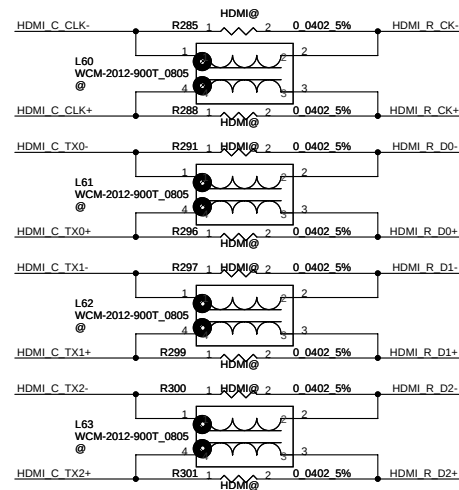


UMA 715 ohm

<12> GMCH_HDMI_TXD2-	C550	HDMI@	1	0.1U_0402_16V7K	HDMI C TX2-	R286	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD2+	C551	HDMI@	1	0.1U_0402_16V7K	HDMI C TX2+	R287	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD1-	C552	HDMI@	1	0.1U_0402_16V7K	HDMI C TX1-	R289	1	HDMI@	2	715_0402_1%
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<12> GMCH_HDMI_TXD0-	C554	HDMI@	1	0.1U_0402_16V7K	HDMI C TX0-	R292	1	HDMI@	2	715_0402_1%
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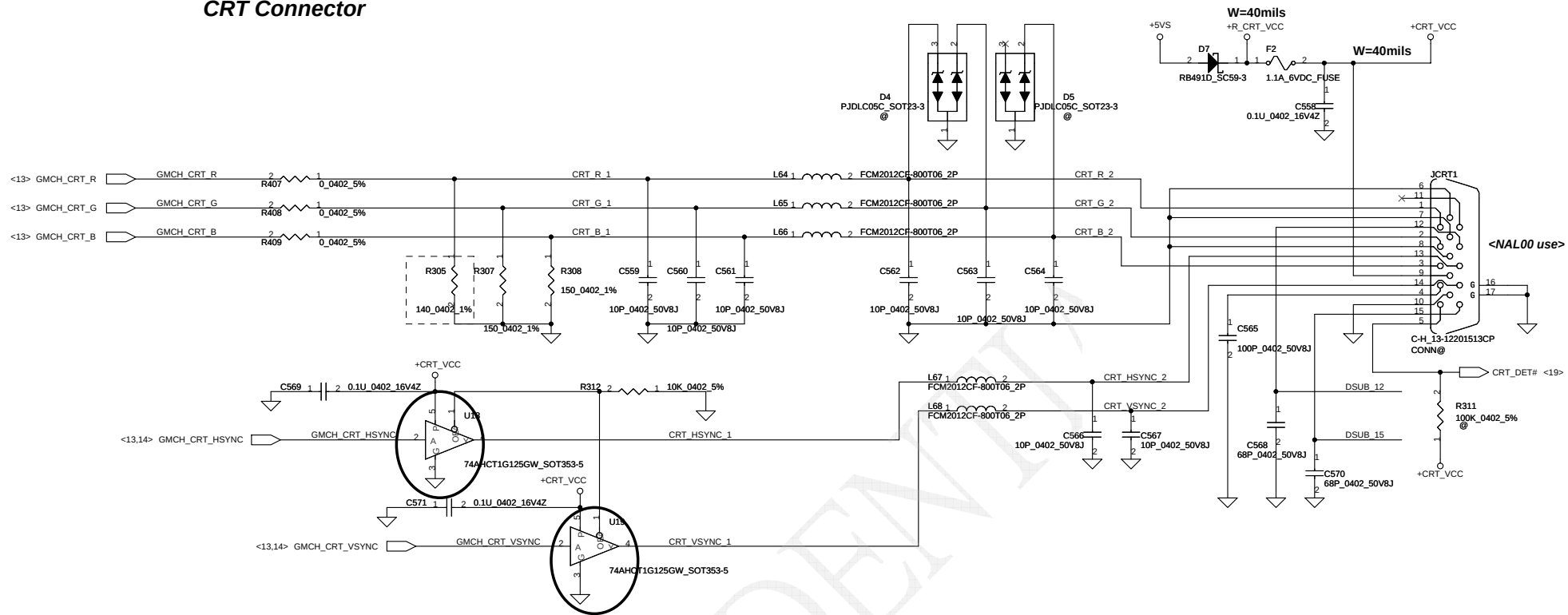


Place closed to JHDMI1



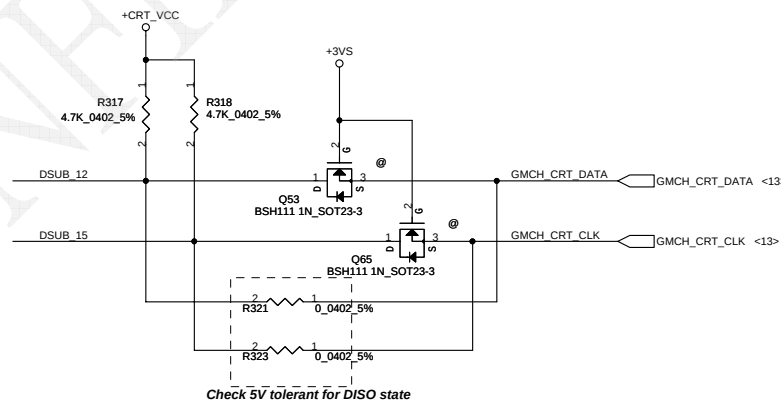
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CRT Connector

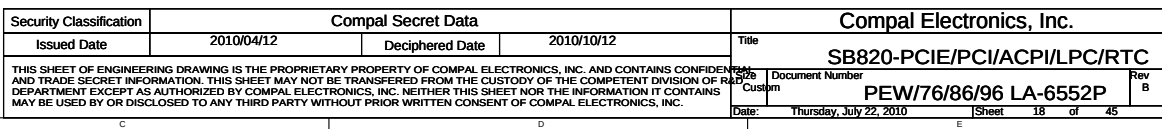
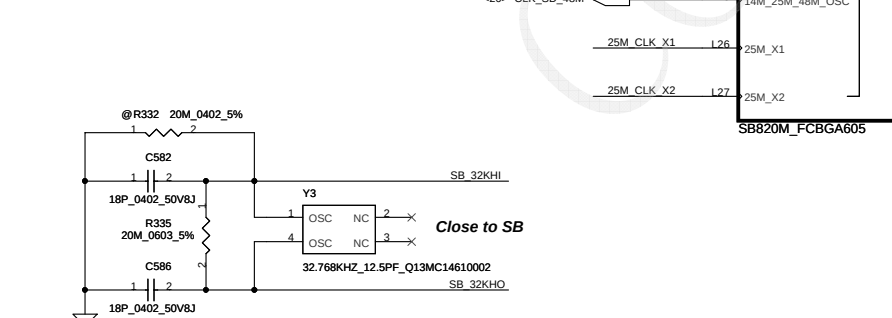


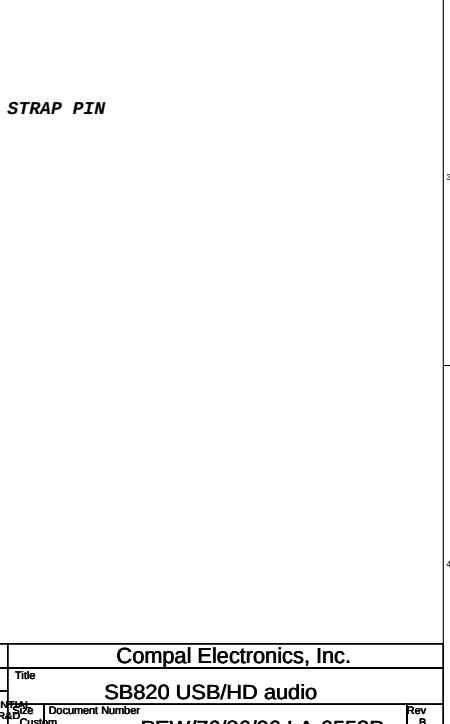
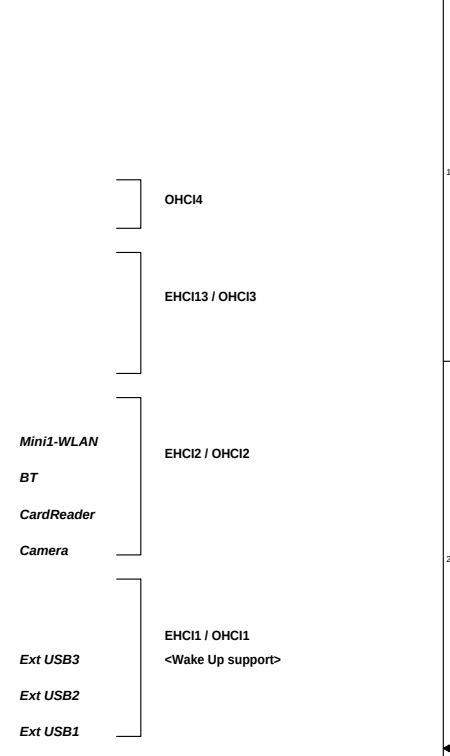
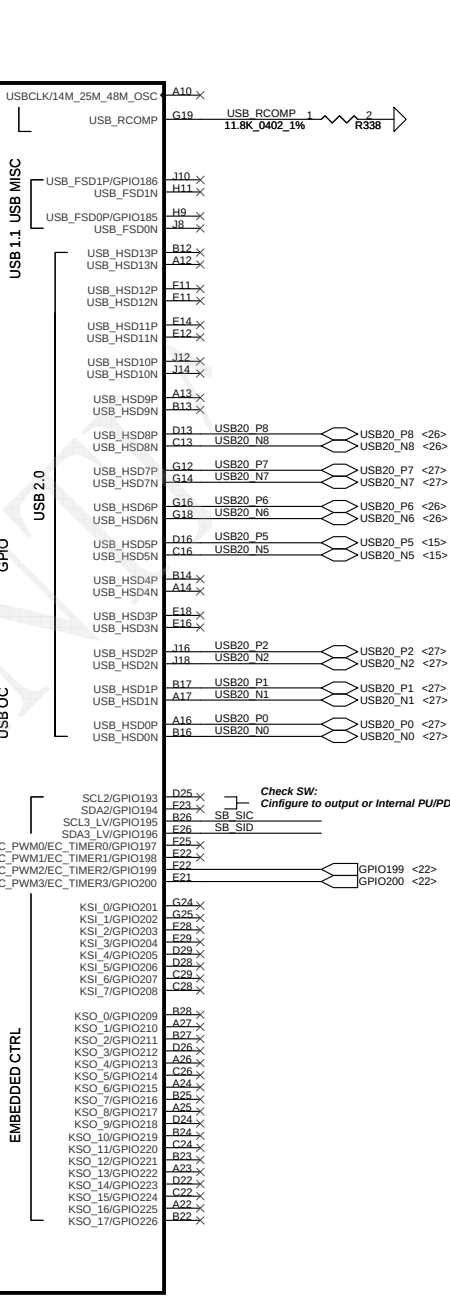
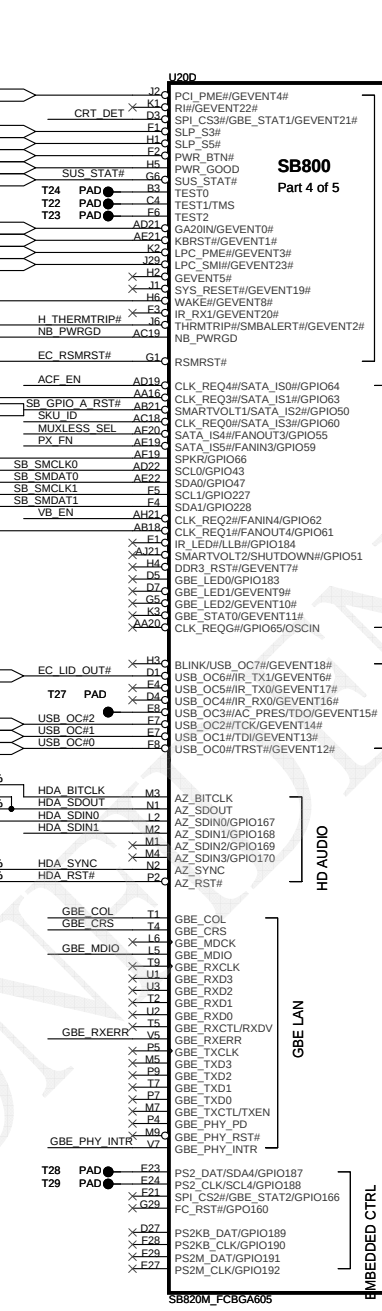
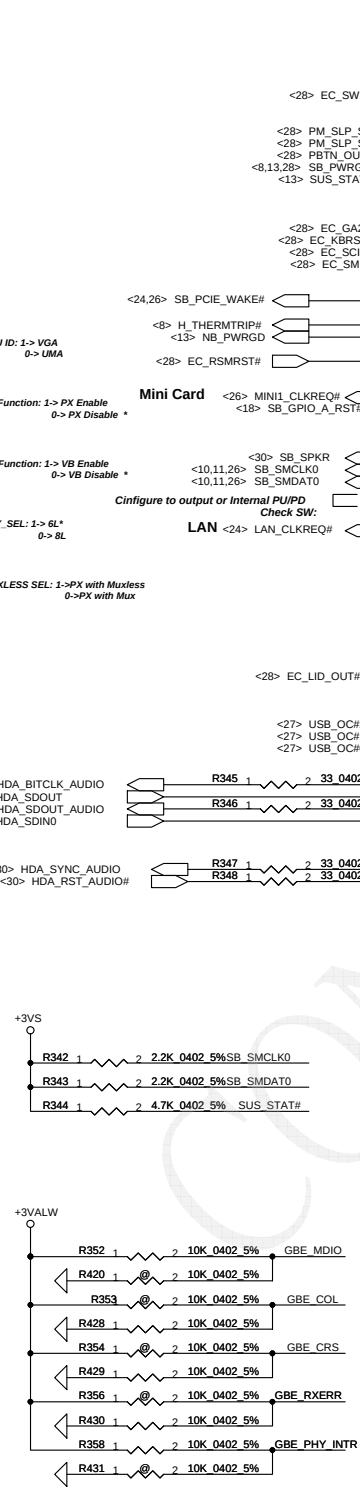
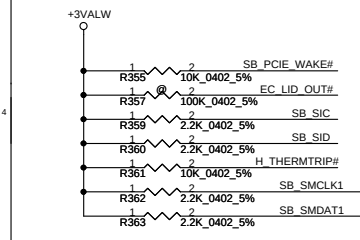
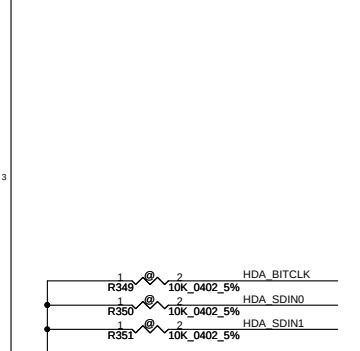
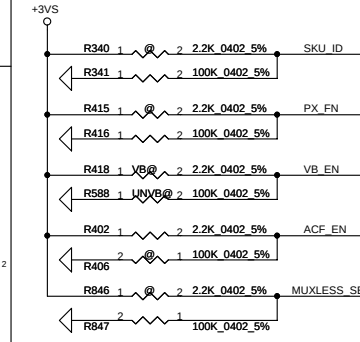
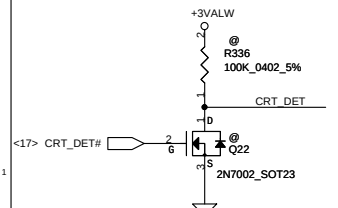
Change as SA411250110

Close to Conn side

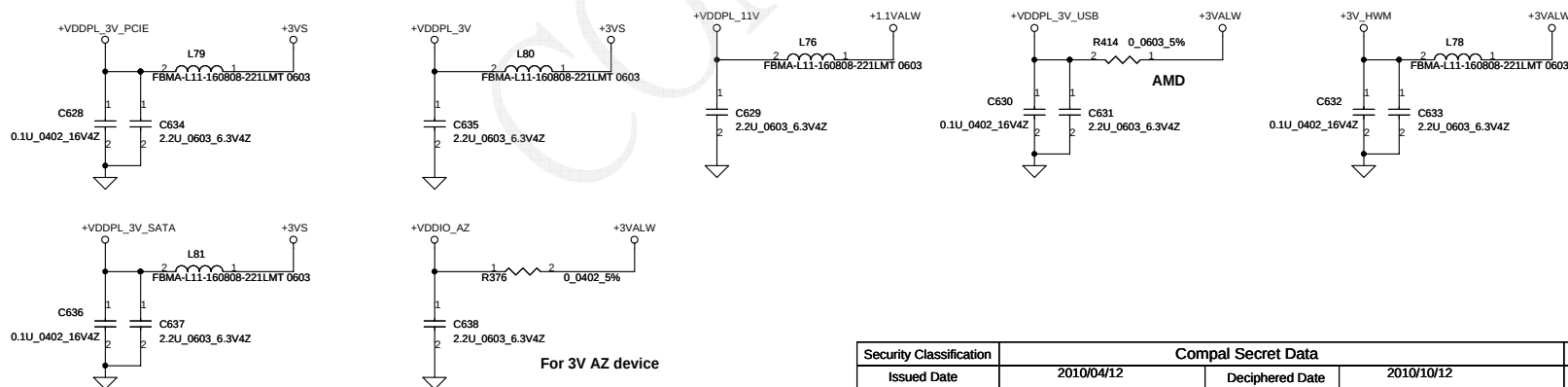
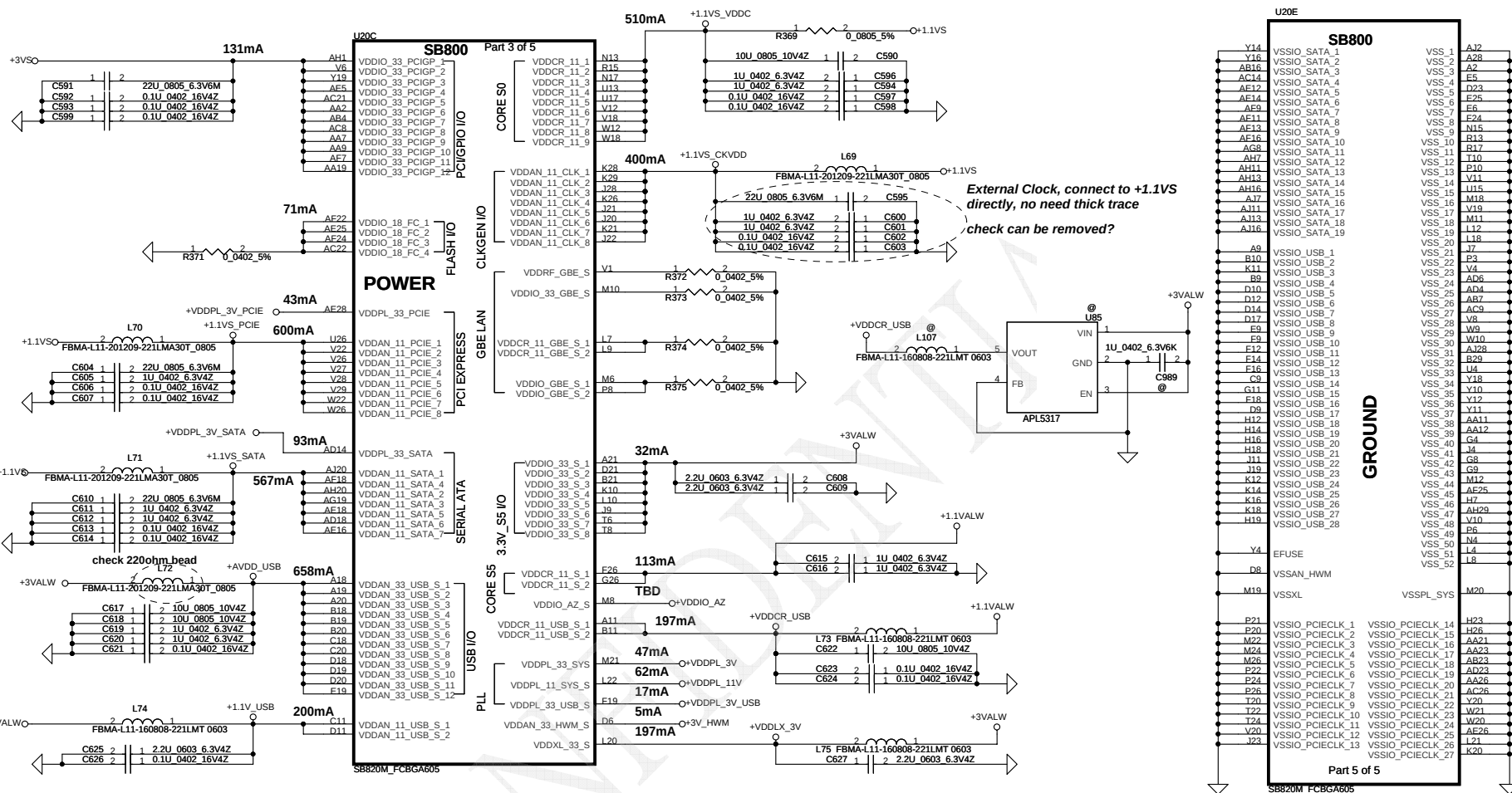


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				Document Number	Rev B
				PEW/76/86/96 LA-6552P	
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				Sheet	19 of 45

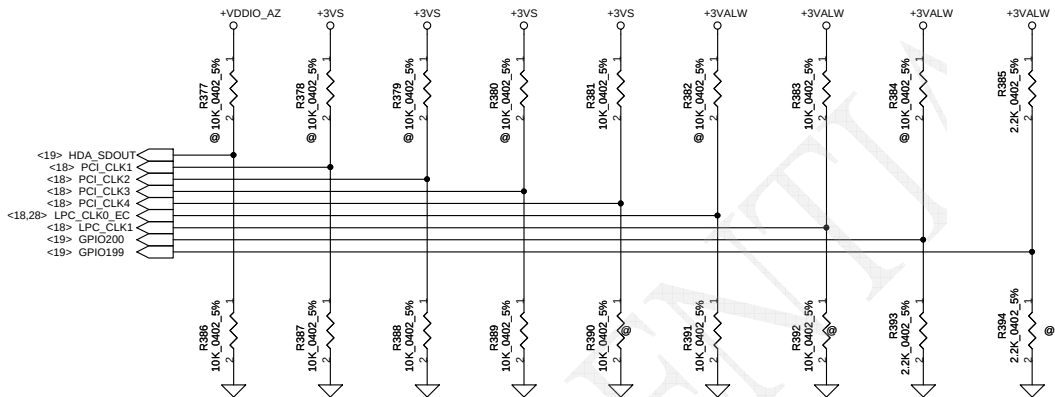


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								Date:		Thursday, July 22, 2010		Sheet		21		of 45	
								Rev		B							

REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1		GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable	EC ENABLE	CLOCKGEN ENABLE		H,H = Reserved H,L = SPI ROM	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	Inter CLK Gen Mode Disable	EC DISABLE	CLOCKGEN DISABLE		L,H = LPC ROM (Default L,NC) L,L = FWH ROM	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT			



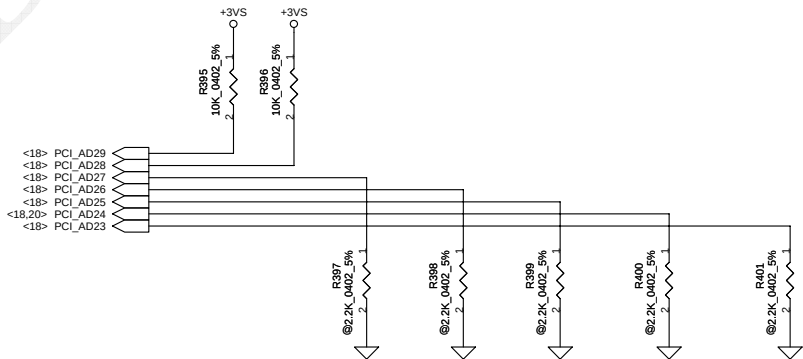
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

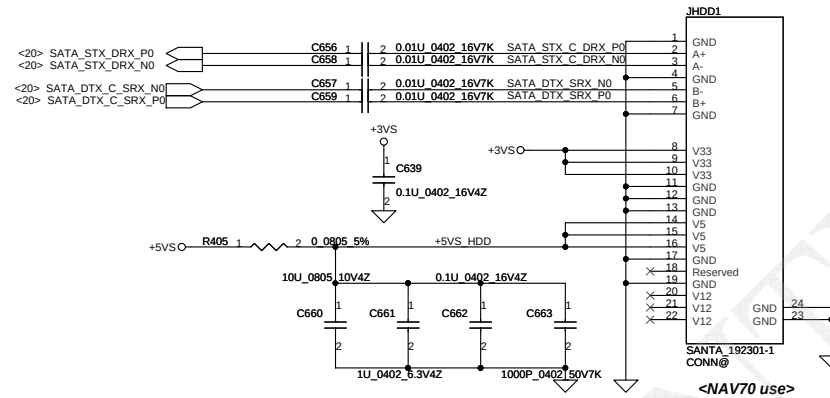
		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

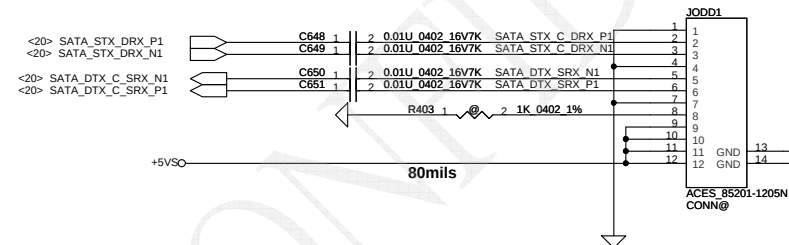
check default



SATA HDD Conn.

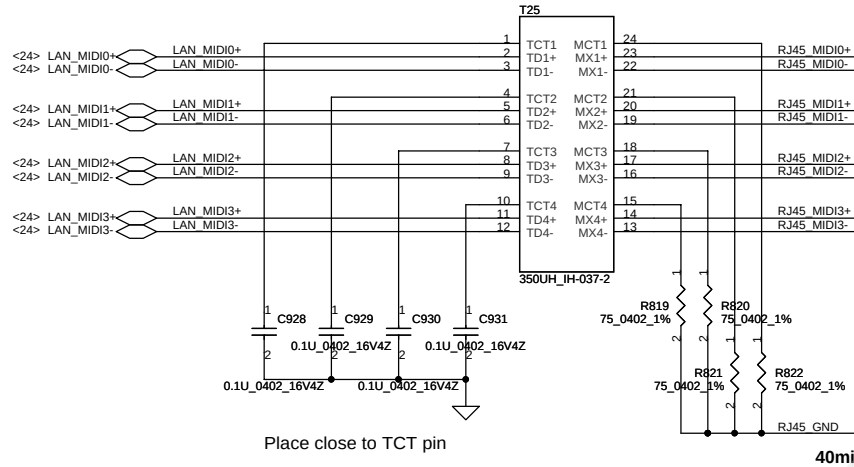


SATA ODD FFC Conn.

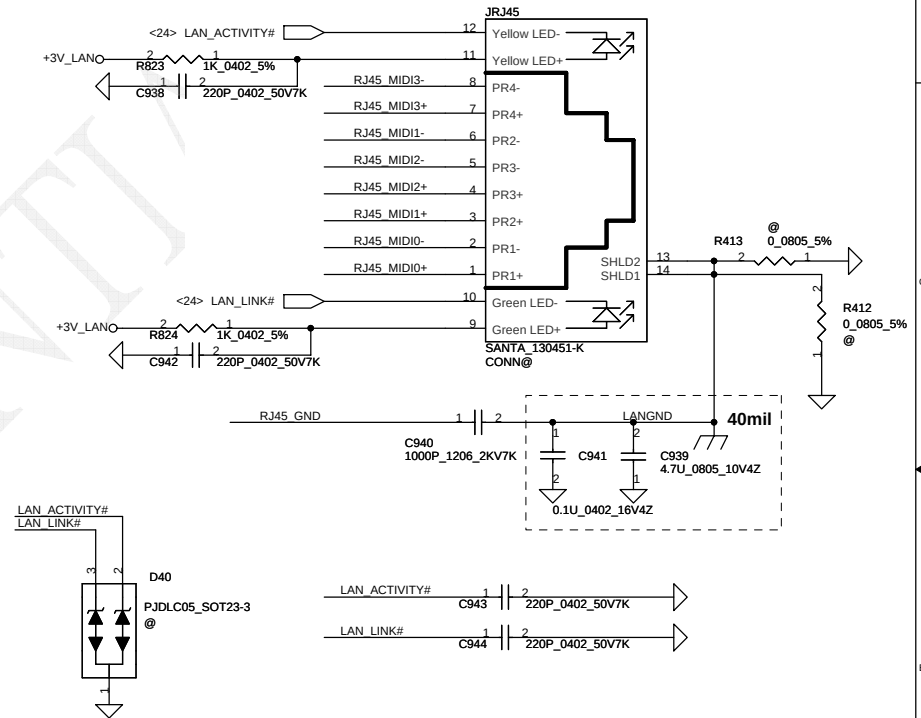


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Date: Thursday, July 22, 2010				Sheet 23 of 45				HDD & ODD Connector			
PEW/76/86/96 LA-6552P											

BH GS5009-D <SP050006B00>

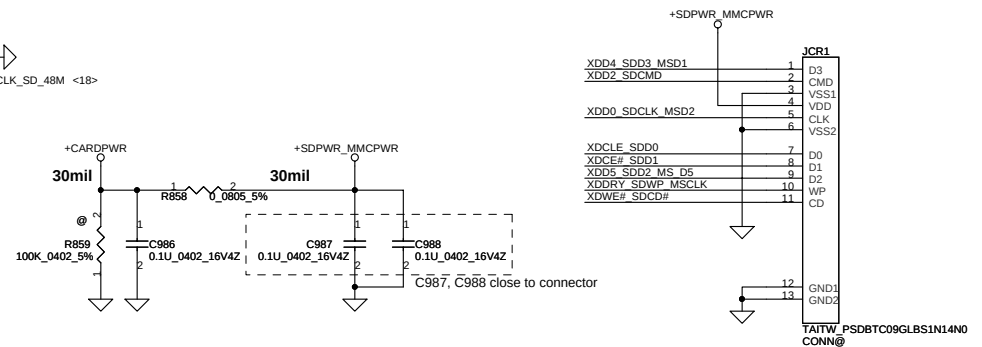
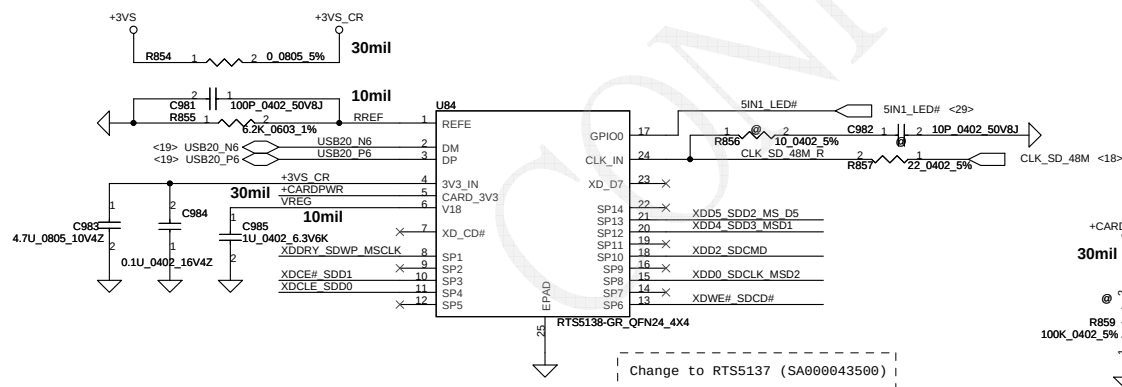
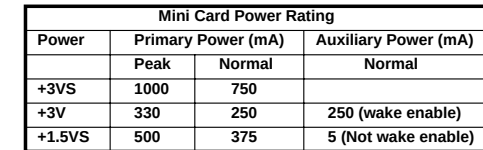


LAN Connector

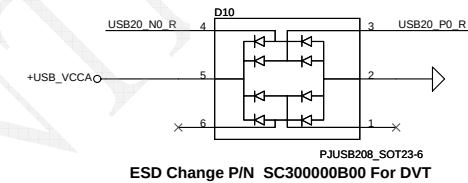
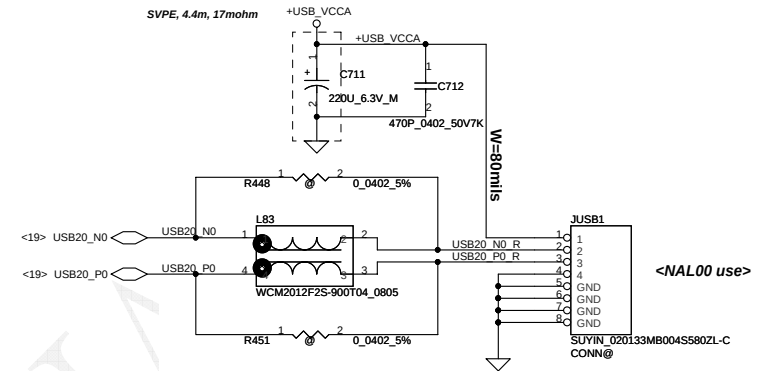
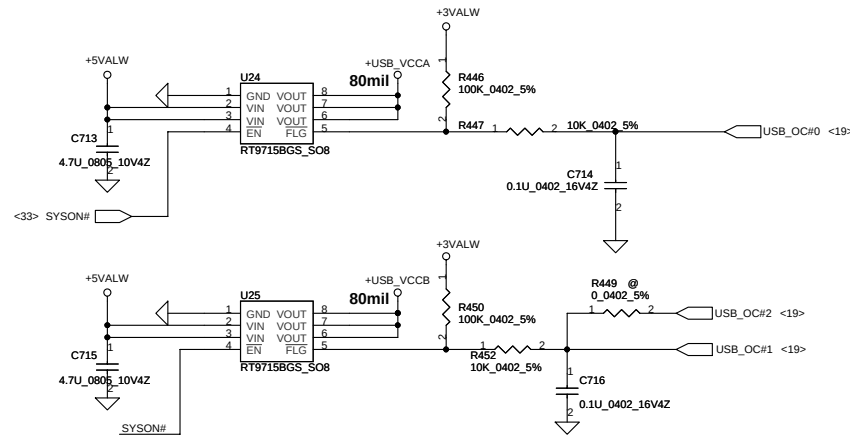


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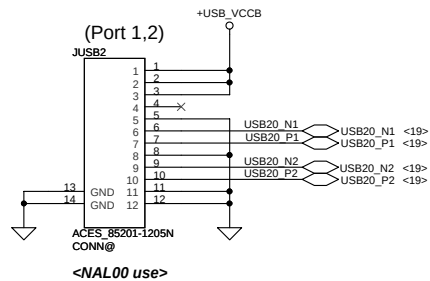
Card Reader Connector



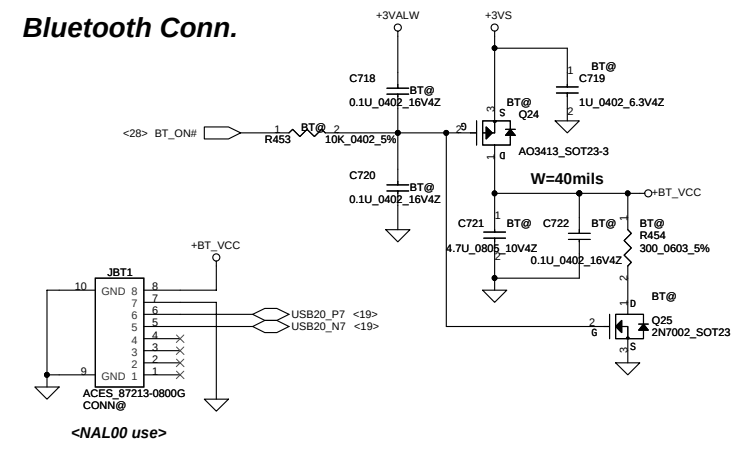
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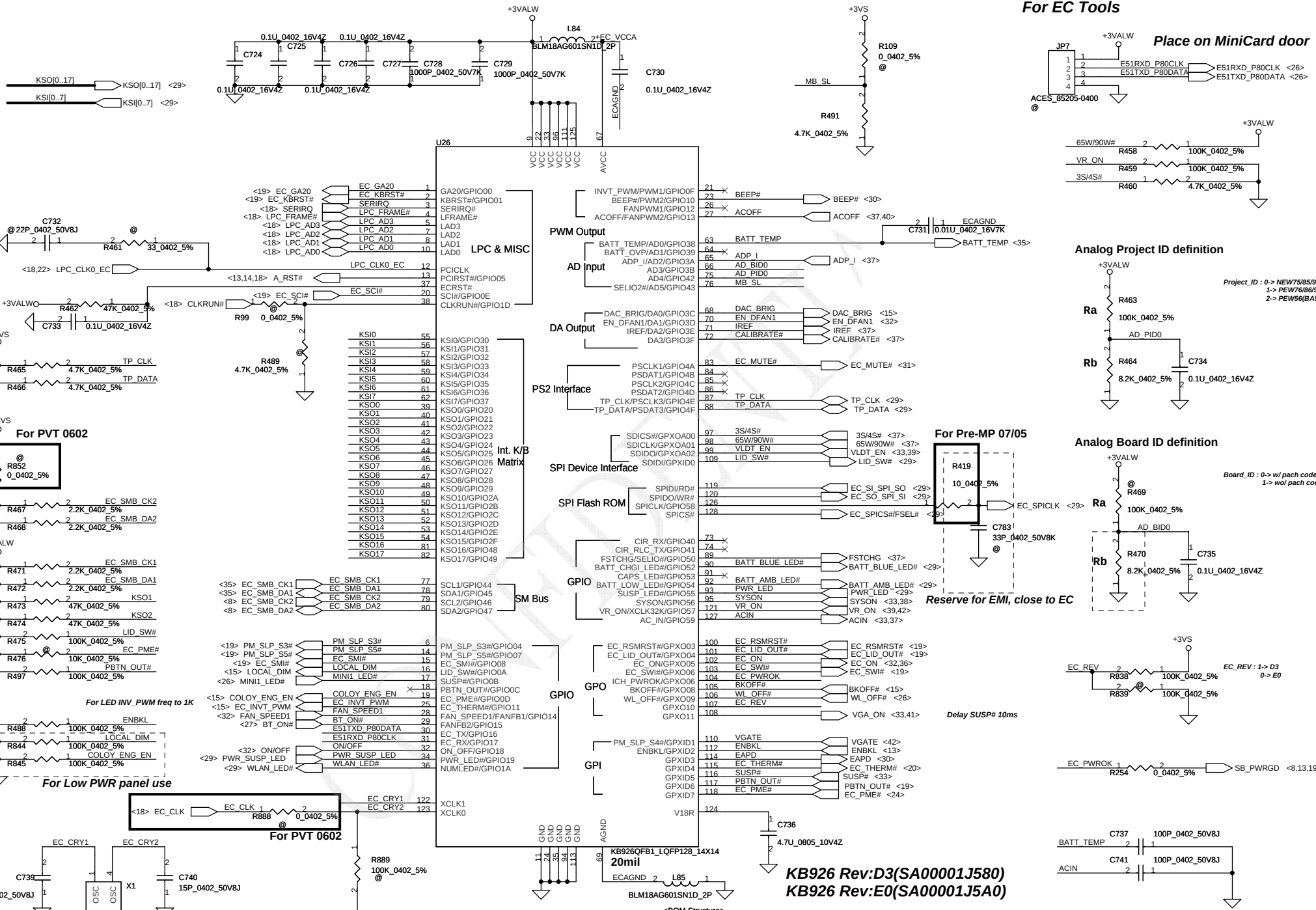
To USB/B Connector



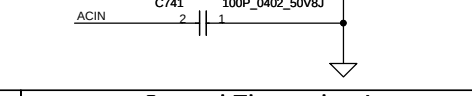
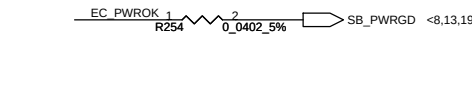
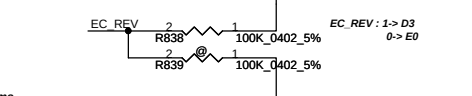
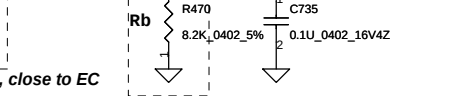
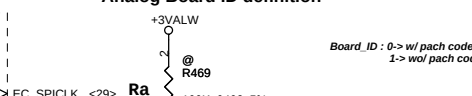
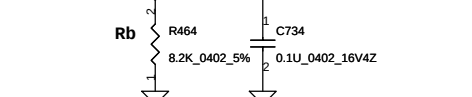
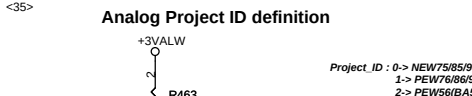
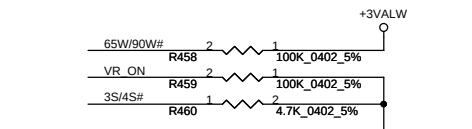
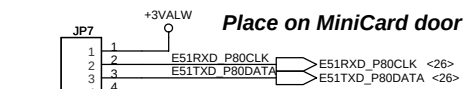
Bluetooth Conn.



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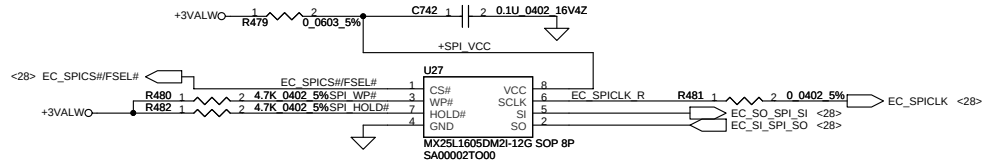


For EC Tools

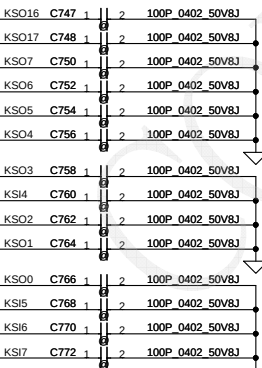
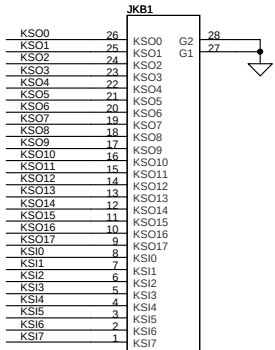


KB926 Rev:D3(SA00001J580)
KB926 Rev:E0(SA00001J5A0)

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						Document Number			
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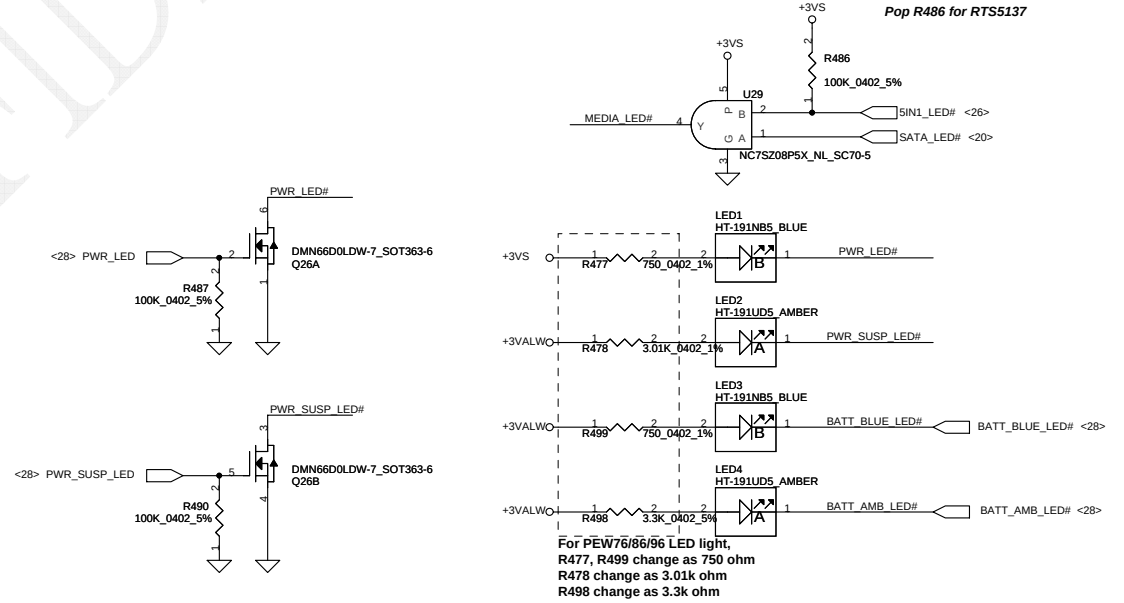
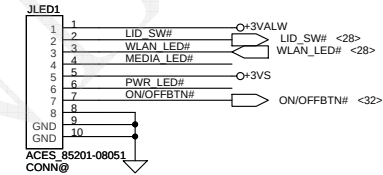
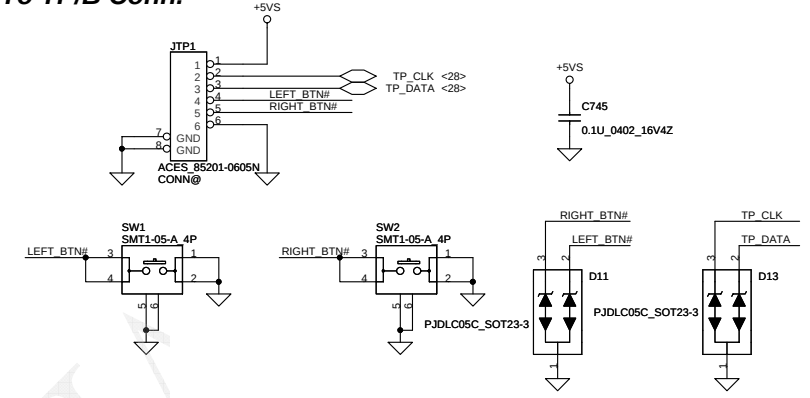


INT_KBD Conn.

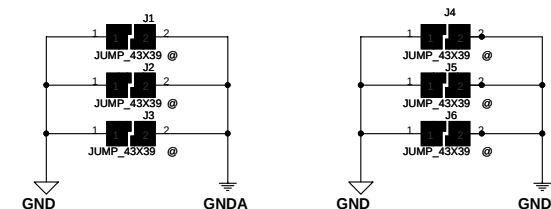


For PVT 0608 Unpop Cap.

To TP/B Conn.

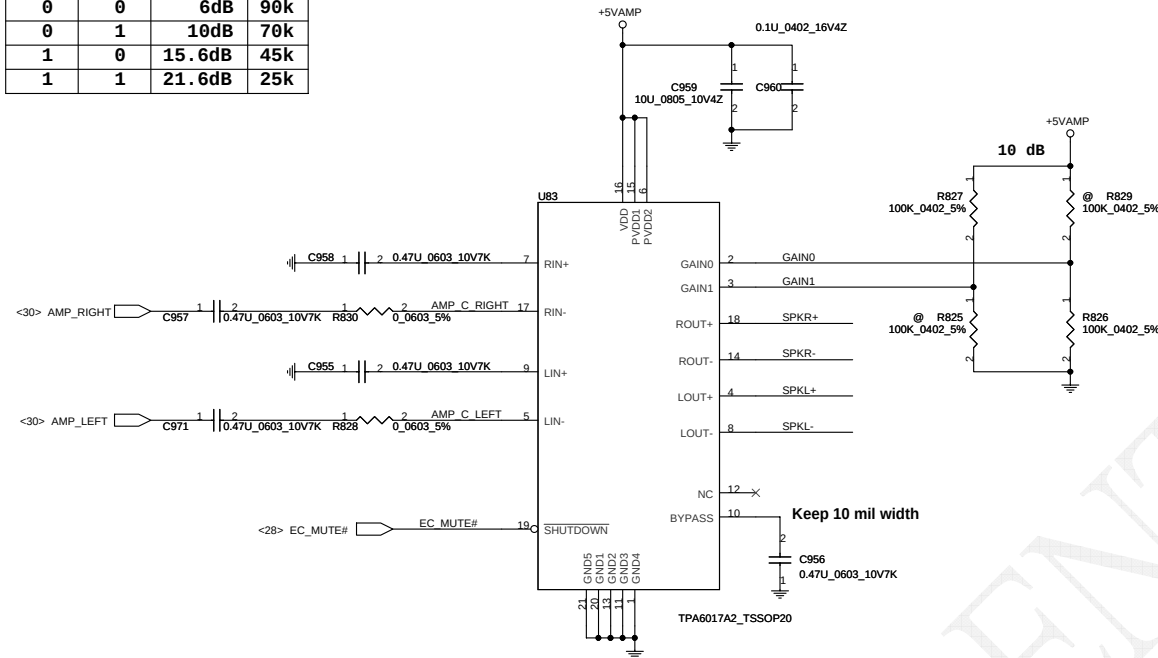


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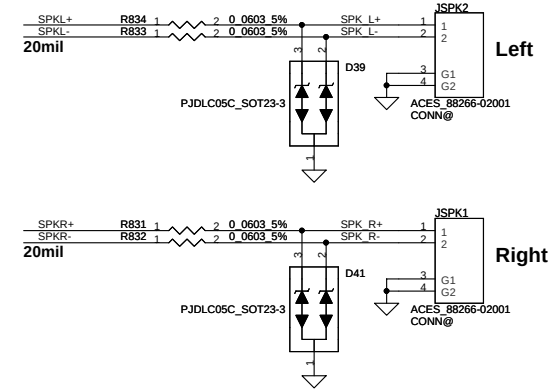


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				HD Audio Codec ALC272X	
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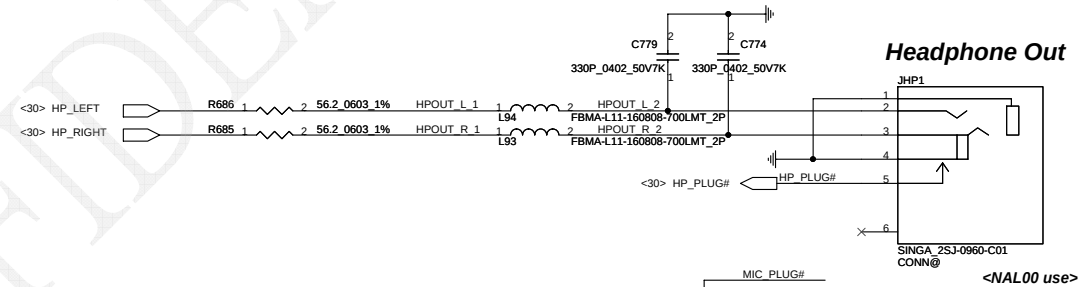
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0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



Int. Speaker Conn.

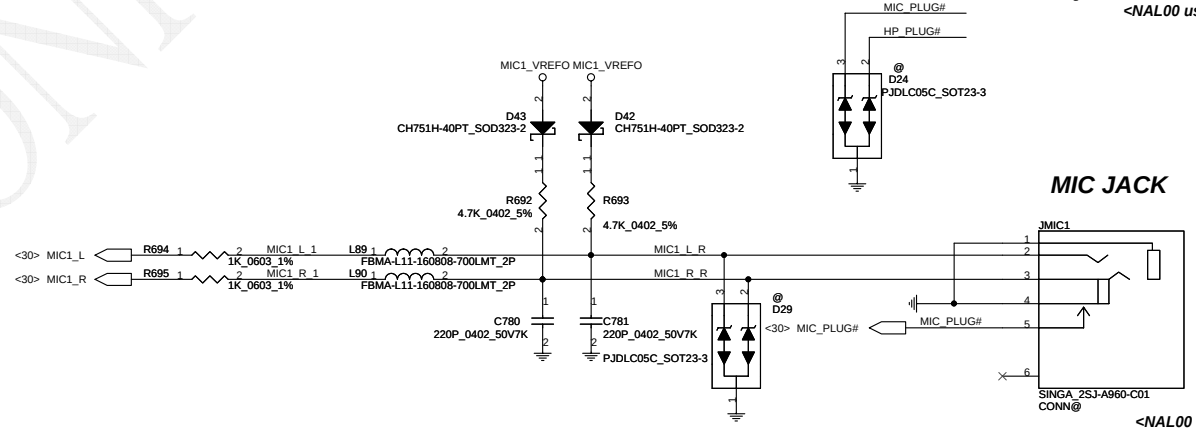


Headphone Out



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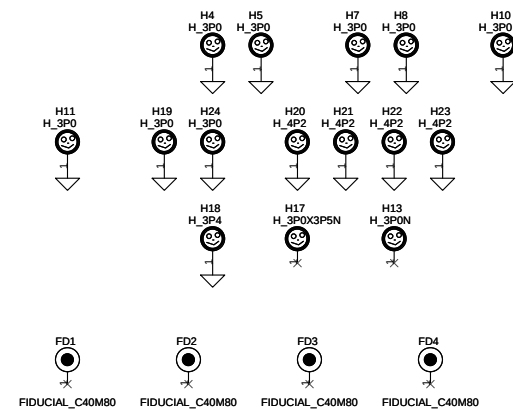
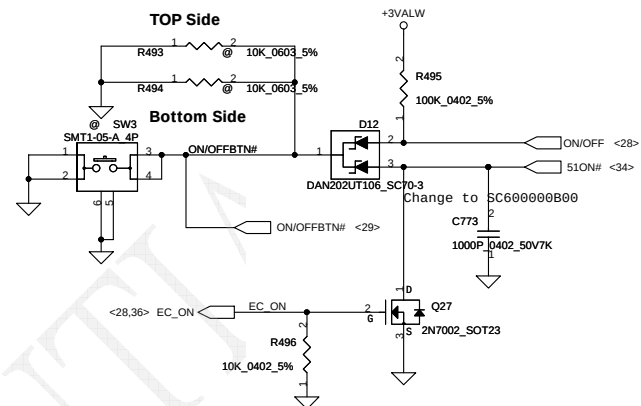
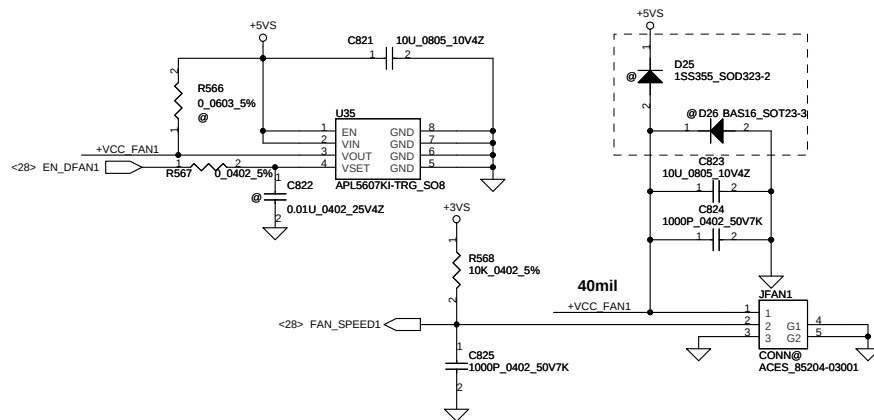
MIC JACK



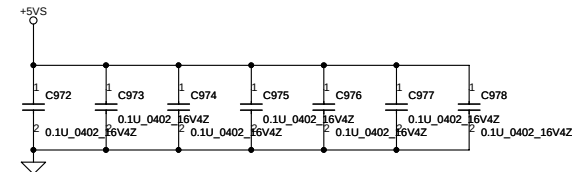
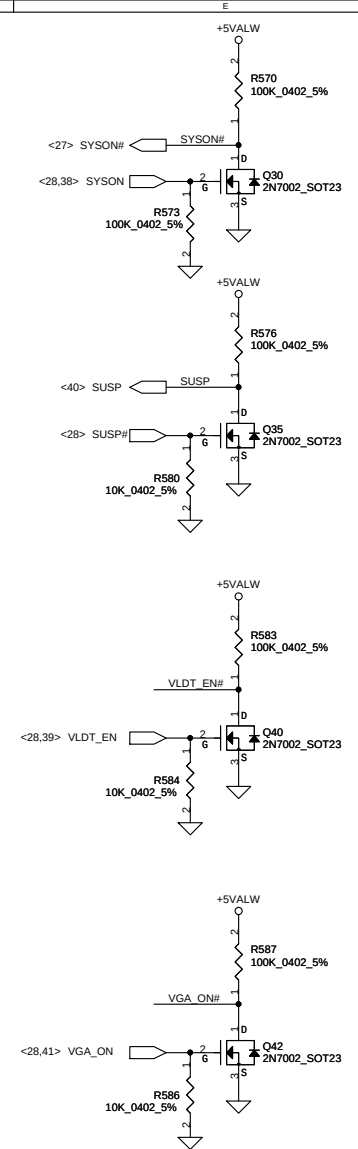
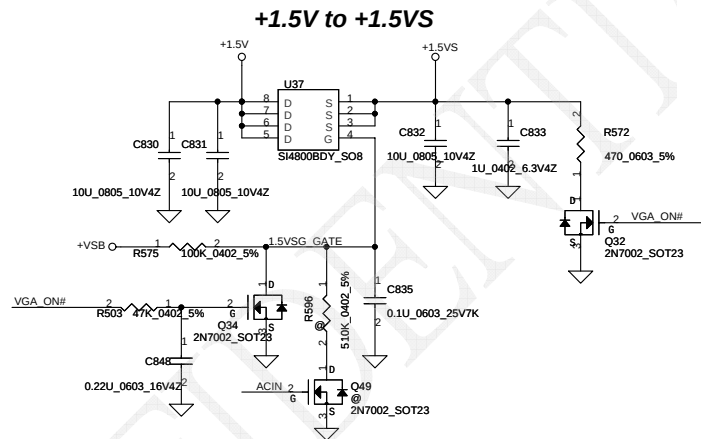
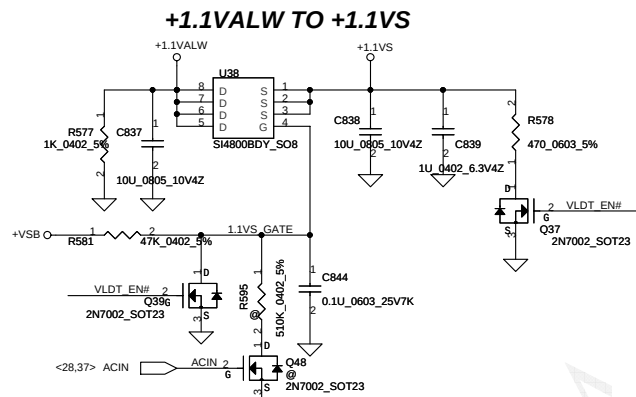
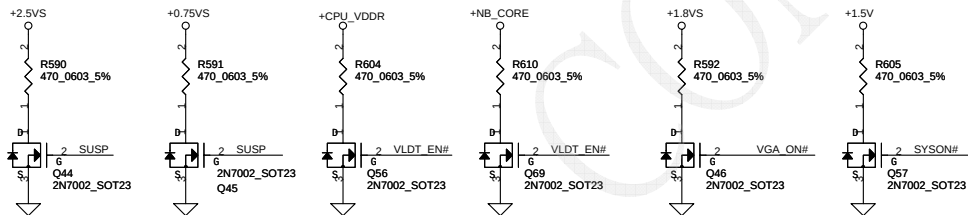
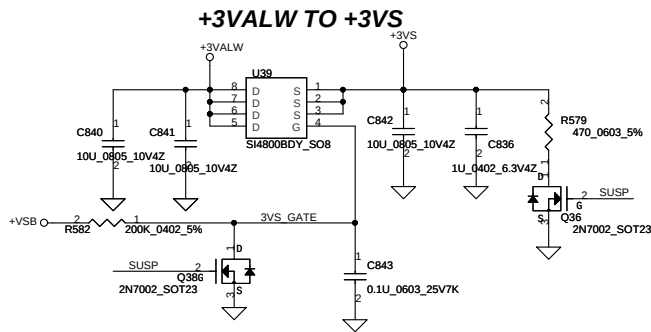
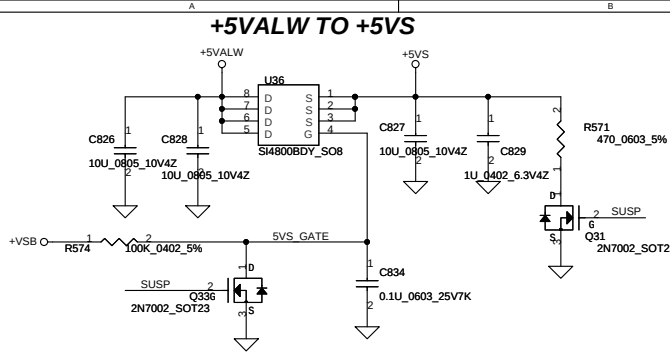
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ON/OFF switch **Power Button**



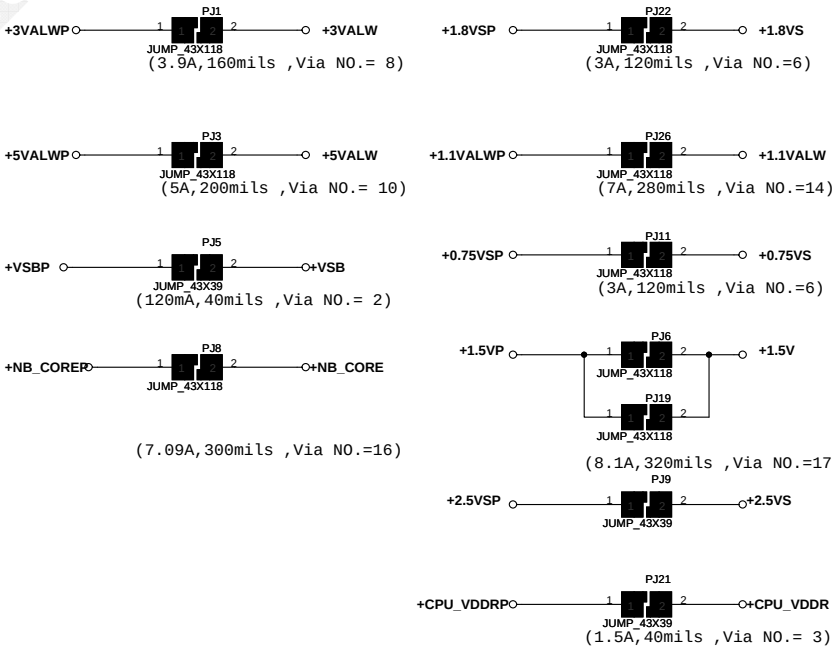
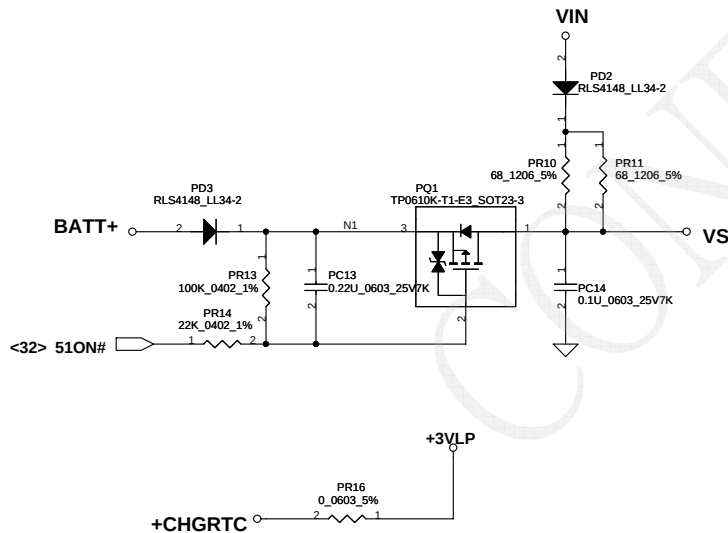
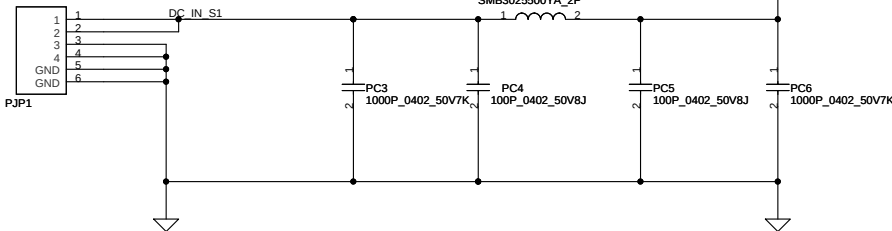
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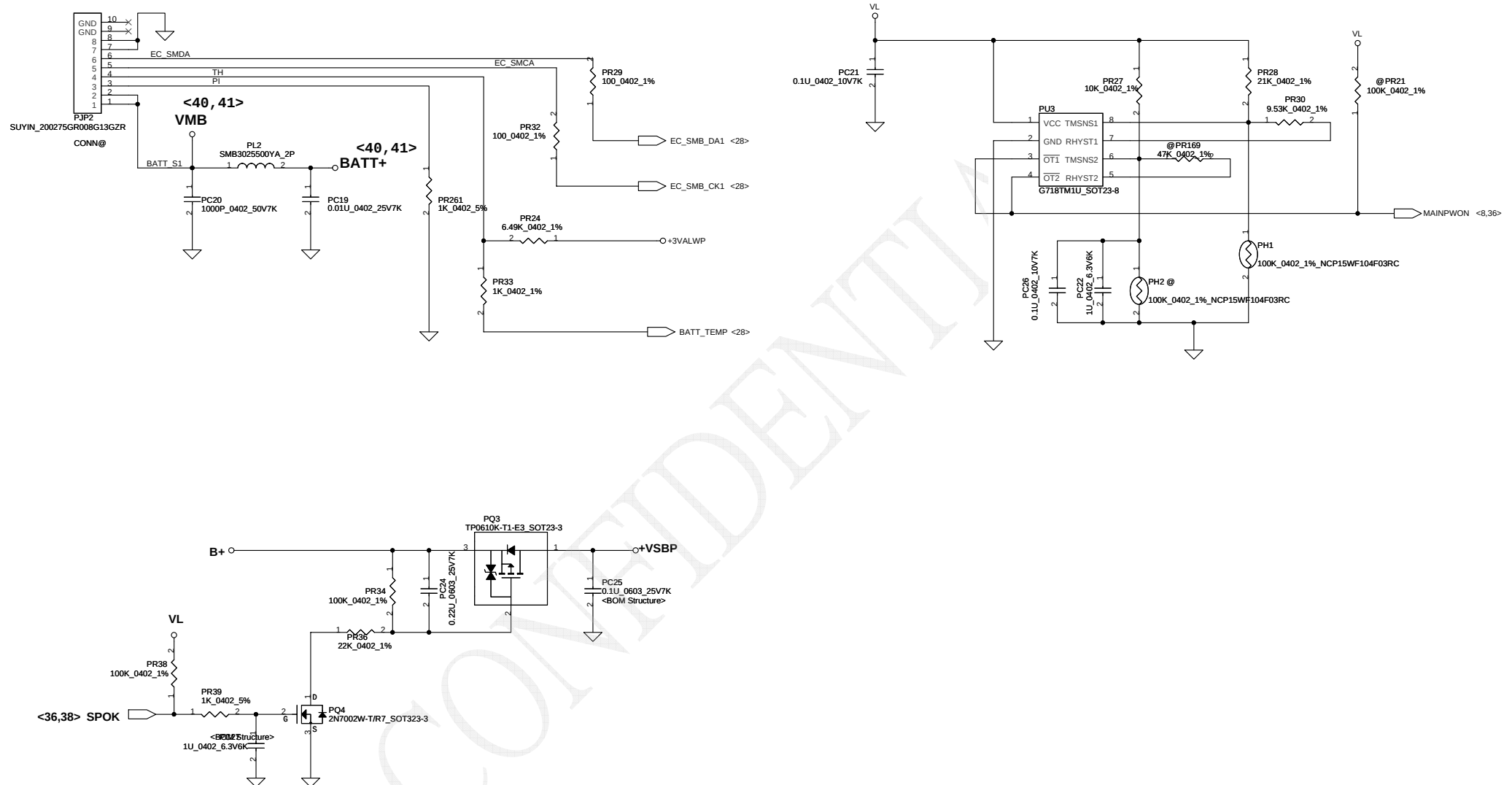
DC-IN cable: DC301009W00 (Yellow)

SP02000GC00
ACES_90305-00441-001



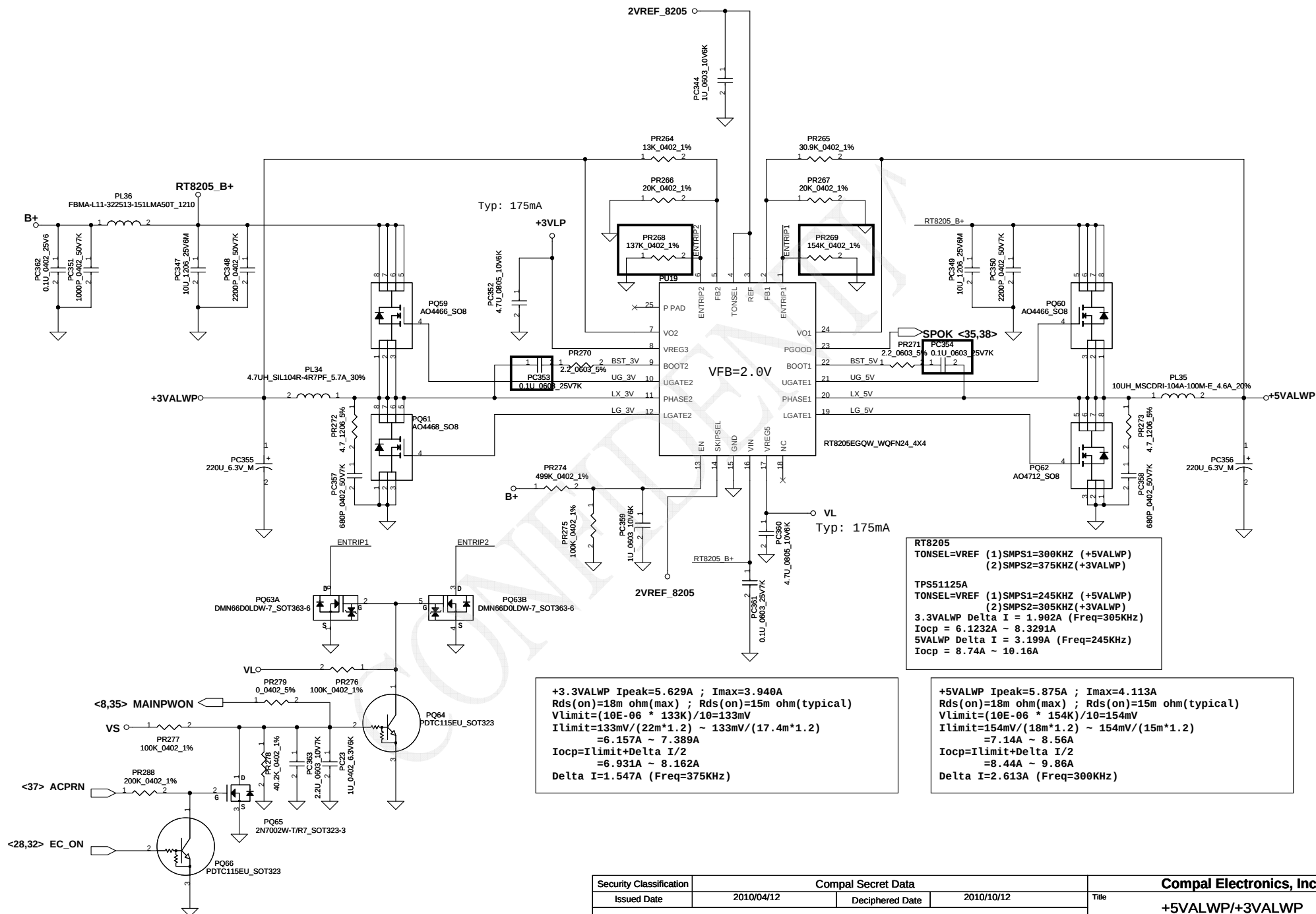
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PH1 under CPU bottom side : Not SPEC, reference only!
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

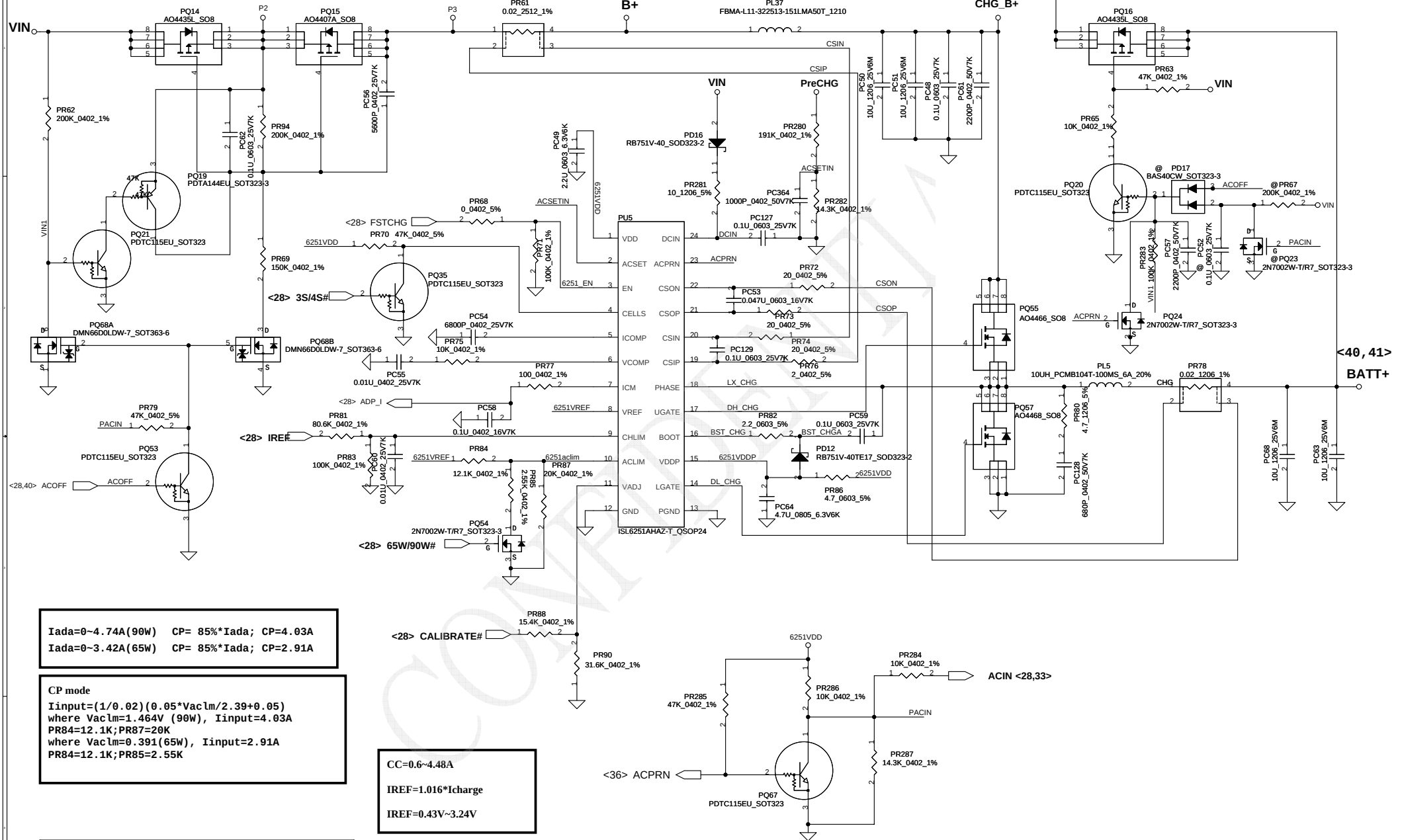


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Iada=0~3.42A(65W/19V=3.421A)
Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85*Iada ; CP = 2.91A
CP = 85*Iada ; CP = 4.07A



Iada=0~4.74A(90W) CP= 85*Iada; CP=4.03A
Iada=0~3.42A(65W) CP= 85*Iada; CP=2.91A

CP mode
Iinput=(1/0.02)(0.05*Vacm/2.39+0.05)
where Vacm=1.464V (90W), Iinput=4.03A
PR84=12.1K;PR87=20K
where Vacm=0.391(65W), Iinput=2.91A
PR84=12.1K;PR85=2.55K

CC=0.6~4.48A

IREF=1.016*Icharge

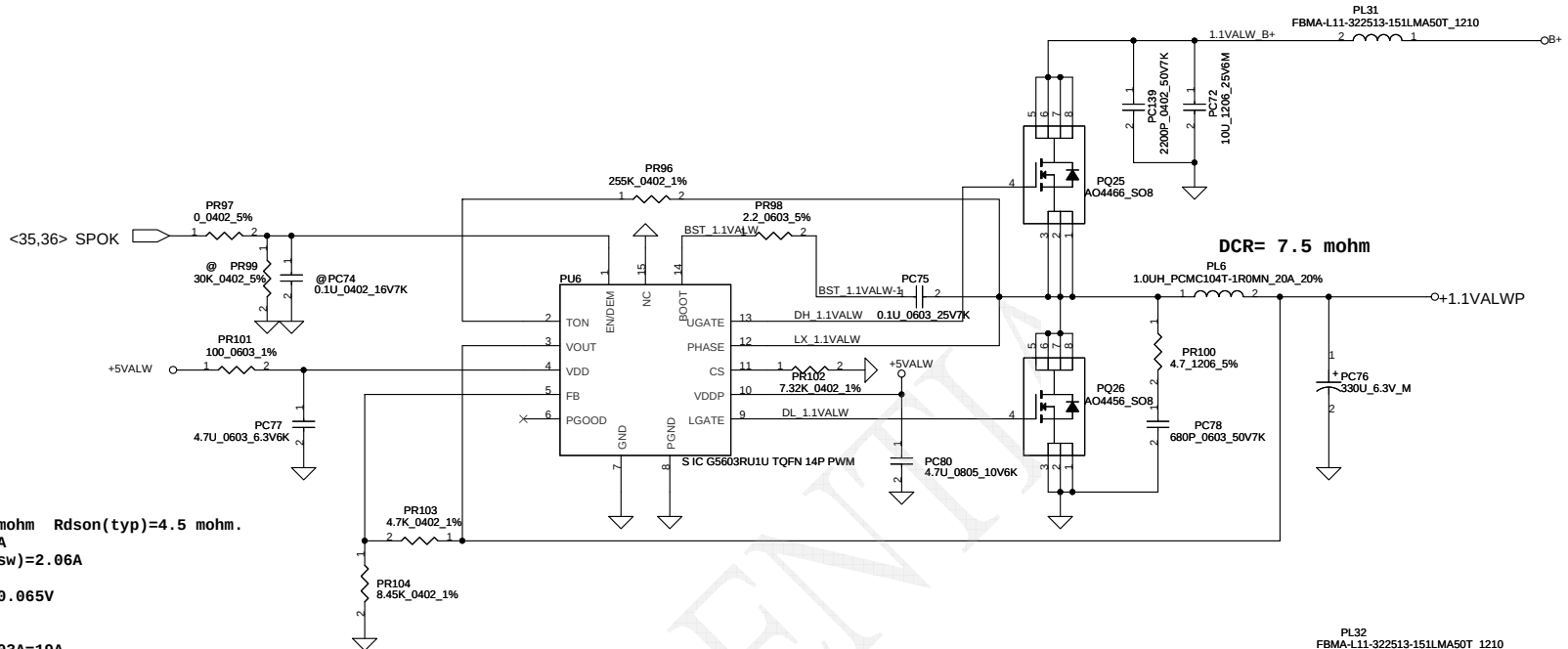
IREF=0.43V~3.24V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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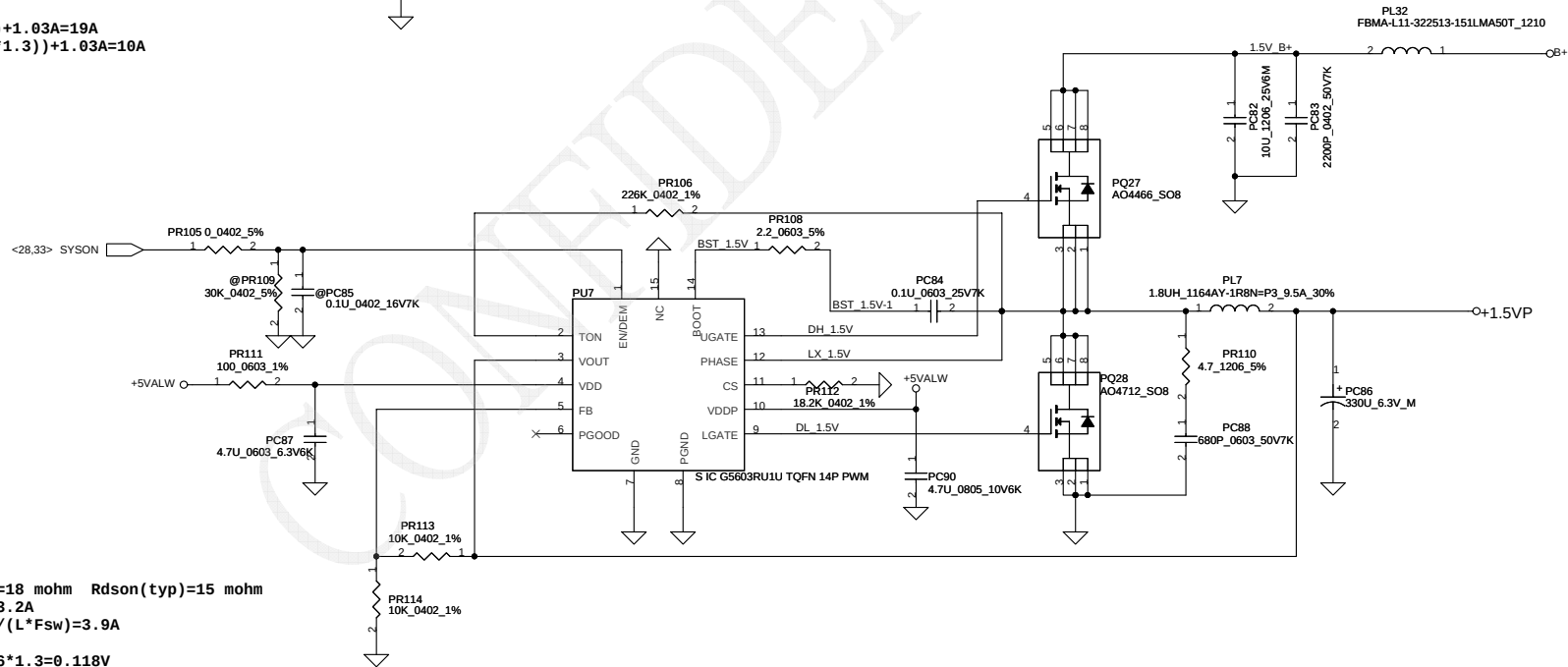
<Vo=1.1V> VFB=0.75V
 $V=0.75*(1+4.7K/10K)=1.1V$
 $Fsw=280KHz$

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
 $I_{peak}=7.42A$, $I_{max}=5.2A$, $I_{ocp}=8.9A$
 $\Delta I=((19-1.1)*(1.1/19))/(L*Fsw)=2.06A$
 $\Rightarrow 1/2\Delta I=1.03A$
 $V_{tripmax}=I_{ocp}*R_{dson}=8.9*5.6*1.3=0.065V$
 $R_{cs}=V_{trip}/9uA=0.065V/9uA=7.2K$
 choose $R_{cs}=7.32K$
 $I_{ocpmax}=(7.32K*11uA)/0.0045+1.03A=19A$
 $I_{ocpmin}=(7.32K*9uA)/(0.0056*1.3)+1.03A=10A$
 $I_{ocp}=10A-19A$



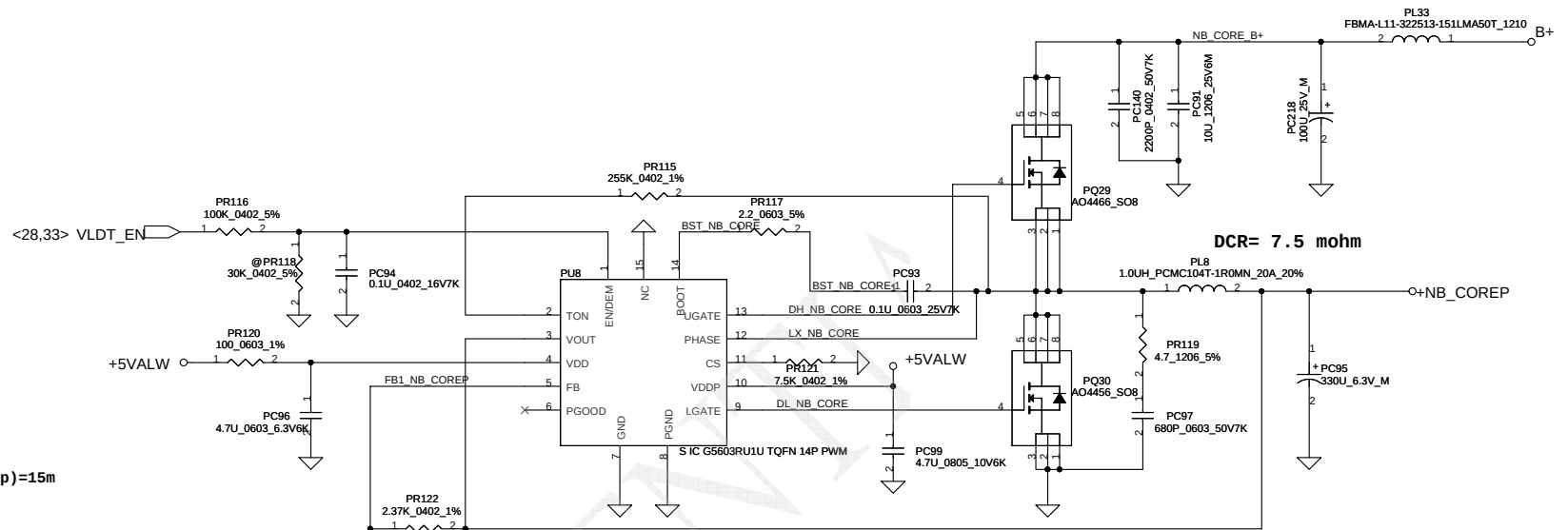
<Vo=1.5V> VFB=0.75V
 $V=0.75*(1+10K/10K)=1.5V$
 $Fsw=335KHz$

Cout ESR=17 mohm Rdson(max)=18 mohm Rdson(typ)=15 mohm
 $I_{peak}=7A$, $I_{max}=8.4A$, $I_{ocp}=13.2A$
 $\Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=3.9A$
 $\Rightarrow 1/2\Delta I=1.95A$
 $V_{tripmax}=I_{ocp}*R_{dson}=16.2*5.6*1.3=0.118V$
 $R_{cs}=V_{trip}/9uA=0.118V/9uA=13.1K$
 choose $R_{cs}=13K$
 $I_{ocpmax}=(13K*11uA)/0.0045+1.95A=32A$
 $I_{ocpmin}=(13K*9uA)/(0.0056*1.3)+1.95A=18A$
 $I_{ocp}=9.94A-13.2A$

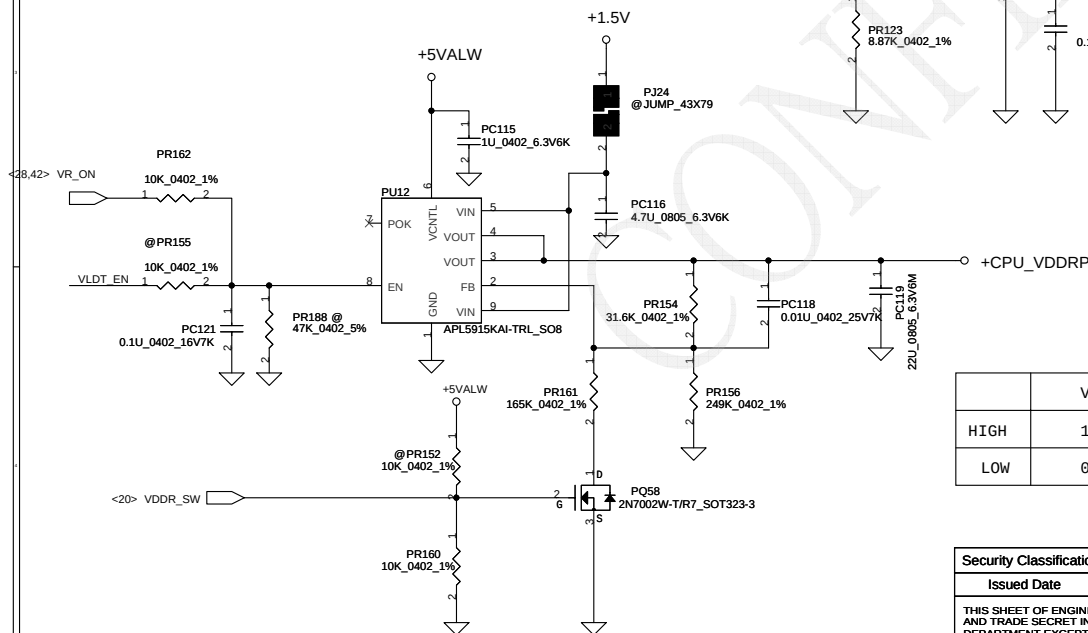


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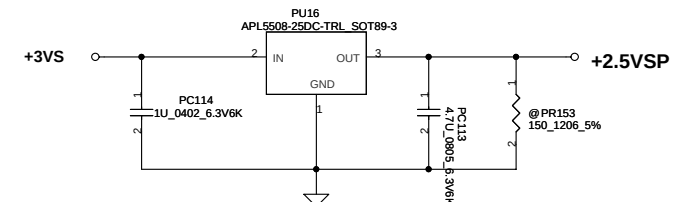
$<V_o=1.1V>$ $V_{FB}=0.75V$
 $V=0.75*(1+4.7K/10K)=1.1V$
 $F_{sw}=280KHz$
 $C_{out} ESR=15m\ ohm$ $R_{dson(max)}=18m$ $R_{dson(typ)}=15m$
 $I_{peak}=7.6A$, $I_{max}=5.4A$, $I_{ocp}=9.2A$
 $\Delta I=((19-1.1)*(1.1/19))/(L*F_{sw})=2.06A$
 $\Rightarrow 1/2\Delta I=1.03A$
 $V_{tripmax}=I_{ocp}*R_{dson}=9.2*5.6*1.3=0.067V$
 $R_{cs}=V_{trip}/9\mu A=0.067V/9\mu A=7.44K$
 choose $R_{cs}=7.5K$
 $I_{ocpmax}=(7.5K*11\mu A)/0.0045+1.03A=19.36A$
 $I_{ocpmin}=(7.5K*9\mu A)/(0.018*1.3)+1.03A=10.3A$
 $I_{ocp}=10.3A\sim 19.36A$

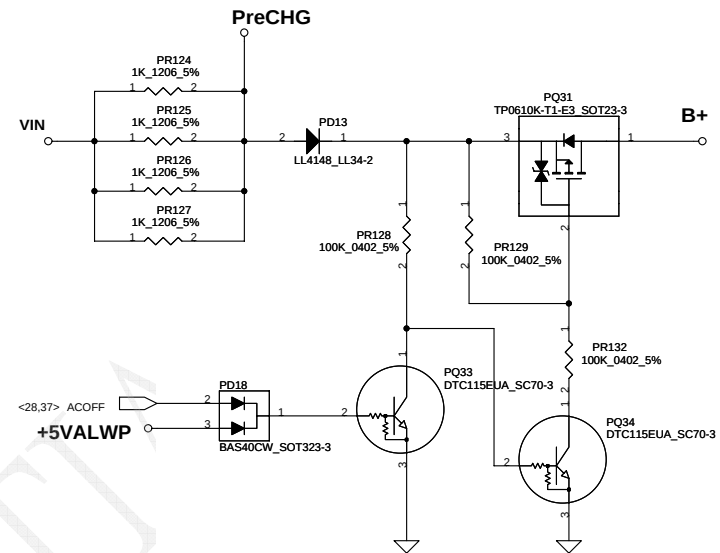
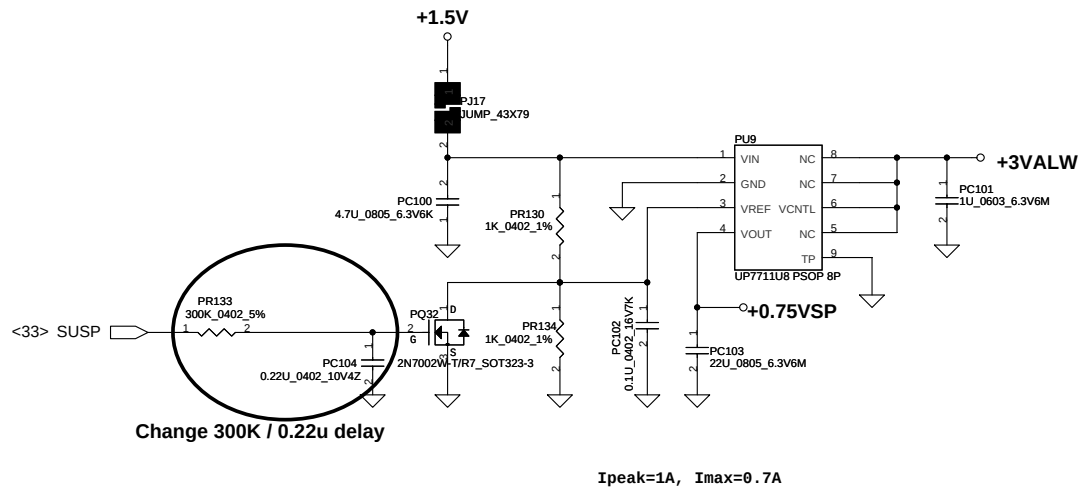


	POWER_SEL
HIGH	0.95V
LOW	1.1V

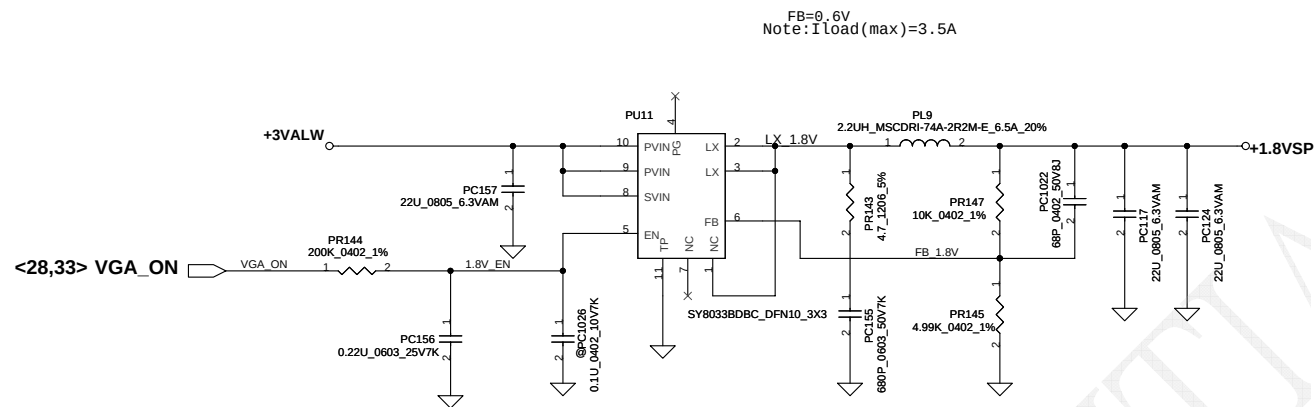


	VDDR_SW
HIGH	1.05V
LOW	0.9V





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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	Modify Pre-charger				Add PR279,PR288,PC57 Change PR285 100K to 47K Change PR287 20K to 14.3K Change PQ67 2N7002 to PDTTC115 Change PR62 47K to 200K Change PR79 22K to 47K Change PR283 0 to 100K	2010 0528	PVT
2	Meet common rule				Change PJ30 to PL36, PJ23 to PL37 Add PC361,PC362	2010 0602	PVT
3	HDMI test fail	5V voltage too low at test termial		36	Change PR265 from 30K to 30.9K	2010 0604	PVT
4	ESD test fail	ESD solution			Add PC22, PC23	2010 0608	PVT
5	EMI test fail	EMI solution			Enable 3V,5V,1.1V,1.5V,NB_CORE,CPU snubber	2010 0608	PVT
6	Power sequence tune			41	Change PR144 from 22K to 200K Change PC156 from 0.47u to 0.22u	2010 0609	PVT
7	Costdown	Costdown		38	Change PQ28 from AO4456 to AO4712 Change PR112 from 13K to 18.2K Change PL7 from 1.0uH to 1.8uH Change PQ61 from AO4712 to AO4468	2010 0617	PVT
8					PR268 from 133K to 137K PQ57 from AO4466 to AO4468		
9	For DDR voltage default/HW YC	DDR 2 need 0.9V, DDR 3 need 1.05V But DDR2 voltage is critical then DDR 3		39	Disable PR152 Enable PR160	2010 0705	Pre MP
10	Aprove 200MHz~220MHz/EMI Chris	EMI solution		37	Enable PR80, PC128 Change PR82 from 0 to 2.2	2010 0705	Pre MP
11	Add a bypass path/ESD Chris	ESD solution		35	Add PC26 near PC22	2010 0705	Pre MP
12							
13							
14							
15							
16							

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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1							
2							
3							
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5							
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7							
8							
9							
10							
11							
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16							

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05/10 First release

- 1. Change Cardreader chip (RTS5137/RTS5138)
- 2. ODD used to ODD sub/b
- 3. RTC Battery change (w/o charge)

06/11 PVT

- 1. P.28 Reserve R889 For EC_CLK, pop R851, unpop R852 For EC_SMBus leakage
- 2. P.26 Remove R853
- 3. P.28 project ID-->1 Board ID -->1, unstuff KSI, KSO Cap.
- 4. P.8 Change R41 as 31.6k ohm and R42 as 30k ohm for TSI

07/05 Pre-MP

- 1. P.19 Reserve R890 For MEM_1V5
- 2. P.28 Change R419 as 10 ohm For EMI

07/20

- 1. P.29 Change R477, R499 as 750 ohm; change R478 as 3.01k ohm; change R498 as 3.3k ohm for LED light

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