

PWWAA

De1hi

LA-6847P REV 1.0 Schematic

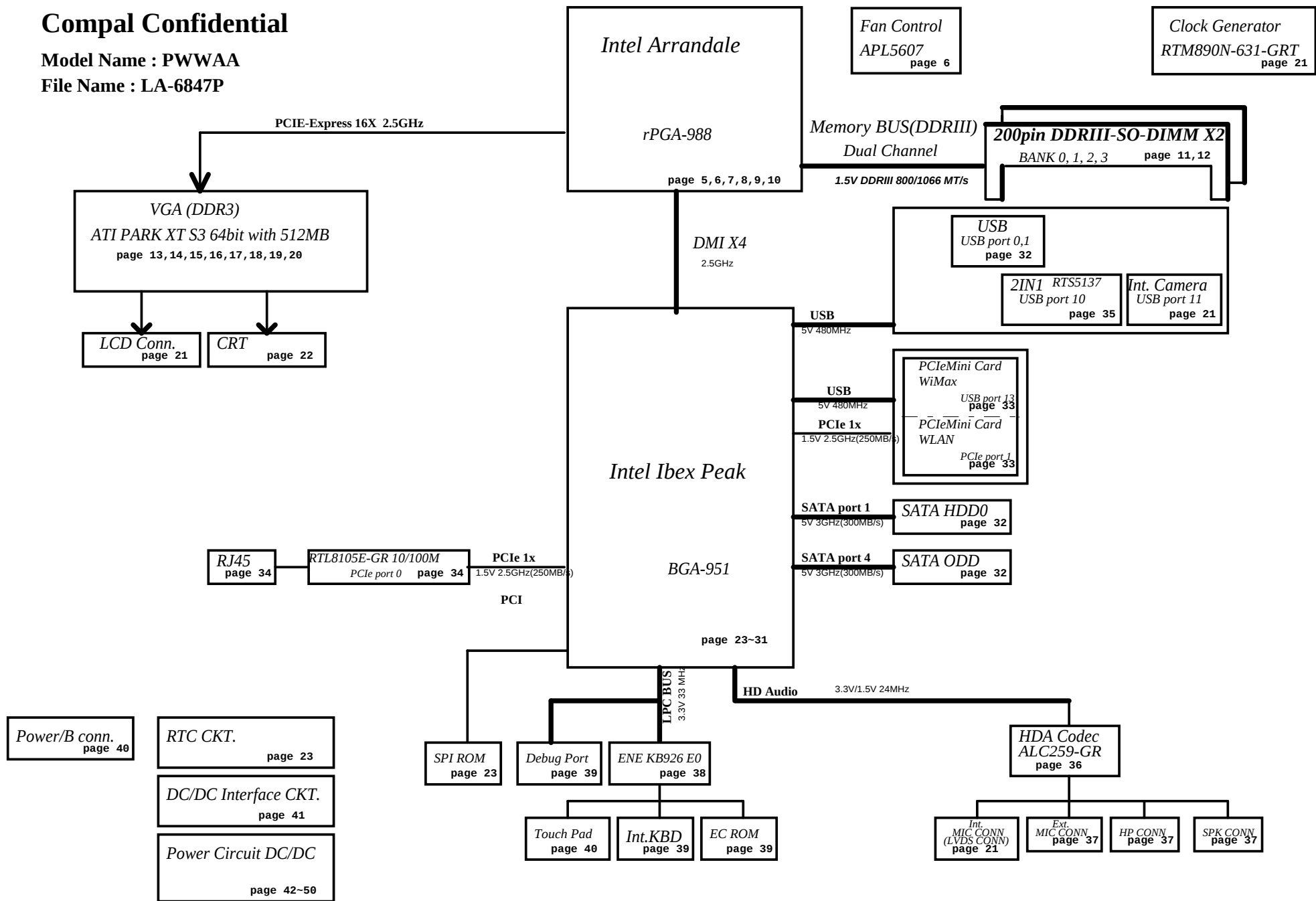
**Intel Processor(ARD) /PCH(HM55)
2010-10-07 Rev 1.0**

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Issued Date	2010/09/05	Deciphered Date	2011/09/05	Title	SCHEMATICS,MB A6847
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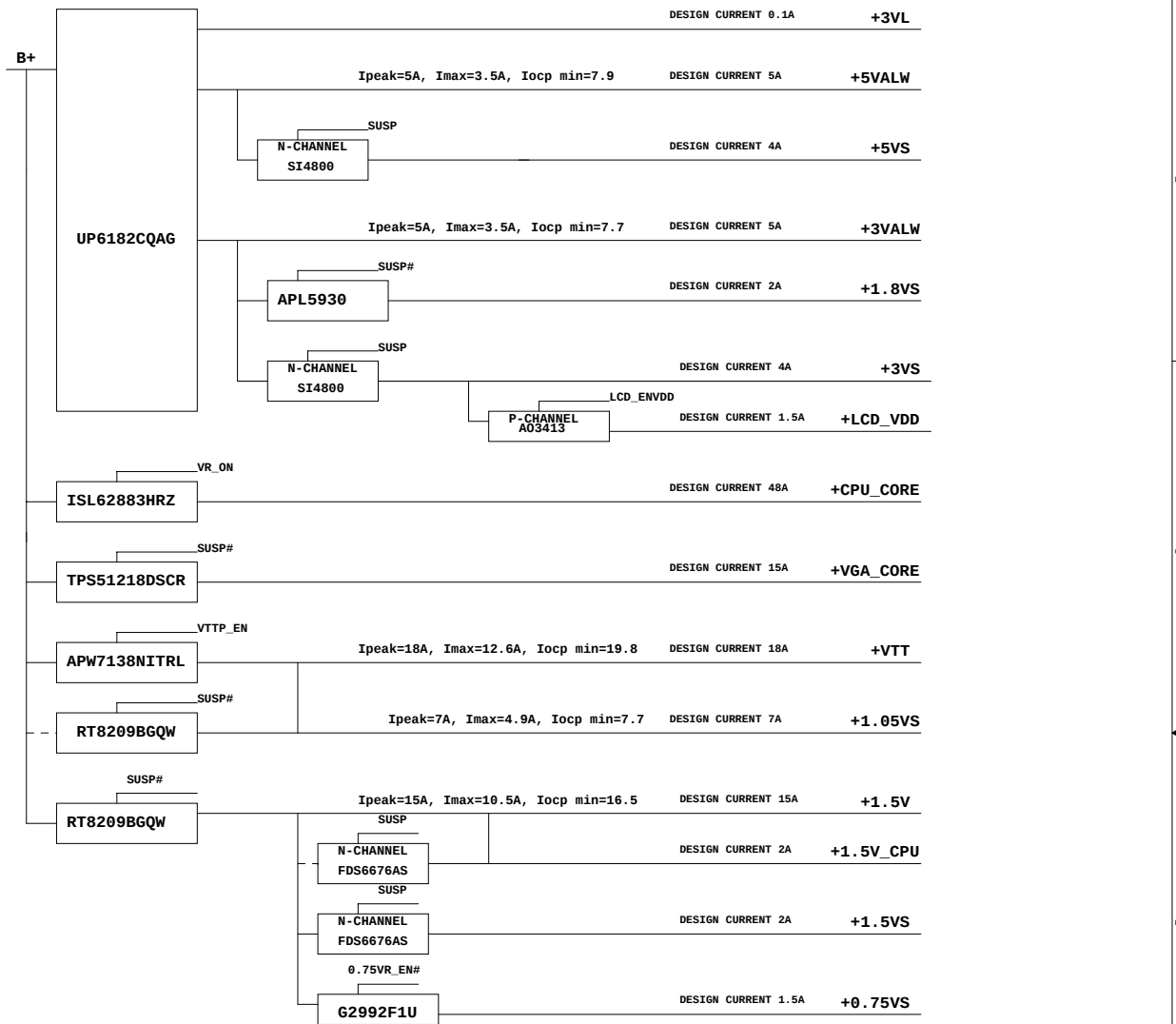
Compal Confidential

Model Name : PWWAA

File Name : LA-6847P



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power plane State	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

Function	MINI PCI-E SLOT			LAN					
description			SLOT1	LAN					
explain			WLAN/BT	10/100M					
BTO									

Function				Camera & Mic				
description				Camera & Mic				
explain				Camera & Mic				
BTO				CAM@				

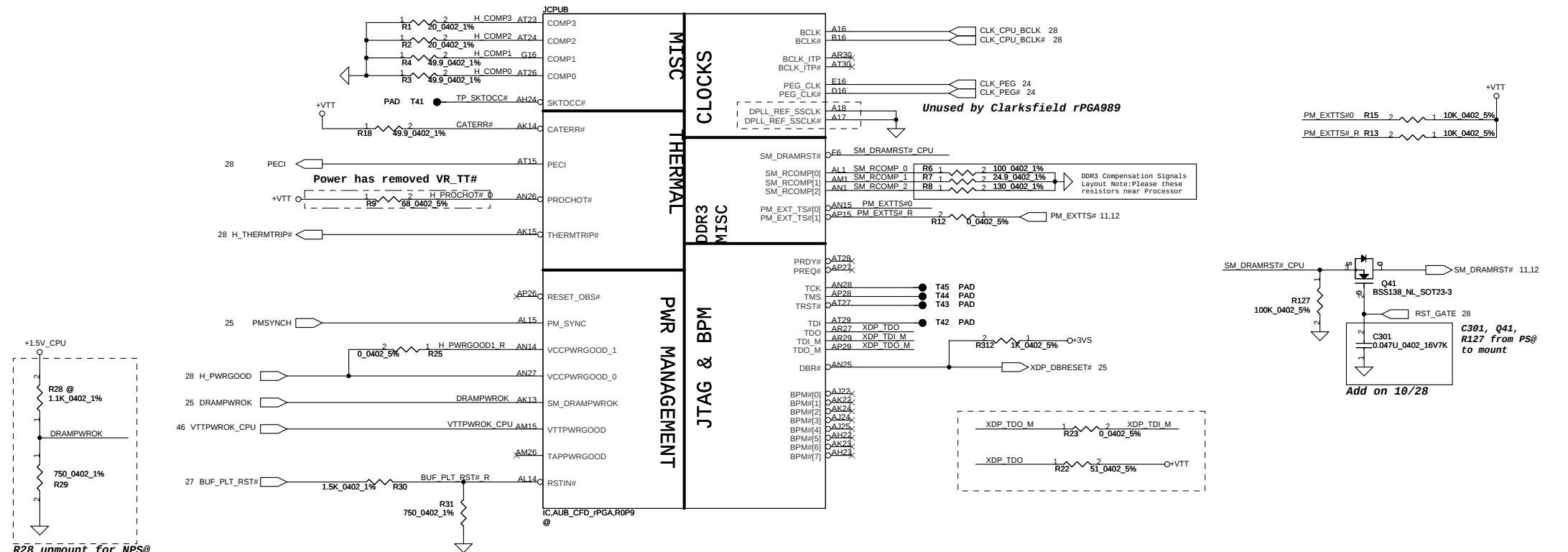
Function	S3 Power Saving		
description	S3 Power Saving		
explain		Power Saving	
BTO			

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

EC SM Bus1 Address				EC SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
Power	Device	HEX	Address				

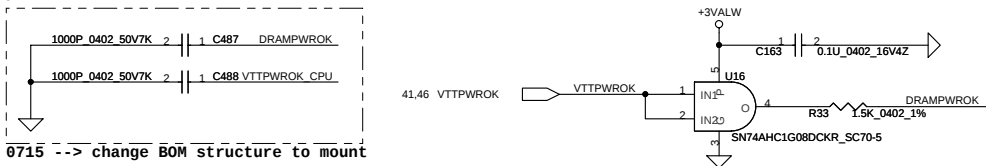
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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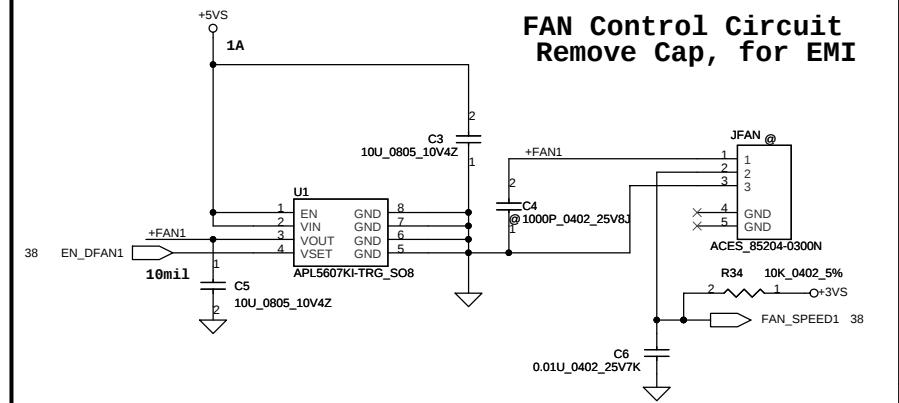
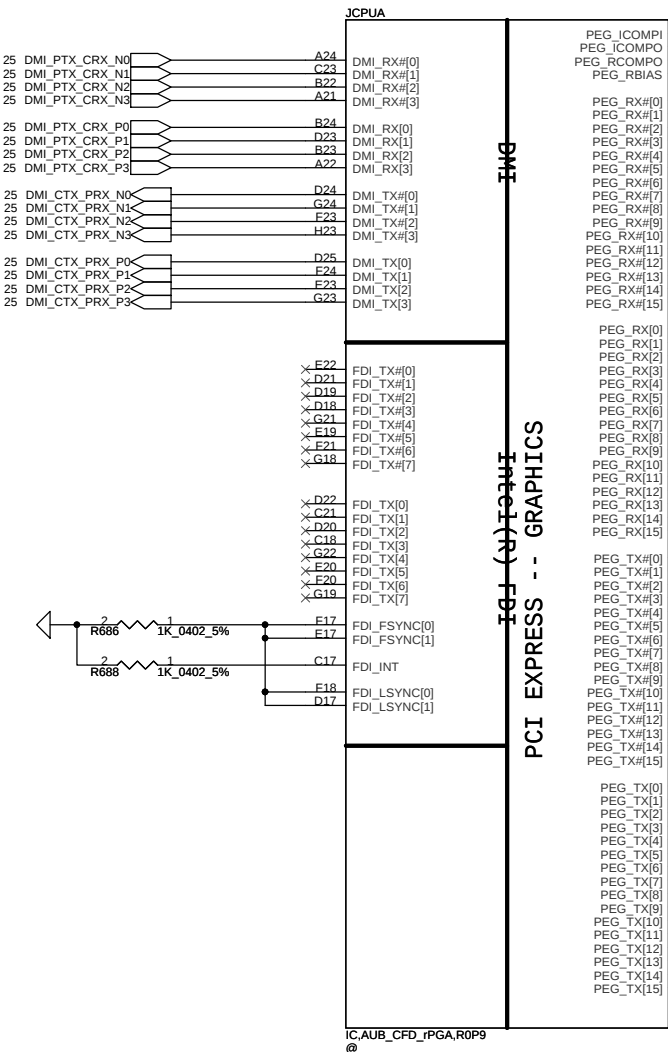


For S3 CPU Power Saving

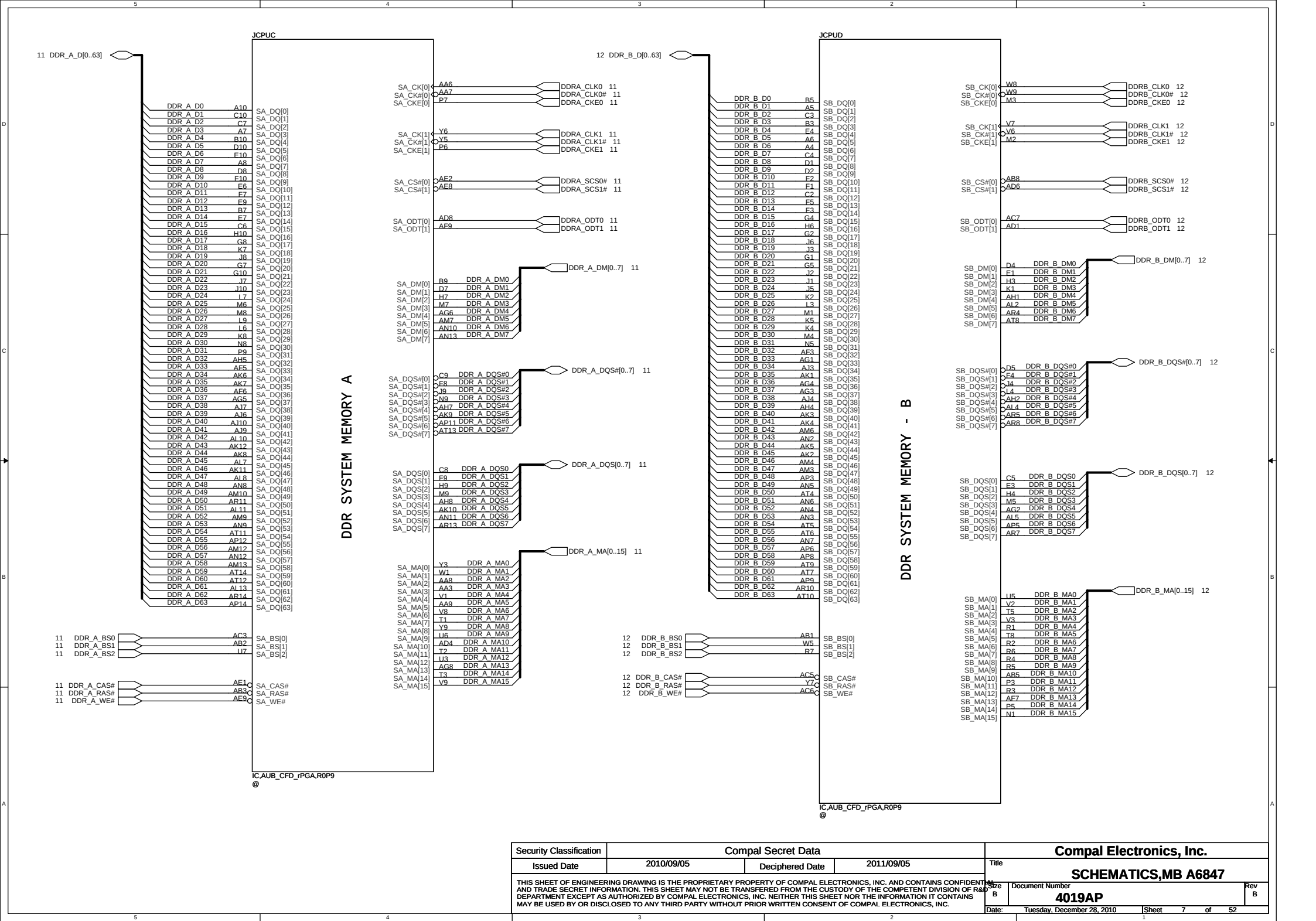
place near JCPU

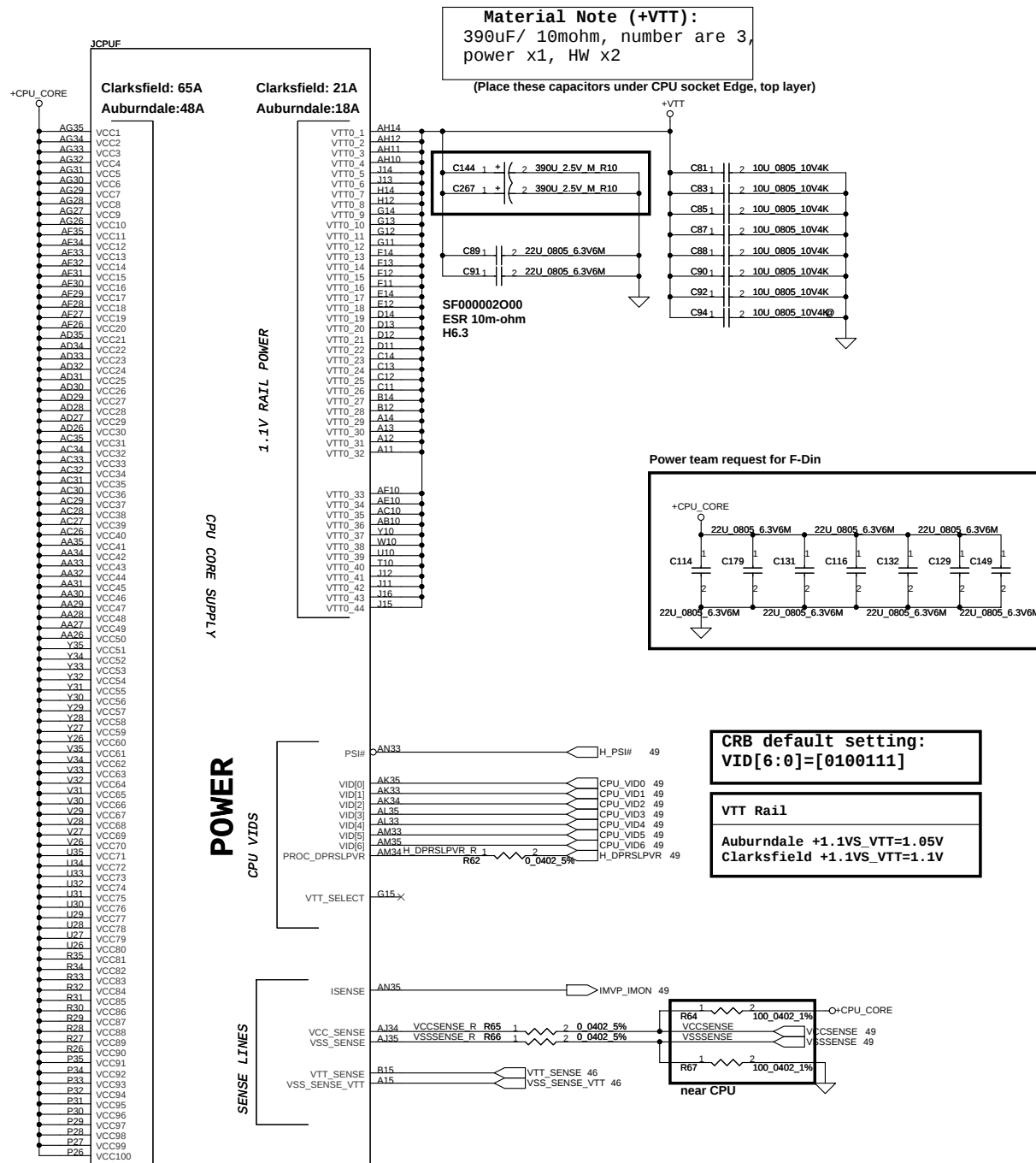


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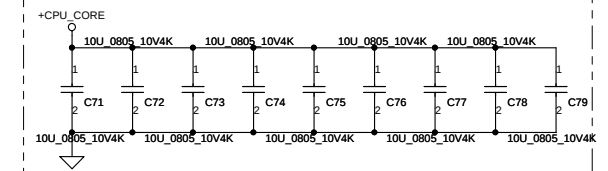


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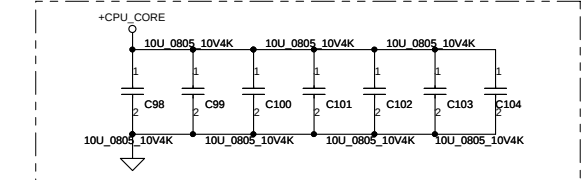




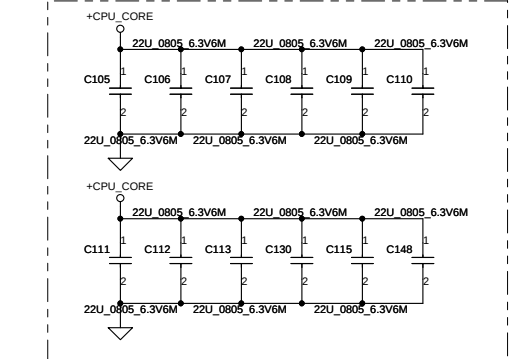
(Place these capacitors between inductor and socket on Bottom)



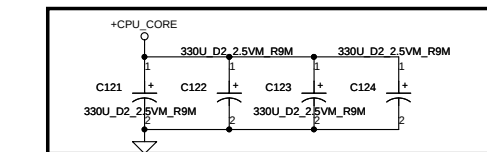
(Place these capacitors under CPU socket, top layer)



(Place these capacitors on CPU cavity, Bottom Layer)

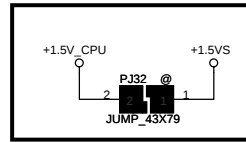


TOP side (under inductor)

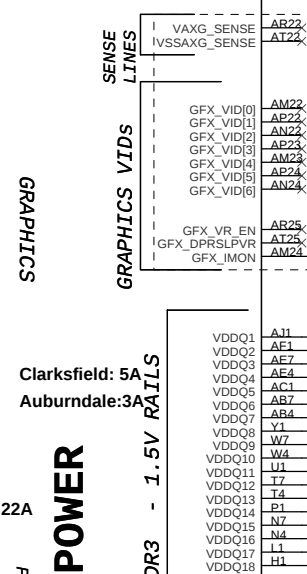
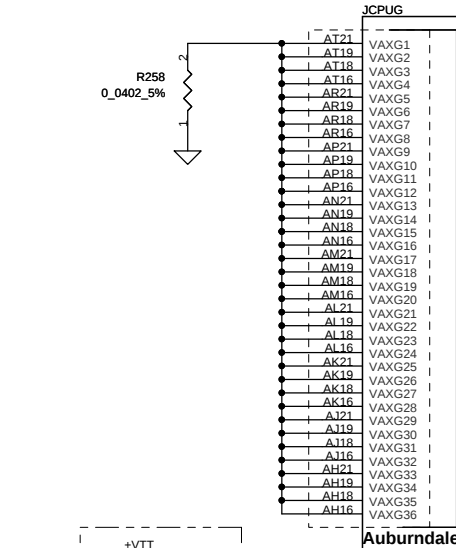
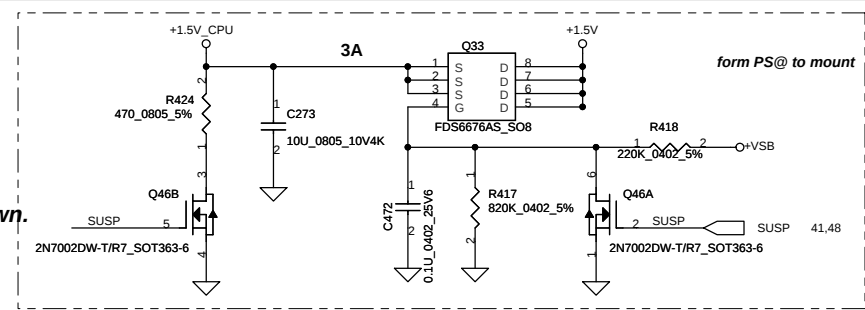


Check list:

+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF
+VTT: 4x 330uF, 7x 22uF, 8x 10uF



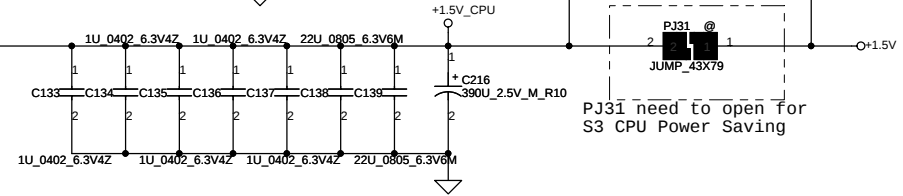
7/22 modified for cost down.



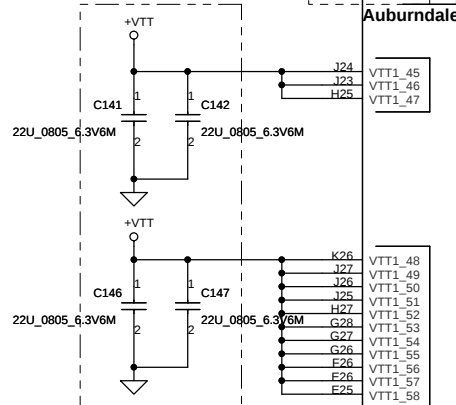
Clarksfield: 5A
Auburndale: 3A

POWER

DDR3 - 1.5V RAILS



remove PJ30
PJ31 need to open for S3 CPU Power Saving



(Place these capacitors under CPU socket, top layer)

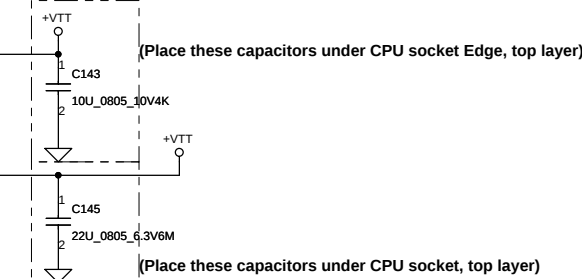
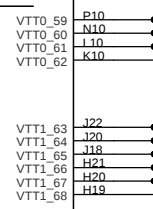
Clarksfield: 21A
Auburndale: 18A

PEG & DMI

1.1V

1.8V

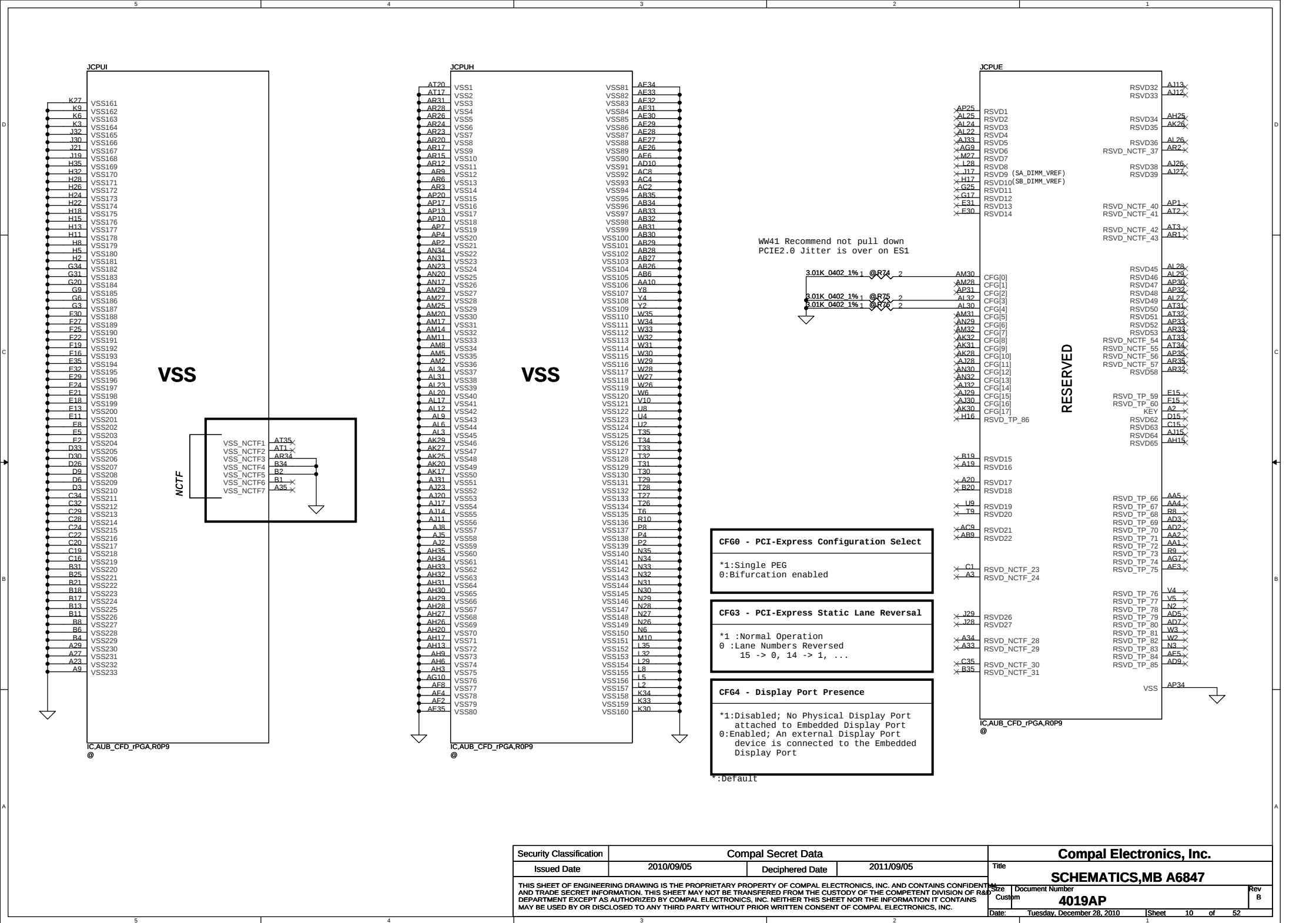
Clarksfield: 0.6A
Auburndale: 1.35A



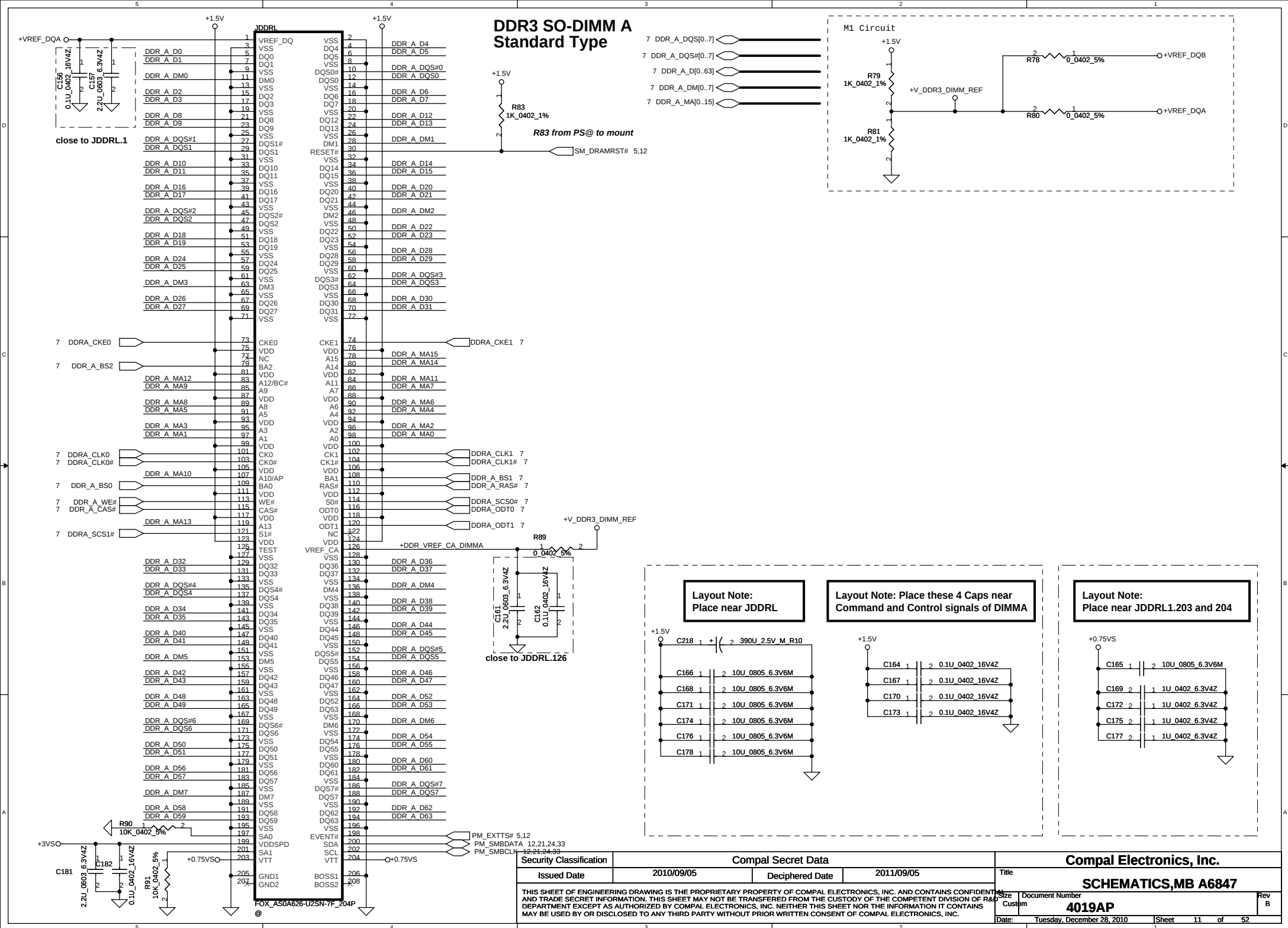
(Place these capacitors under CPU socket Edge, top layer)

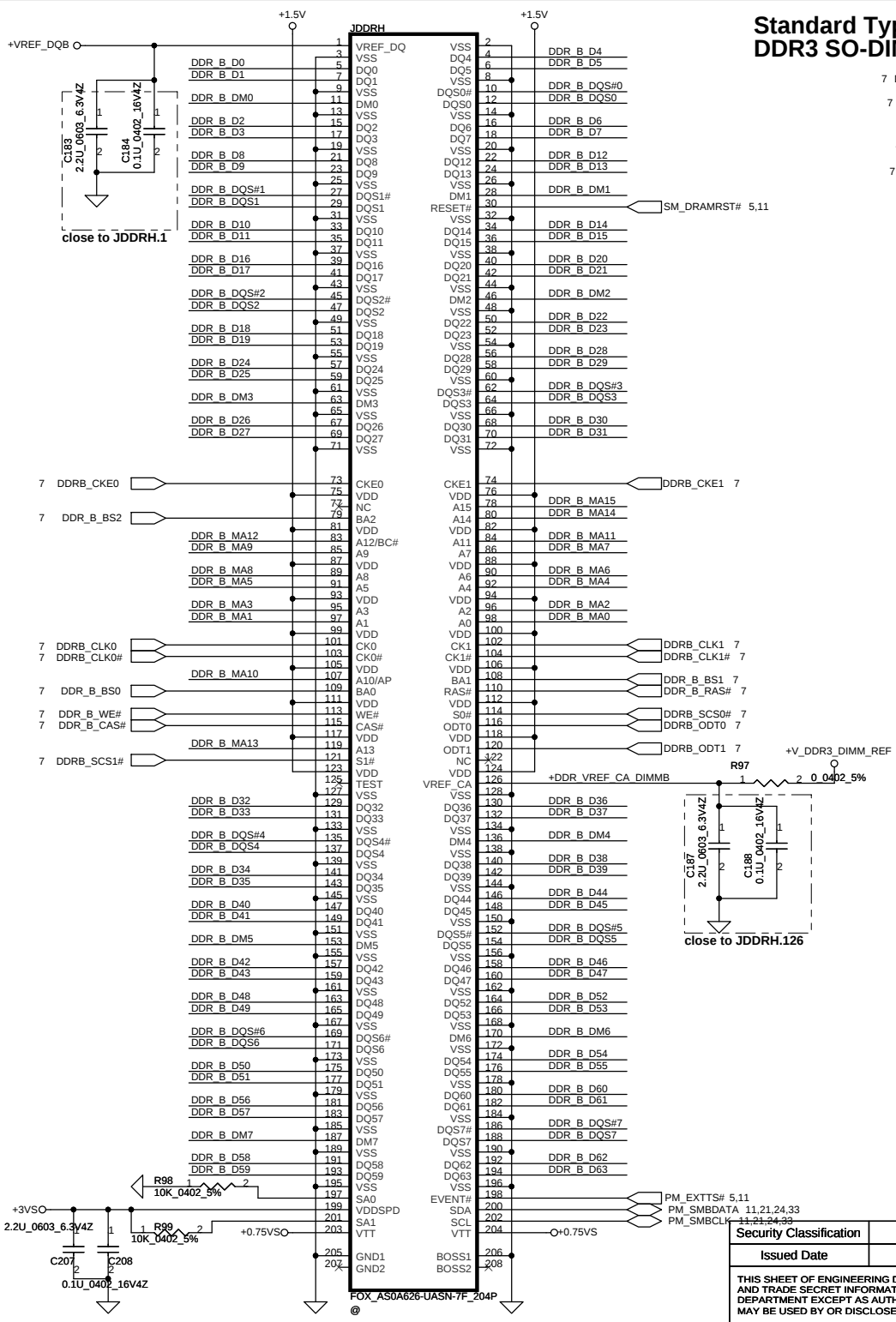
(Place these capacitors under CPU socket, top layer)

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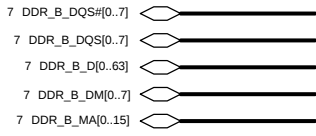


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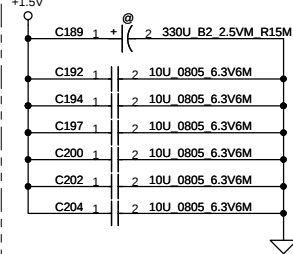




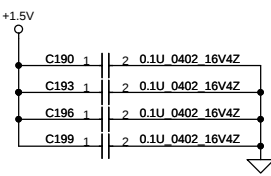
Standard Type DDR3 SO-DIMM B



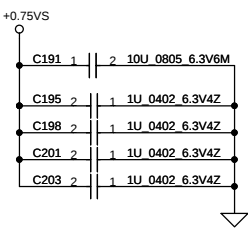
Layout Note:
Place near JDDRH



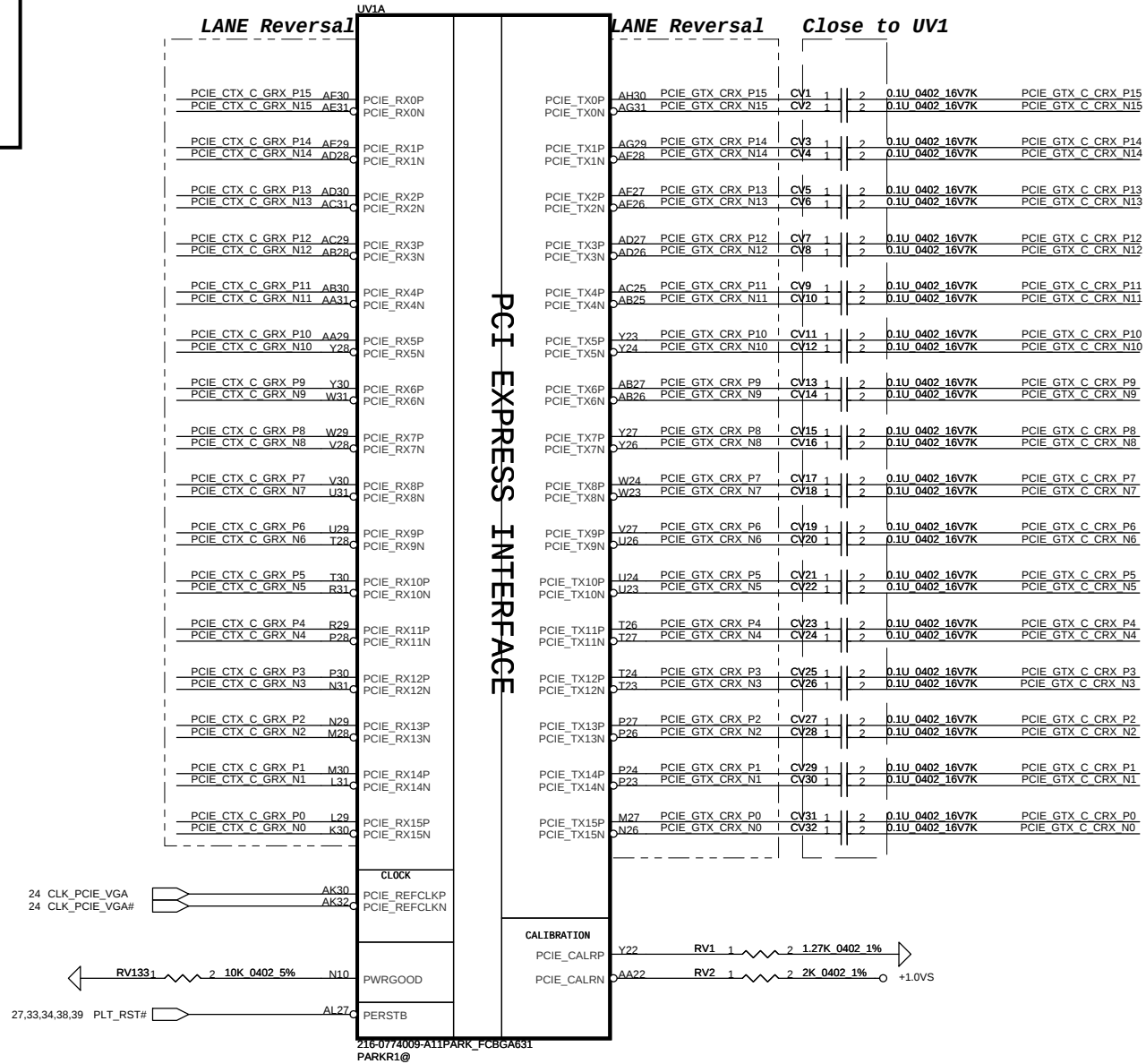
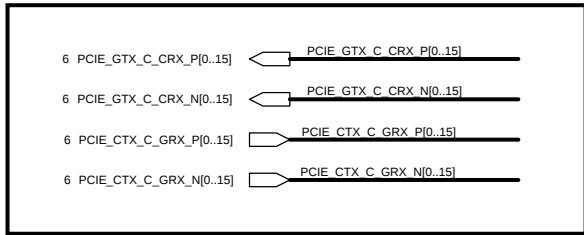
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB



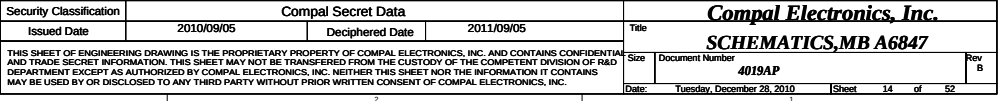
Layout Note:
Place near JDDRH.203 and 204

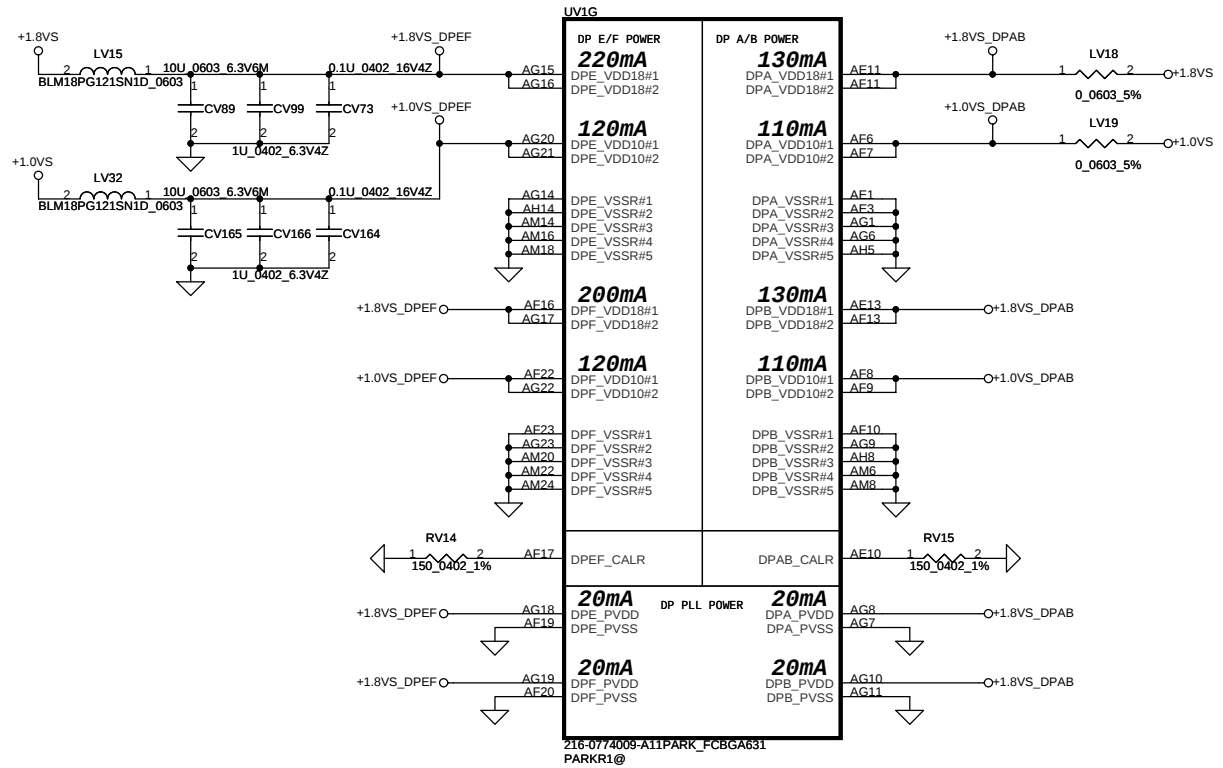
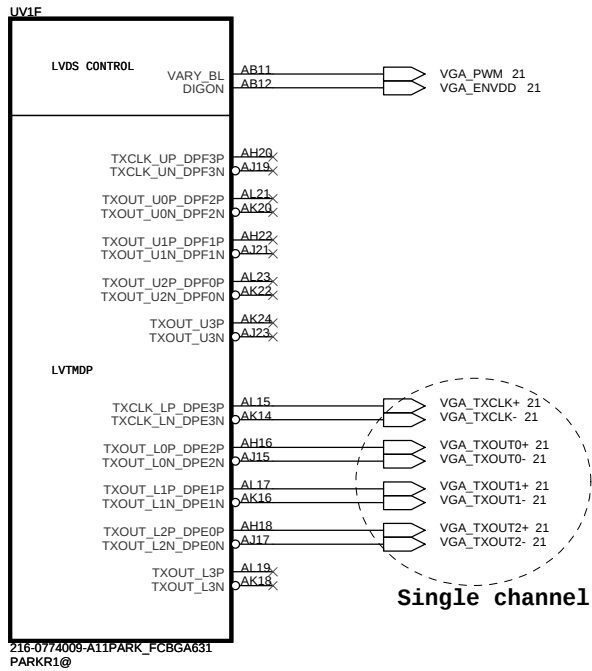


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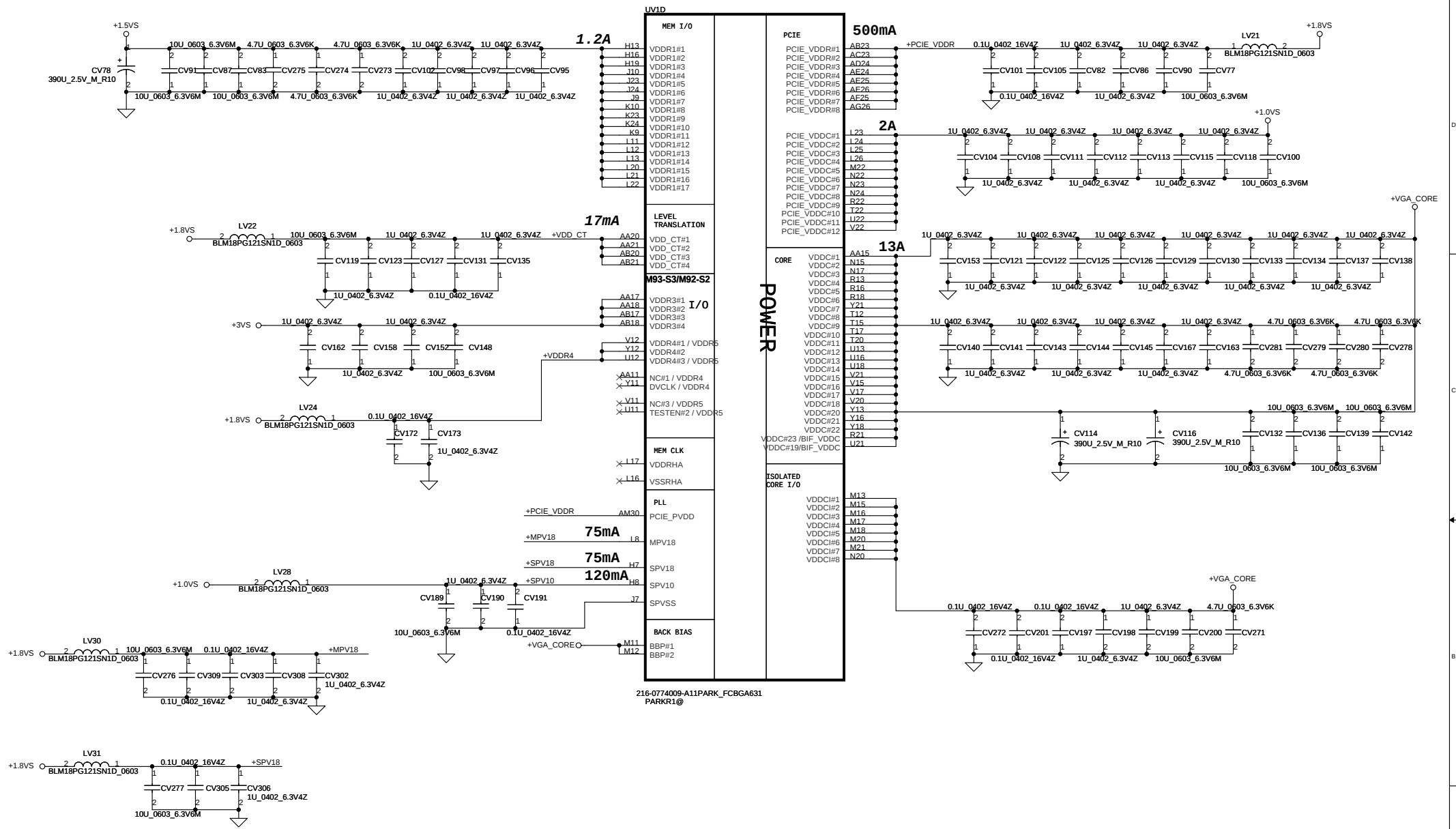


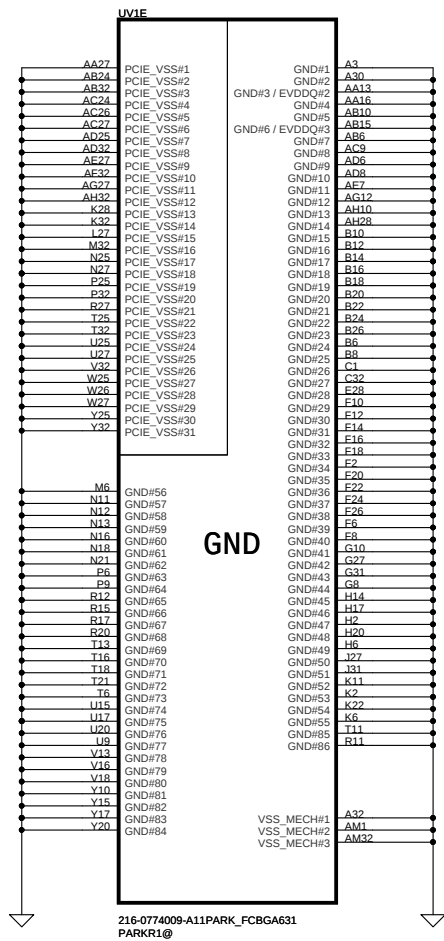
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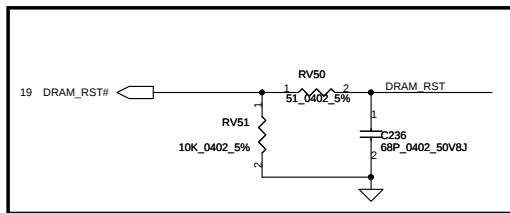
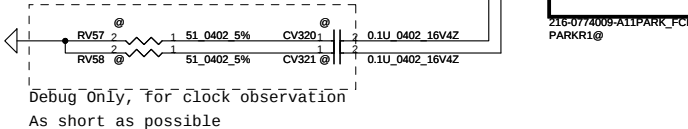
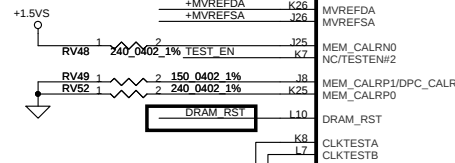
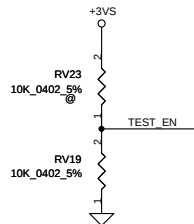
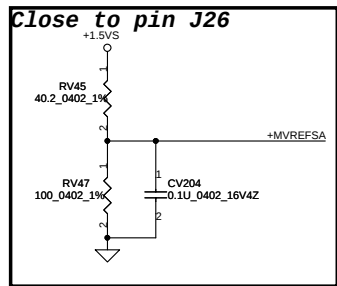
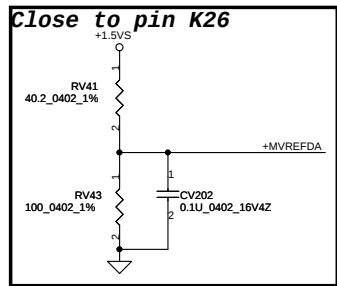




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Check with ATI FAE

UVIC

MEMORY INTERFACE

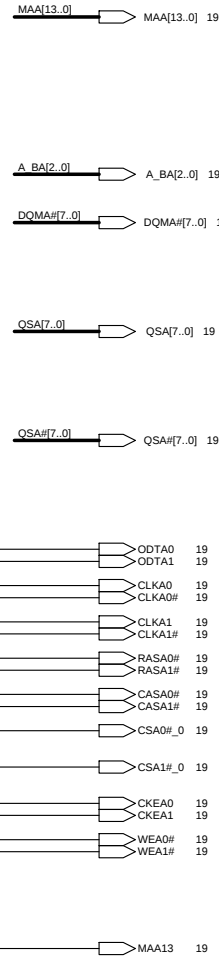
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MDA7 F30 DQA_7
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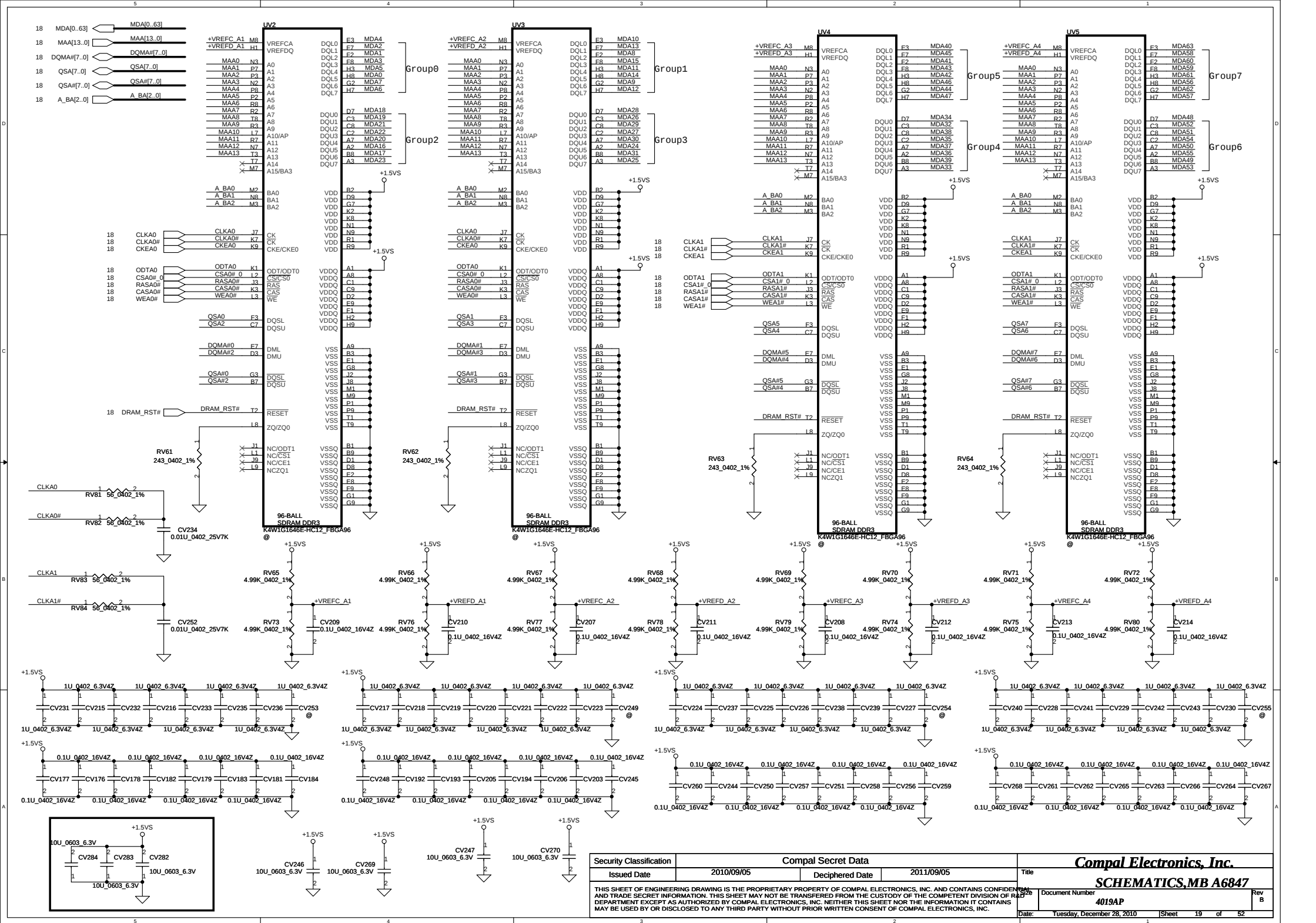
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MAA_9 K14 MAA9
MAA_10 J11 MAA10
MAA_11 J13 MAA11
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DQMA_2 A21 DQMA#2
DQMA_3 C21 DQMA#3
DQMA_4 F13 DQMA#4
DQMA_5 D12 DQMA#5
DQMA_6 E3 DQMA#6
DQMA_7 F4 DQMA#7

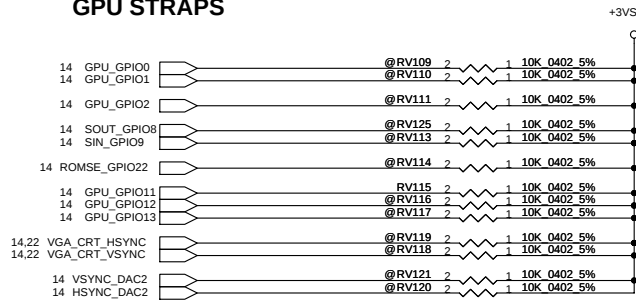
RDQSA_0 H28 QSA0
RDQSA_1 C27 QSA1
RDQSA_2 A23 QSA2
RDQSA_3 E19 QSA3
RDQSA_4 F15 QSA4
RDQSA_5 D10 QSA5
RDQSA_6 D6 QSA6
RDQSA_7 G5 QSA7

WDQSA_0 H27 QSA#0
WDQSA_1 A27 QSA#1
WDQSA_2 C23 QSA#2
WDQSA_3 C19 QSA#3
WDQSA_4 C15 QSA#4
WDQSA_5 E9 QSA#5
WDQSA_6 C5 QSA#6
WDQSA_7 H4 QSA#7





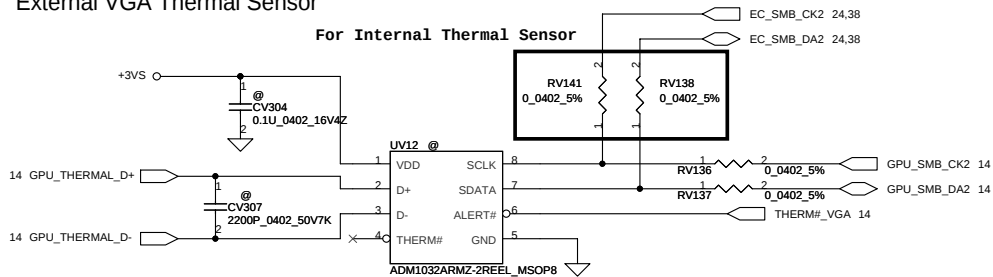
GPU STRAPS



GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0
0 0 1	256MB	(M25P05A)
0 1 0	64MB	

External VGA Thermal Sensor

For Internal Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

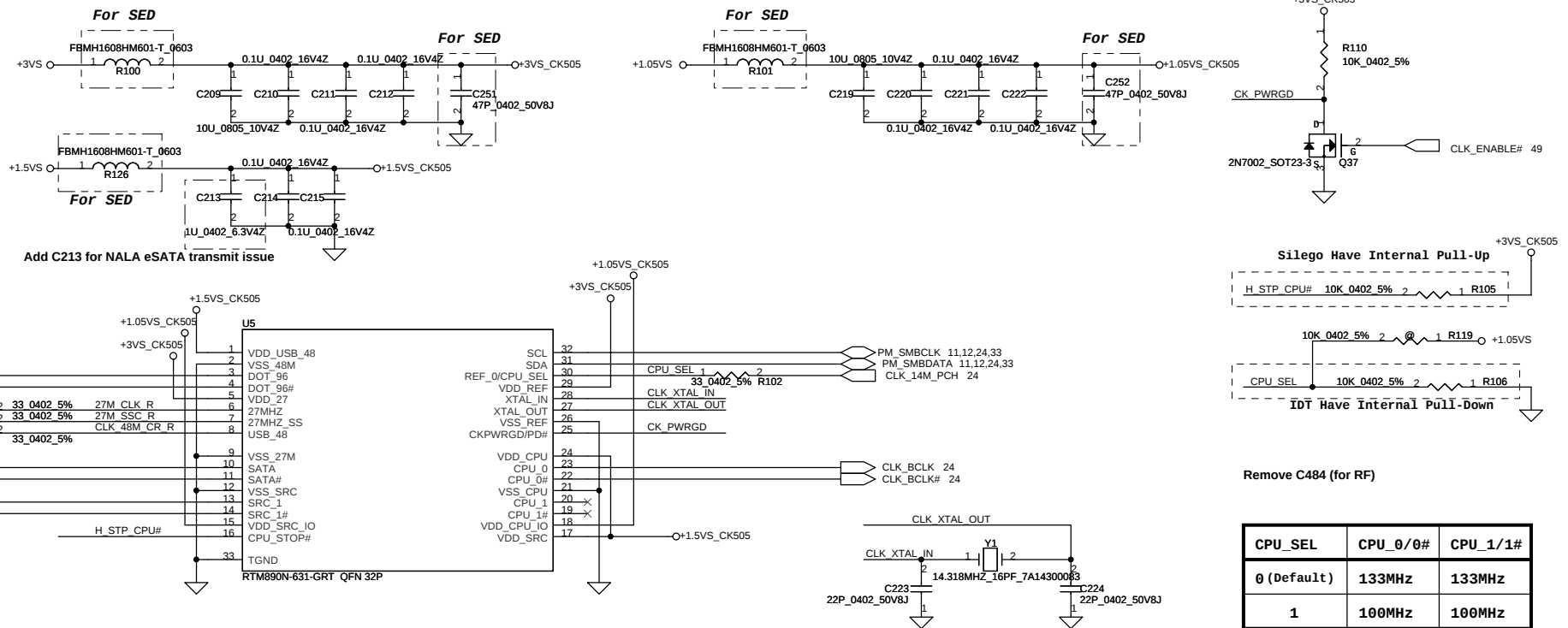
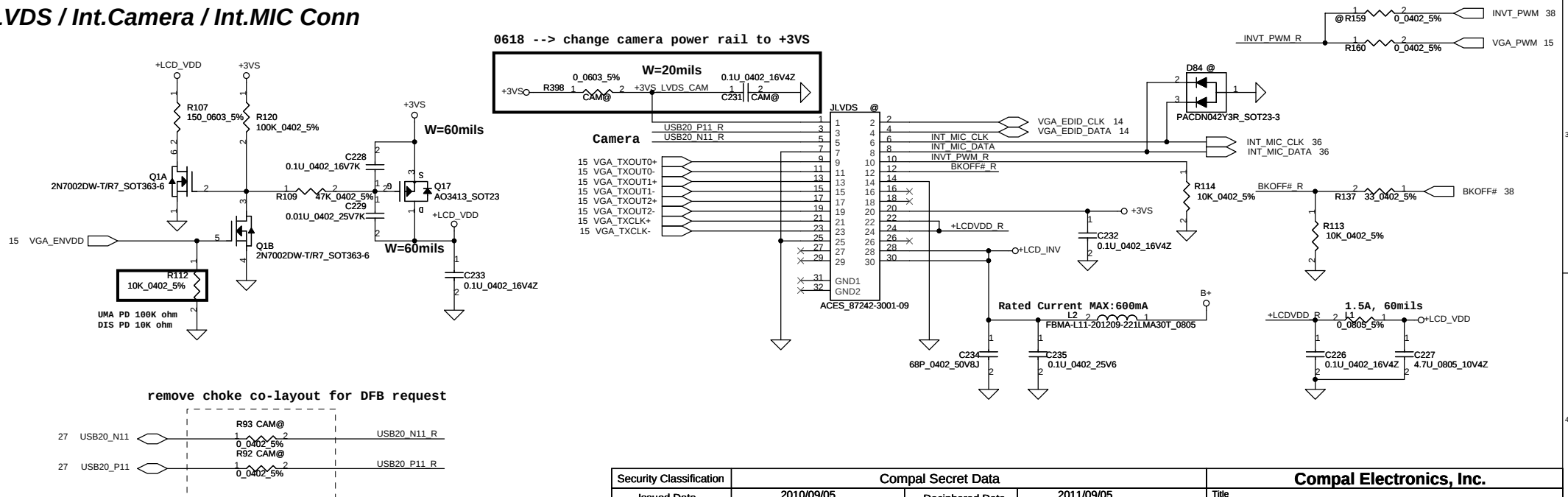
Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 5.0 GT/s capability will be controlled by software
RESERVED	GPIO_8_ROMSO	SOUT_GPIO8	RESERVED	0
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (Internal pulldown)
VGA_DIS	GPIO_9_ROMSI	SIN_GPIO9	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
CONFIG(2:0)	GPIO[13:11]	GPU_GPIO11 GPU_GPIO12 GPU_GPIO13	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1 (256M)
VIP_DEVICE_STRAP_DIS	V2SYNC	VSYNC_DAC2	VIP Device Strap Enable indicates to the software driver 0 - Driver would ignore the value sampled on VHAD_0 during reset 1 - Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device is connected	0
RESERVED	H2SYNC	HSYNC_DAC2	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	VGA_CRT_HSYNC VGA_CRT_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	0 0

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVDATA (2,1,0)	Park XT S3	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C-C	SA000032460	0 0 0
			512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	0 0 1
			1G 128Mx16 (x4)	HYN H5TQ2G63BFR-12C	SA00003VS00	0 1 0
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC12	SA00003MQ40	0 1 1
		Robson LP S3	Design Ready			
			512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C-C	SA000032460	1 0 0
			512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	1 0 1
			1G 128Mx16 (x4)	HYN H5TQ2G63BFR-12C	SA00003VS00	1 1 0
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC12	SA00003MQ40	1 1 1

Design Ready

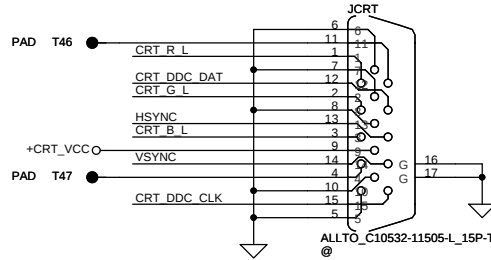
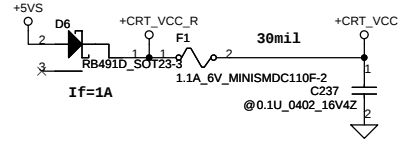
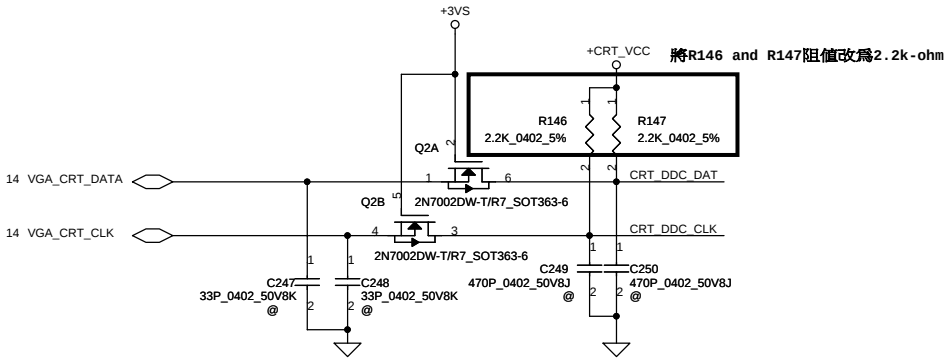
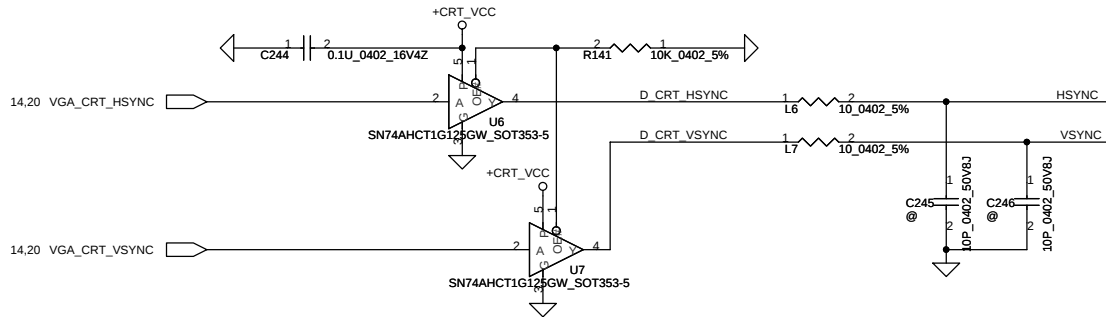
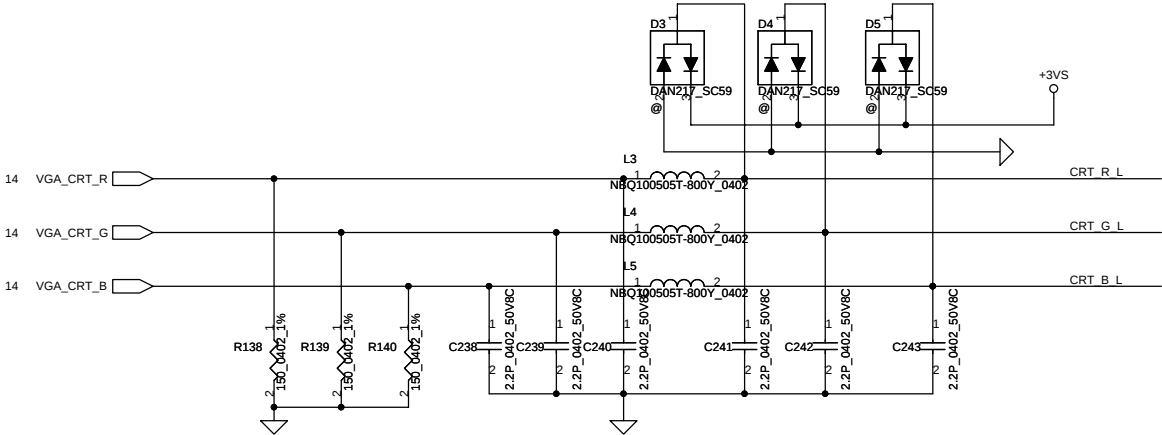
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Clock Generator

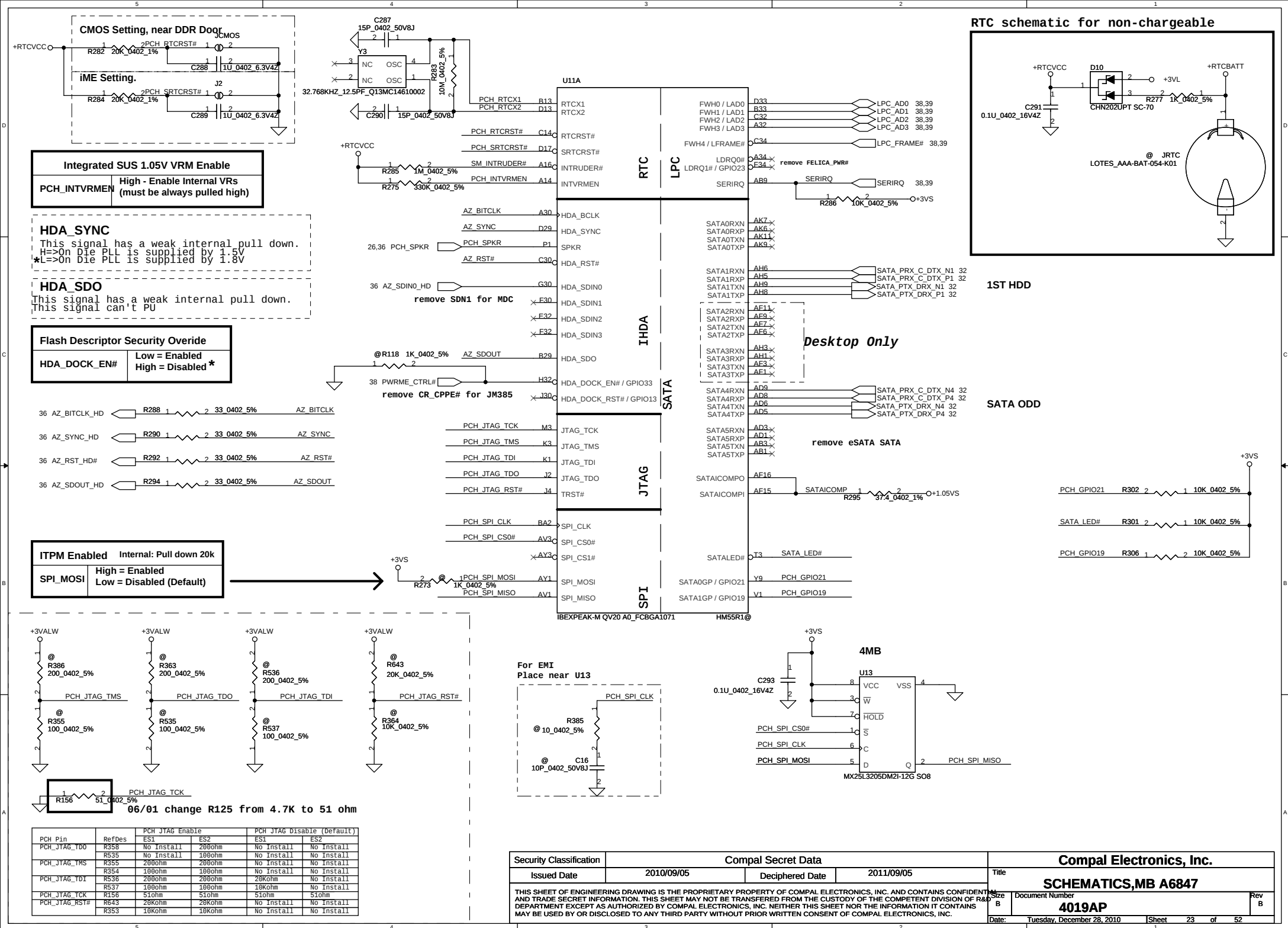
**LVDS / Int.Camera / Int.MIC Conn**

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CRT CONNECTOR



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For LAN

34 PCIE_PRX_C_LANTX_N1
34 PCIE_PRX_C_LANTX_P1
34 PCIE_PT_X_C_LANRX_N1
34 PCIE_PT_X_C_LANRX_P1

For WLAN

33 PCIE_PRX_WLANTX_N2
33 PCIE_PRX_WLANTX_P2
33 PCIE_PT_X_C_WLANRX_N2
33 PCIE_PT_X_C_WLANRX_P2

LAN

WLAN

form CLKREQ_NEW# to PCH_GPIO20

form CLKREQ_JET# to PCH_GPIO25

form CLKREQ_CR# to PCH_GPIO26

remove NewCard PCIE

remove JET PCIE

remove CardReader PCIE

remove NEWCARD CLK

remove JET CLK

U11B

PCIE_PRX_C_LANTX_N1 BG30
PCIE_PRX_C_LANTX_P1 B130
PCIE_PT_X_LANRX_N1 BE29
PCIE_PT_X_LANRX_P1 BH29

AW30
BA30
PCIE_PT_X_WLANRX_N2 BC30
PCIE_PT_X_WLANRX_P2 BD30

AU30
AT30
AU32
AV32
PERN3
PERP3
PETN3
PETP3

BA32
BB32
BD32
BE32
PERN4
PERP4
PETN4
PETP4

BE33
BH33
BG32
BJ32
PERN5
PERP5
PETN5
PETP5

BA34
AW34
BC34
BD34
PERN6
PERP6
PETN6
PETP6

AT34
AU34
AU36
AV36
PERN7
PERP7
PETN7
PETP7

BG34
BJ34
BG36
BJ36
PERN8
PERP8
PETN8
PETP8

AK48
AK47
CLKOUT_PCIE0N
CLKOUT_PCIE0P

CLKREQ_LAN# P9
PCIECLKRQ0# / GPIO73

AM43
AM45
CLKOUT_PCIE1N
CLKOUT_PCIE1P

PCIECLKRQ1# / GPIO18

AM47
AM48
CLKOUT_PCIE2N
CLKOUT_PCIE2P

PCIECLKRQ2# / GPIO20

AH42
AH41
CLKOUT_PCIE3N
CLKOUT_PCIE3P

PCIECLKRQ3# / GPIO25

AM51
AM53
CLKOUT_PCIE4N
CLKOUT_PCIE4P

PCIECLKRQ4# / GPIO26

AT50
AT52
CLKOUT_PCIE5N
CLKOUT_PCIE5P

PCIECLKRQ5# / GPIO44

AK53
AK51
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P

PEG_B_CLKRQ# / GPIO56

IBEXPEAK-M QV20 A0_FCBGA1071

PCI-E*

SMBUS

PEG

From CLK BUFFER

Clock Flex

SMBALERT# / GPIO11

SMBCLK H14 PCH_SMBCLK

SMBDATA C8 PCH_SMBDATA

SML0ALERT# / GPIO60

SML0CLK C6 PCH_SMLCLK0

SML0DATA G8 PCH_SMLDATA0

SML1ALERT# / GPIO74

SML1CLK / GPIO58

SML1DATA / GPIO75

CL_CLK1 T13

CL_DATA1 T11

CL_RST1# T9

PEG_A_CLKRQ# / GPIO47

CLKREQ_PEG# CLKREQ_PEG# 14

CLKOUT_PEG_A_N AD43

CLKOUT_PEG_A_P AD45

CLKOUT_DMI_N AN4

CLKOUT_DMI_P AN2

CLKOUT_DP_N / CLKOUT_BCLK1_N AT1

CLKOUT_DP_P / CLKOUT_BCLK1_P AT3

CLKIN_DMI_N AW24

CLKIN_DMI_P BA24

CLKIN_BCLK_N AP3

CLKIN_BCLK_P AP1

CLKIN_DOT_96N E18

CLKIN_DOT_96P E18

CLKIN_SATA_N / CKSSCD_N AH13

CLKIN_SATA_P / CKSSCD_P AH12

REFCLK14IN P41

CLKIN_PCIELOOPBACK I42

XTAL25_IN AH51

XTAL25_OUT AH53

XCLK_RCOMP AF38

CLKOUTFLEX0 / GPIO64

CLKOUTFLEX1 / GPIO65

CLKOUTFLEX2 / GPIO66

CLKOUTFLEX3 / GPIO67

HM55R1

HM55R1

HM55R1

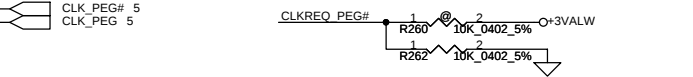
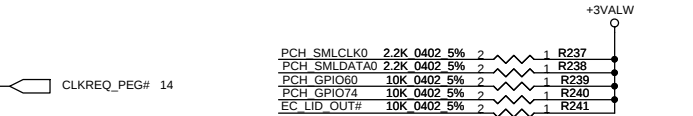
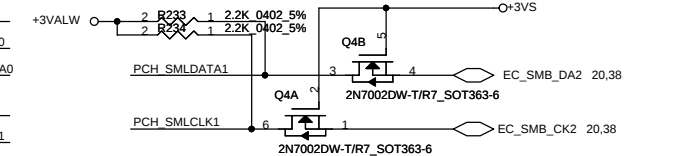
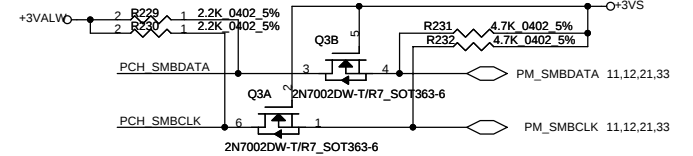
HM55R1

HM55R1

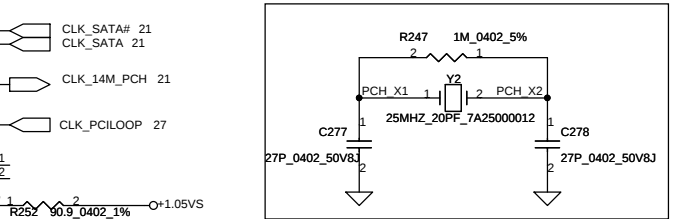
HM55R1

HM55R1

HM55R1

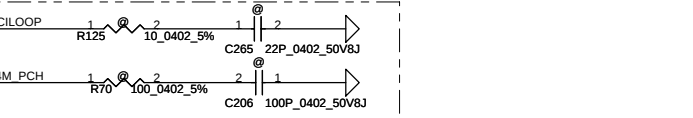


FROM CLK GEN FOR: 133/100/96/14.318 MHZ

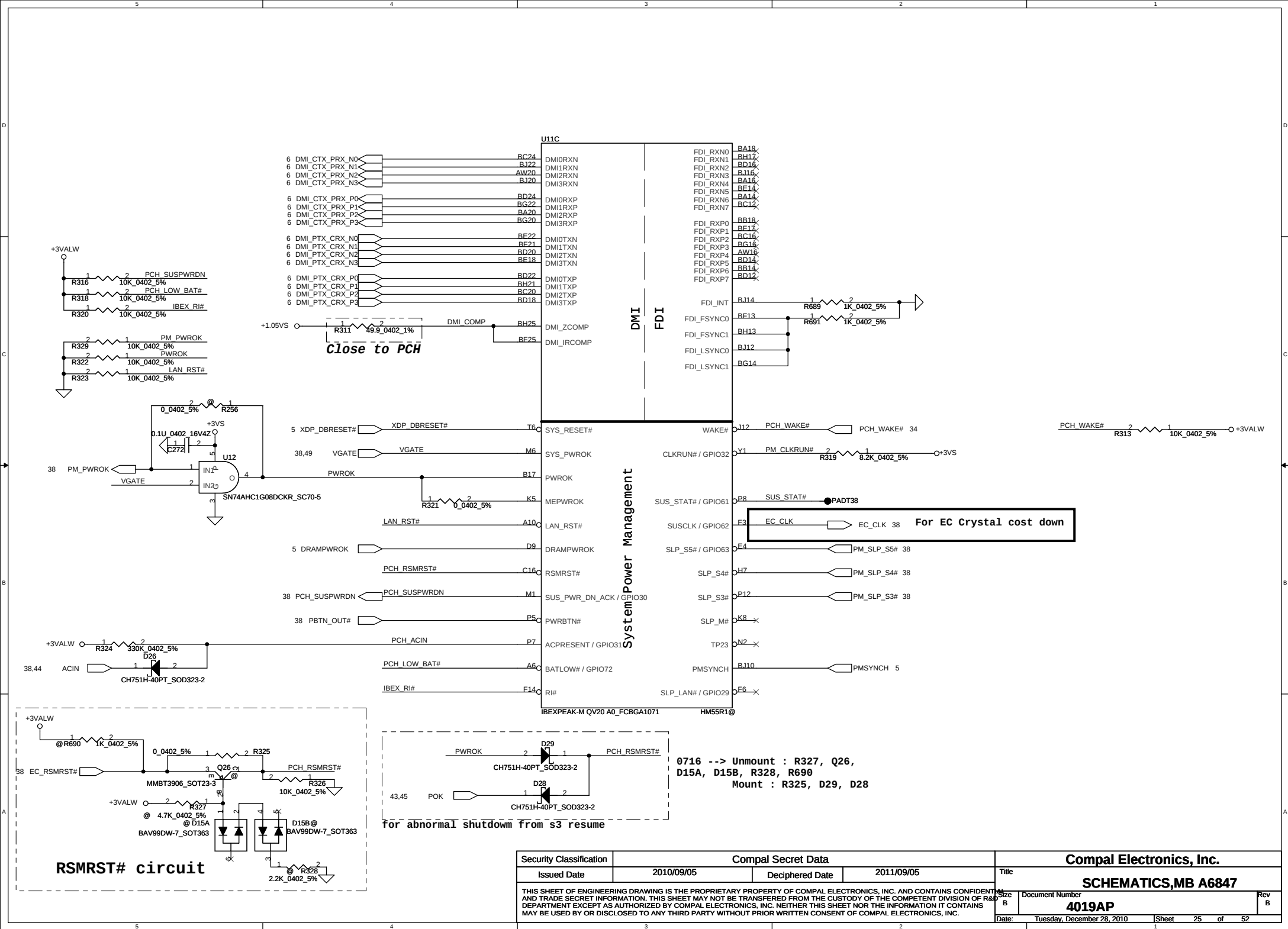


Note: Stuff 0 ohm if 25MHz crystal un-stuff

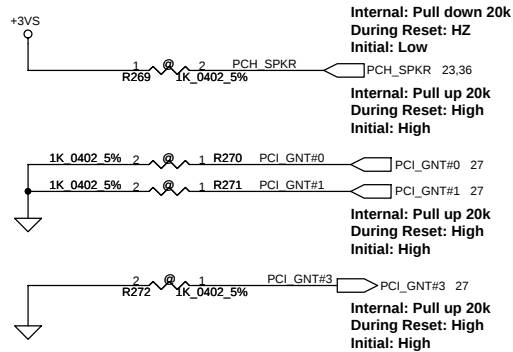
for EMI request



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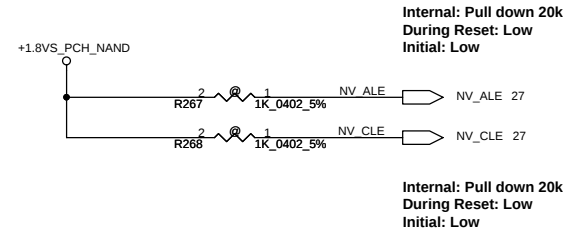
PCH Strap Pin



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

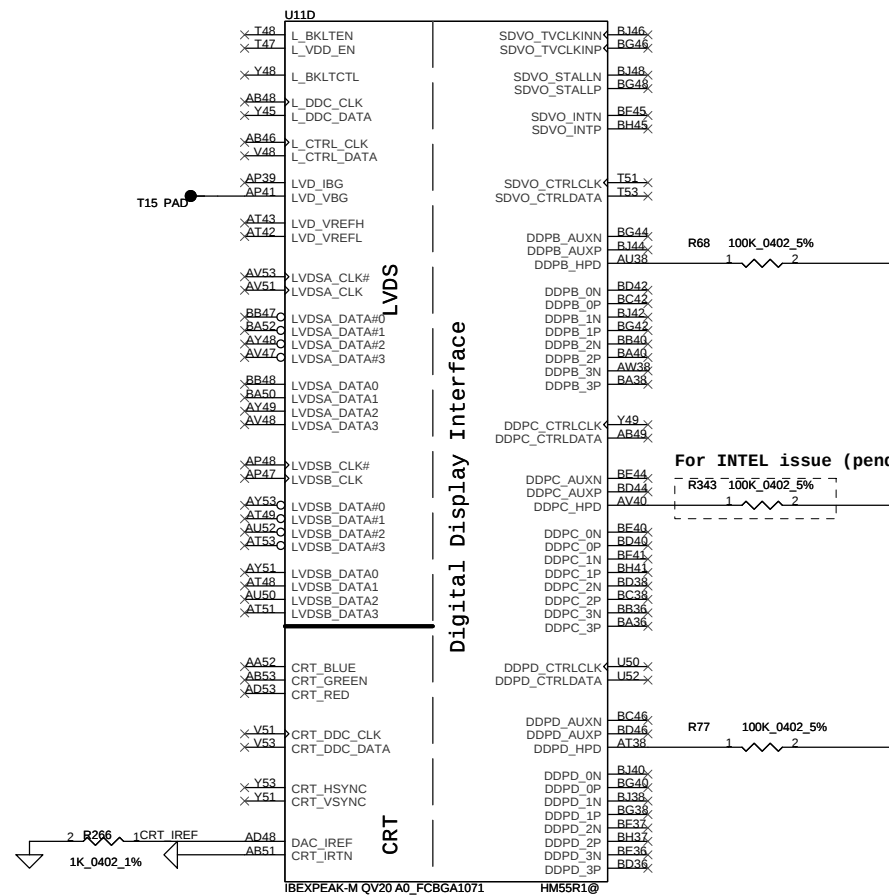
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc



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GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

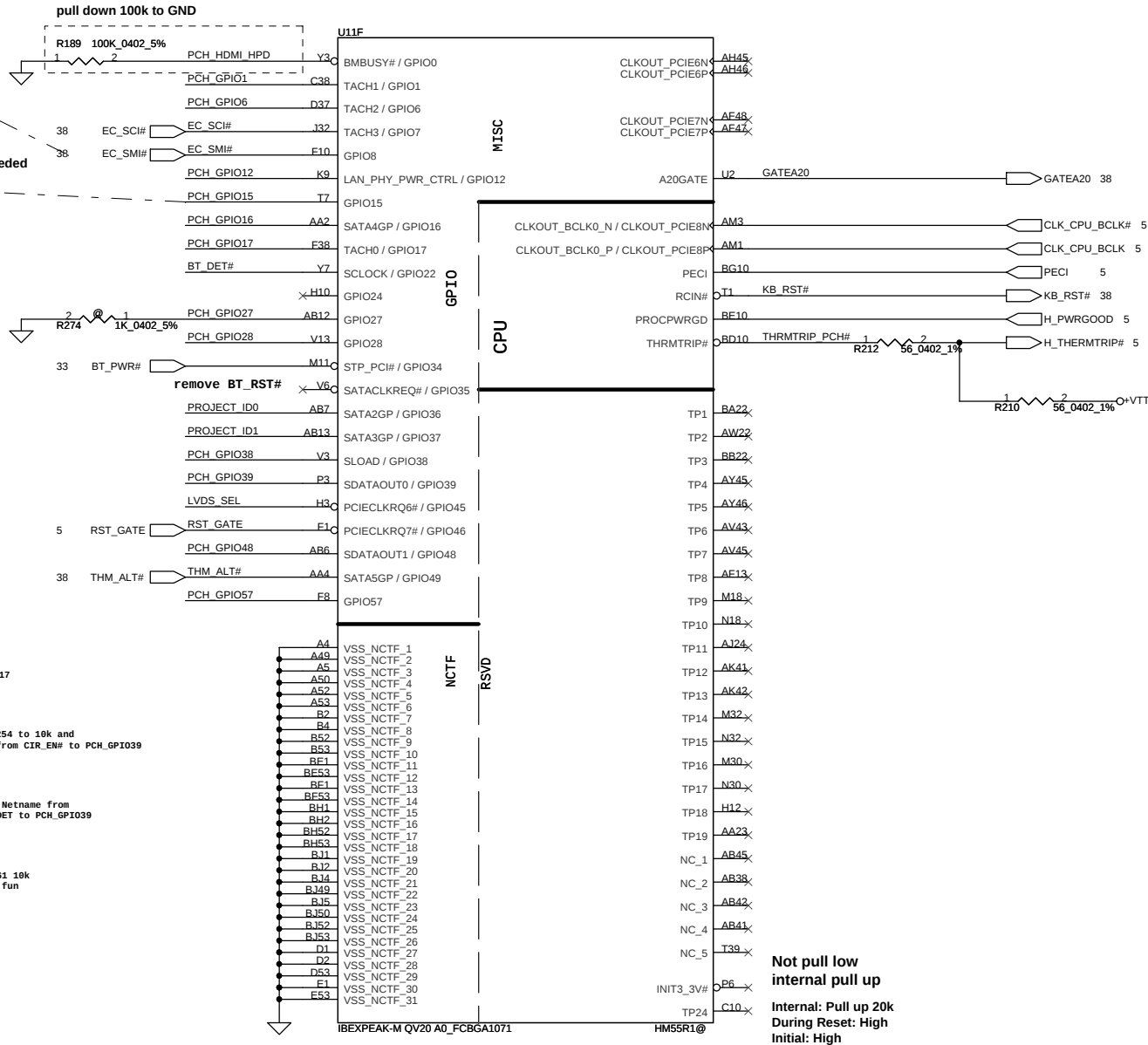
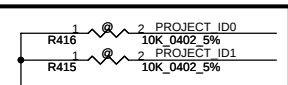
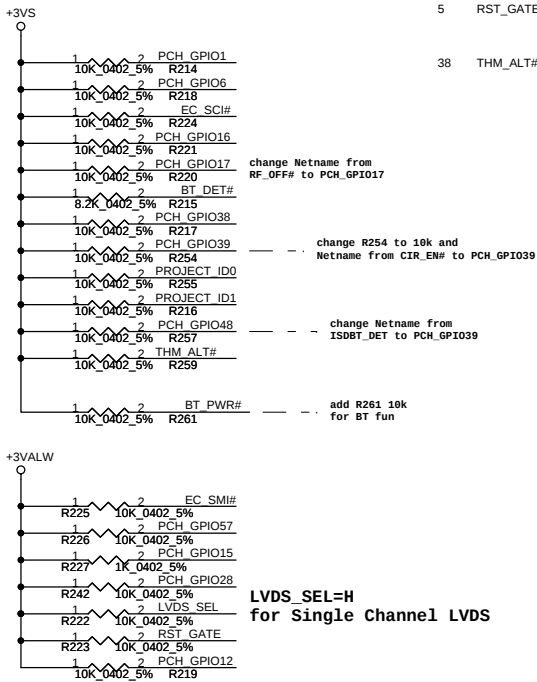
GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR

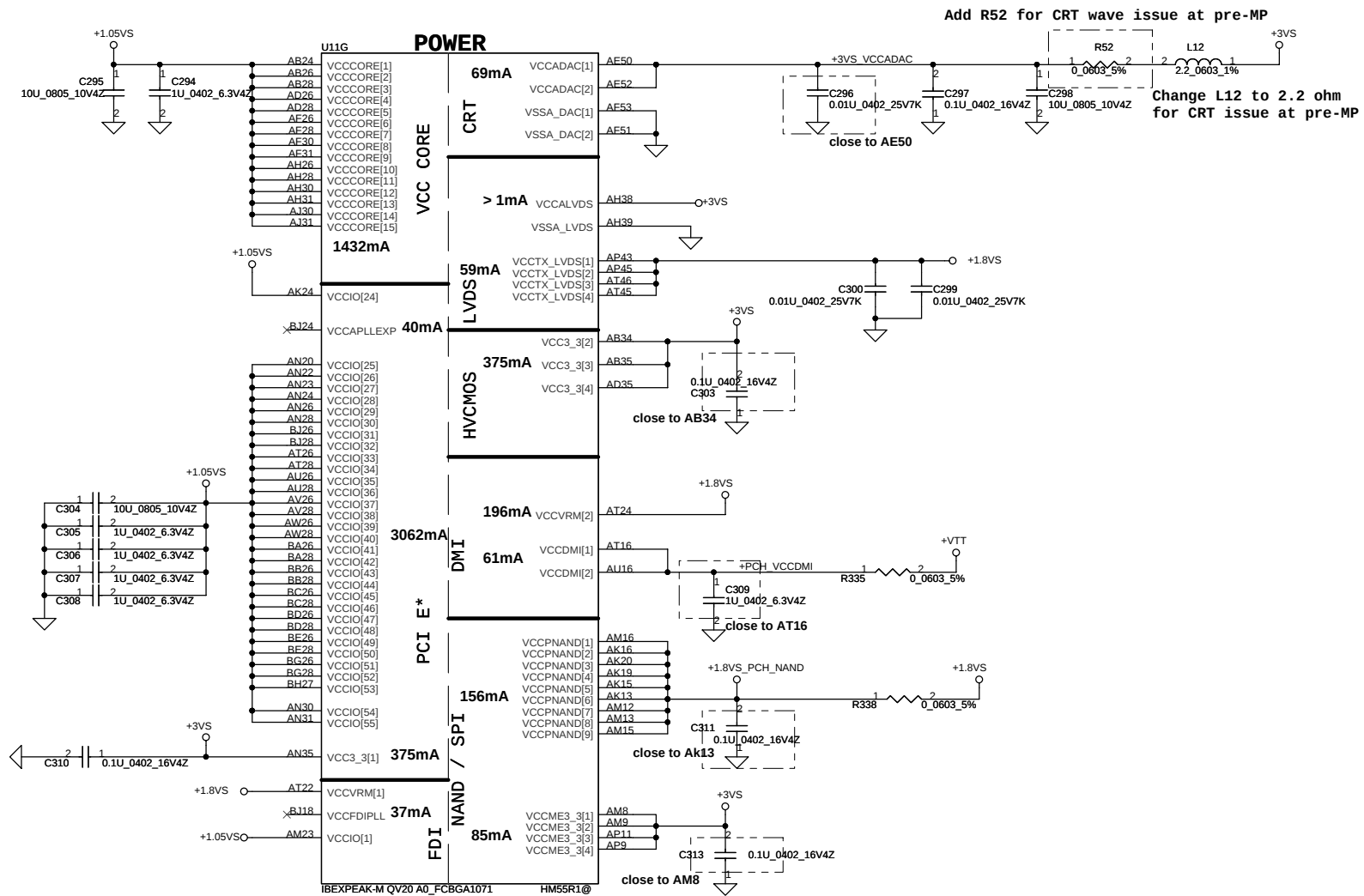
PCH_GPIO27 High = Enabled (Default)
Low = Disabled

PROJECT_ID

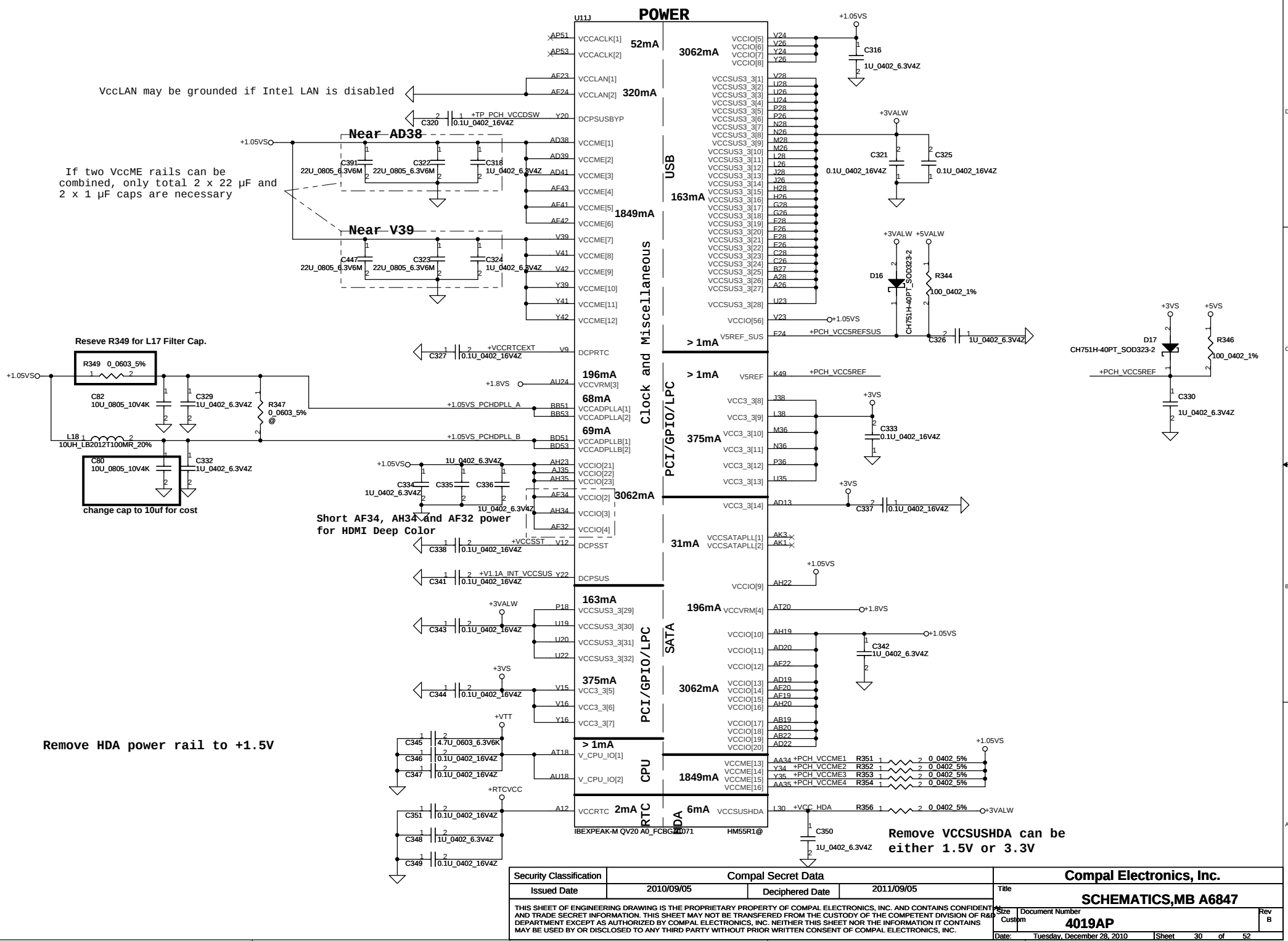
Name	ID0	ID1
NBQAA 11.6/13.3"	L	L
NBQAA 14"	L	H
*NWQAA 16"	H	L
NALAA 17.3"	H	H

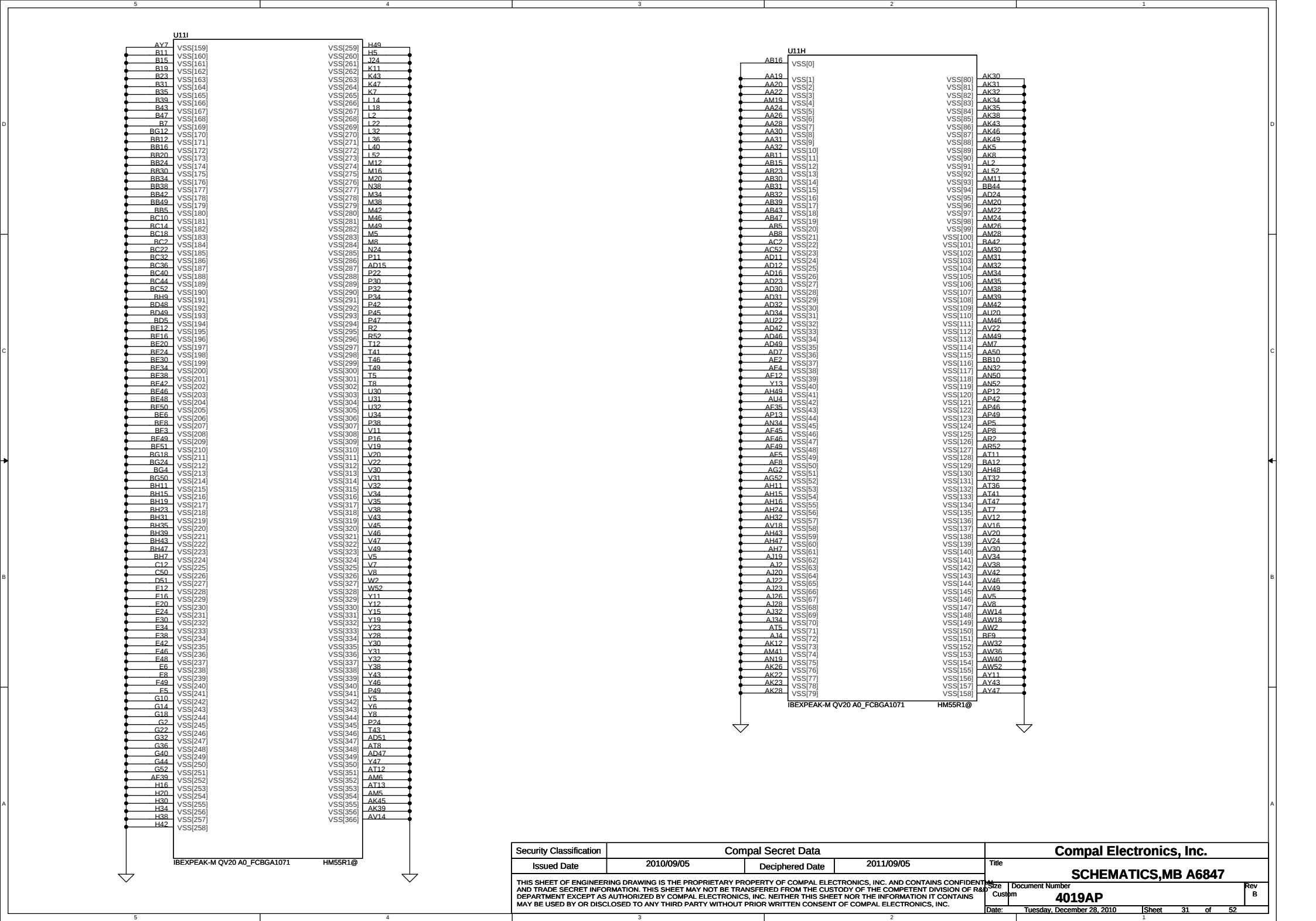


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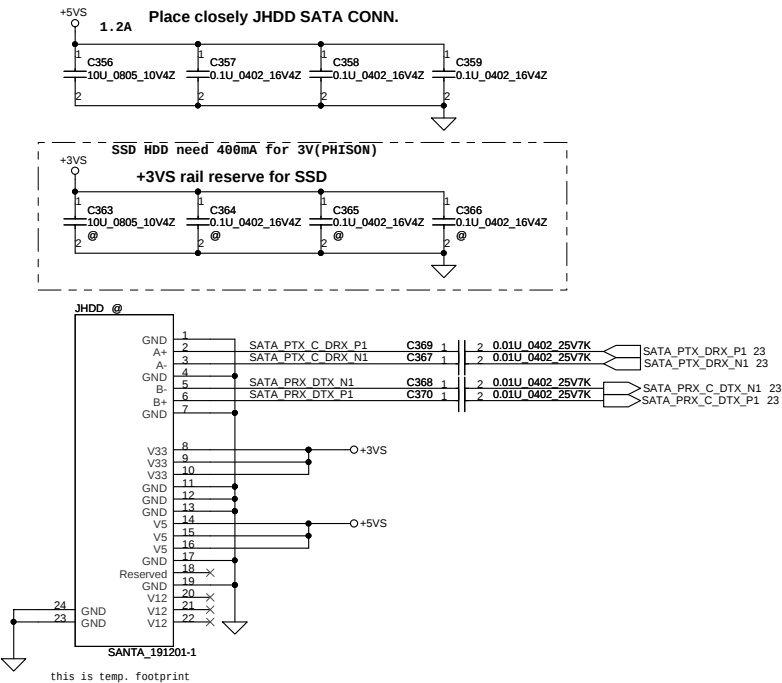
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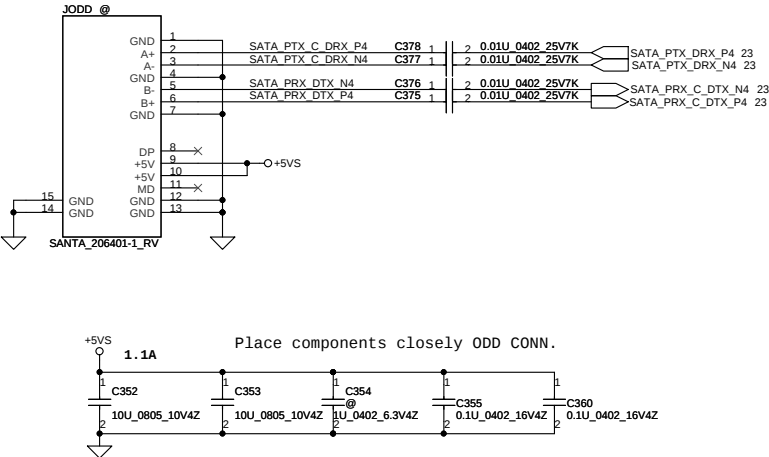


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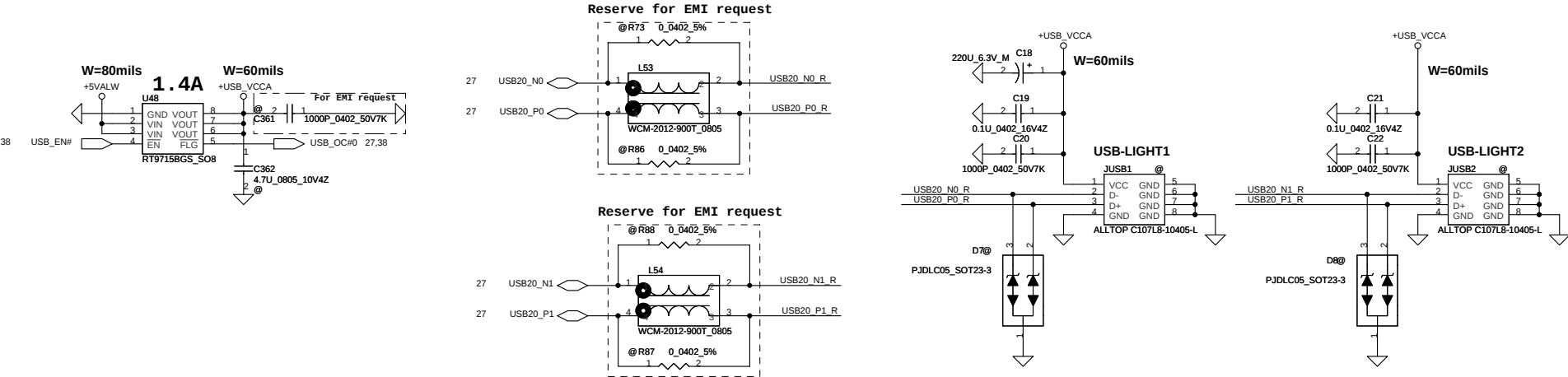
SATA HDD Conn.



SATA ODD Conn



USB Conn. (2 Port)



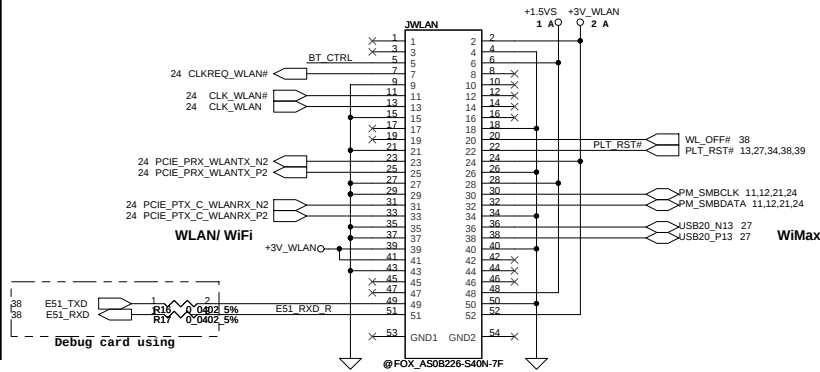
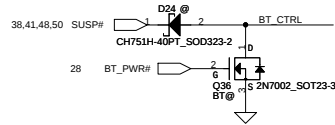
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PCle Mini Card-WLAN/WiMax

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

**If +3V_WLAN is +3VS, please remove D24.

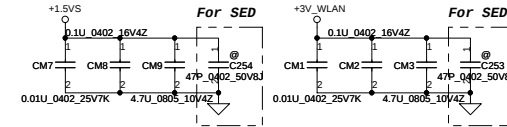


E51_RXD_R 2 R287 1K_0402_5% BT_CTRL

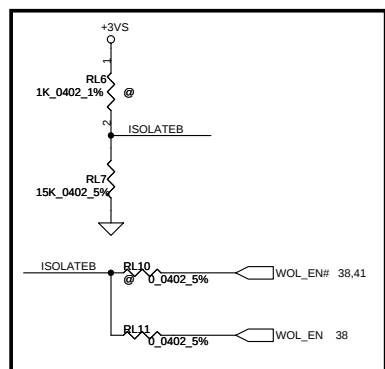
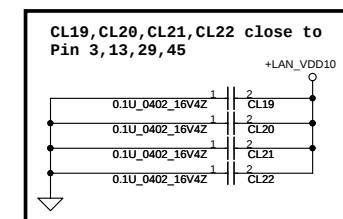
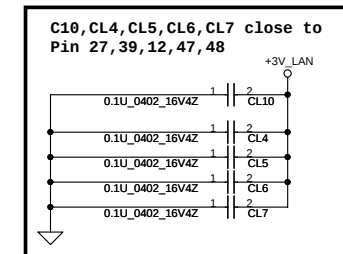
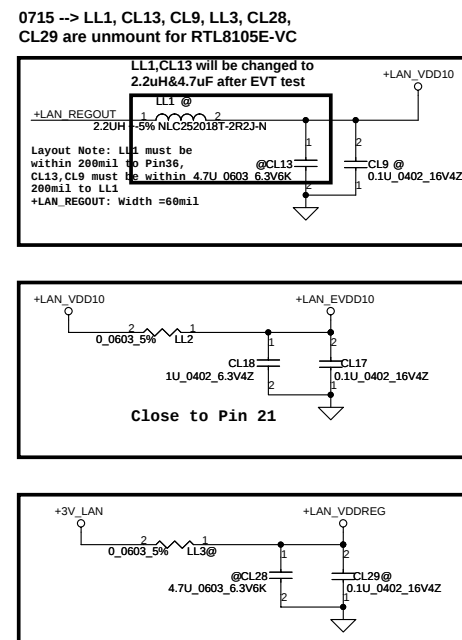
Slot#1 Half PCIe Mini Card-WLAN/WiMax

+3VSC @ PJ26 1 JUMP_43X79 3V_WLAN

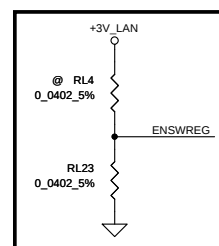
Short PJ26 for WiFi(WLAN) module only.



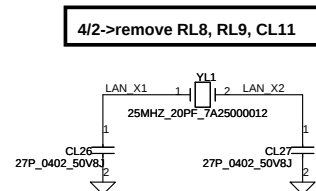
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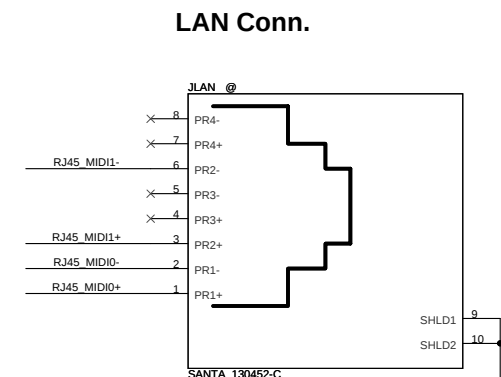
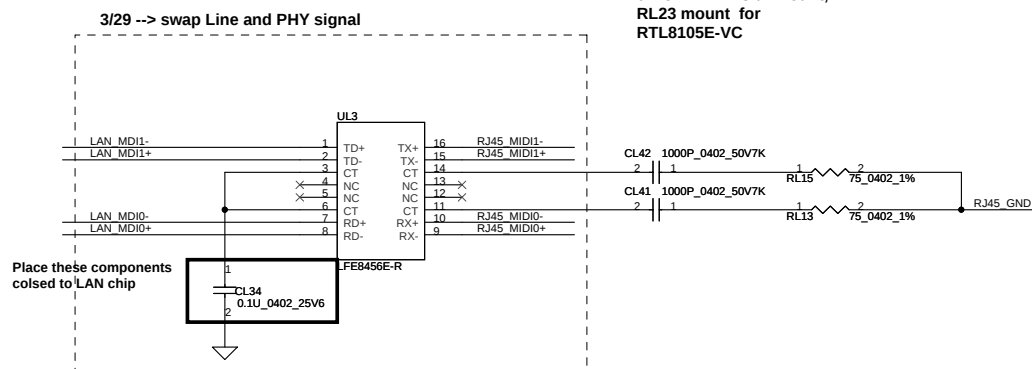
Add RL10 for +3V_LAN power enable signal
Add RL11 for wake on LAN function enable signal



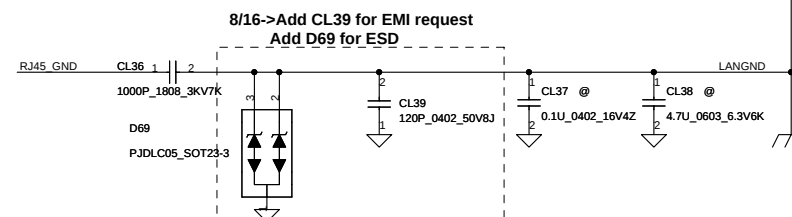
0715 --> RL4 is unmount,
RL23 mount for
RTL8105E-VC



4/2->remove RL8, RL9, CL11

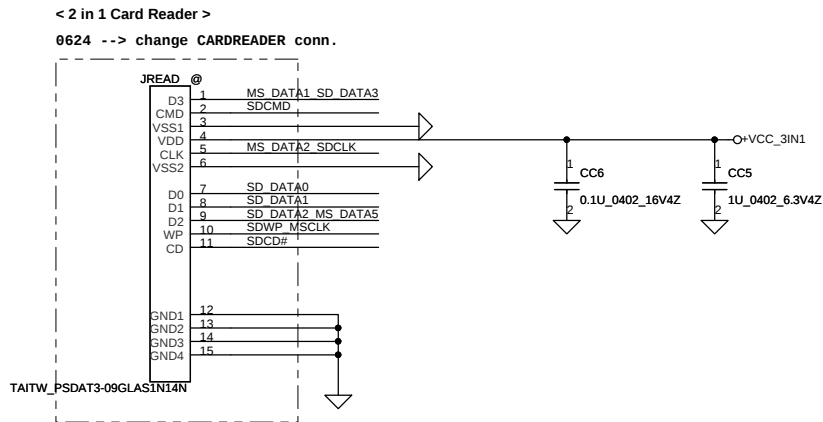
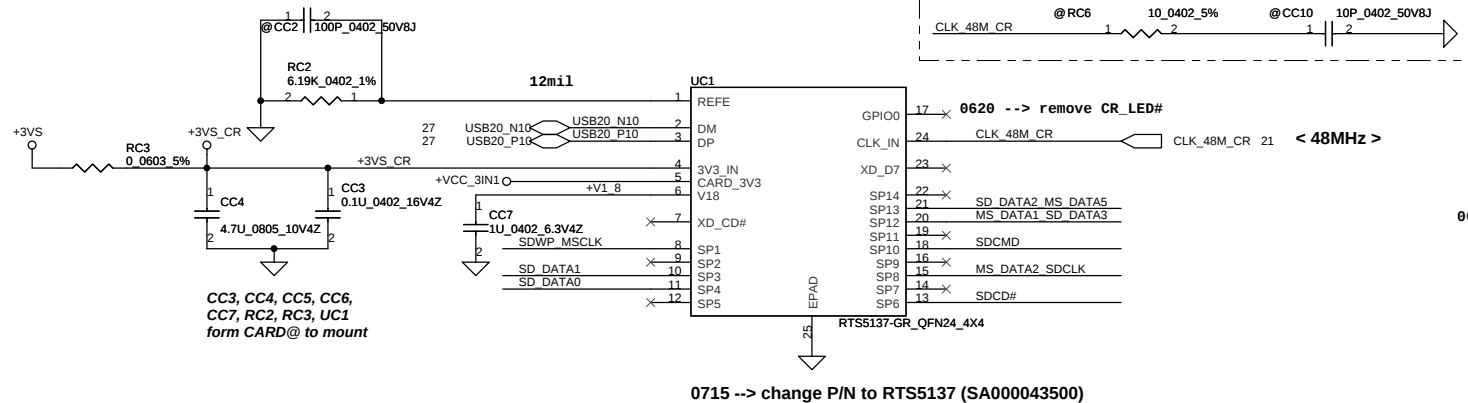


LAN Conn.

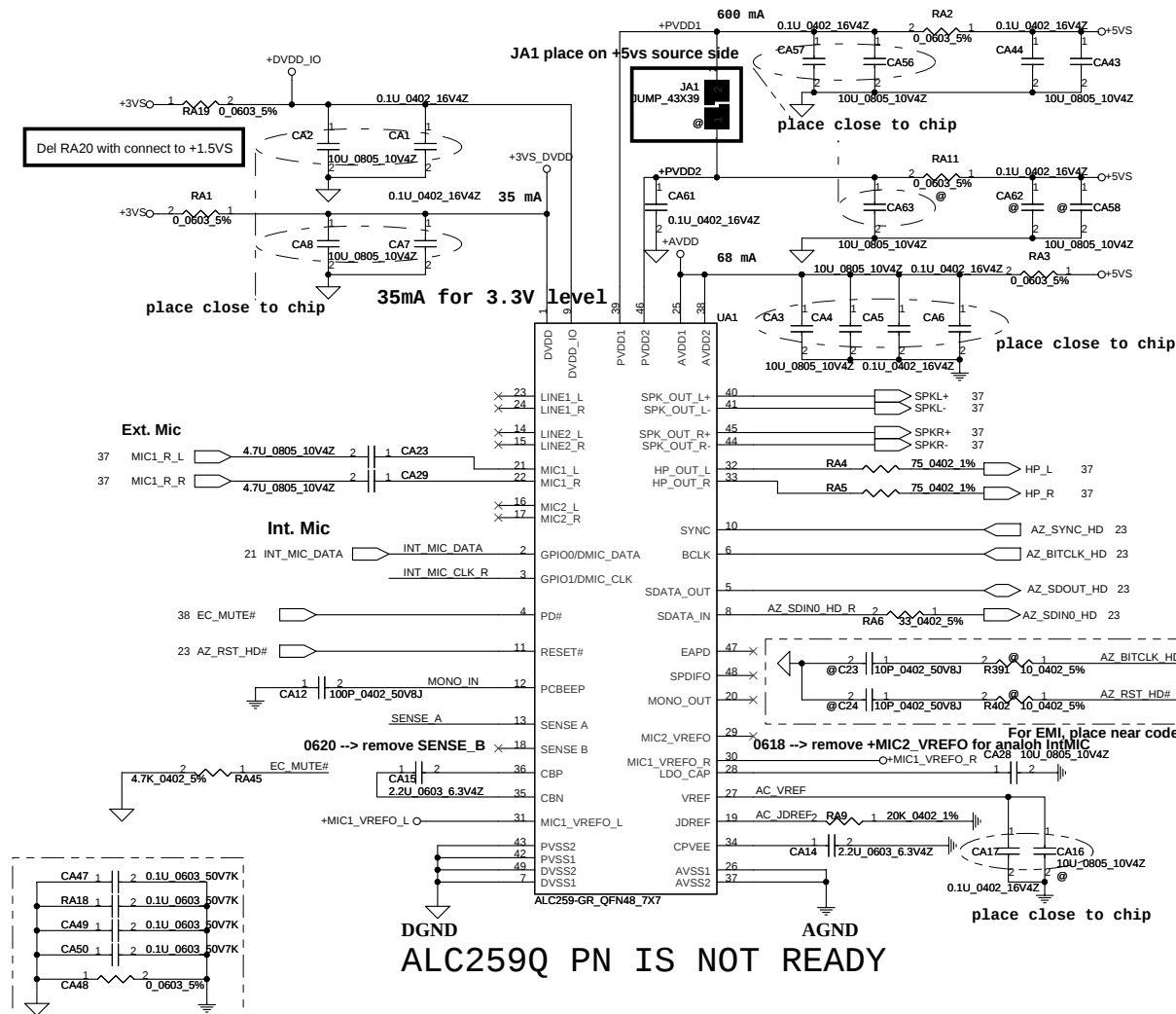


8/16->Add CL39 for EMI request
Add D69 for ESD

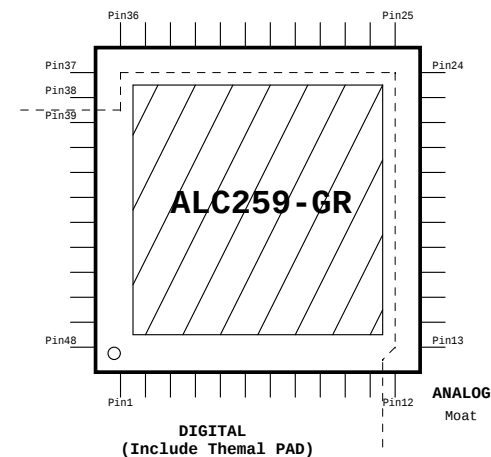
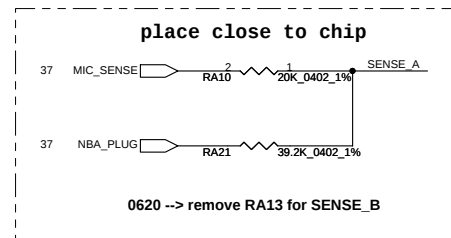
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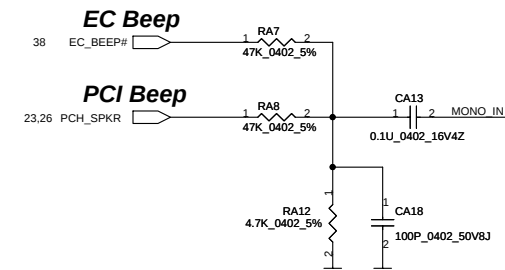
Codec



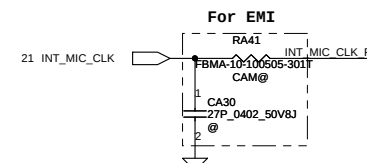
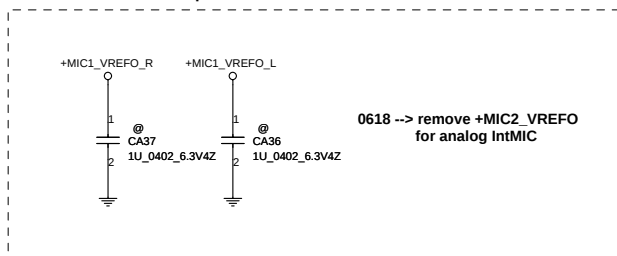
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	



Beep sound

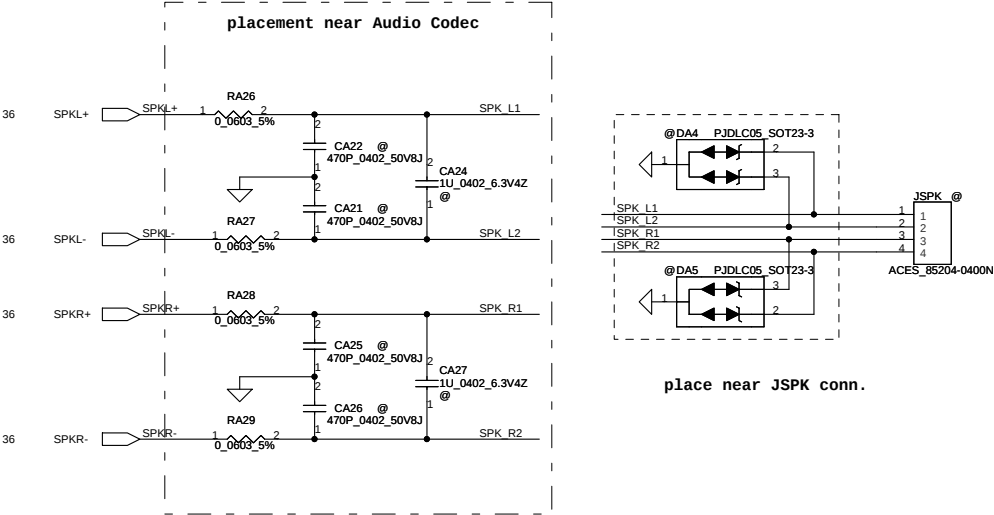


Place close to chip

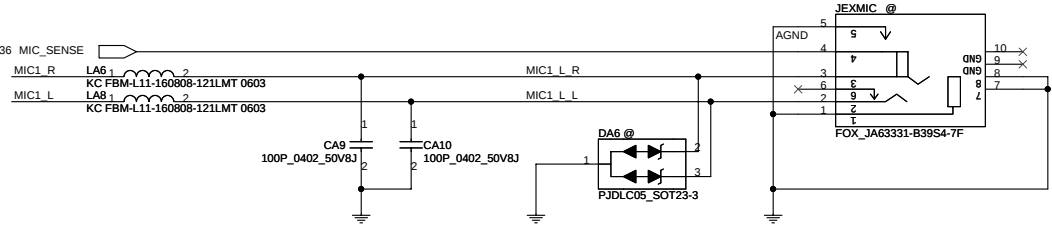


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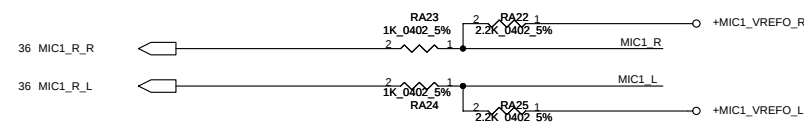
Speaker Connector



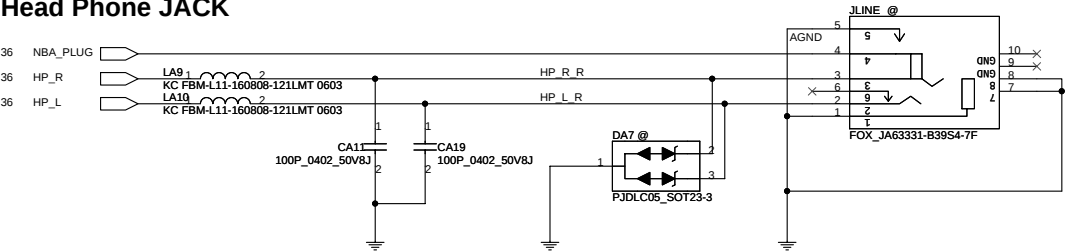
Ex.MIC JACK



Ext.MIC/LINE IN



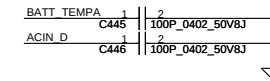
Head Phone JACK



Int. Mic

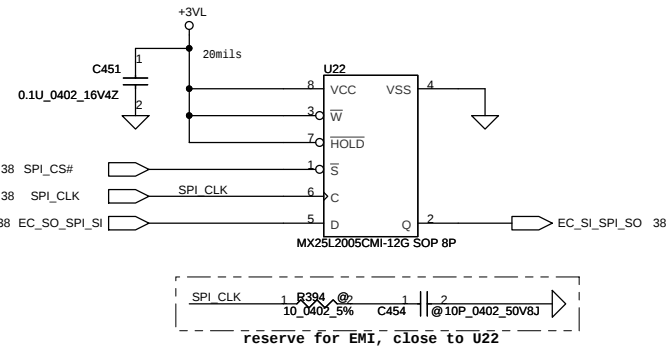
0618 --> remove Analog IntMIC, and change to DIGITAL MIC

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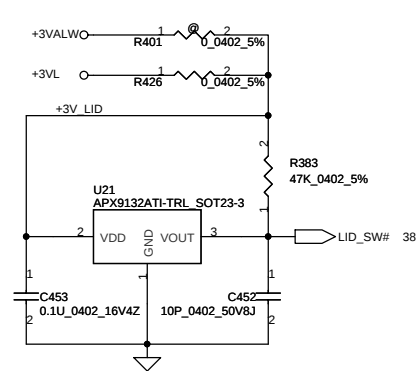


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SPI Flash (256KB)

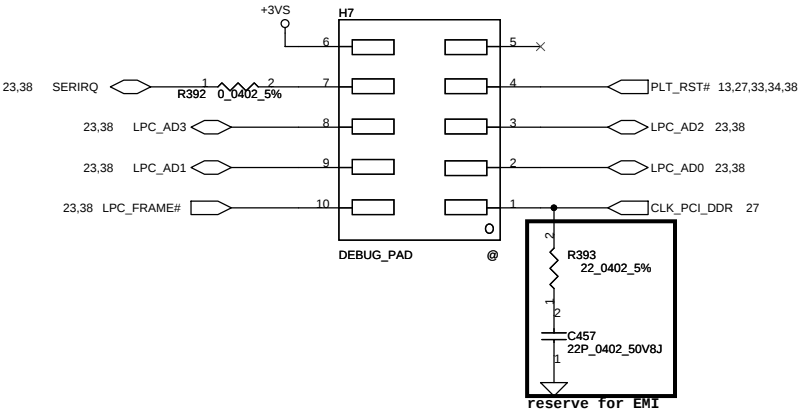


Lid SW



LPC Debug Port

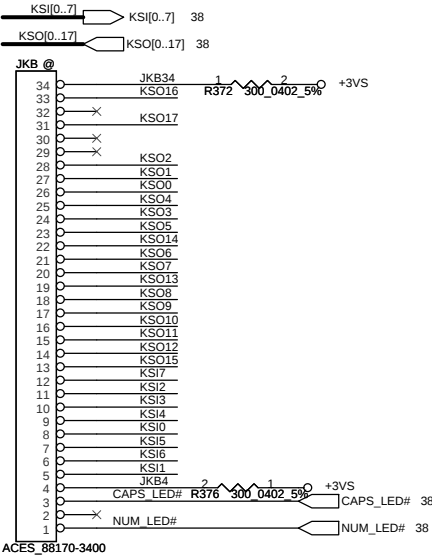
Please place the PAD under DDR DIMM.



KEYBOARD CONN.

Noticed: KB Connector Pin Definition Reversed with KB Membrane Pin Definition

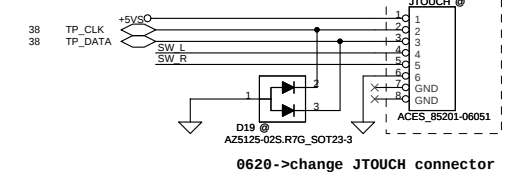
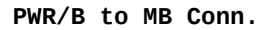
please close to JKB



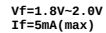
KSO16	1	2
KSO17	1	2
KSO2	1	2
KSO1	1	2
KSO0	1	2
KSO4	1	2
KSO7	1	2
KSO5	1	2
KSO14	1	2
KSO6	1	2
KSO13	1	2
KSO8	1	2
KSO9	1	2
KSO10	1	2
KSO11	1	2
KSO12	1	2
KSO15	1	2
KSI7	1	2
KSI2	1	2
KSI3	1	2
KSI4	1	2
KSI0	1	2
KSI5	1	2
KSI6	1	2
KSI1	1	2
CAPS_LED#	1	2
NUM_LED#	1	2
C435	1	2

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debug phase using



Vf=1.9V~2.4V
If=5mA



MINI CARD

SB

For Codec AGND

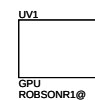
Dummy

3G

MDC

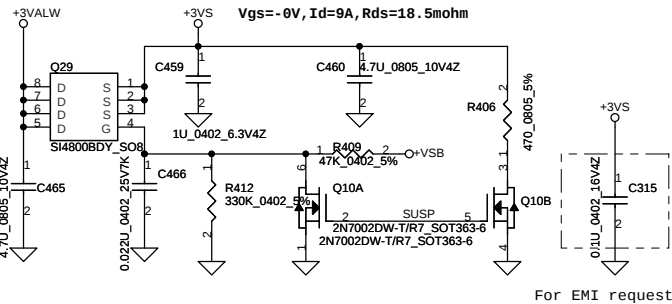
PCB Fedical Mark PAD

DC - IN

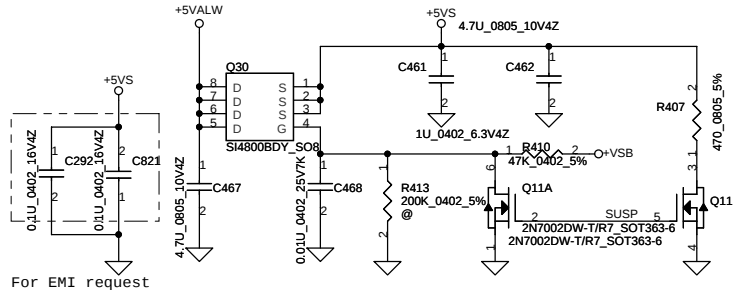


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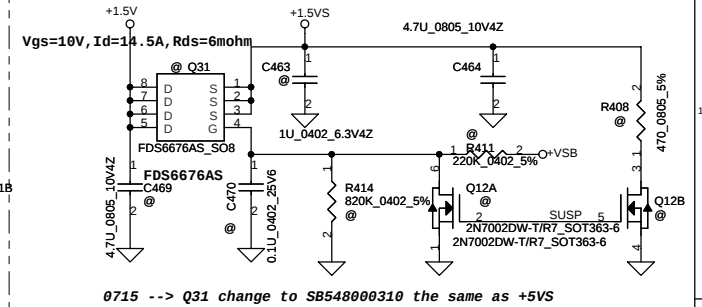
+3VALW TO +3VS



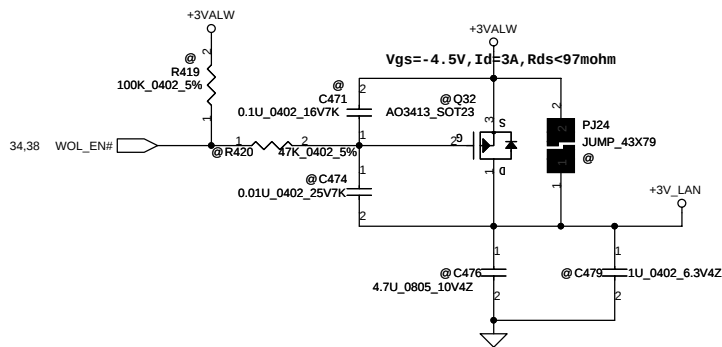
+5VALW TO +5VS



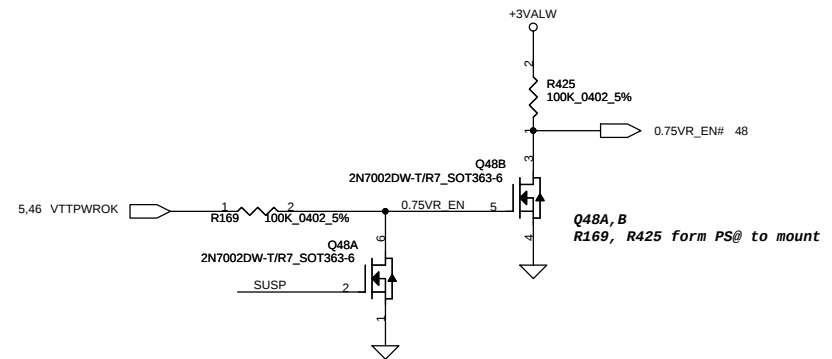
+1.5V to +1.5VS Combine with +1.5V_CPU



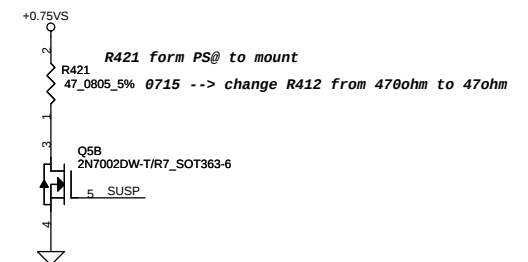
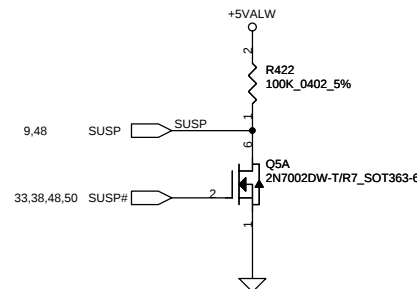
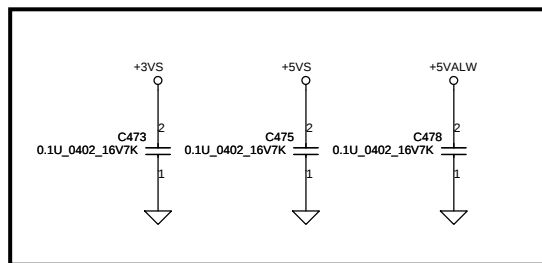
+3VALW TO +3V_LAN



For S3 CPU Power Saving

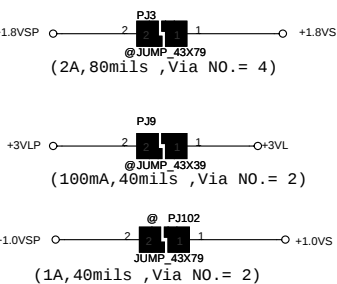
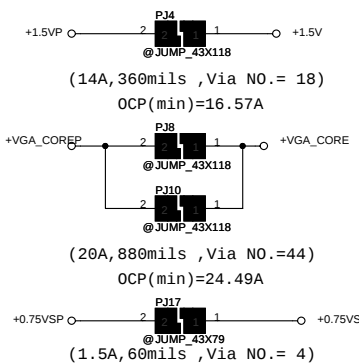
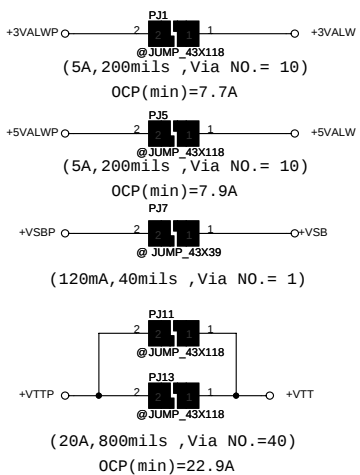
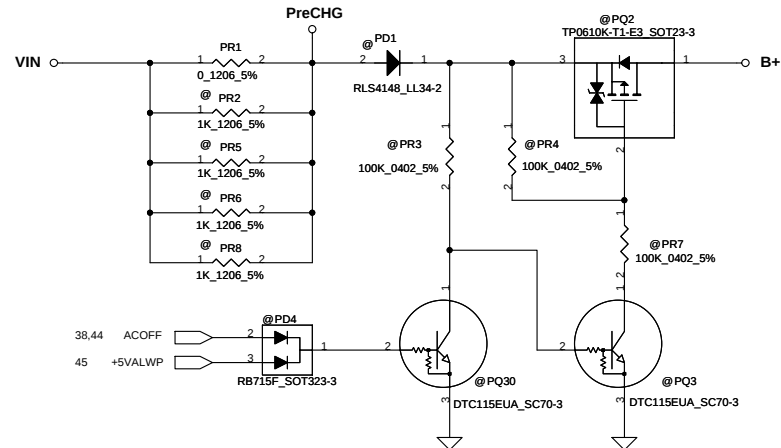
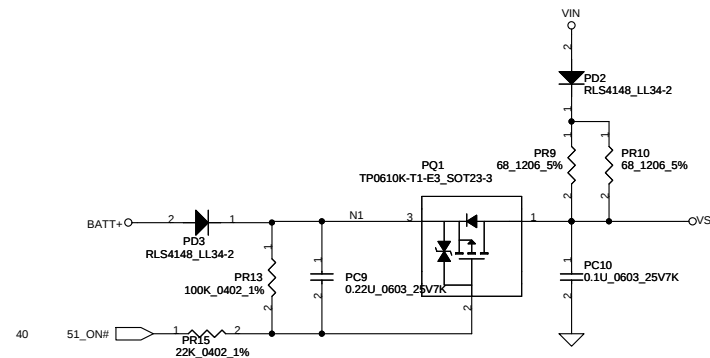
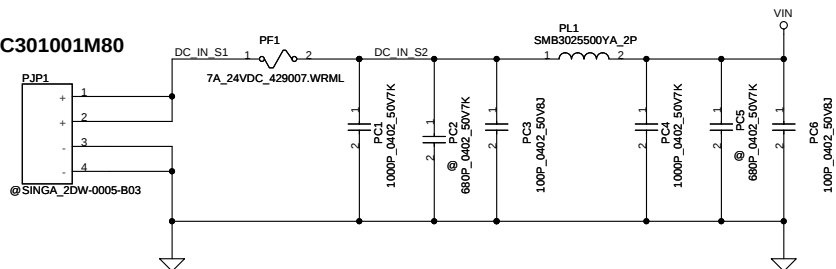


Reserve for EMI test

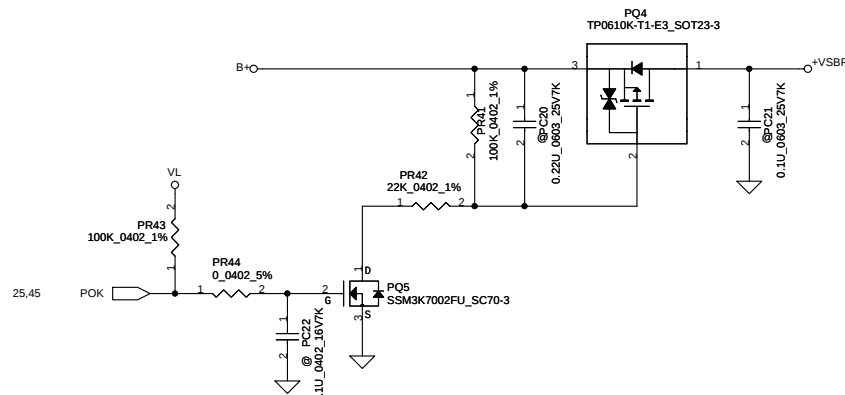
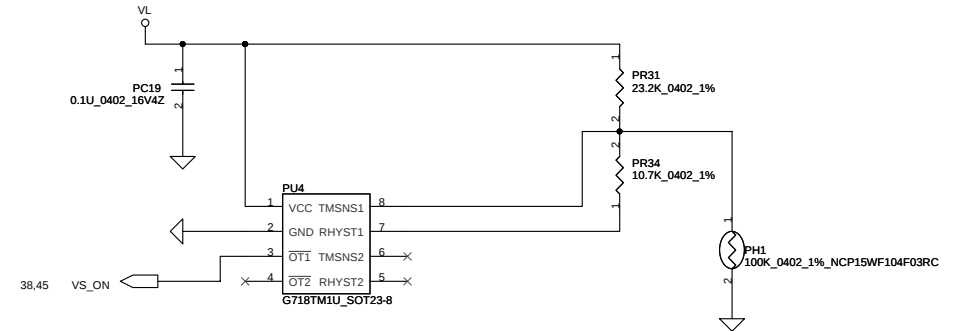
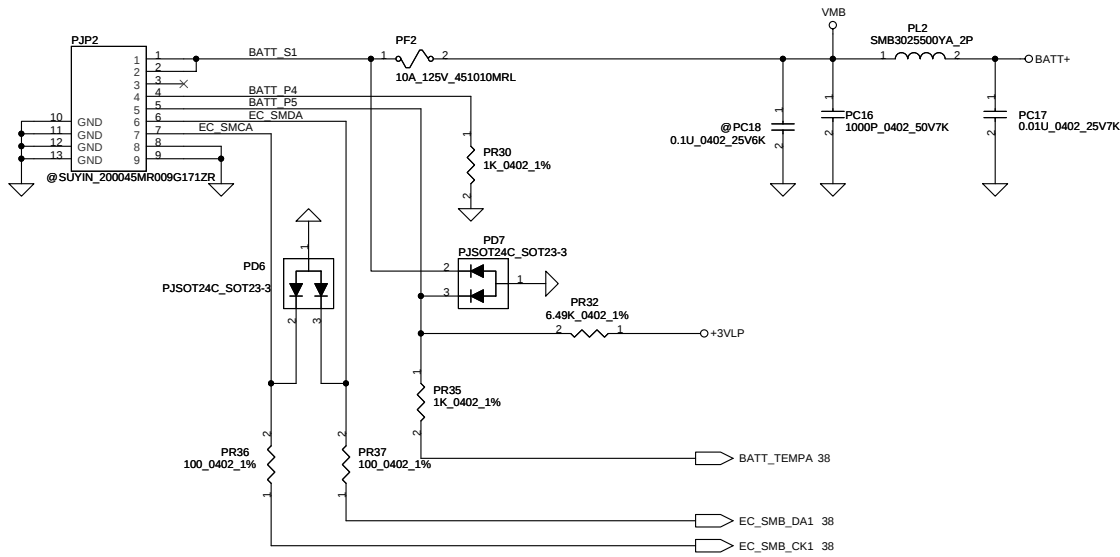


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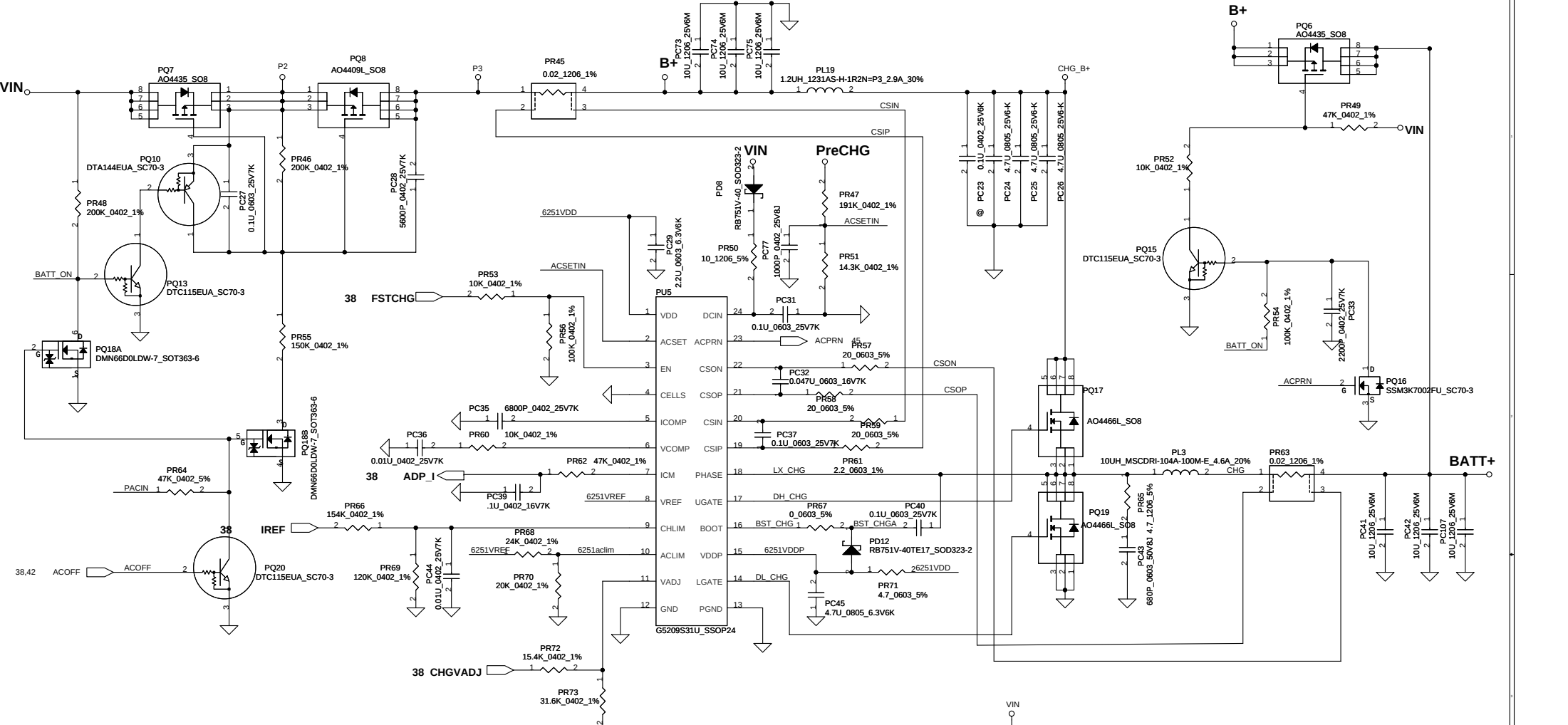
DC301001M80



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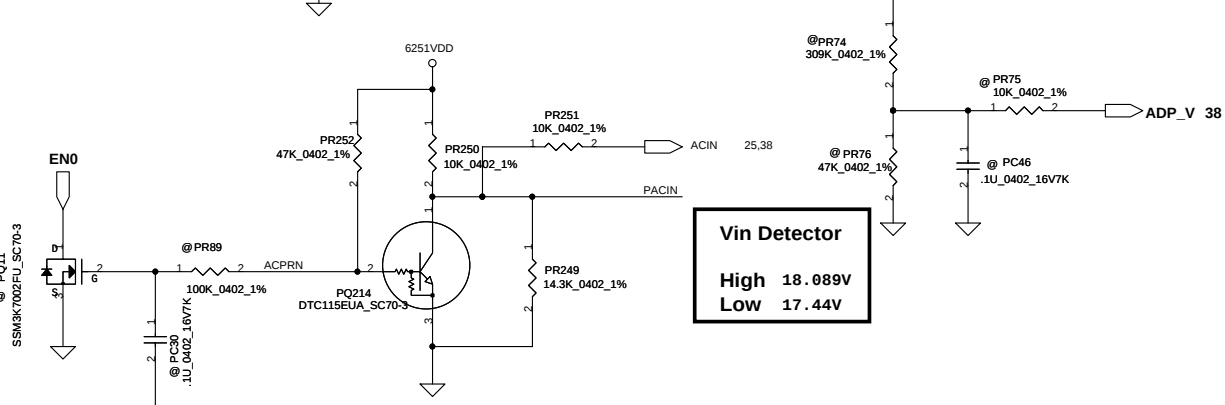


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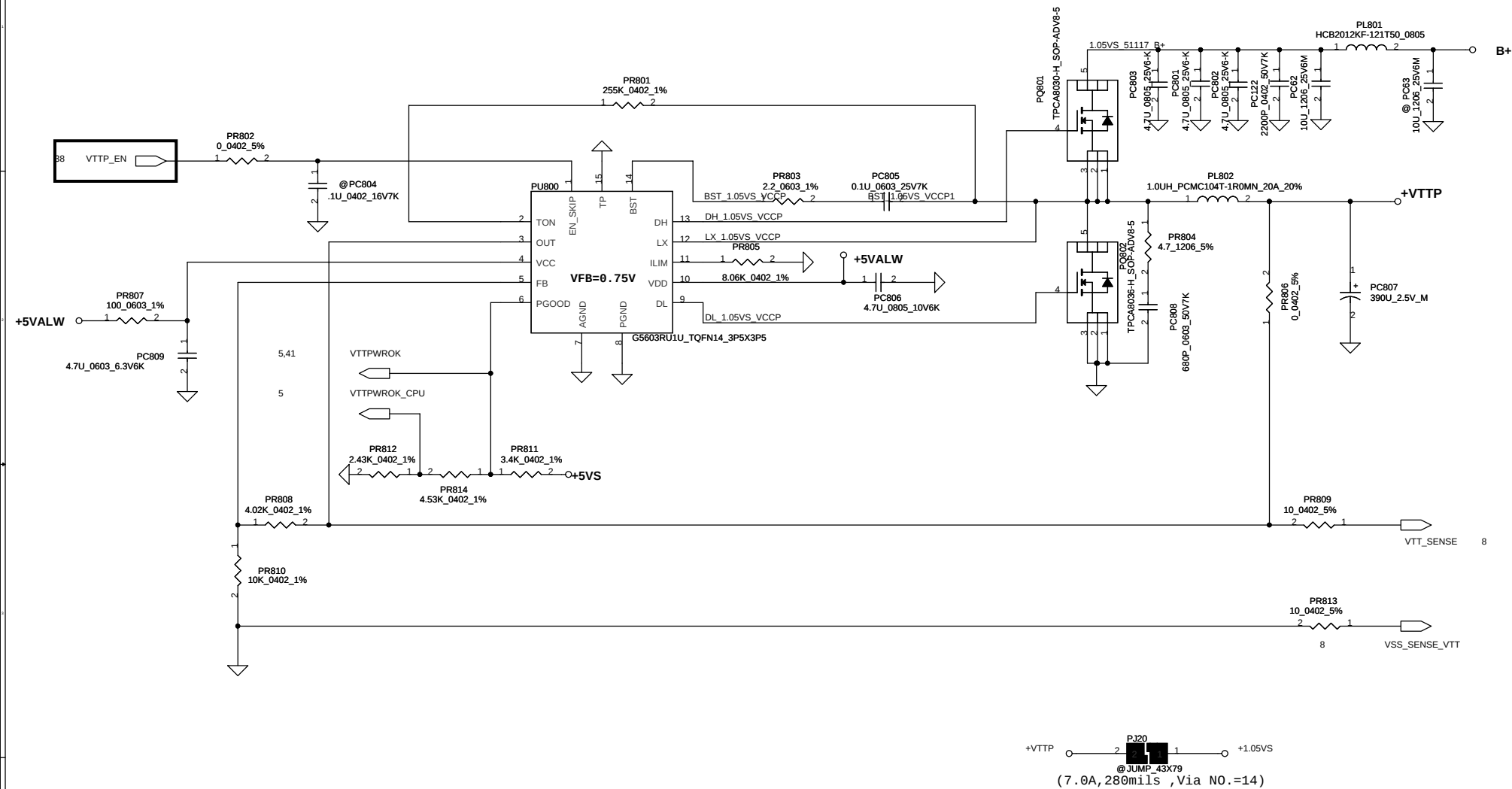


CP mode
 $I_{ada} = 0 \sim 3.42A (65W)$ $CP = 92\% \cdot I_{ada}$; $CP = 3.147A$
 $V_{ac1im} = 1.08V (65W)$ $PR68 = 75k$ $PR45 = 0.02$

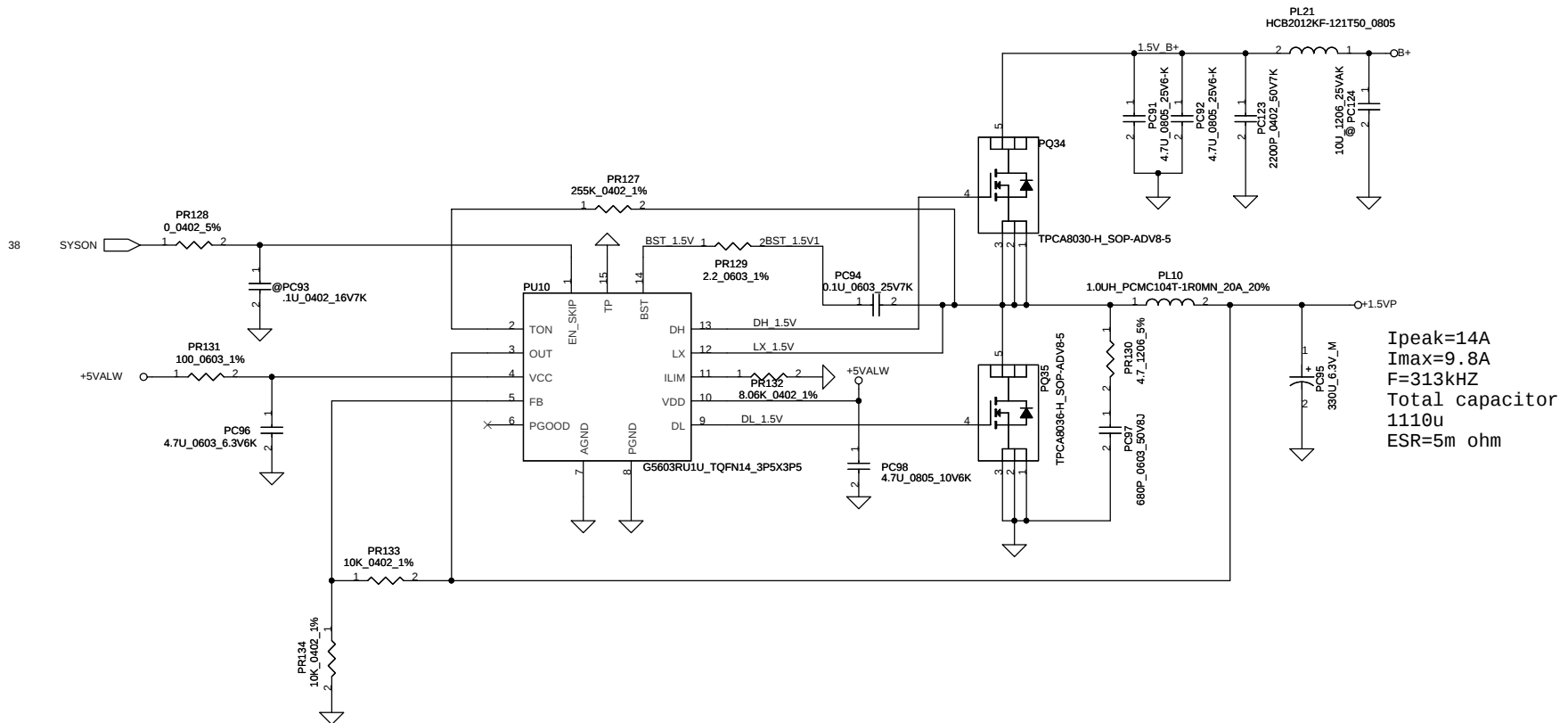
$CC = 0.25A \sim 3A$ $I_{REF} = 1.016 \cdot I_{charge}$ $I_{REF} = 0.254V \sim 3.048V$ V_{CHLIM} need over 95mV	
$CHGVADJ = (V_{cell} - 4) / 0.10627$	
V_{cell}	$CHGVADJ$
4V	0V
4.2V	1.882V
4.35V	3.2935V



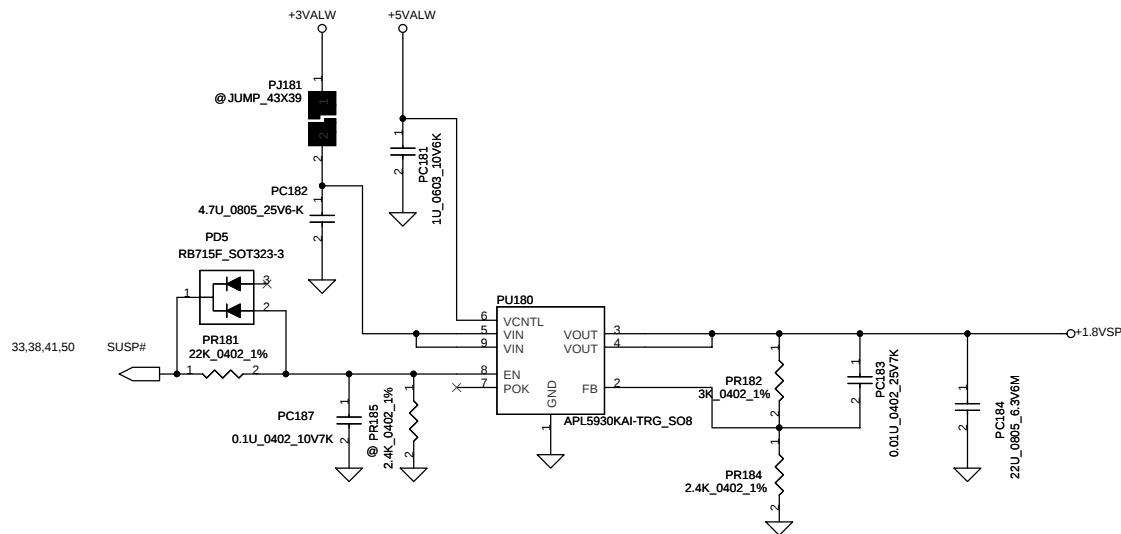
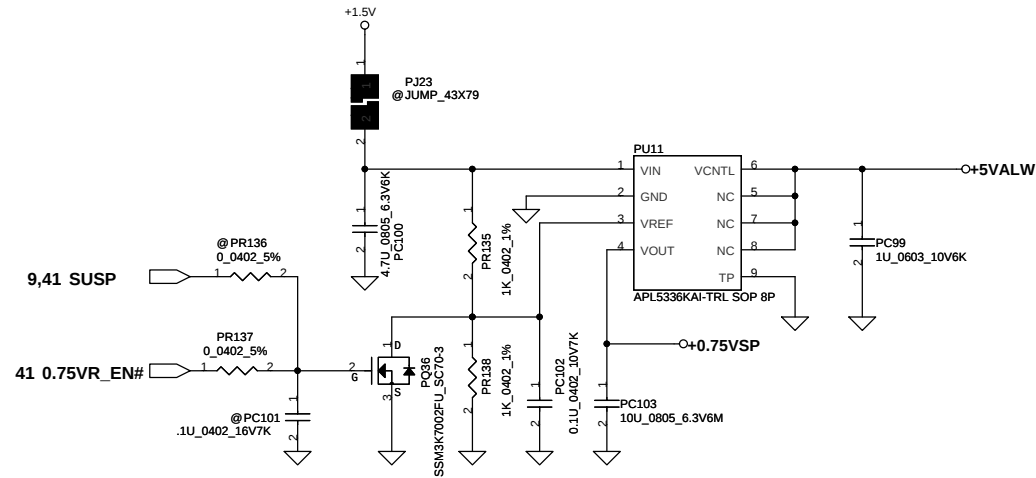
Vin Detector
High 18.089V
Low 17.44V



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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/10/14	42		Remove PR2,PR3,PR4,PR5,PR6,PR7,PR8,PD1,PD4,PQ2,PQ3,PQ30 Change PR1 to 0_1206_5%	Remove Pre charge
2010/10/14	44		Change PQ8 to A04409L,remove PR89,PC30,PQ11 Change PR68 to 24K ohm,add PC107	Remove Pre charge
2010/10/14	45		Change PU6 to TPS51125A	Circuit modify
2010/10/14	46		Change PQ802 to TPCA8036	Circuit modify
2010/10/14	48		Change PU11 to APL5336,PR181 to 15K ohm, add PC187(0.22U)	Circuit modify
2010/10/14	50		Change PR621 to 54.9k ohm,Delete PR104,PC622 Add PR606,PC606	Circuit modify
2010/10/21	45		Add PC64(0.1U_0402_25V)	EMI request
2010/10/21	48		Change PR181 to 22k ohm,PC187 to 0.1UF,add PD5	HW request
2010/10/21	50		Change PR605 to 2.2 ohm,PR635,PR637 to 5.1Kohm,PR103 to 2Kohm Add PC190	HW request

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PIR (Product Improve Record)

PWWAA LA-6847P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0

NO DATEPAGEMODIFICATION LISTPURPOSE

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