

COMPAL CONFIDENTIAL

MODEL NAME : VAUA0
PCB NO : LA-9591P (DAA00005W10)
BOM P/N : 4319LK31L01
GPIO MAP: 3.0

Goliad 14"

Haswell ULT

2013-05-17

REV : 1.0 (A00)

- @ : Nopop Component
- 1@ : M/B SPI ROM
- 2@ : TAA/B SPI ROM
- EMC@ : EMI, ESD and RF Component
- XDP@ : XDP Component
- CONN@ : Connector Component
- 3@ : M/B for non support WWAN
- 4@ : M/B SPI 4M ROM Component
- 5@ : TAA/B SPI 4M ROM Component
- 7@ : M/B for Non-Vpro

	SPI on M/B	TAA
Vpro	1@/3@/4@/EMC@	2@/3@/5@/EMC@
non-Vpro	1@/EMC@	2@/EMC@

MB PCB	
Part Number	Description
DAA00005W10	PCB 0VN LA-9591P REV1 M/B

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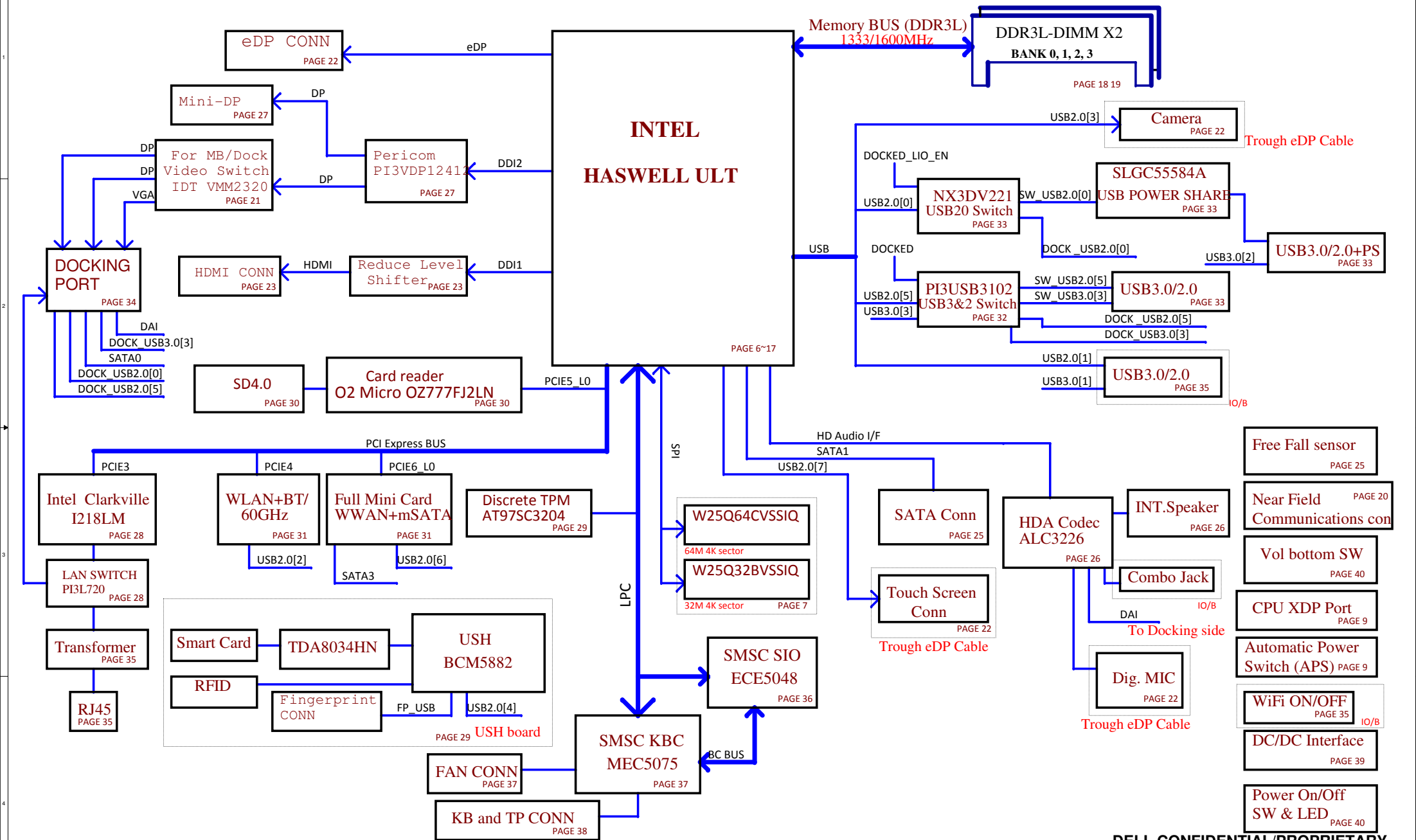
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Title
Cover Sheet

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Goliad 14 Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and
PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB3-->IO-->Right
	USB3.0 2		JUSB1-->Rear left
PCIE 1	USB3.0 3		JUSB2-->Rear Right//DOCK
PCIE 2			
PCIE 3			LOM
PCIE 4			WLAN (WiGi)
PCIE 5			MMI (CARD READER)
PCIE 6		SATA 3	WWAN(PP/mSATA)
		SATA 2	NA
		SATA 1	HDD
		SATA 0	DOCK

HSW ULT	USB PORT#	DESTINATION
	0	JUSB1 // E-Dock 1
	1	IO/ JUSB3
	2	WLAN + BT
	3	CAMERA
	4	USH->SMART CARD
	5	JUSB2 // E-Dock 2
	6	WWAN
	7	TOUCH

USH	0	BIO
	1	NA

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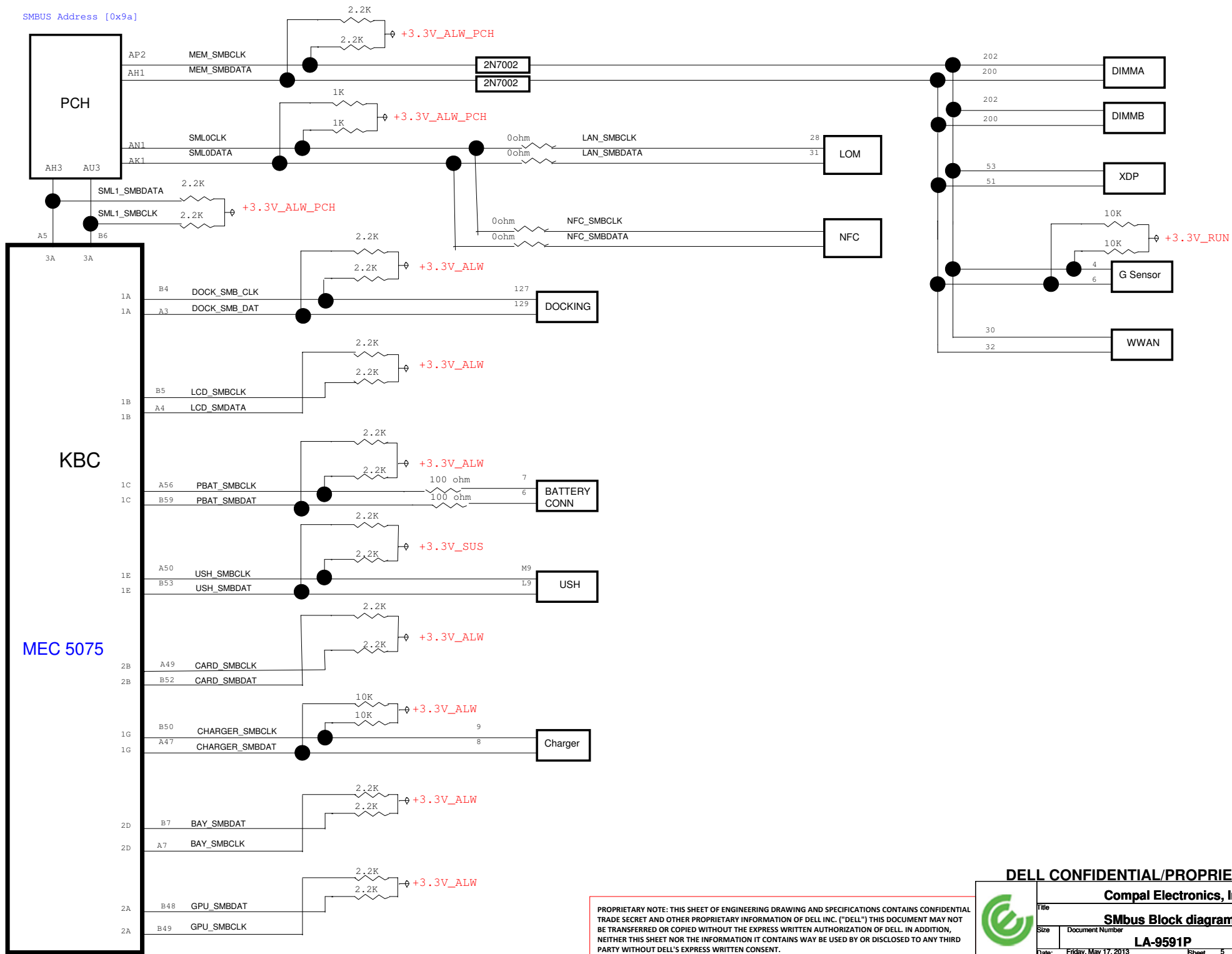
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SMBUS Address [0x9a]



MEC 5075

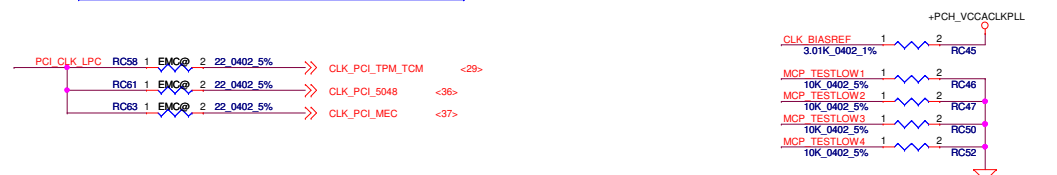
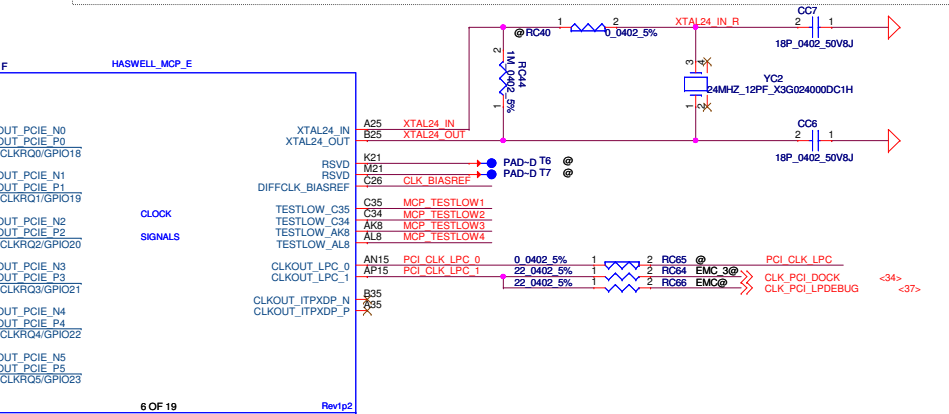
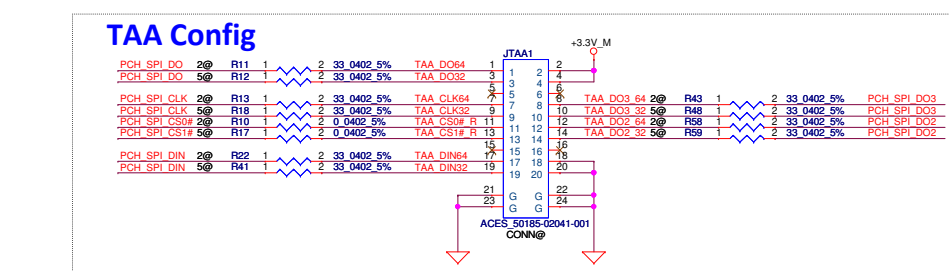
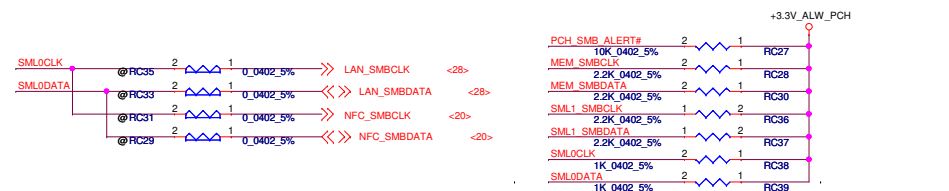
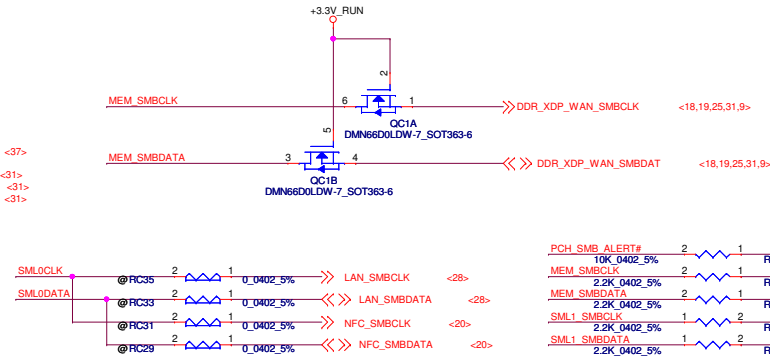
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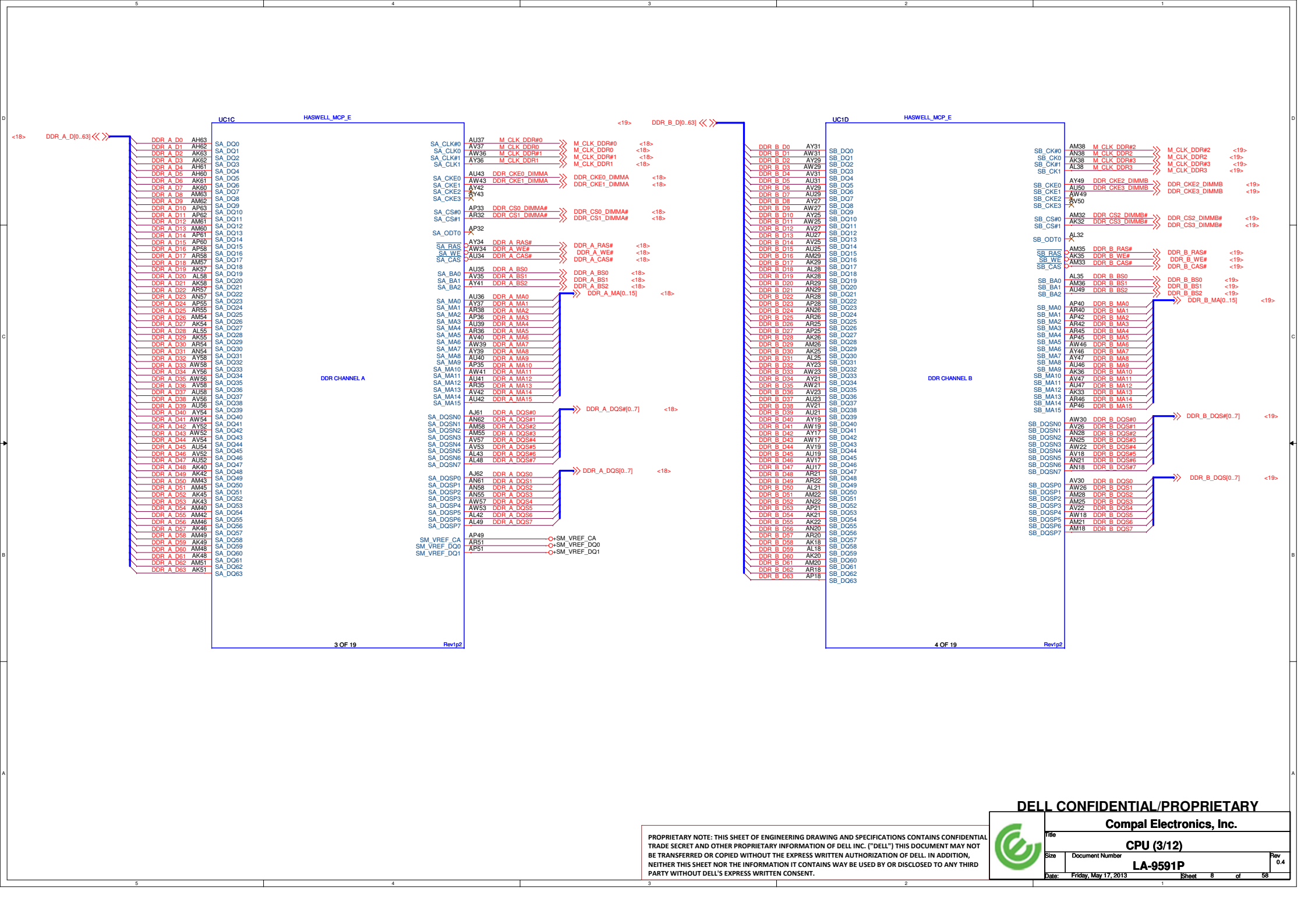
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Title			
SMBus Block diagram			
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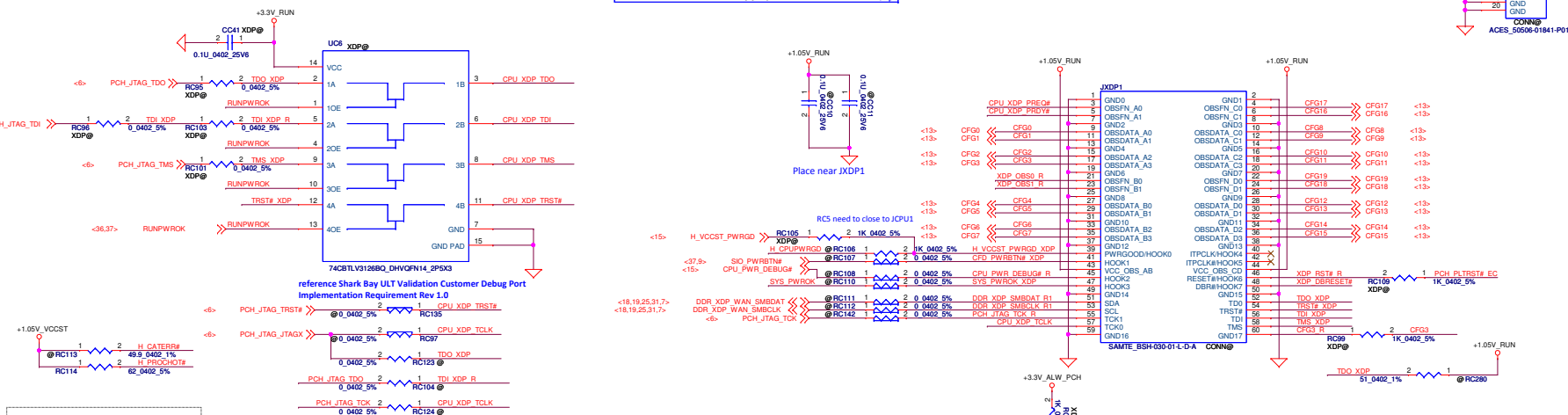


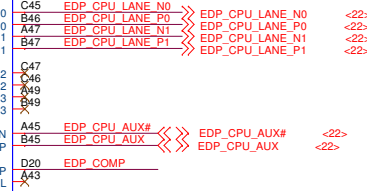
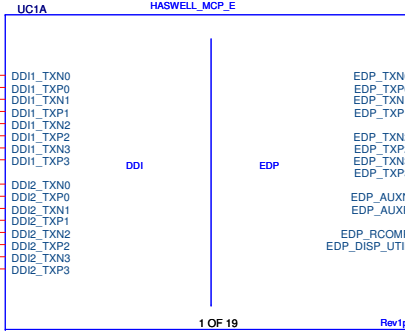
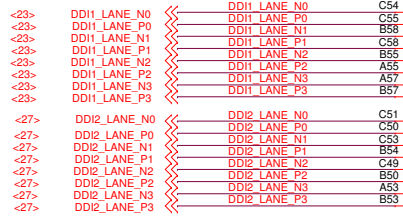
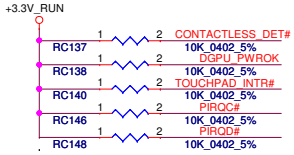
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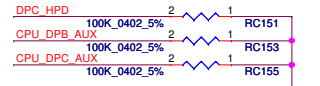
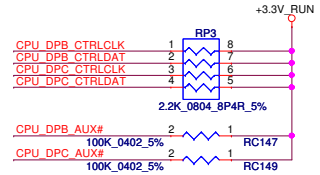
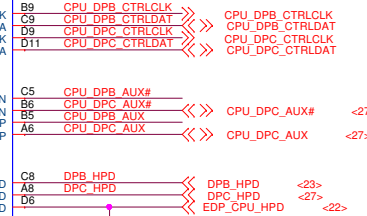
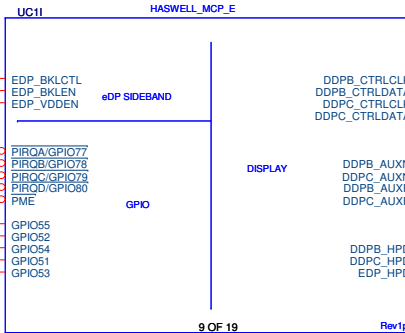
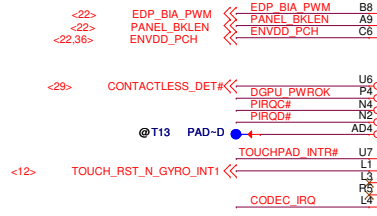
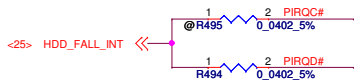
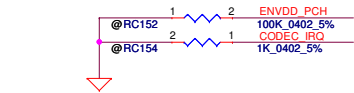
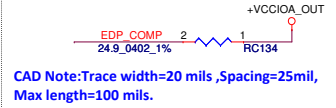
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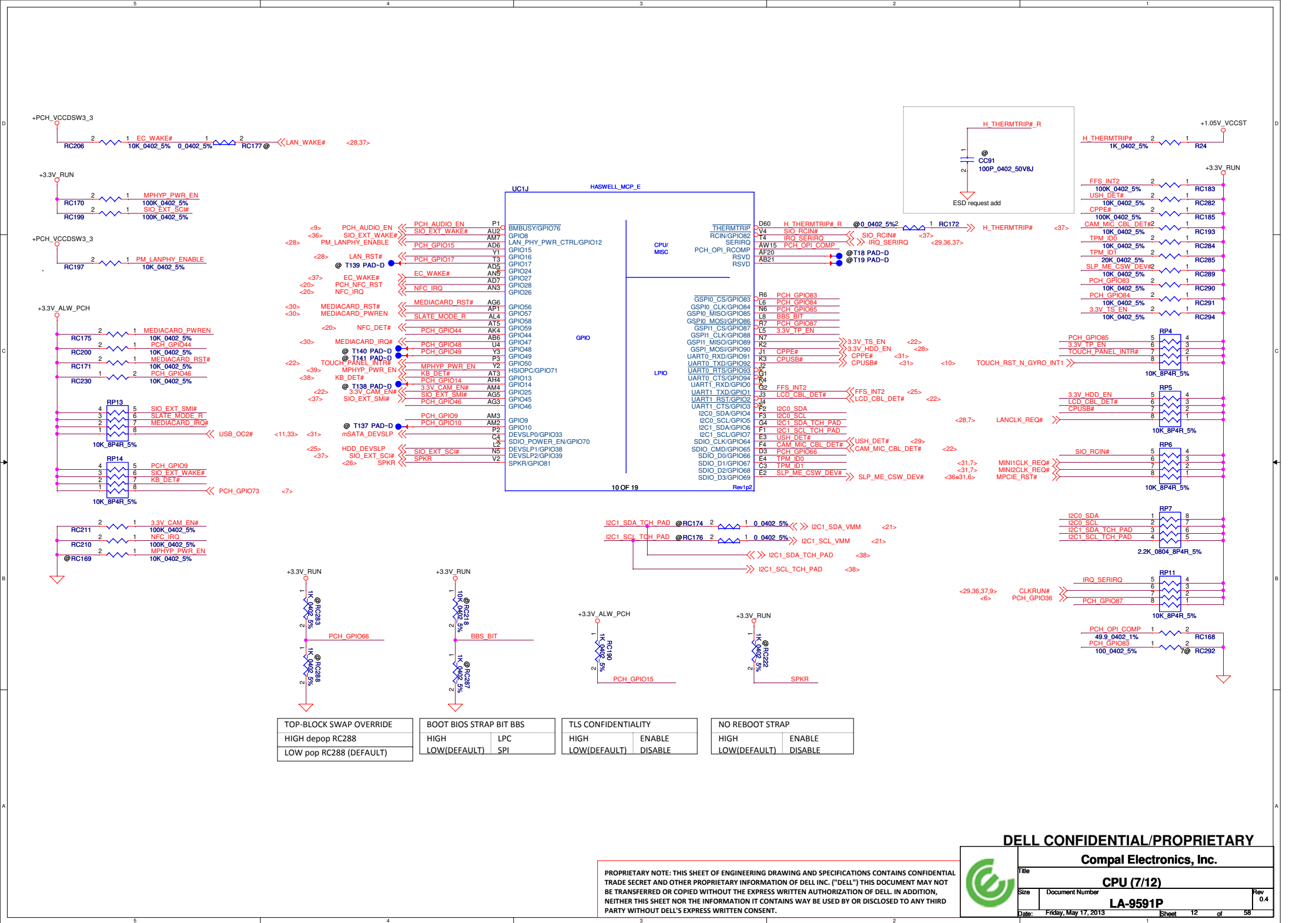


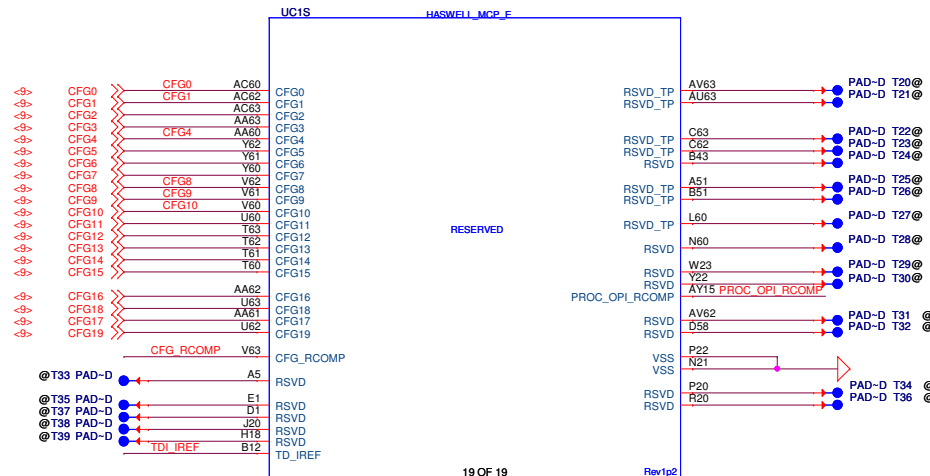


COMPENSATION PU FOR eDP

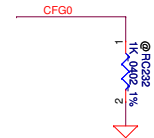


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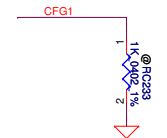




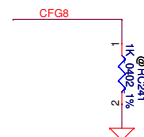
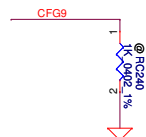
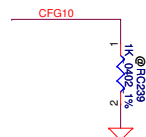
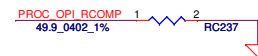
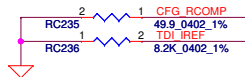
CFG STRAPS for CPU



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed



PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed



SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0:Disable Noa will be available pegrardless of the locking of the unit

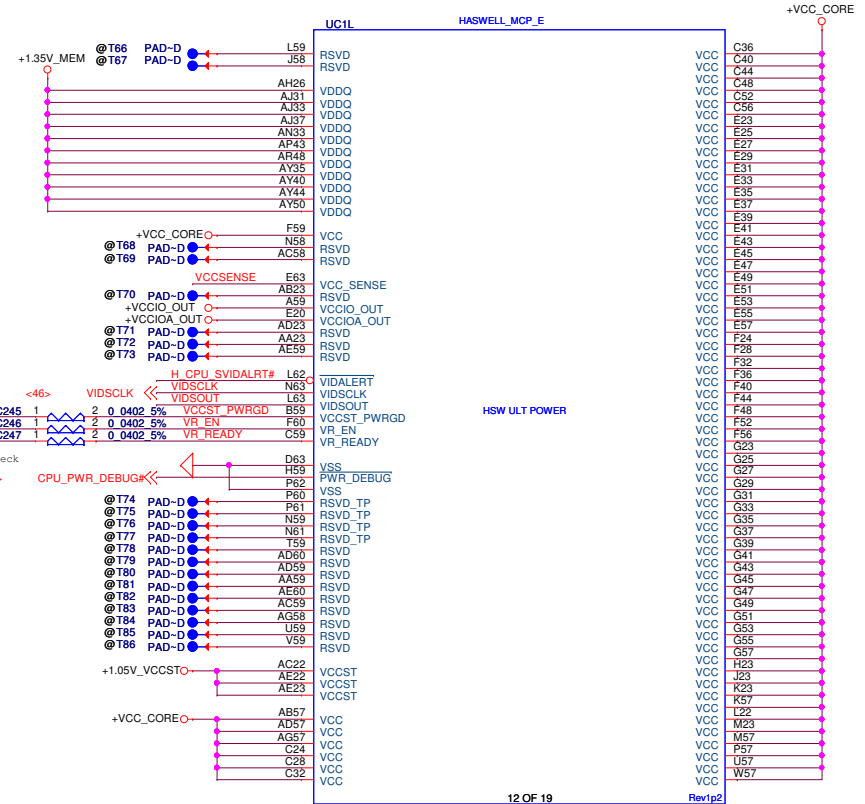
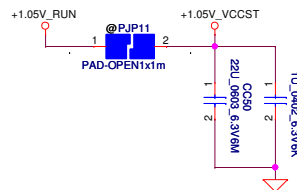
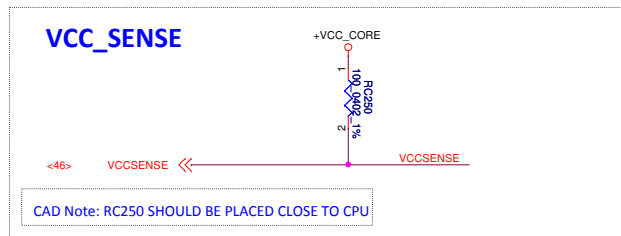
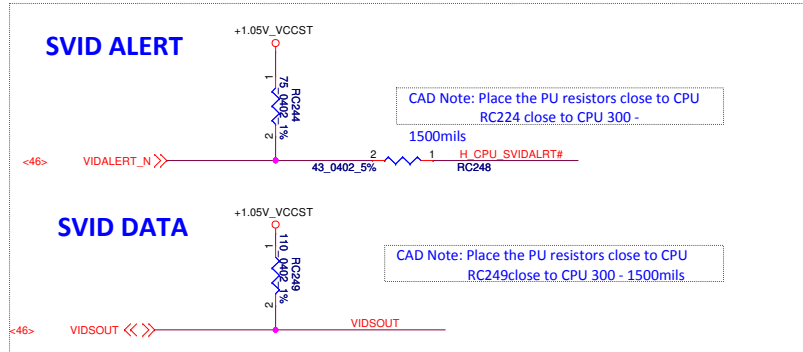
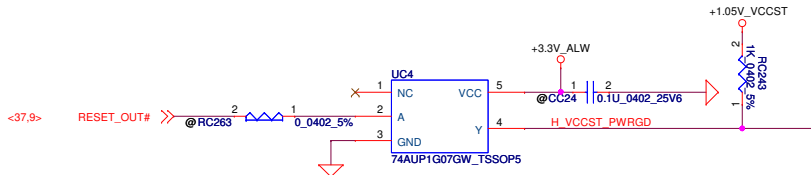
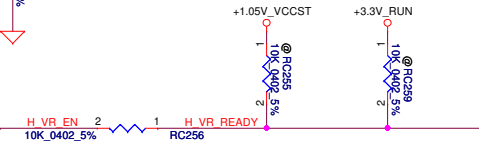
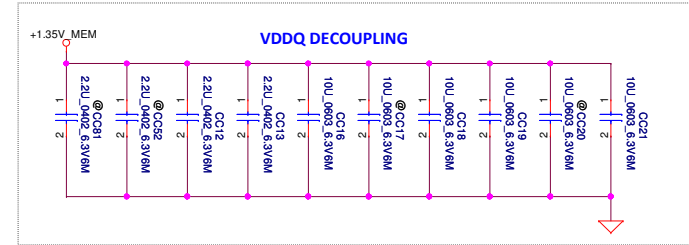
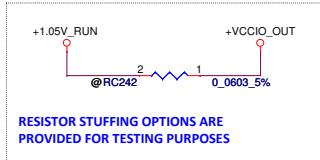
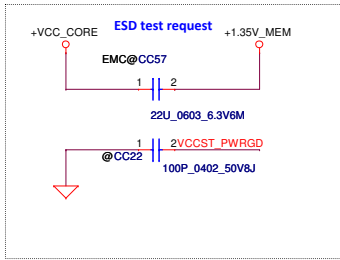
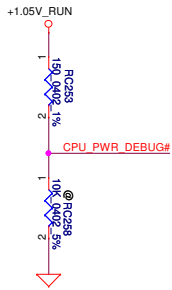
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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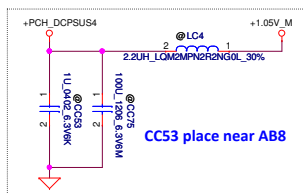
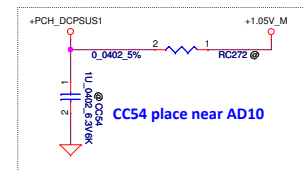
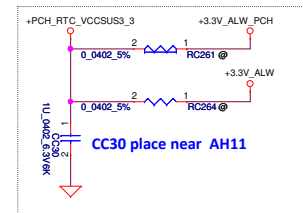
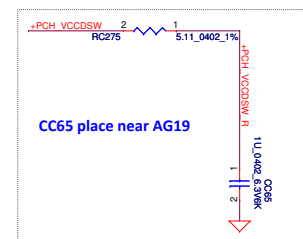
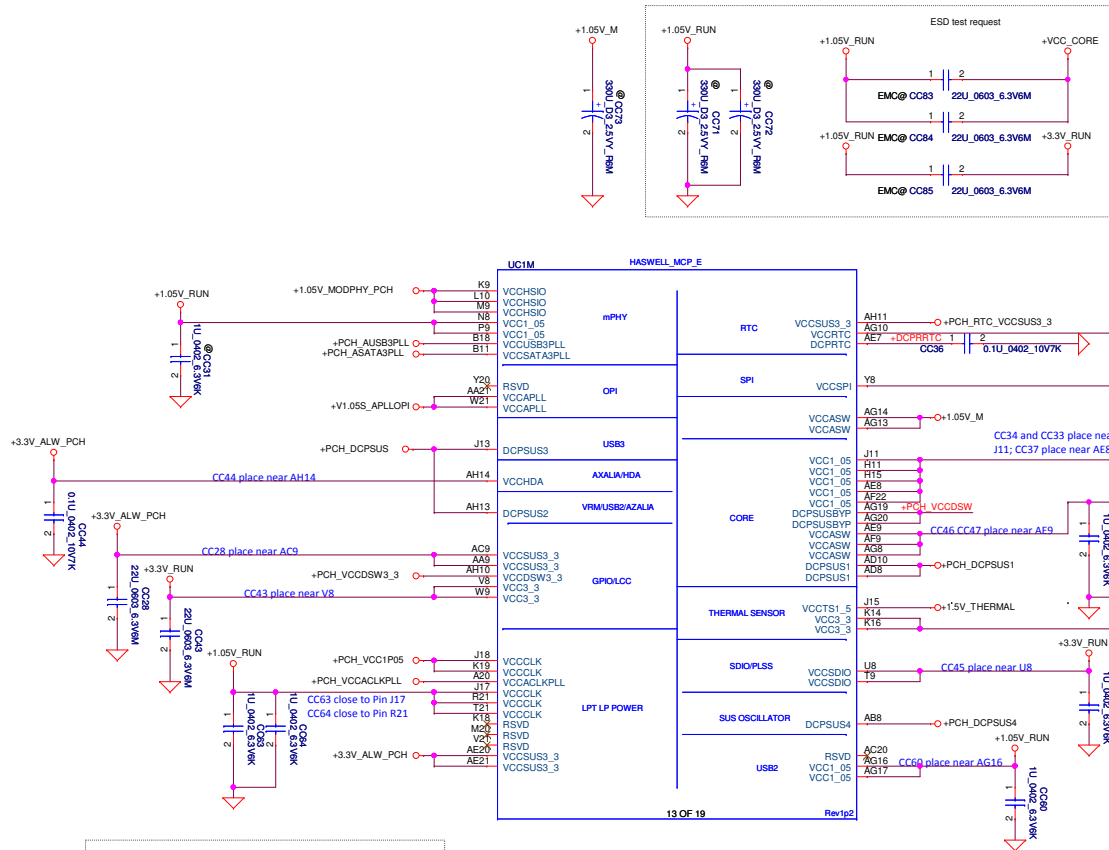
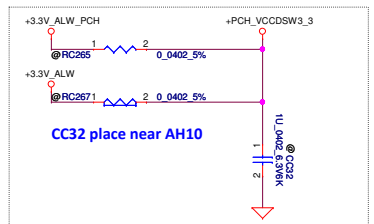
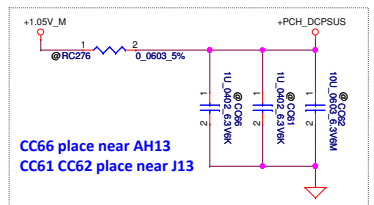
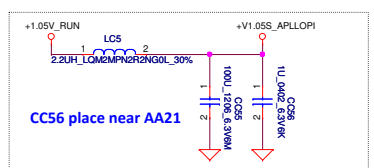
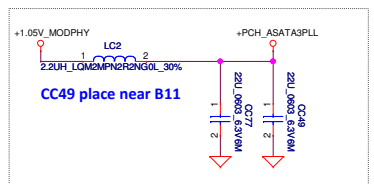
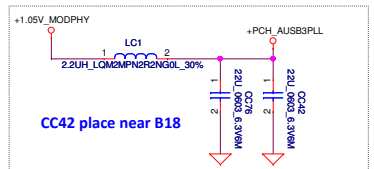
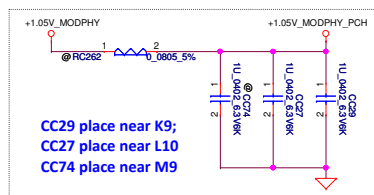


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CPU (8/12)		
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Voltage Rail	Voltage (V)	S0 Iccmax Current (A) ³	Sx Iccmax Current (A) ³	Deep Sx Iccmax (A) ³	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	<1 mA	0	0
VCCUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1 ⁴	1.05	0.109	0.014	0	0
DcpSus2 ⁴	1.05	0.025	0.001	0	0
DcpSus3 ⁴	1.05	0.010	0.003	0	0
DcpSus4 ⁴	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 μ A See note 1, 2

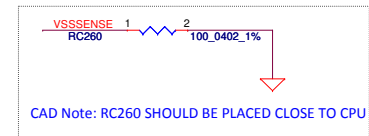
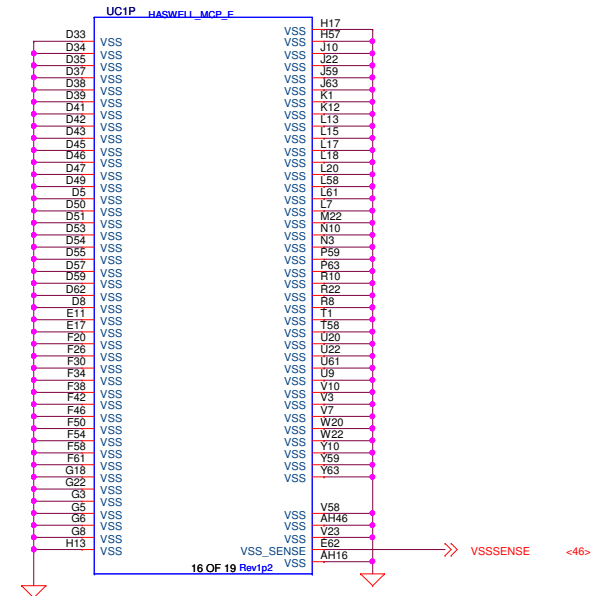
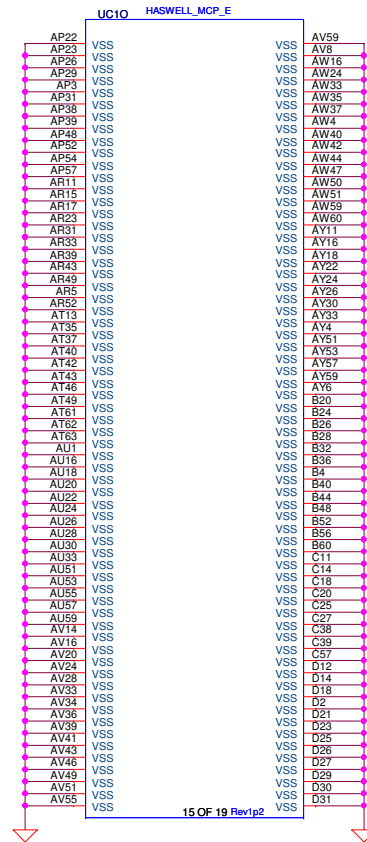
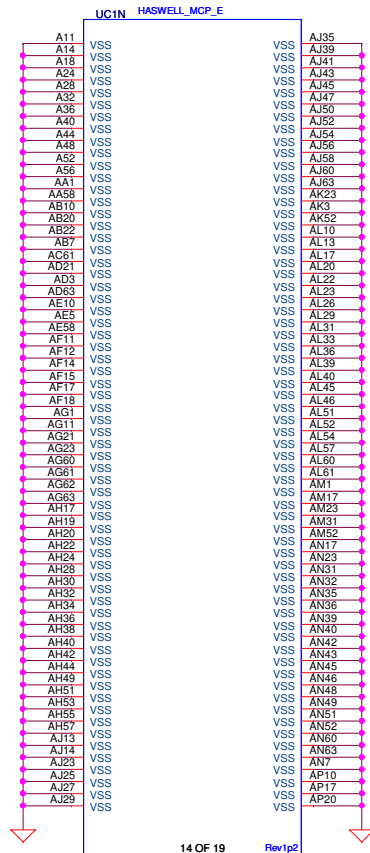
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	LA-9591P	0.4	
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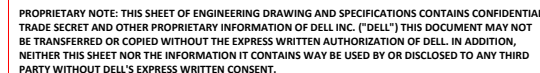
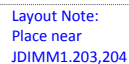
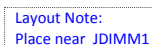
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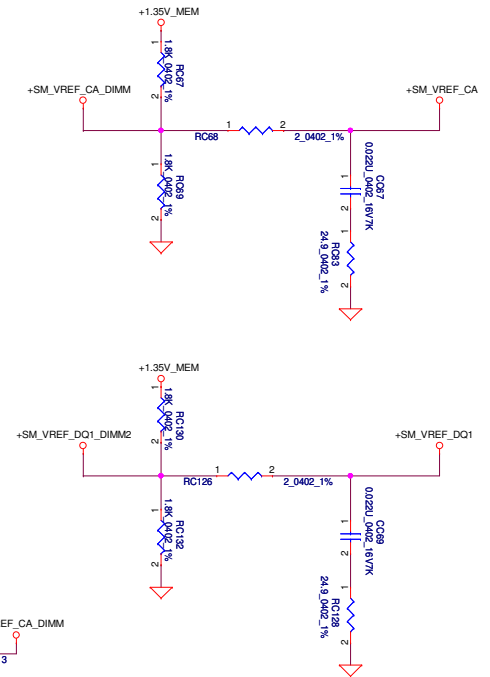
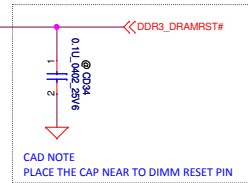
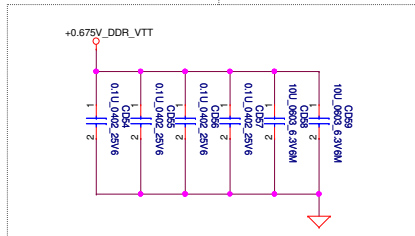
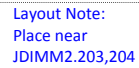
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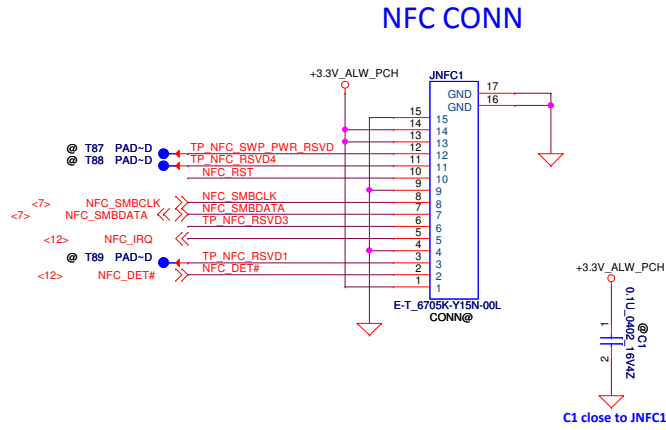
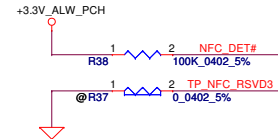
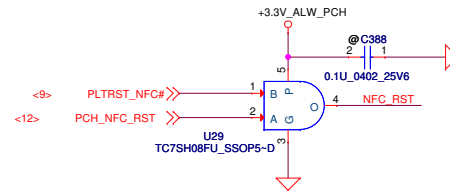




Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



Title			
DDR3L			
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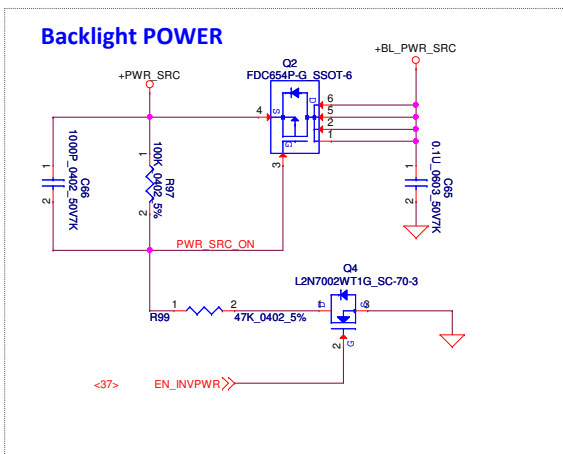
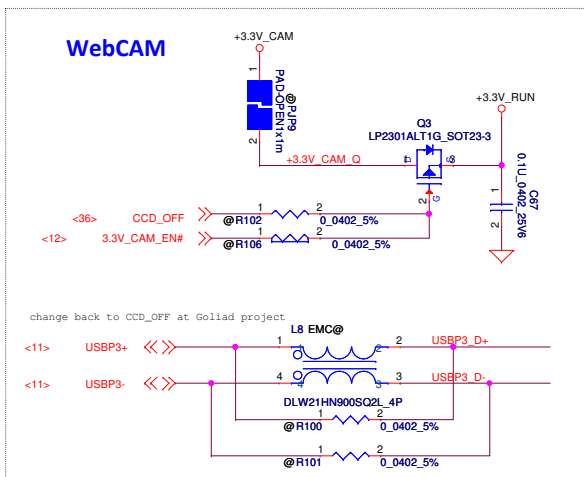
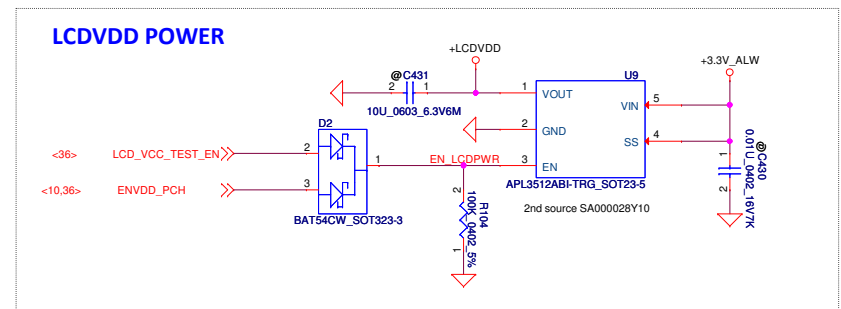
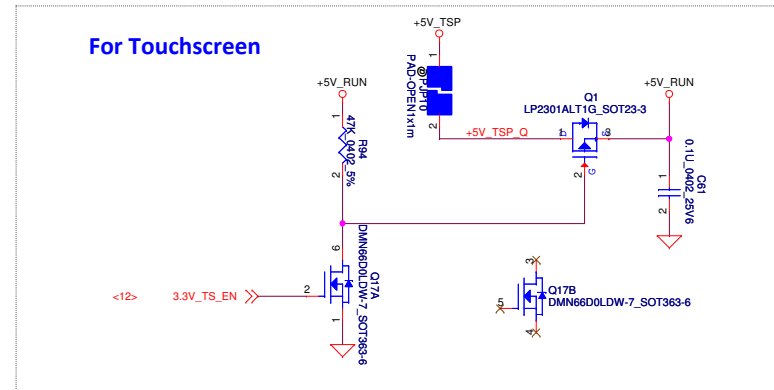
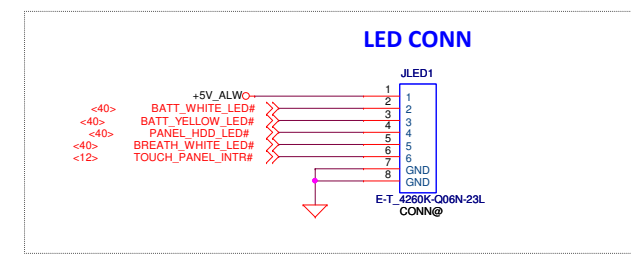
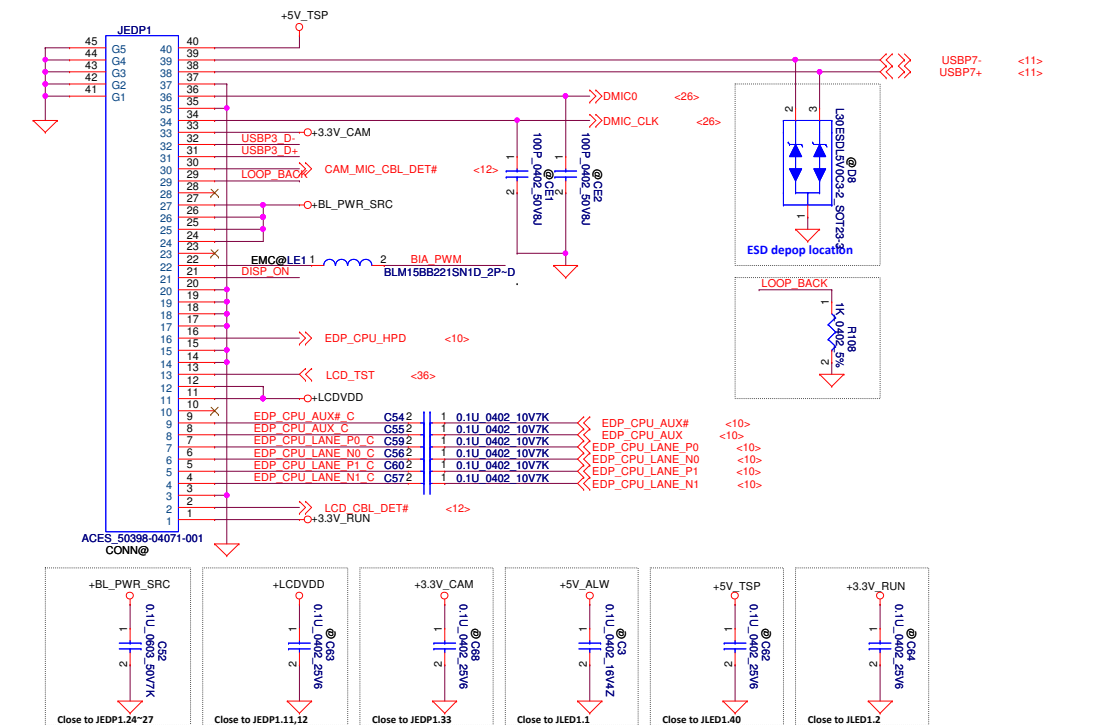
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NFC

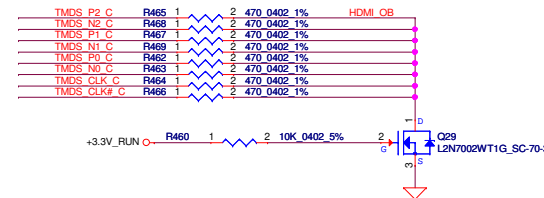
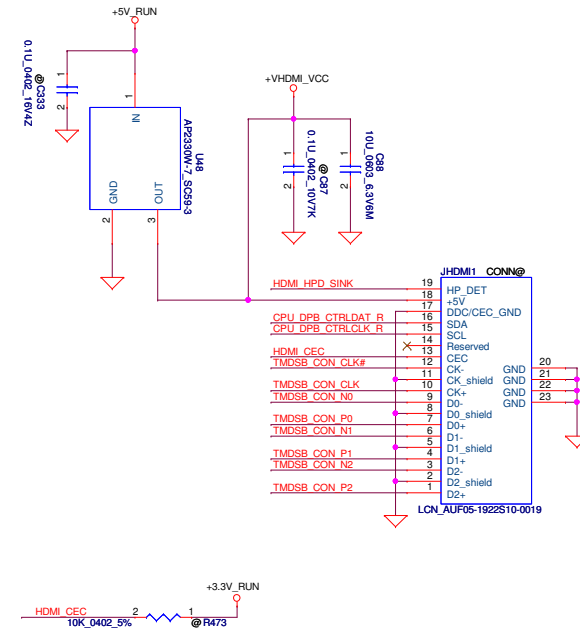
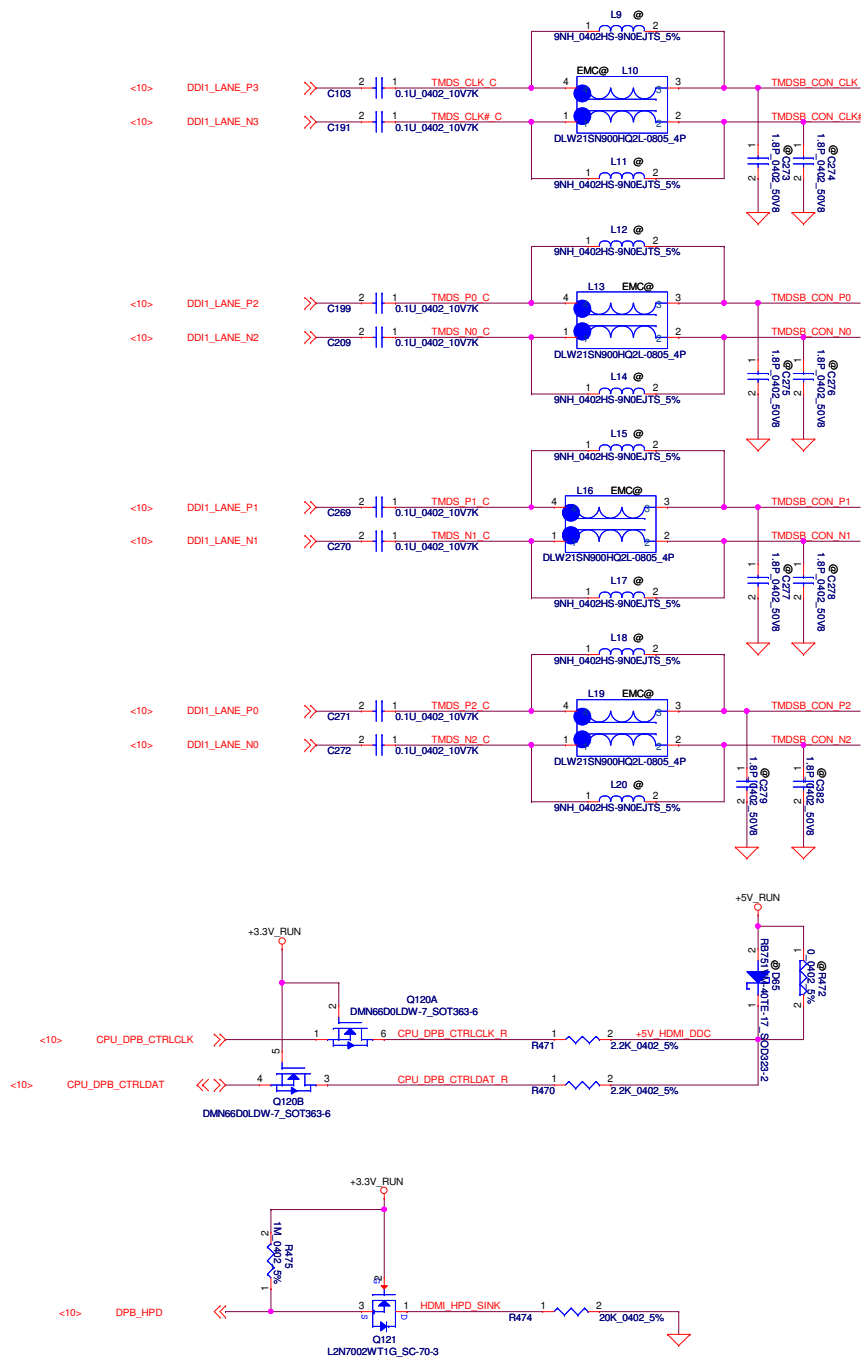
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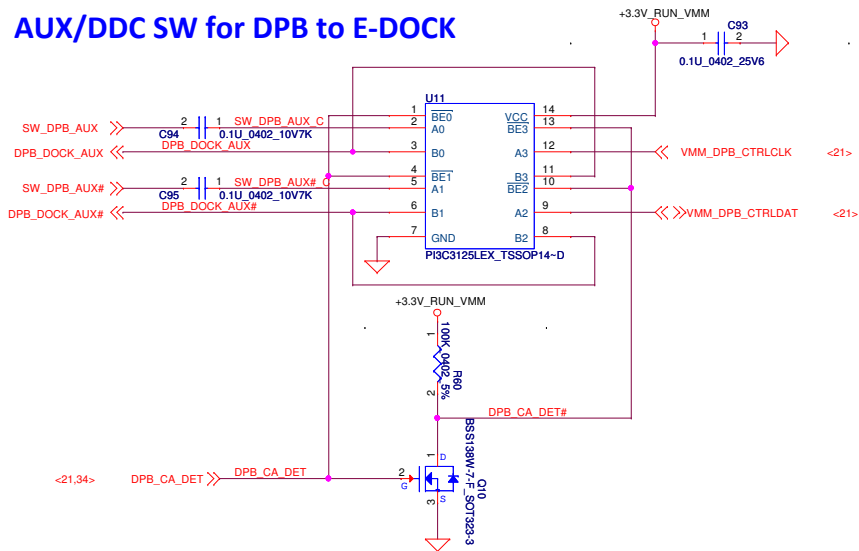
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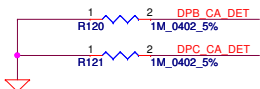
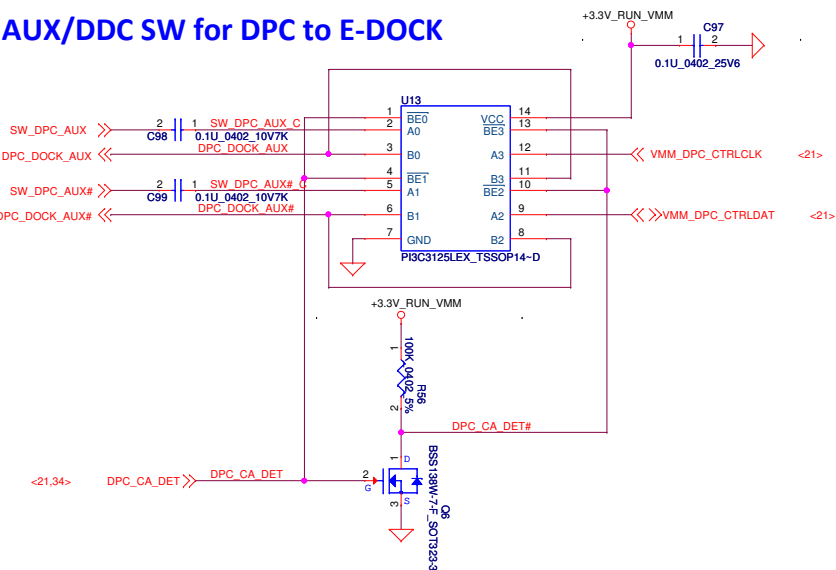
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Title			
HDMI CONN			
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AUX/DDC SW for DPB to E-DOCK



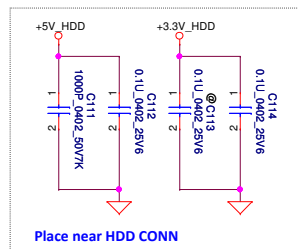
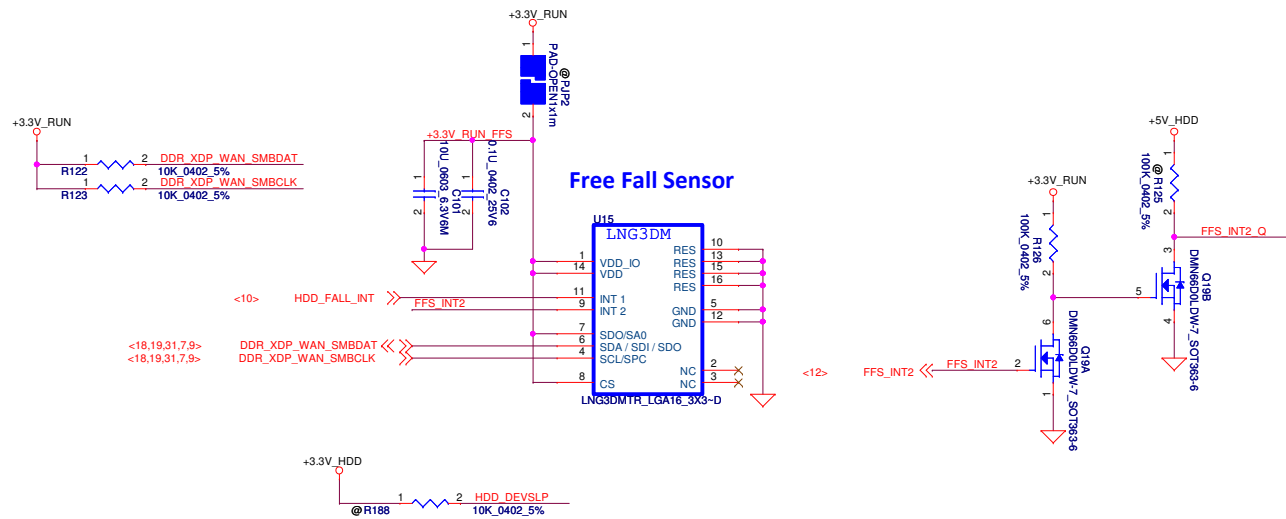
AUX/DDC SW for DPC to E-DOCK



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Title			
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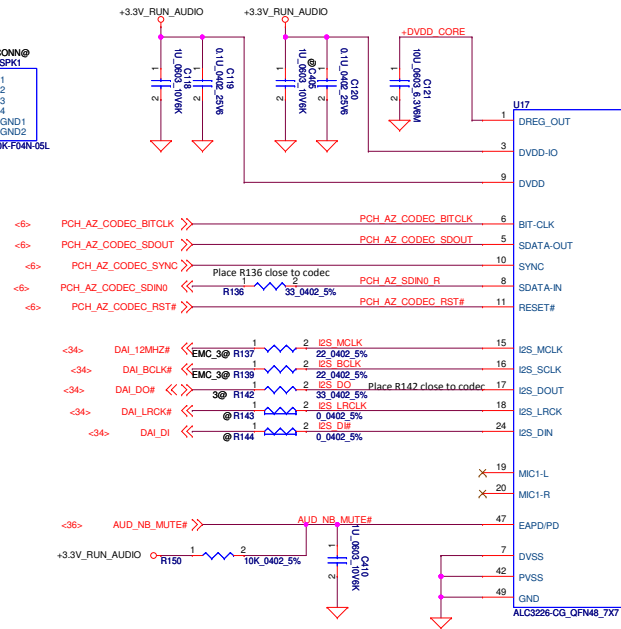
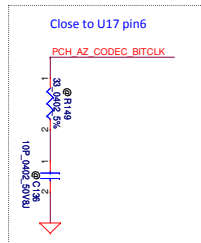
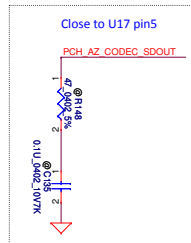
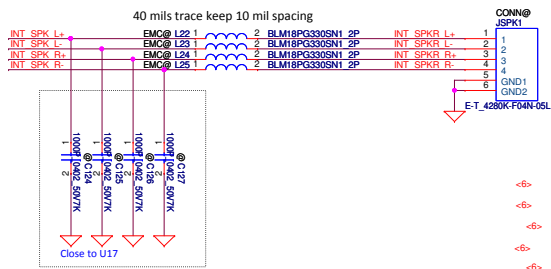
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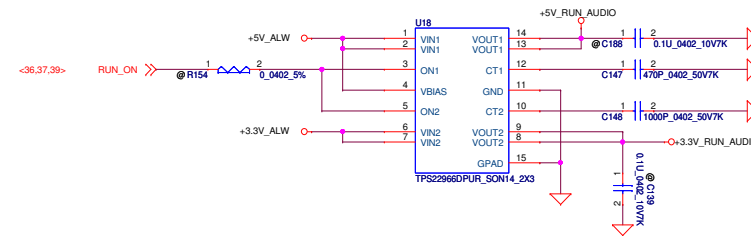
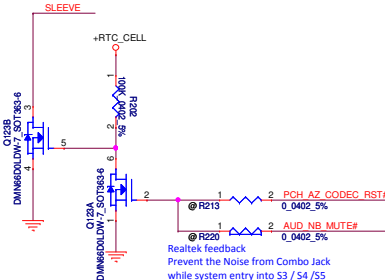
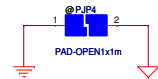
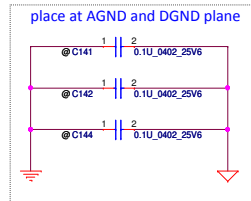
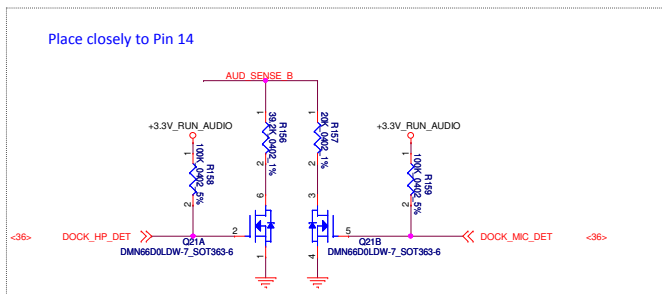
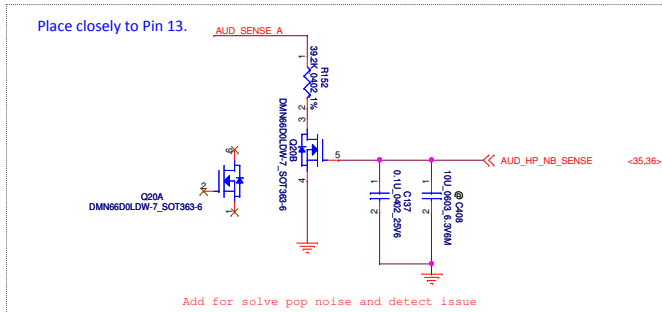
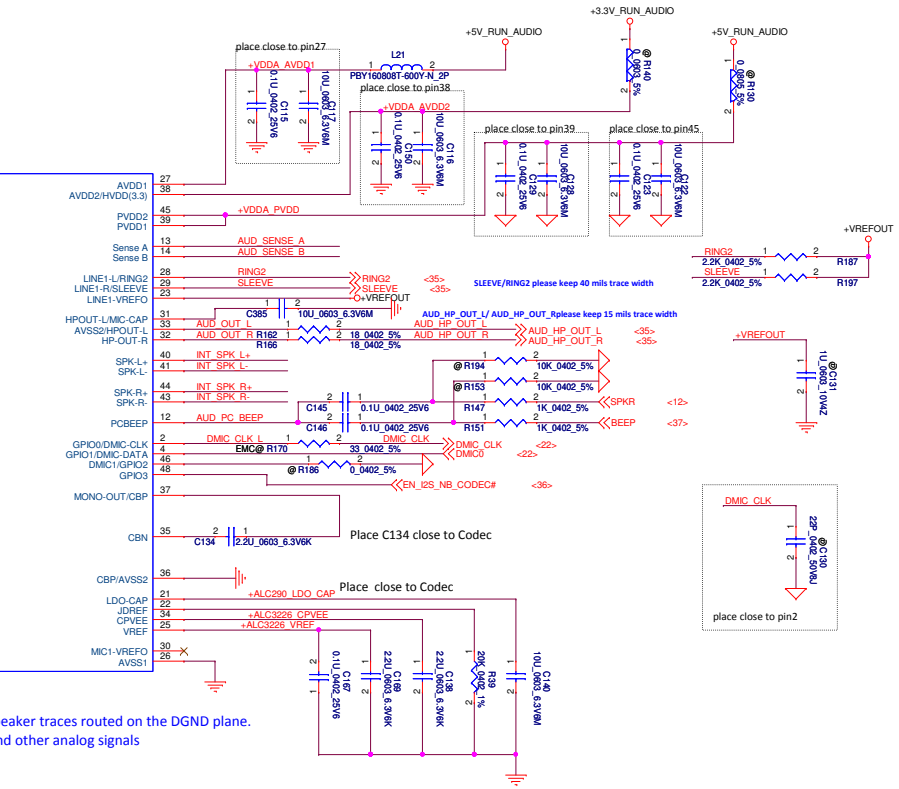
Compal Electronics, Inc.			
Title			
HDD CONN			
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Internal Speakers Header



Notes:

- Keep PVDD supply and speaker traces routed on the DGND plane.
- Keep away from AGND and other analog signals



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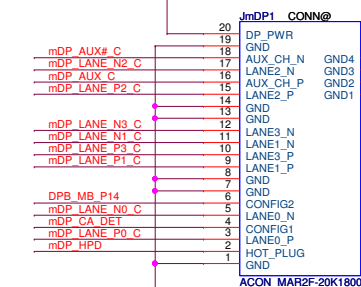
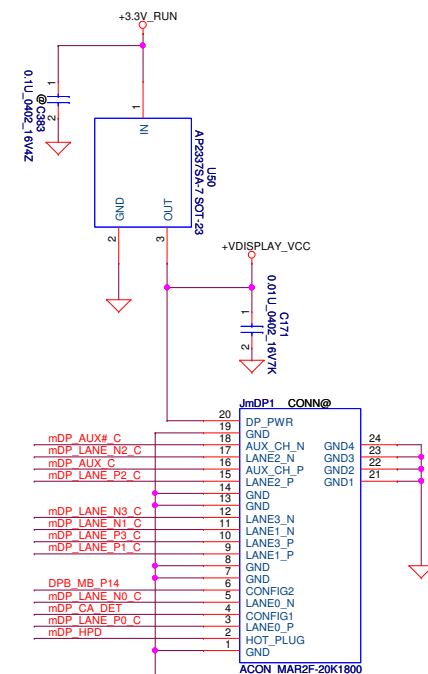
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Codec ALC3226**LA-9591 F**

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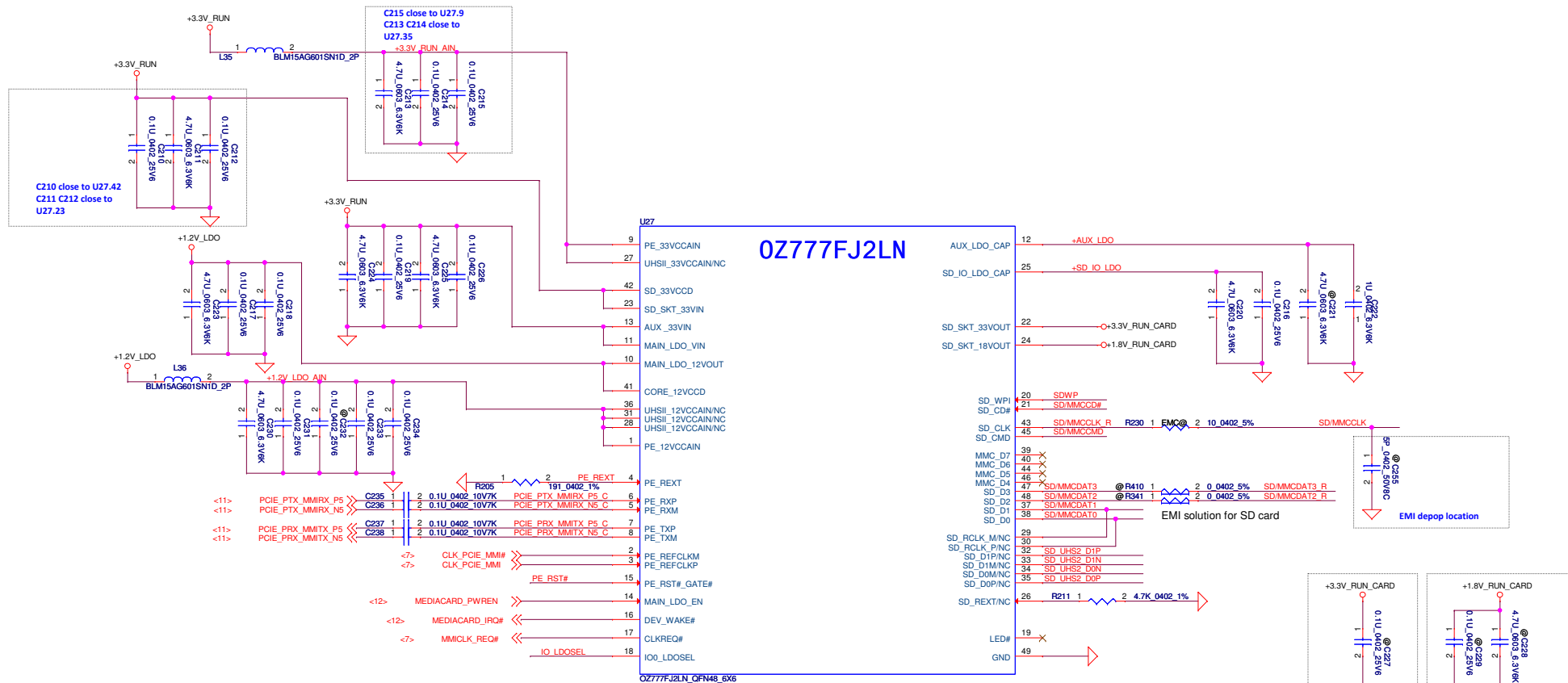
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Friday, May 17, 2013

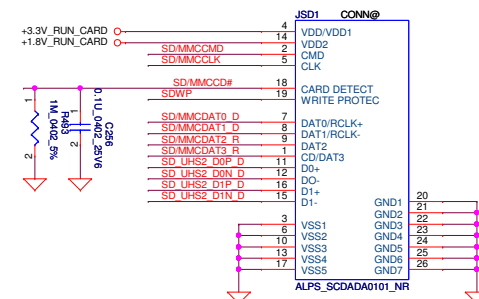
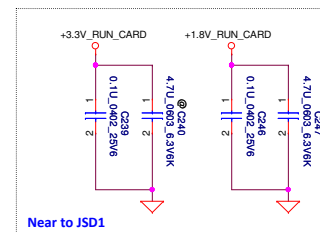
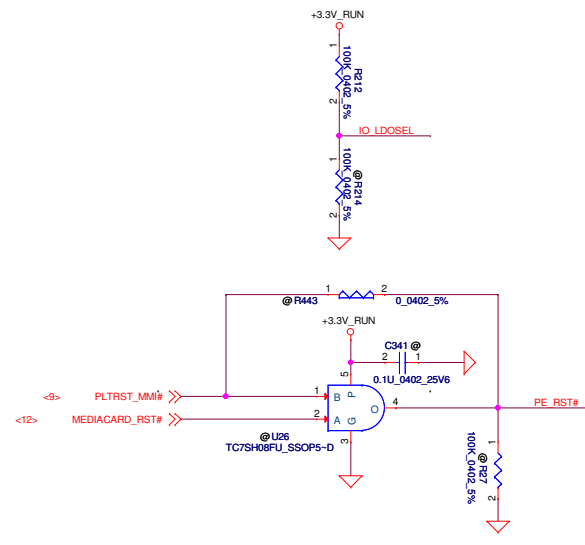
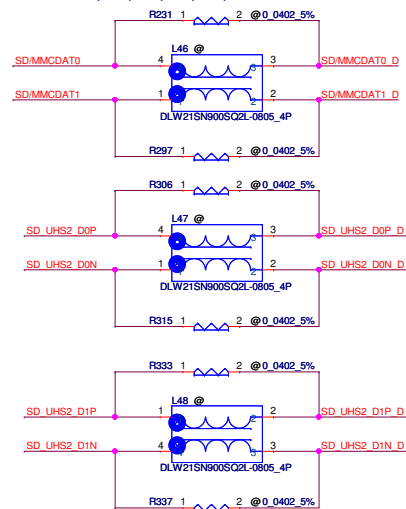
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please routing daisy chain
 1. from U27.38 (SD_D0) -> U27.32 (SD_RCLK_P) -> L46.4
 2. From U27.37 (SD_D1) -> U27.33 (SD_RCLK_N) -> L46.1

R231, R297, R306, R315, R333, R337 for EMI solution



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Card Reader

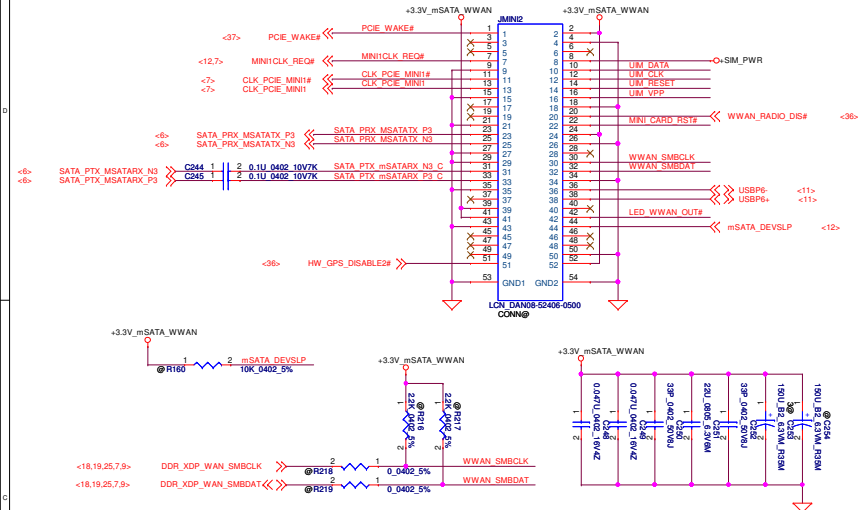
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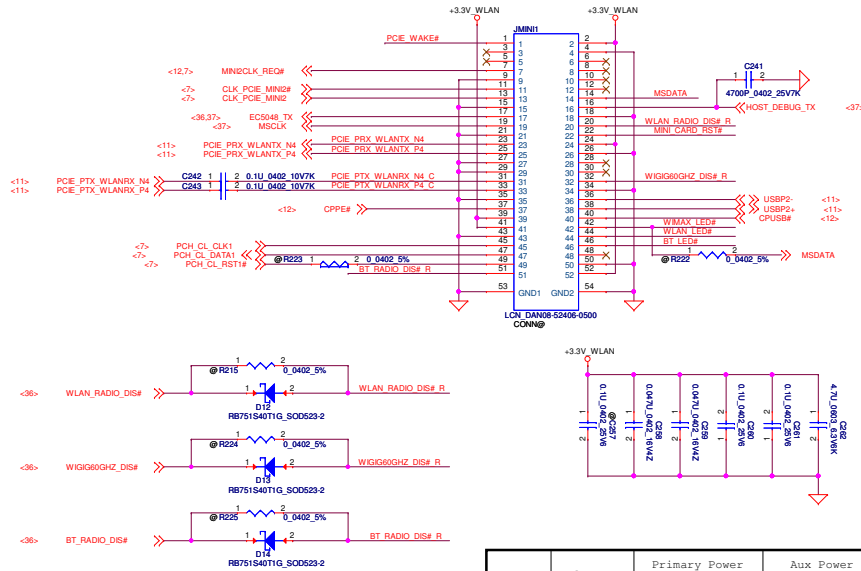


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Mini WWAN/GPS/LTE/mSATA/PP H=4

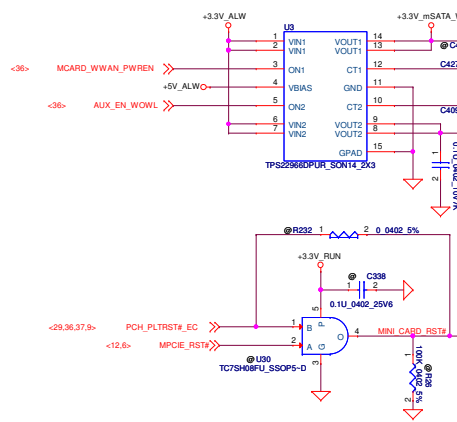
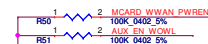
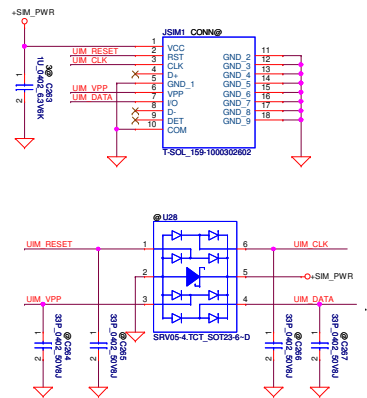


Mini WLAN/WiFi/BT H=4

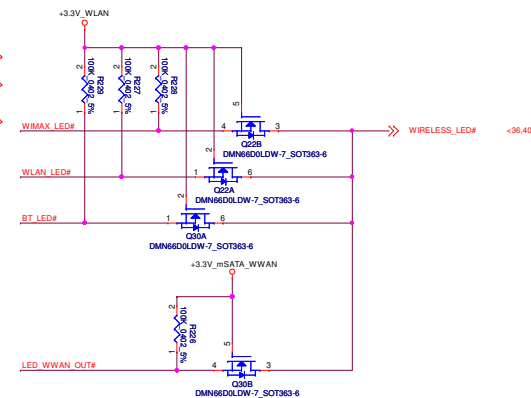


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+/-9%	1000	750	
+3.3Vaux	+/-9%	330	250	250 (Wake enable) 0 (Not wake enable)

SIM Card Push-Push



LED control circuit



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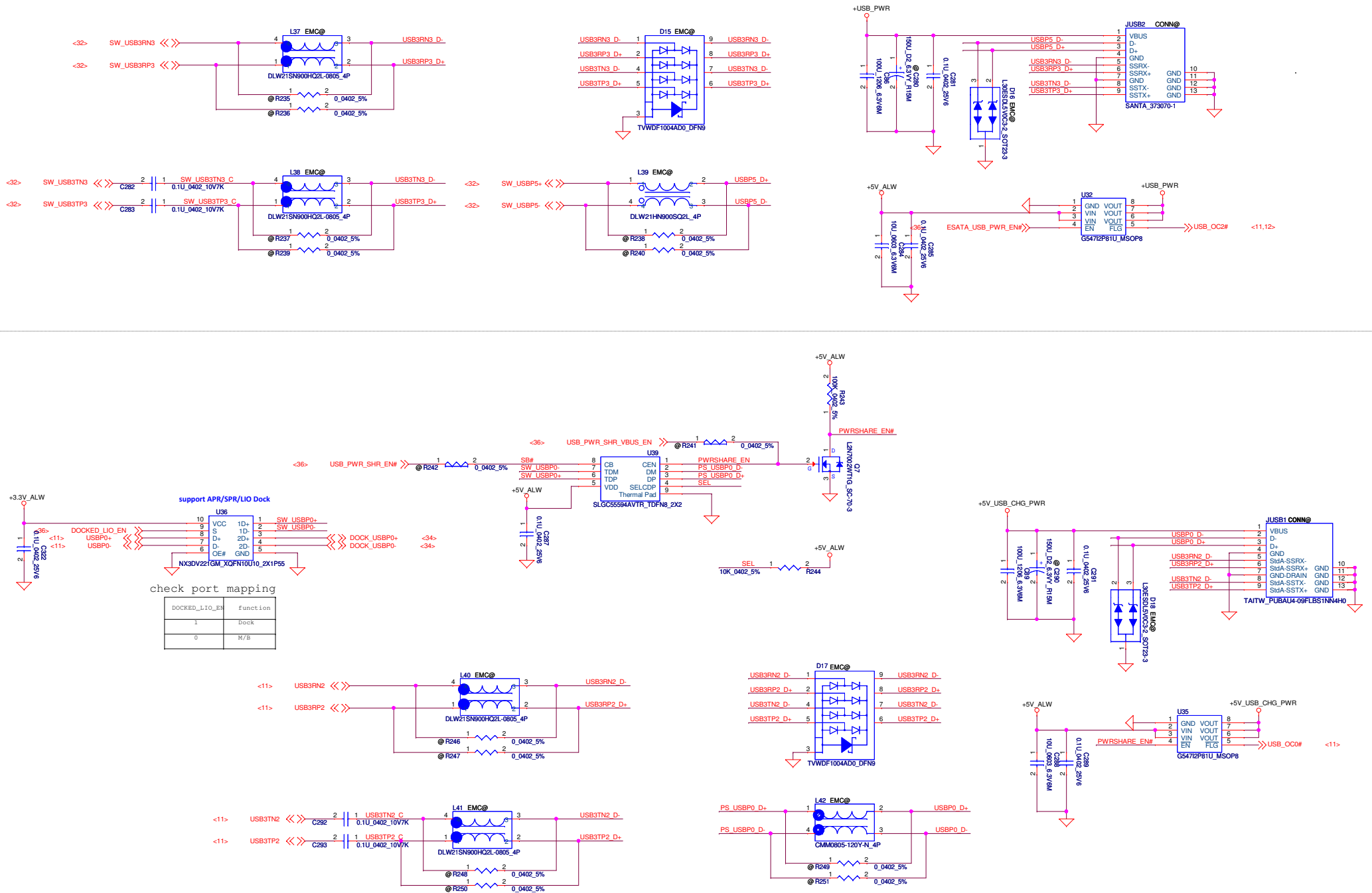
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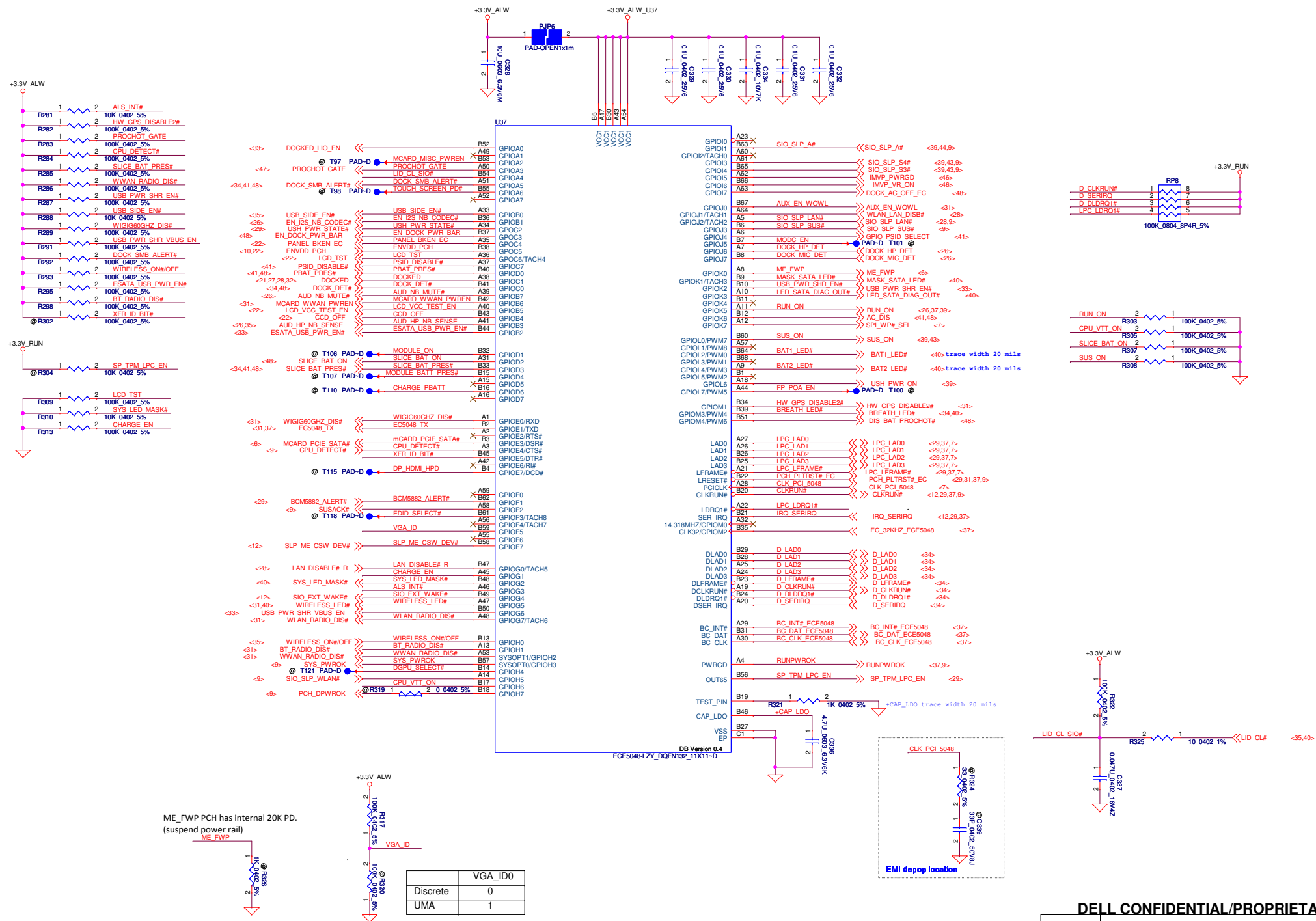
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File	USB3.0		
Size	Document Number	LA-9591P	Rev 0.4
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File: ECE5048

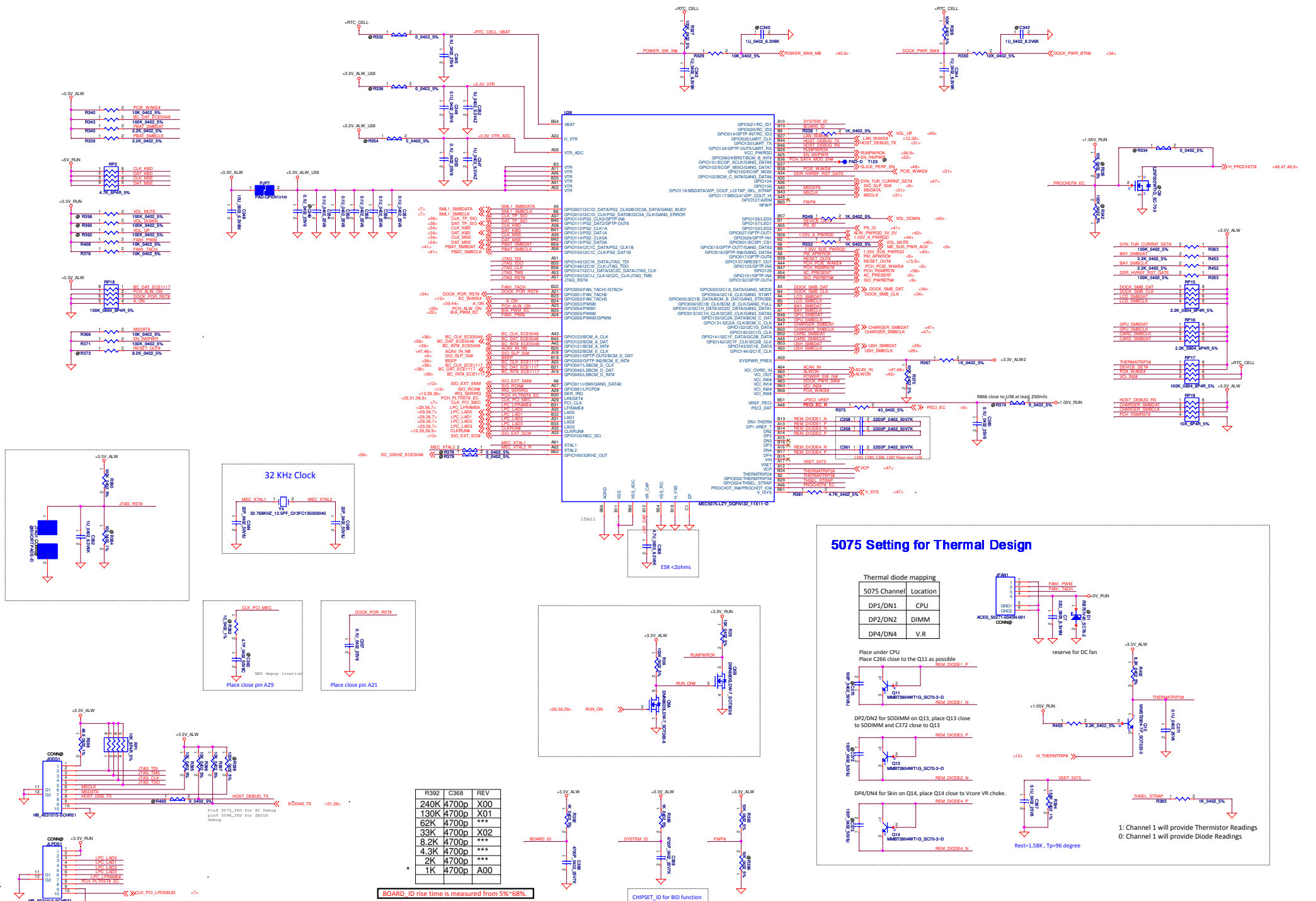
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MEC5075

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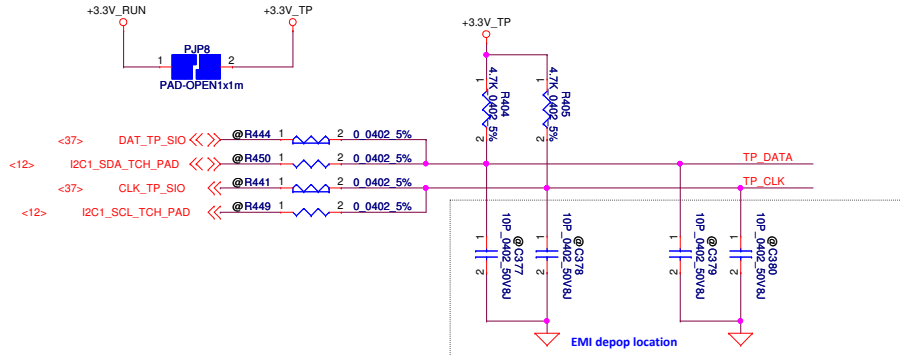
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Date: 2013/05/17/2013

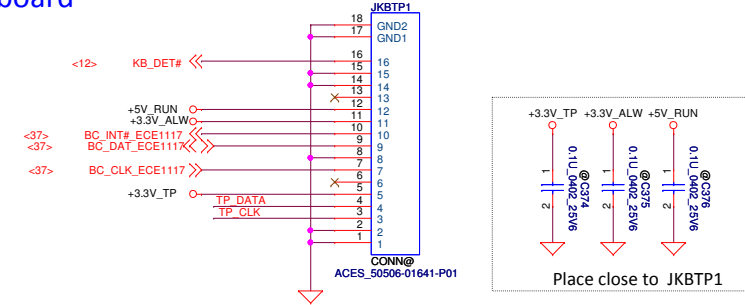
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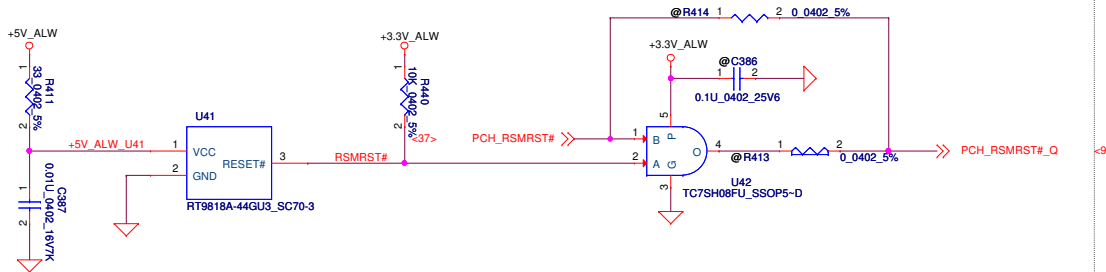
Touch Pad



Keyboard



RSMRST circuit



Part Number	Description
DA30000GZ00	FFC 0VN LF-9591P REV0 M/B-IO/B

Part Number	Description
DC02C004500	H-CONN SET 0VN MB-LCD-LED-CAM-TS

Part Number	Description
DC02C004T00	H-CONN SET 0VN MB-LCD-LED-CAM

Part Number	Description
DC02C004K00	H-CONN SET 0VN MB-HDD

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

Part Number	Description
NBX0001CW00	FFC 8P G P0.5 PAD0.3 50MM MB-MEDIA/B 0VN

Part Number	Description
NBX0001CZ00	FFC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

Part Number	Description
NBX0001CZ00	FFC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

Part Number	Description
NBX0001CY00	FFC 20P G P0.5 PAD=0.3 75MM MB-USH/B 0VN

Part Number	Description
NBX0001D100	FFC 6P G P0.5 PAD=0.3 75MM USH/B-FP 0VN

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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Keyboard

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The schematic diagram illustrates the +1.05V_MODPHY power supply circuit. It is powered by +5V_ALW and +3.3V_ALW2. The circuit includes a voltage divider (R445, R442) to sense the output voltage. The output is regulated by a PMOSFET (Q12AB) and a PMOSFET (Q12A). The output is filtered by capacitors C412 and C413. The output voltage is +1.05V_MODPHY. The circuit also includes a feedback network with resistors R447, R413, and R412.

+3.3V_ALW_PCH/+1.05V_RUN source

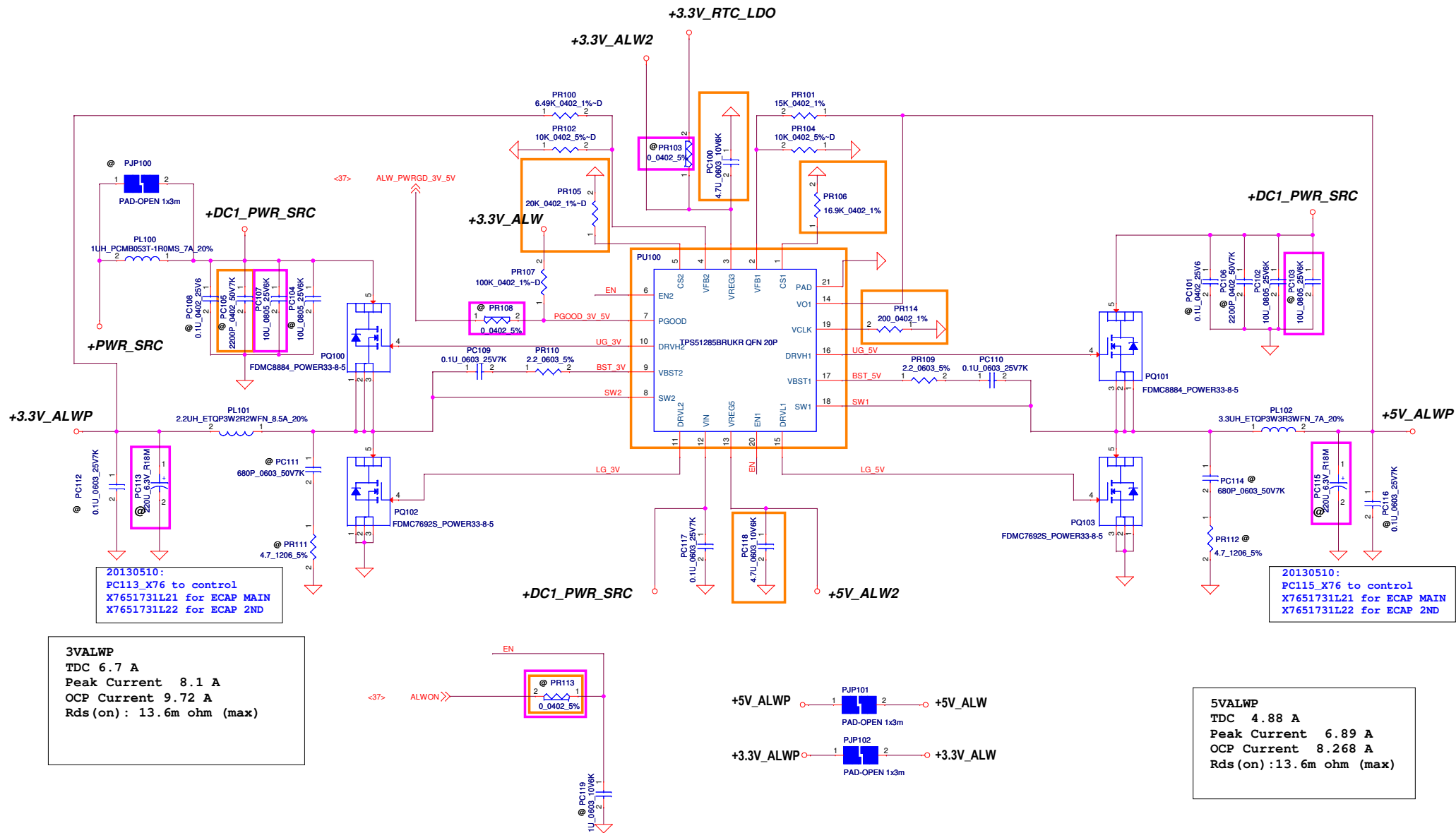
The schematic diagram illustrates the power source for the +3.3V_ALW_PCH and +1.05V_RUN rails. The circuit is centered around the TPS22966DPU_SONT4_2X3 PMOS driver (U43). The driver's VIN1 and VOUT1 pins are connected to the +3.3V_ALW_PCH rail, while VIN2 and VOUT2 are connected to the +1.05V_RUN rail. The driver is controlled by three input signals: PCH_ALW_ON (pin 1), RUN_ON (pin 2), and SIO_SLP_S3# (pin 3). Each input signal is connected to the driver through a 0.0402_5% resistor (R416, R418, and R417 respectively). The driver's output is connected to the +3.3V_ALW_PCH and +1.05V_RUN rails. The driver is also connected to a 0.1uF 10V7K capacitor (C389) and a 470pF 50V7K capacitor (C390) on the +3.3V_ALW_PCH rail, and a 470pF 50V7K capacitor (C381) on the +1.05V_RUN rail. Additionally, a 0.1uF 10V7K capacitor (C383) is connected to the +1.05V_RUN rail. The driver's GND pin is connected to the common ground.

+3.3V_SUS/+3.3V_M source

+3.3V_RUN/+5V_RUN source

The diagram illustrates the circuit for the +3.3V_RUN/+5V_RUN source. The TPS22966DPUR_SON14_2X3 IC (U46) is the central component. Its VIN1, VIN2, and VBIAS pins are connected to the +5V_ALW source. The VOUT1 and VOUT2 pins are connected to the +5V_RUN and +3.3V_RUN sources, respectively. The CT1 and CT2 pins are connected to ground. The GND pin is connected to ground. The GPAD pin is connected to ground. The output capacitors are C400 (0.1uF, 0402, 10V7K), C401 (470P, 0402, 50V7K), C402 (1000P, 0402, 50V7K), and C403 (0.1uF, 0402, 10V7K). The input capacitors are R425 and R426 (0.0402, 5%).

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	Power control		
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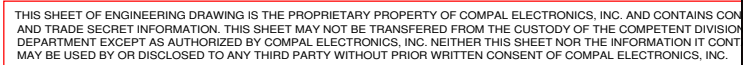


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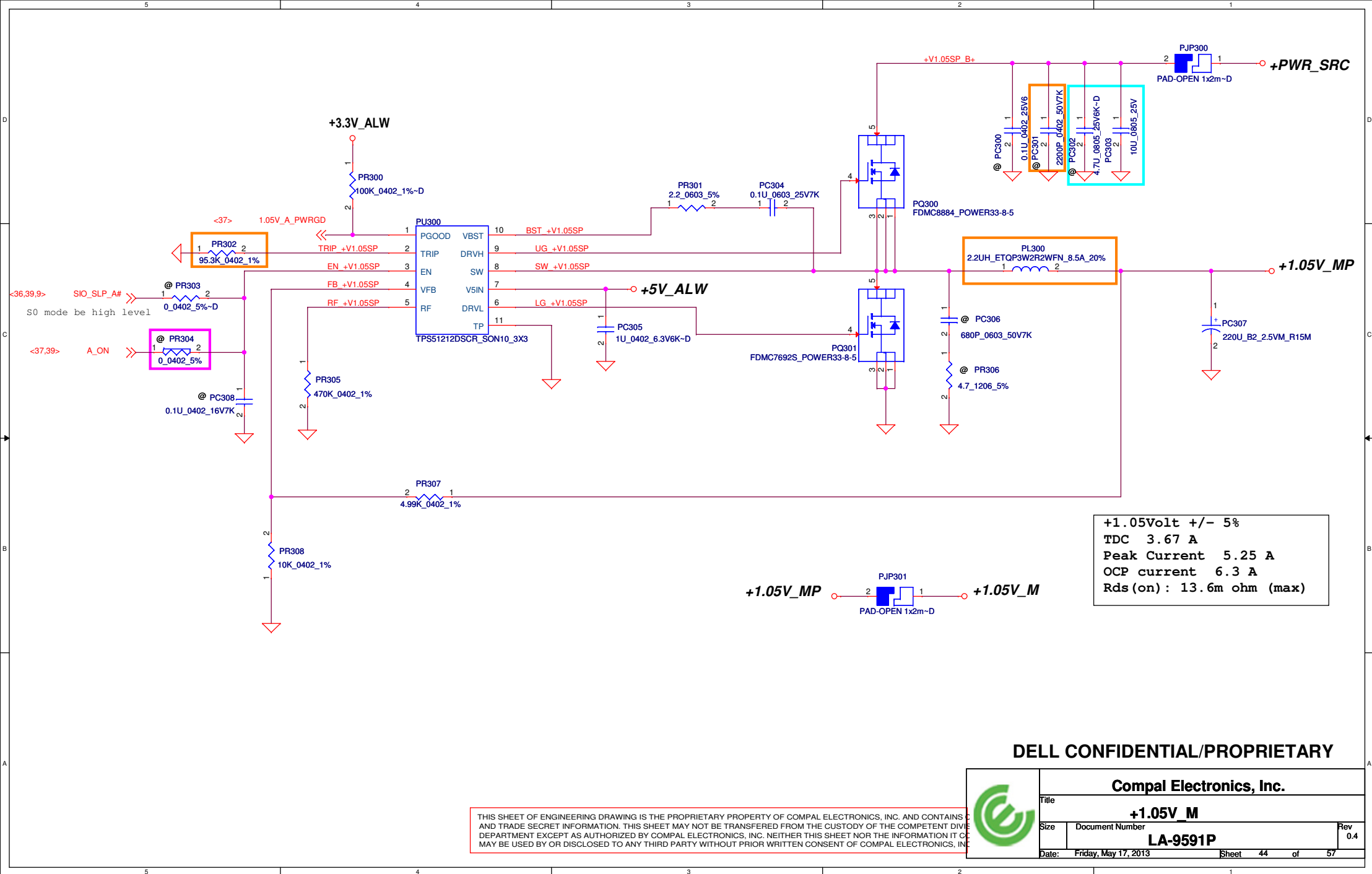


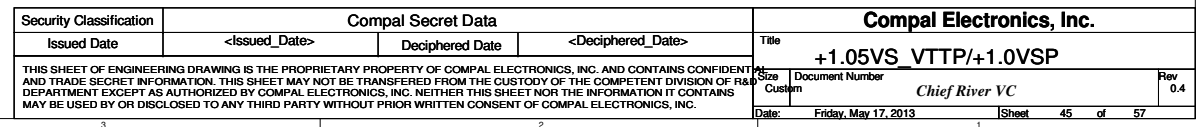
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Title		+5V_ALW/3.3V_ALW	
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```
0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A
```

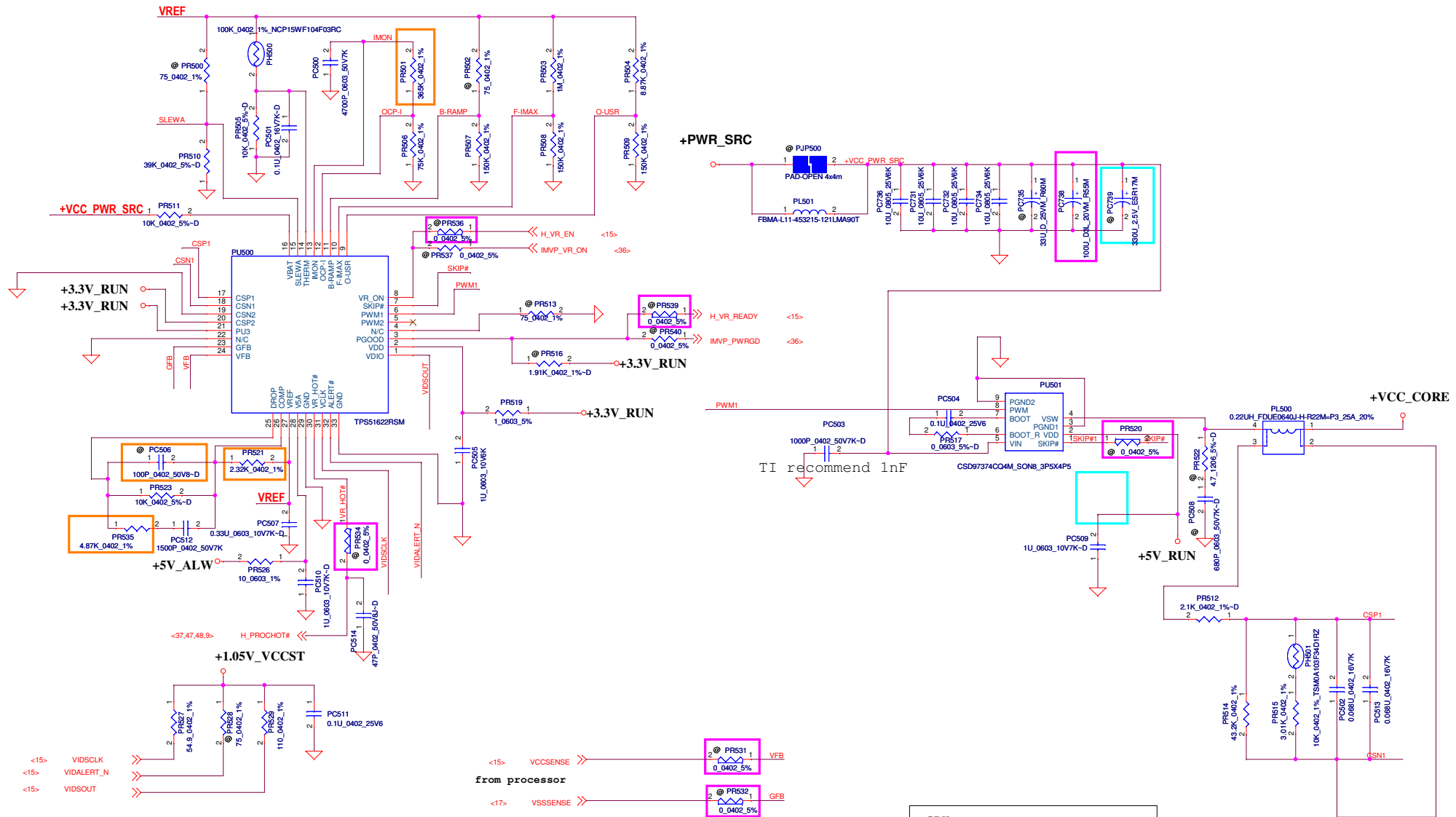


+1.35V MEN/+0.675V DDR VTT			
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20120911 TI-Alex Note: Although there is no pulse-overlap in 1-phase mode, during USR, the pulse comes in immediately. So, the problem with FR504 = DNP is that if there is a high ripple, and USR is faultily detected, you will get a double-pulse. So, we want to make sure USR is not active if it is not necessary. So, I moved it all the way to highest level so FR504 works to 8.87k



```
CPU
TDC 10 A
Peak Current 32 A
OCP Current 38.4 A
DCR: 0.82m +-5% ohm
PH500 B value: 4250k 1%
PH501 B value: 3435k 1%
```

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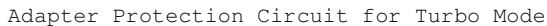
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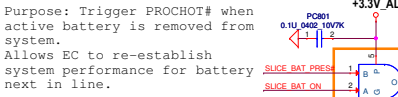
+VCC_CORE

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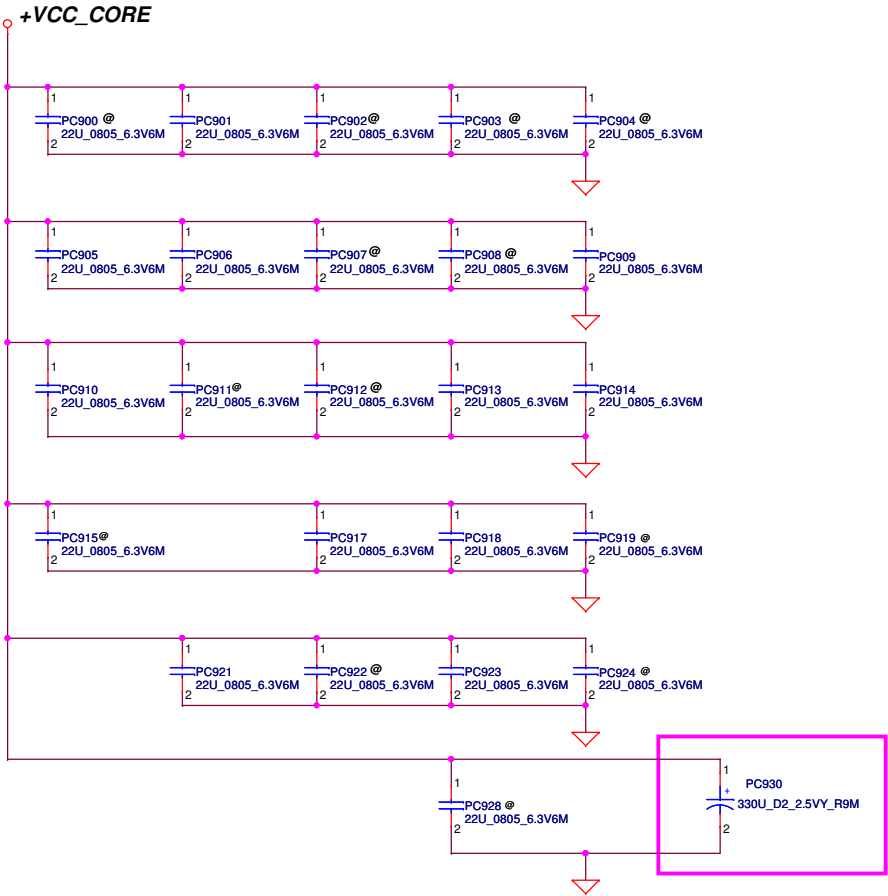


3V_ALW2 Purpose: Turn on the PQ817 for Slice battery discharge without AC exist

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Based on PDDG rev 0.7 Table 5-1.



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P45	1.5VSP	8/17	Compal	Base power budget request, add 1.5V powre rail	Add PU400	
2	P42	+5V/+3.3V	8/17	Compal	reserver PR114 for TPS51282 application	ADD @PR114	
3	P47	Charger	8/17	Compal	EC can't detect charger IC cause can't charger	modify SMBus net for correct connect	
4	P46	Vcore	8/17	Compal	schematic control error cause can't set OCP	add Vref net for correct connect	
5	P48	Selector	8/17	Compal	in order to meet latest multi-battery request	change control signal for meet E5 request	
6	P43	1.35V/0.675V	8/17	Compal	chagne OCP setting	change PR201 from 20k to 24.9k.	
7	P42	+5V/+3.3V	10/22	Compal	Reserve 0ohm for 3v5v enable debug	Change PR113 from SD03420018L (S RES 1/16W 2K +-1% 0402) to SD028000080 (S RES 1/16W 0 +-5% 0402)	X01
8	P44	+1.05V_MP	10/22	Compal	+1.05V_MP EA for ripple portion can't meet spec. 31.5mv, after change from 1u to 2.2u test is pass	Change PL300 from SH00000PJ00 (S COIL 1UH +-20% PCMB063T-1R0MS 12A) to SH00000MR00 (S COIL 2.2UH +-20% ETQP3W2R2WFN 8.5A)	X01
9	P42	+5V/+3.3V	10/22	Compal	Original 3v5v IC -TPS51225 can't support 2cell battery follow TI suggestion, When TPS51285A/B is used, please update the below four components. 1)VREG5 cap to 4.7uF 2)VREG3 cap to 4.7uF 3)CS1 resistor to 1/5 of the Tps51275's value 4)CS2 resistor to 1/5 of the Tps51275's value 5)VCLK connection (when not be used): add 200-ohm to GND	Change PU100 from SA00005LS00 (S IC TPS51225CRUKR QFN 20P PWM) to SA000064T00 (S IC TPS51285BRUKR QFN 20P PWM) 1)2)Change PC118(VREG5 Cap) and PC100(VREG3 Cap) from SE080105K80 (S CER CAP 1U 10V K X5R 0603) to SE00000MA00 (S CER CAP 4.7U 10V K X5R 0603) 3) Change PR106(for CS1) from SD03484528L (S RES 1/16W 84.5K +-1% 0402) to SD034169280 (S RES 1/16W 16.9K +-1% 0402) 4) Change PR105(for CS2) from SD03410038L (S RES 1/16W 100K +-1% 0402) to SD034200280 (S RES 1/16W 20K +-1% 0402) 5) Add PR114 SD034200080 (S RES 1/16W 200 +-1% 0402)	X01
10	P47 P48	Charger Selector	10/22	Compal	To avoid HW and Power SMT materials can't entirely replace	Change PU3,PU801,PU804,PU805,PU806,PU807 from SA74108040L (S IC 74AHC1G08GW SOT353 AND) to SA00708012L (S IC TC7SH08FU SSOP 5P AND)	X01
11	P47	Charger	10/22	Compal	follow E5- Salado 14"15" schematic	1) @PQ819, @PQ824 2) EMI request for add PL700 SH00000IW00 (S COIL 1UH +-20% PCMB042T-1R0MS 4.5A)	X01
12	P46	Vcore	11/02	Compal	follow TI suggestion modify setting value to meet Intel VR12.6(ULV) validation EA 1) Imon 2) Loadline 3) transient	1) Change PR501 from SD034422380 (S RES 1/16W 422K +-1% 0402) to SD034365380 (S RES 1/16W 365K +-1% 0402) 2) Change PR521 from SD000009M80 (S RES 1/16W 2.61K +-1% 0402) to SD00000WS8L (S RES 1/16W 2.32K +-1% 0402) 3) @PC506 100p_0402 and change PR535 from SD02810028L (S RES 1/16W 10K +-5% 0402) to SD034487100 (S RES 1/16W 4.87K +-1% 0402 (LF))	X01

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13	P47	Charger	11/05	Compal	1) TI suggestion BQ24715 cell pin pull high 3.3V change to V_regn(6v) for sequence issue 2) Reserve 0 ohm for debug	1) Change PR711 from SD02800008L (S RES 1/16W 0 +-5% 0402) to SD034100280 (S RES 1/16W 10K +-1% 0402) ,add PR750 SD028000080(S RES 1/16W 0 +-5% 0402) 2) Add @PR751	X01
14	P42	+5V/+3.3V	11/05	Compal	follow E5- Salado 14"15" schematic	1) @PR863, @PR870, @PR869, @PR824, @PR875, @PQ823 2) Add @PR848, @PR851 and add PR834, PR852, PR853, all is SD028000080(S RES 1/16W 0 +-5% 0402) 3) Add PR874 SD028100480(S RES 1/16W 1M +-5% 0402) 4) Add PD819 SCS0340L01L(S SCH DIO SDMK0340L-7-F SOD-323)	X01
15	P47	Charger	11/05	Compal	Improve charger efficiency	Change PR715 from SD028200A80 (S RES 1/16W 20 +-5% 0402) to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	X01
16	P47	Charger	11/05	Compal	follow E5- Salado 14"15" schematic	Delete @PR731, @PR733, @PU702	X01
17	P44	+1.05VTTP	11/05	Compal -QAD team -Huang.Hanks (PCP)	Support QAD WCEPTA analysis, to modify 1.05 OCP Rtrip resistance to 95K, Cpk value will pass specification.	Change PR302 from SD00000H880 (S RES 1/16W 54.9K +-1% 0402) to SD034953280 (S RES 1/16W 95.3K +-1% 0402)	X01
18	P48	+5V/+3.3V 1.35V/0.675V +1.05V_MP	11/05	Compal - EMC team Wen. Andy	EMC team suggestion	@PC105, @PC203, @PC301	X01
19	P48	Selector	11/15	Compal	follow E5- Salado 14"15" schematic for undock shutdown issue	Add PQ827 SB00000U000 (S TR DMN65D8LW-7 1N SOT323-3), @PR856 SD028000080 (S RES 1/16W 0 +-5% 0402), PQ816 SB534020000 (S TR AO3402 1N SOT-23), PQ828 SB00000U000 (S TR DMN65D8LW-7 1N SOT323-3), PR861 SD028000080 (S RES 1/16W 0 +-5% 0402) PR802, PR827, PR840 change from SD028240380 (S RES 1/16W 240K +-5% 0402) to SD028470280 (S RES 1/16W 47K +-5% 0402), PR804, PR826, PR839 change from SD028470280 (S RES 1/16W 47K +-5% 0402), to SD028240380 (S RES 1/16W 240K +-5% 0402)	X01
20	P47 P48	Charger Selector	12/12	Compal		Change PR713 from SD034294380 (S RES 1/16W 294K +-1% 0402) to SD034261380 (S RES 1/16W 261K +-1% 0402) @PR844	X01
21	P41	+DCIN	2013 /01/11	Compal- ESD team	ESD team's PD1 vendor(NXP) proposal PD1 pin 5 connected to the VCC (5V or 3.3V).	PD1 pin5 connect to +3.3V_ALW	X01_2

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
28	P48	Selector	2013/ 02/21	Compal	follow E5- Salado 14"15" schematic 1) For Input current sense stablilze 2) To provent charger into sleep mode dual AC transient. 3) Fine tune ACOK response time. 4) Adapter protect rating setting 5) Fine tune H_PROCHOT# response time. 6) Improve ACAV_IN_NB ref voltage accuracy. 7) Improve current sense accuracy.	1). Change PC703 from 0.1U to 1U P/N: SE000006900 (S CER CAP 1UF 25V K X5R 0603) 2). Change PC706 from 1U to 10U P/N: SE00000QK00 (S CER CAP 10U 25V K X5R 0805 H1.25) 3). Change PC708 from 0.01U to 0.1U P/N: SE00000G880 (S CER CAP 0.1U 25V K X5R 0402) 4). Change PR734 from 100K ohm to 210K ohm P/N: SD034210380 (S RES 1/16W 210K +-1% 0402) Change PR735 from 46.4K ohm to 69.8K ohm P/N: SD034698280 (S RES 1/16W 69.8K +-1% 0402) 5). Add @PC740 6). Change PR738.pin1 from BQ24715_REGN connect to +3.3V_ALW2. Change PR738 from 118K ohm to 48.7K ohm P/N: SD034487280 (S RES 1/16W 48.7K +-1% 0402) Change PR744 from 12K ohm to 10K ohm P/N: SD034100280 (S RES 1/16W 10K +-1% 7). Change PR748 from 6.8 ohm to 210K ohm P/N: SD034442A80 (S RES 1/16W 44.2 +-1% 0402) Change PR749 from 10 ohm to 69.8K ohm P/N: SD00000W200 (S RES 1/16W 59 +-1% 0402)	X02
29	P48	Selector	2013/ 02/27	Compal	Modify resistor value to meet voltage tolarence	1). Change PR802,PR827,PR840 from 47K ohm to 100K P/N: SD028100380 (S RES 1/16W 100K +-5% 0402) 2). Change PR804,PR826,PR839 from 240K to 100K P/N: SD028100380 (S RES 1/16W 100K +-5% 0402)	X02
30	P47	Charger	2013/ 03/18	Compal	follow E5- Salado 14"15" schematic to add charger input MLCC to 88u	1). Add PC741, PC742 P/N: SE00000XH80 (S CER CAP 22U 25V M X5R 0805 H1.25)	X02_1
31	P42 P43 P44	+5V/+3.3V 1.35V/0.675V +1.05V_MP	2013/ 03/20	Compal	support DFX team change choke layout pad to avoid soldering issue	1). Change PL101, PL102, PL200, PL300 PCB FootPrint change from CYNTE_PCMC063T-2R2MN_2P to CYNTE_PCMB064T-3R3MS_2P	X02_1
32	P47 P49 P46	Charger PROCESSOR DECOUPLING Vcore	2013/ 03/21	Compal	Support acoustic team to reduce noise	1). Add PC930 P/N: SGA00002680 (S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9) 2). Del PC916, PC920, PC925, PC926, PC927, PC929 P/N: SE000001120 (S CER CAP 22U 6.3V M X5R 0805 H0.85) 3). Change PC738 from 33U(SGA00005M00) to 100U P/N: SGA00008R00 (S POLY C 100U 20V M D ESR55M (D3L_H=2.8mm) 4). Depop PC928, PC924, PC919, PC915, PC911 and Add PC901 P/N: SE000001120 (S CER CAP 22U 6.3V M X5R 0805 H0.85)	X02_1
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1	40 36	HW	10/23/2012	DELL	DELL drop Media LED function	Remove backlight LED function and change connector to 6pin	X01
2	10	HW	10/23/2012	COMPAL	Remove EMI solution at Speaker side	Remove R132, R133, R134 and R135	X01
3	22	HW	10/23/2012	DELL	DELL drop ALS function	Remove ALS interface from EC and CPU side than move touch screen signal to eDP side	X01
4	22	HW	10/23/2012	COMPAL	change LCDVDD power control circuit	change U9 from TPS22966 to APL3512 solution	X01
5	22	HW	10/23/2012	COMPAL	change Webcam power enable from PCH	pop R106 and de-pop R102	X01
6	10	HW	10/23/2012	COMPAL	remove eDP backlight control pull up resistor	Remove RC150	X01
7	21	HW	10/23/2012	COMPAL	Vendor update schematic for power saving	change +1.05V_RUN_VMM power enable signal from LP_EN to DOCKED and add +3.3V_RUN_VMM for DP2320 series 3.3V power rail remove L3 and move U6.E5 to +1.05V_VMM_VDD power rail change U6.J4 to +3.3V_RUN_VDDA R85 change to 3.74K_1% remove LP_EN, R232 and U6A.A5 to NC remove R55 and pop-option R207 when use VMM2310	X01
8	21	HW	10/23/2012	COMPAL	change VMM2320 config	remove DP to VGA PTN3392 circuit and add 0ohm pop option for 2320 config	X01
9	18 19	HW	10/23/2012	COMPAL	Remove DIMM VREF power rail from power side	Remove RD2, RD4, RD8 and RD9	X01
10	26	HW	10/23/2012	COMPAL	change miniDP OCP solution	remove D10 R160 F2 and add U50 de-pop C383	X01
11	26	HW	10/23/2012	COMPAL	refer salado 14" to change PCBEEP circuit	remove C132,C146,R146,R138,C133 and C143 than add C145,C146,R147,R151 and de-pop R194 R153	X01
12	26	HW	10/23/2012	COMPAL	If doesn't has external power, Sleeve will be floating mode and no reference GND.	Add AUD_NB_MUTE# to control Sleeve pin.	X01
13	37,36,12 20	HW	10/23/2012	COMPAL	GPIO map update to 2.7 version	Move EC_WAKE# from ECE5048[L]5 to MEC5075 GPIO52. Change name: 1.5V_SUS_PWRGD to 1.35V_SUS_PWRGD for DDR3L. Add NFC_DET# ECE5048 GPIOL[5] to NFC moudle and add pull up 10K resistor	X01
14	37	HW	11/8/2012	COMPAL	Change board ID to X01	change R392 form 240K to 130Kohm	X01
15	10 12 21 36 37	HW	11/8/2012	COMPAL	change to network resistor	remove RC167,RC202,RC293 and RC290 then add RP4 remove RC295,RC189,RC191 and RC51 then add RP5 remove RC177,RC15,RC62 and RC43 then add RP6 remove RC201,RC203,RC204 and RC208 then add RP7 remove R299,RC300,R301 and R296 then add RP8 remove R53,R54,R70 and R72 then add RP9 remove RC216,RC178,RC80 and RC21 then add RP11 remove RC77,RC85,RC71 and RC215 then add RP12 remove RC207,RC214,RC205 and RC164 then add RP13 remove RC229,RC188,RC34 and RC196 then add RP14 remove R359,R361,R451 and R387 then add RP15 remove R445,R456,R457 and R454 then add RP16 remove R346,R347,R364 and R365 then add RP17 remove R344,R368,R369 and R372 then add RP18 remove R401,R348,R350 and R377 then add RP19	X01

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16	22	HW	11/8/2012	COMPAL	Add Mic power and remove DBC function	Add 3.3V_RUN for Mic power and remove DBC function at JeDP.2	X01
17	39	HW	11/8/2012	COMPAL	+1.05V_MODPHY can't meet INTEL timing spec	change +1.05V_MODPHY to MOS solution	X01
18	19	HW	11/8/2012	COMPAL	refer PDG1.0 to change SODIMM control circuit resistor	change RC68, RC126 and RC173 from 2.2 to 2ohm 1% change RC67,RC69,RC130,RC132,RC217 and RC221 from 1.82K to 1.8Kohm 1%	X01
19	27, 32, 26, 20, 40	ME	11/8/2012	COMPAL	ME change connector	change JmDP1, JSIM1, JSPK1, JNFC1, JMEDIA, SW1, JSD1	X01
20	2, 3, 6, 34	HW	11/13/2012	COMPAL	update SATA topology fro Mainstream CPU	exchange SATA1&SATA2 topology	X01
21	12	HW	11/13/2012	COMPAL	refer Goliad 12" add LAN_WAKE# T-topology	add RC177 to link LAN_WAKE# and EC_WAKE#	X01
22	15	HW	11/13/2012	COMPAL	remove RC252 for cost saving	change RC252 to PJP11(1mm jumper-short)	X01
23	34	ME	11/14/2012	COMPAL	ME change Docking connector	change JDock1	X01
24	16	HW	11/14/2012	INTEL	MOW_WW46 request change for VCCUSB3PLL and VCCSATA3PLL	change CC42 and CC49 from 1u_0402 to 22u_0603 change CC76 and CC77 from 100u_1206 to 22u_0603	X01
25	20, 28, 30, 31	HW	11/14/2012	COMPAL	change AND gate to same source	Change U20, U26, U29 and U30 from SA74108040L to SA00708012L	X01
26	33	HW	11/14/2012	COMPAL	add USB power cap 150u co-layout with 100u	add C86,C89(1206) co-layout with C280,C290(B2)	X01
27	24	HW	11/14/2012	COMPAL	change AUX/DDC power rail same as VMM2320	Change U11,U13 power rail from +3.3V_RUN to +3.3V_RUN_VMM	X01
28	38, 12	HW	11/14/2012	COMPAL	remove +3.3V_TP power load switch solution	remove U40, R458,C424 and C423	X01
29	31	HW	11/14/2012	COMPAL	remove TPS22965 solution	remove U51(TPS22965) and U34(TPS22965) than add U3(TPS22966)	X01
30	22	HW	11/15/2012	COMPAL	change diode to daul-diode fro cost saving	remove D4,D5,D6,D7 and add D10,D21	X01
31	9	HW	11/16/2012	COMPAL	change APS pin 11 net_name for DELL APS debug	Change JAPS1.11 net name from SIO_PWRBTN# to POWER_SW#_MB	X01
32	31, 12	HW	11/16/2012	COMPAL	add mSATA_DSLP for mSATA HDD	add mSATA_DEVSLP from UC1.P2(DEVSLP1/GPIO38) to mSATA_HDD(JMINI2.44) and pull up 10K(R160 depop) to +3.3V_mSATA_WWAN. de pop HDD_DEVSLP pull up resistor R155	X01
33	37	HW	11/16/2012	COMPAL	change thermal diode for cost saving	change D11,D13 and D14 form SB000008P0L to SB33904510L	X01
34	12, 28	HW	11/16/2012	COMPAL	support TLS confidentiality	change net name from HOST_ALERT1_R_N to PCH_GPIO15, and pop RC190 remove R188	X01
35	38, 26, 30, 22	HW	11/16/2012	COMPAL	change Bead for cost reduce	change L44 and L45 from SM01000558L to SM01000C500 change L35 and L36 from SM01000AM0L to SM01000C500 change LE1 from SM01000DH0L to SM01000BV00 change L21 from SM01001788L to SM010005N00	X01

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36	29	HW	11/19/2012	COMPAL	exchange JUSH1, JMEDIA pin define for ME update	exchange JUSH1 and JMEDIA pin define	X01
37	25	HW	11/19/2012	COMPAL	remove HDD_DEVSLP resisrtor	remove R189	X01
38	37	HW	11/19/2012	COMPAL	change thermal OTP to 98 degree	change R394 from 1.24K to 1.82K_1%	X01
39	28	HW	11/20/2012	COMPAL	LOM LED issue	reverse Q32,Q33 of C & D gate	X01
40	22 40 38 26	HW	11/22/2012	COMPAL	Remove ESD reserve location	Per ESD experiment, D3,D27,D22,DE1,DE2 can be remove	X01
41	15	HW	11/23/2012	COMPAL	Per Intel CRB updated	Change VCCST_PWRGD pull high value from 10K ohm to 1K ohm.	X01
42	26	HW	11/23/2012	COMPAL	Universal Jack no longer supported on X5	Remove D9,D11,R209,R210,C195,C196,R198,R199	X01
43	12	HW	11/27/2012	COMPAL	Change GPIO connection	change NFC_DET# connection from EC GPIO_L[5]/PWM2 to LPT_LP GPIO59	X01
44	6	HW	11/28/2012	COMPAL	To support mainstream and Premium CPU, change to SATA port assignment.	Change docking SATA port form SATA port 1 to SATA port 0 and spindle HDD from port 0 to port 1	X01
45	12	HW	11/28/2012	COMPAL	To support the SATA DevSLP function for new SATA port assignment.	Change DEVSLP0/GPIO33 to mSATA_DEVSLP and DEVSLP1 to HDD_DEVSLP	X01
46	12	HW	11/28/2012	COMPAL	USB port 0 EA result	Change L42 from DLW21SN900SQ2L to OCE2012120YZF	X01
47	31	HW	11/28/2012	COMPAL	Change WWAN power control.	Change power control signal from 3.3V_WWAN_EN & 3.3V_msATA_EN to MCARD_WWAN_PWREN	X01
48	31	HW	11/28/2012	COMPAL	Change WLAN power control.	Change power control signal from 3.3_1.5V_WLAN_EN to AUX_EN_WOWL	X01
49	38	HW	11/28/2012	COMPAL	Per EMI test result	Remove L44,L45	X01
50	34	HW	11/28/2012	COMPAL	Per EMI test result	Change R259,R252,R253,R255,R257,R263,R265,R266 R260,R261,R254,R256,R262,R264,R258,R267 from 0 ohm to 33 ohm.	X01
51	9	HW	1/9/2013	COMPAL	add RSMRST pull down resistor	add RC136	X01
52	38	HW	1/9/2013	COMPAL	add repeater at USB3 RX IO connector side	add U51 circuit	X01
53	22	HW	1/9/2013	COMPAL	change LCDVDD power chip soft start cap	change C430 from 0.1u to 0.01u	X01
54	36	HW	1/9/2013	COMPAL	change dock SMBus alert pull up resistor	change R292 from 10K to 100Kohm	X01
55	40	HW	1/17/2013	COMPAL	change LED series resistor form LED measure	change R435 from 1.8K to 390ohm, change R430 from 2.2K to 220ohm, change R434 from 220 to 150ohm, change R427 from 1K to 390ohm.	X01

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56	1 9	HW	1/23/2013	COMPAL	add XDP@ for XDP component	change XDP circuit to XDP@	X02
57	37	HW	1/23/2013	COMPAL	change board ID to ST config	change R392 from 130K to 33Kohm	X02
58	37	HW	1/30/2013	COMPAL	change HW thermal shortdwon temperature	change R394 from 1.82K to 1.58Kohm	X02
59	22	HW	2/1/2013	COMPAL	change eDP connector pin define for factory burn out issue	1.add pull down 1Kohm at JEDP1.29 2.Swap JEDP1.1 and JEDP1.2	X02
60	26	HW	2/1/2013	COMPAL	update speaker EMI bead for audio precssion fail issue	change L22~L25 from SM01000L300 to SM010019400	X02
61	26	HW	2/1/2013	COMPAL	update XDP circuit for INTEL ITE can't boot	remove RC121 and pop RC102	X02
62	36	HW	2/18/2013	COMPAL	power update AC_DIS# circuit to high active	change AC_DIS# net name to AC_DIS	X02
63	11 35	HW	2/21/2013	COMPAL	Fixed 2 USB IO Port use the same OC# signal issue	1.change IO/B USB OC# from USB_OC0# to USB_OC1# 2.change USB_OC1#/3# to USB_OC1#, USB_OC3# and add RC166 for OC3# pull up resistor	X02
64	7	HW	2/21/2013	COMPAL	add jumper for clock buffer co layout	add PJP12, PJP13 and PJP14 between UC5	X02
65	7	HW	2/21/2013	COMPAL	change TAA connector from ME request	change JTA11 from ACES_50185 02041 001 to PANAS_AXX820145WG	X02
66	16	HW	2/22/2013	COMPAL	add ESD solution	1.Pop CC71 and CC72 2.Add two 22u 0603 between +VCC_CORE and +1.05V_RUN power plan 3.Add 22u 0603 between +1.05V_RUN and +3.3V_RUN power plan	X02
67	33	HW	2/22/2013	COMPAL	change USB charge solution for SAMSUNG phone	change U39 from SA00004VH00 to SA00006L600	X02
68	7	HW	2/25/2013	COMPAL	add RF noise solution at clock buffer	1. add CC86~CC89 between clock signal 2. add RC62 for UC5 power rail 3. change RC100 from 0ohm short to 10ohm 4. change UC5 from IDT_5V60034DCG8 to CYPRESS_CY2304SXI-1T	X02
69	23	HW	2/25/2013	COMPAL	refer INTEL MOW to update HDMI cost reduce level shifter main link	cahnge R462~R469 resistor from 680(SD034680080) to 470ohm(SD034470080)	X02
70	11 12	HW	2/25/2013	COMPAL	For AOAC function, can't wake up from S3 through SIO_EXT_SMI#	change net name from USB_OC3# to SIO_EXT_SMI#, and change SIO_EXT_SMI# to PCH_GPIO45	X02
71	9	HW	2/26/2013	COMPAL	add EMI solution at H_PROCHOT#	add CC149_22P_0402(SE071220J80) depop for EMI request	X02
72	26	HW	2/26/2013	COMPAL	for Fixed BIOS flash HOTSOS issue	change R154 from PCH_AUDIO_EN to RUN_ON	X02
73	7	HW	2/28/2013	COMPAL	remove clock Buffer solution	1.remove item 68 location and CC25 CC57 CC80 CC22 UC5 RC100 and CC23 2.change RC65 to 0ohm_short	X02
74	7 29	HW	2/28/2013	COMPAL	refer GPIO3.0 to add PCH_TPM_LPC_EN	add RC56 for pull up enable signal and add R198 for pop option	X02
75	30	HW	3/12/2013	COMPAL	For O2 enters into test mode unexpectedly with SD card inserted incompletely issue.	1. SD/MMCCD# add C256(0.1uF) & R493(1M) pull-down to GND 2. C222 change to 1uF(SE000000K80) from 0.1u(SE000000G880)	X02

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76	7	HW	3/13/2013	COMPAL	Base on INTEL EDS SPEC Update Rev 1.5.1	1. LANCLK_REQ# change to UC1.AD1 from UC1.Y5 2. MINI1CLK_REQ# change to UC1.T2 from UC1.U2 3. MINI2CLK_REQ# change to UC1.N1 from UC1.T2 4. MMICLK_REQ# change to UC1.U5 from UC1.AD1 5. PCH_TPM_LPC_EN change to UC1.Y5 from UC1.U5	X02
77	7	HW	3/14/2013	COMPAL	For PCIE CLK & PCIE CLK REQ signal mapping	1. CLK_PCIE_LAN change CLKOUT_PCIE port2 2. CLK_PCIE_MINI2 change CLKOUT_PCIE port3 3. CLK_PCIE_MMI change CLKOUT_PCIE port4 4. CLK_PCIE_MINI1 change CLKOUT_PCIE port5	X02
78	21	HW	3/15/2013	COMPAL	remove VMM2310 co-layout schematic	remove U8, R93, R98, R105 circuit	X02
79	15	HW	3/15/2013	COMPAL	add ESD solution	add CC22 and CC57	X02
80	7	HW	3/18/2013	COMPAL	For INTEL request	PCIECLK_REQ0# add RC57(10k) pull-high to+3.3V_RUN	X02
81	21	HW	3/20/2013	COMPAL	For Synaptics vender request	1. Delete R78/R80/R82 2. add C132	X02
82	9 12	HW	3/21/2013	COMPAL	add ESD solution	add CC90 and CC91	X02
83	35	HW	4/02/2013	COMPAL	For USB3.0 1M cable	Pop R478, R479 and change R476 to 3.01K ohm	X02
84	37	HW	4/25/2013	COMPAL	change board ID to A00 version	change R392 from 33K to 1K ohm	A00
85	33	HW	4/25/2013	COMPAL	for JUSB2 can't wake from S3 issue	change U33 power rail from +3.3V_RUN to +3.3V_SUS	A00
86	9	HW	4/25/2013	COMPAL	for XDP signal should be contact to PCH	change RC97 and RC135 to 0ohm short	A00
87	28	HW	4/25/2013	COMPAL	for support Vpro reset pin	depop U20 and add R145	A00
88	12	HW	4/25/2013	COMPAL	reserve for support non vpro pop option pin	reserve RC292 pull down	A00
89	40	HW	4/25/2013	COMPAL	current LED resistor for LED EA measure	R434 change from 150 to 330ohm, R430 change from 220 to 330ohm, R438 change to 2.2K to 150ohm, R436 change from 2.2K to 220ohm and R429 change from 620 to 220ohm	A00
90	10	HW	5/14/2013	COMPAL	HDD Free Fall Sensor	add R494 & R495	A00
91	15 16	HW	5/16/2013	COMPAL	add ESD solution	Pop CC57, depop CC71 , CC72	A00
91	12	HW	5/16/2013	COMPAL	reserve for support non vpro pop option pin	Follow Goliad12, Pop RC290 & change RC292 from 10K to 100ohm.	A00
							X02

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