

Compal Confidential

QCL51 Schematics Document

AMD Comal Platform

AMD Trinity APU / Hudson FCH / ATI Chelsea Pro M2

Muxless/UMA / PX 4.0 / PX 5.0

2011-10-26

LA-8712P REV: 0.1

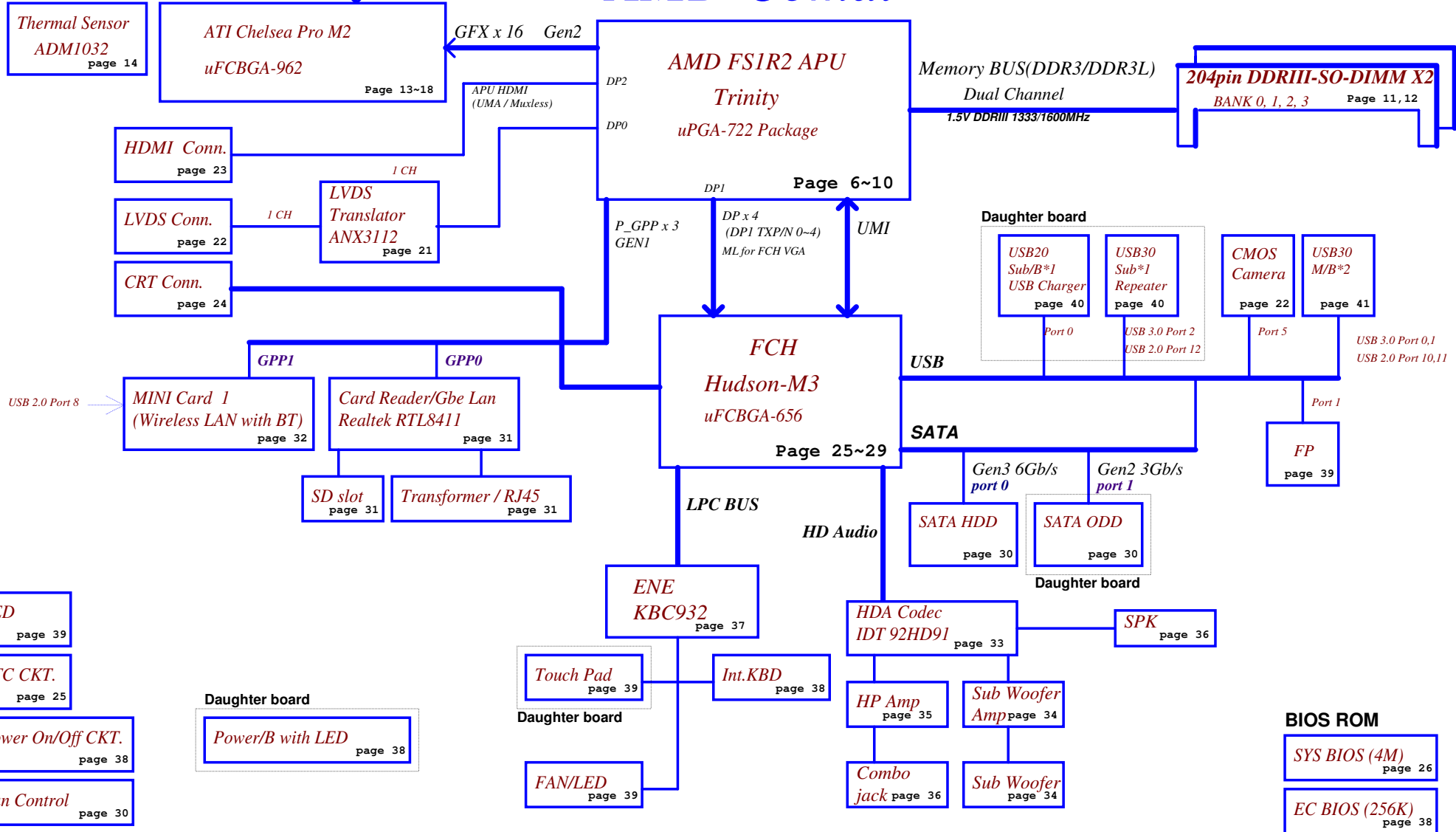
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				QCL51 LA-8712P	0.1
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Model Name : QCL51 AMD
Board Name : LA-8712P

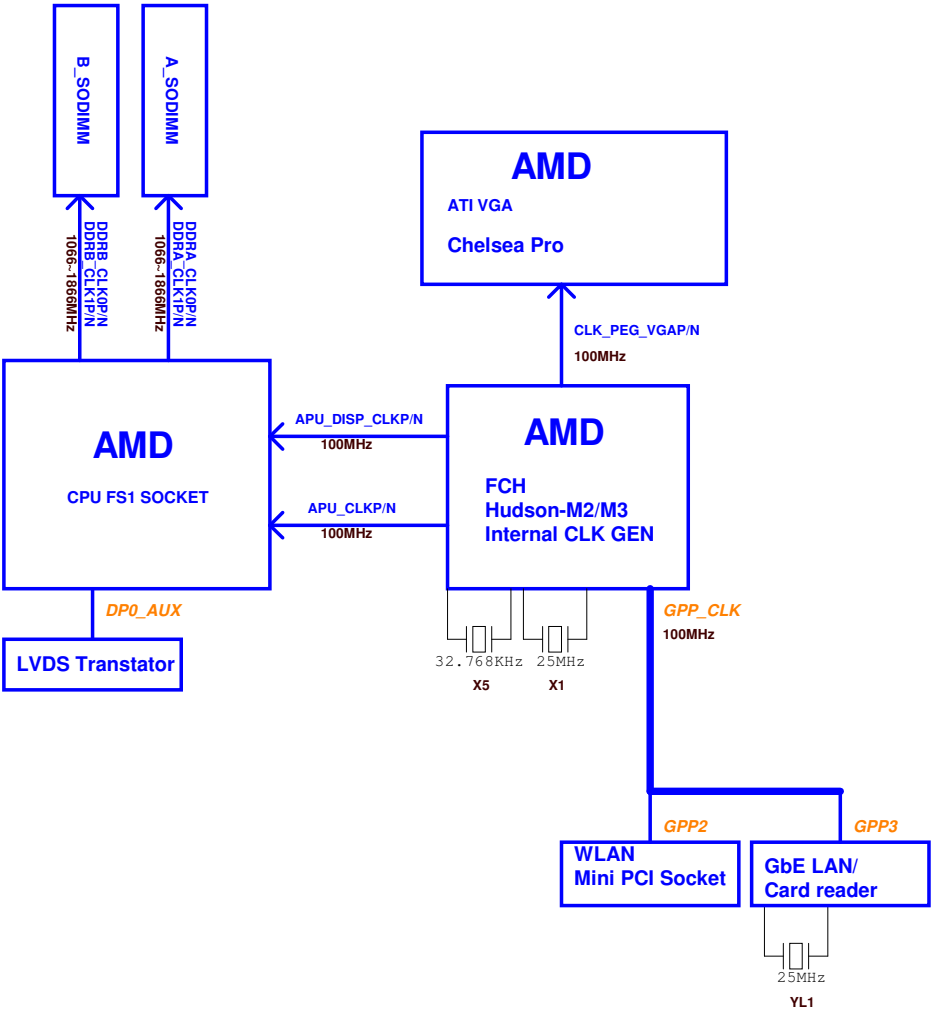
64M x16
128M x 16
VRAM DDR3
page 19, 20

AMD Comal

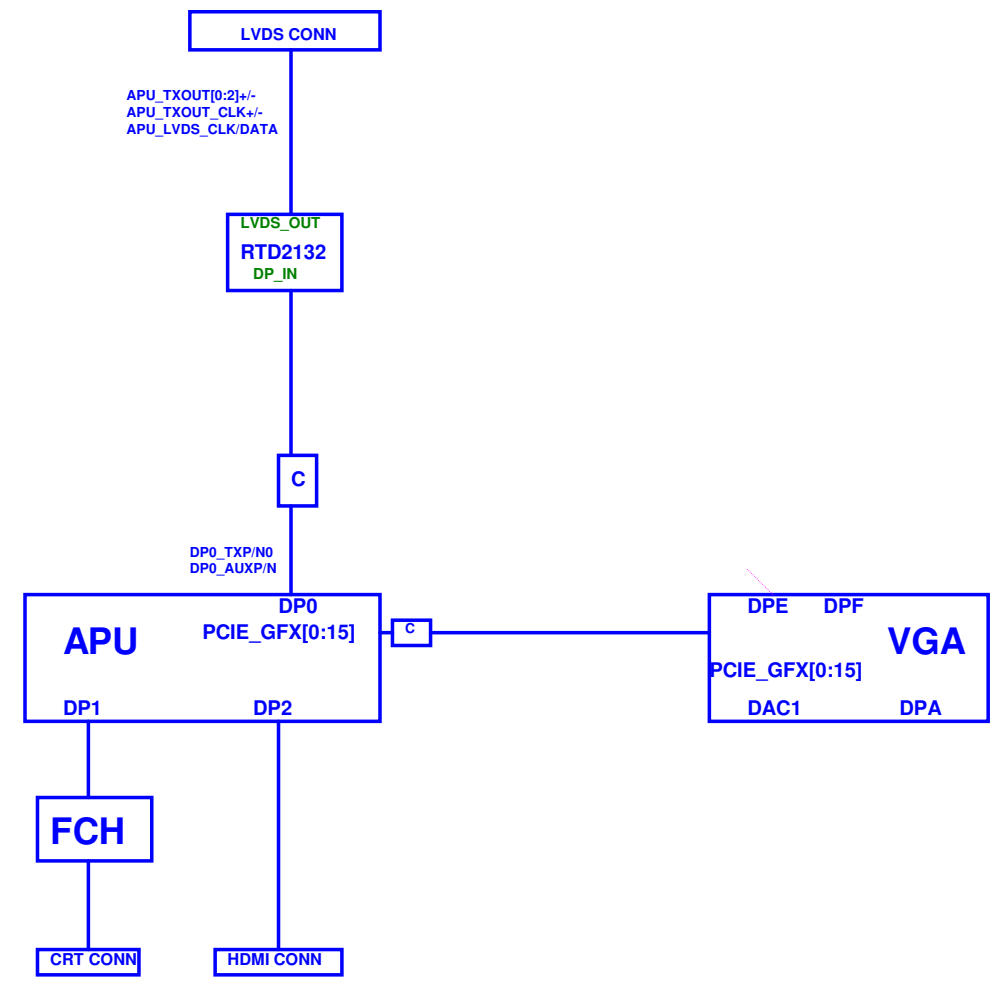


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CLOCK DISTRIBUTION



DISPLAY OUTPUT



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				CLOCK / DISPLAY DISTRIBUTION	

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+0.935VGS	0.935V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5V_PCIE	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_VDD_3V3	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
	Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW	
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF	
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rb	100K +/- 5%			
Board ID	Ra / Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

ZZZ1



PCB
Part Number = DA8000SH00
PCB OCH LA-8712P REV0 M/B

BOARD ID Table

Board ID	PCB Revision
0	DB
1	
2	
3	
4	
5	
6	
7	

BOM Option Table

BOM
Structure
PX@

Description
PX function

BOM Config

UMA
PX
V

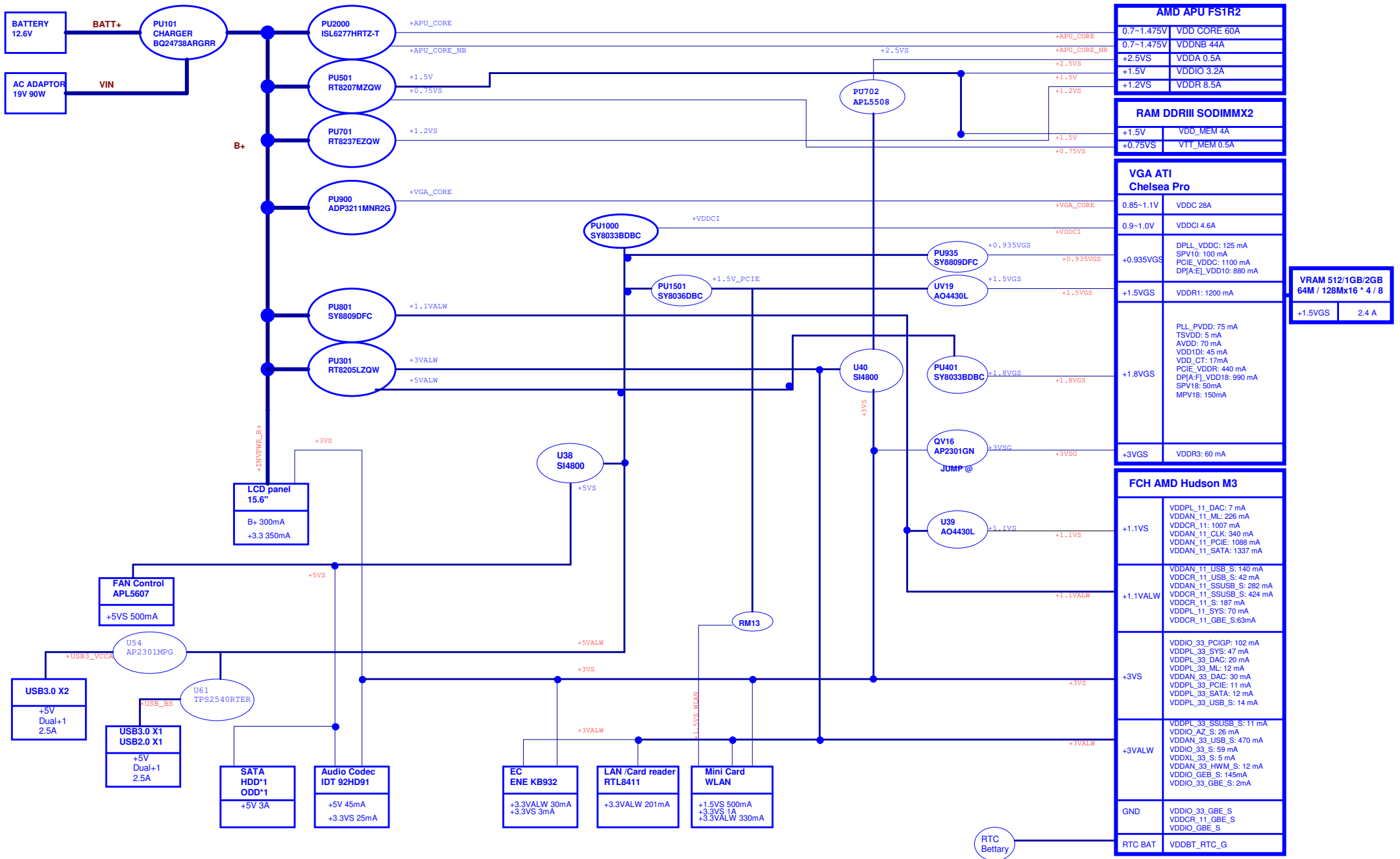
x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices			
Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (GPU)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH (S0) SM Bus 0 address			FCH (S0~S5) SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000X b	A0	Touch pad		
DDR DIMM2	1010 001X b	A2			
Amplifier					

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AMD APU FS1R2	
0.7~1.475V	VDD CORE 60A
0.7~1.475V	VDDNB 44A
+2.5VS	VDDA 0.5A
+1.5V	VDDIO 3.2A
+1.2VS	VDDR 8.5A





RAM DDRIII SODIMM X2	
+1.5V	VDD_MEM 4A
+0.75VS	V11_MEM 0.5A

VGA ATI Chelsea Pro	
0.85~1.1V	VDDCI 28A
0.9~1.0V	VDDCI 4.6A
+0.935VGS	DPLL_VDDC: 125 mA SPV10: 100 mA PCI_E_VDDC: 1100 mA DP[A:E]_VDD10: 880 mA
+1.5VGS	VDDR1: 1200 mA
+1.8VGS	PLL_PVDD: 75 mA TSVDD: 5 mA AVDD: 70 mA VDD1D: 45 mA VDD_CT: 17mA PCI_E_VDDR: 440 mA DP[A:F]_VDD18: 990 mA SPV18: 50mA MPV18: 150mA
+3VGS	VDDR3: 60 mA

VRAM 512/1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VGS	2.4 A

FCH AMD Hudson M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 42 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA VDDCR_11_GBE_S: 63mA
+3VS	VDDIO_33_PCIEP: 102 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 12 mA VDDAN_33_DAC: 30 mA VDDAN_33_PCIE: 11 mA VDDPL_33_SATA: 12 mA VDDPL_33_USB_S: 14 mA
+3VALW	VDDPL_33_SSUSB_S: 11 mA VDDIO_AZ_S: 26 mA VDDAN_33_USB_S: 470 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HMM_S: 12 mA VDDIO_GBE_S: 145mA VDDIO_33_GBE_S: 2mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G

13 PCIE_GTX_C_FRX_P[0..15]  
 13 PCIE_GTX_C_FRX_N[0..15]  

PCIE_FTX_C_GRX_P[0..15] 13  
 PCIE_FTX_C_GRX_N[0..15] 13  

JCPU1A
 PCI EXPRESS

PCIE GTX C FRX P0	AB8	P_GFX_RXP0	P_GFX_TXP0
PCIE GTX C FRX N0	AB7	P_GFX_RXN0	P_GFX_TXN0
PCIE GTX C FRX P1	AA9	P_GFX_RXP1	P_GFX_TXP1
PCIE GTX C FRX N1	AA8	P_GFX_RXN1	P_GFX_TXN1
PCIE GTX C FRX P2	AA5	P_GFX_RXP2	P_GFX_TXP2
PCIE GTX C FRX N2	AA6	P_GFX_RXN2	P_GFX_TXN2
PCIE GTX C FRX P3	Y8	P_GFX_RXP3	P_GFX_TXP3
PCIE GTX C FRX N3	Y7	P_GFX_RXN3	P_GFX_TXN3
PCIE GTX C FRX P4	W9	P_GFX_RXP4	P_GFX_TXP4
PCIE GTX C FRX N4	W8	P_GFX_RXN4	P_GFX_TXN4
PCIE GTX C FRX P5	W5	P_GFX_RXP5	P_GFX_TXP5
PCIE GTX C FRX N5	W6	P_GFX_RXN5	P_GFX_TXN5
PCIE GTX C FRX P6	V8	P_GFX_RXP6	P_GFX_TXP6
PCIE GTX C FRX N6	V7	P_GFX_RXN6	P_GFX_TXN6
PCIE GTX C FRX P7	U9	P_GFX_RXP7	P_GFX_TXP7
PCIE GTX C FRX N7	U8	P_GFX_RXN7	P_GFX_TXN7
PCIE GTX C FRX P8	U5	P_GFX_RXP8	P_GFX_TXP8
PCIE GTX C FRX N8	U6	P_GFX_RXN8	P_GFX_TXN8
PCIE GTX C FRX P9	T8	P_GFX_RXP9	P_GFX_TXP9
PCIE GTX C FRX N9	T7	P_GFX_RXN9	P_GFX_TXN9
PCIE GTX C FRX P10	R9	P_GFX_RXP10	P_GFX_TXP10
PCIE GTX C FRX N10	R8	P_GFX_RXN10	P_GFX_TXN10
PCIE GTX C FRX P11	R5	P_GFX_RXP11	P_GFX_TXP11
PCIE GTX C FRX N11	R6	P_GFX_RXN11	P_GFX_TXN11
PCIE GTX C FRX P12	P8	P_GFX_RXP12	P_GFX_TXP12
PCIE GTX C FRX N12	P7	P_GFX_RXN12	P_GFX_TXN12
PCIE GTX C FRX P13	N9	P_GFX_RXP13	P_GFX_TXP13
PCIE GTX C FRX N13	N8	P_GFX_RXN13	P_GFX_TXN13
PCIE GTX C FRX P14	N5	P_GFX_RXP14	P_GFX_TXP14
PCIE GTX C FRX N14	N6	P_GFX_RXN14	P_GFX_TXN14
PCIE GTX C FRX P15	M8	P_GFX_RXP15	P_GFX_TXP15
PCIE GTX C FRX N15	M7	P_GFX_RXN15	P_GFX_TXN15

GRAPHICS

GPU

GPU

GLAN/Card reader
 WLAN

31 PCIE_DTX_C_FRX_P0	AE5	P_GPP_RXP0	P_GPP_TXP0
31 PCIE_DTX_C_FRX_N0	AE6	P_GPP_RXN0	P_GPP_TXN0
32 PCIE_DTX_C_FRX_P1	AD8	P_GPP_RXP1	P_GPP_TXP1
32 PCIE_DTX_C_FRX_N1	AD7	P_GPP_RXN1	P_GPP_TXN1
	AC9	P_GPP_RXP2	P_GPP_TXP2
	AC8	P_GPP_RXN2	P_GPP_TXN2
	AC5	P_GPP_RXP3	P_GPP_TXP3
	AC6	P_GPP_RXN3	P_GPP_TXN3

GPP

AD5 PCIE_FTX_DRX_P0	C950	1	2	.1U 0402 16V7K	PCIE_FTX_C_DRX_P0	31
AD4 PCIE_FTX_DRX_N0	C951	1	2	.1U 0402 16V7K	PCIE_FTX_C_DRX_N0	31
AD2 PCIE_FTX_DRX_P1	C952	1	2	.1U 0402 16V7K	PCIE_FTX_C_DRX_P1	32
AD1 PCIE_FTX_DRX_N1	C953	1	2	.1U 0402 16V7K	PCIE_FTX_C_DRX_N1	32

GLAN/Card reader
 WLAN

UMI

25 UMI_MTX_C_FRX_P0	AG8	P_UMI_RXP0	P_UMI_TXP0
25 UMI_MTX_C_FRX_N0	AG9	P_UMI_RXN0	P_UMI_TXN0
25 UMI_MTX_C_FRX_P1	AG6	P_UMI_RXP1	P_UMI_TXP1
25 UMI_MTX_C_FRX_N1	AG5	P_UMI_RXN1	P_UMI_TXN1
25 UMI_MTX_C_FRX_P2	AF7	P_UMI_RXP2	P_UMI_TXP2
25 UMI_MTX_C_FRX_N2	AF8	P_UMI_RXN2	P_UMI_TXN2
25 UMI_MTX_C_FRX_P3	AE8	P_UMI_RXP3	P_UMI_TXP3
25 UMI_MTX_C_FRX_N3	AE9	P_UMI_RXN3	P_UMI_TXN3



UMI

AG2 UMI_FTX_MRX_P0	C956	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_P0	25
AG3 UMI_FTX_MRX_N0	C957	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_N0	25
AF4 UMI_FTX_MRX_P1	C958	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_P1	25
AF5 UMI_FTX_MRX_N1	C959	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_N1	25
AF1 UMI_FTX_MRX_P2	C960	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_P2	25
AF2 UMI_FTX_MRX_N2	C961	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_N2	25
AE2 UMI_FTX_MRX_P3	C962	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_P3	25
AE3 UMI_FTX_MRX_N3	C963	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_N3	25

UMI

+1.2VS  1 R539  2 P_ZVDDP AG11 196_0402_1%

 P_ZVDDP W/S=8/12 mil, <3000mil

AH11  1 P_ZVSS  2 R540 196_0402_1%

 P_ZVSS W/S=8/12 mil, <3000mil

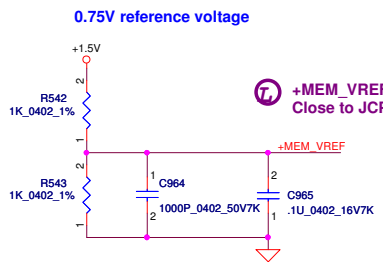
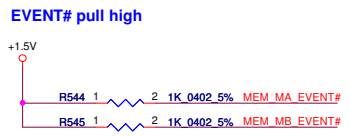
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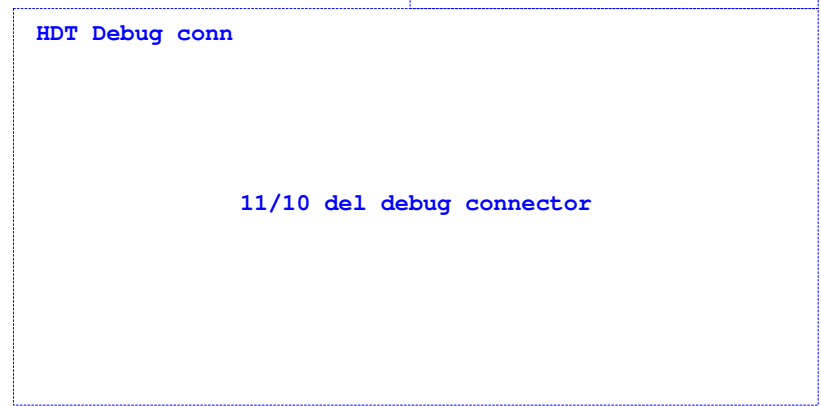
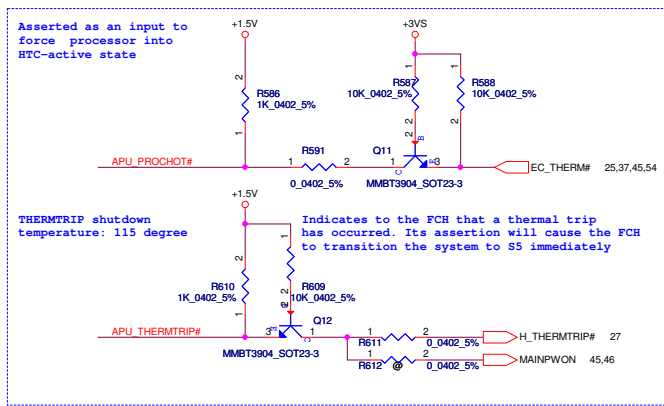
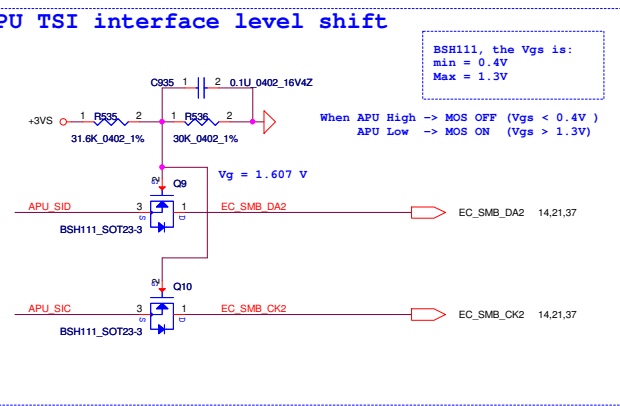
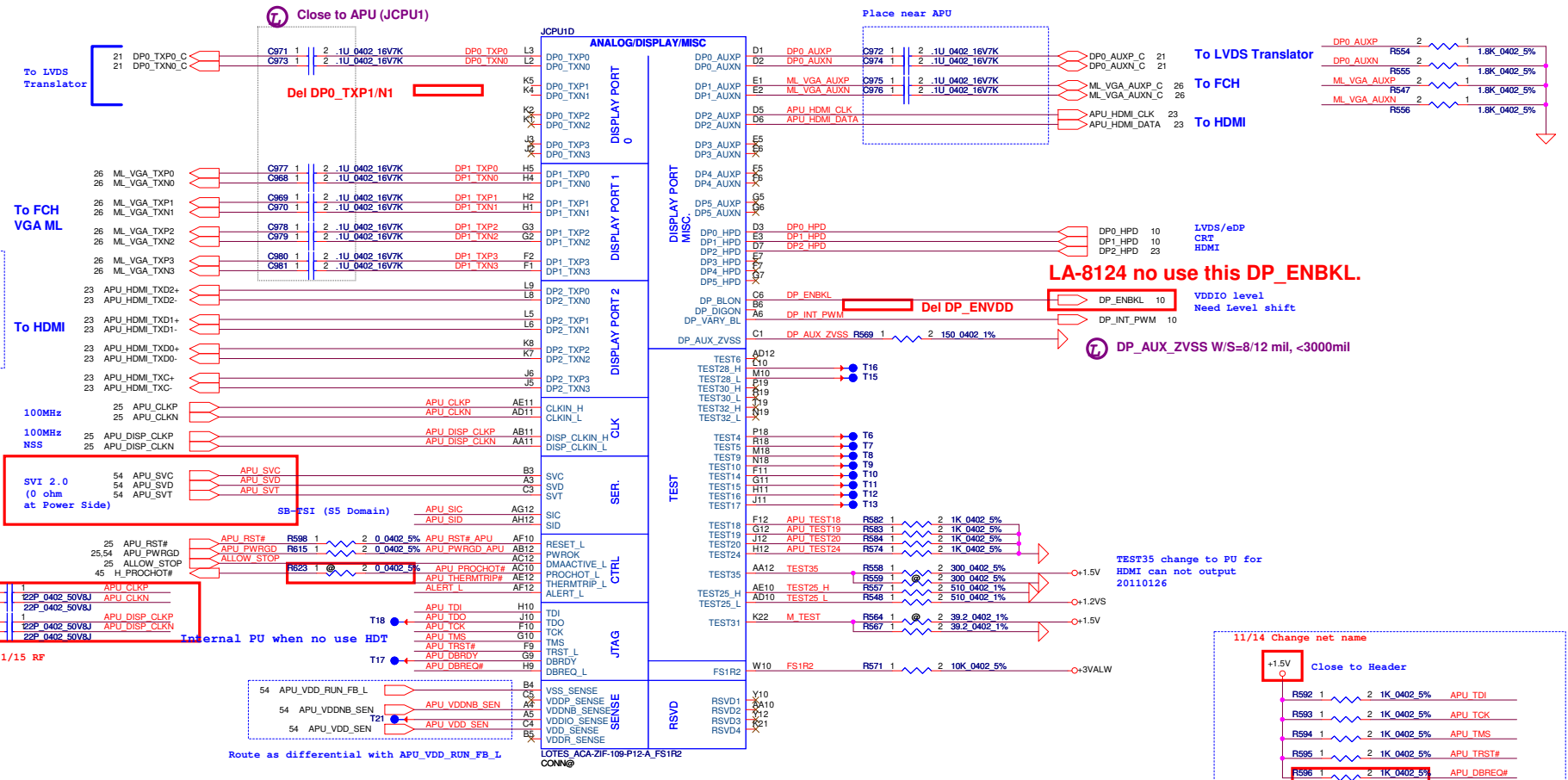
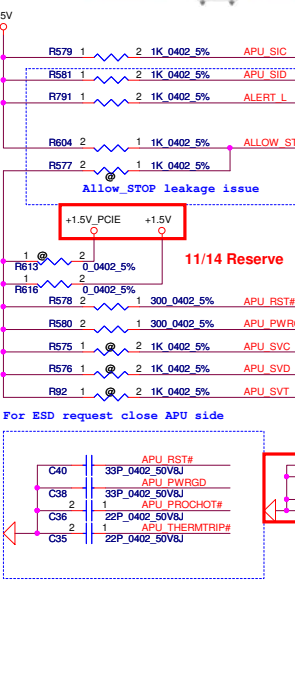
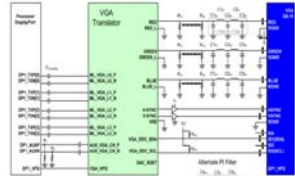
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LOTES_ACA-ZIF-109-P12-A_FS1R2 CONN@



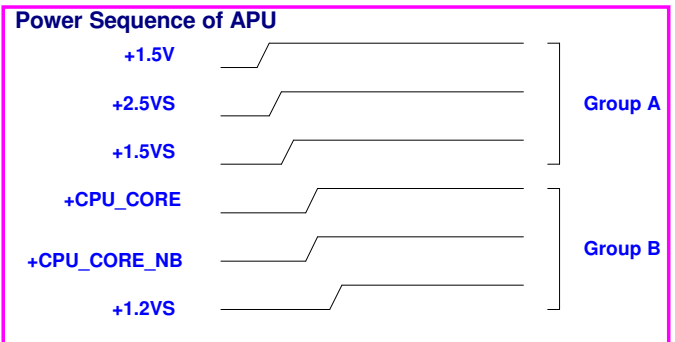
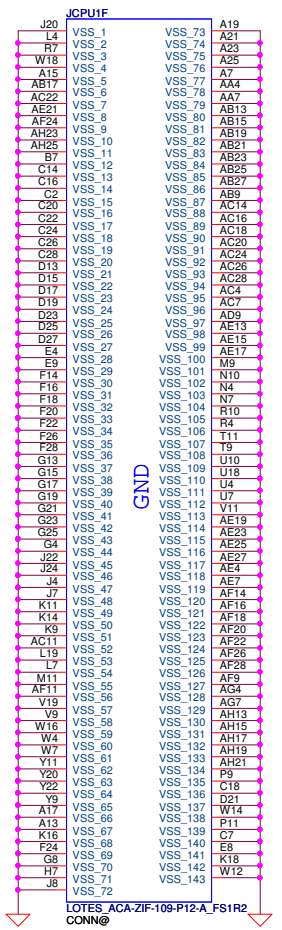
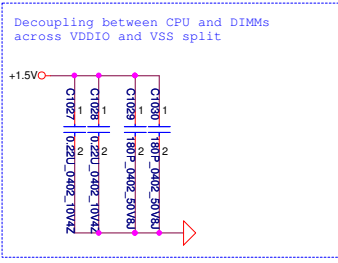
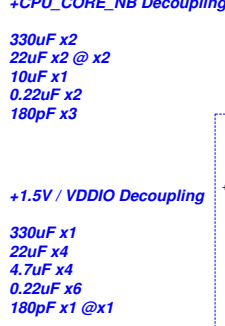
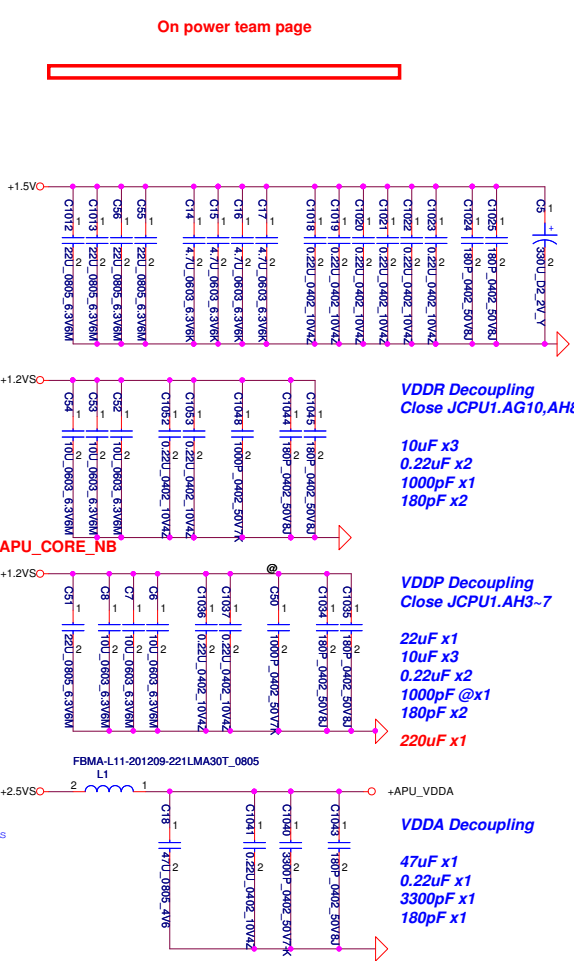
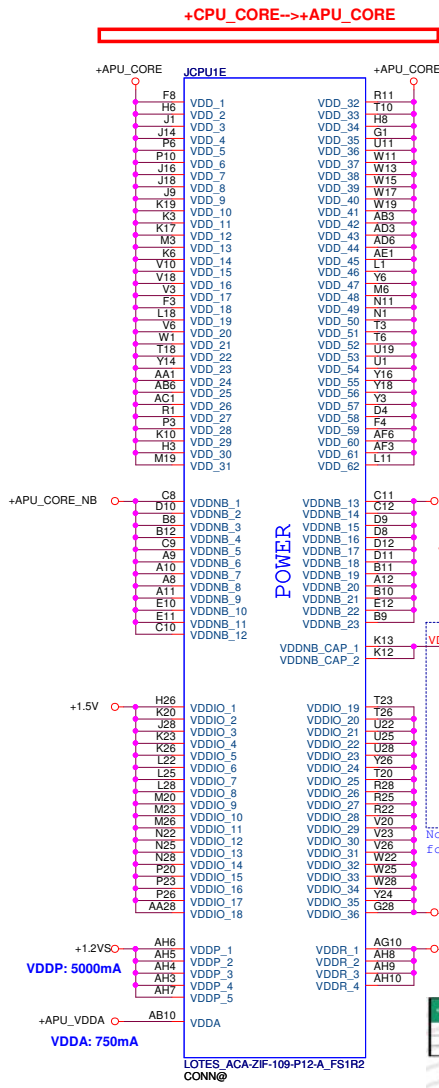
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Figure 44. Schematic Diagram--DisplayPort, Translator and VGA



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Power Name	Consumption
VDD	
+CPU_CORE	60A
VDDNB	
+CPU_CORE_NB	37A
VDDIO	
+1.5V	3.2A
VDDP / VDDR	
+1.2VS	5A / 3.5A
VDDA	
+2.5VS	0.75A

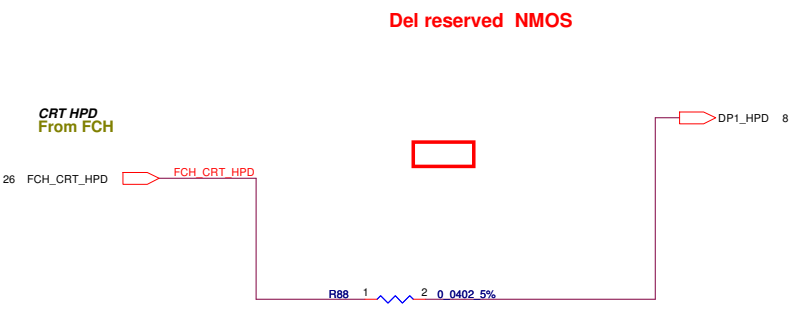
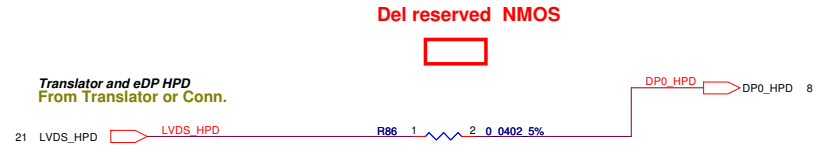


Decoupling Caps.

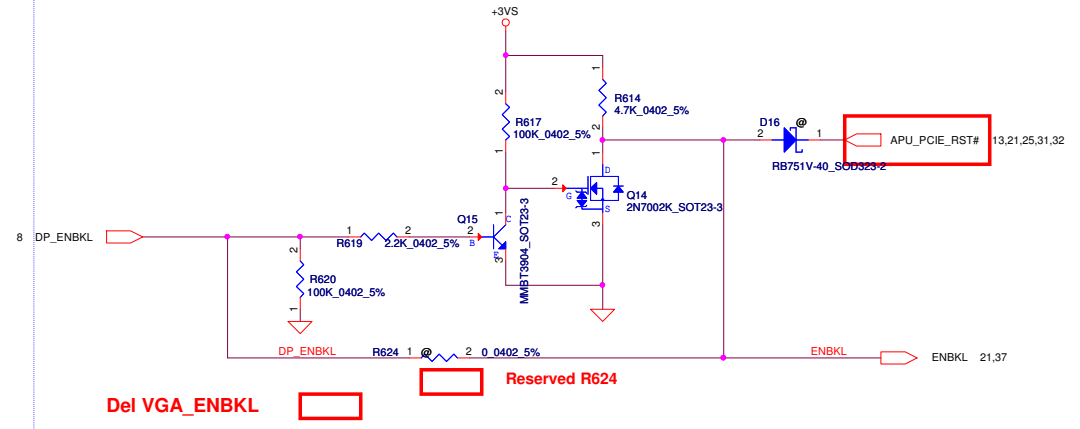
Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0		0	19/11	7	5	17	3	1	1 / 1	13/3	
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

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HPD



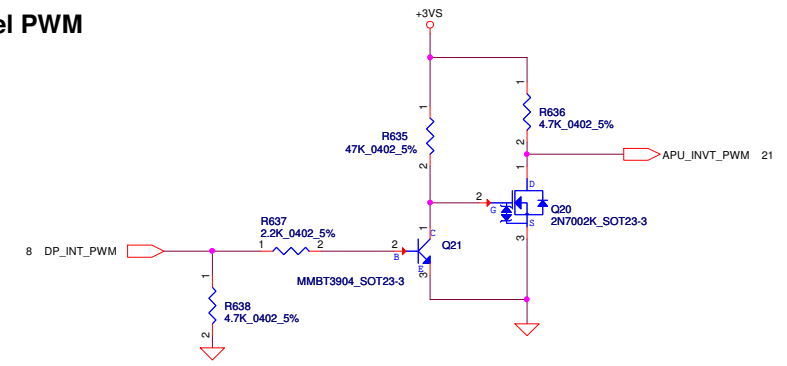
Panel ENBKL LA-8124 no use this DP_ENBKL.



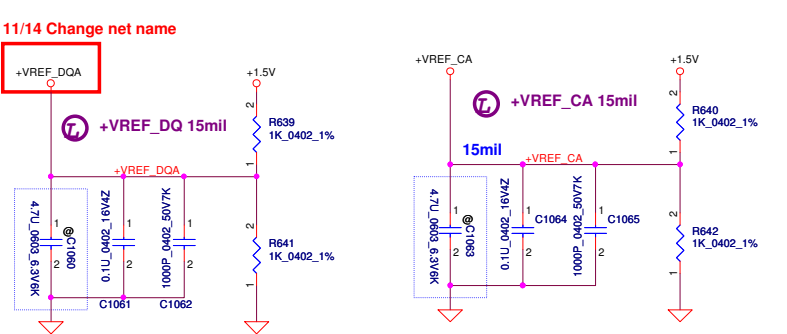
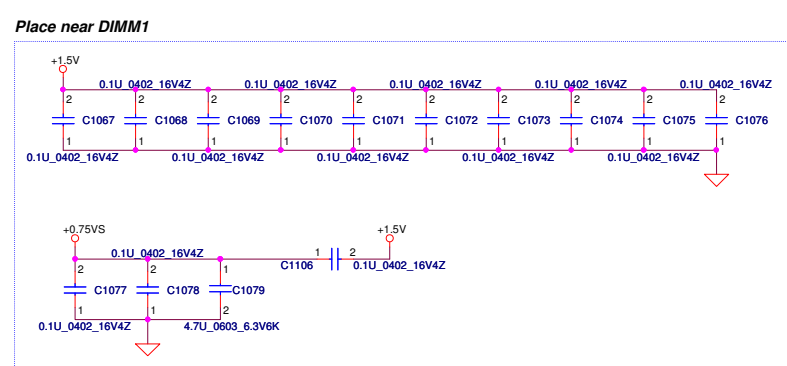
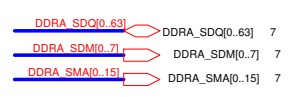
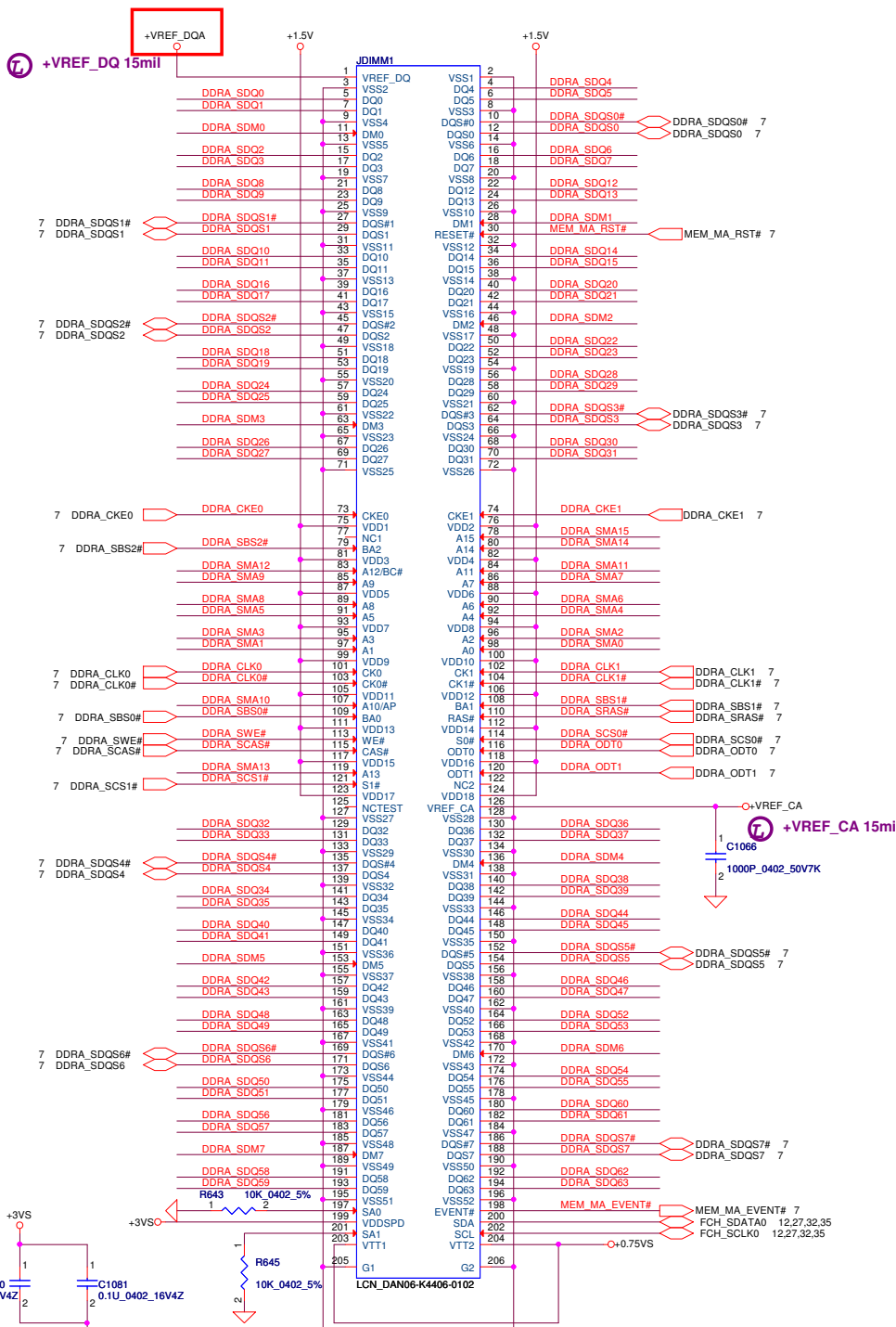
eDP Panel ENVDD



Panel PWM

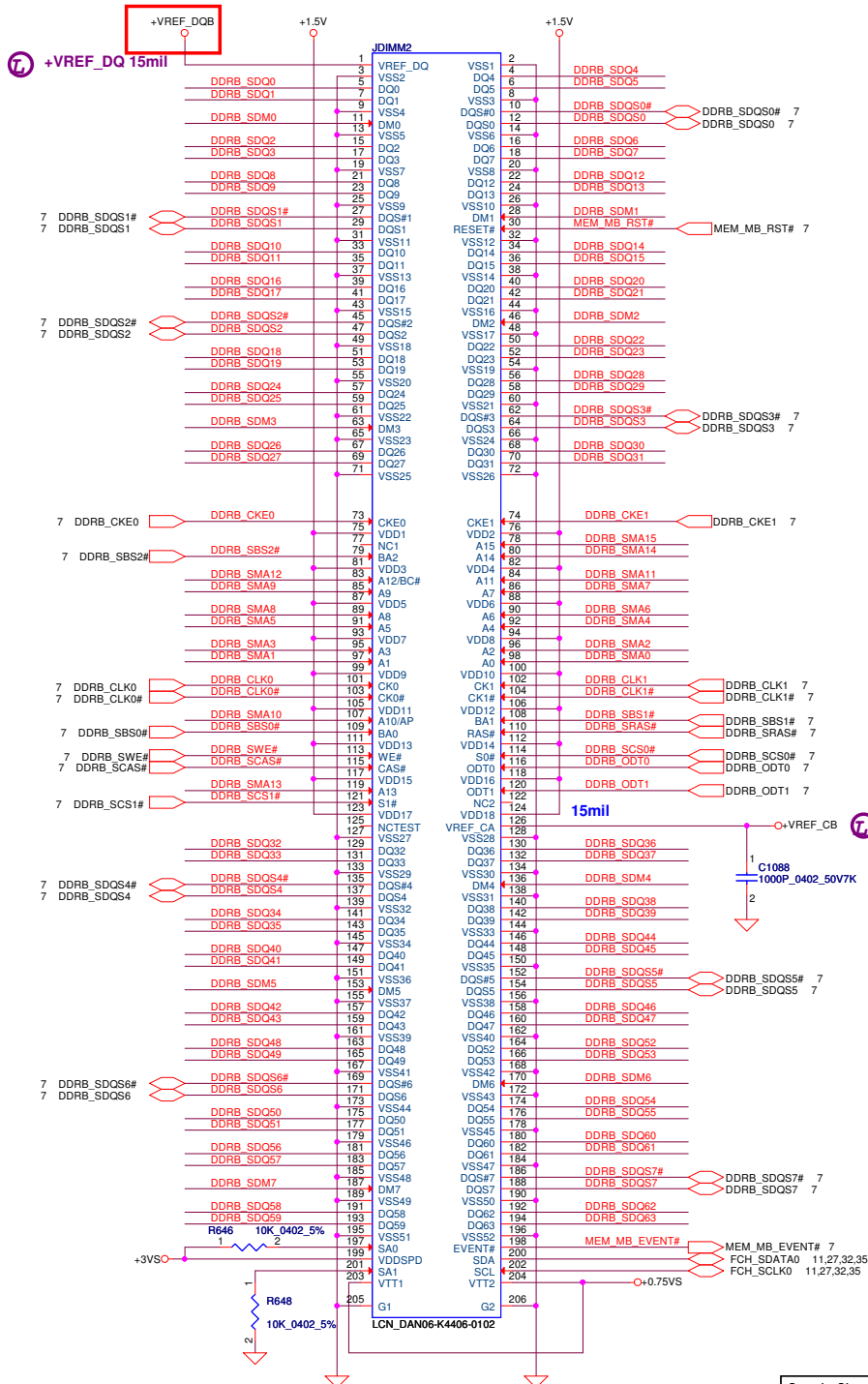


Security Classification	Compal Secret Data			Title	AMD FS1R2 Singal Level Shifter	
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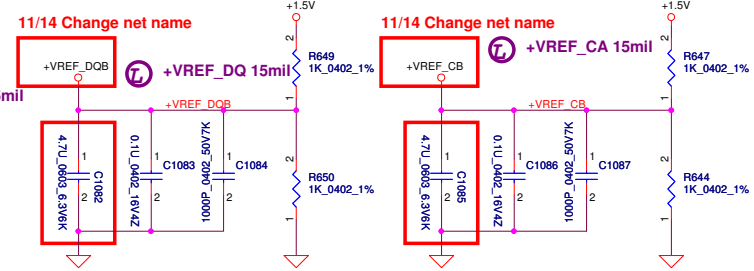
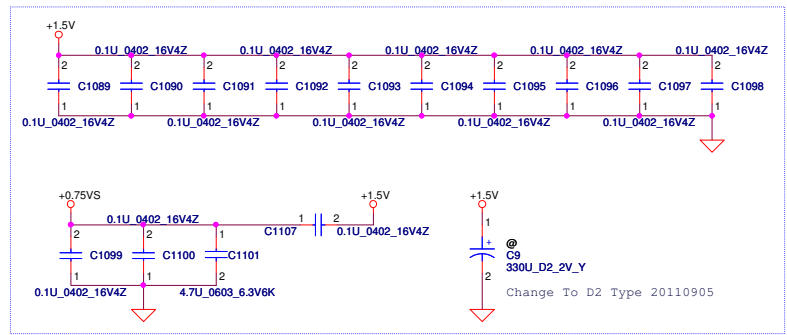


DIMM_A REV H:4mm
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				0.1



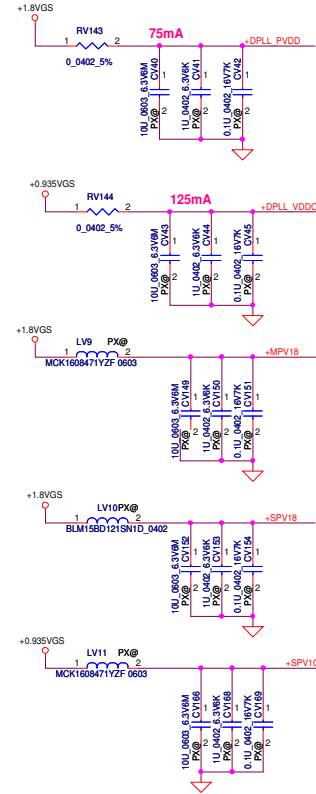
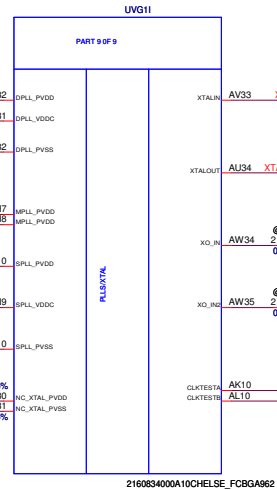
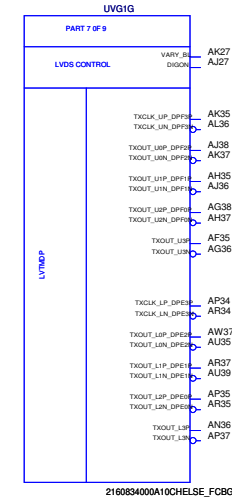
Place near DIMM2



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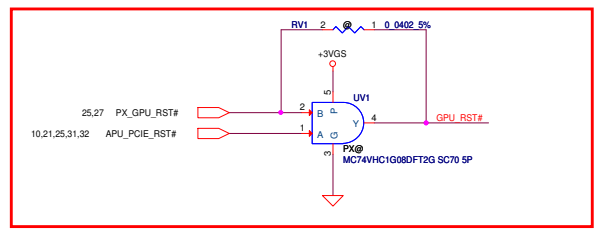
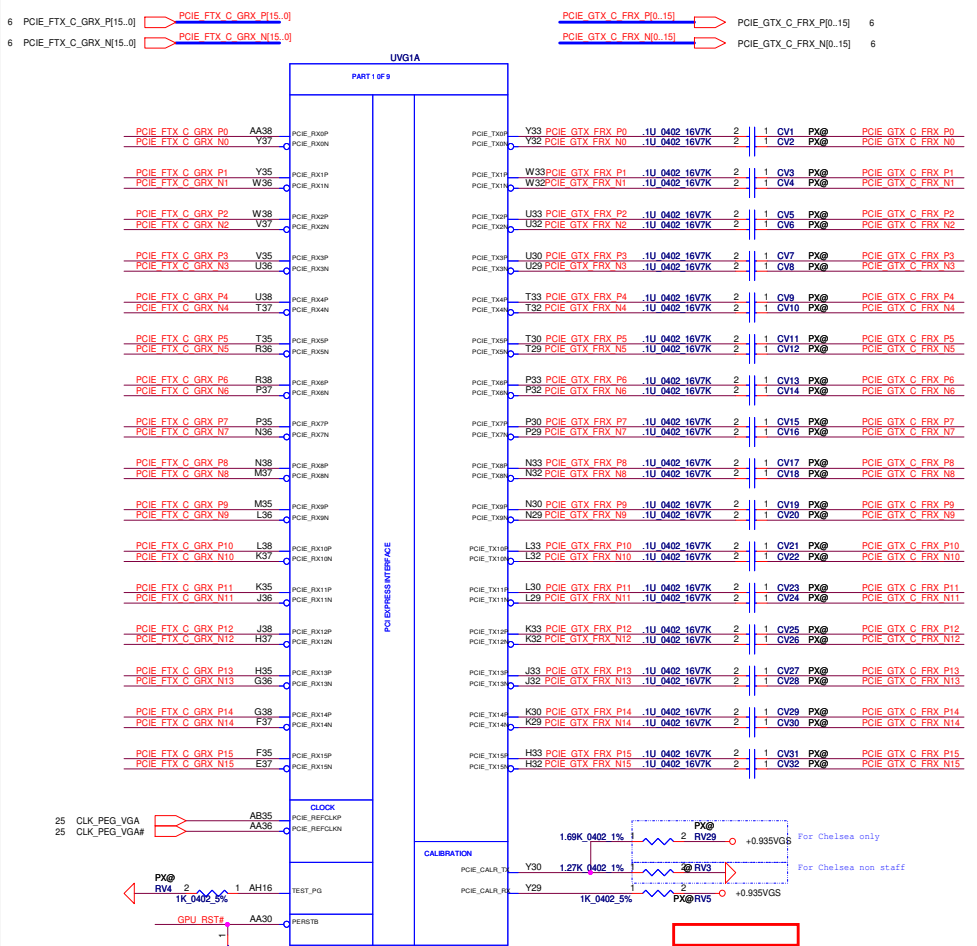
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LVDS Interface

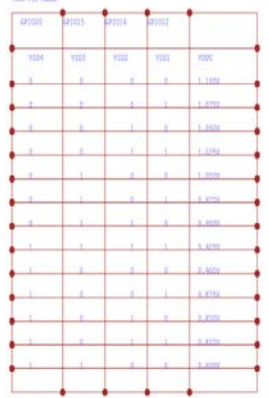


route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DN1 5mil 5mil

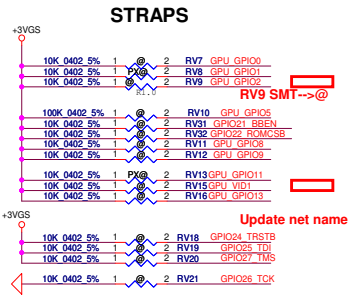
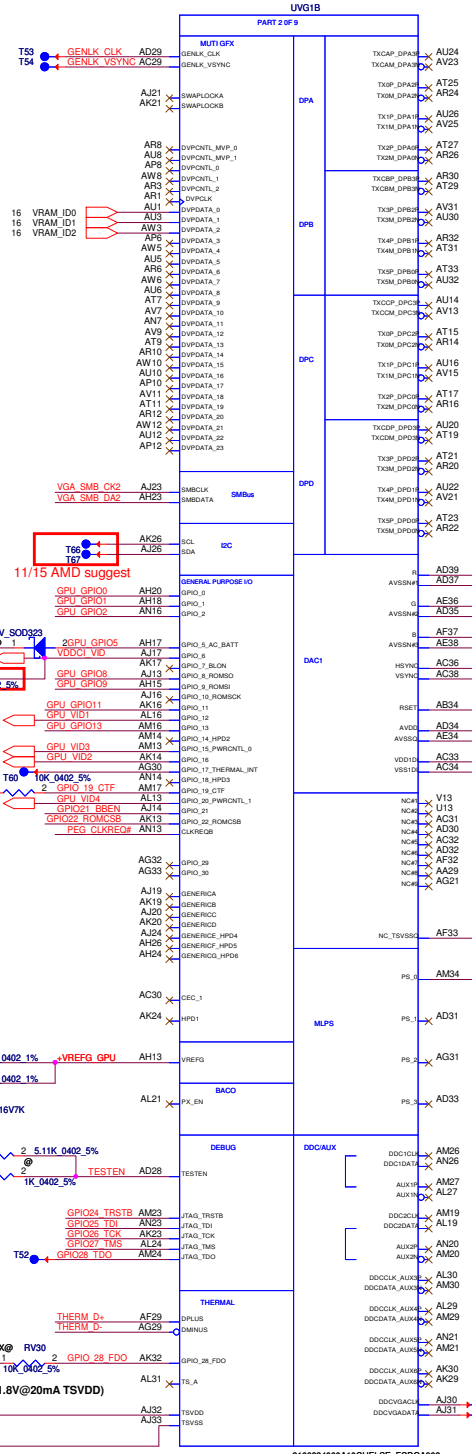
PCIE GTX C FRX P0..15] PCIE GTX_C_FRX_P0..15] 6
PCIE GTX C FRX N0..15] PCIE GTX_C_FRX_N0..15] 6



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Size	C	Document Number	QCL51 LA-8712P
Date	Monday, November 28, 2011	Sheet	13 of 56



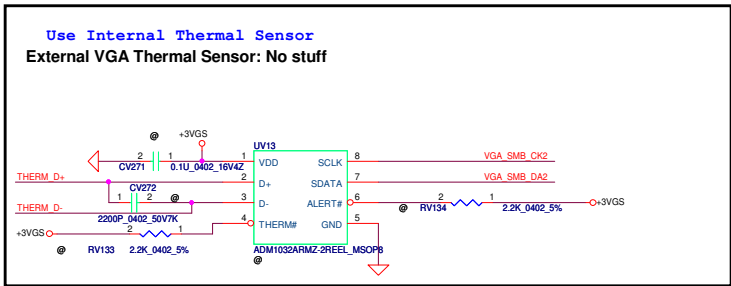
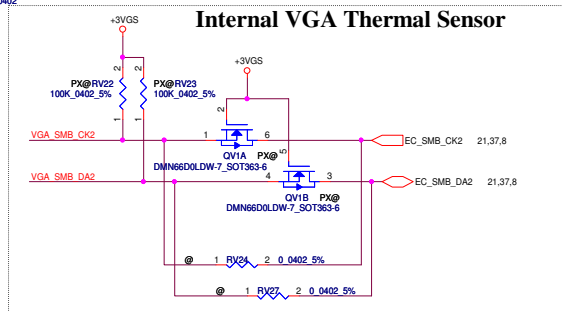
VRAM ID



CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
RECOMMENDED SETTINGS			
0 = DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS <all internal PD>	RECOMMENDED SETTINGS
TX_PWRs_ENB	GPIO0	PCIe TRANSMITTER Power Saving Enable	0: 50% swing 1: Full swing X
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS	0: disable 1: enable X
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.50T/s 1: 50T/s 0
RSVD	GPIO8	Internal use only. This Pad has an internal PD and Must be 0V at reset. The pad may be left unconnected.	0
RSVD	H2SYNC		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSYSNC	1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	

AMD RESERVED CONFIGURATION STRAPS
 ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

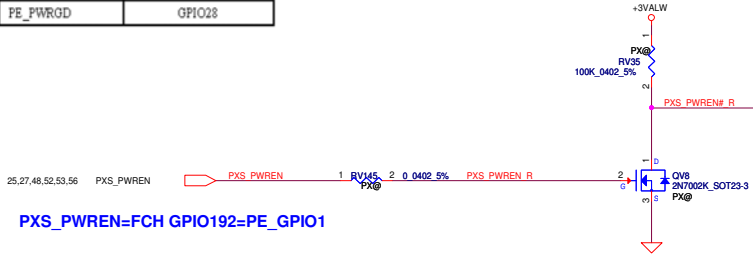
TX_PWRs_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



Name	FCH Pin Assignments
FE_GPIO0	GPIO191
FE_GPIO1	GPIO192
FE_PWRGD	GPIO28

GPU_Reset

PWREN

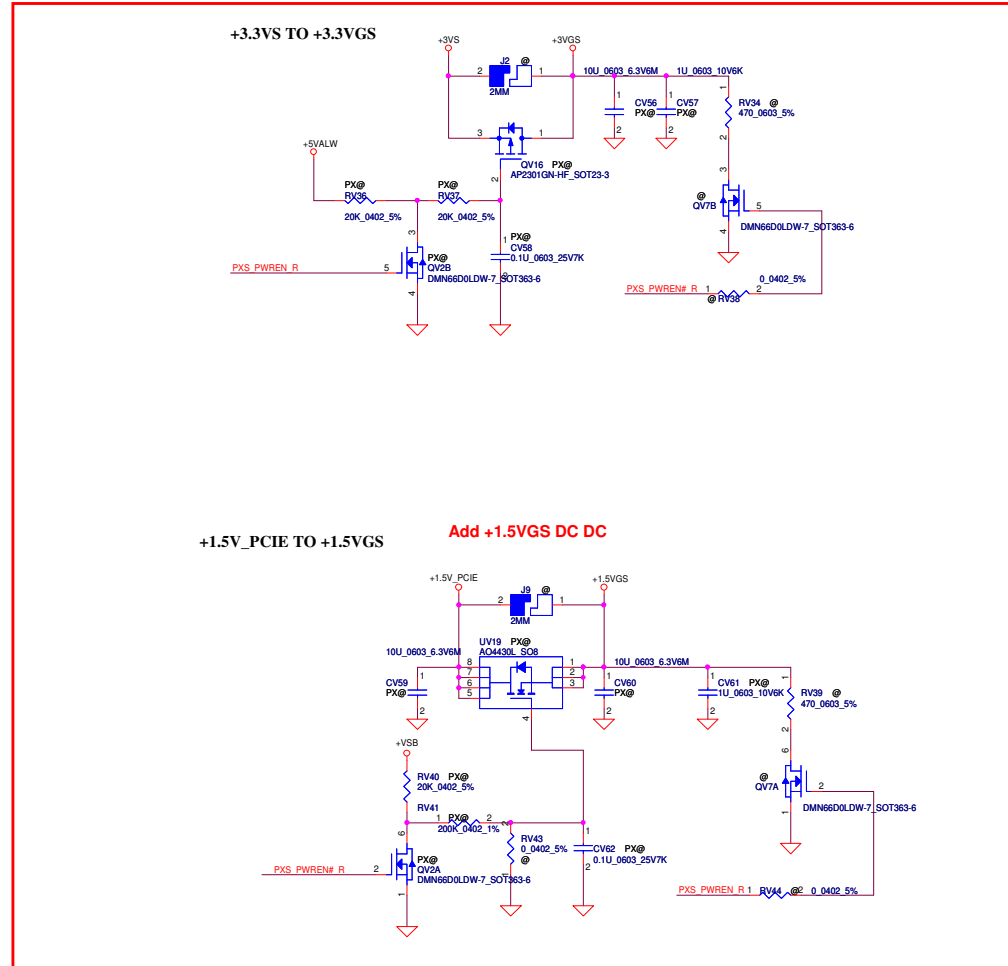


PXS_PWREN=FCH GPIO192=PE_GPIO1

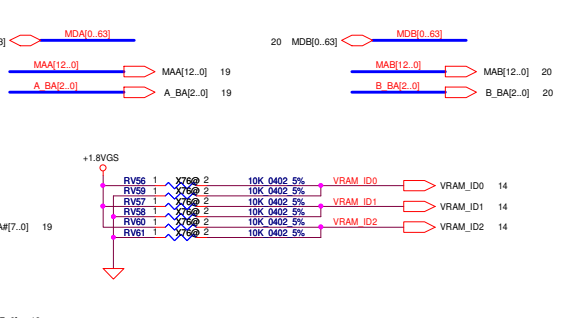
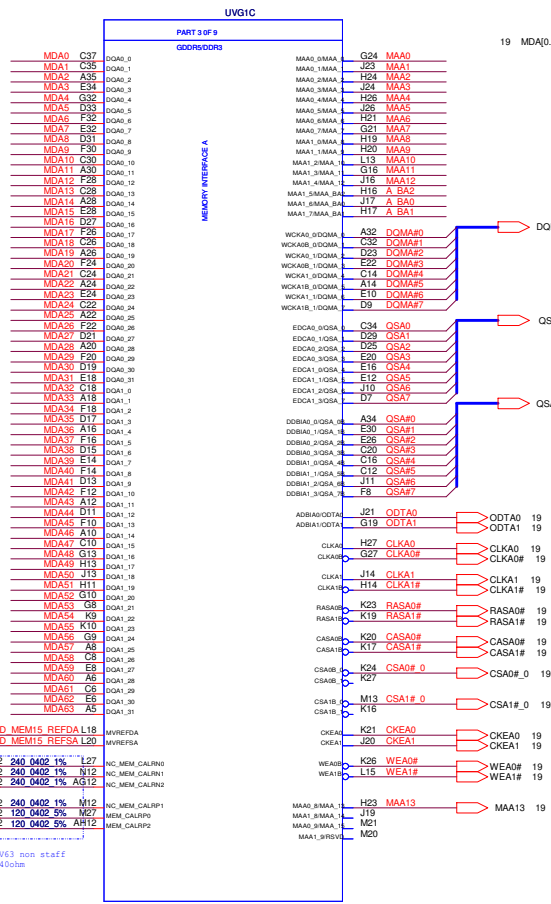
Del +1.8VGS DC DC



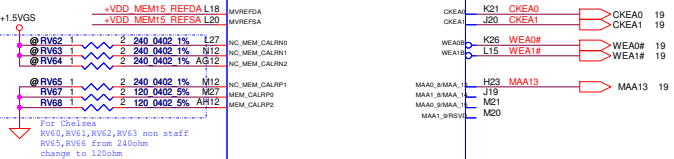
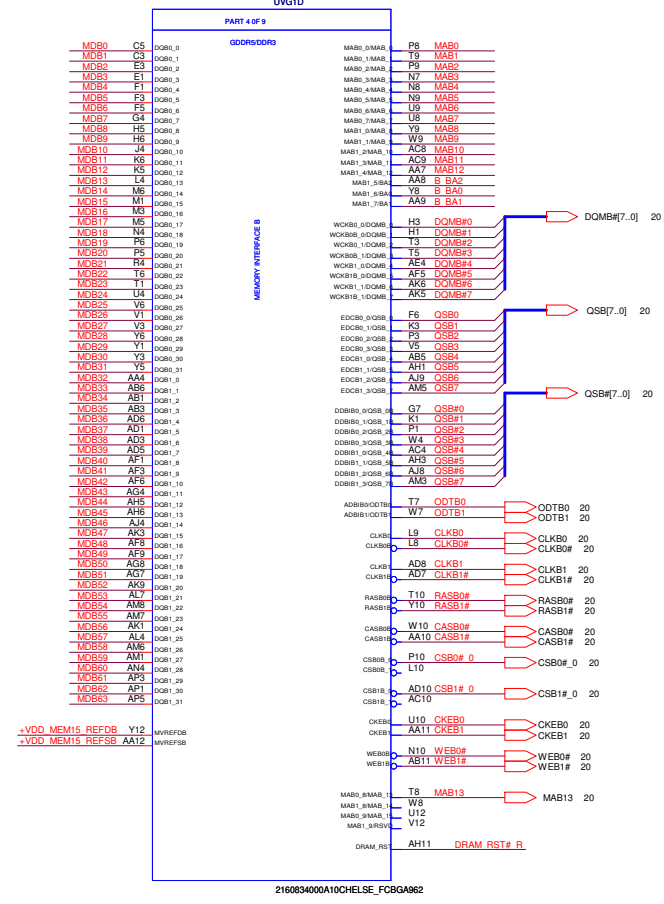
11/10 follow Lotus



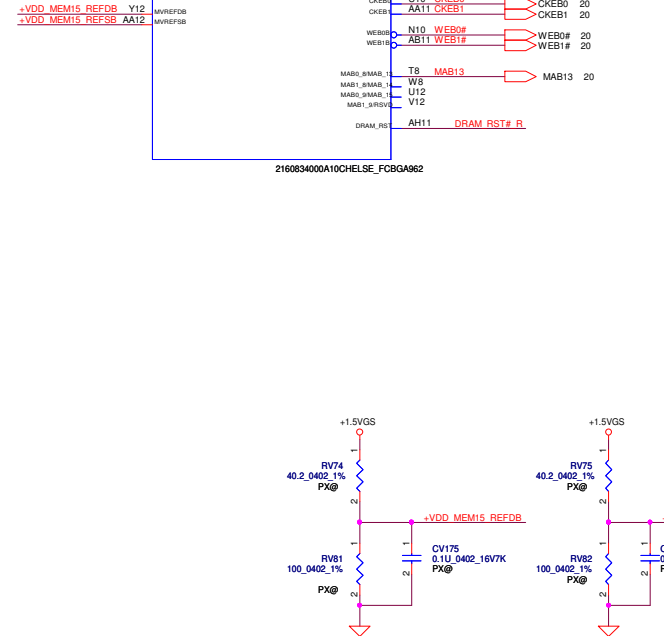
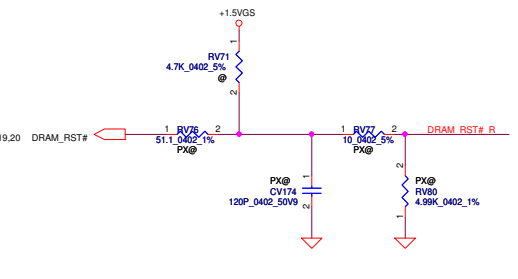
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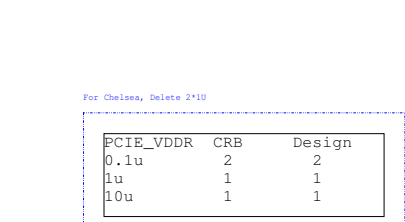
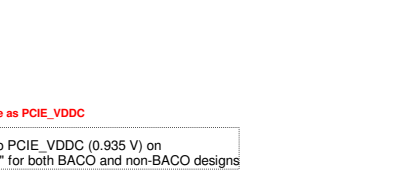
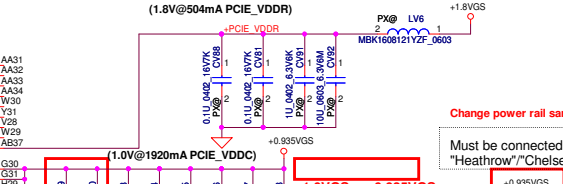
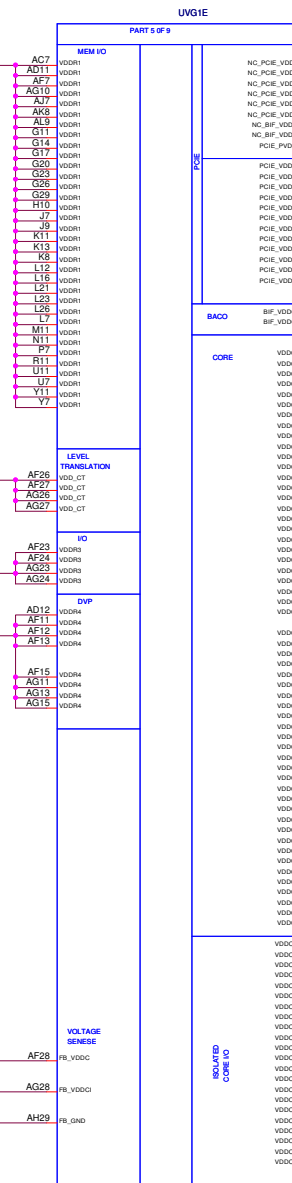
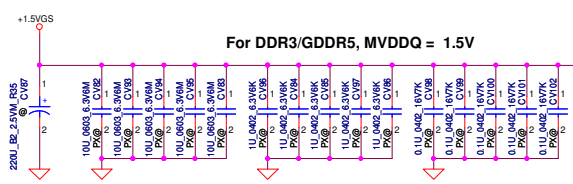


Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix 2GB H5TQ2G63DFR-11C PN:SA00003YO70	RV56	RV58	RV61
Samsung 2GB K4D50166EC-0611	RV56	RV57	RV61
Hynix 1GB H5TQ1G63DFR-11C PN:SA000041S20	RV59	RV58	RV60
Samsung 1GB K4D50166EC-0611 PN:SA00004GS20	RV59	RV57	RV60



This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2





VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
0.1u	3	3
1u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	1	1
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

56 VCC_GPU_SENSE
53 VDDCI_SEN
56 VSS_GPU_SENSE

VCC_GPU_SENSE & VSS_GPU_SENSE needs to be routed as differential pair

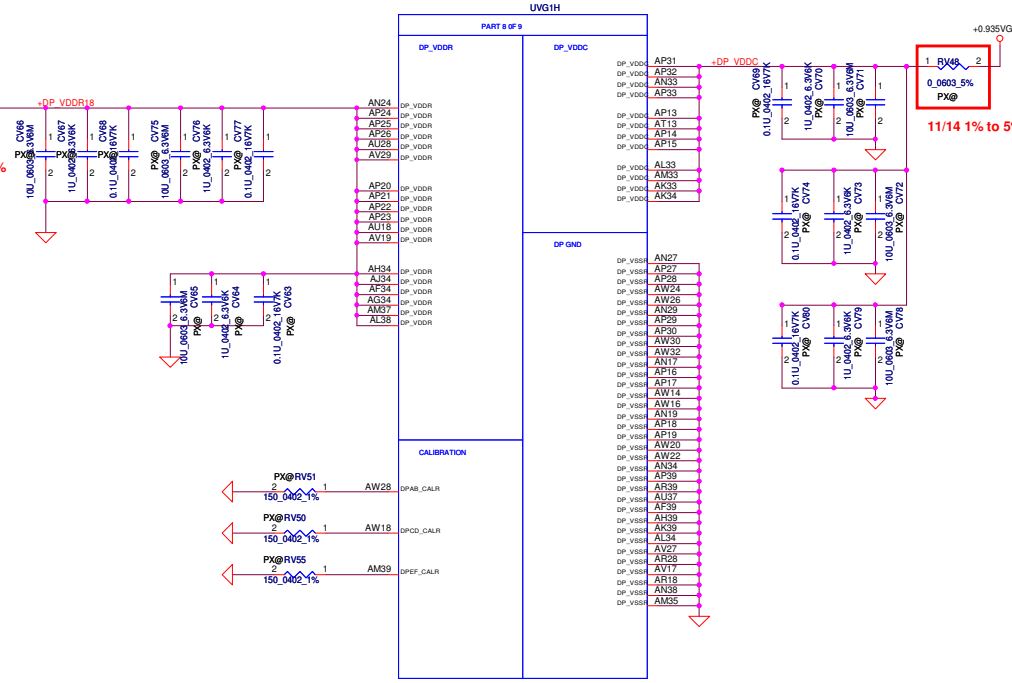
11/09 On power team page

On power team page

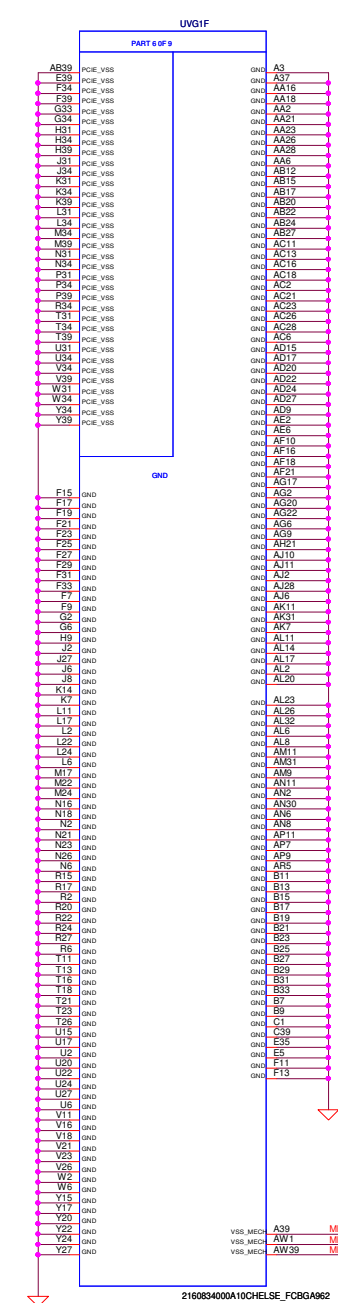
2160834000A10CHELSE_FC8GA962

VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

+1.8VGS
 1 RV47 2
 0.0603 5%
 PX@
 11/14 1% to 5%

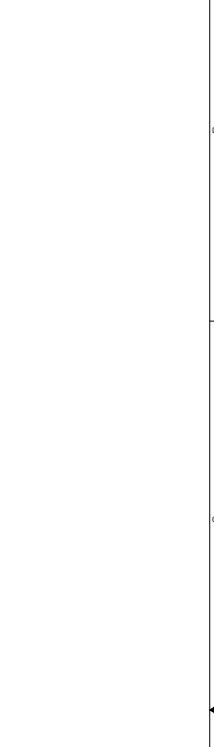
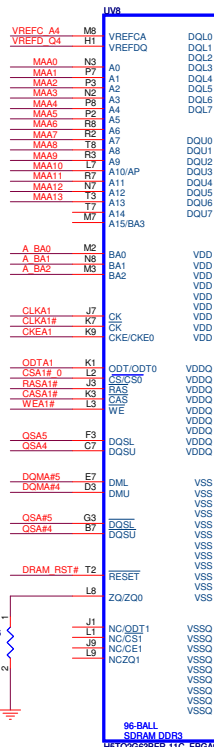
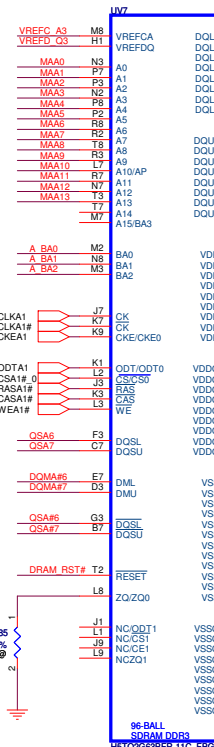
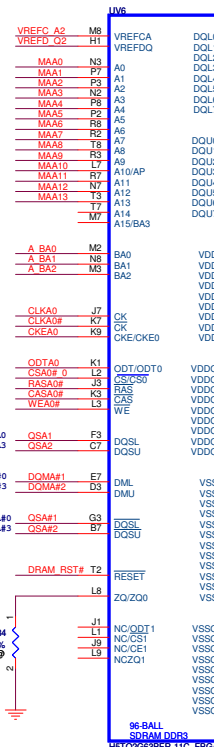
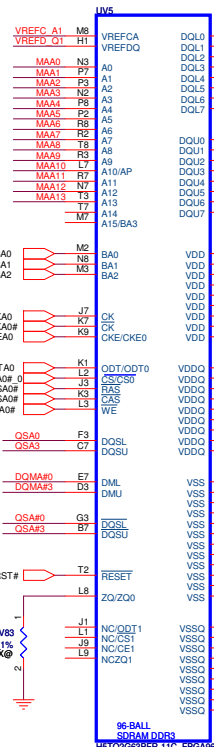
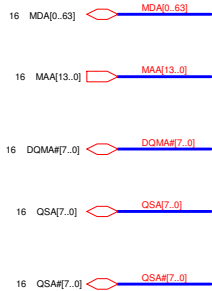


+0.935VGS
 1 RV48 2
 0.0603 5%
 PX@
 11/14 1% to 5%

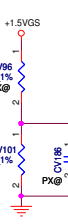
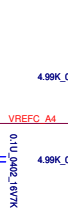
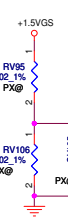
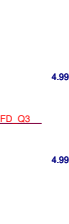
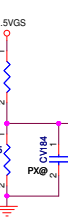
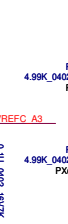
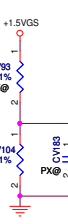
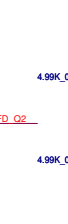
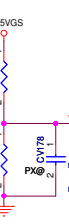
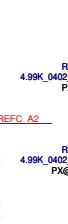
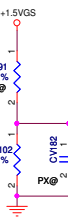
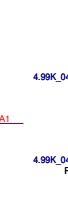
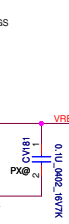
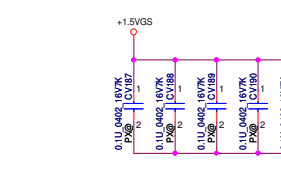
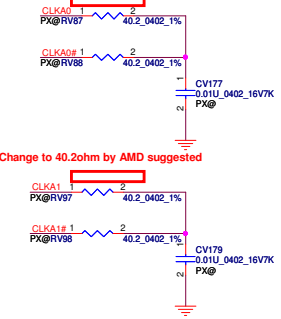


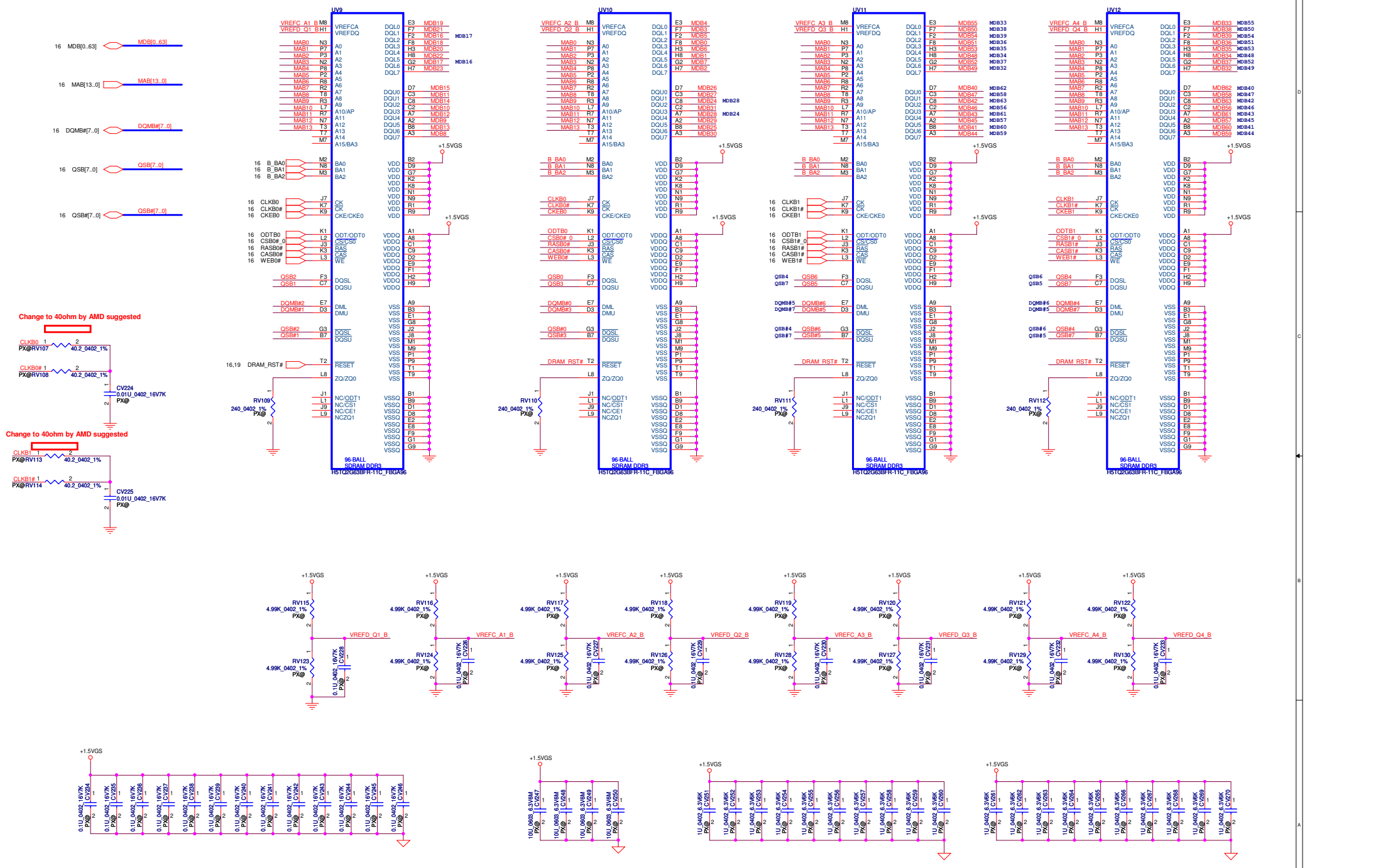
VSS_MECH A39 MECH#1
 VSS_MECH AW11 MECH#2
 VSS_MECH AW39 MECH#3
 T56 PAD
 T56 PAD
 T57 PAD

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Size	C	Document Number	QCL51 LA-8712P	Rev
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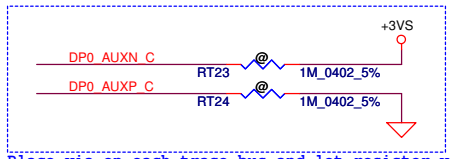
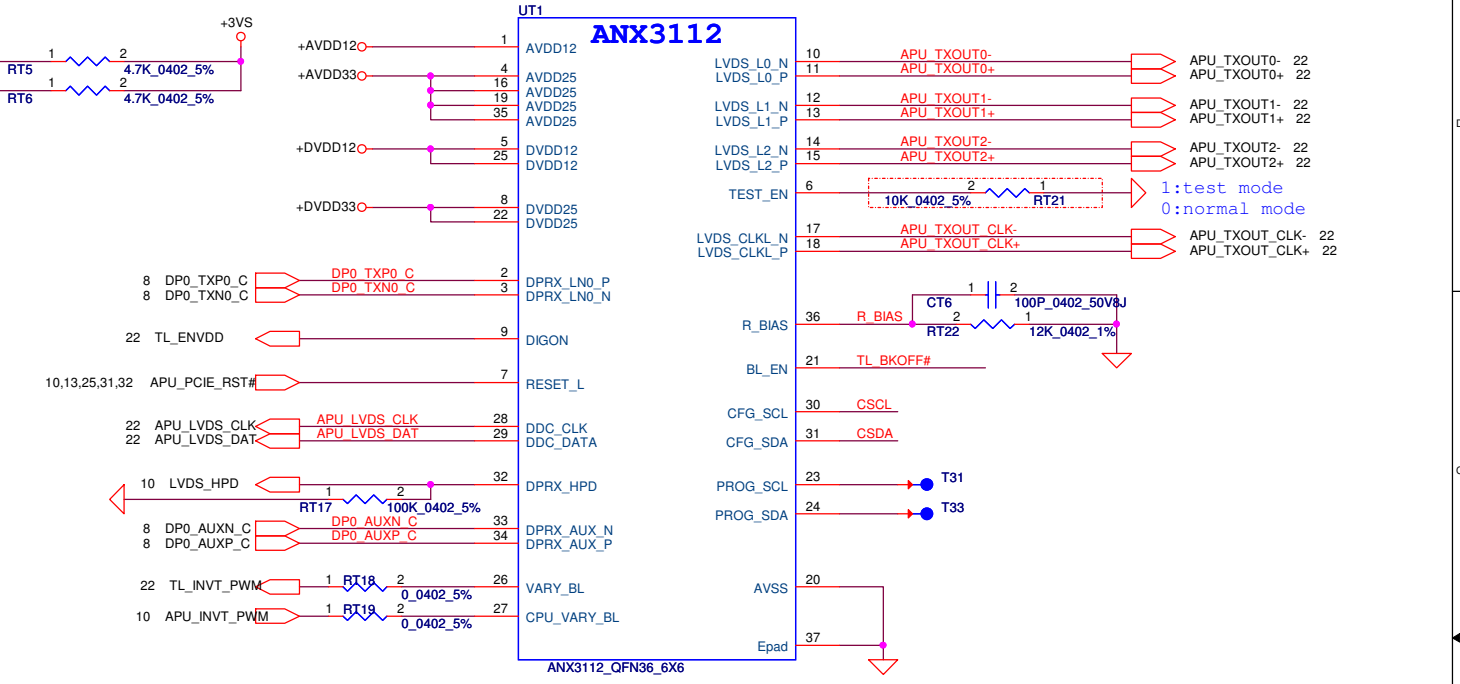
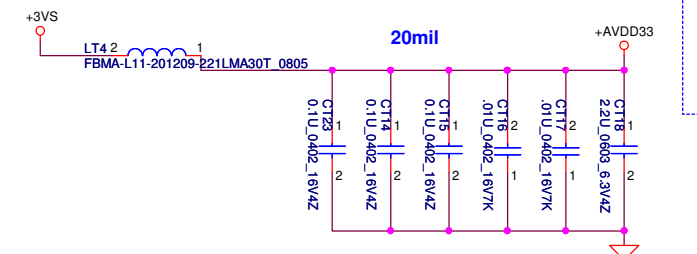
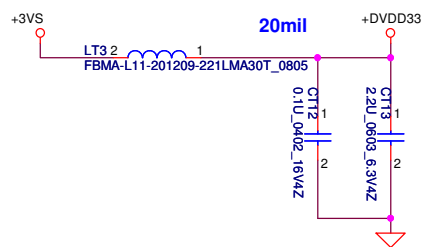
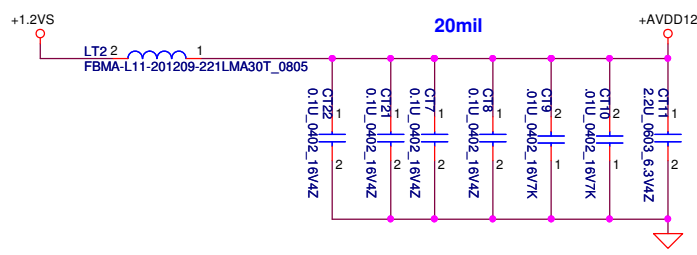
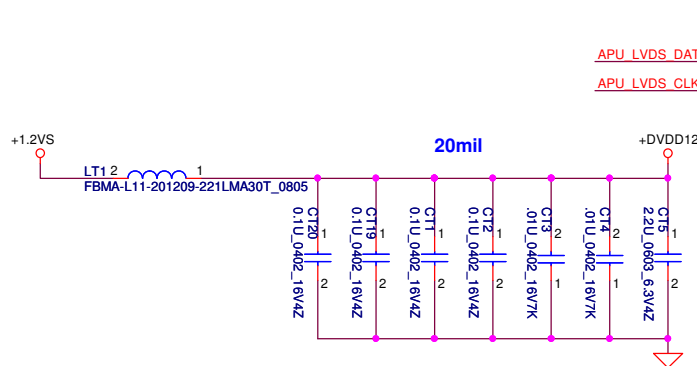


Change to 40.2ohm by AMD suggested

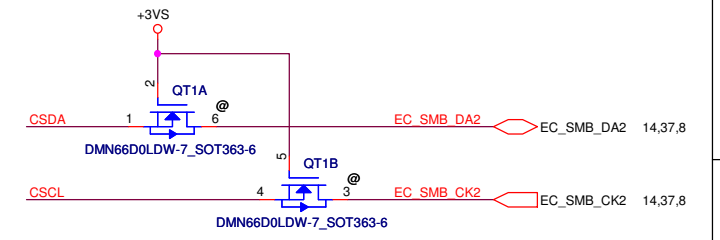
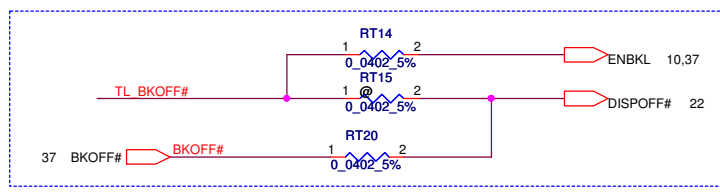




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Size	C	Document Number	QCL51 LA-8712P	Rev 0.1
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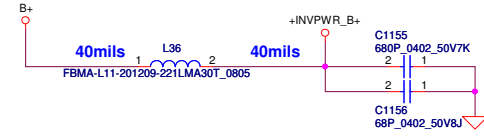
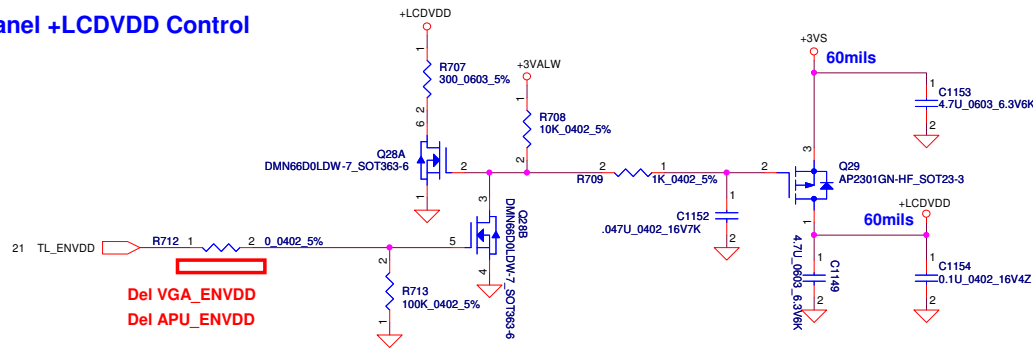


Place via on each trace bus and let resistor very close the via



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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Document Number		
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Panel +LCDVDD Control



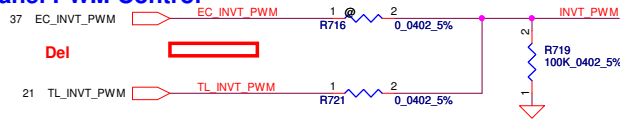
DISPOFF#	1	2	220P_0402_50V7K
INVT_PWM	1	2	220P_0402_50V7K

Panel Backlight Control

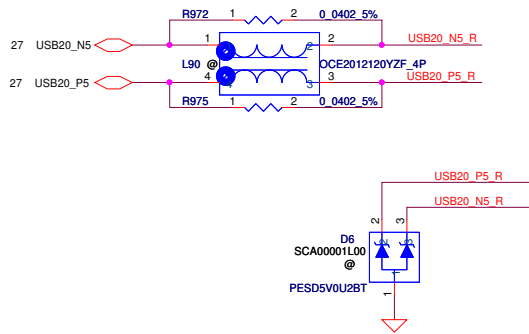
Modify and change to page 21



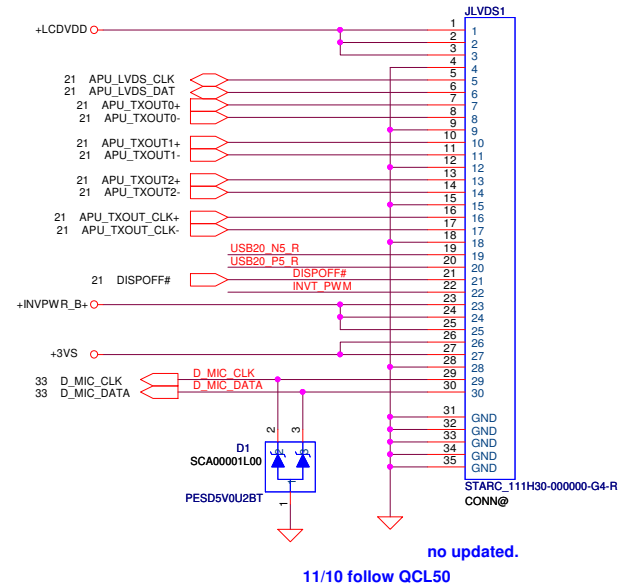
Panel PWM Control



<Translator LVDS Output>

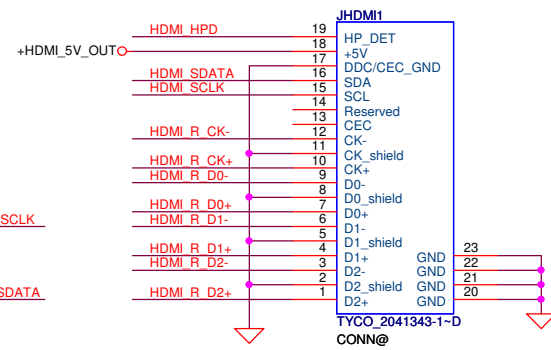
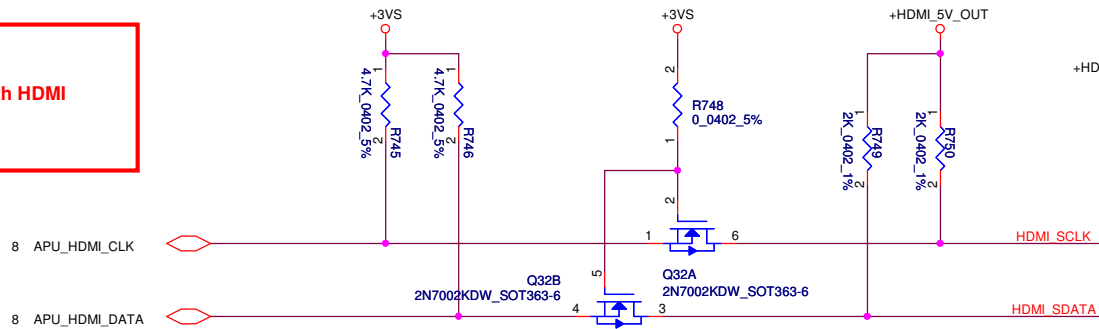


LVDS Connector



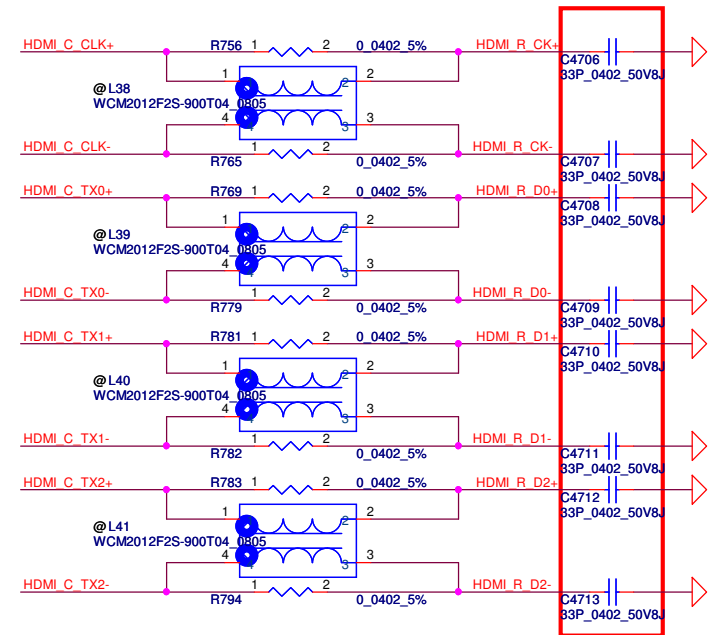
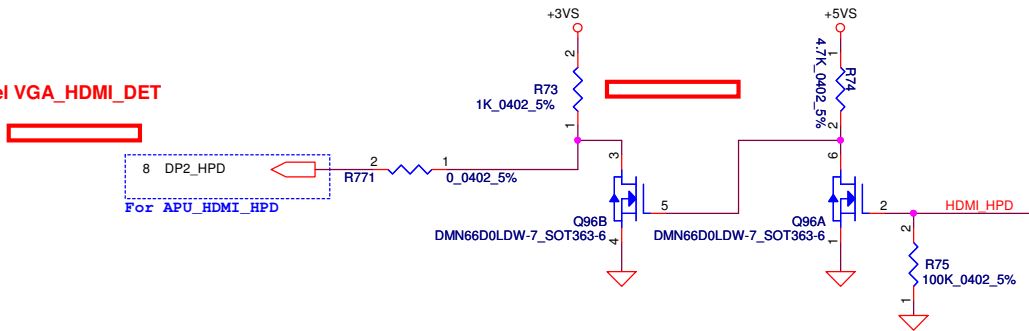
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title
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Size			Document Number	Rev
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Combine with HDMI



11/05 update footprint.

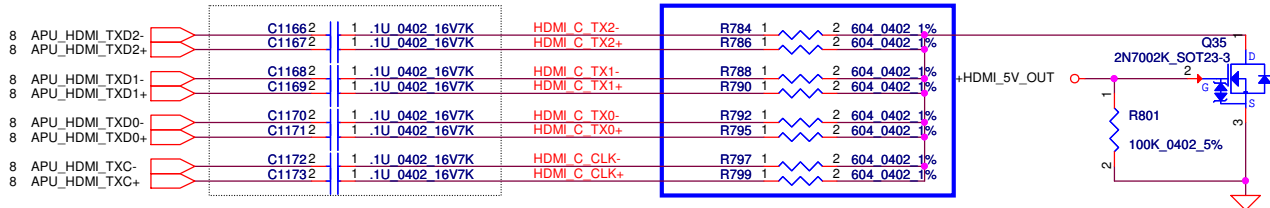
Del VGA_HDMI_DET



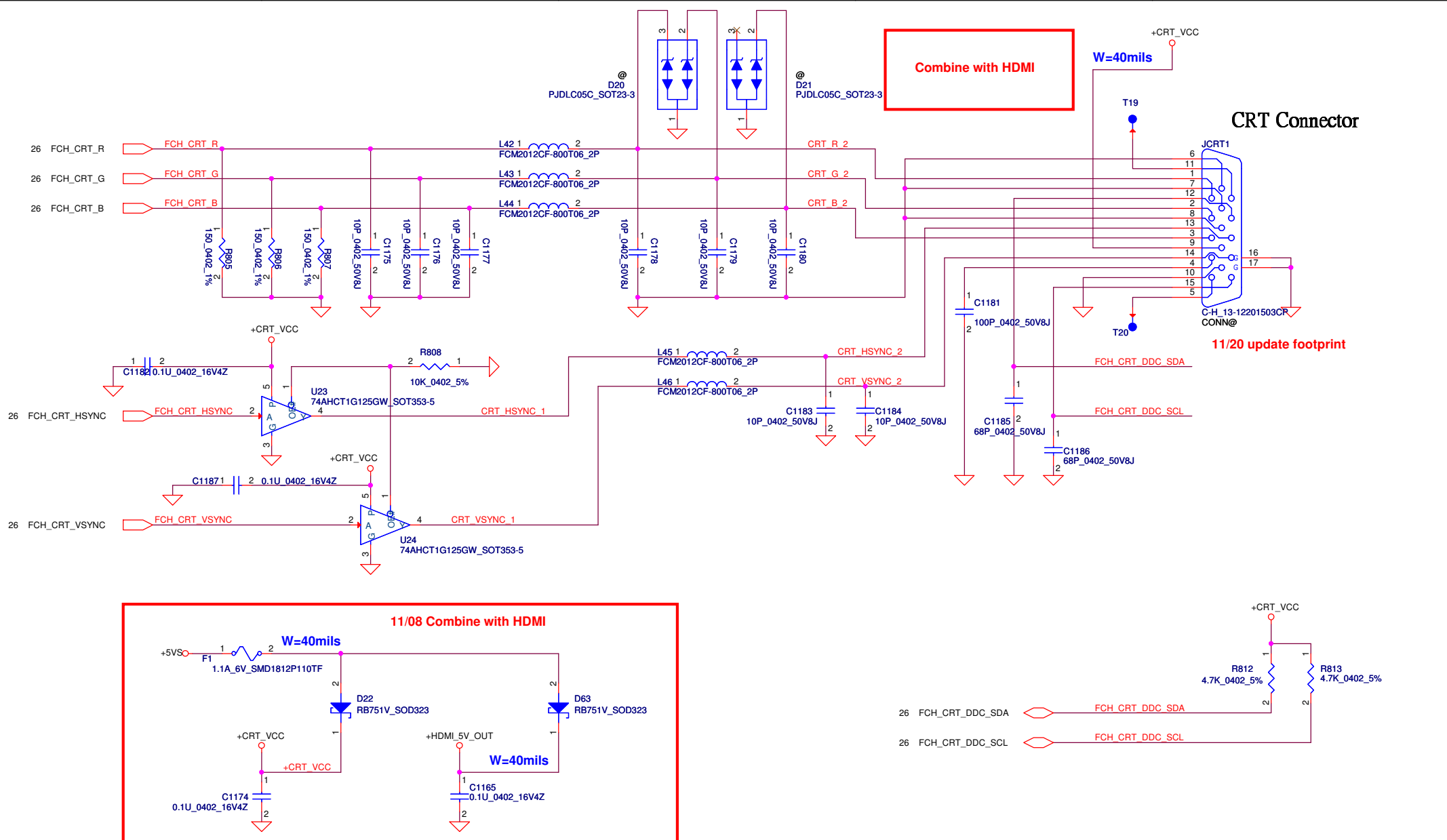
11/15 EMI
Near connector

Close to HDMI conn

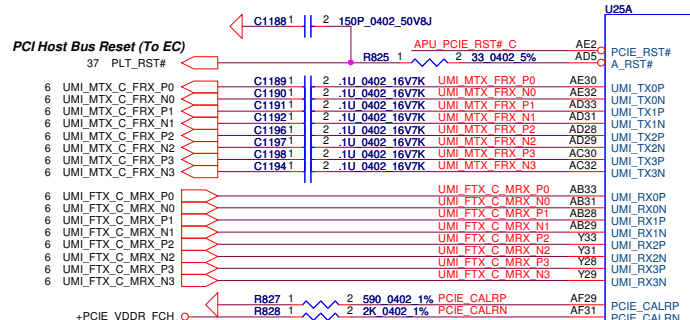
10/27 change to 604 ohm.



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				Document Number
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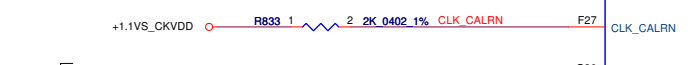


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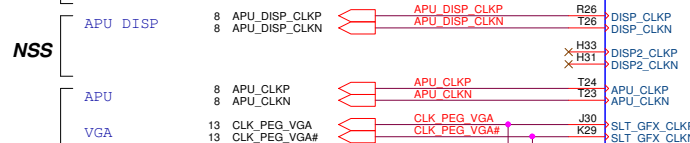


PCI_CALRP R=50ohm, 4mil,<1000mil
 PCI_CALRN R=50ohm, 4mil,<1000mi

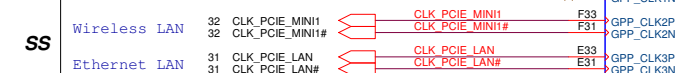
Del GPP PCI-E
 ABO connect to USB3.0 PHY.



For "EXT" CLK mode, input to PCIE,



11/15 RF

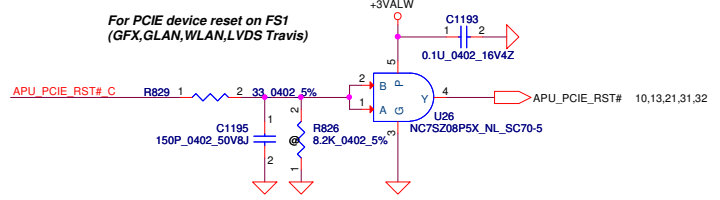
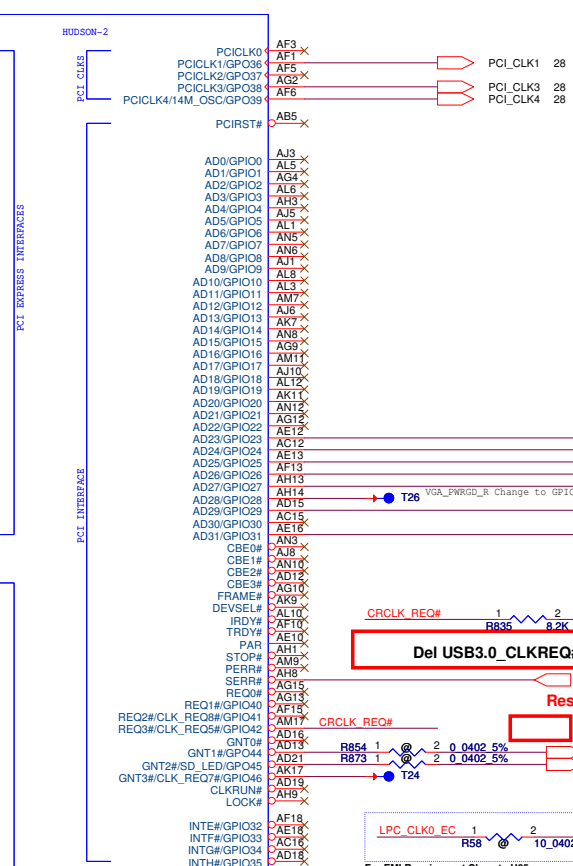


Del MI2, Card reader, USB 3.0 IC



C1205, C1206
 Change for G3
 RTC timing issue
 <improve amplitude>

32K_X1=50ohm, 4mil,<1500mil
 32K_X2=50ohm, 4mil,<1500mil



For PCIE device reset on FS1 (GFX, GLAN, WLAN, LVDS Travis)

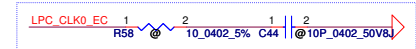


Del USB3.0_CLKREQ# PH.

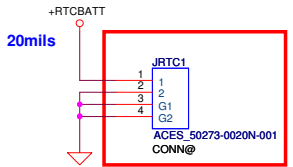
Reserved for card reader
 11/20 add



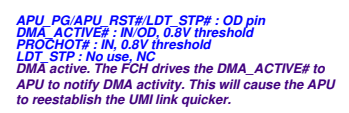
Update net name



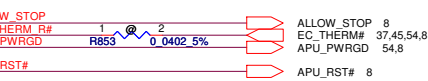
For EMI Requirement Close to U25



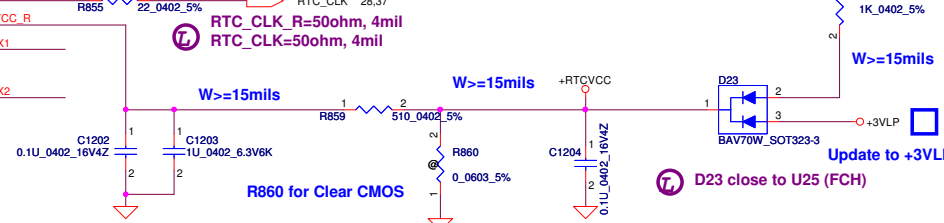
20mils
 11/19 update footprint



for ESD Cause FCH Side



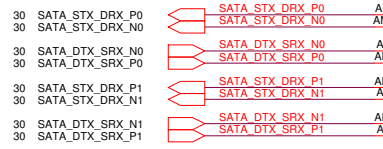
RTCC CLK R=50ohm, 4mil
 RTC_CLK=50ohm, 4mil



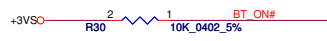
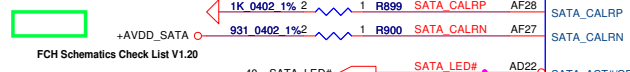
W>=15mils
 W>=15mils
 Update to +3VLP
 D23 close to U25 (FCH)

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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC	
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Document Number	QCL51 LA-8712P	Revision	Rev 0.1	Date: Monday, November 28, 2011	
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HDD1
ODD



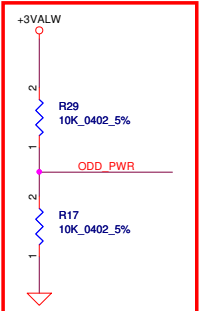
SATA_CALRP=35ohm,<1000mil
SATA_CALRN=35ohm,<1000mil



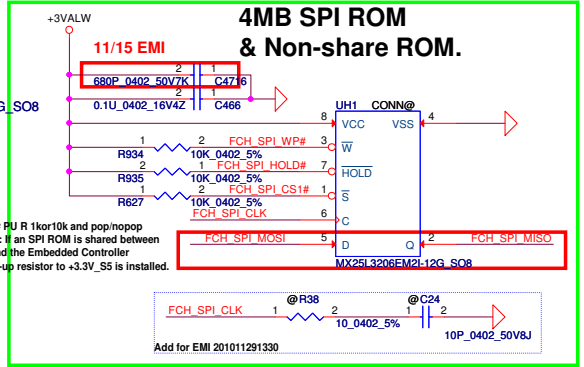
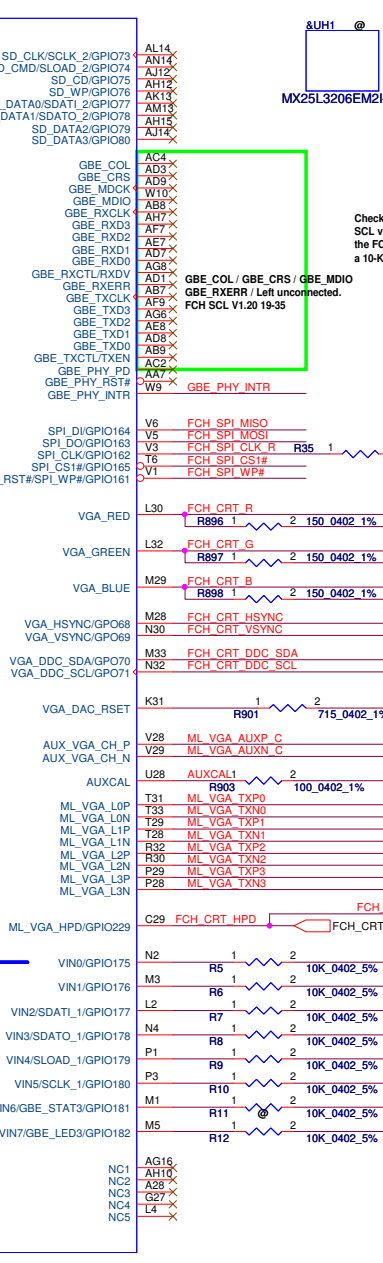
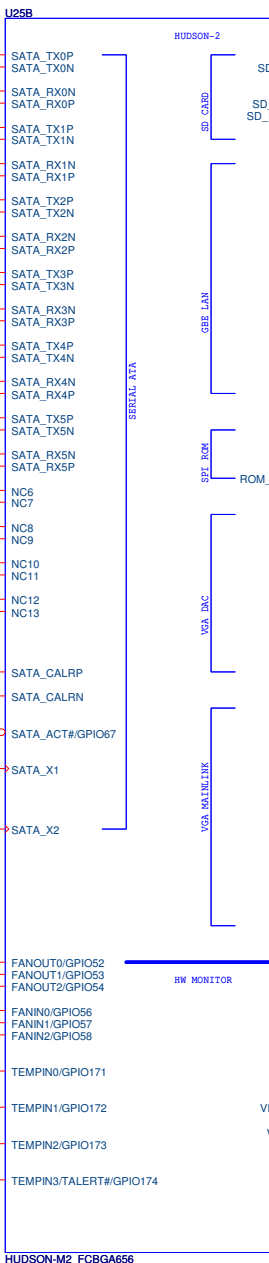
Del_WL_Off#_2



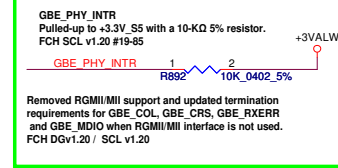
11/16 Follow Q5WV8
Del_W_DISABLE#_2



11/15 AMD check list for reserved.



Check CS# PU R 1k or 10k and pop/nopop
SCL v1.20: If an SPI ROM is shared between
the FCH and the Embedded Controller
a 10-K pull-up resistor to +3.3V_S5 is installed.



GBE_PHY_INTR
Pulled-up to +3.3V_S5 with a 10-K 5% resistor.
FCH SCL v1.20 #19-85

Removed RGMII/MII support and updated termination
requirements for GBE_COL, GBE_CRS, GBE_RXERR
and GBE_MDIO when RGMII/MII interface is not used.
FCH DGV1.20 / SCL v1.20

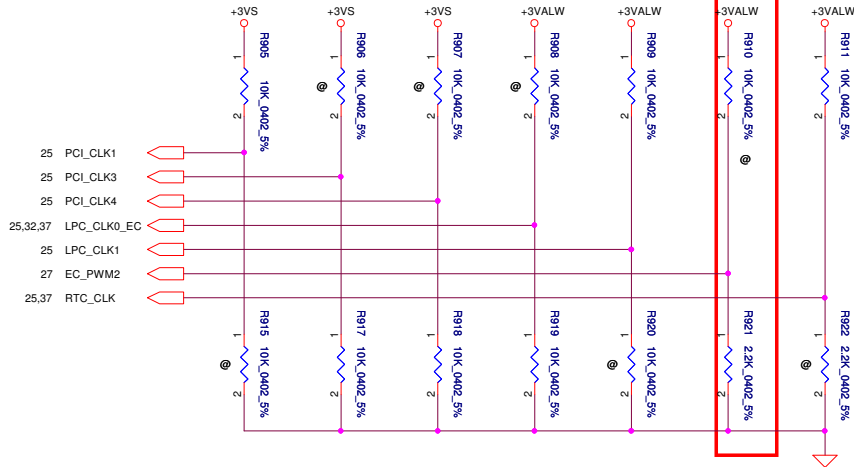
AUXCAL <1000mil

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File Name	Document Number	Revision	Date	Sheet	of
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STRAP PINS

Change to SPI

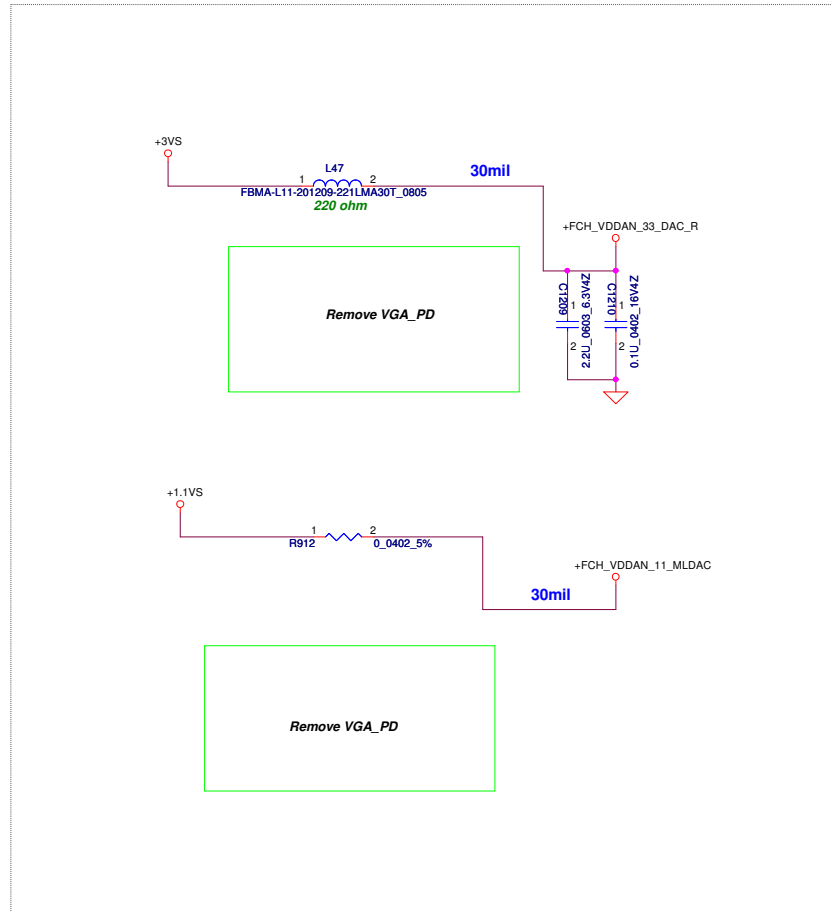
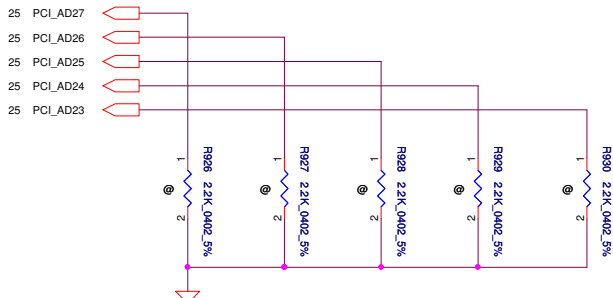
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCI GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCI GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED



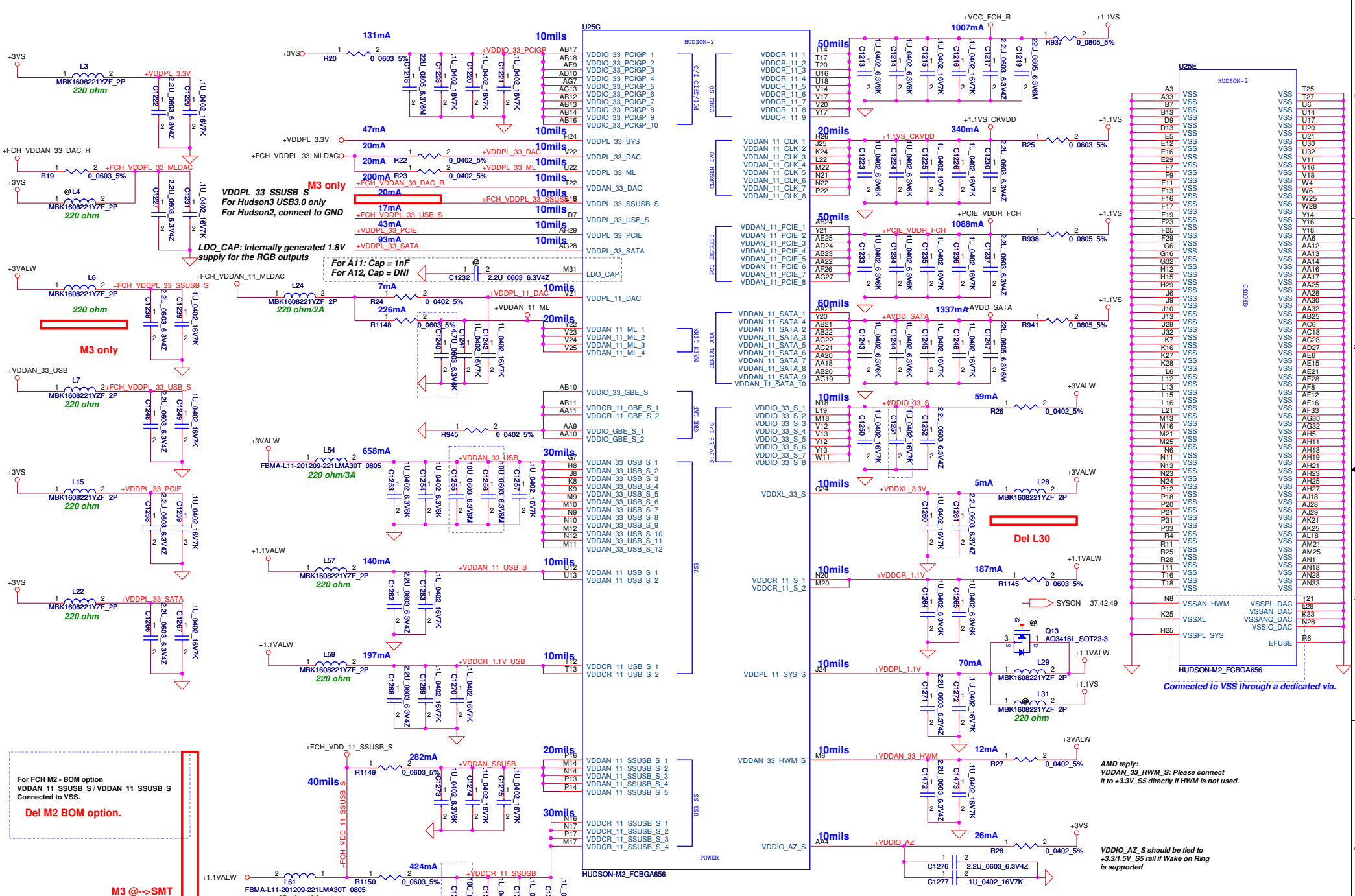
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
No external R	USE PCI PLL DEFAULT	Normal REFCLK termination DEFAULT	USE DEFAULT PCI STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	Inverted REFCLK termination	USE EEPROM PCI STRAPS	ENABLE PCI MEM BOOT



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For FCH M2 - BOM option
VDDAN_11_SSUSB_S / VDDAN_11_SSUSB_S
Connected to VSS.

Del M2 BOM option.

M3 only @->SMT

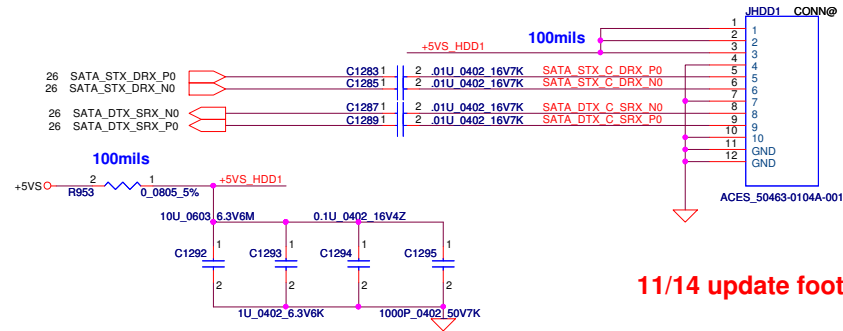
AMD reply:
VDDAN_33_HWM_S: Please connect
it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to
+3.3/1.5V_S5 rail if Wake on Ring
is supported

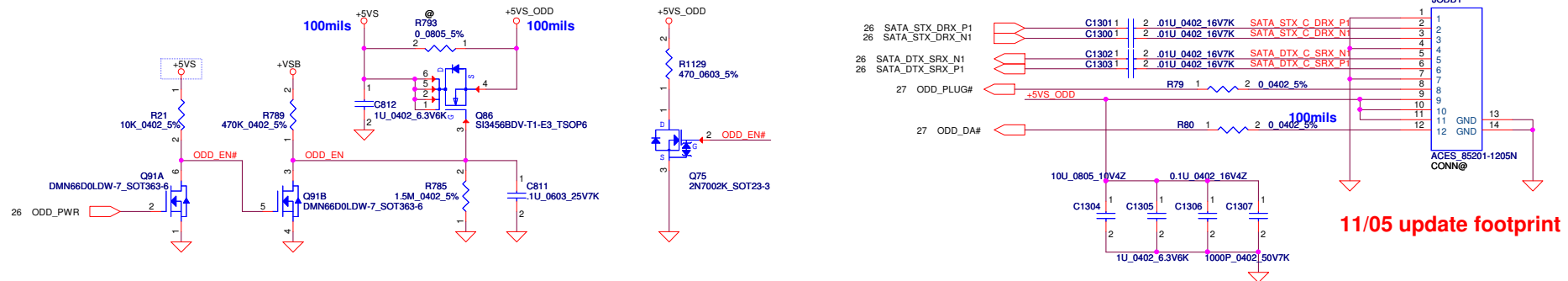
Connected to VSS through a dedicated via.

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Date	Monday, November 28, 2011		Sheet	29 of 56		

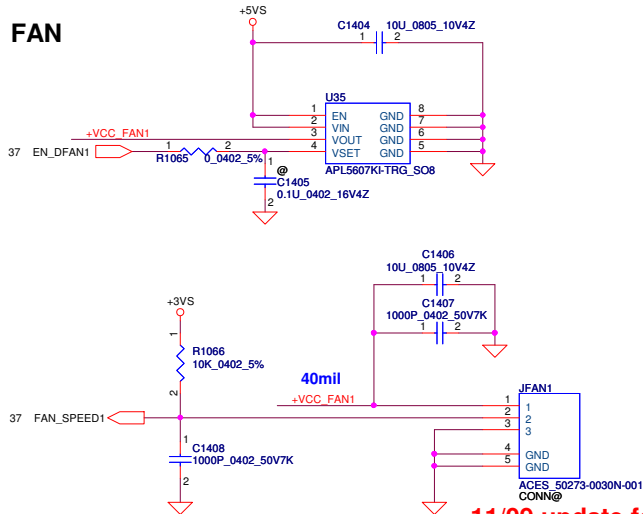
SATA HDD1 Conn.



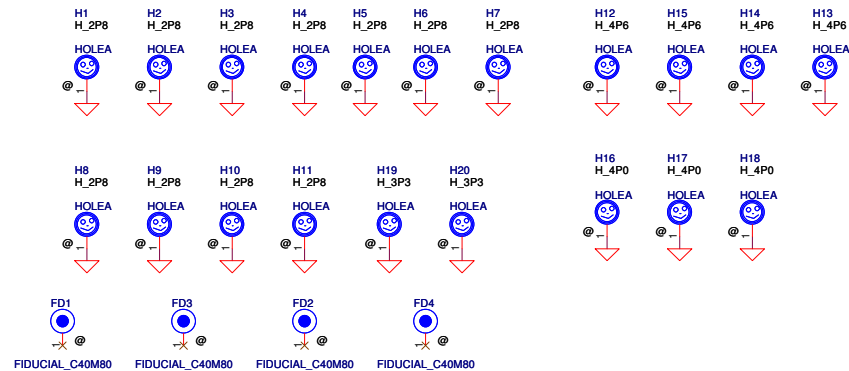
ODD conn



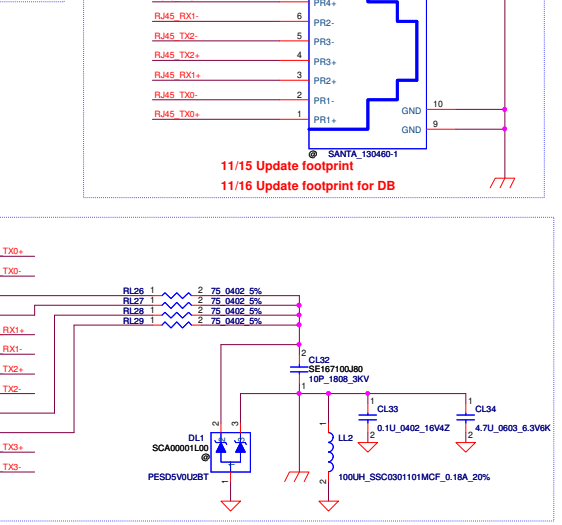
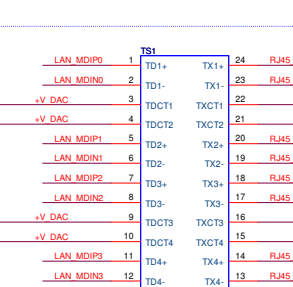
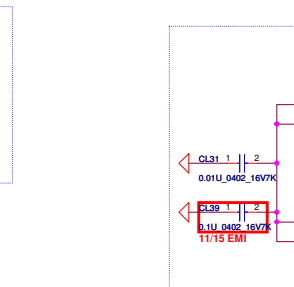
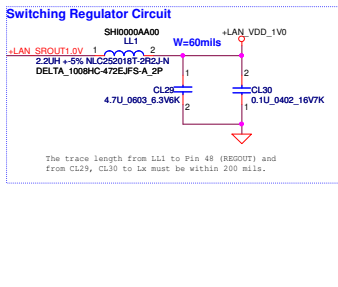
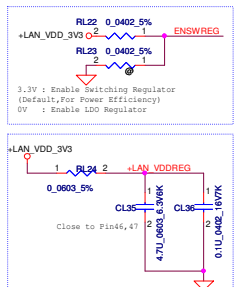
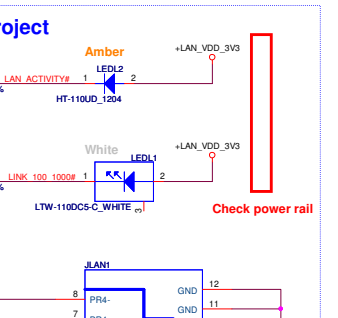
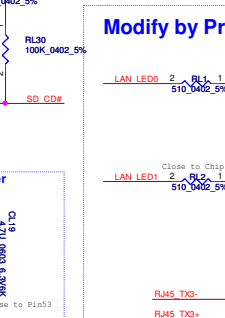
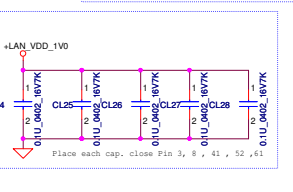
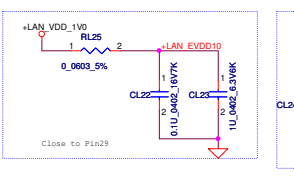
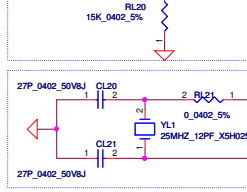
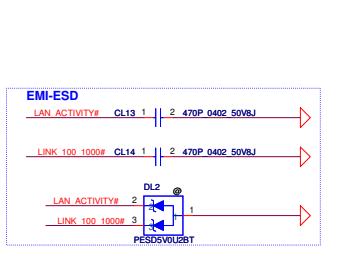
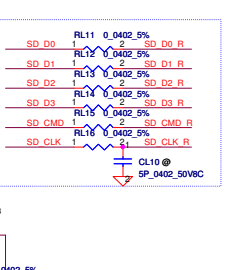
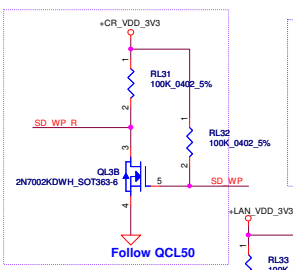
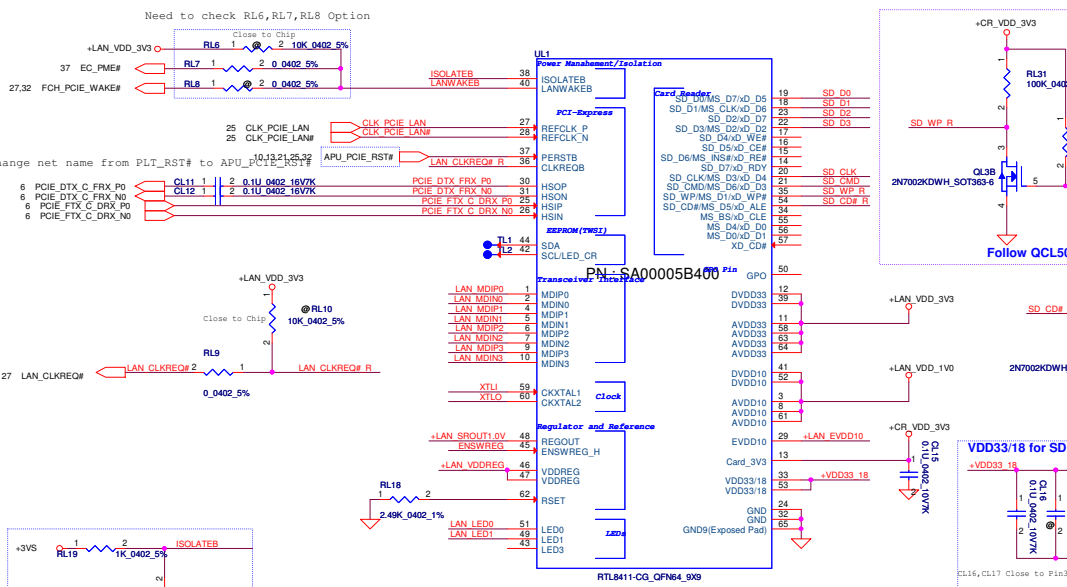
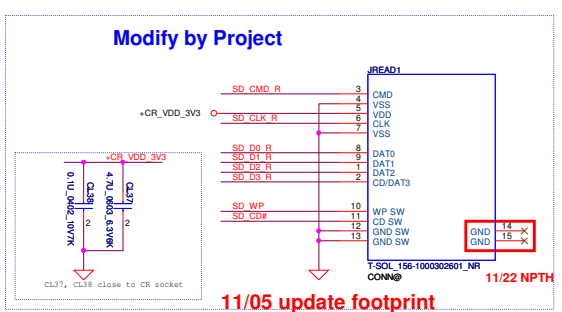
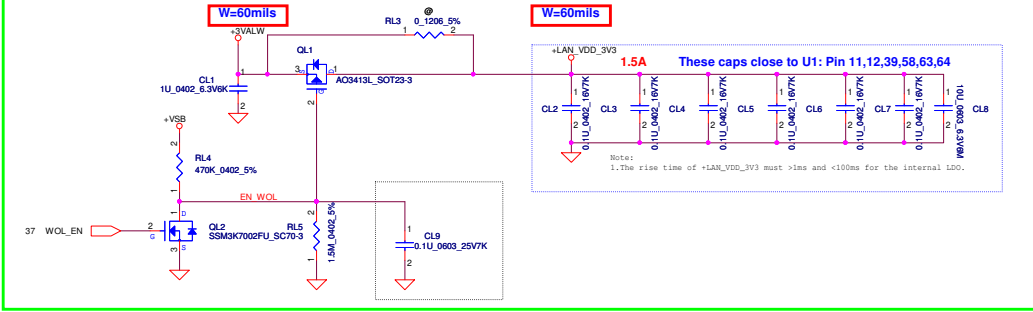
FAN



Screw Hole



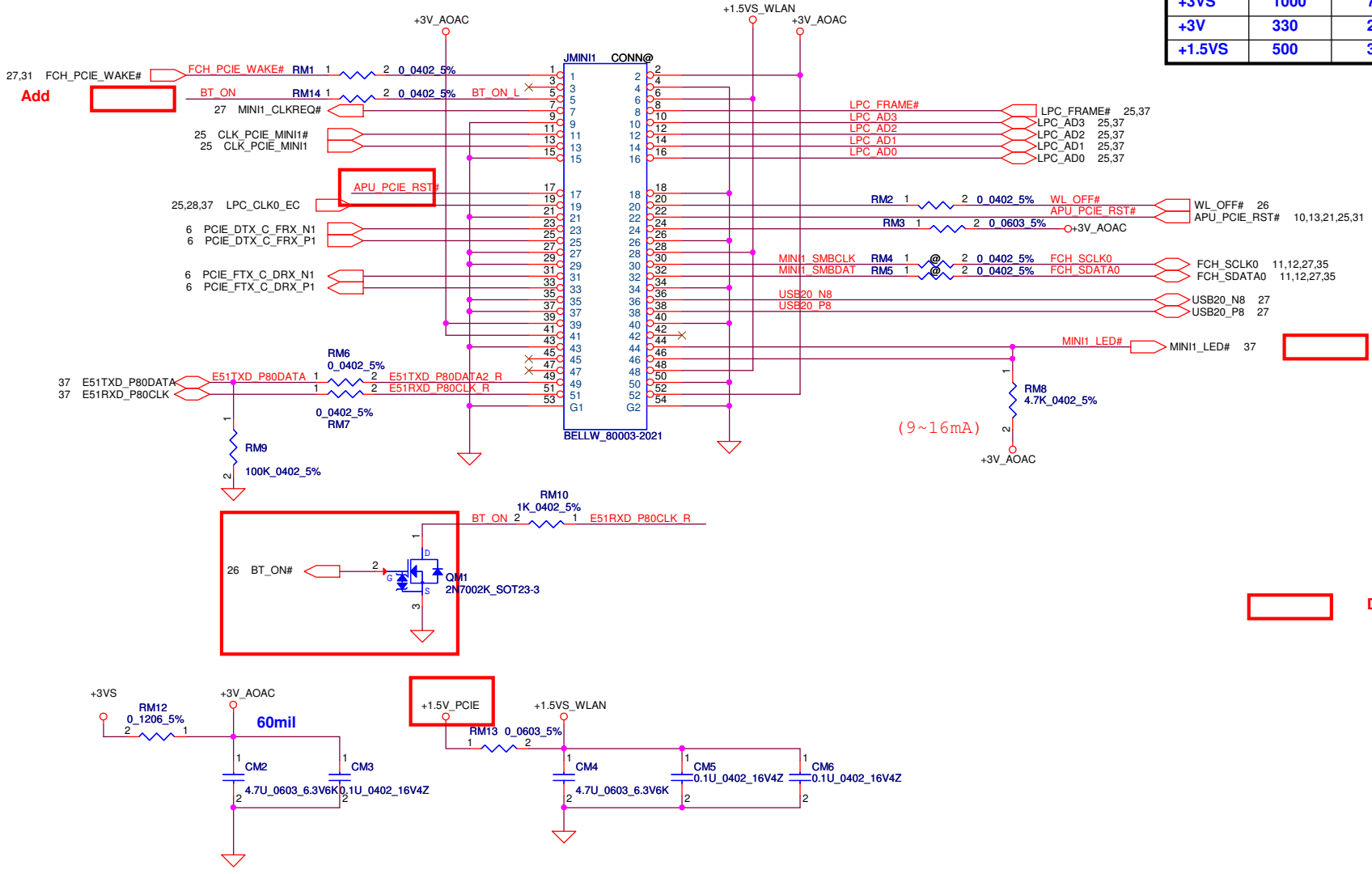
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title
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<p>Compal Electronics, Inc.</p> <p>LAN&CardReader Realtek RTL8411</p>			<p>Document Number</p> <p>QCL51 LA-8712P</p> <p>Date: Monday, November 28, 2011 Sheet: 31 of 56</p>	

WLAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

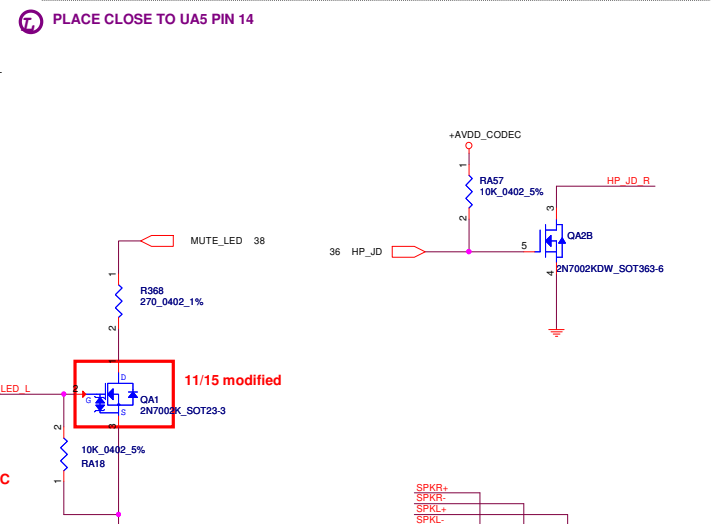
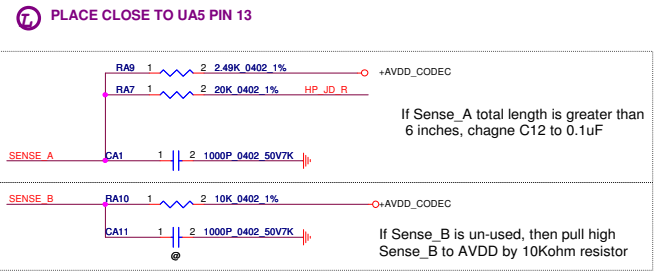
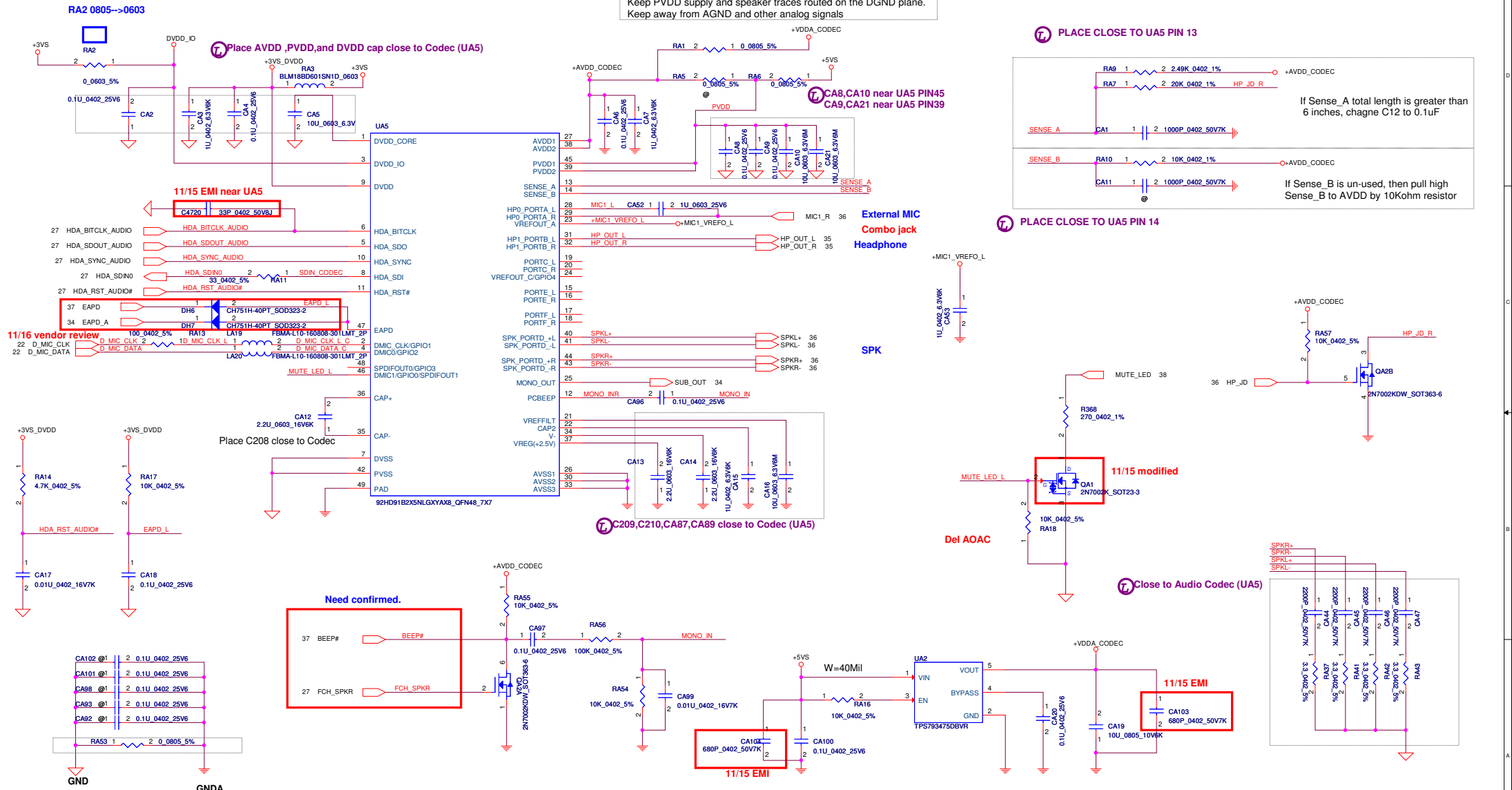


Control by EC

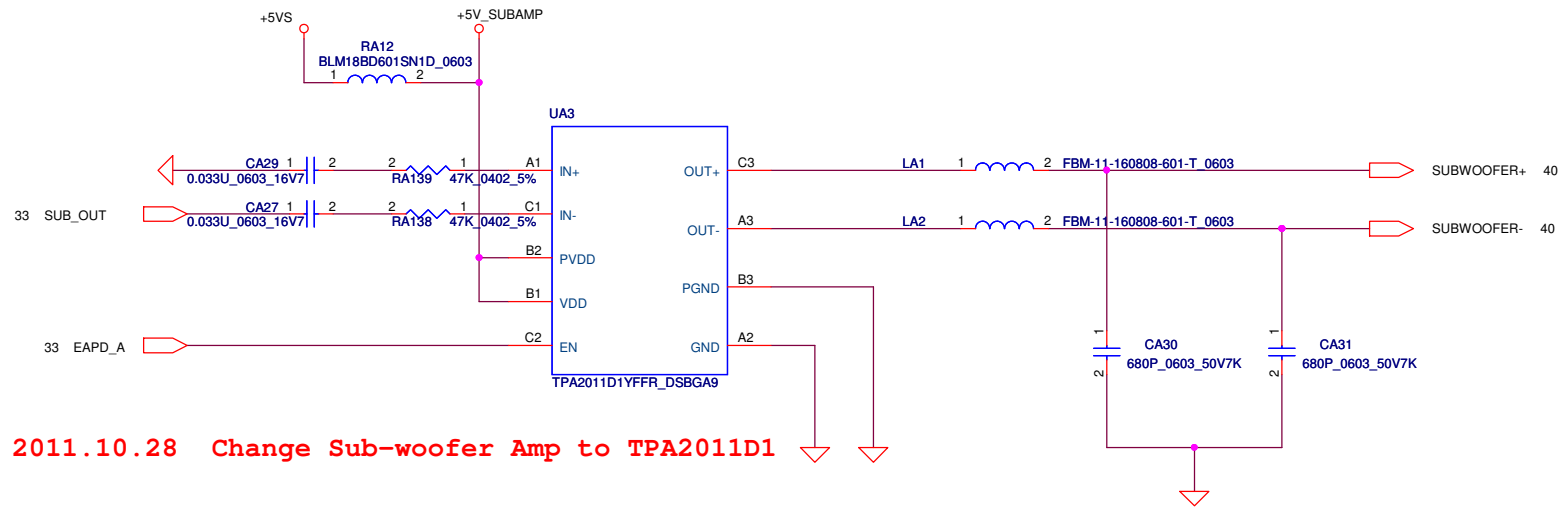
Del AOAC

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Notes:
 Keep PVDD supply and speaker traces routed on the DGND plane.
 Keep away from AGND and other analog signals



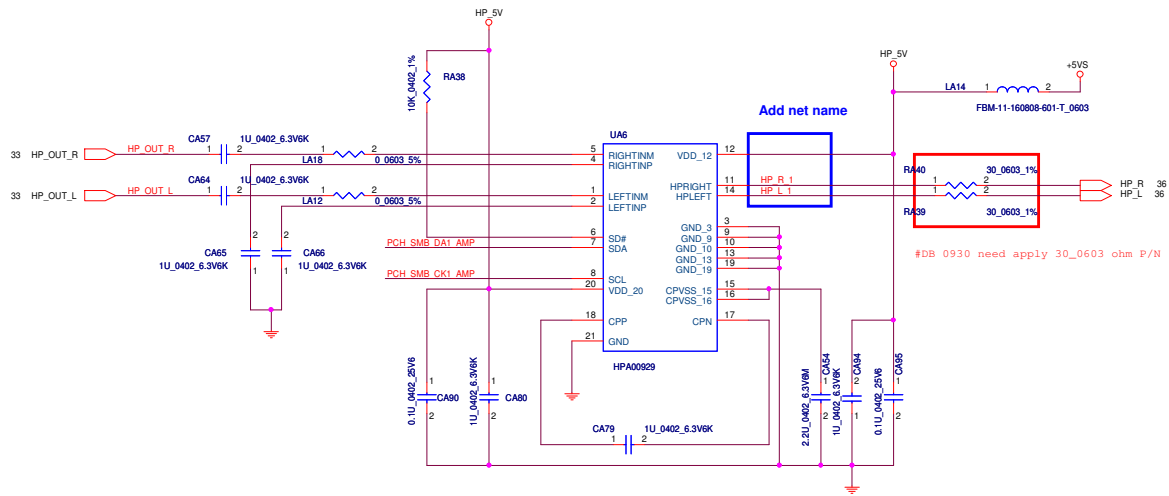
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Date:	Monday, November 28, 2011				



2011.10.28 Change Sub-woofer Amp to TPA2011D1

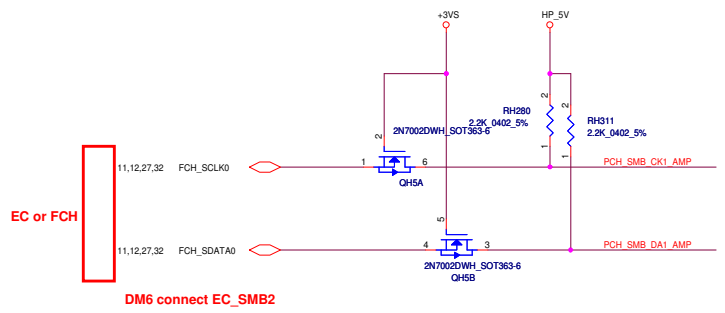
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Headphone amplifier



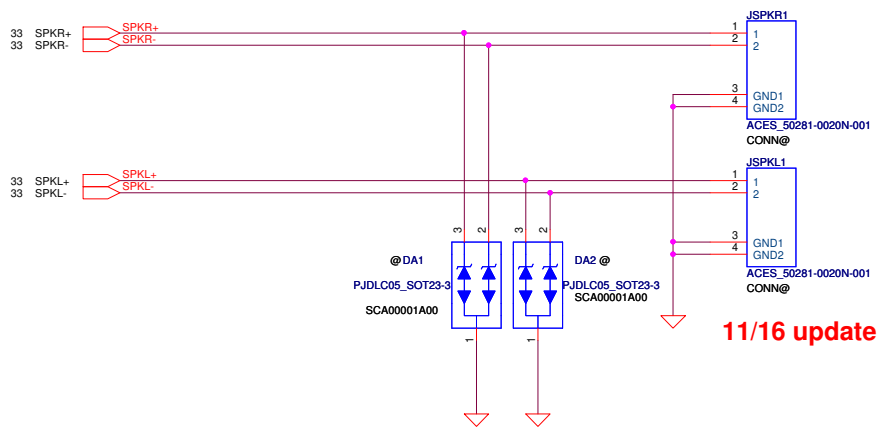
Add net name

#DB 0930 need apply 30_0603 ohm P/N

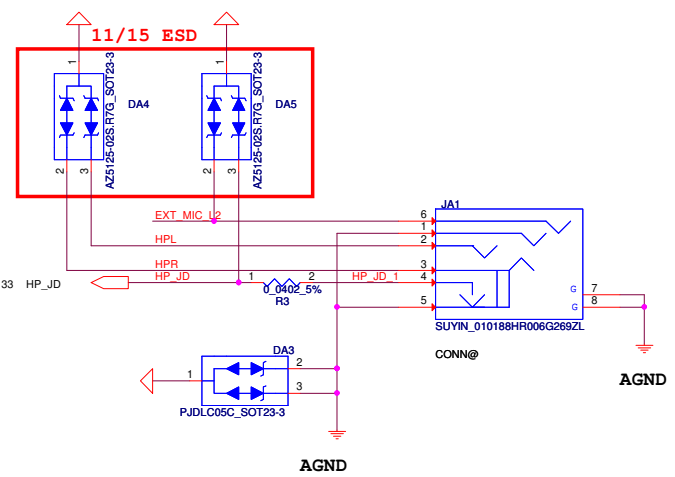
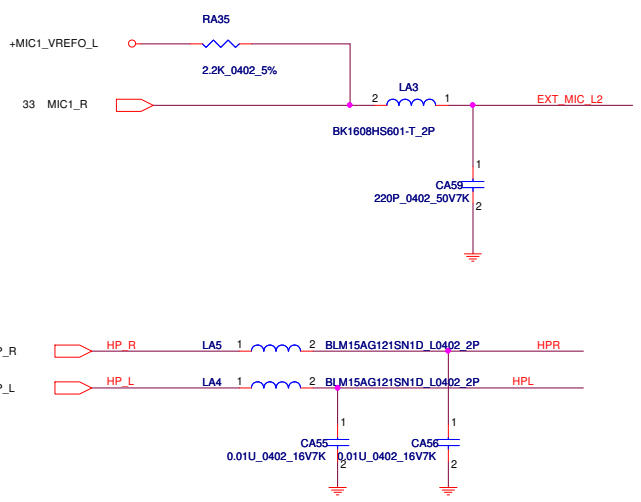


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title
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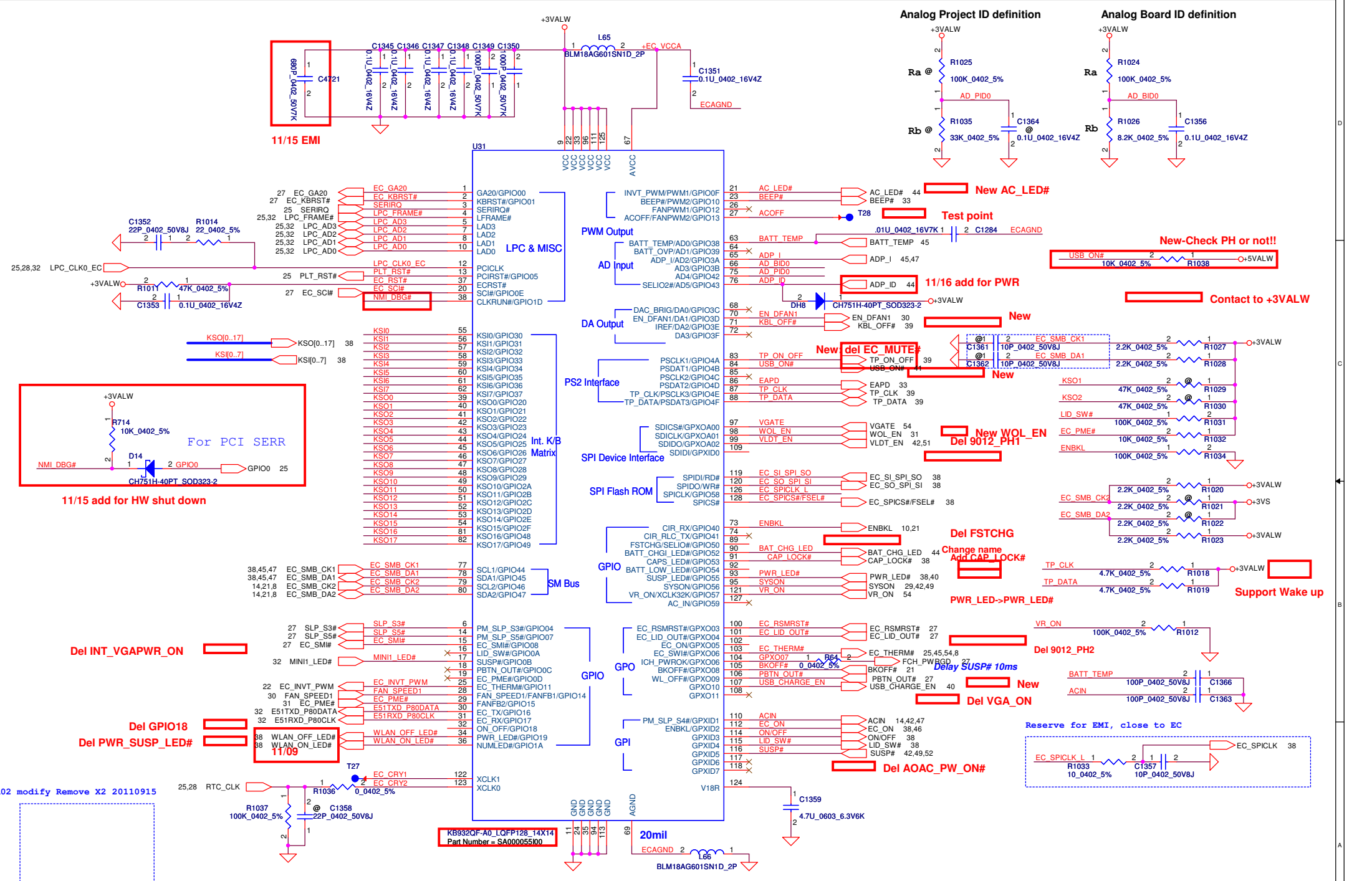
SPK conn



11/16 update footprint



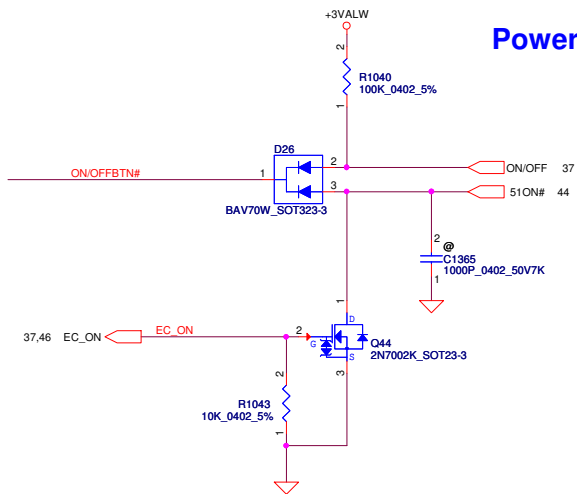
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/04/07	Deciphered Date	2012/10/21	Title	Audio SPK Conn/Jack/MIC
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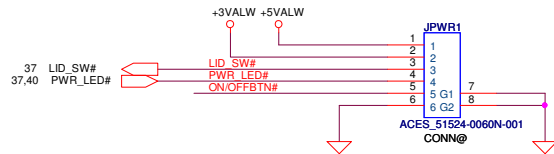
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Title EC ENE KB930/9012			
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Power Button

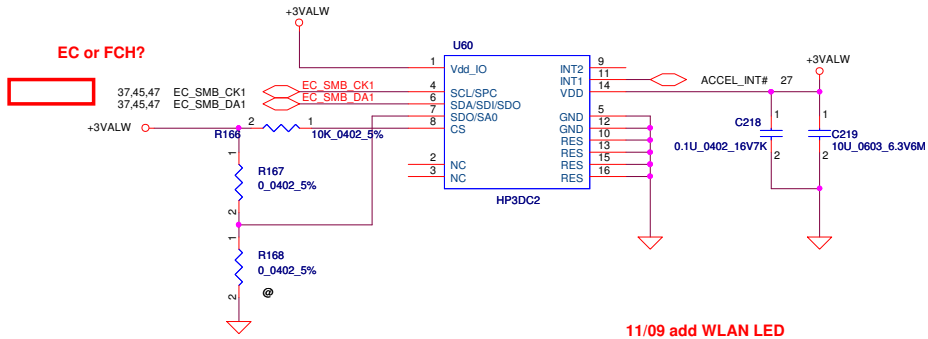


POWER/B

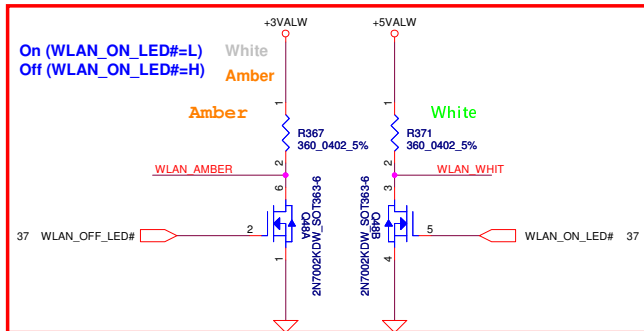


11/05 update footprint

ACCELEROMETER

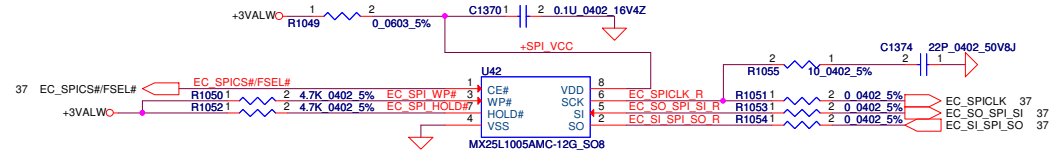


11/09 add WLAN LED

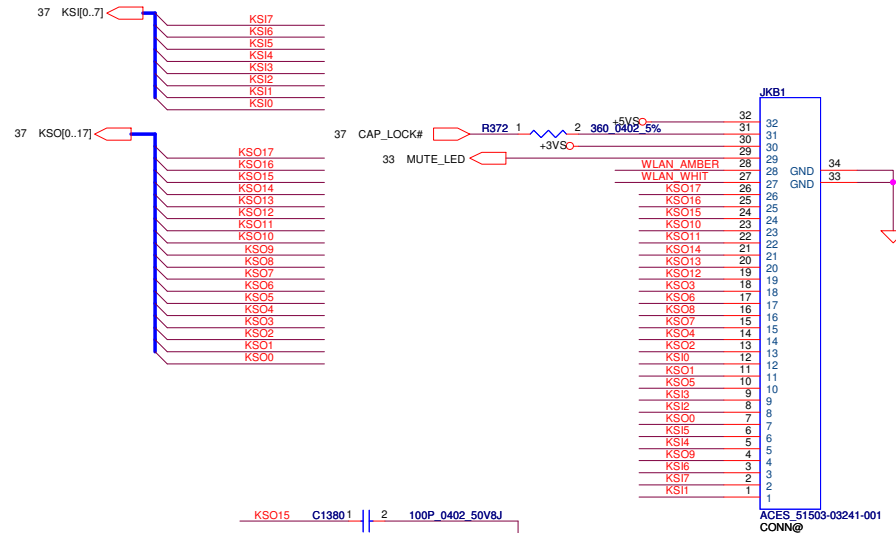


On (WLAN_ON_LED#=L) White
Off (WLAN_ON_LED#=H) Amber

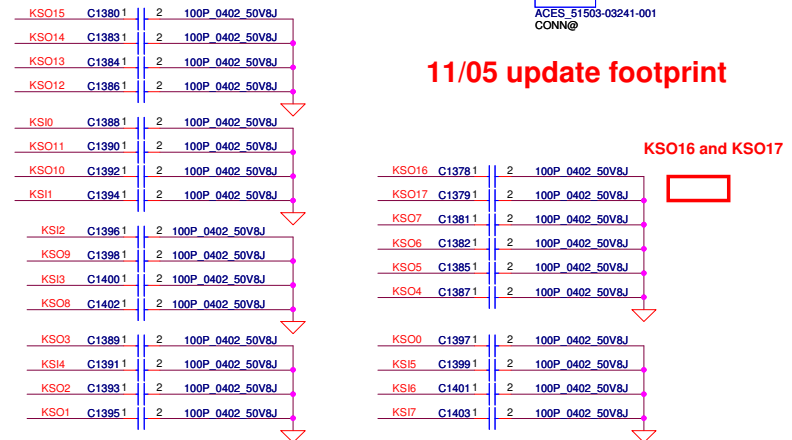
EC BIOS ROM



KB conn

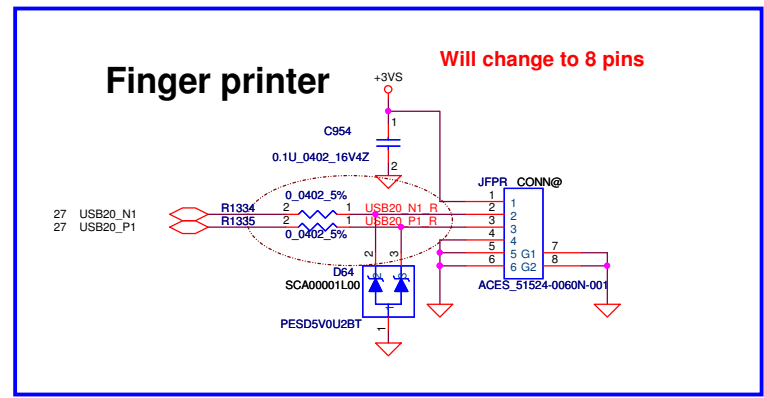
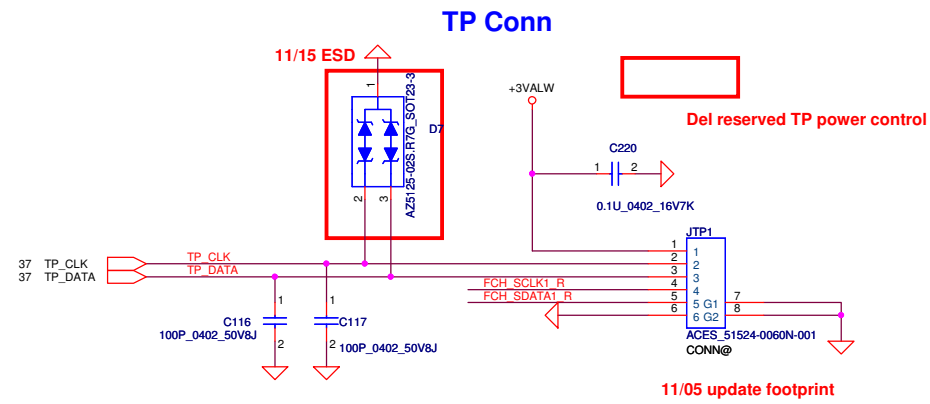


11/05 update footprint



KSO16 and KSO17

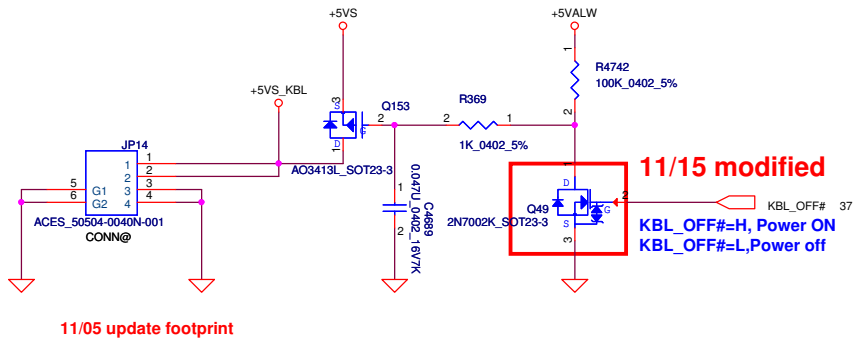
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WLAN ON/OFF LED

11/09 Change to KB connector

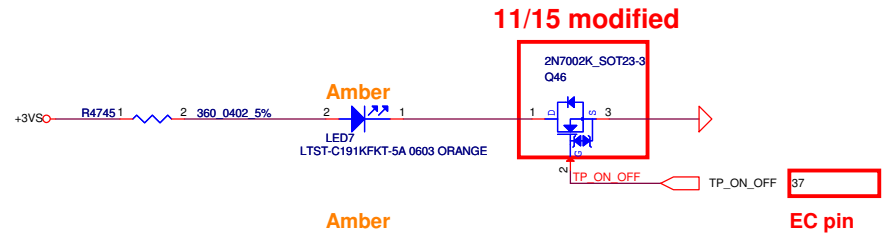
Keyboard backlight Conn



AOAC power control

Del AOAC

T/P On/Off LED



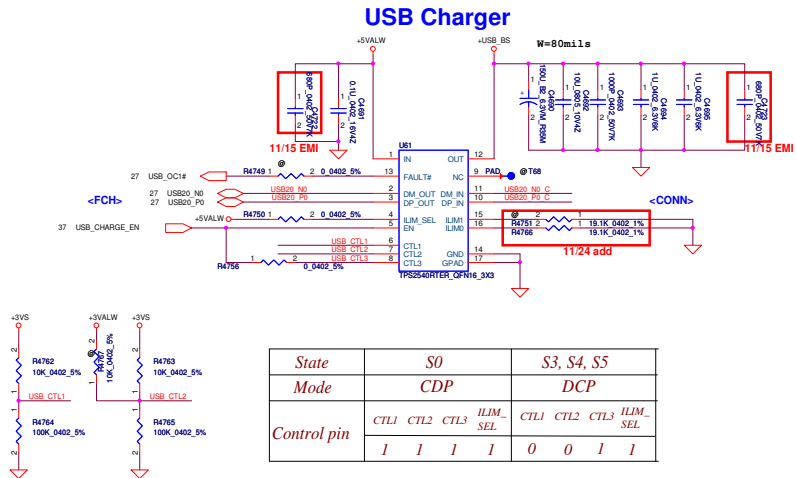
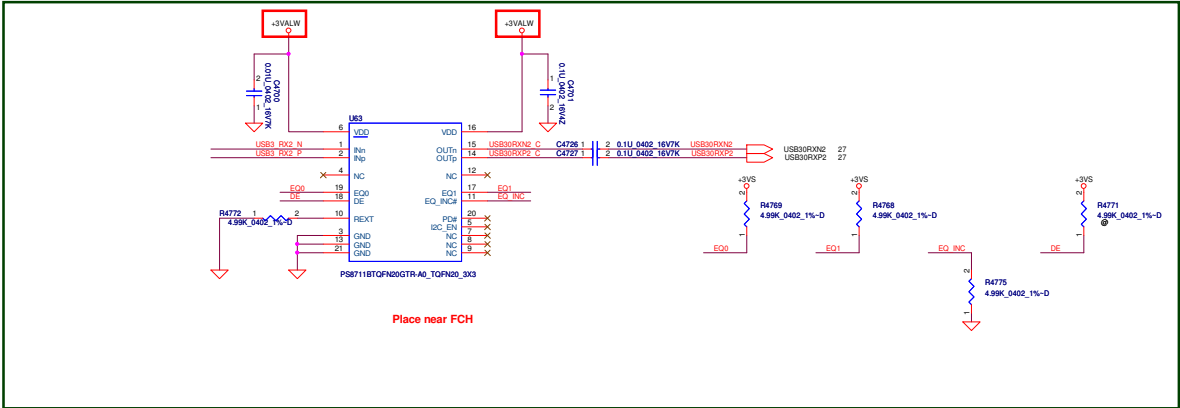
Mute On/Off LED

11/09 Change to KB connector

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				LAN Magnetic & RJ45
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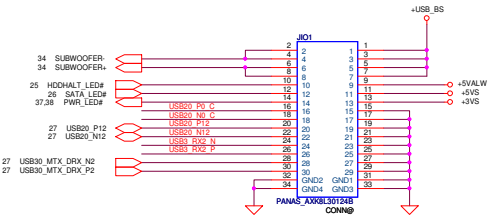
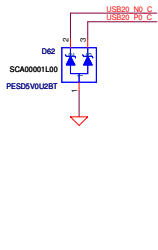
11/24 move to sub board

USB3.0 Repeater

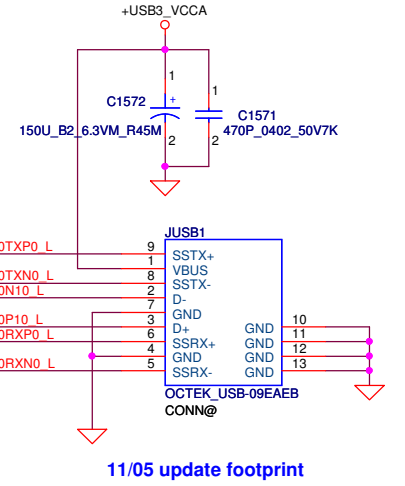
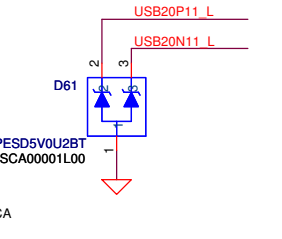
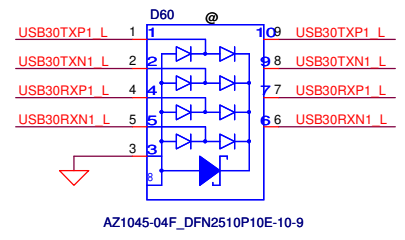
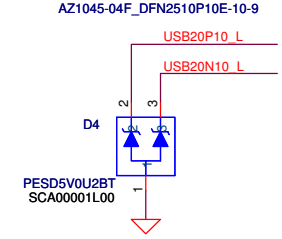
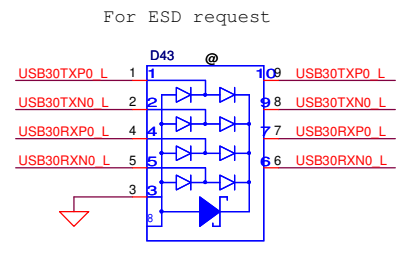
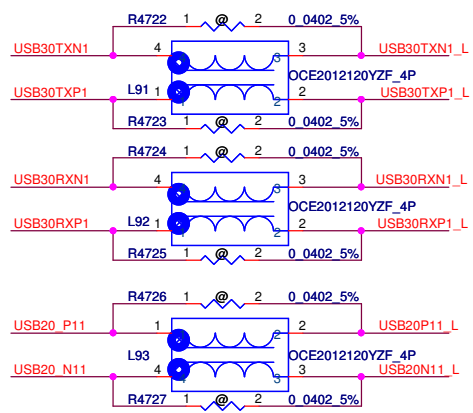
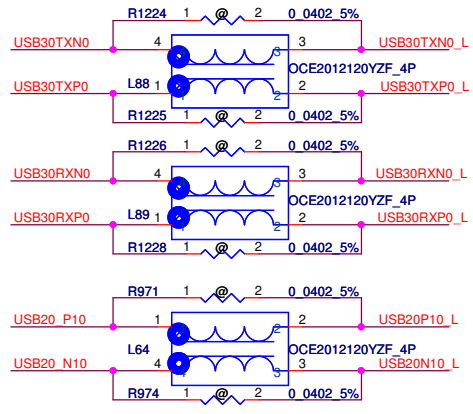
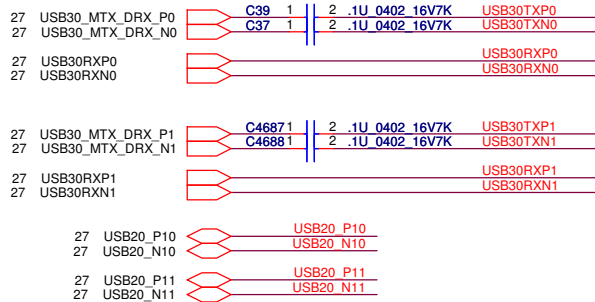


State	S0				S3, S4, S5			
Mode	CDP				DCP			
Control pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	1	1	0	0	1	1

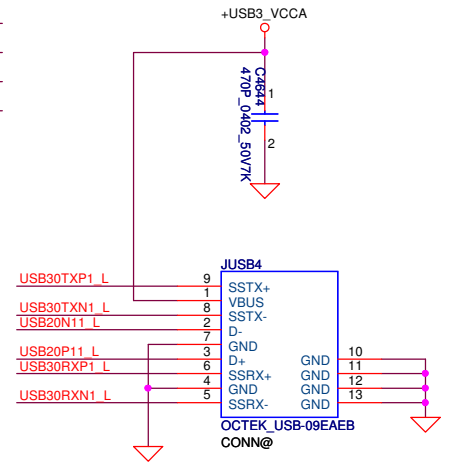
11/10 del check



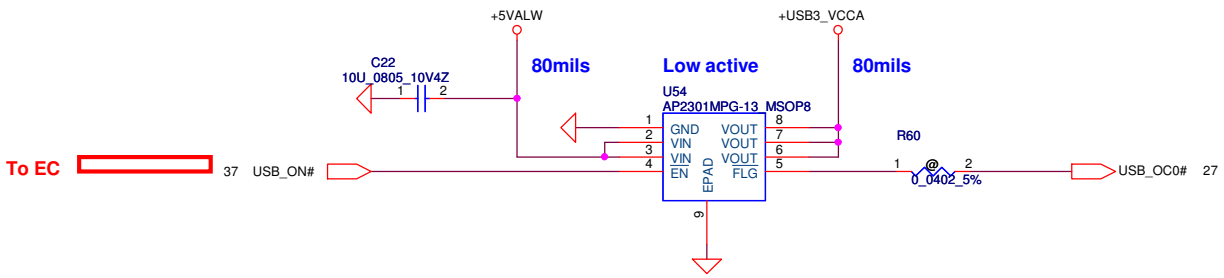
11/16 update footprint
11/24 change pin definition



11/05 update footprint

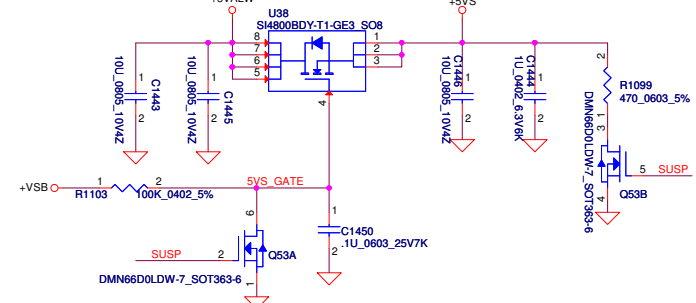


11/05 update footprint

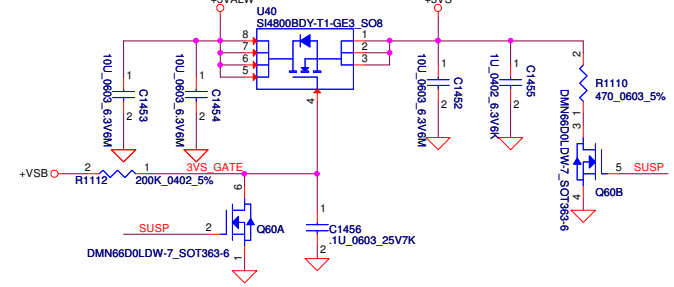


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+5VALW TO +5VS (5A)

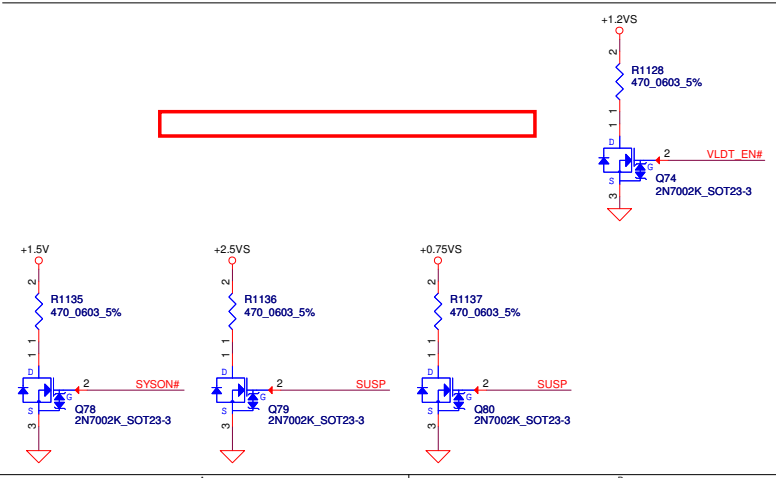


+3VALW TO +3VS (3.3A)

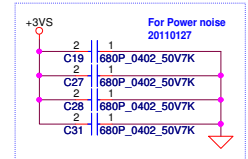
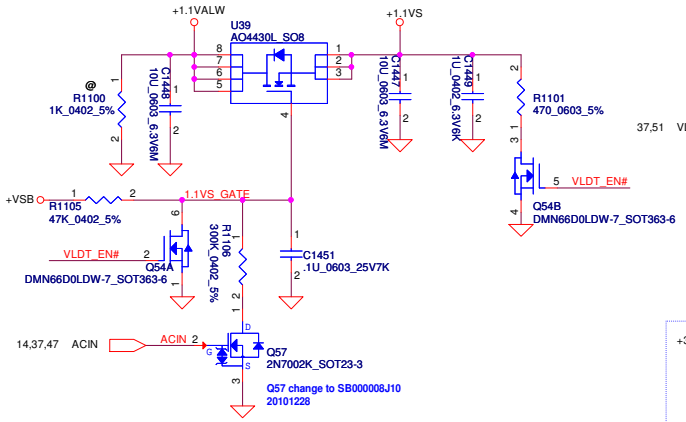


+1.5V TO +1.5VS (1.5A)

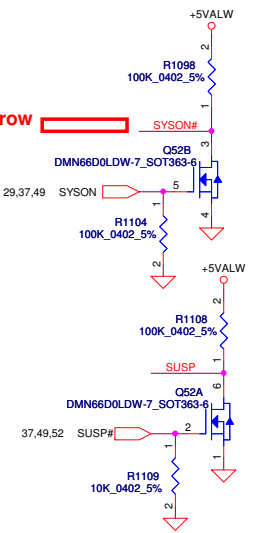
Del +1.5V to +1.5VS



+1.1VALW TO +1.1VS (1.1A)



Del arrow



VGA Power +1.5V to +1.5VSG (1.5A)

Del +1.5VSG and reserved on GPU

Del +3VSG and reserved on GPU

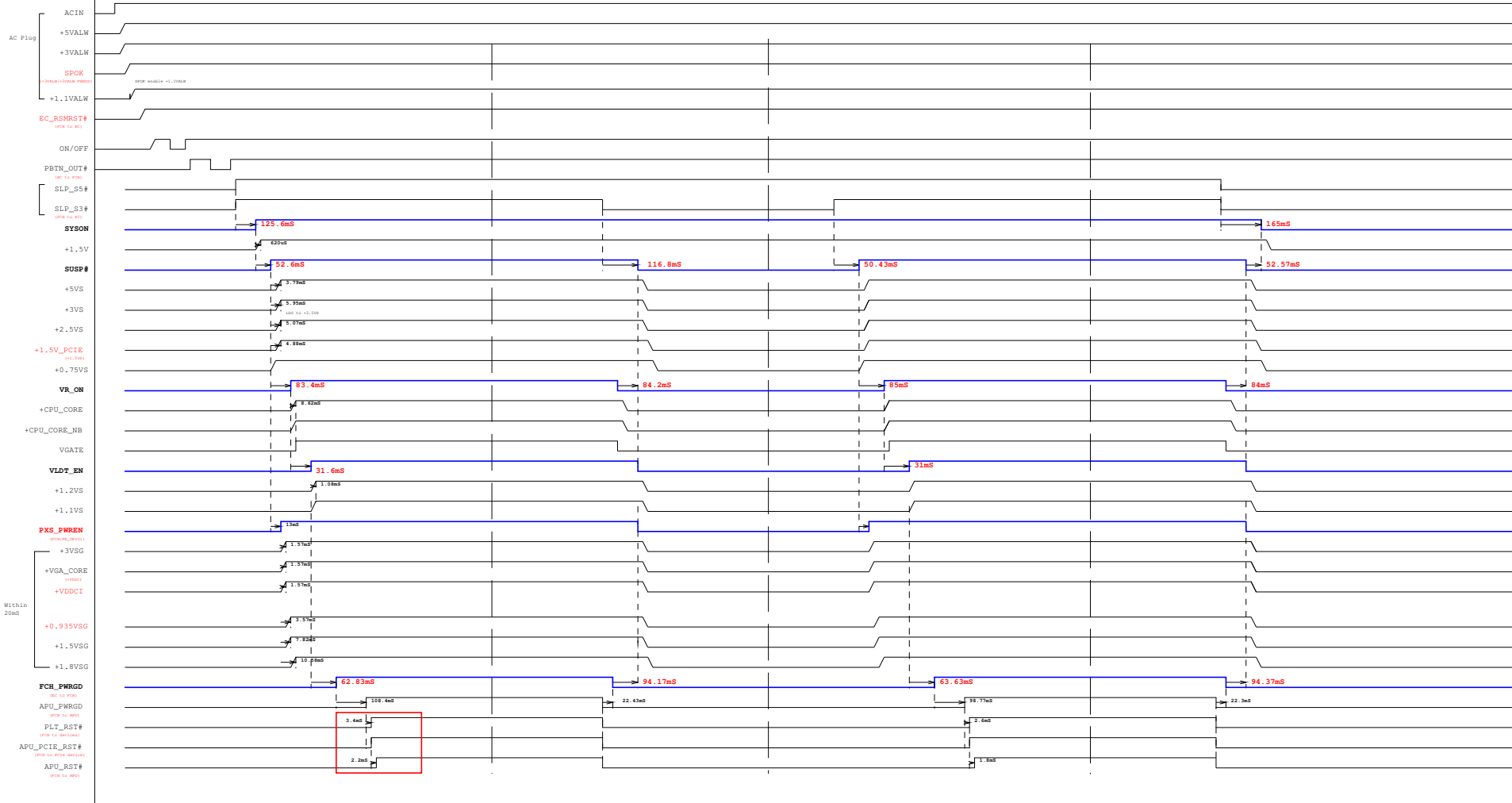
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	DC Interface	
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Boot

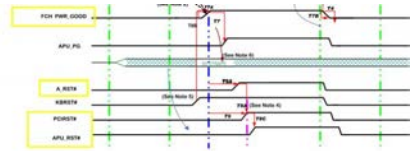
Enter S3

S3 Resume

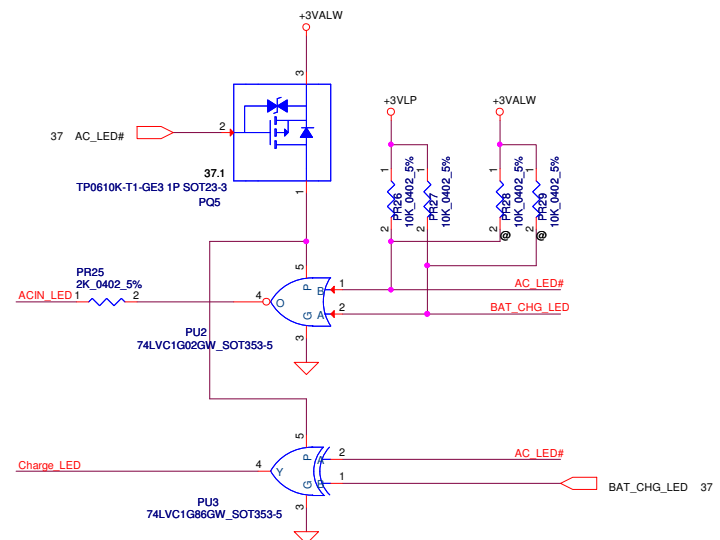
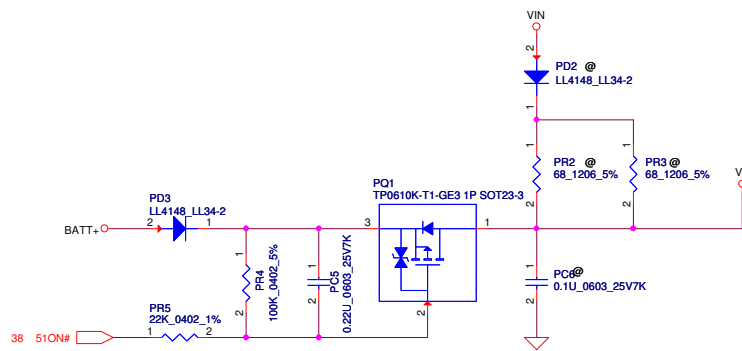
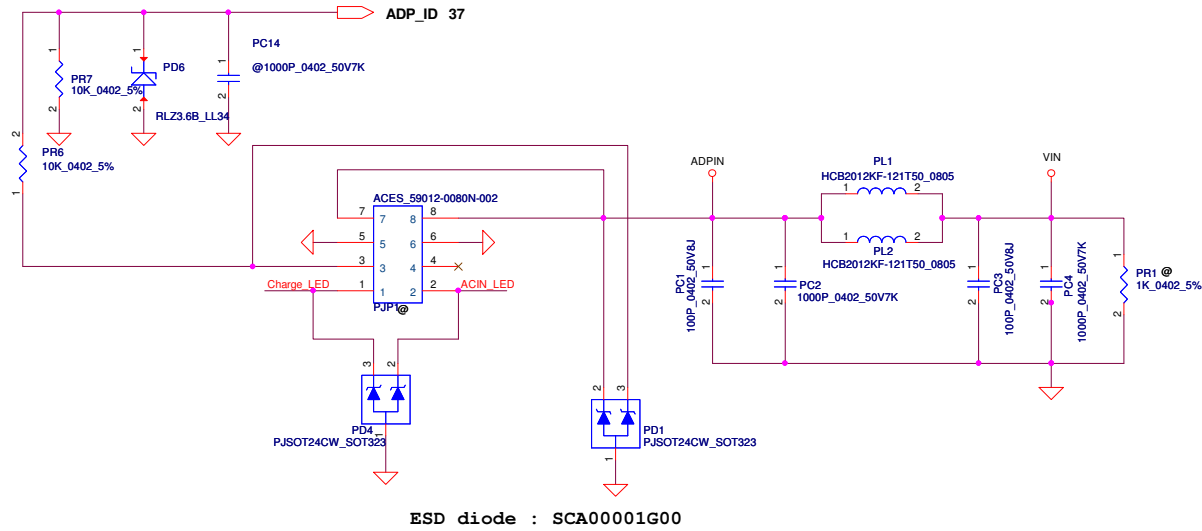
Shut Down



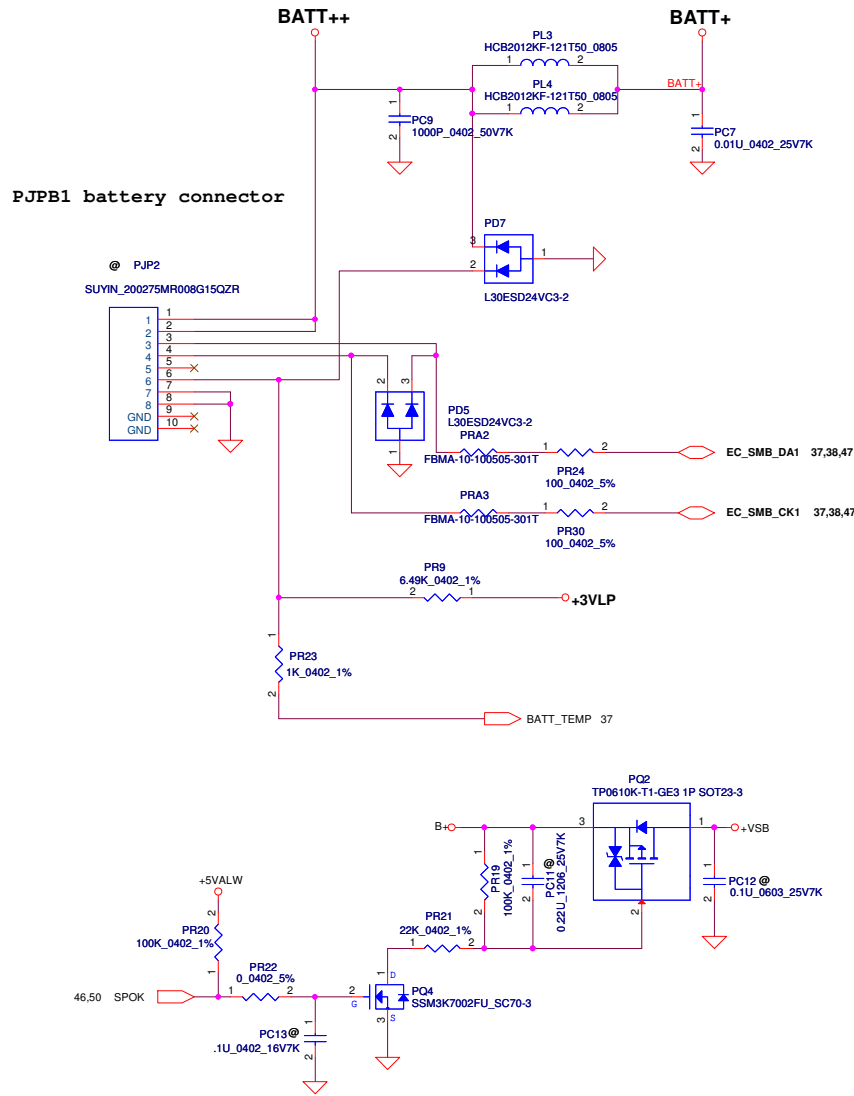
Within 20mS



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Doc#	OC151 LA-8712P	Rev	1.0	61
Rev	Multiple Revisions	Rev	4	2



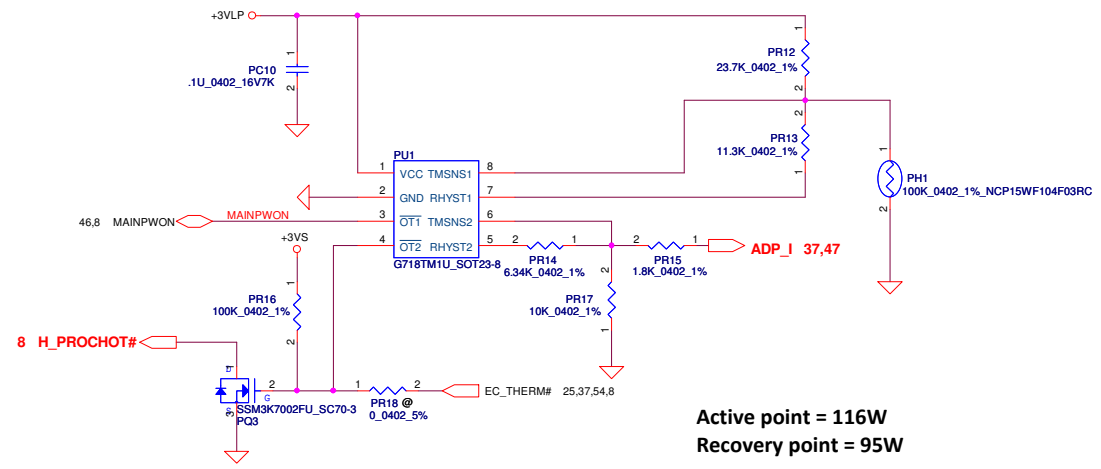
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Issued Date	2011/10/03	Deciphered Date	2014/12/31	Title	
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				PWR- DCIN / Vin Detector	0.1
				QCL51 LA-8712P	
				Date: Monday, November 28, 2011	Sheet 44 of 56



For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

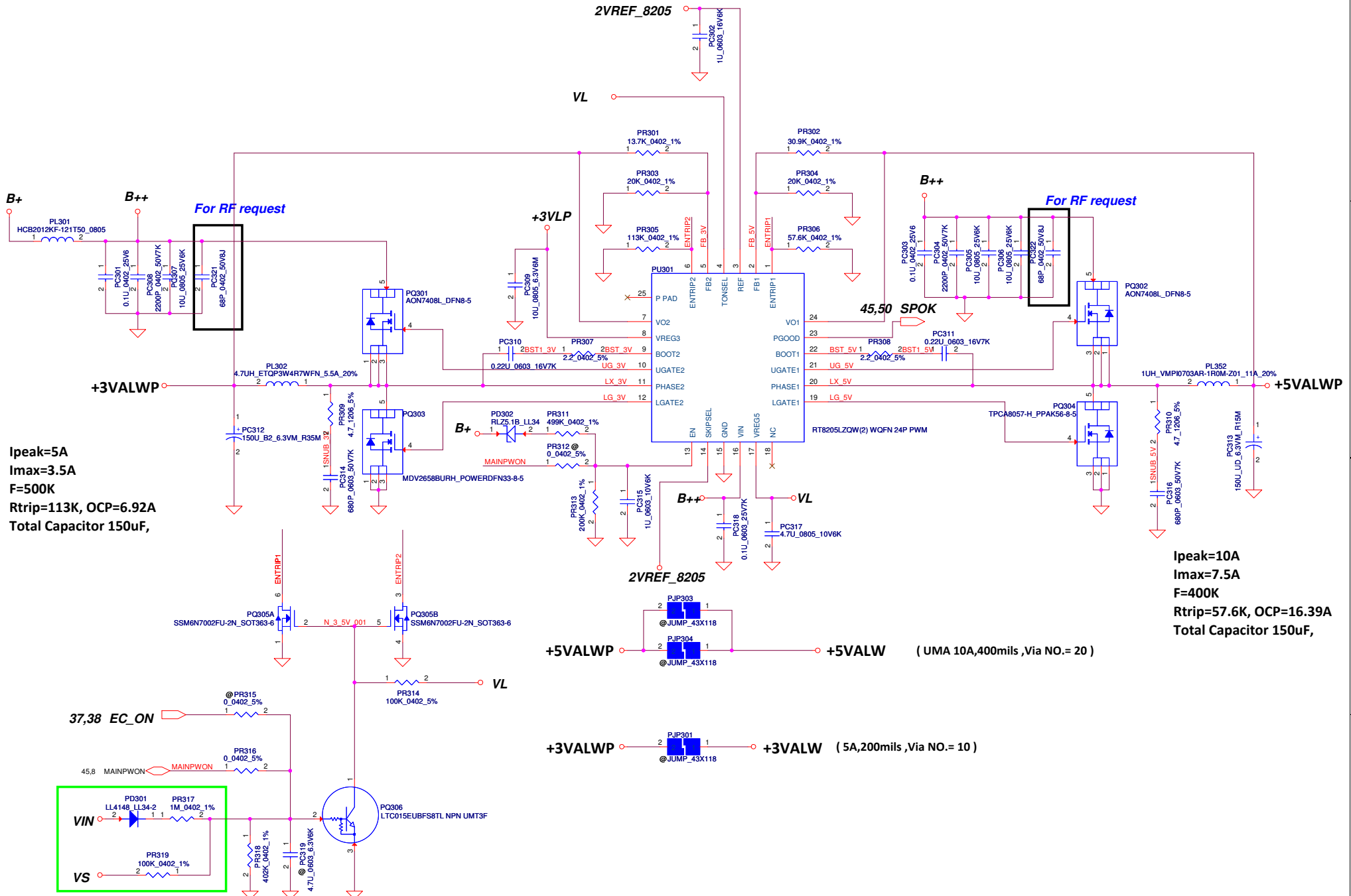
PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C
Recovery at 56 +/-3 degree C

Rset = 3 * Rtmh
 $R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$
 Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
 $R_{set} = 3 * 7.8K = 23.4K \implies 23.7K$
 $R_{hyst} = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K \implies 11.3K$



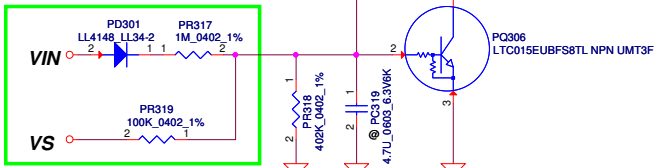
Active point = 116W
Recovery point = 95W

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				PWR- BATTERY CONN
				Customer
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				0.1
				Date: Monday, November 28, 2011 Sheet 45 of 56



Ipeak=5A
I_{max}=3.5A
F=500K
R_{trip}=113K, OCP=6.92A
Total Capacitor 150uF,

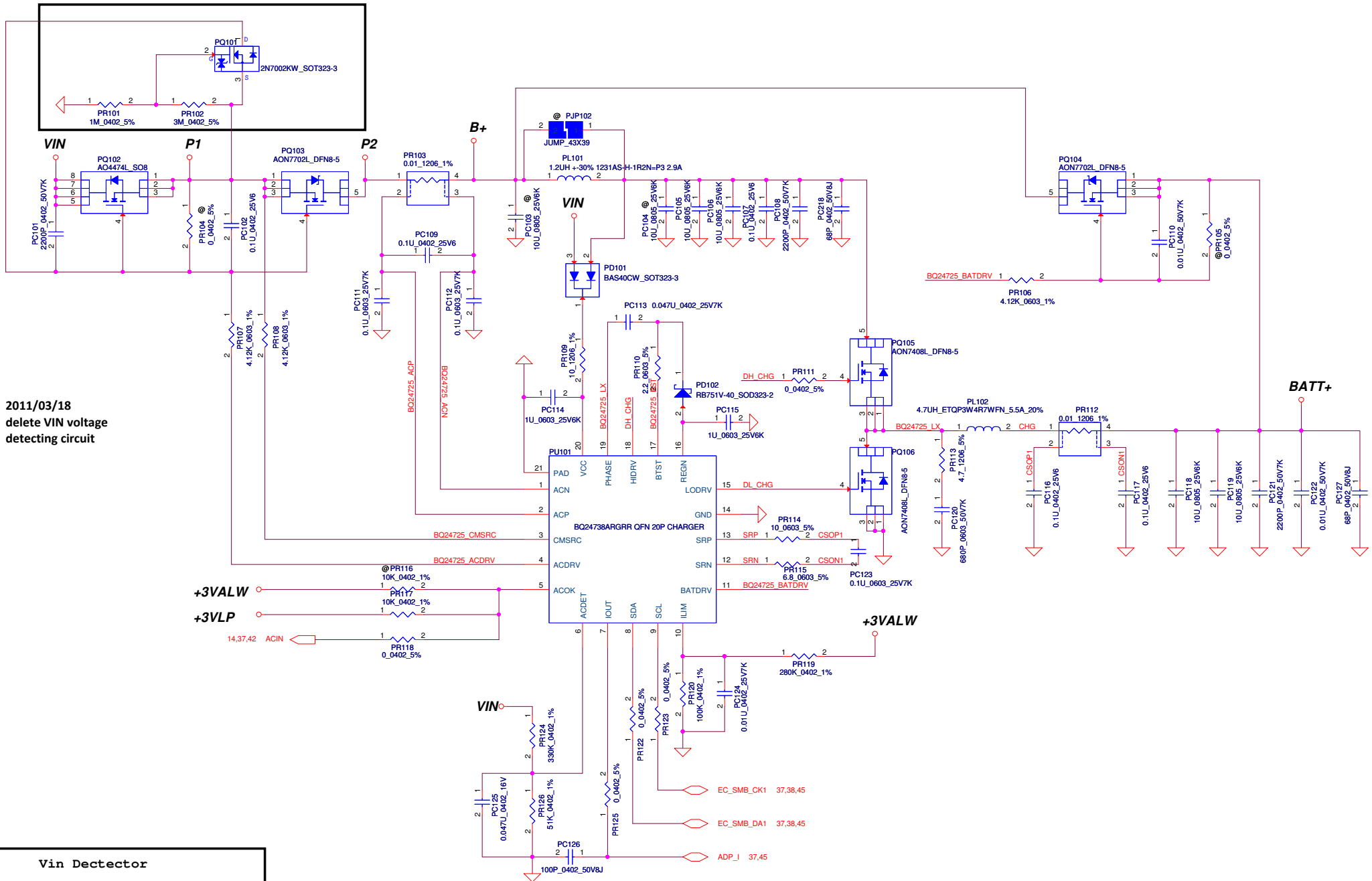
Ipeak=10A
I_{max}=7.5A
F=400K
R_{trip}=57.6K, OCP=16.39A
Total Capacitor 150uF,



For KB930 --> Keep PD301, PR317, PR319

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for reverse input protection

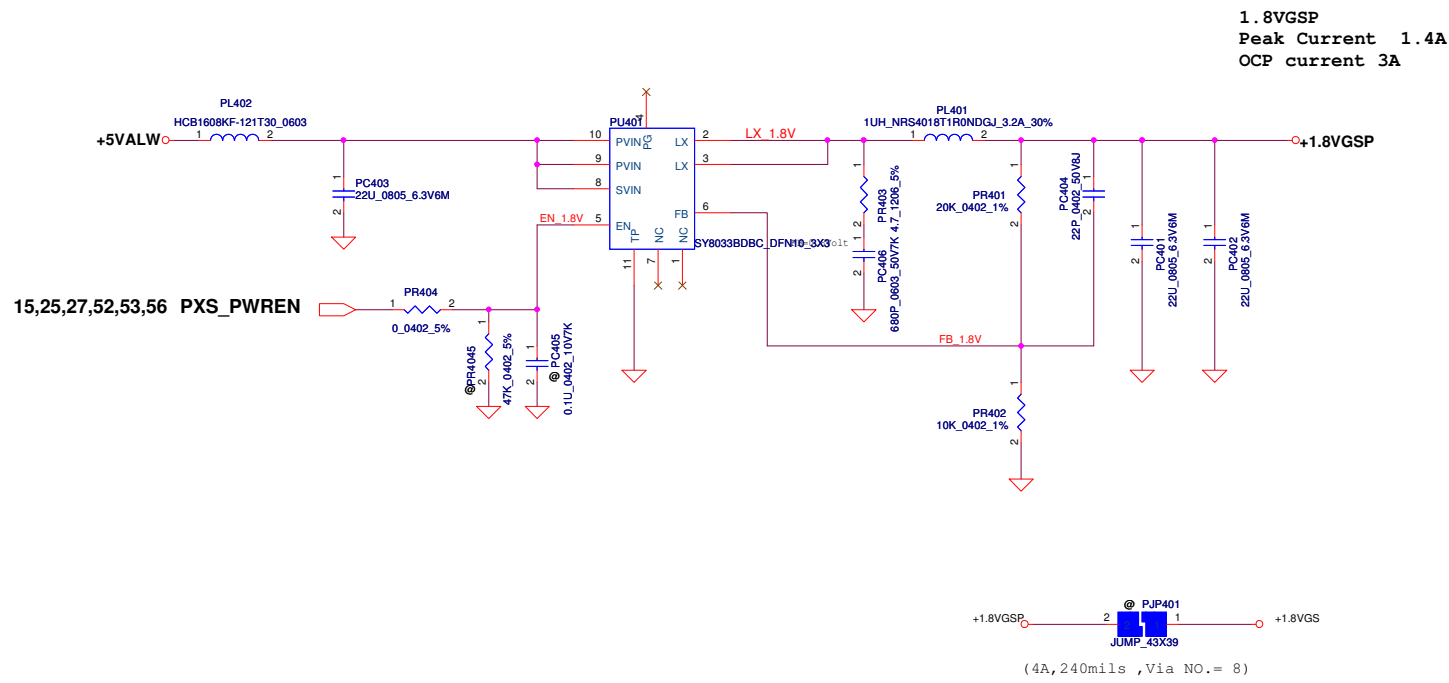


2011/03/18
delete VIN voltage
detecting circuit

Vin Detector			
	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	
ILIM and external DPM			
4.36A			

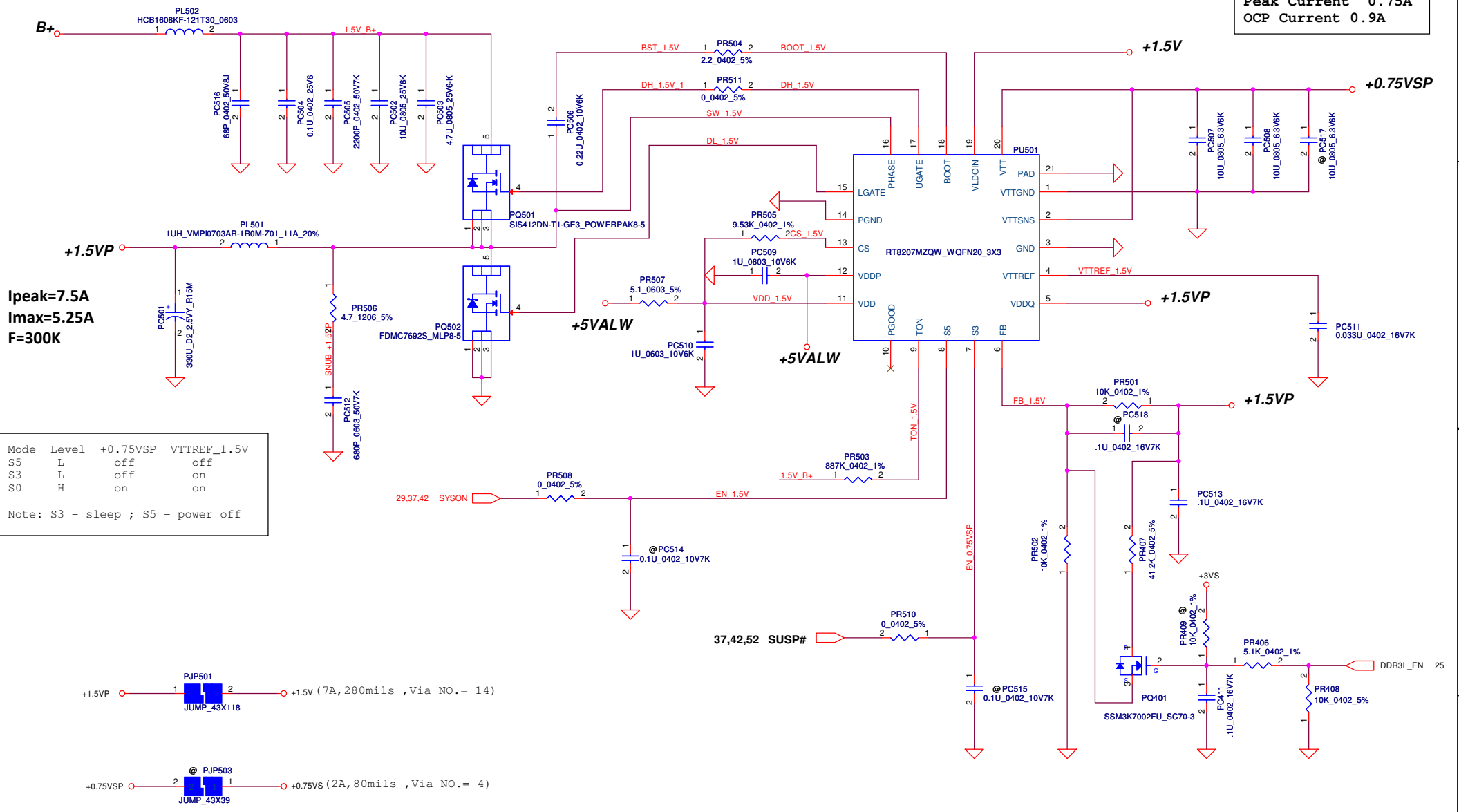
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Compal Electronics, Inc.			
PWR- CHARGER			
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Issued Date	2011/07/29	Deciphered Date	Title +1.8VP	
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0.75Volt +/- 5%
 TDC 0.525A
 Peak Current 0.75A
 OCP Current 0.9A



I_{peak}=7.5A
 I_{max}=5.25A
 F=300K

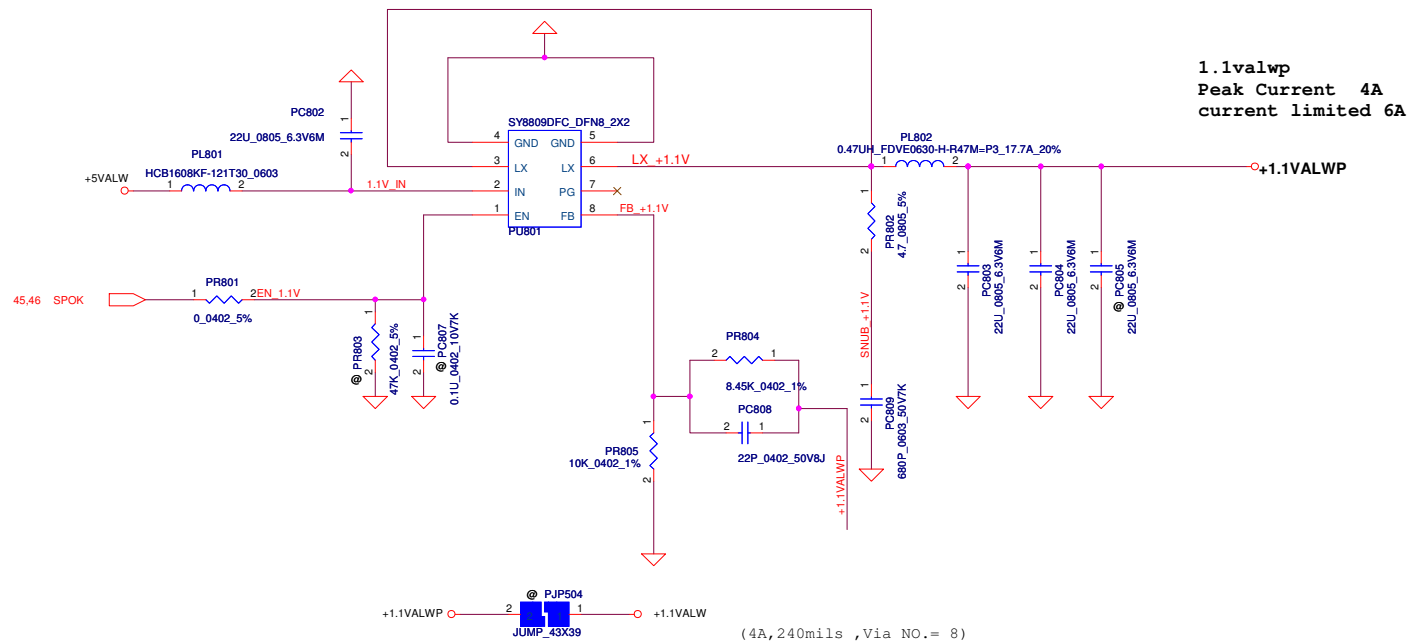
Mode	Level	+0.75VSP	VITREF_1.5V
S5	L	off	off
S3	L	off	off
S0	H	on	on

Note: S3 - sleep ; S5 - power off

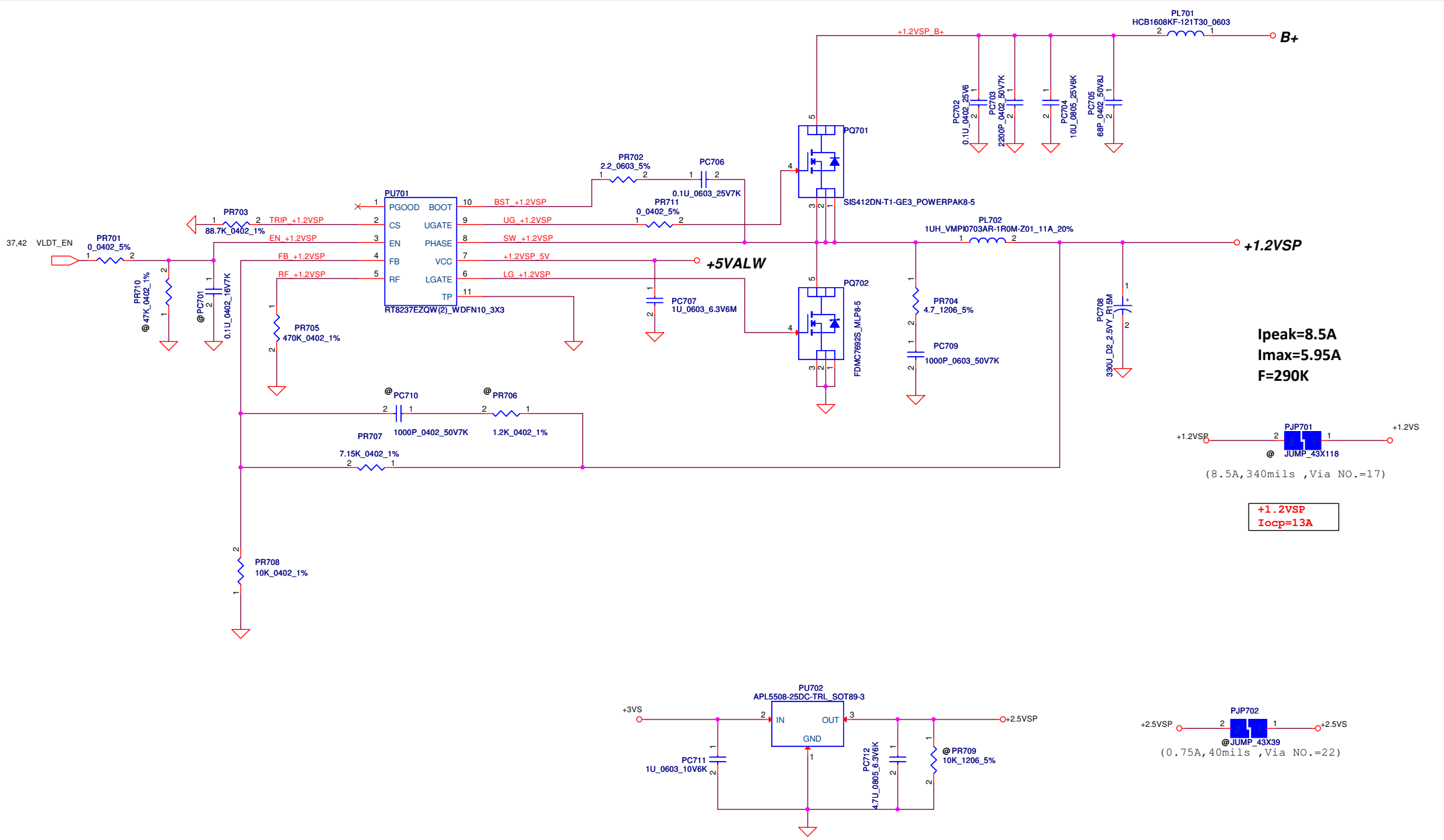
+1.5VP → 1 JJP501 JUMP_43X118 → +1.5V (7A, 280mils, Via NO.= 14)

+0.75VSP → 2 @ JJP503 JUMP_43X39 → +0.75Vs (2A, 80mils, Via NO.= 4)

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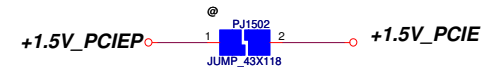
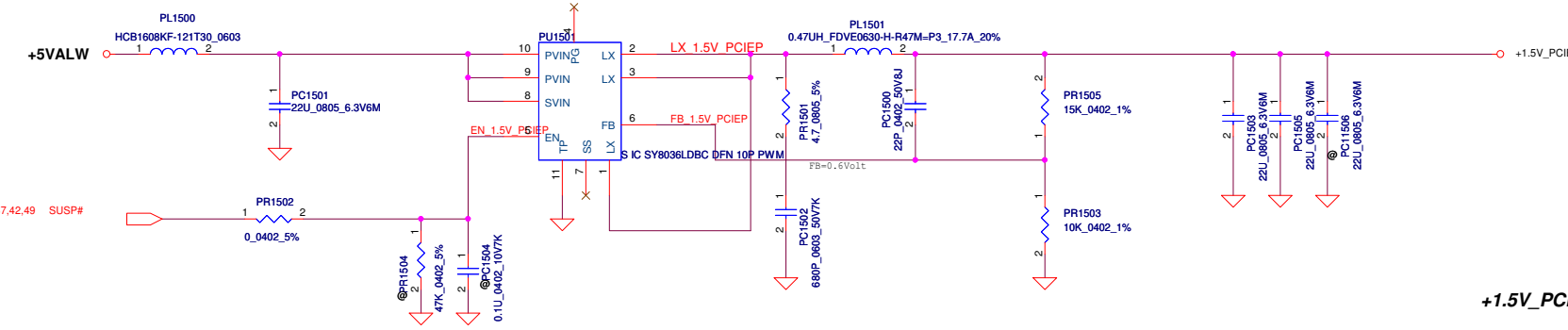
I_{peak}=8.5A
I_{max}=5.95A
F=290K

+1.2VSP
I_{ocp}=13A

PJP702
 @JUMP_43X39
 (0.75A, 40mils, Via NO.=22)

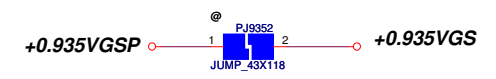
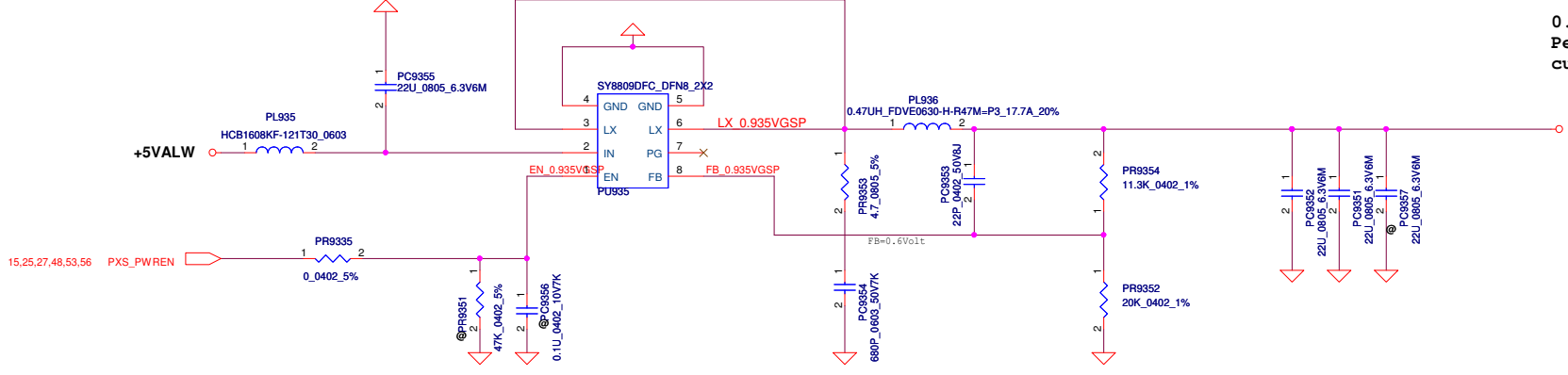
Security Classification	Compal Secret Data		Compal Electronics, Inc. +1.2VSP/+2.5VSP	
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1.5VPCIEP
Peak Current 6A
OCP current 6A



(6A, 240mils, Via NO. = 12)

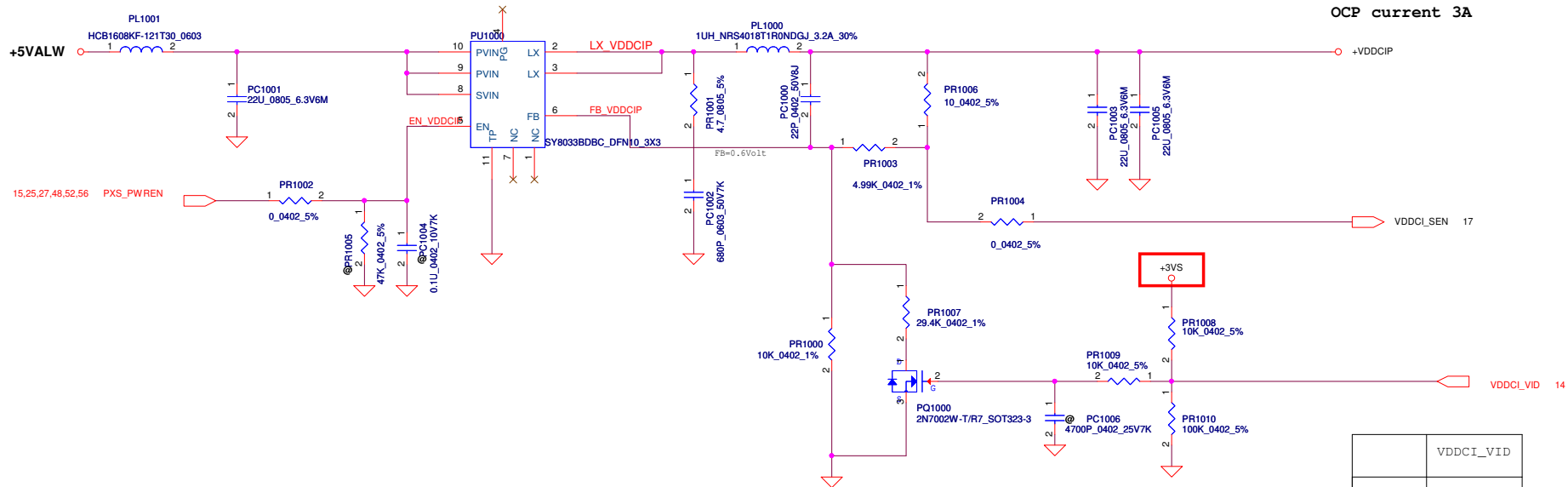
0.935VGSP
Peak Current 4.2A
current limited 6A



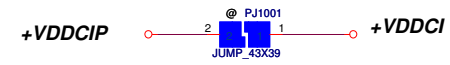
(4.2A, 460mils, Via NO. = 8.4)

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				Size	Document Number	Rev
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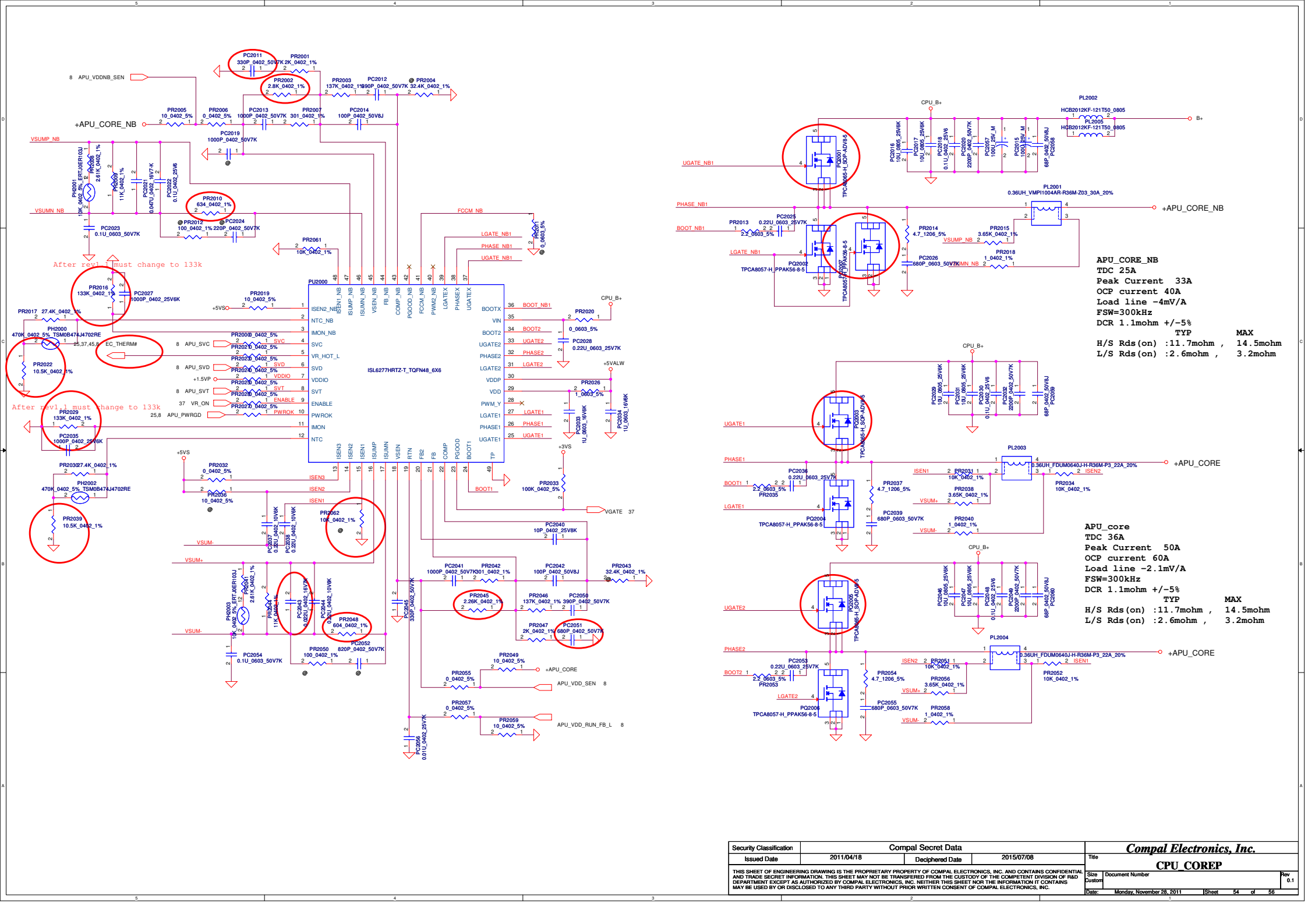
+VDDCI
TDC 2.2A
OCP current 3A



	VDDCI_VID
High	1V
Low	0.9V



(2.2A, 100mils, Via NO.= 5)



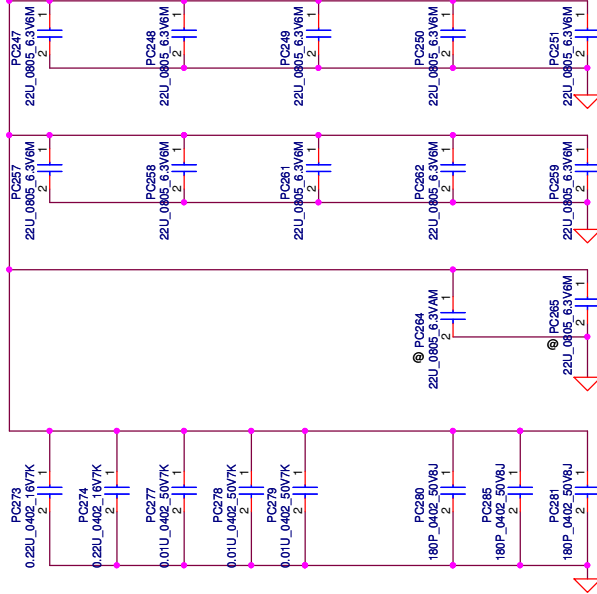
APU_CORE_NB
 TDC 25A
 Peak Current 33A
 OCP current 40A
 Load line -4mV/A
 FSW=300kHz
 DCR 1.1mohm +/-5%
 TYP
 H/S Rds (on) : 11.7mohm , 14.5mohm
 L/S Rds (on) : 2.6mohm , 3.2mohm

APU_core
 TDC 36A
 Peak Current 50A
 OCP current 60A
 Load line -2.1mV/A
 FSW=300kHz
 DCR 1.1mohm +/-5%
 TYP
 H/S Rds (on) : 11.7mohm , 14.5mohm
 L/S Rds (on) : 2.6mohm , 3.2mohm

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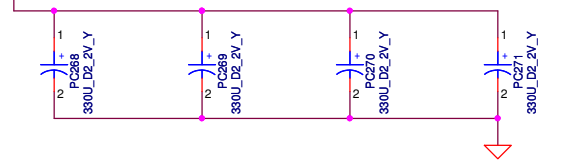
+APU_CORE

+APU_CORE



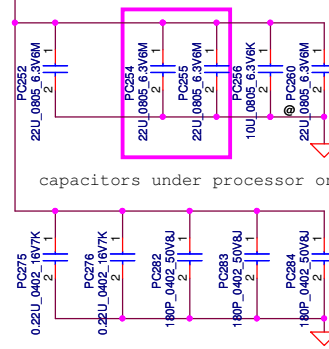
+APU_CORE

Local



+APU_CORE_NB

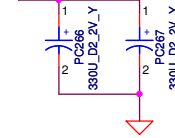
+APU_CORE_NB



capacitors under processor on bottom side of board

+APU_CORE_NB

Local



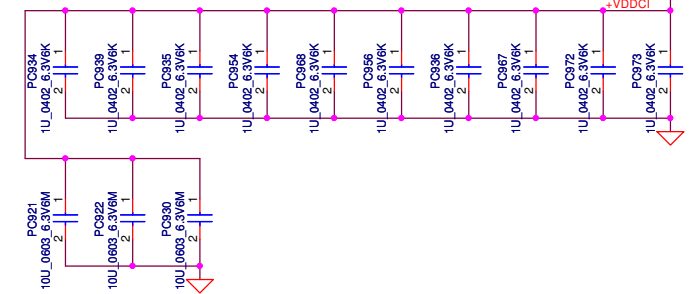
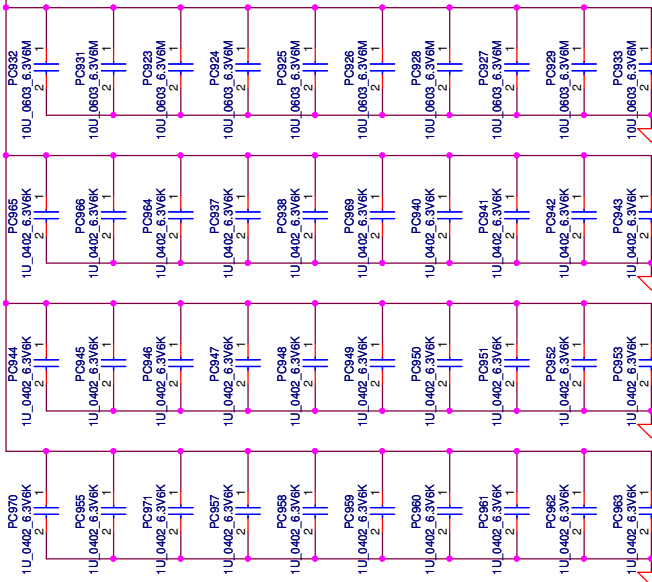
+VGA_CORE

+VGA_CORE

+VDDC

+VDDCI

+VDDCI



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				Date: Monday, November 28, 2011	Rev 0.1
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