Compal Confidential

VIWZ1/VIWZ2 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N14P-GV2

2012-12-26

LA-9063P

REV:1.0

Security Classification	Compal Secret Data		
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Title: Cover Page		
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Compal confidential
File Name : VIWZ1/VIWZ2

U4 HM76@ PCH-HM76 SA00005FH70
U4 HM70@ PCH-HM70 SA00005MQ80
ZZZ 14@ LA9063 DA_PCB DA8000XJ000
ZZZ6 15@ LA9063 DA_PCB DA8000XJ100

VIWZ1
LS9061P PWR/B
LS9062P USB/B

VIWZ2
LS9065P PWR/B
LS9062P USB/B
LS9063P ODD/B
LS9064P LED/B

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nVIDIA N14P-GV2
*VRAM 128Mb*16 DDR3*4 1GB*
*VRAM 256Mb*16 DDR3*4 2GB*

PCI-E x8

Intel Ivy Bridge
Socket-rPGA988B
37.5mm*37.5mm
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DDR3 SO-DIMM *2
BANK 0, 1, 2, 3
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Up to 8GB

Dual Channel
DDR3 1066MHz(1.5V)
DDR3 1333MHz(1.5V)
DDR3 1600MHz(1.5V)

100MHz 2.7GT/s *FDI *8* *DMI *4*

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CRT Connector Page34
LVDS Connector Page33
LVDS
eDP

Intel Panther Point
HM70 / HM76
FCBGA 989
25mm*25mm
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AZALIA

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Combo Jack*1 Page43

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USB2.0

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*SATA *6*

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ENE KB9012
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Card Reader Reltek Page44
RTS5178 for SDR50
SDXC/MMC

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RTL8105E-VD(10/100)
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Int. KBD Page43

Thermal Sensor
EMC1403 Page39

Mini PCIE Half size Slot *1
WLAN Page36
PCI-E(WLAN)

Mini PCIE Full size Slot *1
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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	LA-9061P 1.0
1	LA-9061P 0.3
2	LA-9061P 0.2
3	LA-9061P 0.1
4	LA-9063P 0.2
5	LA-9063P 0.2 15_TS
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	Z-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	Z-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	Z-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	Z-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Re-flash	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Reserved	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Reserved	PVT
7	NC	2.500 V	3.300 V	3.300 V	Reserved	MP

EC SM Bus1 address

Address

Device	
Smart Battery	0001 011X b
USB Charger	1010 111X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB Port (Left Side) USB3.0
		1	Touch Screen
	UHCI1	2	Blue Tooth
		3	Camera
EHCI1	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Port (Right Side USB-BD)
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
GPU:N14P-GV2	GV2@
OPTIMUS part	OPT@
integrate Graphic part	UMA@
GPU:N14P-GV2 Strap	GV2@
GPU:N14P-GV2 GC6 function	GC6@
OPTIMUS no support GCLK	OPTNOGCLK@
OPTIMUS support GCLK	OPTGCLK@
Support Green CLK	GCLK@
not Support Green CLK	NOGCLK@
Support Green CLK 244	GCLK244@
Support Green CLK 304	GCLK304@
Cardreader	CR@
Support HP Woofer	woofer@
Gastube	Gastube@
EC RESET function	RESET@
HDMI	HDMI@
BlueTooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8105@
GIGA LAN	GIGA@
Deep Sleep S3	DS3@
Not Support Deep Sleep S3	NODS3@
ISCT	AOAC@
ISCT not support	NOAOAC@
Camera	CMOS@
For Z490 (14")	14@
For Z590 (15")	15@
Unpop	@
USB Charger	CHG@
not USBCharger	NOCHG@
Keyboard Back Light	KBL@
Touch Screen	TS@
HM76 by PCH	HM76@
HM70 by PCH	HM70@
Cardreader RTS5178	RTS5178@
Cardreader RTS5170	RTS5170@
for 14" Touch Screen	TS_14@
for 15" Touch Screen	TS_15@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	TP
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS	X
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X	V +3VS
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X	X

GPU BOM Structure Table

BOM Structure	N14P-GV2
OPT@	V
OPTNOGCLK@	V
GV2@	V
GC6@	Select

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Title: Notes List

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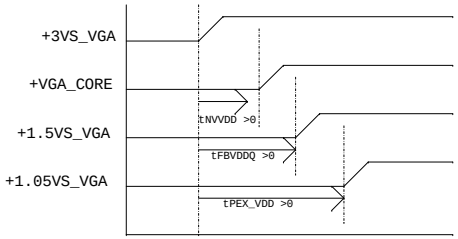
Hot plug detect for IFP link C

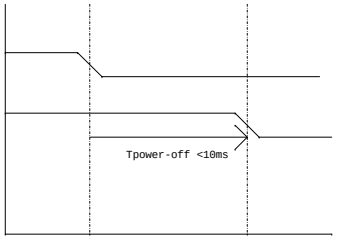
VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	I	H	GC6_FB_CLAMP
GPIO1	OUT	-	MEM_VDD_CTL
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	RESERVED
GPIO6	OUT	L	GC6_FB_REQ
GPIO7	OUT	-	3DVision
GPIO8	I/O	L	Thermal Catastrophic Over Temperature
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	PWM_VID
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	PSI
GPIO14	OUT	N/A	
GPIO15	IN		
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us

2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



1.all GPU power rails should be turned off within 10ms

Performance Mode P0 TDP at Tj = 102 C* (GDDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

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Title: VGA Notes List

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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
*	0:Lane Reversed

JCPU1A

PCI EXPRESS* - GRAPHICS

DMI

Intel(R) FDI

eDP

TYCO_2013620-2_IVY BRIDGE

+V1.05S_VCCP

R1 24.9_0402_1%

PEG_COMP

PCIE_CRX_GTX_N[0..15] <23>

PCIE_CRX_GTX_P[0..15] <23>

PCIE_CTX_GRX_N[0..15] <23>

PCIE_CTX_GRX_P[0..15] <23>

R7 24.9_0402_1%

EDP_COMP

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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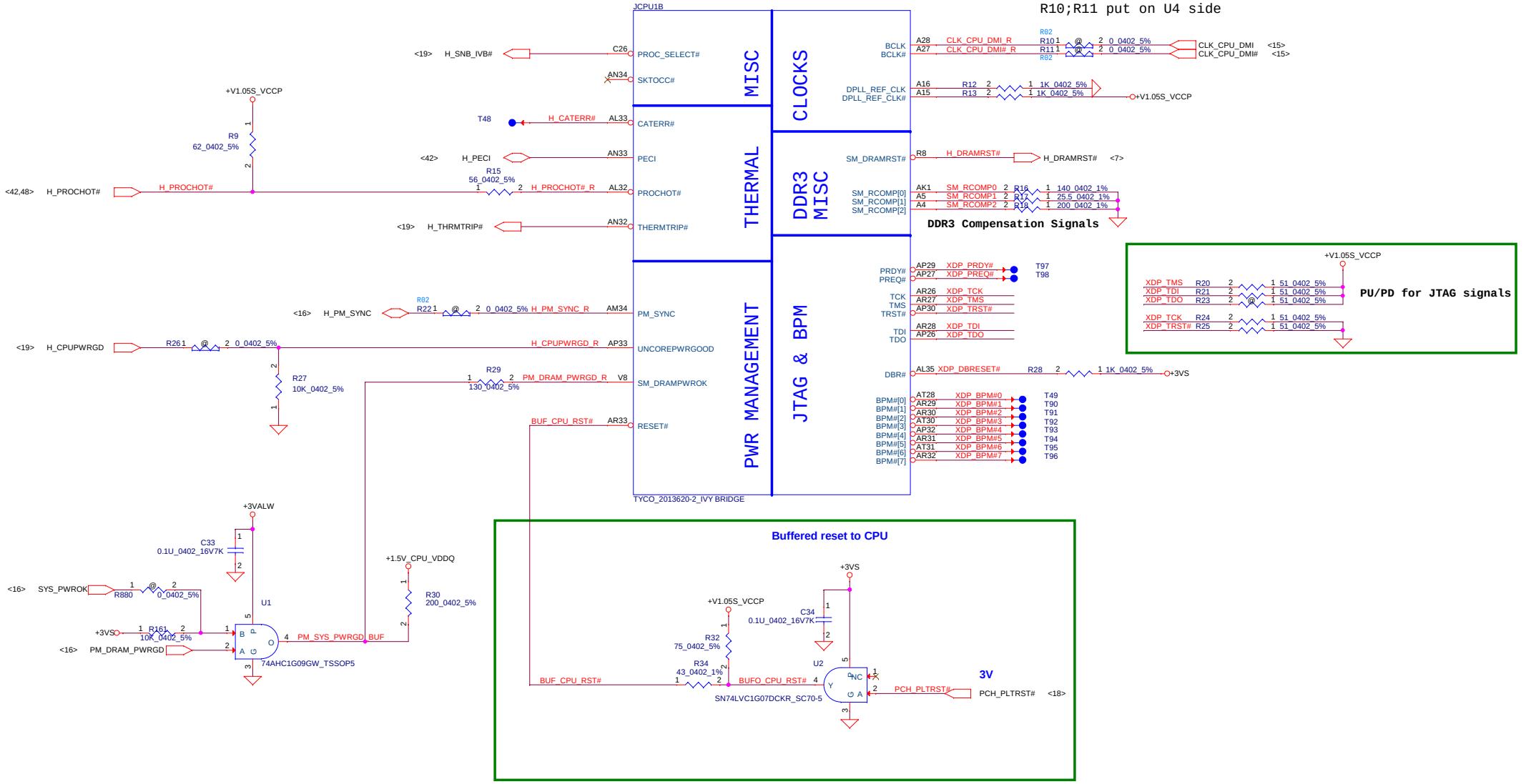

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Title	PROCESSOR(2/7) PM,XDP,CLK		
Size: Custom	Document Number: LA-9603P		Rev: 1.0
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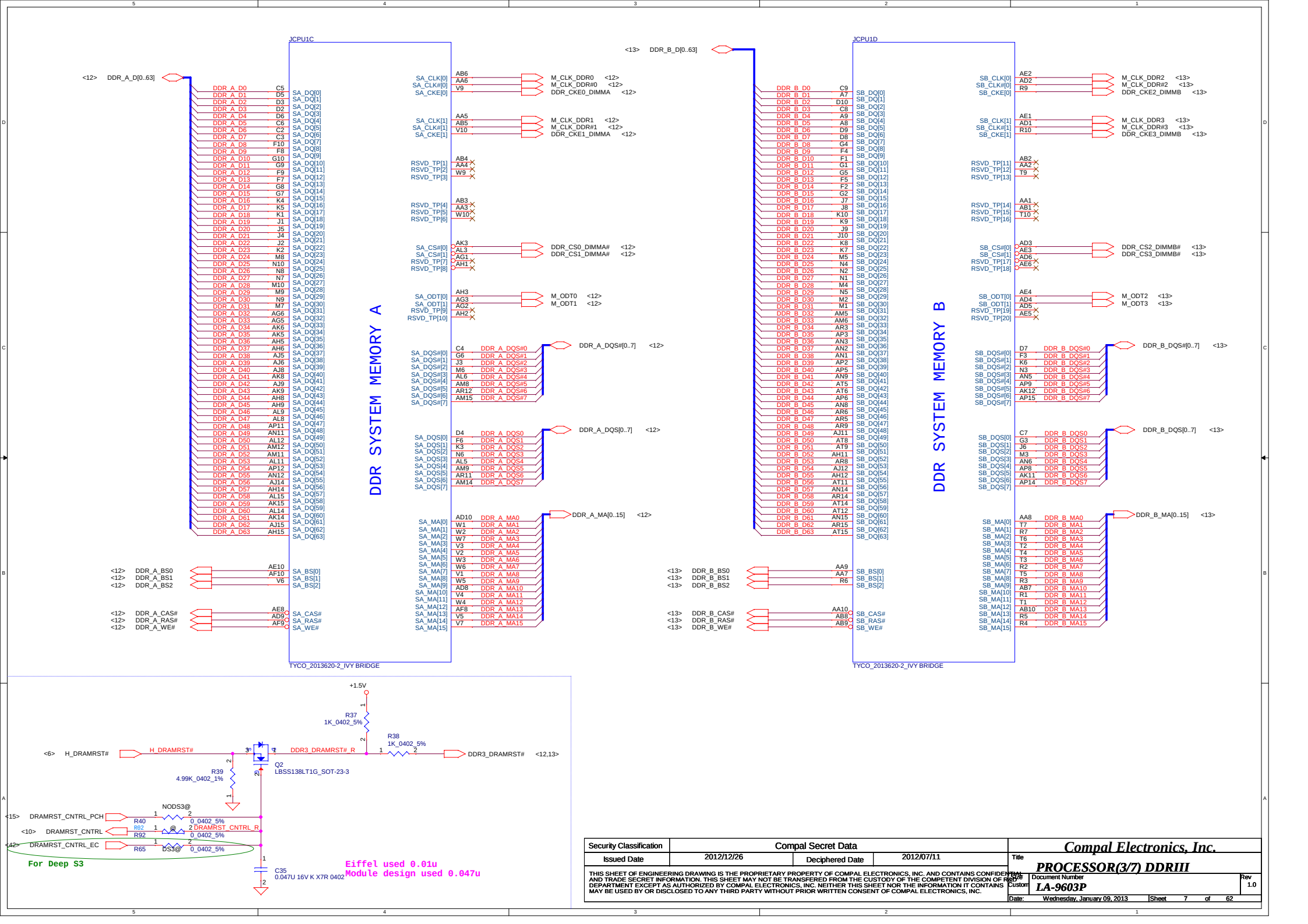

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Title: PROCESSOR(3/7) DDRIII

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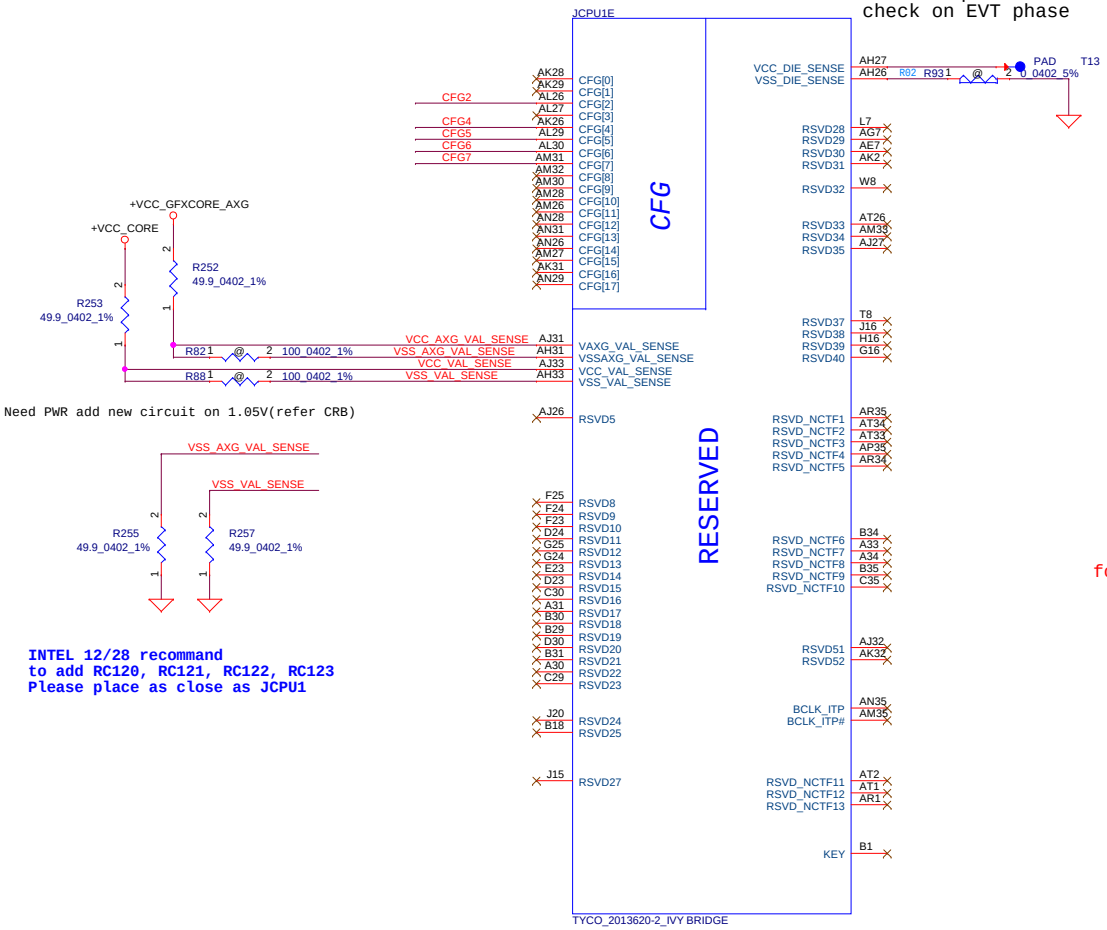
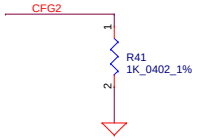
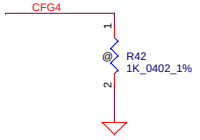
CFG Straps for Processor

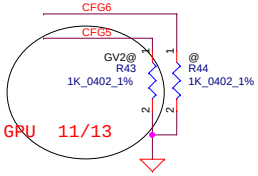




PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

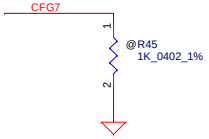


Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



for N14P_GV2 GPU 11/13

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

VCC1 AG35, VCC2 AG34, VCC3 AG33, VCC4 AG32, VCC5 AG31, VCC6 AG30, VCC7 AG29, VCC8 AG28, VCC9 AG27, VCC10 AG26, VCC11 AF35, VCC12 AF34, VCC13 AF33, VCC14 AF32, VCC15 AF31, VCC16 AF30, VCC17 AF29, VCC18 AF28, VCC19 AF27, VCC20 AF26, VCC21 AD35, VCC22 AD34, VCC23 AD33, VCC24 AD32, VCC25 AD31, VCC26 AD30, VCC27 AD29, VCC28 AD28, VCC29 AD27, VCC30 AD26, VCC31 AC35, VCC32 AC34, VCC33 AC33, VCC34 AC32, VCC35 AC31, VCC36 AC30, VCC37 AC29, VCC38 AC28, VCC39 AC27, VCC40 AC26, VCC41 AA35, VCC42 AA34, VCC43 AA33, VCC44 AA32, VCC45 AA31, VCC46 AA30, VCC47 AA29, VCC48 AA28, VCC49 AA27, VCC50 AA26, VCC51 Y35, VCC52 Y34, VCC53 Y33, VCC54 Y32, VCC55 Y31, VCC56 Y30, VCC57 Y29, VCC58 Y28, VCC59 Y27, VCC60 Y26, VCC61 V35, VCC62 V34, VCC63 V33, VCC64 V32, VCC65 V31, VCC66 V30, VCC67 V29, VCC68 V28, VCC69 V27, VCC70 V26, VCC71 U35, VCC72 U34, VCC73 U33, VCC74 U32, VCC75 U31, VCC76 U30, VCC77 U29, VCC78 U28, VCC79 U27, VCC80 U26, VCC81 R35, VCC82 R34, VCC83 R33, VCC84 R32, VCC85 R31, VCC86 R30, VCC87 R29, VCC88 R28, VCC89 R27, VCC90 R26, VCC91 P35, VCC92 P34, VCC93 P33, VCC94 P32, VCC95 P31, VCC96 P30, VCC97 P29, VCC98 P28, VCC99 P27, VCC100 P26

PEG AND DDR

VCCIO1 AH13, VCCIO2 AH10, VCCIO3 AG10, VCCIO4 AC10, VCCIO5 Y10, VCCIO6 U10, VCCIO7 P10, VCCIO8 L10, VCCIO9 J14, VCCIO10 J13, VCCIO11 J12, VCCIO12 J11, VCCIO13 H14, VCCIO14 H12, VCCIO15 H11, VCCIO16 G14, VCCIO17 G13, VCCIO18 G12, VCCIO19 F14, VCCIO20 F13, VCCIO21 F12, VCCIO22 F11, VCCIO23 E14, VCCIO24 E12, VCCIO25 E11, VCCIO26 D14, VCCIO27 D13, VCCIO28 D12, VCCIO29 D11, VCCIO30 C14, VCCIO31 C13, VCCIO32 C12, VCCIO33 C11, VCCIO34 B14, VCCIO35 B12, VCCIO36 A14, VCCIO37 A13, VCCIO38 A12, VCCIO39 A11, VCCIO40 J23

SVID

+V1.05S_VCCP

C99 0.1U_0402_16V7K

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# — R47 43_0402_5% — VR_SVID_ALRT# <55>
VIDSCLK AJ30 H_CPU_SVIDCLK — R02 R48 0_0402_5% — VR_SVID_CLK <55>
VIDSOUT AJ28 H_CPU_SVIDDAT — R02 R49 0_0402_5% — VR_SVID_DAT <55>

R50 130_0402_5% +V1.05S_VCCP

0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

SENSE LINES

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

+VCC_CORE

R51 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R — R02 R52 0_0402_5% — VCCSENSE <55>
VSS_SENSE AJ34 VSSSENSE_R — R02 R53 0_0402_5% — VSSSENSE <55>

R54 100_0402_1%

VCCIO_SENSE B10 — VCCIO_SENSE <53>
VSS_SENSE_VCCIO A10 VSSIO_SENSE_L — R74 10_0402_1% — VSSIO_SENSE

R74 & R79 put together

+V1.05S_VCCP

R79 10_0402_1%

VSSIO_SENSE_L <53>

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_IVY BRIDGE

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Title: PROCESSOR(5/7) PWR,BYPASS

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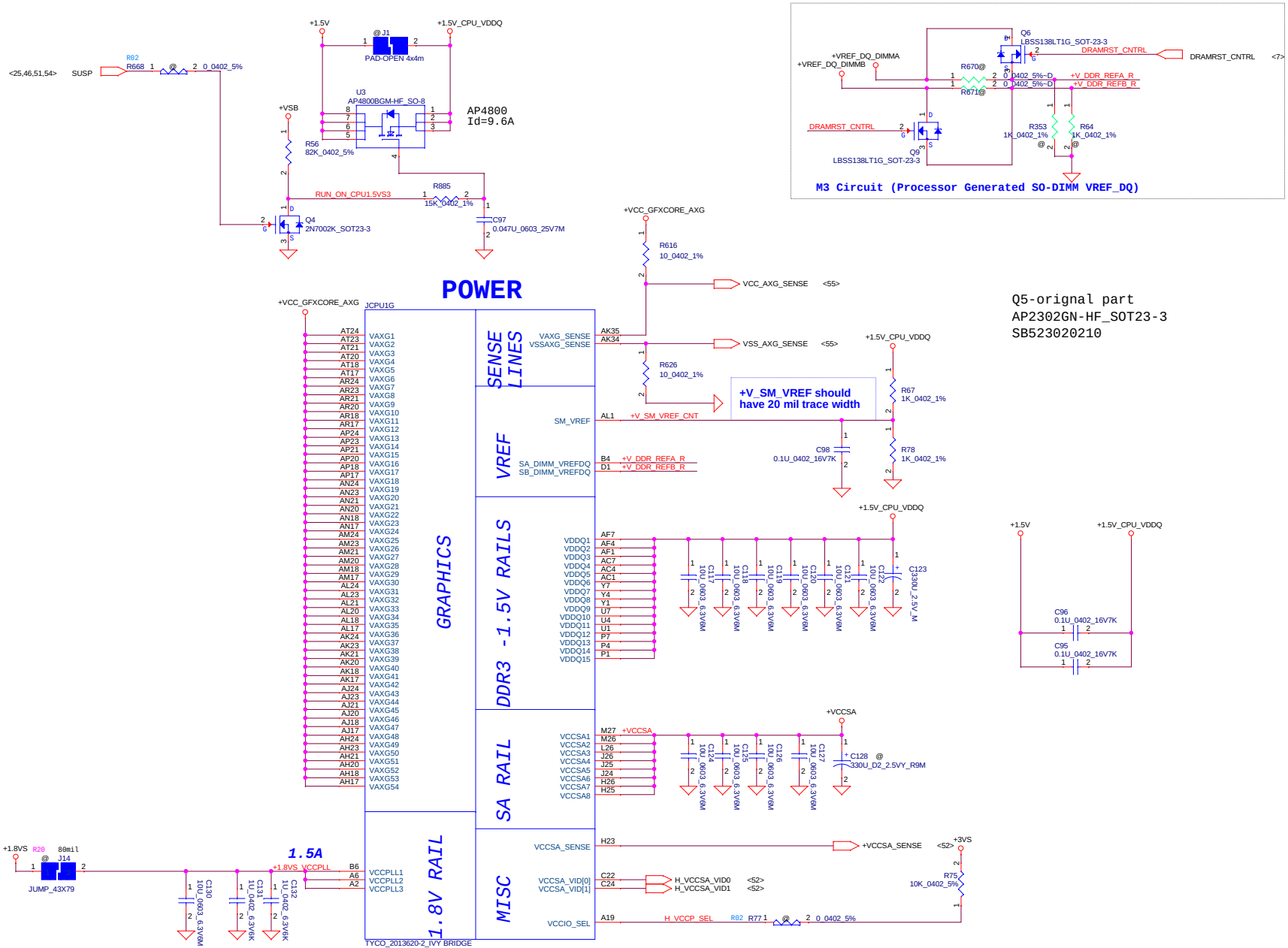

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Title	PROCESSOR(6/7) PWR		
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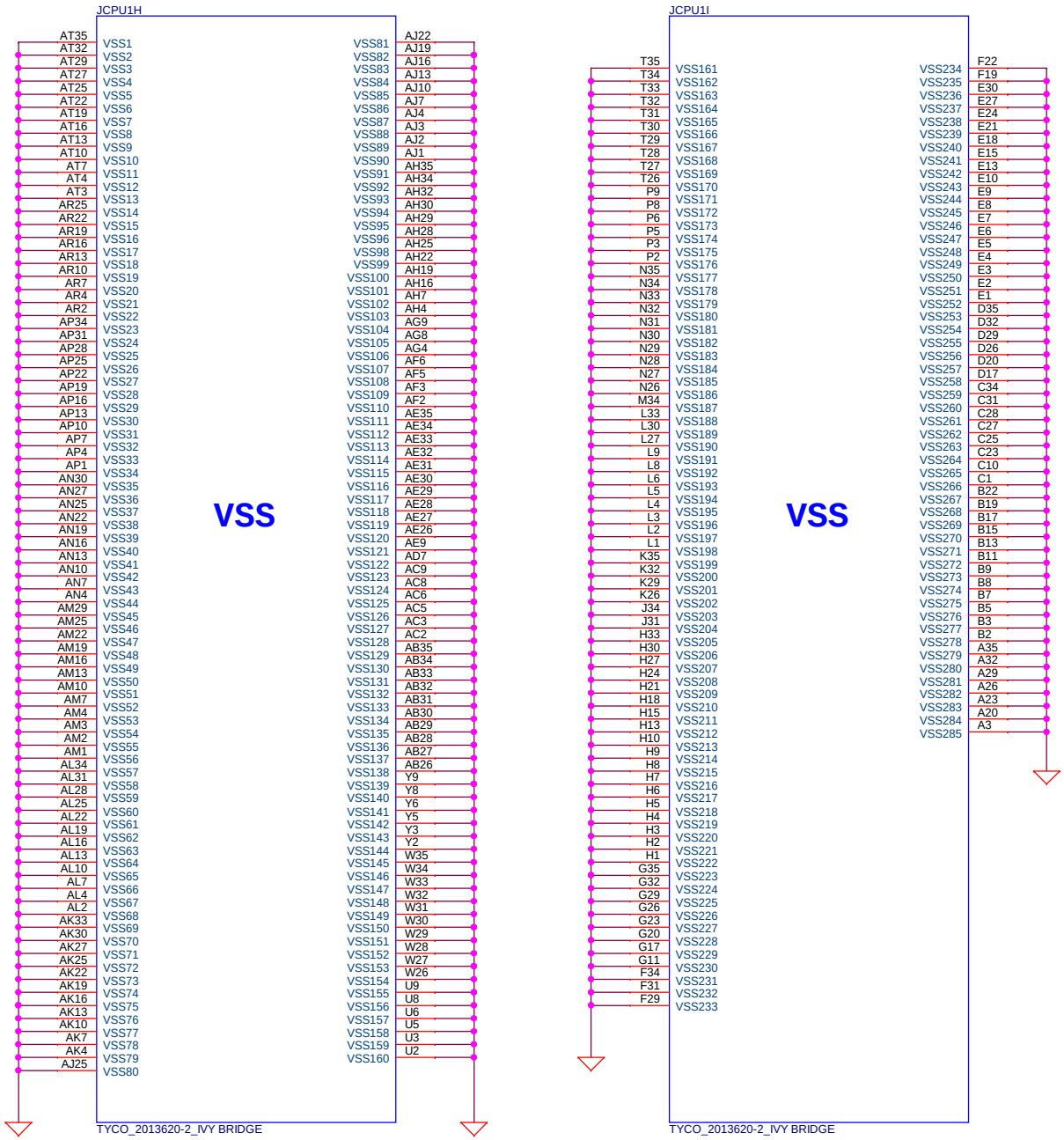

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Title: **PROCESSOR(7/7) VSS**

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DDR3 SO-DIMM A

JDIMM1

LCN_DAN06-K4806-0103

ME@

+1.5V

+VREF_DQ_DIMMA

R70 1K_0402_1%

R71 1K_0402_1%

C134 22U_0603_6.3V6K

C133 0.1U_0402_16V7K

DDR_A_D[0..63]

DDR_A_DQS[0..7]

DDR_A_DQS#[0..7]

DDR_A_MA[0..15]

DDR3_DRAMRST# <7,13>

SMB_DATA_S3 <13,15,36,43>

SMB_CLK_S3 <13,15,36,43>

+0.75VS

0.65A@.75V

+3VS

R81 10K_0402_5%

R83 10K_0402_5%

C155 2.2U_0603_6.3V6K

C156 0.1U_0402_16V7K

C135 0.1U_0402_16V7K

C136 22U_0603_6.3V6K

R72 1K_0402_1%

R73 1K_0402_1%

+VREF_CA

M_CLK_DDR0 <7>

M_CLK_DDR#0 <7>

M_CLK_DDR1 <7>

M_CLK_DDR#1 <7>

DDR_A_BS2 <7>

DDR_A_BS0 <7>

DDR_A_BS1 <7>

DDR_A_RAS# <7>

DDR_A_WE# <7>

DDR_A_CAS# <7>

DDR_CS1_DIMMA# <7>

DDR_CS0_DIMMA# <7>

M_ODT0 <7>

M_ODT1 <7>

DDR_CKE0_DIMMA <7>

DDR_CKE1_DIMMA <7>

Layout Note: Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)

(10uF_0603_6.3V)*8

(0.1uF_402_10V)*4

C139 10U_0603_6.3V6M

C140 10U_0603_6.3V6M

C141 10U_0603_6.3V6M

C142 10U_0603_6.3V6M

C143 10U_0603_6.3V6M

C144 10U_0603_6.3V6M

C145 0.1U_0402_16V7K

C146 0.1U_0402_16V7K

C147 0.1U_0402_16V7K

C148 0.1U_0402_16V7K

C149 @ 220U_6.3V_M

EVT Check

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

Layout Note: Place near DIMM

7/28 Update connect GND directly

C152 1U_0402_6.3V6K

Layout Note: Place near DIMM

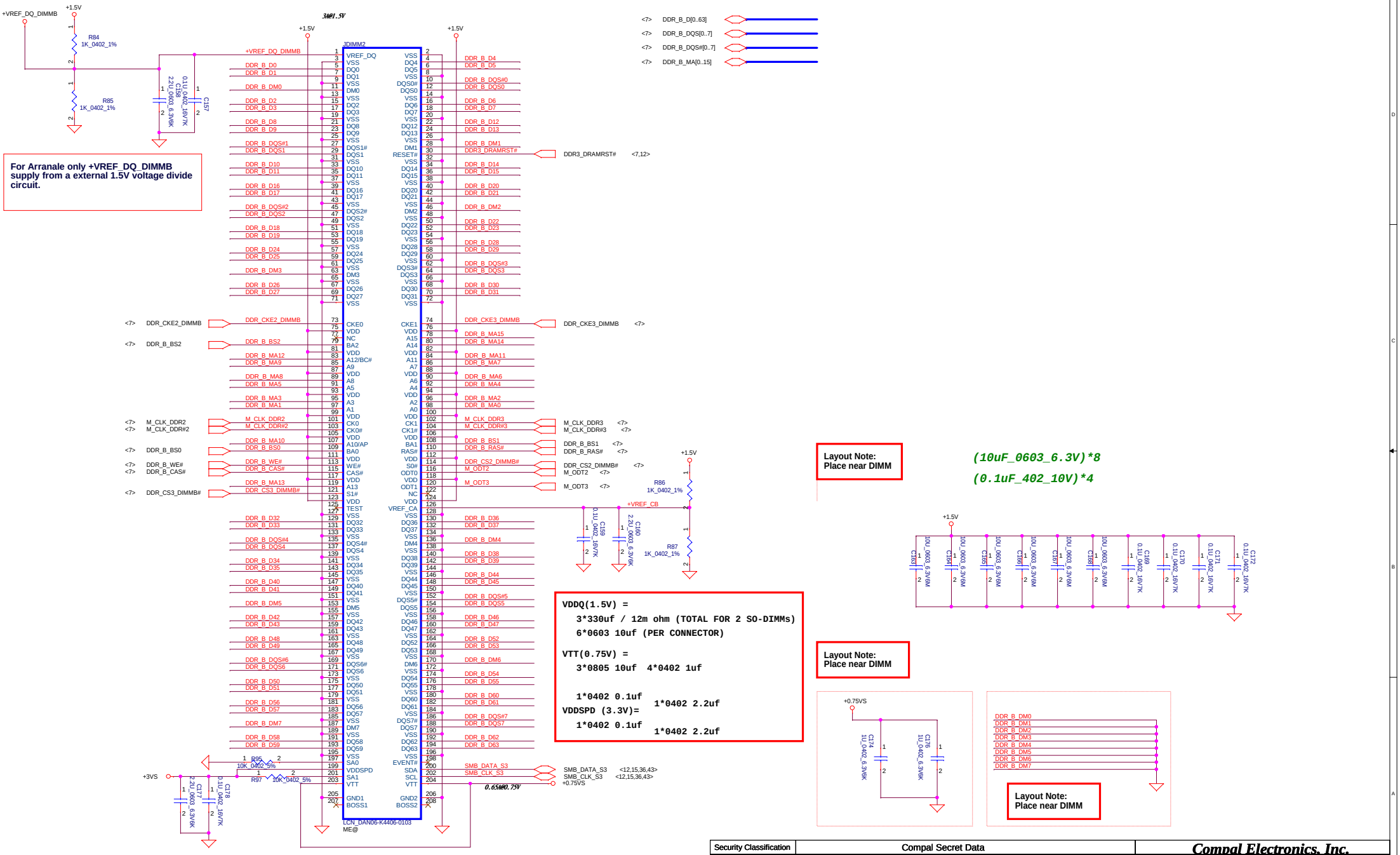
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size: Custom | Document Number: **LA-9603P** | Rev: 1.0

Date: Wednesday, January 09, 2013 | Sheet 12 of 62



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size	Document Number	Rev
	LA-9603P	1.0

Date: Wednesday, January 09, 2013 | Sheet 13 of 62

W=20mils
+RTCVCC
R99 1K_0402_5%
C179 1U_0402_6.3V6K
W=20mils
+RTCBATT
CLRP1 SHORT PADS

PCH_RTCX1
R98 10M_0402_5% NOGCLK@
PCH_RTCX2
Y1 32.768KHZ_12.5PF_CM31532768DZFT
C180 18P_0402_50V8J NOGCLK@
C181 18P_0402_50V8J NOGCLK@
R82 Remove R176
close to Y1

R182 0_0402_5% GCLK@
GCLK_32K
GCLK_32K <44>

CMOS
+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN
INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

C183 1U_0402_6.3V6K
R103 20K_0402_5%
R100 20K_0402_5%
C182 1U_0402_6.3V6K
CLRP2 SHORT PADS
CLRP3 SHORT PADS

U4A

PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

LPC
FWH0 / LAD0 C38 LPC_AD0 — LPC_AD0 <36,42>
FWH1 / LAD1 A38 LPC_AD1 — LPC_AD1 <36,42>
FWH2 / LAD2 B37 LPC_AD2 — LPC_AD2 <36,42>
FWH3 / LAD3 C37 LPC_AD3 — LPC_AD3 <36,42>
EC and Mini card debug port
FWH4 / LFRAME# D36 LPC_FRAME# — LPC_FRAME# <36,42>
LDRQ0# E36
LDRQ1# / GPIO23 K36
R104 10K_0402_5% +3VS
SERIRQ V5 SERIRQ — SERIRQ <42>

+3VS
R105 1K_0402_5% HDA_SPKR
HIGH= Enable (No Reboot)
LOW= Disable (Default)

+3V_PCH
R106 1K_0402_5% HDA_SDOUT
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH
R108 1K_0402_5% HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
*1.8V when sampled low
Needs to be pulled High for Chief River platfrom

HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
<41> HDA_SPKR HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
<41> HDA_SDIN0 HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
IHDA

<42> ME_FLASH R109 0_0402_5% HDA_SDOUT A36 HDA_SDO
R107 1K_0402_1% PCH_GPIO33 C36 HDA_DOCK_EN# / GPIO33
+3V_PCH 10K_0402_5% R264 N32 HDA_DOCK_RST# / GPIO13

R110 51_0402_5% PCH_JTAG_TCK J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG

SATA
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7 SATA_ITX_C_DRX_N0 0.01U_0402_16V7K
SATA0TXP AP5 SATA_ITX_C_DRX_P0 0.01U_0402_16V7K
C184 SATA_ITX_DRX_N0
C185 SATA_ITX_DRX_P0
CAP on Conn, side
SATA_DTX_C_IRX_N0 SATA_DTX_C_IRX_P0
SATA_DTX_C_IRX_N0 <36> SATA_DTX_C_IRX_P0 <36> SATA_ITX_DRX_N0 <36> SATA_ITX_DRX_P0 <36>
SSD

SATA1RXN AM10 SATA_DTX_R_IRX_N1 — 0_0402_5% HM70@ R311
SATA1RXP AM8 SATA_DTX_R_IRX_P1 — 0_0402_5% HM70@ R312
SATA1TXN AP11 SATA_ITX_R_DRX_N1 0.01U_0402_16V7K — C198 SATA_ITX_C_DRX_N1 — 0_0402_5% R5593 SATA_ITX_DRX_N1
SATA1TXP AP10 SATA_ITX_R_DRX_P1 0.01U_0402_16V7K — C199 SATA_ITX_C_DRX_P1 — 0_0402_5% R5594 SATA_ITX_DRX_P1
CAP on Conn, side
SATA_DTX_C_IRX_N1 SATA_DTX_C_IRX_P1
SATA_DTX_C_IRX_N1 <40> SATA_DTX_C_IRX_P1 <40> SATA_ITX_DRX_N1 <40> SATA_ITX_DRX_P1 <40>
HDD

SATA2RXN AD7 SATA_DTX_C_IRX_N2
SATA2RXP AD5 SATA_DTX_C_IRX_P2
SATA2TXN AH5 SATA_ITX_C_DRX_N2
SATA2TXP AH4 SATA_ITX_C_DRX_P2
SATA_DTX_C_IRX_N2 <40> SATA_DTX_C_IRX_P2 <40> SATA_ITX_C_DRX_N2 <40> SATA_ITX_C_DRX_P2 <40>
ODD

SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
HM70 Disable SATA Port 1,3

SATA4RXN Y7 SATA_DTX_R_IRX_N4 — 0_0402_5% HM70@ R318 SATA_DTX_C_IRX_N1
SATA4RXP Y5 SATA_DTX_R_IRX_P4 — 0_0402_5% HM70@ R315 SATA_DTX_C_IRX_P1
SATA4TXN AD3 SATA_ITX_R_DRX_N4 0.01U_0402_16V7K — C229 SATA_ITX_C_DRX_N1
SATA4TXP AD1 SATA_ITX_R_DRX_P4 0.01U_0402_16V7K — C237 SATA_ITX_C_DRX_P1
HDD

SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1

SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP — R111 37.4_0402_1% +1.05VS_VCC_SATA
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP — R113 49.9_0402_1% +1.05VS_SATA3
SATA3RBIAS AH1 RBIAS_SATA3 — R115 750_0402_1%

SATALED# P3 SATALED# — R117 10K_0402_5% +3VS
SATA0GP / GPIO21 V14 PCH_GPIO21 — R119 10K_0402_5% +3VS
SATA1GP / GPIO19 P1 BBS_BIT0_R — R187 10K_0402_5% +3VS

PANTHER-POINT_FCBGA989

<41> HDA_BITCLK_AUDIO R112 33_0402_5% HDA_BIT_CLK
<41> HDA_SYNC_AUDIO R114 33_0402_5% HDA_SYNC_R
<41> HDA_RST_AUDIO# R116 33_0402_5% HDA_RST#
<41> HDA_SDOUT_AUDIO R118 33_0402_5% HDA_SDOUT

+5VS
Q10 LBSS138LT1G_SOT-23-3
HDA_SYNC
R878 1M_0402_5%

SPI_CLK_PCH_R T3 SPI_CLK
SPI_SB_CS0# Y14 SPI_CS0#
SPI_SB_CS1# T1 SPI_CS1#
SPI_SI V4 SPI_MOSI
SPI_SO_R U3 SPI_MISO
SPI

check with vender
Del Q10 check with codec
VDDIO using 3VALW

8MB SPI ROM FOR ME
& Non-share ROM.

R82 R291 0_0402_5% SPI_SB_CS1# — CS1# SPI_SO1
SPI_SO_R — SPI_WP#1
R188 33_0402_5%
U6 CS# SO WP# GND VCC HOLD# SCLK SI
16M W25Q16BVSSIG SOIC 8P
+3VS
R82 R199 0_0402_5% SPI_CLK1 — SPI_CLK_PCH_R
SPI_SI1 — SPI_SI
R196 33_0402_5%

SPI_CLK_PCH_R
R124 33_0402_5% @
C190 22P_0402_50V8J @
R124;c190 close to U4.T3 pin

+3VS
R266 3.3K_0402_5% SPI_WP#1
R221 3.3K_0402_5% SPI_HOLD#1
R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#

U6 Rersver 4M+2M Solution

+3VS
C191 0.1U_0402_16V7K
R82 R130 0_0402_5% SPI_SB_CS0# — CS#
SPI_SO_R — SPI_SO_L — SPI_WP#
33_0402_5% R131
U5 CS# SO WP# GND VCC HOLD# SCLK SI
W25Q32BVSSIG_SO8
R82 R132 0_0402_5% SPI_HOLD# — SPI_CLK_PCH
SPI_SI_R — SPI_CLK_PCH_R
SPI_SI
R133 33_0402_5%

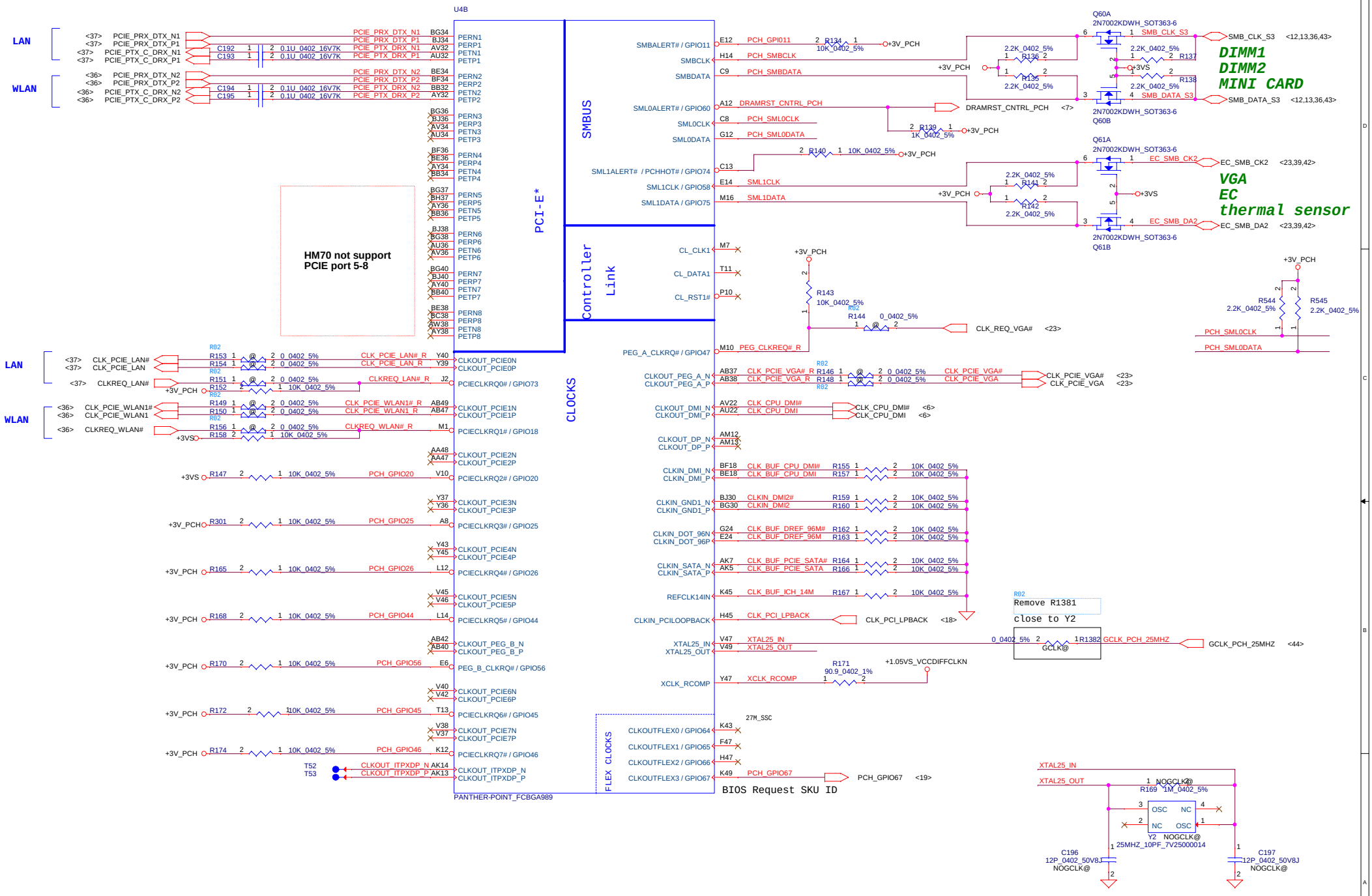
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
Custom	LA-9603P	1.0

Date: Wednesday, January 09, 2013 Sheet 14 of 62



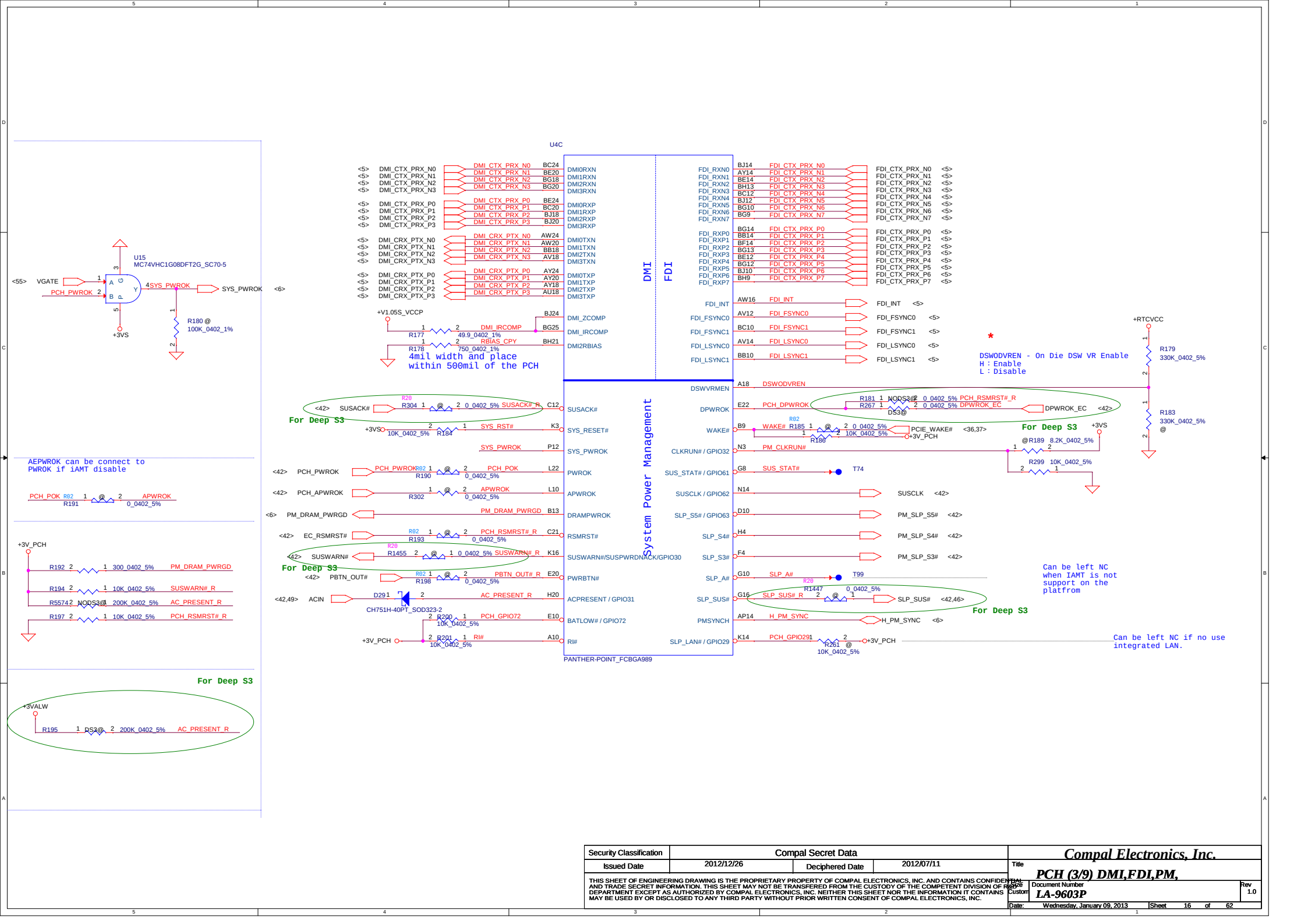
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-9603P	1.0

Date: Wednesday, January 09, 2013 Sheet 15 of 62



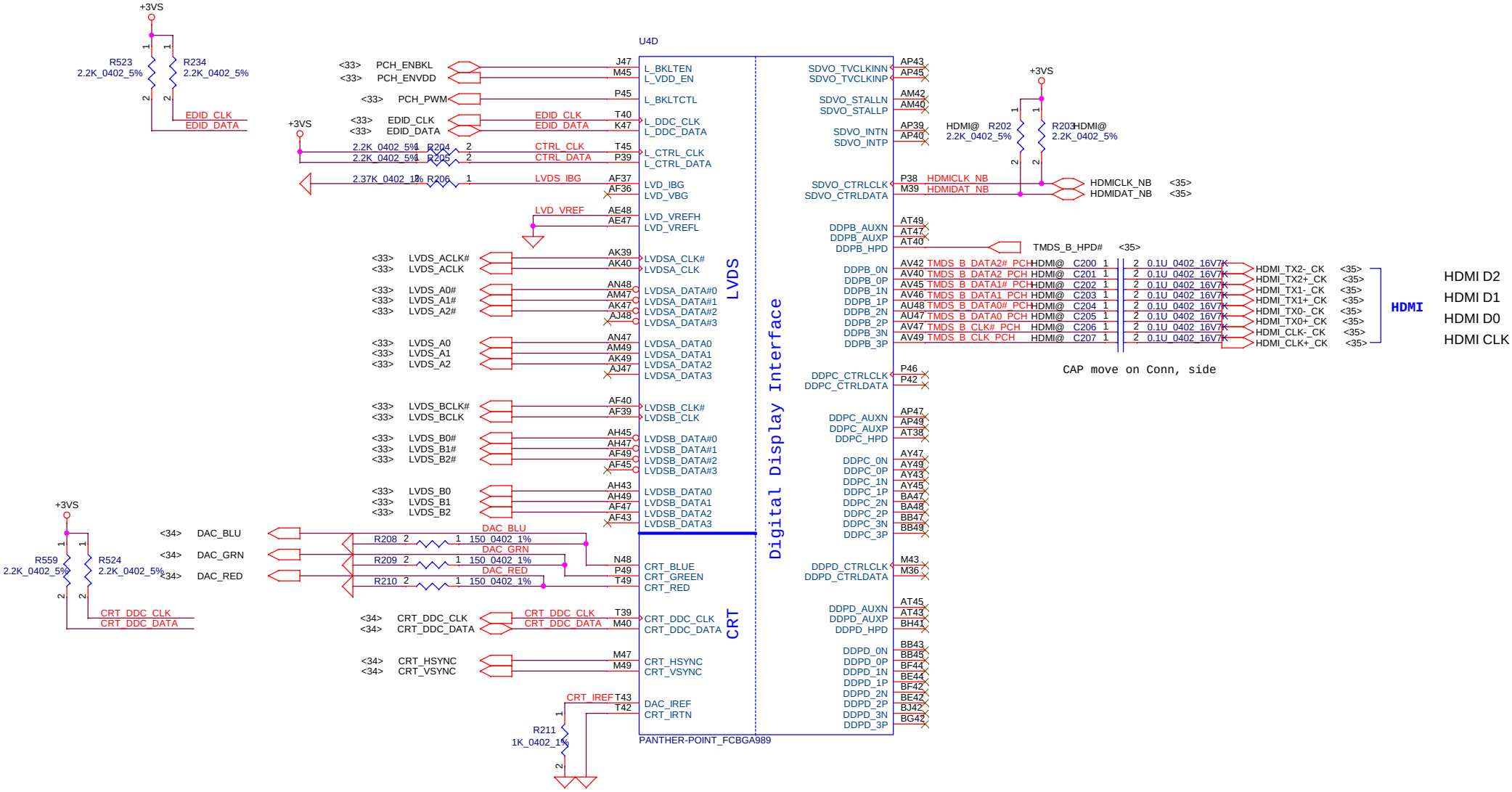
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size	Document Number	Rev
Custom	LA-9603P	1.0

Date: Wednesday, January 09, 2013 Sheet 16 of 62

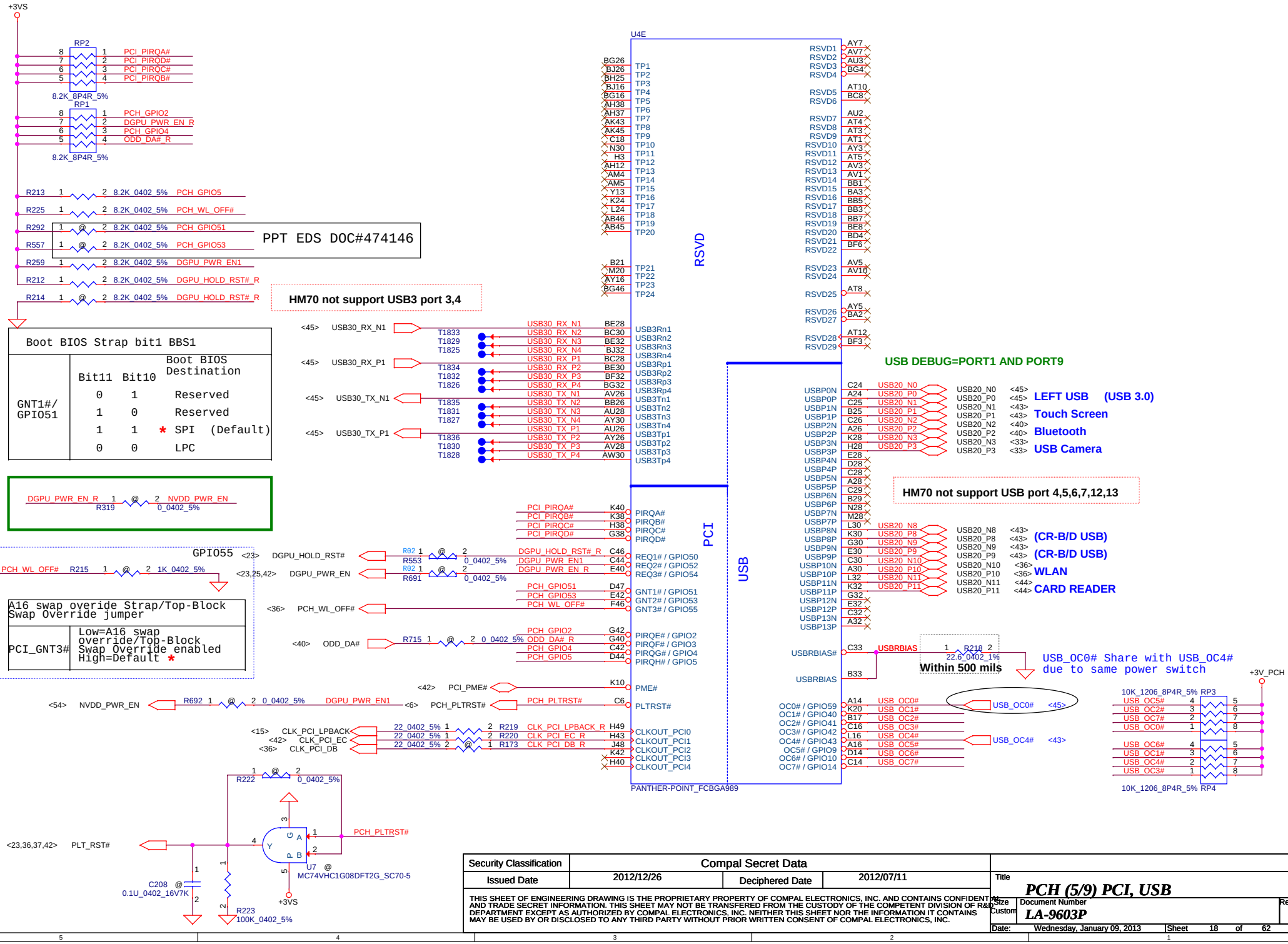


Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Title: **PCH (4/9) LVDS,CRT,DP,HDMI**

Size	Document Number	Rev
B	LA-9603P	1.0

Date: Wednesday, January 09, 2013 Sheet 17 of 62



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Title: **PCH (5/9) PCI, USB**

Size	Document Number	Rev
Custom	LA-9603P	1.0

Date: Wednesday, January 09, 2013 Sheet 18 of 62

PCH_GPIO69	Function
0	HM76 by PCH
1	HM70 by PCH

PCH_GPIO70	Function
0	UMA
1	N14P-GV2

+3V_PCH — Weak internal pull-high — R235 10K_0402_5% — EC_SMI#

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

R240 @ 1K_0402_5% — PCH_GPIO28

* Deep S4,S5 wake event signal
  RTC alarm,Power BTN,GPIO27

PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal

For DS3

+3VALW — DS3@ Q5530 — 10K_0402_5% — R245 @ 10K_0402_5% — PCH_GPIO27

+3VS — R244 @ 10K_0402_5% — PCH_GPIO37 — R881 10K_0402_5%

+3VS — R250 @ 10K_0402_5% — INTEL_BT_OFF# — R547 10K_0402_5%

BIOS Request SKU ID

+3VS — R711 UMA@ 10K_0402_5% — R246 10K_0402_5% UMA@ — PCH_GPIO38 — PCH_GPIO67 — PCH_GPIO67 <15>

OPT@ R709 10K_0402_5% — R293 10K_0402_5% OPT@

PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
1	1	UMA

+3VS — HM70@ R702 10K_0402_5% — PCH_GPIO69 — R707 HM76@ 10K_0402_5%

+3VS — GV2@ R703 10K_0402_5% — PCH_GPIO70 — R705 200K_0402_5% UMA@

U4F

+3VS — R233 10K_0402_5% — PCH_GPIO0 — T7 BMBUSY# / GPIO0
+3VS — R227 10K_0402_5% — PCH_GPIO1 — A42 TACH1 / GPIO1
+3VS — R228 10K_0402_5% — PCH_GPIO6 — H36 TACH2 / GPIO6
<42> EC_SCI# — EC_SCI# — E38 TACH3 / GPIO7
<42> EC_SMI# — EC_SMI# — C10 GPIO8
+3V_PCH — R229 @ 10K_0402_5% — PCH_GPIO12 — C4 LAN_PHY_PWR_CTRL / GPIO12
R230 1 2 1K_0402_5% — EC_LID_OUT# — G2 GPIO15
<42> EC_LID_OUT#
+3VS — R231 10K_0402_5% — <36> mSATA_DET# — mSATA_DET# — U2 SATA4GP / GPIO16
<46,54> DGPU_PWROK — R297 @ 0_0402_5% — R232 @ 10K_0402_1% — DGPU_PWROK_R — D40 TACH0 / GPIO17
PU on power side
+3VS — R238 10K_0402_5% — BT_DISABLE — T5 SCLOCK / GPIO22
<36> BT_DISABLE
<40> ODD_EN — ODD_EN — E8 GPIO24
PCH_GPIO27 — E16 GPIO27
<36,40> PCH_BT_ON# — +3V_PCH — R241 10K_0402_5% — PCH_GPIO28 — P8 GPIO28
+3VS — R242 10K_0402_5% — PCH_BT_ON# — K1 STP_PCI# / GPIO34
+3VS — R243 10K_0402_5% — PCH_GPIO35 — K4 GPIO35
<36> INTEL_BT_OFF# — INTEL_BT_OFF# — V8 SATA2GP / GPIO36
PCH_GPIO37 — M5 SATA3GP / GPIO37
PCH_GPIO38 — N2 SLOAD / GPIO38
+3VS — R247 10K_0402_5% — PCH_GPIO39 — M3 SDATAOUT0 / GPIO39
R248 10K_0402_5% — PCH_GPIO48 — V13 SDATAOUT1 / GPIO48
+3VS — R249 10K_0402_5% — PCH_GPIO49 — V3 SATA5GP / GPIO49 / TEMP_ALERT#
+3V_PCH — R251 10K_0402_5% — PCH_GPIO57 — D6 GPIO57

GPIO

TACH4 / GPIO68 — C40 — PCH_GPIO68 — 10K_0402_5% — R224 — +3VS
TACH5 / GPIO69 — B41 — PCH_GPIO69
TACH6 / GPIO70 — C41 — PCH_GPIO70
TACH7 / GPIO71 — A40 — PCH_GPIO71 — 10K_0402_5% — R704 — +3VS
R236 10K_0402_5% — +3VS
A20GATE — P4 — GATEA20 <42>
PECI — AU16
RCIN# — P5 — KBRST# — KBRST# <42>
PROCPWRGD — AY11 — H_CPUPWRGD <6>
THRMTRIP# — AY10 — PCH_THRMTRIP# R 1 — R239 390_0402_5% — 2 H_THRMTRIP# — H_THRMTRIP# <6>
PCH_THRMTRIP#_R <23>
INIT3_3V — T14
DF_TVS — AY1
INIT3_3V
This signal has weak internal PU,can't pull low
TS_VSS1 — AH8
TS_VSS2 — AK11
TS_VSS3 — AH10
TS_VSS4 — AK10
NC_1 — P37

KBRST# — R226 1 — 10K_0402_5% — +3VS

DMI Termination Voltage

NV_CLE	
	Set to Vcc when HIGH
	Set to Vss when LOW

+1.8VS — R216 2.2K_0402_5% — H_SNB_IVB# <6>
NV_CLE — R217 1K_0402_5%
Weak internal PU,Do not pull low
CLOSE TO THE BRANCHING POINT

CPU/MISC

NCTF

VSS_NCTF_1 — A4
VSS_NCTF_2 — A44
VSS_NCTF_3 — A45
VSS_NCTF_4 — A46
VSS_NCTF_5 — A5
VSS_NCTF_6 — A6
VSS_NCTF_7 — B3
VSS_NCTF_8 — B47
VSS_NCTF_9 — BD1
VSS_NCTF_10 — BD49
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE49
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF49
VSS_NCTF_15 — BG2
VSS_NCTF_16 — BG48
VSS_NCTF_17 — BH3
VSS_NCTF_18 — BH47
VSS_NCTF_19 — BJ4
VSS_NCTF_20 — BJ44
VSS_NCTF_21 — BJ45
VSS_NCTF_22 — BJ46
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ6
VSS_NCTF_25 — C2
VSS_NCTF_26 — C48
VSS_NCTF_27 — D1
VSS_NCTF_28 — D49
VSS_NCTF_29 — E1
VSS_NCTF_30 — E49
VSS_NCTF_31 — F1
VSS_NCTF_32 — F49

PANTHER-POINT_FCBGA989

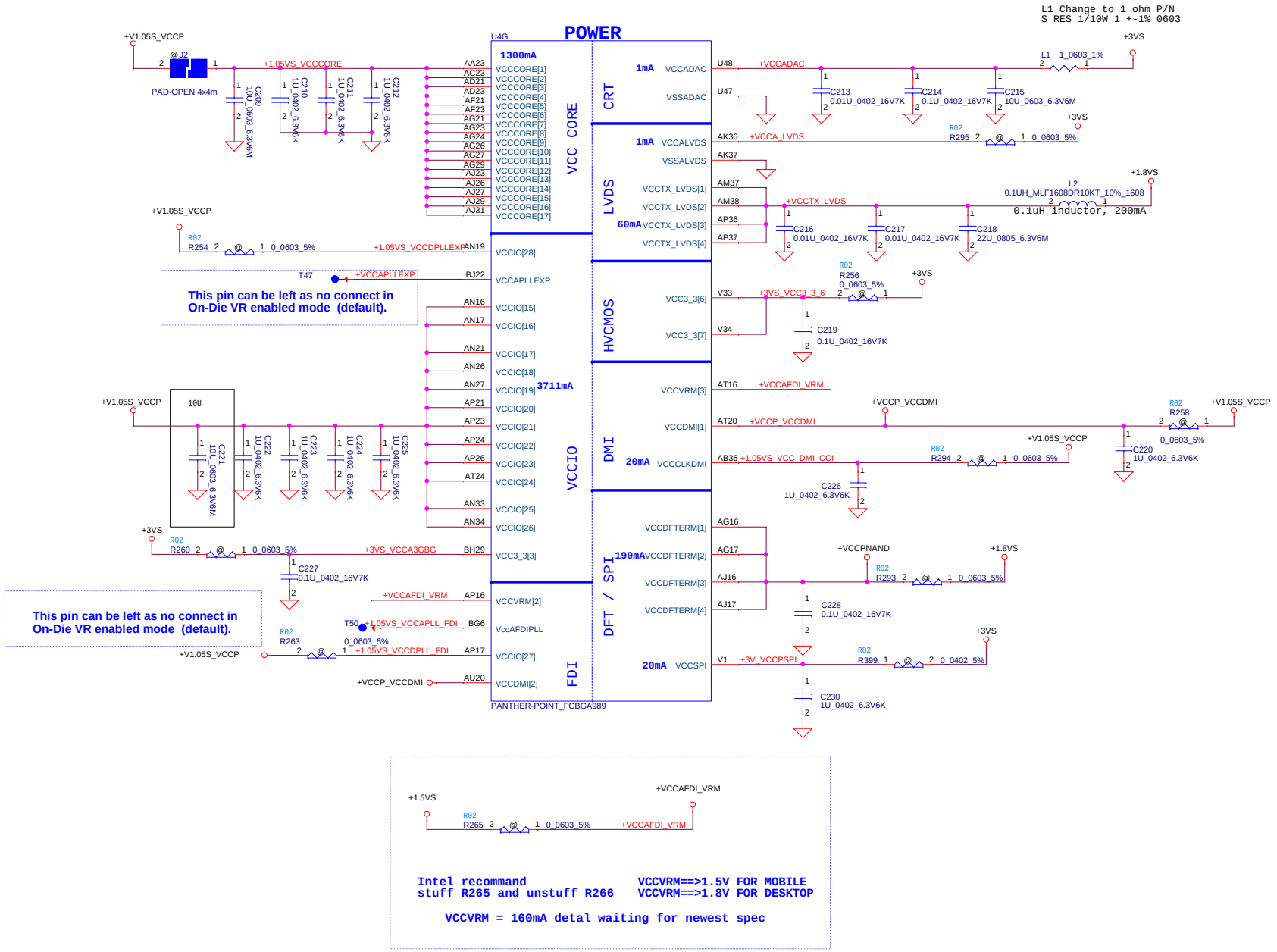
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-9603P | Rev: 1.0

Date: Wednesday, January 09, 2013 | Sheet 19 of 62



PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

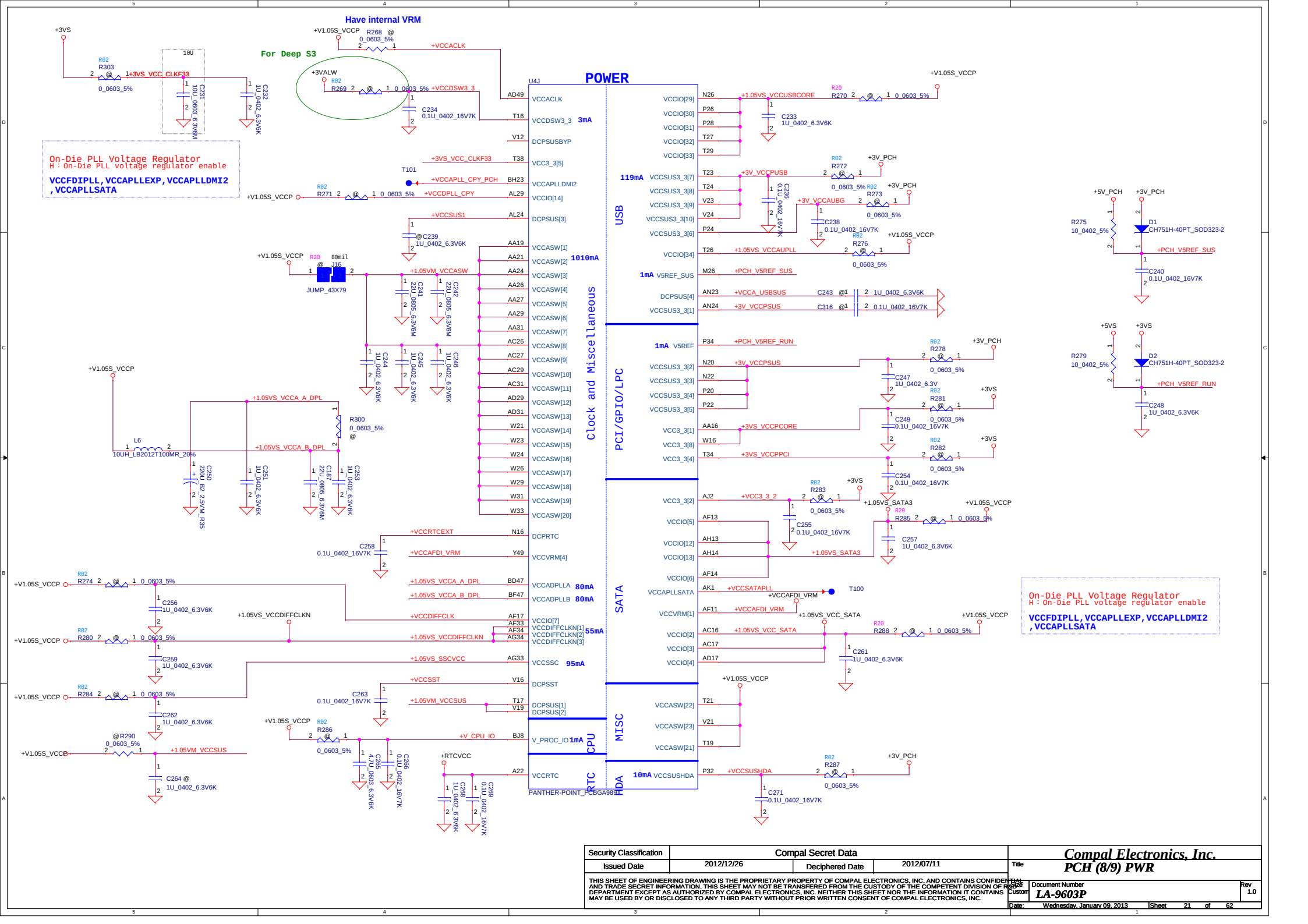
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

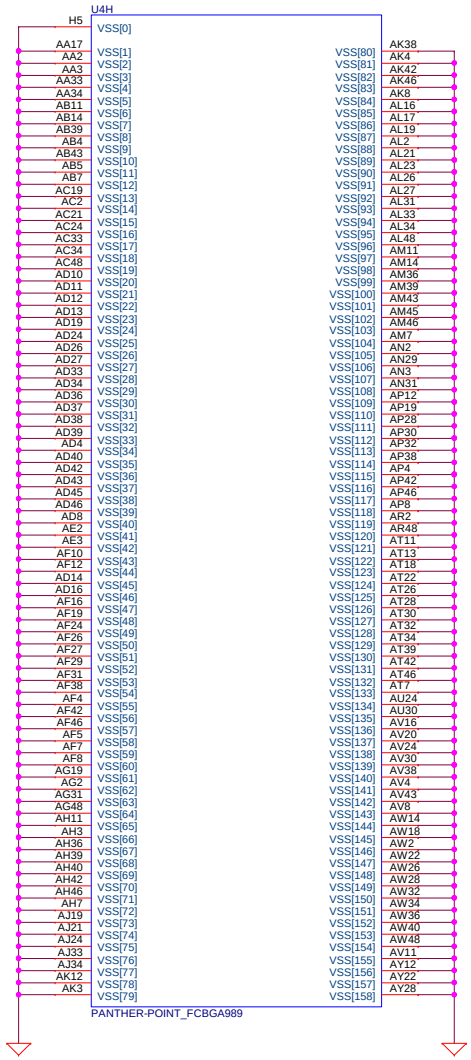
Size: Custom | Document Number: LA-9603P | Rev: 1.0

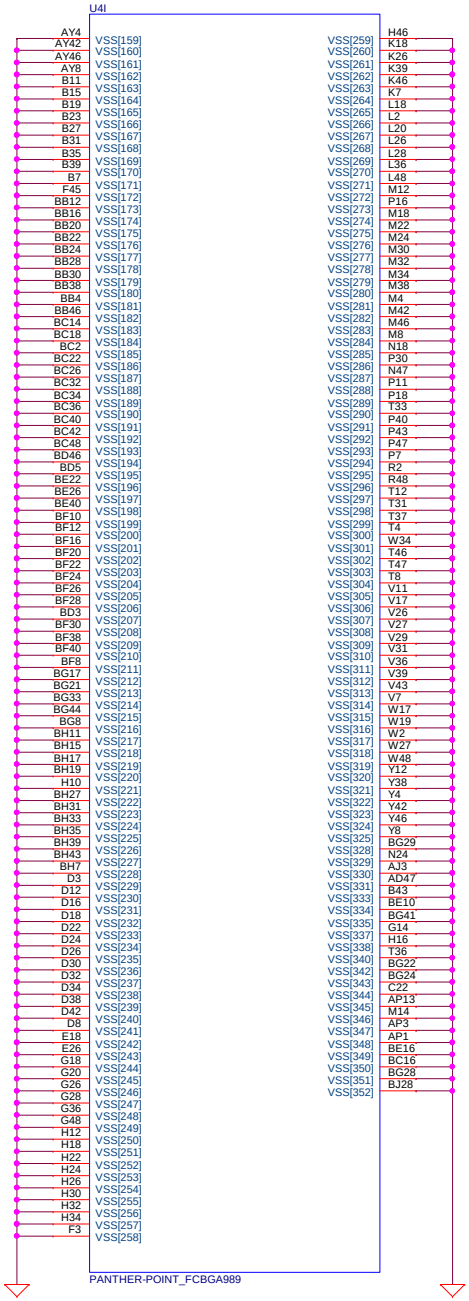
Date: Wednesday, January 09, 2013 | Sheet 20 of 62



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: PCH (8/9) PWR			
Size: Custom	Document Number: LA-9603P		Rev: 1.0
Date: Wednesday, January 09, 2013	Sheet 21 of 62		





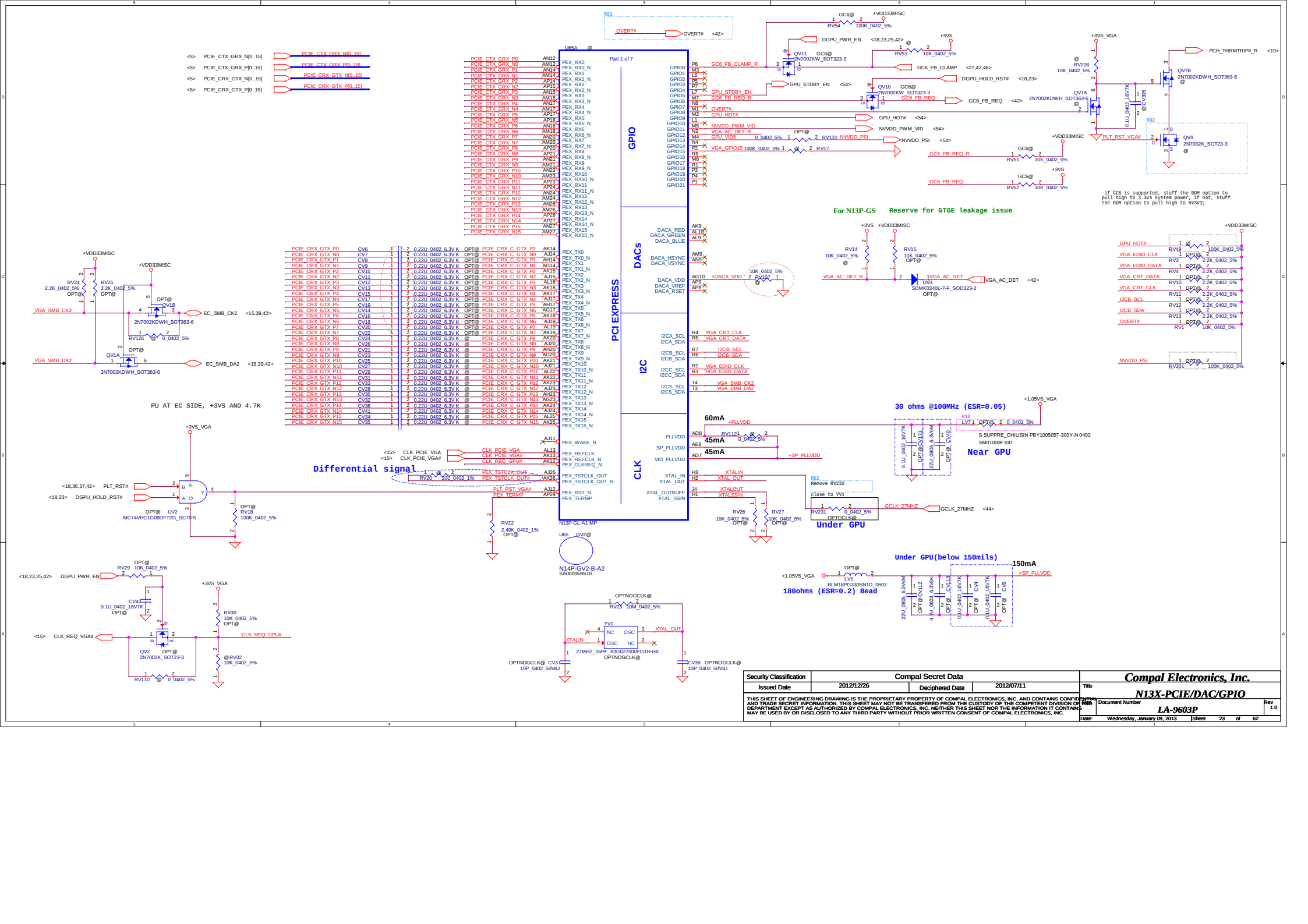
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: LA-9603P | Rev: 1.0

Date: Wednesday, January 09, 2013 | Sheet 22 of 62



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

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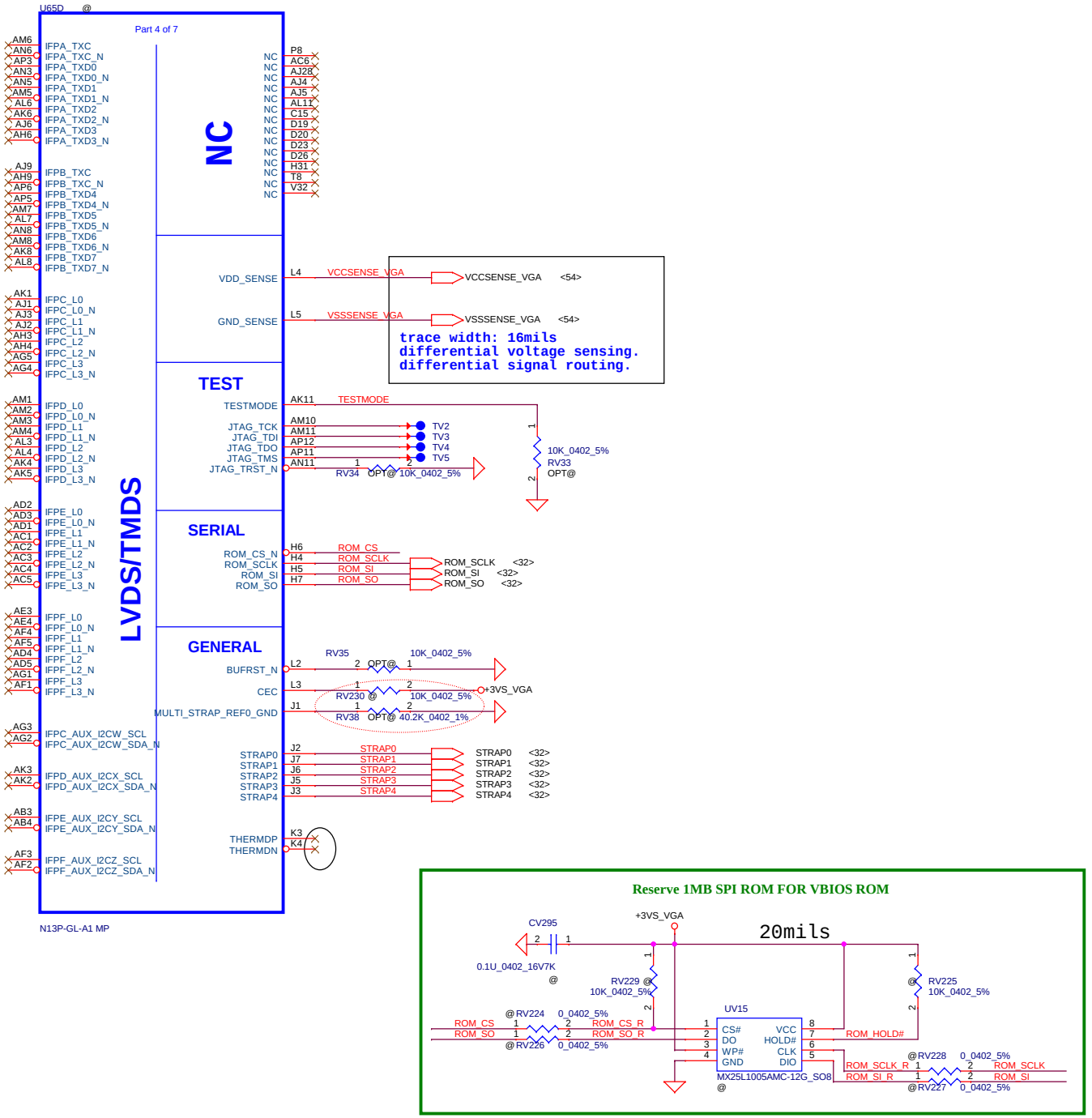
Compal Electronics, Inc.

Title: **N13X-PCIE/DAC/GPIO**

Document Number: **LA-9603P**

Rev: 1.0

Date: Wednesday, January 09, 2013 Sheet 23 of 62



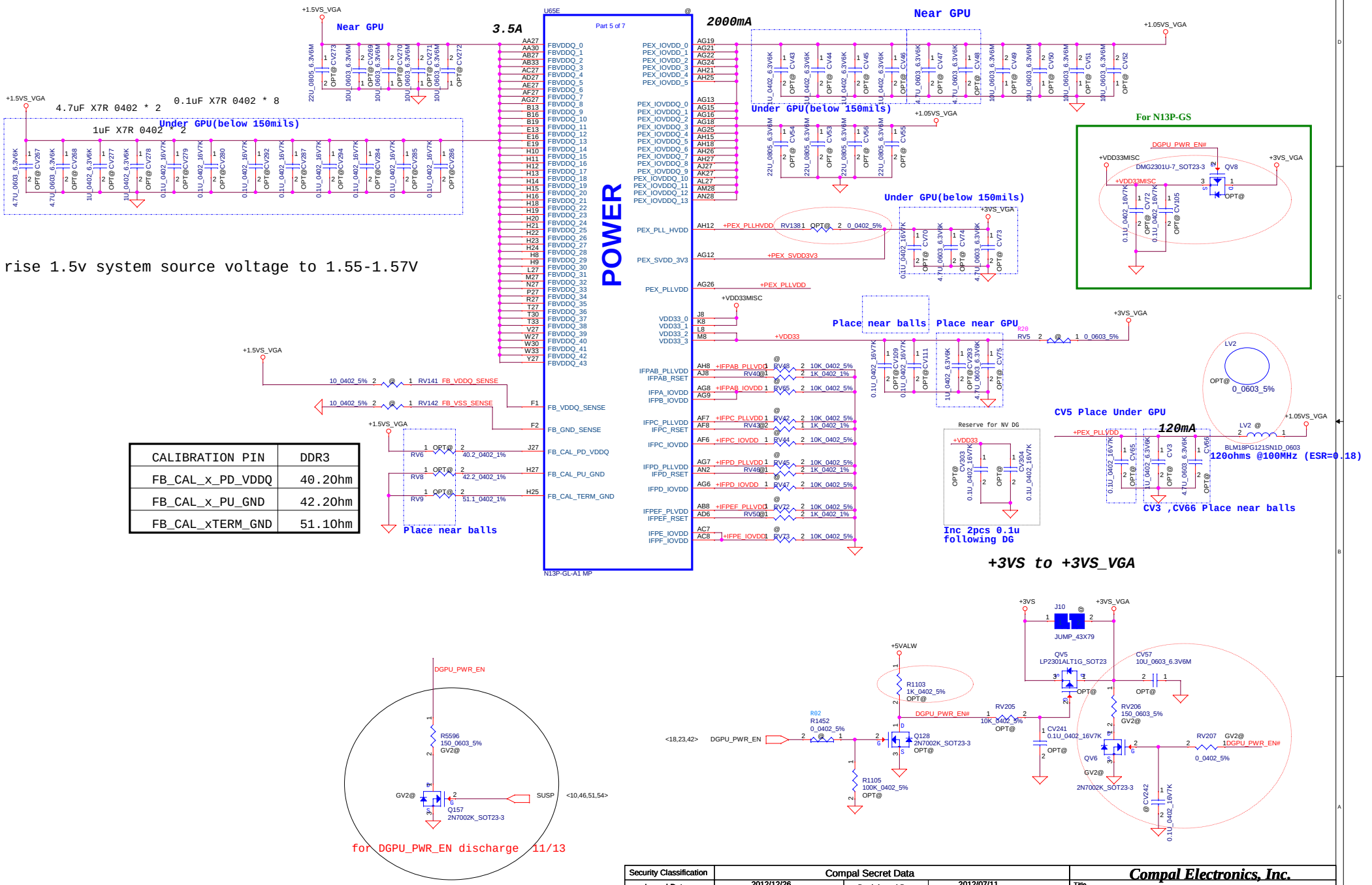
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13X-LVDS/HDMI/DP/THM**

Size	Document Number	Rev
	LA-9603P	1.0

Date: Wednesday, January 09, 2013 Sheet 24 of 62



CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.20hm
FB_CAL_x_PU_GND	42.20hm
FB_CAL_xTERM_GND	51.10hm

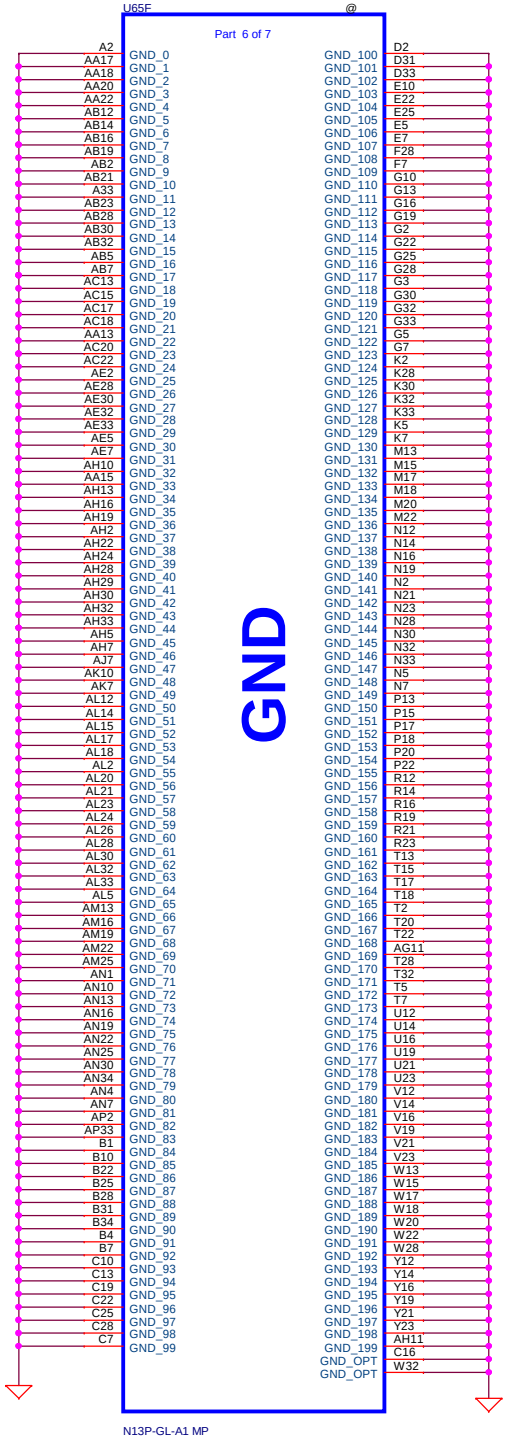
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

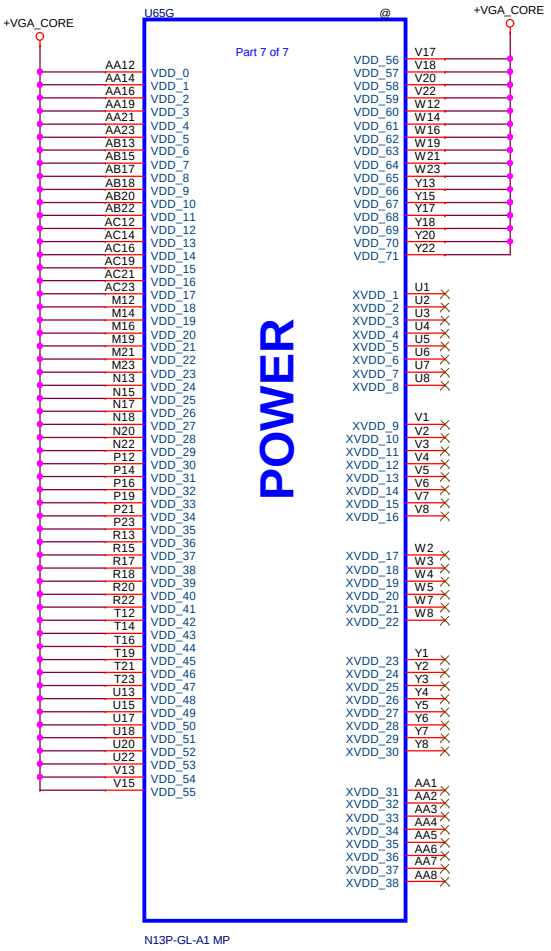
Compal Electronics, Inc.

Title: N13X-POWER

Size | Document Number: LA-9603P | Rev: 1.0

Date: Wednesday, January 09, 2013 | Sheet 25 of 62





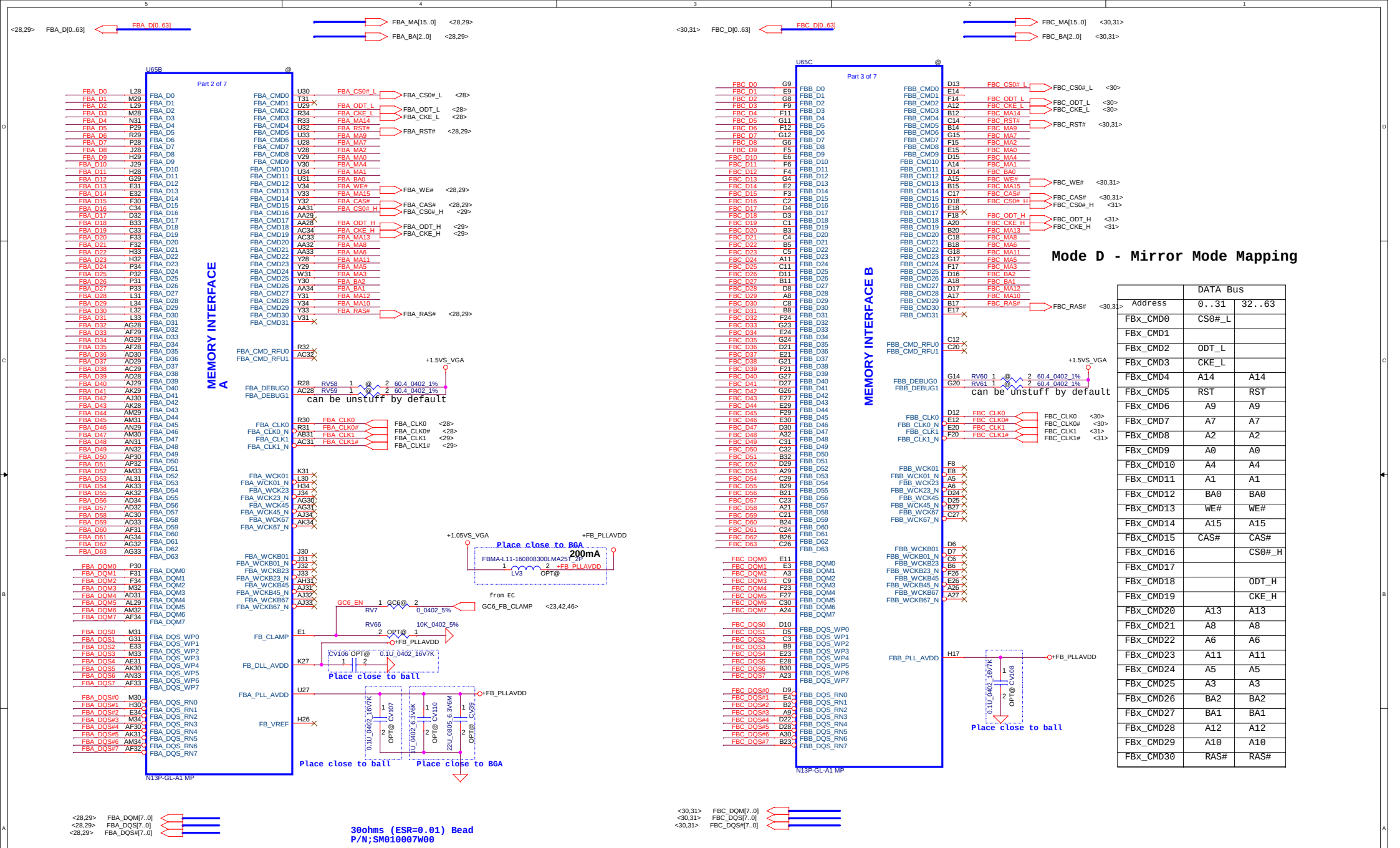
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13-VGA CORE, GND**

Size	Document Number	Rev
	LA-9603P	1.0

Date: Wednesday, January 09, 2013 Sheet 26 of 62



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

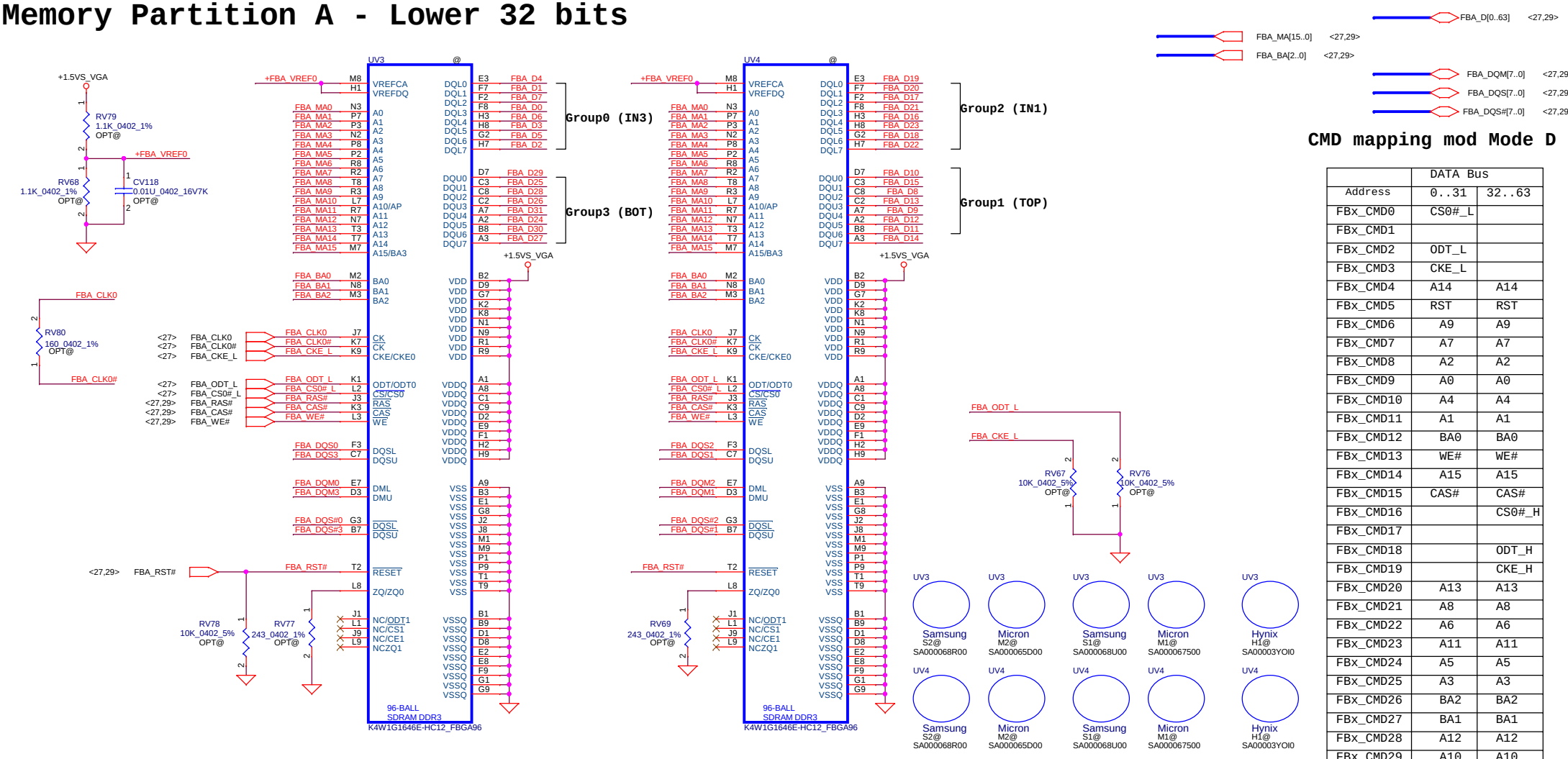
Compal Electronics, Inc.

Title: **N13X-MEM Interface**

Size	Document Number	Rev
	LA-9603P	1.0

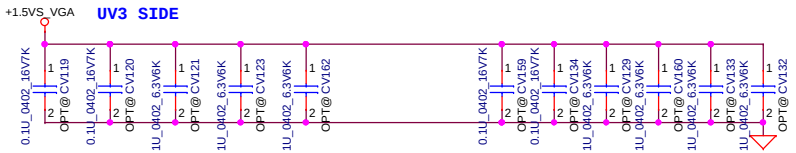
Date: Wednesday, January 09, 2013 | Sheet 27 of 62

Memory Partition A - Lower 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: N13X-VRAM A Lower

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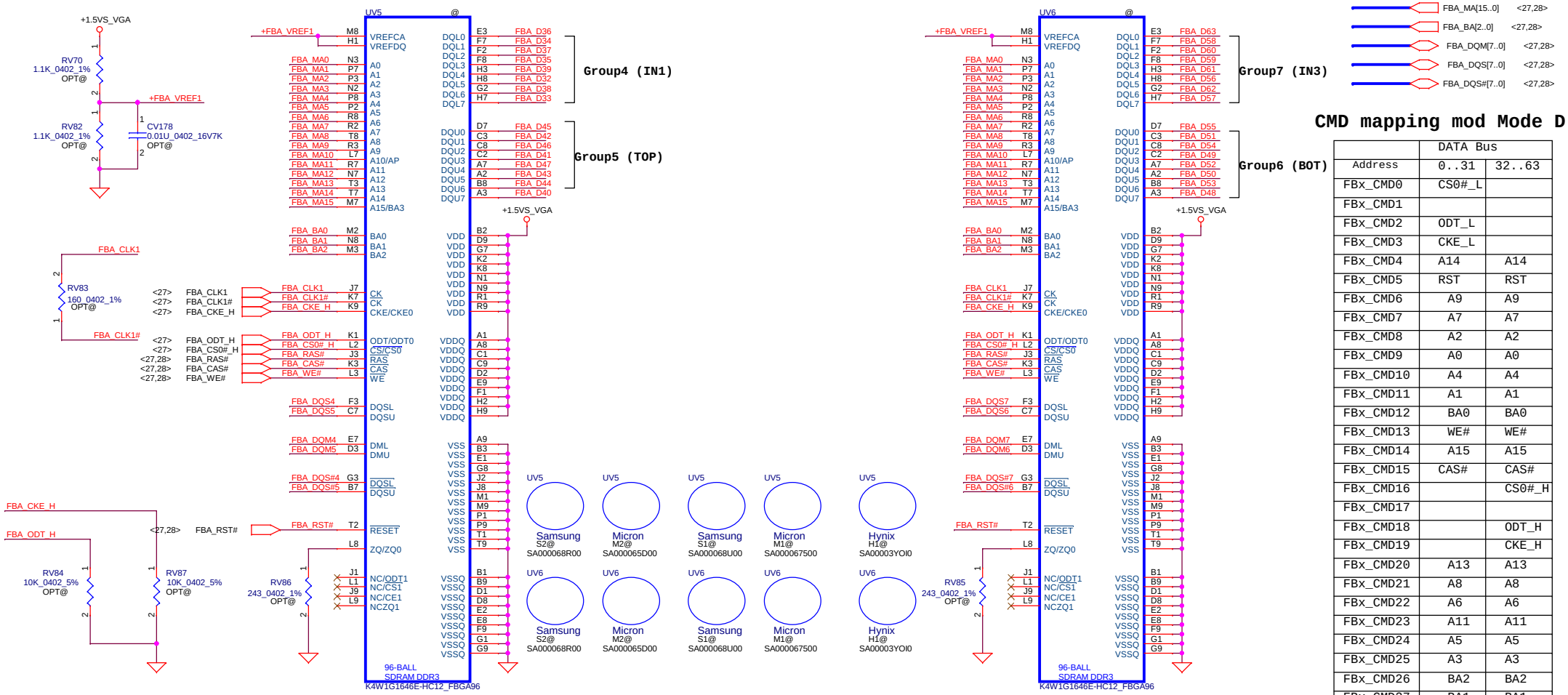
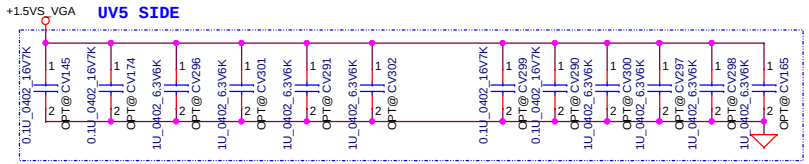
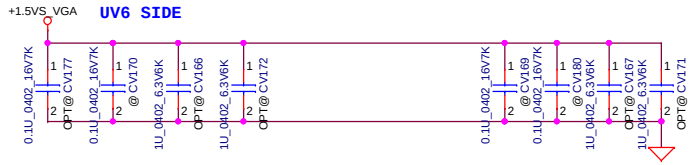
Memory Partition A - Upper 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **N13X-VRAM A Upper**

Size: | Document Number: **LA-9603P** | Rev: 1.0

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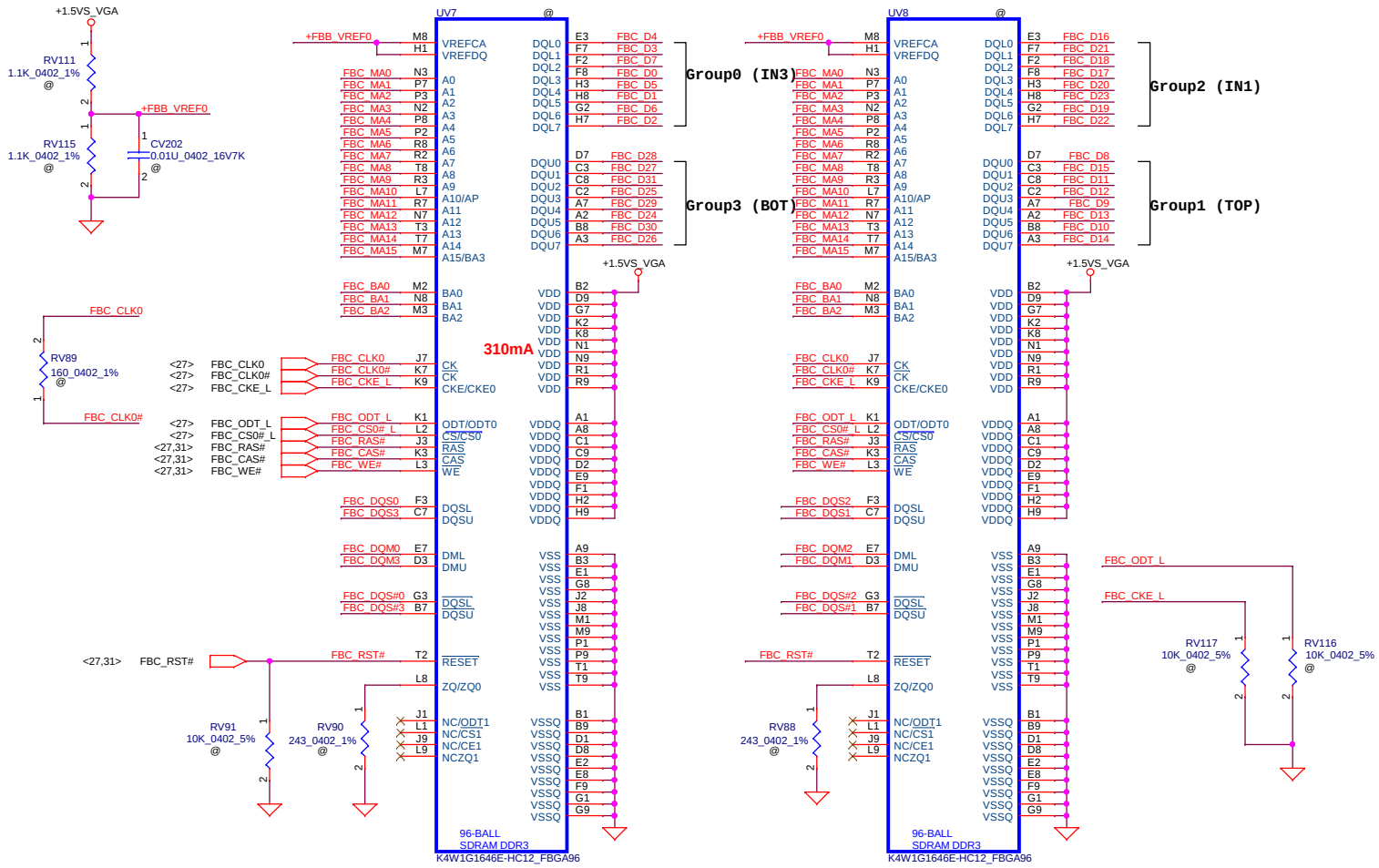
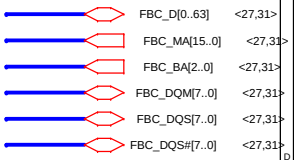
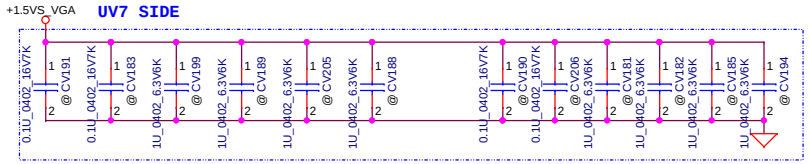
Memory Partition C - Lower 32 bits





CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13X-VRAM C Lower**

Size: Custom | Document Number: **LA-9603P** | Rev: 1.0

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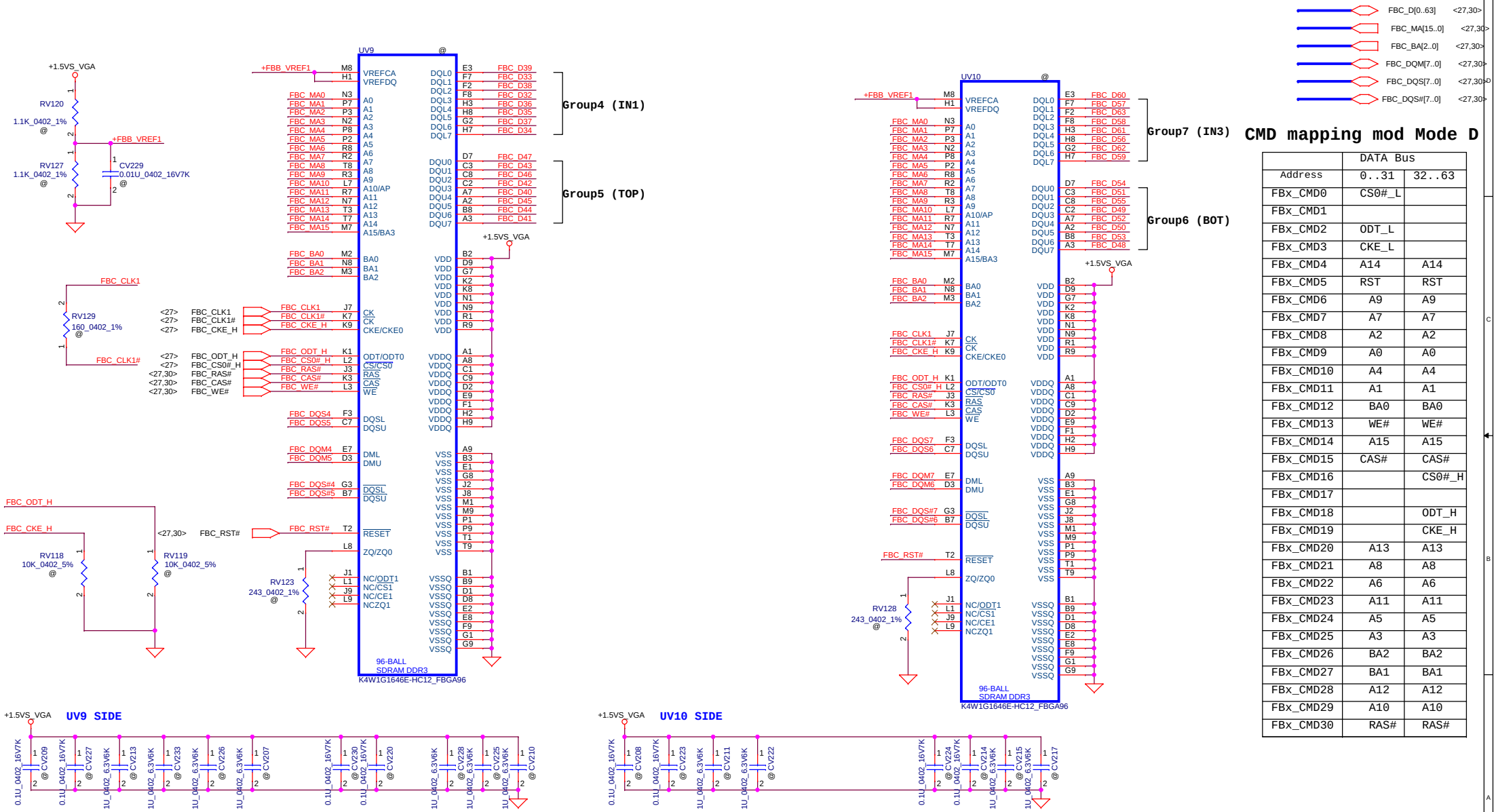
Memory Partition C - Upper 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **N13X-VRAM C Upper**

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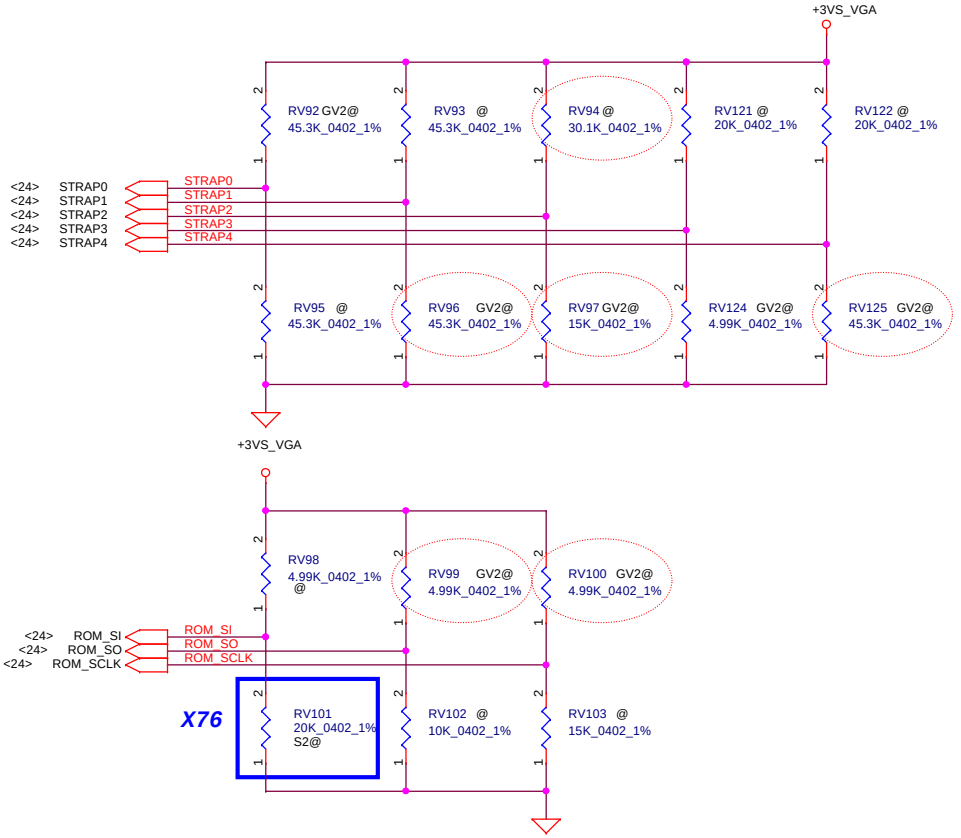


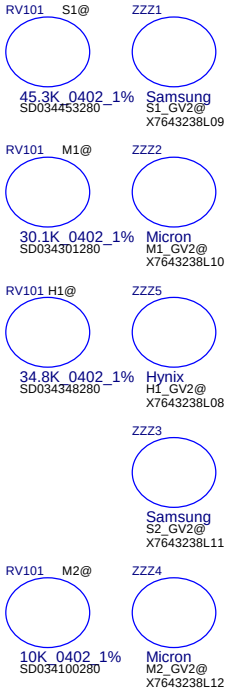
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Vendor	VRAM Sturcture
Samsung 2G	S2@
Micron 2G	M2@
Samsung 1G	S1@
Micron 1G	M1@

Table 3. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-N0C	1000	N/A	Production Candidate
				H5TQ2G63DFR-11C	900	N/A	Production Candidate
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production Candidate



SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG

3GIO_PADCFG[3:0]	
0110	Notebook Default

FB_0_BAR_SIZE

0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

USER Straps

User[3:0]	
1000-1100	Customer defined

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

XCLK_417

0	277MHz (Default)
1	Reserved

PCIE_MAX_SPEED

0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

VGA_DEVICE

0	3D Device (Class Code 302h)
1	VGA Device (Default)

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Compal Electronics, Inc.

Title: N13X_MISC

Size	Document Number	Rev
Custom	LA-9603P	1.0

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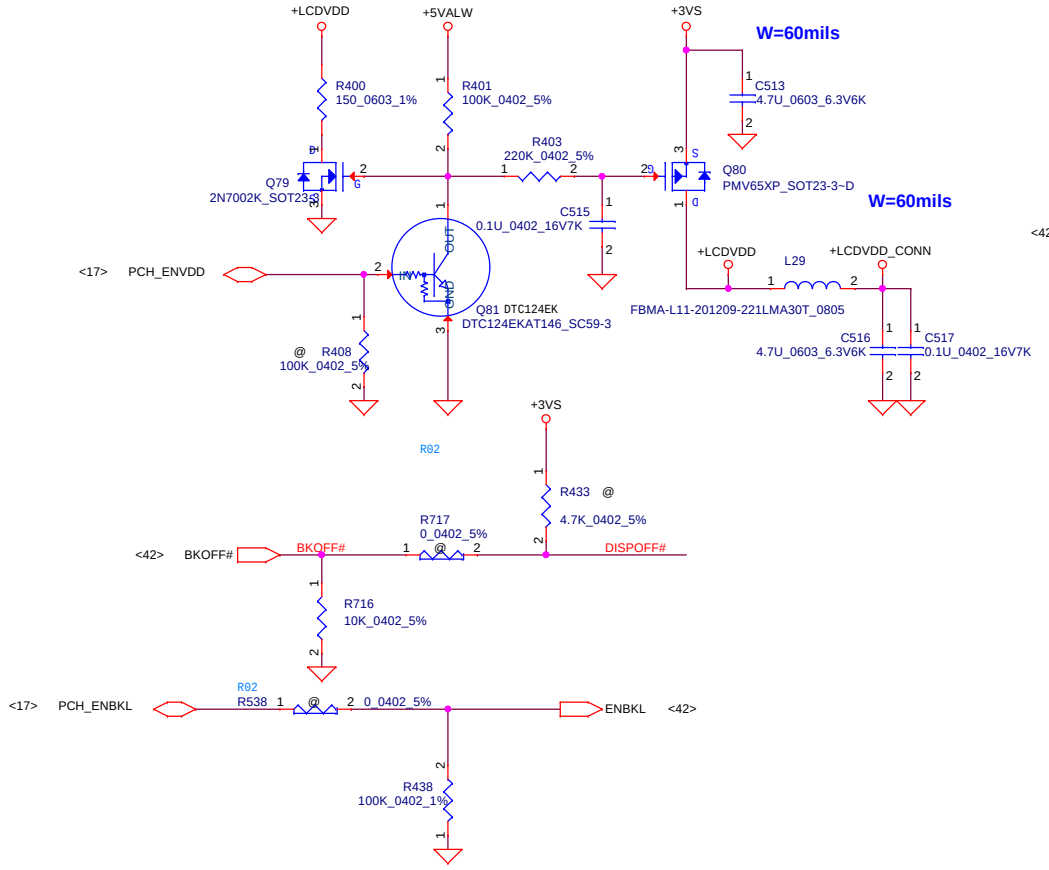
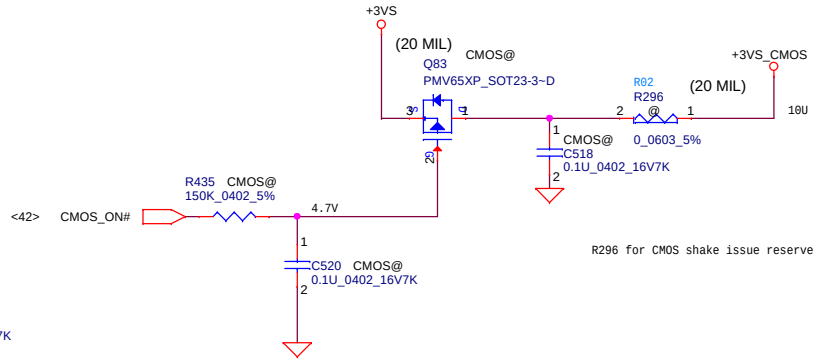
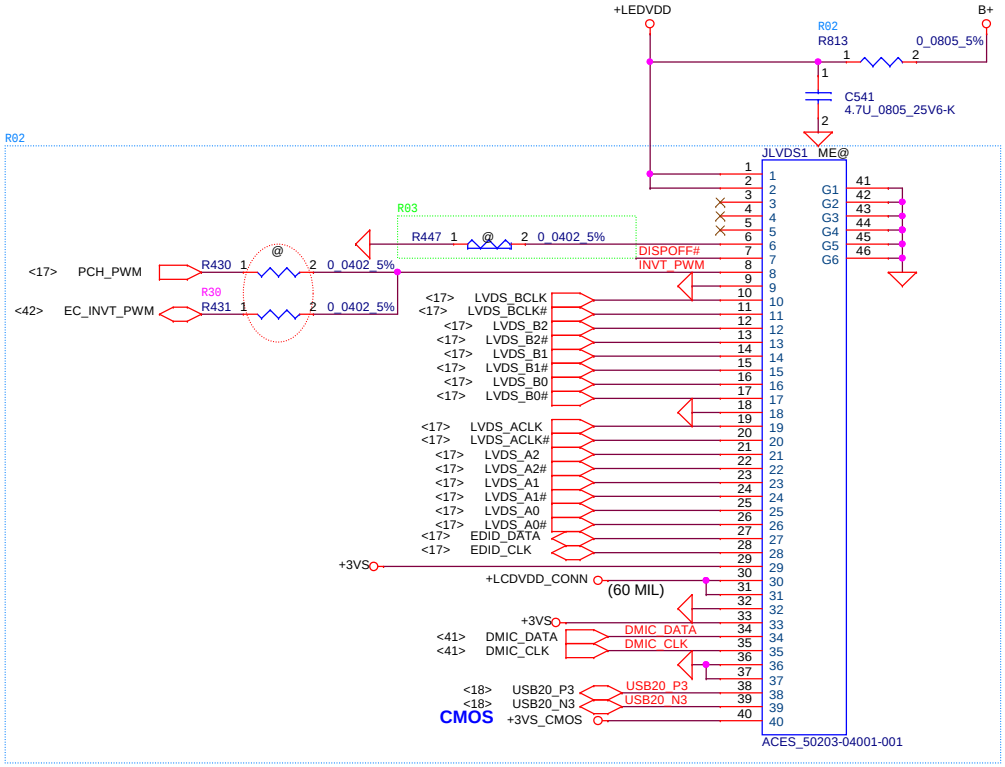
LCD POWER CIRCUIT



CMOS Camera



VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LVDS/CAMERA

Size	Document Number	Rev
Custom	LA-9603P	1.0

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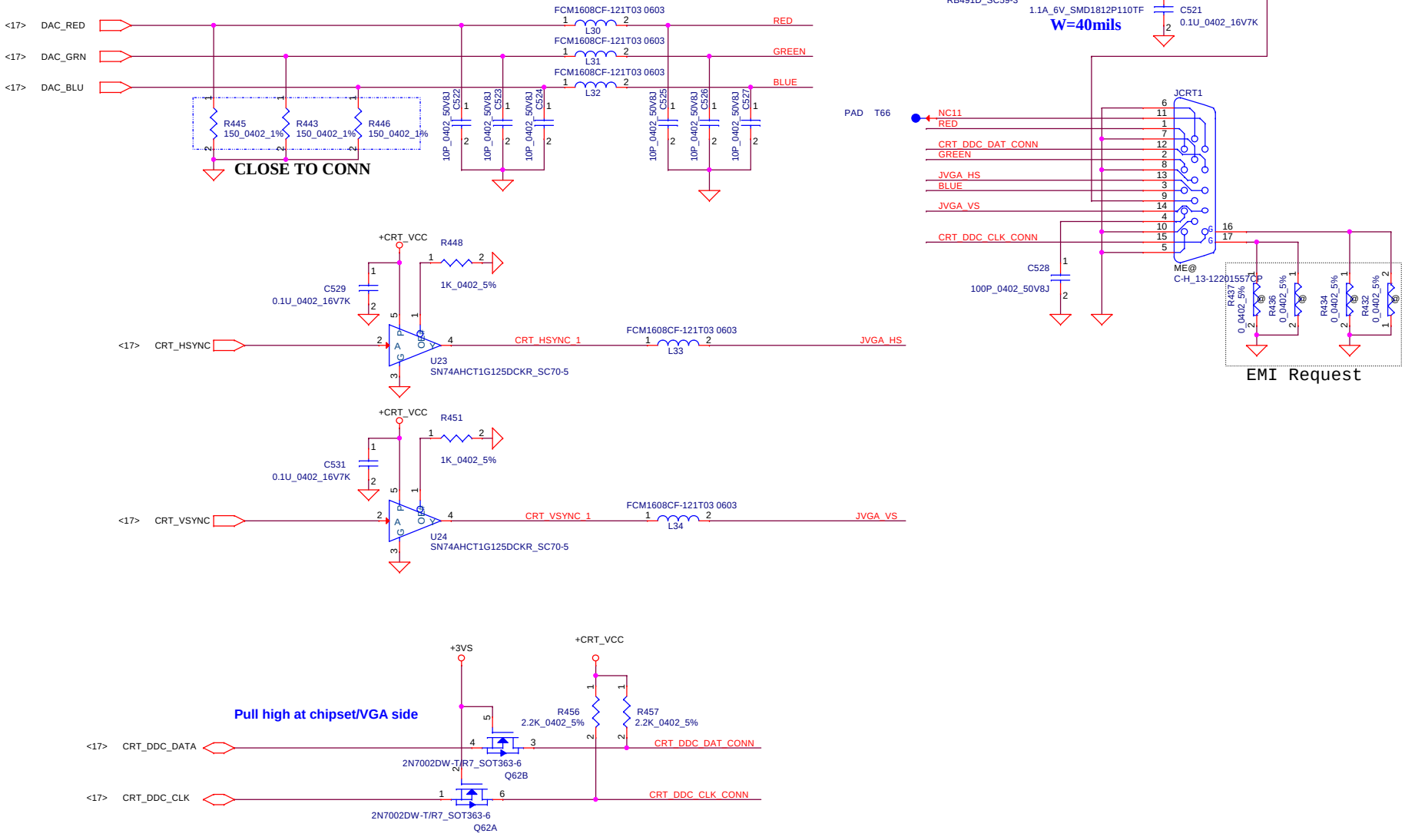
CRT Connector



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	LA-9603P	1.0

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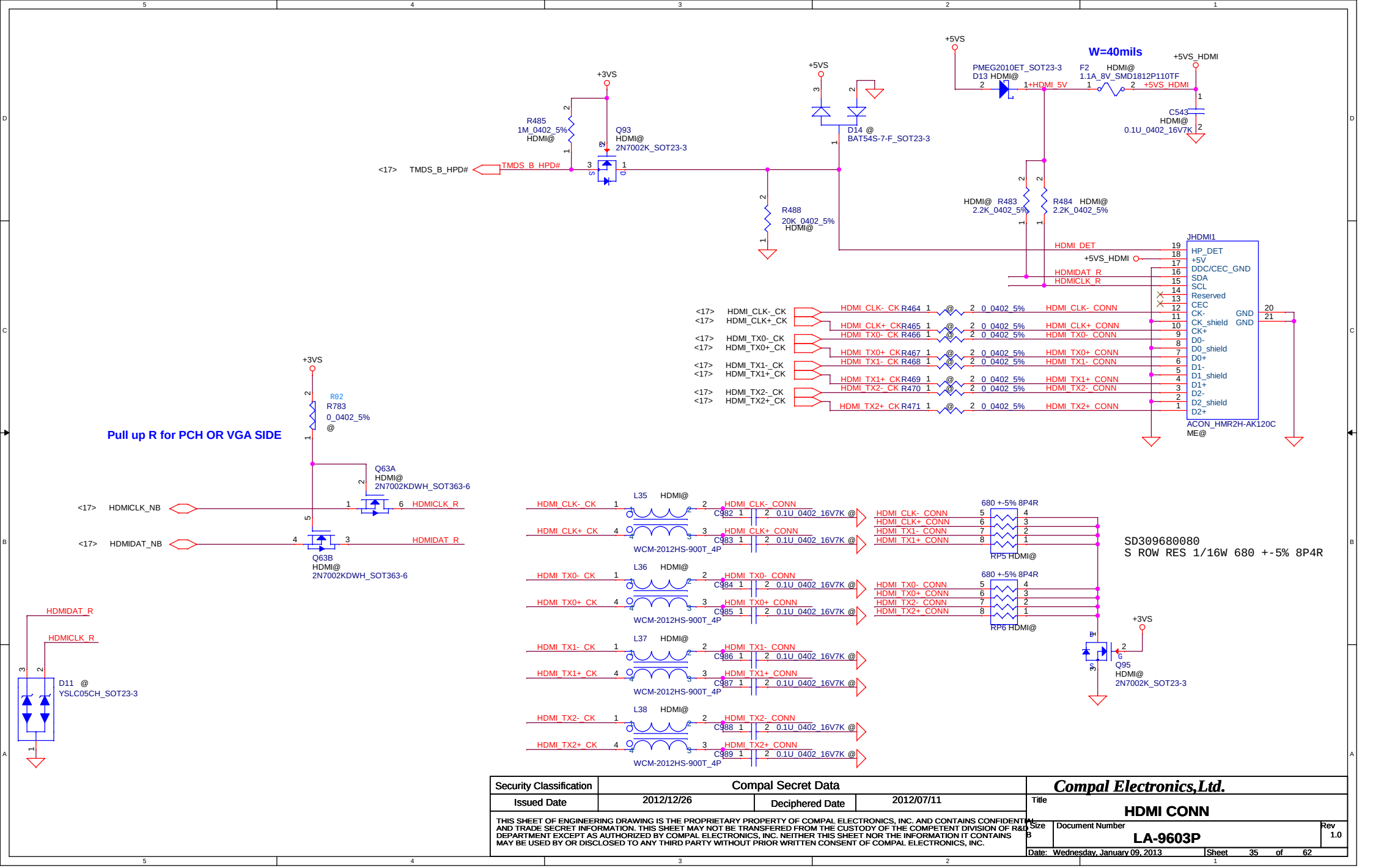

Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
B	LA-9603P	1.0

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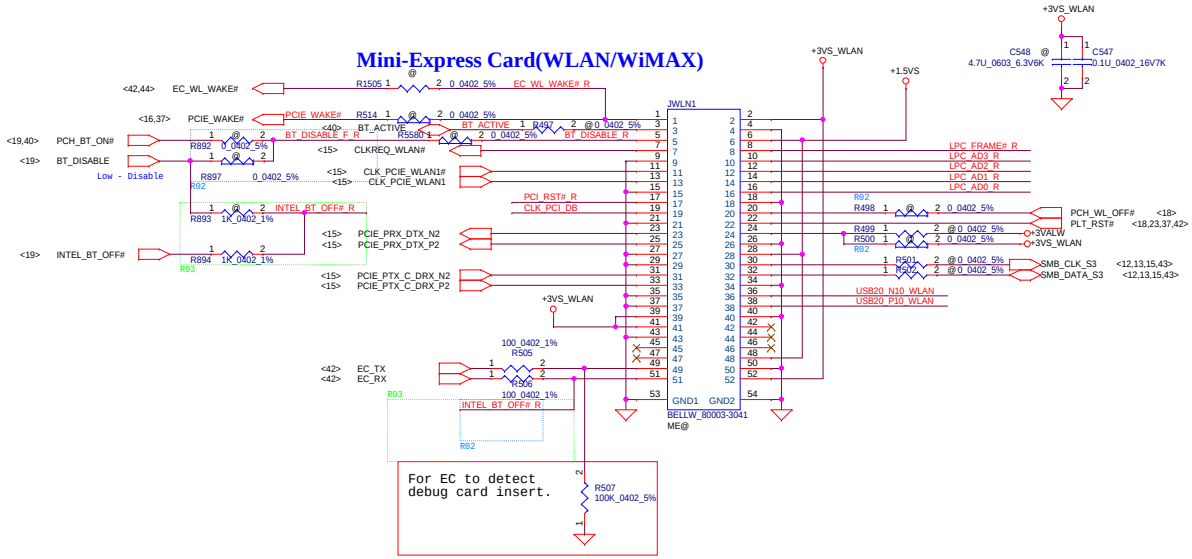
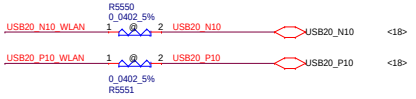
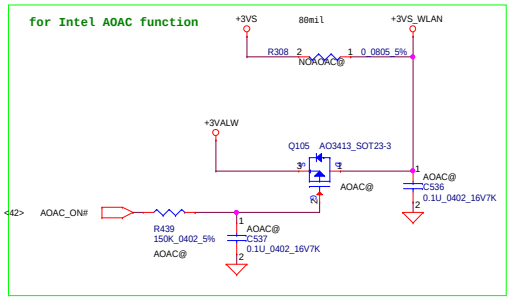
Mini-Express Card for WLAN/WiMAX(Half)

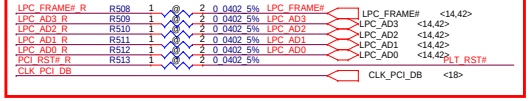


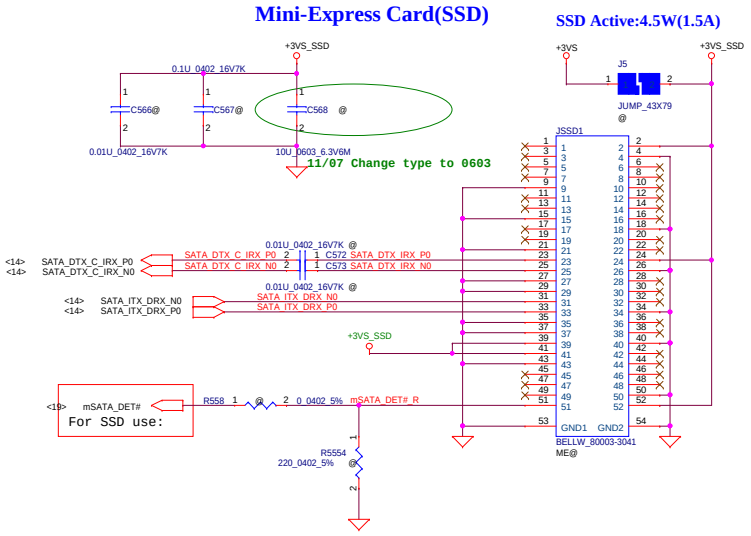


for Intel AOAC function Reserved



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.





Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

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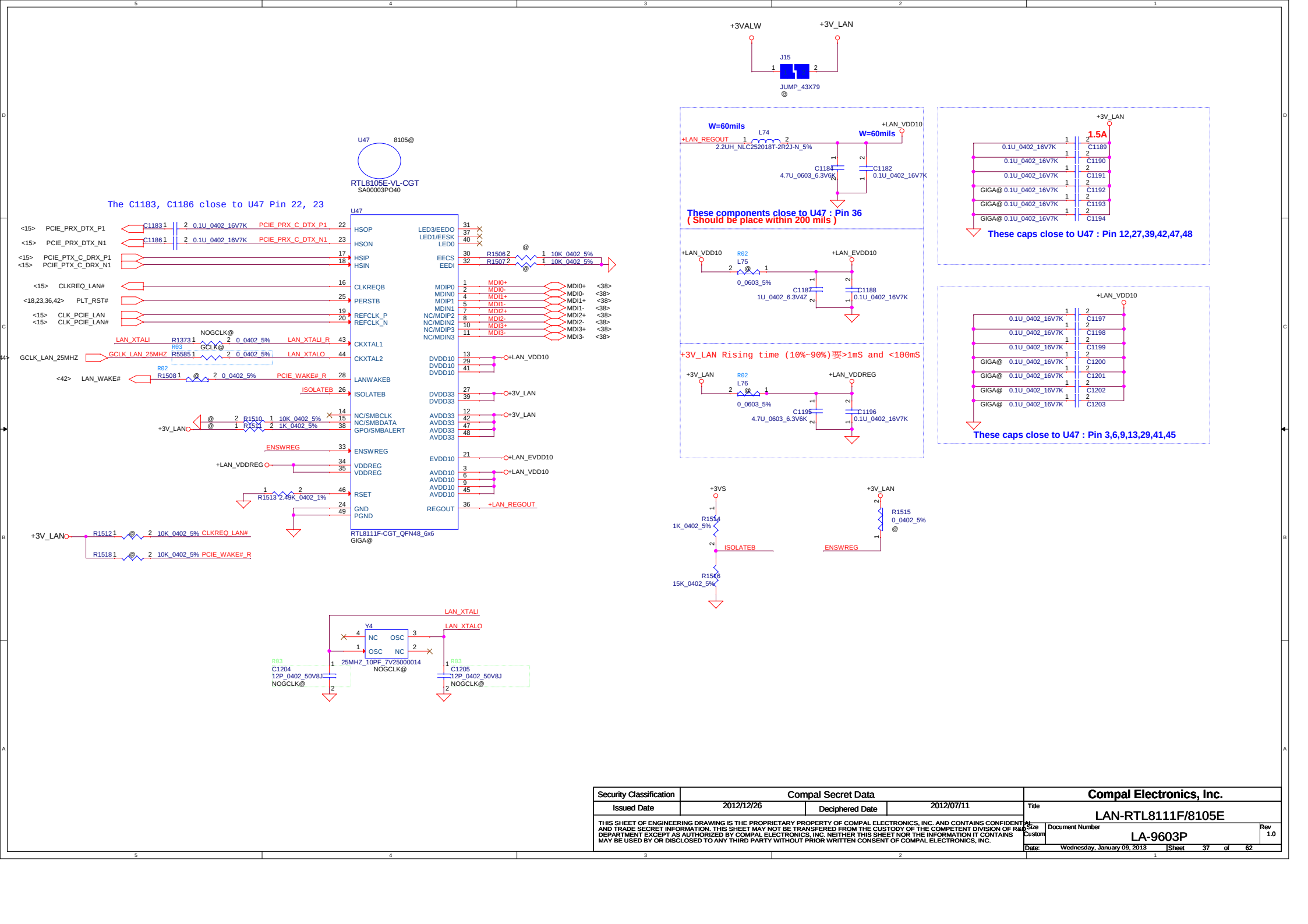
Compal Electronics, Inc.

Title: Mini-Card/NEW Card/SIM

Size	Document Number	Rev
	LA-9603P	1.0

Date: Wednesday, January 09, 2013 Sheet 36 of 62



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

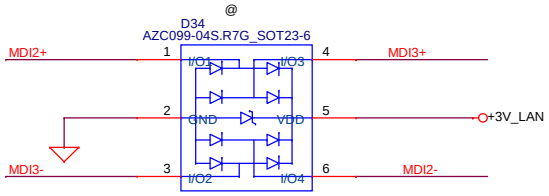
Compal Electronics, Inc.

Title: LAN-RTL8111F/8105E

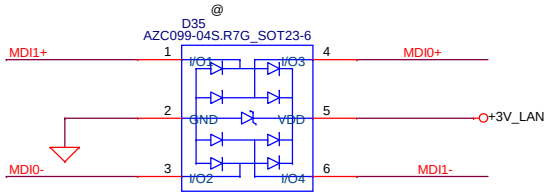
Size: Custom | Document Number: LA-9603P | Rev: 1.0

Date: Wednesday, January 09, 2013 | Sheet 37 of 62

Reserve gas tube for EMI go rural solution

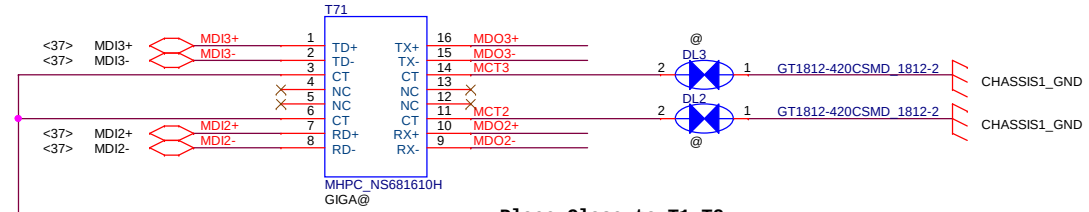


Place Close to T71

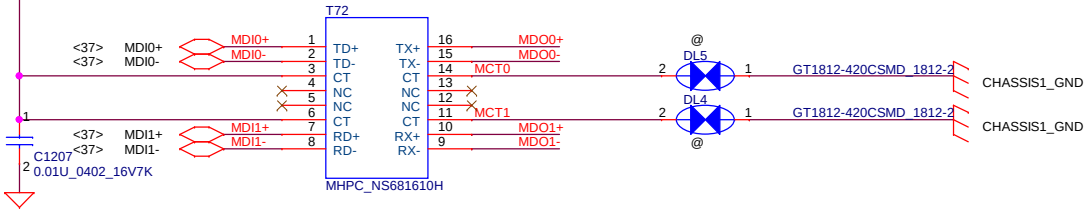


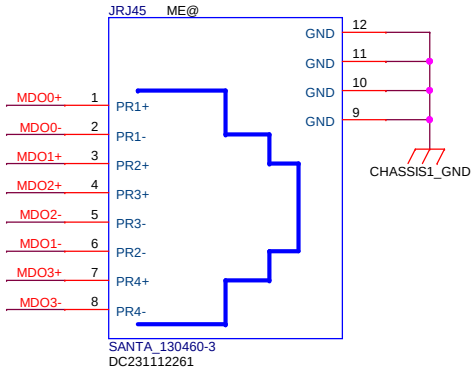
Place Close to T72

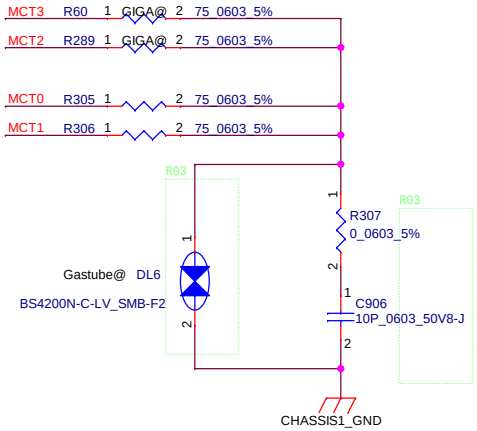
D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00

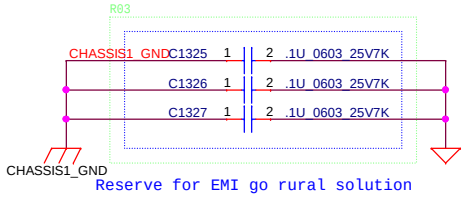


Place Close to T1,T2









Reserve for EMI go rural solution

Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN_Transformer

Size	Document Number	Rev
B	LA-9603P	1.0

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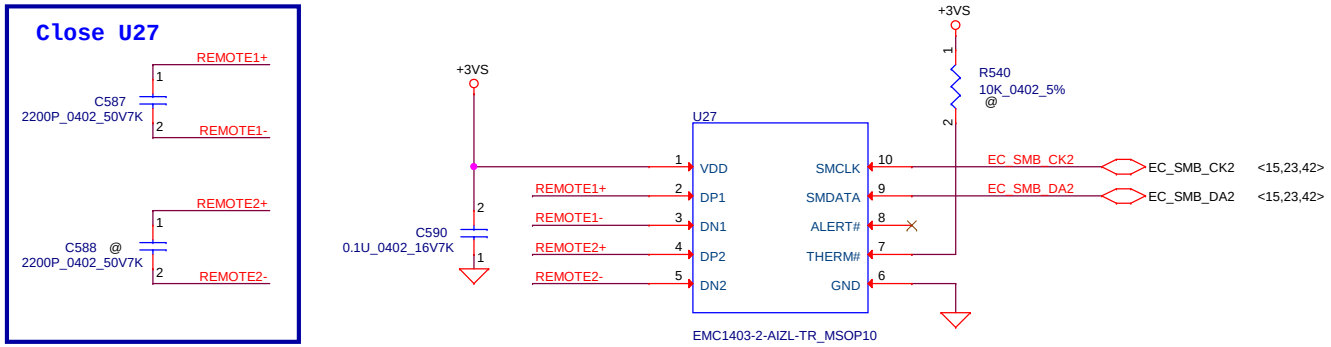
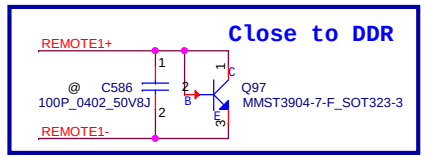
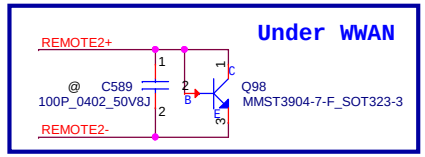
SMSC thermal sensor placed near by VRAM

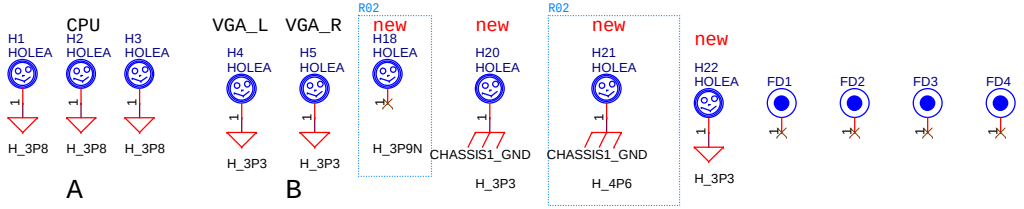


Address 1001_101xb

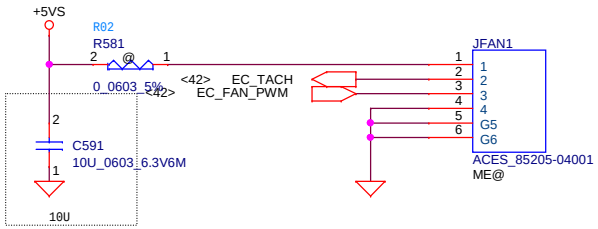


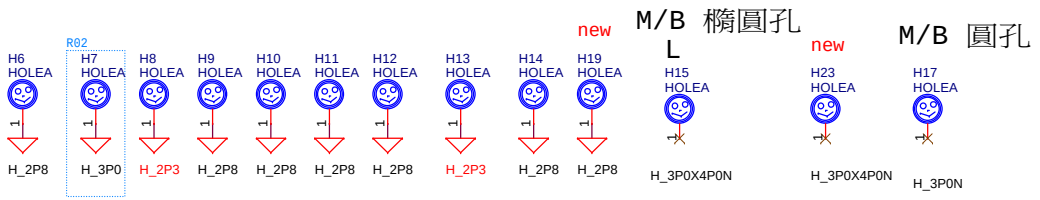


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



FAN1 Conn





2P8 * 7 pcd

Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

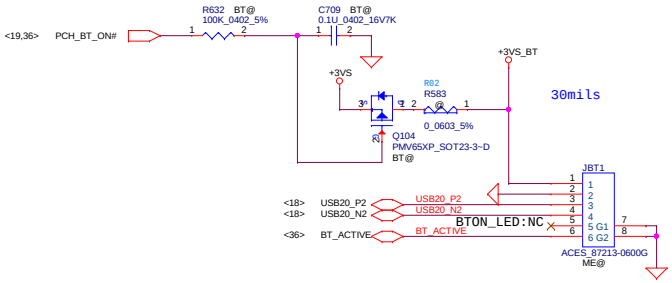
Compal Electronics,Ltd.

Title: **Fintek-Thermal IC/FAN/screw**

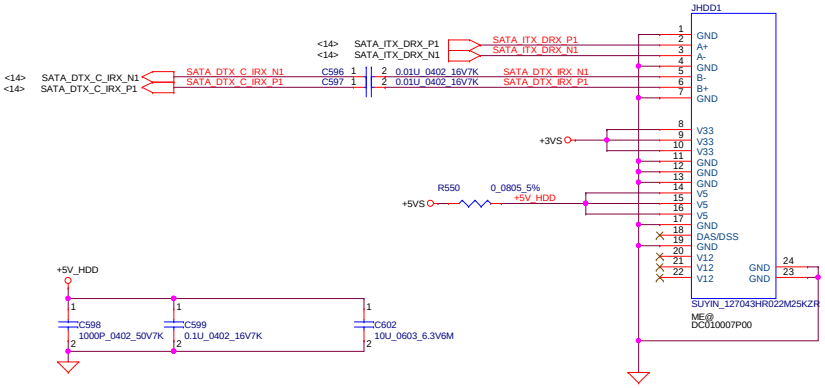
Size: B | Document Number: **LA-9603P** | Rev: 1.0

Date: Wednesday, January 09, 2013 | Sheet 39 of 62

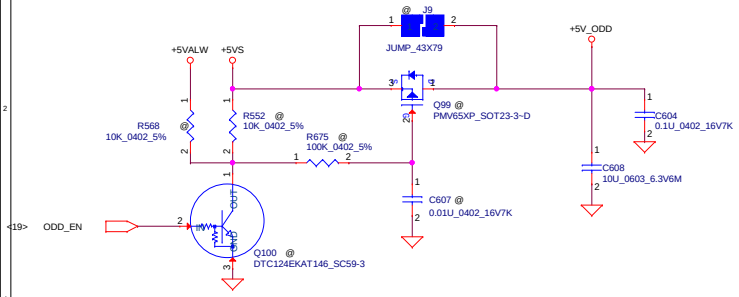
BT MODULE CONN



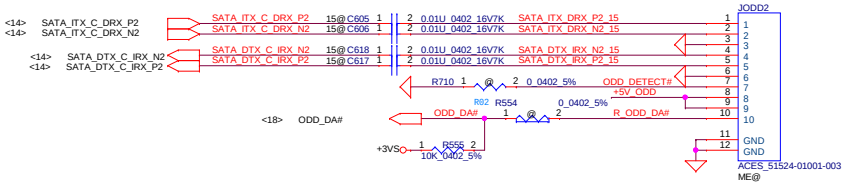
SATA HDD Conn.

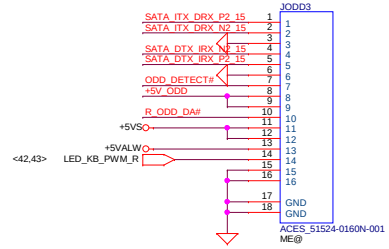


ODD Power Control

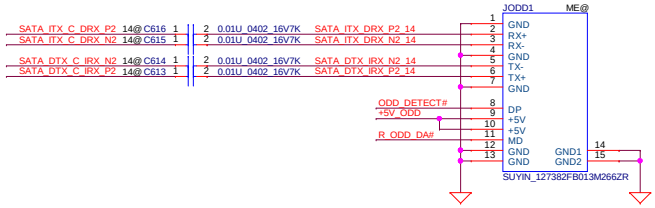


FOR 15"
SATA ODD FFC Conn.





Co-lay
FOR 14"
SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size	Document Number	Rev
Custom	LA-9603P	1.0

Date: Wednesday, January 09, 2013 Sheet 40 of 62

600ohms @100MHz 1A
P/N: SM01000BU00

600ohms @100MHz 2A
P/N: SM01000EE00

Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage

Vendor recommend. 2.2K

Vendor recommend. 2.2u

Placement near Audio Codec

Head Phone Woofer

MIC Sense
R939 place near pin13

Capless HP Sense
R940 place near pin34

Internal Speaker

Headphone

external MIC

Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

wide 25MIL

SPK L+L-R+R- trace width
Speaker 4 ohm ==>40 mils
Speaker 8 ohm ==>20 mils

Combo Jack detect (normal open)

R1123,C1134
Close to U50.47

R1559 and C1135
R5582
Close to U73.1

PC Beep

EMI

Reserve for ESD request.

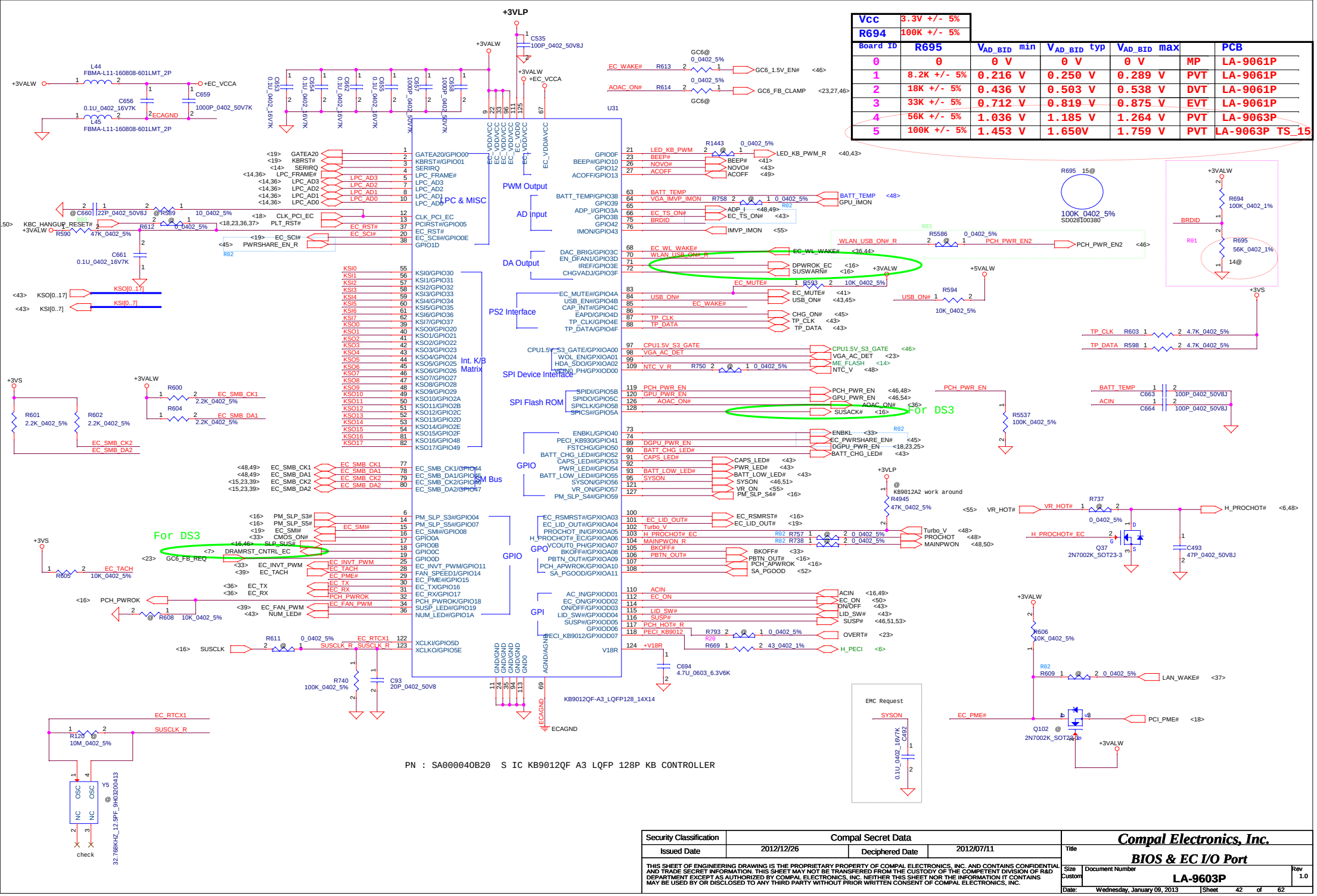
Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: HD Audio Codec_ALC259Q-VC

Size: C | Document Number: LA-9603P | Rev: 1.0

Date: Wednesday, January 09, 2013 | Sheet 41 of 62



Vcc	3.3V +/- 5%					
R694	100K +/- 5%					
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max		PCB
0	0	0 V	0 V	0 V	MP	LA-9061P
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT	LA-9061P
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT	LA-9061P
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT	LA-9061P
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	PVT	LA-9063P
5	100K +/- 5%	1.453 V	1.650V	1.759 V	PVT	LA-9063P TS_15

Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: BIOS & EC I/O Port

Size	Document Number	Rev
Custom	LA-9603P	1.0

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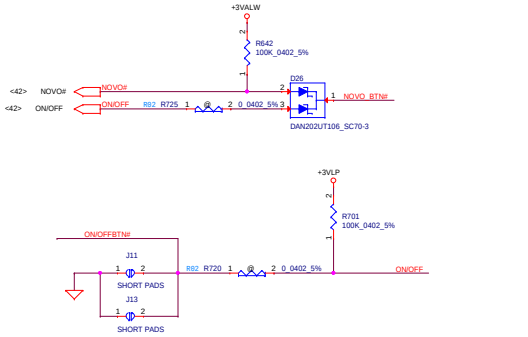
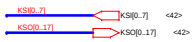
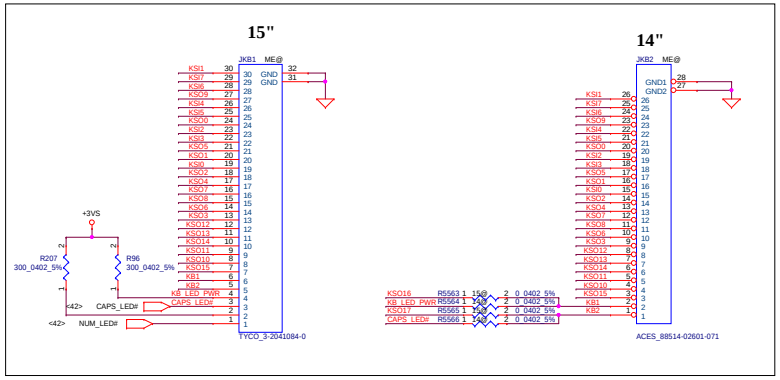
ON/OFF switch

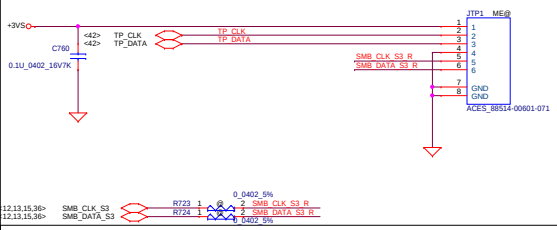


K/B Connector

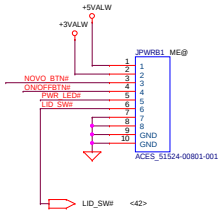




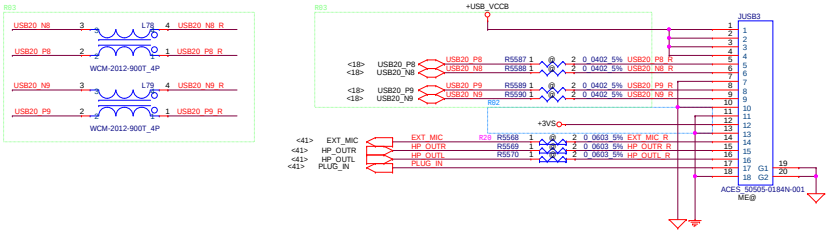
TP/B Connector



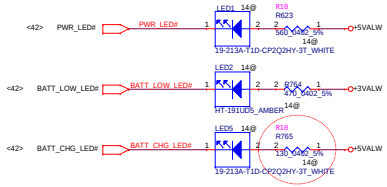
PWR/B Connector



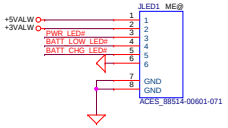
USB I/O Connector



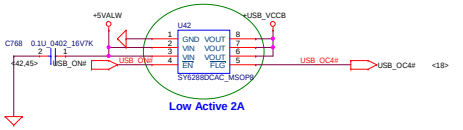
LED (For 14")



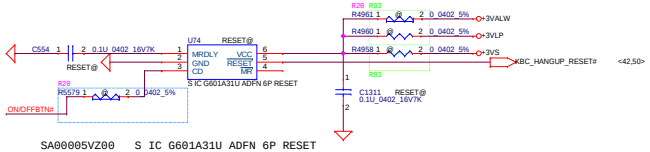
LED (For 15")



Right Side USB2.0 Port X 2 (USB/B)

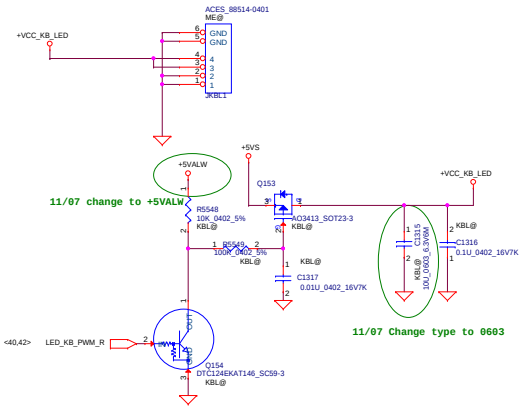


EC RESEST function

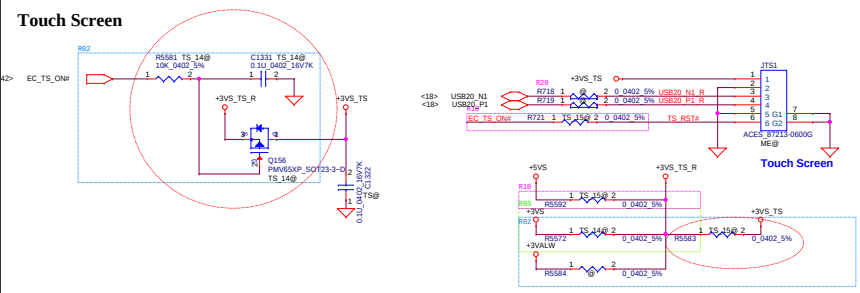


SA00005VZ00 S IC G601A31U ADFN 6P RESET

KB Lighting CONN.4pin



Touch Screen



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Title	Compal Electronics, Inc.		
	ROM/KBD/PWR/CR/LED/TP Conn.		
Size	Document Number		Rev
Custom	LA-9603P		1.0
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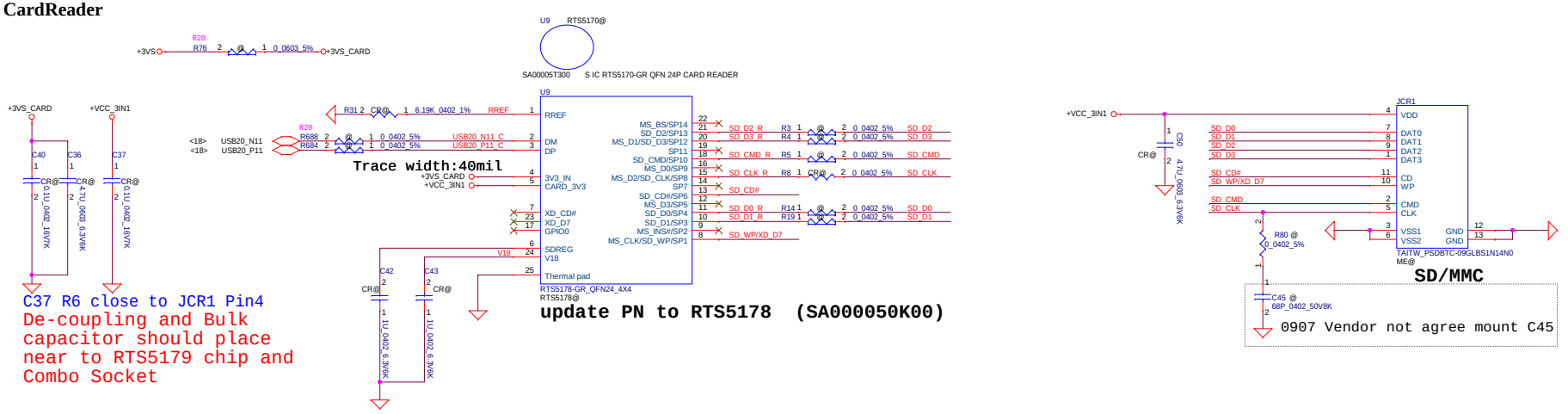
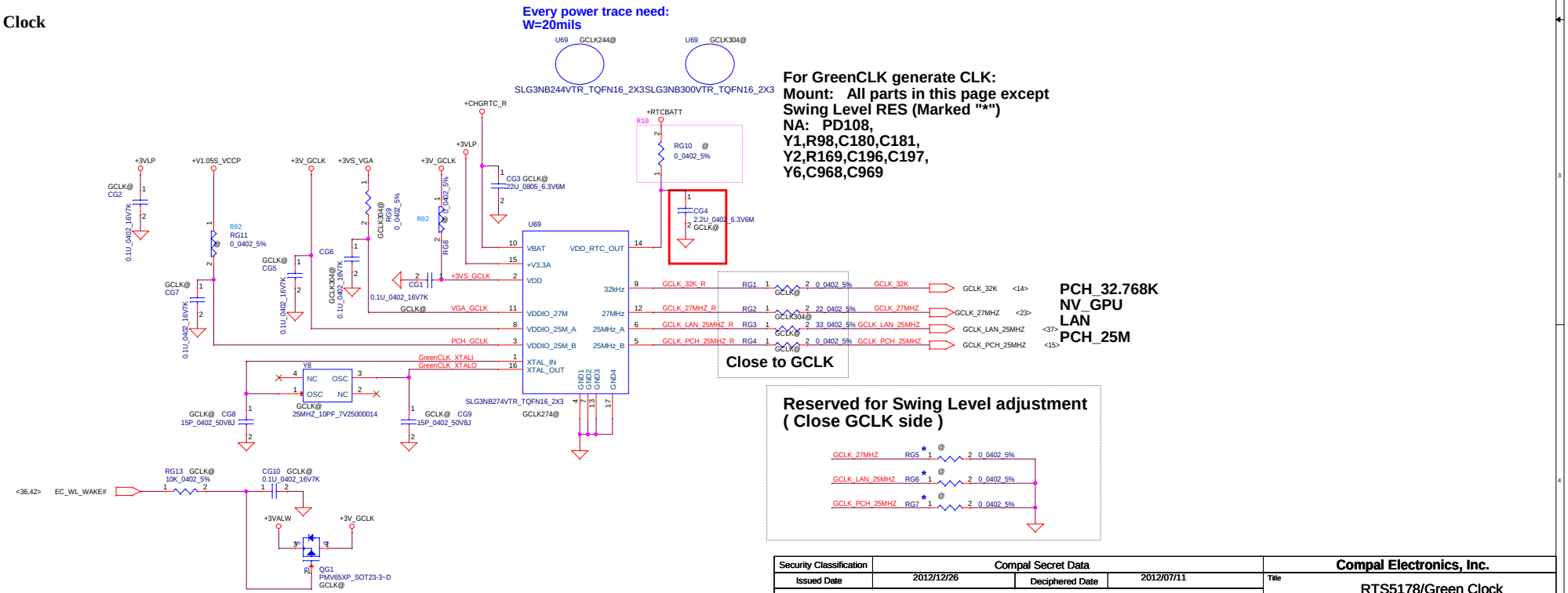
RTS5178 CardReader



Green Clock

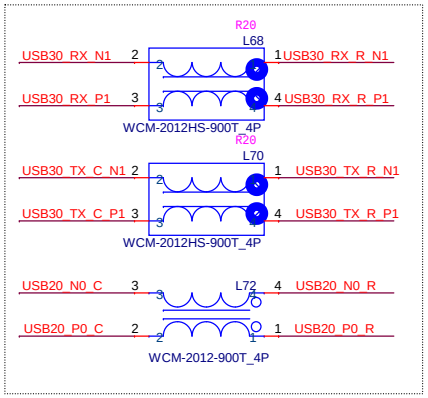


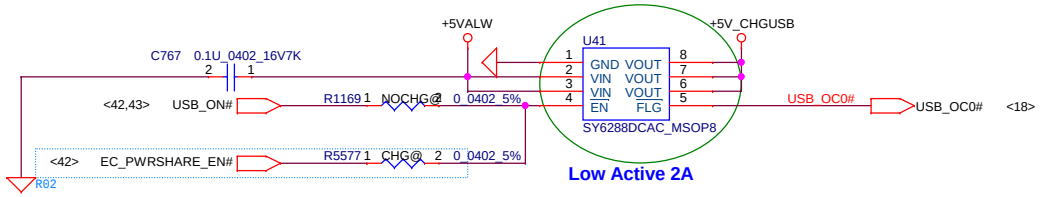
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/12/26	Deciphered Date 2012/07/11	Title: RTS5178/Green Clock

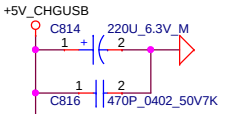
Size C	Document Number LA-9603P		Rev 1.0
Date: Wednesday, January 09, 2013	Sheet 44 of 62		

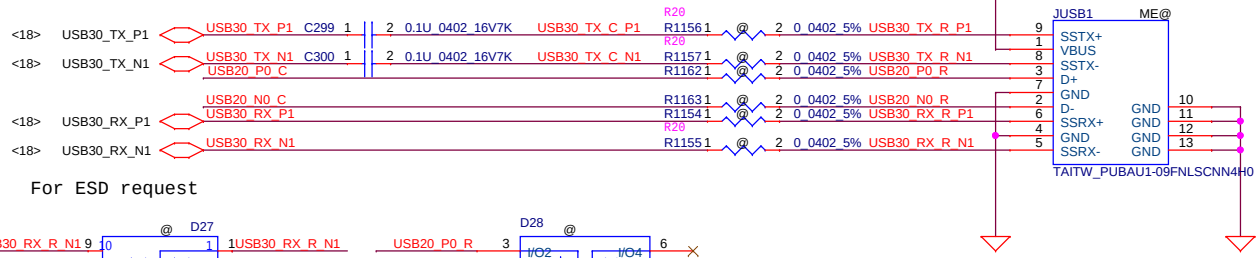
LEFT SIDE USB3.0 PORT X1

For EMI request
USB2.0 choke --> SM070000K00
USB3.0 Choke --> SM070001S00

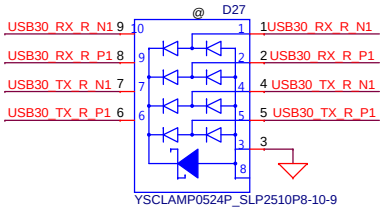


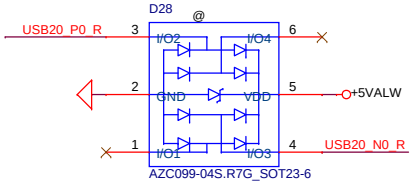




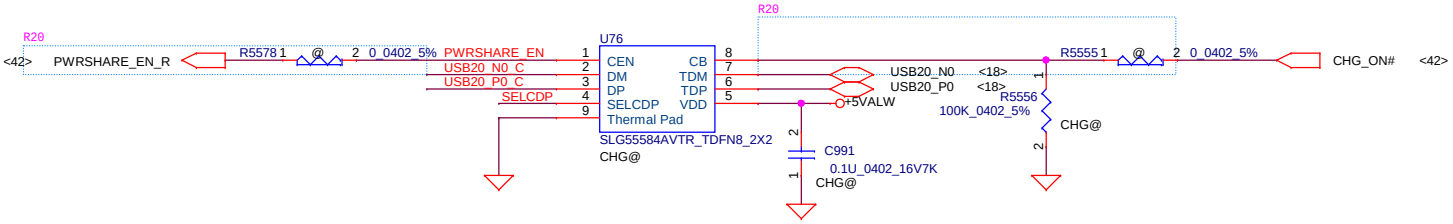


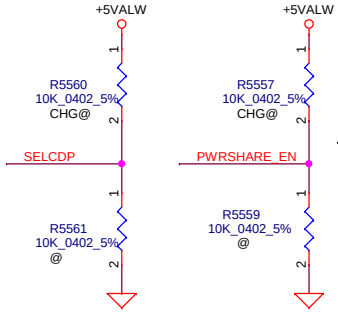
For ESD request

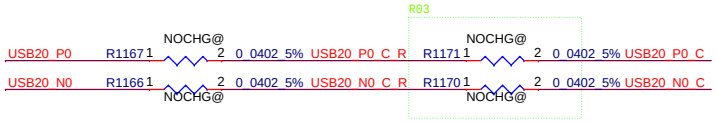




Left Side Charger USB3.0 Port



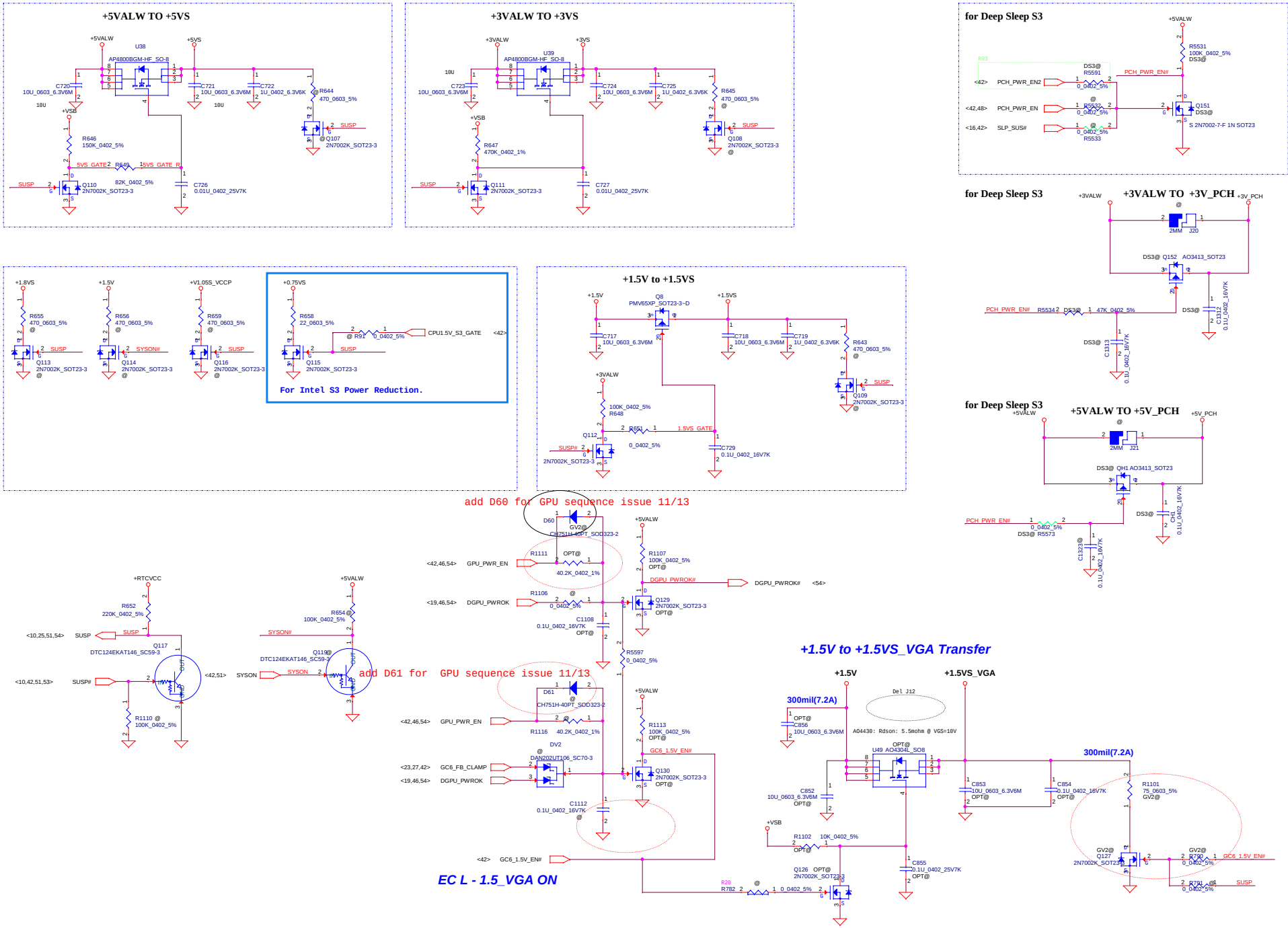




CB	SELCDP	Function
0	X	DCP autodetect with mouse /keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

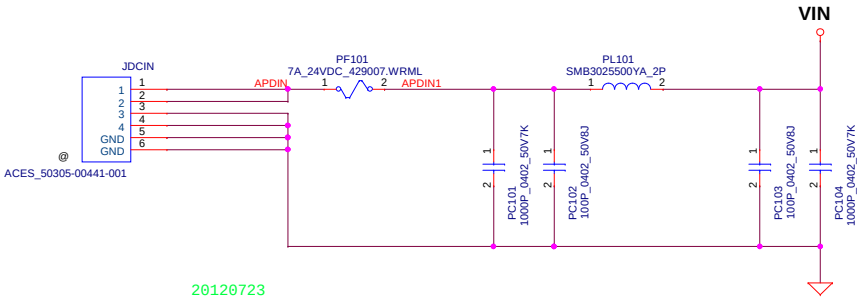
USB2.0/3.0 choke and ESD diode at sub-B.

Title			
USB3.0/Left USB Ports			
Size: Custom	Document Number		Rev: 1.0
Date: Wednesday, January 09, 2013	Sheet 45 of 62		

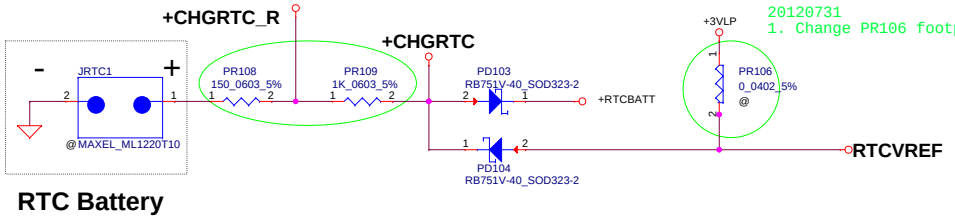


Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: DC Interface			
Size: Custom	Document Number: LA-9603P		Rev: 1.0
Date: Wednesday, January 09, 2013	Sheet: 46	of: 62	



20120723
For all sku
1. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080
   Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080



RTC Battery

20120731
1. Change PR106 footprint to R0402_0ohm-NEW

20120731
1. Add PR110 SD013000080 0_0603_5%
   Add PR111 SD013150080 150_0603_5%

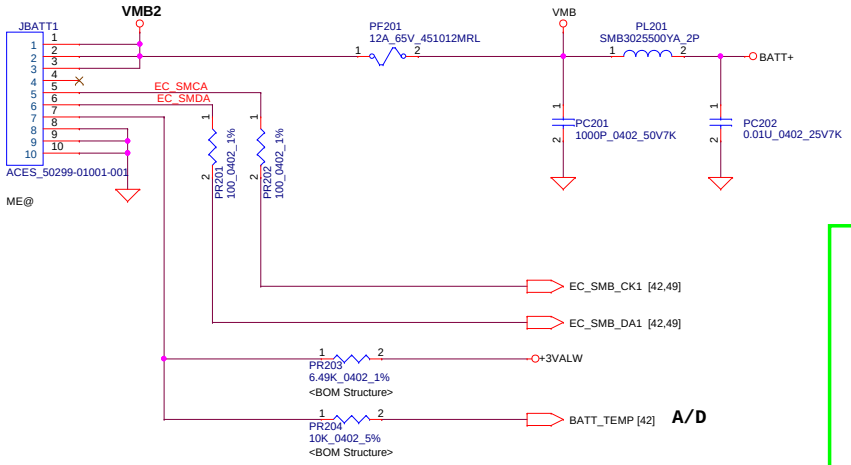
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

Size	Document Number	Rev
Custom	Xz90	0.1

Date: Wednesday, January 09, 2013 Sheet 47 of 62



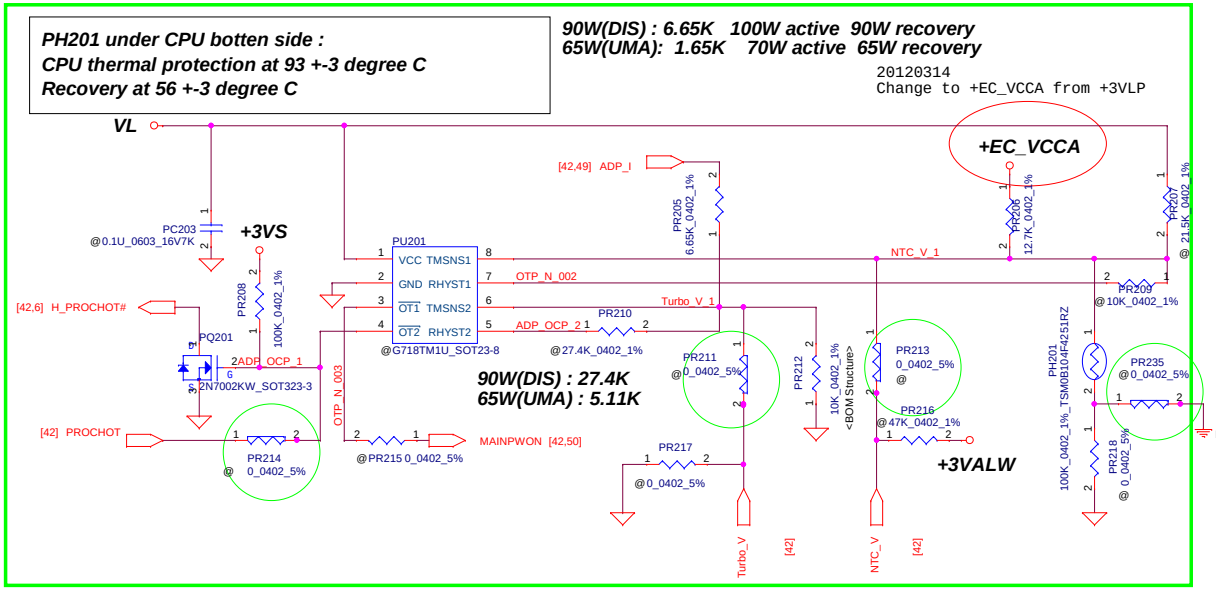
ADP_I need to write Charge Options Register (0x12H)=> bit6=1

0: IOUT is the 20x current amplifier output <default @ POR>
1: IOUT is the 40x current amplifier output

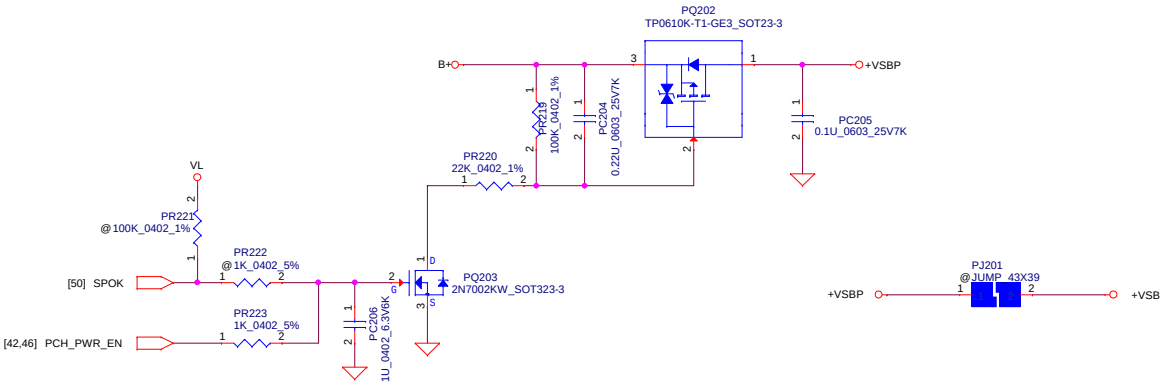
PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

90W(DIS) : 6.65K 100W active 90W recovery
65W(UMA): 1.65K 70W active 65W recovery

20120314
Change to +EC_VCCA from +3VLP



20120731
1. Change PR214,PR211,PR213 and PR235 footprint to R0402_0ohm-NEW



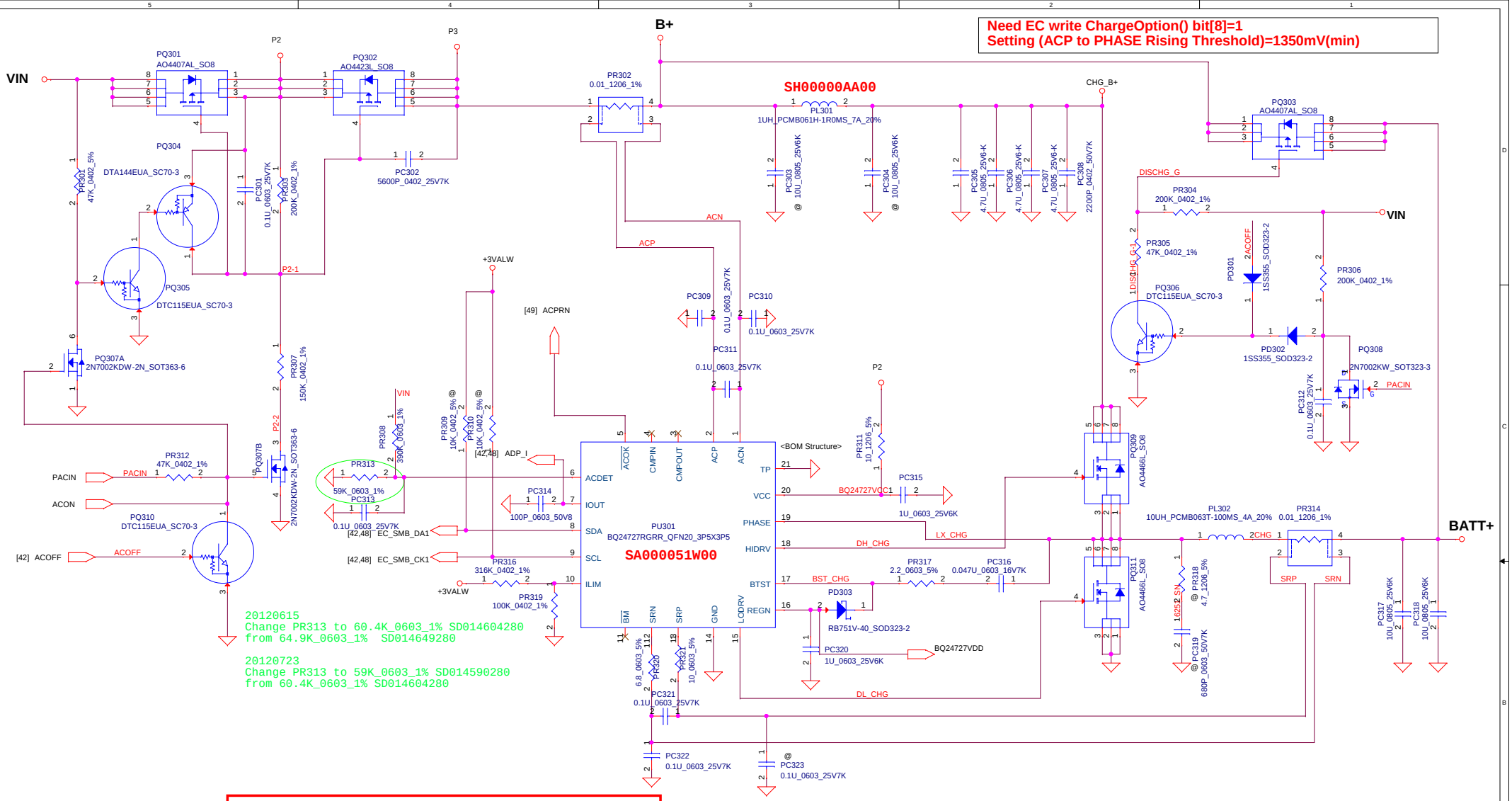
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: Zx90 | Rev: 0.1

Date: Wednesday, January 09, 2013 | Sheet 48 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2012/07/11

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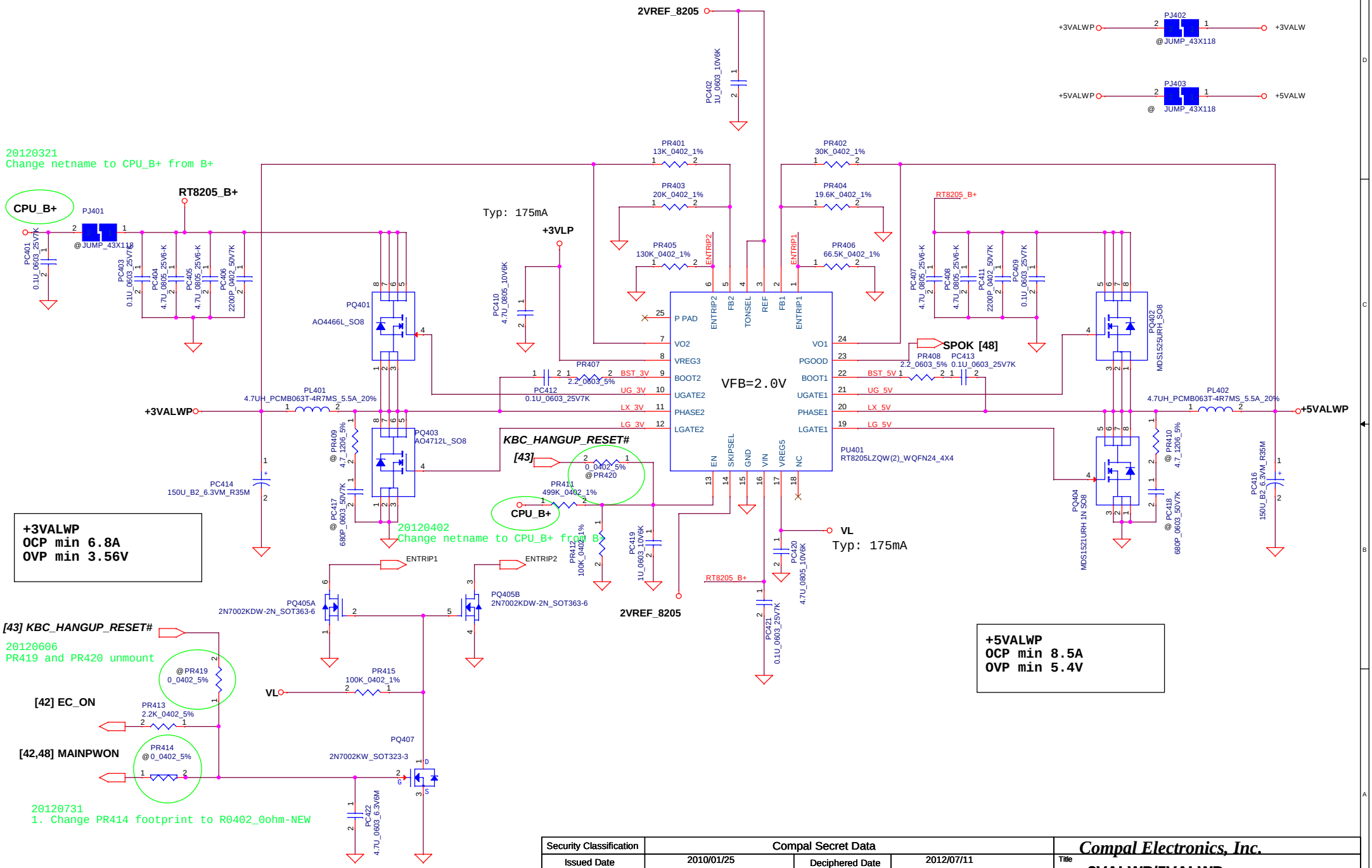
Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
	Zx90	0.1

Date: Wednesday, January 09, 2013 Sheet 49 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

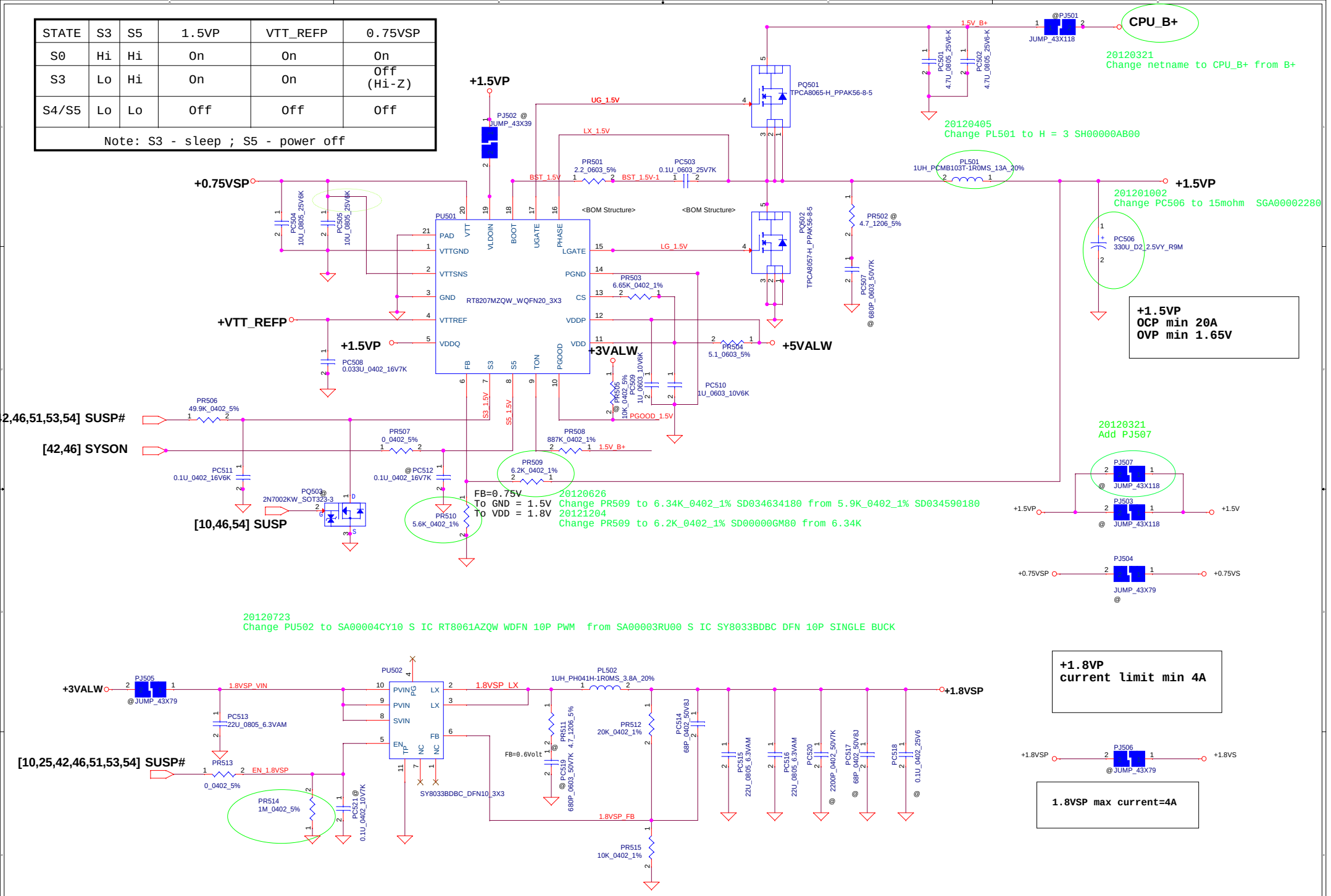
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	Zx90	0.1

Date: Wednesday, January 09, 2013 Sheet 50 of 62

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

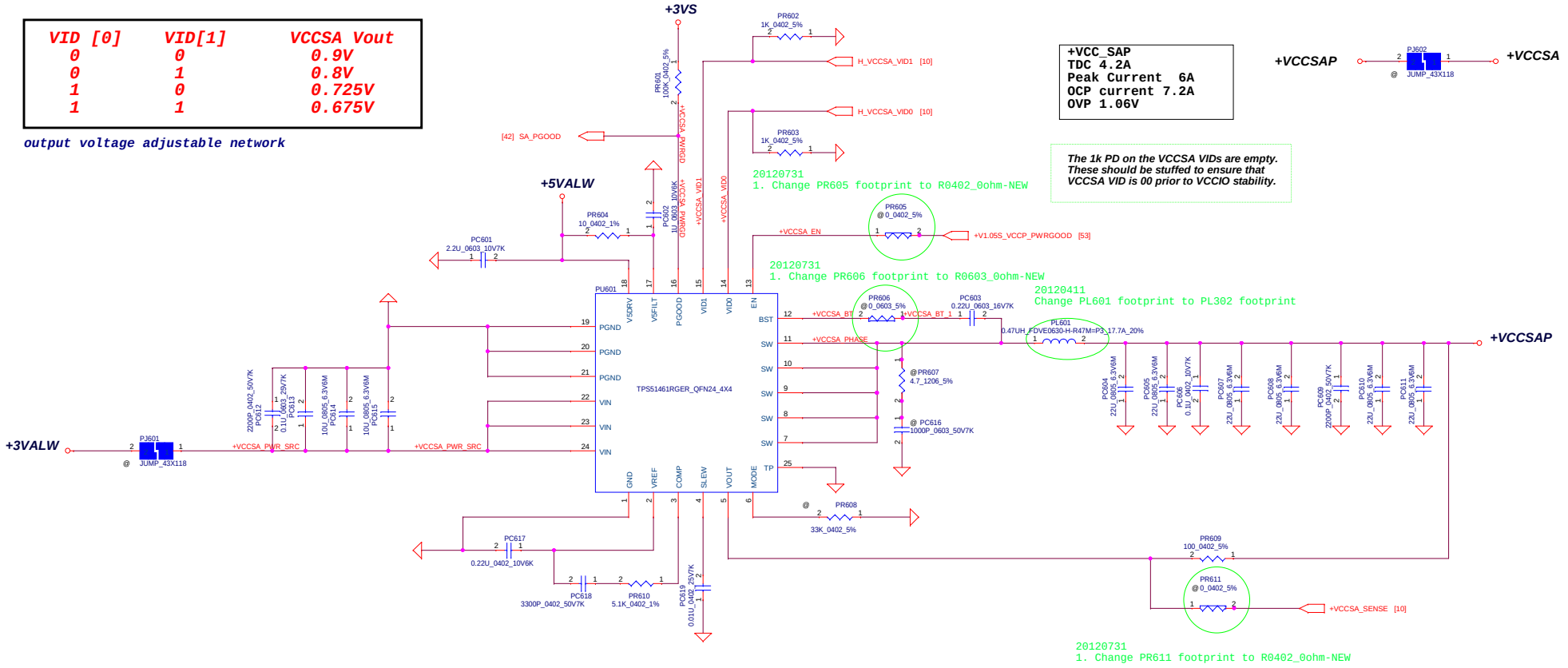
Title: +1.5VP/+1.8VSP

Size: Custom | Document Number: Zx90 | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 51 of 62

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
OVP 1.06V

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

20120731
1. Change PR605 footprint to R0402_0ohm-NEW

20120731
1. Change PR606 footprint to R0603_0ohm-NEW

20120411
Change PL601 footprint to PL302 footprint

20120731
1. Change PR611 footprint to R0402_0ohm-NEW

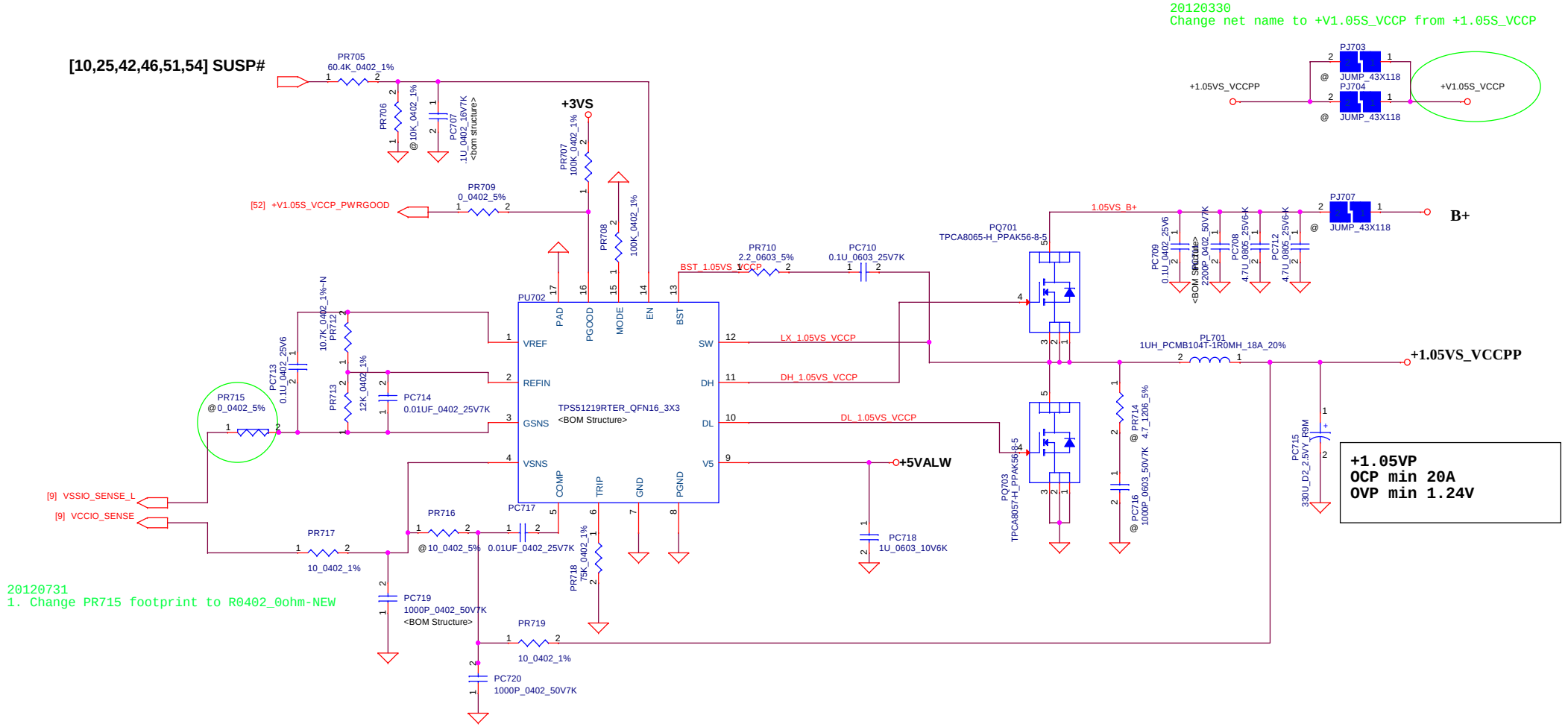
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +VCCSAP

Size	Document Number	Rev
C	Zx90	0.1

Date: Wednesday, January 09, 2013 Sheet 52 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +1.05VS_VCCP

Size	Document Number	Rev
Custom	Zx90	0.1

Date: Wednesday, January 09, 2013 Sheet 53 of 62

20121015
1.Change PR816 from SD028100380 S RES 1/16W 100K +-5% 0402 to SD028100180 S RES 1/16W 1K +-5% 0402

2.Change PQ803 from NA to SB000009Q80 S TR 2N7002KW 1N SOT323-3

3.Change PR813 from NA to SD000001R80 S RES 1/10W 22 +-5% 0603

4.Change PR815 from NA to SD028000080 S RES 1/16W 0 +-5% 0402

20120405
Change PQ802 and PJ802 netname to +V1.05S_VCCP from +1.05VS

[46,54] DGPU_PWROK#
[10,46,51,54] SUSP

DGPU_PWROK# [46,54]
SUSP [10,46,51,54]

20120926
1. Add PC871 for reserve

20120919
1. Change PQ810 gnd net name to gnd from GPU_FBRTN

2phase --> PSI > 2.4V
1phase --> PSI < 0.8V
HW pull high

Change PR842 to 12K from 8.6K

+VGA_COREP
OCP min 60A
OVP min 1.525V

20120919
1. Del PC847,PC844,PC850,PC851 0.1u_0402_10V7K
2.Add PC828,PC855,PC862,PC863,PC868,PC869 22u_0805_6.3V6M

20121026
Del PC823,PC825,PC828,PC855,PC862,PC869 SE000000I10 S CER CAP 22UF 6.3V M X5

20121023
1.Change PR807 to 0ohm SD028000080 from 100ohm SD031100080

+VGA_CORE Under VGA Core

+VGA_CORE Near VGA Core

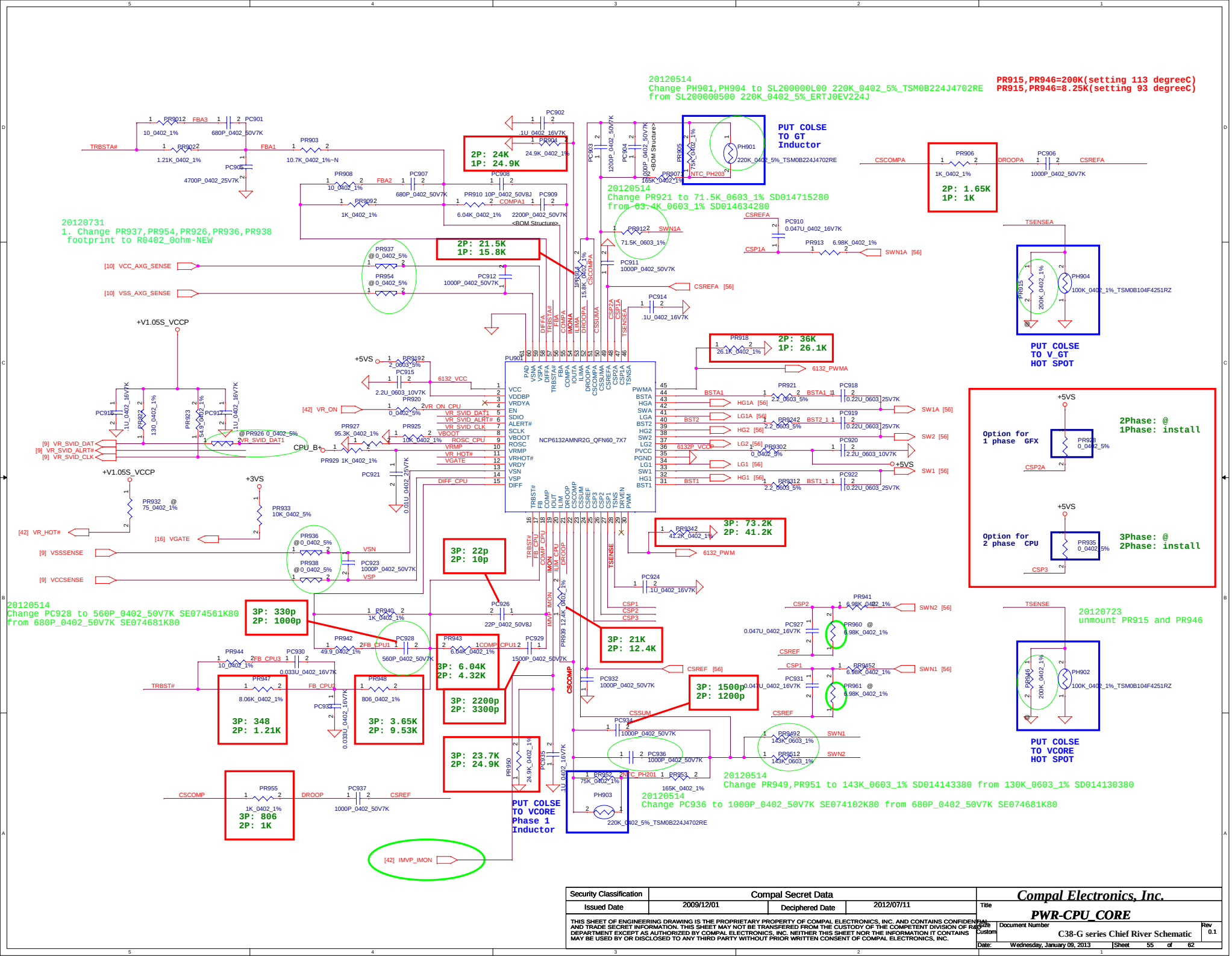
Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: VGA_COREP

Size: | Document Number: LA-9601P | Rev: 0.1

Date: Wednesday, January 09, 2013 | Sheet 54 of 62



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

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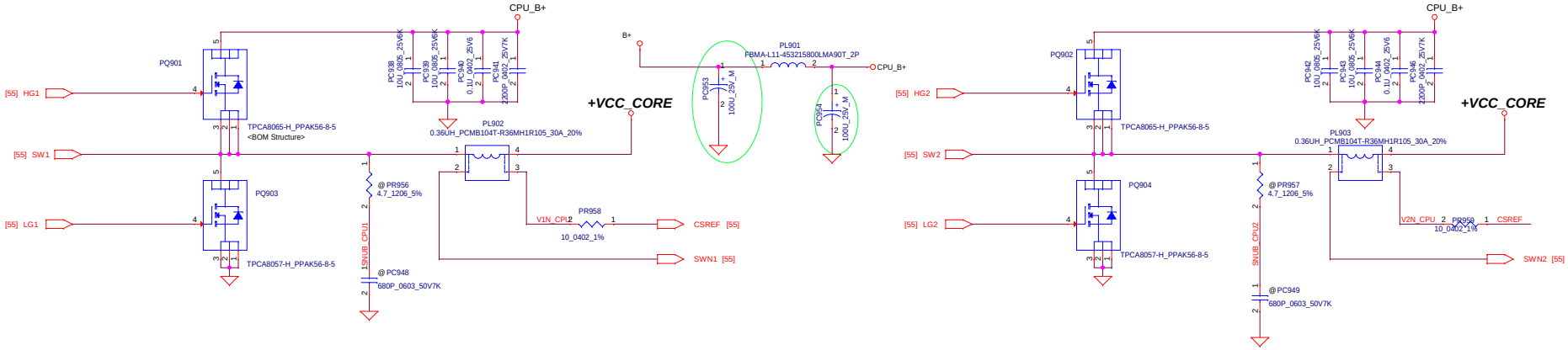
Compal Electronics, Inc.

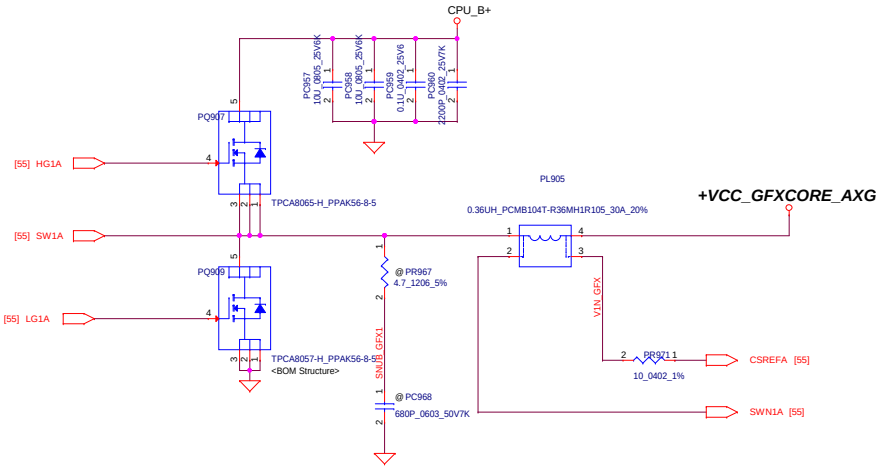
Title: PWR-CPU_CORE

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Wednesday, January 09, 2013 | Sheet 55 of 62



DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

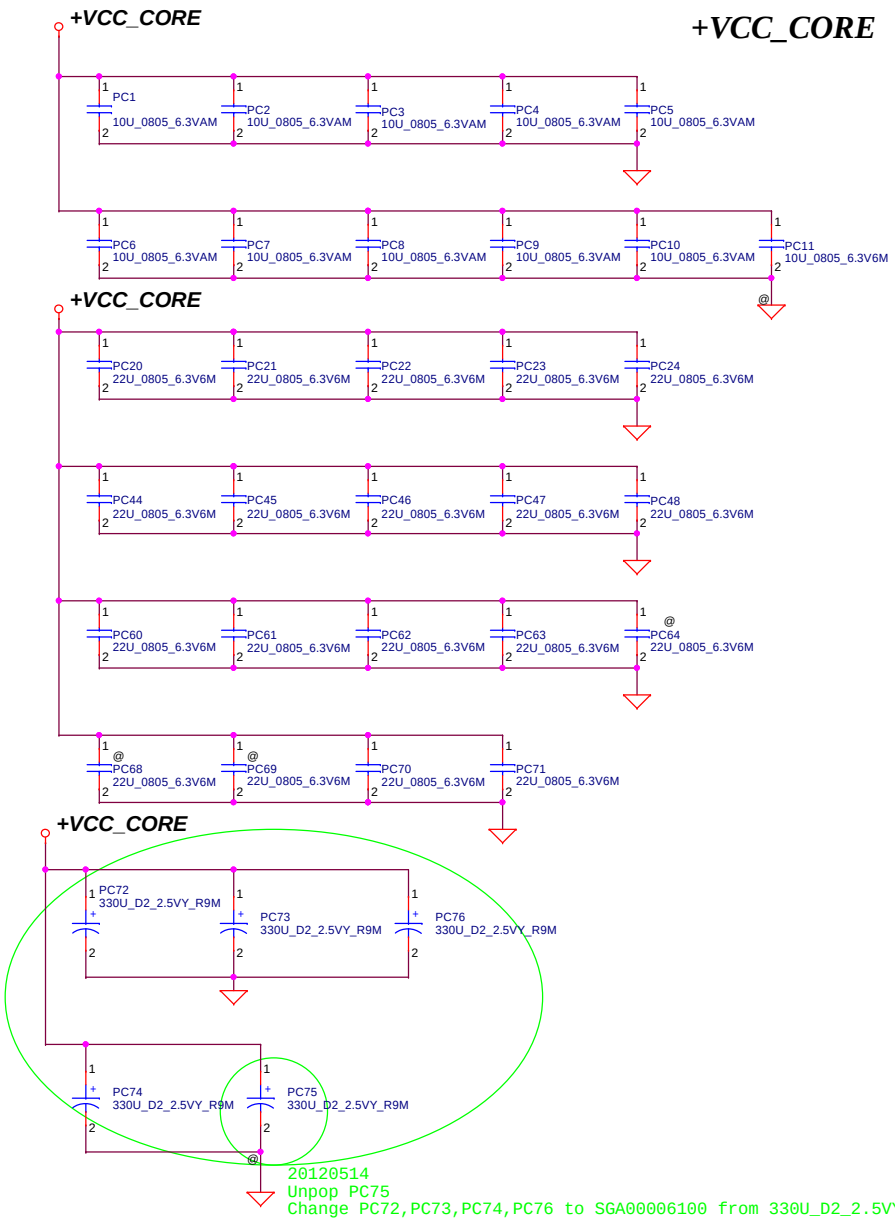
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **PWR-CPU_CORE**

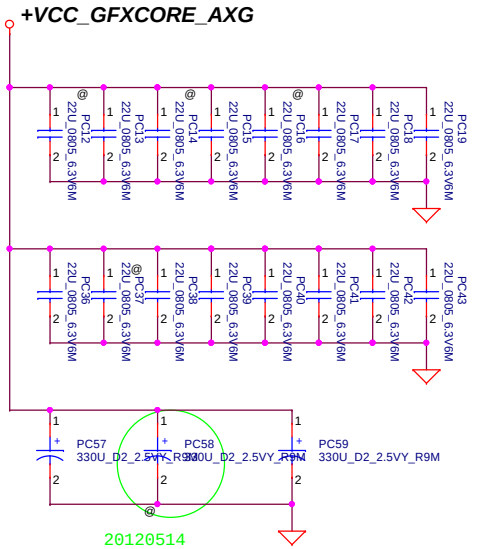
Size	Document Number	Rev
C	C38-G series Chief River Schematic	0.1

Date: Wednesday, January 09, 2013 | Sheet 56 of 62



20120514
Unpop PC75
Change PC72,PC73,PC74,PC76 to SGA00006100 from 330U_D2_2.5VY_R9M SGA00002680

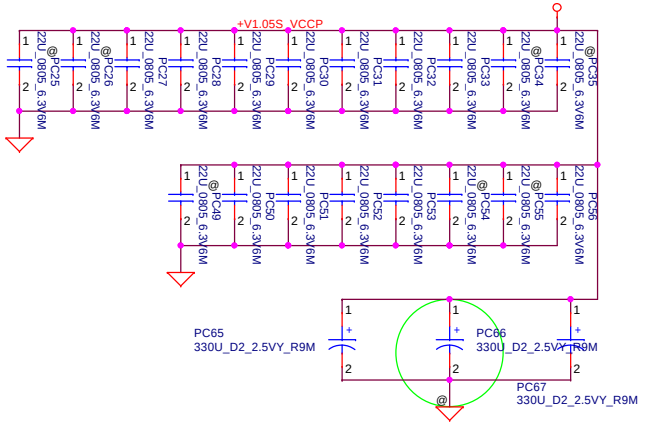
20120318
Change PC72,PC73,PC74,PC75 to 2 pin footprint



20120514
Unpop PC58

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



20120514
Unpop PC66

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-9601P	0.1

Date: Wednesday, January 09, 2013 Sheet 57 of 62

Version change list (P.I.R. List)

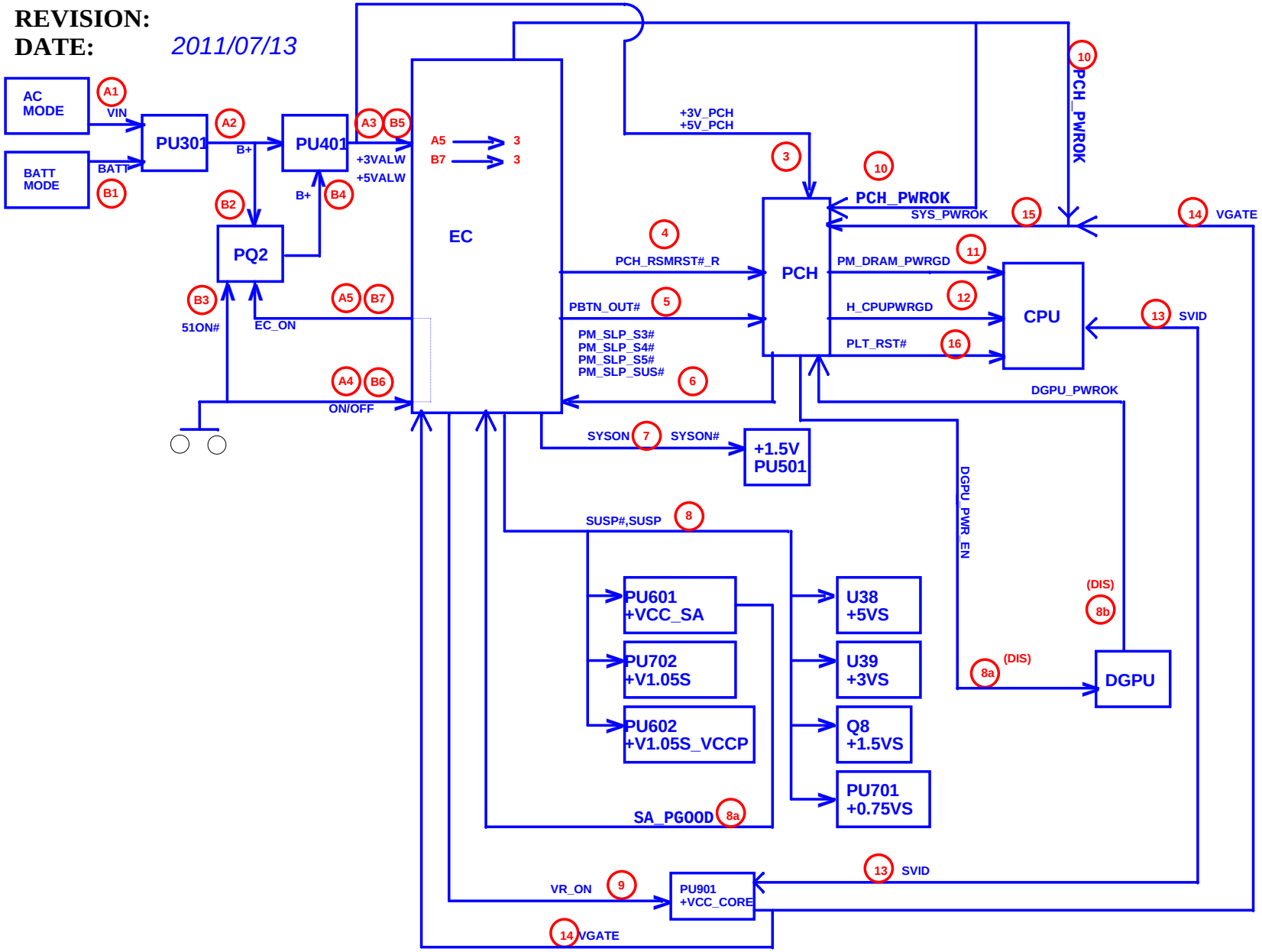
Item	Reason for change	PG#	Modify List	Date	Phase
1	For EC net name	P48	PR206 change pull high voltage to +EC_VCCA from +3VLP	20120316	EVT
2	Intersil advise	P54	1.Change PR848 to 1.47K SD000009480 from 1.15K 2.Unmount PC864	20120316	EVT
3	VGA IMON setting	P54	Change PR853 to 11K SD034110280 from 11.3K	20120316	EVT
4	set OCP is 56A	P54	Change PR869 to 1.58K (SD00000SJ80) from 1K	20120316	EVT
5	For 1.5V current	P51	Add PJ507 for 1.5V	20120321	EVT
6	For B+ layout	P55 P50 P51 P50	1.Change PC954 pull high to CPU_B+ from B+ 2.Change 3/5VALWP B+ input netname to CPU_B+ 3.Change 1.5VALWP B+ input netname to CPU_B+ 4.Change PR411 netname to CPU_B+ from B+	20120321	EVT
7	For HW net name	P53 P54	1.Change +1.05S_VCCP netname to +V1.05S_VCCP 2.Change PQ802.5 netname to +V1.05S_VCCP from +1.05VS	20120330	EVT
8	For HW power sequence	P54	1.Add control PU801 pin GPU_PWR_EN and reserve PR956 0_0402_5% 2.Change PR820 to SD034150380 150K_0402_1% from 100K 3.Change PC810 to SE071101J80 100P_0402_50V8J from 0.1u	20120330	EVT
9	For Intersil advise	P54	Change PR853 pull down netname to gnd	20120409	EVT
10	For IMON design	P55	Change PU901 to NCP6132A from ISL95836	20120412	EVT
11	For layout design	P54	1.Del PJ803 PJ804 2.Change net name to VGACORE from VGACOREP	20120511	DVT
12	For 1.05V, GFX_CORE,CPU_CORE design fine tune	P57	Unpop PC58, PC66,PC75 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
13	For CPU_CORE design fine tune and ON advise	P57	Change PC72,PC73,PC74,PC76 to S POLY C 330U 2V M D2 ESR9M SGA00006100 from 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
14	For CPU_CORE design fine tune and ON advise	P55	1.Change PC928 to 560P_0402_50V7K SE074561K80 from 680P_0402_50V7K SE074681K80 2.Change PR949,PR951 to 140K from 130K 3.Change PR912 to 71.5K_0603_1% SD014715280 from 63.4K_0603_1% SD014634280 4.Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJ0EV224J	20120514	DVT
15	For material EOL	P55	Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJ0EV224J	20120514	DVT
16	For HW VGA power sequence	P54	Add PR972 SD028000080 0_0402_5% Unmount PD801 Change PR820 to 0_0402_5% SD028000080 from 150K_0402_1% SD034150380 Unmount PC810	20120516	DVT

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
17	For HW reset function	P50	1.Add PR420 SD028000080 0_0402_5% for reserve 2 reserve.PR419 and PR420	20120606	PVT
18	For ACDET function	P49	1.Change PR313 to 60.4K_0603_1% SD014604280 from 64.9K_0603_1% SD014649280	20120615	PVT
19	For HW Grenn clock UMA sku trial tun	P47	1. unmount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120625	PVT
20	For ACDET function	P49	1.Change PR313 to 59K_0603_1% SD014590280 from 60.4K_0603_1% SD014604280	20120705	PVT
21	For VR_HOT	P55	1.unmount PR915 and PR946	20120705	PVT
22	For HW Grenn clock	P47	1. mount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120723	SVT
23	For material issue	P51	1.Change PU502 to SA00004CY10 S IC RT8061AZQW WDFN 10P PWM from SA00003RU00 S IC SY8033BDBC DFN 10P SINGLE BUCK	20120723	SVT

COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



Security Classification	Compal Secret Data		
Issued Date	2012/12/26	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ***Power sequence***

Size: Custom | Document Number: ***LA-9603P*** | Rev: 1.0

Date: Wednesday, January 09, 2013 | Sheet 60 of 62

Item	Reason for change	PG#	Modify List	Date	Phase
1	Initial				EVT
2	For LVDS blacklight PWM	P33	R431 change from 0ohm_short to 0ohm mount	5/7	EVT
3	For Change Audio Woofer MOSFET from Dual to single channel	P15	Changer Part from SB00000EO10 to SB00000EN00	5/7	EVT
4	For OVERT# Glitch issue at Power on status	P23	Add QV9	5/7	EVT
5	For BT&WLAN Combo Card	P36	to modify R897 value from 0 ohm to 1K ohm add BT_DISABLE_F_R on JWLN1.51 add R5580	5/8	DVT
6	For Factory request and cost down LVDS PIN Define	P33	To Modify LVDS PIN Define	5/8	DVT
7	For USB Charger mode control request	P45 P42	To Add PWRSHARE_EN_R on U31.38 To Add EC_PWRSHARE_EN# on U31.74 add R5577 and R5578, delete CHG_ON#	5/8	DVT
8	To change Reset IC G601	P42	to change R4959 value from 200K ohm to 0 ohm add R5579 0 ohm	5/8	DVT
9	Reserved Touch Screen Power Control	P42 P43	add R5581,C1331,R5572,R5583,R5584 and Q156 add EC_TS_ON on U31.66 add +3VS_TS,+3VS_TS_R	5/8	DVT
10	To change Speaker PIN define for ME routing request	P41	SPK_L2+ R1556 net in JSPK1.1 SPK_L1- R1554 net in JSPK1.2 SPK_R1- R1555 net in JSPK1.3 SPK_R2+ R1553 net in JSPK1.4	5/8	DVT
11	for Realtek Vendor recommand	P41	R1123,C1134 close to U50.47 R5582,R1559 and C1135 Close to U73.1 EXT_MIC_R	5/8	DVT
12	for ME request	P39	To Modify H21,H7,H18 PCB Footprint as below H21 from H_3P3 to H_4P6 H7 from H_2P8 to H_3P0 H18 from H_3P3 to H_3P9N	5/8	DVT
13	for LAN Clock be better	P37	change C990 value from 5PF to 0 ohm.	5/9	DVT
14	for Audio Vendor recommand	P43	change JUSB3.11 from GND to +3VS change JUSB3.12 from +3VS to AGND	5/10	DVT
15	for Crystal finetune Capacitor	P43	C180,C181 from 18PF to 12PF	5/16	DVT
16	for DVT Board ID request	P42	R695 from 33K to 18K	5/17	DVT
17	for PVT request	P37	Change Reference from C990 to R5585	5/23	PVT
18	for Surge request	P38	C1325,C1326,C1327 change package from 0402 to 0603	5/23	PVT
19	for Reset IC function	P42, P50,P43	add R612,PR420,R4960,R4961 Delete R4959	5/24	PVT

Compal Electronics, Inc.

Title: *HW-PIR1*

Size: Custom | Document Number: LA-9603P | Rev: 1.0

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Item	Reason for change	PG#	Modify List	Date	Phase
20	modify N14P_GV2 GPU power sequence	P18 P46 P46	Remove R5575,connect DGPU_PWR_EN to U31.pin89 Add diode D60;D61 add discharge(Q157) for DGPU_PWR_EN	11/13	PVT
21	for GC6 function	P23	Change RV54 from 10K to 100k	11/29	PVT
22	for GC6 function	P46	Add a 0 ohm R5597 between Q129 pin 2 and Q130 pin	12/26	Pre-MP
23	due to they are cap not resistor.	P46	R1108,R1112 location change to C1108,C1112	12/26	Pre-MP

Compal Electronics, Inc.

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