



LA-7491P
DA60000N810

Compal Confidential

Brazos PCW20 LA7491 Schematics Document

AMD APU Ontario-FT1+ FCH Hudson-M1

2011-03-29

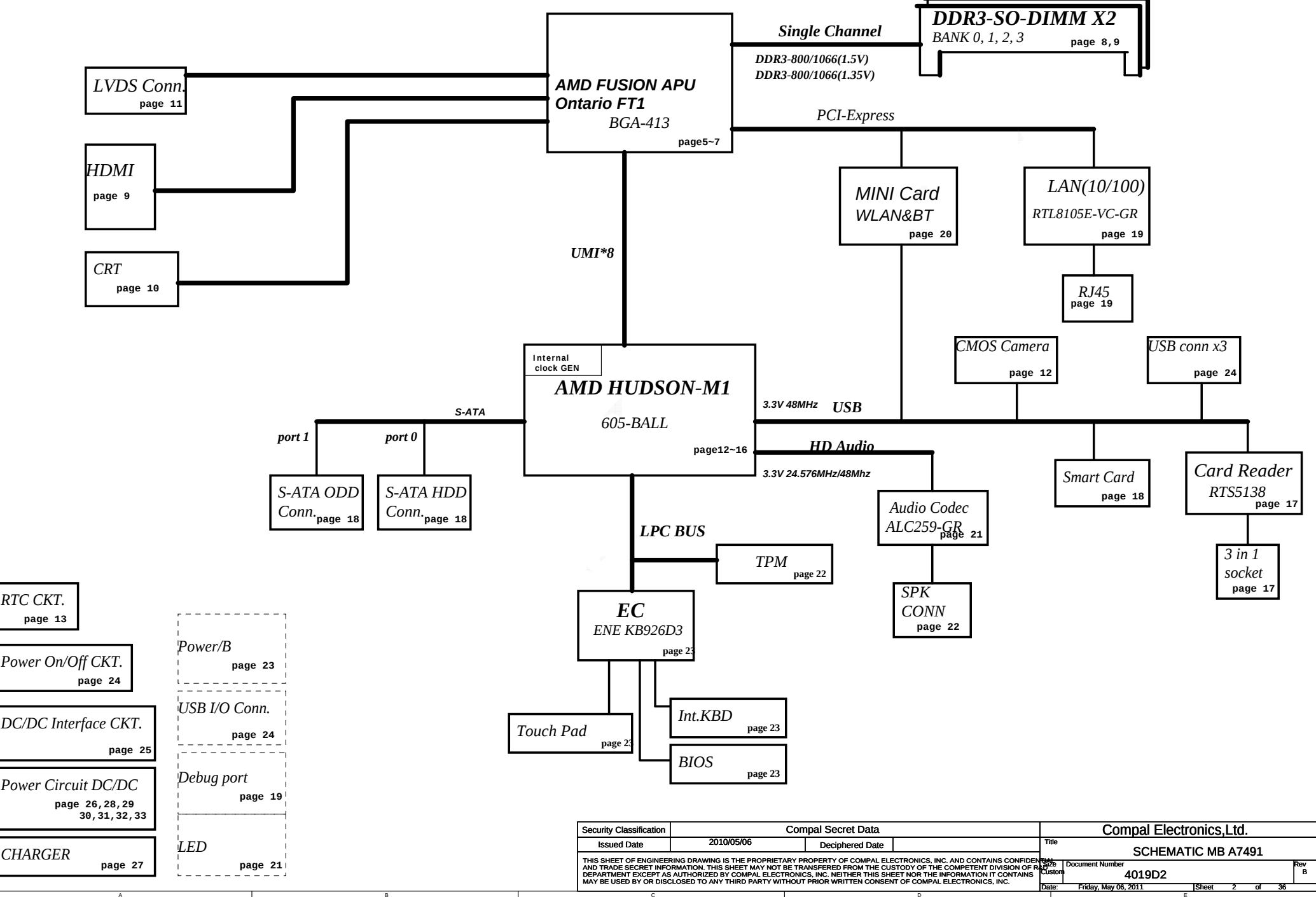
REV:1.0

Security Classification		Compal Secret Data		Compal Electronics,Ltd.	
Issued Date	2010/05/06	Deciphered Date		Title	
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Model Name : Brazos

File Name : LA7491



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DDR3 Voltage Rails

power plane State				
	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +NB_CORE +1.8VS +0.75VS +1.1VS +1.0VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

@	Reserve
CONN@	ME CONNECTOR
8105E@	100M LAN function
8111E@	GLAN function
REAL@	ALC259-GR
VIA@	V1802T
ROM@	not support flash ROM
FROM@	Support flash ROM

FCH SM Bus0 address

Device	HEX	Address
SDDIM I	A0	1010 0000
SDDIM II	A2	1010 0010

FCH SM Bus1 address

Device	HEX	Address
WLAN		

EC SM Bus1 address

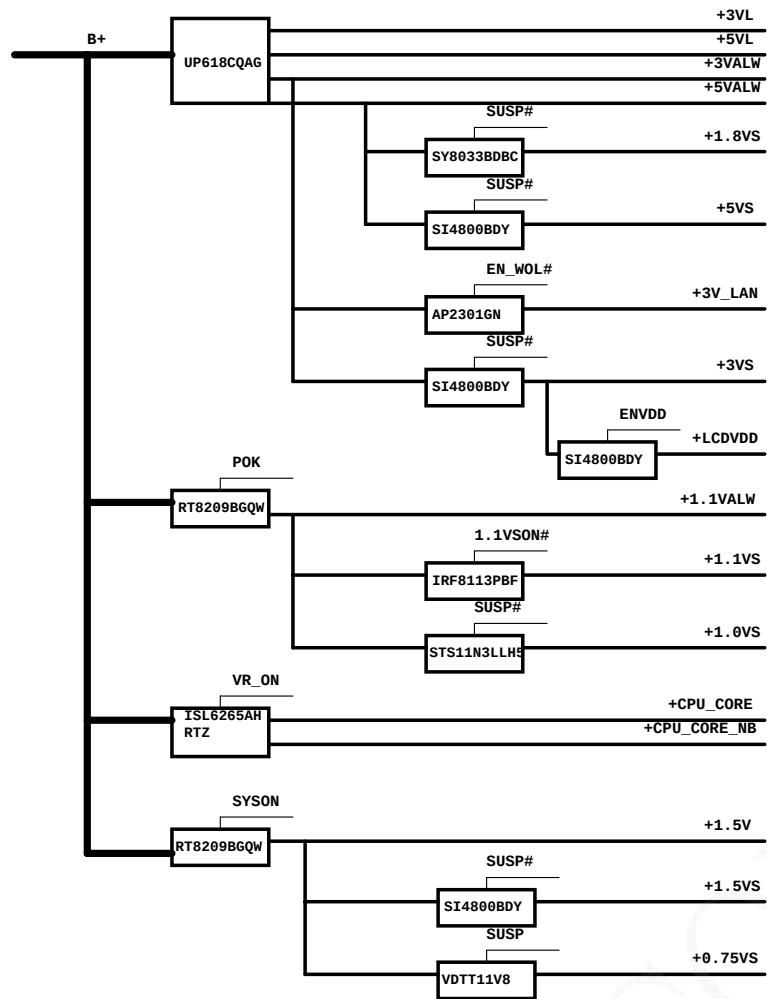
Device	HEX	Address
Smart Battery	16H	0001 011X b

EC SM Bus2 address

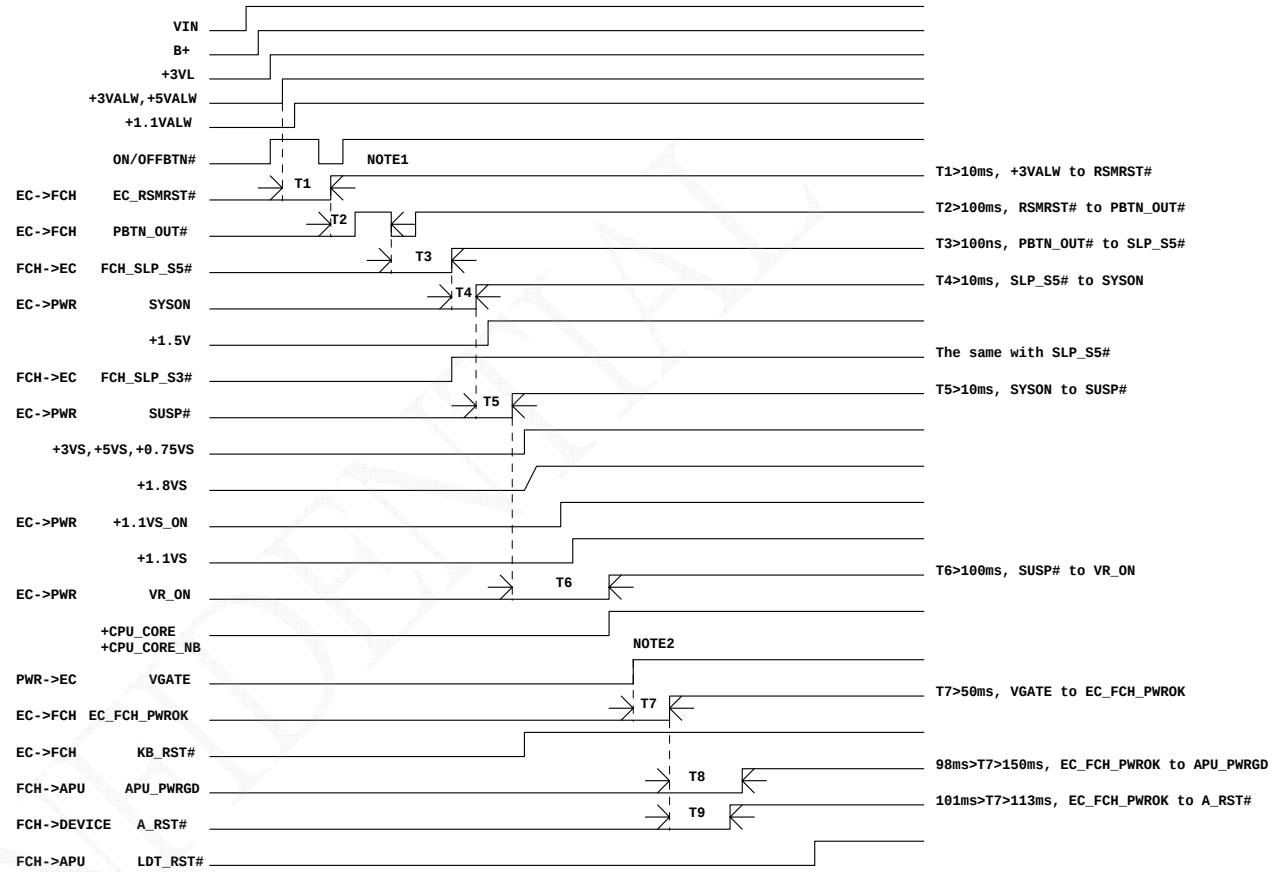
Device	HEX	Address
APU internal thermal sensor		1001 100X b

	SOURCE	POWER PLAN	HDMI	LVDS	CRT	FCH	CPU CORE	SDDIM I / II	WLAN	BATT	APU
TDP1_AUXP TDP1_AUXN	APU	+3VS	V								
LTDP0_AUXP LTDP1_AUXN	APU	+3VS		V +5VS							
DAC_SCL DAC_SDA	APU	+3VS			V +5VS						
SIC SID	APU	+3VS				V +3VALW					
SVC SVD	APU	+1.8VS					V				
SMB_FCH_CK0 SMB_FCH_DA0	FCH	+3VS						V			
SMB_FCH_CK1 SMB_FCH_DA1	FCH	+3VALW							V		
SMB_EC_CK1 SMB_EC_DA1	EC	+5VALW								V	
SMB_EC_CK2 SMB_EC_DA2	EC	+3VS									V

POWER MAP



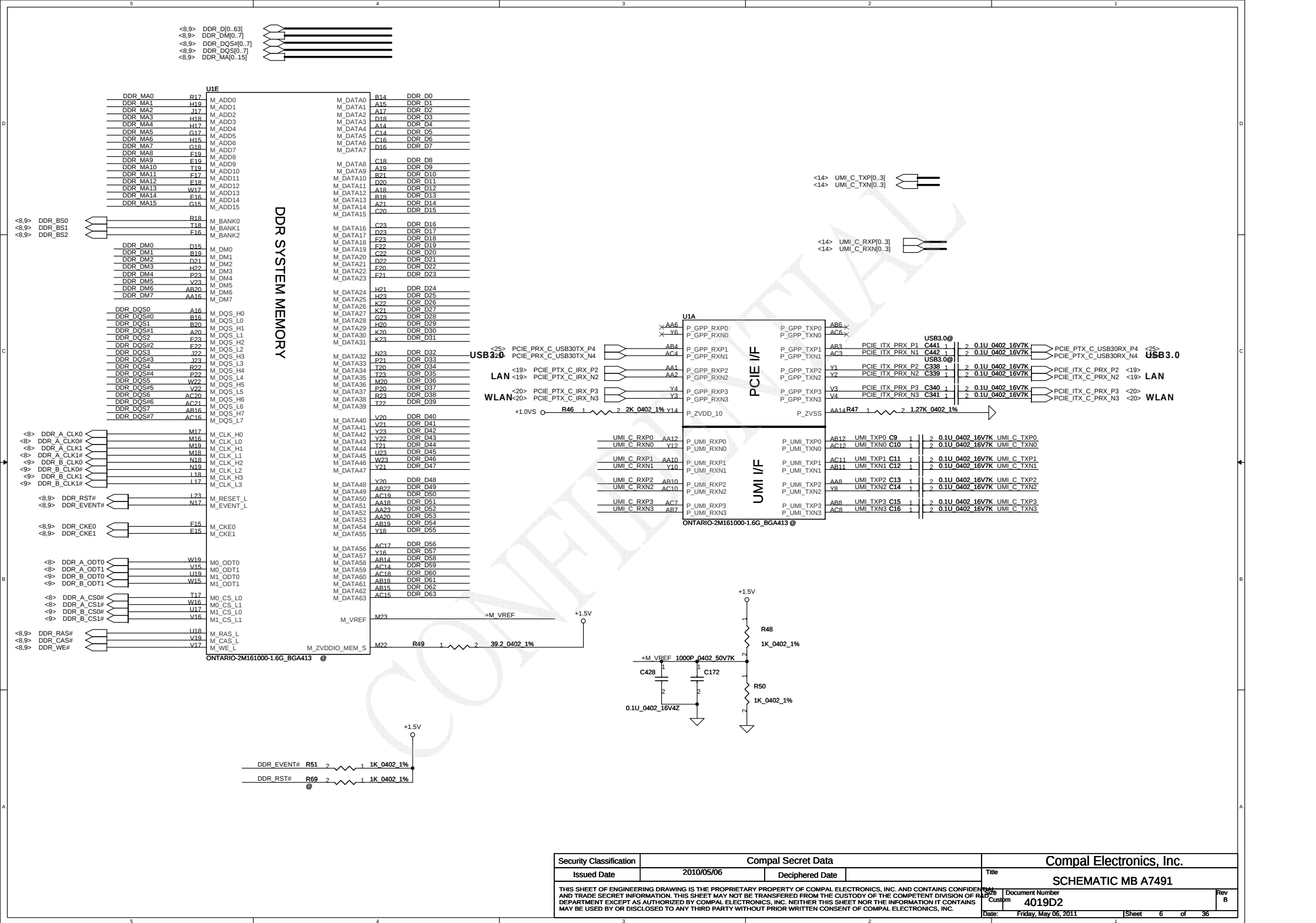
POWER SEQUENCE



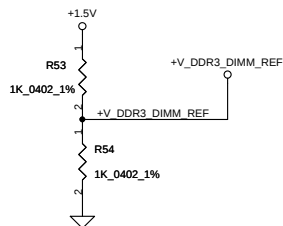
NOTE1: RSMRST# rise time(10% to 90%)<50ms
fail time<1ms

NOTE2: EC_FCH_PWROK rise time(10% to 90%)<50ms
fail time<1ms

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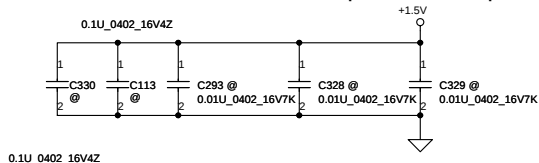


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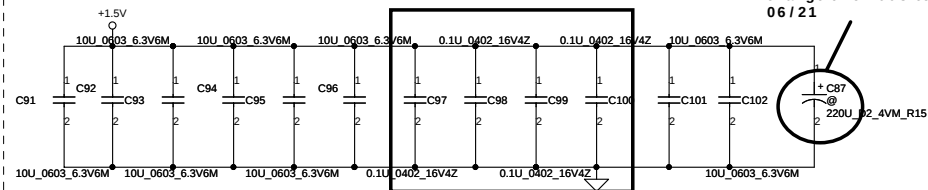
<6,9> DDR_DQS#[0..7]
 <6,9> DDR_D[0..63]
 <6,9> DDR_DM[0..7]
 <6,9> DDR_DQS[0..7]
 <6,9> DDR_MA[0..15]

Put it between DDR3 +1.5VS shape and GND shape

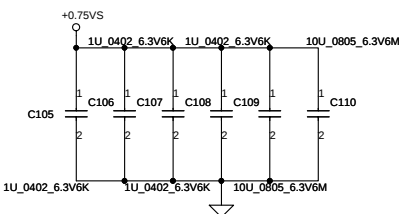


Layout Note:
Place near JDDR1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDDR1.203 & JDDR1.204



<6,9> DDR_CKE0
 <6,9> DDR_BS2
 <6,9> DDR_A_CLK0
 <6,9> DDR_A_CLK0#
 <6,9> DDR_BS0
 <6,9> DDR_WE#
 <6,9> DDR_CAS#
 <6,9> DDR_A_CS1#

DDR MA12
 DDR MA9
 DDR MA8
 DDR MA5
 DDR MA3
 DDR MA1
 DDR MA10
 DDR MA13

DDR D32
 DDR D33
 DDR DQS#4
 DDR DQS4
 DDR D34
 DDR D35
 DDR D40
 DDR D41
 DDR DM5
 DDR D42
 DDR D43
 DDR D48
 DDR D49
 DDR DQS#6
 DDR DQS6
 DDR D50
 DDR D51
 DDR D56
 DDR D57
 DDR DM7
 DDR D58
 DDR D59

DDR D32
 DDR D33
 DDR DQS#4
 DDR DQS4
 DDR D34
 DDR D35
 DDR D40
 DDR D41
 DDR DM5
 DDR D42
 DDR D43
 DDR D48
 DDR D49
 DDR DQS#6
 DDR DQS6
 DDR D50
 DDR D51
 DDR D56
 DDR D57
 DDR DM7
 DDR D58
 DDR D59

JDDR1
 VREF DQ
 DDR D0
 DDR D1
 DDR DM0
 DDR D2
 DDR D3
 DDR D8
 DDR D9
 DDR DQS#1
 DDR DQS1
 DDR D10
 DDR D11
 DDR D16
 DDR D17
 DDR DQS#2
 DDR DQS2
 DDR D18
 DDR D19
 DDR D24
 DDR D25
 DDR DM3
 DDR D26
 DDR D27

CONN@
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<6,8> DDR_DM[0..7]

<6,8> DDR_DQS[0..7]

<6,8> DDR_MA[0..15]

Layout Note:
Place near JP3

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA

change two 100U to one 220U
06 / 21

Layout Note:
Place near JP3.203 & JP3.204

	SA0	SA1
Compal common design	0	1
ADM CRB	1	0

Security Classification

Compal Secret Data

Issued Date

2010/05/06

Deciphered Date

Title

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SCHEMATIC MB A7491

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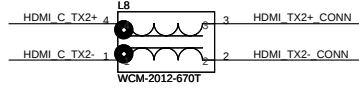
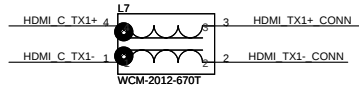
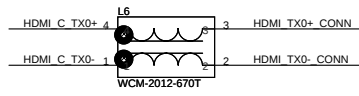
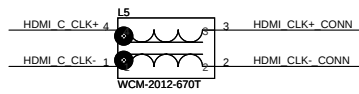
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Rev
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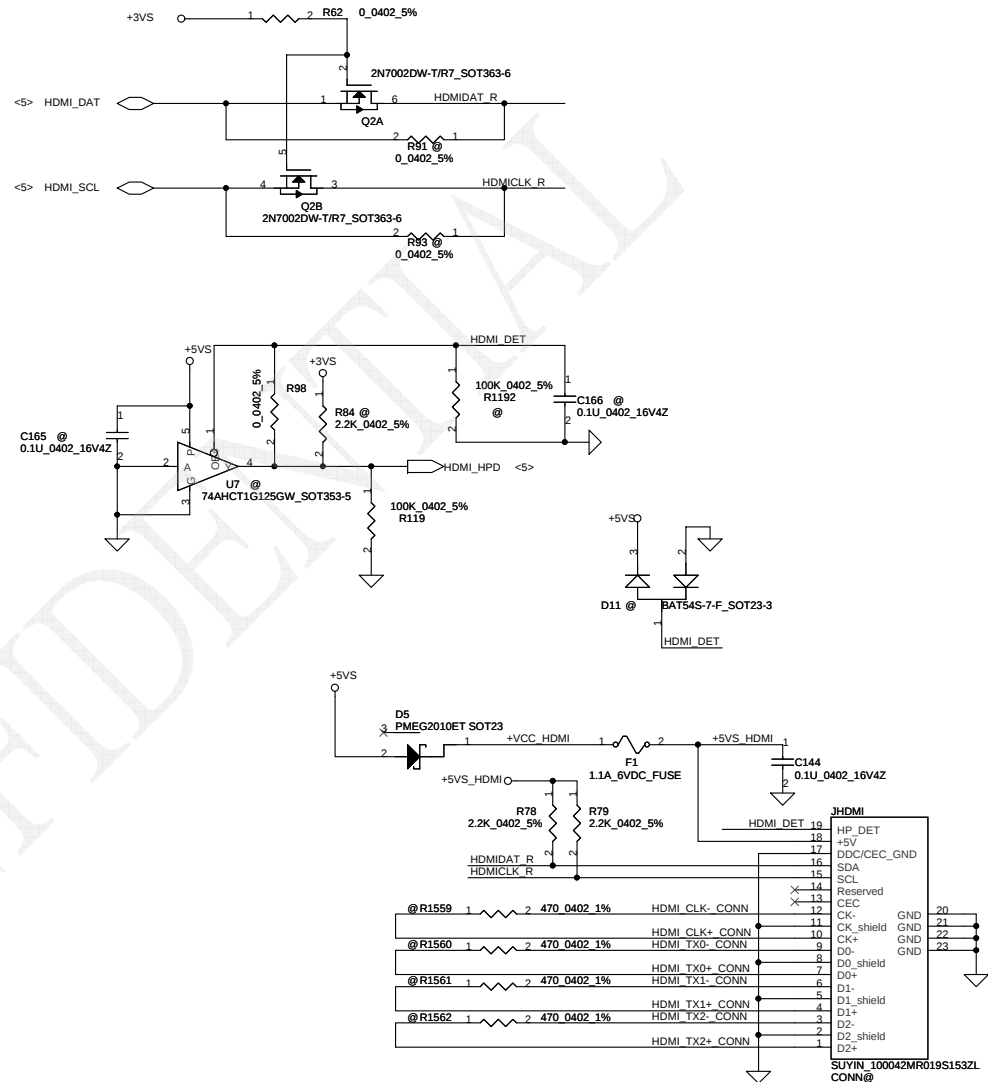
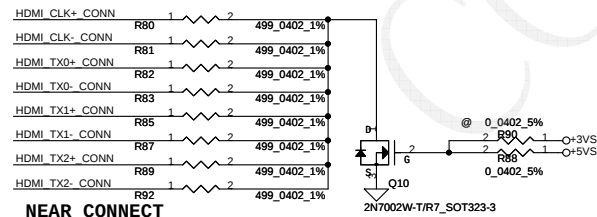
Date: Friday, May 06, 2011

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<5> HDMI_CLK-	HDMI_CLK-	C136	1	2	0.1U 0402 16V7K	HDMI C_CLK-
<5> HDMI_CLK+	HDMI_CLK+	C137	1	2	0.1U 0402 16V7K	HDMI C_CLK+
<5> HDMI_TX2+	HDMI_TX2+	C138	1	2	0.1U 0402 16V7K	HDMI C_TX2+
<5> HDMI_TX2-	HDMI_TX2-	C139	1	2	0.1U 0402 16V7K	HDMI C_TX2-
<5> HDMI_TX1+	HDMI_TX1+	C140	1	2	0.1U 0402 16V7K	HDMI C_TX1+
<5> HDMI_TX1-	HDMI_TX1-	C141	1	2	0.1U 0402 16V7K	HDMI C_TX1-
<5> HDMI_TX0+	HDMI_TX0+	C142	1	2	0.1U 0402 16V7K	HDMI C_TX0+
<5> HDMI_TX0-	HDMI_TX0-	C143	1	2	0.1U 0402 16V7K	HDMI C_TX0-

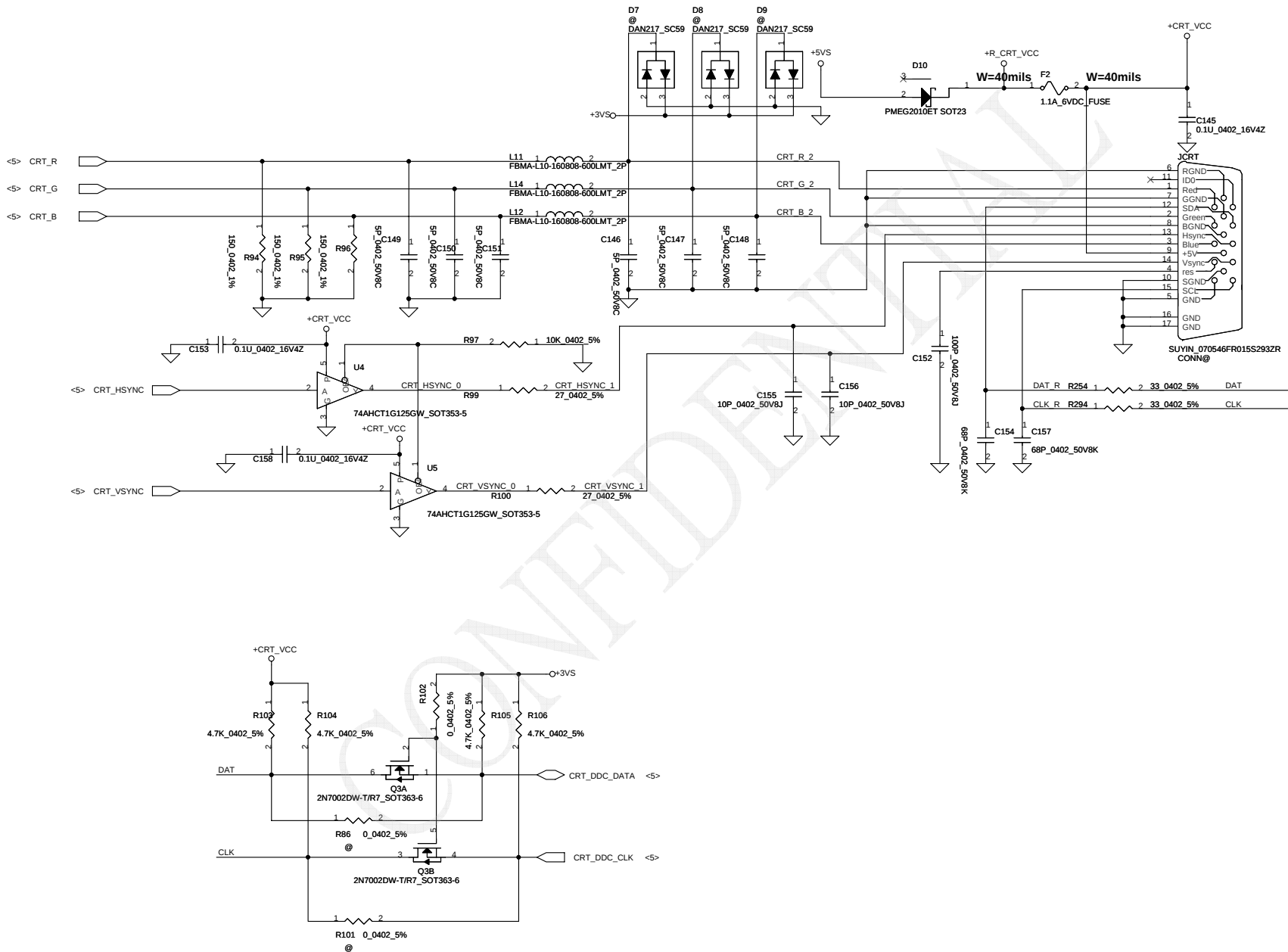


HDMI C_CLK+	@	R65	1	2	0.0402_5%	HDMI_CLK+ CONN
HDMI C_CLK-	@	R66	1	2	0.0402_5%	HDMI_CLK- CONN
HDMI C_TX0+	@	R67	1	2	0.0402_5%	HDMI_TX0+ CONN
HDMI C_TX0-	@	R68	1	2	0.0402_5%	HDMI_TX0- CONN
HDMI C_TX1+	@	R71	1	2	0.0402_5%	HDMI_TX1+ CONN
HDMI C_TX1-	@	R72	1	2	0.0402_5%	HDMI_TX1- CONN
HDMI C_TX2+	@	R73	1	2	0.0402_5%	HDMI_TX2+ CONN
HDMI C_TX2-	@	R75	1	2	0.0402_5%	HDMI_TX2- CONN



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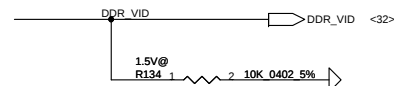
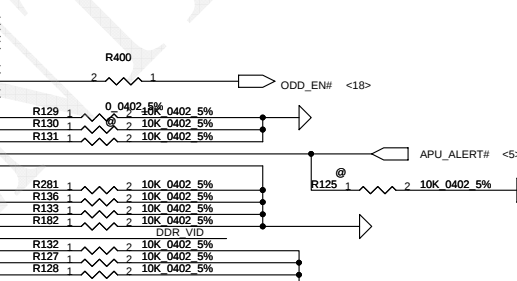
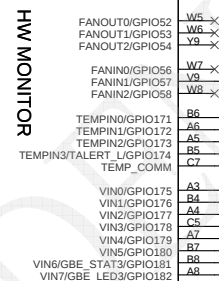
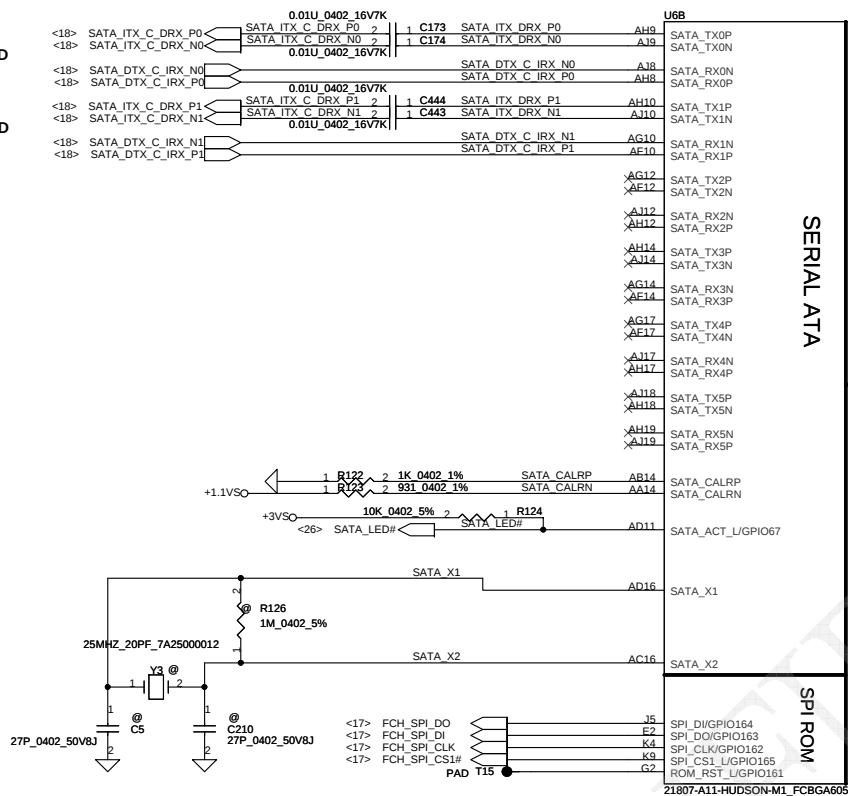
CRT Connector



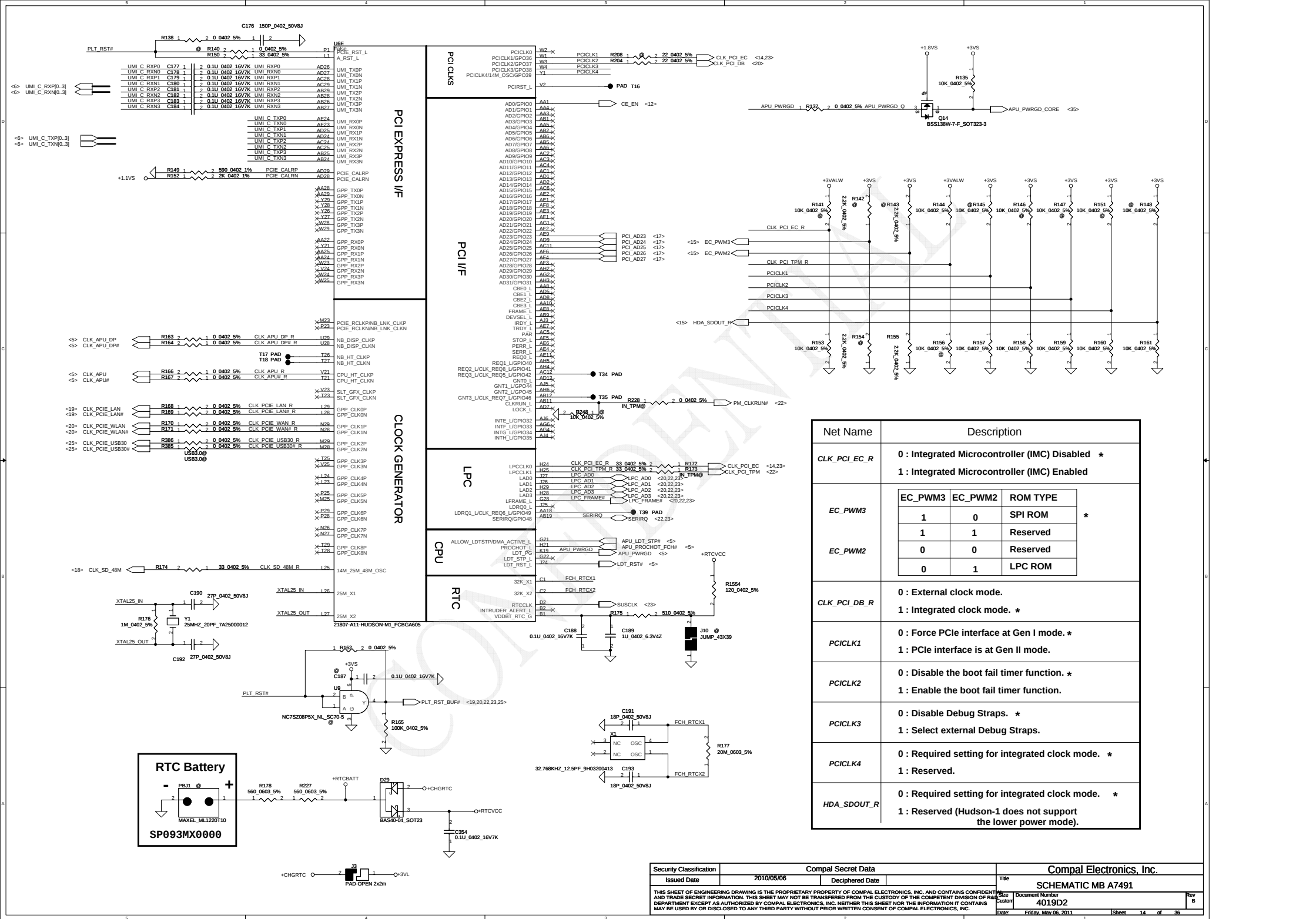
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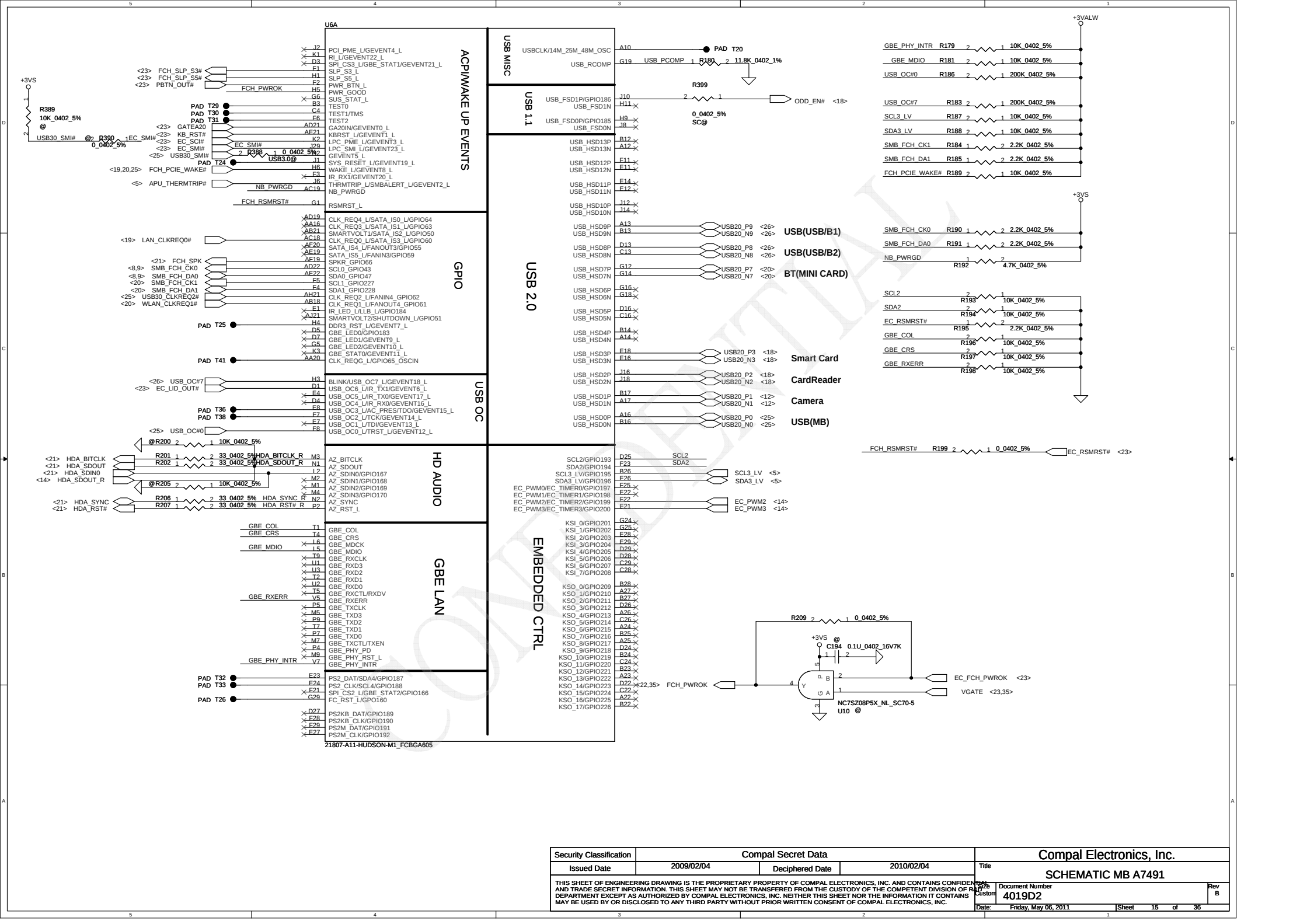
SATA for HDD

SATA for ODD

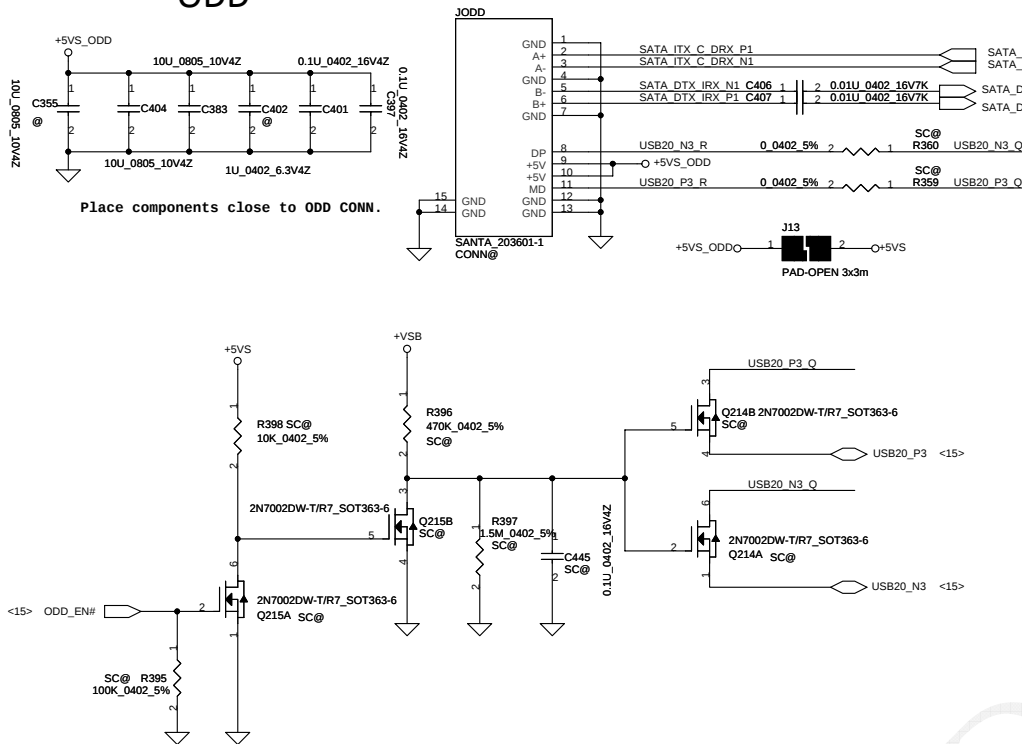


DDR_VID	DDR voltage
0	+1.5V
1	+1.35V

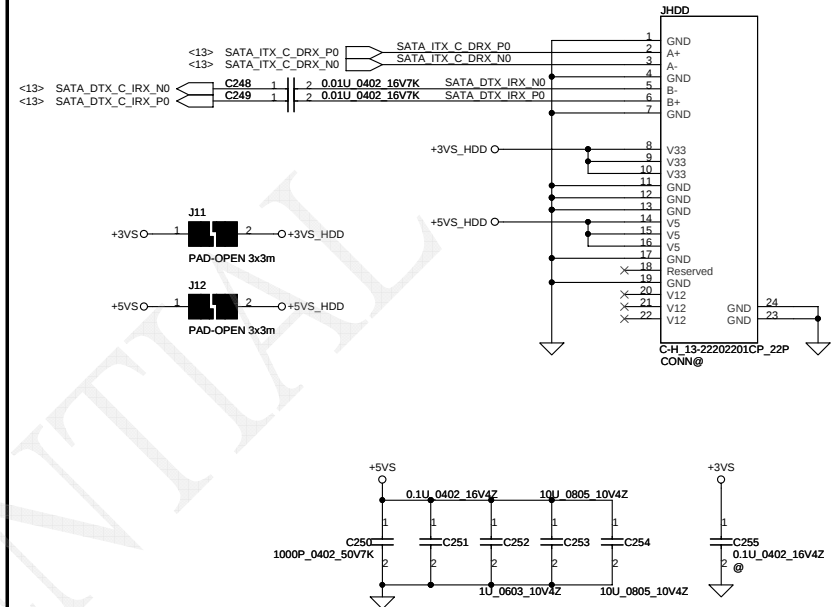




ODD

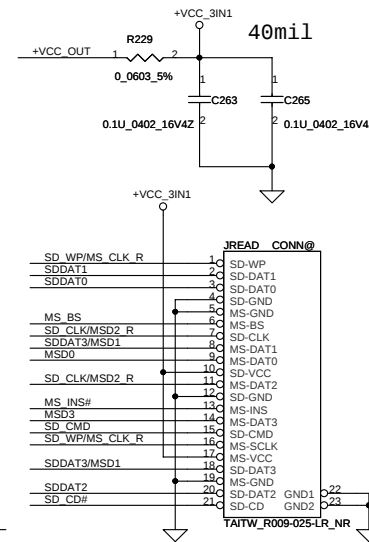
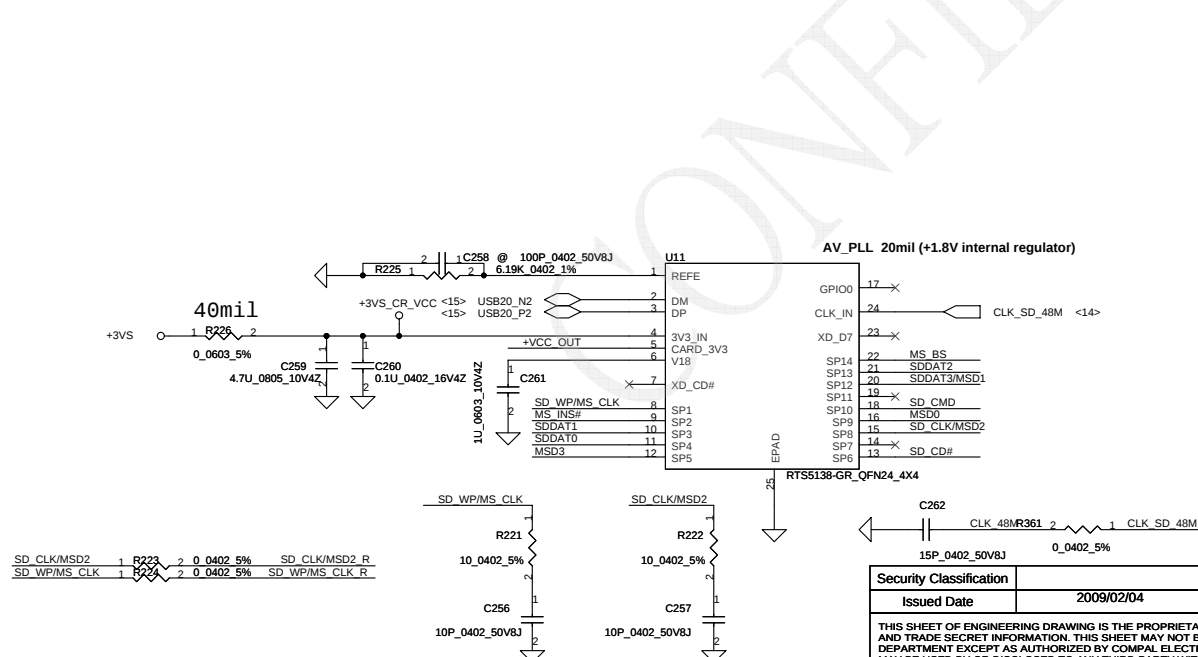


HDD



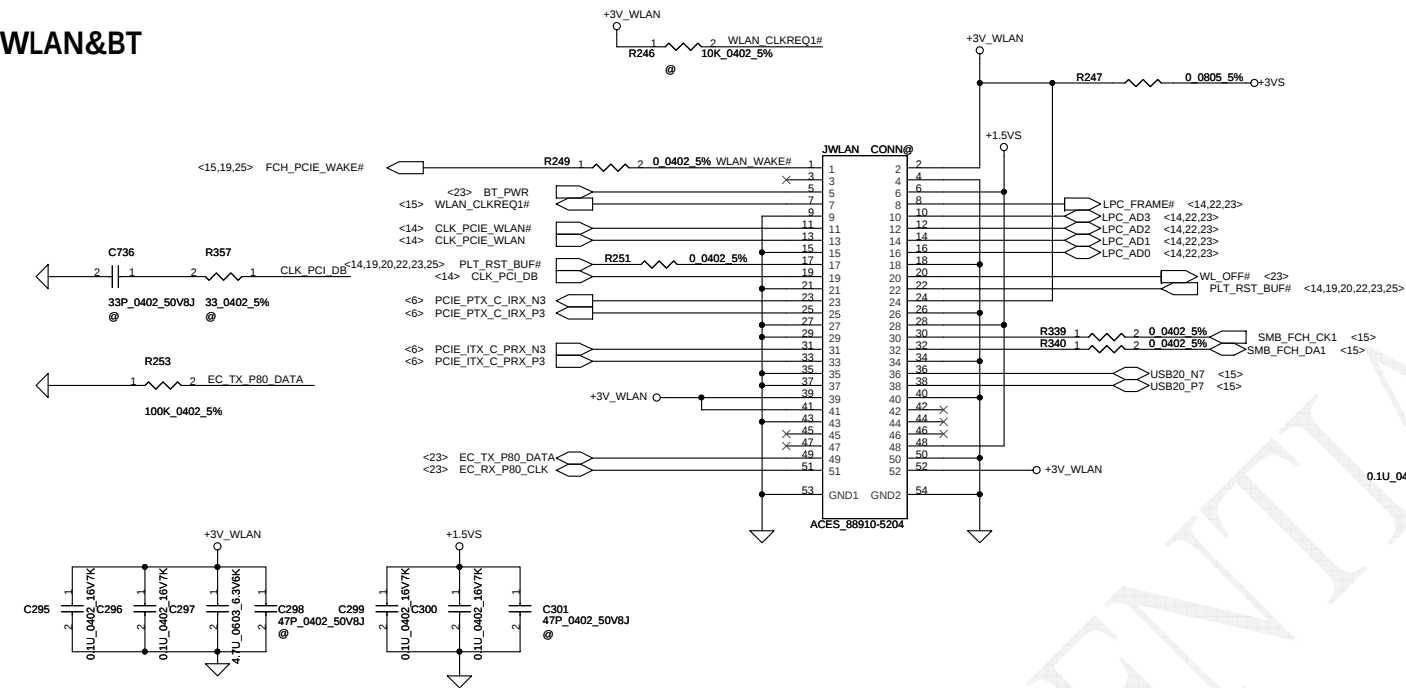
SD, MMC, MS multi-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1	SP1		SP1
SP2			
SP3			
SP4			
SP5			
SP6			
SP7			
SP8			
SP9			
SP10			
SP11			
SP12			
SP13			
SP14			
SP15			
SP16			
SP17			
SP18			
SP19			

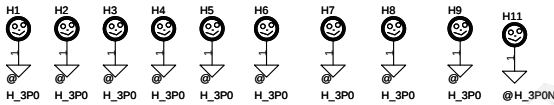


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WLAN&BT



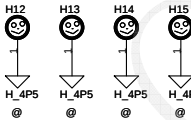
Screw Hole



NPTH



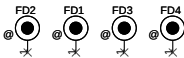
CPU



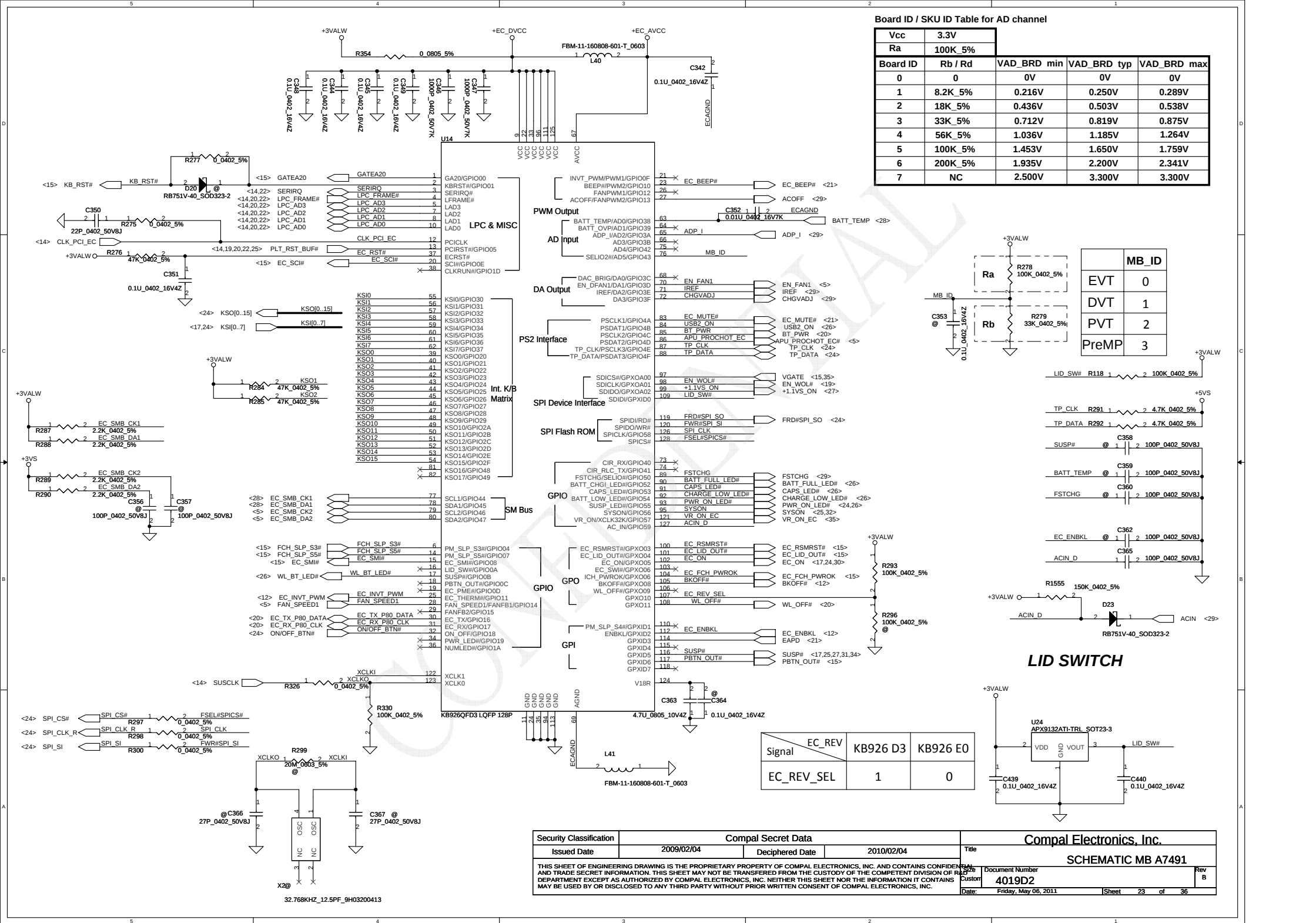
JWLAN

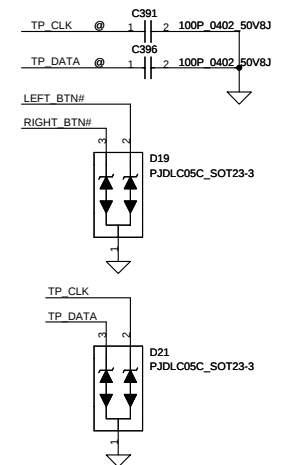
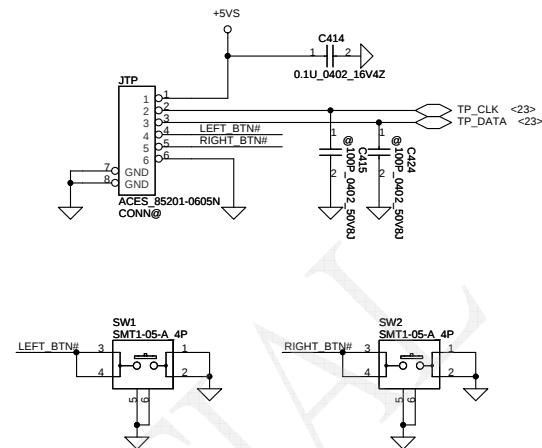
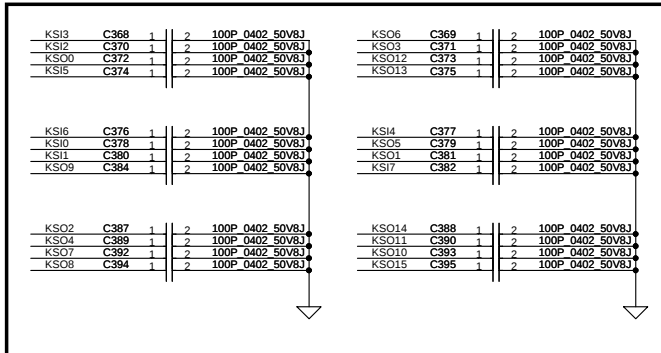


PCB Fedical Mark PAD



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SPI CLK R 1 2 @ 1 2 C400 @
0_0402_5% R304 22P_0402_50V8J

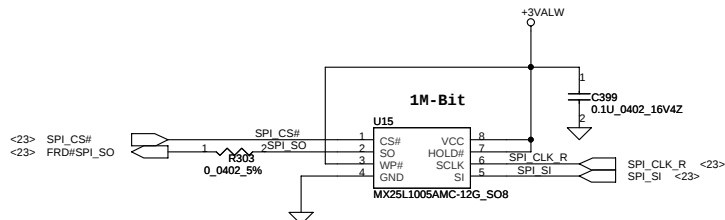
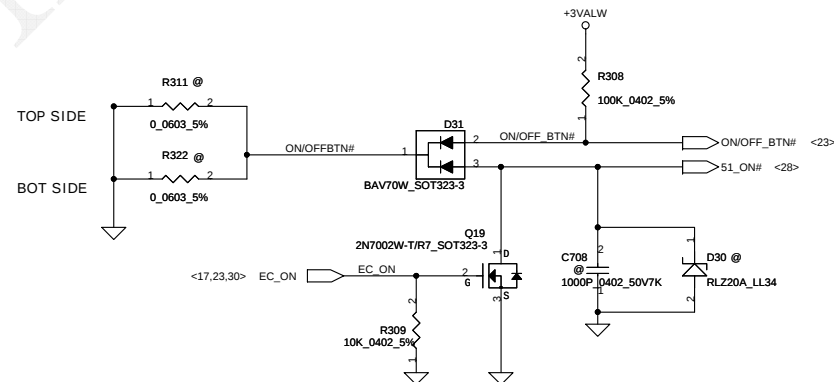


Diagram illustrating the Pin 1 connection for the ACES_85201-0605N component. The component is a 6-pin connector. The connections are as follows:

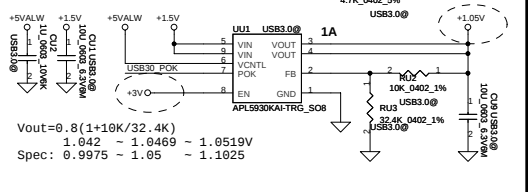
- Pin 1: +5VALW
- Pin 2: PWR_ON_LED# (<23.26>)
- Pin 3: ON/OFFBTN#
- Pin 4: GND
- Pin 5: GND
- Pin 6: GND

The component is labeled ACES_85201-0605N and CONN@.

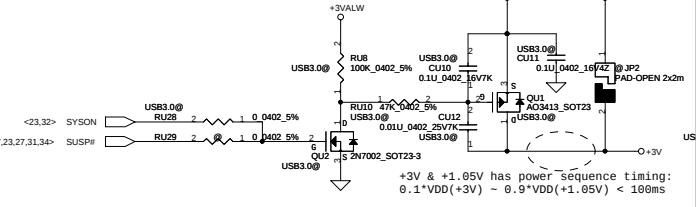


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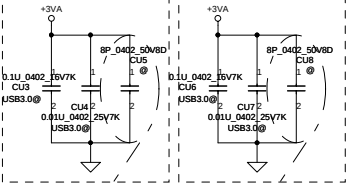
+1.5V to +1.05V Transfer



+3VALW to +3V Transfer

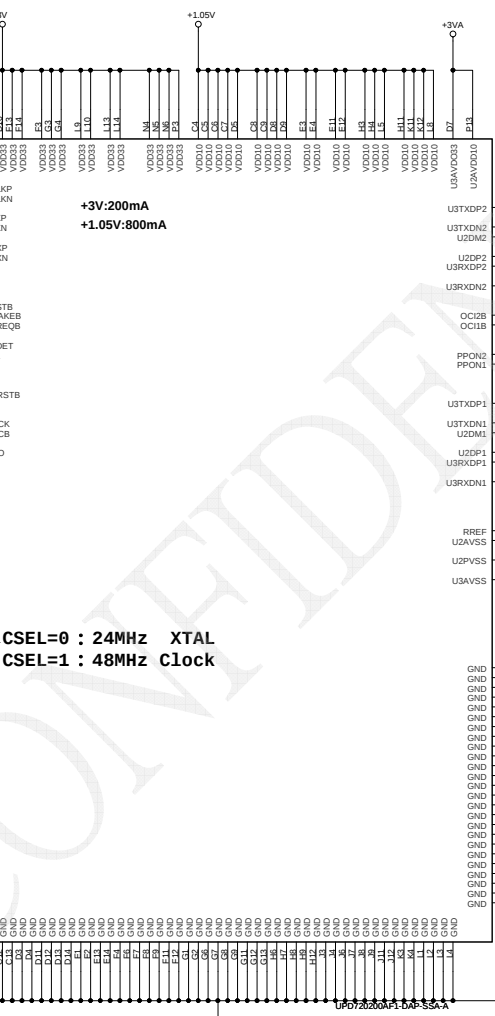


Close to U102.D7 Close to U102.P13



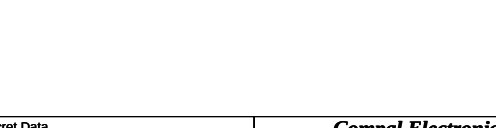
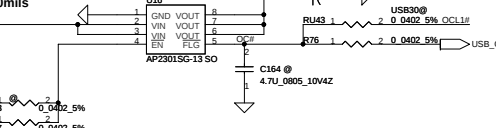
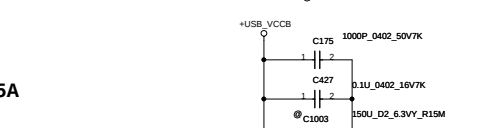
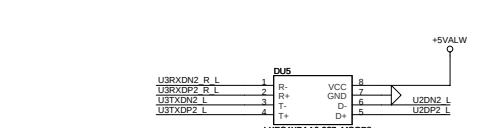
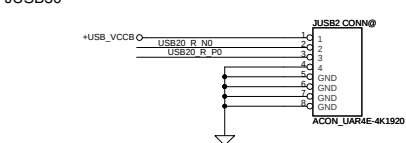
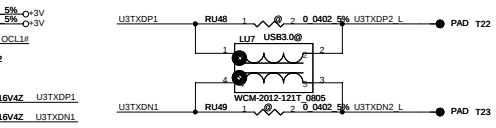
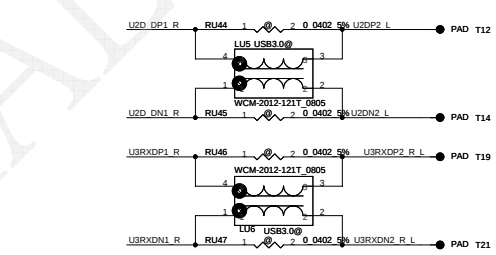
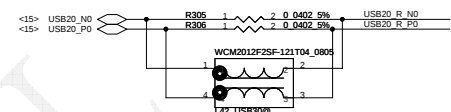
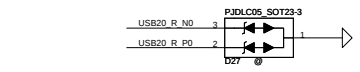
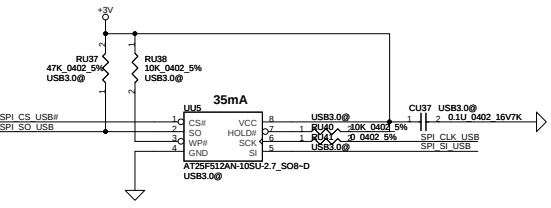
Follow Vendor recommend.

**+3V:200mA
+1.05V:800mA**



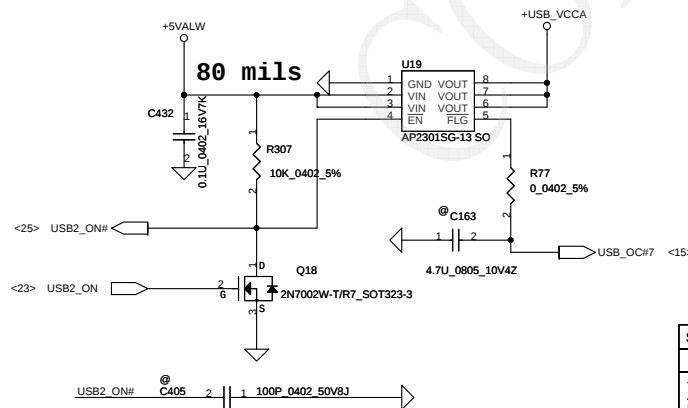
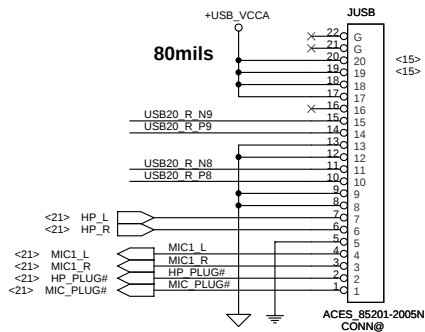
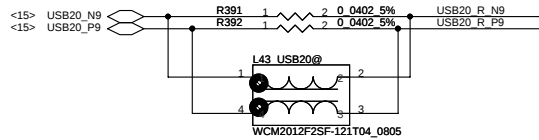
**CSEL=0 : 24MHz XTAL
CSEL=1 : 48MHz Clock**

Place as close as possible to U2.N14 and U2.M14



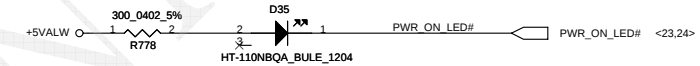
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USB/B Conn

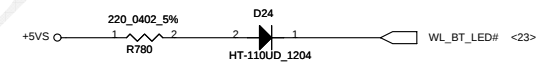


LEDs

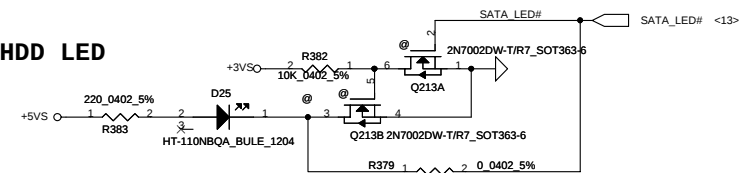
Power on LED



WL&BT LED



HDD LED



BATT LED

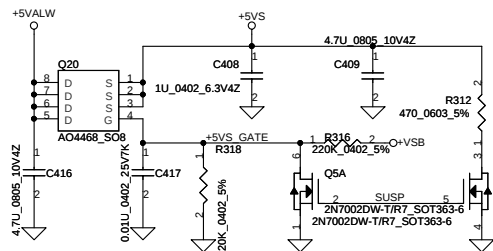


CAP LOCK LED

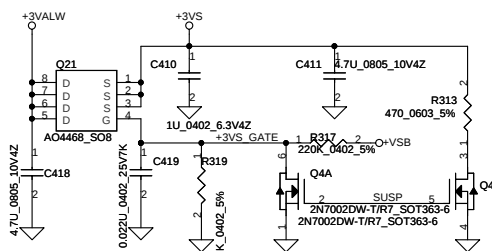


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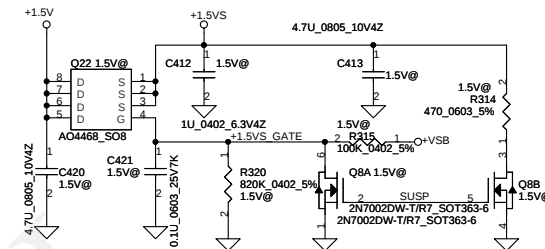
+5VALW TO +5VS



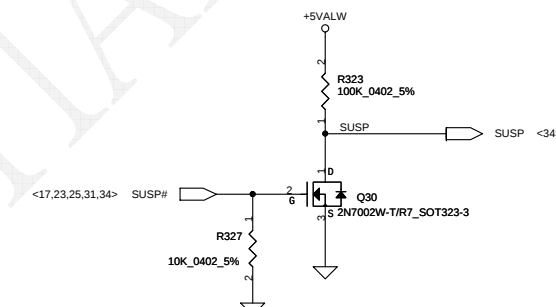
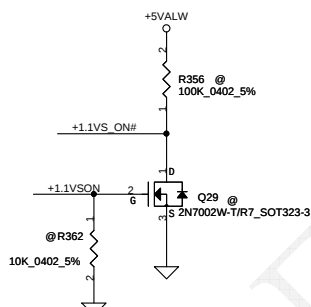
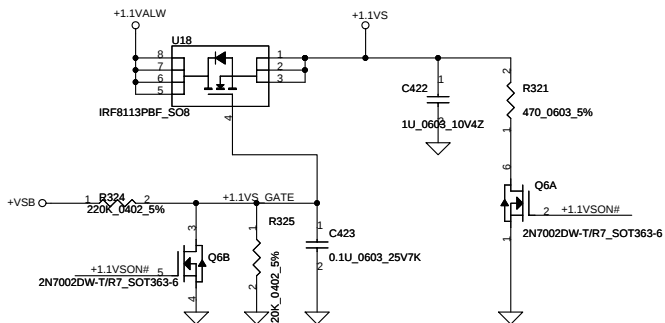
+3VALW TO +3VS



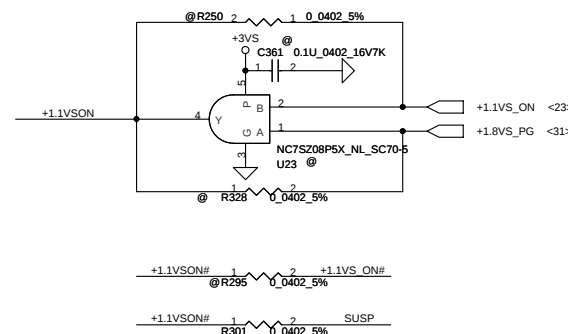
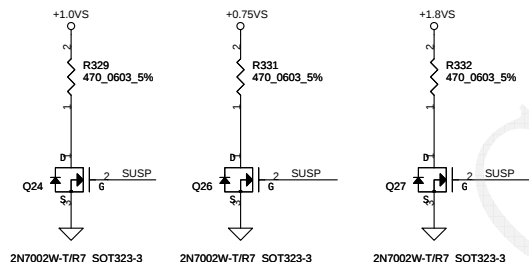
+1.5V TO +1.5VS



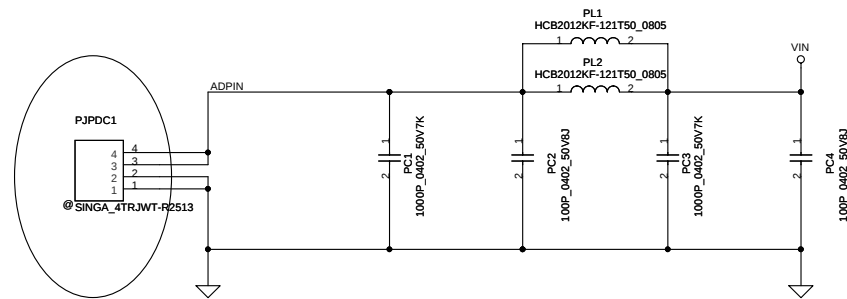
+1.1VALW TO +1.1VS



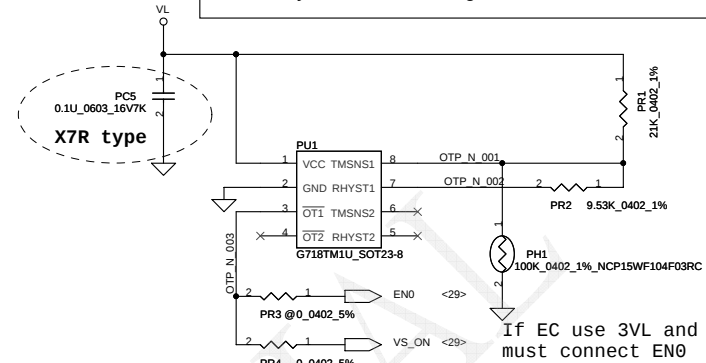
DISCHARGE



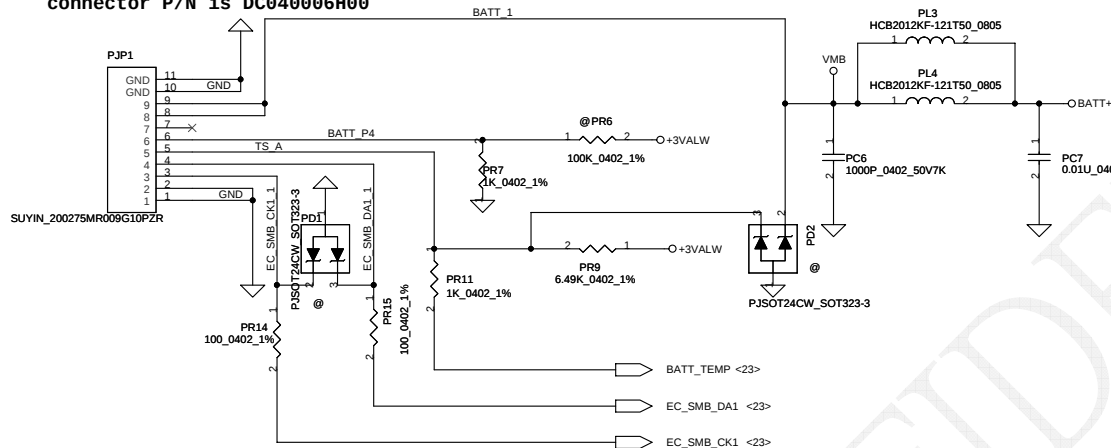
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PH1 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

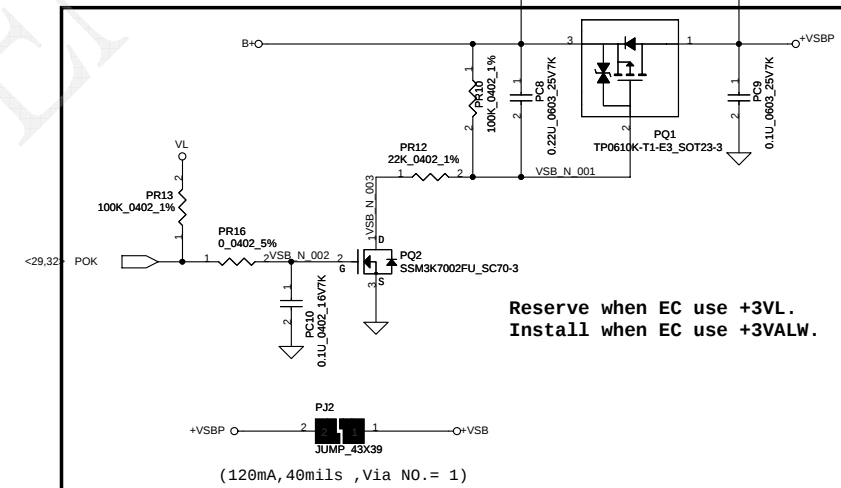


need confirm: ME give us battery
connector P/N is DC040006H00

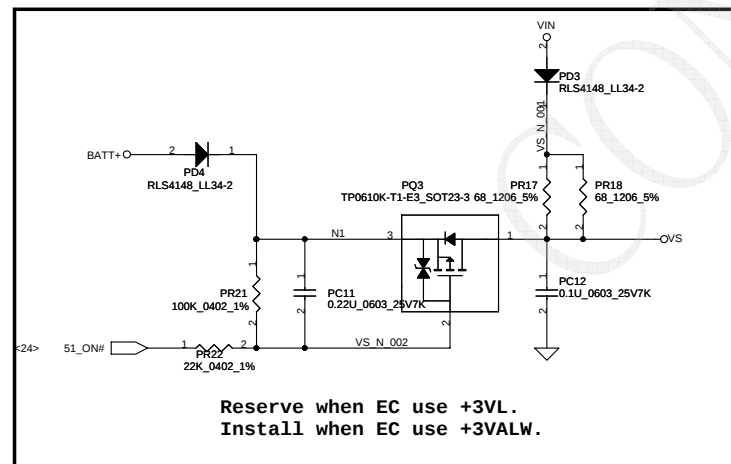


Install when EC use +3VL
and SUSP was Pull high to +3VL.

Reserve when EC use +3VALW.

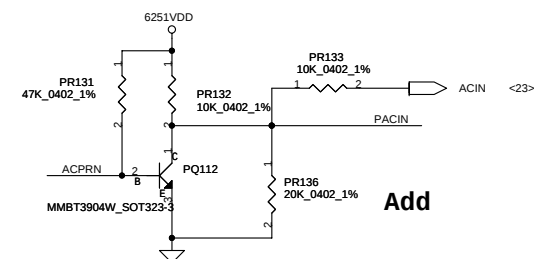


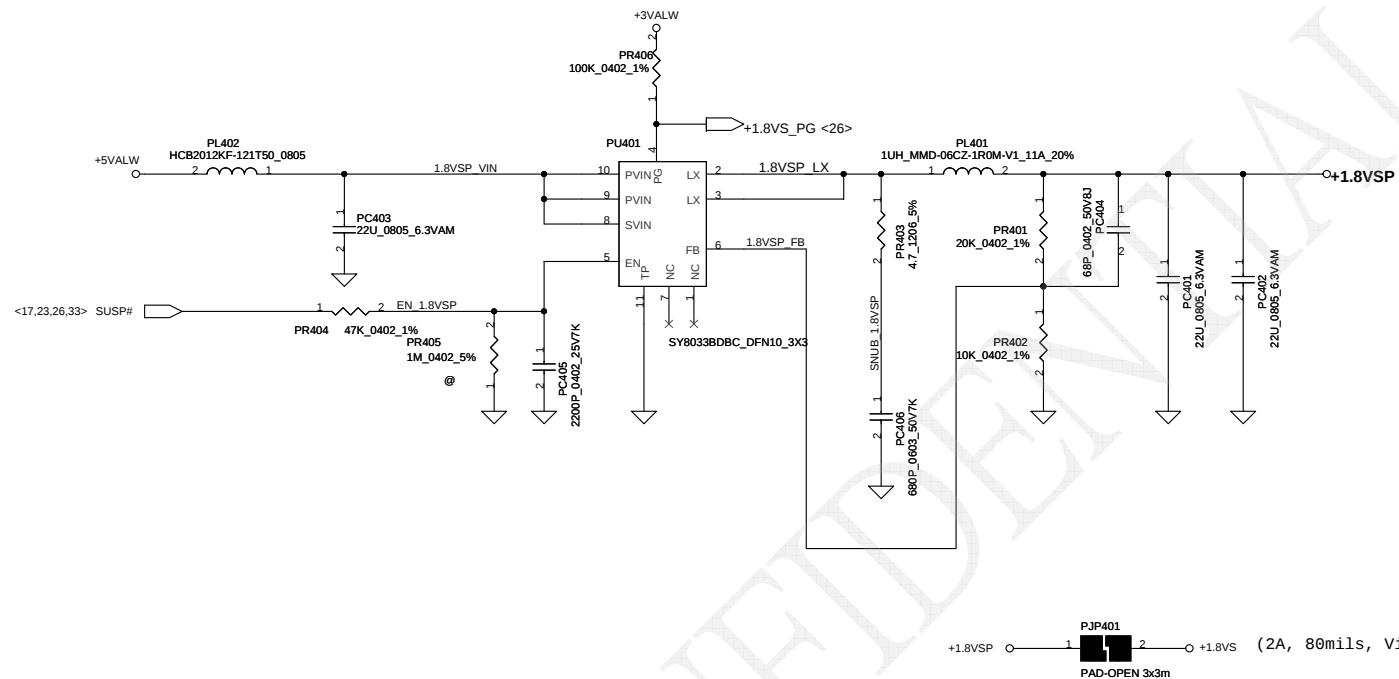
Reserve when EC use +3VL.
Install when EC use +3VALW.



Reserve when EC use +3VL.
Install when EC use +3VALW.

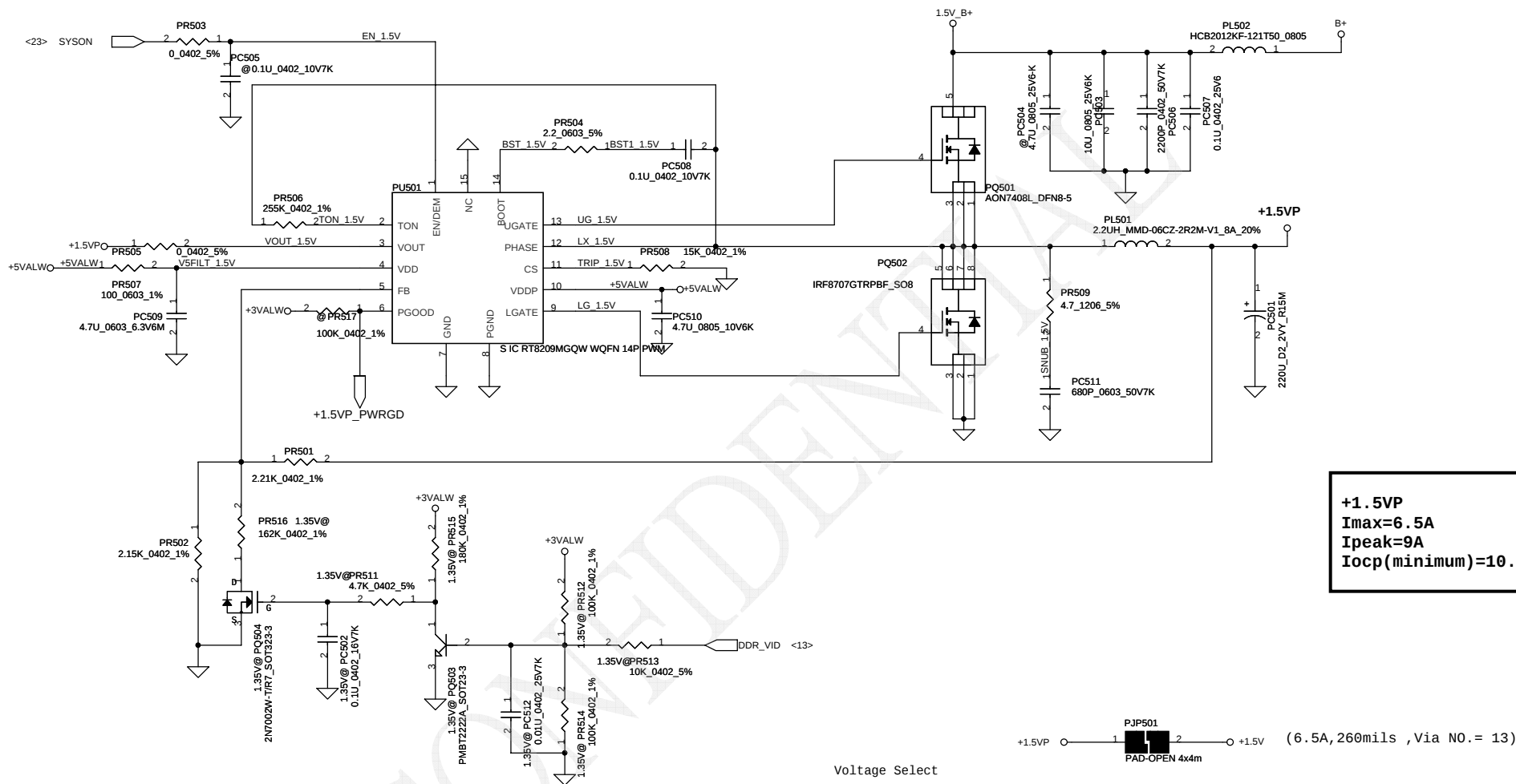
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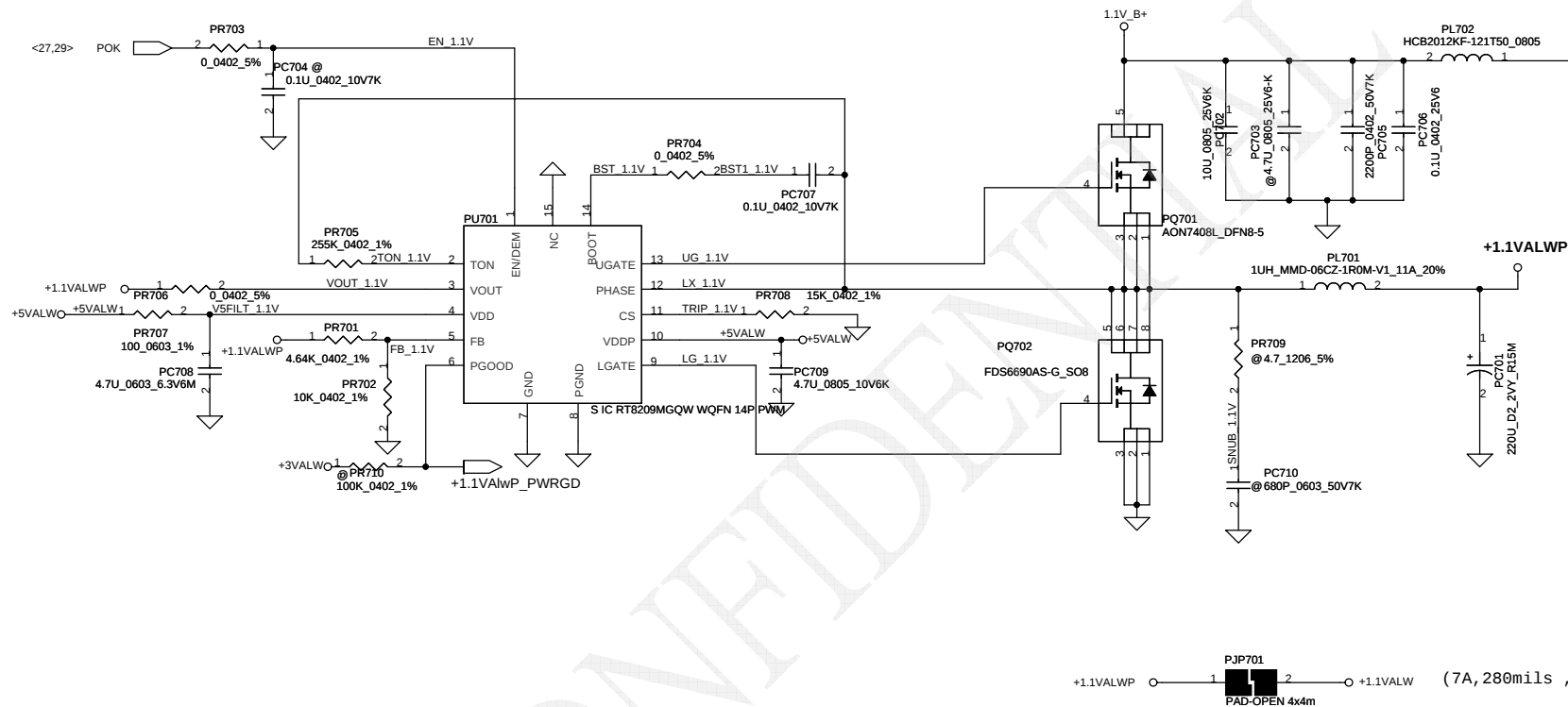




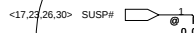
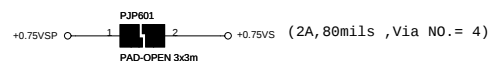
$$V_0 = V_{FB} * (1 + PR401 / PR402) = 0.6 * (1 + 20K / 10K) = 1.8V$$

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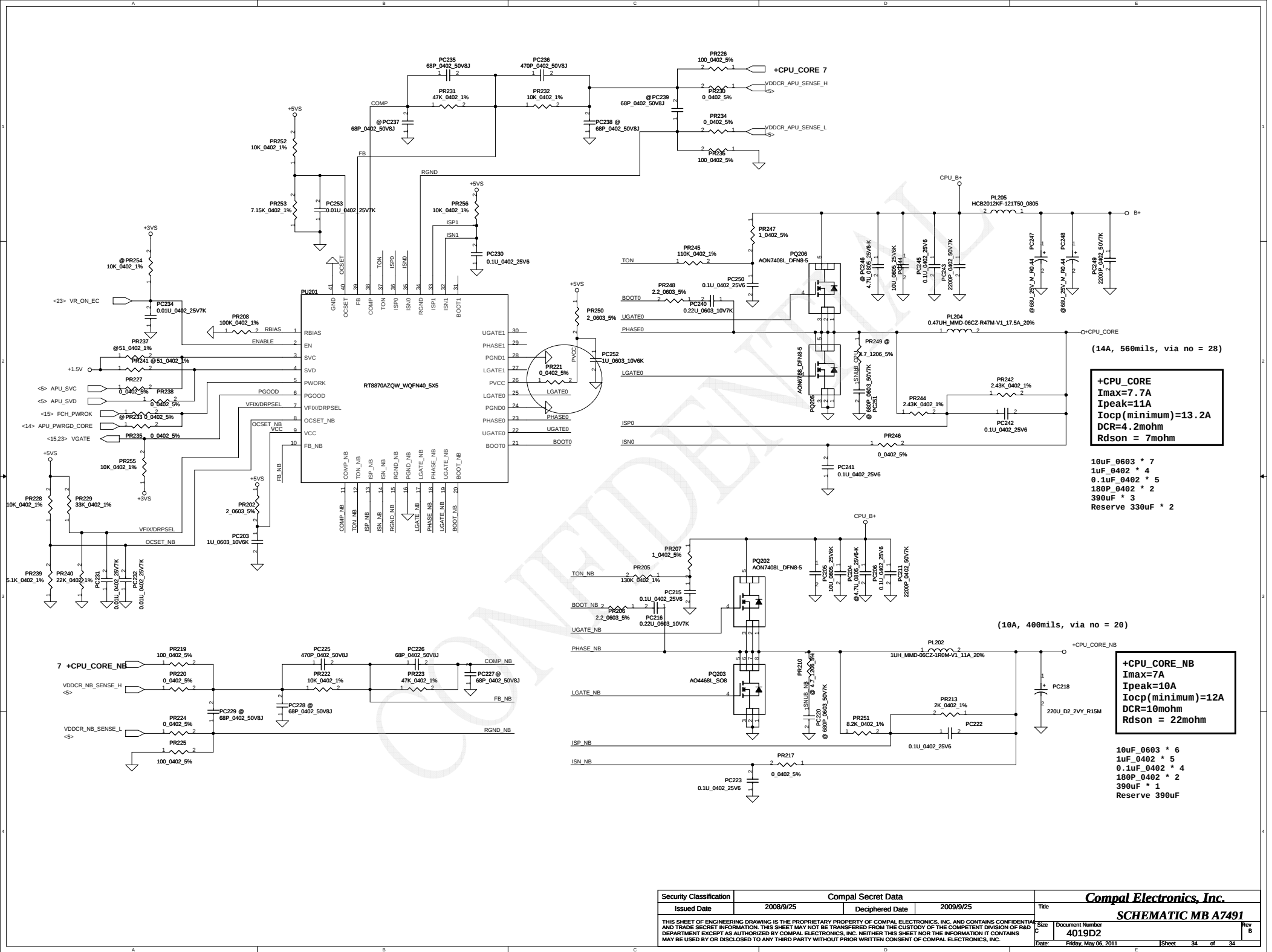




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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Reason for change	Description	phase	modify	Rev.
1	31	Follow EMI request to add PR54, PR59, PC511 for EMI issue.	add PR54, PR59, PC511	PVT	add PR54, PR59, PC511	
2	34	Follow ME request change PQ205 for height issue	Change PQ205 from AO4726L AON6788	PVT	Change PQ205 from AO4726L AON6788	
3	28	For common desgin	Delete PC107	Pre-MP	Remove PC107	
4	28	For common desgin	PR110 from 47K change to 200K	Pre-MP	PR110 from 47K change to 200K	
5	28	For common desgin	PR112 from 10K change to 47K	Pre-MP	PR110 from 10K change to 47K	
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