

COMPAL CONFIDENTIAL

MODEL NAME : QAM00
PCB NO : LA-7731P
BOM P/N : 4319ET31L01
GPIO MAP:

Dalmore 12 UMA

Ivy Bridge + Panther POINT
2011-8-30
REV : 0.3 (X01)
@ : Nopop Component
CONN@ : Connector Component

MB Type	BOM P/N	
M/B SPI ROM		5@
TAA SPI ROM		6@
SATA re-driver with CD function		7@
Normal E-SATA re-driver		8@

MB PCB	
Part Number	Description
DA60000P700	PCB OFH LA-7731P REV0 M/B UMA

@HDMI Royalty	
Part Number	Description
RO0000002HM	HDMI Royalty

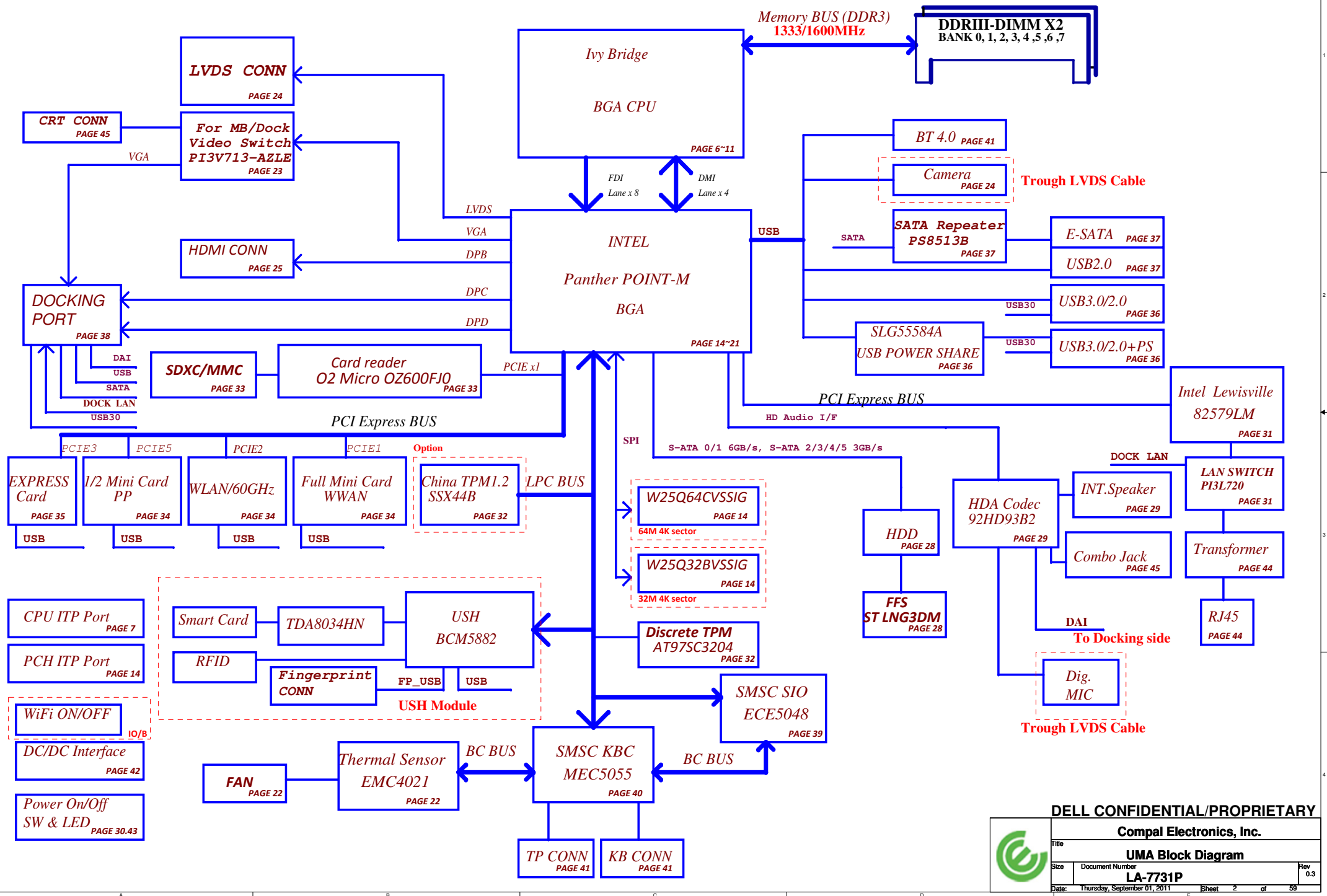
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Block Diagram



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UMA Block Diagram			
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.00
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
3	Slg 1		Copper foil	1oz	1.35
		4.7	Prepreg	7628HRC+2116HRCx2+7628HRC	23.60
4	Slg 2		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
5	GND/PWR		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
6	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.00
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)				47.6	46.32000

SATA	DESTINATION
SATA 0	HDD
SATA 1	NA
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side)
	1	JUSB2 (Bot side)
	2	NA
	3	MLK DOCK
	4	WLAN
	5	WWAN
	6	JMINI3(PP)
	7	USH->BIO
	8	DOCKING
	9	JESATA1 (Left)
	10	Express card
	11	Bluetooth
	12	Camera
	13	NA

USH	0	BIO
	1	NA

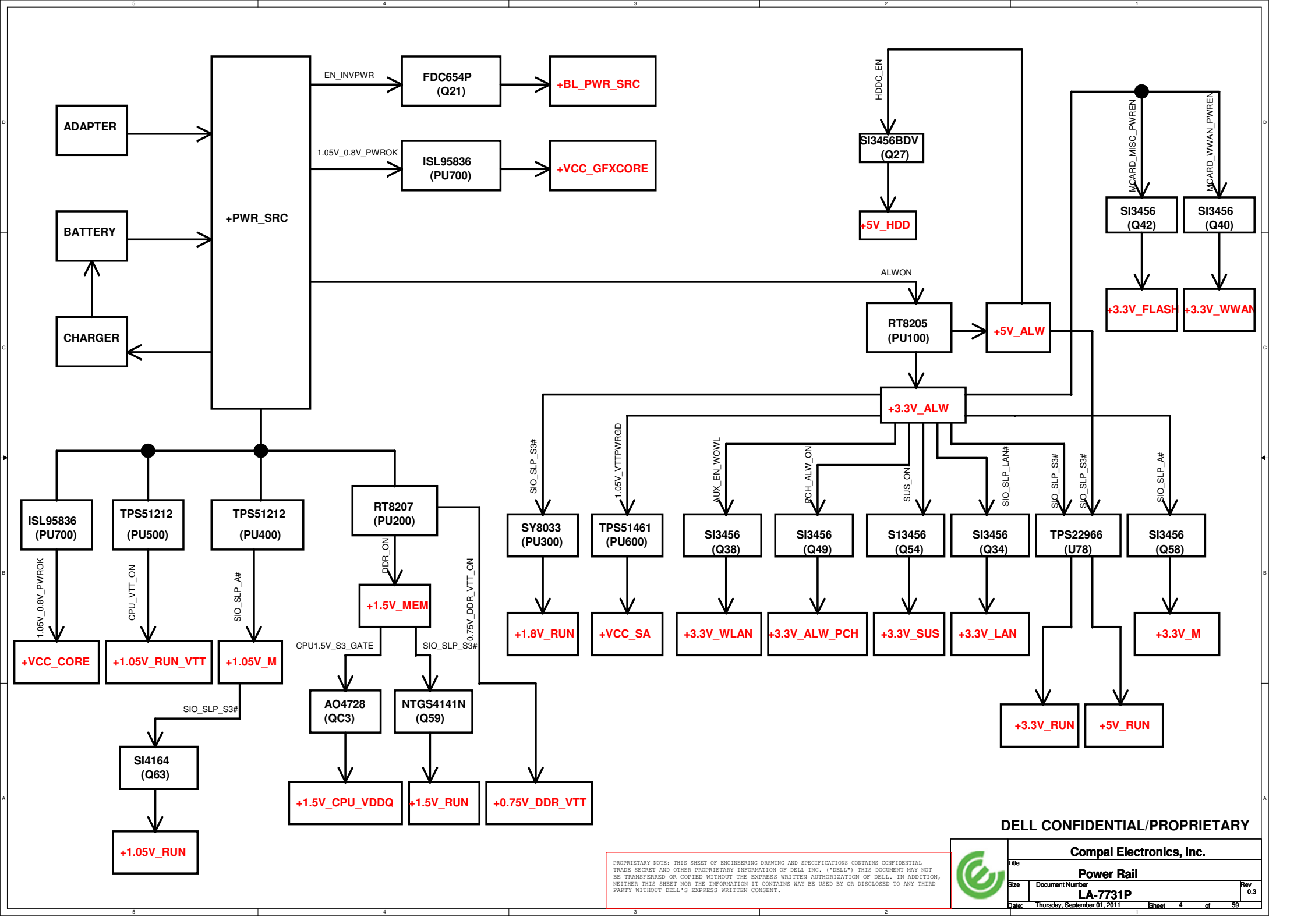
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	None
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

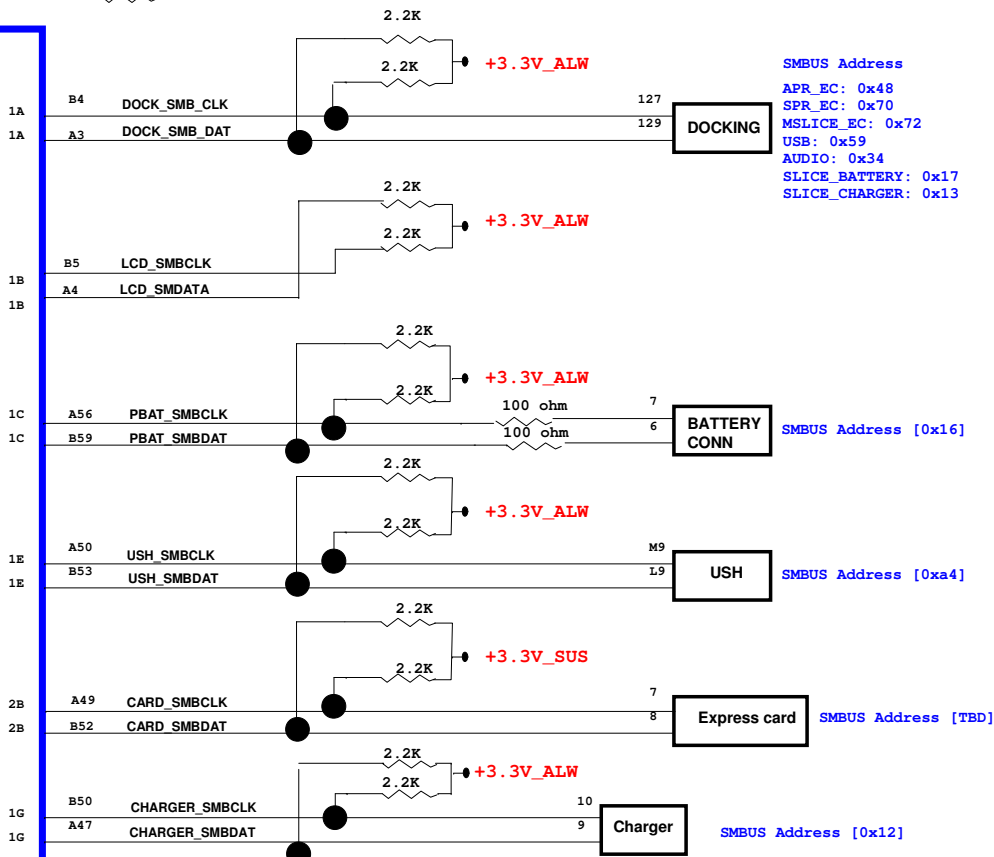
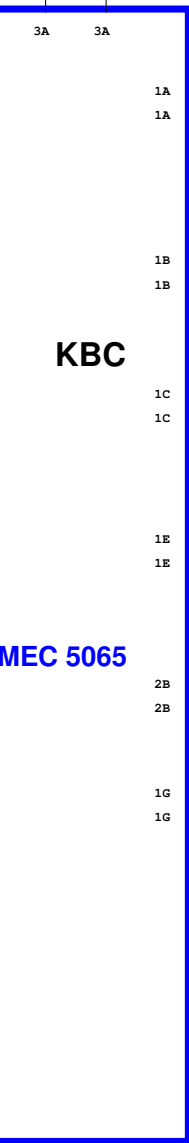
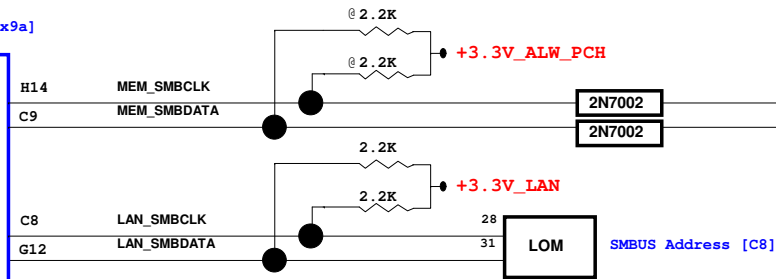
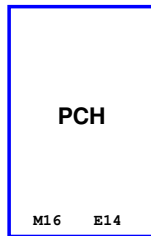
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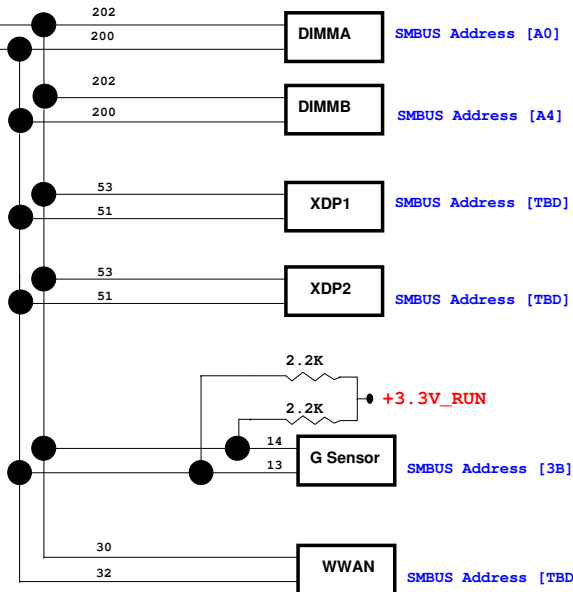
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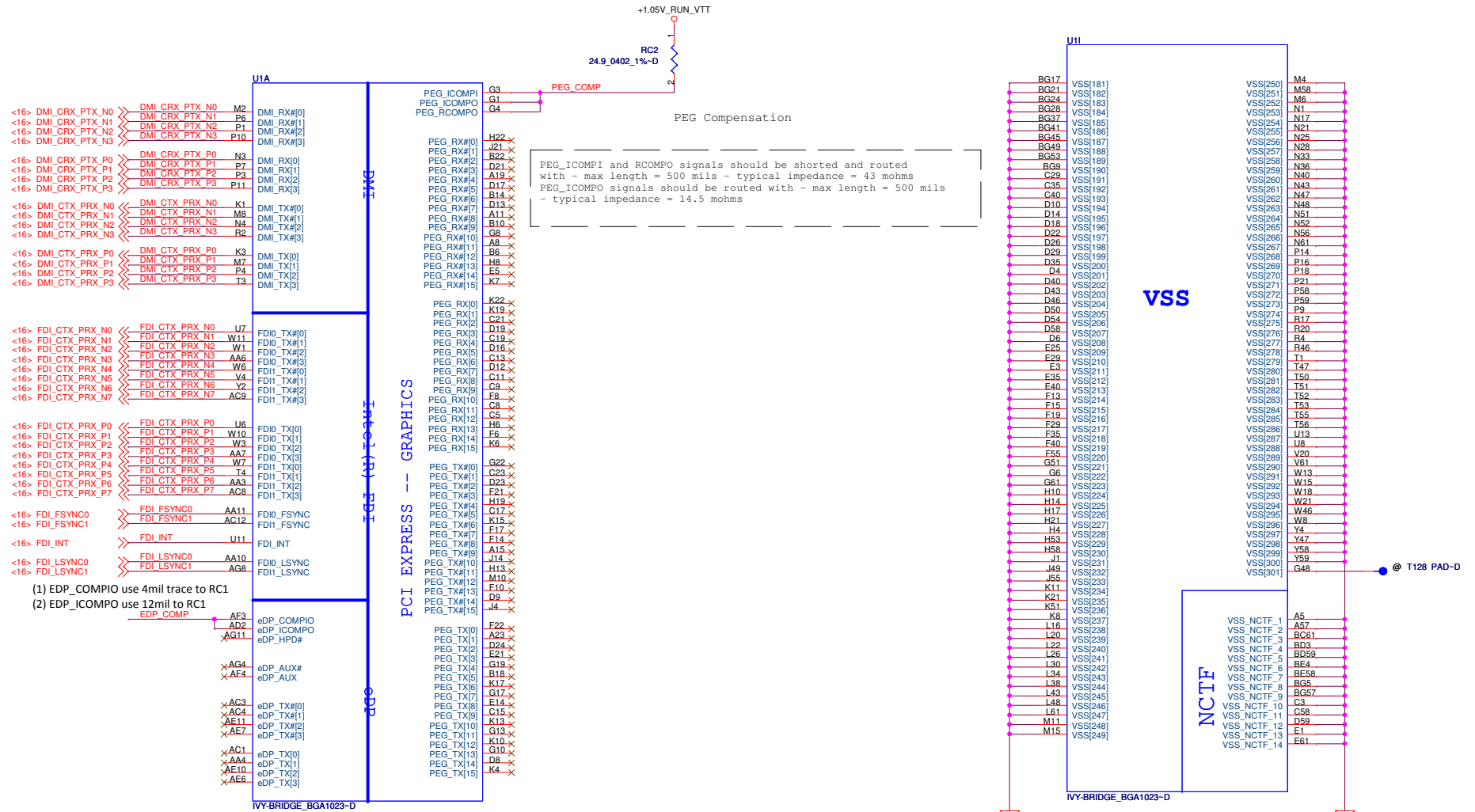
SMBUS Address [0x9a]



SMBUS Address
APR_EC: 0x48
SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13



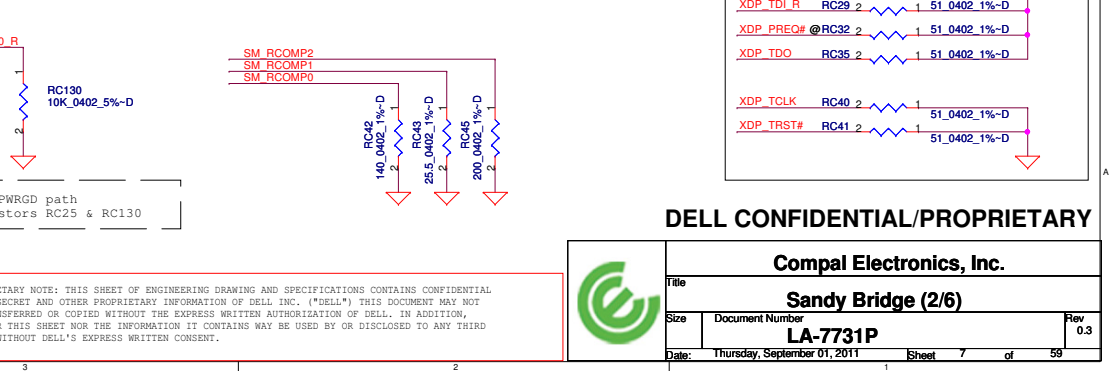
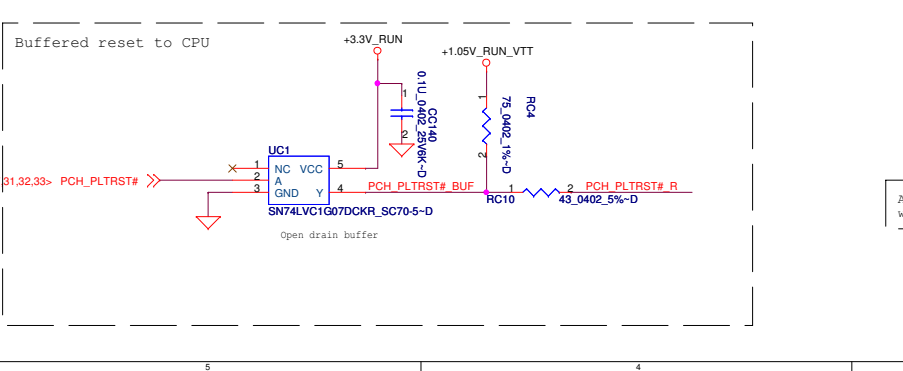
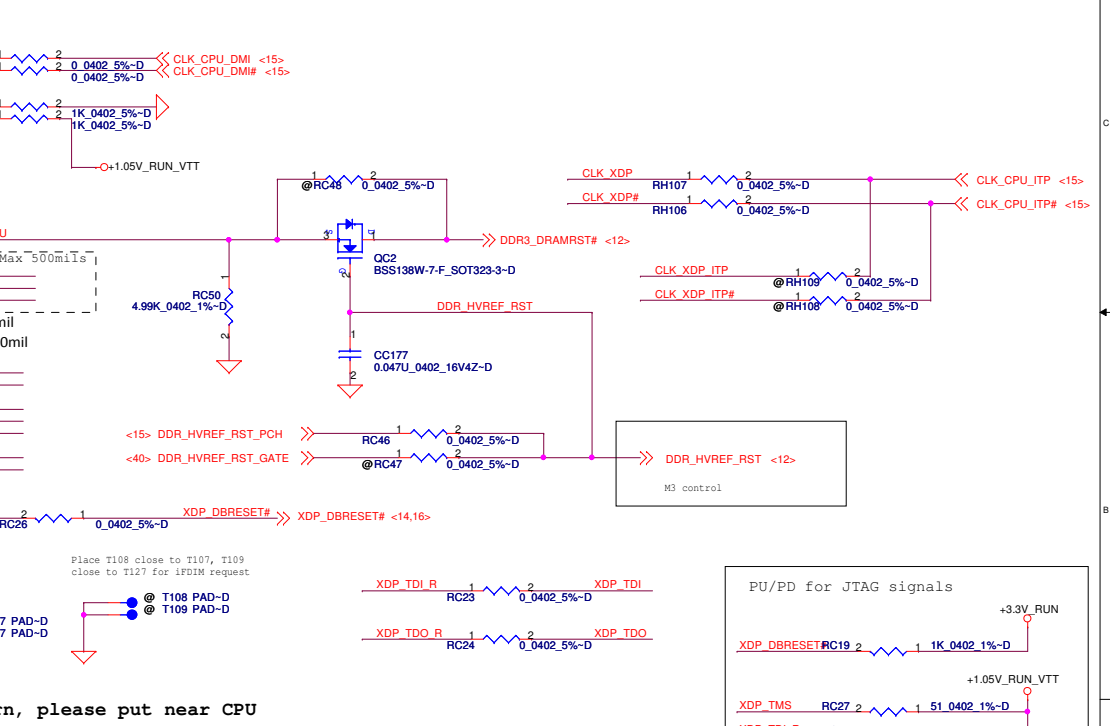
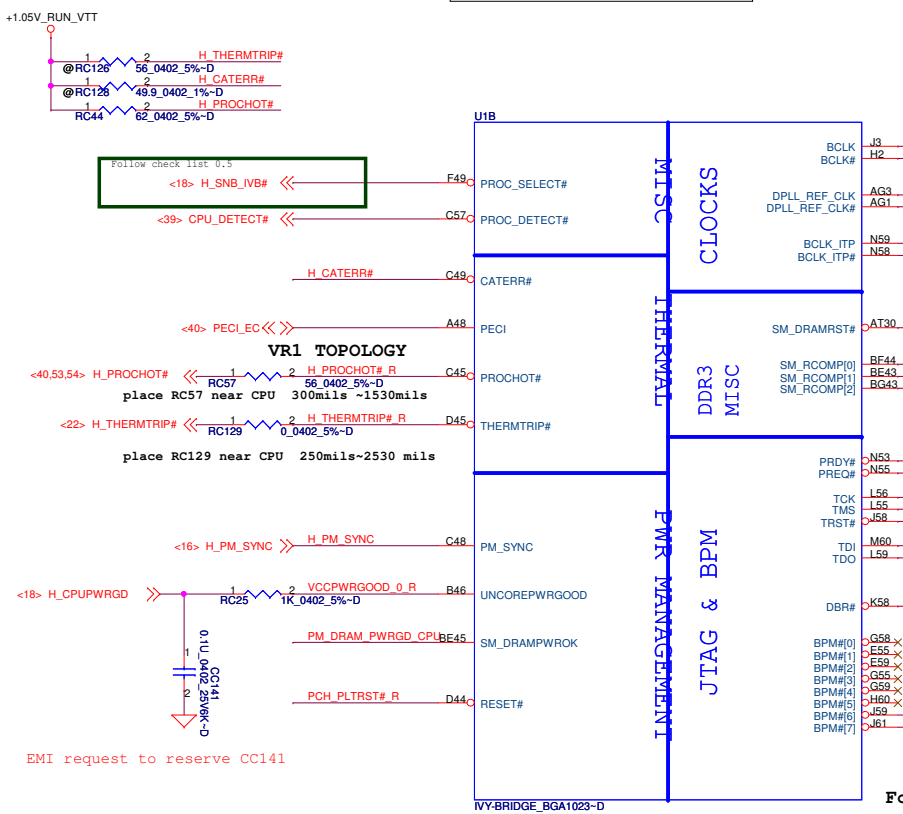
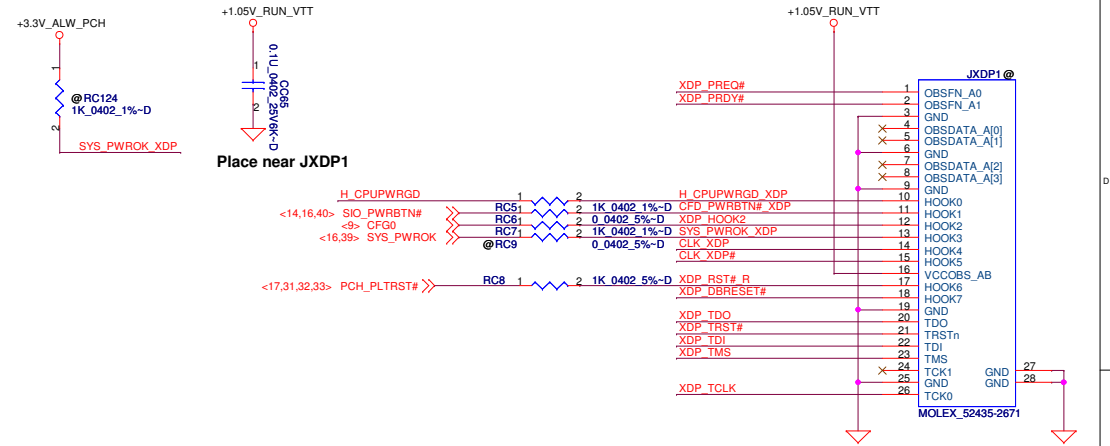
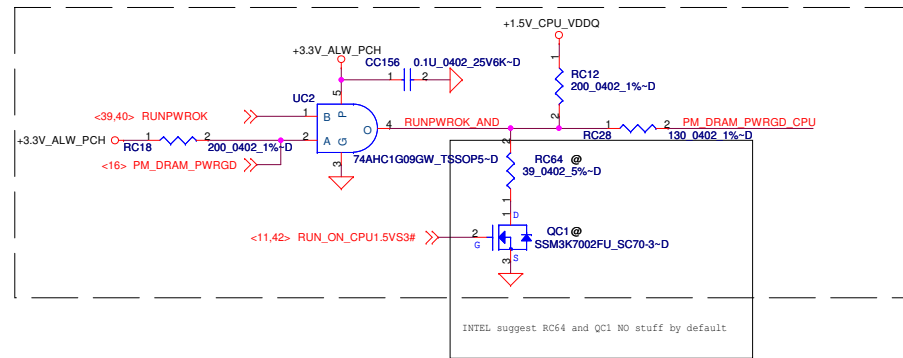
- (1) PEG_RCOMP (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
(2) PEG_ICOMPO use 12mil connect to RC2



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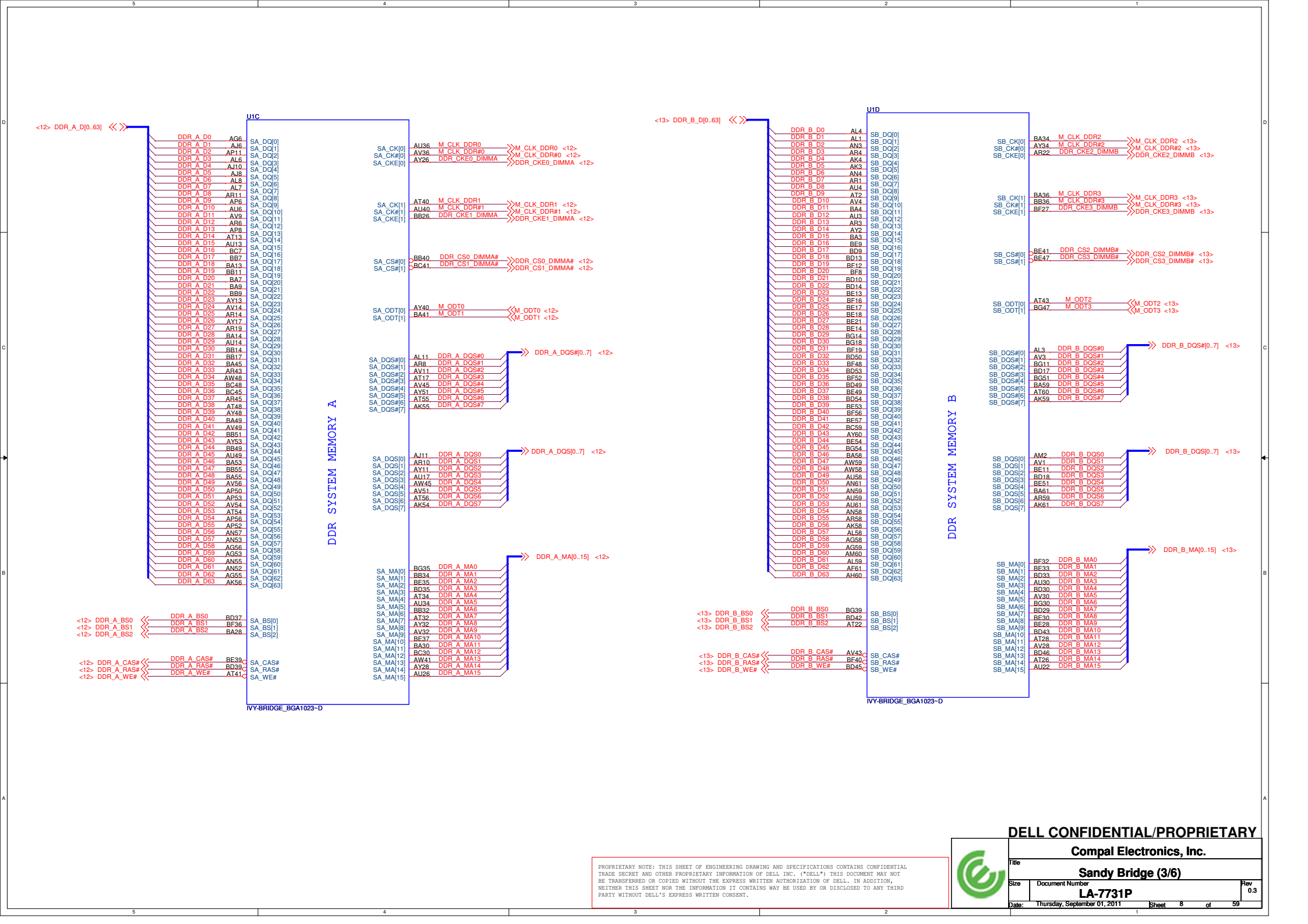
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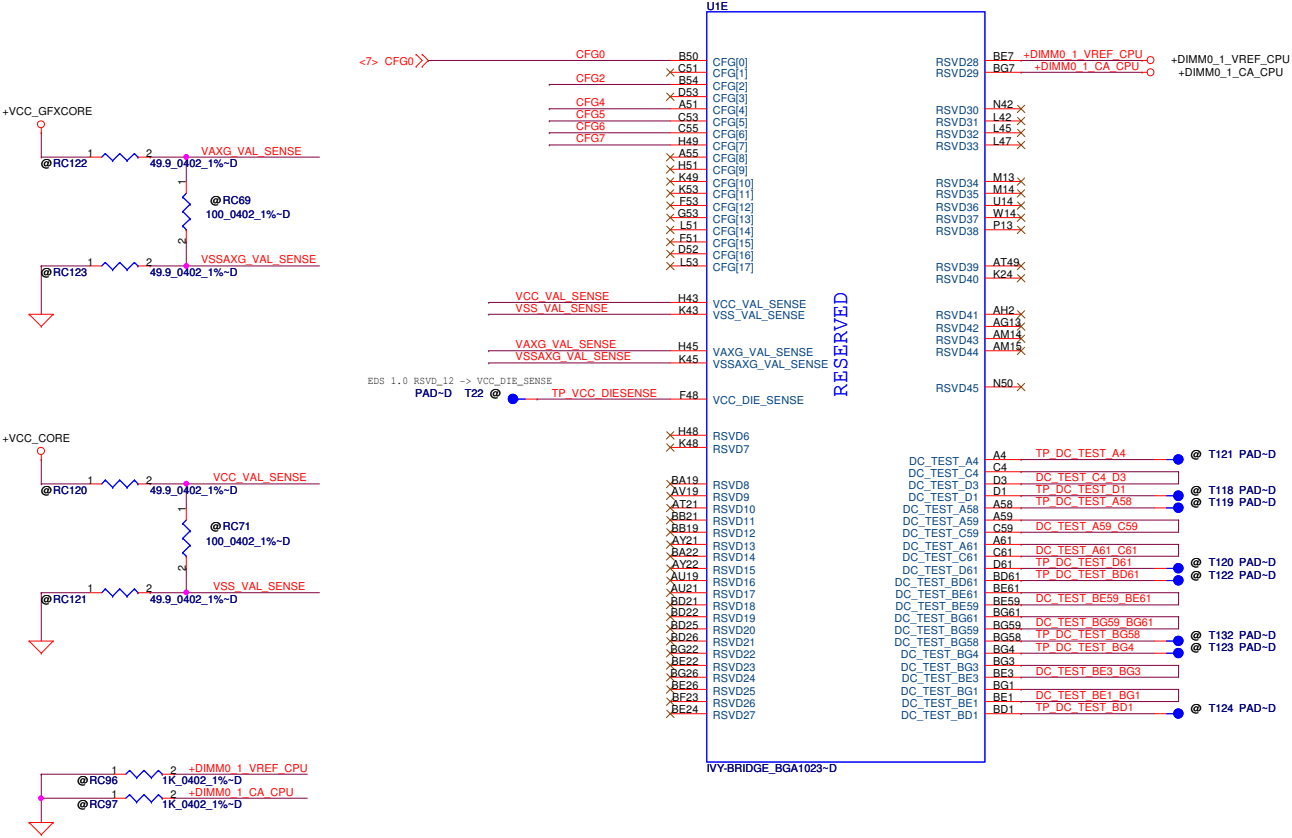
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Sandy Bridge (2/6)							
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CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training

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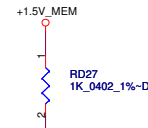
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Sandy Bridge (4/6)

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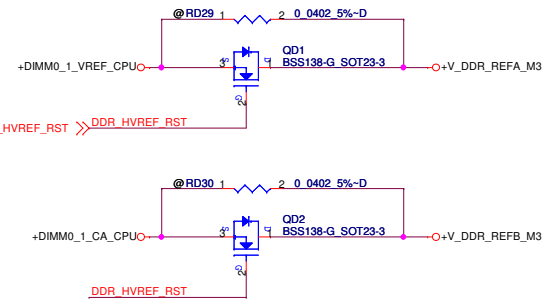
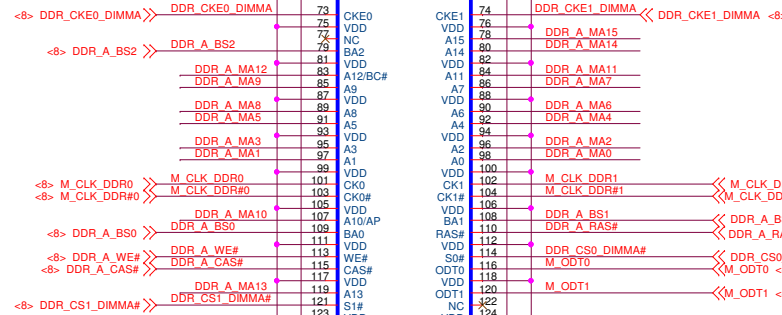
```
Populate RD1, De-Populate RD7 for Intel DDR3
VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3
```

All VREF traces should have 10 mil trace width

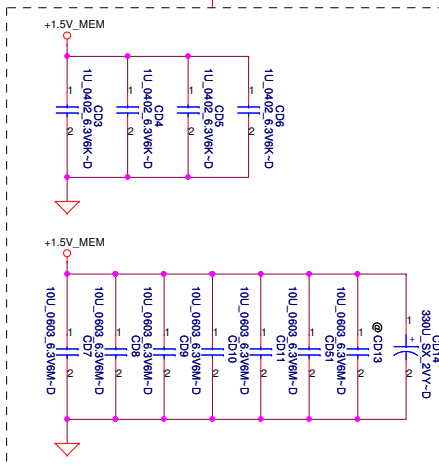


Layout Note:
Place near JDIMM1

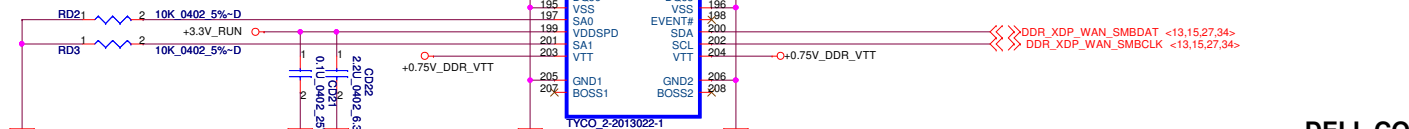
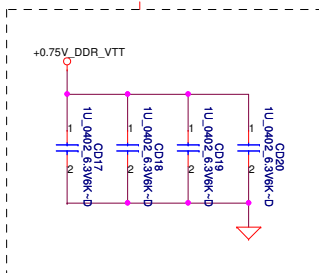
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



M3 Circuit (Processor Generated SO-DIMM VREF_DQ)



Layout Note:
Place near JDIMM1.203,204



CONN@

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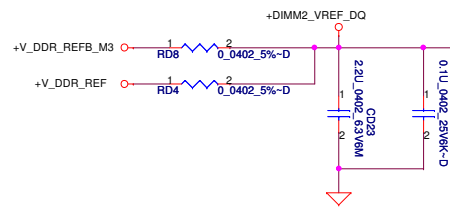
DDRIII-SODIMM SLOT1

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JDIMMB Reverse Type



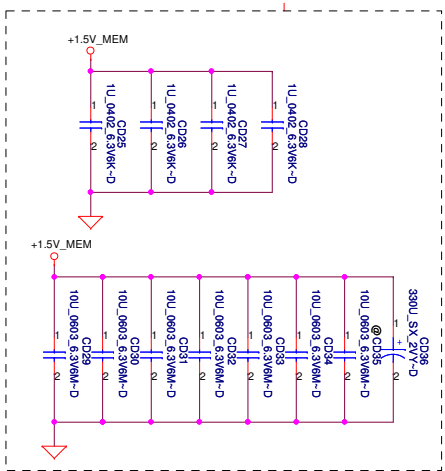
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3

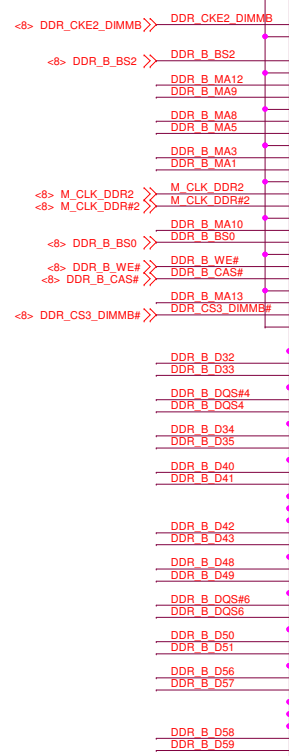
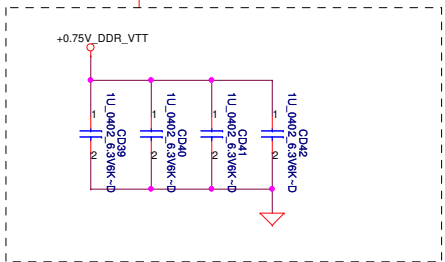
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<8> DDR_B_DQ[0.63] <<>
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<8> DDR_B_MA[0.15] <<>

All VREF traces should
have 10 mil trace width

Layout Note:
Place near JDIMM2

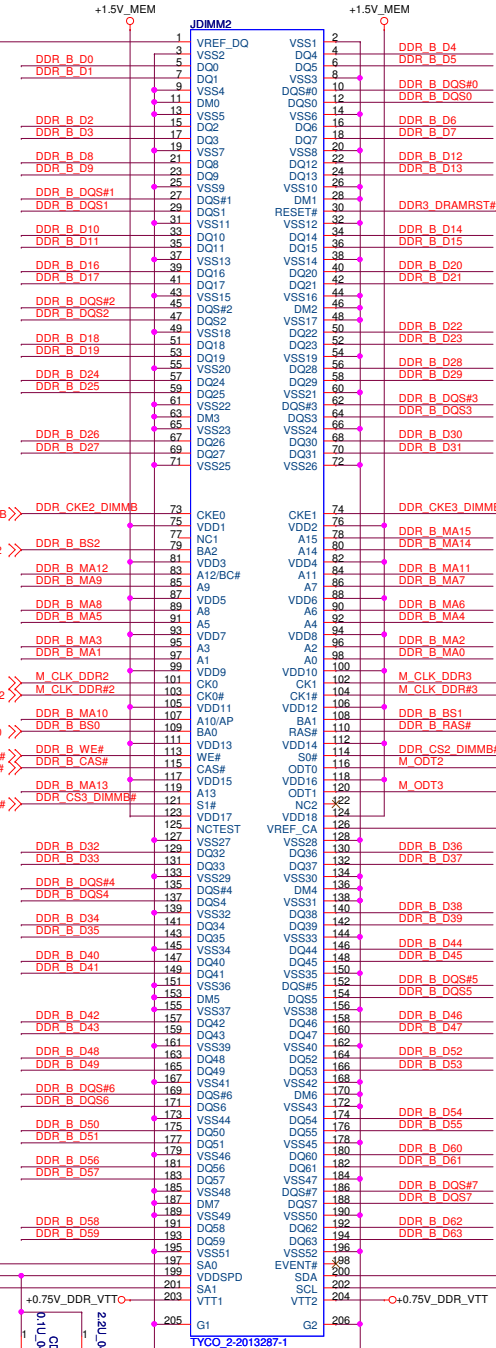


Layout Note:
Place near JDIMM2.203,204



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H=4mm 2-3A to 1 DIMMs/channel



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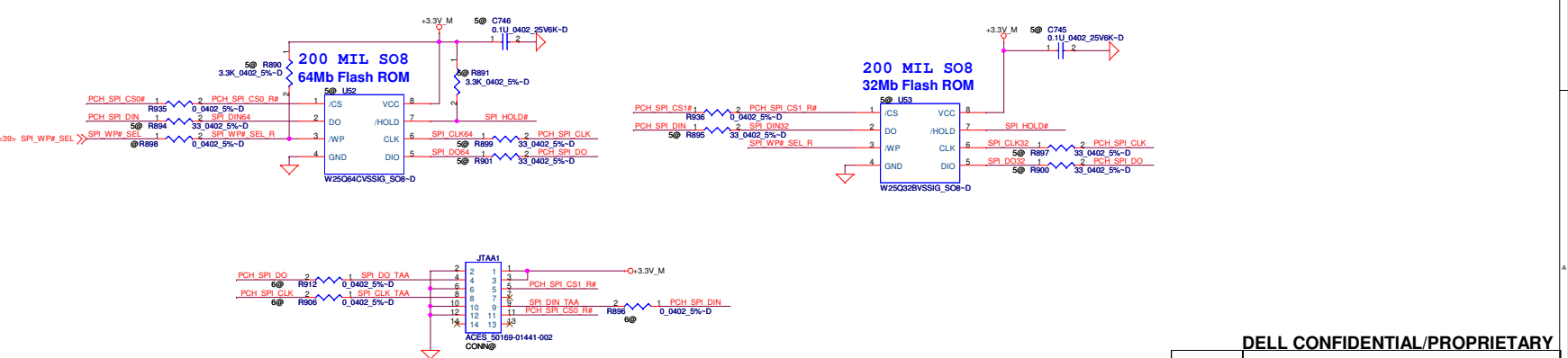
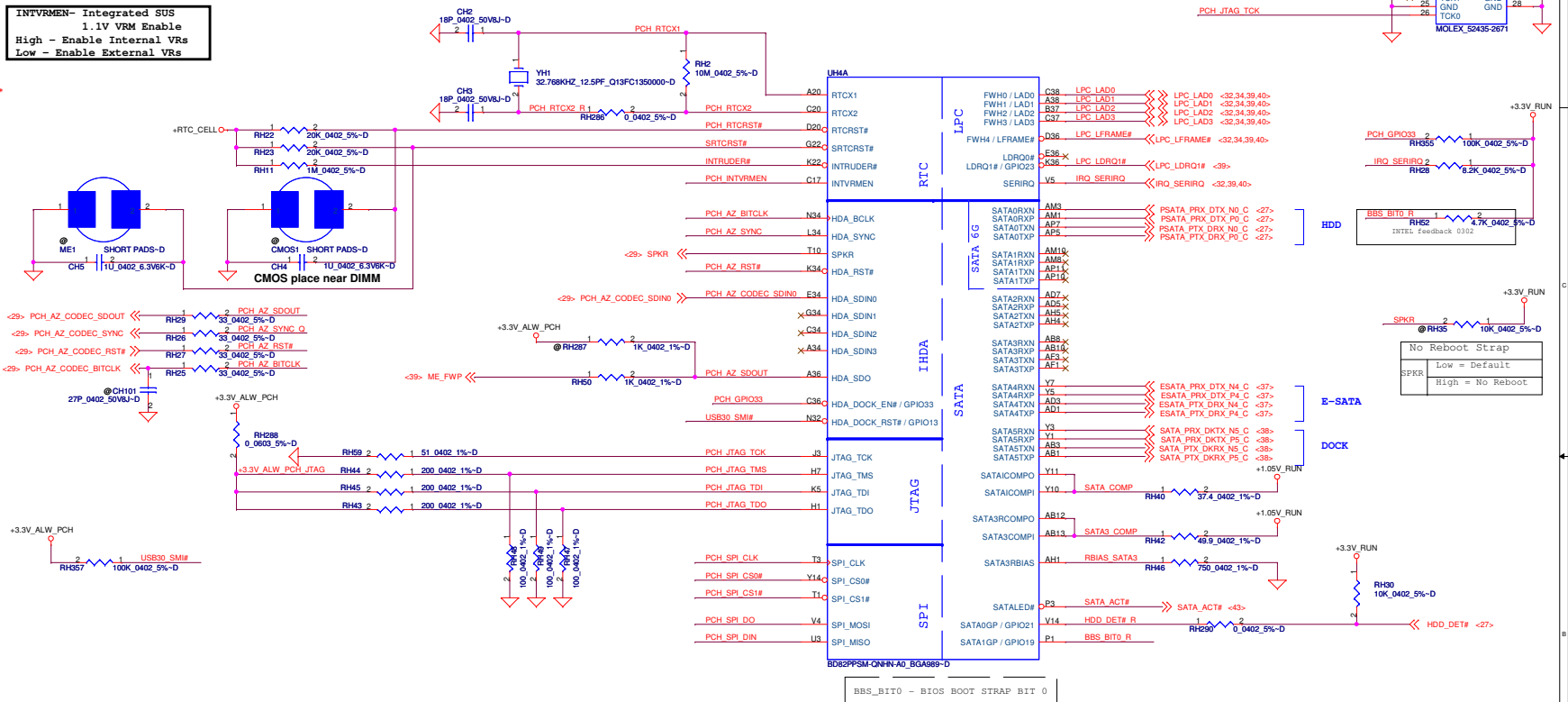
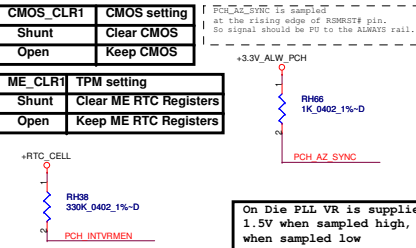
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DDRIII-SODIMM SLOT2

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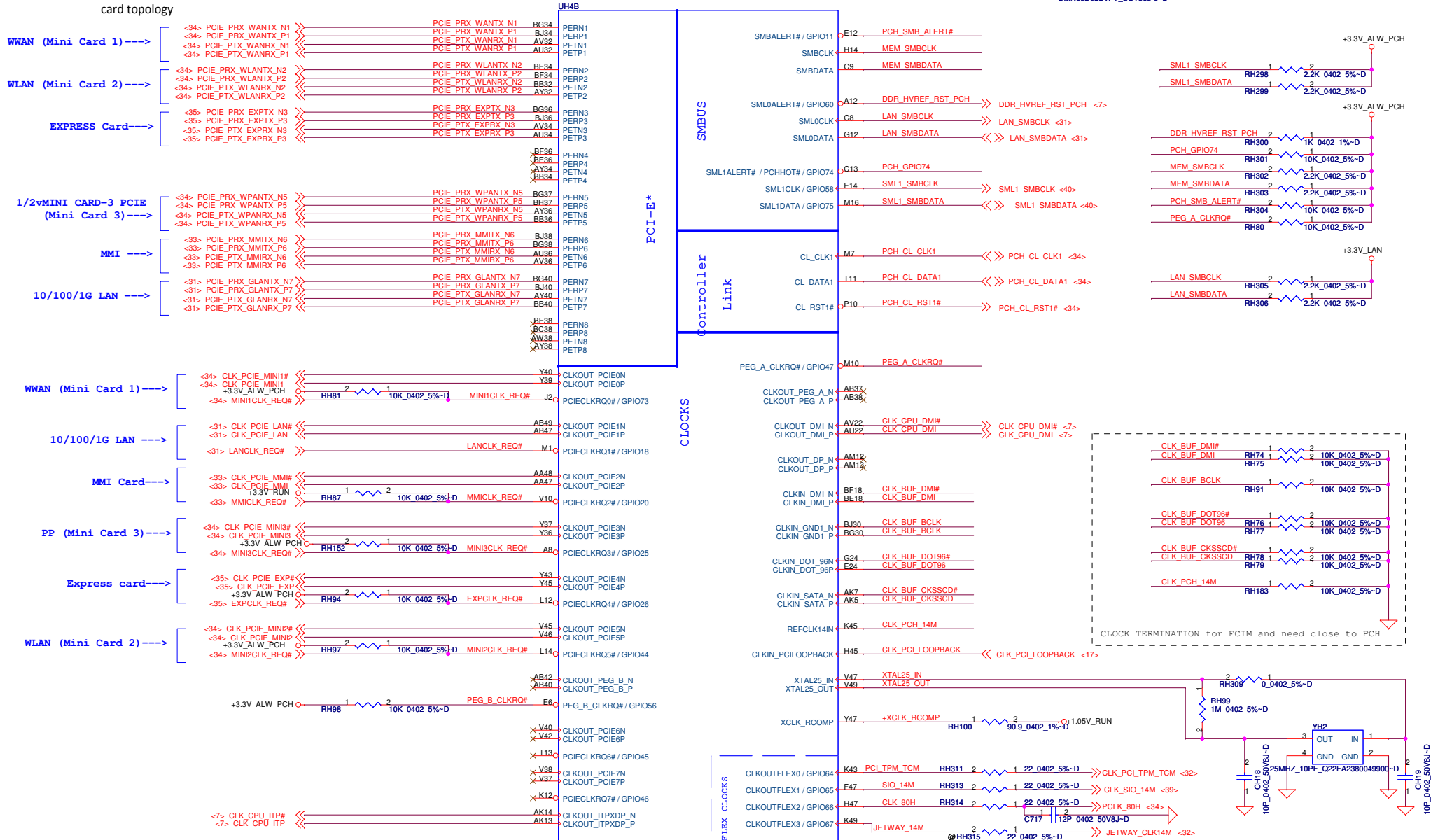
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Follow DG0.9 Device
down & Express/Mini
card topology



PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

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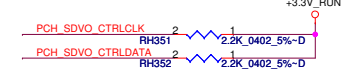
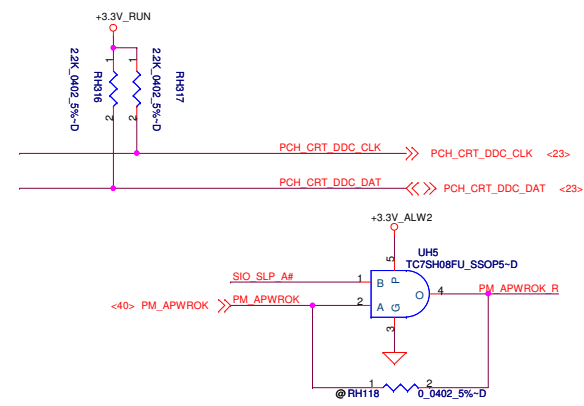
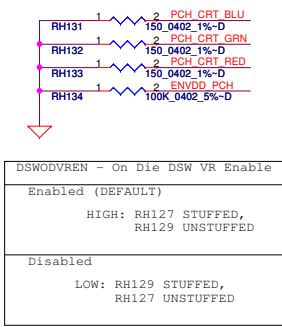
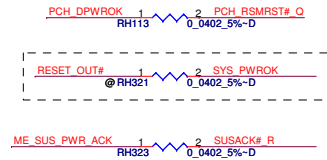
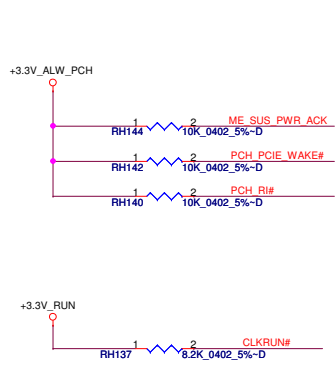
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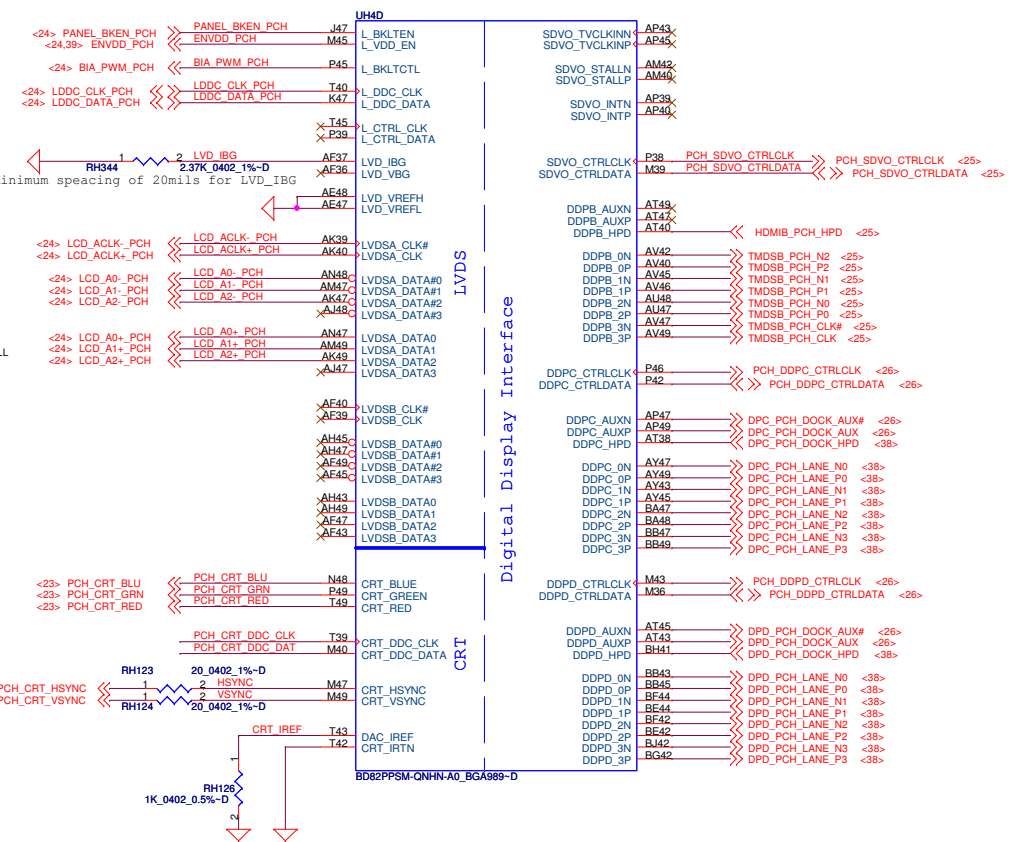
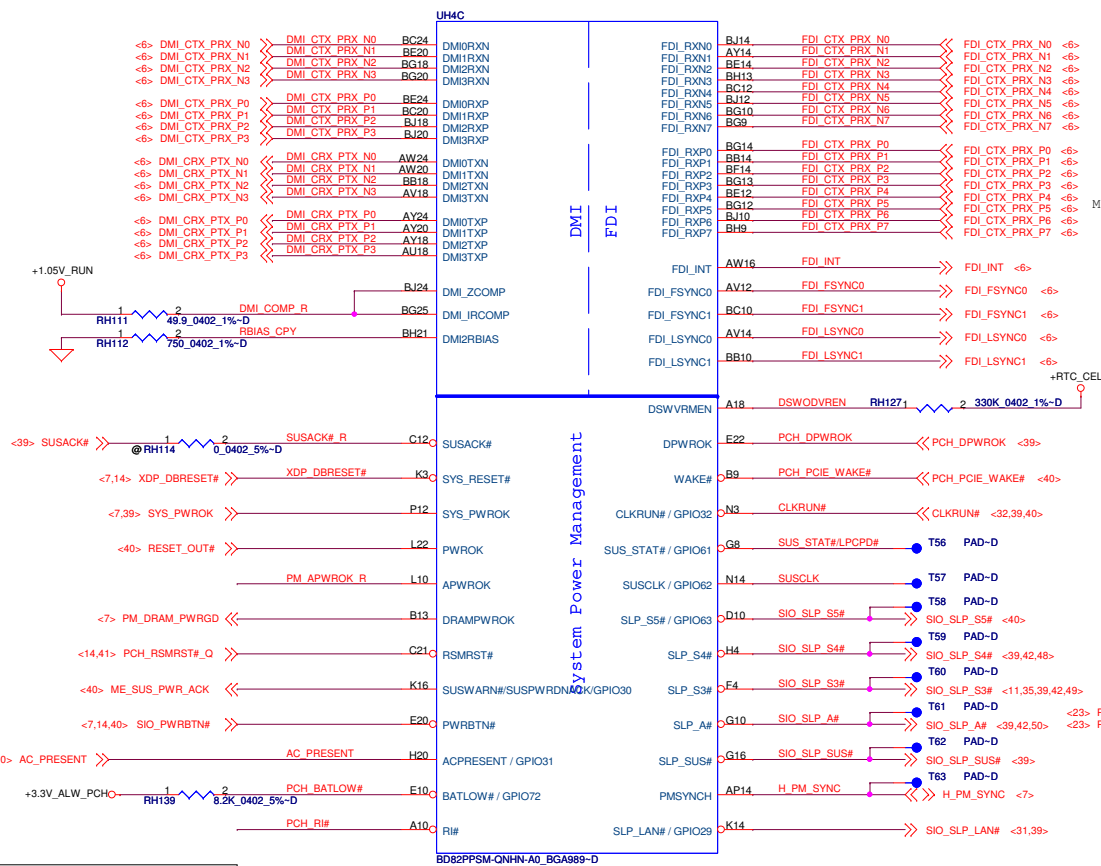
PCH (2/8)

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Intel request DDPB can not support eDP

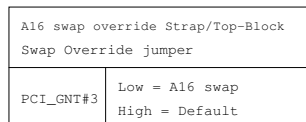
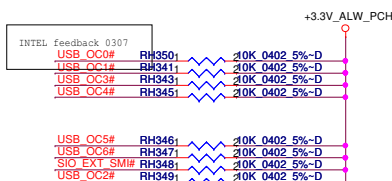
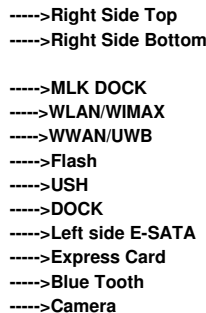
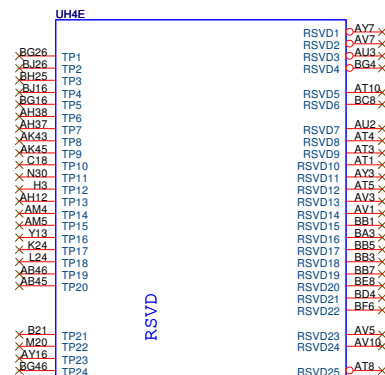


Remove RH116, RH117, RH118, RH320, RH120, RH121, RH122 to save room for D4 12" only

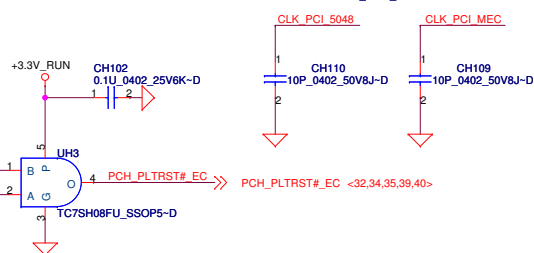
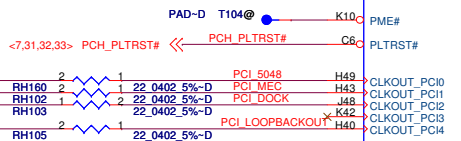
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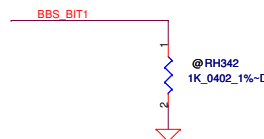
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	_____	PCI_PIRQ#A	K40_	PIRO#A
	_____	PCI_PIRQ#B	K38_	PIRO#B
	_____	PCI_PIRQ#C	H38_	PIRO#C
	_____	PCI_PIRQ#D	G38_	PIRO#D
	_____	PCI_REQ1#	C46_	REQ1# / GPIO50
<34> PCIE_MCARD2_DET#	>>> _____	BT_DET#	C44_	REQ1# / GPIO52
<<<1> BT_DET#	>>> _____	BBS_BIT1	E40_	REQ3# / GPIO54
	_____		D47_	GNT1# / GPIO61
	_____		×	GNT2# / GPIO53
	_____	PCI_GNT3#	F46_	GNT3# / GPIO55
	_____	LCD_CBL_DET#	G42_	PIROE# / GPIO2
<24> LCD_CBL_DET#	>>> _____	PCI_GPIO3	G44_	PIROF# / GPIO3
	_____	CAM_MIC_CBL_DET#	D44_	PIROG# / GPIO4
<24> CAM_MIC_CBL_DET#	>>> _____		D42_	PIROH# / GPIO4
<24> HDD_FALL_IN#	>>> _____		D44_	

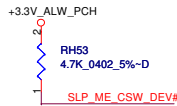


Boot BIOS Strap		
BBS_BIT1	SATA_SLDP (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



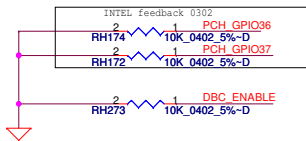
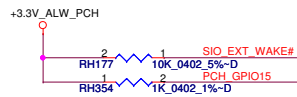
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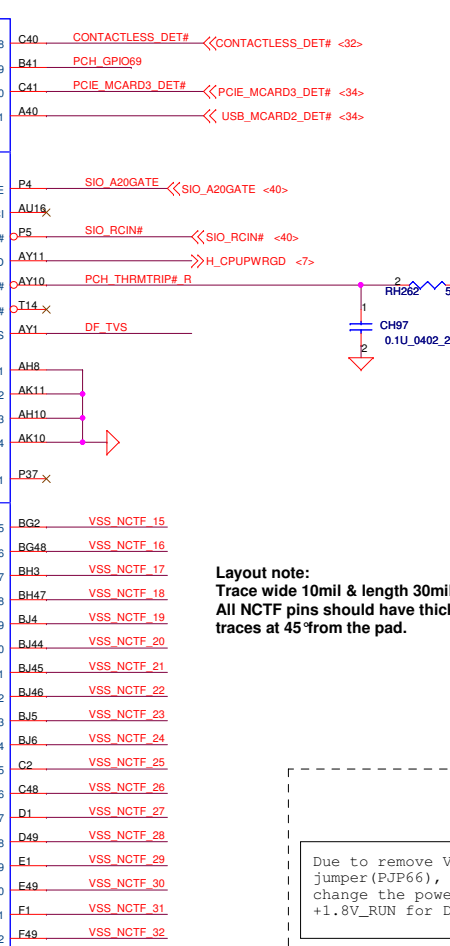
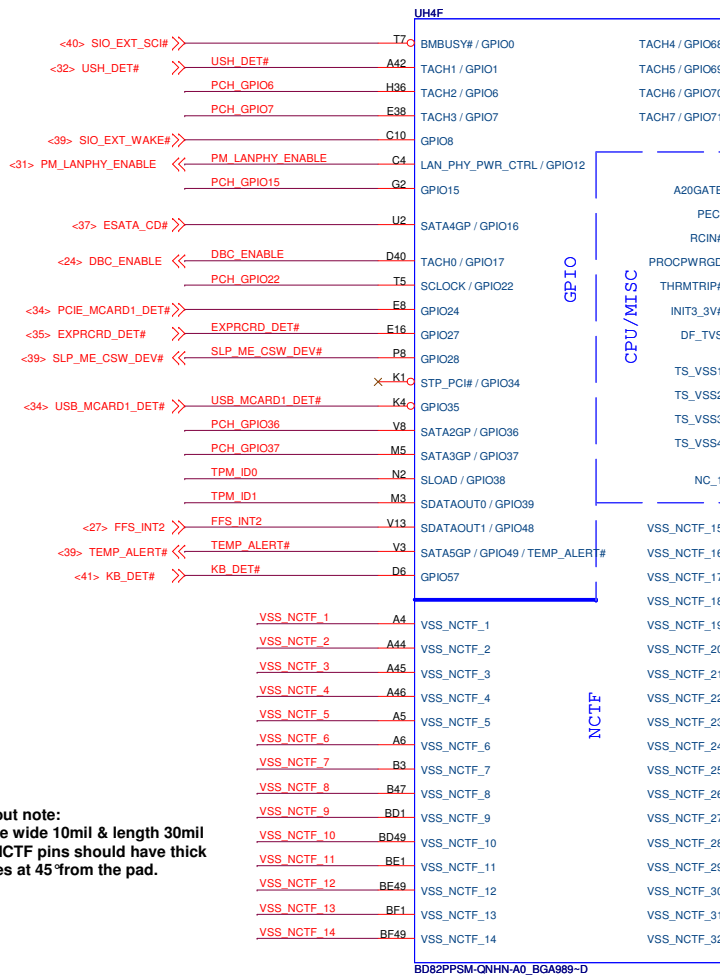
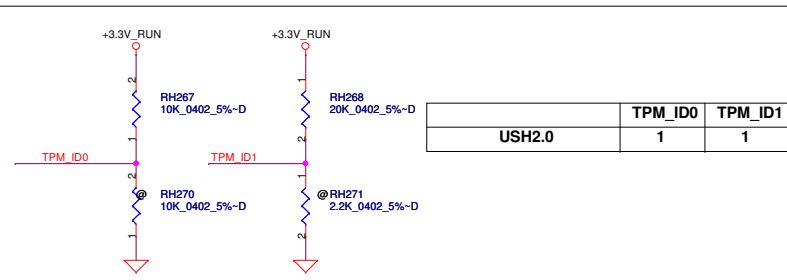
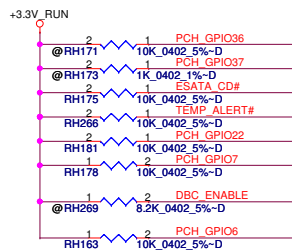
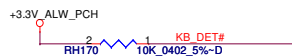


Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

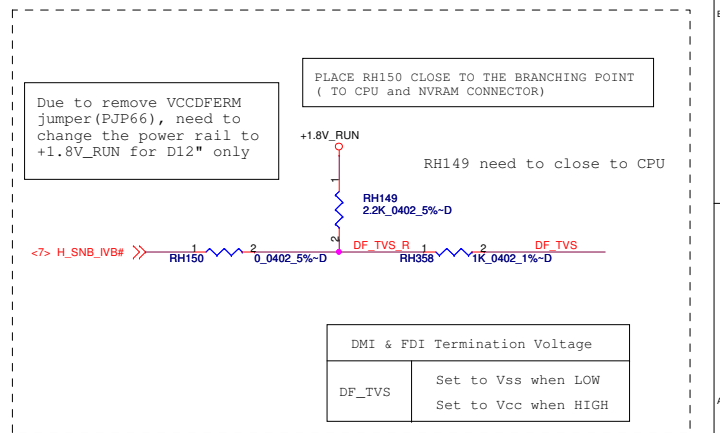
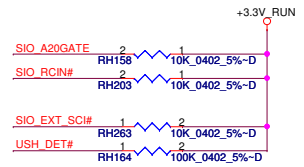
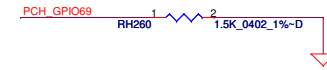
SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT	
DISABLED - LOW	



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



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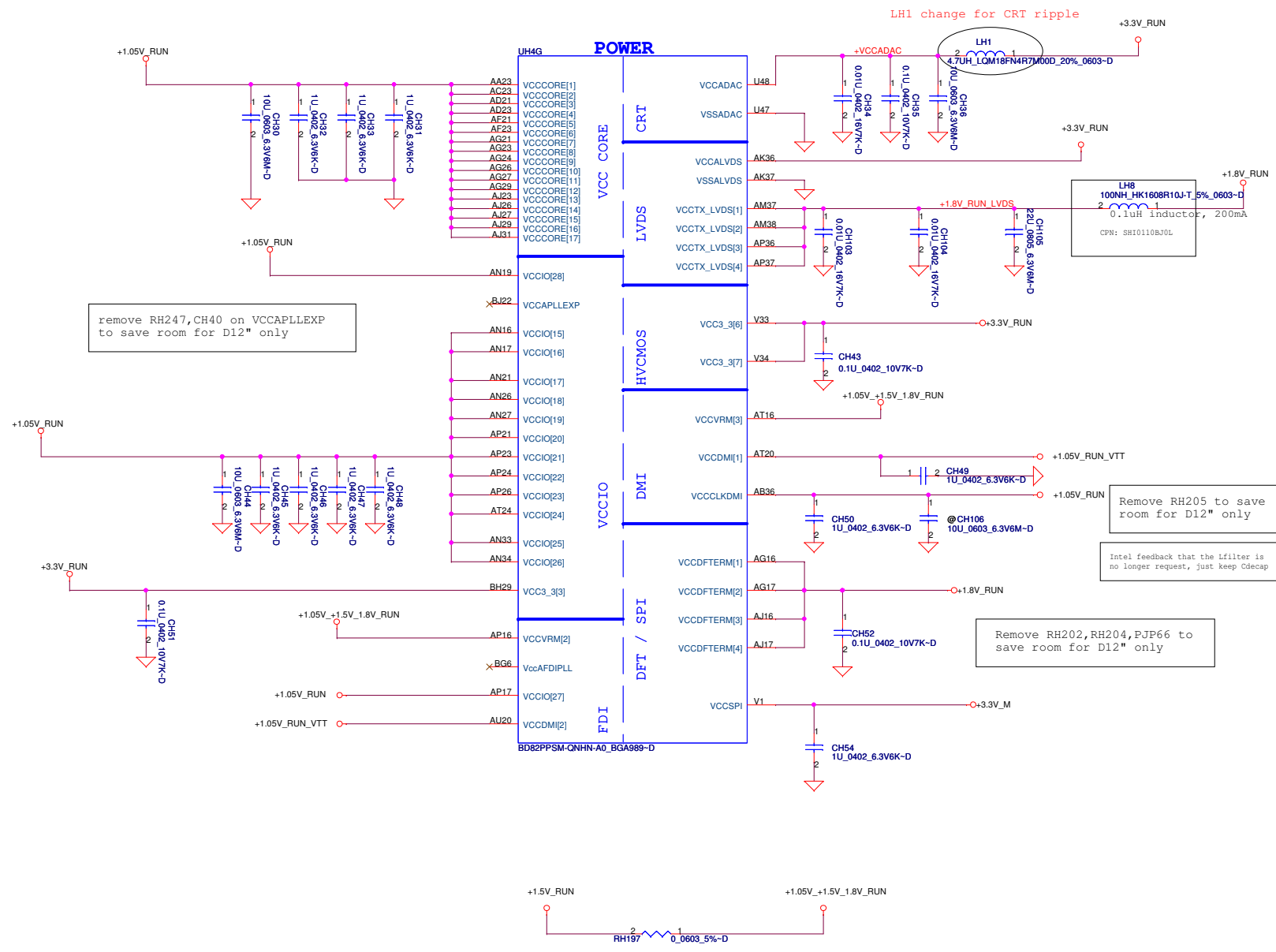
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PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
VCCDFTERM	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06
VccAPLEXP	1.05	0.05

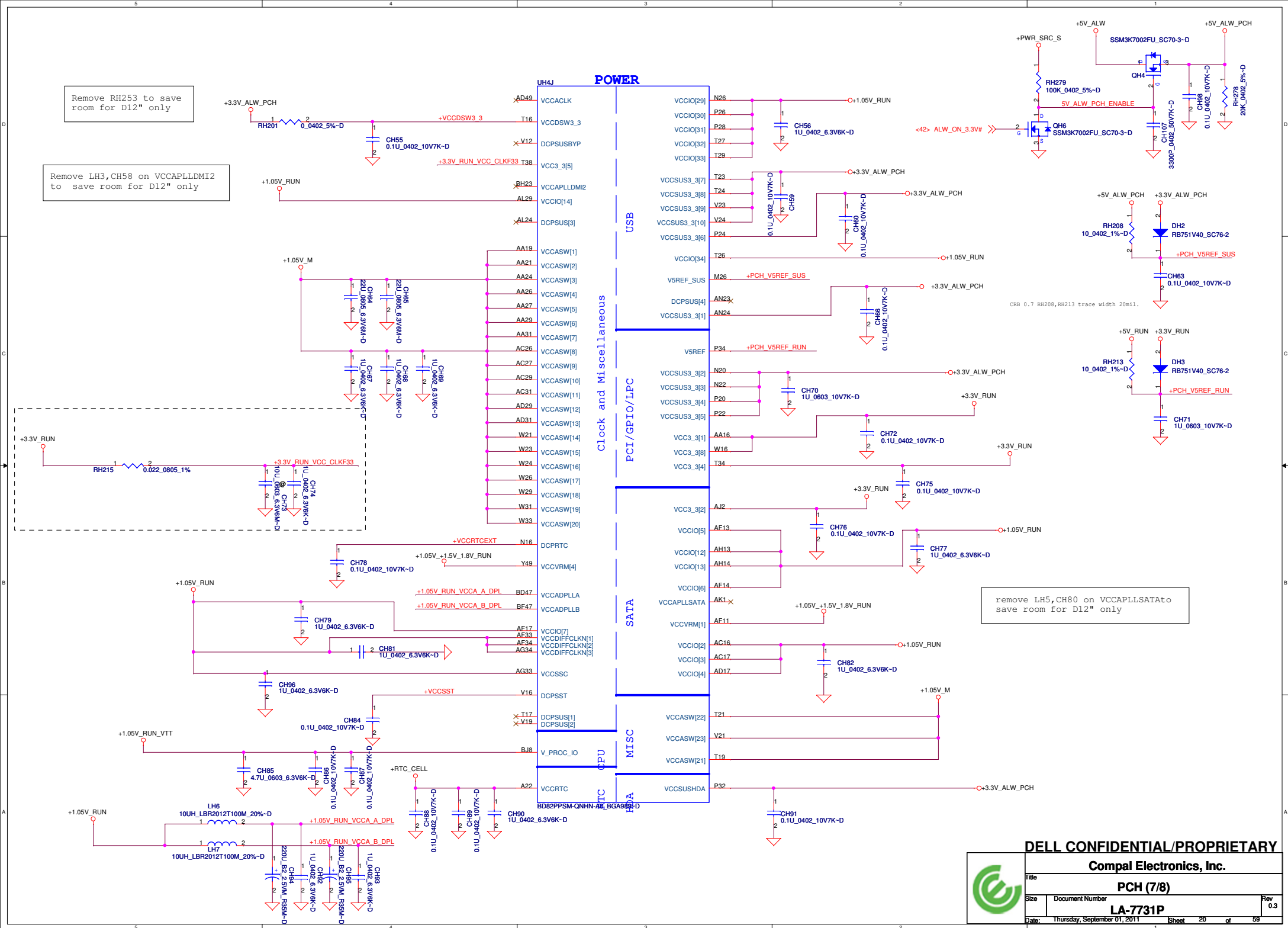
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UH4H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK46
AA33	VSS[4]	VSS[83] AK5
AA34	VSS[5]	VSS[84] AK8
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL26
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL34
AC24	VSS[16]	VSS[95] AL48
AC33	VSS[17]	VSS[96] AM11
AC34	VSS[18]	VSS[97] AM14
AC48	VSS[19]	VSS[98] AM36
AD10	VSS[20]	VSS[99] AM39
AD11	VSS[21]	VSS[100] AM43
AD12	VSS[22]	VSS[101] AM45
AD13	VSS[23]	VSS[102] AM46
AD19	VSS[24]	VSS[103] AM7
AD24	VSS[25]	VSS[104] AN2
AD26	VSS[26]	VSS[105] AN29
AD27	VSS[27]	VSS[106] AN3
AD33	VSS[28]	VSS[107] AN31
AD34	VSS[29]	VSS[108] AP12
AD36	VSS[30]	VSS[109] AP19
AD37	VSS[31]	VSS[110] AP28
AD38	VSS[32]	VSS[111] AP32
AD39	VSS[33]	VSS[112] AP38
AD4	VSS[34]	VSS[113] AP4
AD40	VSS[35]	VSS[114] AP42
AD42	VSS[36]	VSS[115] AP46
AD43	VSS[37]	VSS[116] AP8
AD45	VSS[38]	VSS[117] AR2
AD46	VSS[39]	VSS[118] AR48
AD8	VSS[40]	VSS[119] AT11
AE2	VSS[41]	VSS[120] AT13
AE3	VSS[42]	VSS[121] AT22
AF10	VSS[43]	VSS[122] AT26
AF12	VSS[44]	VSS[123] AT28
AD14	VSS[45]	VSS[124] AT30
AD16	VSS[46]	VSS[125] AT32
AF16	VSS[47]	VSS[126] AT34
AF19	VSS[48]	VSS[127] AT39
AF24	VSS[49]	VSS[128] AT42
AF26	VSS[50]	VSS[129] AT46
AF27	VSS[51]	VSS[130] AU24
AF29	VSS[52]	VSS[131] AU30
AF31	VSS[53]	VSS[132] AV16
AF38	VSS[54]	VSS[133] AV20
AF4	VSS[55]	VSS[134] AV24
AF42	VSS[56]	VSS[135] AV30
AF5	VSS[57]	VSS[136] AV38
AF7	VSS[58]	VSS[137] AV4
AF8	VSS[59]	VSS[138] AV8
AG19	VSS[61]	VSS[139] AW14
AG2	VSS[62]	VSS[140] AW18
AG31	VSS[63]	VSS[141] AW2
AG48	VSS[64]	VSS[142] AW22
AH11	VSS[65]	VSS[143] AW26
AH3	VSS[66]	VSS[144] AW28
AH36	VSS[67]	VSS[145] AW32
AH39	VSS[68]	VSS[146] AW36
AH40	VSS[69]	VSS[147] AW40
AH42	VSS[70]	VSS[148] AW44
AH46	VSS[71]	VSS[149] AW48
AH7	VSS[72]	VSS[150] AY11
AJ19	VSS[73]	VSS[151] AY12
AJ21	VSS[74]	VSS[152] AY22
AJ24	VSS[75]	VSS[153] AY28
AJ33	VSS[76]	VSS[154]
AJ34	VSS[77]	VSS[155]
AK12	VSS[78]	VSS[156]
AK3	VSS[79]	VSS[157]
		VSS[158]

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UH4I		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B39	VSS[169]	VSS[269] L38
B7	VSS[170]	VSS[270] L48
F45	VSS[171]	VSS[271] M12
B12	VSS[172]	VSS[272] M18
BB16	VSS[173]	VSS[273] M22
BB20	VSS[174]	VSS[274] M24
BB22	VSS[175]	VSS[275] M30
BB24	VSS[176]	VSS[276] M32
BB28	VSS[177]	VSS[277] M34
BB30	VSS[178]	VSS[278] M38
BB38	VSS[179]	VSS[279] M4
BB4	VSS[180]	VSS[280] M42
BB46	VSS[181]	VSS[281] M46
BC14	VSS[182]	VSS[282] M8
BC18	VSS[183]	VSS[283] M18
BC18	VSS[184]	VSS[284] M24
BC2	VSS[185]	VSS[285] M30
BC22	VSS[186]	VSS[286] M32
BC26	VSS[187]	VSS[287] M34
BC32	VSS[188]	VSS[288] M38
BC34	VSS[189]	VSS[289] M4
BC36	VSS[190]	VSS[290] M42
BC40	VSS[191]	VSS[291] M46
BC42	VSS[192]	VSS[292] M48
BC48	VSS[193]	VSS[293] M54
BD46	VSS[194]	VSS[294] M58
BD5	VSS[195]	VSS[295] M6
BE22	VSS[196]	VSS[296] M12
BE26	VSS[197]	VSS[297] M18
BE40	VSS[198]	VSS[298] M24
BF10	VSS[199]	VSS[299] M30
BF12	VSS[200]	VSS[300] M32
BF16	VSS[201]	VSS[301] M34
BF20	VSS[202]	VSS[302] M38
BF22	VSS[203]	VSS[303] M4
BF24	VSS[204]	VSS[304] M42
BF26	VSS[205]	VSS[305] M46
BF28	VSS[206]	VSS[306] M48
BF30	VSS[207]	VSS[307] M54
BF38	VSS[208]	VSS[308] M58
BF40	VSS[209]	VSS[309] M6
BF48	VSS[210]	VSS[310] M12
BF8	VSS[211]	VSS[311] M18
BG17	VSS[212]	VSS[312] M24
BG21	VSS[213]	VSS[313] M30
BG33	VSS[214]	VSS[314] M32
BG44	VSS[215]	VSS[315] M34
BG8	VSS[216]	VSS[316] M38
BH11	VSS[217]	VSS[317] M4
BH15	VSS[218]	VSS[318] M42
BH17	VSS[219]	VSS[319] M46
BH19	VSS[220]	VSS[320] M48
H10	VSS[221]	VSS[321] M54
BH27	VSS[222]	VSS[322] M58
BH31	VSS[223]	VSS[323] M6
BH33	VSS[224]	VSS[324] M12
BH35	VSS[225]	VSS[325] M18
BH39	VSS[226]	VSS[326] M24
BH43	VSS[227]	VSS[327] M30
BH7	VSS[228]	VSS[328] M32
D1	VSS[229]	VSS[329] M34
D12	VSS[230]	VSS[330] M38
D16	VSS[231]	VSS[331] M4
D18	VSS[232]	VSS[332] M42
D22	VSS[233]	VSS[333] M46
D24	VSS[234]	VSS[334] M48
D26	VSS[235]	VSS[335] M54
D30	VSS[236]	VSS[336] M58
D32	VSS[237]	VSS[337] M6
D34	VSS[238]	VSS[338] M12
D38	VSS[239]	VSS[339] M18
D42	VSS[240]	VSS[340] M24
D8	VSS[241]	VSS[341] M30
E18	VSS[242]	VSS[342] M32
F26	VSS[243]	VSS[343] M34
G18	VSS[244]	VSS[344] M38
G20	VSS[245]	VSS[345] M4
G26	VSS[246]	VSS[346] M42
G28	VSS[247]	VSS[347] M46
G36	VSS[248]	VSS[348] M48
G48	VSS[249]	VSS[349] M54
H12	VSS[250]	VSS[350] M58
H18	VSS[251]	VSS[351] M6
H22	VSS[252]	VSS[352] M12
H24	VSS[253]	
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F3	VSS[258]	

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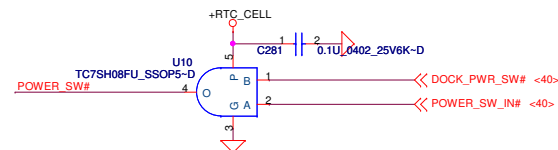
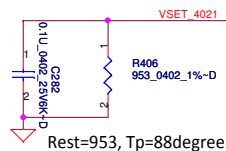
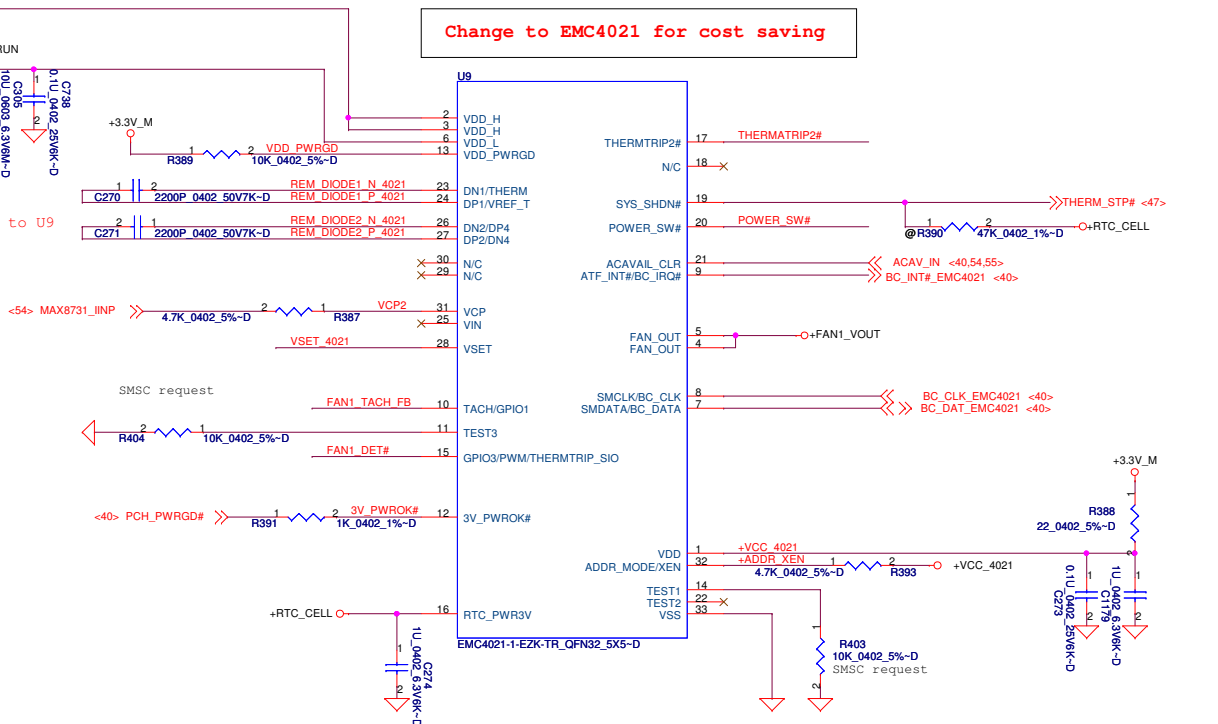
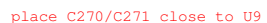
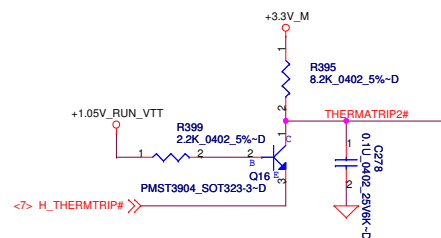
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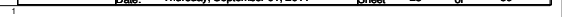
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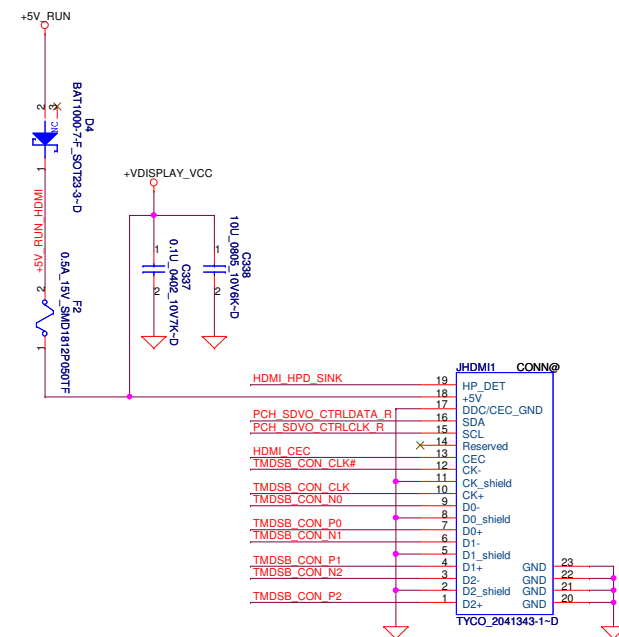
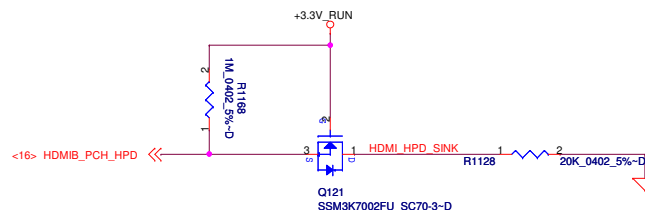
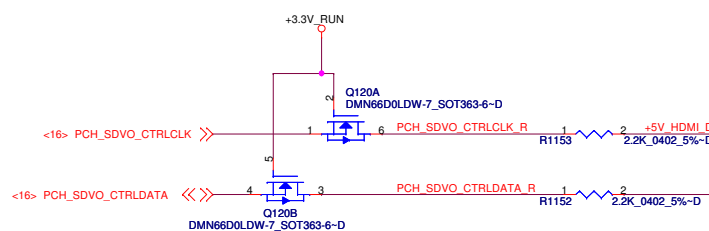
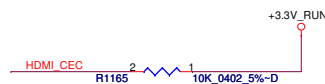
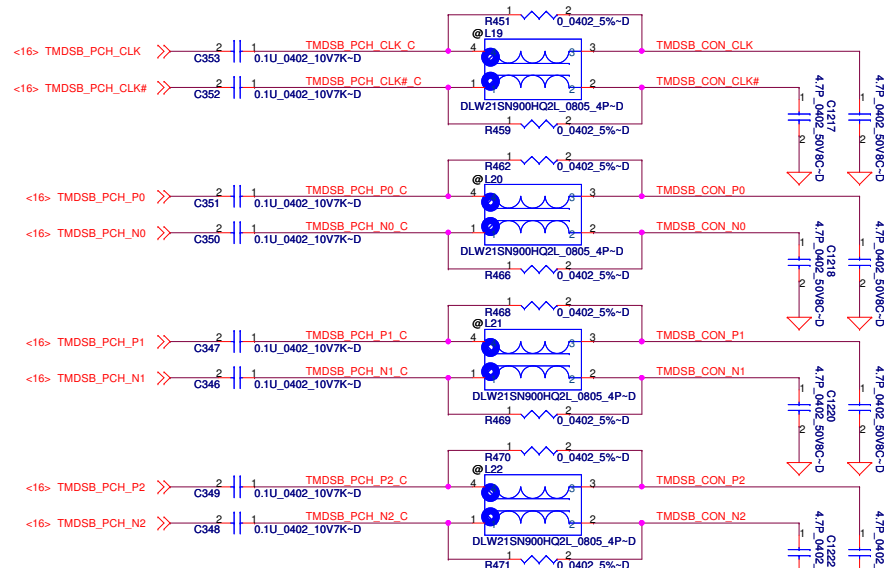
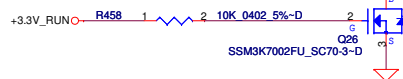
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[illegible][illegible]

TMDSB_PCH_P2_C R452 1 2 680_0402_5%-D HDMI_OB
 TMDSB_PCH_N2_C R450 1 2 680_0402_5%-D
 TMDSB_PCH_P1_C R448 1 2 680_0402_5%-D
 TMDSB_PCH_N1_C R449 1 2 680_0402_5%-D
 TMDSB_PCH_P0_C R454 1 2 680_0402_5%-D
 TMDSB_PCH_N0_C R453 1 2 680_0402_5%-D
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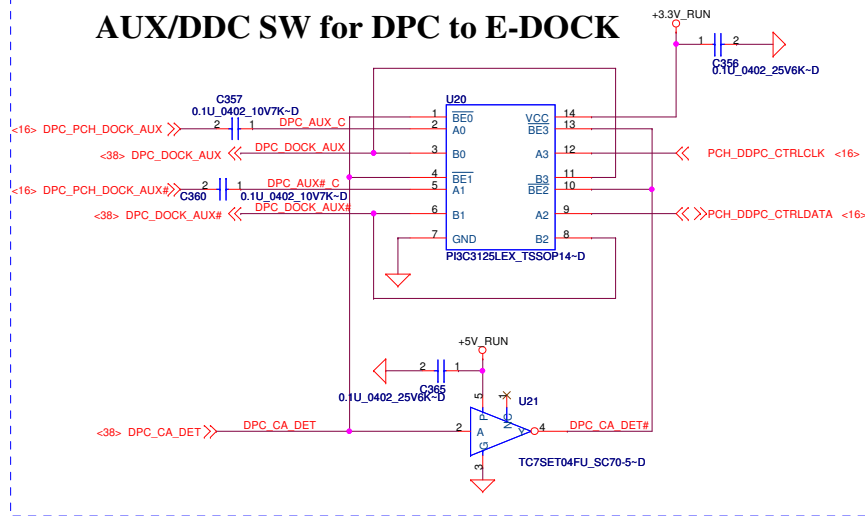


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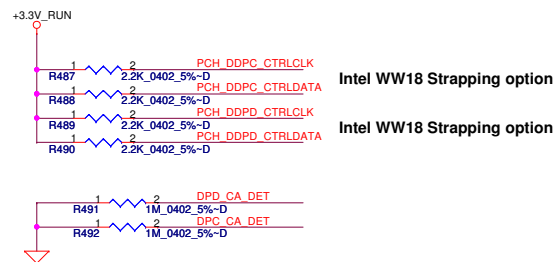
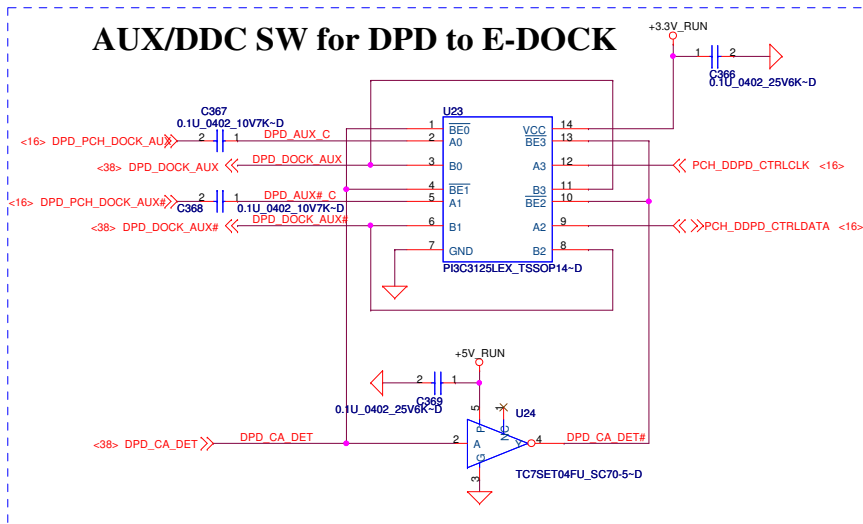
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HDMI port			
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AUX/DDC SW for DPC to E-DOCK



There is a new die for PI3C3125. Sample available on May.

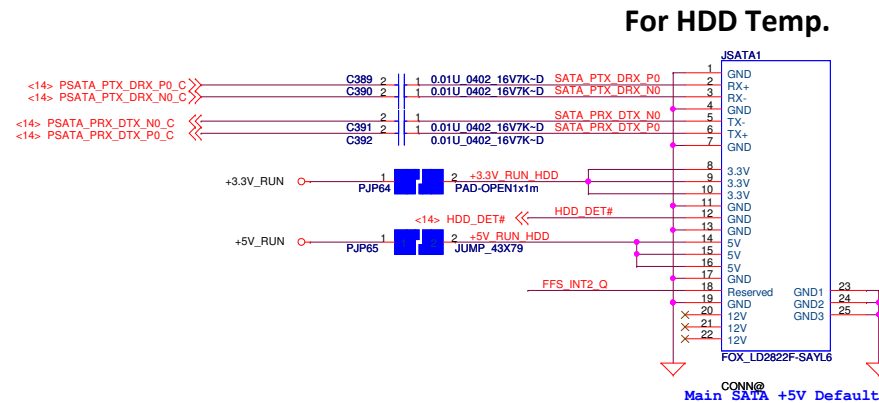
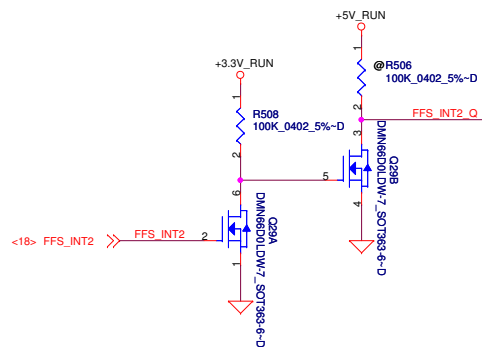
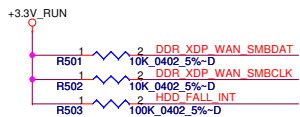
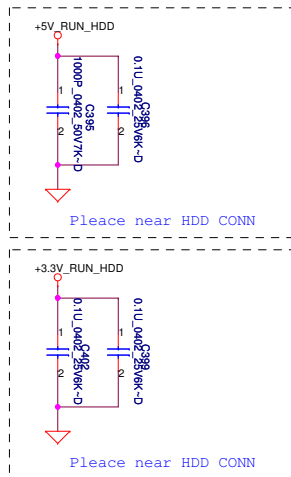
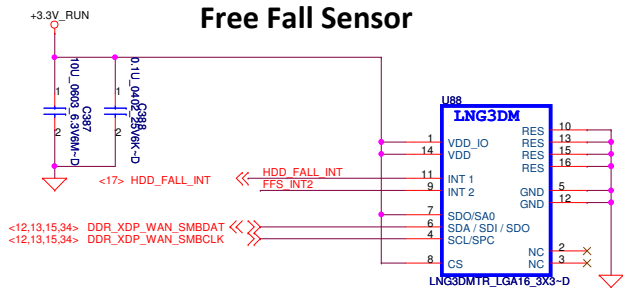
AUX/DDC SW for DPD to E-DOCK



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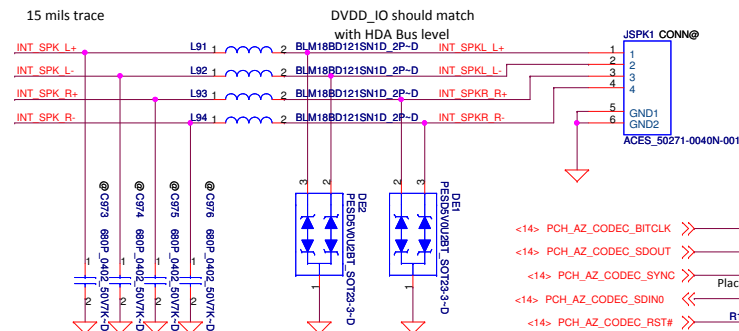


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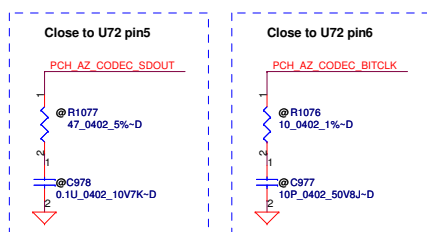


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Compal Electronics, Inc.		
Title		
ODD CONNECTOR		
Size	Document Number	Rev
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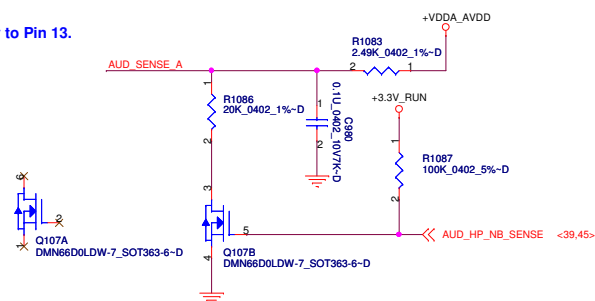
Internal Speakers Header



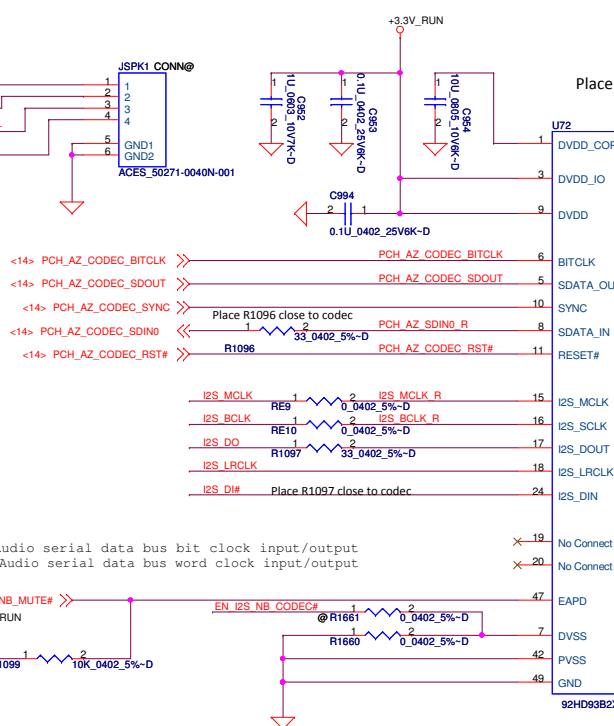
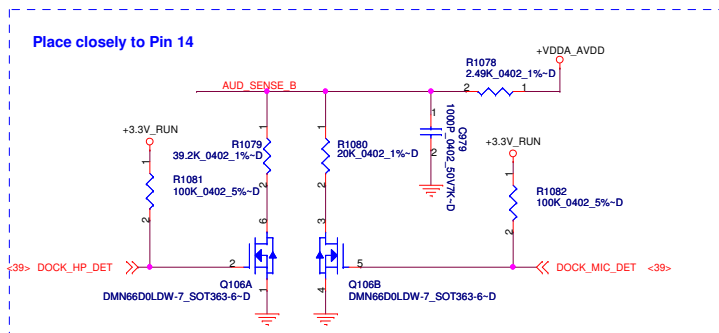
ESD ask to add DE1,DE2



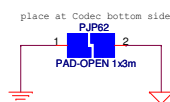
Place closely to Pin 13.



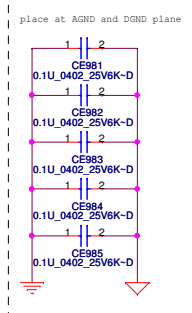
Place closely to Pin 14



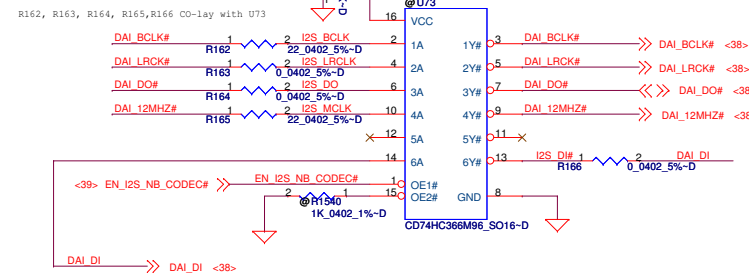
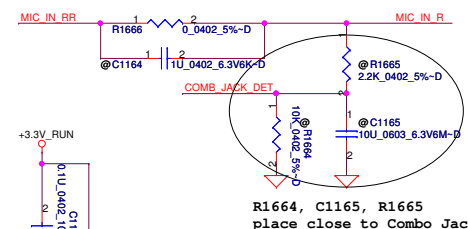
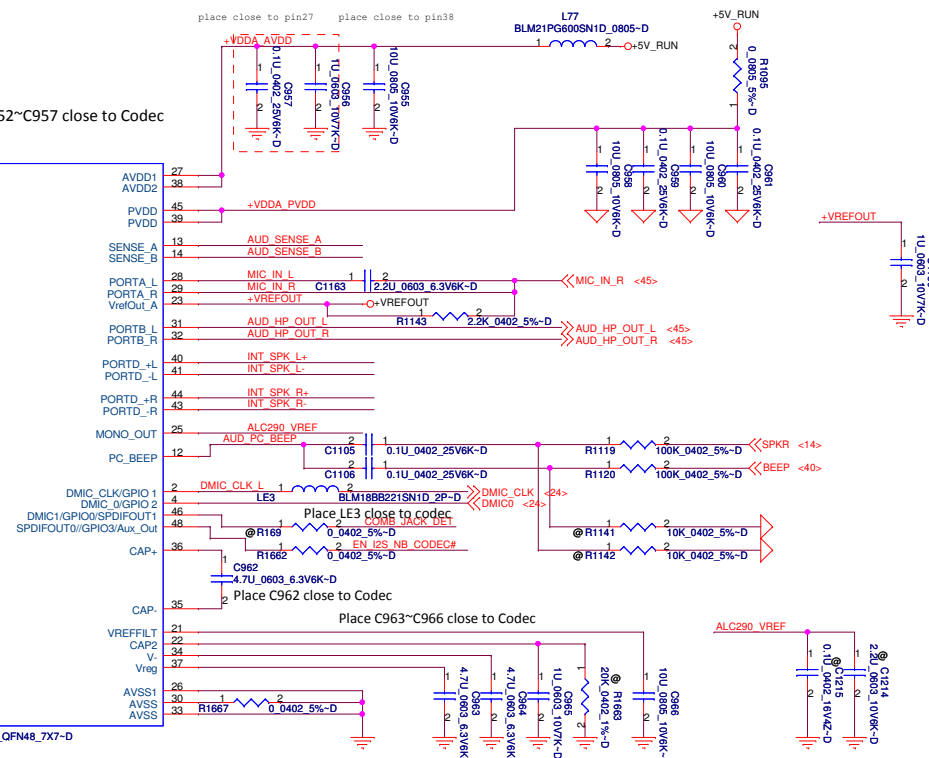
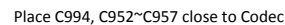
Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals



EMI request to add C984,C985



PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Intel
PORT D	Internal SPK
PORT E	DOCK
PORT F	DOCK



Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

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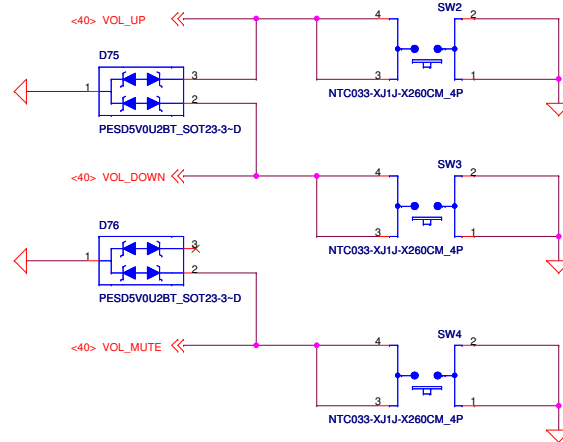
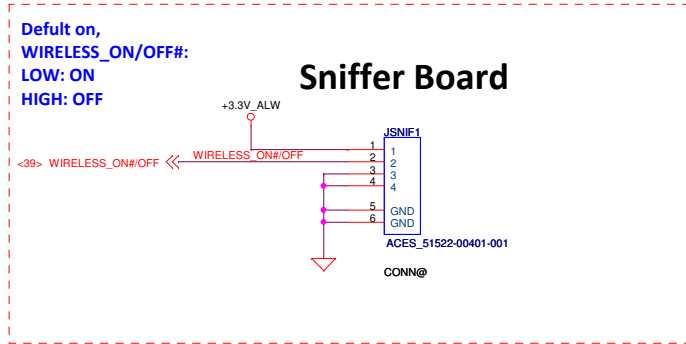
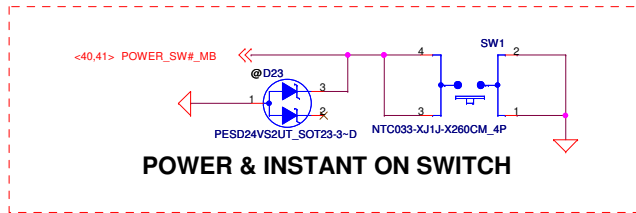
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Azalia (HD) Codec

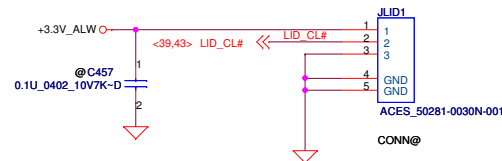
umber
LA 3301D

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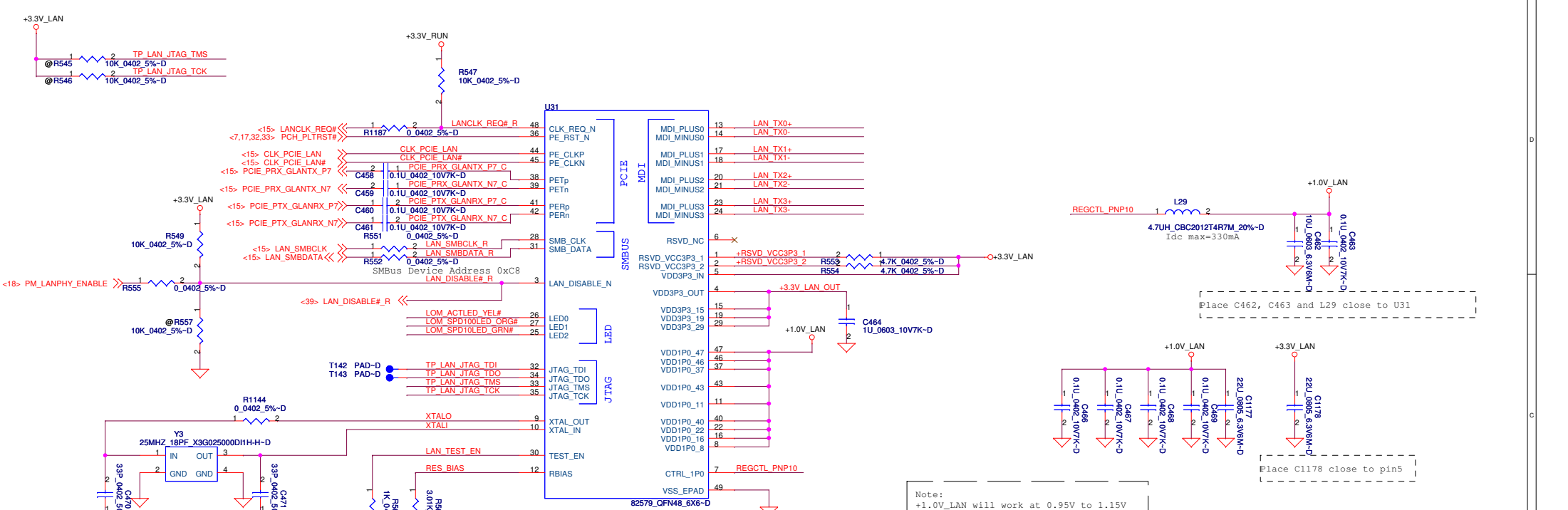


Lid board



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Compal Electronics, Inc.			
Title	PWR SW/Sub-board Connector		
Size	Document Number	LA-7731P	Rev 0.3
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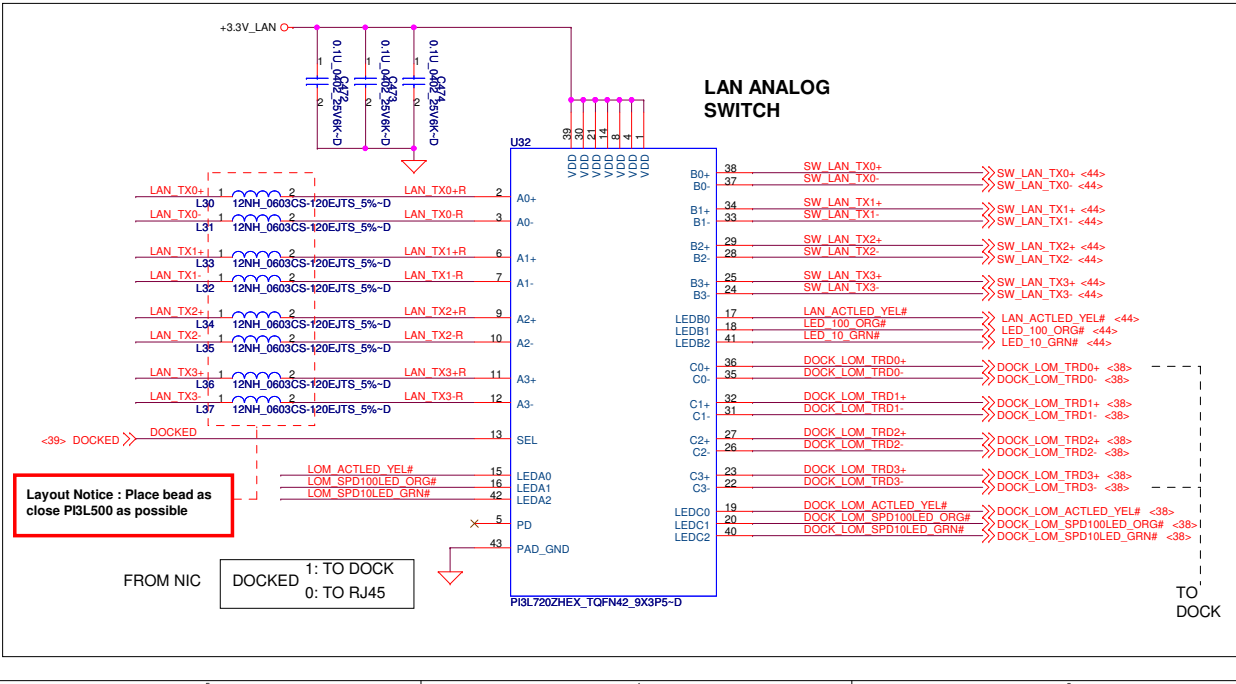


Note:
+1.0V_LAN will work at 0.95V to 1.15V

+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R548 NO STUFF: L29	STUFF: L29 NO STUFF: R548

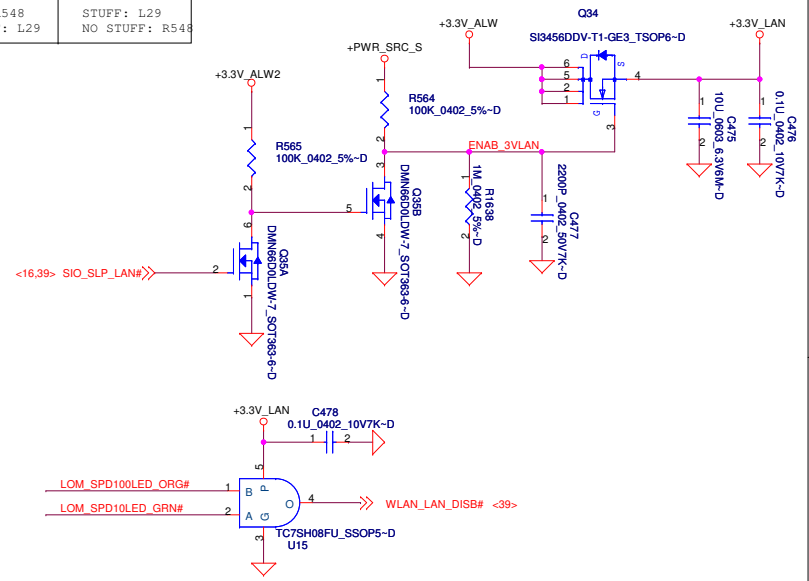
Need to verify A3 silicon drive power before removing C427 KDS crystal vender verify driving level in A3

R1200 Resistor Value:
3.01 kohm for Hanksville-M LOM
2.37 kohm for Hanksville-D LOM



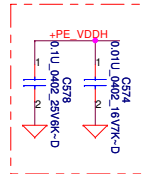
Layout Notice : Place bead as close P13L500 as possible

FROM NIC DOCKED 1: TO DOCK 0: TO RJ45

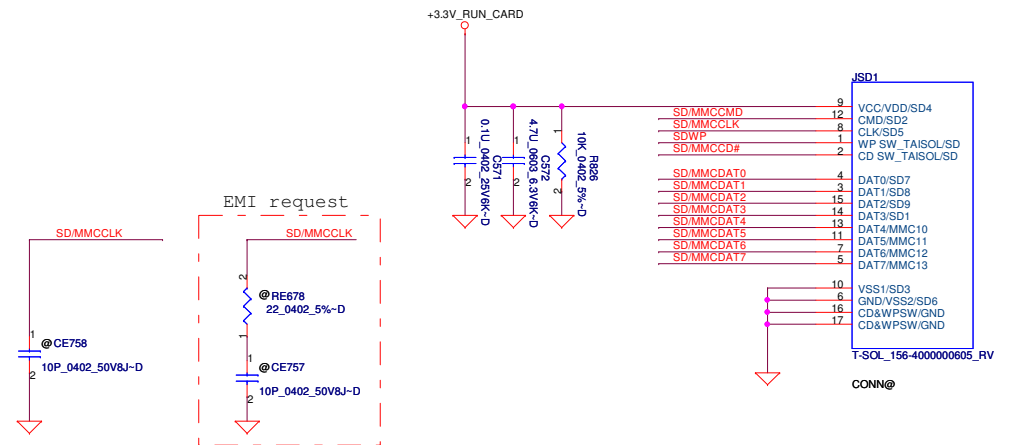
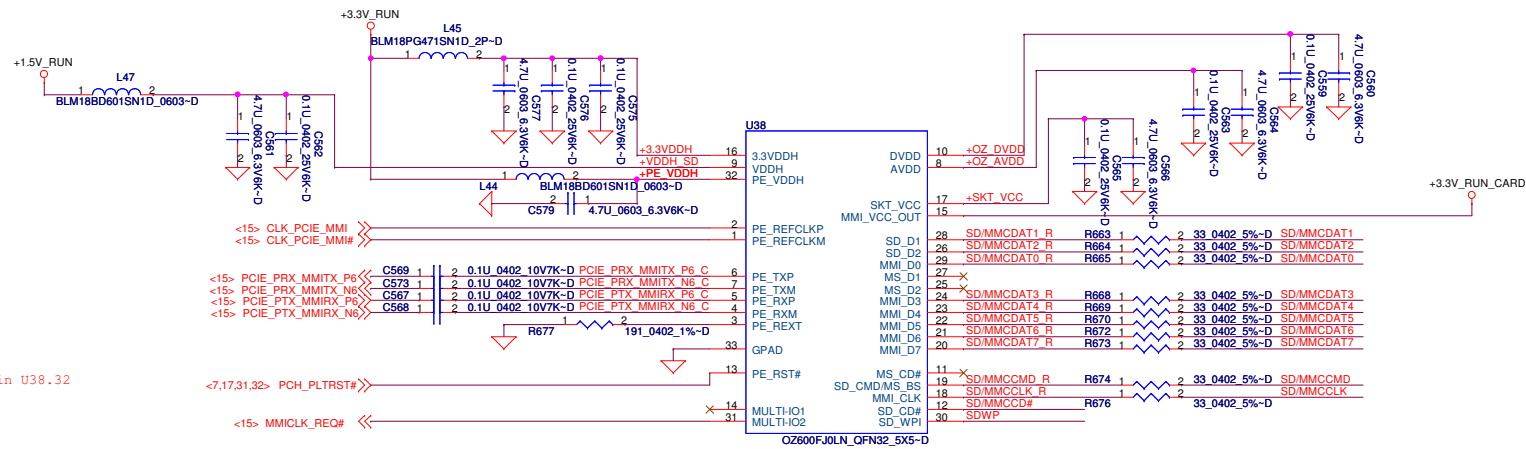


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Compal Electronics, Inc.	
Intel 82579 (Hanksville) / LAN SW	
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place close to pin U38.32



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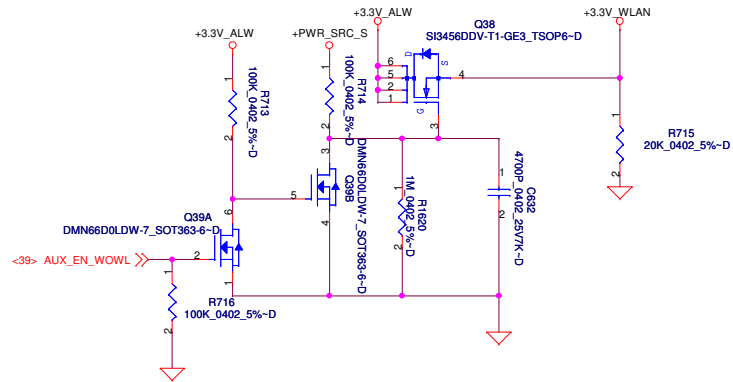
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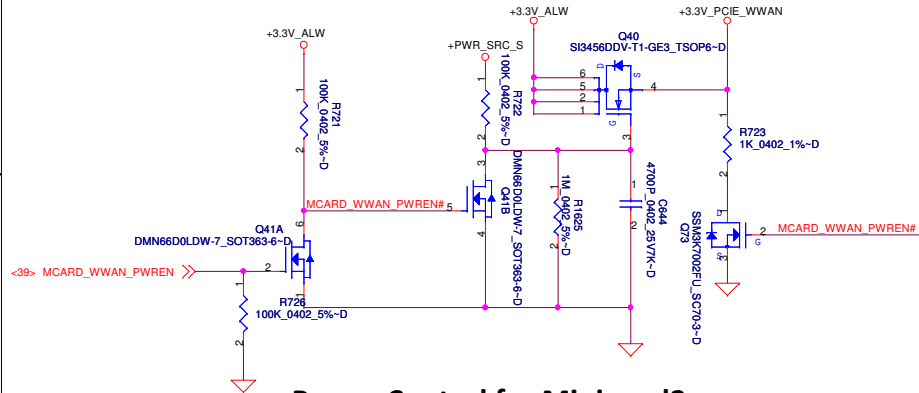
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Card Reader			
LA-7731P			
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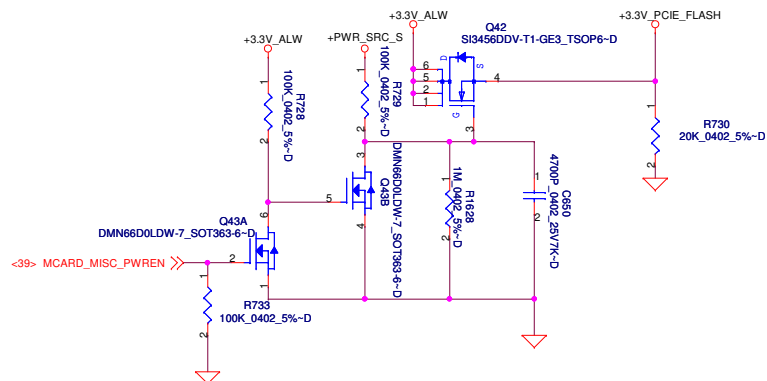
Power Control for Mini card1



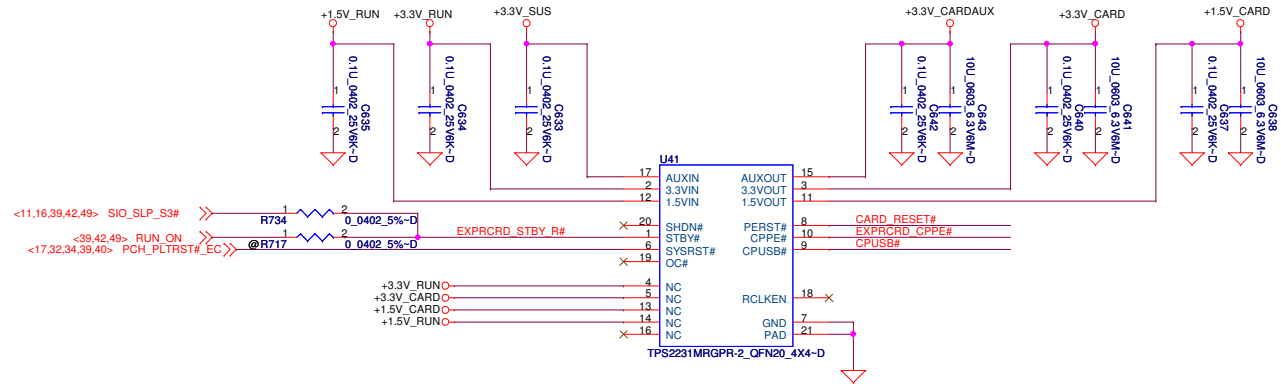
Power Control for Mini card2



Power Control for Mini card3

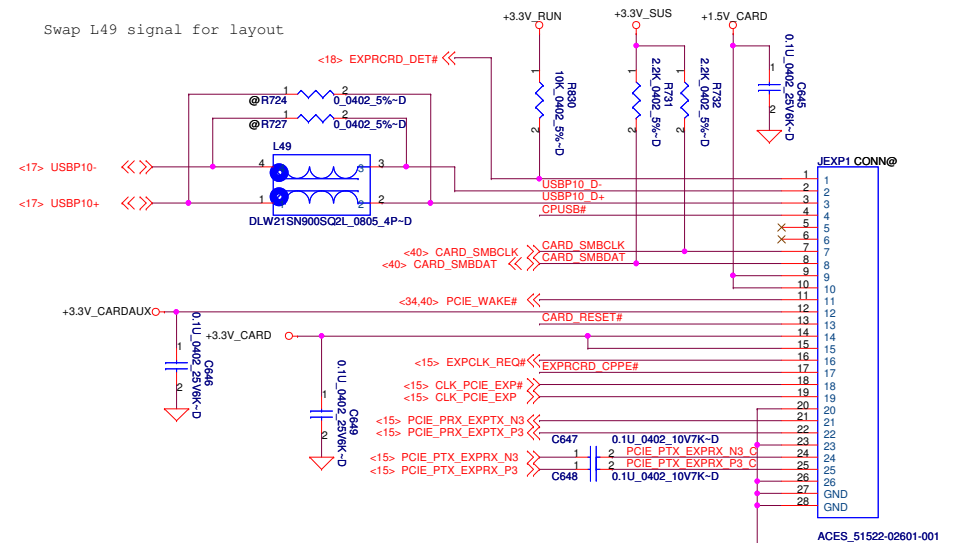


Express Card PWR S/W



Note: Add connection on pin4, pin5, pin13 and pin14 to support GMT 2nd source part

Express Card Conn.



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PCIE-SATA SW / PCIE PWR

LA-7731P

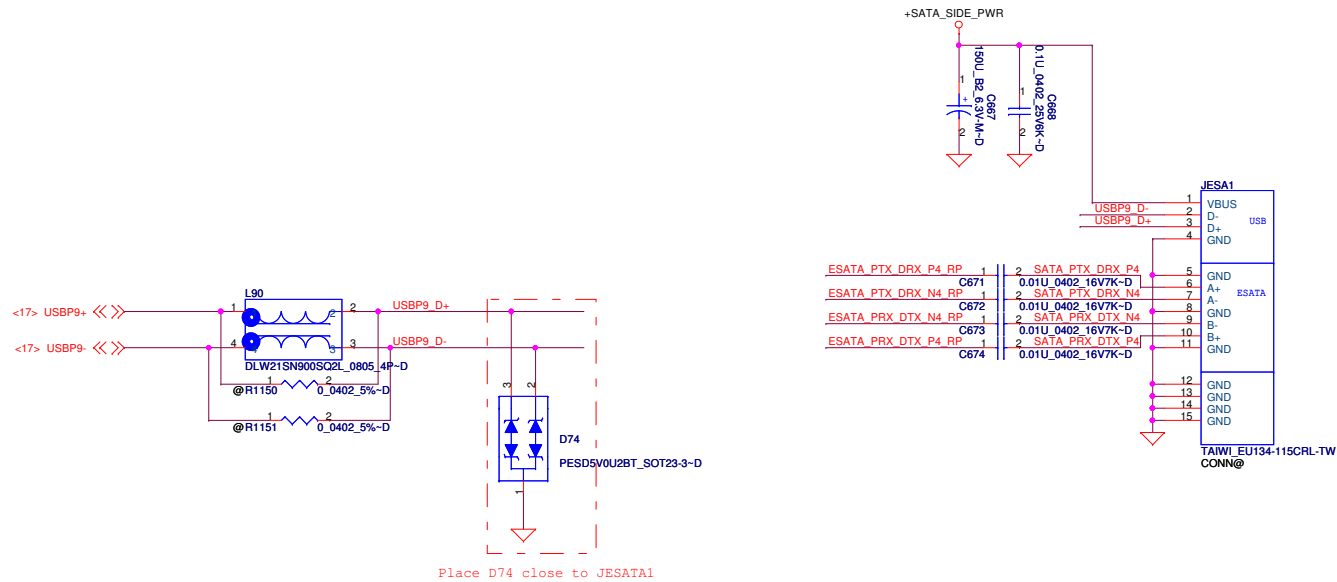
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8@ U44

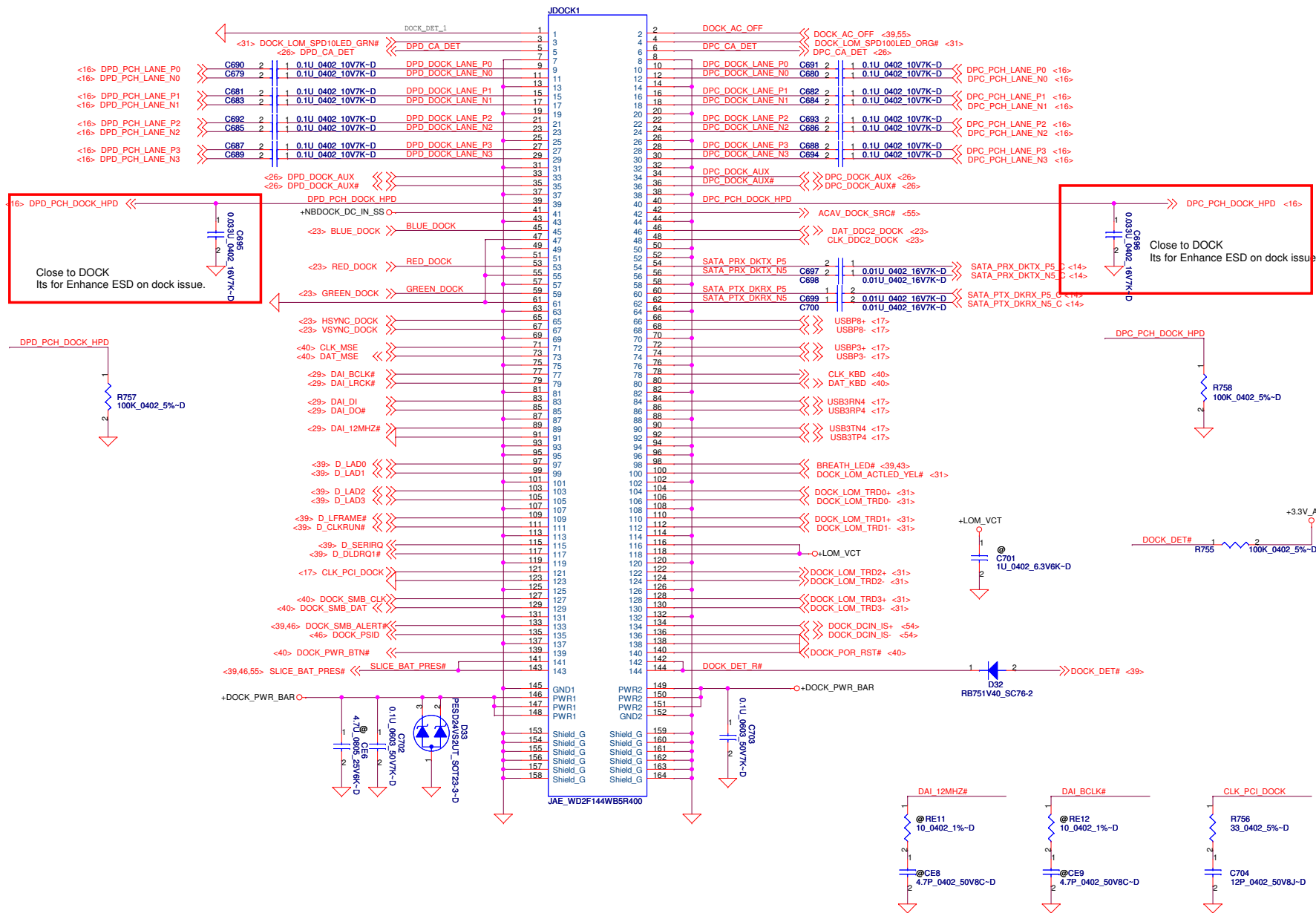
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SA00004WR00



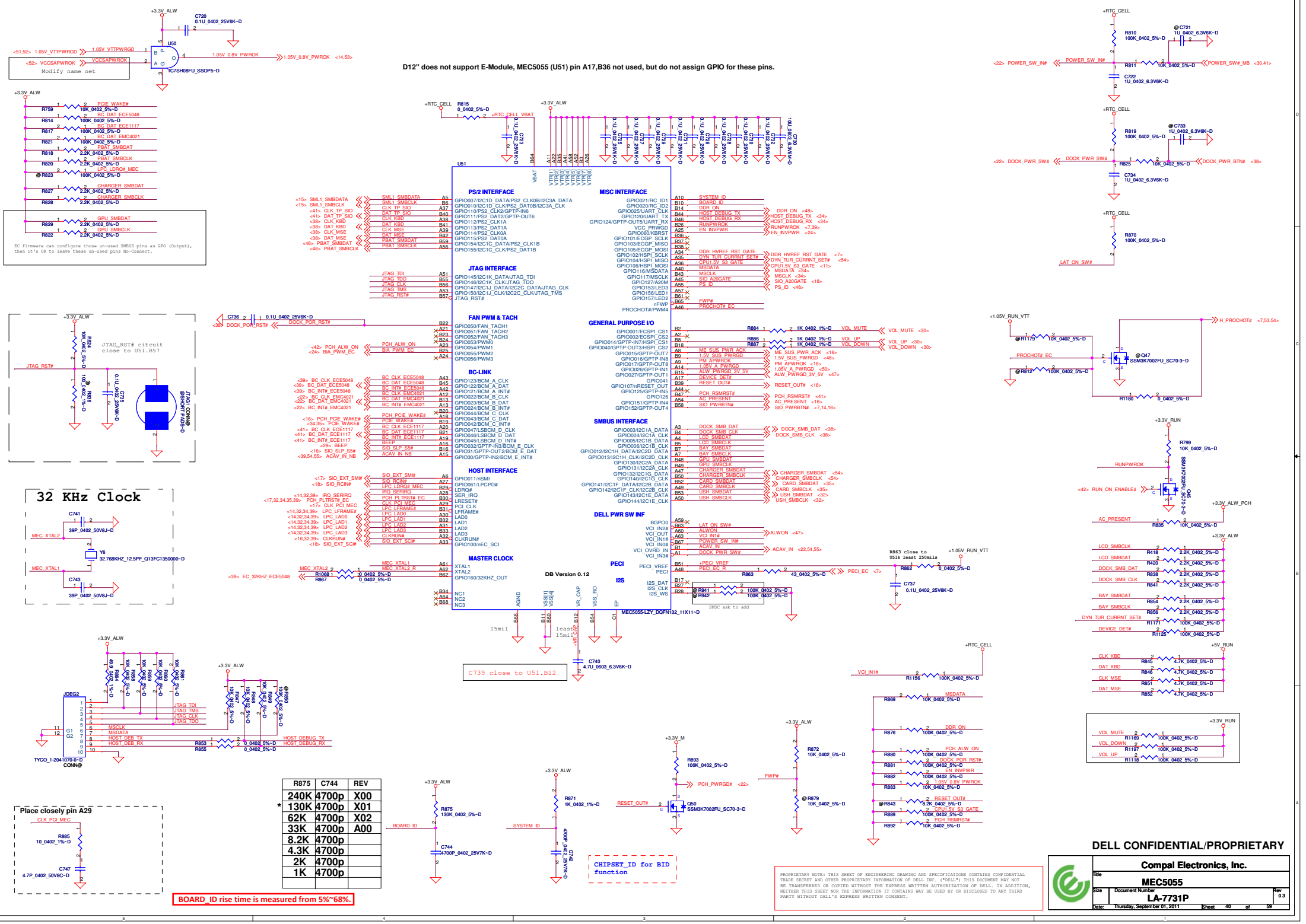
Title			
USB/ESATA/IO/MDC			
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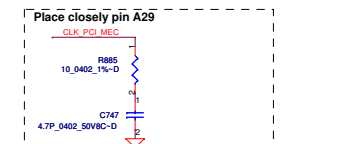
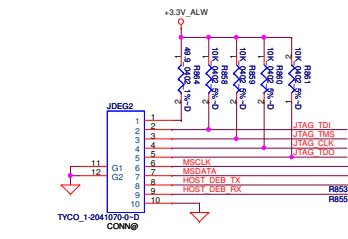
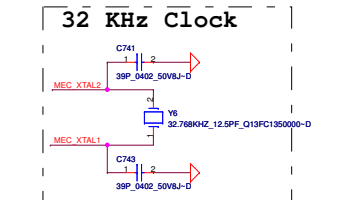
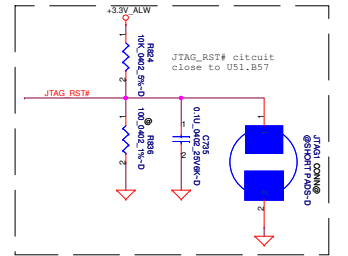
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D12" does not support E-Module, MEC5055 (U51) pin A17,B36 not used, but do not assign GPIO for these pins.

EC firmware can configure these un-used SMBus pins as GPIO (Output), then it's OK to leave these un-used pins No-Connect.



R875	C744	REV
240K	4700p	X00
130K	4700p	X01
63K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

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File
MEC5055

Size
LA-7731P

Date
Thursday, September 01, 2011

Rev
0.3

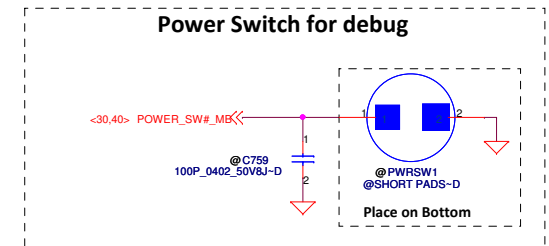
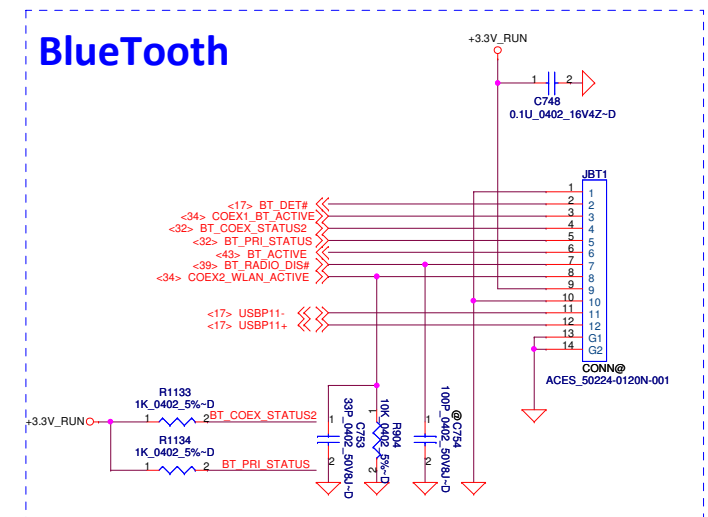
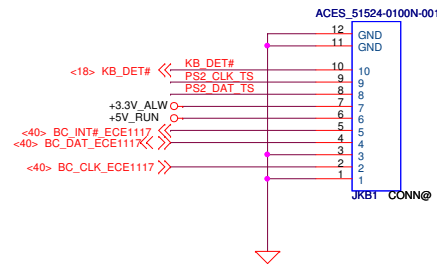
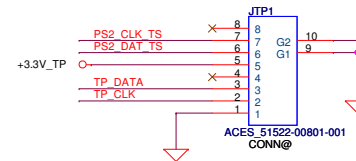
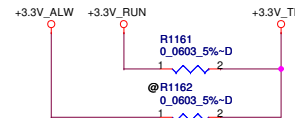
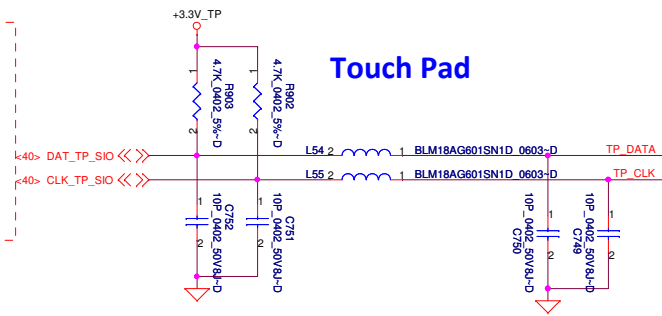
Sheet
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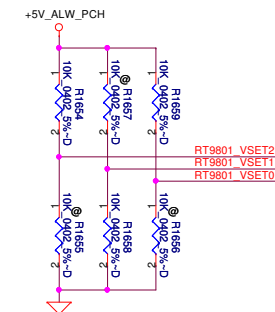
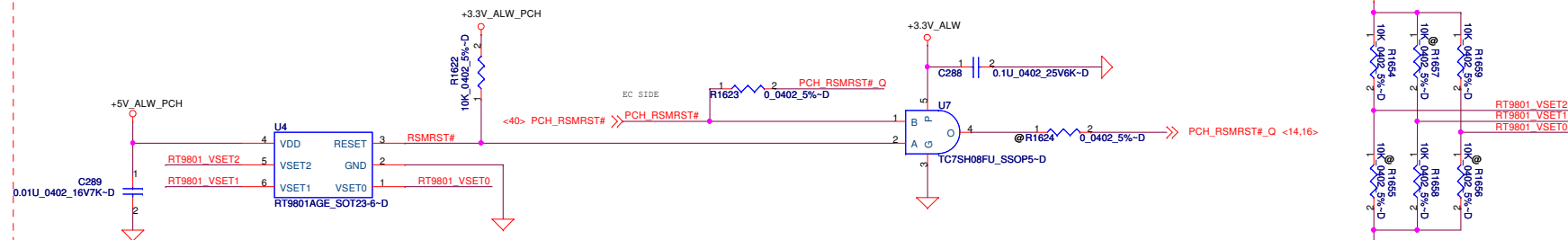
Place close to JTP1

D37 ESD ask to change to SOT23-3

Place close to JKB1



RSMRST circuit



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Title	Touch PAD/Int KB/BT
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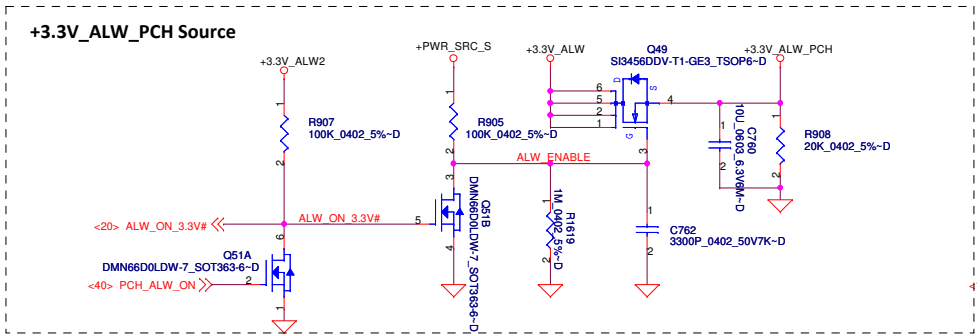
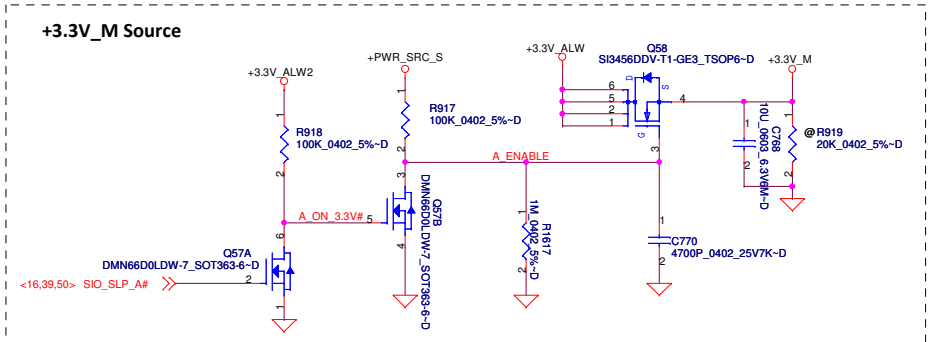
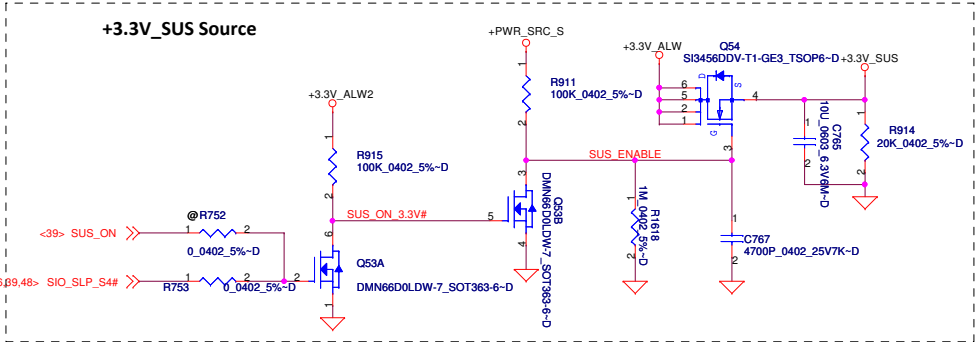
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+3.3V_ALW_PCH Source

The schematic diagram illustrates the +3.3V_ALW_PCH Source circuit. It features a power source PWR_SRC_S connected to a network of resistors (R907, R905, R1619, R908), capacitors (C762, C760), and MOSFETs (Q51A, Q49). The output is labeled +3.3V_ALW_PCH. A red line labeled 'ALW ENABLE' connects the gate of Q49 to the gate of Q51A. The circuit is labeled '+3.3V_ALW_PCH Source'.

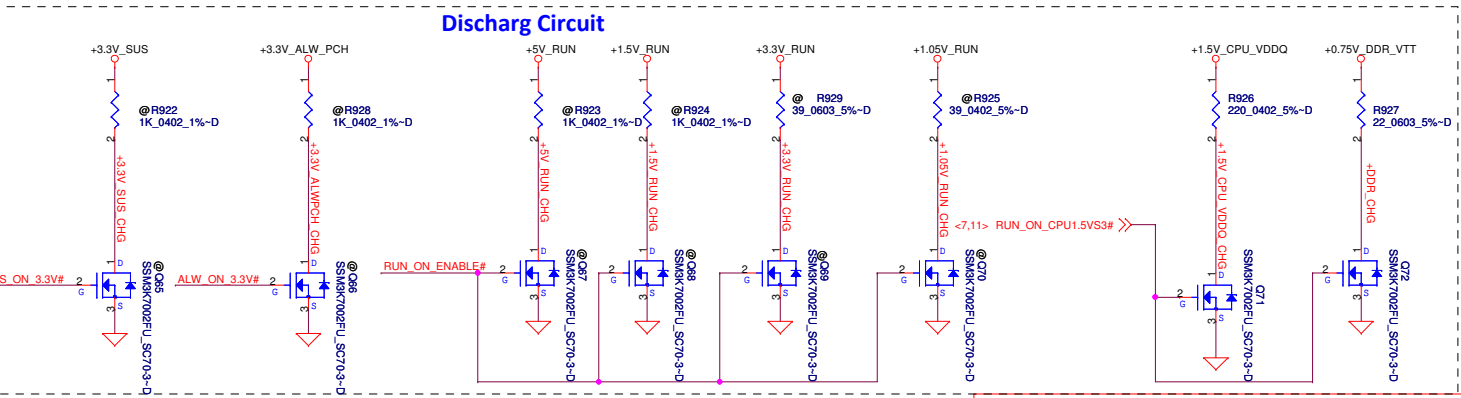
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Discharge Circuit

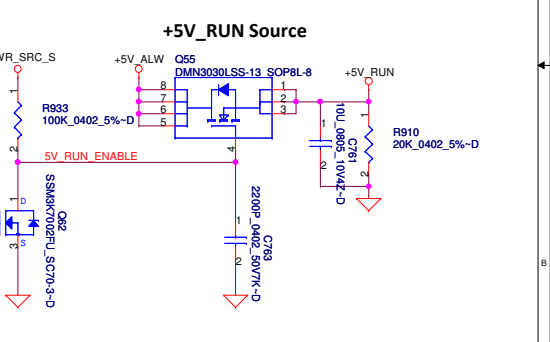
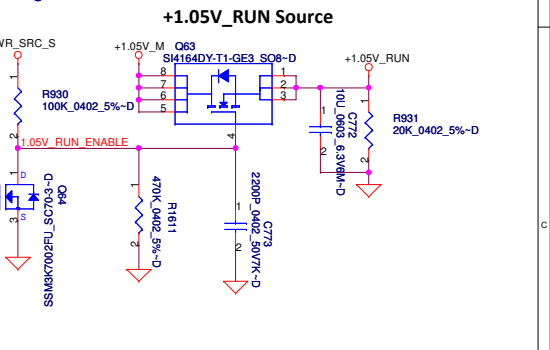
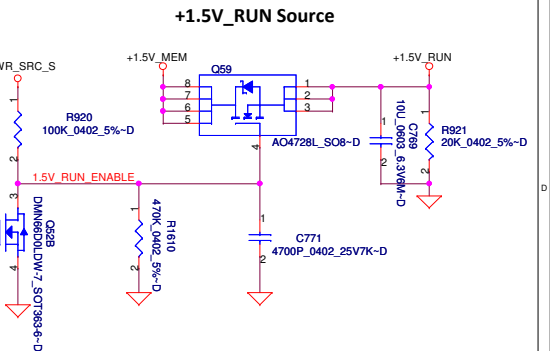
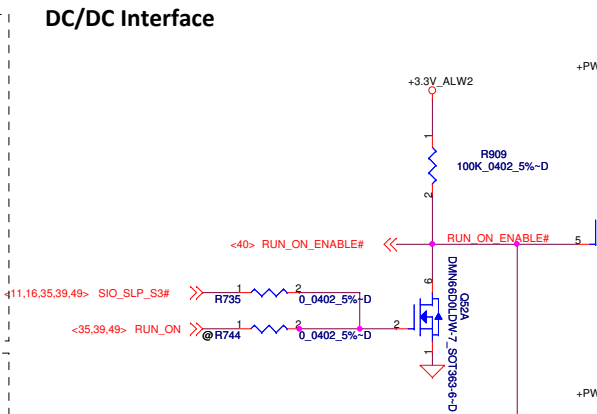
The diagram illustrates the discharge circuit for various power rails. Each rail is connected to a discharge resistor (R) and a MOSFET (M) controlled by the RUN_ON_ENABLE# signal. The components and their values are as follows:

- +3.3V_SUS:** Resistor R922 (1K_0402_1%-D), MOSFET Q65 (SS18K702F-U, SC70-3-D).
- +3.3V_ALW_PCH:** Resistor R928 (1K_0402_1%-D), MOSFET Q66 (SS18K702F-U, SC70-3-D).
- +5V_RUN:** Resistor R923 (1K_0402_1%-D), MOSFET Q67 (SS18K702F-U, SC70-3-D).
- +1.5V_RUN:** Resistor R924 (1K_0402_1%-D), MOSFET Q68 (SS18K702F-U, SC70-3-D).
- +3.3V_RUN:** Resistor R929 (39_0603_5%-D), MOSFET Q69 (SS18K702F-U, SC70-3-D).
- +1.05V_RUN:** Resistor R925 (39_0402_5%-D), MOSFET Q70 (SS18K702F-U, SC70-3-D).
- +1.5V_CPU_VDDQ:** Resistor R926 (220_0402_5%-D), MOSFET Q71 (SS18K702F-U, SC70-3-D).
- +0.75V_DDR_VTT:** Resistor R927 (22_0603_5%-D), MOSFET Q72 (SS18K702F-U, SC70-3-D).

The MOSFETs are controlled by the RUN_ON_ENABLE# signal, which is connected to the gate of each MOSFET. The source of each MOSFET is connected to ground, and the drain is connected to the power rail. The discharge resistors are connected between the power rail and the drain of the MOSFET.



The schematic diagram illustrates the DC/DC interface for the ADXL345. The ADXL345 component is shown with its pins connected to the system power and I2C bus. The VDD pin is connected to a +3.3V supply through a 100k pull-up resistor (R909). The GND pin is connected to the system ground. The SDA pin is connected to the I2C bus through a 100k pull-up resistor (R735). The ADXL345 is represented by a blue component symbol labeled 'ADXL345'.



+3.3V_RUN Source

VR_SRC_S

+3.3V_ALW

R940
100K_0402_5%-D

3.3V_RUN_ENABLE

Q61
DMN3030LS-13 SOP8L-8

+3.3V_RUN

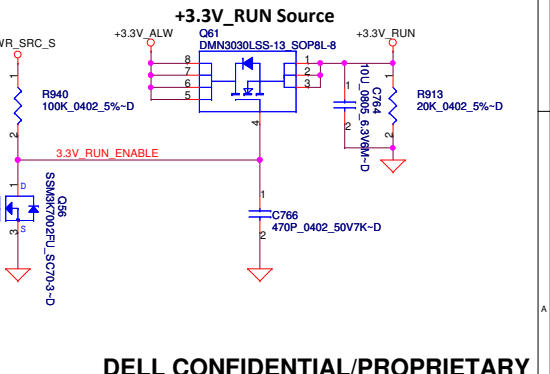
R913
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C764
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Q56
SSM3K702FU-SC70-5-D

C766
470P_0402_50V7K-D

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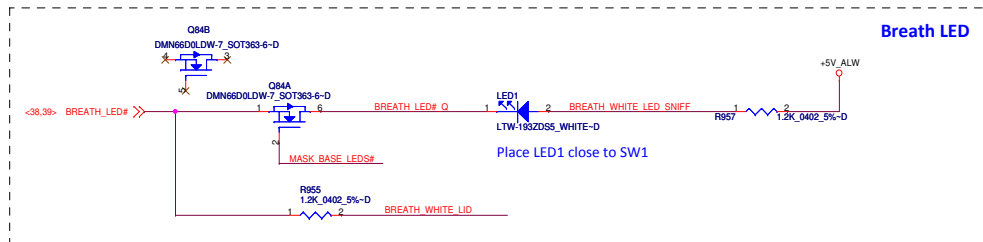
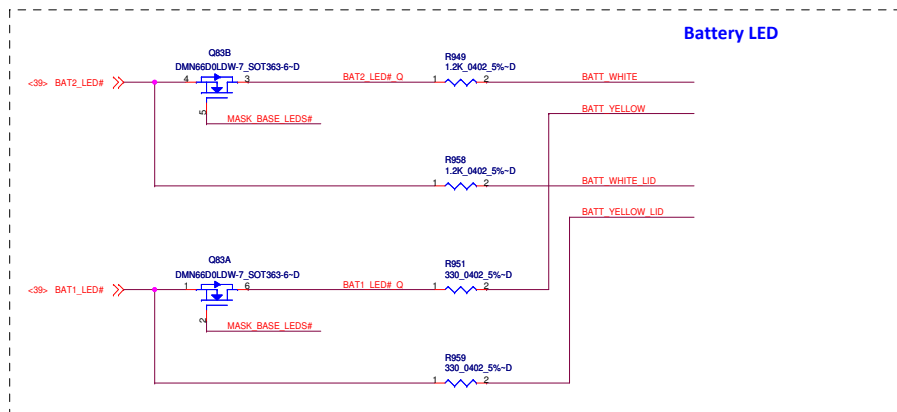
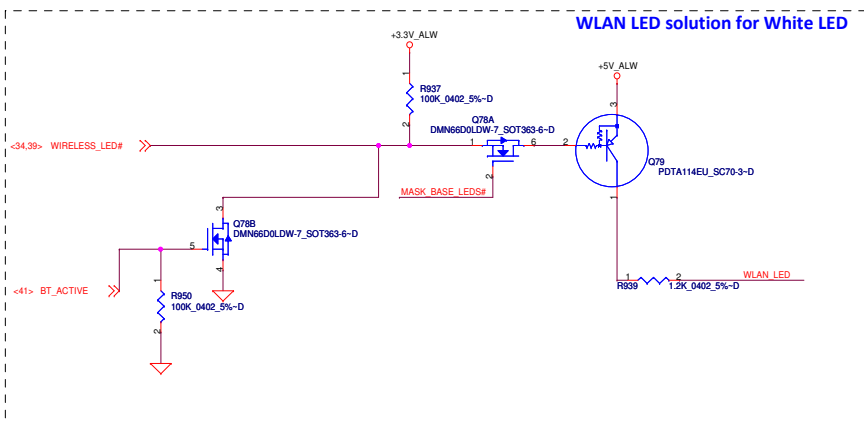
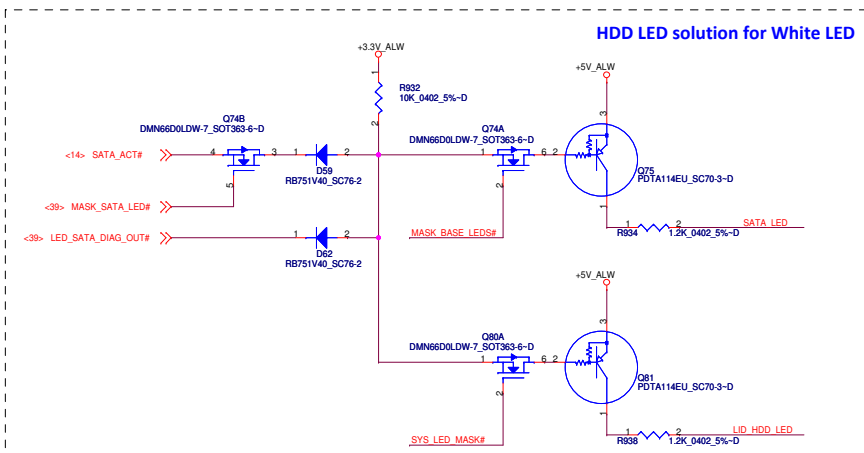
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Title **POWER CONTROL**

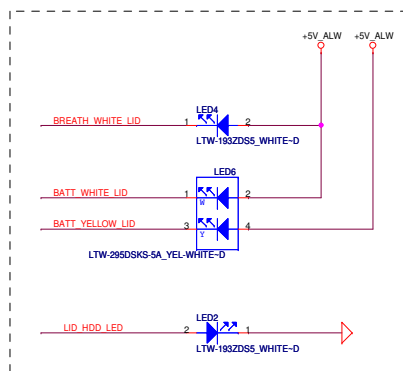
Size	Document Number	Rev
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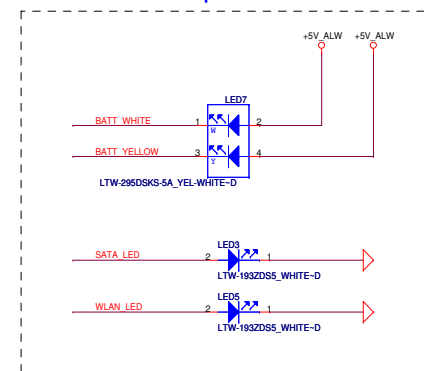
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Status LED when LID Close



Status LED when LID Open

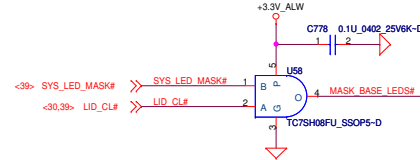
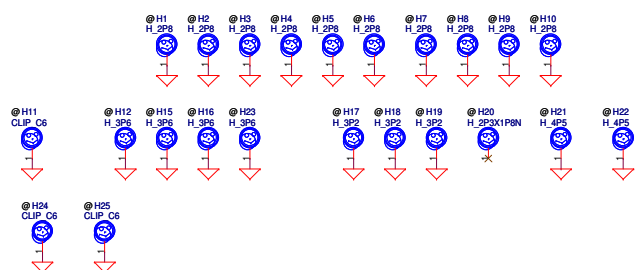


LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

- FD1
- FIDUCIAL MARK-D
- FD2
- FIDUCIAL MARK-D
- FD3
- FIDUCIAL MARK-D
- FD4
- FIDUCIAL MARK-D



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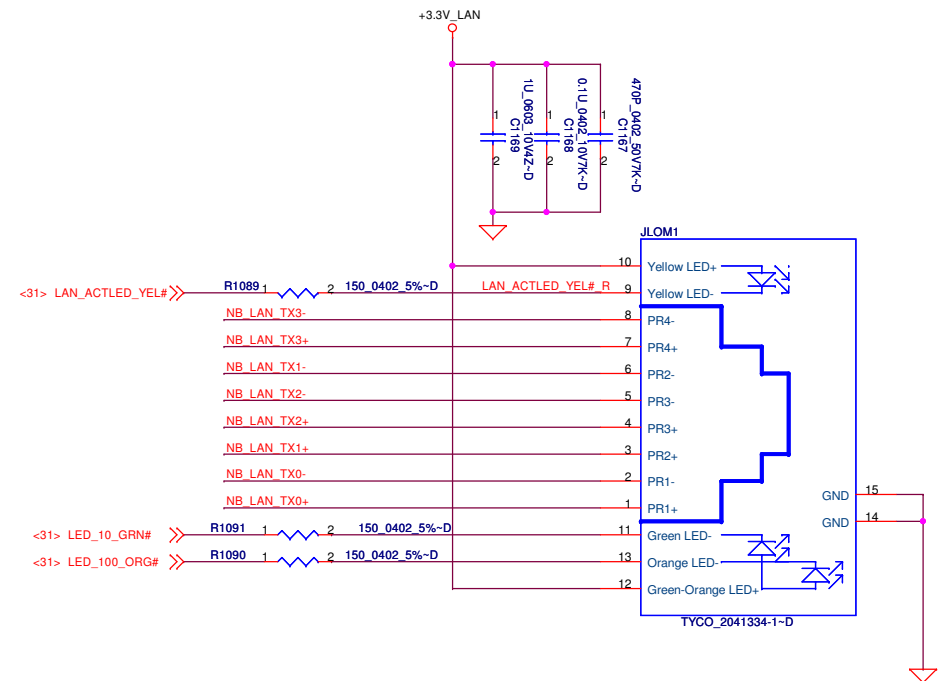
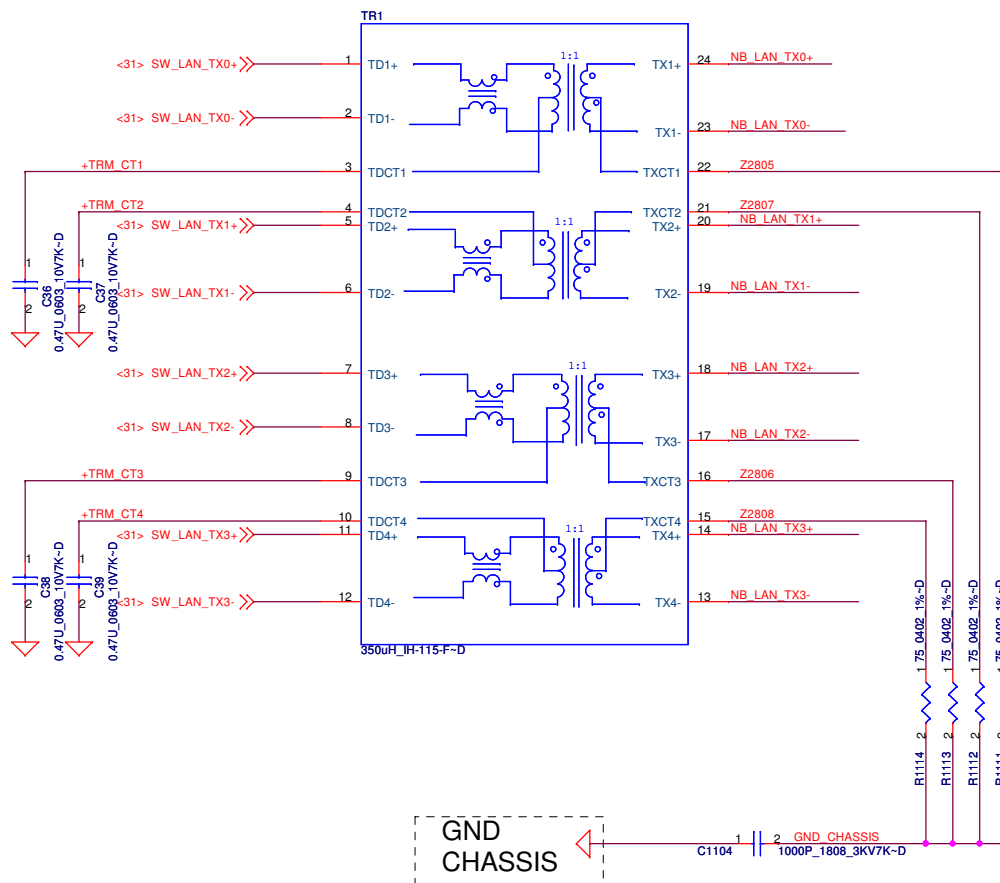
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PAD and Standoff

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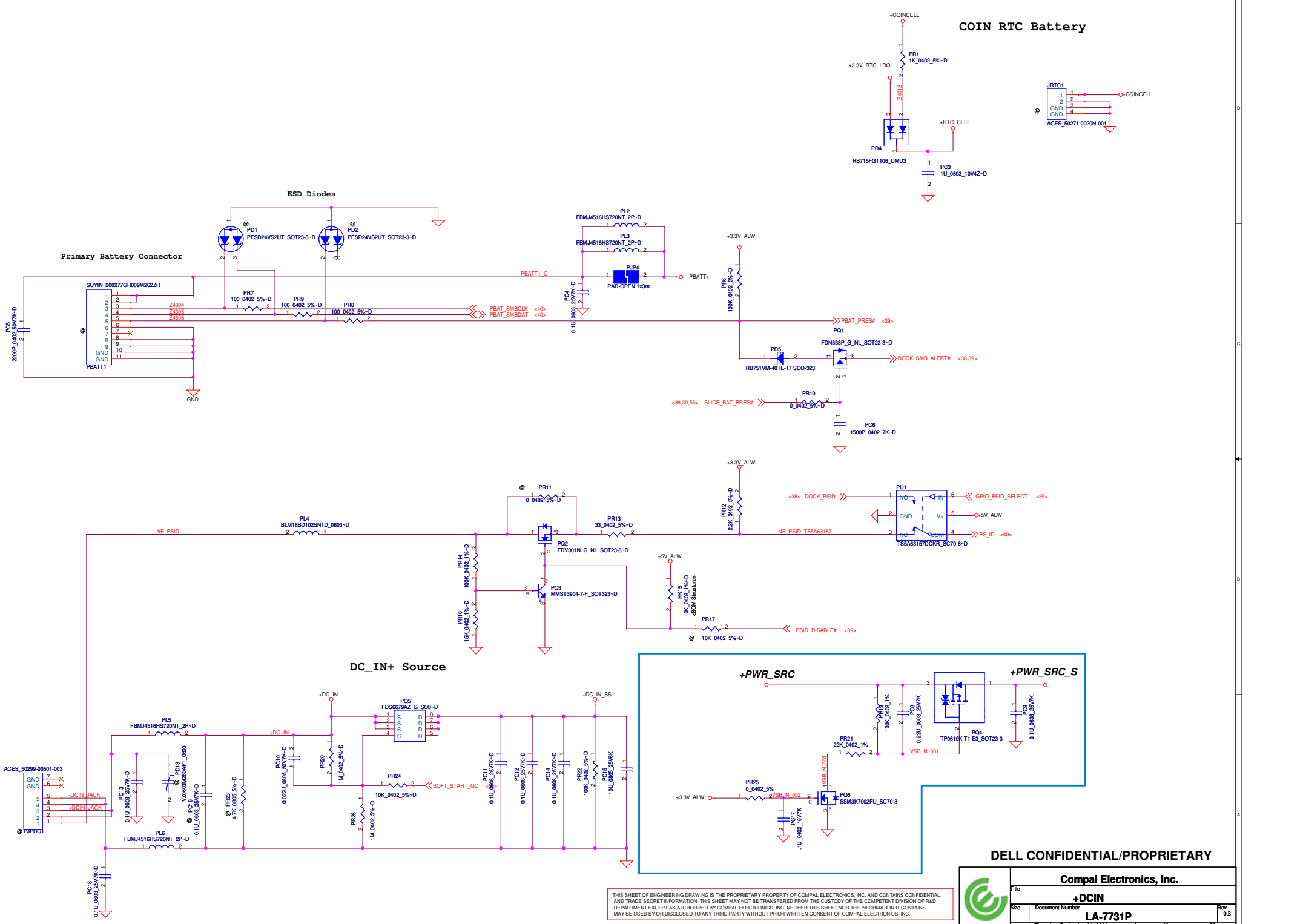
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Rev 0.3

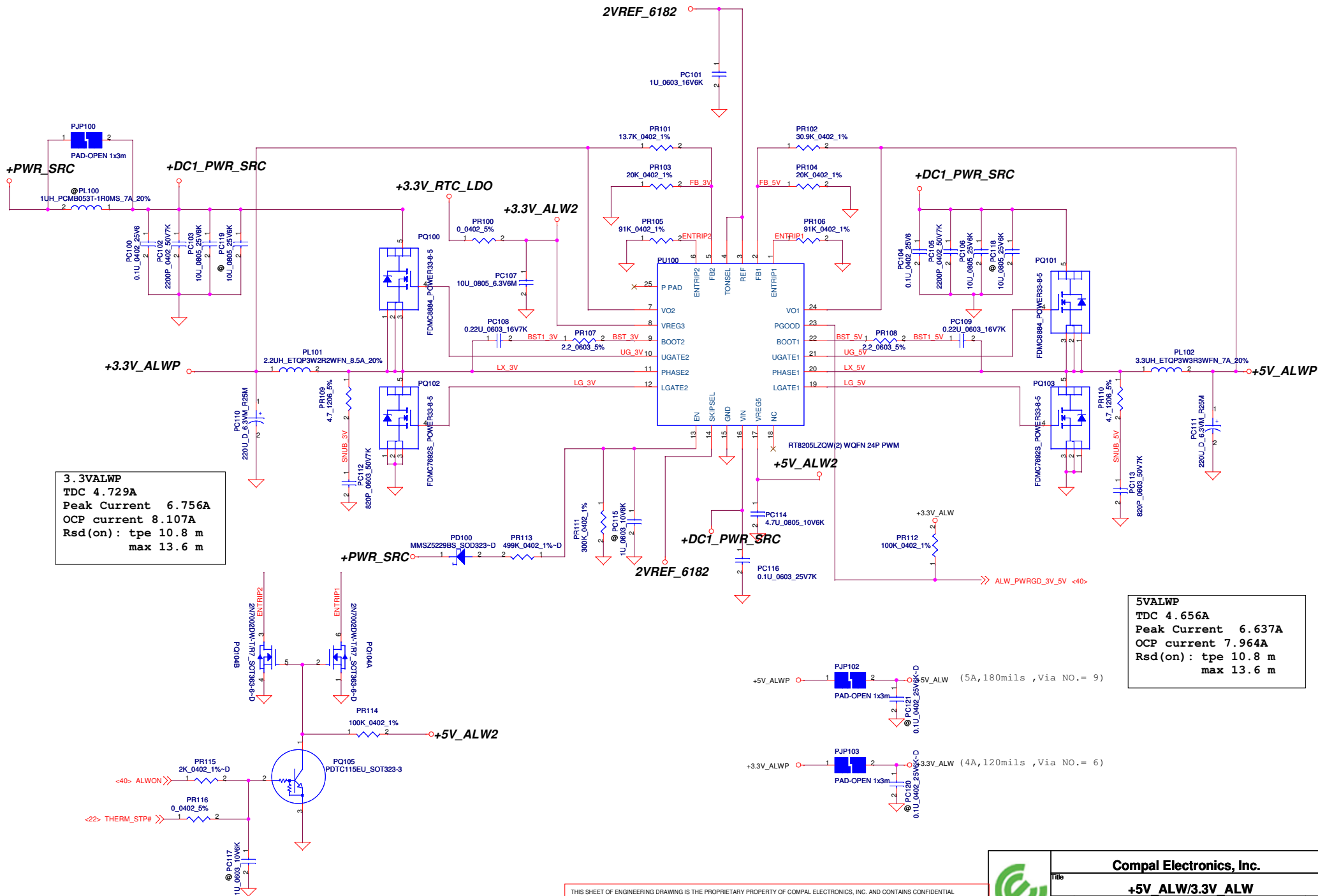


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+PWR_SRC

PJP200
@ PAD-OPEN 4x4m

1.5Volt +/- 5%
TDC 7.14A
Peak Current 10.2A
OCP current 12.24A
Rsd(on): tpe 3.6 m
max 4.5 m

0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A

+1.5V_MEN_P

PL200
1UH_ETQP3W1R0WFN_11.8A_20%
PC208
330U_SX_2VY-D
PC209
4.7_1206_5%
0.1U_0603_25V7K-D

Mode	Level	+0.75V_P	+V_DDR_REF
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

+1.5V_MEN_P

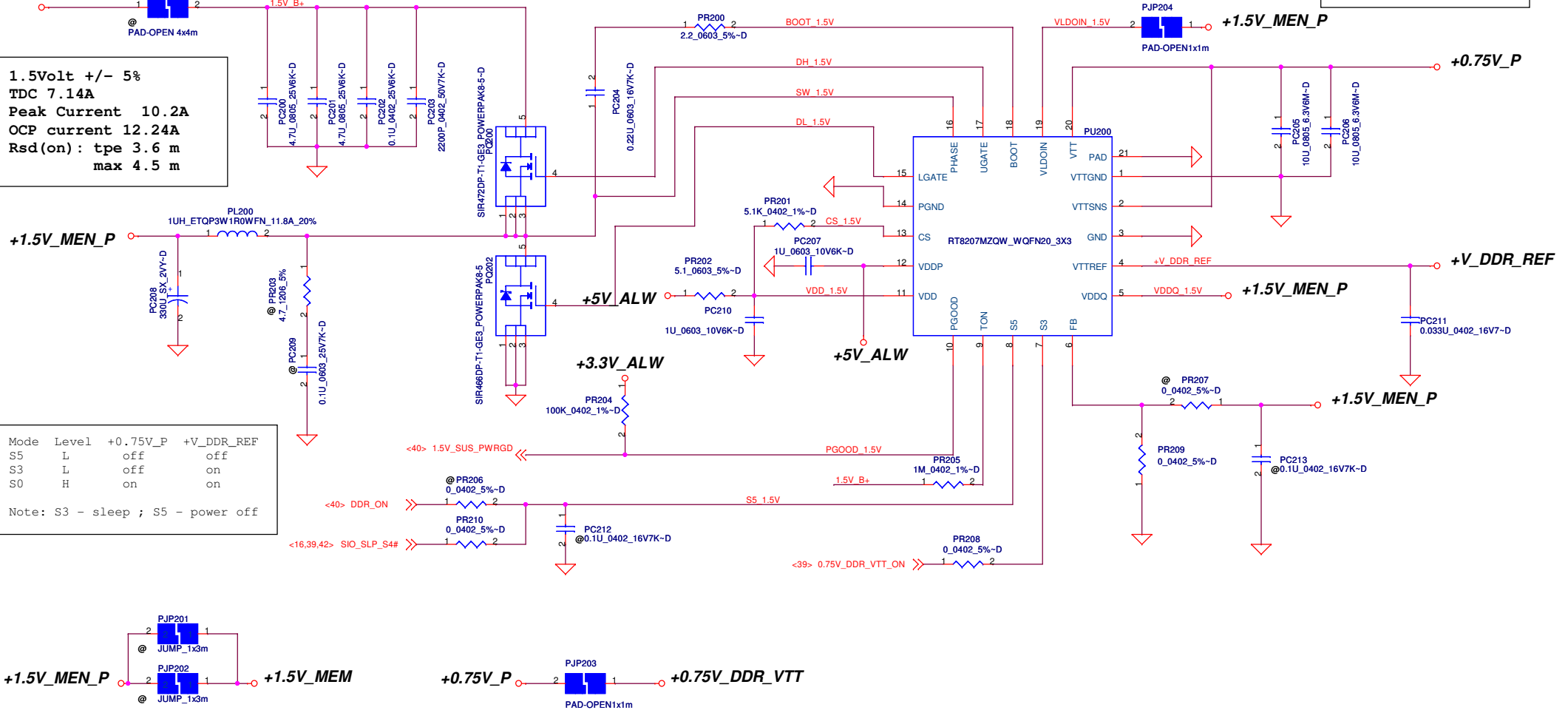
PJP201
@ JUMP_1x3m
PJP202
@ JUMP_1x3m

+1.5V_MEM

+0.75V_P

PJP203
@ PAD-OPEN1x1m

+0.75V_DDR_VTT



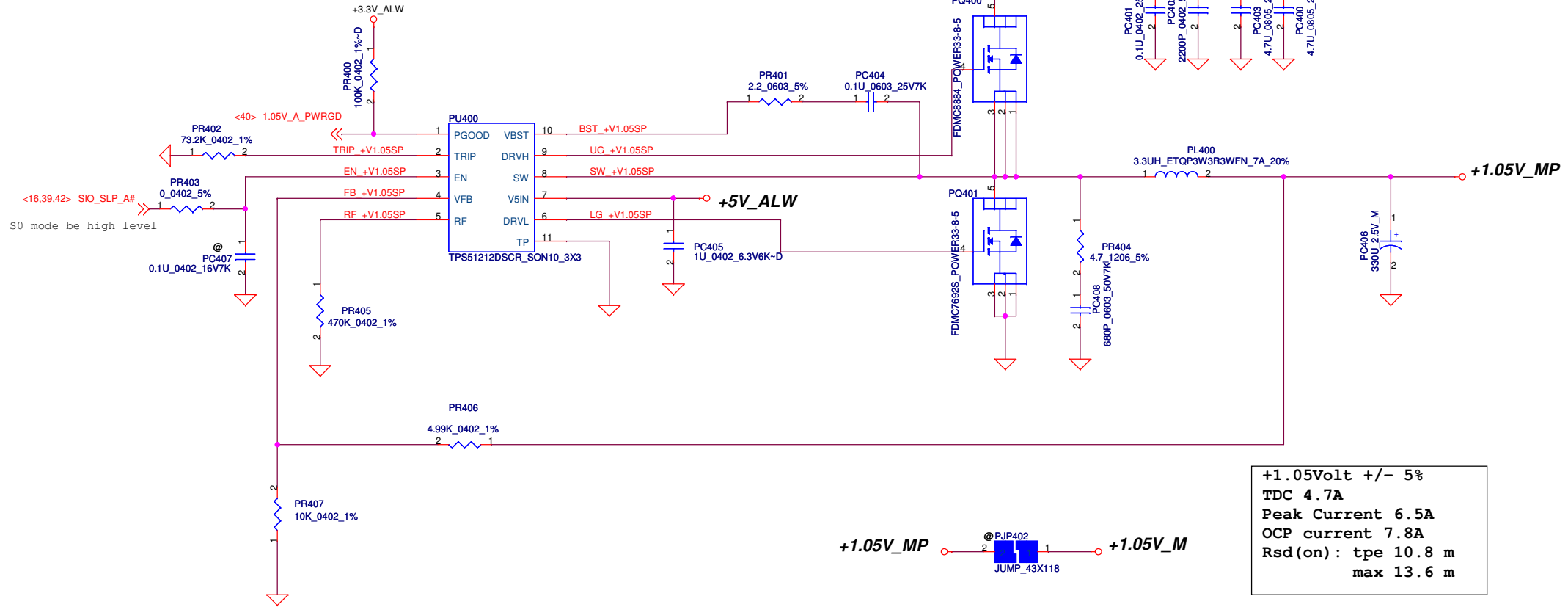
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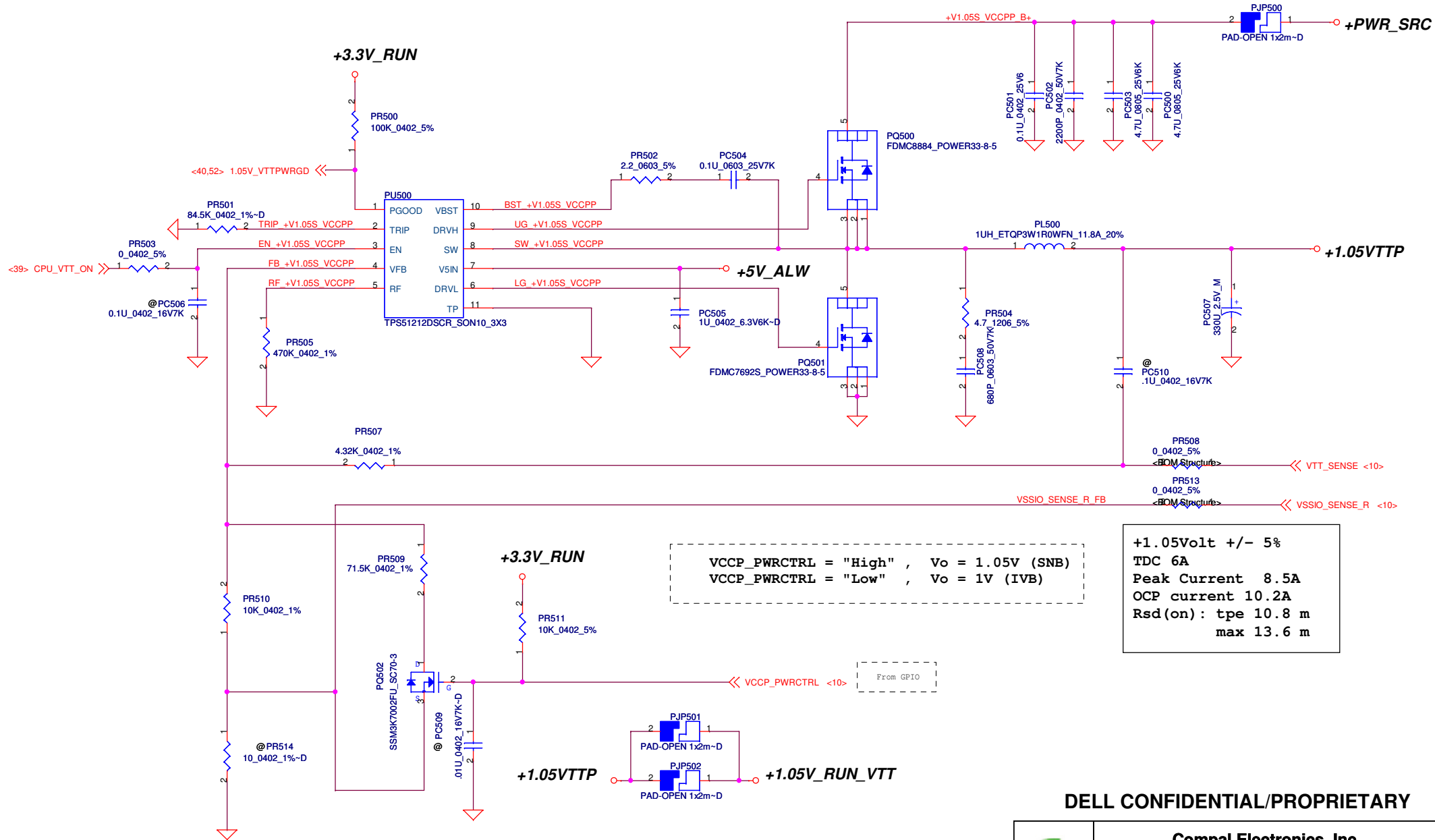
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+1.05V_M			
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+1.05V_RUN_VTT		
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+3.3V_ALW

GND_VCCSA

+5V_ALW

+3.3V_RUN

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A

+VCCSA_P

GND_VCCSA

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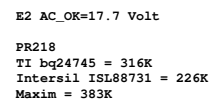


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+VCC SA		
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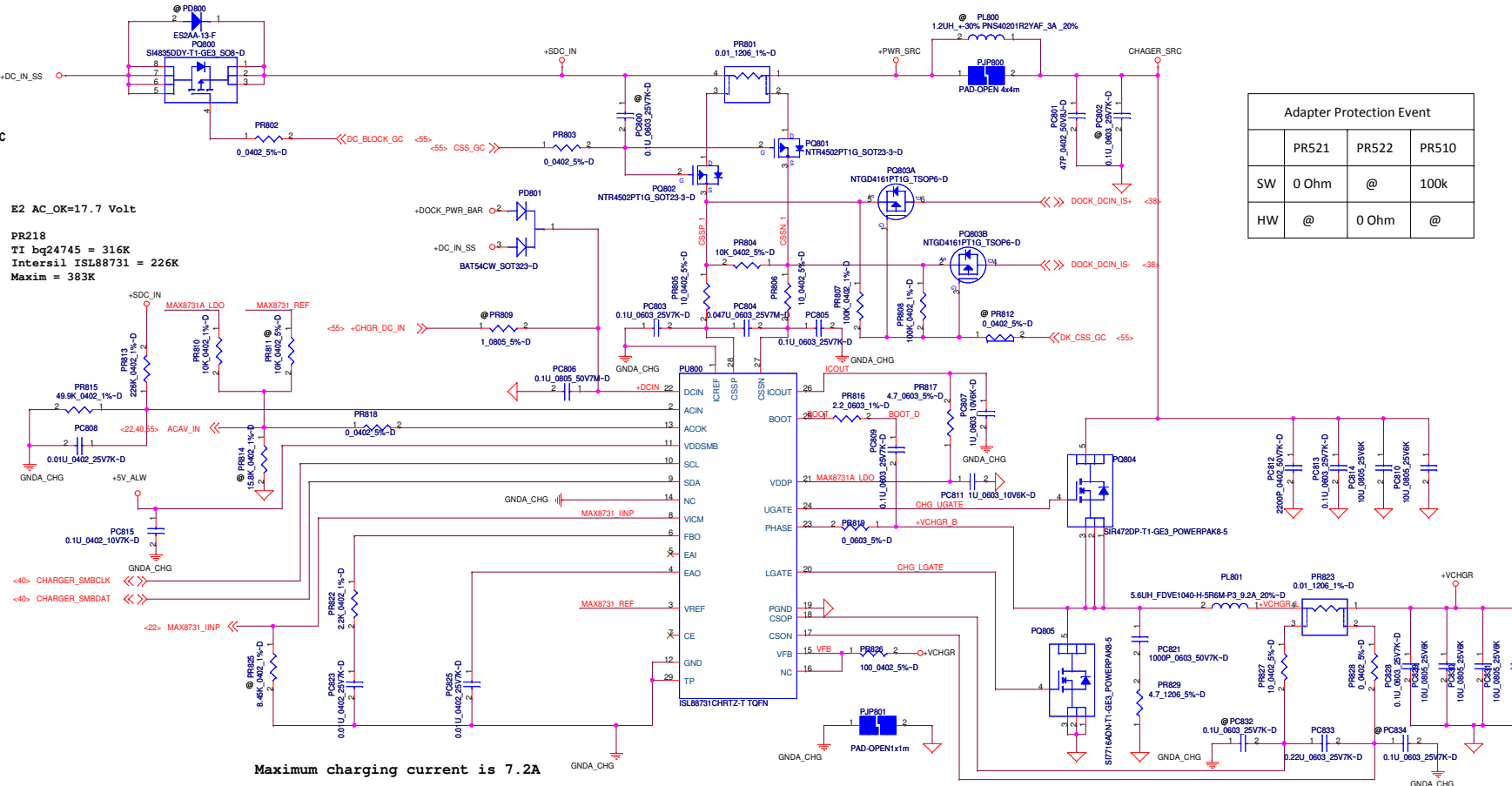
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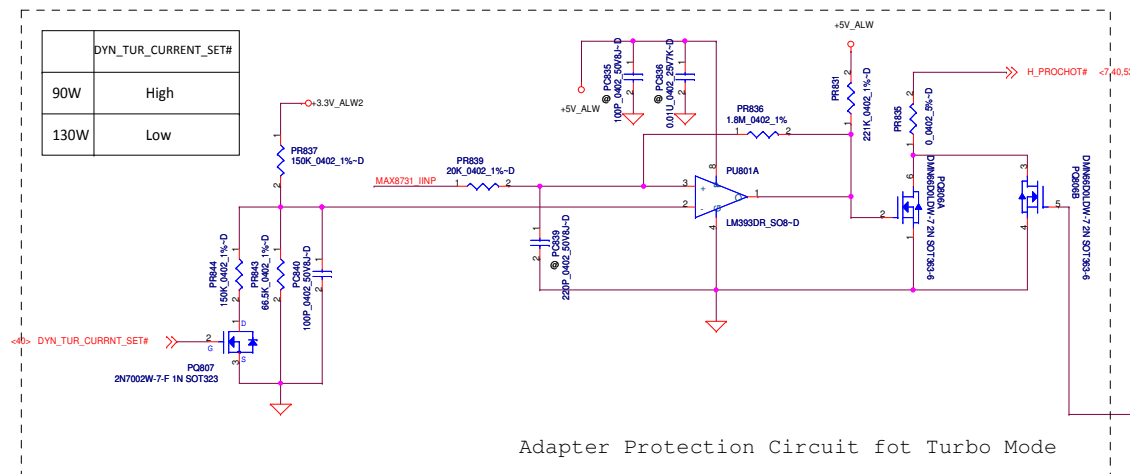


Adapter Protection Event			
	PR521	PR522	PR510
SW	0 Ohm	@	100k
HW	@	0 Ohm	@

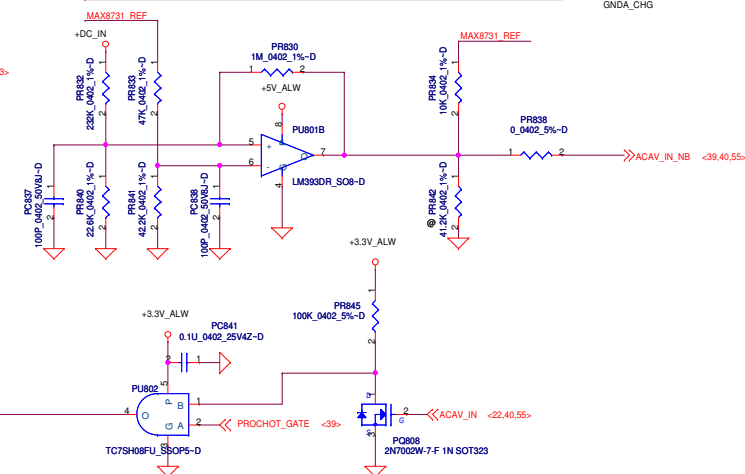


Maximum charging current is 7.2A

	DYN_TUR_CURRENT_SET#
90W	High
130W	Low



Adapter Protection Circuit fot Turbo Mode



To preset system to throttle
switching from AC to DC

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Charger

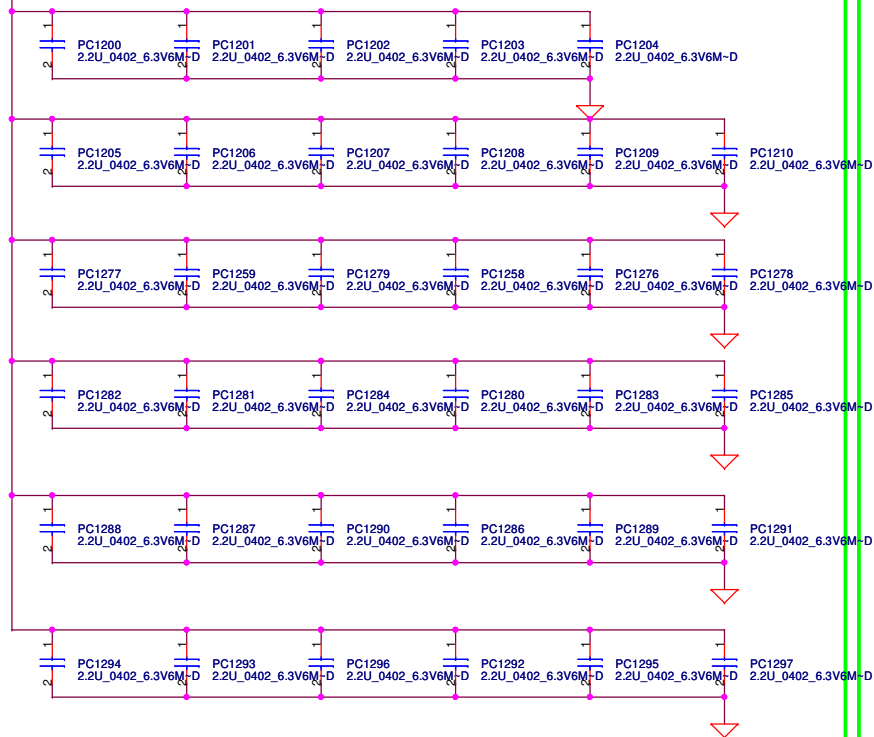
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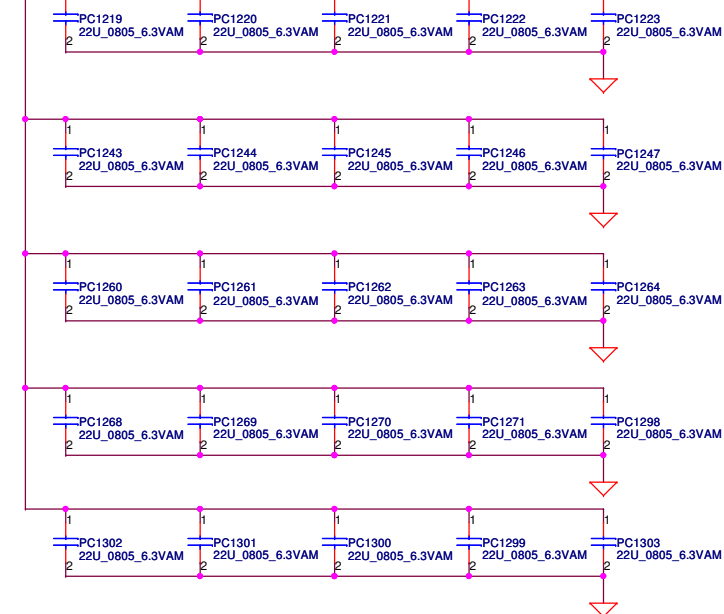
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+VCC_CORE



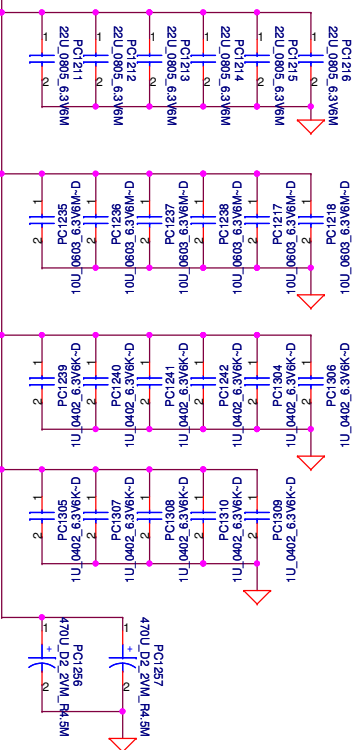
+VCC_CORE



+VCC_CORE

+VCC_GFXCORE

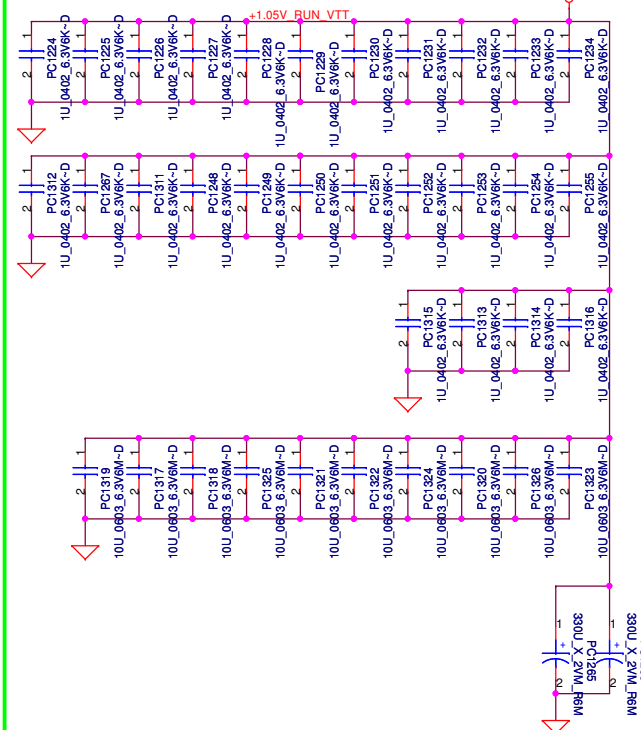
+VCC_GFXCORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

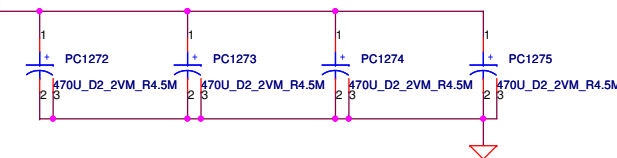
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05V_RUN_VTT



+VCC_CORE

+VCC_CORE



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	48	+1.5V_MEN	8/16	Dell	Follow VC , enable use SIO_SLP_S4#.	Add PR210 for net "SIO_SLP_S4#"	X01
2	46	DCIN	8/16	Dell	ME design change.	PJPDC1 change from 7pin to 5pin	X01
3	47	+5V/3.3V	8/16	Dell	Main and 2nd IC common setting.	De-pop PD100,PR113,PR111	X01
4	53	Vcore/GFX core	8/16	Compal RF_team	Suppress WWAN BB noise.	Pop PC751,PR760,PC725,PR731, PC745,PR751(680pF 0603, 4.7 ohm 1206)	X01
5	50 51	+1.05VM/ +1.05VTT	8/16	Compal	COS concern, change from D2 Polymer cap to OScon cap	PC406, PC507	X01
6	53	Vcore/GFX core	8/16	Compal	Prevent output voltage glitch when power up.	PU700 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
7	47, 53 , 54	Vcore, Charger +5V/3.3V	8/16	Compal RF_team	EMI solution.	Pop PL700.PL1300,PL100	X01
8	53	Vcore/GFX core	8/16	Compal	adjust OCP and DC load line.	PR740 change to 2.1k ohm, PR750 change to 392 ohm.	X01
9							X01
10							X01
11							X01
12							X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39, 40, 42	HW	7/14/2011	DELL	E4 uses SIO_SLP_S4# for power control	Add @R752, R753	X01
2	11	HW	7/14/2011	Compal	Change DDR channel A signal to DSL	Add CC149, CC152, CC178, CC179	X01
3	18	HW	7/26/2011	DELL	Follow GPIO map rev1.0	Change RH273 from 1k to 10k	X01
4	29	HW	7/26/2011	Compal	EMI request	Pop CE981, CE982, CE983	X01
5	35	HW	7/26/2011	Compal	Solve Express card PAID issue	Add R830	X01
6	7, 22	HW	7/27/2011	Compal	Solve ESD issue	Reserve D84, D85	X01
7	25	HW	7/27/2011	Compal	Layout routing	Swap HDMI trace connection on L19, L20, L21, L22 for layout routing	X01
8	29	HW	7/28/2011	Compal	EMI request	Add CE984, CE985	X01
9	7	HW	8/1/2011	Compal	EMI request	Reserve CC141	X01
10	17	HW	8/3/2011	Intel	Request from Intel review feedback	Pop RH332	X01
11	14, 39	HW	8/4/2011	SMSC	SMSC request to delete LPC_LDRQ0#	Leave LDRQ0# no connection on both of 5048 and PCH side	X01
12	20, 42	HW	8/4/2011	Compal	Vgs less than cut-in voltage in battery mode	Add QH6, RH279, CH107	X01
13	42	HW	8/4/2011	Compal	Load SW sources output rising time mismatch and COS. cost concern.	Change back to E3 +3.3V/5V RUN discrete solution. Add Q55, Q56, Q61, Q62, R933, R940, R1627, remove U78, R749, R747, C1199, C1198, C1197, C1196, change C761, C764 to 10uF	X01
14	10	HW	8/4/2011	Compal	Follow INTEL PDDG 0.8	De-pop RC140	X01
15	32	HW	8/4/2011	Compal	RESET_OUT# power sequence issue	Add R1653, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
16	40	HW	8/4/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
17	34	HW	8/4/2011	COMPAL	PCH GPIO52 need 8.2~10K pull up +3.3VS	Change R695 from 100K to 10Kohms	X01
18	23	HW	8/4/2011	COMPAL	CRT SW 2nd source TI, TS3V713 pin29 is VDD	Connect pin29 to +3.3V_RUN	X01
19	16	HW	8/4/2011	COMPAL	+1.05V_M turn off before APWROK de-assert	Add UH5 circuit for backup HW solution	X01
20	41	HW	8/4/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable)	X01
21	29	HW	8/4/2011	COMPAL	Co-lay 92HD93 with ALC290	Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642 Reserve for ALC290 only: C1204, C1205, R171, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963	X01
22	29	HW	8/4/2011	COMPAL	Codec is change to 92HD93	Pop R162~R166 and de-pop U73	X01
23	40	HW	8/8/2011	COMPAL	Please depop VOL MUTE/UP/DOWN due to EC code enable internal PU resistors (3V_ALW)	De-pop R1169, R1197, R1118	X01
24	41	HW	8/8/2011	COMPAL	For debug purpose	Add R1624	X01
25	42	HW	8/8/2011	COMPAL	power suggestion	Change Q59 to A04728L	X01
26	43	HW	8/9/2011	COMPAL	Align with E4	Change LED6, LED7 power source from +3.3V_ALW to +5V_ALW	X01
27	14, 40	HW	8/10/2011	COMPAL	Crystal EA result	Change C741, C743 from 22p to 39p, CH2, CH3 from 15p to 18p, CH18, CH19 from 12p to 10p for crystal EA	X01
28	41	HW	08/11/2011	COMPAL	For RSMRST# debug	Reserve R1655 and pop R1623	X01
29	26	HW	08/11/2011	COMPAL	DPX_CA_DET voltage too low through dongle	Change U21 and U24 to SA000055G0L	X01
30	43	HW	08/11/2011	COMPAL	Tune white light LED brightness	Change R934, R938, R939, R949, R958, R957 and R955 to 2.2K ohm	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
31	20, 22, 34 38, 39, 43	HW	8/11/2011	COMPAL	Cost saving	Change D2, D31, D32, D34, D59, D62, DH2, DH3, D65, D66, D67, D68, D69, D70 to SCS00002G00	X01
32	11	HW	8/12/2011	COMPAL	Solve S3 wake up issue	Pop RC79 and de-pop RC82	X01
33	36, 41	HW	8/14/2011	ME	ME change connector	Change JUSB1, JUSB2, JBT1	X01
34	30	HW	8/16/2011	ME	ME change connector	Change JLID1	X01
35	17, 32 39, 40	HW	8/18/2011	COMPAL	RF request	Pop R885, C747, R795, C713, RE5 and change CE3 to 12pF and pop it, and add CH109, CH110	X01
36	36	HW	8/19/2011	COMPAL	Follow Intel design guide	Change C410~C413 from 0.01uF to 0.1uF	X01
37	25	HW	8/24/2011	COMPAL	EMI request to solve HDMI issue	Add C1216~C1223	X01
38	7	HW	8/25/2011	COMPAL	ESD request	Change RC25 to 1k and pop CC141	X01
39	40	HW	8/26/2011	SMSC	SMSC request	Reserve R941, R942	X01
40	24, 33	HW	8/26/2011	EMI	EMI request to solve SD/DMIC issue	Reserve CE758, CE279, CE280	X01
41	43	HW	8/27/2011	ME	Solve standoff shift issue	Change H11, H24, H25 to 6mm	X01
42	43	HW	8/29/2011	COMPAL	Tune white light LED brightness	Change R934, R938, R939, R949, R958, R957 and R955 to 1.2K ohm	X01
42	14	HW	8/29/2011	ME	change TAA connector	Change JTAA1	X01

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